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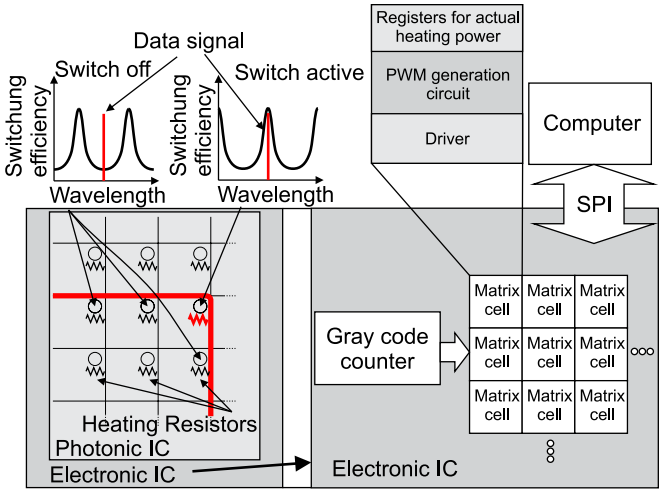

Photonic and electronic IC connected via inter wafer connects

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Integrated Pulsewidth Modulation Control for a Scalable Optical Switch Matrix

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Abstract: A scalable pulsewidth control approach with 7-bit resolution for thermal control of optical ring resonator switch matrices in 0.16-μm Bipolar-CMOS-DMOS (BCD) with a cell size of $79 * 105\ \mu m^2$ is introduced. One Gray counter at up to 1.2-GHz clock and pulsewidth modulation generation in each matrix cell leads to an electrical power consumption of 330 mW for all electronic control circuits of an optical 1000-switch-node matrix, resulting in a reduction of 11.1% of the power needed by a constant-voltage control approach.

Index Terms: Microring resonators, electronics-photonics integration, low power consumption, control.

1. Introduction

Worldwide network traffic and consumers' hunger for more bandwidth are increasing rapidly. To satisfy network operators' needs new technologies have to be developed. Cheap, reliable, and easily scalable integrated optical switches will be one of the key technologies in this field [1]–[11]. One very promising approach is utilizing microring resonators as optical switching elements [1]–[3]. If the resonance of a microring (MR) is matched with the wavelength of an optical signal passing the MR, then this signal will be switched. To use an MR as active switching element the resonance of the MR has to be controlled. One way to do so is to change the MR's temperature [2], [5] by controlling the dissipated power of a heating resistor placed closely to the MR. This heating power can be used, not only to set the actual state of the MR but to fine-tune the resonance to compensate for production tolerances as well. Fig. 1 shows a block diagram for such an electrically controlled MR switch matrix.

2. Architecture of the System

So far, thermally controlled MRs were tuned by applying a constant heating power [2], [5]. In this paper, we present the first energy efficient scalable chip that is capable of controlling the heating power for MRs by using a pulse width modulation (PWM) approach. In our proof of concept, we present a 3×3 matrix capable of controlling nine MRs. However, this approach is easily scalable to control many more elements.

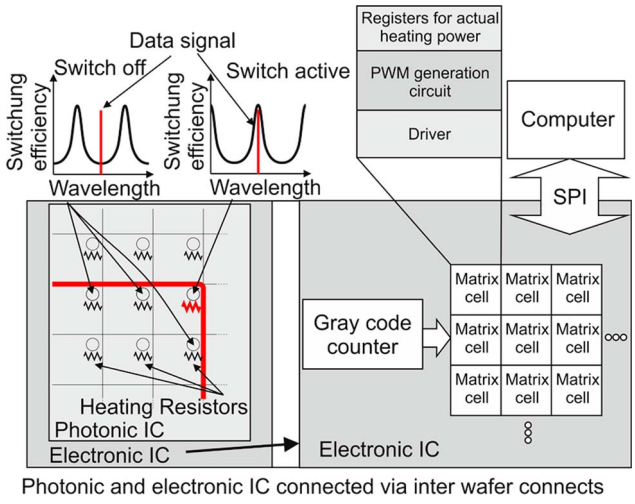

Fig. 1. Block diagram of an optical switch matrix including the electronic integrated circuit for controlling the heating power.

Only a low number of switches are on and many are off in typical applications of an optical switch matrix [3]–[11]. For the off switches, only a small amount of heating power is necessary to compensate for production tolerances and to keep them in their optimum off position by increasing the isolation of the off-path. In a constant voltage approach, for these off-switches, most of the voltage would be across the driver, and therefore, the power dissipated in the driver would be larger than the power dissipated in the corresponding heating resistor.

Assuming, for example, a supply voltage of 1.8 V and a voltage of 0.6 V across the heating resistor would lead to a voltage of 1.2 V across the driving transistor. In this case, the power dissipation of the driving transistor would be two times the power dissipation of the heating resistor itself. This gets even worse if the voltage across the heating resistor is further decreased.

Contrary to the situation in the constant voltage approach, in our presented PWM approach, the heating power for the MRs is regulated with the duty cycle of the output signal of the driver. This means that the driver is either on or off. If the driver is off, it does not have any power consumption at all (the leakage currents can be neglected). Only if it is on, the saturation voltage of the transistor leads to a small amount of dissipated power. However, the driver transistor is designed to have a saturation voltage of less than 5% of the supply voltage of 1.8 V. This means that the corresponding power consumption can be neglected and the only relevant power dissipation in the matrix cell is caused by the digital circuits for generation of the PWM signal.

Compared to driving the heating resistor with constant voltage or current, the PWM approach helps to keep the power dissipation of the control circuit low.

3. Implementation and Measurement Results

The chip was fabricated in 160 nm BCD8sP [12], [13]. The design was made with the complementary metal-oxide semiconductor (CMOS) part of this technology. The main parts of the chip are the Gray counter and the control matrix (see Fig. 1). Additionally, a serial peripheral interface (SPI) is included, which allows to set the heating power for all of the heating resistors by a micro controller or a computer.

The counter was designed according to the architecture depicted in Fig. 2 to guarantee that it is operating with clock frequencies of 1 GHz and even above. It is built out of seven parallel 128 bit shift registers. This implementation is neither small in area, nor the most energy efficient way to implement a counter, but it is very fast. Moreover, this counter architecture allows easily implementing a Gray code counter instead of a standard binary counter. Using a Gray counter is very important, since in this type of counter, only one bit is different in two successive values.

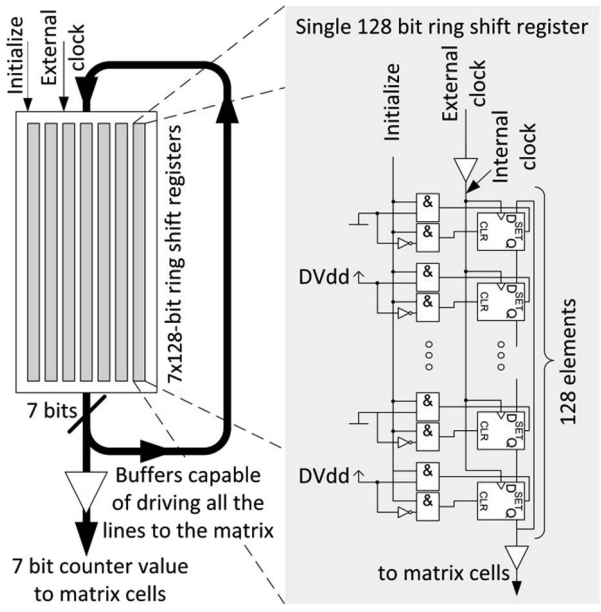

Fig. 2. Circuit diagram of Gray counter.

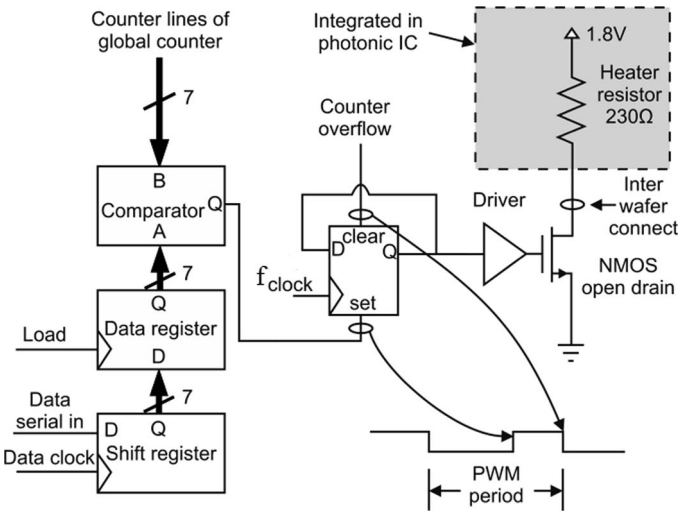

Fig. 3. Detailed circuit diagram of one matrix cell.

This allows us to do the PWM generation in each matrix cell in a very energy efficient and compact way, since it is not necessary to consider glitches, that could occur when two or more bits are changing between two successive counter values. There is a 7-bit bus from the counter to all matrix cells. The counter is implemented only once on the chip. Therefore, the power consumption of this counter can be neglected for large control matrices.

Each cell of the control matrix contains the driver circuits for the heating resistors, registers to store the actual heating power (PWM code) and a logic block for the generation of a PWM signal (see Fig. 3). Therefore, each cell consists of a 7-bit shift register to load new heating power settings, a 7-bit data register to store the actual heating power for each node, and the circuit block for the generation of the PWM signal. An asynchronous digital comparator is used to compare the counter value with the register value stored in each matrix cell. As soon as the counter value equals the stored value, the output of a flip-flop is set. This output is connected to the

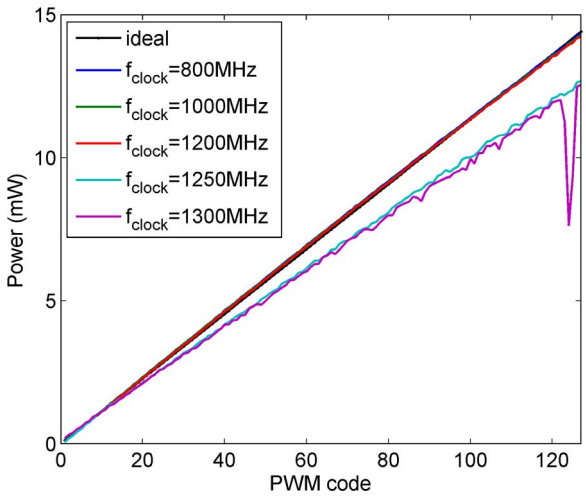

Fig. 4. Heater power for all possible PWM codes (7 bit) of the heater control circuit calculated from measured PWM output signals.

switching transistor that drives the heating resistor. When the counter overflows, the output of the flip-flop gets cleared again.

The outputs of the drivers will be connected to the heating resistors on the photonic IC via inter wafer connects (IWCs) [14] adding a 40 fF parasitic capacitance. The heating resistor implemented is 230 Ω. The supply voltage is 1.8 V resulting in a maximum heating power of ~14 mW. This heating power corresponds to a temperature change of $\sim$ 120 °C in the microrings we intend to control.

Most critical parts in the chip are the counter and the circuit blocks for generation of the PWM signal. For MR resonators as in [3], a minimum PWM frequency of 7.58 MHz is necessary to keep thermal ripple introduced by the PWM signal below critical limits. Furthermore, 7-bit pulse width resolution is required to be able to tune the resonance of the MR fine enough to activate it and to compensate for production tolerances. For digital generation of the PWM signal, a counter is necessary with a clock frequency defined by the PWM frequency and the resolution (7.58 MHz*128). For the given values, this minimum clock frequency is 970 MHz. Therefore, the control circuit was designed to operate with a clock frequency larger than 1 GHz, which is at the limit of the process used.

The measurement results in Fig. 4 prove the feasibility of the PWM approach. The relation between the PWM code stored in the register and the corresponding mean heating power is very linear up to clock frequencies of 1.2 GHz and there are no missing codes. This is 200 MHz faster than necessary to guarantee that the temperature ripple is below critical limits for typical MR resonators [12], [13].

At clock frequencies above 1.2 GHz, the logic block responsible for the generation of the PWM signal gets to its limit. In Fig. 5, the output signal is shown for all possible PWM codes at a clock frequency of 1.3 GHz to show the limit for this approach in the used technology. The brighter lines (brighter red in colored version) on the top of the 3-D graph show codes and time periods where the PWM generation does not work anymore. This can be explained by the maximum operating speed of the digital comparator. Above a clock frequency of approximately 1.2 GHz, the digital comparator is not fast enough anymore to detect when the counter value reaches the value stored inside the data register. If this happens, the flip flop is not set and the output stays off. If the clock frequency is further increased, of course at some point, the counter will also stop working.

This behavior is also visible in Fig. 4. Since the output driver is not set in each PWM period for clock frequencies higher than 1.2 GHz, the mean heating power is decreasing. This effect gets stronger with increasing clock frequency.

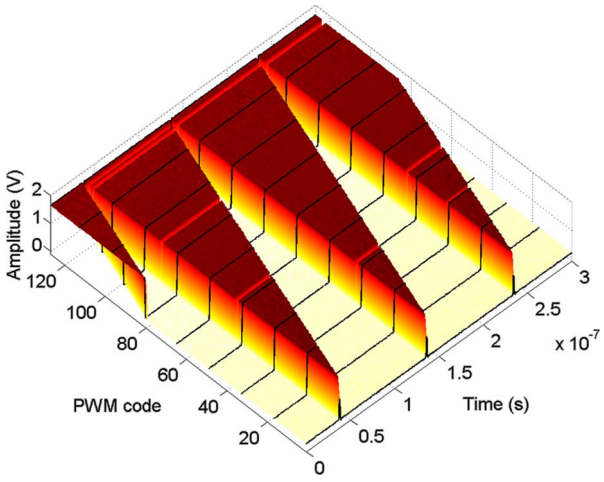

Fig. 5. Measured PWM output signals of the heater control circuit for a clock frequency of 1.3 GHz for all possible PWM codes.

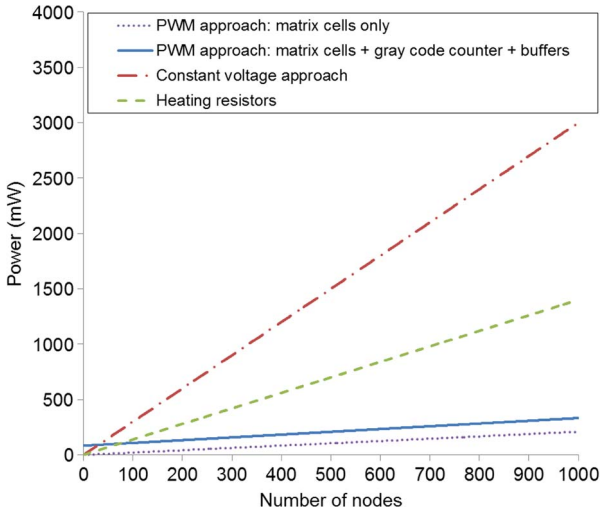

Fig. 6. Power consumption as a function of the number of photonic switch nodes for the PWM and constant voltage heater control approaches in comparison to the heater power dissipated by the heating resistors. Only non-active microrings tuned for compensating process variations are considered.

4. Comparison With Constant Voltage Approach and Conclusion

The chip area of one matrix cell is $79 \times 105\ \mu m^2$. In a typical optical switch matrix, only a few MRs are activated, and therefore, they can be neglected in the estimation of the total power consumption of a large matrix. All the other MRs have to be tuned only slightly to compensate process variations resulting in a typical heating power in the range of 1.4 mW each.

Fig. 6 shows a comparison of the power consumption, depending on the number of MRs of i) the matrix cells with the presented PWM approach, ii) the matrix cells including the gray counter and the buffers, iii) the estimated power for a control circuit with a constant voltage approach, and iv) the power dissipated by the heaters. In Fig. 6, only the off-state MRs are considered, since they are typically many more than the on-state MRs.

In our PWM approach, the power consumption per matrix cell is $\sim 210\ \mu W$ at 1 GHz and almost independent of the set heating power. Additionally, the power consumption of the counter

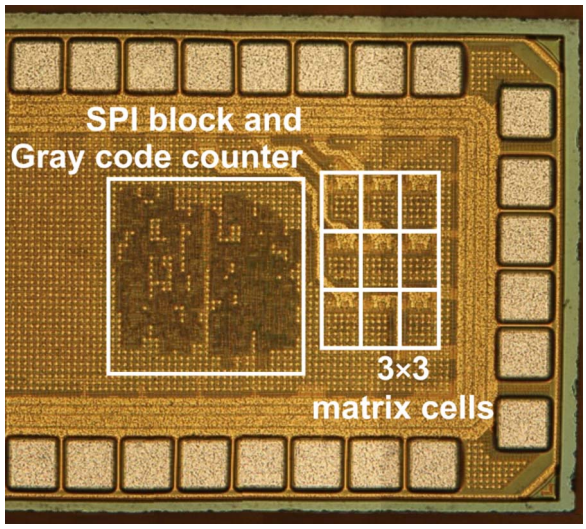

Fig. 7. Chip micrograph.

is approximately 83 mW (at 1 GHz clock). However, only one counter is needed for the whole matrix.

For a constant voltage approach, the power consumption per matrix cell circuit is approximately 3 mW, assuming a supply voltage of 1.8 V, a heating resistor of 230 Ω, and a heating power for compensating production tolerances of approximately 1.4 mW.

Starting from 30 nodes, the PWM approach has considerably lower power consumption than the constant voltage approach. Typical applications will involve switch matrices with several 100 nodes or even several thousand nodes. The presented chip can be easily extended to control matrices with that many elements. For 1000 nodes, the power consumption of the PWM approach (including the counter and necessary bus drivers) is reduced to 11.1% of that of the constant voltage approach. This not only helps reduce the power consumption of the total system. The additional power dissipated in the constant voltage approach would detune the MR resonators. Furthermore, if you want to keep the system small it gets increasingly difficult to dissipate the heat generated inside the package if the power consumption increases. Reducing the power consumption of the control circuit by this PWM approach is therefore a crucial step towards large integrated optical switch matrices.

In Fig. 7, a chip micrograph is shown. The chip size is 1.2×1 mm^2.

Acknowledgment

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