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DIPLOMARBEIT

Upgrade Studies for the Belle Silicon Vertex Detector

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Kurzfassung

Silizium-Mikro-Streifen-Detektoren sind heutzutage von sehr großer Bedeutung für die Hochenergiephysik, da sie in nahezu allen Experimenten zur Messung der Spuren elektrisch geladener Teilchen, welche bei der Kollision von Teilchenstrahlen in Beschleunigeranlagen entstehen, verwendet werden. Ein Beispiel ist der Belle-Detektor, der sich um den Kollissionspunkt des Elektron-Positron-Beschleunigers der High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, befindet.

Der derzeit im Belle-Experiment installierte Silicon Vertex Detector (SVD) leidet unter der immer größer werdenden Occupancy (darunter versteht man den Anteil der Streifen, die zu einem beliebigen Zeitpunkt ein Signal ungleich Null liefern) der innersten Lage. Diese Diplomarbeit beschäftigt sich mit Methoden zur Reduktion der Occupancy von Silizium-Detektor-Systemen. Um dies zu erreichen, besteht eine Möglichkeit darin, die Streifenlänge und somit die sensitive Fläche der Silizium-Sensoren zu reduzieren, was aber zwingend zu einer Erhöhung der auszulesenden Kanäle führt. Ein anderer Ansatz ist es, die derzeitige Ausleseelektronik durch ein System mit kürzerer Integrationszeit zu ersetzen, wodurch das sensitive Zeitfenster verringert wird.

In dieser Arbeit wird gezeigt, wie der schnelle und moderne Auslesechip APV25, welcher ursprünglich für den Silicon Strip Tracker des Compact-Muon-Solenid-Projekts (CMS) am CERN (Geneva, CH) entwickelt wurde, unter den Bedingungen des Belle-Experiments eingesetzt werden kann. Im Gegensatz zu CMS, wo einseitige Sensoren verwendet werden, arbeitet der Belle-SVD mit doppelseitigen Silizium-Streifen-Detektoren (DSSD), was umfassende Änderungen des Auslesesystems erfordert.

Die Hauptaufgabe des Projekts bestand darin, einen Prototypen einer solchen Ausleseelektronik zu entwerfen und die Software zur Datennahme und -analyse an die neuen Erfordernisse anzupassen. Weiters wurde eine verbesserte Methode der Datenauswertung unter Verwendung des APV25 in die Software implementiert, welche es ermöglicht, den wahren Durchtrittszeitpunkt eines Teilchens mit bisher nicht erreichter Genauigkeit zu rekonstruieren.

Abschließend wurde die Funktion des Protoypen, der Software und der modifizierten Datenanalyse durch mehrere Messreihen in Teilchenstrahlen (Beam Tests) am KEK und am Paul Scherer Institut (PSI, Villigen, CH) evaluiert. Die dabei gewonnen, hervorragenden Ergebnisse waren ausschlaggebend dafür, dass bereits an einer Implementierung des Nachfolgers des derzeitigen Belle-SVDs gearbeitet wird, wobei der APV25 und andere Teile des neu entworfenen Auslesesystems zum Einsatz kommen werden.

Diese Diplomarbeit umfasst nur die Anfänge meiner im Jahr 2004 begonnenen Tätigkeit für das Institut für Hochenergiephysik der Österreichischen Akademie der Wissenschaften (HEPHY). Weiterführende Themen werden im Kapitel “Summary and Outlook” kurz vorgestellt. Da die Entwicklungsarbeit zu diesem Projekt weiterläuft, kann zum jetzigen Zeitpunkt noch kein abschließender Bericht verfasst werden.

Stichworte: Siliziumdetektor, Streifendetektor, Vertexdetektor, Ausleseelektronik, Verstärker, APV25, Belle, SVD, KEK, Upgrade, Occupancy

Abstract

Today silicon microstrip detectors are very important for the research of high energy physics, because in virtually every experiment they are used to measure the tracks of charged particles which are produced by colliding particle beams. Such an experiment is the Belle detector, which is located around the collision point of the electron positron accelerator of the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan.

The currently installed Silicon Vertex Detector (SVD) of the Belle experiment suffers from the increasing occupancy (fraction of hit channels with non-zero signal at any random moment) of its innermost layer. This diploma thesis describes methods to reduce the occupancy of such a detector system. One possible improvement is to shorten the strips of the silicon sensors and thus reduce their active area, but this implies an increase of the total number of readout channels. Another method is to replace the currently installed readout electronics by one with a shorter integration period, which reduces the sensitive time window.

It will be shown how the fast and modern readout chip APV25, which was originally developed for the Silicon Strip Tracker of the Compact Muon Solenoid (CMS) project at CERN (Geneva, CH), can be used in the environment of the Belle experiment. In contrast to CMS, which uses single-sided sensors, the Belle SVD employs double-sided silicon strip detectors (DSSDs) which require significant modifications to the readout system.

The main task of this thesis was the development of a prototype of such a readout system and the revision of the data acquisition and analysis software to meet the new requirements. Furthermore, an advanced data processing method which can be applied using the APV25 was implemented into the software. With this method it is possible to reconstruct the time when the particle traversed the sensor with unprecedented precision.

Finally the readout system, the software and the improved data acquisition method were evaluated in several particle beam tests at the KEK and the Paul Scherer Institut (PSI, Villigen, CH) with excellent results. Since the requirements are easily met, it was decided to initiate the replacement of whole the Belle SVD, using the APV25 and other components of the new readout system.

This thesis covers only the earlier part of my work for the Institute of High Energy Physics of the Austrian Academy of Sciences (HEPHY), which i started in 2004. Additional topics are briefly introduced in the chapter “Summary and Outlook”. As work is ongoing, it is too early to give a final report.

Keywords: silicon detector, strip detector, silicon vertex detector, occupancy, readout electronics, amplifier, APV, Belle, SVD, KEK, upgrade

Contents

1. Introduction

A lot of new phenomena and principles were discovered by particle physicists in the last century. They established a sophisticated theory called "Standard Model" (SM) of particle physics, describing elementary particles, which are the building blocks of matter and the universe, and their interactions. Even tough the SM was very successful, several open issues remained and have to be investigated.

Therefore, large-scale accelerators are used to generate highly energetic beams in opposite directions and bring them to collision in order to produce and study a variety of particles that are not available in nature today. Physicists are interested to observe these new particles because they help to understand the conditions of the universe shortly after the big bang.

1.1. The KEK B-Factory

KEKB is an asymmetric electron-positron collider located at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan. Asymmetric means that the two beams of the collider are operated at different (kinetic) energies. It is a B-factory aiming to produce copious B and $\bar{\mathrm{B}}$ meson[1] pairs from the $\Upsilon(4\mathrm{S})$ resonance at a center of mass energy (E_{CM}) of 10.58 GeV. The $\Upsilon(4\mathrm{S})$ is a meson which contains a b-quark and a b-antiquark and immediately decays into a $\mathrm{B}^0\bar{\mathrm{B}}^0$ pair with a very high probability [1]. The physics goal of KEKB is to study decays of such $\mathrm{B}^0\bar{\mathrm{B}}^0$ pairs and will be described in detail in section 1.2.

The construction of the collider was started in April 1994 and completed in November 1998 [2]. It has two rings of 3016 m circumference, the high energy ring (HER) for 8 GeV electrons and the low energy ring (LER) for 3.5 GeV positrons installed side by side in a tunnel 11 m below ground level. Fig. 1.1 shows the schematic layout of the KEKB collider. A linear accelerator system generates and injects both beams directly into each ring at full energies. The rings cross at the interaction point in the so-called Tsukuba experimental hall where the electrons and positrons are brought to collision. At this location, the Belle experiment[2] (see section 1.2) with its particle detector is installed around the interaction point. To get equal circumferences of both rings, a second crossing is situated opposite to the collision point in the so-called Fuji hall where the two rings pass each other at different heights without interaction.

The rate R of reaction in a collider is defined by

$$R = \sigma\mathcal{L} \tag{1.1}$$

where σ is the cross section of the interaction region at the collision point and $\mathcal{L}$ is called the luminosity, usually expressed in $\mathrm{cm}^{-2}\mathrm{s}^{-1}$. In a system with two oppositely directed

[1] Mesons are non-elementary particles composed of an even number of quarks and antiquarks. The B meson consists of a b-antiquark and either an u- or d-quark. Its antiparticle, the $\bar{\mathrm{B}}$ meson, is made of a b-quark and an u- or d-antiquark.

[2] In terms of High Energy Physics, "experiment" is often used synchronously to "detector".

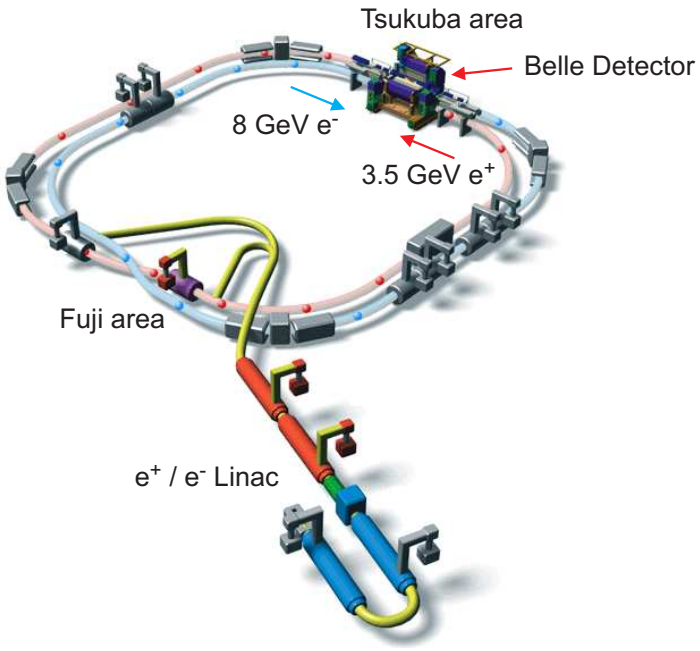

Figure 1.1.: Schematic layout of the KEKB collider with the LER colored in red and the HER colored in blue, respectively.

beams of particles traveling in bunches it can be expressed by

$$\mathcal{L} = fn\frac{N_1 N_2}{\sigma_x \sigma_y} \quad . \tag{1.2}$$

In eq. 1.2 f stands for the revolution frequency, n is the number of bunches present in the rings, N_1 and N_2 are the number of particles in each bunch and the product $\sigma_x\sigma_y$ describes the cross sectional area σ of the beams [1].

Due to the aims of Belle the collider was originally designed to obtain a luminosity of more than 10^{34} cm^{-2}s^{-1} which is more than one order of magnitude higher than the maximum ever achieved by other electron-positron colliders [3]. The design beam currents in the rings are 1.1 A in the HER and 2.6 A in the LER carried by approximately 5000 bunches with 0.6 m bunch spacing. In November 2006, a peak luminosity of $1.712 \cdot 10^{34}$ cm^{-2}s^{-1} was reached and is aimed to be even further increased in the future.

An important value to characterize the performance of an accelerator is the integrated luminosity, which is the integral of the luminosity with respect to time. Its unit is m^{-1}, but in terms of particle physics, it is usually expressed in inverse Barn (b^{-1}), where 1 b $= 10^{-28}$ m^2. Since the commissioning of KEKB an integrated luminosity of 771296 pb^{-1} was achieved, which approximately corresponds to 771 M B$\bar{\text{B}}$ pairs. Fig. 1.2 illustrates the history of the total integrated luminosity.

Another interesting feature of the KEKB collider is the finite-angle crossing at the interaction point, which means that the electron and positron bunches collide at an angle of ± 11 mrad. Using this scheme, parasitic collisions are reduced and furthermore no separation dipole magnets are necessary such that the interaction region is much simpler than in systems with head-to-head collision. [4]

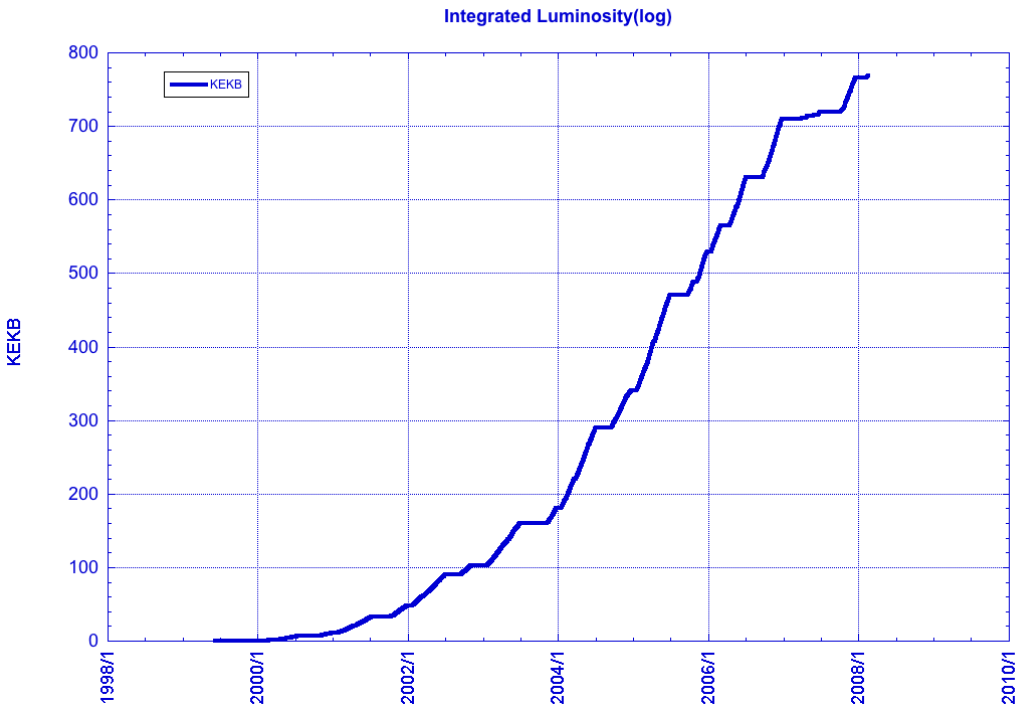

Figure 1.2.: Integrated luminosity history of KEKB since the commissioning in 1998.

1.2. The Belle Experiment

Physicists suppose that the very young universe consisted of equal amounts of matter and antimatter. Today's world is entirely made of matter, while antimatter can only be artificially produced in laboratories. What is the reason of this fact? Why has matter become dominant to antimatter? This is one of the unsolved questions in physics for which scientists try to find an answer. One explanation of this phenomenon can be found in the violation of the Charge-Parity (CP) symmetry, also called CP violation. The CP transformation describes a combined inversion of charge (C) and parity (P) of particles. In detail, the C operation reverses all quantum numbers like electric charge, lepton number, strangeness, etc., which means the transformation of a particle into its antiparticle, for instance an electron into a positrons. The P conversion revolves the direction of all coordinates of the position vector and corresponds to a reflection in a plane mirror, followed by a rotation by 180° [5].

For a long time it was commonly assumed that the CP is conserved. However, in 1964 the physicists Christenson, Cronin, Fitch and Turlay detected a violation of the CP symmetry at the decay of neutral K mesons [6]. Since then, CP violation has been measured and confirmed in several experiments. Until recently, it was only possible to observe a very small effect in the decay rates of K mesons.

A theoretical explanation of the CP violation within the SM was given by Makoto Kobayashi and Toshihide Maskawa in the year 1973 [7]. They published a complex unitary 3 x 3 matrix, later called Cabibbo-Kobayashi-Maskawa-Matrix (V_{CKM}), which was derived from Nicola Cabibbos work [8] by adding a third, at this time still undiscovered, generation[3] of quarks. The matrix describes the mixing between different quark

[3]Quarks of different generations only differ in their mass, all other interactions and quantum numbers are identical. In the SM there are three generations with two quarks in each, one with -1/3 e charge

generations and is given by

$$\begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix} = \begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} \quad . \tag{1.3}$$

On the left side of eq. 1.3 the CKM matrix is multiplied with a vector of flavor[4] eigenstates of the quarks and on the right are the mass eigenstates of the quarks, which are a linear combination of them. Kobayashi and Maskawa further postulated that the phenomenon of CP violation is only possible in accordance with the SM when the elements V_{ub} and V_{td} have a complex phase. There are several parameterizations of the CKM. Using the Wolfenstein parameterization [9], the matrix can be expressed by

$$V_{CKM} = \begin{pmatrix} 1 - \frac{\lambda^2}{2} & \lambda & A\lambda^3 (\rho - j\eta) \\ -\lambda & 1 - \frac{\lambda^2}{2} & A\lambda^2 \\ A\lambda^3 (1 - \rho - j\eta) & -A\lambda^2 & 1 \end{pmatrix} \quad , \tag{1.4}$$

where the imaginary term η is the so called Kobayashi-Maskawa phase and A, ρ and λ are real numbers. The unitarity of the CKM determines

$$\sum_i V_{ij} V_{ik}^* = \delta_{jk} \quad \text{and} \quad \sum_{\mathrm{j}} \mathrm{V_{ij}} \mathrm{V_{kj}^*} = \delta_{\mathrm{jk}} \quad , \tag{1.5}$$

and the six resulting combinations can be represented as triangles in a complex plane, each of which is called an unitary triangle. Their shapes are in general very different, but they all confine the same area, which is related to the CP violation phase.The most commonly used unitary triangle derives from

$$V_{ud} V_{ub}^* + V_{cd} V_{cb}^* + V_{td} V_{tb}^* = 0 \tag{1.6}$$

by dividing each side by the best-known one, $V_{cd} V_{cb}^*$. The aim of physicists is to determine

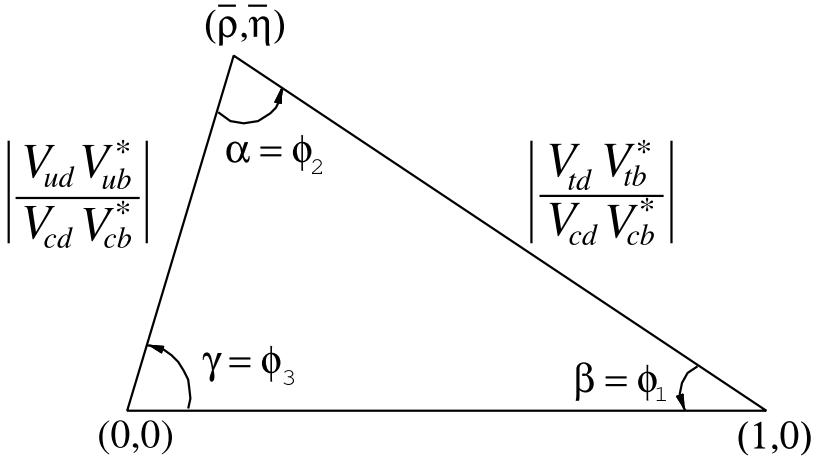

Figure 1.3.: Sketch of the unitary triangle derived from eq. 1.6 [10]

the sides and the three angles (ϕ_1, ϕ_2, ϕ_3) of the unitary triangle by measurements in

(down-type) and the other with +2/3 e charge (up-type).

[4]Flavor is a quantum number of elementary particles related to their weak interactions.

large-scaled experiments. Such a dedicated experiment is Belle[5], located around the interaction point of the KEKB accelerator (see 1.1). The primary motivation of Belle is to measure CP violating effects in neutral B meson decays to get direct information on the angles of the unitary triangle.

One of these effects is the time-dependent CP asymmetry [11, 12] of neutral B decays given by

$$a\left(\Delta t\right) = \frac{\Gamma\left(\mathrm{B}^0_{\mathrm{phys}}\left(\mathrm{t}\right) \rightarrow \mathrm{f}\right) - \Gamma\left(\bar{\mathrm{B}}^0_{\mathrm{phys}}\left(t\right) \rightarrow f\right)}{\Gamma\left(\mathrm{B}^0_{\mathrm{phys}}\left(\mathrm{t}\right) \rightarrow \mathrm{f}\right) + \Gamma\left(\bar{\mathrm{B}}^0_{\mathrm{phys}}\left(t\right) \rightarrow f\right)} = sin\left(2\phi_1\right) sin\left(\Delta m \Delta t\right) \quad , \tag{1.7}$$

where $\mathrm{B}^0_{\mathrm{phys}}$ and $\bar{\mathrm{B}}^0_{\mathrm{phys}}$ are pure B^0 and $\bar{\mathrm{B}}^0$ mesons at $t = 0$, f denotes a final decay state, $\Delta m = 0.463 \pm 0.018$ ps^{-1} is the $\mathrm{B}^0 - \bar{\mathrm{B}}^0$ mass difference, Δt is the difference in decay time between the two and ϕ_1[6] is one angle of the unitary triangle shown in fig. 1.3.

The goal is to observe B^0 and $\bar{\mathrm{B}}^0$ decays that fit the conditions of eq. 1.7, measure Δt and determine the angle ϕ_1. The required integrated luminosity for this measurement is estimated to be between 30 and 100 fb^{-1} [4], which corresponds to the data of about $30 \cdot 10^6$ to $100 \cdot 10^6$ B-meson decays. At Belle the luminosity continuously increased since operation started in 1999 and reached the world's highest value of $1.712 \cdot 10^{34}$ cm^{-2}s^{-1} in November 2006. The decay time difference between $\mathrm{B}^0_{\mathrm{phys}}$ and $\bar{\mathrm{B}}^0_{\mathrm{phys}}$ is just about few

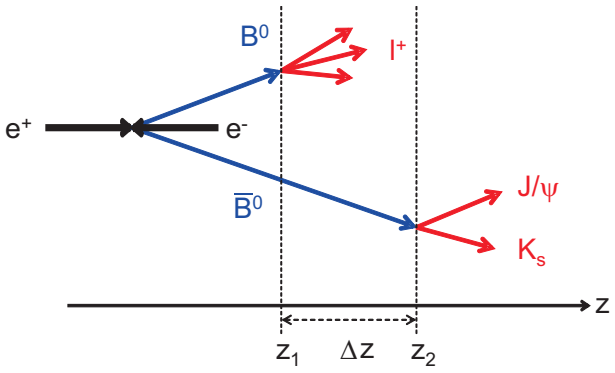

Figure 1.4.: Schematic depiction of a $\mathrm{B}^0\bar{\mathrm{B}}^0$ event. At z1 the B^0 decays into one hadron (l^+) and other particles, while at position z2 the $\bar{B}^0$ decays into a ($J/\Psi K_s$) pair. The distance between those decay (Δz) is of interest at the Belle experiment.

picoseconds and thus cannot be measured directly. As mentioned in section 1.1, the KEKB produces copious B^0 and $\bar{\mathrm{B}}^0$ meson pairs from the $\Upsilon(4\mathrm{S})$ resonance at a center of mass energy of 10.58 GeV. Moreover the collider works with asymmetric energies of 8 GeV and 3.5 GeV for electrons and positrons, respectively. This leads to $\mathrm{B}^0\bar{\mathrm{B}}^0$ pairs with a boost factor $\beta\gamma = 0.42$ and thus a center of mass moving in the labsystem. Hence the mesons decay at different locations in z direction[7], depending on their lifetime. The distance Δz of the two decay vertex positions is related to Δt via

$$\Delta z = \beta\,\gamma\,c\,\Delta t \quad , \tag{1.8}$$

where $\beta = \frac{v}{c}$, v is the center of mass velocity, c the speed of light and $\gamma = \frac{1}{\sqrt{1-\beta^2}}$.

[5]The name Belle is derived from the French word for beauty. Without a B, Belle is reduced to the T-reversal-invariant palindronomic French pronoun elle.

[6]Also named β in literature.

[7]z is the coordinate which coincides with the beam axis.

Since Δz is only about 200 μm, it is required to use silicon strip detectors (see section 2.1) with a resolution of less than 100 μm for an accurate measurement. Fig. 1.4 illustrates an e^+e^- collision where Δz is the interesting distance between the decay vertices of the B^0 and $\bar{B}^0$ mesons.

The B physics of Belle is not only restricted to the measurement of the angle ϕ_1, also various other parameters of the unitary triangle and thus the CKM matrix are of interest. Further information about the work of the collaboration and publications of their results can be found at the project's web site [13].

1.3. Belle Detector

The Belle detector is composed of various types of subdetectors which are arranged cylindrically around the beam pipe at the interaction point in the Tsukuba hall. A cross section of the detector is shown in fig. 1.5. From inside to outside those subdetectors are the Silicon Vertex Detector (SVD), the Central Drift Chamber (CDC), the Aerogel Cherenkov Counter (ACC), the Time-of-Flight counters (TOF), the Electromagnetic Calorimeter (ECL), surrounded by the superconducting solenoid and the K^0_L Meson and Muon detector (KLM) [14]. The whole detector has an octagonal-prism shape with a circumference and a length both about 8m. In the Belle experiment, a cylindrical coordinate system is used to appoint any position inside the detector. The z axis is defined in the direction of the electron beam and the r-ϕ plane is orthogonal to this axis. All subdetectors are designed to cover a θ region extending from 17° to 150°, where θ is the polar angle relative to the z-axis with the interaction point as the origin.

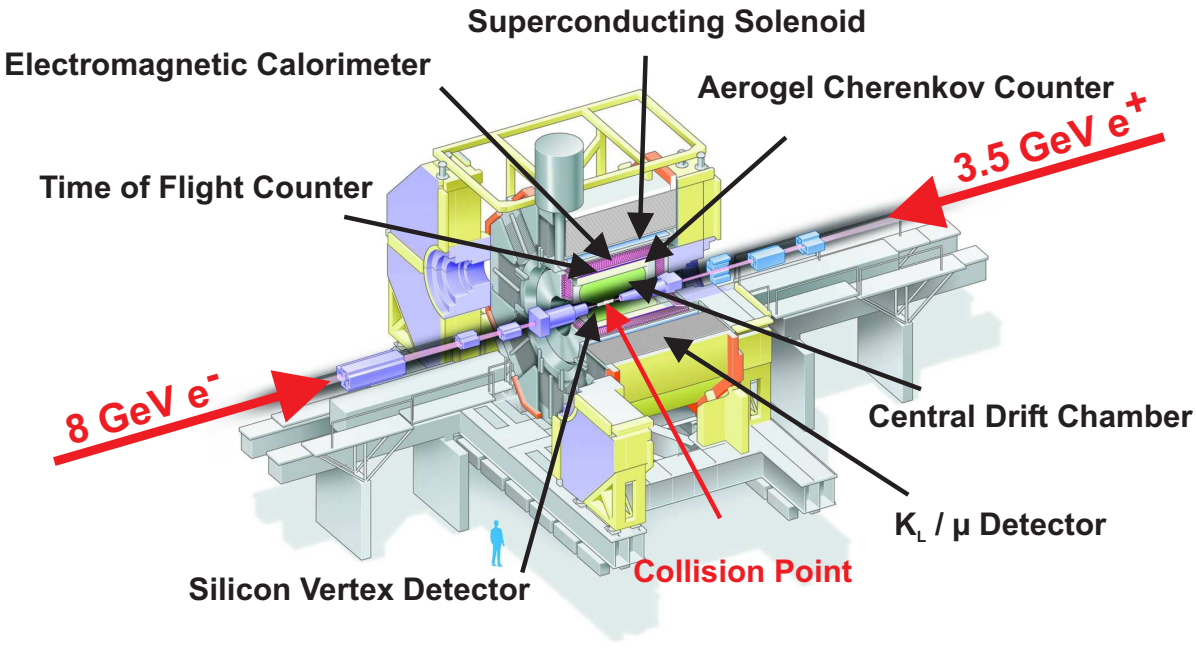

Figure 1.5.: Cross section of the Belle detector.

1.3.1. Silicon Vertex Detector

The SVD is the innermost system of the Belle detector and currently consists of four layers of double-sided silicon sensors which are described in sections 2.1 and 2.2 in detail.

It is used to measure the vertices of the two B meson decays (see 1.2) with a position resolution of less than 100 μm and it also plays an important role for track reconstruction. A more detailed description of the SVD design is given in section 3.

1.3.2. Central Drift Chamber

The Central Drift Chamber[8] (CDC) is intended to measure the tracks left by charged particles and to determine their momenta as well as the sign of their charge. It consists of 50 cylindrical layers and a total number of 8400 drift cells. The length of the CDC is 2400 mm and its inner and outer radii are 83 and 874 mm, respectively. A mixture of 50% helium and 50% ethane, with a radiation length of about 640 m and a drift velocity that saturates at 4 cm/μs is used. The sense wires are made of gold-plated tungsten with 30 μm diameter. These sense wires are surrounded by 126 μm thick aluminum field wires to produce a proper electrical field. Overall there are 8400 readout channels and 24944 field wires installed.

The CDC provides a position resolution of few millimeters in z and about 130μm in r-ϕ direction and its momentum resolution is about $0.19p_t \oplus 0.30/\beta$ % [15], where p_t denotes the traverse momentum. Furthermore, the particle tracks found by the CDC are extrapolated inwards to the SVD where they are used as a starting point to determine the vertices of the B meson decays.

1.3.3. Silica-Aerogel Cherenkov Counter (ACC)

The ACC is placed around the CDC and is used for particle identification, in particular to distinguish between pions and kaons. A Cherenkov detector is a particle detector which utilizes the effect of the mass-dependent threshold energy of Cherenkov radiation. Each material has its specific velocity of propagation of light, which is always significantly lower than the speed of light in vacuum c. Cherenkov radiation is emitted, when a charged particle passes through a material at a velocity exceeding the speed of light in that medium. This radiated light is transformed into an electrical signal and amplified by photomultiplier tubes, which are attached to the aerogel modules. For the Belle ACC aerogels with a refractive index between 1.01 and 1.028 where chosen so that pions emit Cherenkov light, while kaons stay below the threshold. The covered momentum range of identified particles is between 1.2 GeV/c and 3.5 GeV/c [16]. The ACC is composed of two parts, the barrel and the forward endcap. The barrel consists of 960 counter modules, segmented into 60 cells in ϕ direction. The endcap is arranged in five concentric layers with a total of 228 counter modules.

1.3.4. Time-of-Flight Counters (TOF)

The TOF is composed of 128 plastic scintillaters read out by 256 photomultipliers tubes. It is used to identify particle types by measuring their velocity. Therefore the detector

[8] In a drift chamber many parallel wires (sense wires) are arranged as a grid and put on high voltage, with the metal casing or field forming wires being on ground potential. The chamber is filled with gas and a particle traversing it leaves a trace of ions and electrons, which drift toward the nearest sense or field wires, respectively. By labeling the wires with a current signal it is possible to measure the track of the traversing particle. In a drift chamber also the timing of the pulse and thus the drift time of the charges is measured, which improves the resolution within the cell.

determines the time of flight of these particles from the collision point to the counter with an accuracy of about 100 ps. In addition to particle identification the TOF also provides fast timing signals for the trigger system to generate gate signals for other subsystems like the CDC or the SVD.

1.3.5. Electromagnetic Calorimeter (ECL)

The ECL is intended to detect photons from B meson decays with high efficiency and good resolution in energy and position. It consists of a highly segmented array of thallium-doped cesium iodide crystals (CsI(Tl)). When a charged particle enters the calorimeter its whole energy is deposited in the crystals whereby light is emitted. The intensity of this emitted light is measured with photodiodes.

Most of the particles that should be detected are products of cascade decays and thus have relatively low energy, hence the ECL is designed to have a good performance below 500 MeV [17].

1.3.6. Kaon and Muon Detection System (KLM)

The KLM is the outermost subsystem of the Belle detector. It is designated to detect muons, which penetrate through most materials, and K_L^0 mesons, which are electrically neutral and thus are not seen by any other subsystem. It consists of alternating layers of charged particle detectors and 4.7 cm thick iron plates. Glass-electrode-resistive plate counters (RPCs) are used for the charged particle detectors . Those are two parallel plate electrodes with high bulk resistivity ($\geq 10^{10}$ Ω) separated by a gas-filled gap. An ionizing particle initiates a local discharge of these plates, which is limited by the high resistivity of the plates. The location and the time of this local ionization is detected by external pickup strips.

The neutral kaons, as well as the muons, interact with the iron plates and initiate a local shower of ionizing particles, which are detected by the sensitive planes. The multiple layers of charged particle detectors and iron allow the discrimination between muons and kaons, since muons travel much farther than kaons [14].

1.3.7. Superconducting Solenoid

The superconducting solenoid provides a homogeneous magnetic field of 1.5 T in the central volume of the Belle detector which is about 3.4 m in diameter and 4 m in length. All subdetectors are located inside this magnetic field except the KLM which is integrated into the iron structure of the solenoid, providing the return path of the magnetic flux as well as the overall support for the detector components. It consists of a fixed barrel part, which includes the plates of the KLM and two movable end-caps to allow access to the inner components of the detector for maintenance. The coil wire is made of a superconducting alloy of Niobium-Titanium. It is operated in a superconducting condition, cooled down to 5 K using liquid helium.

The magnetic field is used to determine the momentum of charged particles from the bending of their trajectories as well as to minimize the background of low energetic charged particles, which are also produced by the collisions but are not of interest.

2. Silicon Detectors and Readout

In high energy physics several types of particle detectors are commonly used. A very important family are the so called ionization detectors, which utilize the ionizing effect when charged particles traverse matter. One type of this concept is gaseous ionization like drift chambers, proportional counters and Geiger-Müller tubes, which were most widely used in the 1970s. Nowadays, they are often superseded by the more sophisticated semiconductor detectors. The main base material of such sensors is silicon, but germanium and diamond are also used in specific applications. An advantage of silicon microstrip sensors is that the well known technology of integrated circuit production provides the ability to manufacture high-density micron-scale electrodes on large wafers, offering an excellent position resolution. Furthermore the low ionization energy of silicon results in sufficient signals with active layers of typically 300 μm thickness.

In this chapter the design and the basic functionality of silicon particle sensors are discussed. Furthermore an overview about the components of the readout electronics for such detectors is given.

2.1. Silicon Detector

2.1.1. Energy Loss

When a charged particle traverses a solid state detector it loses energy due to the generation of free electron-hole pairs. This energy loss is described by an equation published by H.A.Bethe and F.Bloch [10], hence also known as Bethe-Bloch equation.

$$-\frac{1}{\rho}\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_ec^2\beta^2\gamma^2T_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} - \frac{C}{Z}\right] \tag{2.1}$$

Eq. 2.1 represents the differential energy loss per mass surface density in units of $[\mathrm{MeV}\,(\mathrm{g\,cm^{-2}})^{-1}]$, where $K = 4\pi N_A r_e^2 m_e c^2$, N_A is Avogadro's number, Z and A are the atomic number and the atomic mass of the traversed material, r_e is the classical electron radius $\left(\frac{e^2}{4\pi\epsilon_0 m_e c^2}\right)$ and m_e its mass, ze is the charge of the incident particle, $T_{\max}$ is the maximum kinetic energy which can be imparted to a free electron in a single collision, I is the mean excitation energy, $\beta = v/c$ and $\gamma = \frac{1}{\sqrt{1-\beta^2}}$. In comparison to the original Bethe-Bloch formula which describes the energy loss of particles traversing gases eq. 2.1 includes two additional terms. $\delta(\beta\gamma)$ is a correction for the shielding of the particle's electric field by the atomic electrons, the density effect caused by atomic polarization. The second correction term C considers that the basic assumption of atomic electrons is violated at very low incident particle energies.

Anyway, in thin layers like silicon detectors with a typical thickness of 300 μm a fraction of the lost energy is carried off by high energetic knock-on or δ electrons, which have enough energy to produce, themselves, additional electron-hole pairs while traversing the

medium (secondary ionization). These considerations lead to the restricted energy loss, which is expressed by an additional term in the Bethe-Bloch equation [18],

$$-\frac{1}{\rho}\frac{dE}{dx} = Kz^2\frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\frac{2m_e c^2\beta^2\gamma^2 T_{\text{upper}}}{I^2} - \beta^2\left(1+\frac{T_{\text{upper}}}{T_{\max}}\right) - \frac{\delta(\beta\gamma)}{2} - \frac{C}{Z}\right] \tag{2.2}$$

where

$$T_{\text{upper}} = \min\left(T_{\text{cut}}, T_{\max}\right) \tag{2.3}$$

with T_{cut} depending on the material and the incident particle momentum. Fig. 2.1 shows the comparison of the Bethe-Bloch equation to the restricted form for a pion traversing 300 μm of silicon. There is no difference between the standard and the restricted form

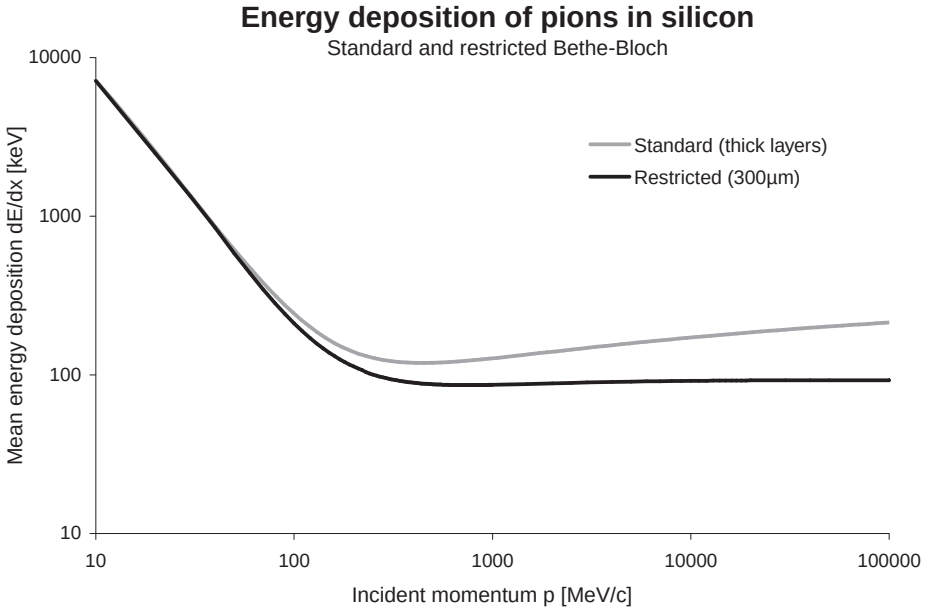

Figure 2.1.: Comparison of the standard Bethe-Bloch equation to the restricted form for a pion traversing 300 μm of silicon [18].

at low energies, because in this region the production of δ electrons is very unlikely. However, at momenta higher than 100 MeV/c a significant deviation of the curves is evident. The relativistic rise of the restricted form is quite flat because energy is carried off by δ electrons. Furthermore the energies of a minimum ionizing particle (MIP), that match the minima of each curve, are different. They are about 450 MeV/c for the original equation and 750 MeV/c for the restricted version, respectively.

In practice, the model of the restricted energy loss has been confirmed by countless experiments and beam tests with silicon sensors. One example is shown in fig. 2.2 for pions in a silicon detector of 300 μm thickness where an excellent match of the measured data and the restricted model is obvious.

2.1.2. Charge Collection

As described in the last section, the energy deposition of a traversing particle in a detector material leads to the production of free electron-hole pairs. Without any electric field these carriers will recombine after a while. To move this carriers out of the sensor

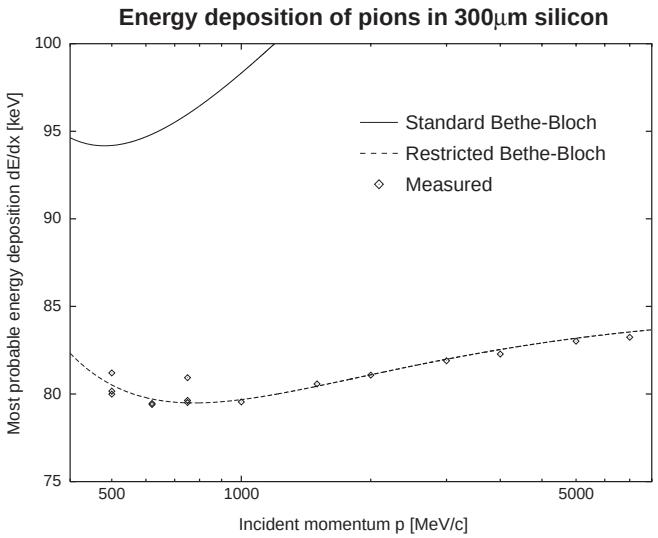

Figure 2.2.: Restricted model of energy loss of pions in a silicon detector of 300 μm thickness, compared to the measured most probable value and the standard Bethe-Bloch theory [18].

and thus being able to measure them, an electric field is necessary between two electrodes which are placed on the surface of the detector. Fig. 2.3 shows the principle configuration of such a detector with opposite electrodes.

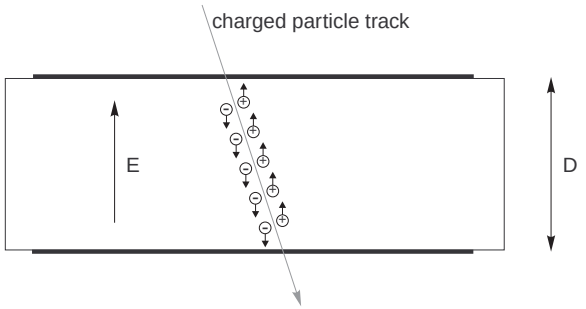

Figure 2.3.: The electric field between two electrodes drains the electron-hole pairs, which are created along the track of a traversing particle [18].

The number n of carrier pairs is given by the quotient of the total energy loss E_{loss} of the incident particle and the ionization energy E_{eh}, which is required for the pair production,

$$n = \frac{E_{\text{loss}}}{E_{eh}}. \tag{2.4}$$

Due to $E_{eh} = 3.6$ eV in silicon, the most probable charge for a MIP in a standard silicon sensor with a thickness of 300 μm is about $n = 22500$ pairs . The measured energy loss of MIPs for such a detector is subjected to statistical fluctuations which are described by the convolution of a Gauss and a Landau distribution. The typical shape of such a distribution is shown in fig 2.4 in terms of the collected charge. An important property of the Landau distribution is its asymmetric form, caused by the long upper tail which is a result of the rare but high energetic δ electrons. An ideal Landau distribution has a range that extends to infinite energies, but due to limitation of the measurement the

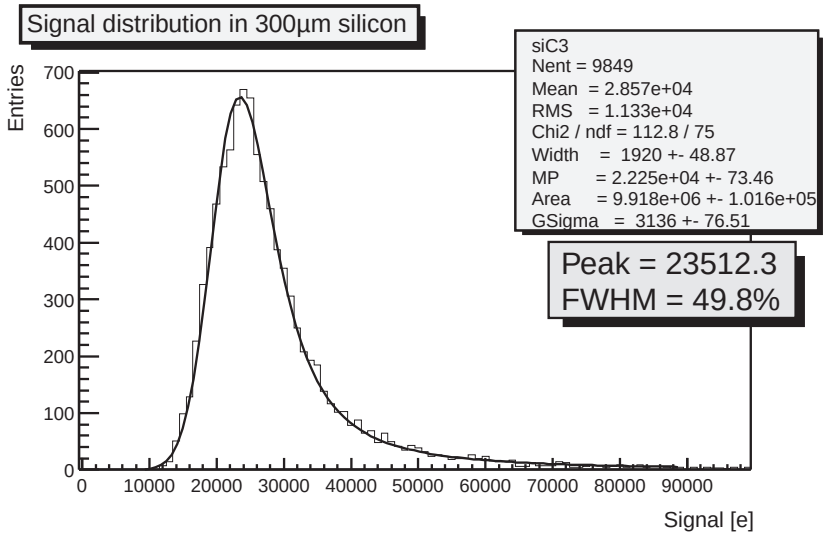

Figure 2.4.: Measured MIP signal distribution in a silicon detector of 300 μm thickness [18].

curve is always truncated in real systems. The edges are given by the pedestal threshold for the lower one and the dynamic range of the readout electronics for the upper one, respectively. As a result of the asymmetry, the mean energy loss is typically about 1.2 to 1.3 times higher [19] than the most probable (MP) charge, which is represented by the peak of the distribution. Moreover the MP signal can be obtained more accurate from a measured distribution than the mean value, because cuts on either end of the curve only affect the mean, but not the MP.

The electric field between the electrodes causes the carriers to move according to

$$v = \mu E \quad , \tag{2.5}$$

where is v is the mean carrier drift velocity, μ the carrier mobility and E the electric field. The mobilities and also the drift velocities of electrons and holes are different and depend on the material. The linear relation of eq. 2.5 is only valid for weak electric fields. At high field strength the increasing number of collisions between the carriers and the crystal lattice has to be considered, which results in a saturation of the average drift velocity. Empirical functions describing both linear and saturation ranges for silicon are given by eq. 2.6 and eq. 2.7 for electrons and holes, respectively [20].

$$v_e = \frac{\mu_e E}{\sqrt{1 + \left(\frac{\mu_e E}{v_{e,\,\mathrm{sat}}}\right)^2}} \tag{2.6}$$

$$v_h = \frac{\mu_h E}{1 + \frac{\mu_h E}{v_{h,\,\mathrm{sat}}}} \tag{2.7}$$

The saturation velocities $v_{e,\,\mathrm{sat}}$ and $v_{h,\,\mathrm{sat}}$ used in these equations are in the order of 10^7 cm/s, corresponding to an electric field in the order of 10^5 V/m.

Because of the moving charges inside the detector material a current is induced in the electrodes, no matter whether the carriers finally reach the electrodes or not. This current i is caused by both electrons and holes and is proportional to the sum of all carrier velocities as shown in eq. 2.8

$$i = \frac{q_e}{D}\left(\sum v_e + \sum v_h\right) \quad , \tag{2.8}$$

where q_e is the elementary charge and D the sensor thickness [21]. The total collected charge Q_c, which is usually measured with integrating amplifiers, results from the integration of i using

$$Q_c = \frac{q_e}{D} \int \left(\sum v_e + \sum v_h \right) dt \quad . \tag{2.9}$$

The generated electrons move to the positive electrode while the holes move to the negative electrode. This means that if no charges are trapped, the total travel distance of each pair equals the thickness of the sensor. With $v = \frac{ds}{dt}$ the integral term in eq. 2.9 results to nD and thus the total collected charge is obviously

$$Q_c = n\,e \quad . \tag{2.10}$$

In pure silicon, the number of thermally created carriers is many order of magnitude higher than the charge produced by a MIP. This means that it is impossible to use silicon as a detector material in this way. The charge collection area has to be depleted from these intrinsic carriers, which can be achieved by a reverse-biased pn-junction. Therefore on one surface of a homogeneously doped silicon a thin layer with high doping concentration of the other type is applied. Fig. 2.5 shows the principal layout of a silicon detector based on n-type bulk. The highly doped n^+-implant on the second surface is known as backplane and creates an Ohmic contact to the electrode.

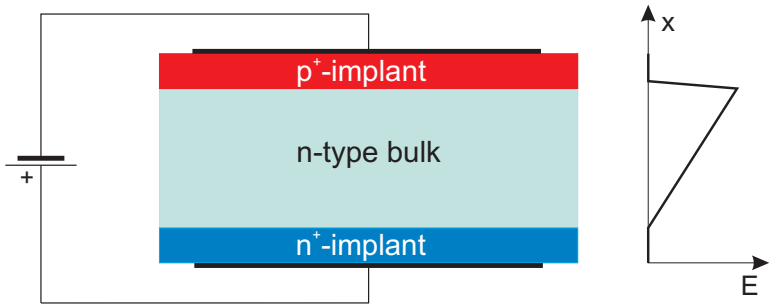

Figure 2.5.: Schematic cross-section of a silicon detector with n-type bulk. The implantation zones are shown much thicker than they are in reality. The electric field to the right is shown at the depletion voltage.

With increasing reverse bias voltage a zone without free carriers, the depletion zone, grows from the pn-junction toward the electrodes. It reaches the electrodes when the bulk is totally depleted at the so called depletion voltage V_{depl}. At this state only the core excess charges of donors and acceptors remain and the charge densities of bulk (ρ_{d}) and the p^+ implant (ρ_{a}) are

$$\rho_{\mathrm{d}} = e\,N_{\mathrm{d}} \quad \text{and} \quad \rho_{\mathrm{a}} = -e\,N_{\mathrm{a}} \quad , \tag{2.11}$$

where N_{d} is the density of donors and N_{a} of acceptors, respectively. The charge density is constant over the full width of the bulk and the charges are

$$Q_{\mathrm{d}} = d_{\mathrm{d}}\,\rho_{\mathrm{d}} \quad \text{and} \quad Q_{\mathrm{a}} = d_{\mathrm{a}}\,\rho_{\mathrm{a}} \quad , \tag{2.12}$$

where d_{d} and d_{a} are the width of the space charge areas. At equilibrium, the global charge has to be balanced ($Q_{\mathrm{d}} + Q_{\mathrm{a}} = 0$) and d_{a} can be expressed by

$$d_{\mathrm{a}} = d_{\mathrm{d}} \frac{N_{\mathrm{d}}}{N_{\mathrm{a}}} \quad . \tag{2.13}$$

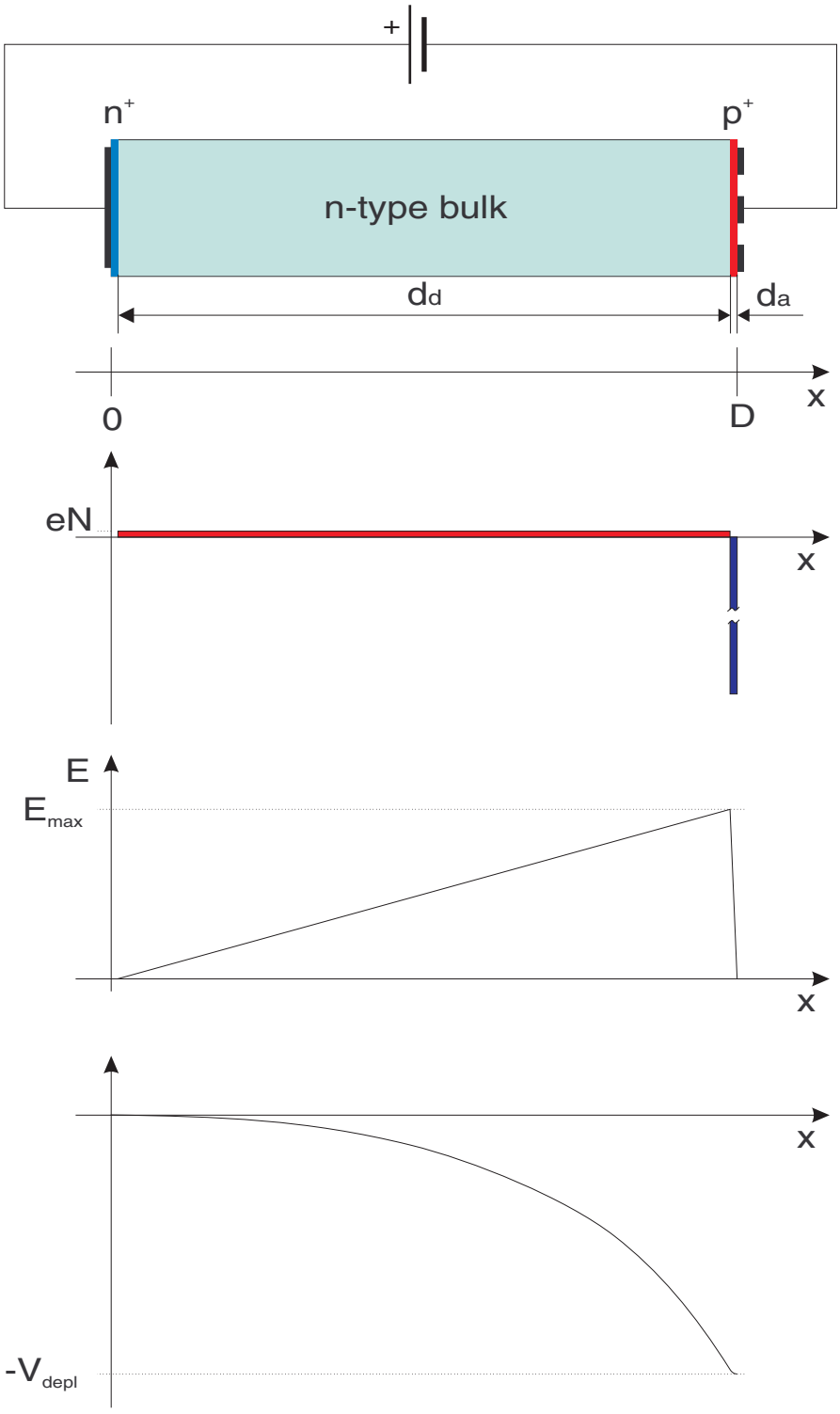

Figure 2.6.: Charge density, electric field and potential of a simplified model of a silicon detector at full depletion [18].

The relation between the charge density ρ and the electrical field strength is given by the one-dimensional Poisson equation

$$\frac{dE}{dx} = \frac{\rho}{\epsilon} \quad , \tag{2.14}$$

with the dielectric constant ϵ. Integration of the Poisson equation leads to an electric field of triangular shape as shown in fig. 2.6. It starts from zero at the backplane, rises to its maximum

$$E_{\max} = \frac{\rho_{\mathrm{d}}}{\epsilon} d_{\mathrm{d}} = \frac{\rho_{\mathrm{a}}}{\epsilon} d_{\mathrm{a}} \tag{2.15}$$

at the pn-junction and quickly falls down to zero again in the p^+ implant. The electric potential φ is defined by

$$\varphi = -\int E \, dx \tag{2.16}$$

and the difference of the potential at the electrodes is the voltage V applied to the sensor. By using above equations and considering that the the p^+ and n^+ regions are very thin and thus can be neglected compared to the bulk thickness ($d_{\mathrm{a}} \ll d_{\mathrm{d}}$ and $d_{\mathrm{d}} \approx D$), the depletion voltage becomes

$$V_{\mathrm{depl}} = \frac{e N_{\mathrm{bulk}} D}{2\epsilon} \tag{2.17}$$

with $N_{\mathrm{bulk}} = N_{\mathrm{d}}$. As described before, the electrical field extends over the whole bulk and is of triangular shape in case of full depletion ($V_{\mathrm{bias}} = V_{\mathrm{depl}}$). A bias voltage higher than V_{depl} adds an additional but constant offset to the field, which results in an approximately constant field at very high voltages ($V_{\mathrm{bias}} \gg V_{\mathrm{depl}}$). On the other hand, when the supplied voltage is below the depletion voltage, the field still is triangular with its maximum at the junction, but it does not reach the edges and only a part of the bulk is depleted. This leads to an inefficient charge collection with an active collection distance given by

$$d_c = D\sqrt{\frac{V_{\mathrm{bias}}}{V_{\mathrm{depl}}}} \quad . \tag{2.18}$$

In a fully depleted silicon detector all carriers induced by a traversing particle move towards the electrodes due to the electrical field where they are drained until all charges are gone. As shown in eq. 2.5 the mobilities of electrons and holes are different, thus the resulting current is a superposition of two pulses with different slope, but equal area as shown in fig. 2.7. At $V_{\mathrm{bias}} = V_{\mathrm{depl}}$ the shape of both currents is exponential, but it becomes more and more linear with increasing bias voltage. A more detailed discussion about the detector currents can be found in [18, 22].

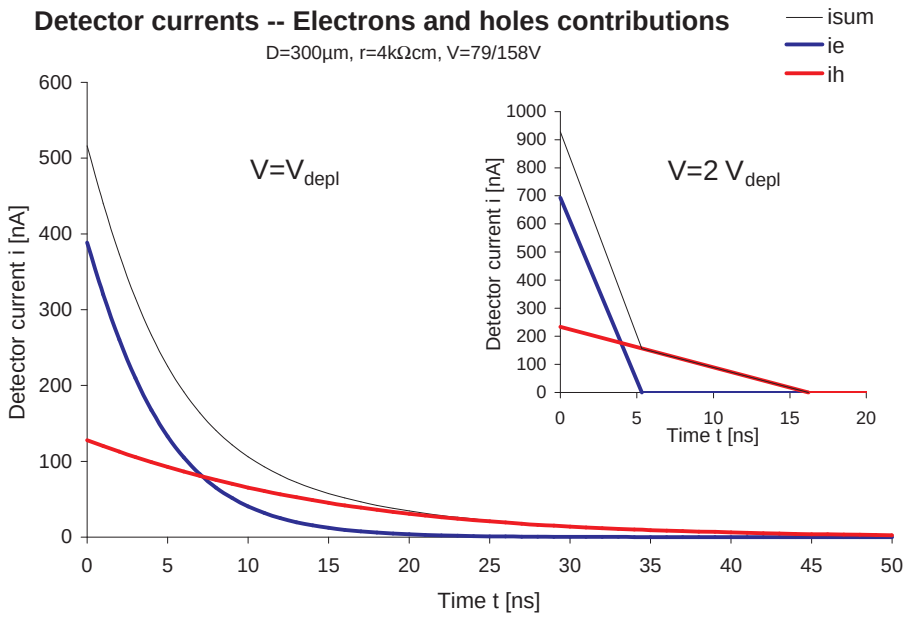

Figure 2.7.: Shape of the electron and hole currents in a standard silicon detector with a thickness of 300 μm at depletion voltage and at ($V = 2V_{\text{depl}}$)) [22].

2.2. Detector Design

The main purpose of silicon detectors in High Energy Physics is to measure the track of particles which are for instance the result of colliding particle beams. Therefore several detectors are placed in multiple layers around the interaction point of the collider. A segmented design of the electrodes is essential to achieve spatial information from silicon sensors. The two commonly used layouts are strips and pixels.

2.2.1. Strip Detectors

On strip detectors at least one of the electrode surfaces is made up of long thin lines with a typical spacing between 50 μm and 250 μm, while the second is either segmented in orthogonal direction or made of a single plate covering the entire sensor (backplane). The distance between two strips is also known as pitch and is an important parameter for the spatial resolution. The size of such sensors is primarily limited by the dimension of the silicon wafer from which they are cut out. Today wafers with a diameter of 4" or 6" are used and thus sensors of up to 10×10 cm^2 can be produced in a single piece. For larger detectors, two or more strip detectors have to be electrically and mechanically ganged to enlarge the total strip length. The outer layers of the Belle detector (see section 3), as an example, use up to three daisy-chained sensors.

As the signals of the sensors are very small, special readout chips with integrated low-noise amplifiers (see section 2.3.1) are used for signal processing. The common electromechanical technique for the connection between sensor and amplifier chips is wire bonding[1]. In general the pitch of the sensors strips is not equal to the bonding pad spacing on the readout chip and a so called pitch adapter has to be placed between

[1]Wire bonding is a method to make an interconnection between microchips and other electronics using thin wires with a diameter of typically 25 μm. This is done with a special machine (bonding station) by welding the wire onto the contacts with ultrasonic power.

them.

Usually, each strip of a detector is connected to a separate channel of the front-end chip. Sometimes only every second strip is read out and the remaining are terminated with high impedance. Such strips are called intermediate strips. Signals on these intermediate strips are partially transfered to the readout strips by capacitive coupling. This method has the advantage that the number of amplifier channels can be reduced. The performance of such a sensor is worse than with full readout, but still better than without intermediate strips [23].

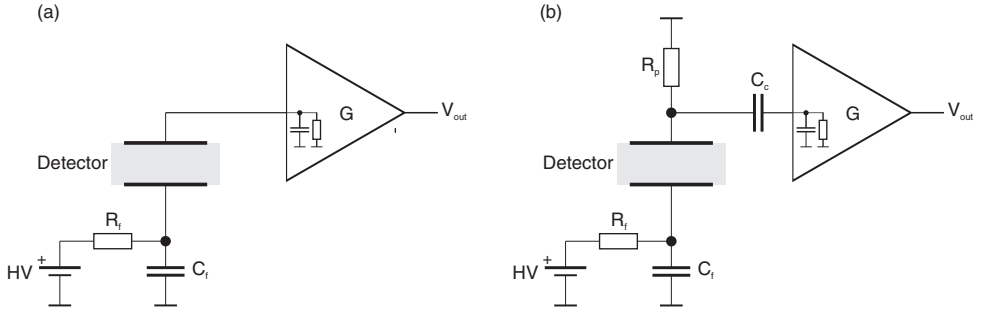

Figure 2.8.: The two possible connection scheme for a single channel of a silicon strip detector: DC coupling (a) and AC coupling (b) [18].

From the electrical point of view there a two possible coupling methods. The first one is to join each strip directly with its corresponding amplifier input (DC coupling). In that case the signal and also a fraction of the leakage current flows into the amplifier. Depending on the applied bias voltage, the sensor geometry and the radiation damage this leakage current varies in a wide range and can be higher than the signal itself. It is difficult to build amplifiers that are able to handle such a large range of input currents. The second method is to place a capacitance between the strip and the amplifier input and to bypass the DC leakage current over a resistor. Then only the AC part of the signal is seen by the readout chip and it does not have to provide a wide input range. Today, AC coupling is the preferred technique for silicon detectors. Fig. 2.8 shows the two possible coupling schemes of a single channel of a silicon detector.

Normally, the coupling capacitor is implemented by an additional aluminum layer on the top of the sensor. A thin silicon oxide film between the strips and the aluminum provides the required isolation. The implementation of the bias resistor is typically done by a polysilicon meander structure. Fig. 2.9 shows a magnified view of a such a silicon strip detector with n substrate and p^+ implants (strips), where the meander of the polysilicon is clearly displayed. In case of AC coupling all polysilicon resistors are connected to a common bias ring, so that the bias voltage can easily be applied to the sensor with a single contact. Furthermore a, RC filter is normally foreseen to decouple the bias voltage and thus reduce the noise.

Sensors which have a single backplane also called single-sided, because only one electrode is made up of thin lines and thus just a single coordinate can be measured. In order to get more information, one possibility is to design both electrodes as thin lines but with orthogonal orientation. Such sensors are called double-sided strip detectors (DSSD). The layout of the electrode of the second side is more complicated, because the strips have the same doping as the substrate and would be shorted without any additional measures. Nowadays, n doped silicon is commonly used as substrate for sil-

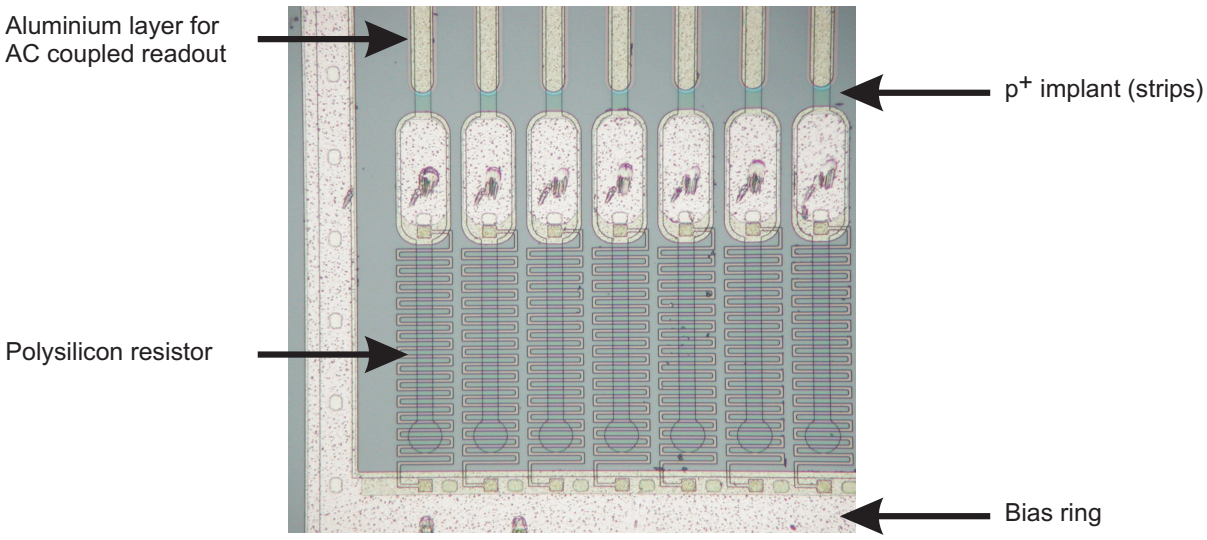

Figure 2.9.: Magnified part of a silicon strip detector with n substrate, p^+ implants and an aluminum layer for AC coupled readout.

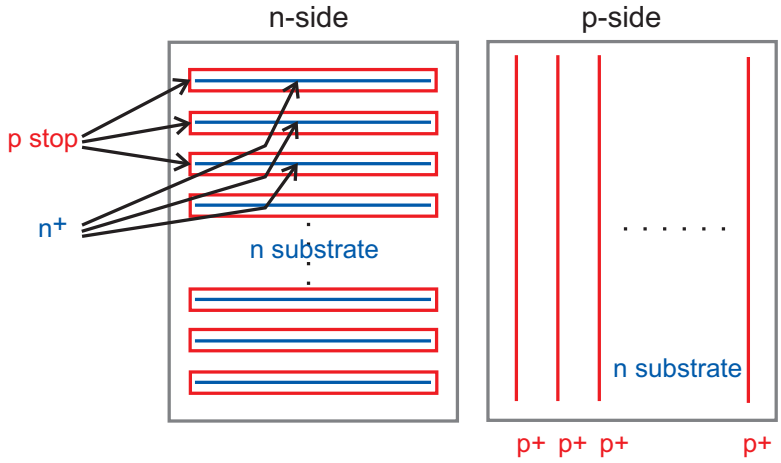

Figure 2.10.: Layout scheme of a DSSD based on a n-doped substrate with n^+ readout strips and atoll type p stops on n-side and p^+ readout strips on p-side, respectively.

icon strip detectors. In that case the design of the electrodes which are made up of p^+ implants is very easy, because the strips are automatically isolated against each other by the substrate. However, on the second side the electrodes are of n^+ doped silicon and additional p^+ implants, so-called p stops, are required between the strips to avoid short circuits. A typical strip layout of such a DSSD using so-called atoll type p stops, where each n^+ strip is surrounded by a floating p atoll, is displayed in fig. 2.10. Various p-stop types are compared in [24]. It was shown, that the atoll type has a lower interstrip capacitance and detector noise at the cost of slight charge losses.

Such double sided sensors provide two-dimensional information, which may be ambiguous in case of two or more particles traversing the sensitive area at the same time. Assumed that there is just a single hit, only one or a small group of neighboring strips, which is also called a cluster, on each side carry a signal from this event. As the strips on both sides are orthogonal, the traversing point can be extracted from the crossing of the involved channels. Fig. 2.11 illustrates the situation when two particles traverse the

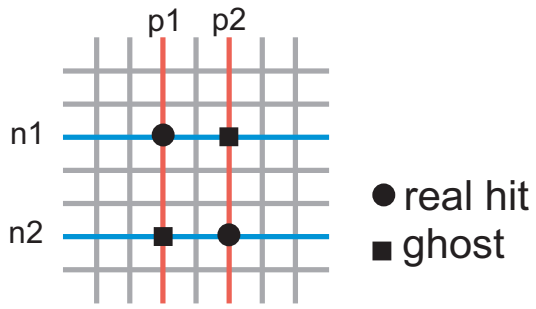

Figure 2.11.: Ambiguous hit positions in case that two particles traverse a DSSD.

detector at the same time. Then there are two real hits at positions p1/n1 and p2/n2, respectively, which lead to a signal on those four strips. Trying to reconstruct the real hits from the strip information is ambiguous: In addition to the real hit points, there are two more possible hits at the crossing of p1/n2 and p2/n1, commonly named ghosts. The true hit points have to be reconstructed by combinatorics using data from several layers of silicon detectors.

2.2.2. Pixel Detector

One electrode can be divided into square pads with a dimension of about $50 \times 50\,\mu\text{m}^2$ to achieve higher resolution and solve the ambiguity problem of DSSDs (see above). Such pads are called pixels and the charge is collected at the pixel where the particle traverses the sensor. A pixel detector provides a two dimensional hit information, even though the second electrode is manufactured as a common backplane as it is done on single sided strip detectors. The advantage of such a sensor is that it allows a very accurate determination of the hit position at the cost of a complicated structure. In contrast to strip detectors the connection beween the pixels and their corresponding amplifier inputs cannot be done by wire bonding, because the pads are distributed in a two-dimensional array and wire bonding is restricted to only one dimension. One solution is to route all pads to a single row of bonding pads on one edge of the sensor, but this is only suitable for sensors with large pixels and it reduces the signal quality. The more sophisticated method is to place the readout chip directly onto the sensor in a sandwich-like compound as shown in fig. 2.12. An advanced bonding method called bump bonding is used to connect the pixels with the input channels of the amplifier. Thereby small solder bumps, which are for instance made of Indium, are deposited onto the pads, then parts are brought together and treated thermally. This method was recently used and enhanced by the Paul Scherer Institut (PSI), Villigen, Switzerland, for the production of the CMS[2] pixel detector modules with a pixel size of $100 \times 150\mu$m. A detailed description of this technique can be found in [26, 27]. As this is a very complicated technique one may ask why the amplifier is not be integrated onto the same wafer as the sensor, because both are made of silicon? The reason is that the requirements in doping concentration, purity and operating voltage for silicon detecors and electronic circuits are quite different. However, the research on such detectors is in progress and a promising candidate is the Monolitic Active Pixel Sensor (MAPS) [28, 29]. Conventional

[2]The Compact Muon Solenoid (CMS) experiment is one of two large general-purpose particle physics detectors being built at the proton-proton Large Hadron Collider (LHC) at CERN in Switzerland.

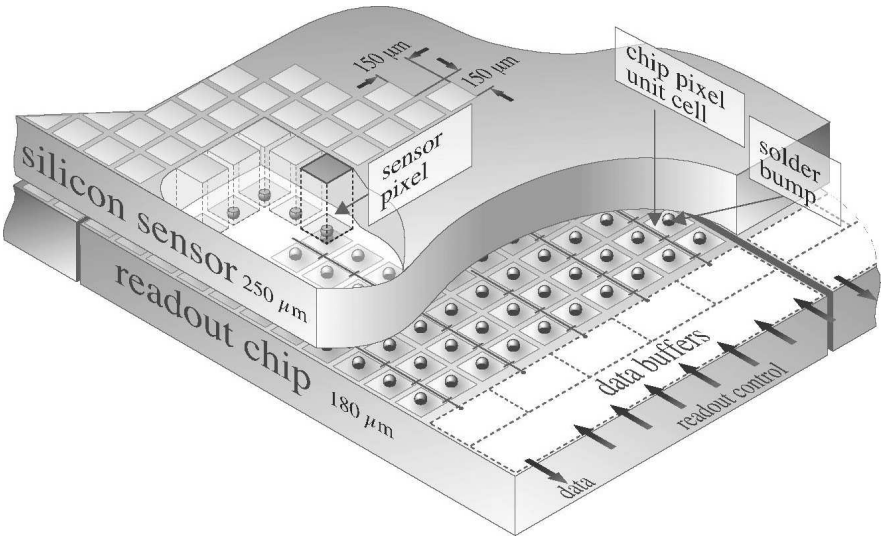

Figure 2.12.: Sketch of a pixel detector, bump-bonded onto the readout chip [25].

detectors use high-resistivity silicon as active volume which is optimized for the charge collection efficiency, but require a dedicated fabrication process. In case of the MAPS a lightly doped undepleted epitaxial layer is used for charge collection and thus those chips can be manufactured using a standard, cost-effective and easily available CMOS process, integrating the readout chip on the same wafer.

2.3. Readout Electronics

A MIP traversing a 300μm thick silicon detector produces a most probable charge of about 22500 electrons, with a pulse duration of only few nanoseconds. Thus the signal has to be amplified before it can be transmitted and processed. As readout chips with an integrating preamplifier and a CR-RC shaper are used in most present silicon detector systems, this type will be described here. The structure of a typical readout system

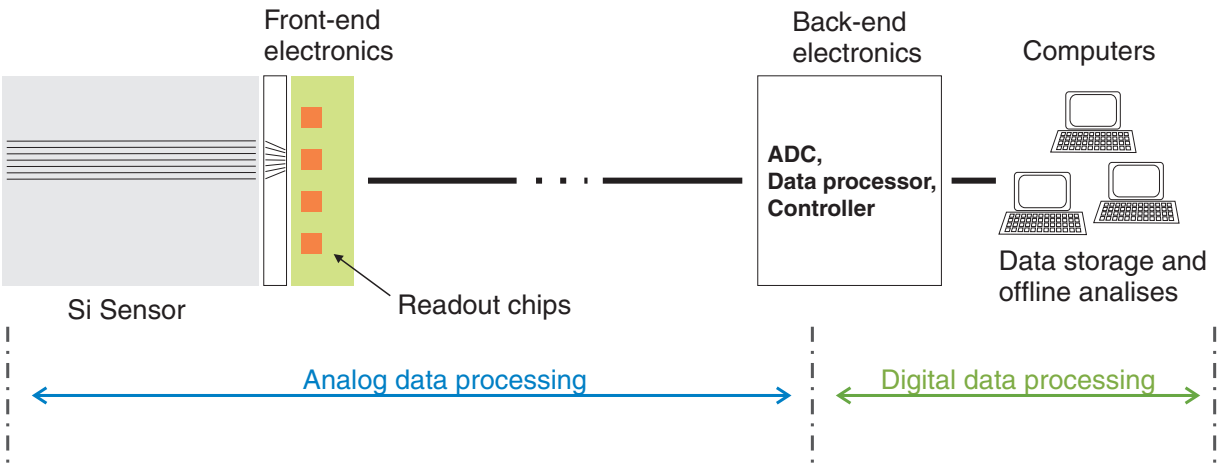

Figure 2.13.: Basic scheme of a readout system for silicon detectors.

is shown in fig. 2.13. It usually consists of a front-end and a back-end part. The first one is always situated as close as possible to the sensor to minimize noise, thus inside

the interaction region where high radiation may occur. Hence radiation hard design is required for all of its components. It commonly includes the readout chips, drivers and some control and monitoring devices, such as thermal and voltage sensors. The back-end is placed in some distance to the detector, mostly in a separate room. It is used to collect, digitize, preprocess and finally transmit the data of the readout chips to a computer or rather a computer farm where the data are stored for offline analysis. Depending on the speed and distance between those two subsystems the data transmission can either be done by conventional copper cables (with twisted pairs) or if necessary by more expensive and more sophisticated fiber optics.

2.3.1. Front-End Electronics

The most important function of the front-end electronics is to amplify the sensor signal. Nowadays, detectors with a huge number of strips are used in high energy physics experiments, therefore amplifiers with high integration are required. Most present readout chips contain 128 input amplifier channels as well as sample/hold circuits, the dedicated control logic, sometimes also an analog pipeline storage for each channel and a multiplexed output stage. In most cases the output of the readout device is an analog sequence of the sampled signal of all channels, but some types also include a digitization circuit.

As semiconductor detectors provide a current signal the input of the amplifier has to be of low resistance. The actual shape of the current pulse depends on the applied bias voltage and is impossible to measure directly at room temperature due to noise. Anyway, it is more convenient to measure the integrated current which corresponds to the collected charge. Hence, the first stage of the amplifier is implemented as an integrator, followed by a special filter (shaper) in the second stage to reduce the noise and form the pulse to a defined shape. Fig. 2.14 shows the scheme of such an amplifier

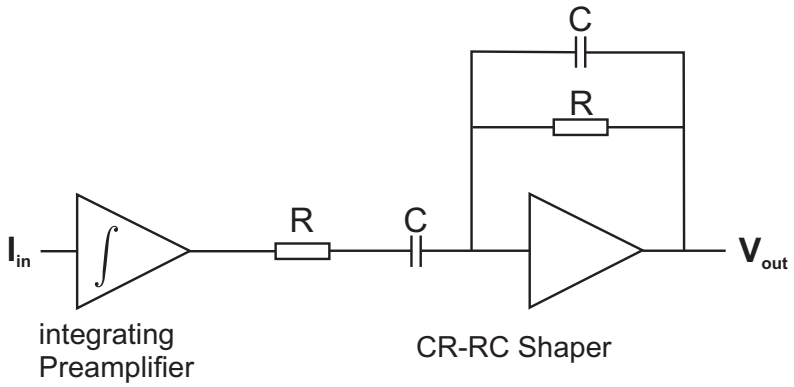

Figure 2.14.: Typical amplifier scheme for silicon detector readout with a integrating preamplifier followed by a CR-RC shaper.

composed of a integrating preamplifier together with a CR-RC shaper, named after the components arranged around the amplifier. The basic function of the shaper is a combination of a high-pass and a low-pass filter which leads to a semi-Gaussian output signal. When equal resistors and capacitances are used the system has only one time constant $T_p = RC$. In that case the transfer function in the Laplace domain is given by

$$\frac{V_{out}(s)}{I_{in}(s)} = \frac{AT_p}{(1+sT_p)^2} \tag{2.19}$$

with the factor A determined by the preamplifier. T_p is called shaping time which extends from 25 ns to 10 μs, depending on the application. Since the current pulse of a silicon detector is always much shorter than T_p it can be approximated by a Dirac-δ pulse weighted with the collected charge Q_c. Using eq. 2.19 the amplifier response to such an input signal in the time domain is

$$v_{out}(t) = AQ_c \frac{t}{T_p} \mathrm{e}^{-\frac{\mathrm{t}}{\mathrm{T_p}}} \quad . \tag{2.20}$$

In fig. 2.15 the shaper output voltage resulting from a Dirac-δ pulse is compared to the one obtained by a simulation of the actual silicon detector signal (see fig. 2.7) [22]. Because the absolute voltage depends on the gain of the preamplifier both curves are normalized to the peak voltage V_{peak} of the Dirac-δ answer. One noticeable difference between the two curves is that the Dirac-δ answer reaches its maximum at $t = T_p$, also called "peaking time", while the signal coming from the sensor simulation is slightly delayed.

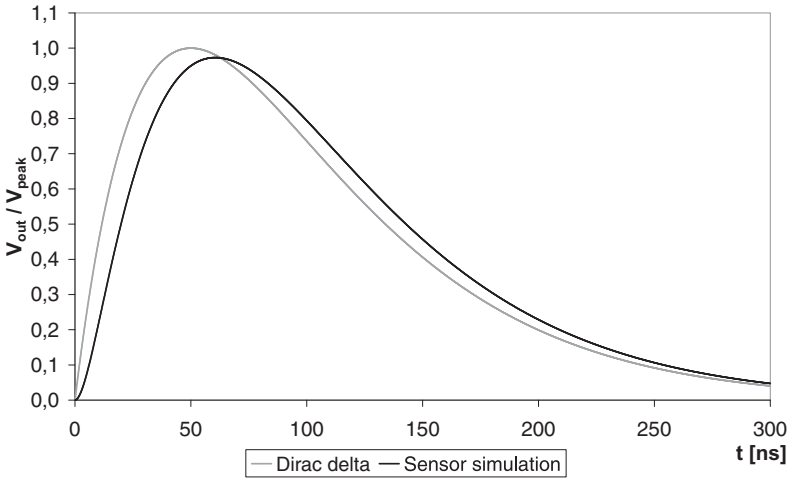

Figure 2.15.: Shaper output ($\mathrm{T_p}$ = 50ns) with a signal coming from a silicon detector (simulation) and a ideal Dirac-δ pulse [18].

2.3.2. Back-End Electronics

The back-end electronics is the second stage in the data processing chain of the detector readout system. Its primary purpose is to collect and (pre)process the data of the front-end units before they are sent to the final storage devices, but it also has to take care of the required control signals such as clock and trigger to ensure a synchronized readout of the amplifiers. In practice the silicon sensor is only one part of a High Energy Physics experiment, thus the back-end also needs interfaces to the global control and trigger systems.

Since the readout chips usually provide an analog output signal the back-end system includes one analog to digital converter (ADC) per readout chip. It further contains several amplifiers, FIFO[3] buffers and control electronics. Concerning the data flow,

[3]FIFO is the abbreviation for first-in, first-out and describes the principle of a queue behavior. Data are always read from the output of a FIFO buffer in same order as they were written into its input before.

the back-end is the boundary between analog and digital data processing. State of the art back-end systems often contain programmable logical devices (FPGA[4]) which make them suitable to implement some advanced processing features like data compression and correction procedures. Furthermore, FPGAs have the advantage that it is possible to implement the same logic circuit many times with a minimum need of hardware and space. Thus, the data stream of many input channels can be handled in parallel, which is very important to ensure fast online data processing. The output of the back-end is then transmitted to a computer farm where high level processing is done before the data are stored for off line analyses.

2.4. Noise

Considering the noise is very essential in silicon strip detector applications since the signal is very low. Even though every electronic component in the data processing chain contributes to the total noise, the detector itself and the input transistor of the preamplifier are the most critical sources. The electronic noise of a silicon sensor systems is commonly given in terms of equivalent noise charge (ENC) referred to the amplifier input and thus directly related to the measured signal charge.

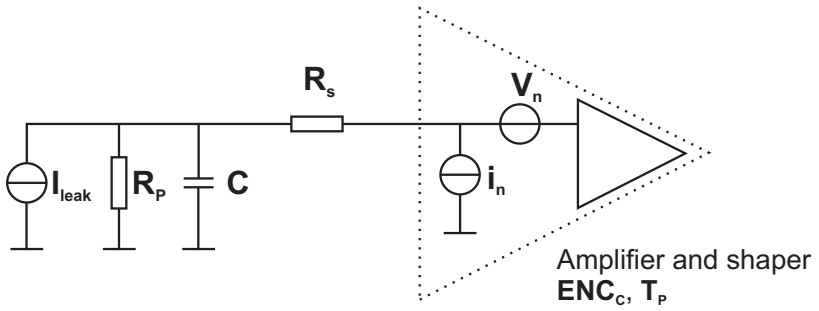

Figure 2.16.: Noise sources of a silicon stip sensor and its amlifier.

Fig. 2.16 displays all noise related components of a typical AC coupled silicon detector configuration with a polysilicon bias resistor. In this scheme the noise sources of the sensor are the fraction of the sensor's leakage current seen by one strip I_{leak}, the bias resistance R_p and the line resistance of the strip R_s. The influence of the AC coupling capacitance can be neglected. In a system with an integrating amplifier followed by a CR-RC shaper as it is described in section 2.3.1, the noise contributions of the sensor can be expressed by

$$\mathrm{ENC_{Ileak}} = \frac{e}{2}\sqrt{\frac{I_{leak}\,T_p}{q_e}} \quad , \tag{2.21}$$

$$\mathrm{ENC_{Rp}} = \frac{e}{q_e}\sqrt{\frac{kT\,T_p}{2R_P}} \quad \text{and} \tag{2.22}$$

$$\mathrm{ENC_{Rs}} = \frac{e}{q_e}\,C\sqrt{\frac{kT\,R_s}{6\,T_P}} \tag{2.23}$$

[4]A field-programmable gate array (FPGA) is a semiconductor device containing programmable logic components (logic blocks) and programmable interconnects. They allow to implement complex logical combinations. Many types also includes predefined memory blocks and advanced logic elements.

with ENC the number of electrons, the elementary charge q_e, the Euler number e, the Boltzmann constant k and the integration time T_p [30, 31]. The equations show that $\mathrm{ENC_{Ileak}}$ and $\mathrm{ENC_{Rp}}$ rise with increasing peaking time while $\mathrm{ENC_{Rs}}$ behaves opposite.

However, the most important noise source is the input stage of the amplifier, which can be modeled by a voltage source in series and a current source in parallel to the input as shown in fig. 2.16. Due to the integrating preamplifier the parallel noise current i_n results in a constant value while the voltage source leads to a noise charge which increases with the capacitive load C of the input.

$$\mathrm{ENC_C} = a + bC \quad , \tag{2.24}$$

Both a and b are parameters of the used amplifier and depend on its implementation. C represents the sum of the capacitive load present at the amplifier input. Often, the sensor is the dominant capacitive contribution, but sometimes long pitch adaptors or bond wires have to be considered, too, adding up to the total capacitance as seen by the amplifier.

As all contributions can be considered statistically independent and thus uncorrelated, the total noise is given by the square sum of them.

$$\mathrm{ENC} = \sqrt{\mathrm{ENC_{Ileak}^2} + \mathrm{ENC_{Rs}^2} + \mathrm{ENC_{Rp}^2} + \mathrm{ENC_C^2}} \tag{2.25}$$

To give an example for the order of magnitude of individual noise components they are calculated for the future Belle detector in combination with the APV25 readout chip as amplifier, which will be described later in section 5.1. In tab. 2.1 the basic parameters of the DSSD are listed for both p-side and n-side. The resulting noise contributions are shown in tab. 2.2. It can clearly be seen that the amplifier chip is the dominant noise source for both sides of the detector.

Belle SVD3 sensor		**p-side**	**n-side**
strip width	[μm]	10	24
strip length	[mm]	77.7	25.6
pitch	[μm]	51	152
C	[pF]	15.1	5.1
$\mathrm{R_S}$	[Ω]	110	15
$\mathrm{R_P}$	[MΩ]	10	10
$\mathrm{I_{leak}}$	[nA]	0.86	0.86

Table 2.1.: Sensor parameters of the future Belle DSSD for both sides of the sensor.

On the p-side the line resistance R_s, which primarily depends on the length and the width of the strip metalization, is also a significant noise source. In comparison to the n-side the strips on the p-side are three times longer and only half as wide due to the narrow pitch. This results in a $\mathrm{ENC_{RS}}$ which is considerably higher than the contributions of the other sources but still negligible compared to the noise caused by the amplifier input.

Noise		**p-side**	**n-side**
$\mathrm{ENC_C}$	[e]	792	435
$\mathrm{ENC_{RS}}$	[e]	163	60
$\mathrm{ENC_{RP}}$	[e]	54	54
$\mathrm{ENC_{Ileak}}$	[e]	22	22
$\mathrm{ENC_{total}}$	[e]	811	443

APV25: $\mathrm{ENC_C} = 250 + 36\mathrm{C}$

Table 2.2.: Noise values resulting from the sensor parameters given in tab. 2.1 using the APV25 amplifier. The total noise in the bottom row is calculated using eq. 2.25.

3. Belle Silicon Vertex Detector

3.1. History

The initial version 1 of the Belle silicon vertex detector (SVD1) was installed in 1999 and was used for four years. It was composed of three cylindrical layers of 102 DSSDs in total and had a polar angle coverage of $23° < \theta < 138°$. The radii of the three layers were 30, 45.5 and 60.5 mm. Each layer was constructed from 8, 10 and 14 independent ladders with two, three and four DSSDs for the first, second and third layers, respectively. The sensors were manufactured by Hamamamatsu Photonics and had a sensitive area of 57.5×33.5 mm^2, a thickness of 300 μm and a pitch of 50 μm in r-ϕ and 84 μm in z direction [32]. There were 640 strips on each side which were read out by VA1 front-end chips produced by IDE AS, Norway. This chip was manufactured in a 1.2 μm CMOS process and featured a limited radiation tolerance of about 200 krad. Since the actual radiation dose was higher than expected in the design stage, parts of the SVD1 and its readout chips had to be replaced repeatedly.

Another problem was the long dead time of about 128 μs during the readout of the VA1 chips, because they were arranged in groups of five daisy-chained chips and read out serially using a single readout line.

Moreover the sensor bias voltage was separated from the grounded front-end electronics by the AC coupling capacitance of the sensor. This led to the loss of some ladders due to shorts created by pinholes on the sensor which broke down the AC coupling and caused the bias voltage being applied to the VA1 chip.

3.2. Current State

The SVD in operation is the SVD2, an improved design that addresses all the issues of SVD1. Its installation was in summer 2003 and since then it has been working without any serious problems. Not only the electrical components were upgraded, also the mechanical structure was revised to achieve a better vertex resolution and tracking efficiency.

3.2.1. Silicon Sensors

The SVD2 consists of 246 DSSDs arranged in four layers, read out by VA1TA chips (see 3.2.2), which permit an operation to at least 20 Mrad. Furthermore, the power scheme of the front-end chips was replaced by a floating one, where the VA1TA low voltage potential sits on the top of the bias voltage levels of the sensor connected with them. The voltage decoupling between front-end and back-end electronics and the translation of the signals are now performed by subsequent optocouplers. In this configuration only negligible current can flow into the input of the readout chip in case of a pinhole on the sensor. However this current is some order of magnitude higher than the signal

from the particle and thus causes the saturation the affected channel but not the loss of the whole chip as it was the fact in SVD1. Moreover, each VA1TA chip is now read out individually, thus the readout dead time has been reduced to 26 μs.

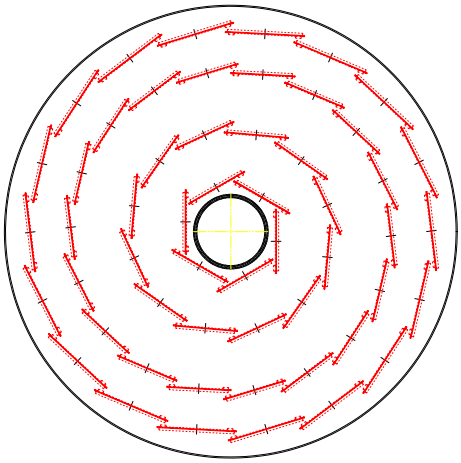

Figure 3.1.: SVD2, r-ϕ view.

As depicted in fig. 3.1, the four layers of the SVD2 are made up of 6, 12, 18 and 18 ladders, from the first to the fourth layer. Each of these ladders consists of 2, 3, 5 and 6 DSSDs, respectively, glued onto a mechanical support structure. The sensor used for the layers one to three has an area of 76.8 $\times$ 25.6 mm^2 with 512 readout strips on each side and a readout pitch of 50 μm in r-ϕ and 150 μm in z direction. That of the fourth layer has an area of 73.8 $\times$ 33.3 mm^2 and a readout pitch of 65 μm and 146 μm for r-ϕ and z, respectively, and also 512 readout strips per side. In z direction there is an intermediate strip between two neighboring readout channels for both sensor types.

The radius of the innermost layer is 20 mm and thus smaller than that of SVD1 (30 mm), while that of the outermost one is 88 mm.

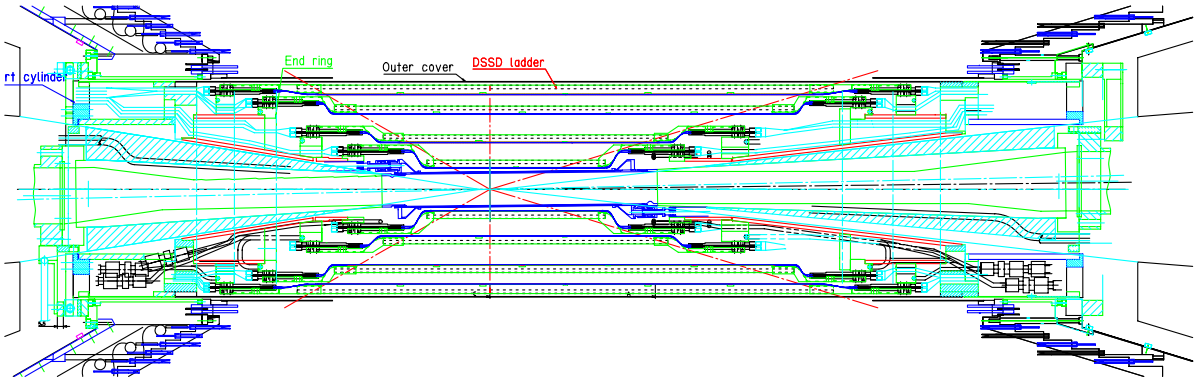

Figure 3.2.: Side view of the SVD2.

The SVD2 covers a polar angle of $17° < \theta < 150°$ which now matches the acceptance of the surrounding CDC (see 1.3.2) and the other subdetectors. A side view of the SVD structure is shown in fig. 3.2. All the modifications of the mechanical structure were intended to improve the vertex resolution of the system [32, 33].

On both ends of the ladders, printed circuit boards (hybrids), each equipped with four VA1TA chips, are mounted to read out the 512 strips of one side of the sensors.

In the innermost layer each DSSD is connected to one such board per side, while in the layers two, three and four the strips of up to three sensors are ganged and read out together by only one hybrid. This is done to minimize the material budget inside the active volume and maximize the resolution of the SVD. The drawback of this method is that it results in ambiguous data in z direction, which has to be resolved by tracking software. Fig. 3.3 shows the four different ladder types used in SVD2. The strips of

Figure 3.3.: SVD2 ladders of all four layers.

the r-ϕ coordinate are ganged by wire bonds, while for the orthogonal z coordinate a flexible printed circuit (FCP) with a 50 μm pitch is glued onto the surface of the sensors, providing the interconnections between adjacent sensors and wire bonds. In SVD1 detectors with a double metal layer (DML) structure were used instead. Such DSSDs have an additional layer where the strips are routed to the orthogonal edge of the sensor. The advantage of using the FCP is that its distance to the strips is much larger than that of a DML structure and thus its capacitance and hence the noise is significantly lower at the cost of a more complex mechanical design and a small increase of material budget.

3.2.2. VA1TA

The VA1TA [34] is a readout chip with 128 channels of low-noise preamplifier and CR-RC shaping circuits, simultaneous sample-hold and a multiplexed analog differential output as well as some calibration and trigger facilities. It is manufactured in a 0.35 μm N-well CMOS process, which permits operation up to a radiation dose of 20 Mrad (= 200 kGy). The chip is about 9.28 mm x 6.12 mm large and 725 μm thick.

In addition to the analog amplifier part (VA) the chip also contains a trigger part (TA) for each channel. This is implemented by a second fast shaper stage followed by an adjustable threshold comparator. All of these comparator outputs are ORed together and present a chip level trigger signal. A block diagram of the VA1TA with the circuit of one channel of both the VA and TA part is given in fig. 3.4. The key parameters of the readout chip are listed in tab. 3.1.

The peaking time (T_p) of the standard shaper can be adjusted between 300 ns and 1 μs, while that of the fast shaper can be switched between 75 ns and 300 ns. All shaper outputs of the analog part are passed through a one stage multiplexer to a

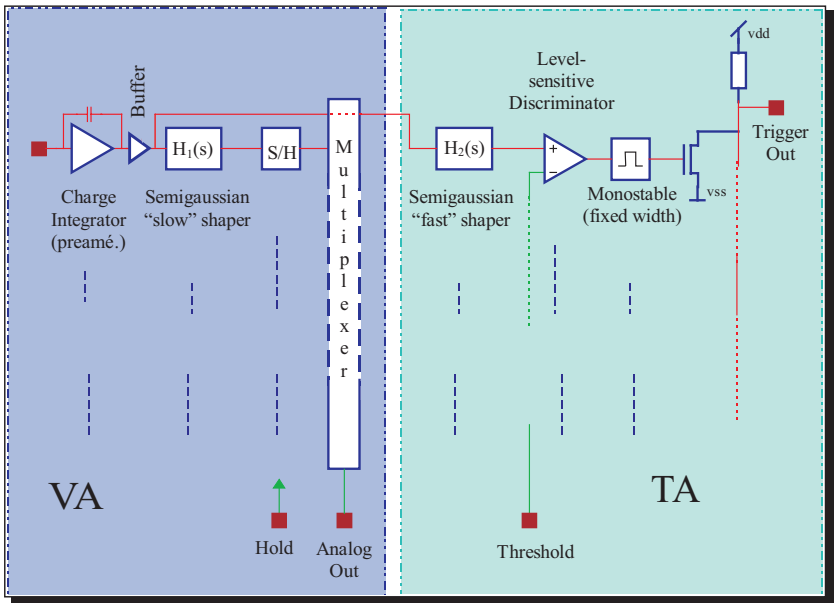

Figure 3.4.: VA1TA block diagram. [34]

Amplifier:	Charge sensitive pre-amplifier with CR-RC shaper stage.
Input channels:	128
Supply Voltages:	$V_{dd} = +1.5V$ $V_{ss} = -2.0V$
Power dissipation:	195 mW (nominal)
Peaking time:	Slow shaper: 0.3 μs - 1 μs Fast shaper: 75 ns/300 ns (switchable)
Output:	analog differential current output
Readout:	10 MHz max. serial, multiplexed, controlled via shift register
Noise:	$ENC_C = 180 + 7.5C\ e^-$ rms (at $T_p = 1\mu s$)
Chip size:	9.28×6.12 mm^2, 725 μm thick
Manufacturing process:	0.35 μm N-well CMOS
Radiation tolerance:	up to 20 Mrad

Table 3.1.: VA1TA parameters.

single differential, analog output. The differential current gain of this output is about 10 μA/fC, but depends on the configuration of the integrated bias generators. A serial bit register is used to control the multiplexer and thus only one channel can be connected to the output at any time.

A typical readout cycle and the signal of the shaper output are depicted in fig. 3.5. As long as the input *holdb* is held at high level each channel integrates its incoming signal (sample mode). T_p after a physics event was triggered *holdb* is set to low which stops the sampling of all channel (hold mode) and the current values of the shapers can be read out sequentially. The input *shift_in_b* of the bit register is set to low for one cycle of the readout clock *ckb*, which switches the first channel to the analog output. Then *ckb* is pulsed 128 times to read out all the other channels consecutively. The chip supports a maximum readout clock frequency of 10 MHz, but a readout clock of 5 Mhz was chosen

for the SVD2.

When the last channel was read out the output *shift_out_b* is set to low for one cycle of *ckb*. This signal can be used to cascade several chips by connecting *shift_out_b* from one chip to *shift_in_b* of the next one, which allows to read out these chips sequentially. Since the output of the VA1TA provides a current signal, several chips can be connected in parallel in that case.

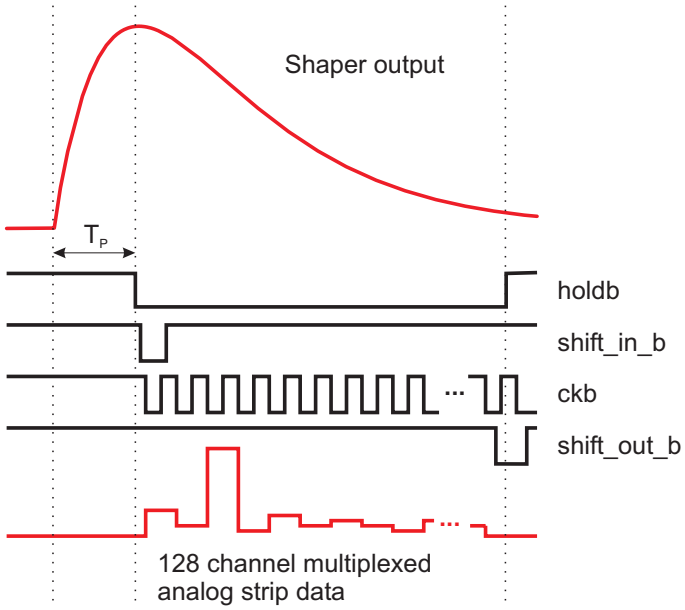

Figure 3.5.: VA1TA shaper signal and readout cycle.

Furthermore, the chip contains several bias generators and configuration facilities to adjust the peaking time and shape of both the VA and TA shapers as well as the threshold of the discriminators in the trigger part. All adjustable parameters of these facilities are defined by the control register which consists of a 680 bits long shift register. A detailed description of these parameters can be found in [34].

The VA1TA also provides a test or calibration mode. Therefore the chip contains a second bit register controlled multiplexer at the input of the analog amplifiers, connecting one channel to the *cal* pad.

With this facility it is possible to apply a defined voltage step via a small capacitance into each channel of the chip and measure the output of its shaper. This allows to check the functionality of the selected channel. The injected charge of this test pulse is determined by

$$\Delta Q = C\Delta V \tag{3.1}$$

and leads to 3.6 fC or 22500 e^- (= 1 MIP) when 2 mV voltage step is applied onto a 1.8 pF capacitor.

3.2.3. Readout System

As mentioned already, the VA1TA chips are placed on small printed circuits located at the end of the ladders. The next stage in the readout chain are repeater boards (REBO) which are located in about 2 m distance to the SVD. These boards are used to control the readout of the front-end chips and provide all necessary signals as well

as the power supply. Furthermore they perform the level shifting of the analog signals which are on the floating DC power levels of the VA1TA chips. The analog output data and the trigger information of the TA part are transmitted to the back-end Fast ADC with Trigger Facilities (FADCTF) board [35, 36] located in the electronics hut. The same shielded twisted pair cables with a length of 30 m are shared by both signals. The trigger information is disabled during the analog data readout to avoid any potential interferences. On the FADCTF boards, the analog data are digitized, buffered and finally passed on to Linux PCs through fast parallel data links for data processing. The distribution of clock, trigger and status signals for both the front-end and and the back-end electronics is done by the Trigger Timing Module (TTM). A block diagram of the SVD2 readout system is shown in fig. 3.6.

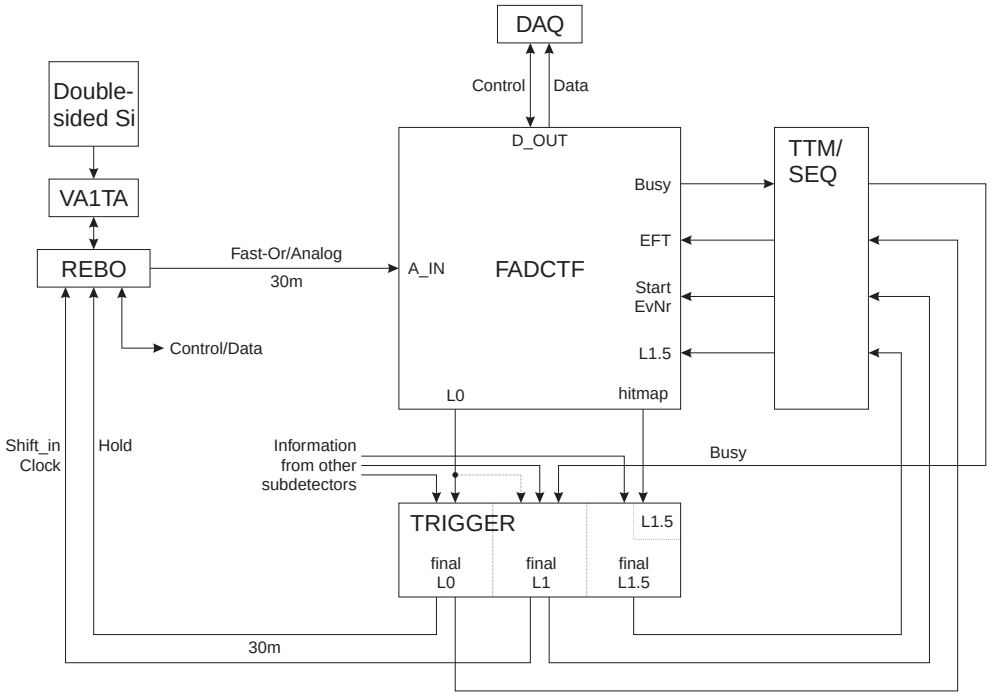

Figure 3.6.: Block diagram of the SVD2 readout and trigger chain [35].

The FADCTF system consists of a total of 36 VME [1] (9U size) boards with 24 analog input channels each, located in two crates, one for r-ϕ and z, respectively. The whole logic is programmed into several FPGAs with the possibility to alter their firmware via the VME interface to offer fast and flexible data processing. The digitization of the analog input signals is done with 10-bit ADCs operated at 20 MHz. Since the VA1TA readout speed is 5 MHz only every fourth sample is passed on. However, the faster sampling is used in a test mode where the full pulse shape of a dedicated channel is transfered rather than multiplexed peak values.

The readout is controlled through various hardware trigger levels. In idle mode the inputs of the FADCTF boards are watched for signals of the TA part of the front-end

[1] The Versa Module Eurocard (VME) bus is an asynchronous computer bus used in process control applications. The original version was standardized by ANSI and IEEE as ANSI/IEEE 1014-1987 providing a framework for 8-, 16- and 32-bit parallel-bus systems. In 1994, VME64 was formally approved by ANSI as ANSI/VITA 1-1994, incorporating all the features of VME32 and adding support for 64-bit transfers.

chips. This information is then passed on to the global trigger logic which also gets data from the CDC and the TOF subsystems to make a level 0 (L0) trigger decision within 800 ns after a physics event. In case of a positive L0 decision the Hold signal is sent to the VA1TA chips and the signal of each channel is sampled at the peak of its shaping curve. The signals are stored in the front-end chips until a L1 trigger decision, which is again built using data of the CDC and TOF, initiates the readout by the FADCTF system. Otherwise the Sample/Hold is released and thus the sampled data are discarded. The signals are then digitized and stored in a FIFO of the FADCTF units, which can buffer up to four events, awaiting a higher level trigger (L1.5 trigger). Upon reception of a L1.5 decision, the stored data are transfered to the next buffer stage called "final memory" from where they are sent to the Linux PC farm via a custom interface card for further processing. In case no L1.5 trigger is received the data are overwritten by the next event and thus discarded.

3.3. Limitations of the SVD2

Since the installation in 2003 the SVD2 has been working without any serious trouble and the collected data brought fruitful physics results. However, improvements of the accelerator led to an increased luminosity (eq. 1.2), which reached a peak value of $1.712 \cdot 10^{34}$ cm^{-2}s^{-1} on 15$^{\text{th}}$ November 2006 and it shall be continuously boosted the in future. It is planed to increase the luminosity up to $5 \cdot 10^{35}$ cm^{-2}s^{-1} aiming to search for physics beyond the SM in rare B decays.

As a consequence of such a high luminosity it is estimated that the background, mainly caused by off-time particles and synchrotron radiation (SR), will be 20 times higher than now. Furthermore an increase of the level one trigger rate from 450 Hz to 10 kHz in average with a maximum of 30 kHz is expected. Neither can be handled by the SVD without any improvements. On one hand the higher background causes an equivalent increase of the occupancy (see below) of the silicon detectors. On the other hand the possible trigger rate is limited by the dead time and the speed of readout electronics.

3.3.1. Occupancy

At Belle the reconstruction of the particle trajectories is done by extrapolating the tracks found by the outer subdetectors, such as the CDC, inwards to the SVD. Tue do the magnetic field inside the detector, the tracks of charged particles are helically. The hit finding efficiency describes how precise hits of an SVD layer match those extrapolated tracks.

To find the best approximation of a track, fitting is done in the vicinity of a reference point, called pivotal point $\mathbf{x}_0 = (x_0, y_0, z_0)^T$. A set of five parameters $\mathbf{a} = (d_\rho, \phi_0, \kappa, d_z, \tan\lambda)^T$ is used for track fitting by the Belle data analysis [37], where d_ρ is the signed distance of the helix from the pivot in x-y plane, ϕ_0 is the azimuthal angle[2] to specify the pivot with respect to the helix center, κ is the reciprocal of the transverse momentum $(1/P_t)$ and its sign represents the charge of the track assigned by the track fitting, d_z is the signed distance of the helix from the pivot in the z direction and $\tan\lambda$ is the slope of the track. The parameters of that point on the helix that is nearest to

[2] ϕ_0 ranges from 0 to 2π at Belle

the pivot are called impact parameters (IP) and the precision of their measured values is the IP resolution.

Although the SVD is the innermost subdetector of Belle, it is not possible to measure the vertices of the B meson decays directly, because the lifetime of B^0 mesons, as an example, is only about 1.5 ps and thus they decay inside the beam pipe. However, using the data of their decay products measured by the silicon detectors and the track information got from the outer systems it is possible to determine the vertices by extrapolating the helices of the fitted tracks. The quality of these reconstructed tracks strongly depends on the IP resolution, hence it is an important characteristic of the detector performance. Thus the resolution of the measured distance Δz between the two B^0 decays, the vertex resolution, is also related to the IP resolution.

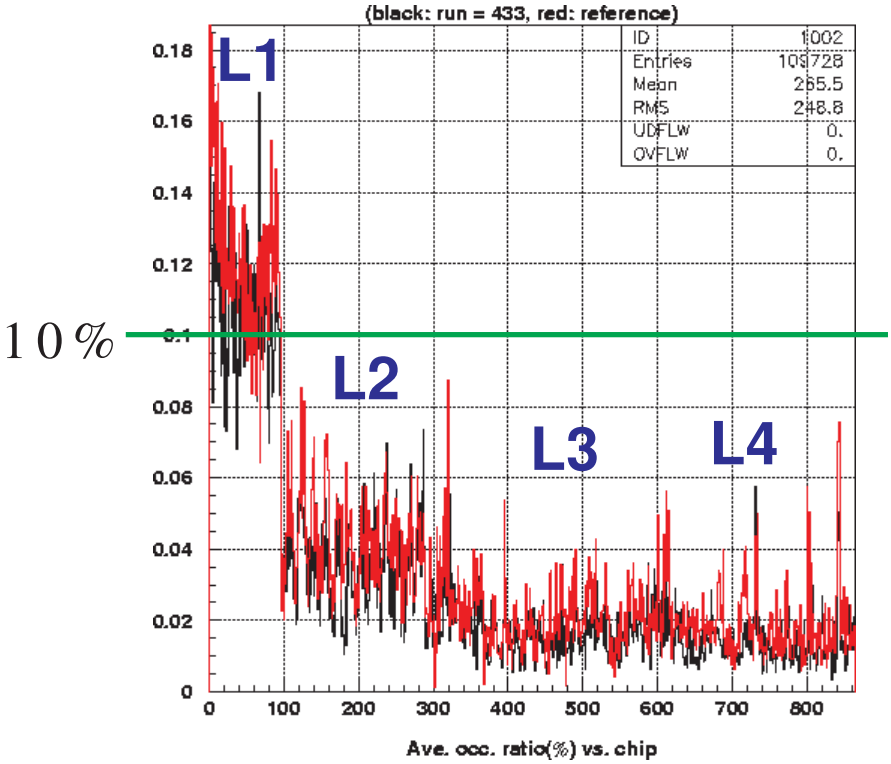

Figure 3.7.: Occupancy of all four layers of the SVD2. The average occupancy of the innermost layer L1 is about 10% and therefore significantly higher then that of the other layers.

The occupancy of a silicon detector is defined by

$$O = \frac{N_h}{N} \tag{3.2}$$

where N_h is the number of hit channels at any random moment and N is the total number of strips. Fig. 3.7 shows the current occupancy per layer of the SVD. For the innermost layer it is about 10%, while that of layers two to four is 4%, 2% and 2%, respectively. Studies have shown that the occupancy has an important influence on the hit finding efficiency and the impact parameter (IP) resolution of the SVD [33]. To show the effects of a three times higher background level, the performance of the SVD was analyzed in these studies at the condition of up to 30% occupancy for the first layer. Fig. 3.8 (a) shows the IP resolution in $r\phi$ direction using data from muon pair events

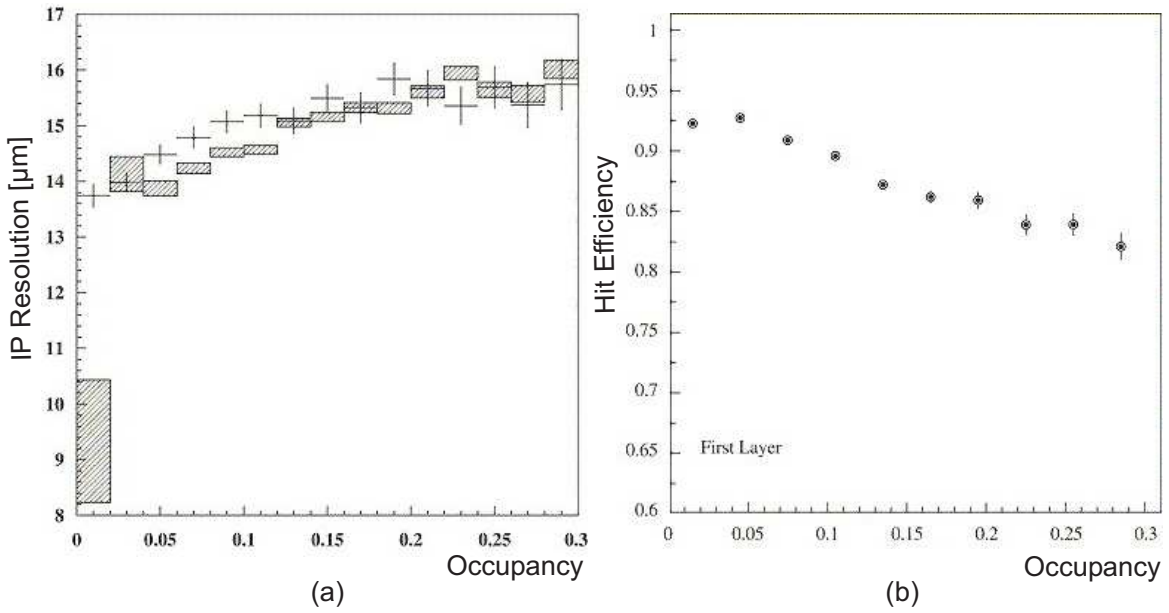

Figure 3.8.: IP resolution in $r\phi$ (b) and hit finding efficiency (a) as a function of the occupancy using μ pairs. In fig. (b) crosses indicate collision data, while boxes are from a Monte Carlo simulation. [33]

as a function of the occupancy of the layer one, compared to the results of a Monte Carlo simulation. In Fig. 3.8 (b) the hit finding efficiency as a function of the occupancy is depicted. At low occupancies the efficiency is limited by hardware defects like noisy sensor strips or bad wire bonds.

For both, the IP resolution as well as the hit finding efficiency, a considerable degradation at an occupancy of 30% is evident, which is about 15% and 10%, respectively. Furthermore, the vertex resolution for $J/\Psi K_s$ events at tripled background is estimated to be about 104 μm. Compared to the current value of 86 μm at 10% occupancy this is a worsening of 21%. There are two reasons for the degradation at high occupancies. Due to overlapping of background signals and the particle hits the clusters becomes wider and the determined hit position is displaced. Moreover, background signals are wrongly interpreted as hits and associated to particle tracks. A Δz resolution better than 100 μm is required to ensure a proper vertex reconstruction, which demands an occupancy of less than 10% [38].

However, the estimated background at Super Belle will be 20 times higher than now. Thus, a significant occupancy reduction is required to cope with the high background level of the future SVD.

Two parameters of a silicon strip sensor system directly affect the occupancy. One is the sensitive area of the sensors strips, given by their width and their length, because the probability that a strip is hit by two or more particles scales with its dimensions. The second parameter is the sensitive time window of the readout chip, which is defined by the duration that the shaper output signal is above a given threshold, hence the peaking time of the chip. The occupancy increases with this period, since the likelihood that the output is above the threshold due to a previous background hit is higher for longer shaping times.

Methods aiming at the reduction of the occupancy in silicon strip detector systems using both a geometrical and a time approach are discussed in chapter 4. Their efficiency

was tested with prototype DSSD modules in several beam test and the corresponding results are presented in section 7.

3.3.2. Dead Time

As mentioned before the trigger rate is currently about 450 Hz and it is estimated that it will be about 30 kHz when the luminosity will be increased to $5 \cdot 10^{35}$ $\mathrm{cm}^{-2}\mathrm{s}^{-1}$. Assuming that triggers arrive periodically at 450 Hz, the duration between two triggers is 2.2 ms. In reality, the trigger rate is not constant and the given trigger rate is just its mean value. However, using the mean is precise enough for the following discussion concerning the dead time problem.

The readout of all 128 channels of one VA1TA chip takes 25.6 μs at 5 MHz readout clock. Due to, the input signals are not sampled during the readout of the VA chips, triggers within these 25.6 μs can not be processed. That means the percentage of dead time of the front-end chips as a rate of the trigger period is currently about 1.15%. When the trigger rate becomes 30 kHz this value will rise up to 77%, thus the VA1TA chip is not suitable for such a high number of triggers. Even when the readout clock will be doubled (the VA chips can be read out with up to 10 MHz) the dead time then will be about 38%, which is still to much.

The only solution is to replace the VA1TA chips by ones with an integrated pipeline attached to the shapers output, which allows continuous sampling of the input signals, even during the readout cycle. This was one reason to choose the APV25 chip (see 5.1) as a possible candidate to be used as front-end chip for the future Belle SVD.

However, the dead time of the whole SVD readout system is not only caused by the VA1TA chip. The adjacent electronics also suffers under an increasing trigger rate and will not be fast enough in future. These units have to be accelerated together with the front-end chips to match the requirements of the proposed high luminosity.

4. Occupancy Reduction

Some ideas will be presented in this chapter aiming to solve the problems of the SVD2, which were discussed in 3.3. The main focus is given on the increasing occupancy with the goal to implement the proposed solutions into a prototype and validate them within beam tests. However, all introduced methods are based on the usage of a new and faster front-end chip, thus also require a redesign of the readout electronics. Therefore, the dead time problem will be solved automatically as long as the expected trigger rate is considered for the choice of the used front-end chip and the design of the new readout electronics.

In order to achieve a reduction of the occupancy either a geometrical approach by reducing the sensitive strip area per channel or a temporal one by shortening the sensitive time window of the front-end chip can be followed. Below, three methods, namely the "shaping time reduction", the "hit time reconstruction" and a new sensor layout are discussed. These techniques actually can, but not necessarily need to be used together. If they are used in combination, then their occupancy reducing effects will be multiplied.

4.1. Shaping Time Reduction

The shaping curve of the front-end chips follows an exponential function as defined in eq. 2.20. The main parameter of the function is the peaking time T_p , defining the time from the particle hit until the signal shape rises to its maximum. However, the curve is also characterized by a long tail, which can be more than two times T_p long.

Usually the shaper output is sampled T_p after a particle traverses the sensor to achieve the maximum signal. Due to the background not all particles crossing the sensor are of interest, only some of them are part of the physics event. Commonly, only one sample of the pulse is taken and each channel having a signal above a threshold at trigger time is accepted as a hit. As a result of the long tail also channels carrying a signal from a background hit previous to the triggered event are wrongly accepted as event hits, because their signal may be still above the threshold at the sampling time. This finally leads to a higher occupancy caused by the background.

The sensitive time window of the front-end chip is given by the period during that the shaper output is above a threshold and is primarily determined by the peaking time. In fig. 4.1 the shaper output signal of the VA1TA chip, with $T_p = 800$ ns, is compared to that of the APV25 (see 5.1), a chip providing a shorter peaking time of 50 ns. For both, a channel carrying the signal from the event hit (solid line) and from an earlier hit (dashed line) is depicted. The green, dashed line is the threshold above which signals are accepted as hits. By measurement the sensitive window was obtained to be about 2000 ns for the VA1TA and 160 ns for the APV25, respectively. For both chips the curve is sampled T_p after the physics event happened (T_0). This is at T_1 for the VA1TA and T_1' for the APV25. The sampled pulse heights are marked with red arrows.

It can be clearly seen that the signal of the off-time hit is still above the threshold

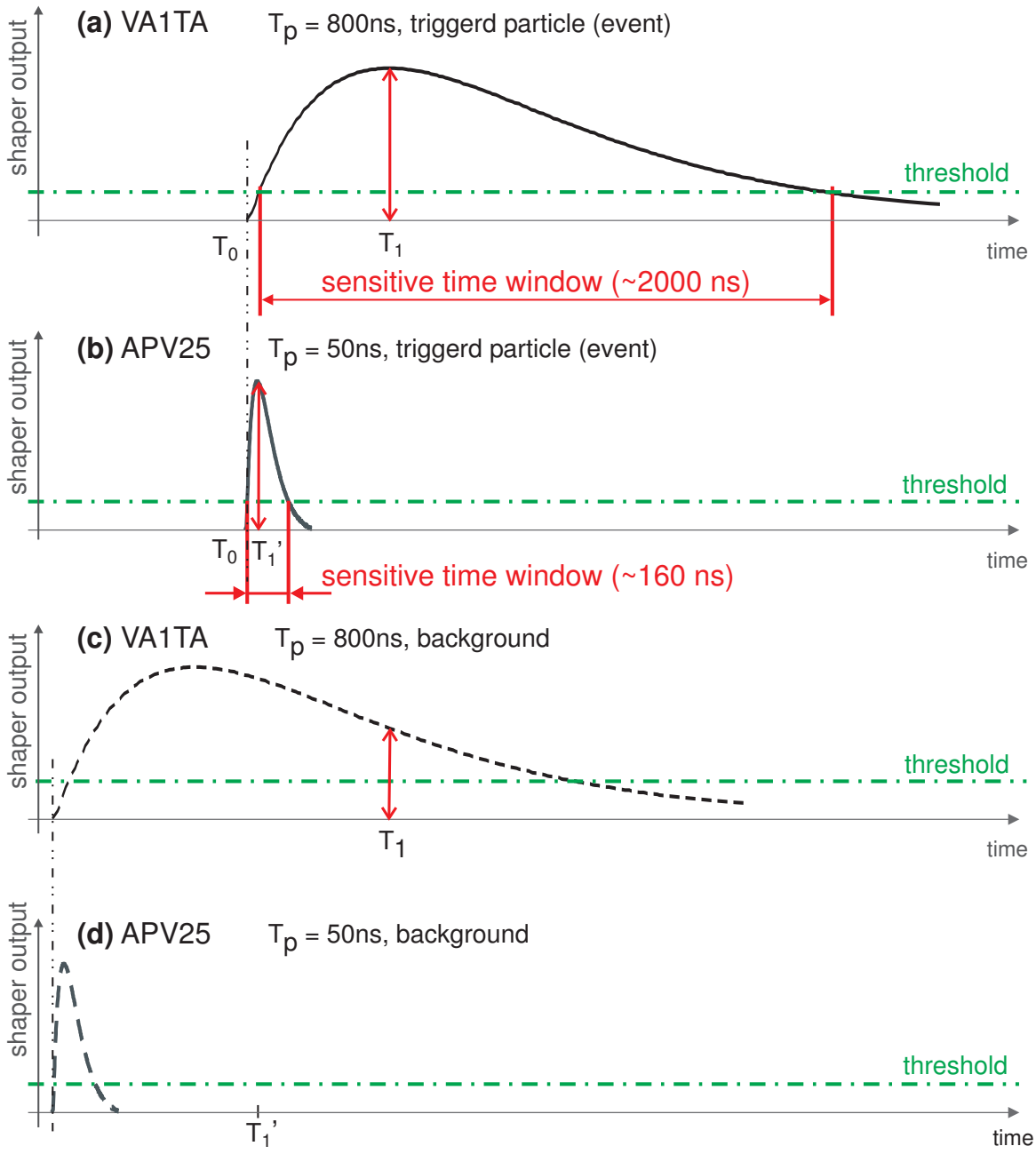

Figure 4.1.: Comparison of the shaper output of the VA1TA and the APV25, where the signals are drawn for a triggered particle (solid curve) and a background particle (dashed curve). The physics event happens at T_0. The data are taken at T_1 and T_1', for the VA1TA (a) and the APV25 (b), respectively. Due to the long tail the earlier background signal is still above the threshold at T_1 in case of the VA1TA (c), thus wrongly accepted as hit, which is not the case with the APV25 (d).

at T_1 in case of the VA1TA chip but not for the APV25 thanks to its shorter T_p. Hence, by shortening the sensitive time window of the front-end chips the occupancy can be reduced considerably. The estimated occupancy reduction factor corresponds to the quotient of the two sensitive time windows and is about 12.5 when the VA1TA is replaced by the APV25.

In the situation described above the signals from the background and the event each affect different channels. However it might also be possible that both, the off-time and the event particle, will hit the same strip(s) of the sensor, which is called pile-up. Even though, such a case does not increases the occupancy, it leads to a considerable distortion of the signal shape, because the signals of both hits are superimposed. While normally the collected charge can be determined from the sampled pulse height, this is not possible with a pile-up signal, because of its distorted shape. Similar to the occupancy, this effect also depends on the long tail of the shaper output, thus a shorter peaking time reduces the probability of pile-ups. Moreover, it is not possible to distinguish between the signal of a pile-up and that of a normal hit, when only a single sample of the shaping curve is read out. To be able to identify pile-ups it is necessary to read out several consecutive samples and reconstruct the actual pulse shape.

4.2. Hit Time Reconstruction

As already mentioned, only one sample is usually taken from the shaping curve, thus the data does not give any information about the real time at which the particle traverses the sensor. If the information is limited to a single sample, the timing precision is given by the sensitive time window of the readout chip. There is no possibility to ensure that the data are actually taken at the peak of the shaping curve. As discussed before it is also possible that a signal is sampled on the rising edge or the tail. However, the whole shaping curve, which follows an exponential function defined in eq. 2.20, also contains information about the real hit time. One important property of this function is that it always reaches its peak T_p after the particle traverses the sensor, independent of the signal amplitude.

Below a method to obtain precise hit time information from the shaping curve will be presented. Therefor it is necessary to take several consecutive samples around the peak of the signal. By performing a fit to these samples using the theoretical exponential function or a measured reference shape it is possible to determine the real position of the peak and furthermore the maximum pulse height. In fig. 4.2 an example of a sampled shaper output measured with the APV25 readout chip at a beam test (see chapter 7) is shown. Two different fit functions were applied to determine the location of the peak.

At this point only the basic technique is illustrated. Information about the implementation within the hard- and software of a readout system prototype, the actually applied fit functions, the fit algorithm used in the analysis software, the performance tested with data from several beam tests as well as the accuracy of the extracted peak time that can be achieved with this method are presented in detail in chapters 6 and 7.

In order to perform such a measurement, a readout chip with the ability to sample a series of points of the shaper output is required. Moreover, the chip also has to be equipped with a pipeline attached to the shaper, which can buffer the samples until they are read out. The VA1TA does not support this functionality and due to its long T_p it would not offer high precision. A front-end chip that meets these requirements is the

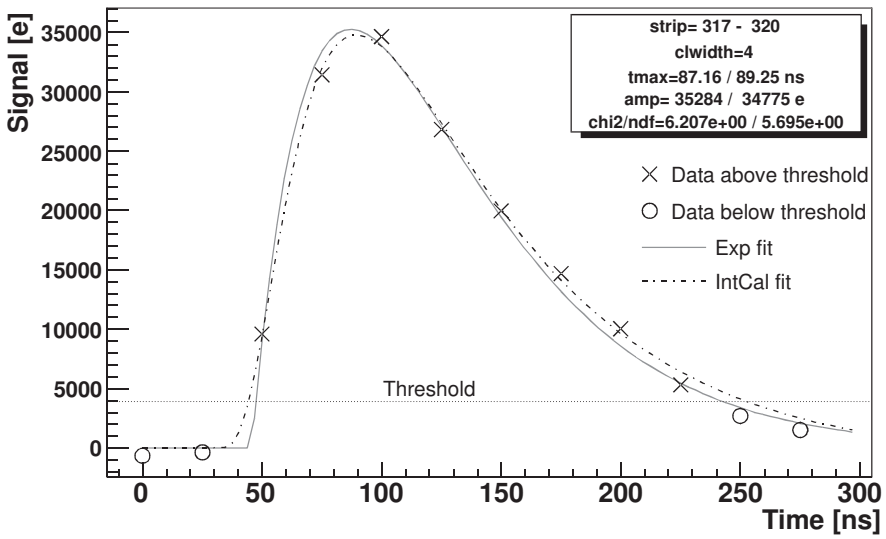

Figure 4.2.: Sampled shaper output values fitted with two different fit functions. The samples were acquired by an APV25 chip within a beam test.

APV25 which will be described in section 5.1.

4.3. Sensor Geometry

The techniques described above are indended to scale down the sensitive time window. However, there is also a geometrical approach in order to reduce the occupancy of a silicon strip detector system. The probability that a strip is hit by a particle within a defined time period depends on its geometrical dimensions. Usually the width and the pitch of the strips is given by the required spatial resolution of the sensor and the affordable number of readout channels, thus they can not be modified easily. That means, the only remaining parameter that can be altered to achieve an occupancy reduction is the strip length. In a commonly used DSSD design the strips are arranged orthogonally in parallel to the detectors edges. To achieve the maximum possible coverage of the detector area their length is chosen to be almost as long as the sensor itself. As the sensors of the SVD2 are rectangular with an area of 76.8×25.6 mm^2 such a strip design leads to relatively long strips of about 76.8 mm on one side of the detector. However, dividing these strips into smaller parts has the disadvantage that not all bonding pads can be placed along the sensors edges and thus makes the contacting of the strips more difficult.

A more sophisticated approach is to rotate the strips on both sides by 45° compared to a conventional sensor. The merit of this inclined design is that the strips on both sides are shortened and wire bonding can still be done along the sensors edges. A prototype of such a sensor was designed by the Belle group and will be described in section 5.2 in detail. With this sensor, called “UV striplet”, the occupancy can be reduced by a factor of five as a result of the shorter strips [38, 39]. However, this method implies an increase of the total number of readout channel of the same factor. Furthermore the rotated coordinates, compared to the other subdetectors, makes the vertex reconstruction more complicated and requires an essential modification of the analysis software. Hence, the method of shorter sensitive time is preferable.

5. SVD Upgrade

A conceptual design for a KEK Super B Factory experiment for an ultimate luminosity of $5 \times 10^{35}\ cm^{-2}s^{-1}$ was proposed [40]. To keep up with such a high luminosity all Belle detector subsystems need to be upgraded. The layout of the planned SVD4[1] for the Super B Factory consists of 6 layers. The radius of the innermost layer is 1.3 cm and that of the outermost about 14 cm. Compared to the SVD2 the innermost layer will be closer to the beam pipe, while the outer radius is almost doubled. Fig. 5.1 compares the SVD2 and the SVD4 layouts.

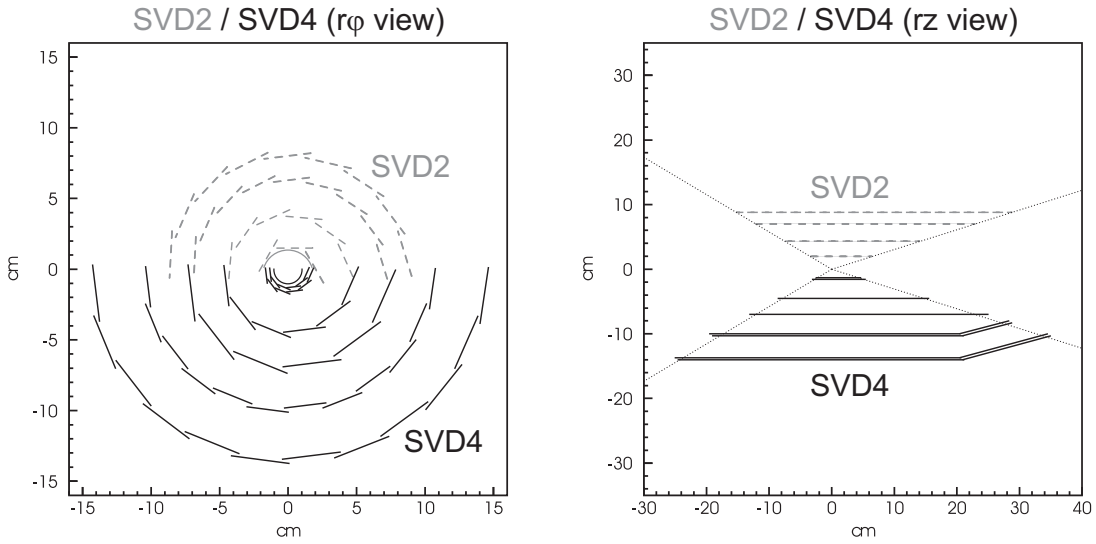

Figure 5.1.: Comparison of SVD2 and SVD4 layouts [39].

In section 3.3 the limitations of the currently installed SVD were discussed and the increasing occupancy as well as the dead time of the readout electronics have been identified as its main weak spots. In chapter 4 some general methods how the occupancy of a silicon strip detector system can be reduced were introduced.

One main issue of the upgrade concept is the replacement of the currently used VA1TA chip by a faster and more modern one. In order to be able to handle the expected higher luminosity the new chip should provide a significantly shorter peaking time than the VA1TA and it further should be read out at a higher clock frequency. With respect to the dead time problem, it needs to have a pipelined structure to allow continuous data sampling without any interruption during the readout of the chip.

A comparison of all currently available candidates [40] concluded, that the APV25 chip, originally developed for the CMS tracker at CERN, will fulfill all the requirements listed above. The APV25 operates at 40 Mhz, has a shaping time of nominally 50 ns and an internal pipeline of 192 cells. A detailed description of this chip is given in section 5.1.

[1] Originally an intermediate upgrade called SVD3, where only the innermost layer of the SVD is replaced, was planned for summer 2008 but was canceled in autumn 2007 in favor of a full upgrade.

However, there are some considerable differences between CMS and Belle. One important point is that in the CMS tracker only single-sided detectors are used, while the Belle SVD consists of DSSDs. This requires some modifications to the readout electronics compared to the CMS system.

Moreover, the KEKB factory operates at 8 GeV and 3.5 GeV for the HER and the LER, respectively, which is three orders of magnitude lower than the center of mass energy at CMS (14 TeV with protons). Hence, multiple scattering and its influence on the vertex resolution is an important issue at Belle but not at CMS. Therefore the minimization of the material budget inside the active area of the Belle SVD is very essential. While in the CMS tracker the APVs are placed as close as possible to the silicon sensors, they should be located outside the active area at Belle. It was unknown whether the APV25 can be operated stably with such long "fanouts"[2] of up to 30 cm between the sensor and the readout chips. In order to get a feeling about the usability of the APV25 chips a test setup, called "Long Line", with two types of a more than 50 cm long printed circuit board between the sensor and the APV25 was constructed. A more detailed description as well as the results of the performed measurements using a ^{90}Sr source are given in section 7.1.

Beside the replacement of the VA1TA it is planed to use a special type of double-sided silicon sensor called "UV striplet" for the two innermost layers. A description of this sensor is given later in section 5.2.

5.1. APV25

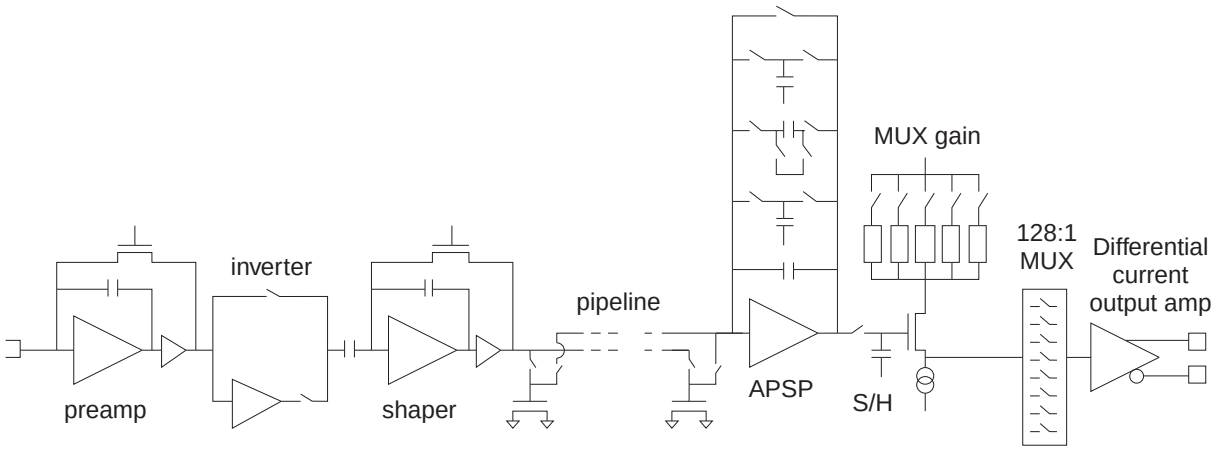

Figure 5.2.: Block diagram of the APV25 chip. The components to the left of the multiplexer (MUX) are implemented 128 times for each channel.

The APV25 is an ASIC with 128 channels of charge sensitive preamplifiers followed by CR-RC shaper stages and a common multiplexed differential analog output. It is manufactured in a 0.25 μm IBM deep sub-micron CMOS technology and is radiation tolerant to more than 100 MRad (1 MGy). It was originally developed as front-end chip for the CMS silicon tracker; the full name of the final version is APV25S1. Fig.5.2 shows

[2] As connection between the readout chips and the sensors a high density printed circuit made up of a thin flexible foil is used in the Belle SVD. This part is usually named fanout or pitch adapter by the high energy physics community.

the schematic of one input channel as well as the common multiplexer and the output driver [18, 41].

The integrating low noise preamplifier is followed by an optional inverter stage. It usually has to be switched on for single sided p-bulk detectors as well as for the n-side (n+ strips) of a n-bulk DSSD to achieve equally polarized signals for both sides. After the inverter there is the CR-RC shaper with a peaking time of nominally 50 ns, but adjustable in the range from about 30 ns to more than 200 ns. The feedback resistors and all bias currents and voltages of both the amplifier and the shaper as well as the inverter switch can be programmed via an I^2C interface. The output of the shaper is continuously sampled with the clock frequency of nominally 40 MHz and then fed into the analog pipeline, which is 192 cells long. When a trigger arrives, the data are extracted from the pipeline and passed to an analog pulse shape processor (APSP). When the APV is set to deconvolution mode, this switched capacitor filter performs a three-weight deconvolution as described in section 5.1.1. In peak mode the APSP is disabled and a single sample is propagated without modification. A sample/hold (S/H) stage and an amplifier with programmable gain follow. In the end the signals of all 128 channels are multiplexed onto a common, analog, differential current output line.

The APV25 provides three different operation modes, which are the peak mode, the deconvolution mode and the multi-peak mode. It further supports a special internal calibration mode to check the functionality of each channel. A description of these modes is given in section 5.1.1.

The equivalent noise charge of the APV25 in peak mode can be expressed by

$$\mathrm{ENC_C\,[e]} = 250 + 36\,\mathrm{C\,[pF]} \quad , \tag{5.1}$$

where $\mathrm{ENC_C}$ is given in number of electrons and C is the capacitive load at the preamplifier input in pF. Obviously the APV25 has a higher noise figure than the VA1TA (see tbl. 3.1), which is a consequence of the shorter shaping time. The key parameters of the APV25 chip are listed in tab. 5.1.

Amplifier:	Charge sensitive pre-amplifier with CR-RC shaper stage.
Input channels:	128
Supply Voltages:	$V_{dd} = +2.5$ V $V_{ss} = 0$ V
Power dissipation:	350 mW nominally
Peaking time:	50ns nominally adjustable between 30 ns and more than 200 ns
Pipeline:	192 cells
Output:	multiplexed, analog differential current output
Readout:	40 MHz nominally
Logical inputs:	Low Voltage Differential Signals (LVDS)
Chip size:	8.055×7.1 mm^2
Manufacturing process:	0.25 μm IBM deep sub-micron CMOS
Radiation tolerance:	more than 100 Mrad

Table 5.1.: APV25 parameters.

5.1.1. Operation Modes

The selection of the active operation mode of the APV25 as well as the adjustment of all other parameters and settings can be done via the I^2C interface of the chip. Independent of the selected mode, the shaper output is continuously sampled and stored in the analog pipeline at the clock frequency. Three of the available operation modes differ in the number of samples of the shaping curve that are used and how they are processed by the APSP before they are passed on to the output. The fourth mode is the internal calibration, that is intended to test each channel.

Trigger Line Symbols

The readout of the APV25 is initiated by the trigger line, which is a low voltage differential signal (LVDS) input. Whenever a single pulse (one clock wide) is sent to this input the corresponding signals stored in the pipeline are taken and transmitted to the output of the chip.

Symbol	Meaning
1	Trigger
101	Reset
11	Calibration

Table 5.2.: Trigger line symbols of the APV25.

The trigger input is also used for (soft) reset and initiating the calibration pulse. To distinguish between these functionalities special symbols are used, which are listed in tab. 5.2. A single logic 1 on the trigger line is interpreted as trigger, while a 101 causes a reset of the chip and the symbol 11 is a calibration request (see below). Thus, a the minimum distance between two incoming triggers is three clock cycles or 75 ns at 40 MHz. More frequent triggers would be miss-interpreted as soft reset or calibration request.

Peak Mode

In peak mode only a single sample of the shaping curve is taken from the pipeline of each channel and passed to the output of the APV25 without any further processing by the APSP. Assuming that the clock and the trigger latency are configured correctly, this sample exactly corresponds to the peak of the shapers output. In this mode the APV25 works in same manner as the VA1TA, but with a shorter peaking time and a faster sampling and readout clock frequency.

Deconvolution Mode

In the deconvolution mode the APV25 extracts three consecutive samples from the pipeline and builds the weighted sum of them using the APSP, resulting in

$$d_k = w_3\, p_{k-2} + w_2\, p_{k-1} + w_1\, p_k \quad . \tag{5.2}$$

In eq. 5.2 p_i are the sampled shaper output values, which are taken from the pipeline and w_i are individual weights. The target of this method is to essentially restore the original

detector current pulse. A detailed description and the mathematical background can be found in [42]. Applying this method leads to a narrow signal which is approximately zero at any time expect for one clock period. The advantage of this mode is that off-time signals can be filtered out in an easy way, at the cost of a higher noise level. However, this method requires a sampling frequency that is synchronized to the particle hits and thus to the bunch crossing, as it is the case at CMS. Due to the quasi-continuous beam of the KEKB accelerator, this mode cannot be used at Belle.

Multi-Peak Mode

As mentioned before, the APV25 only supports consecutive triggers with a spacing of at least three clock cycles. This limitation is solved by the multi-peak mode, where three consecutive samples are read out after the reception of only a single trigger. Contrary to deconvolution mode, no signal processing is performed by the APSP in this mode.

The multi-peak mode also provides the ability to read out more than three samples, by sending a sequence of triggers, each in a distance of three clock cycles (75 ns at 40 MHz), to the APV chip. As an example, nine consecutive samples can be obtained by the sequences 1001001 on the trigger line. Continuing this pattern, up to 30 samples (limited by the pipeline FIFO, see section 5.1.2) of the shaping curve of the APV25 can be read out.

Internal Calibration

The internal calibration is actually not an operation mode like the ones described avove, it rather provides the ability to test the functionality of each channel using the integrated calibration pulse generator of the APV25 chip. This can be done with each of the three modes, described above.

The principle of this internal calibration is to apply a voltage step pulse ΔV to a series capacitor which is connected to the input of the amplifier. The injected charge is given by

$$\Delta Q = C\,\Delta V \quad . \tag{5.3}$$

Controlled by a programmable mask register the pulse can be applied to one (or more) out of eight groups, each connected to sixteen input channels of the chip. Furthermore, the amplitude of the voltage step and hence the injected charge is programmable. Also the timing of the pulse can be adjusted in steps of 1/8 of the clock frequency, which are 3.125 ns at 40 MHz. A detailed description of the internal calibration system is given in [18].

The calibration generator is initiated when the symbol 11 is received on the trigger line. After the programmed delay a toggle switch is activated and the calibration pulse is applied to the selected groups of input channels. The calibration request only generates the charge pulse, but does not initiate the readout of the chip. Thus, a separate trigger has to be send after the calibration request, which has to be separated by the latency time. As the calibration switch toggles with each calibration request, the polarity of the produced voltage pulse alternates. To achieve a series of signals of the same polarity, it is useful to send the sequence 11 ... 1 ... 11 on the trigger line, where the second calibration request is used to dump the signal of the inverse polarity.

5.1.2. Pipeline

The pipeline of the APV25 is implemented as a ring buffer of 192 cells and cycling write and read pointers. The distance between these two pointers is programmable and should correspond to the latency between the particle signal and the arrival of the trigger. After a trigger was received it takes about 5 μs to send all the data to the output through the multiplexer. To avoid that valuable data are overwritten, the address of the corresponding pipeline cell is stored in a FIFO with a depth of 32 locations. All cells, whose addresses are in the FIFO are then protected against overwriting and skipped by the write pointer as long as they are not read out. While in peak mode only one cell is marked, three addresses are stored in this FIFO in deconvolution and multi-peak modes. This scheme avoids dead time and allows continuous sampling of the shaper output, even during the readout of the data.

5.1.3. Multiplexer

The multiplexer is implemented in a three stage design. Its principle structure is shown in fig. 5.3. Due to the three stages the analog data of the 128 channels are not transmitted to the output in their natural order. To retrieve the physical channel number c from the output sample number n, the equation

$$c = 32\,(n \bmod 4) + 8\,\mathrm{int}\left(\frac{n}{4}\right) - 31\,\mathrm{int}\left(\frac{n}{16}\right) \tag{5.4}$$

(or a corresponding lookup table) has to be used. At the last stage ot the MUX some additional digital data, such as the pipeline cell address and some header bits are added to the output data frame, which is described in the following section. The output levels of this digital data are ±4 mA (±8 mA differential), while those of the channel data correspond to the sampled signal.

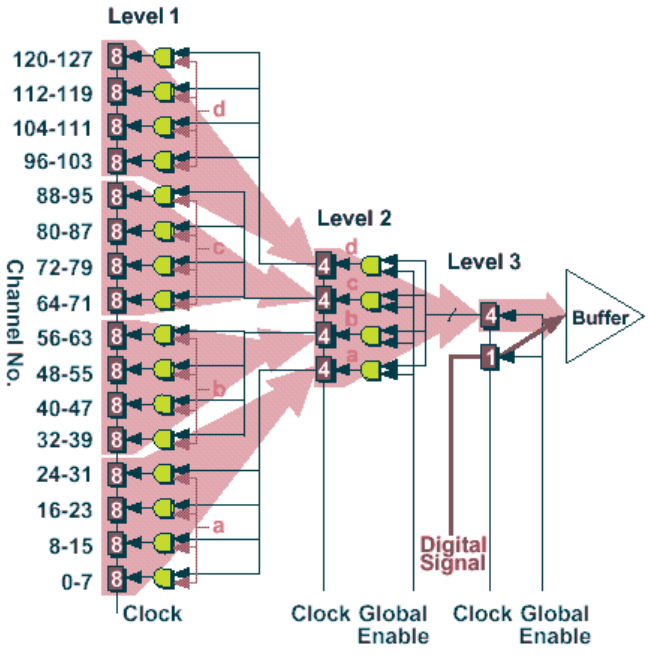

Figure 5.3.: Structure of the three stage APV25 multiplexer [18].

5.1.4. APV25 Output

The output of the chip provides a analog, differential current signal. It can be read out either with the half (20 MHz) or the full (40 MHz) clock frequency. When there are no data in the output buffer, the output is at logic low level, which is about −8 mA of differential current. Depending on the selected readout clock, every 70 or 35 system clocks, for 20 MHz or 40 MHz readout, respectively, a pulse is transmitted through the output. These pulses are called "tick marks" and they are suitable as debugging signals. As long as the APV25 sends these tick marks, one knows that the chip is alive and correctly receives the clock.

After a trigger the chip waits until the next live tick before it starts the data output. The sequence of a typical output data frame is depicted in fig. 5.4. Each frame starts

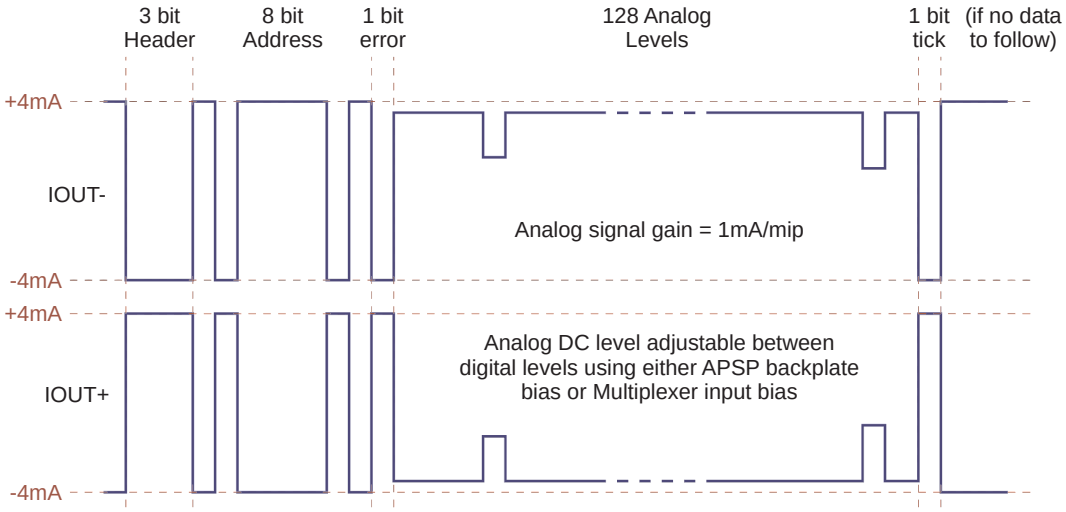

Figure 5.4.: Output data frame of the APV25 [18].

with a header of three bits with logic high level. The readout electronics can use these three consecutive high level bits to identify the beginning of a data frame. The header is followed by the eight bit address of the read out pipeline cell. These addresses are numbered in a specific scheme that is derived from the Gray Code. When a group of equally configured chips is running in parallel on the same trigger and clock lines, they should always deliver the same pipeline cell address. Thus this address can be used by the readout system to check the synchronicity of all chips. After this address a single error bit concludes the header. This is set by the chip internal error logic and indicates whether the latency between the read and write pointer is equal the programmed value or not. The bit is further set when the FIFO to store the pipeline addresses is full. The type of error can read out via the I^2C interface. Either a soft or a hard reset has to be applied to the affected chip to clear such an error state.

After the header the analog data of all 128 channels are transmitted in the multiplexed order. The total length of one frame is 140 bits. As the frame always starts at the position where a tick mark is transmitted when no data are pending and it further has exactly the duration of two (20 MHz mode) or four (40 MHz mode) tick marks including the void following the pulse, the next tick mark follows immediately after the frame. However, in the case of further pending triggers or in multi peak-mode the frame is directly followed by the next one without any tick marks between them.

5.2. UV sensor

A DSSD with 45° rotated strips was designed aiming at an occupancy reduction of a factor of five. The sensor has a length of 71 mm and a width of 8.5 mm. The length of the strips is only about 11 mm, because of their diagonal direction. An image of this sensor is shown in fig. 5.5, where the directions of the U and V coordinates are indicated by a solid and a dashed white line, respectively.

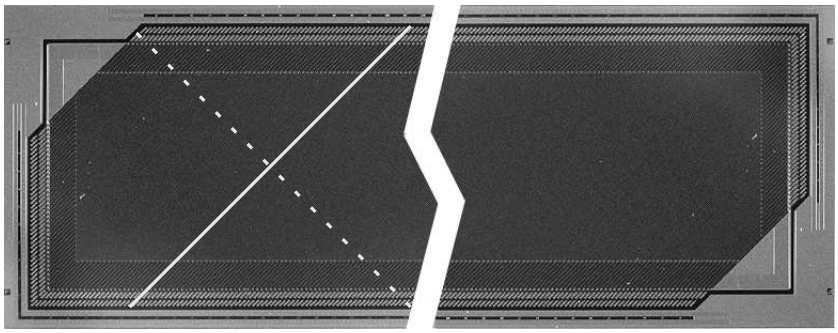

Figure 5.5.: DSSD with 45° rotated strips, called "UV striplet". The solid and the dashed white lines indicates the strips in the direction of U and V coordinates, respectively.

It was designed by the Belle group at KEK and fabricated by Hamamatsu Photonics, which also delivered the sensors of the current SVD. It has 1024 readout strips on each side. The pitch of the p-side is 25.5 μm with one intermediate strip, thus the readout pitch is 51 μm. On the n-side the pitch is 51 μm and each strip is surrounded by an atoll type p-stop (see fig. 2.10 on page 16). Due to limitations on the minimum strip length there are small triangular dead areas in two corners of the sensor where no strips can be placed. This dead area might have negative influence on the resolution of a SVD built up with sensors of this type.

The CV curve of a prototype sensor was taken to determine the depletion voltage of the UV striplet. Therefore the bulk capacitance was measured at different voltages and the curve $1/C^2$ as a function of the voltage is drawn [19]. The measured curve can be approximated by two linear segments and their intersection determines the depletion voltage. As shown in fig. 5.6, the depletion voltage of this sensor is about 65 V. The key features of the UV sensor are summarized in tab. 5.3.

A thin flexible printed curciuts (FLEX) is foreseen for the connection between the sensor and the readout chips. To due the small sensor area and the relatively high number of readout channels, this FLEX must be constructed of multiple layers at a very narrow pitch between the lines. Even though the production of such a circuit is very difficult, prototypes with a pitch of 37 μm could be fabricated [38]. However, the yield of these FLEX circuits is not very good, thus further studies are necessary.

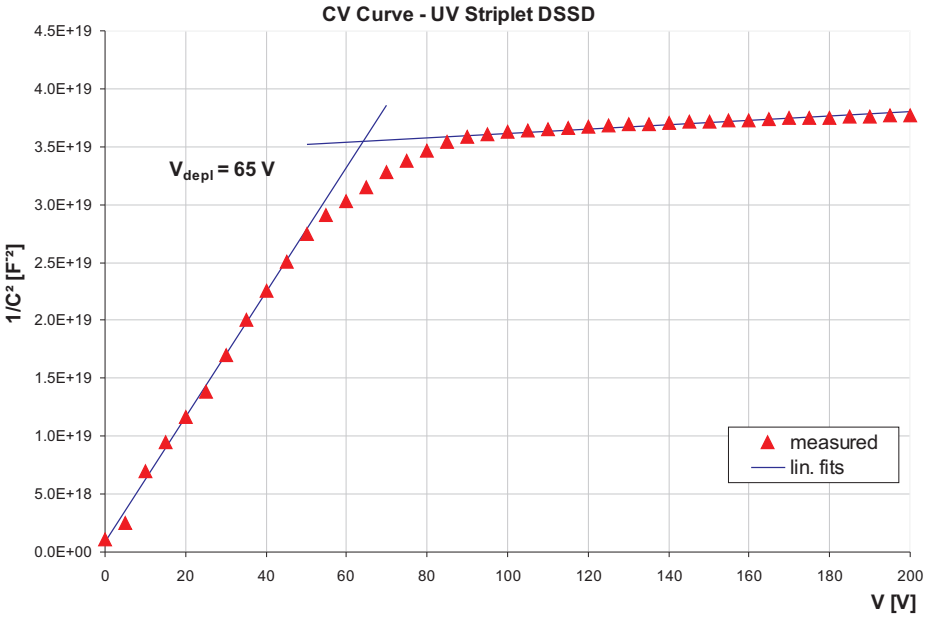

Figure 5.6.: Mesured CV curve of the UV striplet DSSD. The blue lines are linear fits of the two regions and their intersection point determines the depletion voltage, which is about 65 V for this sensor.

	p-side	**n-side**
readout strips	1024	1024
strip pitch	25.5 μm	51 μm
readout pitch	51 μm	51 μm
intermediate strips	1	-
p stop	-	atoll type
sensor size	71 mm $\times$ 8.5 mm	
strip direction	45° (UV coordinates)	
strip lenght	11 mm	
depletion voltage	65 V	

Table 5.3.: Key parametes of the UV striplet sensor.

6. APVDAQ Test System

6.1. Overview

A readout test system, which can be used for laboratory measurements as well as at beam tests, was designed to evaluate the suitability of the APV25 chip under the conditions of the Belle experiment. At the same time, this test system is a small-scale prototype of the future SVD readout, which will consist of the same building blocks.

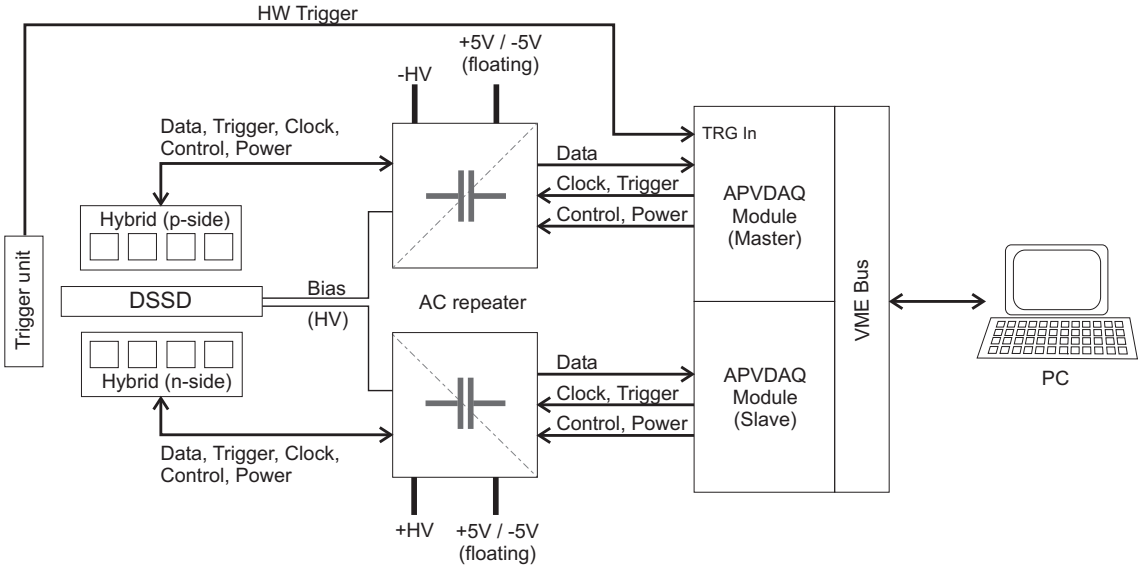

Figure 6.1.: Block diagramm of the APVDAQ system. The displayed configuration shows the readout of a DSSD. The HV bias of the sensor is applied via the AC repeaters and the low voltage potentials of the hybrids sit on the top of the bias voltage levels +HV and -HV (typically ±40 V).

The key requirements of this system were:

- APV25 used as front-end chip.
- Readout of both single-sided and double-sided silicon strip detectors.
- Floating power scheme that allows the operation of the APV25 at the bias voltage level of the sensor.
- Front-end system with up to four APVs and thus 512 readout channels per sensor side, respectively.
- Modular and scalable VME based back-end electronics using FPGAs to provide a programmable logical circuit that can easily be modified as needed.

- Data acquisition and front-end chip control via the VME bus interface.
- Adjustable delay for both the trigger signal and the clock of the ADCs to allow easy timing configuration.
- Full support of all operation modes of the APV25 chip.

The test system is called APV25 data acquisition (APVDAQ) system. Fig. 6.1 shows the block diagram of the basic configuration as it is used for the readout of a DSSD. From the front-end to the VME crate, it consists of the APV25 hybrid, the AC repeater and finally the APVDAQ VME module. Two units of each component are required to readout a DSSD, one per side of the sensor. Moreover a 6U VME crate, a VME bus controller and a personal computer are needed. Below, an overview of all components of the APVDAQ system and the cabling is given. More details, such as a description of the VME commands used to control the system, can be found in the APVDAQ reference manual [43].

6.2. APV25 Hybrid

The APV25 hybrid is the front-end part of the APVDAQ system, which is located close to the silicon strip sensor. It is a 39 mm × 64 mm large printed circuit board (PCB) with 6 layers. It can be equipped with up to four APV25 chips, and thus it can read out up to 512 strips of a sensor. The left photo of fig. 6.2 depicts a fully equipped hybrid bonded to the UV striplet DSSD via a pitch adaptor. On the right image the layout of the hybrid is shown.

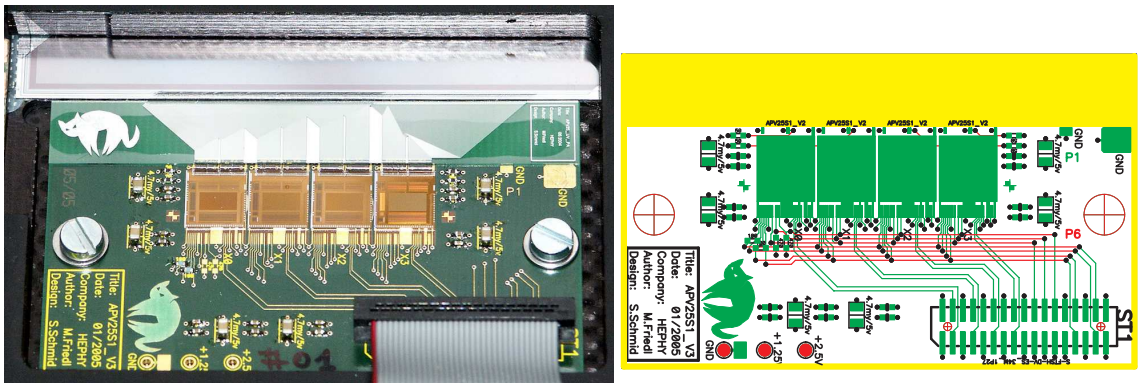

Figure 6.2.: The left image shows the APVDAQ hybrid equipped with four APV25 chips bonded to a UV striplet sensor via a pitch adaptor. On the right side the layout of the hybrid is depicted.

The APV chips are glued onto the board using a conductive adhesive, which provides an electrical connection between the local ground of the hybrid and the bulk of the chip. All supply powers, the data outputs and the control signals of the APV25 are connected to the hybrid by wire bonds. The surfaces of all bond pads as well as all the other contacts are coated with gold to ensure proper bonding conditions. Beside the APV chips, the board contains some decoupling and storage capacitors as well as terminating resistors for the LVDS trigger and clock signals. All four APV chips can be configured via a I^2C bus. The address of each chip is set by bond wires defining its address bits [44].

The hybrid is connected to the repeater by a single 34 wire flat cable that carries all necessary signals and supply voltages, except the bias voltage of the sensor, which can be provided from the repeater by a separate cable.

At the front of the APV25 chips there is an approximately 9 mm wide area without any traces and electrical devices. A pitch adaptor can be glued onto this free space, because usually the bonding pattern of the sensor does not match that of the APV25 chips. Such adapters are printed circuits with a very fine structure and are commonly made of glass, ceramics or a thin flexible polyimide foil (e.g. Kapton). An example of a glass adapter, which converts the straight, staggered 44 μm pitch of the APVs to the 45° rotated 51 μm pitch of the UV striplet detector is shown in the left photo of fig. 6.2.

6.3. AC Repeater

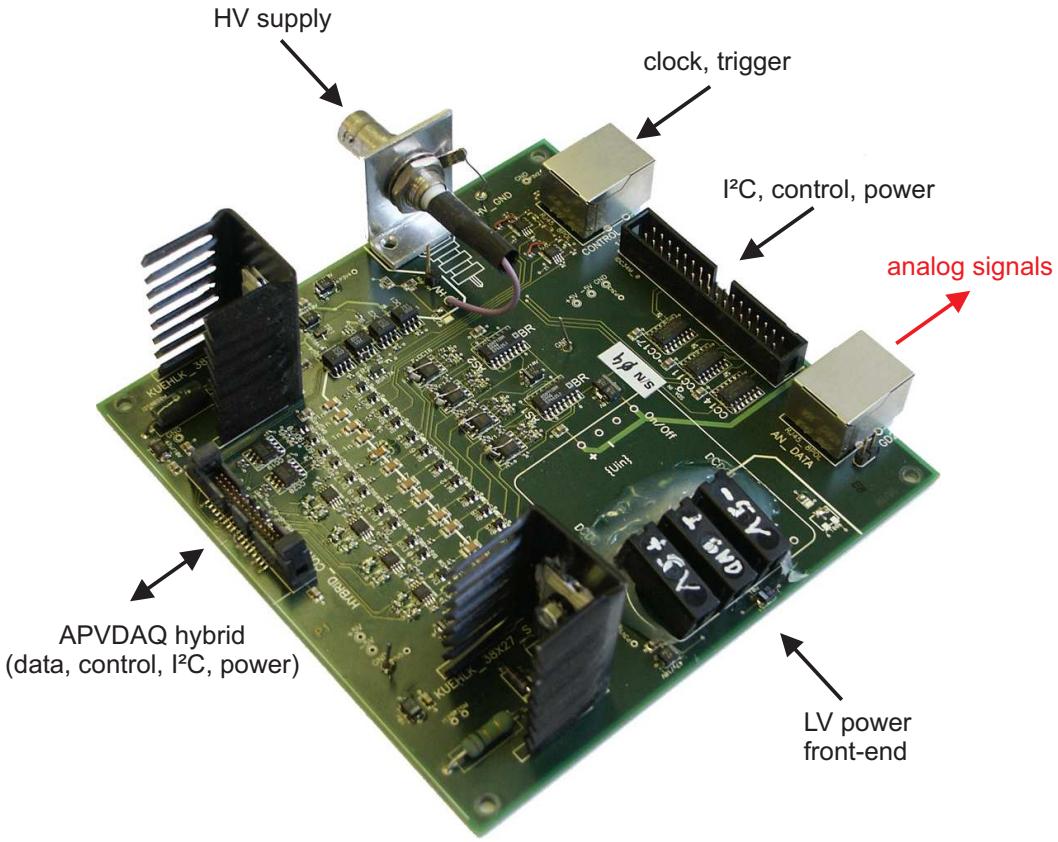

Figure 6.3.: APVDAQ AC repeater board.

The AC repeater is an interface board between the APV25 hybrid and the remote APVDAQ VME module, which can be up to 30 m apart. Its key function is to separate the floating front-end units, which are at HV levels, from the grounded VME system and to transform their signals. Hence, the electrical circuit of the board is divided into two zones, one with floating ground, the second with VME ground (earth) level. Fig. 6.3 shows an image of the repeater board, where the white line on the PCB indicates the border between these two areas. A capacitive coupling scheme is implemented to perform level shifting and decoupling of clock, trigger and analog signals, while the slower I^2C and reset signals are bridged by optocouplers.

The schematics of the coupling circuit of one analog channel is shown in fig. 6.4. On

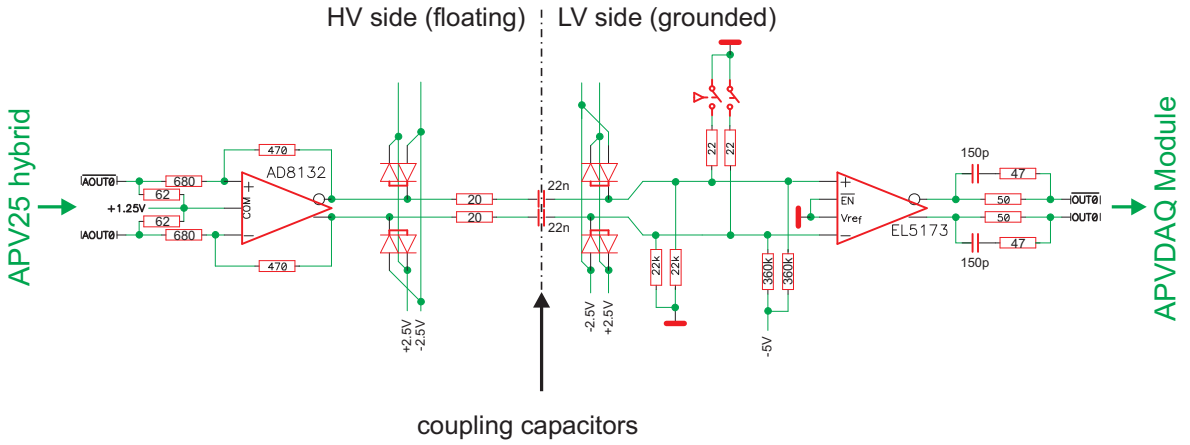

Figure 6.4.: Schematics of the AC coupling circuit of one analog channel.

the HV side, there is a high-speed differential amplifier (AD8132), whose gain is set to 0.7 by the external resistors. The coupling is done by the 22 nF capacitors in the center. Their voltage rating has to be higher than the bias voltage of the used silicon sensor, as that voltage is dropped across the capacitor. As the typical bias voltage is ±40 V, of the UV sensor is about 65 V, the repeater was equipped with a type that provides a rated voltage of 100 V.

The LV side primarily consists of a high impedance line driver for twisted pair cables (EL5173) with a fixed gain of two. It is followed by a pre-emphasis circuit made up by a high-pass filter (150 pF and 47 Ω) in parallel to a 50 Ω resistor. At the receiver, which is on the APVDAQ module, the analog channels are also terminated by 50 Ω resistors. The series resistors at the driver output and the termination of the line make up a voltage divider, which corresponds to a gain of 0.5. Hence, the overall gain of the repeater is 0.7 for analog signals. The fact that the repeater is an attenuator rather then an amplifier is owed to the high output levels of the APV25, which make the signals immune against noise pickup.

There is another voltage divider at the input of the line driver, built by the 22 kΩ and the 360 kΩ resistors. Its purpose is to define the DC signal level at the inputs of the cable driver. The coupling capacitance together with the resistors at the driver input form a high pass filter with a time constant of 456 μs. As the APV output signals are above the baseline, their level decays slowly. This effect is negligible as long only one sample is read out, but becomes an issue in multi-peak mode, particularly when a large number of samples (e.g. 30) is taken. Therefore, an electronic switch, which can be controlled by the APVDAQ VME module (see 6.4), is foreseen to tie the capacitance to local ground level over two 22 Ω resistors, whenever the APV25 output is idle. Thus, the time constant is some order of magnitude smaller when the switch is closed and the baseline of the signal is restored quickly.

The power of the LV side is provided by the APVDAQ module over a 34 wire flat cable, that also carries the slow control signals. A DC/DC converter was originally foreseen to supply the floating part of the reapeater and the APV25 hybrids. However, measurements have shown, that such a converter causes excessive noise in the APV25, because its switching frequency is inside the sensitive range of the APV chip (see 7.1). Thus the converter was replaced by three banana plugs through which the front-end

side has to be supplied by an external, preferably linear, laboratory power supply. The APVs on the hybrids need two supply voltages, which are 1.25 V and 2.5 V, respectively. They are generated from the floating +5 V by two voltage regulators near the hybrid cable connector which are equipped with heat sinks (see fig. 6.3).

Furthermore, there is a HV connector foreseen, at which a high voltage cable can be attached to apply the bias of the sensor. Close to this connector there is the HV pin, where the high voltage can be picked up and applied to the sensor.

6.4. APVDAQ VME Module

The APVDAQ VME module is a 6U VME board used for both control and readout functionality. It consists of a central FPGA (Altera Stratix) on a daughter board, another FPGA (Altera Acex) for VME bus control, the ADC daughter board and some supplemental components, e.g. a voltage regulator, a delay chip, an oscillator and some drivers. A photo of the board and its main components is shown in fig. 6.5.

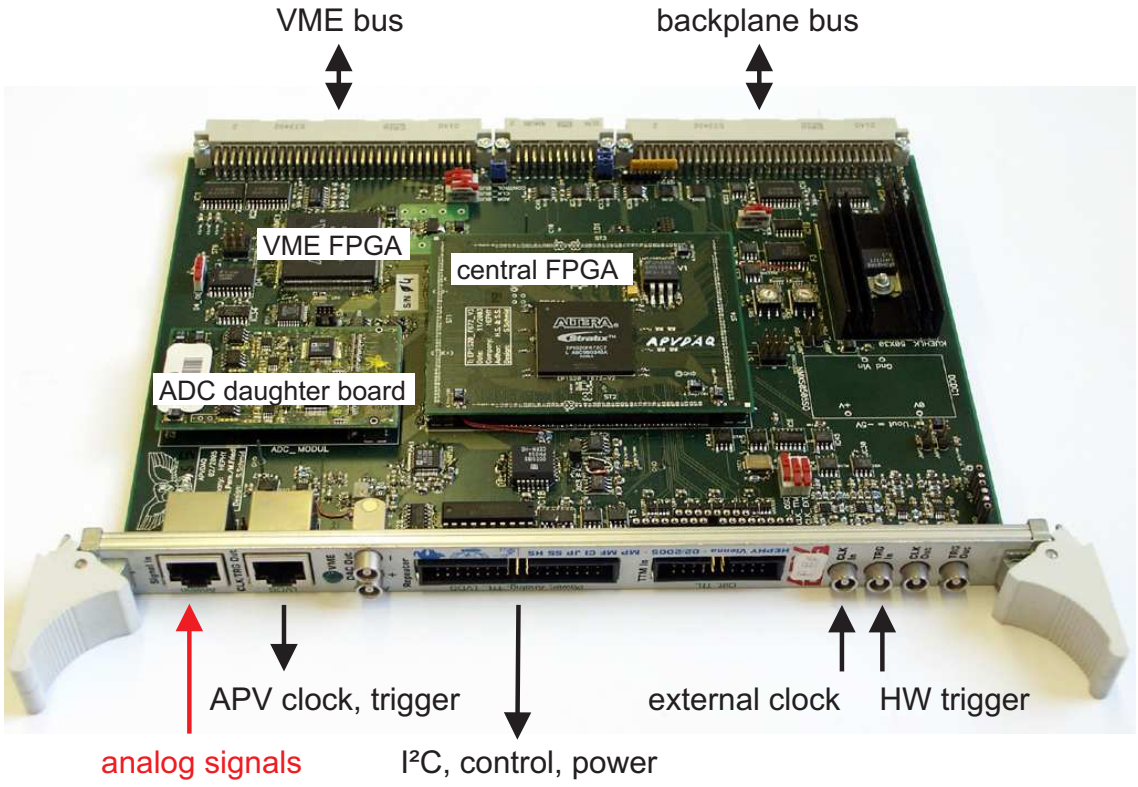

Figure 6.5.: APVDAQ VME board

On the ADC daughter board there are two 10 bit fast analog digital converters (AD9218), each with two channels. Thus, one module can read out up to 4 APVs chips. The APVDAQ system can either be used with one single VME module, such as to read out a single sided detector, or with two or more modules. Using several modules in parallel, one of them has to be configured as master, while all the others must be operated in slave mode. This settings can be done by several DIP-switches on the board. In multi-module operation a customized backplane (or cable) has to be applied at the P2 connector of the VME bus, over which the trigger and clock signals are distributed from the master to the slaves.

Most of the logical functionality is programmed into the central FPGA. The second (smaller) FPGA chip is called "VME Altera", as its firmware is responsible for handling the VME bus protocol. It further contains two I^2C masters; one is used to communicate with the APV25 chips, while the second is intended to control the delay chip (PHOS4[1] [45]). The APVDAQ module uses 32-bit addressing at the VME bus, where the upper 8 bit of the base address can be configured by two hexadecimal-coded micro switches. Since the most significant bit A31 is reserved for broadcast, the base address can be configured between 0x01000000 and 0x7f000000.

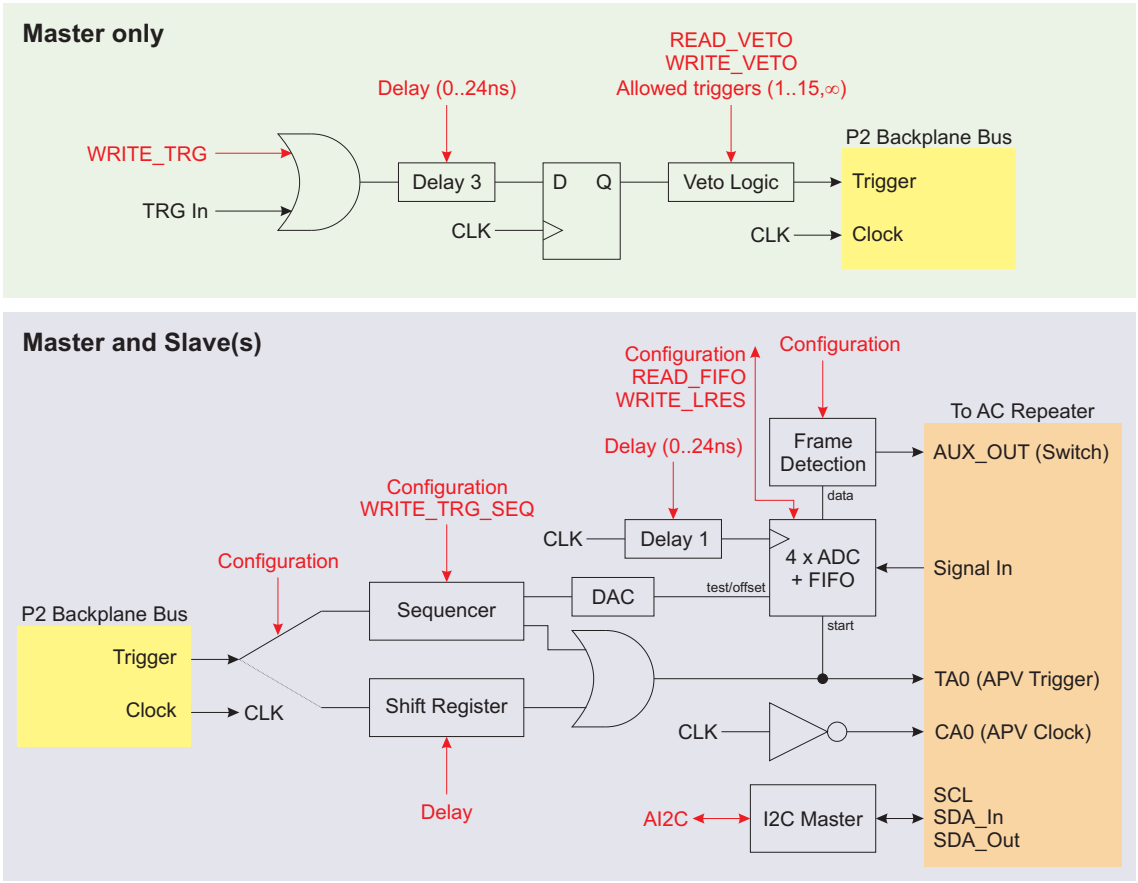

Figure 6.6.: Block diagram of trigger and data path of the APVDAQ VME board. The red colored items correspond to VME functions, which are described in [43].

The firmware of both chips can be programmed by their JTAG[2] interface, either directly through dedicated connectors next to the FPGAs or - in case of the central FPGA - via the VME bus using a special software.

The data flow within the APVDAQ module is shown in fig. 6.6. The red items correspond to VME functions, which are described in detail in the reference manual [43]. Although the same firmware is used for both master and slave, the units depicted in the top box are only available with the master and disabled for the slaves. The master provides clock and trigger signals on the P2 backplane bus to the slaves and also to

[1] Designed at CERN

[2] Joint Test Action Group (JTAG) is the usual name for the IEEE 1149.1 standard entitled "Standard Test Access Port and Boundary-Scan Architecture", which is used to test interconnections of integrated circuits located on a PCB using boundary scan. Moreover, this interface is commonly used to program the firmware of FPGAs.

itself. Three different clock sources can be selected by DIP-switches, namely the internal 40 MHz oscillator, the "CLK In" connector on the front panel of the module and finally the P2 backplane. The first two sources are only available at the master, while the third one has to be chosen for all slaves (and actually the master also picks up the clock at the P2 backplane, yet is also provides it there). The external clock input supports a wide range of frequencies and was successfully tested with 40, 50, 63 and 80 MHz.

A hardware trigger can arrive at any time through the "TRG In" connector of the front-panel. This signal is first sent through a programmable delay (Delay 3), before it is synchronized to the system clock. The delay is adjustable between 0 and 24 ns and is suitable for fine tuning of the timing, particularly when narrow trigger pulses (shorter than the clock period) are used. The delayed trigger is then it is passed on to a trigger conditioner and veto logic, which ensures that the minimum trigger spacing of the APV (two emtpy clock cycles, see 5.1.1) is met and blocks all incoming triggers exceeding a predefined number (typically 1) until the veto signal is cleared via the VME interface. Every trigger that passes this logic is distributed to all modules including the master itself on the P2 backplane.

The trigger and clock signals are picked up from the bus by both, the master and the slave modules to ensure synchronously data processing. Then the trigger is either delayed by a shift register of programmable length or initiates a predefined sequence. Both methods are equally suitable if only one single trigger has to be propagated to the APVs. The shift register has to be used when a series of incoming triggers shall be forwarded from "TRG In" to the front-end. On the other hand the sequencer is suitable when a series of triggers shall be sent to the APVs after the reception of a single HW trigger. A typical application of this method is the multi-peak mode, when not just 3, but 6, 9, ..., 30 samples shall be read out, which requires the sequences 1001, 1001001, etc. Both the shift register and the sequencer have a (maximum) length of 256 bits and can be configured by VME commands. In addition to the sequence initiated by a HW trigger, three more programmable sequences are foreseen. They can only be issued by software and are used for software trigger, calibration request and (soft) reset. Moreover, a 10 bit DAC with three independent channels is available on the module. An additional programmable sequence is implemented for each channel. One of the DAC channels is connected to the inputs of the ADCs and thus can be used to apply any test pattern or just to define a static baseline offset which is added to incoming signals.

The timing of the sampling clock of the ADCs can be adjusted with another delay (Delay 1). This timing strongly depends on the clock frequency and the length of the analog cables, thus it has to be configured carefully. A special mode (ADC delay scan), which scans all possible delay steps, is implemented in the readout software (see section 6.6) to find the optimum setting.

The "Frame Detection" can be used to detect the beginning and the end of the APV data frames. It is responsible to close the baseline restoration switch on the AC repeater (see 6.3) whenever the APV output is idle. In order to ensure a reliable operation, the timing has to be programmed carefully, considering the cable length between VME module and AC Repeater. This feature can be turned off completely, such that the switch on the repeater is always open.

6.5. Cabling

6.5.1. Hybrid - Repeater

The connection between AC repeater and APV25 hybrid is done by a single 34 wire unshielded flat cable and fine pitch (0.025") connectors. Both cable and connectors are manufactured by Samtec Inc. Their order numbers are listed below:

Repeater side connector: FTSH-117-01-L-DV-EJ-K-A, with ejection mechanics

Hybrid side connector: FTSH-117-01-L-DV-K-A, without ejection mechanics

Cable assembly: FFSD-17-D-xx.xx-01-N, where xx.xx is length in inch

The cable used in the beam tests was 5 cm long, but one with 2 m was also tested in the laboratory. No significant difference in signal quality and noise level was observed between both cable lengths. The results of this comparison are shown in tab. 6.1, where signal and noise are given in ADC counts.

	0.05 m cable	**2.0 m cable**	**difference**
Signal [ADC]	83.25	83.38	+0.2%
Noise [ADC]	1.97	1.99	+1.2%

Table 6.1.: Comparison of two Samtec cables of the same type but different lengths. Both measured signal and noise are averaged over eight APV chips, respectively.

6.5.2. Repeater - APVDAQ module

The AC repeater is connected to the APVDAQ module by three cables, one CAT7 cable for analog signals, a CAT5 cable for trigger and clock and a 34 wire flat cable with twisted pairs for control and power. The connections of both flat and CAT cables are straight, i.e. pin1-pin1, pin2-pin2, etc. with adjacent pairs. Thus, standard Ethernet patch cords are not suitable since they have different pairing. The reason to use CAT7 cables for the analog signal is, that their propagation delay between pairs (skew) is less different than with CAT5. This is important since the APVDAQ module provides only a common ADC clock delay and thus all four channels are sampled by the ADC at the same time.

Cables with 2, 7 and 30 m where tested. While the length does not matter for digital signals (trigger, clock, control) and power, the pre-emphasis circuit of the line driver for analog signals, located on the AC repeater, has to be adjusted to the actual cable length. This is no issue for short cables up to a few meters, but important for the 30 m cables. For this adjustment the capacitor across the 50 Ω resistor (see fig. 6.4 on page 52), which compensates the attenuation of the cable, has to be adapted to the actual length. Proper values for different cable lengths are listed in tab. 6.2. These optimum values were found by trying different capacitors for each cable length. The ADC delay scan (see 6.6.1) of the APVDAQ software was used for these measurements. In this mode a tick mark of the APV25 is recorded with a time resolution of 1 ns. This tick marks are a good emulation of a huge analog signal and its shape becomes distorted when a wrong

Cable length [m]	Capacitors [pF]
≤ 2	68
7	82
30	150

Table 6.2.: Suitable capacitors for the pre-emphasis circuit with various cable lengths.

capacitor is used. Fig. 6.7 shows the resulting signals of the three possible cases, namely under-compensation, optimal compensation and over-compensation.

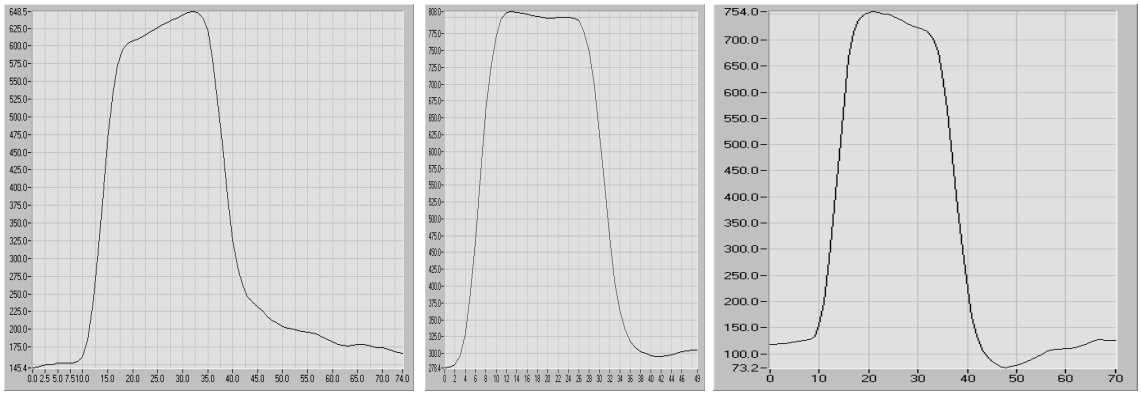

Figure 6.7.: APV25 tick marks recorded with the ADC delay scan of the APVDAQ software. The cable length was 30 m and different capacitors were used in the pre-emphasis circuit. The pulse height is given in ADC counts and the abscissa shows the time in ns.

6.6. Data Acquisition Software

The data acquisition software provides a graphical user interface that allows easy control and readout of the APVDAQ module by the VME interface. It is a Windows application programmed in C with LabWindows^{TM}/CVI from National Instruments [46].

The layout of the user interface is divided into logical sections; a screen shot of it is shown in fig. 6.8. On the left side, there are some control buttons and data fields to configure, start and stop the data acquisition. In the center there is a large graph window, where the raw data and some histograms, which are provided by a simple online analysis (see below), can be displayed. Furthermore, this section contains a meter for the actual trigger rate, a status window, a progress bar (showing the progress of the current run) as well as some other fields to show information about the present state of a run.

The included online analysis provides quick noise calculation, pedestal subtraction, common mode correction and hit finding. These functions are implemented as a simplified version of their equivalents of the offline analysis and will be described in section 7.4. In contrast to the offline analyses, all data are processed at chip level and are indented to give a first impression about the data quality. Various diagrams to be displayed in the graph window can be selected by the huge slide-button down to the right.

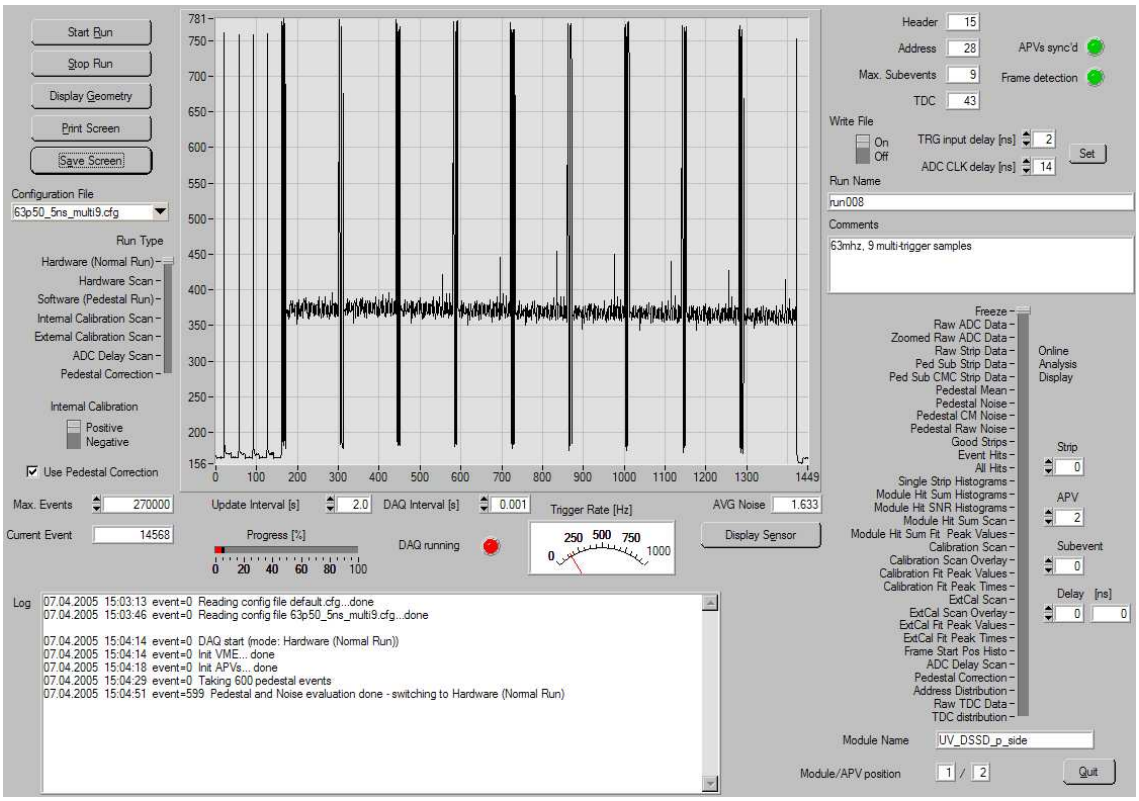

Figure 6.8.: Screenshot of the APVDAQ software, recorded at the beam test in April 2005 at KEK.

A timer based software design was chosen, which allows that the user can interact with the software even when the data acquisition (DAQ) is running. Separate timers for both data acquisition and refresh of the graph window are foreseen. The intervals of these timers are defined by two data fields below the graph. Usually, the update interval (nominally 1 s) is set to a value that is comfortable for the human eye and thus orders of magnitude higher than that of the DAQ timer (nominally 1 ms). When the update interval is set to zero, the display is refreshed with the same rate as data are acquired.

The data fields on the right side are designated to enter data file path, run name and some comments. It can be defined whether the acquired data are written to a file by a toggle-switch nearby. Although the software includes simple data analysis, only the APV25 raw strip data as well as a copy of the actual configuration file (see below) are stored. The strip data are extracted from the APV25 data frames and no further processing is done except for re-ordering such that the saved values correspond to the physical strip order.

Moreover, the software provides a sensor display, which displays a simplified model of the attached sensors based on their definitions in the configuration file. In this display particle hits are indicated by coloring the affected strips in blue (n-side) or red (p-side). Assuming that the sensor configuration is correct, it shows where the sensor is hit by particles and thus allows easy alignment between sensor and particle beam (or source) at a beam test (or a source run in the laboratory).

The software is scalable and can easily be adapted to the actual setup by a configuration file. An overview of the parameters that can be specified in this configuration file is given by the (non-exhaustive) list below.

Configuration file parameters:

- Number of installed APVDAQ modules and their VME base addresses.
- Configuration of the trigger logic, such as number of accepted triggers, usage of shift register or sequencer, entry list of each of the sequencer memories for hardware trigger, software trigger, calibration request and (soft) reset.
- Trigger and ADC clock delays.
- I^2C settings of the APV25 chips. A configuration file can contain more than one such set, which have to be assigned to the installed APV chips elsewhere. These entries define all bias currents and voltages, the peaking time (T_p), the operation mode (peak, multi-peak, deconvolution), the inverter setting and the latency of the APV25 chips.
- Number of APV25 hybrids and their assignment to APVDAQ modules.
- Definition of the actually installed APV25 chips. With these entries the number of installed chips, their I^2C addresses and the reference to a (previously defined) hybrid is given. Furthermore one of the I^2C settings has to be selected for each installed APV25.
- Sensor settings, which define the (basic) geometry of the installed sensors and their connections between the sensor strips and the APV25 channels. Furthermore zones, which are processed separately in the analysis software, can be defined here.
- Bad strips that should not be used for analysis.
- Some parameters concerning the online analysis, i.e. the seed values for hit finding.

The list above shows, that a huge number of parameters has to be defined. They will not be described in detail at this point, but a commented sample file is listed in appendix A.

6.6.1. Run Types

The software provides five run types which can be selected by a slider on the left side of the interface. Independent of the actual run type, the first n (normally 600) events, which are called "Init Events", are taken using random software triggers, where n is an integer number that is defined in the configuration file. These "Init Events", also called pedestal events, are intended to evaluate pedestal and noise of each strip as it is shown in section 7.4. An overview of each run type and its purpose is given below. The implemented data acquisition procedure is similar for all modes and will be described later in section 6.6.2.

Hardware Run

The "Hardware Run" is the default run type used to acquire data at a beam test or a source measurement in the laboratory. After taking the 600 pedestal events, the software polls the veto status of the APVDAQ module periodically. Every time when the veto logic indicates that a trigger was received, the digitized APV data frames are

read out from the ADC FIFOs. As already described above, the raw strip data are then determined from the APV data frames and re-ordered. When the "Write File" toggle-switch is set to "On", the re-ordered strip data are saved in a file without any further processing.

Software Run

The "Software Run" is almost identical to the "Hardware Run", except that the veto logic of the APVDAQ module is disabled and thus no triggers signals coming from particle hits are accepted by the hardware. Instead, the readout of the APV25 chips is initiated entirely by software triggers, which are periodically sent by the software. That means that the data are taken randomly, because there is no correlation between data acquisition and particle hits. This run type is also called pedestal run, because it is used to determine noise and pedestals of the actual setup. As no beam or source is necessary, it is also suitable to check the functionality of a setup in the lab.

Internal Calibration

This run type is intended to record the shape of the calibration pulse of each APV25 chip by using their internal calibration functionality. In order to scan the whole shaping curve with a time resolution of 1/8 clock periods (3.125 ns at 40 MHz), several calibration requests with different timing, each followed by a software trigger, are sent to the APV chips. For each time point an average over a configurable number of samples (nominally 50) is calculated to reduce the influence of noise. The pulse height and the number of calibration groups to scan (see section 5.1.1), the covered time domain and the number of samples per position are defined in the [cal] section of the configuration file (see appendix A).

No raw strip data are saved, but the scanned averaged waveform is written to disk in a text file for every channel.

The calibration run is suitable to check the peaking time and obtain calibration constants (e/ADC) for each channel, which are used in the offline analysis to convert the ADC values into signals given in terms of electrons. Since gain, pedestal and noise level vary between the APV25 chips and/or channels, it is more meaningful to use the converted signals rather than pure ADC values for further analysis.

The software provides a graph where the curve of each channel is drawn separately as well as an overlay plot, which displays the signals of all channels of a specific APV chip together in a single graph. Since the applied charge is shared between shorted channels and thus their calibration signal is significantly lower, the summary graph can be used to quickly identify such shorts. On the other hand, channels which are not connected to the sensor have a lower capacitive load and thus are characterized by a slightly higher calibration signal. As an example, the overlay plot of the calibration signals of one APV25 chip with two shorted channels is shown in fig. 6.9.

Moreover, the normalized average of the calibration curves of all APV25 channels on one side of a sensor was used as a reference shape to perform a fit on the measured samples and determine the real hit time (see section 7.6).

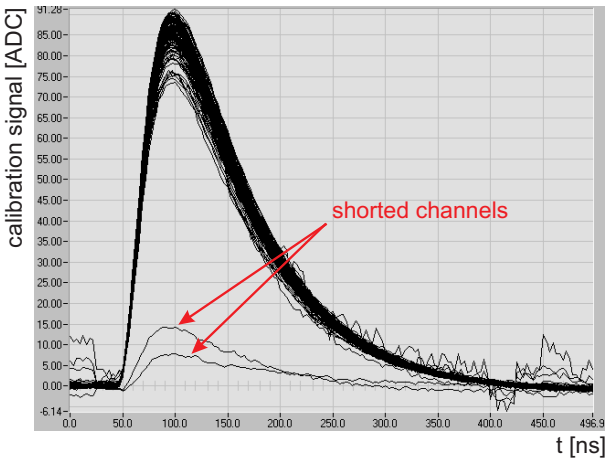

Figure 6.9.: Overlay plot of the internal calibration signal of an APV25 chip with two shorted channels. T_p was set to the nominal value of 50 ns.

ADC Delay Scan

As mentioned in section 6.4, the timing of the ADC sampling clock strongly depends on the clock frequency and the length of the analog cable. It can be adjusted by a delay chip located on the APVDAQ VME module. In the ADC delay scan an APV25 tick mark is sampled with a resolution of 1 ns by scanning all possible delay settings. Thus, this run type is suitable to find the optimum setting of the ADC clock delay. An average over 300 samples is built for each delay step to minimize the influence of noise. Starting with 0 ns, the delay is adjusted in steps of 1 ns. Since the scan should cover the range of one clock period, the total number of delay steps is chosen according to the clock frequency. For a clock frequency of 40 MHz, the delay is adjusted between 0 and 24 ns, as an example.

The result of this run type is a graph (see fig. 6.7 on page 57) which displays the scanned pulse as a function of time. The required delay setting can be determined from the abscissa of this plot. As there is only a common clock delay for all four analog channels, it is sometimes necessary to trade of between channels and find a setting, which is suitable for all of them, but may be not the optimum of a specific channel. No data are saved to disk in this run type.

Pedestal Correction

The pedestal correction generates a file that is intended to compensate a kind of aftermath caused by a slow component of long cables used in the analog path. This effect was first recognized during the preparations of a beam test (PSI, August 2005) for which cables with a length of 30 m were required. Measurements had shown, that the noise of the channels 0, 32, 64, 96, 8, 40, ... of each APV chip is significantly higher than those of the other strips, when such long cable are used. The sequence of affected channel follows the order in which their analog signal is transmitted by the APV25 chip. Furthermore, this effect decreases with increasing position of the channel data within the APV data frame.

The header of the APV frame, which consists of digital data with huge amplitude (see section 5.1.4), was identified to cause this effect. The distortion depends on the pipeline address transmitted in the header, the cable length and the clock frequency. Thus, the

analog data can be corrected in a proper way by subtracting a constant value for each channel and pipeline address as shown in eq. 6.1

$$d\_corr_i = d_i - ped_i - pcorr_{i,a} \quad , \tag{6.1}$$

where d is raw data of channel i, ped_i its pedestal (obtained from the initial events), $pcorr_{i,a}$ the corresponding correction value for the pipeline address a and d_corr_i stands for the corrected and pedestal subtracted analog signal.

The aim of the pedestal correction run is to obtain such $pcorr_{i,a}$ values and save them in a file, which can be used by the analysis software to perform the correction described above. Therefore a pedestal run at high statistics is executed, which builds an average over about 300 samples of the analog data for each channel and pipeline address. At the end of the run, the actual pedestal, which is determined from the (600) initial events, is subtracted and the results are saved in a two-dimensional array. Its first dimension is the channel number, the second one corresponds to the pipeline address. Finally this array is written to a (pedestal correction) file.

Although this method was successfully used to analyze a huge number of beam test data, a hardware solution, such as an equalizer at the receiver part that compensates these effects, would be preferable for the readout electronics of the future Belle detector.

6.6.2. Data Acquisition Procedure

After selecting a run type and pressing the "Start Run" button, the data acquisition procedure is characterized by the flow chart shown in fig. 6.10. Each run starts with an initialization phase, where the times are configured and some internal variables and data memories are set accordingly to the run type. Then the configuration of the APV25 chips, including operation mode, bias current settings, latency, etc. as well as the current values of the trigger and ADC clock delays are sent to the APVDAQ hardware. Once this is done, the run will be started and the software waits for the timeout of the DAQ timer.

When this timeout occurs the data acquisition is continued according to the actual run type. In case that "Hardware Run" was selected and all "Init Events" were already taken, the veto status, which indicates that a trigger was received by the hardware and data are pending, is read out from the APVDAQ module. In all other run modes a software trigger and/or a calibration request is sent by software, and it can safely be assumed that data are available anyway. If data are available, they will be read out and passed to the raw data processing, where the strip data are extracted from the APV25 data frames, re-ordered and stored in an array for each APV and sub-event (sample). Furthermore the actual number of sub-events is calculated and compared to the configured value and the error status of the APV chips, which is encoded in the frame header (see 5.1.4), is checked. If an error is detected, the whole event is discarded and a (soft) reset is sent to the APV chips, otherwise a simple online analysis is performed. The results are stored in arrays and can be displayed in the graph window as described before.

When the toggle-switch "Write File" is set to "On" and the actual run type is either "Hardware Run" or "Software Run", the raw strip data, including those of the 600 initial events, are saved in a file in the next stage. This is not done for the other run modes, because they provide special functionality and generate summary files at the end of each run.

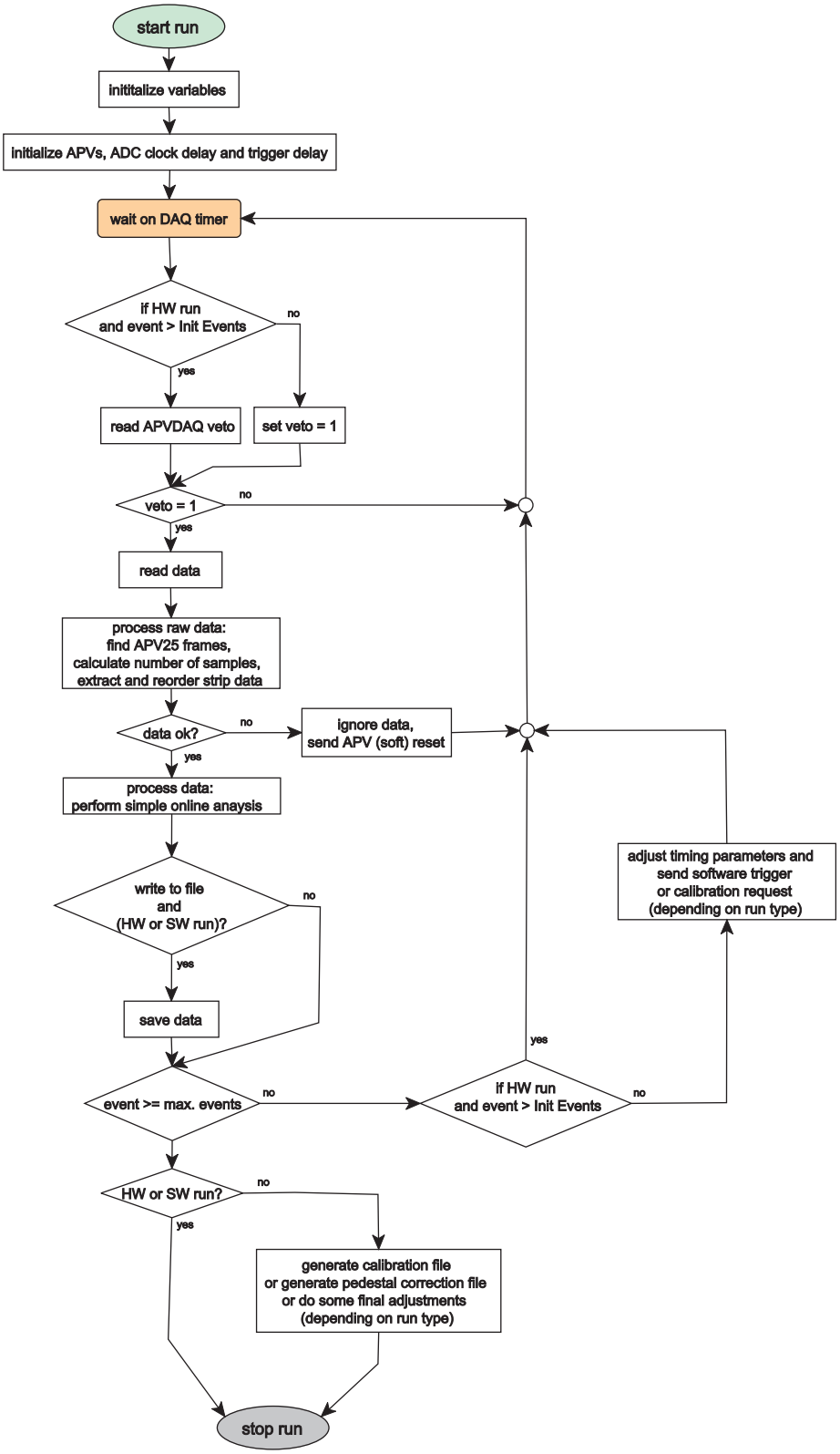

Figure 6.10.: Flow chart of the APVDAQ software.

In case of "Hardware Run" the data acquisition is now finished and the software returns to idle state, where it awaits the next DAQ timer event. The other run types require some additional adjustments, which will be done in the next step. Furthermore, a software trigger and/or calibration request has to be sent in these cases, before the software returns to idle state.

The above steps are repeated until a predefined number of events is reached or the "Stop Run" button is pushed by the user.

7. Measurements and Results

Several sensor modules, all read out by APV25 chips, were built to study the upgrade options of the Belle SVD. Particularly those are a test setup, called "Long Line", with a more than 50 cm long fanout between a single-sided sensor and the APV chips and two modules using the UV striplet detector (see section 5.2). The first UV sensor module is equipped with one APV25 hybrid and supports single-sided readout of the UV striplet. At the second UV module both sides of the sensor are attached to hybrids and read out by the APVDAQ system.

The setup of the "Long Line" and the double-sided UV module and the results of several beam tests and measurements performed in the laboratory using a ^{90}Sr source are discussed in this chapter. Furthermore, a description of the analysis software is given and a sample implementation of the peak time reconstruction method (see section 4.2) is presented.

7.1. Long Line

The "Long Line" is a test setup intended to evaluate the behavior of the APV25 when a long fanout is used between sensor and readout chips. Particularly, signal quality, signal to noise ratio (SNR) and stability of the chip under such conditions are studied.

7.1.1. Setup

The setup consists of a single-sided silicon strip detector connected to an APV25 hybrid by a printed circuit board with 384 fine lines at a pitch of 80 μm and a length of about 50 cm. An image and the principal design are shown in fig. 7.1. As there was no Belle sensor available at that time, the IB1 type of the CMS tracker was used instead. It is 12 cm long, 320 μm thick and has a pitch of 80 μm. The hybrid is equipped with three APV chips, which are connected to the "Long Line" by a pitch adaptor made of glass.

Two types of PCBs with slightly different geometry were compared. One was manufactured by ILFA Feinstleitertechnik GmbH, Germany, the other one was made at CERN, Switzerland. Both vendors got the same specifications concerning the width of strips and gaps. Depending on their different production techniques the results show minor deviations with respect to the given geometry. While IFLA used laser technology to cut out the gaps from a copper coated board, the CERN type is made in a conventional etching process. The electrical and geometrical parameters of both types are shown in tab. 7.1. C_{int} is the (inter-strip) capacitance between adjacent lines, C_b the capacitance between a line and a grounded backplane (a 3 mm thick Al plate placed below the "Long Line") and R_s the ohmic resistance of a single line. The given resistance is an average of about 150 individual measurements using a multimeter (Metex M-4630), where both ends of a line were contacted by probe needles. The resistance of the cables and the contact resistance of the probes were subtracted from the measured values. Furthermore,

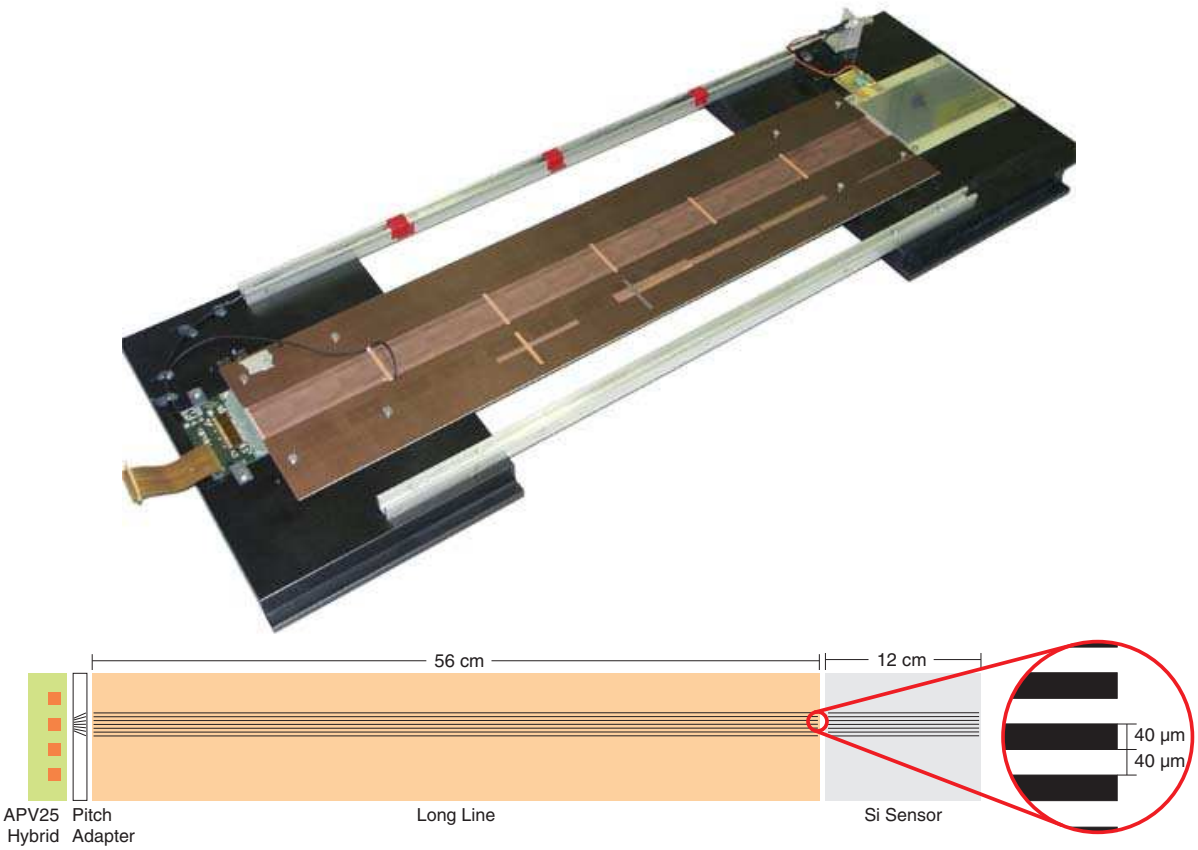

Figure 7.1.: Image and schematic view of the "Long Line". The depicted PCB was manufactured by ILFA Feinstleitertechnik GmbH, Germany.

	"Long Line" type	
	ILFA	**CERN**
Strip width:	55 μm	35 μm
Strip gap:	25 μm	45 μm
Length:	530 mm	550 mm
Metal:	17 μm Cu	5 μm gold plated Cu
C_{int}:	20 pF	14.5 pF
C_b:	9.3 pF	5.7 pF
R_s:	13 Ω	122 Ω

Table 7.1.: Mechanical and electrical characteristics of the two long fanouts. C_{int} is the inter-strip capacitance and R_s the ohmic resistance of the line.

the resistance between adjacent lines was measured to identify shorts.

In a first attempt, the ILFA type had several shorts and the average resistance between neighbors was about 10 kΩ, which is actually a poor value. The reason was that the copper between the lines was not fully removed by laser cutting. After an additional etching step performed by ILFA, most of the shorts were removed and the resistance between the lines was about 1.5 MΩ and thus sufficiently high.

The gap of the CERN type is about 35 μm and thus larger than that of the ILFA (25μm) "Long Line". Only two shorts were found on this board and the resistance

between two lines is higher than the range of the ohmmeter. As the lines of this PCB are only 45 μm wide and 5 μm thick, their resistance is about 123 Ω, which is ten times more then that of the IFLA type.

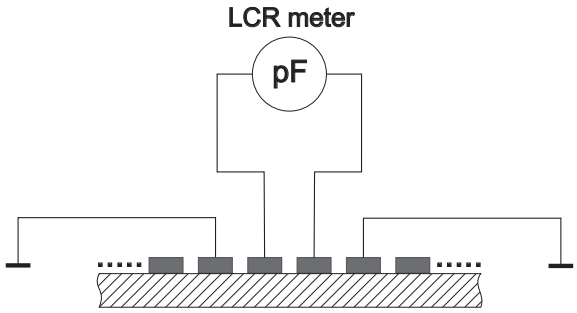

Figure 7.2.: Measurement of the capacitance between two adjacent lines (C_{int}). Each line is contacted by a probe needle and the left and right neighbors are grounded.

An Agilent HP4285A LCR meter was used to determine both C_{int} and C_b, respectively. Similarly to the R_s measurement the lines were contacted by fine probe needles. A 3 mm thick, grounded Aluminum plate was put under the "Long Line" and the capacitance between this plate and the lines was measured in order to determine C_b. As shown in fig. 7.2, C_{int} was measured between two adjacent lines, while their left and right neighbors were grounded. All values of the CERN board, which are listed in tab. 7.1, are averaged over several measurments, too.

Since the APVDAQ hardware was not available at that time, its predecessor and a previous version of the data acquisition software was used for readout. This readout electronics provides less functionality than the APVDAQ system and can not be used for double-sided sensors, but it is sufficient enough for the single-sided "Long Line" module. Similarly to the APVDAQ system, it consists of a repeater and some VME boards. In this system the functionality of one APVDAQ VME module was distributed onto three separate VME cards, a controller that provides clock, trigger and power supply for the APV chips, an ADC board to digitize the analog signals and a VME I^2C master to configure the APV chips via the I^2C bus. Since this readout system is already obsolete and the new APVDAQ system (see section 6) provides more functionality and flexibility the old system will not be described in more detail here.

7.1.2. Results

Several internal calibration and some source runs using a ^{90}Sr source were performed for both "Long Line" types. The calibration pulse was recorded after finishing each stage of module assembly. In particular, such measurement was done with the hybrid only, the hybrid bonded to the pitch adaptor and the "Long Line" as well as the final setup. Bias settings of the APV25 preamplifier and shaper were adjusted to obtain a shaping time of 100 ns with no input load.

The results of the calibration runs for both types are shown in tab. 7.2. Caused by the high capacitive input load the shape of the calibration curve was stretched and the peaking time increased from originally 100 ns to 135 ns and 120 ns for the ILFA and CERN "Long Line" boards, respectively. Apart from that effect, the setup showed good performance and no negative behavior, such as oscillation of the APV chips, was

		Peak Signal [ADC]	**Average Noise** [ADC]	[e]	**SNR** (single strip)	**T_p** [ns]
	Hybrid only	64	1.33	472	48	100
ILFA	Hybrid + "Long Line"	58	5.93	2300	9.8	130
ILFA	Hybrid + "Long Line" + Sensor	55	6.97	2851	7.9	135
CERN	Hybrid + "Long Line"	62	5.51	2000	11.3	120
CERN	Hybrid + "Long Line" + Sensor	60	6.8	2550	8.8	125

Table 7.2.: Peak signal, average noise, SNR and shaping time of the "Long Line" obtained from measured calibration pulses. The noise in electrons is calculated assuming that the peak signal corresponds to 22500 e (1 MIP).

observed. An average noise of about 6.97 ADC was measured for the ILFA type, while that of the CERN board was 6.8 ADC and thus slightly lower, corresponding to the total input capacitance values. Assuming that the calibration pulse produces the same charge as a MIP (22500 e), the noise values above correspond to 2851 e and 2550 e. Consequently the SNR of the CERN is lightly higher. The obtained values are about 8.8 and 7.9 for the CERN and ILFA types, respectively.

	MP Signal [ADC]	**Average Noise** [ADC]	[e]	**Average Cluster Width**	**MP SNR (cluster)**
ILFA	77.24	7.63	2223	1.79	8.2
ILFA shielded	74.25	7.34	2219	1.78	8.3
CERN	74.25	7.19	2179	1.64	9.2

Table 7.3.: Source measurements results of both ILFA and CERN "Long Line", respectively. For signal and SNR the most probable (MP) value is obtained from a fit using a convolution of Gauss and Landau distributions.

The results of the source runs are listed in tab. 7.3. Again the values of the CERN type are somewhat better than that of the ILFA "Long Line". For both setups the amplitude of the measured signal followed the typical Landau distribution and did not show any noticeable problems. Depending on the particular APV chip common mode noise between 10 and 30 ADC was observed for the ILFA type, while that of the CERN "Long Line" was between 4.5 and 13 ADC. The common mode noise is the fraction of the noise that affects all channels in the same manner and thus can be removed by the analysis software (see section 7.4). Similar to the signal, the SNR also follows a Landau distribution. Hence, the most probable (MP) value was obtained by a fit using a convolution of Gauss and Landau distributions. The resulting (MP) SNR was about 8.2 for the ILFA type and 9.2 for the CERN sample. Furthermore, the benefit of shielding was tested by placing a grounded Aluminum plate on top and beneath the "Long Line", but no significant improvement was obtained.

A direct comparison with the SNR given in tab. 7.3 is not suitable, because the values

obtained from the calibration pulse are calculated using the average noise and thus assuming a cluster width of one, while for the source measurement results the actual cluster signal and cluster noise was used. Since the noise contributions of all strips of a cluster are uncorrelated, the square sum corresponds to the total cluster noise. Assuming that the noise of every single strip is equal to the average noise, the single strip SNR has to be divided by the square root of the mean cluster width to get the signal to noise ratio of the cluster. Doing so, the SNR obtained from the calibration pulse becomes about 6 for the ILFA "Long Line", which is slightly lower than the result of the source measurement. There are two possible reasons for this deviation, either the amplitude of the test pulse was programmed to low (see section 5.1.1) or the source signal was slightly above a MIP. Truly reliable values can only be obtained in a beam test using minimum ionizing particles, but such a test was never performed for the "Long Line" setup as the intention was not to measure precise SNR, but rather investigate stability and overall performance of the "Long Line".

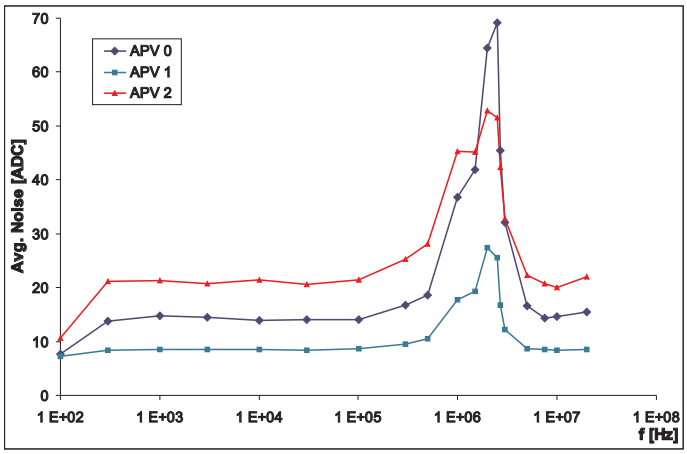

Figure 7.3.: Frequency response of the noise of the APV25 chip caused by a sine wave signal applied to plates on the top and beneath the "Long Line".

In a further measurement the sensibility of the APV chips on interfering signals was tested. A sine wave of about 40 mV_{pp} was applied to two Aluminum plates, placed on the top and beneath the "Long Line". Then the average noise level was measured for several frequencies in the range from 100 Hz to 20 MHz using the software run of the DAQ software. The results are shown in fig. 7.3, where the noise level of each APV chip is plotted as a function of the frequency of the applied signal. A significant peak of the noise was observed around 1 MHz for each of the three APV chips. That means the APV25 chip is sensitive to disturbing signals in the range from approximately 300 kHz to 5 MHz and hence such frequencies should not be present anywhere near the APV chips. The problems with the DC/DC converter which was originally foreseen on the AC repeater (see section 6.3), is an example of such a disturbance.

7.2. The UV Sensor Module

The UV module was built to study the performance of the new UV striplet sensor, previously described in section 5.2. The sensor is clamped and glued between two almost identical frames, which are rotated by 180 ° to each other and mounted together by

screws. Each frame has an opening that allows to mount one APV25 hybrid (see 6.2) onto the other frame and bond it to the sensor. An image of both sides of the module is shown in fig. 7.4.

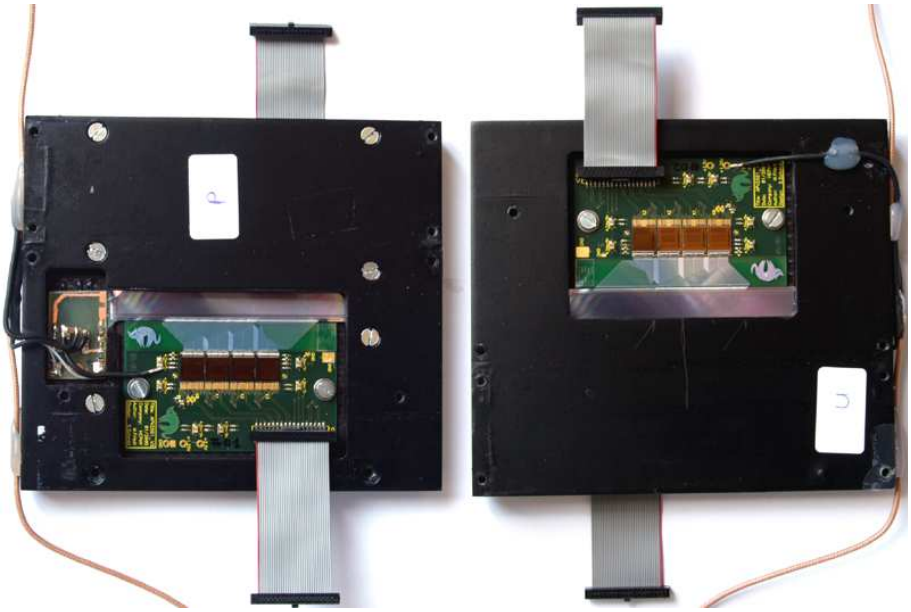

Figure 7.4.: Image of both p-side (left) and n-side (right) of the UV sensor module.

On each side of the sensor, 512 of the 1024 strips are read out by four APV25 chips. A pitch adapter made of glass is used to convert the skewed pitch of the sensor to the straight and staggered pitch of the APV25 chips. Due to the special design of the pitch adapter the 384 channels of the first three APV chips on each side are connected to every readout strip of the sensor, while the 128 of the fourth chip are attached to every second readout strip. Hence the readout area of the sensor is divided into two zones with readout pitches of 51 μm and 102 μm, respectively. A sketch of the UV module is depicted in fig. 7.5. The p-side hybrid is drawn in top view, while that of the n-side is mirrored and thus shown in bottom view. In order to point out the two different zones of the sensor with a readout pitch of 51 μm and 102 μm, respectively, all strips connected to the first three APVs are drawn in red and those attached to the fourth chips are colored blue. The resulting readout configuration is listed in tab. 7.4 for both zones and sides.

readout pitch (zone)	**51 μm**	**102 μm**
readout strips	384	128
configuration p-side	ro/int/ro	ro/int/int/int/ro
configuration n-side	ro/p/ro	ro/p/int/p/ro

Table 7.4.: Readout configuration of the UV module, ro = readout strip, int = intermediate strip, p = p-stop.

At the 51 μm zone of the p-side there is already one intermediate strip (int) between two readout strips (ro) and thus the resulting configuration for the 102 μm zone yields three intermediate strips. On the n-side there is a p-stop instead of an intermediate strip

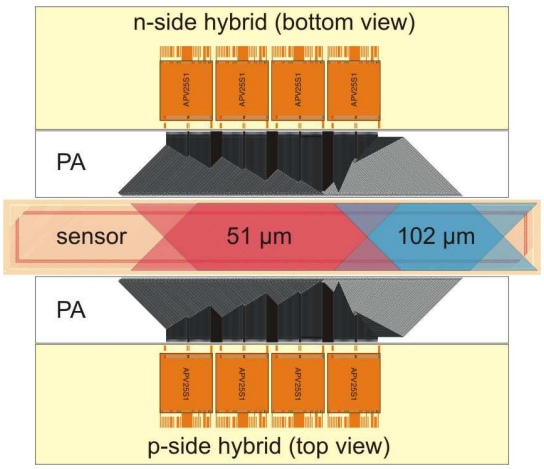

Figure 7.5.: Schematic view of the UV module, natural size. Sensor, pitch adapters (PA) and hybrids of both p-side (top) and n-side (bottom), respectively, are depicted. The readout strips of the 51 μm zone are colored red, those of the 102 μm zone are blue.

between two readout strips of the 51 μm zone. Hence, the corresponding configuration of the 102 μm zone has a single intermediate strip.

The bias voltage for both sides is applied through a low-pass filter, placed on a small PCB beside the sensor on the p-side of the module. The p-side bias ring is bonded directly to the -HV pad of this PCB, while that of the n-side is connected via an (almost) ohmic contact through the sensor[1] at the corner of the sensor called "n-sub".

7.3. Beam Test Setup

Two beam tests were performed to evaluate the APVDAQ system and the UV sensor module. The first was at KEK in April 2005, the other one at PSI in August 2005. Pions (π^+) at a momentum of 4 GeV/c and 300 MeV/c were used at KEK and PSI, respectively. The setup for both beam tests was almost identical, except that the length of the cables between AC repeater and APVDAQ module were 7 m at KEK and 30 m at PSI, imposed by the distance between beam area and control room ("counting house").

A block diagram of the experimental setup is shown in fig. 7.6. The standard configuration of the APVDAQ system for double-sided silicon sensors, as described already in section 6, was used for the main readout electronics. It consists of the UV module with each of its hybrids connected to an AC repeater and APVDAQ module, respectively.

A 12 × 12 mm^2 large scintillator, mounted between two photomultiplier tubes, was used as a trigger unit. The coincidence of the output signals of the photomultipliers was formed to a pulse with a duration of either 5 ns or 30 ns by some NIM[2] electronics. The time window with respect to the next clock edge of the APVDAQ system during which triggers are accepted is defined by the length of this trigger pulse. Both the 5 and 30 ns trigger windows were used alternately during the measurements at the beam tests. At a clock frequency of 40 MHz and above the 30 ns signal ensures that all incoming triggers

[1] n^+ implant on both sides of the wafer with n-type bulk.

[2] NIM stands for "Nuclear Instrumentation Module" standard, which defines mechanical and electrical specifications for electronics modules used in experimental particle and nuclear physics.

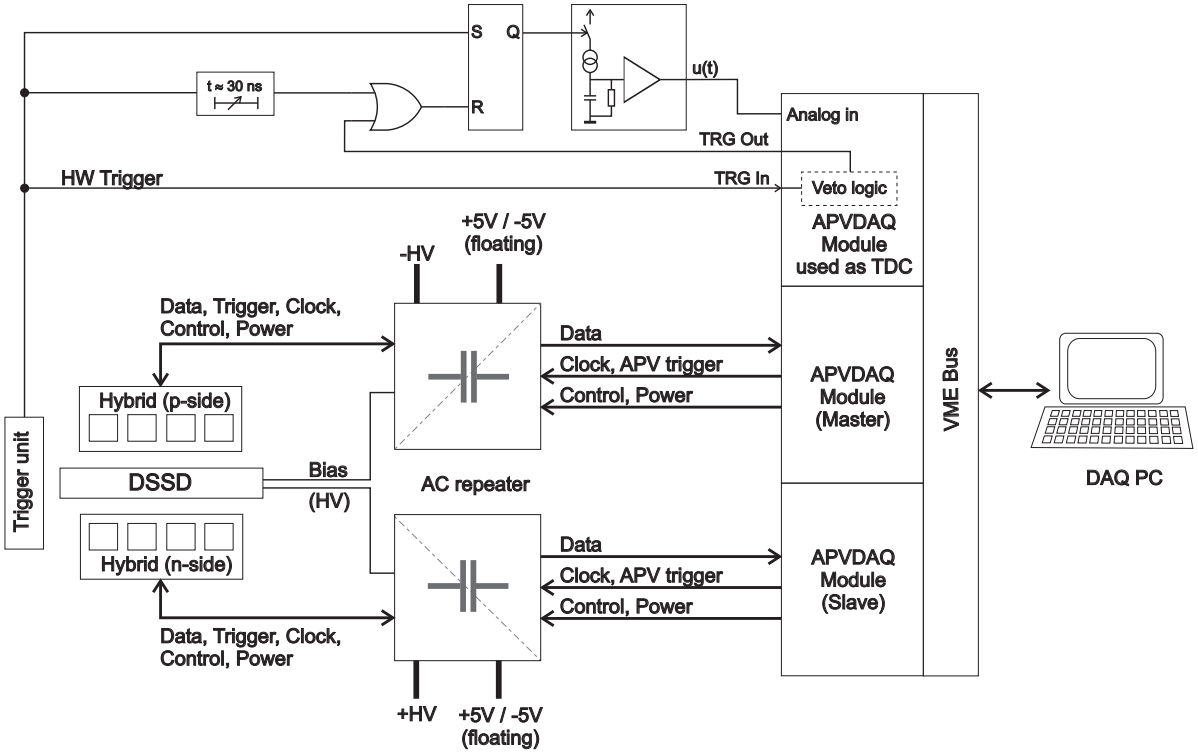

Figure 7.6.: Block diagram of the setup of both the KEK and PSI beam tests.

are accepted by the trigger logic of the APVDAQ module (see fig. 6.6 on page 54), because in that case the clock period is shorter than the trigger pulse width.

In addition to the standard components and the trigger unit, a time to digital converter (TDC), which will be described below, was used to measure the time between the incoming trigger and the clock synchronized trigger of the APVDAQ module. In the analysis, this measured time was used as a reference to verify the results of the hit time reconstruction method (see section 7.6.2).

7.3.1. Time to Digital Converter

The principal circuit of the TDC is shown in the top area of fig. 7.6. It consists of an RS flip-flop, a small printed circuit board equipped with an RC element and an amplifier, some NIM logic and a third APVDAQ VME module, which is operated as clock and trigger master and its veto logic is used to control the time measurement.

This circuit is intended to measure the charge collected by the capacitor during the time it is pumped up by a current source. When a trigger arrives, the RS flip-flop is set. This turns on the switched current source and thus starts charging the capacitor. At the same time the trigger and veto logic of the APVDAQ module is activated, where the incoming trigger is synchronized to the system clock. This clock synchronous trigger signal is then propagated to the "TRG Out" output. As this output is connected to the reset of the RS flip-flop, the current source and thus the charging of the capacitance is stopped by the synchronized trigger signal. The charging period can also be stopped after a timeout of about 30 ns, in case the incoming trigger is not accepted by the veto logic and hence does not propagate to "TRG Out".

The voltage at the capacitance rises linearly during the charging period and falls

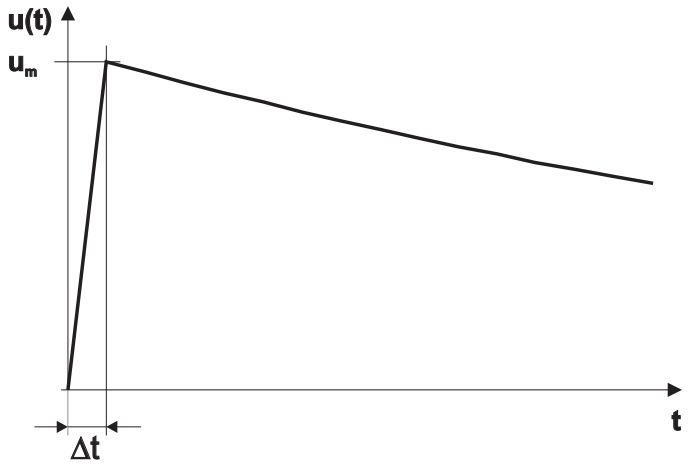

Figure 7.7.: Principal shape of the output voltage of the amplifier attached to the RC element, which is used to measure the time (Δt) between incoming and clock synchronized trigger signals.

exponentially with a time constant of about 44 μs once the current source is turned off. Its peak value corresponds to the time (Δt) between incoming and clock synchronized triggers. This voltage is not measured directly, but passed through an amplifier, which also converts it into a differential signal as expected by the APVDAQ analog input. The resulting (differential) output signal of this circuit is shown in fig. 7.7, where u_m is the voltage which is measured by the analog channel of the APVDAQ module. u_m scales with Δt, since the charging slope is constant.

The characteristic of the TDC circuit is given by

$$\Delta t\,[\mathrm{ns}] = k\,[\mathrm{ns/ADC}] \cdot u_m\,[\mathrm{ADC}] \quad , \tag{7.1}$$

with the slope k and the voltage u_m sampled by the ADC. The slope was determined to be 0.158 ns/ADC by measurements using an input signal with a defined delay relative to the APVDAQ clock instead of uncorrelated trigger signals. Even though this TDC is constructed with very simple means, a precision of 121 ps RMS was measured with the defined delays over the full operating range.

7.4. Analysis Software

7.4.1. Overview

The analysis software consists of three steps, which have to be executed sequentially. A LabWindows^{TM}/CVI application called "APVDAQ Analysis" is used in the first stage to process the raw data of the APVDAQ software and perform hit finding and zero suppression. Then the peak time and signal amplitude of each found hit is reconstructed by a Linux program based on the CERN ROOT [47] framework. Finally the results of both stages are filled into several histograms like signal, SNR, noise, cluster width etc. for subsequent graphical display by a ROOT script.

The analysis procedure of the "APVDAQ Analysis" software (stage one) and particularly the new two-dimensional clustering method are discussed below. A detailed description of the hit time reconstruction software is given in section 7.6. The main

task of the last stage is to combine the results of the former two steps, prepare them for graphical display and perform some fits on the resulting histograms to obtain several parameters such as the most probable signal amplitude and SNR. This is done using several standard classes of the ROOT framework and will not be described in detail here.

7.4.2. Analysis Procedure

The "APVDAQ analysis" uses three input files, the data file of the data acquisition software, a calibration file containing the calibration constants of each APV25 channel (see 6.6.1, page 60) and a pedestal correction file to compensate the aftermath of long cables as described on page 61. Each of these files was generated by the data acquisition software during the beam tests using different run modes[3]. The pedestal correction file is optional and only necessary for long cables, while the two others are required anyway.

The measured ADC value ($S_i{}^{ADC}$) is a convolute of several contributes and is given by

$$S_i{}^{ADC}(k) = S_i{}^{part}(k) + P_i + N_i(k) + N_{CM}(k) \quad , \tag{7.2}$$

where k denotes the event and i the actual strip number [23]. $S_i{}^{part}$ is the signal of the traversing particle, P_i the pedestal (DC offset) and N_i the random (uncorrelated) noise contribution of each individual channel, respectively. The last term is the common mode noise ($N_{CM}(k)$), which is the fraction of the noise that affects all channels in the same manner. While P_i and N_{CM} can be removed by the analysis, this is not possible for the individual strip noise.

At the beginning of each data file there are 600 events, which are taken with random (software) triggers by the DAQ software. An average of the first 200 of them is used to determine the pedestal of each channel. Then the strip noise is obtained from the remaining 400 initial events. This is done in two passes using 200 events for each iteration. Often, pedestal and noise values are updated throughout the run, however this is not done by our analysis software, because investigation of pedestal and noise history throughout a run shows that they are perfectly stable and thus do not need any update.

Once the initial events are treated, all (real) events of the data file are processed according to the flowchart depicted in fig. 7.8. First the event is read from the file and the pedestals are subtracted. Then a two-stage common mode correction (CMC) is performed. CMC is done for groups of 32 channels, which is a legacy from the previous APV version (called APV6), where this was necessary. Event though CMC correction in groups of 32 strip works fine, it might be replaced by chip-wise (128 strips) CMC in a future version of the analysis software.

In the first iteration, the average of the pedestal subtracted signals ("pedsub") of the strips of a group is built. The five highest and lowest values are excluded to avoid an influence of strips with high noise level and those actually carrying the signal of a particle hit. Then the (temporary) pedestal subtracted and common mode corrected signals ("pedsubcmc") are calculated by subtracting the resulting common mode noise from the "pedsub" values for each strip.

[3]These run modes are hardware run (data file), internal calibration (calibration file) and pedestal correction (pedestal correction). A description of them is given in section 6.6.1.

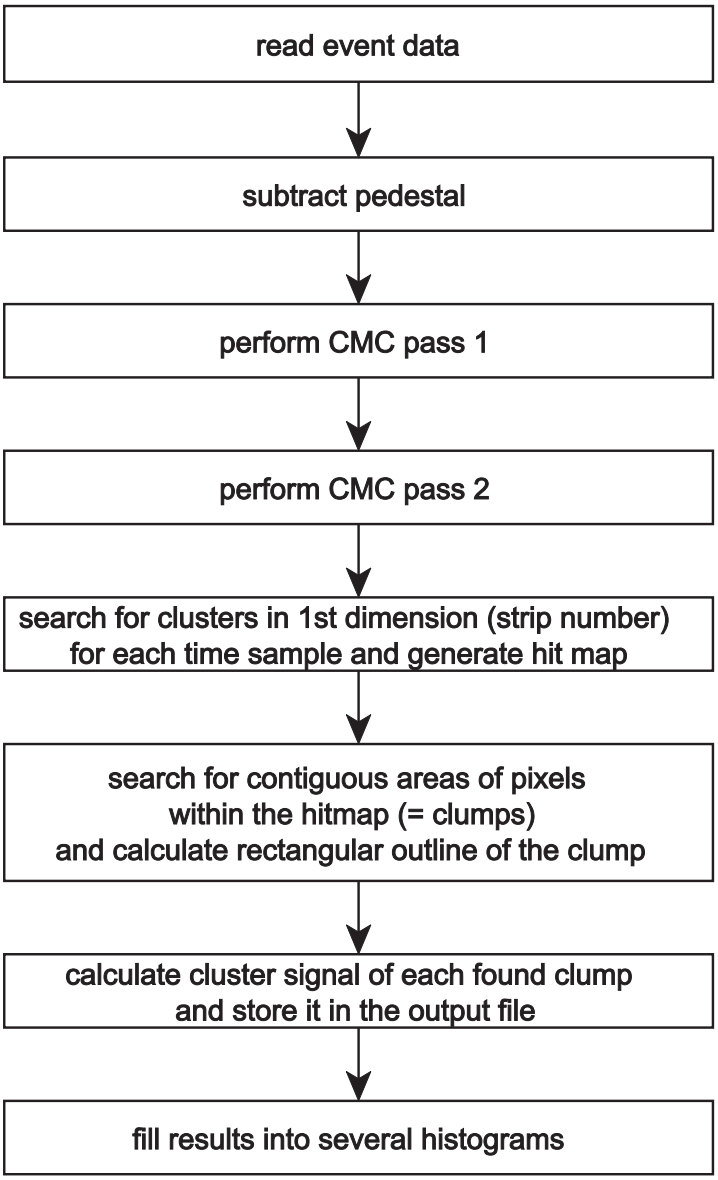

Figure 7.8.: Flow chart of the analysis procedure applied to the data of each event.

In the second CMC iteration, the average of the "pedsub" signals of each group is built again, but now all strips with "pedsubcmc" higher than a given threshold (5 × strip noise), hence all strips probably carrying a hit signal, as well as dead strips are excluded. Then the "pedsubcmc" signal of each strip is calculated again using the common mode noise of the second stage. Referring to eq. 7.2, the resulting "pedsubcmc" values consist of the particle signal (if the strip was hit) and the strip noise, which is random and cannot be removed.

All steps of the analysis described above are processed on chip level, for each APV25, while the following hit finding procedure is performed for each hybrid and zone (51 μm and 102 μm), respectively. Usually the charge deposited by a particle is shared by a group

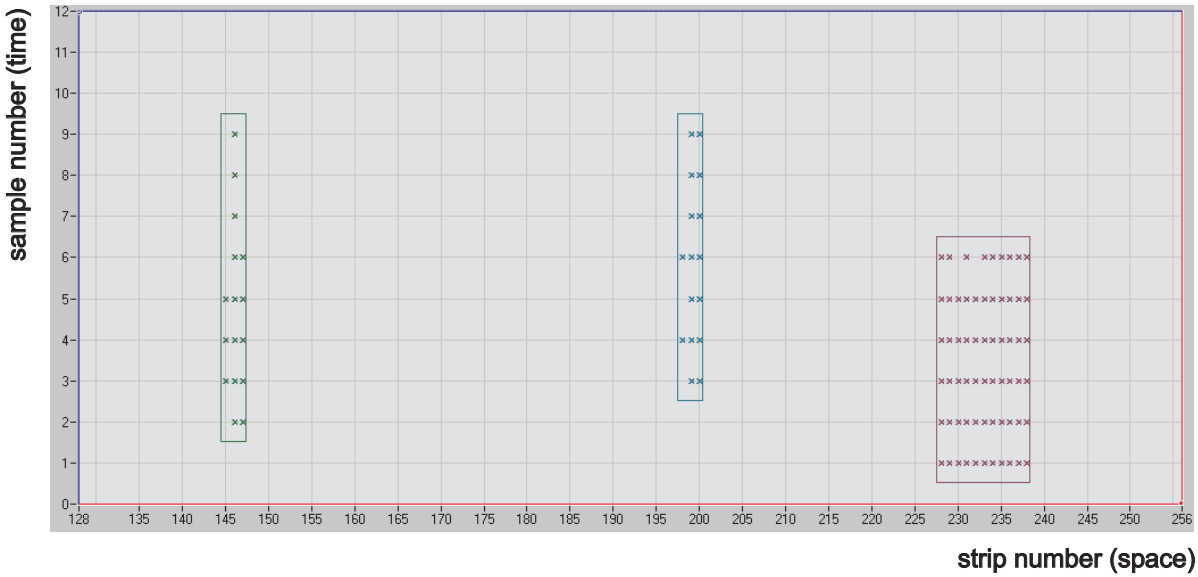

Figure 7.9.: Three contiguous hit areas identified by the clump finder of the analysis software. All hits above threshold are marked with an ×, and surrounding rectangles show the outlines of the clumps.

of neighboring strips, which is called cluster. The next step of the analysis searches for such clusters by using three different thresholds: one for the seed strip (typically 5 × N_i), one for the neighboring strips (3 × N_i) and one for the total cluster signal (5 × $N_{cluster}$). These thresholds (5/3/5) are typical values, which yield good results for the beam test data. However, in some cases it might be suitable to choose other thresholds, depending on the actual setup and signal quality.

As multiple consecutive samples along the shaping curve are taken, cluster finding is performed into a two-dimensional space, spanned by strips (space) and samples (time). This task is split into two stages. The first one searches for channels carrying a signal higher than the given thresholds for each sample separately and marks the corresponding entries (pixels) of a two-dimensional hitmap, where one dimension (x) denotes the strip and the other one (y) the sample number, respectively.

In the second stage, contiguous areas of pixels (clumps) within the hitmap are identified and the rectangular outlines of these clumps are calculated. This means that each clump is widened to the smallest surrounding rectangular. This is necessary, because a strip which carries only a small fraction of the cluster signal might be above the threshold for some samples, but below for the rest of the hit. However, in order to achieve correct cluster signal and noise values for each sample, the contributions of all strips

involved with the particle hit have to be considered in the same way for each sample. An example of such clumps is given in fig. 7.9, where the hits found in the first stage are marked with an × and the clumps are given by the surrounding rectangles.

The cluster signal and noise of all found hits (clumps) are determined after clump finding . For the cluster signal the sum of the strip signals is built for each sample. Since the strip noise is uncorrelated the square sum of the individual contributions is built to calculate the cluster noise. Only clumps with a cluster signal above the cluster threshold, which is typically five times the cluster noise ($5 \times N_{cluster}$), are accepted.

Finally, the results are filled into several histograms and stored in an output file together with additional information of the hit, such as event number, location in space and time, cluster width, zone number and TDC value.

7.5. System Performance

Numerous series of measurements were performed at beam tests in order to test the efficiency of the UV module and the APVDAQ test system, where several parameters like bias voltage (HV scan), angle between sensor surface and particle beam (angle scan), peaking time of the APV25 chips and readout clock frequency were varied. A meaningful overview of the performance of a silicon strip detector and the used readout electronics is given by the distributions of signal amplitude, cluster width and signal to noise ratio, respectively. These values were determined from the raw data using the analysis chain described above in section 7.4 and compared to the values expected by theory.

The overall performance of the APVDAQ system and the UV module was excellent. They worked reliably without any problems throughout the beam tests, which each took several days and resulted in a total of about 90 GB recorded raw data.

The distributions of signal amplitude and SNR of both zones (51 μm and 102 μm) and sides of the UV module, respectively, are shown in fig. 7.10. These results are obtained from a measurement perfomed at KEK (run019) using nominal settings for peaking time (T_p = 50 ns), clock frequency (f_{clk} = 40 MHz) and bias voltage (U_{bias} = 80 V). The signal distributions of both zones of the p-side as well as the 51 μm of the n-side perfectly match the expected Landau shape, convoluted with a Gaussian component, which accounts for electric noise and intrinsic detector fluctuations.

On the n-side there is a p-stop between two readout channels (see tab. 7.4 on page 70) instead of an intermediate strip (as on the p-side) and thus charge sharing is not so effective. This results in most hits featuring a cluster width of one or two on the n-side. While the charge a MIP deposits in the sensor and thus also the amplitude of the cluster signal is almost independent of the width of the cluster in case of efficient charge charing (p-side), the cluster noise is given by the square sum of the contribution of each involved strip and thus increases with the cluster width. Assuming that the noise contribution of each channel is essentially the same, the cluster noise increases with the square root of the cluster width. As clearly seen in fig. 7.10, this directly affects the signal to noise ratio and leads in a significant distortion of the SNR distribution, which is therefore split up depending on the cluster width. At the 102 μm zone of the n-side this effect is even more noticeable, because there are two p-stops between the readout strips. The result is an enveloping SNR distribution with two peaks for the most likely cluster widths one an two, respectively. Moreover the charge charing is very inefficient at this zone and thus even the curve of the signal amplitude is distorted, showing two peaks.

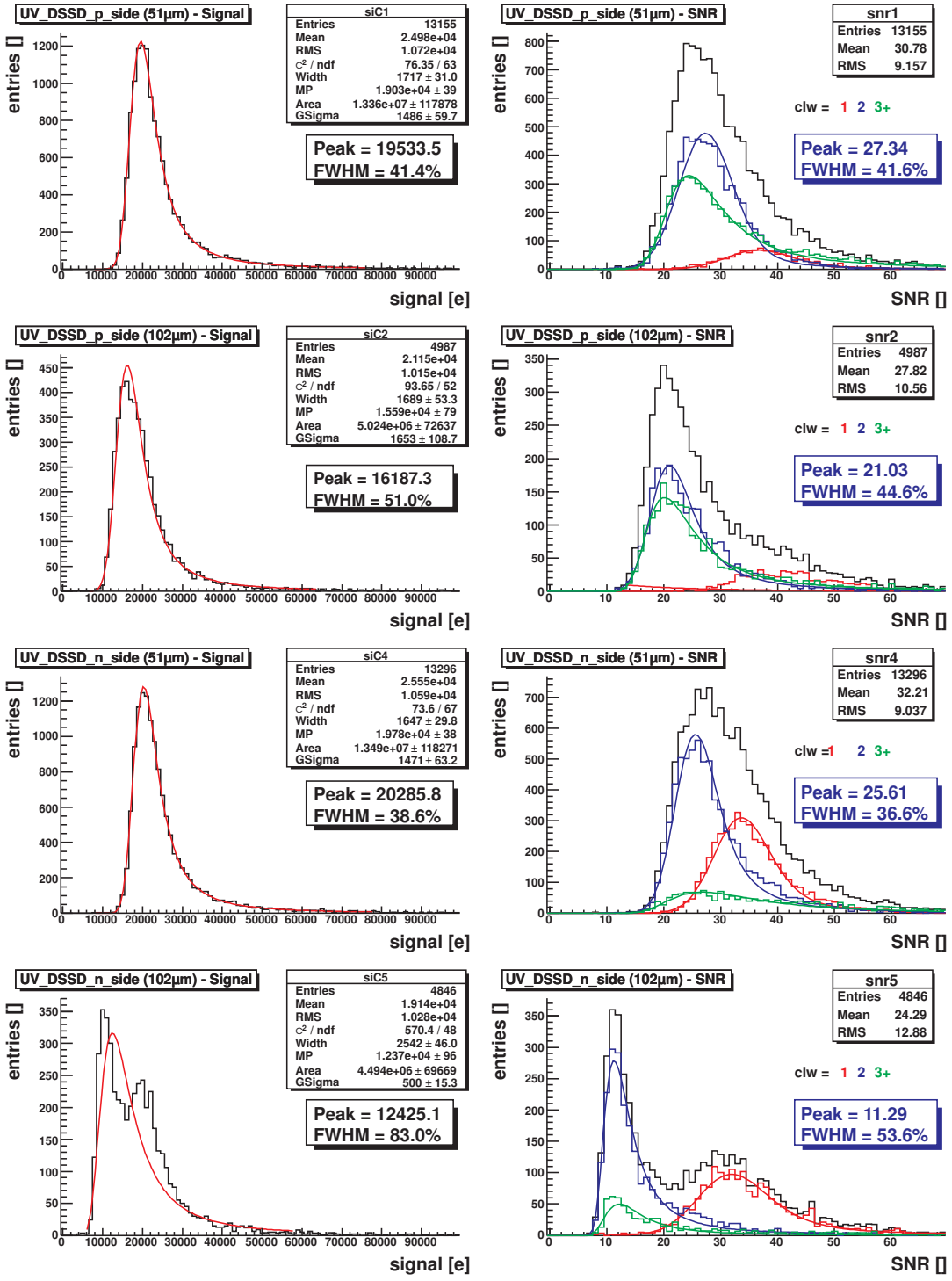

Figure 7.10.: Distribution of signal amplitude (left row) and SNR (right row) at nominal settings (T_p = 50 ns, f = 40 MHz and U_{bias} = 80 V) for each zone and p- and n-sides of the UV module, respectively. The SNR is drawn and fitted separately for each cluster width (1, 2 and $\geq$ 3). The peak SNR values shown in the inserts belong to the SNR curve which is closest to the average cluster width and hence are not equal to the calculated SNR which takes a non-integer average cluster width into account.

	p-side		n-side	
	51 μm	102 μm	51 μm	102 μm
Cluster Signal [e]	19533	16187	20285	10000 / 19000
Strip Noise [e]	515	519	591	649
Cluster Width	2.51	2.44	1.87	1.81
Custer SNR	24	20	25	11/29

Table 7.5.: Most probable cluster Signal, average strip noise, average cluster width and calculated cluster SNR (see eq. 7.3) of the UV module for each zone and side.

Numerical values of the most probable cluster signal (S_{MP}), the average strip noise (N_{avg}), the average cluster width (clw) and the calculated cluster signal to noise ratio (eq. 7.3) of each zone and side are listed in tab. 7.5, where the amplitude and the SNR of the 102 μm zone on the n-side are given for both peaks separately, corresponding to cluster widths of one and two, respectively.

$$\mathrm{SNR} = \frac{\mathrm{S_{MP}}}{\mathrm{N_{avg}}\sqrt{\mathrm{clw}}} \tag{7.3}$$

Thanks to the short length of both the sensor strips and the pitch adapter, the capacitive load is small, which leads to a good SNR of about 25 for the 51 μm zone.

The goal of the two zone design was to compare different pitches and evaluate the necessity of a the narrow 51 μm pitch in order to minimize the number of readout channels. However, the results show that the charge sharing is very inefficient at the 102 μm zone of the n-side due to the doubled p-stops between two readout channels. Consequently, intermittent readout is feasible for the p-side, but not on the n-side which would require a different sensor design with doubled pitch.

7.5.1. HV Scan

During the HV scan the bias voltage of the sensor was varied between 0 and 200 V, whereas 30,000 events with 6 samples per event were recorded at T_p =50 ns and f_{clk}=40 MHz for each voltage step. The goal of this measurement was to determine the true depletion voltage and compare the bias dependence of the measured signal amplitude to the theoretical curve given by

$$\begin{array}{rcll} \frac{S}{S_{depl}} & = & \sqrt{\frac{V_{bias}}{V_{depl}}} & \text{for} \quad V_{bias} < V_{depl} \\ \frac{S}{S_{depl}} & = & 1 & \text{for} \quad V_{bias} \geq V_{depl} \quad , \end{array} \tag{7.4}$$

where S is the signal amplitude, S_{depl} the amplitude at depletion voltage, V_{bias} the applied bias voltage and V_{depl} the depletion voltage. Theoretically, the amplitude does not depend on the applied bias voltage above V_{depl} and thus the amplitude remains constant equal to S_{depl}.

As shown in fig. 7.11, the measured values perfectly fit the theoretical square root function for both zones of the UV module. Furthermore, the signal saturates at high voltages as expected and the depletion voltage was determined to be about 60 V. This value also corresponds to voltage obtained from the CV curve shown in fig. 5.6 on page 48, which is the result of a clean room measurement.

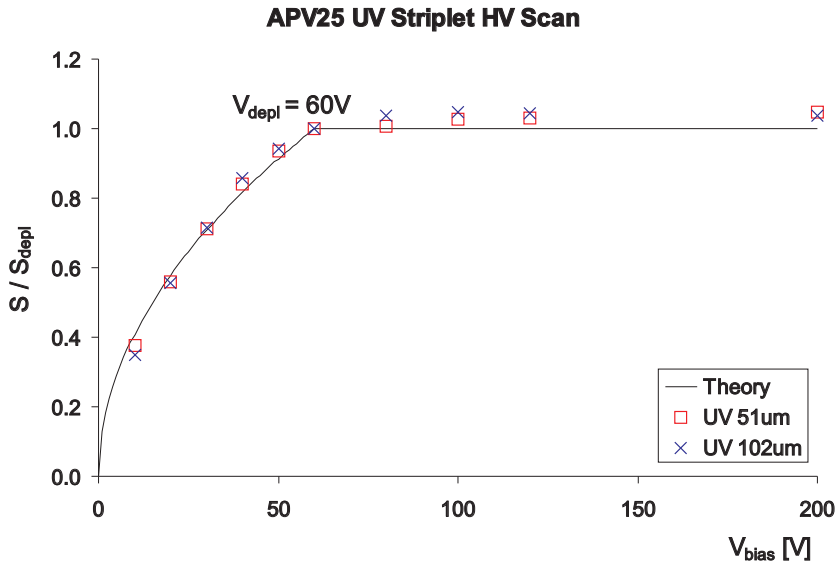

Figure 7.11.: Normalized cluster signal amplitude as a function of the bias voltage for both 51μm and 102μm zones of the UV module, respectively, compared to the theoretical function (eq. 7.4).

7.5.2. Angle Scan

The angle scan was intended to study signal amplitude, cluster width and SNR as a function of the angle between the sensor and the beam. Therefore the module was mounted on a remotely controlled turntable as shown in fig. 7.12. During the measurement the tilt angle between beam direction and sensor surface (α) was varied between 0° and 75° in sevem steps. 30,000 events with 6 samples per event and nominal settings (T_p =50 ns,

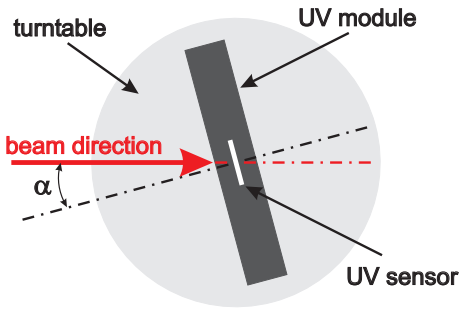

Figure 7.12.: Sketch of the angle scan setup.

f_{clk}=40 MHz and U_{bias} = 80 V) were recorded for each angle.

The signal amplitude is proportional to the charge collection distance, which is the distance covered by the particle inside the sensor. According to the geometry, the charge collection distance grows with $1/\cos\alpha$ and thus the relation between α and signal (S_α) is given by

$$S_\alpha = \frac{S_0}{\cos\alpha} \quad , \tag{7.5}$$

where S_0 is the amplitude at α=0. The measured amplitudes as a function of the tilt angle are drawn in fig. 7.13, revealing a perfect match between the measurement and

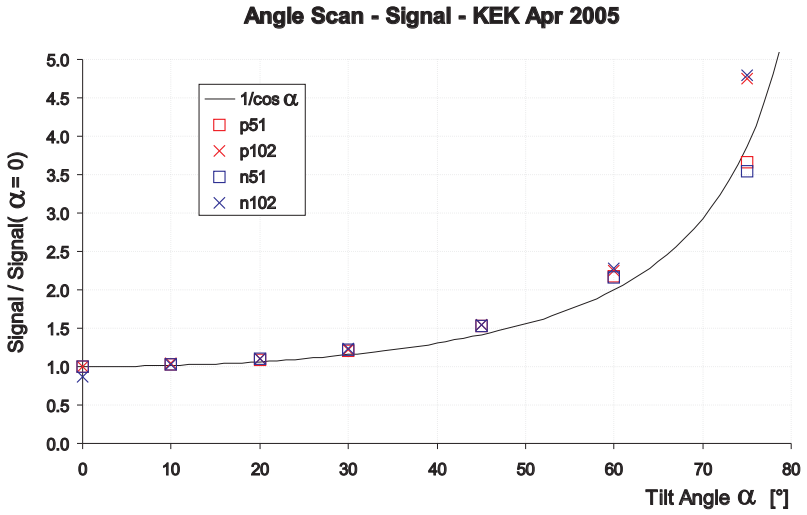

Figure 7.13.: Signal amplitude as a function of the tilt angle for both sides and zones of the UV module, respectively. The measured values are compared to the theoretical curve, which is given by $1/\cos\alpha$.

the theoretical $1/\cos\alpha$ function.

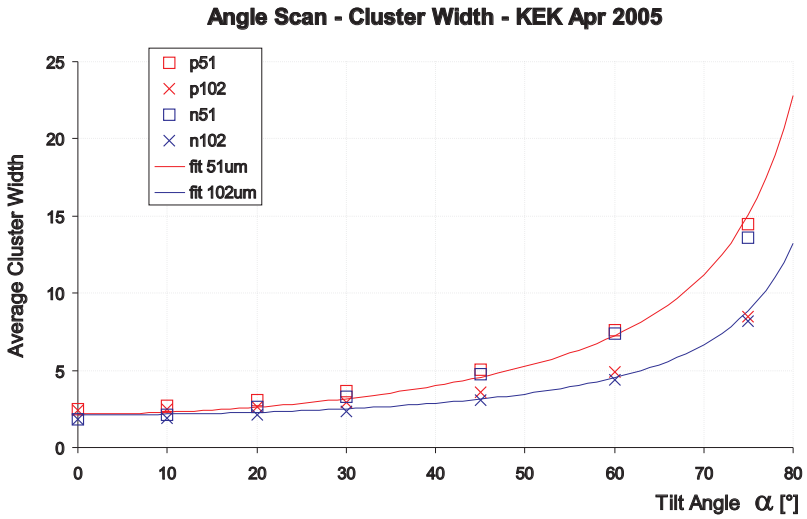

Figure 7.14.: Cluster width as a function of the tilt angle for both sides and zones of the UV module, respectively. The measured values are fitted by the empirical function $\sqrt{a^2 + (b\,\tan\alpha)^2}$.

The expected relation between cluster width and α is given by the empirical function

$$clw_\alpha = \sqrt{a^2 + (b\,\tan\alpha)^2} \quad , \tag{7.6}$$

where a is a constant offset that considers the non-zero cluster width at α=0 and $b\,\tan\alpha$ represents the geometrical term [48]. In fig. 7.14 the measured cluster width is plotted

as a function of α. For both the 51 μm and the 102 μm zone, respectively, a fit was performed using eq. 7.6, returning parameters a and b. Again, a good match of measurement and expectation is obvious.

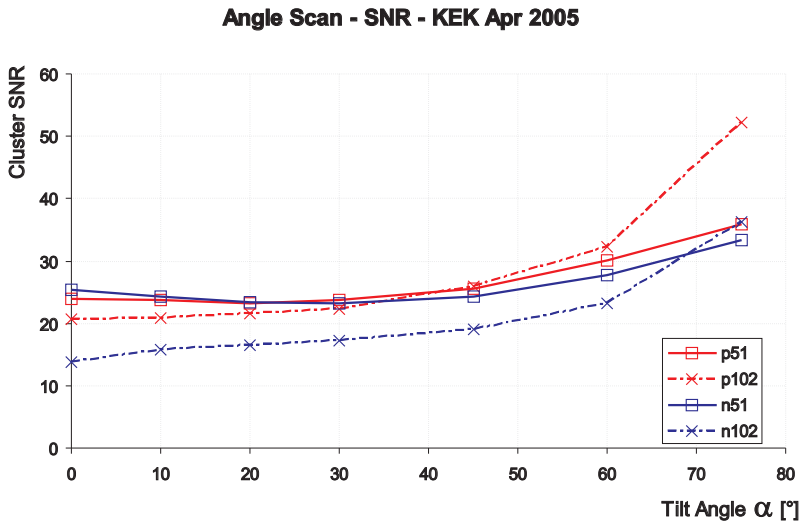

Figure 7.15.: SNR as a function of the tilt angle of both sides and zones of the UV module, respectively.

On one hand the signal to noise ratio increases with the signal, but on the other hand it depends on the cluster noise, which increases with the square root of the cluster width. Since both signal and cluster width depend on the tilt angle, the SNR also depends on α, but this relation is a more complex function and no analytic expression will be given here. The result of the measurements is shown in fig. 7.15. The SNR of the 102 μm zone is almost constant up to an angle of about 35° and increases at higher angles, while that of the 51 μm zone reveal a shallow minimum around $\alpha = 30°$, before rising with higher angles, too. An explanation of the increasing SNR at higher angles is that the signal amplitude grows faster than the square root of the cluster width. Fig. 7.14 shows that the cluster width of the 51 μm zone increases faster than that of the 102 μm zone simply due to geometrical reasons. Consequently, the SNR curves also differ between 51 μm and 102 μm zones.

7.5.3. UV Correlation

Another aspect of the quality of the UV striplet sensor is the correlation of the measurement results between p- and n-sides. A comparison of signal amplitude, cluster width and reconstructed peak time and their correlation residuals for the 51 μm zone are shown in fig. 7.16. A detailed description of the peak time reconstruction is given below in section 7.6. In the upper row of fig. 7.16 event data of p- and n-sides are compared in scatter plots and fitted by a linear function. The second row displays the correlation residuals of each considered value.

A good correlation is evident for the signal amplitude and the peaking time. For the signal amplitude the linear approximation was fixed at the origin and the slope was fitted to the measured values. This results in a slope of 1.02, which indicates a slightly different

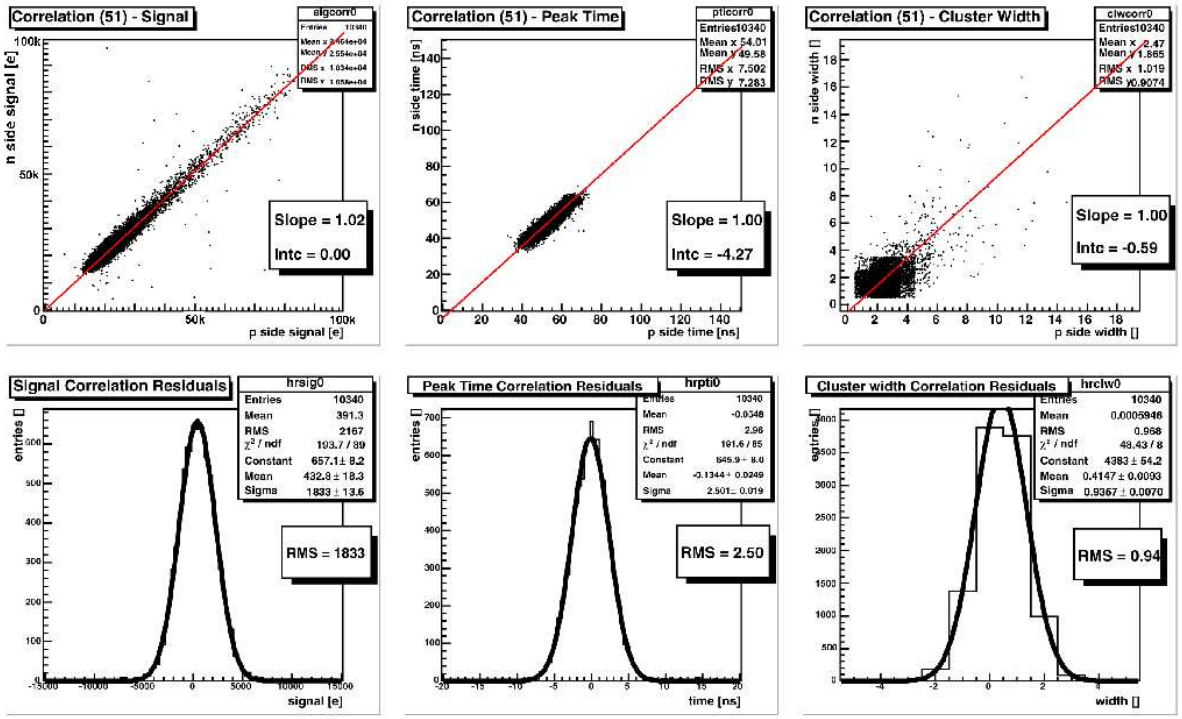

Figure 7.16.: Correlations of signal amplitude, peak time and cluster width of p- and n-sides.

charge collection efficiency for p- and n-sides, respectively. The residuals of signal yield an RMS of about 1833 e, which is less than 10% of the most probable amplitude (see tab. 7.5).

The slope was set to one and the offset was fitted in case of the peak time, which leads in an intercept of about 4.27 ns. A fraction of this offset is caused by poor timing of clock and trigger signals at the APVDAQ modules, where a delay 2.5 ns between p-side and n-side was measured. A possible reason for the remaining peak time offset is the unequal geometry of p- and n-side strips. This causes a different capacitive load of the APV25 chips of the two sides. Since equal I^2C settings were used for the APV25 chips of both sides and the actual peaking time of the shaper output depends on the capacitive load at the preamplifier input, this consequently results in differing shaping curves and moreover causes an offset between the peak time of the two sides. In principle, this effect can be avoided by using different I^2C settings for both p- and n-sides, respectively, which are adapted to the actual capacitive load of the APV chips.

Only the correlation of the cluster width shows poor results. The residuals of the cluster width are about 0.94 RMS, caused by the different strip configuration (intermediate strip on p-side and p-stop on n-side) and thus the inefficient charge charing at the n-side. This unbalance is magnified by the fact that the cluster width is confined to a few integer numbers at perpendicular incidence as shown in fig.7.16. The ratio of RMS / average gets smaller with angular incidence.

7.6. Hit Time Reconstruction

One main goal of the beam tests performed was to show the efficiency of the hit time reconstruction as described in section 4.2. Therefore, a software called "uvhitfitgui" was developed, which uses the resulting hit file of the "APVDAQ analysis". It is a Linux program written in C++ based on ROOT [47], which is an object-oriented data analysis framework developed by CERN and published under the terms of GNU LGPL[4]. This framework was chosen rather than the Labwindows/CVI because of its excellent support of histograms and curve fitting. It further includes a minimizer class call TMinuit, which was used to find the real hit time and signal amplitude using a given fit function.

A simplified flow chart of the "uvhitfitgui" is depicted in fig.7.17. The main component of the software is a class called "MultiPeakHitFitter". It supports two different fit functions, which will be described below in section 7.6.1.

An instance of the "MultiPeakHitFitter" sequentially reads the hit data from the file in a loop. For each hit, one peak time fit is performed, with each fit function. The resulting peak times of both fits as well as the other hit data, which were read from the source file (event number, hit position, cluster width, cluster noise, ...) are stored in a result file. The output file has the same name as the source file, but with an additional ".fit" suffix added. Then the difference to the measured TDC time and the SNR by using the amplitude obtained from the fit are calculated. Optionally, the measured samples and the fitted shaping curves of both functions are plotted together in a graph for a given number of hits (max. 54). Before the data of the next hit are read in, the fitted peak time values, their difference to the TDC time as well as the TDC time itself are filled into several histograms, separately for each side and zone of the sensor. Additionally, the residual time differences with respect to TDC values are stored as a function of SNR in a two-dimensional histogram.

Once all hits are processed, a Gauss fit is performed for each of the histograms containing the differences to the TDC values and the residuals are extracted. These residuals correspond to the RMS[5] of the achieved time resolution. Furthermore the distribution of the difference of the fitted peak time and the TDC time is also extracted for each SNR from the two-dimensional histogram. On the resulting histograms again a Gauss fit is performed and the residuals obtained from these fits are plotted as a function of the SNR. As this procedure is very time-consuming it must explicitly be turned on by a command line parameter. Finally, the histograms, the plotted shaping curves and the time resolution as a function of the SNR are displayed on the screen and saved as encapsulated postscript files (eps).

[4]GNU Lesser General Public License
[5]Root Mean Square value

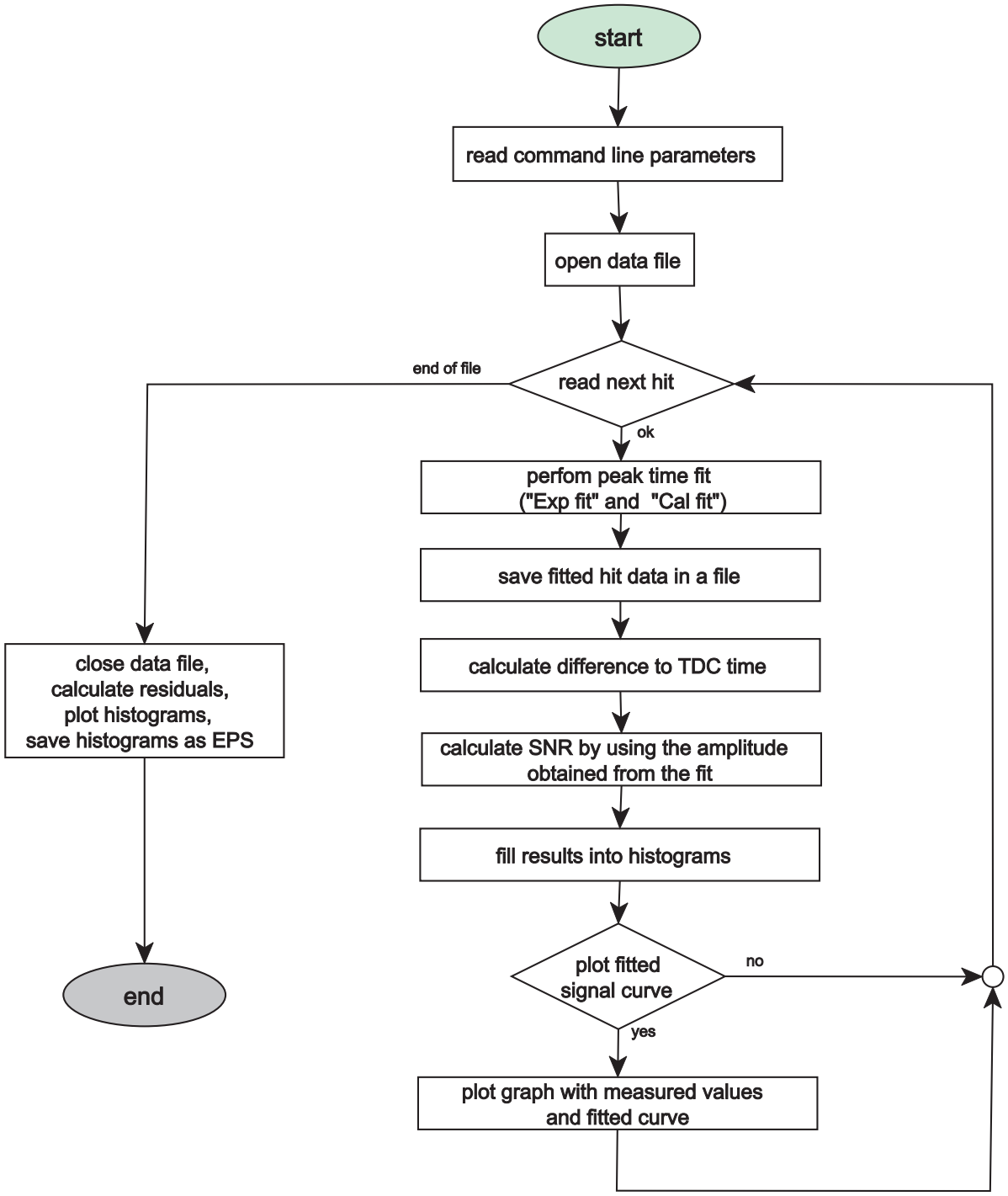

Figure 7.17.: Simplified flow chart of the peak time fitter.

7.6.1. Fitting Methods

The "MultiPeakHitFitter" is derived from the TMinuit class of the ROOT framework and uses its minimizer to perform a fit on the measured samples. TMinuit supports several fit parameters, which are varied within given limits by minimizing the result of a user defined function. Therefore, this function is executed repeatedly with various sets of parameters. In case of the "MultiPeakHitFitter" it calculates the sum of the square deviation between the measured values and the approximated shaping curve for all considered samples. Two different methods are implemented to approximate the shaper output. The first is called "Exp fit" and is based on the theoretical shaping curve of a CR-RC shaper, while the second one ("Cal fit") uses the waveform obtained by the internal calibration of the APV25, where the measured points are connected by cubic splines.

The goal of the fit is to obtain the actual peak time (t_{peak}) and amplitude from the measured samples. The time and the amplitude of the sample with the highest signal are used as initial parameters for each fit. Normally, the fit is performed using all samples of a hit, but it can optionally be restricted to only three samples around the peak.

7.6.1.1. Theoretical Shaper Output

This fit method uses an exponential function based on the output of an ideal CR-RC shaper. It is given by

$$\begin{aligned} f(t) &= A\,\frac{t-t_{peak}+T_p}{T_p}\,\mathrm{e}^{1-\frac{t-t_{peak}+T_p}{T_p}} \quad \text{for} \quad t \geq t_{peak}-T_p \\ f(t) &= 0 \qquad\qquad\qquad\qquad\qquad\qquad\quad \text{for} \quad t < t_{peak}-T_p \quad , \end{aligned} \tag{7.7}$$

where $\mathrm{T_p}$ is the peaking time, A the amplitude and t_{peak} the peak time. In contrast to the original form (see eq. 2.20 on page 22) the peak value of the exponential part is normalized to one by multiplication with e (adding 1 to the exponent). Furthermore, the function is moved along the time axis, so that the maximum is reached at the peak time t_{peak}. Since the shaper output starts at the time of the particle hit, which is $\mathrm{T_p}$ before the peak signal is reached, the function is set to 0 for $t < t_{peak} - T_p$.

The performance of this method was tested with data of both the KEK and PSI beam tests, respectively and compared to the time measured by the TDC. Since the beam was not synchronized to the APV clock a rectangular distribution of t_{peak} within the trigger window was expected. Fig. 7.18 shows the results of run019 (51 μm zone, p-side) of the KEK beam test. Surprisingly, the distribution obtained from the "Exp fit" has a slope and shows two gaps around 40 ns and 65 ns with almost zero entries, while that of the TDC measurement is entirely flat, which confirms the independence of beam and clock.

That means, there must be some conditions were the applied fit method does not work properly. Due to the asymmetric shaping curve most of the taken samples populate the tail and only one or two are on the rising edge. Furthermore only the samples above a given threshold are used to perform the fit. It might be possible that the first sample on the rise is below threshold and thus ignored and the second one, which is the first one used for the fit, is slightly below the actual peak. In such a situation the rising edge of the curve is hardly represented by samples and thus the fit is dominated by the samples of the tail. It was assumed that this kind of hits is responsible for the failure of the fit and causes the gaps.

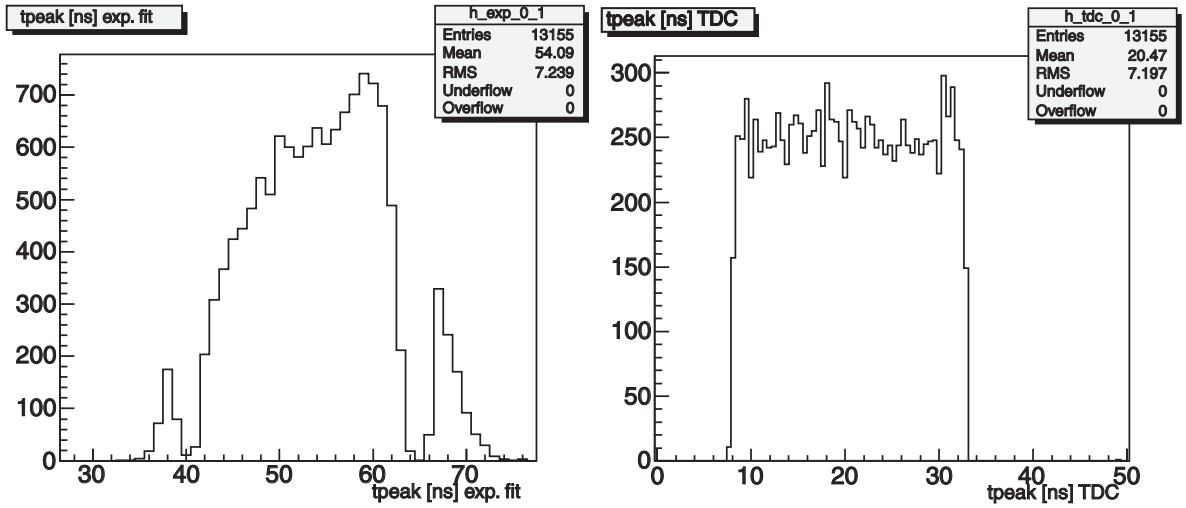

Figure 7.18.: Distribution of the peak time (t_{peak}) obtained from a fit using the theoretical shaping curve ("Exp fit") compared to the TDC time distribution.

In order to verify the above assumption the results of the "Exp. Fit" were split into three groups and filled into separate histograms. The first group contained all hits fulfilling $A_1/A_{max} < 0.4$, where A_1 and A_{max} are the amplitudes of the first and the peak sample, respectively. Members of the second group met the condition $0.4 \leq A_1/A_{max} < 0.7$ and the last set contained all the other hits satisfying $0.7 \leq A_1/A_{max}$ and thus also those assumed to be critical. That means, that the gaps should be visible in the histogram of the third group.

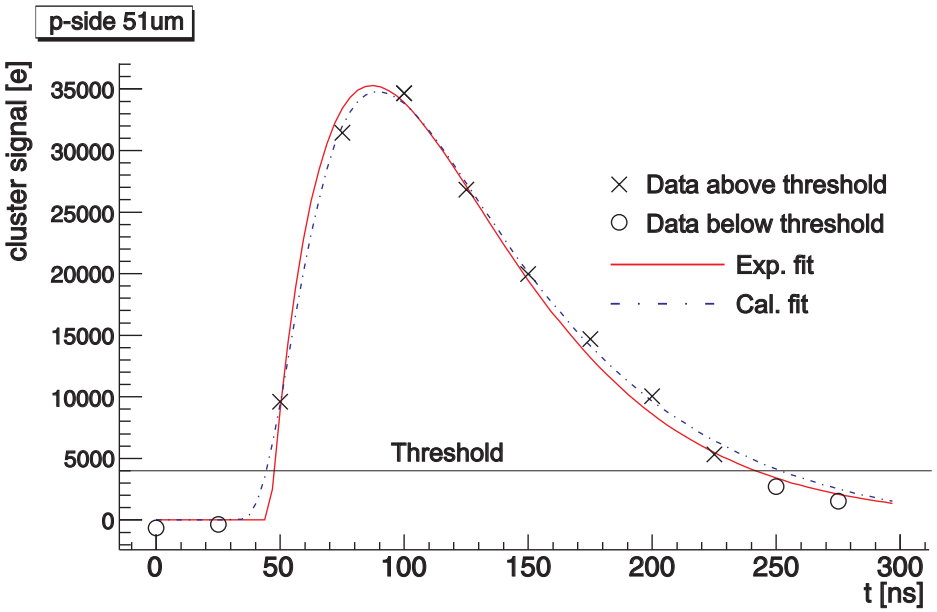

Figure 7.19.: Sampled shaper output values with two different fit functions applied. The deviation of the "Exp. fit" around the peak is obvious.

It was again surprising that the gaps were all found in the distribution of the first group ($A_1/A_{max} < 0.4$), hence those hits with the first sample at the beginning of the rise. So far it was assumed that such data provide the best condition for the fit, but

the result of the analysis is contrary. Further studies showed, that the fit obviously fails when the data contain two samples with almost the same amplitude around peak. Such a situation is shown in fig. 7.19, where the "Exp. fit" (red solid line) is compared to the result of the "Cal. fit" (blue, slash-dotted line, see below) and the measured samples. All samples above the threshold were considered by the fit (black ×), while those below (circle) were ignored.

Several facts were pointed out to cause the insufficient performance of the "Exp. fit". The function given by eq. 2.20 and eq. 7.7 describe the output of an ideal CR-RC shaper as it is shown in fig. 2.14 on page 21 and thus only approximates the shaper output of the APV25. An input signal with the form of a Dirac-δ pulse was assumed for the derivation of this formula, but the sensor current is a pulse with finite amplitude and a length of several nanoseconds (see fig. 2.7). Furthermore the shape of the signal is stretched by the capacitive load of the sensor. These are the reasons why the output of the APV shaper does not match the shape of an ideal CR-RC shaper and the "Exp. fit" fails in some cases. Hence, the theoretical function is not suitable to achieve precise hit time reconstruction.

7.6.1.2. Calibration Curve

A second method called "Cal. fit" was implemented, because of the problems with the "Exp. fit". This method uses the waveform obtained from the internal calibration of the APV25 and thus considers the shape of the actual pulse. In an internal calibration run (see 6.6.1) the shaper output is sampled with a time resolution of 1/8 clock period (3.125 ns at 40 MHz) and the average over several samples is built for each time point and APV25 channel. The shaping curve is determined by averaging the samples of all channels of one APV chip. The amplitude of the resulting curve is normalized and the curve is shifted along the time axis such that the peak is reached at t=0. Such a normalized shaping curve was determined for each peaking time used in the beam tests and stored in a multi-dimensional array used as reference for the "Cal fit".

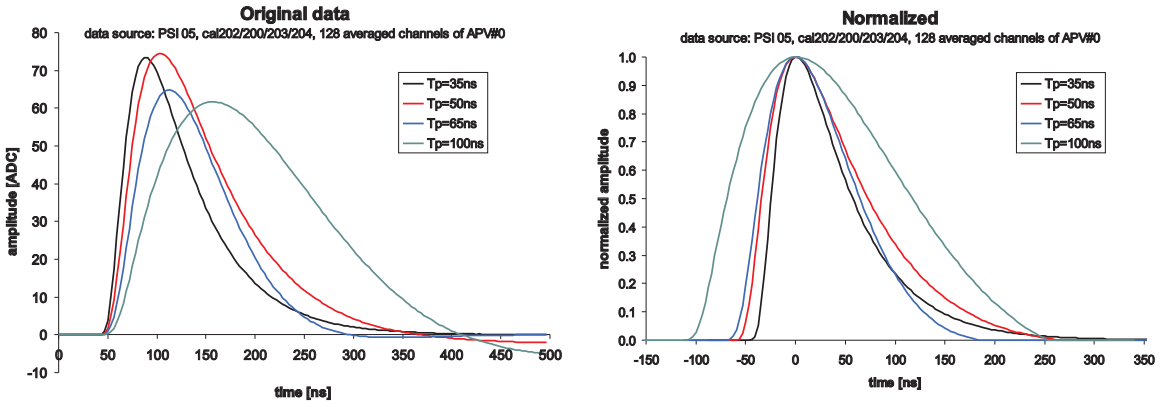

Figure 7.20.: Original and normalized calibration pulses for various shaping times (35 ns - 100 ns) obtained from data of the PSI beam test in August 2005.

As an example, the curves of both the original and the normalized data obtained from calibration runs of the PSI beam test are shown in fig. 7.20. Theses reference curves are used by the "MultiPeakHitFitter" to obtain actual time and amplitude of the hit by connecting the samples with cubic splines.

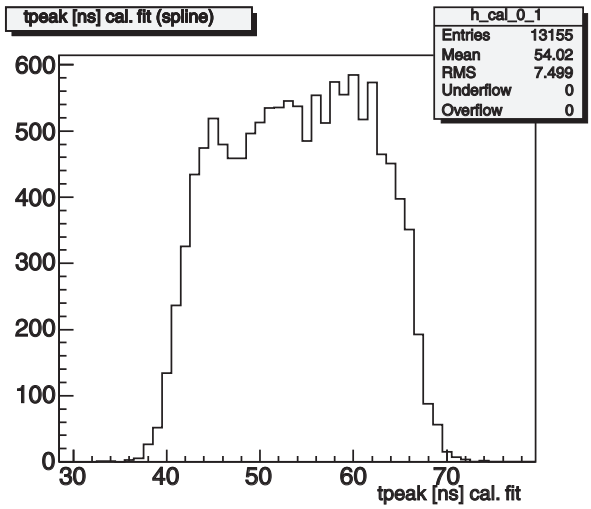

Figure 7.21.: Peak time distribution obtained from beam test data using "Cal. fit".

The resulting peak time distribution using this fit method is shown in fig. 7.21. As expected, the "Cal. fit" leads to an almost rectangular t_{peak} distribution and thus performs noticeably better than the "Exp. fit".

7.6.2. Time Resolution

Since the "Cal. fit" performs much better than the "Exp. fit", only the results of the former are presented here. Excellent results were achieved for both amplitude and peak time by using the hit time reconstruction method described above. The amplitude distribution perfectly fits a Landau shape, convoluted with a Gaussian component to account for electronic noise and intrinsic detector fluctuations. The comparison of the obtained peak time and the TDC values yields an excellent match as shown in fig. 7.22. In the right column the deviation of the determined peak time in relation to the TDC values is depicted. It nicely follows a Gaussian distribution with a RMS resolution of 2.6 and 2.0 ns for p-side and n-side of the UV module, respectively. This value also includes the uncertainty of the TDC and the jitter of the used scintillator, photomultipliers and discriminators, which is found to be about 1 ns from comparison of TDC referred residuals to p-n timing correlation. The scatter plots in the left column of fig. 7.22 show horizontal bars with a peak-to-peak width of about 18 ns and only few outliers. Thanks to such high precision the sensitive time window of the APV25 chip can be reduced from about 160 ns ($T_p = 50$ ns) to only 20 ns. This narrow sensitive time window corresponds to an occupancy reduction factor of about 100 achieved by both replacing the VA1TA chip with the APV25 and using the "hit time reconstruction" whereas the benefit of the shorter shaping time of the APV chip alone is about 12.5 (see section 4.1) and that of the "hit time reconstruction" method is about 8.

The achieved time resolution not only depends on the quality and performance of the applied fit but also on the signal to noise ratio of the system. The measured MP SNR values corresponding to the above results are 25 for the p-side and 28 for the n-side. Fig. 7.23 shows the RMS of the residuals as a function of the cluster SNR for the n-side of the UV module. An increase of the RMS of the residuals and thus a worsening of the time resoluiton is in evidence for a SNR below 20, while the resolution is almost constant at high signal to noise values. Thus it is important to maximize the SNR in

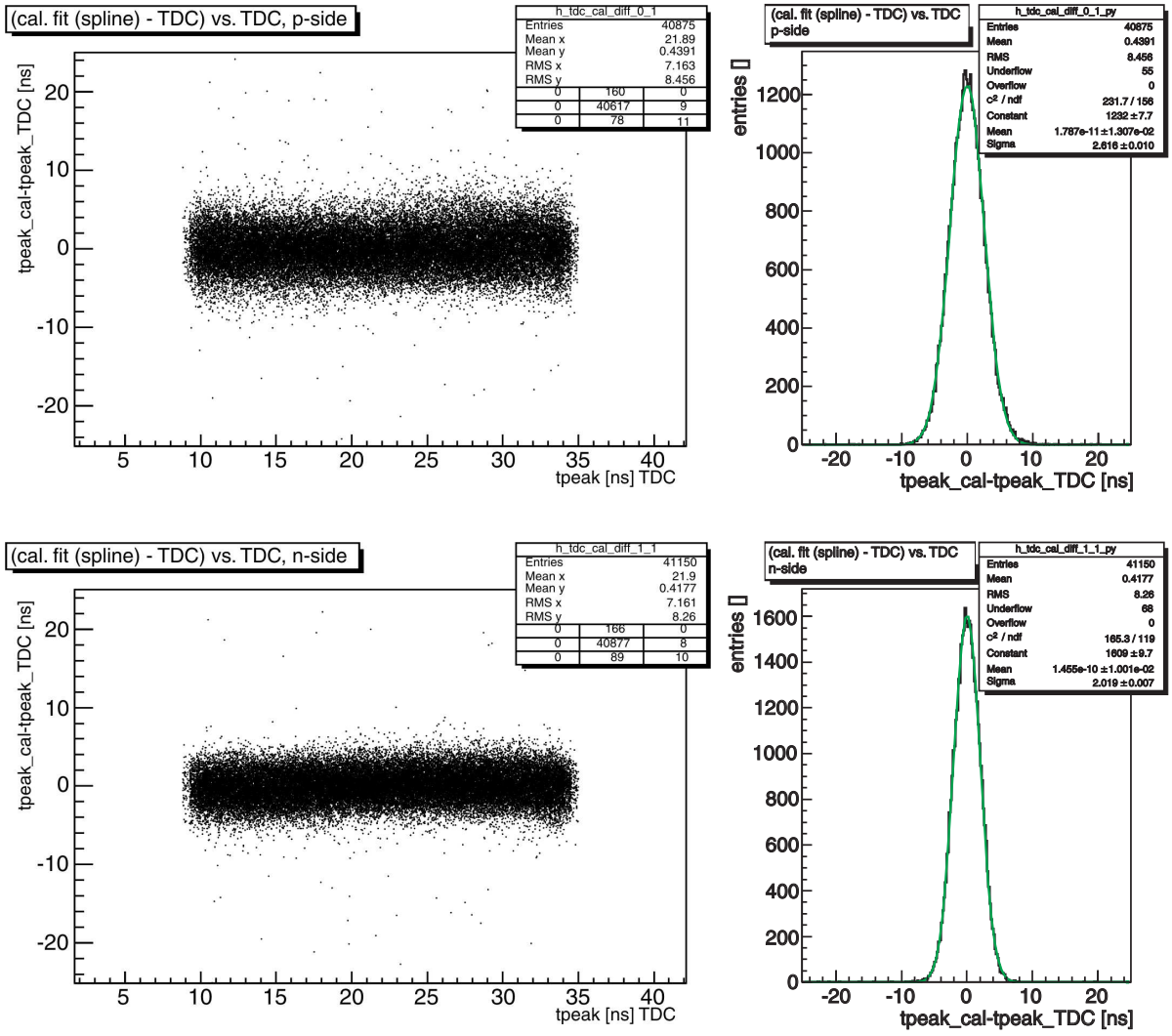

Figure 7.22.: Peak time precision obtained from the comparison to a TDC measurement of both p-side (top row) and n-side (bottom row), respectively. Left column: deviation of the fitted peak time vs. TDC value. Right column: Residual distribution of the fitted peak time.

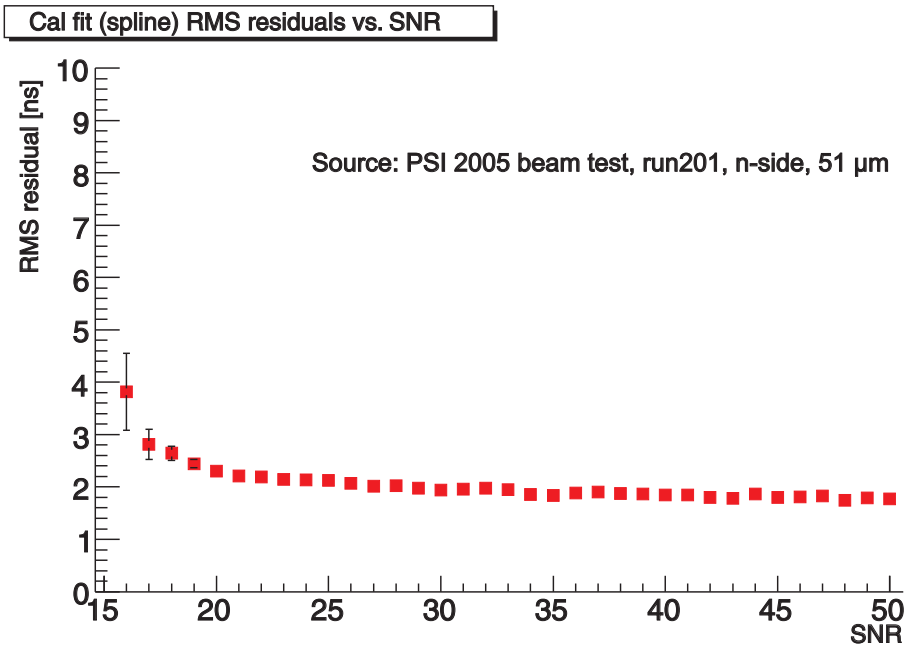

Figure 7.23.: Resolution (RMS of residuls) of the obtained t_{peak} as a function of the cluster SNR for the n-side of the UV module. Conditions: T_p = 50 ns, f = 40 MHz, 12 samples

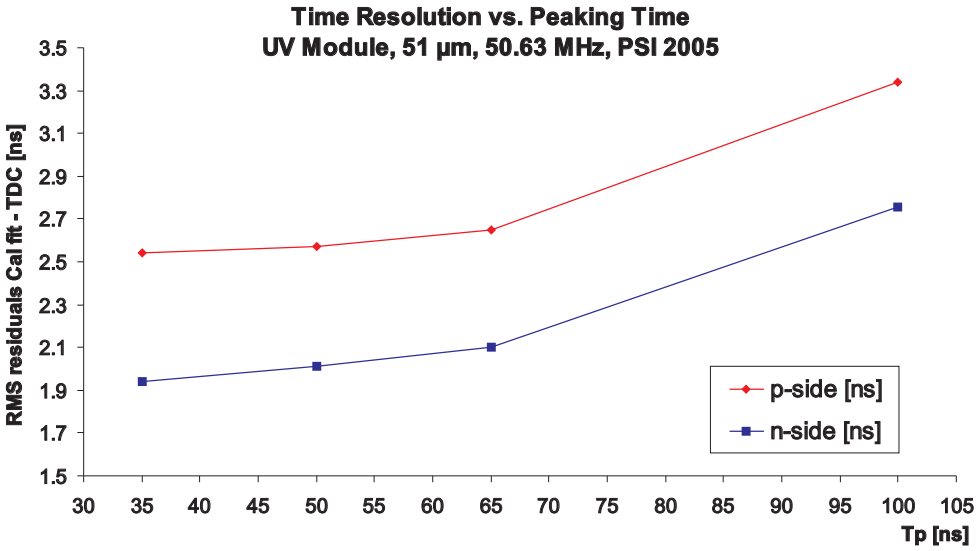

Figure 7.24.: Obtained time resolution as a function of the peaking time for both p-side and n-side of the 51 μm zone of the UV module measured at the PSI beam test.

order to achieve an accurate resolution of the reconstructed peak time.

Moreover, the time resolution depends on the used peaking time. In the PSI beam test several measurements with T_p between 35 and 100 ns were performed. The results of these measurements are shown in fig. 7.24. While the time resolution is almost constant up to T_p = 65 ns, it decreases significantly at 100 ns. Hence the nominal value of the APV25 chip (T_p = 50 ns) is recommended to be used for the future Belle SVD.

8. Summary and Outlook

The Silicon Vertex Detector (SVD) is the innermost subsystem of the Belle detector, which is used to determine the vertices of B meson pair decays in order to study CP violation and other properties of such decays. Currently the version 2 is in operation. Since its installation in summer 2003 the SVD2 has been working reliably without any serious problems and the collected data brought fruitful physics results.

However, improvements of the accelerator led to an increased luminosity, which reached a peak value of $1.712 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in November 2006. A letter of intent for a KEK Super B factory experiment was already published in 2004. The main goal of this upgrade plan is to reach an ultimate luminosity of $5 \times 10^{35}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, which will be more than a magnitude higher than now. One consequence of such a high luminosity is that the background at the interaction region is estimated to be up to 20 times higher than its current level. This higher background causes an equivalent increase of the occupancy, which further causes a worsening of vertex resolution and track finding efficiency of the SVD. Another effect of the high luminosity is that the first level trigger rate will increase from 450 Hz to up to 10 kHz (30 kHz max.). Since the currently used VA1TA readout chip lacks a pipeline, this will lead to an unacceptable dead time.

Three methods aimed to achieve a significant occupancy reduction were discussed in this thesis. One of these is to shorten the strips of the silicon sensor and thus reduce their sensitive area. By following this approach a DSSD called UV striplet with 45° slanted and thus shorter strips on both sides was designed by the Belle group. Thanks to the short strips of this sensor the occupancy can be reduced by a factor of about five. However, such a design implies an increase of the total number of readout channels and moreover makes the vertex reconstruction more complicated due to the rotated coordinate system.

Another approach is to replace the currently installed VA1TA chip by the APV25 chip, which was originally developed for the CMS tracker at CERN. Compared to the VA1TA (T_p=800 ns), the APV provides a significantly shorter nominal shaping time of 50 ns. This results in a shortening of the sensitive time-window of the front-end chip by a factor of 12.5, since the corresponding sensitive time windows are about 2000 ns and 160 ns for the VA1TA and the APV25 chips, respectively. Consequently also the occupancy will be reduced by the same amount. Furthermore, the APV is operated at 40 MHz and provides a 192 cell deep analog pipeline. That means it can be read out fast enough without any dead time even at high trigger rates.

An advanced data processing method using the APV25 chip was introduced as a third solution. With the help of the multi-peak mode of the APV chip several consecutive samples of the shaping curve can be read out. The real peak time of the curve is calculated by applying a fit on these samples. This allows the identification of off-time hits and leads to a further shortening of the sensitive time window and thus an additional reduction of the occupancy.

However, there are some differences between CMS and the Belle experiment, which were studied in this thesis. An important point is that the KEKB collider is operated

at lower energies and thus material budget inside the active volume, which is not a big issue at CMS, is very important at the Belle experiment to minimize multiple scattering. This requires that the readout chips are placed outside the active detector volume at the borders of the SVD, which causes long connections between sensors and APVs. Hence a test setup using a 50 cm long fanout between sensor and APV25 chips was built and evaluated in several laboratory measurements using a ^{90}Sr source. These measurements had shown, that the APV chip is stable even with such a long fanout. Due to the shorter shaping time, the APV25 has a noise figure, which is more sensitive to capacitive load of its preamplifier inputs than that of the VA1TA chip. Hence the achieved signal to noise ratio (SNR) with the long fanout was only about 9 and thus quite poor. This means that a design where long fanouts or ganged sensors are used in order to place the readout chips outside the active volume, as it was implemented for the outer layers of the SVD2, has to be avoided in the future vertex detector.

A better solution is given by a chip-on-sensor design, where the APV25 chips are mounted directly onto the sensor by using a hybrid made of a thin flexible foil (e.g. Kapton) to ensure both minimum material budget and a suitable SNR, respectively. Such a design is currently developed by the Institute of High Energy Physics of the Austrian Academy of Sciences (HEPHY) electronics group. Beyond the scope of this thesis, a first demonstrator module was already built and tested in a beam, yielding excellent results. However, several issues such as cooling of the APV25 chip need further investigation.

In contrast to the CMS tracker, which is entirely built up of single-sided silicon sensors, the Belle SVD consist of double-sided silicon strip detectors, which requires significant modifications to the readout electronics. Hence, a readout test system was designed to evaluate the suitability of the APV25 chip to read out DSSDs under the condition of the Belle experiment. Furthermore a sensor module using the UV striplet was built, where each side is read out by four APV25 chips. Several measurements, such as a HV scan and an angle scan, were performed at beam tests to evaluate the performance of both the APVDAQ test system and the UV module, respectively, leading to very satisfying results. Both, the APVDAQ system and the UV module worked good without any problems throughout the beam tests. A good signal to noise ratio of about 25, a proper signal distribution as well as good correlation between the two sides of the sensor, were achieved for the UV striplet sensor module. Furthermore, an excellent match between the measured values and expectations was observed. As a consequence of these positive results, many building blocks of the APVDAQ system, such as the AC coupling scheme, will also be implemented in the readout electronics of the future Belle SVD.

Moreover, a sample implementation of the hit time reconstruction method was implemented and applied to the data of the beam tests. Therefore the recorded samples were fitted by using both the theoretical exponential function of the shaping curve ("Exp. fit") and a reference waveform obtained from the calibration curve of the APV25 chip ("Cal. fit"), respectively. Unfortunately the "Exp. fit" failed in certain cases, because the theoretical function is only an approximation of the true output signal of the APV25 chip. A much better performance was observed for the "Cal. fit", where an RMS time precision of 2.6 and 2.0 ns was achieved for p-side and n-side of the UV module, respectively. Due to this good time resolution the sensitive time window of the APV25 can be reduced from about 160 ns (T_p=50 ns) to only 20 ns, which corresponds to an occupancy reduction by a factor of 8. This means that a total occupancy reduction factor of about 100 can be achieved by replacing the VA1TA chip with the APV25 and

using the "hit time reconstruction". This is much more than the benefit of the UV sensor, which is only about 5. Hence, the method of shorter sensitive time is preferable.

It was further observed that the time resolution not only depends on the quality and performance of the applied fit but also on the SNR of the system. Therefore it is very important to take care of a proper signal to noise ratio at the design of the future SVD readout system.

The method to reconstruct the peak time by applying a fit function on each event is a feasible method for beam test analysis, but not suitable in an experiment where a large number of channels has to be processed in parallel. By replacing the complex fitting algorithm with lookup tables derived from the calibration curve of the APV25 chip, the time finding procedure will be simplified, thus enabling a straightforward implementation in an FPGA. We currently work on an VME module, which not only digitizes the signals of several APV chips, but also performs pedestal subtraction, common mode correction and peak time finding using FPGAs. While the hardware of this board called "FADC+Processor" is already finalized and well tested, the development and tests of the firmware are still in progress.

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Special thanks goes to my colleagues of the Electronics 2 group Siegfried Schmid and Helmut Steininger, who made the layout and firmware of the electronic modules. I also want to thank Josef Pirker for assembling and soldering the electronics prototypes. He really is talented in handling almost invisible components.

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Appendix

A. APVDAQ Configuration File

```
# 40 mhz
# multi-peak mode (12 samples)
# 50ns peaking time
# 30ns trigger window (built from 5ns window, thus ~12.5ns later)
# APVDAQ 0 = TDC
# APVDAQ 1 = p-side UV
# APVDAQ 2 = n-side UV
#
# CI 05 august 2005
#

# optimized for 30m cables (August 2005 testbeam @ PSI)
#
#
# Lines preceded by a # or ; sign are ignored.
#
# [rem] comments a whole section until the next section start marked by [xxx] .
#

# [vme]
# VME addresses are given in the format
#  {module_name} = {vme_module_number},{vme_address_hex}
#  adq ... particular APVDAQ module
#  adb ... APVDAQ broadcast address
#
# Please note that the address ranges are not defined here,
# they are implicitly given by the hardware.
# Module numbers must fill from 0 (this is not checked).
# Please note that no range checking is performed.
# There is no access to VME modules that are not included in this list,

[vme]
adq = 0,0x1d000000
adq = 1,0x1e000000
adq = 3,0x20000000

adb = 0,0x80000000

# [adq]
# APVDAQ related information
#  mod = 0|1,{shift_register_delay},{adc_range},{br_mode},{frame_length},{tick_length},{max_trg},0    (default: 1,75,0,0,138,18,1)
#  res = {list of entries in reset sequence}                (default: 2,4)
#  cal = {list of entries in cal sequence} (default: 2,3)
#  str = {list of entries in software trigger sequence} (default: 75)
#  htr = {list of entries in hardware trigger sequence} (default: 74)
#
# mod specifies to use either the sequencer (1) or the shift register (0) for hardware trigger and the
#  delay of the shift register (0..255); adc_range (0=1Vpp, 1=2Vpp); br_mode specifies the baseline_restore mode
#  (0=off, 1=internal detection, 2=external detection via P2 RESERV input); frame_length and tick_length are related
#  to the internal detection circuit and only take effect if that is turned on; max_trg is the number of incoming
#  triggers which required to activate the veto logic (usually 1; 0 completely disables the veto logic)
# res, cal, str and htr are containing the bits to set in the 256-element sequencer memory (nothing is set at -1)
# Please note that cal+str together produce a calibration request plus subsequent normal trigger, so the time
#  between them is the latency.
#
# These settings are quite fragile! Do not modify until you know exactly what you are doing.

[adq]

# with baseline correction (30m cables)
#mod = 1,75,0,1,138,9,1,   0

# no baseline correction
mod = 1,75,0,0,138,9,1,   0

# TESTBEAM Aug 05, 30m cables, 40mhz, Tp=50ns, 12 multi-trigger for both hardware and software
mod = 1,75,0,0,138,19,1,   0
htr = 72,75,78,81,-1,-1,-1,-1
str = 72,75,78,81,-1,-1,-1,-1

#common settings
res =  2, 4,   -1,-1,-1,-1,-1,-1
cal =  2, 3,250,251, -1,-1,-1,-1

# [daq]
# DAQ related specifications are given in the format
#  ads = {N},{search_max_subevents},x
#  ini = {initevents},0,x
#  deh = {module_position},{apv_position},x
#  i2t = {N},0,x
#  pat = 0,0,{data_file_path}
#  clk = {N},0,x
#  pdl = {Trigger input delay},{ADC clock delay}
```

```
#
# ads N gives the number of samples that are read out from the ADC FIFO (<=4085), search_max_subevents is the
#  maximum number of subevents to search for within one ADC stream (default=1).
# ini is the number of software triggers in the beginning of a run for pedestal and noise
# evaluation. At the beginning of each run, 2*initevents are generated by software, after that the
# selected trigger source (hardware, software of calibration) is activated. The initial evaluation
# events are written to disk as normal events are.
# deh is the APV chip for which single strip histograms are recorded
# i2t is the maximum number of I2C retries in case of failure
# pat specifies the save path for data files (must include a trailing backslash!)
# clk gives the system clock period in integer ns (25 max.).
# pdl specifies the PHOS4 settings for trigger and ADC delays in ns (0..24)
# tdc gives APVDAQ number used as TDC and the ADC channel
# tdo gives the ADC range and its DC offset
# tdd tells how many channels to read out and how many (starting from zero) define the baseline

[daq]

# TESTBEAM Apr 05
#Multitrigger (12)
ads = 1900,12,x

ini = 300,0,x
deh = 1,0,x
i2t = 5,0,x
pat = 0,0,P:\aug05\

#standard 40mhz clock (25ns)
clk = 25,0,0
pdl = 2,23,0

# TDC
tdc = 0,0,x
tdo = 0,500,x
tdd = 10,3,x

# [hit]
# Hit recognition variables are specified here
#  hcs = {hitcut_seed_strip},{hitcut_neighbor_strips}
#  nok = {x.x},0
#
#
# hcs gives seed and neighbor hit cuts in units of strip sigma
# nok states the threshold over average noise at which strips are excluded from further analysis (to exclude noisy strips)

[hit]
# si sensor
hcs = 6.0,3.0

# do not exclude strips
nok = 2000.0,0

# [cal]
# Calibration related data
#  lvl = {level},0
#  lat = {latbeg},{latend}
#  sam = {average_samples},0
#  grp = {number_of_groups},0
#
# lvl is the CLVL amplitude (0..255), 1 is 625e-, 36 is 1 MIP (22500e-) nominally, in reality 26 is 1 MIP
# lat is the Latency range to cover (latend-latbeg>=2, latend-latbeg<=15)
# sam is the number of samples to average per position
# grp is how many groups to scan (<=8), first group is strips 0,8,16,..., second group is 1,9,17,..., ...

[cal]
#real 1 MIP level (22400e)
lvl = 26,0

#LAT=95/98 Calibration (long peak mode tail display)
lat = 55,74

#common settings
sam = 50,0
grp = 8,0

# [exc]
# External calibration related data
#  lat = {latbeg},{latend}
#  sam = {average_samples},0
#
# lat is the Latency range to cover (latend-latbeg>=2, latend-latbeg<=15)
# sam is the number of samples to average per position

[exc]

#standard external clibration (medium display)
lat = 74,94

#common settings
sam = 50,0

# [scn]
# Hardware signal scan data
#  del = {delbeg},{delend},{delstep}
#  eve = {N},0,0
#
# delbeg and delend gives start and end of the delay scan in ns (delend>delbeg, both 0..24), delstep is the stepsize
# eve gives the number of real harware events per scan point (excluding the 2*initevents; 0..65535)
```

```
[scn]
del = 0,20,5
eve = 10000,0,0

# [i2c]
# This section defines one or more I2C sets for the APV25. In the [mod] section, those sets are referenced to by their number.
#  ia2 = {number},{mode},{lat},{ipre},{ipcasc},{ipsf},{isha},{issf},{ipsp},{imuxin},{vfp},{vfs},{vpsp},{muxgain}
#
# The I2C settings must be individually numbered (ascending from 0). The easiest case is to use the same
# settings for all chips of one type, but one could go so far to use separate settings for each chip.
# vadj/vpsp is set individually for each apv in the [mod] section, the value specified here is meaningless.

[i2c]

# TESTBEAM Apr 05
# apv25s1, peak, inverter ON, Tp=50ns, HYBRID 1 (p side)
#ia2 =          0,    63,   95,    98,      52,    34,    34,    34,    55,      34,   30,   60,     0,       4

# TESTBEAM Apr 05
# apv25s1, peak, inverter OFF, Tp=50ns, HYBRID 2 (n side)
#ia2 =          1,    31,   95,    98,      52,    34,    34,    34,    55,      34,   30,   60,     0,       4

# TESTBEAM Aug 05
# apv25s1, multi-peak, inverter ON, Tp=50ns, HYBRID 1 (p side)
ia2 =          0,    61,   95,    98,      52,    34,    34,    34,    55,      34,   30,   60,     0,       4

# TESTBEAM Aug 05
# apv25s1, multi-peak, inverter OFF, Tp=50ns, HYBRID 2 (n side)
ia2 =          1,    29,   95,    98,      52,    34,    34,    34,    55,      34,   30,   60,     0,       4

# [mod]
# Detector module (actually hybrid) specifications are given in the format
#  mod = {module_position},{apvdaq_number},0,0,0,m,0,0,0,{Name}
#  apv = {module_position},{apv_position},{i2c_address},{i2c_settings},{vadj/vpsp},x,{apcdaq_number},{adc_channel},{adc_offset},x
#
# mod gives the hybrid/module properties: The position counts from 0 to 7 in beam direction,
#  Name must not contain blanks ("_" is allowed).
# apv describes the chips located on a hybrid
#  and the ADC channel where they are read out, either a Vienna ADC (a) or a FED (f).
# The ADC offset is only available with the Vienna ADCs and shifts the baseline.
# The individual chip vadj setting dominates over the [i2c] setting.


[mod]
### BELLE/APV25 DSSD UV-Sensor (p side = hybrid #1)
mod = 1,1,   0,0,0,m,0,0,0,UV_DSSD_p_side

apv = 1,0,34,0,25,x,1,0,250,x
apv = 1,1,36,0,25,x,1,1,250,x
apv = 1,2,38,0,25,x,1,2,250,x
apv = 1,3,40,0,25,x,1,3,250,x

### BELLE/APV25 DSSD UV-Sensor (n side = hybrid #2)
mod = 2,2,   0,0,0,m,0,0,0,UV_DSSD_n_side

apv = 2,0,34,1,25,x,2,0,250,x
apv = 2,1,36,1,25,x,2,1,250,x
apv = 2,2,38,1,25,x,2,2,250,x
apv = 2,3,40,1,25,x,2,3,250,x

# [bad]
# Bad channels description table
#  bad = {module_position},{apv_position},{List of 18 strip values or -1}
#
# Maps bad channels, which are then excluded from hit search. Up to 18 bad strips can be entered per line,
# more lines per APV are allowed. Unused values in the list must be filled with -1

[bad]
# noisy channels uv-sensor p-side
bad = 1,0,0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17
bad = 1,0,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,-1

bad = 1,2,17,18,19,45,127,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1

bad = 1,3,51,52,53,54,55,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
bad = 1,3,82,83,84,85,86,87,88,89,90,91,92,93,94,-1,-1,-1,-1,-1
bad = 1,3,95,96,97,98,99,100,101,102,103,104,105,106,107,108,109,110,111,112
bad = 1,3,113,114,115,116,117,118,119,120,121,122,123,124,125,126,127,-1,-1,-1

# noisy channels uv-sensor n-side
bad = 2,0,0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16,17,18
bad = 2,0,18,19,20,21,22,23,24,25,26,27,28,29,30,31,-1,-1,-1,-1,-1
bad = 2,0,70,71,72,73,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1

bad = 2,1,1,18,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1
bad = 2,2,127,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1,-1

bad = 2,3,82,83,84,85,86,87,88,89,90,91,92,93,94,-1,-1,-1,-1,-1
bad = 2,3,95,96,97,98,99,100,101,102,103,104,105,106,107,108,109,110,111,112
bad = 2,3,113,114,115,116,117,118,119,120,121,122,123,124,125,126,127,-1,-1,-1

[sen]
# sensor configuration
#  sen = {sensor number},{number strips on p side},{numeration direction p},{number strips on n side},
        {numeration direction n},{first_full},{last_full},{pitch [m]},{angle []},{height [m]}
#  apv = {sensor number},{module_position},{apv_position},{first_strip},{num_floating},{side},0,0,0,0
#  zon = {sensor number},{zone number},{first strip on p side},{last strip on p side},{first strip on n side},{last strip on n side},0,0,0,0
```

```
#
# sen defines the sensor proberties:
#  numeration direction can be 0 = from left to right or 1 = from right to left
#
# apv describes the apvs connected to the sensor
#  module_position and apv_position must be identical to the values in section [mod]
#  first_strip is the strip number bonded to channel 0
#  num_floating is the number of floating strips between two apv channels, set it to 0 if all strips are bonded.
#  side: 0 = the apv is bonded to the n side of the sensor
#        1 = the apv is bonded to the p side of the sensor
#
# zon defines zones of strips with similar properties, e.g.bonding density
#  for each zone the data should be processed separately
#

## UV sensor definition
sen = 0,1024,0,1024,1,80,944,51.0,45.0,8500.0

# apv sensor mapping
apv = 0,1,0,299,0,1,0,0,0,0
apv = 0,1,1,427,0,1,0,0,0,0
apv = 0,1,2,555,0,1,0,0,0,0
apv = 0,1,3,684,1,1,0,0,0,0
# n side
apv = 0,2,0,719,0,0,0,0,0,0
apv = 0,2,1,591,0,0,0,0,0,0
apv = 0,2,2,463,0,0,0,0,0,0
apv = 0,2,3,334,1,0,0,0,0,0

# bondig zones
zon = 0,1,299,682,336,719,0,51.0,0,0
zon = 0,2,684,938,80,334,0,102.0,0,0
```

Bibliography

[1] Sundaresan, M. K. *Handbook of Particle Physics*. CRC Press LLC, 2001.

[2] Iijima, T. *Commissioning of the KEK B-factory*. Nuclear Instruments and Methods in Physics Research A, 446: 65–69, May 2000.

[3] Kikutani, E. and Kurokawa, S. *Overview of the KEKB accelerators*. Nuclear Instruments and Methods in Physics Research A, 499: 1–7, 2003.

[4] KEKB. *B-Factory Design Report*. KEK Report, 1995.

[5] Kleinknecht, K. *Uncovering CP Violation : Experimental Clarification in the Neutral K Meson and B Meson Systems*. Springer-Verlag Berlin Heidelberg, 2003.

[6] Christenson, J. H. et al. *Evidence for the* 2π *Decay of the* K_2^0 *Meson*. Physical Review Letters, 13(4): 138–140, Jul 1964.

[7] Koboyashi, M. and Maskawa, T. *CP-Violation in the Renormalizable Theory of Weak Interaction*. Progress of Theoretical Physics, 49(2): 652–657, February 1973.

[8] Cabibbo, N. *Unitary Symmetry and Leptonic Decays*. Physical Review Letters, 10: 531–533, 1963.

[9] Wolfenstein, L. *Parametrization of the Kobayashi-Maskawa Matrix*. Physical Review Letters, 51: 1945–1947, Nov 1983.

[10] Yao, W.-M. et al. *Review of Particle Physics*. Journal of Physics G, 33, 2006.

[11] Marlow, D. R. *B-factory detectors*. Nuclear Instruments and Methods in Physics Research A, 478: 80–87, February 2002.

[12] Gronau, M. *CP Violation in Neutral-B Decays of CP Eigenstates*. Physical Review Letters, 63: 1451–1454, Oct. 1989.

[13] Belle Collaboration. *Belle Webpage*. http://belle.kek.jp.

[14] Abashian, A. et al. *The Belle detector*. Nuclear Instruments and Methods in Physics Research A, 479: 117–232, Februrary 2002.

[15] Tani, N. *Study of the new DSSD for Belle SVD*. Master's thesis, Department of Physics, Tohoku University, January 2007.

[16] Iijima, T. et al. *Aerogel Cherenkov counter for the Belle detector*. Nuclear Instruments and Methods in Physics Research A, 453: 321–325, June 2000.

[17] Miyabayashi, K. *Belle electromegnetic calorimeter*. Nuclear Instruments and Methods in Physics Research A, 494: 298–302, November 2002.

[18] Friedl, M. *The CMS Silicon Strip Tracker and its Electronic Readout*. PhD thesis, Vienna University of Technology, May 2001.

[19] Bergauer, T. *Process Quality Control of Silicon Strip Detectors for the CMS Tracker*. Master's thesis, Vienna University of Technology, August 2004.

[20] Tyagi, M. S. *Introduction to Semiconductor Materials and Devices*. Wiley & Sons, 1991.

[21] Ramo, S. *Currents Induced by Electron Motion*. Proceedings of the IRE, 27: 584–585, 1939.

[22] Friedl, M., Bauer, T. and Krammer, M. *A simple model of charge collection in silicon detectors*. Nuclear Instruments and Methods in Physics Research A, 461: 192–196, April 2001.

[23] Pernegger, H. *The Silicon Ministrip Detector of the DELPHI Very Forward Tracker*. PhD thesis, Vienna University of Technology, February 1996.

[24] Iwata, Y. et al. *Optimal P-Stop Pattern for the N-Side Strip Isolation of Silicon Microstrip Detectors*. IEEE Transactions on Nuclear Science, 45(3): 1187 – 1191, 1998.

[25] CMS Collaboration. *CMS Tracker Project, Technical Design Report,* CERN/LHCC 98-6, CMS TDR 5, April 1998.

[26] Broennimann, C. et al. *Development of an Indium bump bond process for silicon pixel detectors at PSI*. Nuclear Instruments and Methods in Physics Research A, 565: 303–308, September 2006.

[27] König, S. et al. *Assembly of the CMS pixel barrel modules*. Nuclear Instruments and Methods in Physics Research A, 565: 62–66, September 2006.

[28] Deptuch, G. et al. *Design and testing of monolithic active pixel sensors for charged particle tracking*. IEEE Transactions on Nuclear Science, 49: 601 – 610, April 2002.

[29] Turchetta, R. et al. *Monolithic active pixel sensors (MAPS) in a VLSI CMOS technology*. Nuclear Instruments and Methods in Physics Research A, 501: 251–259, May 2003.

[30] Nygard, E. et al. *CMOS low noise amplifier for microstrip readout: Design and results*. Nuclear Instruments and Methods in Physics Research A, 301: 506–516, March 1991.

[31] Baricchello, G. et al. *Performance of Long Modules of Silicon Microstrip Detectors*. CERN-PPE/97-162, December 1997.

[32] Ishino, H. *The Belle Silicon Vertex Detector*. Nuclear Instruments and Methods in Physics Research A, 549: 16–19, September 2005.

[33] Kibayashi, A. *Status of the Belle Silicon Vertex Detector*. Nuclear Instruments and Methods in Physics Research A, 569: 5–7, September 2006.

[34] ideas. *VA1TA Manual*, May 2001.

[35] Friedl, M. et al. *Readout, first- and second-level triggers of the new Belle silicon vertex detector*. Nuclear Instruments and Methods in Physics Research A, 535: 491–496, July 2004.

[36] HEPHY. *FADCTF system, Belle SVD 2.0 readout, User's Manual*. Austrian Academy of Sciences, Institute of High Energy Physics, Nikolsdorfergasse 18, A-1050 Vienna, Austria, July 2002.

[37] Ohnishi, Y. *Track Parametrization*. Belle Note, 148 (1996), 1996.

[38] Kawasaki, T. et al. *Vertex detector for super Belle experiment*. Nuclear Instruments and Methods in Physics Research A, 560: 53–56, December 2006.

[39] Friedl, M. et al. *Belle silicon vertex detector for the Super B Factory*. Nuclear Instruments and Methods in Physics Research A, 569: 37–40, October 2006.

[40] Haba, J., editor. *Letter of Intent for KEK Super B Factory, Part II: Detector*. KEK Report 04-4, 2004.

[41] French, M. J. et al. *Design and results from the APV25, a deep sub-micron CMOS front-end chip for the CMS tracker*. Nuclear Instruments and Methods in Physics Research A, 466: 359–365, 2001.

[42] Gadomski, S. et al. *The deconvolution method of fast pulse shaping at hadron colliders*. Nuclear Instruments and Methods in Physics Research A, 320: 217–227, 1992.

[43] HEPHY. *APVDAQ, APV25 Readout System, Reference Manual*. Austrian Academy of Sciences, Institute of High Energy Physics, Nikolsdorfergasse 18, A-1050 Vienna, Austria, August 2007.

[44] Jones, L. *APV25-S1 User Guide Version 2.2*. RAL Microelectronics Design Group, September 2001.

[45] CERN. *PHOS4, 4-channel delay generation ASIC with 1 ns resolution*. data sheet, Rev. 1.2.

[46] National Instruments Corporation. *LabWindows/CVI*. http://www.ni.com/lwcvi.

[47] CERN. *ROOT, An Object-Oriented Data Analysis Framework*. http://root.cern.ch.

[48] Adam, W. et al. *Response of a silicon strip detector to protons and pions with momenta of 270, 310 and 405 MeV/c*. Nuclear Instruments and Methods in Physics Research A, 441: 427–437, 2000.