

DISSERTATION

Wakeup Receiver for Wireless Sensor Networks

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Kurzfassung

Die sinkenden Kosten der Produktion von Low-Power Silikon Technologien und intelligente Strategien zur Verringerung des Leistungsverbrauchs haben zu einer hohen Wünschbarkeit der schnurlosen Kommunikation für Sensornetzwerke geführt. Zwischen den verschiedenen Anwendungsgebieten für solche Netzwerke, unter anderem Gebäudeautomation, Fahrzeugautomation sowie Container Tracking, gibt es einen gemeinsamen Bedarf an Knoten, die komplett eigenständig sind und mehrere Jahre mit einem Akkumulator funktionieren. Ein langes Leben ist normalerweise mit der zeitlichen Einteilung der aktiven und inaktiven Periode der Knoten und mit der Synchronisation der Kommunikation erreichbar. Die vorliegende Arbeit schlägt einen besonderen Funkempfänger vor, genannt "Wakeup Receiver", der eine Kommunikation ohne zeitliche Einteilung ermöglicht, und der keines komplizierten Synchronisationsverfahrens bedarf. Diese Entwicklung ermöglicht das Aktivieren der Knoten auf Verlangen und ergibt eine viel energieeffizientere Strategie und Kommunikation. Die Auswirkung auf die ganze Energie des Netzwerks wird durch eine integrierte Schaltung analysiert. Zum Schluss wird eine Implementierung des Empfängers vorgestellt, die im Rahmen des erwarteten Leistungsverbrauchs funktioniert. Mit der vorgeschlagenen Lösung werden Sensornetzwerke in Leistungsverbrauch und Kommunikation an Effizienz gewinnen, damit werden die Implementierungen und Anwendungen in ihren Anwendungsgebieten viele Vorteile bringen.

Abstract

Sinking costs in the production of low power silicon technologies and intelligent energy saving strategies have lead to wireless communication for sensor networks becoming highly desirable. In the different fields of application for such networks, which include building automation, car automation or container tracking, there is a common need to have nodes which are completely self-sufficient and last several years on battery operation. A long life is usually realized by scheduling periodical power-ups and power-downs of the node and synchronizing the communications. This work proposes a particular radio receiver called Wakeup Receiver, which allows incoming communication without schedule, removing the constraint of complicated synchronization protocols. This design allows for powering up the nodes on-demand, resulting in much more efficient energy saving strategies and communications. The impact on the overall network energy is also analyzed using a proof of concept custom integrated circuit. Finally, the implementation of the receiver is presented, which performs within the range of expected power consumption. With the proposed solution, sensor networks will achieve efficiency in energy consumption and communication, such that their implementation and utilization will bring great advantages to their application fields.

Vorwort

Das erste Kapitel gibt einen generellen Überblick über Funksensornetzwerke und leitet diese Arbeit ein. Ebenso sind die Aufgabenstellung und die Ziele dieser Dissertation hier zu finden.

Das zweite Kapitel präsentiert den Stand der Technik von Sensorknoten und den verschiedenen entsprechenden Vorschlägen. Die technologischen Aspekte der Integration von Sensorknoten werden analysiert und die Systemarchitektur dargestellt. Diese Analyse deckt alle Basisaspekte und Bausteine von Sensorknoten, inklusive Mikrocontrollern, Sensoren, Glue Logic, Energiemanagement und Scavenging. Der zweite Teil des Kapitels präsentiert einige publizierte Wakeup Empfänger und analysiert diese um eine Basis für die Dissertation zu bilden. Es stehen für diese Thematik nur wenige Publikationen zu Verfügung; nichtsdestotrotz sind alle relevanten Publikationen vorhanden und analysiert um einen Überblick über die (noch) kleine Welt der Wakeup Empfänger zu schaffen.

Kapitel drei erklärt die vorgestellte Architektur, die den Sensorknoten erlaubt ihren Stromverbrauch unter die Schwelle, die viele Lebensjahre ermöglicht, zu senken. Dieses Konzept deckt die beiden ersten Schichten des Protokolls, wobei die zweite Schicht normalerweise von der CPU abgehandelt wird. Es wird eine Architektur für beide Schichten zusammen mit einem allgemeinen Systemkonzept vorgeschlagen, das einen extrem geringen Stromverbrauch erlaubt.

Kapitel vier zeigt die Implementierung dieser Arbeit, die im vorherigen Kapitel vorgestellt wird. Die erste Hälfte des Kapitels deckt alle realisierten funktionellen Tests und diskreten Implementierungen. In diesem Teil der Arbeit wurde die Realisierbarkeit des Konzeptes getestet und einige Schaltkreise wurden realisiert und gemessen, obwohl sie noch nicht für niedrigen Stromverbrauch optimiert wurden. Die zweite Hälfte des Kapitels behandelt die integrierte Implementierung des Wakeup Empfängers, dank den Ergebnissen der vorherigen diskreten Implementierungen.

Kapitel fünf zeigt die Ergebnisse, die durch die Implementierung erreicht wurden, und vergleicht diese mit den erwarteten Resultaten von Kapitel drei. Die Effizienz aller Bausteine des Wakeup Empfängers wurden gemessen und mit den erwarteten Werten verglichen. Eine allgemeine Evaluierung des Empfängers als Teil des Sensorknotens wird durchgeführt.

Kapitel sechs schliesst die Arbeit mit einem Überblick und einem Ausblick für zukünftigen Arbeiten basierend auf dem Konzept des Wakeup Empfängers ab.

Preface

Chapter 1 gives a general background to Wireless Sensor Networks and introduces them to this work. The problem statement and the objectives of this thesis are also found in this chapter.

Chapter 2 presents the state of the art of sensor nodes and the various proposals that are pertinent to this work. The technological aspects in sensor integration are analyzed and the system architecture is presented. This analysis covers all the fundamental aspects and building blocks of sensor nodes works, including microcontrollers, sensors, glue logic, energy management and scavenging. The second part of the chapter presents some proposed wakeup receivers and analyzes them to build a basis to the work of this dissertation. There are not many sources on this thematic; nonetheless all relevant publications are represented and analyzed to give a picture on the (still) small world of the wakeup receivers.

Chapter 3 explains the proposed architecture that enables sensor nodes to reduce their power consumption under the threshold that makes years of life possible. This concept covers both the physical layer of the communication stack, the radio transceiver as the second layer which is normally a task of the CPU. An architecture for both layers is proposed together with an overall system concept that enables ultra low power consumption.

Chapter 4 shows the implementation of the work as explained in the previous chapter. The first half of the chapters covers all the functional test and discrete implementation realized. In this part of the work, the capability of the concept was tested and some proof circuits were realized and measured, for they were not yet optimized for ultra low power. The second half of the chapter covers the implementation on-chip of the wakeup receiver. This is based on the results of the discrete implementations with main focus on the power consumption of the circuit.

Chapter 5 shows the results reached by the implementation and compares them to the expected results from chapter 3. All the performance of the building blocks of the wakeup receiver are measured and compared to the expected values. An overall evaluation of the wakeup radio as part of the sensor nodes is given.

Chapter 6 concludes this work with an overview and the vision for future works based on the concept of wakeup receivers.

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Acronyms

ADC	Analog to Digital Converter
ALU	Arithmetical Logical Unit
API	Application Programming Interface
ASK	Amplitude Shift Keying
BAW	Bulk Acoustic Wave
BER	Bit Error Ratio
CAD	Computer Aided Design
CHLL	Configurable High Level Logic
CPLD	Complex Programmable Logic Device
CPU	Central Processing Unit
CSMA	Carrier Sense Multiple Access
DLL	Delay Locked Loop
DSP	Digital Signal Processor
EMU	Energy Management Unit
FEC	Forward Error Correction
FPGA	Field Programmable Gate Array
FSK	Frequency-Shift-Keying
GPS	Global Positioning System
IDE	integrated Development Environment
I ² C	Inter-Integrated Circuit
ISM	Industrial Scientific Medical
LDO	Low Drop Output voltage regulator
LNA	Low Noise Amplifier
LUT	Look Up Table
MAC	Medium Access Control
MCU	Microcontroller Unit
MEMS	Micro Electromechanical Systems
OOK	On-Off-Keying
PAWiS	Power Aware Wireless Sensors
PCB	Printed Circuit Board
PLL	Phased Locked Loop
PWM	Pulse Width Modulation
RF	Radio Frequency
RFID	Radio Frequency Identification
RTC	Real Time Clock

SAR	Successive Approximation Register
SBER	Synchronized Bit Error Ratio
SIP	System-in-Package
SMD	Surface Mounted Device
SNR	Signal to Noise Ratio
SoC	System-on-Chip
SPI	Serial Peripheral Interface
TPMS	Tire Pressure Monitoring System
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
WSN	Wireless Sensor Network
WUR	Wakeup Receiver

1 Introduction

A Wireless Sensor Network (WSN) is a network consisting of devices that collect environmental data and transmit it with a radio to a higher hierarchical elaboration unit (as shown in figure 1.1 from [4]). Such networks are typically deployed in environment monitoring applications [Pot98]; although the initial motivation thrust of research in this field was military battlefield surveillance, contributing to the ubiquitous computing concept. The typical node is equipped with a micro controller, a wireless communication physical layer and at least one sensor. Such nodes are required to be small scaled so that they can be hidden practically anywhere in the environment.

Some research projects, like EU founded eCubes [RTW08] [12], are willing to integrate a whole sensor with chip stacking techniques in a single minute silicon box. Due to the small dimensions, energy which can be stored or harvested (e.g. from solar panels or piezoelectric elements) is actually very limited. The different environments where a node can be deployed require it to be resistant to harsh stress conditions, such as extreme temperatures or high accelerations. Some sort of redundancy in the positioning of nodes must be taken into account because node failures are likely to happen. Fixed routing in such networks makes less sense because the communication itself represents about 75%-80% of the total power consumption of such nodes [Mah04, p. 136]; therefore it makes sense for routing to choose the best path dynamically, otherwise the consumption can not be balanced between nodes. Because the node is completely unwired from power sources, the energy management must be accurately planned. The energy will be typically stored in a battery or scavenged from the environment through solar panels or mechanical energy generators. The mobility of the nodes and the energy management result in a dynamic network topology, where the nodes can dynamically route messages in the most efficient way to the destination, taking the own energy reserve into account, but also the reserve of the surrounding nodes.

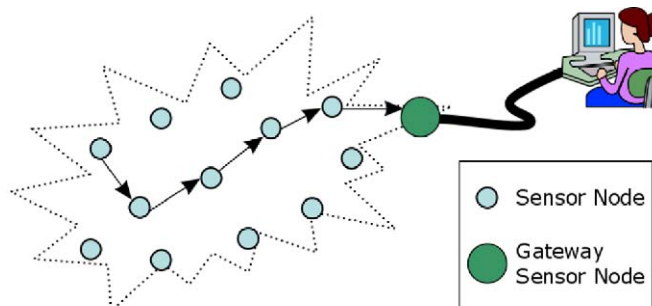


Figure 1.1: Wireless Sensor Network example from [4]

Because of the small energy reserve a node can have, it is not always possible for the nodes to communicate directly with the data collecting base station. Communication failures which can occur also demonstrate the need of dynamical routing. Such types of networks do not constrain the construction and functionality of such nodes, but enhance their application fields by allowing complete heterogeneity. This also allows large scales of deployment (hundreds of nodes) without affecting operation, which in each case should work unattended.

This chapter will to give an overview of the present and future use of WSNs, and a description of the goals of this work. The many fields where WSNs are a key to success in realizing the intelligent environment are the justifications to the great research efforts that have been done. This work will contribute to the field of wireless sensor networks by presenting an innovative architecture for radio communication, which will extend the projected lifetime of a node relying on limited energy sources such as batteries. The result, matched with improvements in network protocols that take into account the energy of the nodes and of the whole network will be a wireless sensor network that is capable of relying on limited energy sources for years, not sacrificing throughput and latency for lifetime.

1.1 Fields of application

The main application scenarios in WSN include building automation, car automation, health care applications, traffic control and container tracking. A small overview of the huge range of different applications that can be made possible will be given here.

In the case of building automation [RKNG07] (figure 1.2), it is possible to imagine modern skyscrapers with hundreds of floors, fifty rooms each floor. Monitoring the environment of each room means measuring, for instance, temperature, humidity, human presence, which are easy tasks with modern electronics. Such a cabled network needs kilometres of copper, precise planning and installation during the construction of the building, leaving no chance for later radical changes in the system at low effort and cost. Using self-powered nodes communicating via radio would represent a valid substitution to wired networks and increase the flexibility and expansibility of the system. Maintenance would be reduced to battery change, which would occur each five to ten years, and would not require a technician to do the job. Substitution of meters of cable is in contrast a complicated and expensive job. Such complex systems have begun to find their way in the commercial market, as shown in [Whe07] and [Gut04].

Another completely different scenario is represented by car automation (e.g. figure 1.3 by [29]). The weight of copper cables in a car can reach 50 kg of weight, 5 km length and mounting costs comparable to the mounting costs of the engine [Chi96], [Kop97]. Maintenance is also in this case very complicated, due to the high density and related work to replace cables. In this field there are a lot of sensors which are not strictly safety related; therefore, they are for the time being eligible to be substituted from their wireless equivalents. Some obvious examples are temperature and humidity sensors, but also seat presence sensors, parking sensors or Tire Pressure Monitoring System (TPMS), which is the main driver for the Power Aware Wireless Sensors (PAWiS) research project related to this work.

Pervasive WSN seem to be a very interesting topic for the health care industry (as [SCL⁺05], [MEEE06] and [BA07]). Patients could constantly carry small and imperceptible sensors that would collect data such as blood pressure, body temperature or pharmaceutical intake. This data could be collected and mined at home or in the clinic for monitoring purposes, analyzed

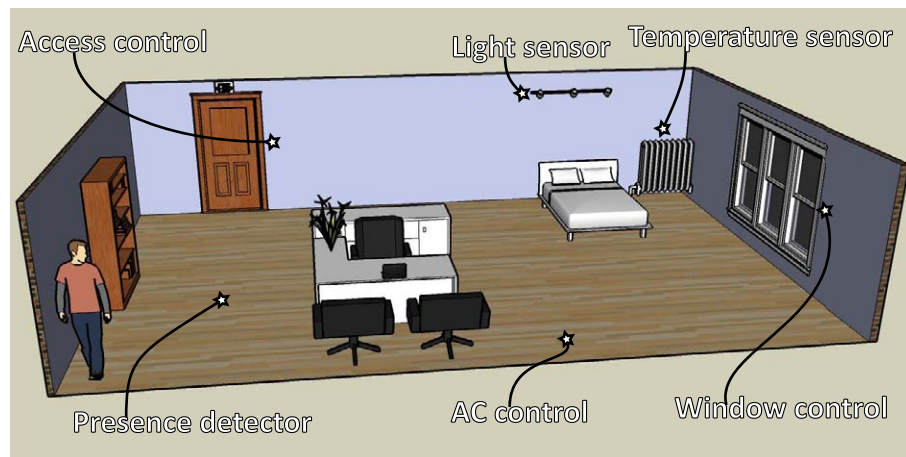


Figure 1.2: Building automation example

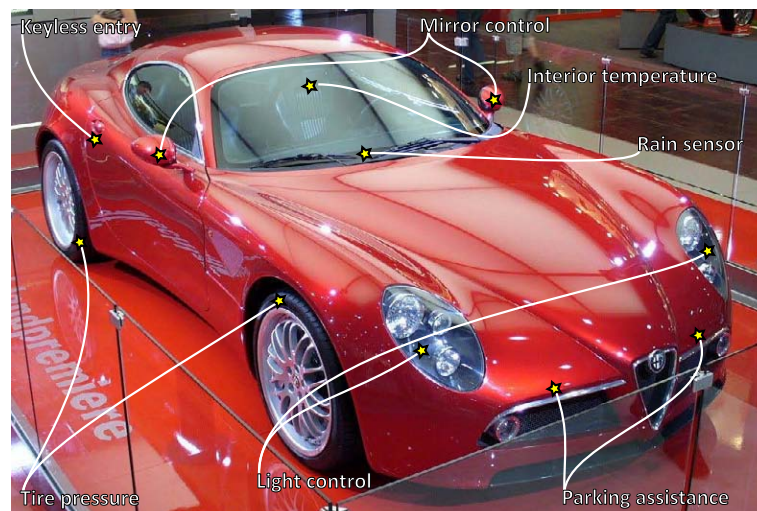


Figure 1.3: Sensors in car automation, photo from [29]

by the doctor while in visit, benefiting not only the patient, but also research on biological and pharmaceutical effects on the human being. As human beings get older, a more discrete and more efficient control of medical parameters could be vital in cases of emergency.

Traffic control could be enhanced by car-to-car communication or dynamic traffic light operation embedding sensors on roads, signs and vehicles (as shown in [RS07], [LL07] and [CCV04]). This could enhance the fluidity of the traffic and prevent traffic jams by transferring live information on car accidents or other causes of problems directly to the in-car navigation systems based on Global Positioning System (GPS) or other positioning systems. Heavily busy road crossings could be optimized for higher car “throughput” instead of normal fixed time behavior by measuring how long the queue on each direction is.

Container tracking, on the other hand, is an application where wireless solutions begin to be developed (see [Sch06], [MM07b] and [BBC⁺07]) because of their complexity and number, as shown in figure 1.4. The idea is to equip containers with GPS sensors, intrusion detection or temperature sensors. The containers located on a port or on a ship could communicate their status to a controlling service or to the owner through on-site infrastructure. While being transported



Figure 1.4: Container terminal from [2]

on a ship, some elected containers could connect via satellite communication, or through ship infrastructure, to transmit data relevant to the owners of the carried goods [MM07a].

This work has been realized as part of the PAWiS project [16], a great contribution to the topic of WSN, which are indeed a very promising market. The outputs of the project are directed to different levels of support to the realization of network nodes. The main subprojects of PAWiS are the simulation framework, the Energy Management Unit (EMU), the Configurable High Level Logic (CHLL) and the Wakeup Receiver (WUR) which is the subject of this work.

For the realization of nodes and networks, a simulation framework [GW07] based on Omnet++ [Var01] has been implemented. The framework helps simulate the behaviour of the nodes and then the behavior of the whole network, focusing especially on the energy resources of both software and hardware issues. This allows an estimation of the projected life of the nodes and of the whole network. The framework supports high modularization of the nodes, such that it is possible to try different implementation of some building blocks of the node (e.g. the Medium Access Control (MAC) layer) without changing the rest of the simulation environment and is intended to be used in a cyclic development scenario. Classes to handle the inter-node communication that considers spatial distribution and noise within the network are provided as well as bit error rate and behaviour of the communication facilities. The CPU can be accurately modeled with power states and interrupts, and the power consumption can be parameterized in integer, float, flow and memory access operations. The normal node is divided generally in the following blocks: the application, the (possibly hierarchical) power supply, the MAC layer, the sensors and the physical communication layer. The application is responsible for the control of each other block. It acts as a controller for each action that occurs in the node. For example, it decides how much and how long the CPU is used to elaborate any incoming packets. In this way, it is possible to accurately model the power consumption of hardware only, software only or mixed tasks. The framework cares for the parallelization of tasks and the queuing of interrupts. On the other hand, the application must ensure that the CPU is not overloaded, since it could be possible to schedule two tasks at the same time, but the framework is aware of CPU utilization and will warn in this case.

The EMU is a complex controller that is able to generate from one source all possible supply voltages that are needed by a sensor node. There are many possible sources that can supply

such a node: a battery, a solar panel, a piezoelectric generator (generates electric energy from mechanical energy) and other energy scavenging sources. All these sources have actually not much in common in matter of total energy available and source resistance (which is sometimes energy dependent); therefore, the EMU must be equipped with all sorts of voltage regulators: buck converter, boost converter and Low Drop Output voltage regulator (LDO). The input voltage is converted to a temporary storage and then converted to multiple outputs. The unit is fully controllable via digital interface, for example with a Serial Peripheral Interface (SPI) bus, and the operation can be modeled in multiple power modes. The EMU should contain some facilities to better control the sensor node such as a watchdog timer or a Real Time Clock (RTC). The EMU will be realized on silicon.

The main task of the CHLL is the building of a library of hardware digital blocks that realize a customizable and dynamically reconfigurable high level logic function. The idea is to create a sort of Field Programmable Gate Array (FPGA) which does not rely on the basic Look Up Table (LUT), but on coarse grained functions, such as adders or multipliers. Together with high level functions, a concept for the routing, that is also a high power consuming part, is also included. On the software side the logic is supported by a custom tool chain. A methodology to develop such libraries is also focus of the subproject. The main focus of the library is of course on ultra low power consumption, but also flexibility, such that simple control logic for a mixed-signal device can be developed in short times.

This work focuses on the WUR which will be explained later in chapter 3. The WUR is the hardware implementation of a MAC and physical layer protocol that enables a node of a WSN to save energy not putting any constraints on the responsiveness of the whole network. The work has been proofed on silicon.

1.2 Problem statement

The realization and integration of such pervasive sensor networks is of obvious interest for both the scientific and industrial world. All possible advantages of wireless sensor networks are realizable if the nodes are able to survive relying on low energy sources such as a battery or solar panel for several years. This constraint is actually a very diffused research topic in electronic as a whole, but

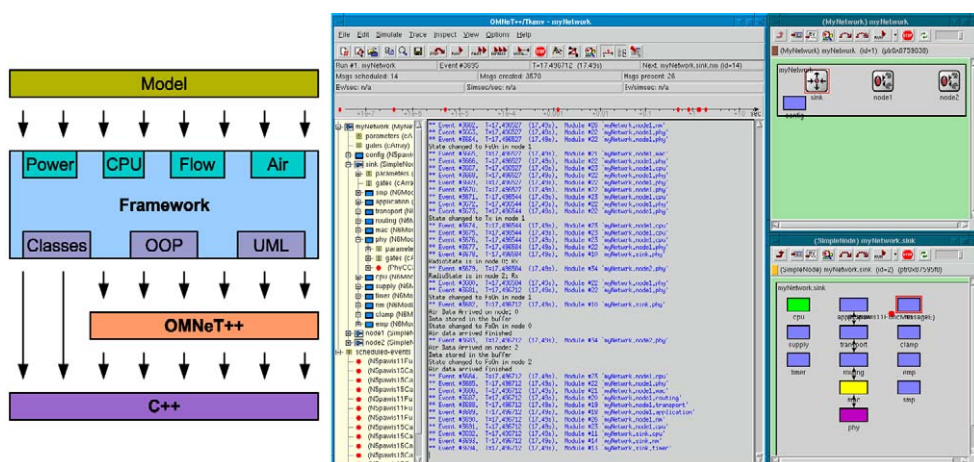


Figure 1.5: Framework and Omnet++ simulation

is also moved by social and economical reasons. Using such networks to prevent wasting Earth's energy resources are certainly of great importance, but also better care for human life can be achieved. The driver for TPMS [TLR⁺08] (see figure 1.6) systems is actually a bill of the United States of America that was disclosed based on the statistics that a high proportion of car accidents is due to tire failure, and that it could be prevented by accurate monitoring of the pressure. The PAWiS project focuses on researching hardware solutions to improve energy consumption of integrated sensor nodes and on simulation of power consumption for such networks. As stated in [MGH05] "...the goal of this project is to develop both efficient system architectures and the related design methodology for power aware Wireless Sensor and Actor Network nodes that allow for capturing inefficiencies in every aspect of the system. These aspects include all layers of the communication system, the targeted class of the application itself, the power supply and energy management, the digital processing unit and the sensor-actuator interface. The evaluation will be based on a prototype system that allows a future integration in a single System-in-Package (SIP) or System-on-Chip (SoC) package.". The evaluation of the system will of course be based not only on a prototype but on reliable simulation results.

The main challenge developing such nodes is to achieve real ultra-low power consumption by preserving low hop-to-hop delay and high data rate transmissions. The normal way of economizing the reserve of energy is to power-down all the devices which are unused except for those vital functions which must have, in each case, ultra-low power consumption. To reach such low power consumption, an optimization of each building block of the single node must be done, as well as an overall optimization, which indicates the need of developing SIP or SoC to realize such nodes, but also network-level energy preservation techniques.

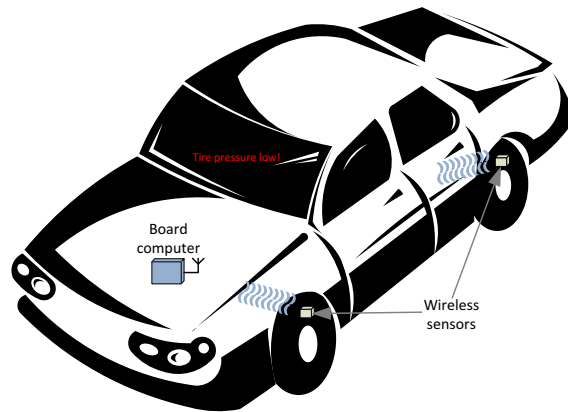


Figure 1.6: Tire Pressure Monitoring System (TPMS)

Using state of the art batteries such as Lithium-Ion or NiMH, energy between 5 and 6 Wh can be stored using 2 to 4 AA sized batteries (see 2.1.4.1). If we consider that a complete node should consume a mean power of $50 \mu\text{W}$ to reach a 10 year lifetime, the maximum mean power budget that the radio communication is allowed to use should be limited to around $10 \mu\text{W}$ ¹, to leave enough energy for the other parts of the system. This is obviously a great challenge as state of the art transceivers need tens of milliwatts when active and must be managed to be off the most the time to lower the power consumption. This leads to great limitations in the communication

¹see chapter 4

capability, which can be circumvented if the radio is always active. This is why the goal of this work is a receiver that consumes less than $10\ \mu\text{W}$ in active mode.

1.3 Tasks and objectives

This work proposes a solution as to how to lower both power consumption and latency in peer-to-peer wireless sensor networks. These are usually strictly connected when using the protocols which will be presented in chapter 2. As usual practice power consumption can be lowered by switching off parts of a system which are not being used. For communication, this means switching the radio receiver on and off periodically; otherwise, no communication is possible. This introduces us to the problem of synchronization: if the nodes are synchronized, then the power consumption can be reduced by growing the time the radio receiver is switched off. In this manner, virtually any power consumption goal can be achieved. Perfect synchronization is not possible, but reasonable results can be achieved by updating the timer periodically. This needs additional protocols and obviously increases power consumption, although it can also be seen as additional network traffic, therefore can be easily quantified. Obviously no communication occurs when the radio is switched off, thus the system has intrinsic latency. This is extended by the fact that depending on how many packets can be processed each period, it can be said that for a state of the art protocol that each hop needs a full time period to forward a packet. In this case, the latency is related to the hop count and to the periodicity of the radio protocol. If the radio is active once each second, then each hop needs at least one second. Clearly, such constraints lower considerably the responsiveness of the network. The proposed work uses a second radio receiver that is used to remote control the main radio. In this way the power consumption can be reduced to a minimum and the radio can be used only when needed, without unnecessary periodical switching on-off. This second radio must consume at least three orders of magnitude less of the main radio otherwise no advantage in its use can be achieved. As this second radio is always active, the latency for each hop is reduced in the best case to the sum of the duration of the packets including all overhead and resides in the range of the millisecond, whereas with state of the art protocols this is a key parameter to power consumption and usually resides in the second range, i.e. three orders of magnitude longer.

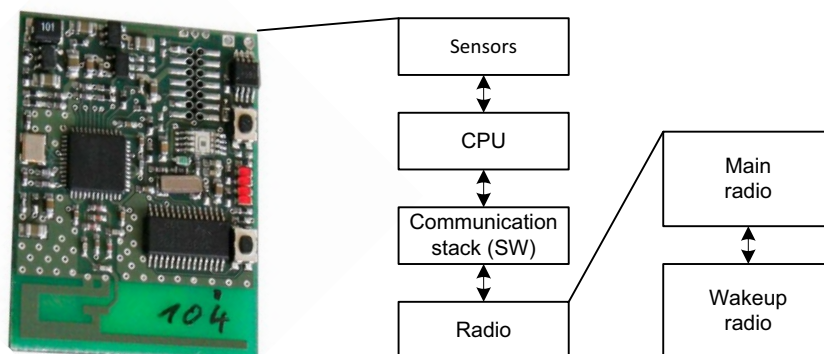


Figure 1.7: Proposed sensor node

The problem to be solved is the engineering of new MAC and physical layer protocols, which allows the activation of neighbouring nodes without a time-schedule mechanism. This would break the trade off mechanism between power consumption and hop-to-hop delay resulting in a highly enhanced responsiveness in forwarding requests and responses in a WSN preserving long life of the nodes. The problem involves particular attention to low-power circuit integration of the physical layer as well to communication protocols to enhance the overall life of the network.

Most of the power consumption of single nodes of wireless sensor networks is dissipated from the RF-transceiver. To reduce this to the minimum, it is necessary to power up the node and particularly the radio transceiver exclusively for successful communication. This introduces the problem of synchronization between nodes, which practically means using particular protocols and handshake procedures, which rely on enabling the receiver periodically, to check if communication is occurring. In such wireless sensor networks the traffic is sparse, resulting in wasting the receiver's energy if no transmission occurs. In order to make such communication really efficient, some type of mechanism is needed to act as a *remote controller*, which is able to activate the receiver on the destination node, such that energy is used only when a communication is effectively needed. This *remote controller* is a radio receiver called *wakeup receiver*. A power consumption of $10\ \mu\text{W}$ in lowest-power state would allow a life of several years for a typical node. To reach this ultra-low power consumption, the receiver must be as simple as possible, completely passive if possible. Such a simple receiver simply needs a diode and a capacitor, in the same way the very first AM receivers were realized. Such simple circuit converts RF power in voltage, rectifying the signal. If the transmission is modulated with On-Off-Keying (OOK), the signal is demodulated directly from such a circuit. The low efficiency of such rectifiers and the low power involved in radio transmission show the need of some signal processing. Analog signal processing is expensive in term of power consumption if compared to similar tasks which can be performed in the digital domain. Various simulation results point out the benefit of such a module on the whole network life. The simulations at network level show that the medium life of the single node improves by 50% compared to the same node with CSMA-MPS MAC protocol [MB04] implementation.

The proposed solution is a receiver that is always powered on, waiting for incoming communication coupled to a simple yet very efficient MAC protocol. This receiver must consume some μW to achieve several node life years. Normally a standard receiver for the 2.4 GHz Industrial Scientific Medical (ISM) band consumes 30 mW [26]. The architecture is the typical super-heterodyne that needs some basic building blocks, such as a mixer or the Phased Locked Loop (PLL) that are very power consuming. The approach to the solution is, for this work, the relaxation of some constraints in the robustness of the receiver and in the amount of exchanged data by simplifying the architecture of the power consuming building blocks. The simplified receiver (WUR) does not replace the main receiver for the data communication, but acts as a controller for the remote activation of the node. The complete concept for the node architecture is presented in this work and also the implementation of the wakeup receiver and of the required protocols.

2 State of the Art: wireless sensor networks nodes

A sensor network node is a complex system realized mostly with separated microcontroller units (MCU), sensors, wireless communication layers and other building blocks, although the trend integrates more of these blocks on a System-on-Chip (SoC) solution. It has already been stated that 75%-80% of the power consumption of such nodes comes from the wireless communication [Mah04, p. 136], but this is related to the strategy of the Medium Access Control (MAC) layer protocol. Usually, for this type of network, all data is sent to one master node (also called sink node) which has the task of collecting data and taking actions, such as reporting unexpected changes in the measured values. The energy of the node can be preserved using intelligent routing protocols that take remaining energy into account to decide the best route to the destination. A typical application for Wireless Sensor Network (WSN) is building automation. As battery based sensor nodes are capable to transmit indoors in a range of 10 m, not every node will connect directly to the sink node. Each node can act, as well as measure station or as router for incoming packets. Publications such as [MMR06] or others show routing protocols developed for low power sensor networks. The routing is dynamically adjusted based on information of energy, position or higher level data. If nodes are deployed all over the rooms of a building, then there are multiple paths through which a packet can travel to the sink node. An intelligent network preserves its overall energy, not only the energy of the single node, but this task is achieved through intelligent use of communication channel. In the next sections, a bottom-up description of typical wireless sensor nodes will be given. The focus on each building block (hardware or software) is mainly set on the energy consumption as it influences the usability of the network. Up to now, home automation is a luxury feature which could be transformed from niche-market to mass-market if sensor nodes are built to consume much less energy.

2.1 Node Architecture

The architecture of sensor nodes will be analyzed in depth in this chapter, as it is compelling to detect which are the weak spots in matter of power consumption and what possible workplaces would optimize them. The following subsection presents each block that composes sensor nodes, analyzing its implementation found in the mass-scale market. The general architecture of a sensor node (figure 2.1) must be simple because the energy aspects are of great importance. Energy supply is usually limited to a small battery that cannot supply more than some Ah. Typically

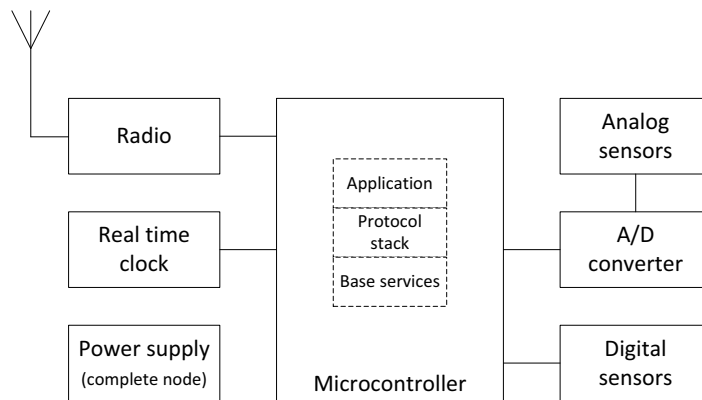


Figure 2.1: Example node architecture

the node will be built out of a Serial Peripheral Interface bus or other serial buses because they are less energetically expensive compared to parallel buses, but also because they need fewer connection pins resulting in smaller footprints on the devices, also saving Printed Circuit Board (PCB) production costs. On the other hand, the protocol overhead is given using such buses that cannot be underestimated because it results in longer use of the MAC-PHY interface. These buses normally allow one master and some slaves, although Inter-Integrated Circuit (I²C) is also specified for a multi master environment. The Microcontroller Unit (MCU) needs to start the sensor and the Analog to Digital Converter (ADC) starts the conversion of the measured value, makes some calculations on the data, verifying a divergence from the old measured value and in the case send the data. At this point, all measurement devices can be set to sleep and the communication phase begins. The Radio is started, the oscillator locks the frequency, and meanwhile the Central Processing Unit (CPU) calculates the best route for the data to the sink. If the channel can be accessed successfully then the packet is sent. This is a simplified procedure of the simple task of sending a data packet, but to build a functioning multi-hop network, routing packets must also be sent to fill the routing tables of each node. Energy efficiency is achieved mainly by optimizing the communications intra-node but also inter-node because heavy *service* network traffic also has a negative influence on the life of the node.

2.1.1 Microcontrollers

Although there are some implementations in the literature (see [WP04]) of microcontrollers specifically implemented for a sensor node, this section will analyze commercial solutions. The first low power architecture analyzed is the 4-bit MARC4 [6] from Atmel Corporation. The target of this core (that is embedded in some differently equipped microcontrollers) are wireless applications such as remote keyless entry, immobilizer systems, wireless keyboards for PC and multimedia, wireless sensors and other data control applications, using wireless communications. The core is a RISC architecture that runs at 2 clock cycle instructions. In active mode, the current consumption is specified at 180 μ A. The whole controller integrates special peripherals such as high performance oscillators, power on reset, watchdog, serial parts, multifunction timers-counters and flexible I/O structures with key interrupt functions and EEPROM modules. The MARC4 instruction set is optimized for a high level programming language called qForth that actually is a 4-bit version of the FORTH-83 standard. The choice of this language is that the MARC4 core and qForth are both stack oriented. qForth is a high-level programming language that has an

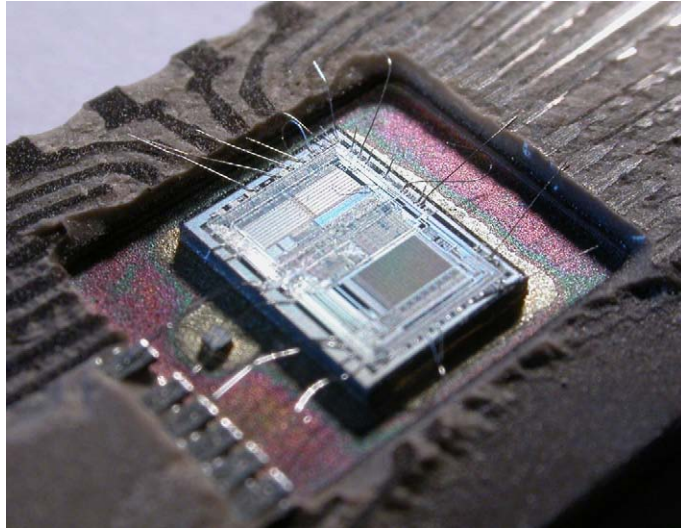


Figure 2.2: Microcontroller die photograph from [18]

efficient memory usage strategy and many of the qForth instructions are directly implemented into the MARC4 instruction set. The development of qForth was focused on real-time instruction execution. The language has instructions for arithmetical and logical operations, control structures like loops and conditional branches, memory operations, 4-bit and 8-bit comparisons, stack operations and compiler directives. Many qForth instructions can be found in other programming languages such as C and Pascal. Most of the MARC4 instructions are single byte instructions that can be executed in one instruction cycle and their values are taken from the stack. The ATAR080 is an example of microcontroller that embeds the MARC4 core. This microcontroller supports supply voltages between 1.8 V and 6.5 V, has a watchdog timer, has power on reset and brown-out function, has two multi-functional timers-counters, has 2048 byte ROM and 1024 bytes for test purposes, has 256 nibbles (4-bit words) RAM, has twelve bi-directional ports including four high-current outputs, has a 8-bit synchronous serial interface, has battery-low detection, has a comparator for zero cross detection, has three internal and four external interrupts, has an internal 32 kHz quartz oscillator, has an internal 4 MHz oscillator and works at operating temperatures from -40°C to $+85^{\circ}\text{C}$.

Another example from Atmel Corporation is the AVR 8-bit MCU [5] that offers a true RISC architecture, single cycle execution ($\frac{1\text{MIPS}}{\text{MHz}}$), 32 general purpose registers, Harvard architecture, 1.8 V to 5.5 V operation, a variety of sleep modes, and On-Chip Debugging. The AVR core combines an instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetical Logical Unit (ALU) allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The ATmega644 (taken as example) provides the following features: The power saving features are interesting; idle mode stops the CPU while allowing the SRAM, Timer-Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents, but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I-O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal-Resonator Oscillator is running while the rest of the device is sleeping. This allows fast start-up combined with low power consumption. In Extended

In-System Programmable Flash	64 kBytes
EEPROM	2 kBytes
SRAM	4 kBytes
General purpose I-O lines	32
General purpose working registers	32
Real time clocks	1 running at 32 kHz
Timer-Counters with compare modes and PWM	3
USARTs	2
2-wire Serial Interface	1
10-bit ADC	1 with 8 channels
Watchdog Timer	1
SPI serial port	1
JTAG test interface	IEEE std. 1149.1 compliant
Power saving modes	6 (software selectable)

Table 2.1: ATmega644 features

Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high-density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation.

The MSP430[27] family of ultra-low-power 16-bit RISC mixed-signal processors from Texas Instruments is also targeted to battery-powered measurement applications. Typical applications include measuring instrumentation, electronic sensors, and consumer electronics. The architecture is a 16-bit RISC CPU, peripherals and flexible clock systems are combined by using a von-Neumann common memory address bus and memory data bus. The key features are ultra-low-power architecture: 0.1 μA RAM retention, real-time clock mode and 250 $\frac{\mu\text{A}}{\text{MIPS}}$ active mode. The MCU is equipped by many and offers a wide range of capabilities from a simple low power controller with a comparator, to complete systems on a chip including high-performance data converters, interfaces and multiplier. The MSP430F1132 is used in the Tinymote sensor node, as described in section 2.1.7.

Cypress PSoC [11] Mixed-Signal Arrays are programmable systems-on-chips that integrate a microcontroller and the analog and digital components that typically surround it in an embedded system. A single PSoC device can integrate as many as 100 peripherals with a microcontroller. Its main features are Rail-to-Rail configurable analog blocks that provide up to 14-Bit Serial Peripheral Interface (SPI) masters and slaves. The MCU provide 32K bytes flash memory, 2K bytes SRAM, internal oscillator crystal, two 8x8 multiply, 32 bit accumulator, I²C slave and master and full speed Universal Serial Bus (USB) 2.0.

2.1.2 Sensors

There is a huge variety of sensors available off-the-shelf and many of them are already optimized for low power consumption. These are used in mostly different applications and are typically provided with a digital interface (a serial bus) that makes the integration in a microcontroller

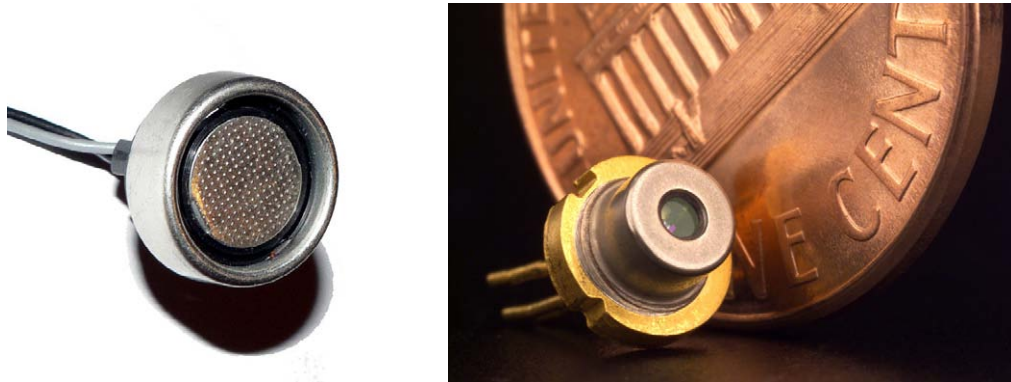


Figure 2.3: Electronic sensors from [9] and [24]

based system seamless. A good example of light sensor is represented by Intersil's ISL29020 [17]. The sensitivity of this sensor is set in the human eye range: the maximum current draw in active mode is $65\ \mu\text{A}$ at $3.3\ \text{V}$ and the measured range is divided into sub ranges that span 0.015 to $64000\ \text{lx}$. The sensors are packaged in $2.0\ \text{mm} \cdot 2.1\ \text{mm}$ and use the I^2C bus as interface. Pressure sensors are usually micromechanical elements and are practically equivalent to a resistor bridge. An ADC and some analog signal treatment are needed to digitalize the measured ambient pressure. Various working ranges are offered from 0 to over $1000\ \text{kPa}$. Temperature sensors are the most common digital sensors, most measure the forward voltage of a calibrated diode to calculate ambient temperature. Many sensors are also not provided by diodes and offer a connection for diodes included in other integrated circuits, such as modern CPU. The measured temperature ranges equal the working range of the IC and accuracy lies in the order of $\pm 0.5^\circ\text{C}$ (but usually not over the whole temperature range). These sensors are also interfaced by SPI or I^2C buses but also voltage or Pulse Width Modulation (PWM) is available. Acceleration sensors are also widely used in many systems, ranging from airbag system to home entertainment consoles. Measured accelerations ranges lie typically between $\pm 1\ g$ and $\pm 2000\ g$, and the sensor is equipped with one, two or three orthogonally arranged axes. The interfaces are analog or digital. Contact sensors are more mechanical than electronic devices and can be seen as normal switches. Presence sensors are typically used for security purposes and are infrared light sensors. A change in the response of the mean infrared power measured is signalled as alarm. These sensors also provide a switch like interface. Gyroscopic sensors detect rotation and return a value representing the number of degrees per second of rotation. This sensor can measure up to $\pm 360^\circ$ per second of rotation and are used for example by navigation purposes. The interface is usually analog. The Hall Effect sensor is capable of measuring magnetic field and to convert it to voltage. These are used in some applications where proximity must be measured, but no contact is allowed mainly for security reasons.

2.1.3 Low power glue logic and analog building blocks

This section reviews some commercially available low power analog and digital integrated circuits that are used in wireless sensor nodes.

The MAX95x is manufactured by Maxim [3] and features combinations of a micro power operational amplifier, comparator, and reference in an 8-pin package. In this component the compara-

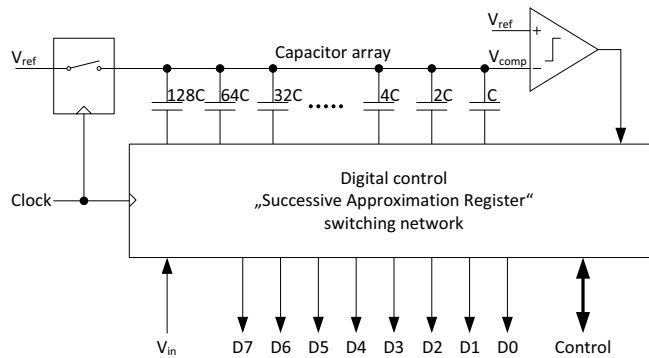


Figure 2.4: ADC architecture from [SBP03]

tor's inverting input is connected to an internal $1.2V \pm 2\%$ bandgap reference. Variants of this comparator are also offered without internal bandgap reference. The MAX95x equipped with bandgap operates from a single 2.7 V to 7 V supply with a typical supply current of $7 \mu\text{A}$, while the versions without reference operate from 2.4 V to 7 V with a $5 \mu\text{A}$ typical supply current. Both the op amp and comparator feature a common-mode input voltage range that extends from the negative supply rail to within 1.6V of the positive rail, as well as output stages that swing rail-to-rail. The operational amplifiers offered are both internally compensated to be unity-gain stable and uncompensated with 125 kHz typical bandwidth, $66 \frac{\text{V}}{\text{ms}}$ slew rate, and stability for gains of $10 \frac{\text{V}}{\text{V}}$ or greater. These operational amplifiers have an output stage that operates with ultra low bias current while maintaining linearity under loaded conditions. The comparator output stage of these devices continuously sources at maximum 40 mA.

As example ADC the MAX1108 low-power, 8-bit, dual-channel is chosen. It features an internal track/hold voltage reference, clock, and serial interface. The MAX1108 is specified from 2.7 V to 3.6 V and needs only $105 \mu\text{A}$. All analog inputs are software configurable, allowing unipolar/bipolar and single-ended/differential operation; battery monitoring capability is also included. The ADC features a software power-down mode that reduces current consumption to $0.5 \mu\text{A}$ when the device is not in use. The device is accessed directly through industry standard 4-wire serial interface without external logic. Conversions up to $50 \frac{\text{samples}}{\text{s}}$ are performed using either the internal clock or an external serial-interface clock.

There are some interesting approaches to the architecture of ADCs for WSNs; one is presented in [SBP03]. This design offers ultra-low power consumption and was developed bearing in mind the following constraints:

- Energy consumption $< 1 \frac{nJ}{8 \text{ bit sample}}$
- Low-power deep-sleep standby mode
- Supply voltage $\sim 1 \text{ V}$
- At least 8 bit resolution
- Maximum sampling rate at least 10 kHz
- Rail-to-rail conversion range

- Reduced resolution function as digital comparator (e.g. $X < V_{in} < Y$)

The design requires a Successive Approximation Register (SAR) architecture because it enables both ultra-low power consumption due to the low use of analog blocks and because of its flexibility that comes from the configuration of the binary search. The binary search can be linear starting from the first code or reconfigured to other starting points and code jumps rendering the ADC flexible. The normal operation samples the reference voltage on the capacitor array and compares it to the input voltage. Depending on the result the next approximation code is chosen via binary search. These operations are iterated until the required resolution is reached. For an N-bit resolution N iterations are required. The results of this design are resumed in table 2.2.

Voltage Supply	1 V
Sampling rate	100 kHz
Power dissipation	3.1 μ W
Energy per sample	31 pJ
Standby Power	70 pW
Die area	0.053 mm ²
Process	0.25 μ m CMOS

Table 2.2: ADC performance from [SBP03]

Complex logic circuits are sometimes realized by the means of a Field Programmable Gate Array (FPGA) or a Complex Programmable Logic Device (CPLD) because of flexibility in changing the design. These devices are re-programmable and allow successive adaptation if design changes are needed. FPGA are usually focused on high performance and are not suitable for sensor nodes because of the power consumption. CPLDs offer low power consumption allowing realization of smaller circuits. An example of ultra low power CPLD is based on Lattice's ispMACH 4000 architecture: the family of devices delivers both low static power and high speed. Devices operate from a 1.8 V supply providing low dynamic power. The 1.8 V ispMACH 4000Z family supports a wide range of 3.3 V, 2.5 V and 1.8 V I/O standards and features 5 V tolerant I/Os when using the LVC MOS 3.3 V interface. Devices are available in commercial, industrial and automotive temperature ranges. This product offers the performance resumed in table 2.3.

Standby current	10 – 13 μ A
Standby power	18 – 23 μ W
Pin-to-pin delay	3.5 ns
Max clock frequency	267 MHz
Pin-to-pin delay	3.5 ns
Global Clocks	4
Inputs per Logic Block	36
Product Terms (PT) per Output	up to 80
Boundary Scan Test	IEEE 1149.1
In-System Programmable	IEEE 1532
Automotive temperature range	–40...130 °C at Junction
PCI compatibility	3.3 V
I/O Support	1.8 V, 2.5 V, 3.3 V
Power supply operating range	1.6 – 1.9 V

Table 2.3: ispMACH 4000Z family typical performance

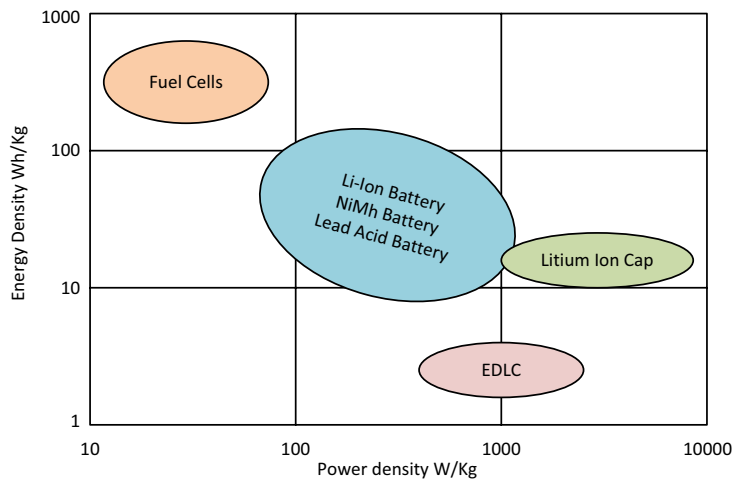


Figure 2.5: Battery comparison from [20]

2.1.4 Energy sources

As wireless sensor nodes cannot rely on wired power supply from the outlet, this section will give a broad overview of the various energy sources that are eligible to supply a low power sensor node. There are two main categories of energy supplies that can be considered for sensor nodes: energy storages, such as a battery or a capacitor, and energy scavenging units, such as solar panels or piezoelectric elements.

2.1.4.1 Rechargeable batteries

The most common energy source for portable devices is the rechargeable battery. This fundamental object for the modern connected world has developed quite a bit in the latest years and although this is not the place for an accurate analysis of its developments, it can be stated that battery technology did not hold the size shrink and performance rise of integrated circuits. As a matter of fact, the cost and energy available from a battery imply the designer of sensor nodes have to use power management strategies if the nodes are to last ten years or more.

As figure 2.5 shows, different chemical components and materials result in different power and energy density, which are parameters that have quite a bit of weight in the choice of the appropriate energy source. The key design factors that need to be evaluated when choosing the appropriate battery for wireless sensor nodes can be summarized here:

- Self discharge rate
- Capacity (depending on current draw)
- Energy storage
- Energy density

The use of rechargeable batteries does require some sort of circuitry if charging is somehow done from the node, but in this case particular sources are employed, such as those explained in the

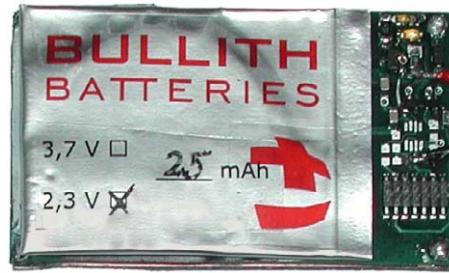


Figure 2.6: Bullith battery

next sections. Issues and challenges facing Lithium Ion rechargeable batteries can be found in [TA01]. An example of a commercially available battery that would fit WSNs is the Energizer L91 [13]. Its details are shown in table 2.4. This is an off-the-shelf product that can be considered in WSN applications thanks to its low discharge rate. This is a non-rechargeable battery; therefore replacement is needed when the battery drains. Commercially-available rechargeable batteries in AA size offer from 1500 mAh to 2500 mAh that can be used to supply a sensor node by using a combination of two or more batteries, either in series or in parallel. As shown in [Röt04], there are many energy supply devices that fit the power need of a sensor node. Although there is apparently not much development in battery technology, an exception is presented from Bullith Batteries AG [10] with their foil accumulator. This accumulator (see figure 2.6) can be manufactured at customer's choice dimensions. Typical design values are presented in table 2.5. This battery was evaluated and used for Tiny mote nodes (see section 2.1.7) and the results are resumed in [Röt04].

Chemical system	Lithium/iron disulfide (Li/FeS_2)
Nominal voltage	1.5 V
Typical weight	14.5 g
Typical volume	8 cm ³
Max discharge	2.0 A DC and 3.0 A 20% pulsed
Typical Li content	0.98 g
Typical internal resistance	90 to 150 m Ω
Shelf life	15 years at 21°C (90% of rated capacity)
Typical capacity	3000 mAh

Table 2.4: Energizer L91 specification

Anode	Lithium-Titanium
Kathode	Lithium-Cobalt
Energy density	140 – 180 $\frac{Wh}{L}$
Specific energy	> 65 $\frac{Wh}{kg}$
Nominal voltage	2.3 V
Capacity	10 – 5000 mAh

Table 2.5: Bullith Foil Accumulator specifications

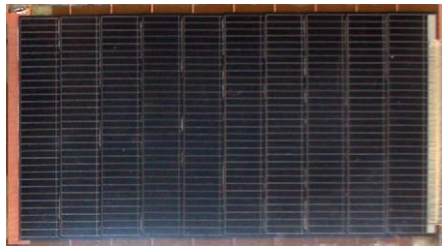


Figure 2.7: Fraunhofer ISE solarcell, used with the TinyMote (see 2.1.7)

2.1.4.2 Solar Cells

Solar cells (figure 2.7 shows a cell used in the TinyMote node, produced from the Fraunhofer ISE [RHEW04]) are interesting yet difficult to commercialize because of their high production costs and relatively low energy efficiency. Nonetheless these are used in many applications where power consumption is not so high that batteries are required, like portable calculators. From the wireless sensor point of view, a node equipped with a solar cell for energy scavenging needs some sort of energy storage for the time where no light is present. Circuits to transform and store this energy will be presented later.

As a commercial example IXYS' [19] Solar Cells will be analyzed. The IXOLAR solar cells are IXYS' monocrystalline, high efficiency products that incorporate an advanced light trapping surface. There are various cell sizes available and are targeted for charging battery powered products, such as mobile phones, cameras, PDAs, MP3 players and toys. Thanks to their typical efficiency of 17%, these cells have good energy scavenging capability even in low light condition, making them also suitable for industrial applications, wireless sensors networks, instrumentation and for charging backup batteries.

The electrical characteristics (as found in [19]) of these solar cells are resumed in the following list:

- Open circuit voltage: 630 mV
- Short circuit current density: 35 mA/cm²
- Voltage at max. power point: 505 mV
- Current density at max. power point: 32.5 mA/cm²
- Maximum peak power: 16.6 mW/cm²
- Fill factor > 75%
- Efficiency 17 %
- Open circuit voltage temp. coefficient: -2.1 mV/K
- Short circuit current temp. coefficient: 0.12 mA/(cm²K)
- Cell thickness: 250 μm

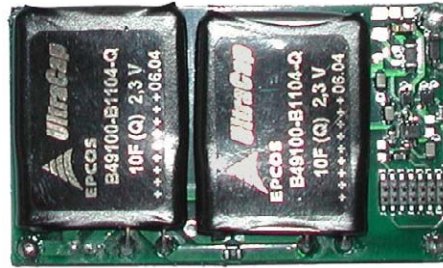


Figure 2.8: Epcos UltraCaps, used with the TinyMote (see 2.1.7)

2.1.4.3 Ultracaps

An UltraCap (as shown in figure 2.8 and presented in [BMP04]) is an electrochemical capacitor consisting of two carbon electrodes separated by a foil and immersed into an electrolyte. The high energy capacity of UltraCaps (in the kFrange) in comparison to electrolytic capacitors originates in the electrodes' material, which has an extremely high specific surface area of about $2000 \frac{m^2}{g}$ and the extremely short distance in the range of 2 – 5 nm between the opposite plates of the capacitor. A capacitance of some thousand Farads is realized in small devices since the dielectric is extremely thin. UltraCaps store charge relying on an electrostatic effect, that is per nature highly reversible, much better than batteries.

Although the UltraCap offers high capacity, their maximum voltage is very limited (the capacitors on figure 2.8 are rated at 2.3V) and still on this voltages the leakage currents are in the 10 – 20 μA range that is way too much for a sensor node power supply. The leakage depends on the voltage so an easy solution is to connect two UltraCaps in series although this halves the total capacity and doubles the cost.

2.1.4.4 Other energy scavenging sources

Another way of supplying wireless sensor nodes is the use of Micro Electromechanical Systems (MEMS) devices (such as in [MMMA⁺01]) that convert mechanical or thermal energy in electrical energy [14]. The most typical scavengers use vibration energy to be transformed in electricity by piezoelectric effect. Other scavengers are targeted at transforming rotational energy in electric energy. With all these devices the main problem is the actual efficiency and the interface to the power supply that is indeed an interesting research topic.

2.1.5 Power management

Power management is of course fundamental to the supply of the different devices that are found in a sensor node. This power management is realized by the MCU that controls the power state of all other devices (as presented in [SC01]), but also from the power conditioning devices that transform energy from one level to another. There are typically two ways to adapt the voltage level coming from the battery or from other sources: a Low Drop Output voltage regulator (LDO) and a switching supply. The LDO circuit uses a feedback loop to control a variable resistor (see figure 2.9). The resistor connects the input voltage to the output and dissipates the power for lowering the voltage. LDOs can only reduce the input voltages and are therefore not always preferred because of their high dissipation and therefore comparatively low efficiency.

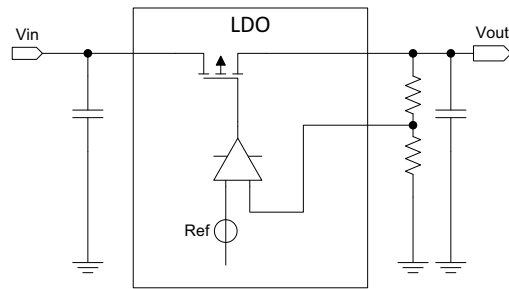


Figure 2.9: LDO power supply

The TPS780 from TI is a LDO regulator that offers the benefits of ultra-low quiescent current (500 nA), small footprint and selectable dual-level output voltage levels. Its main features are resumed here from the datasheet [28]:

- Low quiescent current: 500 nA
- 150 mA, low dropout regulator with pin-selectable dual voltage level output
- Low dropout: 200 mV at 150 mA
- 3% accuracy over load/line/temperature
- Adjustable version from 1.22 V to 5.25 V or a dual-level output
- Vset pin toggles output voltage between two factory-programmed voltage levels
- Stable with a 1.0 μ F ceramic capacitor
- Thermal shutdown and overcurrent protection
- CMOS logic level-compatible enable pin
- Dimensions: 2 mm · 2 mm

Switching power supplies rely on a completely different concept as LDOs. This sort of power supply stores the energy in a passive component like a capacitor or an inductance. The name comes from the main non linear component which is the switch. This is used to transfer energy from the storage to the load in such way that the voltage or current match the chosen values. The important feature of switching power supplies is that they do not use dissipative components such as resistors and therefore reach high efficiencies (even over 90%). Another important feature is the load voltage: it can be generated from higher or lower input voltages.

The LTC3531 from Linear is a synchronous buck-boost switching converter that operates at above, below or equal input to the output voltage. The converters operate in a proprietary mode that reduces component count as well as providing high efficiency. The main features of this low-power DC-DC converter are resumed here:

- Regulated output with input above, below or equal to the output
- Single inductor

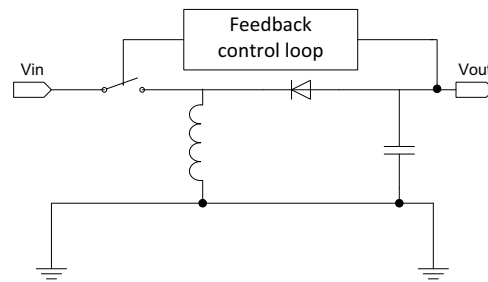


Figure 2.10: Switching power supply

- Up to 90% efficiency
- V_{in} range: 1.8V to 5.5V
- 200mA at 3.3V V_{out} from 3.6V input
- 125mA at 3V V_{out} from 2.5V input
- Ultra low quiescent current: 16 μ A, shutdown current < 1 μ A
- Only 3 external components required
- Short-circuit protection
- Output disconnect in shutdown
- 3 mm · 3 mm DFN packages

2.1.6 Antennas

Antennas play an important role in all wireless application because they are responsible for the transmission of the electrical waves over the air. Without going into too much in detail, this section wants will to give a short overview on the possibility of using a an on-chip integrated antenna, a PCB antenna and a stand-alone antenna.

The use of on-chip antennas is not yet commercially available as it is a difficult task to implement an antenna with enough radiation capacity. This technique is yet interesting and promising for its costs and dimensions, but considering that IC technologies change frequently, it could be a challenging task to redesign the antenna.

Designing a PCB antenna involves a lot of design effort if the antenna needs to be designed from scratch, but if a design is already available, the antenna can be manufactured at negligible PCB production costs. This happens because in the 2.4 GHz band the dimensions of the antennas are in the cmrange. This solution is adopted by many Bluetooth and WLAN adapters and becomes interesting also for sensor networks located in the same band. Figure 2.11 shows the PCB antenna from the TinyMote (section 2.1.7) sensor node.

Other interesting antenna implementations are represented by chip antenna. These are disguised in small Surface Mounted Device (SMD) devices resembling resistors. These are antenna elements embedded in a ceramic substrate, which is extremely stable on temperature changes over the time.

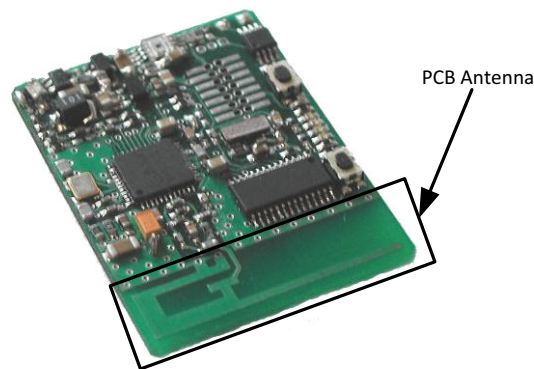


Figure 2.11: PCB antenna example

The small dimensions enable the high frequency range for these antennas and also allow for high integration on the PCB.

The CHP Series from Linx Technologies is an attractive high-performance chip antenna as its features show:

- Cost-effectiveness
- Compact SMD package
- Ceramic technology
- Low loss
- Wide bandwidth
- 50-ohm characteristic impedance
- Linear polarization
- No external matching required
- Highly stable over temperature and time
- Fully hand- and reflow-assembly compatible

2.1.7 The TinyMote, an example sensor node

The TinyMote is sensor node developed at the Institute of Computer Technology of the Vienna university of technology. It is in many ways the predecessor to this dissertation. The TinyMote is an ultra low power sensor node for multi-hop peer to peer wireless sensor networks. Its main features are resumed in this section.

The wireless interface is of course of main importance and is defined as follows:

- 2400 MHz, 79 frequencies of 1 MHz
- Data rate: 10,250,1000 $\frac{kbit}{s}$

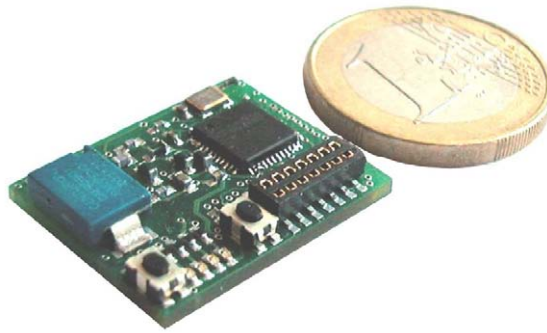


Figure 2.12: The TinyMote sensor node

- RF wakeup time around 1 ms
- Antenna on board
- Ultra low quiescent current voltage regulator ($< 2 \mu\text{A}$)

The microcontroller on board is a model of the TI MSP430 family described in section 2.1.1:

- Model MSP430F1232
- 16Bit RISC-CPU, On-Chip Osc. 4 MHz Max
- JTAG interface at connector
- Real-time clock
- 8 KBytes flash
- 256 bytes ram

The node is equipped with a temperature sensor with $\pm 0.5^\circ\text{C}$ precision and optionally mountable analog sensor that can be sampled with 10 Bit resolution by the onboard ADC, e.g. a brightness sensor with samples in the 10-10000 LUX range. The printed circuit board has two buttons and four signalization LEDs and connects to an external serial port for debug purposes. The node is realized in two versions, one needing 24 x 19 mm with double sided component placement and one with 30 x 24 mm using single sided component placement. The standby current consumption of the entire node is measured to the following values (RTC is active):

- $< 700 \text{ nA}$ at 2 V (RF-Chip turned off)
- $< 3.7 \text{ nA}$ at 2 V (RF-Chip in power down)

The hop-to-hop maximum delay of < 2 second results from the use of the CSMA-MPS protocol [MB04] at a wakeup period of 2 seconds, giving an average hop delay 300ms The average power consumption in the a typical environment (one packet received and transmitted each 5 seconds) is about $100 \mu\text{W}$ that should result in almost 9 years of operation with a lithium battery of 3200 mAh.

2.2 Wakeup Receivers and Protocols

General architectures of receivers (as shown in figure 2.13) are chosen as starting points to develop new types of receivers, as their features and drawback are well known and analyzed into depth. Focus is then put on optimization of the power consumption. This task is not trivial and of utmost importance for receivers targeted at utilization in WSNs. Sampling directly at RF frequency is by no means a low power technique; therefore the RF band is usually shifted to baseband by the receiver's front-end.

The super-heterodyne architecture [Arm24] (figure 2.13a shows a dual conversion type) is a typical frequency conversion receiver for multi channel reception. After some gain from a Low Noise Amplifier (LNA), the useful RF signal band is shifted by a mixer to an intermediate frequency after being filtered for a broad range that includes all channels. At intermediate frequency, the channels can be selected by a tuneable filter followed by mixing the signal to baseband with a tuneable oscillator. This double conversion eases the noise requirements on the signal path.

The direct conversion receiver (figure 2.13b) uses quadrature down conversion to demodulate two baseband (I and Q) signals. This receiver needs a highly spectral purity oscillator and a precise 90° phase shifting to accurately separate the two components. The mixers and oscillator

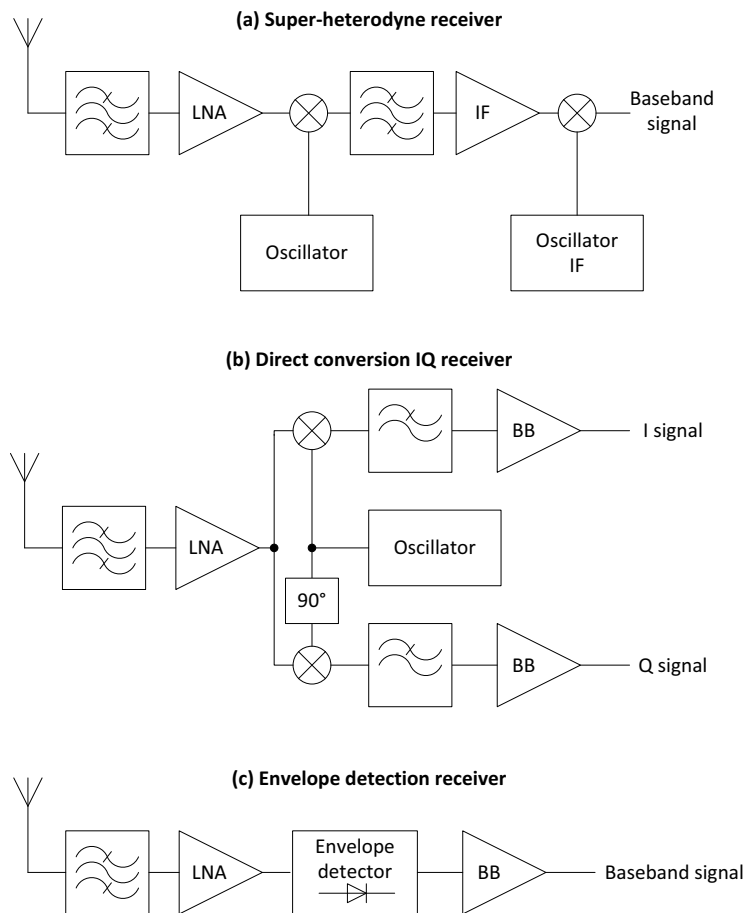


Figure 2.13: Popular receiver architectures

are indeed high power consuming, but this architecture achieves high performance, particularly sensitivity and transfer rates and is used e.g. for satellite communications or telephone cellular networks.

As the main focus in WSNs is put on low power consumption, conversion architectures are not good candidates because of their need for high frequency oscillators and mixers, which are power hungry components of such designs. A much simpler architecture (figure 2.13c) uses the well known rectification to demodulated information contained in the envelope of the carrier signal, such as in the standard AM receivers, which were realized at first completely passive. This technique is used e.g. in RFID tags and uses less components than the other two architectures and is therefore chosen for many implementations of wakeup receivers because of promising power saving features.

The most significant implementations of wakeup receivers are presented here. All the efforts in optimizing the proposed receiver architectures are directed to realize acceptable sensitivity, robustness and data rate for a particular power consumption goal. This objective comes from the fact that no great enhancements are possible in battery technology such that maintaining a node active for years is possible at low cost and space. Therefore each publication tends to reduce at most the consumption of the radio transceiver, as it is shown that it is the most power hungry component of the sensor node.

In [LSGR01], the first concept of wakeup receiver as resource to reduce power consumption extending node's life can be found. The goal of the Pico Radio (figure 2.14 shows a Pico Node architecture) project referenced in this publication is to realize a node that consumes $100\ \mu\text{W}$ enclosed in $1\ \text{cm}^3$ space. To realize this intent optimization both between the layers of the protocol stack and between nodes is considered. At this power consumption however, considering high volumetric energy density (such as Li-ion batteries) is the projected life under 200 days. So the power consumption budget must be reduced if node life (and network life) of several years is required. The MAC protocol proposed is an extension of Carrier Sense Multiple Access (CSMA) into multi-channel CSMA. A channel for communication is chosen randomly and sensed for a present carrier. If busy, the channel is rejected and another between the remaining is chosen for

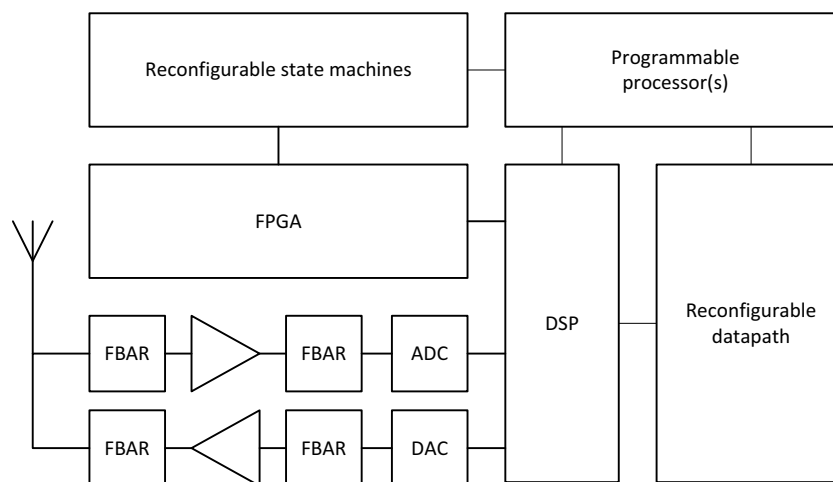


Figure 2.14: Pico Node from [LSGR01]

the same procedure until one free channel is found, otherwise the node backs off for a random time for each channel and begins the search again for those of which the timer has expired.

The algorithm is fully distributed as there is no higher hierarchy entity that controls it. No synchronization is needed as each communication is asynchronous because this means less power, which is the strong point of this publication. If no synchronization is required then no power is wasted for it and no power for handshaking is needed. To suppress the need for synchronization and handshaking, this paper envisions a wakeup radio that consumes less than 1 μ W when fully active in receive modus. Most of the time the node is in sleep mode with all components in power down so that ultra low power consumption can be achieved. The wakeup radio is the only active device in the node besides power supply. This is needed because state of the art radios consume in the mW range. The task of the wakeup radio is to activate the main radio when the node is selected for reception, as its address is modulated in the wakeup signal.

In this way, the main radio does not spend energy when it is not needed, allowing power consumption to sink to low levels. Such a low power consumption for the wakeup radio is realizable at the moment only if high RF transmitted power is available, which in turn drains the battery of the transmitter, thus rising the overall power consumption. Another problem in the realization of the wakeup radio lies in the channel selection, which cannot be realized passively. The transmitter has to sense the channel and therefore has to turn on the main radio wasting energy. The advantage of such a setup is that there aren't any delays in the transmission and the use of multiple channels raises the throughput. Although there are some obstacles to the realization, this approach is simple and robust because of its lack of scheduling or synchronization.

An interesting hybrid low power "rendezvous" protocol is presented in [NT02]. This publication studies the use of Radio Frequency Identification (RFID) technology (as in [NBJW07]) in sensor networks using base stations to coordinate the communication and the wakeup process reckoning that WSNs need high responsiveness, which is not possible using traditional scheduling "rendezvous" schemes if ultra low power consumption is required. The RFID technology is chosen because of its low power consumption compared to typical commercial radios. WSNs are generally divided in two main categories: the first, referred as "passive", does not have its own energy source and is activated by the electromagnetic field of the transmitter. This energy is stored (with low efficiency) and used to power the circuit and eventually transmit data back. The second category is referred to as "active" and is usually battery operated. The ranges for these two categories differ greatly as passive RFIDs have a maximum operating distance of around one meter. Long range RFIDs have the great drawback that data rate is reduced to few $\frac{bit}{s}$ which is unacceptable for most WSN applications.

The proposed idea is to use the RFID downlink channel for signalling the wakeup event and activate the sensor node. The first assumption is that there is a single base station that serves the communication to sensor nodes within communication range. The sensor nodes are battery operated and lie in a radius of ten meters. Three different protocols are evaluated and simulated to estimate the power consumption. The first protocol is a typical scheduling technique that requires to nodes to be synchronized and exchanges data only at the predefined meeting time. This protocol is able to reduce power consumption virtually to zero provided the periodic exchange happens seldom.

The drawback in this technique is that the responsiveness is directly proportional to power consumption, meaning that high responsiveness results inevitably in high power consumption. The second technique is purely wakeup dependent using an RFID radio in addition to the normal

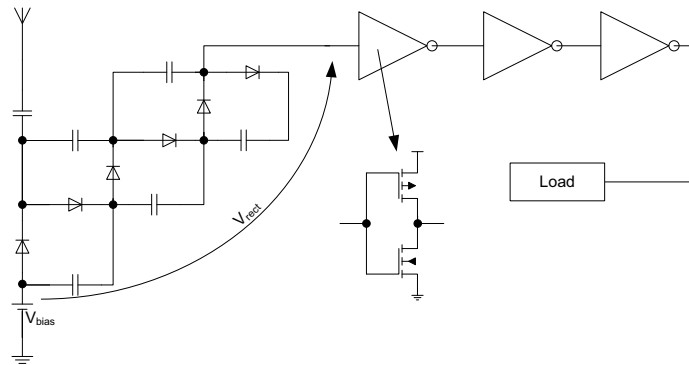


Figure 2.15: RF detector from [MB07]

radio transceiver. Data exchange is initiated from the base station with special pre-wakeup packets that announce all the active nodes that starting a communication is forbidden to prevent collisions. A wakeup packet is sent on the RFID channel and the destination node activates the main radio. The modulation chosen for the wakeup channel is Amplitude Shift Keying (ASK), as in all RFID solutions because of its easy demodulation. In particular, On-Off-Keying (OOK) is used and the protocol adds a bit with value 1 each two data bit to prevent long zero sequences of bits in the channel. Additional strategies to prevent collisions are introduced using both the main and wakeup radio.

The result of the comparison that is found in chapter 3 of the scheduling protocol and the wakeup protocol represents the well known features and drawbacks of both strategies. The scheduling protocol consumes less if the period is made long and has better responsiveness if the period is short. The wakeup protocol on the other hand consumes less by small traffic without affecting the responsiveness, but does not achieve as high data throughput as scheduling protocols because of the wakeup overhead. To overcome the negative sides of these protocols, the authors propose a mixed form of wakeup and scheduling protocol. The idea is to use the scheduled wakeup times to transfer data from the nodes to the base station and the wakeup signals to raise the responsiveness between base station and sensor node. The overall responsiveness is better than in the case of pure scheduling, but power consumption is somewhere depending on the period of the schedule. If the base station does not need data from the sensor, it uses the schedule to synchronize the nodes, always using the RFID channel. The only reason to use such a mixed operation mode would be in the case the RFID radio has relatively high power consumption, such that the full wakeup operation mode is not possible, thus this operation should be considered a trade-off solution between power consumption and enhanced responsiveness, with the necessity of many coordination efforts.

In [MKHB05] an interesting concept for a complete wakeup receiver is presented based on the RF detector presented in [MB07]. The detector shown in figure is based on the use of cascaded rectifiers that build up the envelope of the incoming signal. The rectifier, shown in figure 2.15, is proposed to be realized with zero-bias Schottky diodes. As stated in the paper, the diodes need high saturation current I_s to load the capacitors with low RF input voltages. The other two parameters that influence the rectification are the junction capacitance C_j and series resistance R_s . The junction capacitance is of great importance to achieve good performance and must be reduced as much as possible, otherwise attenuating the RF voltage resulting in less rectified voltage. Series resistance in turn not an issue as currents are low enough.

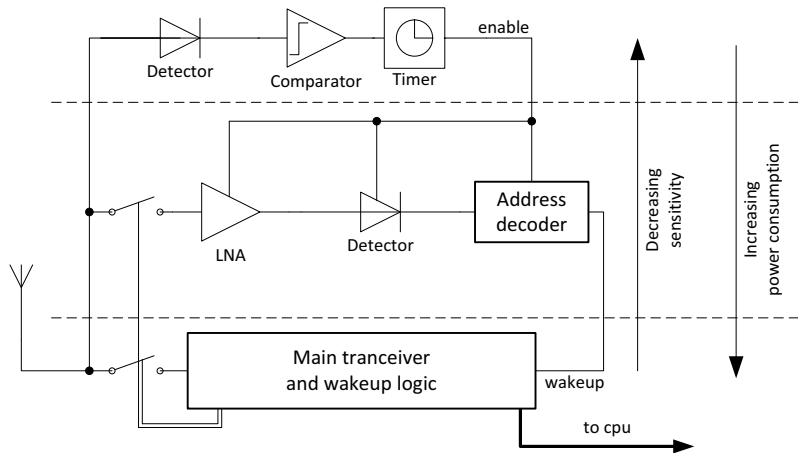


Figure 2.16: Three stage wakeup receiver from [MKHB05]

These three factors are the design parameters and influence directly the performance of the rectifier. The saturation current and the junction capacitance increase with the width of the diode, therefore a trade-off must be found so that performance is maximized for the given technology. It must be said that not each CMOS technology implements the Schottky diode, which is a metal-semiconductor junction; therefore a wakeup receiver with such a detector must be built in an appropriate technology (e.g. BiCMOS) or off chip, which could lead in each case to an increase in the production costs.

The proposed detector is followed by a comparator realized with an inverter chain. The rectifier is biased such that the output voltage, when no signal is present at the input, is little below the switching threshold of the first inverter. The sensitivity of this circuit lies in the voltage difference between the bias voltage and the inverter's threshold voltage which in turn is not desirable as this is different between wafer and even between chips of the same wafer. This would also create the need to compensate for this uncertainty with the use of negative feedback, which would result in increased power consumption. Another drawback of this design is that the inverter chain is always biased near the switching threshold, which also means increased power consumption because CMOS inverters connect the power supply with ground through both P and N transistors.

The complete wakeup receiver for OOK (figure 2.16) presented in [MKHB05] is based on the detector presented in [MB07]. The main idea is to divide the complete receiver in three hierarchical units. The first hierarchical unit is composed by the Schottky RF detector, the comparator and a timer. This first stage acts simply as a simple power detector for the chosen transmission band. It must be activated by a high power burst because of its low sensitivity. The time sequence to activate all three stages is shown in figure 2.17. This stage does not have the capability of decoding any type of information from the incoming signals and therefore is proposed to consume in the nW range.

The second stage is activated if the burst that initializes the comparator in the first stage lasts long enough. This stage has an LNA that is connected directly to the antenna through a switch. When the first stage detects the burst, the input switch is closed so that the LNA can amplify the signal from the antenna. At this point the OOK signal is transformed to baseband using

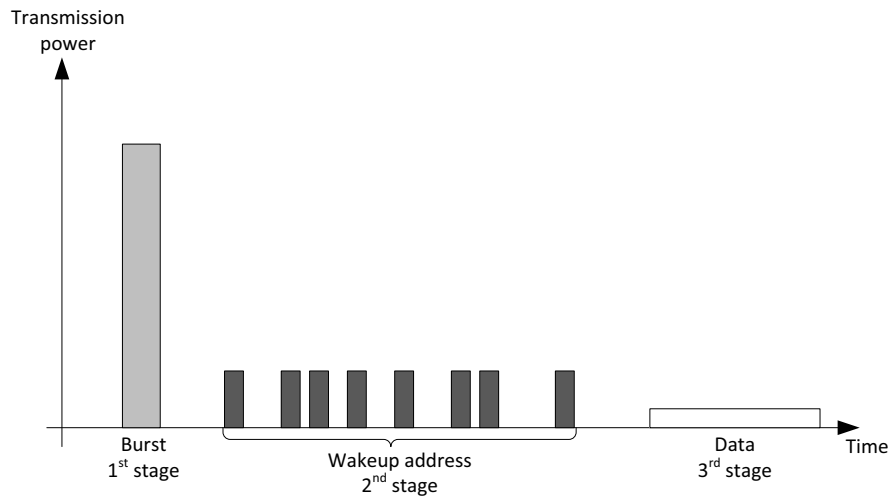


Figure 2.17: Wakeup signals for the three stage wakeup receiver from [MKHB05]

again a detector. The sensibility is higher because of the LNA. An additional logic decodes the address that is contained in the signal for the second stage. If the address matches, then the main transceiver is activated and communication can occur.

A thorough analysis of the three stage concept reveals some drawbacks in the design and in the circuits. The first stage has a comparator which is the key for the sensitivity of the system. The proposed architecture is an inverter chain which input is biased a little below the switching threshold. One problem with this choice is that the switching threshold cannot be precisely designed to be within a reasonably small range because of process tolerances, but this is important to control sensitivity. A variation of some millivolts could provoke a dramatic change in the sensitivity, and the threshold depends also on the temperature. The other problem is that a CMOS inverter draws at its threshold quite some current because both transistors connect the supply voltage to ground. This is normally no problem if the signal driving the inverter is fast enough. In this application the signal coming from the detector is not so fast and the sensitivity is proposed to be as high as possible, thus placing the bias voltage near to the switching voltage. The current at threshold is estimated to be around 10 mA which of course is high. Given that the bias of the detector will be set near to the switching threshold to raise the sensitivity of the first stage, it is very likely that the comparator triggers a lot of false alarms that will indeed waste a lot of energy.

As no input filter is considered in the design, it is assumed that the antenna will filter the incoming signals to the complete band of the main transceiver, which could be the 2.4 GHz ISM band, which is 100 MHz wide. The circuit would then detect each communication in the band and therefore reduce the sensitivity of the first stage because the bias would have to be set farther from the switching threshold. To trigger the complete first stage a high power burst has to be generated from the transmitter for a comparatively long time. The receiver does not consume more energy because of this, but to optimize the power consumption of the sensor nodes both roles must be taken into account. As normal applications consider some nodes to be in near range, a burst would trigger all the nodes within distance although only one node is intended for communication. This would also raise the average power consumption because most of the time nodes are woken up unintentionally.

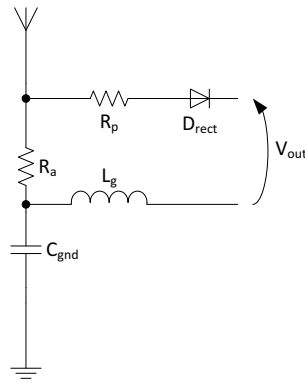


Figure 2.18: Wakeup trigger from [GS04]

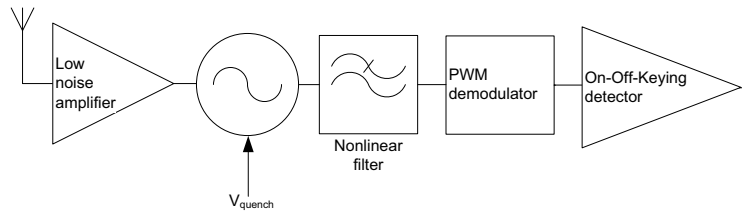


Figure 2.19: Receiver architecture from [OCR05]

The second stage is by design more power hungry as it must be able to detect an incoming packet with the destination's address of sensor nodes. The architecture proposed is again a detector, although driven by an LNA. This increases the sensitivity by the gain of the LNA at the cost of the comparatively high power consumption of the LNA. If there are a lot of false alarms triggered by the first stage, the second stage wastes a lot of precious energy because no address is being transmitted. The choice of having a detector after the LNA is to keep consumption under control but in turn does not allow the sensitivity to increase too much. For an address decoding a correlation receiver is proposed which must detect a PWM code. A long sequence is necessary to reduce the amount of false alarms that reach the third stage of the radio that is the main transceiver, which consumes more than the second stage.

The final power consumption of this three stage concept is bound to many factors, most of which are not circuit dependent. The energy needed increases if the average traffic of the network increases because wakeup become more and more frequent. In-band noise and interference is also a source of false alarms and therefore of energy waste. This connection between power consumption and average traffic and interference must be avoided if real ultra-low power consumption is to be reached.

A purely analytical implementation of radio triggered wakeup for wireless sensor networks is proposed in [GS04]. The paper studies the impact of a simple radio-triggered wakeup capability compared to timer-based protocols. The proposed circuit is a theoretically realizable diode rectifier that has the duty to collect energy from the radio signals and trigger the node if the signals are detected as valid. The system is considered to have two completely different antenna and signalling bands for data and wakeup, which can ease the requirements on the wakeup trigger if the data channel is load with high traffic. The simple wakeup circuit is shown in figure 2.18.

The proposed circuit is only representative of the real function that the radio-triggered circuit should comply, as it is too simplified to work. The diode alone as non linearity source is considered to be ideal (though with some dependence on its forward voltage) which of course is not the case. The diode is actually the key-element to this simple design as it converts Radio Frequency (RF) energy to DC and this is where all the engineering is needed. On the other side, the publication gives the right weight to the antenna as it is surely also an important element in the receiver chain.

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi D)^2} \quad (2.1)$$

Equation 2.1 explains the received power P_r depending on transmission power P_t , transmission antenna gain G_t , reception antenna gain G_r and distance D . The gains are considered as key factor to the radio triggered circuit, but it is also stated that the gains are limited on the upper side, meaning that physical dimension are an obstacle to the realization and commercialization. The proposed circuit, with the proposed parameters should deliver 0.6 V as output if a carrier is present on the wakeup channel. As it is stated in the paper, this voltage is today not problematic for modern digital circuits to be handled as interrupt. The potential power saving is then evaluated thanks to SPICE simulations showing that the radio-triggered version of the node lasts up to 4 times longer as the schedule-based equivalent. Some other circuits are evaluated then also with SPICE. These improve the distance for which operation is possible by proposing the use of transformers and amplifiers.

The ability to realize such a simple radio trigger is very limited because of many engineering factors and simplifications done. First of all, the diode is the main weak spot as its integration is complex and the forward voltage (i.e. the nonlinearity) cannot be chosen at will. This means that the transmitting node must send enough energy to activate the diode. In the calculated case, the node survives 178 days by 10 wakeups per day, which is obviously not a very high traffic. The radio-triggered circuit does not distinguish on the very first phase if the trigger is aimed at itself; therefore all nodes in the range of the transmitter will wake up and use precious energy going back to sleep after having rejected the incoming packet. The robustness of this simple radio trigger is not high enough as such a circuit cannot differentiate between noise, wakeup signal or disturbance from other transmissions.

A 400 μ W super-regenerative transceiver is presented in [OCR05]. The architecture is simple yet efficient. The radio is able to receive and transmit OOK at 1.9GHz. The power consumption during transmission is 1.6mW. The architecture is presented in figure 2.19. The LNA is an inductive degenerated PMOS topology with two on-chip inductors. The amplified input signal is then mixed down directly to baseband and sampled. The detector has a lot of gain (55 dB) and therefore a very high measured sensitivity of -100.5 dBm at $5 \frac{kBit}{s}$. Although the results appear very interesting, the power consumption still remains very high for a wireless sensor node if this receiver has to be used as wakeup receiver. It would be interesting if some of the sensitivity could be traded for power consumption, as a sensitivity of -80 dBm would still be enough for a wakeup receiver, although higher data rates would also certainly be an advantage. As main radio this proposal would fit very well to the overall concept of wireless sensor node.

In [KL07] an implementation of a passive RF front-end to be used as a wakeup radio is presented. The proposed front-end is shown in figure 2.20 and eliminates completely active RF components. Some techniques are then analyzed that should minimize the disadvantages of this

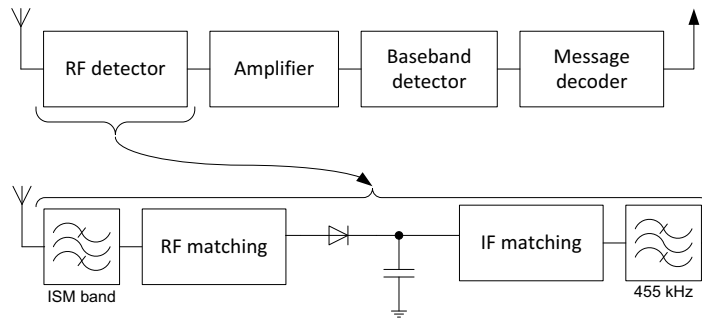


Figure 2.20: Receiver architecture from [KL07]

approach. The proposed receiver operates in the 915 MHz Industrial Scientific Medical (ISM) band where transmission power up to +30 dBm is allowed provided some sort of spread spectrum modulation is employed distributing the power over 500 kHz bandwidth. The detector uses the square-law rectification effect of a diode to demodulate the incoming signals, being insensitive to small frequency jitters on the input signal. If the down-converted signal is filtered appropriately all out of band signals are suppressed and do not raise the overall noise level of the receiver. All the noise that falls in the allowed input range is rectified and raises the required input Signal to Noise Ratio (SNR) of the receiver.

The chosen wakeup signal is an amplitude modulated RF carried, which demodulated signal is a sine at 455 kHz. This is used to filter very specifically the desired signals from interference and to raise the overall sensitivity of the receiver. The article evaluates the link budget for such architecture and evaluates the path loss in a typical WSN indoor environment. Simulated and measured results show that the lowest detectable level lies around -69 dBm although at very low SNR. This proposal uses transmit powers between +20 dBm and +30 dBm, which are indeed very high for sensor nodes, and allow relaxing the sensitivity requirements of the detector, but raise the mean power consumption if network traffic is sustained.

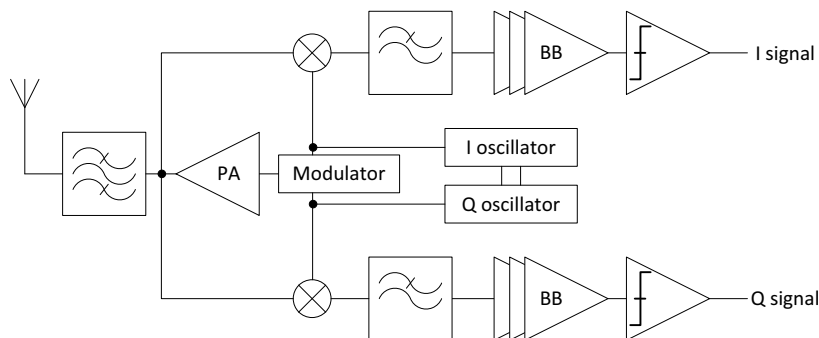


Figure 2.21: Transceiver architecture from [CBM⁺06]

In [CBM⁺06] a complete binary Frequency-Shift-Keying (FSK) transceiver is presented. A block diagram is shown in figure 2.21. The chosen architecture for this transceiver is the direct conversion IQ demodulation, which offers good robustness and efficient band utilization because of the frequency modulation, rather than the usual choice of amplitude modulation. The antenna

matching is realized completely on-chip by the means of LC network. The use of integrated inductors results in low Q, rendering a wider FSK tone separation necessary. This sacrifices spectral efficiency but allows reduction of power consumption. The input mixers are implemented by passive mixers and therefore reduce power consumption in one of the weak spots in FSK designs. The input mixers can be utilized as power amplifiers as well, reducing the additional load to the antenna, which also helps consuming less. It is not clear what sensitivity the receiver is capable to support, although this figure is of main importance. This can be explained by the fact that this implementation includes only the front-end receiver and additional logic is needed to extract information from the incoming signals. Nonetheless, given the architecture, it can be assumed that high sensitivity such can be achieved. The consumption of the Voltage Controlled Oscillator (VCO) is comparable to the total consumption of the receiver as table 2.6 shows. Even if the presented architecture is realized and achieves low power consumption, it cannot be used to realize a wakeup radio, which of course does not mean that such a radio would not fit the role of main-transceiver well.

Supply voltage	400 mV
RX power consumption	200 – 750 μ W
RX noise figure	5.1 – 11.8 dB
Binary FSK deviation	300 – 1000 kHz
VCO power consumption	160 – 700 μ W
VCO frequency	1.95 – 2.38 GHz
VCO phase noise (1 MHz)	$-106 \frac{\text{dBC}}{\text{Hz}}$
TX power consumption	700 – 1120 μ W
TX output power	140 – 320 μ W
TX efficiency	> 44%

Table 2.6: Performance from [CBM⁺06]

The two following implementations of Wakeup Receivers are architectures that are below their maximum power consumption budget of 100 μ W and are specifically targeted at building nodes of a wireless sensor network. The budget for this work has been set much lower (10 μ W) keeping in mind that with standard energy supply storage medium life of several years can be achieved. Nonetheless these are the only implementations of Wakeup Receiver front-ends integrated on-chip and published to date and will be presented here.

The first proposed architecture can be found in [PGR07] and consumes 65 μ W achieving a sensitivity of -56 dBm. The sensitivity is computed using an atypical metric to define this value. Usually the sensitivity is the power for which 10^{-3} Bit Error Ratio (BER) is measured, but in this publication the sensitivity is characterized by two parameters: probability of detection and false alarm rate. The threshold of the probability of detection was set at 90% and the false alarm rate at 1 per second. The probability of detection is calculated by using a 31 bit long sequence and the false alarm rate is set considering an average traffic several packets per second. With these figures the sensitivity of -56 dBm is measured although the authors state that at a typical baseband SNR of 12 dB the sensitivity is -50 dBm in the worst case.

The architecture of this Wakeup Receiver (WUR) is shown in figure 2.22 and implements an OOK receiver. The first stage is a tuned RF filter, realized with a passive Bulk Acoustic Wave (BAW) resonator. This type of filters has a very high quality factor and very narrow bandwidth. The filtered input signal is then amplified by 18 dB with a noise figure of 9.2 dB from the RF amplifier trading higher noise for lower power consumption. The envelope detector down converts the RF signal directly to baseband, which is then amplified with variable gain and fed to a 6 bit

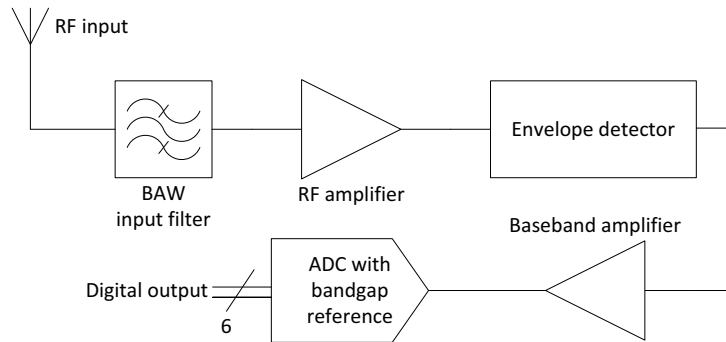


Figure 2.22: Block diagram of the WUR from [PGR07]

ADC. The detection of the wakeup signal has to be done in the digital domain and is estimated to consume only $5 \mu\text{W}$ using a simple correlation bank.

The receiver is realized in standard CMOS 90 nm technology, works with a supply voltage of 0.5 V and consumes $65 \mu\text{W}$. The power consumptions for each single building block are reported in table 2.7. The architecture proposed uses nearly 74% of the power for the RF amplifier alone, which could be saved by improving the efficiency of the envelope detector. Without RF amplifier the sensitivity would sink to -32 dBm , which is unacceptable, reducing the maximum range of communication below 1 m considering a transmitted power of 0 dBm. The choice of digitalization with a 6 bit ADC is also questionable, due to high power consumption of the necessary bandgap reference ($10 \mu\text{W}$). The decoding logic is implemented by a correlation bank which was implemented in Matlab [22] but it is not clear if an implementation of long shift registers and correlation banks with a 6 bit width could be realized with the estimated power consumption in the given technology.

The second proposed architecture can be found in [PGR08] and is a somewhat uncommon approach for an envelope detector receiver. This implementation achieves a much better sensitivity figure. The proposed idea is shown in figure 2.23 and is a mixture between a diode detector receiver and a heterodyne receiver. The input signal is down mixed to an intermediate frequency and then the envelope detector demodulates to baseband. This results in a much lower maximum frequency to be rectified. The local oscillator does not need to be very precise if the envelope detector can rectify the intermediate frequency within the jitter range. Local oscillators trade power consumption for precision and usually a precise frequency is realized with a Phased Locked Loop (PLL), but this not possible with such a tight power budget. As local oscillator, a simple and tuneable ring oscillator is chosen. The ring oscillator is a ring of inverters in which delays can be controlled by a voltage. The inverting nature of the ring does not let the system reach a stable

<i>Block</i>	<i>Power Consumption</i>
RF amplifier	$48 \mu\text{W}$
Envelope Detector	$1 \mu\text{W}$
Baseband amplifier	$2.5 \mu\text{W}$
ADC	$13.8 \mu\text{W}$
Total	$65 \mu\text{W}$

Table 2.7: Power consumption of the WUR from [PGR07]

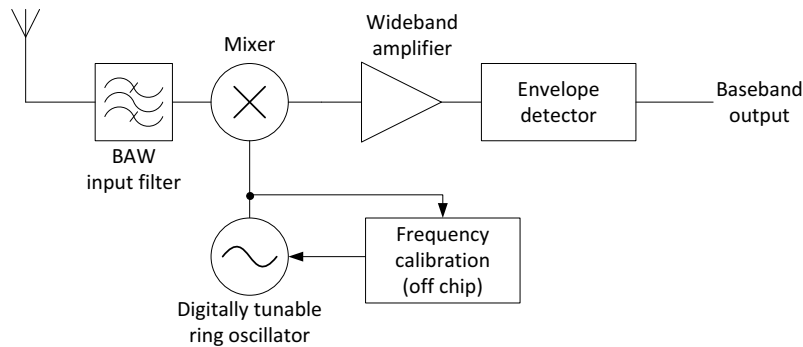


Figure 2.23: Block diagram of the WUR from [PGR08]

balance and the frequency is directly dependent on the delay of each gate. The delay can be controlled by changing the maximum current available to each gate and therefore the frequency can be easily regulated. After calibration the ring oscillates at a given frequency if temperature does not change. The tuning range for the local oscillator is specified between 1.9 and 2.1 GHz so that the image signal appears in the frequency range of the wideband amplifier that is between 1 and 100 MHz for a 2 GHz input signal. The image signal is down converted to baseband by the envelope detector. The power consumption of the building blocks of this receiver is presented in table 2.8. The mixer has a high conversion gain (+15 dB simulated) and proportionally low power consumption. The most power is consumed by the tuneable oscillator and by the wideband amplifier. The receiver consumes 52 μW in total and has a sensitivity of -72 dBm for 10^{-3} BER. Calibration should be performed infrequently with low power consumption although this is application dependent. The detection algorithm is not included in the power budget and no investigation on this part of the receiver is done in the article.

<i>Block</i>	<i>Power Consumption</i>
Digitally tunable ring oscillator	20 μW
Mixer	8 μW
Wideband amplifier	22 μW
Envelope Detector	2 μW
Total	52 μW

Table 2.8: Power consumption of the WUR from [PGR08]

Both these implementations of receiver front-ends are interesting attempts to realize a wakeup receiver. The goal power consumption should lie one decade lower than the allowed budget of 100 μW and the sensitivity should be in the range of the intermediate frequency architecture, although better performance would let the concept of wakeup receiver fade to that of main transceiver.

3 Proposed Solution

Instead of using complicated protocols to synchronize the operation of the radio in sensor networks nodes, the proposed system architecture, spanning over the first two layers of the protocol stack, is capable of reducing both power requirements and latency. The proposed protocol is energy efficient using a Wakeup Receiver (WUR) which basically reduces power used by idle listening to a minimum level and avoids any synchronization of main transmitter and receiver. This results in efficient utilization of the main transceiver that is active only when necessary, i.e. when communication occurs. This mechanism can be seen as a remote control to activate the main transceiver on a remote node. The WUR used a dedicated channel for service communication. This service communication is used to handle the handshake protocol that is needed to share the communication channels and prevent collisions. When the medium is reserved the communication can occur without using the service channel and information data can be exchanged.

This solution addresses the well known problem of idle listening [LSGR01]. Using state of the art receivers in active listening mode consumes just too much energy for a system that has to live years and be contained in some cm^3 ; therefore intelligent strategies are used to synchronize different nodes such as the Medium Access Control (MAC) protocols like CSMA-MPS [MB04]. These have to cope with imperfect clocks and their drift, which prevents ideal function of these scheduling strategies. Moreover the use of time schedule implies a fixed delay in routing packets. This means that for a given hop count (considering a fixed routing) the total delay is in the best case equal to the wakeup period (which is common to all nodes) multiplied by the number of hops. This is unacceptable for many applications and areas where wireless sensor networks could bring great improvements.

The proposed solution is sensor-node application independent and fits well with each wireless sensor network independently of its traffic also because the power consumption tends to the same values of scheduling protocols with very low period, being otherwise much lower. The main advantage of the wakeup receiver concept is the trade-off between system delay and power consumption is broken. Low system delay, that means high channel occupation and throughput, can be achieved without compromising the total life expectation of a node and of the network.

3.1 Solution Development

The solution proposed in the next two sections is developed starting from the state of the art work presented in the previous chapter. The various sources provided in the state of the art

contribute to the architecture of the proposed wakeup receiver in a decisive manner. The first fundamental choice concerns the modulation of the radio signals. State of the art high-speed radio transceivers such as those for Bluetooth (as in [IHA⁺03], [BKL⁺05] and [KSI⁺02]) and for WLAN (see [PDD05], [ZSYHy05] and [TMYMCC07]) use different sorts of frequency modulation, as this allows to obtain a very high sensitivity and high data rates. The advantages of such architectures where frequency modulation is used is that the sensitivity is increased by using very tight filters on the signal and thanks to the mixing process the resulting noise is greatly reduced, thus increasing the overall sensitivity in levels that allow up to 100m range and over. Considering that most wireless sensor networks require a 10m range the requirements on the receiver sensitivity can be loosened. Another reason for which the sensitivity requirements must be set lower is the fact that the receiver architecture is substantially an amplitude modulation receiver. This choice is made because the circuits that demodulate AM signals can be very simple and even completely passive, as in the first radio sets. In this case the simplest modulation possible for a digital receiver is On-Off-Keying (OOK), that associates a bit value to the presence of the carrier and the other value to the absence of the carrier (i.e. to silence).

On-Off-keying modulation requires a simple yet very important first block that is the envelope detector (also called energy detector or rectifier). This first piece of circuit is responsible to convert the Radio Frequency (RF) signal from the antenna into a low frequency signal proportional to the input signal amplitude. This block is very important as it decides of the sensitivity of the receiver. The two factors that influence the sensitivity are the efficiency of the detector and its internal noise. The work presented here discusses the utilization of two different detectors. One detector is composed by Schottky diodes as it is usual for RFID systems (example diodes and circuits can be found in [8] and literature in [BLL06], [SHCW06], [YSJSYC⁺04] and [JM06]). The other detector is realized with MOS transistors because the prototype chip is realized in a 120nm CMOS technology. The reason for this is that a rectifier is a highly non linear circuit that needs as much non linearity as possible to realize the function. In the chosen process the device that shows the highest non linearity is the MOS transistor and therefore it is the clear choice to make. The MOS detector circuit is based on the circuit proposed in [JO04] and shown in figure 4.18. The paper proposes to use the circuit to measure power in RF ICs without loading the transmission lines. This circuit approaches ideal efficiency (the ratio between output DC voltage change and input RF amplitude) of 1 if the applied signals are powerful enough. This concept was transformed from the original amplitude measurement to the demodulation RF signals on the antenna because the output voltage depends from the input amplitude of the RF signal. This brings some problems in the demodulated signal that must be processed, but this will be explained in the next sections. In the case of this work, the detector is optimized to yield maximum efficiency at very low input amplitudes.

As the detector produces signals with very small amplitude, there must be some analog processing before the signal can be fed to the digital processing where information is extracted. If we consider the circuit presented in [GS04] and shown in figure 2.18 (see section 2.2), it could be argued that no processing is needed to achieve the trigger pulse that should wake up the sensor node. That approach is very elementary as it supposes the use of a channel where no other communication occurs. This is not the case if we consider the field of application and the available frequency bands to wireless sensor networks. The 2.4GHz ISM band is normally very crowded and such a circuit would be permanently triggered. The other problem of this approach is the use of an ideal diode as rectification, which cannot be matched in reality. Such circuits has the problem that no addressed wake up is possible, that means that a wakeup call activates all the nodes in the range, where normally only one is intended as destination. All other nodes would the waste

energy to understand that the wakeup call was not intended for them. Given the fact that analog processing is needed, there are some different approaches in the literature as to how this can be done.

The architecture proposed in [MKHB05] tries to raise sensitivity and lower power consumption by dividing the receiver in three decoding stages that are activated sequentially. Each stage has better sensitivity and higher power consumption. The first stage tries to consume very little energy by not being able to decode anything other than a constant carrier wave. This stage is activated in all the nodes reached by enough RF power. The detector that detects the constant tone is realized by a voltage multiplier circuit (see figure 2.15) followed by a chain of inverters biased near to the threshold. This means that if enough RF signal is present at the antenna, the inverters will be activated. This has the big drawback that in this situation the inverters draw a lot of current as both transistors of the inverter are conductive. If the tone lasts a precise timeout, the second stage is activated. At this point, a chain composed by a Low Noise Amplifier (LNA), a detector and an address decoder are activated. The power consumption is not very important here, but the time length of the activation is critical. The use of an LNA is due to the need of increasing the sensitivity of the OOK detector. If the third stage detects a valid address the node is activated for communication. To prevent unnecessary power consumption, the wakeup receiver reduces its architecture to that of the second stage of the receiver because it solves the problem of the sensitivity by using additional analog and digital signal processing.

In [KL07], the detector is more elaborate than as in the other proposed detectors. The receiver defines as activation signal a carrier in the Industrial Scientific Medical (ISM) band modulated by a 500 kHz sine wave. At first the traditional detector demodulates the carrier and generates a sine at 500 kHz. This demodulated sine is filtered by a band pass tuned to its frequency. The chain is then composed by a successive OOK detector which must detect 500 kHz carrier signal which is surely simpler than detecting OOK directly in the RF band. The major problem of such architecture is that the receiver relies on very high input carrier power to reach -69 dBm sensitivity, which is a clear result of the low sensitivity realized by the first RF detector. This publication does not provide a figure for the power consumption, but it can be assumed the lack of RF processing blocks yields low power consumption as it is the case in the wakeup receiver. Nonetheless, this receiver is as power-saving as the transmitter is power hungry on the other side. As the transmitter is required to produce levels from $+20$ dBm to $+30$ dBm, even highly efficient transmitter architecture would still require a lot of energy. The main difference to the wakeup receiver is that the receiver has to work with amplitude modulate signals which is difficult and power hungry. This choice is avoided in the wakeup receiver as better signal analysis can be achieved in the time-digital domain.

The transceiver architecture presented in [CBM⁺06] is that of a full-blown Frequency-Shift-Keying (FSK) radio. The proposed architecture is a classical IQ quadrature detector. This is a non canonical choice for an ultra-low power radio, as the blocks that consume more power such as the oscillator and the mixer are essential. The results are still very good although power consumption for the receiver is with minimum $200 \mu\text{W}$ out of the range that is conceived as acceptable for the wakeup receiver. This architecture represents exactly the opposite architecture to the choice for the wakeup receiver as it uses all possible circuital blocks that consume energy, such as the mixers and the oscillators.

The architecture proposed in [PGR07] specifically addresses the design of wakeup receivers. The realization of this receiver gives a proof of concept for a wakeup analog front-end with interface to the digital signal processing. The proposed architecture is composed by an ultra-low power

consuming amplifier in the RF band, followed by the classical RF detector. The demodulated OOK signal is then amplified by the baseband amplifier and the result is digitized by a 6 bit Analog to Digital Converter (ADC). The additional logic to decode the wakeup signal from the digital signal is not provided in the design and implementation and is projected to be realized by the means of simple correlation. The power consumption goal for this receiver is set much higher than for the wakeup receiver, easing the overall constraints on the current draw of each block. The realization does not cover the required logic for decoding robustly the incoming messages. To prevent consuming in the digital processing, the wakeup receiver digitizes the analog signal to a one single bit digital signal, such that more complex analysis can be done without compromising the power consumption.

The same author of the previous article has published also [PGR08]. The architecture of the receiver has been completely changed to realize a completely analog radio front-end. The version of the receiver uses an ultra-low power mixer and non stable oscillator to mix the OOK signal down to an intermediate frequency where the RF detectors work better. The advantage lies also in the gain that the mixer provides. On the other side, as the oscillator cannot be stabilized with a locked loop, otherwise the power consumption would rise, a periodical calibration is needed. The circuit for this calibration may not be complicated but was not realized on chip; therefore no precise information on its power consumption is available. This receiver shares the idea of providing the following digital signal processing of a single bit signal, as in the wakeup receiver because this provides the better chances to contain the digital processing in the power budget. It must be noted the budget for this receiver is less than $100 \mu\text{W}$, whereas for the wakeup receiver this resides in the $10 \mu\text{W}$ range.

Although its architecture is not generally chosen for wakeup radios, the receiver presented in [OCR05] represents an interesting attempt to use OOK for an ultra-low power consumption radio. The resulting power consumption is far from the goal proposed for the receiver developed in this work as it is measured at $400 \mu\text{W}$. The relatively high power consumption can be attributed to the fact that an oscillator and a mixer are needed by the design to produce the steering signal of a Pulse Width Modulation (PWM) modulator that produces a digitalized signal which is decoded later on by a detector. From a performance point of view, this receiver is able to detect signals until -100.5 dBm at 5 kbit/s , which is a very good sensitivity factor for a low data rate. As this architecture (as shown in figure 2.19) requires the use of an oscillator and a relatively precise oscillator at the RF carrier frequency, the power consumption cannot be reduced beyond certain technological aspects, and the result, yet very good for a main transceiver, cannot be used to leave the receiver always active. The use of a PWM modulator will be taken for the realization of the wakeup receiver because of its immediate advantage in transforming amplitudes in times, they are much easier to analyze.

For the digital processing of the incoming wakeup message, no practical implementation is found in the literature, as it is commonly assumed that a standard logic detector can be effortlessly used in a wakeup receiver design. As it was already shown, the basis of this work relies on identifying which blocks of the design consume more energy and finding a better implementation for low power, or removing them by changing the design. It is then a personal opinion that a standard digital processing logic does not fit a wakeup receiver. The design relies on RF detectors which do not have high efficiency at low input signals, especially worsening the performance with decreasing input signal amplitudes. As a result of this, the idea is to recover signal in the digital domain by not using amplitudes that must be treated analogically to be transformed in digital signals. Digital circuits can analyze timings of edges very well and this is the reason why the

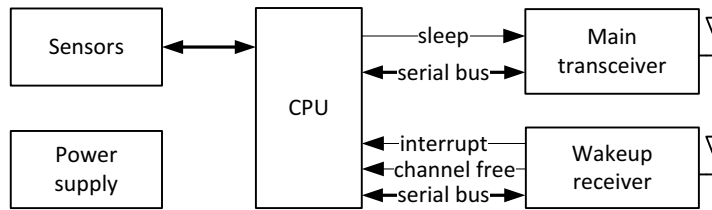


Figure 3.1: Node architecture

amplitudes are transformed into a PWM signal. This is done by modulating the frequency of an oscillator with the output of the RF detector after some amplification.

These are the design choices that lead to the proposed architecture for the wakeup receiver. The methodology for the design is simple yet efficient and involves turning the circuit to a simpler implementation and finding what blocks are responsible for high power consumption. When the blocks are identified, they are replaced by similar functions with lower power consumption blocks or the blocks are removed changing the original design, until the ultra-low power design is finally defined.

3.2 System Architecture

A typical sensor node as presented in chapter 2 is composed by a Central Processing Unit (CPU), one or more sensors, an energy storage, possibly some energy scavengers and the radio transceiver. The proposed work extends this architecture with a wakeup receiver, a separate radio receiver to be used as corner block of the radio protocol. Figure 3.1 shows the connection between the cpu, the main transceiver and the wakeup receiver. The wakeup receiver concept covers both MAC and physical layers. The physical layer of the protocol stack is actually split in two parts: the main transceiver's physical layer and the WUR physical layer. The reason of this division is in the radical differences between the modulations used by each receiver, requiring completely different architectures to deal with these. As already stated, the WUR consumes some microwatts in active receiving mode, allowing the node to always scan the channel for incoming packets. The communication therefore occurs on a dedicated channel and is limited to the handshaking protocol for the data communication.

3.2.1 Wakeup Receiver MAC Protocol

The fundamental function of the proposed MAC protocol is to implement a handshaking for reserving the channel when data must be exchanged. This results in preventing the collision of the packets when two nodes decide to use the channel for transmission. The handshaking protocol is based on the well known [Kar90] Request-to-Send/Clear-to-Send (RTS/CTS) principle. The new idea is to use the wakeup channel for the RTS/CTS handshake and the normal channel for data exchange. If a hypothetical node A needs to communicate with node B, it sends an RTS request. If node B successfully receives the request and decides that the channel can be reserved it sends back a CTS response. At this point, the channel is reserved for the communication and no other nodes are supposed to start transmission while the channel is used. This mechanism allows to circumvent the hidden node [Kar90] problem: in a example network like in figure 3.2, if

node D and node E are communicating, node A cannot sense it and would send an RTS request to B. Node B is aware (because the WUR logs each incoming packet) of the communication of D and E and therefore will wait with the CTS answer until this cannot disturb or even provoke a collision to D and E packets. In this case, this mechanism is extended by the fact that the main data transmission uses other channels than the dedicated WUR channel, so that a WUR RTS/CTS packet does never collide directly data exchange.

The WUR-MAC send operation acts differently based on the destination address which can be that of a particular node or a broadcasted packet. Both point-to-point and broadcast communications have the channel access (CA) strategy in common. The WUR supports the channel access by capturing each communication event in the channel although it does not always generate an interrupt for it. Figure 3.3 shows the slots of a channel access with the typical two transactions found also in other standards, one for channel reservation (RTC/CTS) and the other for data communication with associated acknowledgement. Figure 3.4 represents the power sequence of the main transceiver of two nodes during normal and broadcast communication. The wakeup receiver is always active and therefore not shown. The sleep mode in figure 3.4 includes idle listening of the permanently active WUR.

The wakeup procedure consists of RTS/CTS packet exchanges on the wakeup channel which has its own frame format of Logical Link Layer (LLC) not used for data exchange purposes. It is composed of a preamble, a source and a destination address, a channel information for the main transceiver (if multiple channels are available), and some forward error correction (FEC) as shown in figure 3.5.

The WUR-MAC has to check if the channel is free before starting a wakeup. The channel free (CF) status information is made available by the WUR and is asserted as long as it has not detected an incoming preamble of a wakeup packet. The channel is free only if CF is high for at least T_{unc} only then a request-to-send (RTS) packet is sent after some random time. If the CF bit is low at anytime when it is read, the WUR-MAC waits for the fixed packet duration ($T_{pre} + T_{wpd} + T_{dec}$) and then starts again. Each RTS packet contains information at which main transceiver's channel

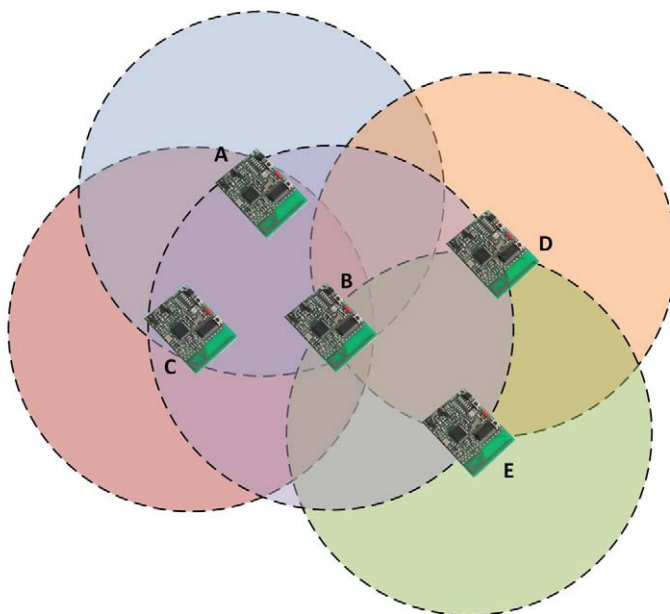


Figure 3.2: Hidden node problem

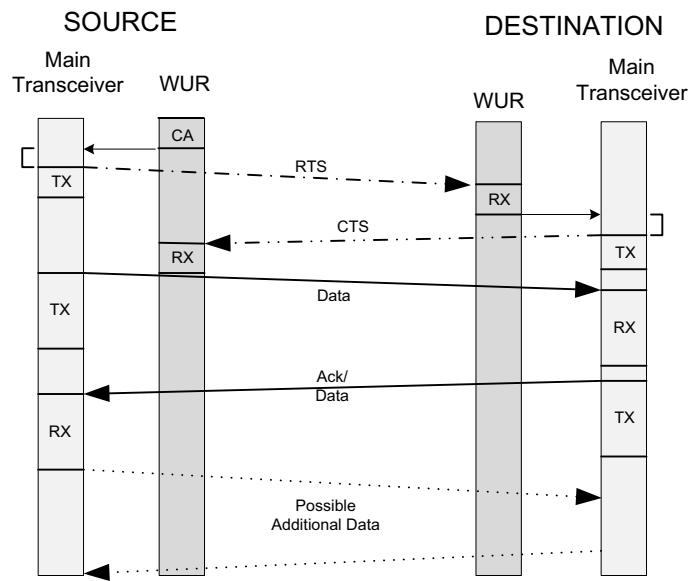


Figure 3.3: Message Sequence Chart

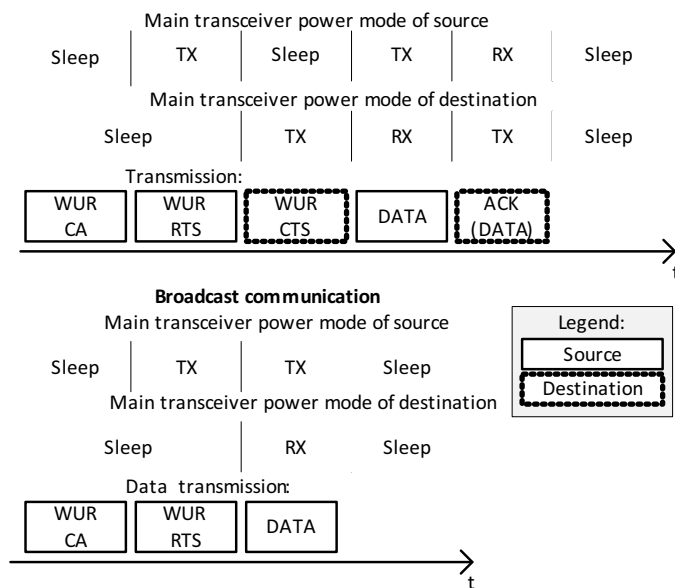


Figure 3.4: Communication sequence

communication will take place; this causes the main receiver of the destination node to turn on at the given channel. This information is only needed for multichannel main transceivers (i.e. IEEE802.15.4, IEEE802.15.1) and reduces the probability of collisions to a minimum, so that direct access to the channel can be started without any further CSMA protocol.

For a known destination, the source will transmit a WUR RTS packet that contains the non broadcast destination address. The destination, which is in sleep mode (or any other mode that does not use the main radio), reacts on interrupt if the address in the WUR packet matches its own or the broadcast. The WUR packet does not contain the source address; therefore the

destination sends a clear-to-send (CTS) with its own address as destination. After the previous RTS, the source's WUR has been programmed to react on the address of the destination. If the CTS is received within a timeout, the source starts to send the data packet on the main channel without any further delay. After this, the roles are inverted and the destination sends an immediate Ack or piggyback data and Ack to the source. Information of additional data to be exchanged is included in the header so that the communicating nodes keep the main transceiver on as long as needed in order to avoid a wakeup messages after each data packet exchange.

When a node issues a broadcast and hence all nodes shall receive it, the protocol is simpler because no CTS packets are expected to be received from the source. After successful channel access, the source sends a WUR RTS with broadcast destination and then sends the data packet via the main channel as indicated in the wakeup packet. All destination nodes that receive the WUR packet activate the main transceiver in receive mode and wait until timeout for an incoming packet.

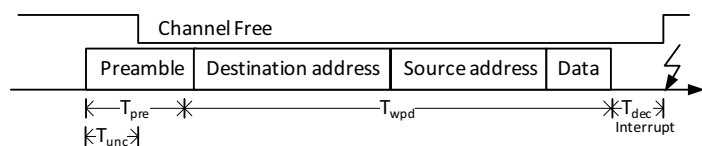


Figure 3.5: WUR Frame Format for RTS and CTS

The RTS/CTS handshake with channel assignment prevents collisions on the main channel. When only a low number of channels are available, collisions are still likely during a burst or high load. Instead of using a carrier sense mechanism on the main channel, we propose to make use of recent information from the wakeup receiver to avoid picking a channel already in use. The node sending an RTS packet has the information of which main channel was used by a neighbouring node during the last communication by reading it from the WUR which captures each incoming RTS/CTS packet. The appropriate channel is then chosen randomly between the remaining channels that have a minimum distance of two frequency channels from the possible still busy channels in the neighbourhood. The CTS response provides the channel number that will be actually used to communicate. The node sending a CTS packet can confirm the channel proposal in the RTS packet or propose a new one based on information of its own WUR. In this case, the channel is chosen randomly from the channels that have minimum distance of two from both the proposed channel and the last known channel from the WUR. The hidden node problem is solved on the wakeup channel with the introduction of RTS/CTS handshaking.

3.2.2 The Complete transceiver

The proposed transceiver is composed of two receivers and one transmitter with two modulation schemes. The wakeup receiver is conceived to work with very low power while listening to the channel, taking into account less sensitivity and less reliability, the main receiver is much more robust and has high sensitivity consuming much more power. The transmitter is able to generate at reasonable power consumption the packets that are demodulated alternatively by both receivers.

The main receiver is capable of state of the art FSK (or other frequency modulation flavors like QPSK like in IEEE802.15.4 specification) demodulation by the means of direct conversion. The receiver must also work with direct sequence spread spectrum (at least in the 2.4 GHz band) and achieve 1 Mbit/s data rate. The sensitivity lies around -90 dBm and the power consumption in active mode around 20 mW. The wakeup receiver demodulates OOK and is capable to demodulate incoming packets with 2 - 3 bytes information. The sensitivity must be at least -60 dBm and the data rate at least 100 kbit/s.

The transmitter supports the same modulations of the main and wakeup receiver. The power consumption while sending must not exceed 20 mW in both main and wakeup working mode. The wakeup receiver has an innovative architecture. As it does not demodulate frequency keying signals, there is no need to use power consuming circuits such as a mixers or local oscillators with PLLs. This is the main tactic to lower power consumption. The demodulation of the RF signals happens at the beginning of the receiver. An envelope detector transforms RF power in a DC level. When the RF carrier frequency is modulated in the amplitude, this DC level changes accordingly. In this way, an amplitude modulated signal is demodulated non-coherently. At this point, the baseband signal is already available, although some analog elaboration is needed before the signal can be fed to the digital data decoding unit. As integrated circuit must live with high tolerances and varying offsets, which differ from wafer to wafer, but also between different chips in different positions of the same wafer (e.g. at the center and at the border), it is not possible to make difficult decisions based on voltage levels. This can be done using circuits that exploit feedback, but this introduces complexity and a weak spot in the design because using feedback means also coping with stabilization of the system to prevent oscillation. The voltage levels which are available are only a fraction of the levels that can be considered digital levels; therefore some transformation is still needed in the analog domain. The small signals available are used to control the frequency generated from a simple type of oscillator. In this way, the digital analysis must detect difference in the timings to distinguish between 0 and 1 bit values, and this is a task that can be easily done in the digital domain.

The first stage of the wakeup receiver is an RF power detector, also called envelope detector because it generates at its output a signal that corresponds as much as possible to the envelope of the amplitude modulated carrier. This block is of course most important, as it decides the performance of the whole receiver in matter of sensitivity. The key parameters that influence the

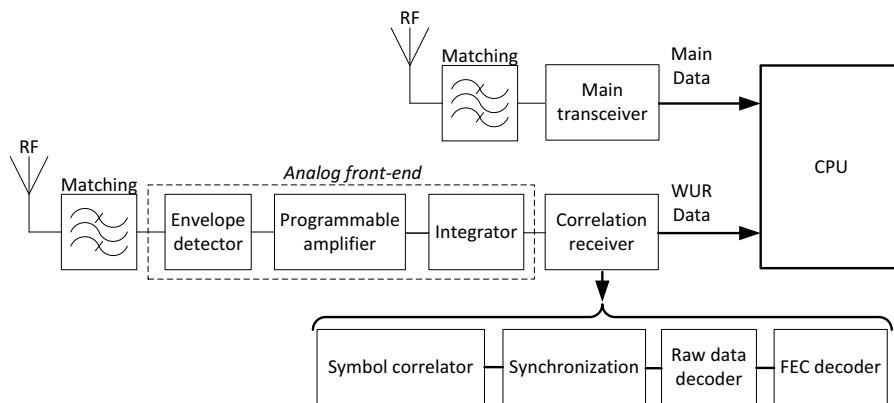


Figure 3.6: WUR architecture

sensitivity are internal noise and efficiency (η) of the detector which can be expressed as follows:

$$\eta(f_{RF}, v_{RX}) = \frac{v_{BB}}{v_{RX}} \quad (3.1)$$

The efficiency is highly nonlinear and depends on the input frequency but also on the input amplitude. The voltage produced from the detector is then amplified by a defined amount of gain which can be considered constant inside a definite range of frequencies. In reality, the amplifier stage will put an upper bound to the baseband frequency response because of the technology and a lower bound due to the topology of the amplifier, which must be AC coupled to prevent saturation on the offsets. This means that DC will not be amplified but only signals that fit the band pass. The digital modulation associates the bit value 1 to the presence of the RF carrier and the value 0 to its absence. Analytically, the voltage signal transmitted has this equation:

$$v_{TX}(t) = A_{RF}b(t)\sin(2\pi f_{RF}t) \quad (3.2)$$

The output signal is represented from A_{RF} that is the amplitude related to the antenna load. The binary pulse code is represented by $b(t)$ that assumes only the values 0 or 1 with ideally no transition time. The carrier frequency is represented by f_{RF} .

$$v_{bb} \in \{v_0 \vee v_1\} \quad (3.3)$$

$$\begin{aligned} v_{amp} &= G(f_{BB})v_{BB} \\ &= G(f_{BB})v_{RX}\eta(f_{RF}, v_{RX}) \end{aligned} \quad (3.4)$$

At the receiver side the signal converted from the RF power detector to baseband (v_{BB}) is amplified by the factor $G(f_{BB})$. The voltage generated from the detector assumes two constant values associated to a 0 and to 1 bit value (v_0 and v_1). The baseband frequency is not related to the carrier frequency for the transmission. The amplitude of the demodulated and amplified baseband signal is v_{amp} . This signal is converted to a current (that is also assuming two constant values depending on the bit value) and fed to an integration capacitor as shown in figure 3.7. The voltage on the capacitor, without the action of the triggered short circuit, is shown in the following equation:

$$i_{int} = g_m v_{amp} \quad (3.5)$$

$$\begin{aligned} &= g_m G(f_{BB})v_{BB} \\ v_{int} &= \frac{1}{C_{int}} \int i_{int}(t)dt \end{aligned} \quad (3.6)$$

The voltage on the output capacitor controls a Schmitt trigger that has a defined hysteresis range V_{hyst} . The Schmitt trigger controls a switch to reset the integration capacitor. For a given input

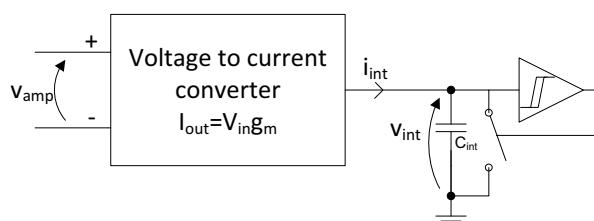


Figure 3.7: Integrator block diagram

constant current, this system produces a sawtooth voltage on the capacitor because the trigger resets the capacitor only at the threshold. The oscillation frequency depends on the current and can be calculated as follows:

$$i_{int} = C_{int}\dot{v}_{int} \quad (3.7)$$

$$i_{int} \equiv \text{constant}$$

$$v_{int}(t) = C_{int}i_{int}t \quad (3.8)$$

$$f_{saw} = \frac{C_{int}\dot{v}_{int}}{V_{hyst}} \quad (3.9)$$

$$\begin{aligned} &= \frac{C_{int}g_m v_{amp}}{V_{hyst}} \\ &= \frac{C_{int}g_m G(f_{BB})v_{BB}}{V_{hyst}} \\ &= \frac{C_{int}g_m G(f_{BB})\eta(f_{RF}, V_{RF})v_{RF}}{V_{hyst}} \end{aligned}$$

The most important factor for the digital receiver is the difference in frequency of the sawtooth signal when a 1 is transmitted (i.e. with RF power) and when a 0 is transmitted. If $f_{saw,idle}$ represents the frequency of oscillation of the sawtooth when no signal is applied to the voltage to current converter the frequency difference between 0s and 1s can be expressed as follows:

$$\Delta f_{0,1} = \frac{C_{int}g_m G(f_{BB})\eta(f_{RF}, V_{RF})v_{RF}}{V_{hyst}} - f_{saw,idle} \quad (3.10)$$

The difference in frequency can be used to calculate how many pulses per bit are generated. This depends on the amplitude of the signal at the antenna, as a smaller input power means less pulse per bit. Given an oversampling factor of the digital receiver (i.e. how many sub-bits are analyzed before deciding for the value), and given a reasonable $\Delta f_{0,1}$ to achieve enough resolution, the other parameters of the circuit can be fixed accordingly. Slower data rates are easier to decode if the digital receiver counts the number of incoming pulses, as longer bits contain more edges at equal $\Delta f_{0,1}$.

3.3 Simulations

The simulations that are presented here estimate the mean power consumption of the radio using scheduling MACs compared to the use of a WUR equipped sensor node. The results present an outlook over the advantages of the use of a WUR in terms of latency and power consumption. Simulations are computed calculating mean power consumptions for equivalent network traffic conditions (i.e. quantity of generated and forwarded packets). Collisions are not considered as they do not influence power consumption because the probability of these events is low and therefore do not need to be added to the medium generated traffic.

The following case study compares an advanced scheduling MAC protocol such as CSMA-MPS [MB04] to the WUR-MAC. The case study compares only CSMA-MPS as this protocol is already compared to other efficient MAC Protocols. As reference for the main channel of the physical layer, TI's CC2400 is taken. It is a good reference as it reflects a multi-channel, very agile, low power transceiver with high bit rate reducing on time to a minimum. The key parameters of

this transceiver and the WUR developed at our department are summarized in the preceding table. The current supply of the WUR ($7\ \mu\text{A}$) is the sum of measured values of the analog WUR implementation on a 130nm CMOS process and the estimated values for the digital part, if realized in the same technology. Currently the digital part is implemented on an external FPGA. The key parameters of this transceiver and the developed WUR are summarized in table 3.1.

The simulation is done evaluating the power consumption of a single node when receiving/transmitting at the defined rate on the horizontal axis. As the duty cycle and the overall bandwidth utilization are very low (also due to the agile multichannel 1Mbit/s transceiver) neighbouring nodes do not significantly affect the overall simulation results. The simulation computes the average power consumption (P_{ave}) in relation to the number of messages forwarded and newly introduced into the network for a given time period. The ratio of forwarding and self-generated packets has been fixed to 10:1. The data rate for RTS/CTS is chosen to be 100 kbit/s, reflecting the actual capability of WUR receivers of current research projects. The length of the overall wakeup frame (RTS and CTS) is set to 88 bits and the length of the data packet is set to 32 bit preamble plus 80 bits of data at 1 Mbit/s. The power consumption of the WUR-MAC is the sum of a constant base (the sleep power of the CC2400 and the power of the WUR in active mode) and the power needed for communication. The calculations take into account the raw send and receive times, but also the times needed to start and change mode of the transceiver. The CSMA-MPS has a fixed duty cycle and wakes up periodically by T_w . For each wakeup only, one packet can be sent or received limiting the maximum data throughput. Because synchronization takes into account the worst-case clock drift, CSMA-MPS consumes more transmit energy because the preamble length is calculated using a longer window depending on the time elapsed from the last communication.

	CC2400	WUR
Supply Voltage	1.8 V	1.5 V
I_{rx}	23 mA	$7\ \mu\text{A}$
I_{tx}	19 mA	-
I_{sleep}	$1.5\ \mu\text{A}$	-
RF frequency	2.40 - 2.48 GHz	
Data rate	1 Mbit/s	100 kbit/s

Table 3.1: Comparison of electrical parameters

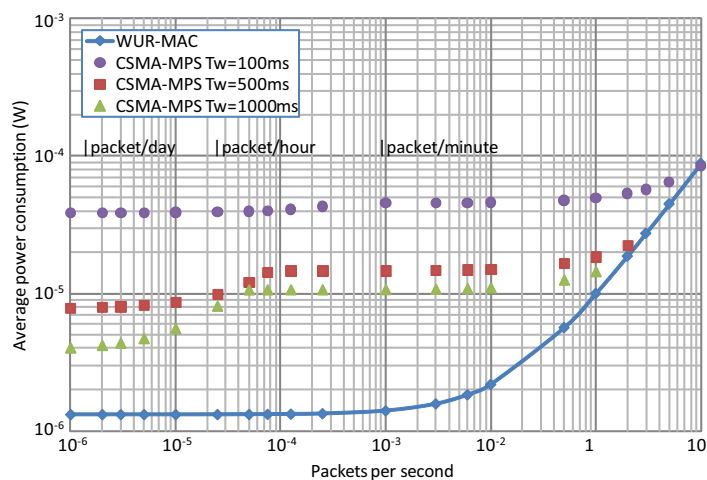


Figure 3.8: Power Comparison between WUR-MAC and CSMA-MPS

CSMA-MPS performs better when frequently communicating because it can count on the implicit synchronization and does not need energy for RTS/CTS handshake. However collisions are not simulated as typical very low data rate is assumed; however, collisions increase when the packet rate reaches an order of $\frac{1}{T_w}$. In contrast WUR-MAC gets into significant collisions only at even higher data rate as the wakeup channel is a 100% ON channel accepting requests at any time. At typical low bandwidth communication, delay for WUR-MAC is closely related to length of the communication (RTS/CTS, Data/Ack), whereas a scheduling MAC is bound to the wakeup period (T_w), which is one or two orders of magnitude longer if significant savings in energy are to be achieved. For instance $T_w = 500$ ms the average delay when not synchronized in CSMA-MPS is 250ms whereas for WUR-MAC at the above given packet sizes is about 6 ms.

The power consumption for the CSMA-MPS node is calculated as follows:

$$P_{ave,csma-mps} = \frac{t_{sync}}{t_w} P_{RX} + \frac{t_{off-on}}{t_w} P_{off-on} + P_{TX} N_{packets} (t_{TX} + \frac{2\Theta}{R}) R \quad (3.11)$$

$$R = \frac{Packets}{s}$$

The first factor of equation 3.11 is the power needed from the synchronization, which is a factor of t_{sync} , the time while the transceiver is waiting for incoming packets, and t_w , that is the periodicity of the protocol. The second factor is the power needed to start the transceiver and the third slot is the power to forward 10 packets and send 1 own packet. The $\frac{2\Theta}{R}$ factor is known to this protocol and accounts for clock drifts between two nodes.

The power consumption for the WUR is calculated as follows:

$$P_{ave,wur} = P_{wur} + P_{XCVR,sleep} + R \frac{N_{fwd}(E_{RX} + E_{TX}) + N_{own}E_{TX}}{N_{fwd} + N_{own}} \quad (3.12)$$

$$R = \frac{Packets}{s} = \frac{N_{fwd} + N_{own}}{t}$$

The first two factors are the idle power of the WUR and the sleep power of the transceiver. E_{RX} and E_{TX} are the energy needed for sending own packets and forwarding packets.

As can be seen in figure 3.8 the lower power consumption is achieved only when the WUR hardware has power consumption lower than 40 μ W for networks that can tolerate about 1 s hop-to-hop delay. When delay shall not exceed 100 ms, the WUR can consume up to 300 μ W still being lower power than CSMA-MPS without WUR. When the packet rate increases and reaches more than one packet per second, the power consumption of the WUR architecture reaches the one of the CSMA-MPS as the RTS/CTS overhead becomes more visible in WUR. At the same time, the better synchronization of the CSMA-MPS lowers the energy overhead for communication establishment.

4 Implementation of the Wakeup Receiver

The result of the implementation of the wakeup receiver as it is proposed in the previous chapter is presented in the following sections. The implementation is a key step to the verification of the concept and helps in finding possible design flaws or drawbacks of the selected architecture. The implementation focuses on the realization of the wakeup receiver in the most energy efficient way, yet performing well enough that a reasonable utilization is possible. The architecture proposed in the previous chapter already accounts for energy consumption in the design, but further optimization is required for the implementation to reach the targeted power consumption. Most of the optimization can be realized by simplifying circuits and by lowering the bias current of the analog circuits. This is only a very limited list of the optimizations that will be explained in the later sections of this chapter.

The implementation of the Wakeup Receiver (WUR) allows minimum reduction of the power consumption by identifying the main power-hungry blocks and replacing them by low power equivalents creating very low power architecture, which is a key factor in the use of such a receiver. At first, a proof of concept with existing commercial components has been realized, as demonstrator and feasibility test. The discrete implementation is realized without paying attention to low power consumption, as this can be only achieved in a fully integrated solution. On the other hand, the integrated implementation is based fully on the concept of the discrete implementation allowing the design to be optimized for low power consumption. This is possible as every single transistor in the front-end can be freely dimensioned in a full custom analog design. The back-end is all-digital and is realized in a semi-custom digital design optimizing the gate usage for low power.

The idea of demodulating On-Off-Keying (OOK) at very low power consumption is borrowed from the passive Radio Frequency Identification (RFID) (as in [NYY⁺06]) architecture because these devices do not have any energy supply source and are activated by the energy of an Radio Frequency (RF) carrier. The energy charges a capacitor until the function threshold. The device is activated and communication can occur. The energy needed for the communication is very low, as the energy scavenged has very low efficiency. The modulation used is OOK, which is the same choice for this wakeup receiver because it allows low power demodulation. RFID need high field strength to produce enough voltage to charge the capacitors and this is the main difference to the WUR, which uses diode rectification only for communication and cannot rely on high-power incoming signals. The physical layer of the wakeup receiver can be interpreted as a voltage controlled oscillator with some additional logic that is needed to decode the incoming packets in digital information. The voltage that controls the oscillating frequency is proportional to the amplitude of the RF amplitude of the input signal. The idea is that frequency can be

better analyzed in the digital domain, where complex data demodulation is achieved at much lower costs in terms of power consumption and complexity. In this chapter, both the discrete and integrated implementations are described and analyzed, giving a complete overview of the principles and details of the Wakeup receiver.

4.1 Discrete implementation tests

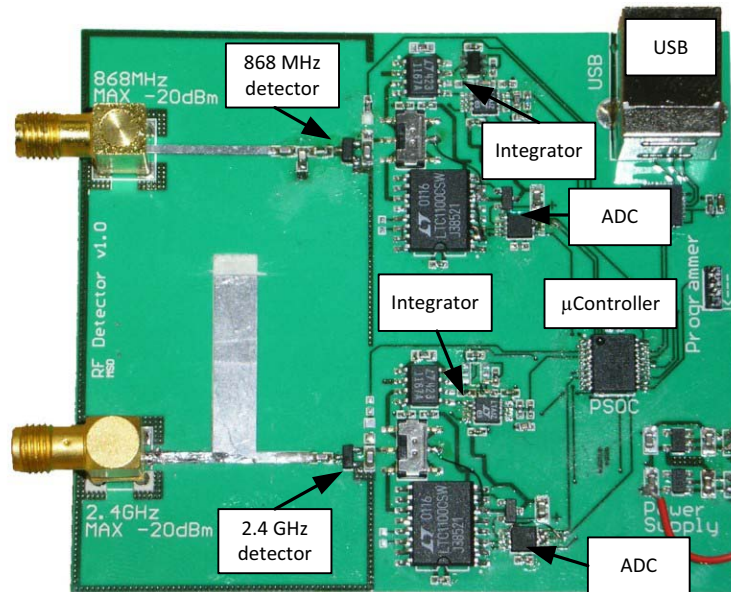


Figure 4.1: Discrete implementation WUR

The main principle of the wakeup receiver is inspired from RFID technology where radio communication is modulated with OOK and demodulated with a simple diode rectifier. This architecture is chosen because RFID have limited amounts of energy to use and the modulation scheme does not need RF blocks such as a mixer that is highly energy demanding. Two discrete realizations of the wakeup receiver were realized and tested proving the idea to be realizable also for low input RF power, which is not the case of RFID.

The implementation of RF detectors implies paying careful attention to PCB layout as RF signal routing demands particular attention. The transmission lines are realized for 50Ω impedance, to match the standard interface of measure equipment such as signal generators or spectrum analyzers. Particular PCB material such as the RO4450 is used to prevent loss and mismatches in the transmission of RF energy, allowing making precise and reproducible measurements on the devices under test. This is possible as the material has an ϵ_r (relative dielectric constant) specified to $\pm 0.1\%$, that makes possible to create microstrip transmission lines with good matching and controlled impedance that depends on the thickness of the material and the width of the conductor. Figure 4.2 shows a typical vertical section of the microstrip transmission line. The impedance of the transmission line depends on the thickness of the dielectric, on the width of the top conductor (and other physical parameters of both). The bottom conductor must be wide enough as it should approximate an infinite ground plane. Equation 4.1 is an empirical formula

to calculate the impedance of the transmission line. T must be calculated in μm whereas W and H need only to be in the same unit.

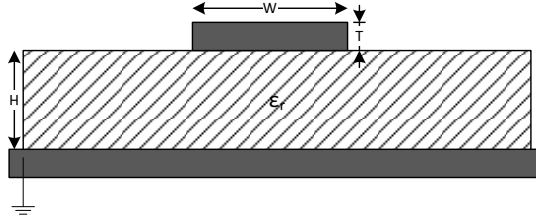


Figure 4.2: Microstrip transmission line

$$Z_0 = \frac{87}{\sqrt{\epsilon_r + 1.41}} \cdot \ln\left(\frac{5.98 \cdot H}{0.8 \cdot W + T}\right) \quad (4.1)$$

4.1.1 Concept

The implementations have as main goal to prove the concept of the amplitude to frequency converter and to measure commercially available RF detector circuits because these are not specified at the input power available in indoor wireless communications.

$$P_{Rx} = P_{Tx} G_{Tx} G_{Rx} \left(\frac{\lambda}{4\pi}\right)^2 d^{-b} \quad (4.2)$$

Equation 4.2 shows the RF received power dependent from the transmitted power P_{Tx} , from the antenna gain from both transmitter and receiver G_{Tx}, G_{Rx} , from the wavelength λ , from the distance d and from the attenuation factor b that is 2 for free space and more appropriately around 3.5 for indoor environments. Empirical data shows that at around 50 dB are lost in the near-field of the antenna, then the attenuation can be calculated. As a matter of fact Bluetooth class 2 transceivers are rated to work in the 10 – 30 m range and have typically a sensitivity of -85 dBm. These figures apply of course to the architecture chosen for those transceivers, and they require quite some power (in the mW range) to be achieved. WUR reduces extremely the power consumption at cost of reducing sensitivity to a smaller value.

The sensitivity goal is set to -60 dBm because of the simulations and available measured data on the Schottky diodes used for rectification. The discrete implementation verifies the feasibility of using a completely passive RF detector at low input power and an integrator to transform the low-amplitude voltages in logical signals. The signal of the rectifier is analyzed by an Analog to Digital Converter (ADC) or “demodulated” from the integrator. In addition to this the algorithm to decode the incoming signal is implemented in different ways. This allows us to later choose the best algorithm in matter of complexity and therefore power consumption. The PCBs are equipped with a microcontroller and as serial-to-USB bridge that allows simple connection and control with any PC. The RF detectors are realized for the 868 – 915 MHz and 2.4 GHz ISM bands and perfectly equivalent except for the matching.

Matching is realized with lumped components for the 868 – 915 MHz ISM band, as this is possible with good results to match over 10 dB due to the quality factor of the components being reasonably high. In the case of 2.4 GHz, a distributed component implementation of the matching was realized based on the reference design [8]. This implementation of the matching network has

a better quality, but also the impossibility to rework the network for fine tuning. This is only possible by new design and test of the Printed Circuit Board (PCB).

As a result of the measures, the discrete implementation offers two ways of characterizing the diode detector. The first method uses an ADC and sends the measured voltage to the PC for visualization purposes. The second method involves the use of an integrator to convert amplitude in frequency that can be analyzed much better in the digital domain. A test bed for the implementation of the digital decoding is provided by the Microcontroller Unit (MCU) that controls all the board.

4.1.2 Software

The software used to control the measures is implemented to give a simple feedback via the serial console, but does not provide digital signal processing not only because of the performance of the MCU, but also because the digital demodulation should be provided by integrated digital logic and not by software. This design choice allows further reduction of the power consumption in the integrated WUR, maintaining the flexibility in the development of the digital processing. This helps on changing setups or matching and being able to visualize instantly any enhancement or deterioration in the performance.

Principally two measures are possible on the rectifier with the discrete implementation. One 16 bit ADC is used to directly measure the voltage produced from the rectifier. The value is sampled at fixed rate and the value is printed on the console. This is used to characterize the RF detectors in reproducible and comparable terms. Offsets are evened out by calculating the arithmetical mean over 1024 samples. This measure could also be used to decode incoming data, although complex signal processing would be required. The other measure is done using an integrator controlled by the RF detector. The integrated signal is fed to a Schmitt trigger that produces the digital signal which correlates frequency to RF amplitude. In this way, the information resides in the timing, which is much easier to analyze as amplitude by digital logic, instead of software.

The microcontroller used is the PSoC from Cypress Technologies [11] which offers a good deal of analog and digital peripherals integrated with the MCU that can be freely used by the designer. The integrated Development Environment (IDE) allows the programmer to write C code and provides the Application Programming Interface (API) to control all the peripherals. In this case, the Universal Asynchronous Receiver Transmitter (UART) and Serial Peripheral Interface (SPI) interfaces are used respectively to connect to the PC via a serial-to-USB converter and to the ADC.

The offered compiler produces efficient code, yet optimization as for the GNU C compiler [15] is not present. The built-in core has flash memory and SRAM and is an 8-bit Harvard architecture design. SRAM memory is used for data and is paged if the device has more than 256 bytes, which

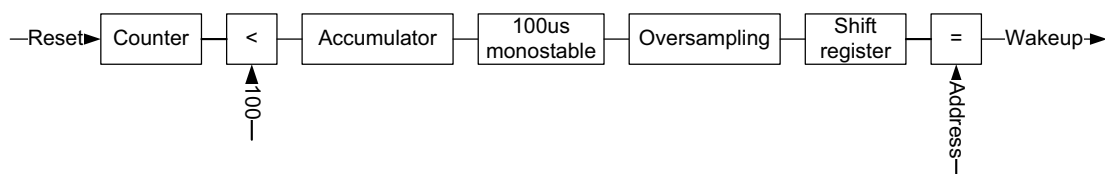


Figure 4.3: Software WUR decoder

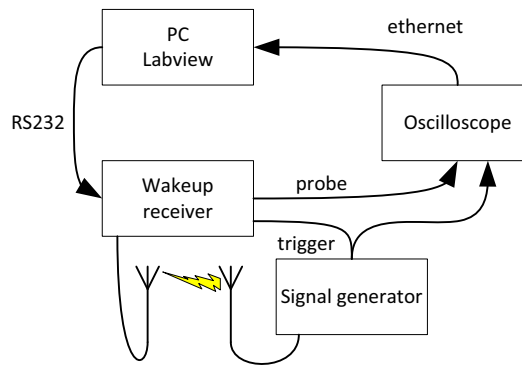


Figure 4.4: Automatic test environments

makes memory management difficult in assembler and slow in C (because of the compiler). The PSoC series does not offer a JTAG port for programming or debugging purposes, but it offers an in-circuit emulator. The emulator can be controlled by the IDE to control program flow and debugging.

The use of the serial port to control the WUR has placed the base to its use in the integrated WUR test bed. Using the PC as controller for the WUR and for measurement instruments, such as signal generators and frequency counters, enables to ease the characterization work by automating the measures. This helps in making long and repetitive measures overnight or on the weekend, saving work time and allowing measures to be more detailed.

Figure 4.5 shows a screenshot from the oscilloscope of a discrete WUR measure of the software decoder. The first trace (in yellow) shows the voltage measured on the integration capacitor. The second trace (in red) shows what the microcontroller demodulates from the reset signals. When RF power is present, the detector controls the current flowing in the capacitor. In this measure the signal is so strong that the reset occur too often for the screen resolution and appear as a thick yellow bar. The decoding algorithm used in this measure does not recover fully the real transmitted envelope.

The reconstructed signal (trace 2 in red in fig 4.3) is generated on the reset pulse timings of the saw tooth curve (yellow trace in fig 4.3). Knowing the bitrates of the transmitted signal a simple algorithm is used to produce the result showed. At the first pulse, which arrived no more than $100\ \mu\text{s}$ later from the preceding, a $100\ \mu\text{s}$ pulse is issued on the output. If more pulses are arriving always respecting the $100\ \mu\text{s}$ constraint the output signal can be prolonged always in multiple of $100\ \mu\text{s}$. Such a simple state machine is fully parametrical. The output signal (red trace) is then oversampled and the result is sent to a shift register. Finally, the value of the register is compared to a stored value and, if true, a wake up signal is asserted. The measure shown is realized using an USB dongle equipped with a cc2400 transceiver from Chipcon [26], which generates the appropriate OOK signal at $0\ \text{dBm}$.

4.1.3 Hardware

The block diagram presented in figure 4.6 shows an overview of the first revision of the discrete WUR. The board has two independent WUR circuits that differ in RF matching and used band. The two chosen bands are the $868 - 915\ \text{MHz}$ and $2.4\ \text{GHz}$ Industrial Scientific Medical (ISM),

that are unlicensed in Europe, USA and Japan. Each detector has two measuring blocks: a 16-bit ADC and amplitude to frequency converter.

The RF detector is realized with Schottky diode voltage doubler. The diodes are the HSMS-2852 from Avago Technologies [8], which are trimmed to work without bias current hence realizing a completely passive RF detector. These diodes have good nonlinearity property in the 868 – 915 MHz and 2.4 GHz ISM bands; this is very important for the rectification effect. The output of the detector is fed to an instrumentation amplifier (INA) which has is used as a voltage controlled current source. This is realized by using the reference input of the INA which has very high impedance, as shown in figure 4.7.

$$V_{out} - V_{ref} = V_{in} \cdot \frac{R_g}{10} \tag{4.3}$$

Equation 4.3 shows the relation between the input voltage and the output voltage of an INA. As ideally no current flows through the reference terminal, a resistor can be connected between output and reference and the current flowing through it is proportional to the input voltage. This current must flow through load back to ground. This current source is then connected to a capacitor. The voltage on the capacitor is effectively the integration of the voltage that controls the current. Of course this voltage cannot grow indefinitely; therefore the capacitor is short-circuited each time its voltage is at the defined threshold. The signal that controls the reset shunt contains the timing and is at all effects a digital signal. Its edges contain information on RF amplitude because the more RF power at the input, more rectified voltage is produced from the diodes. The voltage on the diodes produces a current in the capacitor that is reset with a feedback loop on its voltage. When no RF power is rectified, the system has a frequency of the reset that comes from all offsets in the circuit. The difference in the oscillating frequency signals a difference in input RF power and is therefore a relative measure.

The ADC measure path is realized by an instrumentation amplifier from Linear Technologies (LTC1100 [21]) and from a 16 bit ADC from TI (TLC4541 [30]) with a 4.096 V reference. The integrator path is realized with two instrumentation amplifiers and an analog switch (see figure

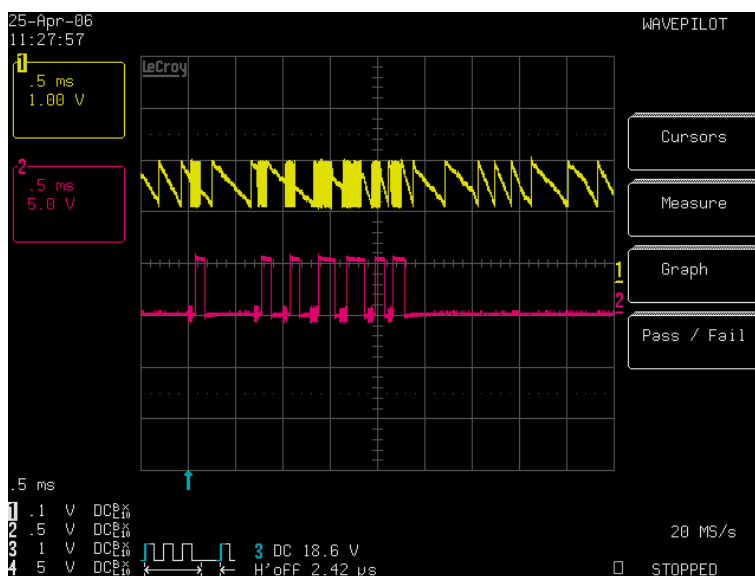


Figure 4.5: Oscilloscope screenshot of a discrete WUR measure

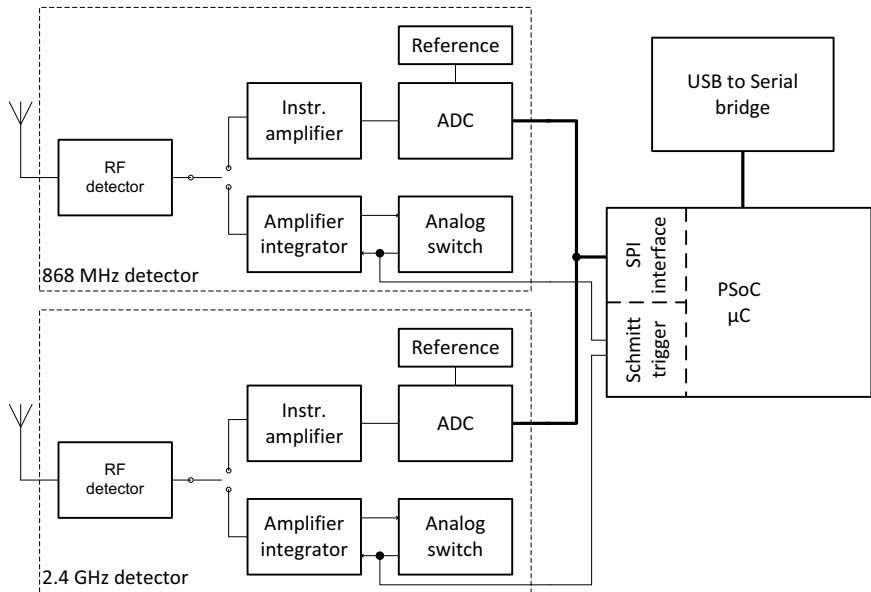


Figure 4.6: Discrete implementation block diagram, revision 1

4.7). The reset operation is realized from the microcontroller. The two paths are exclusive and can be switched manually.

The second revision of the discrete implementation is designed to enhance flexibility and to further examine the discrete implementation of the WUR. The flexibility is enhanced by modularizing the single board in three different boards. The detector is realized on a single board with appropriate material and matching done with lumped elements. This allows us to compare different matching and different detectors, and leave the rest of the system unchanged. The main MCU board acts as a controller and connects the detector board to the Field Programmable Gate Array (FPGA) development board where the actual signal decoding takes place. Figure 4.8 shows the block diagram of the entire system.

The concept of the fpga WUR is similar to the software receiver. The reset pulse is only one clock pulse long. The time between each pulse is measured by a counter, and then compared to be smaller than a constant threshold. If the compare is true a 1 bit long pulse is generated. This pulses are fed to the preamble detector and then to the oversampling unit for address decoding. The preamble detector waits for a “100001” sequence, where the last “1” is used to synchronize

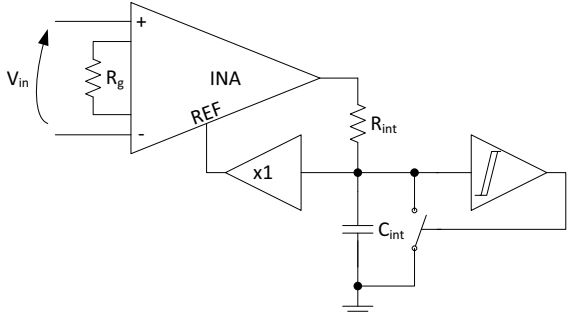


Figure 4.7: Discrete amplitude to frequency converter

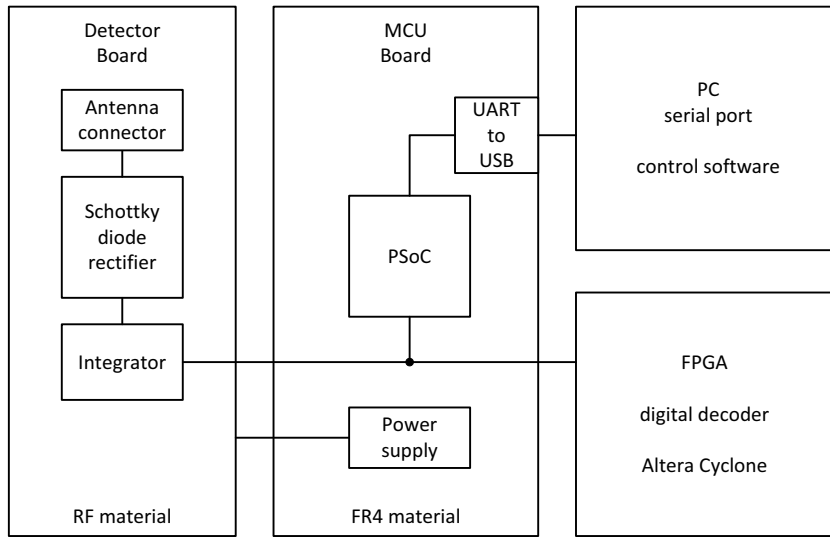


Figure 4.8: Discrete implementation block diagram, revision 2

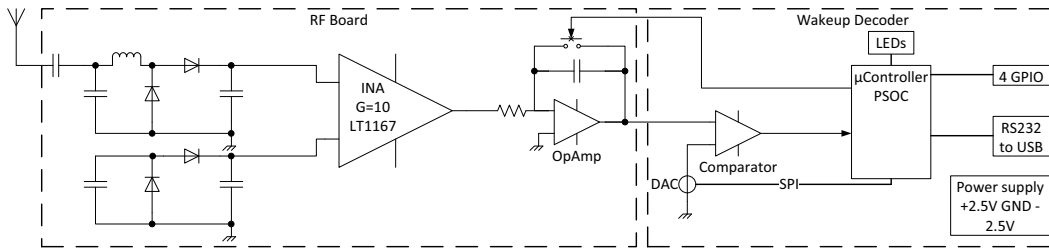


Figure 4.9: Discrete implementation circuit, revision 2

the oversampling unit. The decoded address is shifted in a serial-parallel register and compared with the stored address. When the address coincides, the wakeup signal is asserted.

The receiver is realized in a FLEX10k FPGA from ALTERA and occupies 39% of the resources. The clock frequency is 1 MHz and the decoder achieves no error rate detections at 30cm distance with a 0dBm transmitter (realized with a firmware-modified Bluetooth dongle). The three most important parameters are:

- Gain of the INA
- RC constant of the integrator
- Threshold of the receiver

Increasing the gain of the INA results in higher sensibility of the receiver, but also in higher error rates due to in-band interference. The RC constant can be used to tune the whole integrator path to defined integration times at given input power. Finally, the threshold of the receiver has to be smaller than the half bit length, otherwise it is not possible to decode successfully a wakeup sequence.

The work presented in this section lays the cornerstone to the following integrated version of the WUR. Up to this point, not much interest has been put to power consumption and sensitivity, preferring to realize a working proof-of-concept circuit. The architecture proves to realize the needed function, therefore opening the road to an efficient integrated implementation where the focus will be put on ultra-low power consumption and high sensitivity because these are the factors that matter for a usable WUR.

4.2 Integrated solution

As the discrete implementation proves that the concept works and that the architecture is a viable option for an OOK receiver, the work now focuses on the optimization of the design for integration on-chip. Ultra low power consumption (the goal is 10 mW) and full functionality can be achieved by only integrating the complete receiver on one silicon die. A CMOS 120 nm Mixed Signal technology has been chosen because of its optimal cost/performance ratio because of the vast availability of libraries and its very good modeling of the process parameters, which give reliable simulation results. Reliability of simulation results is of vital importance in chip design to achieve good experimental results.

The realization of an integrated circuit is a complex task successfully achieved with a top-down design methodology. Compared to discrete realizations, integrated circuits have the main drawback that they mostly do not allow a rework or a temporary workaround and the major cost is the production of masks. The high cost (€200k upwards) is usually shared between different projects by using one mask set to produce the so-called shared reticle, which is the composition of different ICs to form one single big block to be produced multiple times on a silicon wafer. The production cost of a single wafer is around 2 – 3% the cost of the masks, therefore not weighing too much on the total cost of a test run. The single projects are then sawed apart and each owner becomes its samples.

The top-down design consists in many phases before coming to the final tape out. For a fully custom designed Integrated Circuit (IC), i.e. an analog circuit, the definition and behavioural simulation of the design is top-down and the implementation in silicon (the layout) is bottom-up. The first phase is the requirements definition and specification of the top level. This includes main design parameters specification such as number of pins (which defines the minimum silicon area of the project) or maximum power consumption. For these parameters, the best technology is then chosen, as usually more than one possibility is available to the designer. After the top-level behavioural model is realized, the circuit is implemented in the Computer Aided Design (CAD) tools that also put strong emphasis on the hierarchy of the design (both top-down and bottom up are possible).

The design is then simulated in the second phase to check the function using standard simulations and worst-case analysis such as Montecarlo to cover process and temperature variations. If the behavioural simulation is successful, the tuning of various parameters is done to meet the specifications (e.g. the timing or the power consumption). It can happen specifications cannot be met by particular topologies of circuits although the behaviour is correct. This happens often when designing for ultra-low power. The block is modified until behaviour and specification is met. In the case of failure, a higher level redesign is needed.

The third phase, following circuit simulation, is layout drawing. This is the most important design step and needs particular attention, as a bad layout can compromise the whole function of

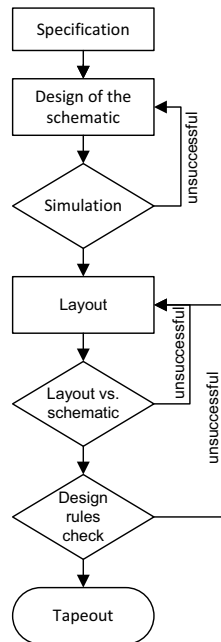


Figure 4.10: IC design flow

the chip, although the behavioural simulations are successful. This step starts with floor-planning the available areas of the chip, defining how much place is available for the blocks and where they are placed, taking into account the position of the pins. The layout is then implemented in pure bottom-up fashion. Starting from the lowest hierarchy level, each single transistor of already available block is drawn in the CAD tool. The layout is checked each block for design rules, which is a very long set of definitions on distances between the objects on different layers. If these checks are successful the layout is checked through the layout-versus-schematic tool, which verifies that the designed silicon is exactly the same as the schematic. Much time can be saved by inverting the procedure: first the layout is drawn such that it matches the schematic, placing the single blocks in the appropriate place and drawing all connections; then the design is trimmed and error in design rules are corrected. It is much more time consuming to trim the layout for all the rules and then having to draw it again because some blocks are connected wrong. When all the checks are successful, the parasitic can be extracted from the layout and used to re-simulate the circuit. This process is called back-annotation. If the simulation of the back-annotated circuit is successful the design can be released for the tape-out. Figure 4.10 represents the work-flow described.

4.2.1 Concept

From the architectural point of view a stand-alone wakeup receiver chip is presented in figure 4.11 as a block diagram. The chip is equipped with a standard serial interface used to setup the wakeup receiver and to read data of the received packets. The serial interface operates at CMOS levels with the I/O voltage which is fed from the user maintaining flexibility from 1.8 V to 3.3 V. The digital part is operated with an input clock coming typically from a real time clock (32.768 kHz). The clock frequency is multiplied internally by an ultra-low power delay locked

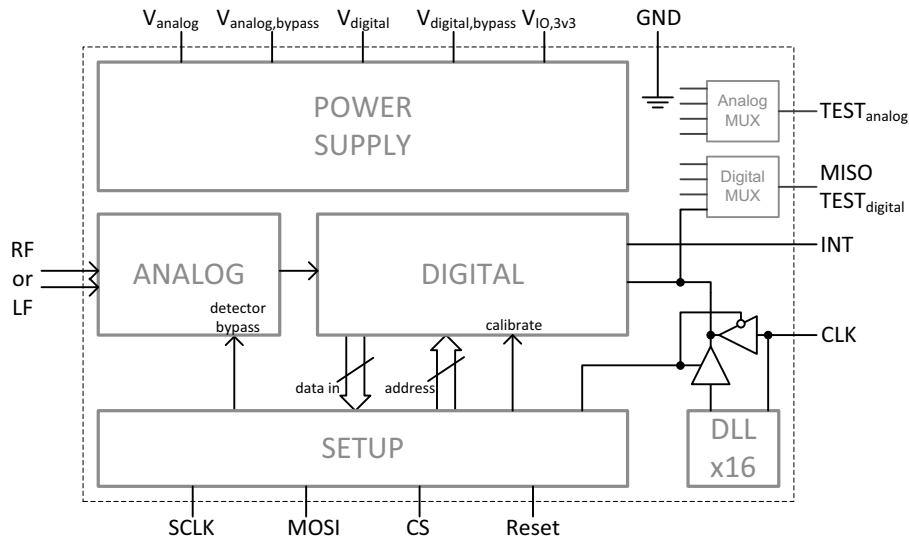


Figure 4.11: Stand-alone wakeup receiver IC

loop. The usage of the serial interface is simple and can be seen as a simple shift register. A setup bit sequence can be clocked in at any time. The most important setup bits represent the address of the wakeup receiver. If an incoming packet is detected and successfully decoded the interrupt pin signals the microcontroller (or any user of the WUR) the data is available. The data packet can then be read from the serial interface. The test purpose pins are not enabled by default and can be left open. The power supply is separated for the analog and the digital domain, as it is possible to lower power consumption tuning the digital domain voltage. The stand-alone WUR has 16 pins as described in table 4.2.

The data packet contains three bytes of data that contain a 16 bit address of the node generating the wakeup call an additional 8 bit for general purpose. One possible use is transmitting the choice of the main communication channel in a channel hopping system. The length of the wakeup packet is held very low to reduce power consumption in the decoding but also in the transmission of the wakeup packet. This is important for it makes no sense to reduce the power of the receiver if the transmitter consumes a lot of power. The idea is that the wakeup receiver sinks the power consumption of the whole network, therefore both sides of the point to point communication must be optimized (although indirectly).

The power supply of the WUR has been conceived to reduce at maximum the needs of external components on the sensor node PCB. The WUR has two separated supply inputs for the digital and analog domains. Each domain as a main input and a bypass input. The main input supports 1.8V to 3.3V supply. If the main input is used then a capacitor of at least 100nF must be connected to the bypass input for stabilization purposes. Internally the input voltage is lowered to 0.8V to 1.5V by a Low Drop Output voltage regulator (LDO), which output can be controlled in 100mV steps. This realizes extreme flexibility in the choice of the effective supply voltage for both domains, but also for testing at which voltage the two domains still work. To reduce power consumption 1.8V supply is preferable as the internal LDO dissipates on the voltage drop, therefore a smaller voltage drop reduces used power. In case an external voltage source is required or used for testing purposes, it is possible to ground the analog and digital supply inputs and

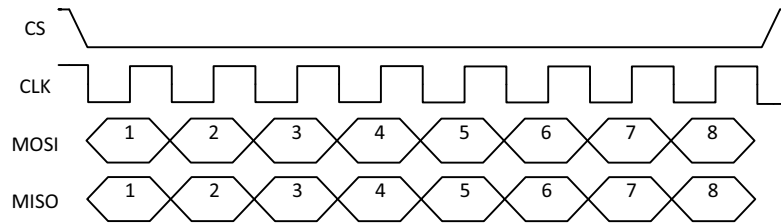


Figure 4.12: SPI bus protocol

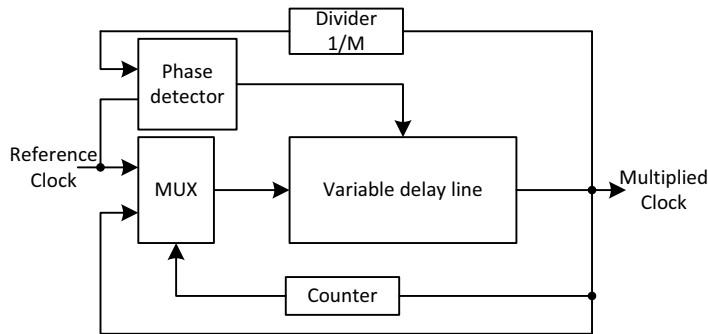


Figure 4.13: DLL block diagram

use the bypass inputs as source. In this case the maximum allowed voltage is 1.5 V. The analog power supply generates internally also all the necessary bias currents for the detector and for the analog signal processing.

The digital interface is modeled on the SPI bus because of its simplicity and support from many commercial MCU. The interface works at an externally defined V_{IO} voltage that can be chosen in the 1.8 V to 3.3 V range and must not match with the supply voltages, neither of the analog nor of the analog domain. The bus transfer for the supported SPI bus mode is shown in figure. The figure shows the chosen clock polarity and phase, typically referred to as “mode 0”. In this case, data bits are latched on the rising edge and are changed on a falling edge of the clock transition, when chip-select is asserted. Additional to the four traditional SPI terminals (chip select, clock, data in and data out, see table 4.2), the interrupt pin signalizes the reception of an incoming packet. The pin is configured as an open collector so that the line can be shared with other devices and releases the signal once the packet is read from the buffer.

The clock can be either fed from the external as reference clock (8x symbol clock) or the internal Delay Locked Loop (DLL) can be used to multiply the external clock up by 16. This is realized with the idea in mind that a sensor node will have a 32.768 kHz Real Time Clock (RTC) on board and that this can be used as source for the WUR communication. In this way the resulting symbol rate would be 65.536 kHz that is acceptable for the WUR. The clock multiplier is a re-circulating DLL based on the architecture proposed in [MM07c] and shown in figure 4.13. The concept on which bases a DLL is similar to that of a Phased Locked Loop (PLL). A DLL uses only digital gates and this is the advantage against a PLL because power consumption can be reduced to very low levels. The main idea is to feedback a delay line such that the frequency generated is divided and equal in phase to the reference clock. In this way the output clock equals the reference clock multiplied by the division factor M. The multiplexer is used to insert a “fresh” edge from the reference clock each M cycle of the output clocks. This helps to reduce jitter in the generated

Bits	Meaning
31:29	Analog LDO voltage (0.8 V to 1.5 V in 0.1 V steps)
28:26	Digital LDO voltage (0.8 V to 1.5 V in 0.1 V steps)
25	DLL Bypass
24:23	Analog Output Mux Select
22:21	Digital Output Mux Select
20	DLL Reset
19	Input Short Circuit
18	RF Detector Bypass
17	Start Calibration
16	Analog test enable
15:0	WUR address

Table 4.1: Setup Bits (MSB...LSB)

output clock. The most critical building block of the DLL is the phase detector, for which a completely digital implementation is used, yielding high accuracy and low power consumption. The details of the implementation will be discussed later in section 4.2.4.

Two balanced inputs for RF are provided. These inputs can be configured to be connected directly to the internal RF detector, which is able to demodulate up to the 2.4 GHz band. If another external RF detector needs to be used in the sensor node, in the case another band is needed or other type of detector is chosen. This widens the flexibility of use of the WUR, which can be adapted to connect to different antenna-RF detector system without changing anything in the signal processing chain, provided the modulation is kept identical. This helps also to characterize the analog front-end without the RF detector.

There are two test output pins that are provided for debug and characterization purposes. The analog test pin can be connected through a multiplexer to different signal around the analog front-end: the output of the RF detector, the following amplifier and the integrator. The digital test pin is also connected through a multiplexer to different signal generated from the digital logic such as the multiplied clock or the synchronization signals as well as the correlation output.

Using the external SPI interface the WUR chip can be setup for different parameters of function. The 31:29 bits as well as the 28:26 bits set the voltage of the internal LDOs (analog and digital respectively). As it is already mentioned each LSB controls the voltage by 100 mV. Bit 25 is needed to deactivate the DLL, in the case the clock is generated externally. The 24:23 and the 22:21 bits control the two four-input multiplexer for the test signal, where the default configuration connects the outputs to ground. The DLL has a personal reset independent of the reset of the digital signal, which is needed to characterize the locked-loop without compromising the function of the digital WUR, or during stabilization of the DLL while other parts of the digital circuit are held in reset. The analog inputs can be short-circuited to ground to calibrate the receiver on its own generated noise with bit 19. Calibration is started by asserting bit 17. Bit 16 activates the analog buffer for the analog test pins, which need some power and are therefore in normal use disabled. The remaining 16 bits (15:0) are the address to which the WUR reacts. The configuration bits are presented in table 4.1.

The next two subsections will explain extensively how the software is required to use the WUR works and how the integrated hardware implementation is realized. Both simple software implementations add ultra-low power dissipation contribute to render the wakeup receiver a viable option for Wireless Sensor Network (WSN). The presented integrated implementation can be

Number	Name	Purpose
1	V_{analog}	Analog power supply 1.8 V – 3.3 V
2	$V_{analog,bypass}$	100 nF capacitor
3	$V_{digital}$	Digital power supply 1.8 V – 3.3 V
4	$V_{digital,bypass}$	100 nF capacitor
5	V_{IO}	IO power supply 1.8 V – 3.3 V
6	GND	Common ground (physically near to RF pins)
7	$SCLK$	Clock for serial interface
8	$MISO/Test_{digital}$	Data out or Test output for digital signals
9	$MOSI$	Data in
10	CS	Negative chip select
11	$RESET$	Negative Reset
12	CLK	Clock for digital circuit (= Manchester rate / 8) 32 kHz
13	INT	Interrupt: WUR packet received with matching address
14	$RF - LF_p$	Input for RF or LF(pos)
15	$RF - LF_m$	Input for RF or LF(neg)
16	$Test_{analog}$	Test output for analog signals

Table 4.2: WUR interface pins

integrated to be a single-chip solution and used in sensor nodes as additional radio interface, or the whole design can be implemented as core in a highly integrated System-on-Chip (SoC) that includes all functions of a sensor node.

4.2.2 Protocol

The implementation of the protocol was tested as proof of concept with Meshnetics' Zigbit [23] modules that are equipped with an ATmega 1281v MCU and AT86RF230 radio from Atmel [7]. These are sensor nodes with temperature and light sensor provided with a C API for the use in ZigBee [1] networks. The reason for the choice for this platform was the simplicity of programming the MCU and the radio and the availability of APIs for the radio, as well as the availability of the GCC [15] compiler for the Atmel CPUs.

At the time of the development of the communication stack, the WUR chips were not yet available, therefore the stack as been added of an additional layer to allow the concept to be tested. This additional layer (as shown in figure 4.14) combines the communication of the WUR and of the main transceiver to use the same physical transceiver. For WUR communication the first channel has been reserved, and the other channels are used for data communication. As the hardware is shared between both WUR and main transceiver, the protocol is not as efficient as it could be as in the real WUR implementation, where WUR packets and data packets can be received at the same time.

The Medium Access Control (MAC) protocol is implemented as described in chapter 3. The interfaces to the upper routing layer is simple and contains only one specific function for packet forwarding, otherwise only a send and a receive function. The interface to the lower layers is more complicated and has to do with the particularity of this protocol. When a WUR packet is received, the routine for the elaboration of the packet is called and action is taken if it is the case. The MAC starts the main transceiver for data communication (that is forwarded to the upper layers) if the RTS/CTS handshake is successful or if a broadcast request has been received.

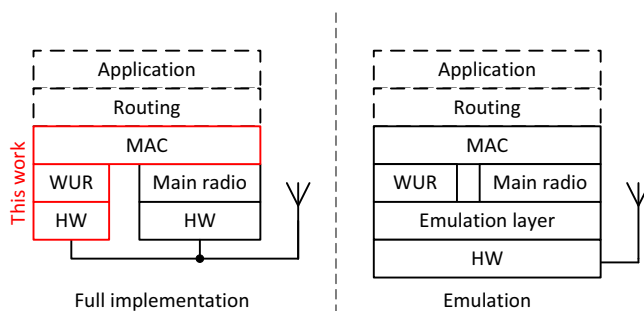


Figure 4.14: Wakeup receiver communication stack

The emulation layer offers an API to intercept hardware specific calls from the WUR and from the main transceiver drivers. The information is encapsulated and some fields are added to decode if a received packet is assigned to the WUR or to the main transceiver. The channel selection (considering the 16 available channels) is done accordingly, i.e. channel 1 is reserved for WUR traffic and data traffic is transmitted on a random choice of the remaining channels following the rule as described in chapter 3.

4.2.3 Wakeup Receiver packet format

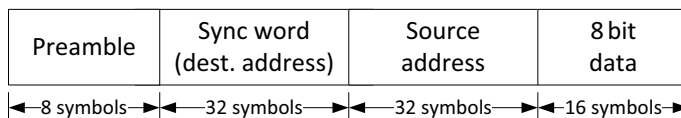


Figure 4.15: Wakeup receiver packet

A complete WUR packet is composed of 8 symbols which are used as preamble, 32 symbols that represent the synchronization word that is used to address the desired node and 40 symbols data divided in 32 symbols for the source data and 16 symbols additional data. On-Off-Keying does not allow carrier locking and clock detection as no carrier is transmitted during 0 bits. Because of the missing carrier detection, the receiver must correlate the incoming signals to detect an incoming data packet.

Each bit is encoded in a Manchester symbol because the amplifier chain that follows the RF detector does not allow DC frequency transmission and therefore no long sequences of same bits are allowed. To overcome such a problem the Manchester symbol encodes each data bit in one transition and occupies the same time. The transition is in the middle of the symbol; therefore the code is self-clocking, allowing easy clock recovery. Manchester code is used in Ethernet and many other wired and wireless applications. Even sending the same bit repeatedly does not produce a DC component in the encoded signal. DC is not dependent on the data and carries no information, being conveyed at best for such media a radio channels. A comparison of normal binary encoding (Non Return to Zero) and Manchester encoding can be seen in figure 4.16.

Before Manchester coding, forward error correction bits are added to packet. The Hamming code [Ham50] for 8 bit length and 4 bit information is referred to as Hamming(8,4) and is chosen for its simple encoding and decoding (completely combinatorial). The code is able to correct one error or detects two, in the unlikely event of three bit errors; the code cannot recover it because

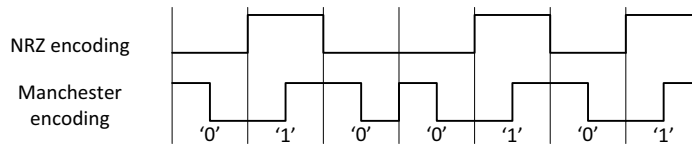


Figure 4.16: Comparison between NRZ and Manchester coding

changing three bits changes the word in a valid code. To raise the sensitivity of the receiver, the synchronization word is also Hamming coded. This prevents a complete packet from being discarded because of an error in the synchronization bit sequence. Forward error correction helps reducing the false alarms that are packet detections triggered by noise because the number of valid words is drastically reduced from 2^{32} to 2^{16} . The source address and the additional byte data are also encoded with forward error correction.

The Hamming codes [Ham50] base their principle in the Hamming distance between two strings of bits. The distance can be calculated by counting the number of different bits when checking the same bit positions in the two strings. For example $0\ 0\ 1\ 1$ and $0\ 1\ 1\ 0$ have Hamming distance of 2. Hamming codes can detect and correct single bit errors and detect single bit error, though not correct them. The encoded data adds redundancy (or parity) bits so that the encoded bit strings have at least Hamming distance of two. In this way, the additional bits enable the detection and correction if necessary. The chosen code Hamming(8,4) produces 8 encoded bits out of 4 data bits as follows (the symbol \otimes represents bit XOR and ! represents a negation):

$$\{b_3, b_2, b_1, b_0\} \Rightarrow \{b_3, b_3 \otimes b_2 \otimes b_1, b_2, !b_2 \otimes b_1 \otimes b_0, b_1, !b_3 \otimes b_1 \otimes b_0, b_0, !b_3 \otimes b_2 \otimes b_0\} \quad (4.4)$$

the encoded 4 bits are presented in the table 4.4. The encoder is implemented fully in combinatorial logic as the equation 4.4 shows. The decoder is also realized fully combinatorial and is based on the calculation of the parity bit (p) and of three check bits (c_2, c_1, c_0) for the received 8 bit word ($h_7h_6h_5h_4h_3h_2h_1h_0$). The parity and check bits are calculated as follows:

$$\begin{aligned} p &= h_7 \otimes h_6 \otimes h_5 \otimes h_4 \otimes h_3 \otimes h_2 \otimes h_1 \otimes h_0 \\ c_0 &= h_7 \otimes h_5 \otimes h_1 \otimes h_0 \\ c_1 &= h_7 \otimes h_3 \otimes h_2 \otimes h_1 \\ c_2 &= h_5 \otimes h_4 \otimes h_3 \otimes h_1 \end{aligned} \quad (4.5)$$

If the p bit is equal to 1 then either no or two errors occurred. If all the check bits are equal to 1 then the 8 bits were received without errors, otherwise there are two errors. If p is 0 there is a single bit error which can be corrected as follows: The wrong bit must be inverted. Wrong bits in the h_6, h_4, h_2 and h_0 position are insignificant since they are not used in the decoded byte, that is composed by the following bits (inverted if necessary): h_7, h_5, h_3 and h_1 .

4.2.4 Hardware Wakeup Receiver

The hardware implementation of the WUR is the step from the concept to real ultra-low power consumption. Each building block of the receiver is analyzed in its function and is implemented in the lowest power consumption version as possible. For analog building blocks this means reducing bias currents as much as possible. For digital circuits this means reducing the total number of gates to reduce gate leakage, and to drive at maximum clock speeds only a subset of the used

c0	c1	c2	wrong bit
1	1	1	h_6
1	1	0	h_4
1	0	1	h_2
0	1	1	h_0
0	0	1	h_7
0	1	0	h_5
1	0	0	h_3
0	0	0	h_1

Table 4.3: Hamming (8,4) error detection

4 bit data	8 bit Hamming coded
0h	0000 15h 00010101
1h	0001 02h 00000010
2h	0010 49h 01001001
3h	0011 5Eh 01011110
4h	0100 64h 01100100
5h	0101 73h 01110011
6h	0110 38h 00111000
7h	0111 2Fh 00101111
8h	1000 D0h 11010000
9h	1001 C7h 11000111
Ah	1010 8Ch 10001100
Bh	1011 9Bh 10011011
Ch	1100 A1h 10100001
Dh	1101 B6h 10110110
Eh	1110 FDh 11111101
Fh	1111 EAh 11101010

Table 4.4: Hamming(8,4) encoding

logic. For flexibility in the verification, the digital receiver was not integrated in the CMOS chip, the digital function was implemented in an FPGA. The validated design can be then directly imported in the tool chain for synthesization and layout production.

The block diagram of this implementation of WUR is shown in fig. 4.17. The first stage is named matching and is implemented both internally and externally to the WUR chip. This stage is intended to raise voltage as high as possible at the input of the envelope detectors as this is what affects the sensitivity of the whole receiver the most. It is not a matching in canonical sense of power-matching because this does not matter for the envelope detectors. The second stage is the analog front-end that includes the detector, the amplifier chain and the integrator. The third stage is the correlation receiver that is implemented off-chip in an FPGA.

The dashed box in figure 4.17 includes the analog front-end that has been implemented in a CMOS 120 nm technology. The analog front-end includes the RF envelope detector (or rectifier), the bandwidth programmable amplifier stage and the integrator. The correlation receiver is a digital circuit and is implemented externally on FPGA.

The RF detector is realized with a complementary circuit based on a simple nonlinearity provide by a transistor, which provides the highest non linearity in a CMOS process. A nMOS transistor rectifier produces a negative voltage and a pMOS transistor rectifier produces a positive voltage

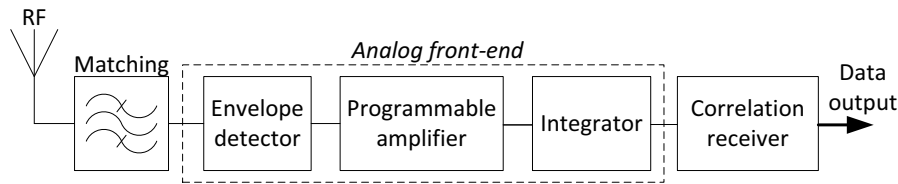


Figure 4.17: Wakeup receiver block diagram

when a carrier signal is applied to their inputs. This detector is based on the model presented in [JO04]. To enhance the non linearity using low current bias, the transistors are kept in weak inversion. The CMOS detector needs 300 nA bias current. The N and P rectifier are used in parallel and are matched to produce the same amount of baseband amplitude for a given input power. As stated before, a voltage-matching is needed to raise the voltage available at the rectifier's input to enhance sensitivity. The rectifiers follow an exponential law and therefore the output amplitude decreases more rapidly than the decreasing input. The input of the detector is mainly capacitive, particularly in the MOS circuit, but also on the Schottky circuit. The amplitude of the applied voltage can be increased by using a capacitive divider and the resonance effect from the internal circuit and the bonding cable, which is to be completed off-chip to tune the resonance frequency to the desired band.

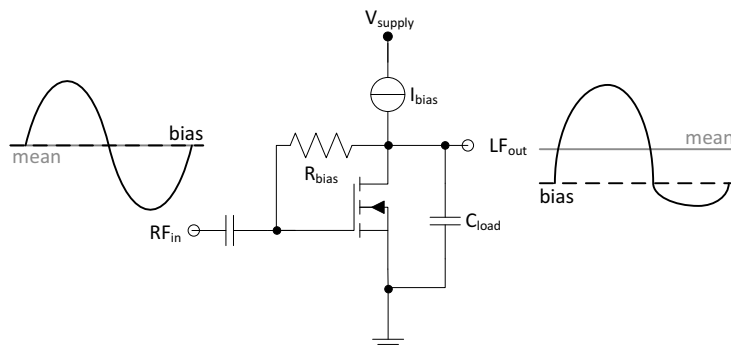


Figure 4.18: MOS RF detector (single ended version) from [JO04]

The MOS rectifier as shown in figure 4.18 is a simple yet effective version of envelope detector. The rectifier works by controlling the gate voltage of the transistor. A coupling capacitor and bias resistor are needed to keep the transistor in the appropriate state. When an alternating signal is overlapped to the gate bias voltage, the output voltage changes accordingly to the gain factor of this simple stage, which is also an amplifier. If the bias is chosen appropriately, the circuit distorts the input signal. The input signal must have zero mean value, and a sinusoidal wave is the best candidate to control the detector. Given the nonlinearity introduced by the transistor stage, the output signal is a distorted waveform that is not symmetrical and therefore it's the mean voltage is not the bias voltage of the output. The load capacitor at the output is used to filter the RF component and to leave only the LF component, which is the envelope of the input signal.

A rectifier with Schottky diodes offers also good rectification. The simple circuit is shown in figure 4.19. The circuit does not need any bias current and is therefore suitable to the WUR. Good Schottky diodes are not easily found in standard CMOS technology but there are enough

off-the-shelf available diodes to choose for. The circuit needs both capacitors that store the peak voltage on each half-wave.

During the positive half-wave the C_c capacitor is loaded because D_1 is conductive and D_2 not, therefore the output voltage on C_{load} is maintained as no path to ground is provided. During the negative half-wave C_c is pre-loaded from the positive half-wave to the peak voltage of the input wave. D_1 is not conductive and current flows to through D_2 charging C_{load} . The voltage applied to C_{load} is the peak of the sine wave added by the voltage on C_c which is also the peak voltage of the input signal. Because of this double charging effect, this circuit is commonly called voltage doubler.

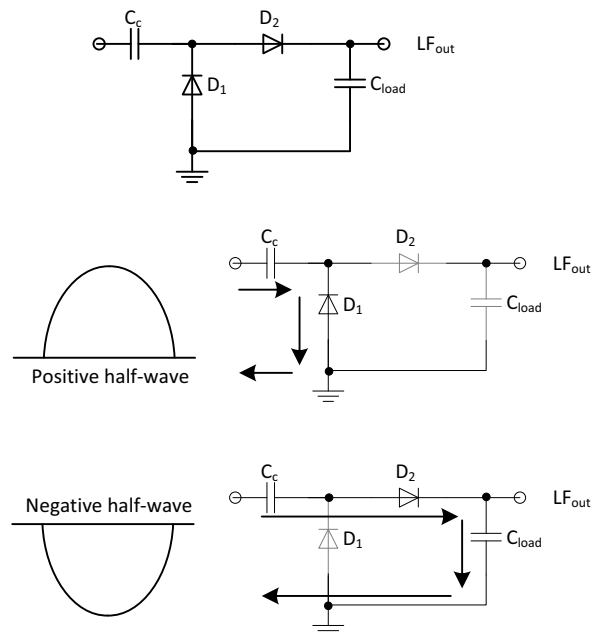


Figure 4.19: Schottky diode RF detector (single ended version)

The internal RF detector can be bypassed, if a particular external detector is used. In this case, the current used by the internal RF detector can be shut down, saving around 300 nA supply current. An external RF detector can be realized for example with Schottky diodes. In [8] a zero-bias RF detector for less than 1 GHz is presented and analyzed. This is used to demodulate analog video signals and for passive RFID tags. A complementary version of this is realized and the results can be seen in chapter 5. The main advantages over the CMOS implementation are the completely passive implementation and the higher nonlinearity.

Such RF detectors are highly nonlinear in the performance, i.e. in the relation between input power and output dc value. This depends from nonlinearity grade of the detector. The MOS transistors in weak inversion have an exponential dependence of the output current in relation to gate voltage. Schottky diodes have also an exponential relation. This has the main drawback that a difference in 10 dB in the input RF power means a bigger loss on the rectified output. This loss increases if the input power diminishes. Measures of this behaviour can be seen in chapter 5.

The weak signal generated from the detector must be amplified and this is realized with a simple chain of differential amplifiers. The topology chosen is the fully differential amplifier. The am-

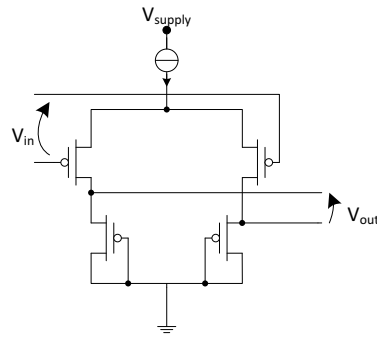


Figure 4.20: PMOS differential amplifier

plifier (figure 4.20) is realized only with PMOS transistor because of their overall lower noise in the used technology. In particular these transistors have lower flicker noise that has a significant power in frequency spectrum below 10 kHz. The gain stages are AC coupled between each other. This is a design constraint because otherwise the offset of the first stage would be amplified by each following stage, saturating the chain output at ground or at the supply voltage. In this way, the differential gain can be quite big without affecting the function of the chain. The gain is around 500 (54 dB), preventing saturation of the internal noise which is produced from the RF detector (that is the other limiting factor for the sensitivity of the receiver). The first gain stage of the amplifier chain is dimensioned to produce less noise as the detector, so that the RF detector's noise dominates and no relevant noise is added. To achieve this, most of the current needed from the amplifier chain is used by the first stage that needs around $1.2 \mu\text{A}$ current bias with a gain of 6 dB, whereas the other stages need around 300 nA each for a 9.5 dB gain. These bias currents allow the bandwidth of the chain to allow enough space for the input signal and yet some more band for testing purposes. The overall power consumption is then $2.4 \mu\text{A}$.

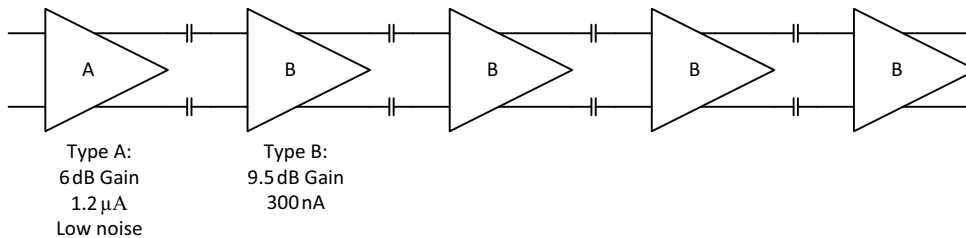


Figure 4.21: Complete AC coupled amplifier

The integration occurs after the signal coming from the RF detector is amplified. The integrator is realized with an additional differential amplifier which has current mirror as active load. The output is a current depending on the voltage difference at the inputs. This current is mirrored and added to a constant current and fed to a capacitor. The voltage on the capacitor is the integrated input voltage. The constant current is needed because the differential amplifier has a random offset at its inputs, and this produces a leakage current at its output that can be positive or negative. To prevent the current being negative, a constant is added.

The voltage at the capacitor controls a Schmitt trigger, which shorts the capacitor to ground if the upper threshold is reached. When no input signal is present, the signal on the capacitor is a sawtooth wave (figure 4.23) because of the feedback of the Schmitt trigger and the constant

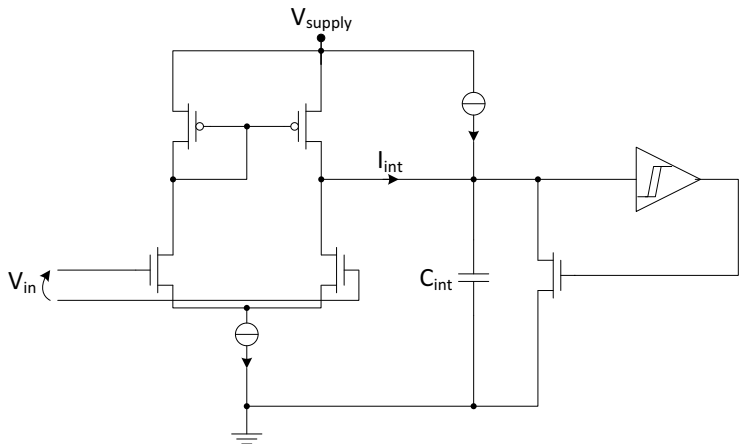


Figure 4.22: Integrator block diagram

current. An input signal changes the frequency of the sawtooth higher or lower depending if the signal is positive or negative. As the amplifier chain is AC coupled, after preamble the presence of RF power produces a positive signal and the absence a negative signal. In this way a “0” can be detected by a slower frequency and “1” by a higher frequency than the idle frequency. The frequency is evaluated using the output positive edge of the Schmitt trigger that resets the integrator capacitor, as it has a full voltage swing that is compatible with digital circuits. The steepness of the edge produced by the Schmitt trigger must be high enough to prevent power consumption of the digital input to which it is connected. A positive side effect to the integration is the filtering of noise. This noise reducing effect is included with the circuit topology and helps in increasing sensitivity.

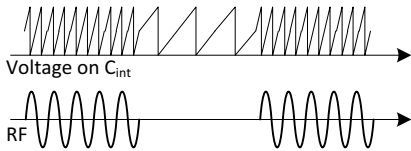


Figure 4.23: Integrator signals

At this point the signal is ready to be processed by the digital correlation receiver that correlates the pattern in the input signal that matches to that of a WUR packet. This stage is important, as it constitutes the interface to the rest of the sensor node and to the digital elaboration and needs to be very efficient by providing robustness in the decoding and ultra-low power consumption.

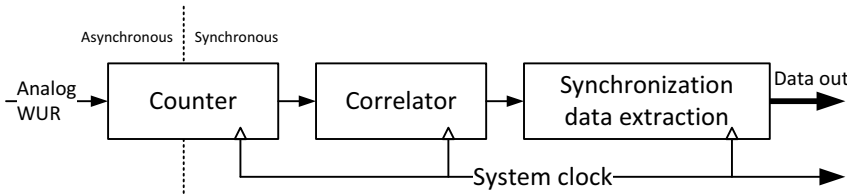


Figure 4.24: Correlation receiver block diagram

The digital WUR is divided in an asynchronous and a synchronous block because the signal

produced by the analog front-end is not provided with a clock signal as this is not necessary. The first stage is an edge counter (see figure 4.25) with capture register and single bit output. The falling edges coming from the analog WUR are counted continually by a synchronous counter. The value of this register is captured each clock cycle in a parallel shift register with two taps. The difference of counted edges between the second and first tap is computed each clock cycle. If this difference is greater of the threshold, the single bit output is asserted. This reduction of the digital signal from the multi-bit information to single bit information can be compared to the choice of using an RF detector as first stage in the analog front-end. This helps reduce the consumption of the processing blocks that follow. In the same way the signal is reduced to a synchronous 1 bit signal that can be processed by the following digital blocks using less energy. The threshold is calculated as arithmetical mean over 1024 samples when the input from the analog WUR is disabled, so that the system is calibrated around internal noise. This does not happen automatically, therefore the user of the WUR (i.e. the MCU) must trigger this calibration periodically, or if environmental condition that affect noise changes.

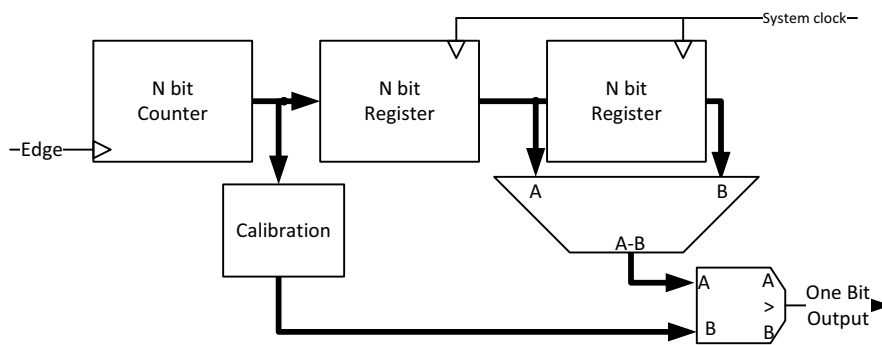


Figure 4.25: Edge counter

The two following blocks of the receiver compute the correlation of the input signal to the parameters that identify a WUR packet. This is the most parameterizable part of the complete receiver. As a design constraint, the system clock must be a factor M of the input symbol, which is a Manchester symbol as explained in section 4.2.3. As the Manchester symbol is composed always by two levels and an edge it is logical that at least two samples per symbol must be provided for data reconstruction. There is a limit on the upper value of samples per symbol other than power consumption given by the increasing sampling frequency (if the data rate is held constant) and the explosion in gate count of the circuit as it will be shown later. Therefore a choice of 8 samples per symbol is considered a good trade-off between complexity, power-consumption and robustness. The choice goes for the highest sample rate per symbol as possible as it results in better synchronization to the incoming packets later in the decoder.

The chosen factor between sample clock and symbol rate is 8 because this allows enough timing flexibility in the synchronization to the incoming packet. This is important as the WUR transmitter and receiver of two different nodes are by no means synchronized. The other reason for the choice is that the data decoder then needs eight chains that each work on one sample over eight. The needed clock for the data decoder is the same as the symbol rate.

The single bit output of the counter is synchronous to the clock. The stage shown in figure 4.26 samples the output of the counter in a eight bit linear shift register. Each clock cycle the byte in the register is correlated to the Manchester symbol for 1. The correlation decides if the symbol

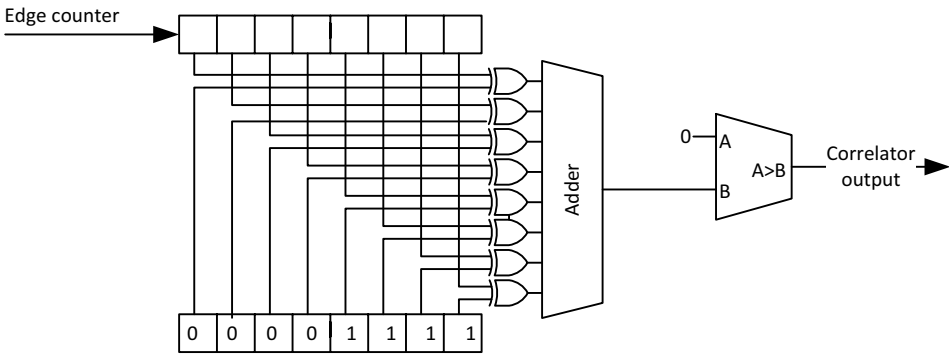


Figure 4.26: Symbol correlator

is a 1 or a 0 with hard threshold. The correlation is done by XORing each bit of the input shift register with each bit of an eight times oversampled symbol. The sum of the 8 XOR outputs is the value of the correlation, when same bit values result in +1 and different values result in -1. For eight bit samples the results of the correlation lie between -8 (matching to 0) and +8 (matching to 1). A correlation value greater than zero is considered a symbol value of 1; otherwise 0. The Manchester code, if considered as the sum of two sub-bits, can be seen as a Barker code. These codes have the peculiarity that the autocorrelation of two non aligned codes always have a maximum autocorrelation of 1, and that the result of the correlation of two aligned codes is equal to the code-length. This difficult decision has been proven experimentally to be the best choice resulting in fewer errors.

At this point the output of the correlation is a synchronous correlation stream clocked 8 times the symbol rate. As the receiver is completely unsynchronized the incoming packet can start at each 8 clock cycle starting from a t_0 time. The detection of the synchronization is done eight times in parallel for successive correlation values so that no synchronization is lost if another synchronization is detected within one packet time. The synchronization is detected if the word is decoded successfully and it matches the address of the WUR. The data is decoded only if the synchronization is successful, in order to reduce power consumption.

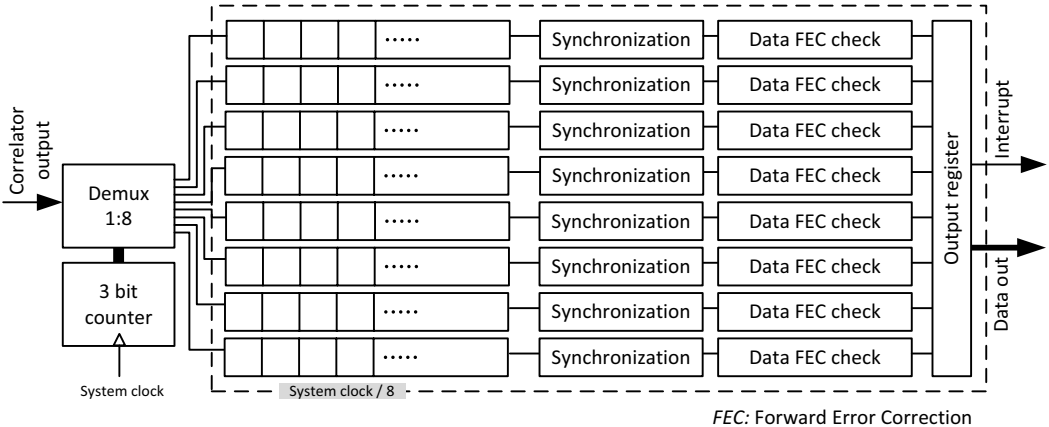


Figure 4.27: Data decoder

To add robustness and decrease the needed minimum input Signal to Noise Ratio (SNR) of

the digital receiver, all information bits in the packet are doubled for Forward Error Correction (FEC). This halves the actual data rate but increases the sensitivity of the receiver because of the ability of correcting single errors over eight bits. The synchronization word is also encoded with FEC and this enhances the ability of the receiver of capture packets because otherwise by only one bit error on the complete word all data is discarded and therefore the whole packet is lost.

The synthesization of the digital WUR shows use of 2000 gates in CMOS 120nm, that needs approximately $200\ \mu\text{m} \cdot 200\ \mu\text{m}$ area. The synthesization tool estimates the power consumption under $5\ \mu\text{W}$ for a clock of 400kHz. As it is shown in the measures in chapter 5, the minimum required input SNR for the digital WUR is 2.8dB giving a sensitivity of $-54\ \text{dBm}$ using the external Schottky RF detector.

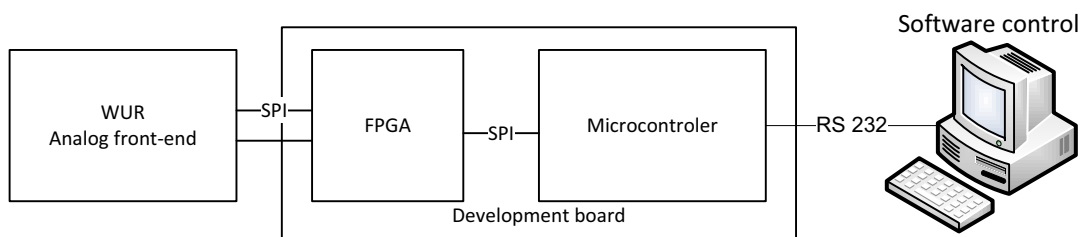


Figure 4.28: WUR test setup

The analog front-end of the WUR has been developed with the Cadence tool chain for full-custom IC design. Figure 4.29 shows a layout plot of the produced chip. This tool chain offers connection to the partner semi-custom tool chain for digital circuits based on standard cells libraries. The digital circuit has been verified with an external development board that provides connections to the WUR and to a PC for the necessary control software as well as the FPGA for the digital receiver prototyping. The major design parameters of the WUR have been summarized in table 4.5. The next chapter will give extensive information on the results of this implementation and its discrepancies to the designed WUR.

The layout plot in figure 4.29 shows the analog front-end of the WUR. The chip includes for test purposes three analog WURs. The first chain is equipped with the MOS detector, the second chain has a MOS detector and a Low Noise Amplifier (LNA) on its front and the third chain has no detector at all to be used with an external RF detector. The circuit uses less than 50% of the area as the dimensions ($1.2\ \text{mm} \cdot 1.2\ \text{mm}$) are constrained from the number of pads. This allows some flexibility in the composition of the final design of the test chip. The plot shows a fairly big size bandgap current reference that is used to bias all the circuits with a stable and known current.

Process	CMOS 120 nm
Supply Voltage	1.5 V
MOS Envelope detector power	1.5 μ W
Amplifier Chain Power	4.5 μ W
max Gain	54 dB
Bandwidth	1 MHz
Integrator	1.5 μ W
simulated power of the Correlation receiver	5 μ W
WUR chip dimensions	100 μ m · 200 μ m
Digital WUR estimated dimensions	200 μ m · 200 μ m
WUR test chip dimensions	1.2 mm · 1.2 mm
<i>Overall performance of the WUR based on the MOS detector</i>	
Power (estimation)	12.5 μ W
Data Rate	100 kbit/s
Sensitivity	-50 dBm
<i>Overall performance of the WUR based on the Schottky detector</i>	
Power (estimation)	11 μ W
Data Rate	100 kbit/s
Sensitivity	-54 dBm

Table 4.5: Design parameters of the WUR

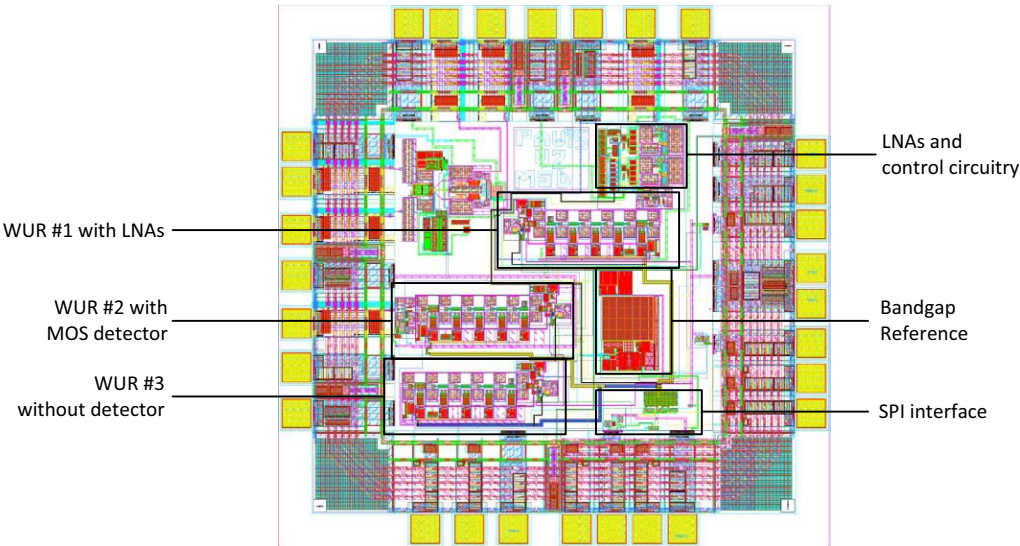


Figure 4.29: Layout plot of the WUR

5 Results and performance

The previous chapter presented the implementation of the Wakeup Receiver (WUR) (shown in figure 5.1) as explained in chapter 3. This chapter gives an overlook of the performance of the implementation in all its details. The results of the discrete implementation are presented as precursor of the integrated implementation of the WUR. The most important objectives of the integrated implementation of the WUR are ultra-low power consumption and reasonable sensitivity of the receiver. These two factors can completely influence the life expectancy of a Wireless Sensor Network (WSN), thus also its economical advantage over “wired” solutions. The reduced power consumption of the WUR has been shown in chapter 4’s analysis to be more than competitive to scheduling MAC protocols.

Circuit-level simulations estimate a maximum total power consumption of $15\ \mu\text{W}$ at $1.5\ \text{V}$ power supply. This has been shown¹ to be a reasonable value for the WUR if the projected life expectancy has to reach over five years. The WUR has been realized at first with discrete components, as proof-of-concept, showing its peculiarities, robustness and problems also in harsh environments such as the $2.4\ \text{GHz}$ ISM band, where IEEE 802.11 wireless-LAN and Bluetooth, among other radio communication standards, are active. The analog part only has been integrated at first, using an FPGA to develop the digital receiver architecture. The final test chip must integrate both parts and can be directly connected to an antenna and to a microcontroller. The measurements demonstrate a power consumption of $12.5\ \mu\text{W}$ at $1.5\ \text{V}$ and room temperature for the analog front-end, with a sensitivity of $-54\ \text{dBm}$.

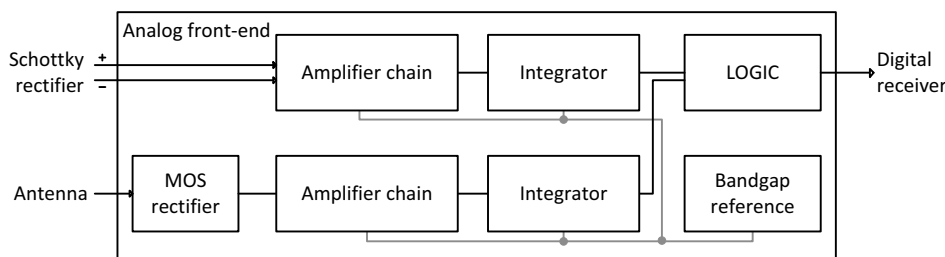


Figure 5.1: WUR block diagram

All the measures presented in this chapter offer an overview on what can be improved in the design of the WUR. The implementation achieves successfully the power consumption of under

¹see chapter 2 and 3

$15\ \mu\text{W}$, which can be considered in each case the most important result of the work. This power consumption coupled with the resulting sensitivity offers a reasonable performance for the receiver to be used in the field of wireless sensor networks.

Specifically, there are some points in the implementation that can be enhanced by further research work. Most importantly is the sensitivity of the receiver, which resides both in the detector efficiency and in the noise floor. Both these factors are strictly connected to the technology and require very specific work to be enhanced. The amplifier chain satisfies its functional requirements, but leaves room for further lowering of the power consumption. The integrator proves to be a most important building block of the receiver in realizing ultra-low power consumption as it transforms low voltage in easily detectable time difference between pulse edges.

5.1 Discrete Wakeup Receiver measures

The circuit presented in section 4.1.3 has the purpose to show the usability of the Radio Frequency (RF) detector directly without an RF amplifier for ultra-low power consumption. The picture presented in 5.2 shows the complete measure setup for the discrete WUR. The developed system uses an RF generator, a function generator for the baseband, an oscilloscope for waveform logging, a computer equipped of Labview [25] software and a network analyzer.

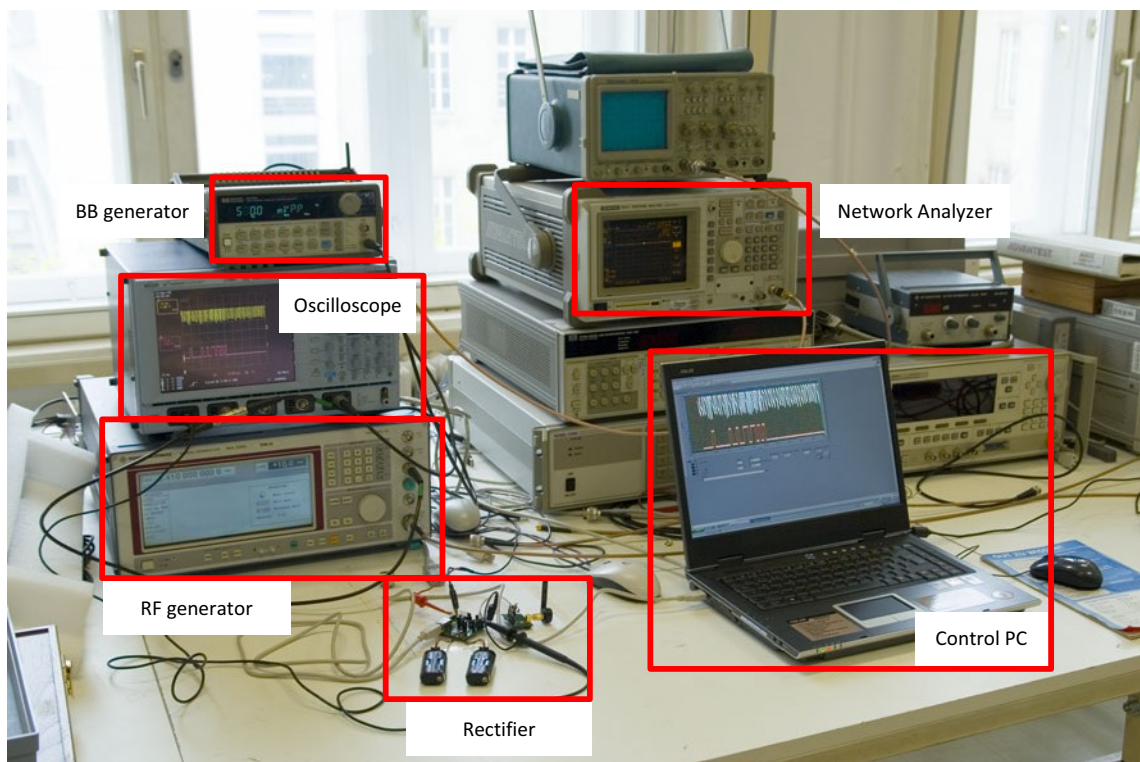


Figure 5.2: Discrete WUR measure setup

This setup allows the unattended automatic repetition of measures and is used to test the efficiency of different algorithms to decode the wakeup signals from the output of the integrator. The measures shown in figure 5.3 are taken from the circuit shown in figure 4.7. The voltage produced

from the Schottky detector is amplified linearly and the converted in a current that charges a capacitor until a threshold that short circuits the charge and resets the voltage on the capacitor. If the input voltage is constant, the charge current will be also constant and the voltage on the capacitor will ramp at constant steepness. These measures show that there is enough difference in the time (needed to reach the threshold) between the different power levels used (-60 dBm to -75 dBm shown in figure 5.3). The exponential character of the rectification diode can also be seen in the difference between each measure step, as the input power is given in dBm, which is a logarithmical measure. As the integrator behaves linearly, meaning that the current charging the capacitor is directly proportional to the input voltage, the steepness of the curve is constant, but the rectification relation is exponential, therefore a graph in a double logarithmical scale of input RF power versus rectified voltage must appear linear (as it can be seen in figure 5.4). For the given integration constant the resulting pulse times are shown in table 5.1.

Input power (dBm)	Time (ms)
-60	1.1
-65	2.8
-70	5.2
-75	6.8

Table 5.1: Discrete integrator measure results

This integration times are not yet acceptable for data rates of approximately 100 kbit/s as the generated pulse would outlast a single bit. Nonetheless, this measure shows that the rectifier produces different levels of DC voltage for variable input power. The optimization and performance tuning of the integrator can then be done while designing the integrated WUR.

5.2 Integrated Wakeup Receiver measures

The first measures on the RF frontend were aimed at defining the influence of matching on the rectification efficiency. Typical power matching is aimed at transferring as much power as possible from the source to the load. This does not care about voltage amplitudes. In this case, the input of the detector is a gate of a transistor or the Schottky diode self. The impedance is therefore highly capacitive. The antenna has typically $50\ \Omega$ impedance and good power matching from the antenna to the high impedance of the detector is very difficult with lumped elements. On the other side all measure instrumentations are designed for $50\ \Omega$ impedance, providing a referenced result. Measures show that there is no particular difference between power matching and connecting the antenna directly to the detector as a result in efficiency. This is explained by the fact that the rectification depends on the amplitude of the voltage at the input of the detector and not by the power of input signal. A voltage matching is therefore much more meaningful. This can be achieved for example by using an inductor that resonates with the input capacitor of the detector. In this way, the voltage amplitude of the detector is higher, resulting in more baseband amplitude.

Figure 5.4 shows the measured results of DC voltage produced by the Schottky rectifier as presented in figure 4.19. The so-called voltage doubler was realized with HSMS-2852 diodes from Avago Tech [8]. The double logarithmical scale of the graph shows the measured values of the produced voltage in relation to the used RF carrier voltage. This rectification was not influenced by the power matching and as a matter of fact a reasonable matching of -16 dB was achieved for

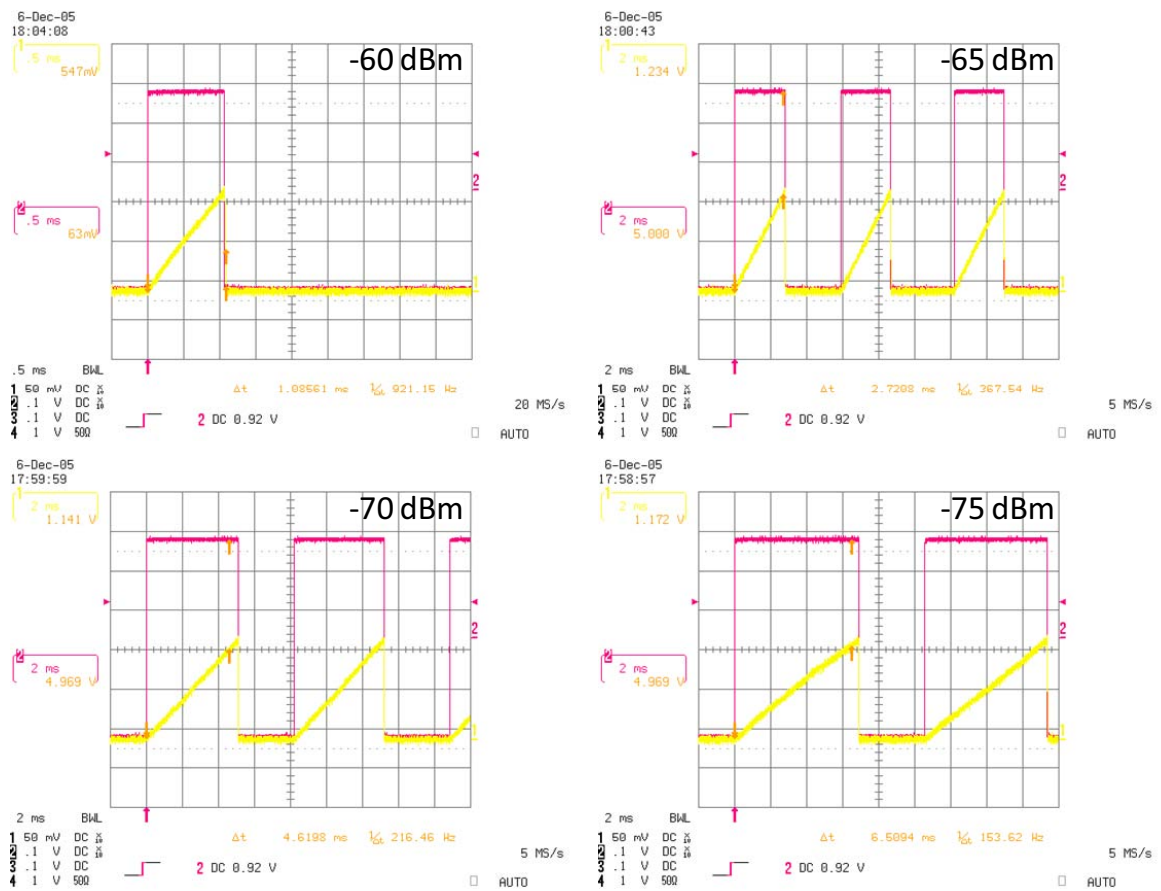


Figure 5.3: Integration pulse times for different RF power levels

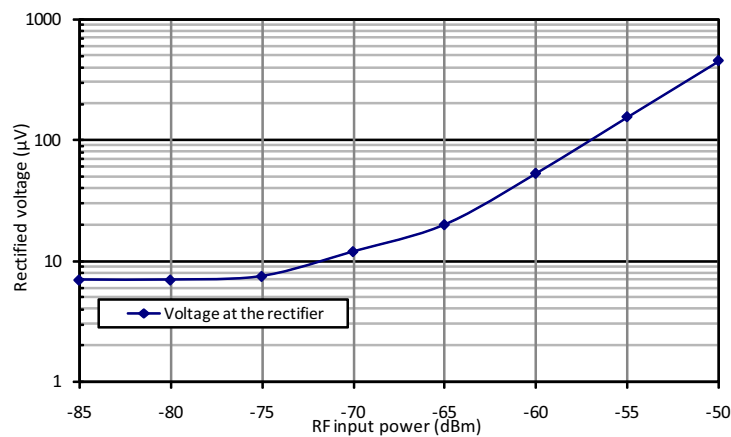


Figure 5.4: Schottky detector voltage

2.41 GHz as figure 5.5 shows. As a result, the rectifier produces a DC voltage difference of $20 \mu\text{V}$ for -65 dBm input carrier power coming from 50Ω source. The power matching was measured using a standard network analyzer also equipped by a 50Ω impedance.

This measure for the integrated detector is not straight-forward as in the discrete implementation.

This is given by circuit and noise problems. The integrated circuit does not have an output pin connected directly to the output of the detector because of pin number constraints and because of parasitic load of the eventual output driver, which has to be big enough to drive a $50\ \Omega$ line and have a very low noise figure. Both these constraints are adverse to the implementation of a buffer for the detector; therefore it was chosen to realize the measure by the means of the amplifier stage already available on chip. The amplifier chain is available on-chip both with and without the detector. In the version without the detector, it is possible to characterize in matter of gain and noise because of the direct access to input and output pins. As the two chains are physically very near on-chip, it can be assumed that both have equal characterization and therefore the produced voltage of the detector can be calculated subtracting the gain of the amplifier chain. To measure the efficiency, the signal stimulus is a 100% AM modulated sine at 100 kHz at the carrier frequency (e.g. 2.4 GHz). After the RF detector the RF component is removed and only the 100 kHz sine is amplified through the gain stages. The gain stages are characterized and the total gain is measured, therefore it is possible to calculate the amplitude of the signal after the RF detector. The spectrum analyzer is used to measure with great accuracy the amplitude of the demodulated sine. The results show that the MOS detector has a better efficiency but this is attributed to better matching as the nonlinearity of the diodes exponential and higher of the nonlinearity of the MOS transistor (even in weak inversion).

Figure 5.7 shows two different measures of the efficiency of the rectifier. The *MOS* labelled curve represents the integrated RF detector and the *Schottky* labelled curve represents the external Schottky diode detector. The 1:1 curve shows ideal rectification, where the DC level at the output is the peak amplitude at the input. This measure was realized with an RF signal generator and a Spectrum analyzer. The measure shows that the MOS detector is approximately 5 dB better

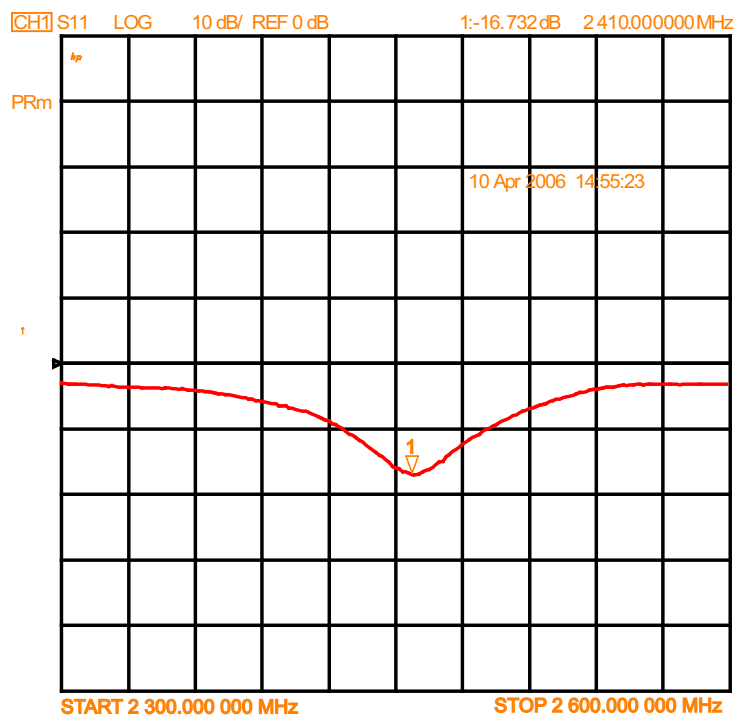


Figure 5.5: Reflection Loss of the Schottky detector

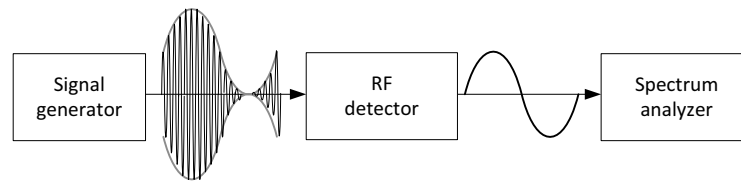


Figure 5.6: Block diagram of the detector efficiency measure

than the Schottky detector, but this must not be mistaken with actual efficiency, it is given by the fact that the external voltage matching was better for the MOS detector as for the Schottky diode detector, which is more difficult to match as it has a relatively high resistive component in its equivalent circuit [8]. The curves show very well how the detector works under high non-linearity condition, but the drawback is that the amplitude of the demodulated signal decreases more rapidly than the input signal, further worsening the sensitivity.

Figure 5.8 shows the single-ended gain of the amplifier chain measured with a network analyzer. As the chain is actually fully differential, the results must be corrected by adding 6 dB for full-differential gain. The figure shows two curves, the blue represents the full gain and the red one the lower gain that results by tuning the amplifier chain. This was provided to prevent possible clipping of the internal noise that reduces the performance of the amplifier. This measure is done on the chain without the detector by the means of a network analyzer able to measure signals from 100 Hz. The amplifier chain was designed to allow a flat response between 100 Hz and 1 MHz, in order to leave free choice for the appropriate bit rate of the wakeup signal. The measured frequency response is nearly flat for all the required range and therefore allows analysis of the performance of the digital receiver from 0.1 kbit/s to at least 500 kbit/s.

Using a reference input level from the generator, the bandwidth of the complete MOS-detector and amplifier chain has been measured using the same setup as for the detector efficiency. The frequency sweep shows that the MOS detector affects the bandwidth by shortening it on both low and high side. The result is a bandpass between around 2 kHz and 400 kHz. These results (shown in figure 5.9) are then used to extract the noise value of the detectors and of the amplifier chain.

Figures 5.10 and 5.11 show the measured noise from both detector-amplifier chain and amplifier

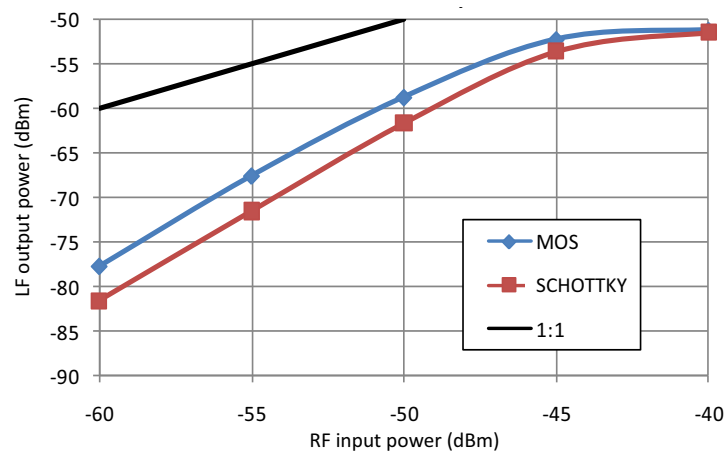


Figure 5.7: Detector efficiency

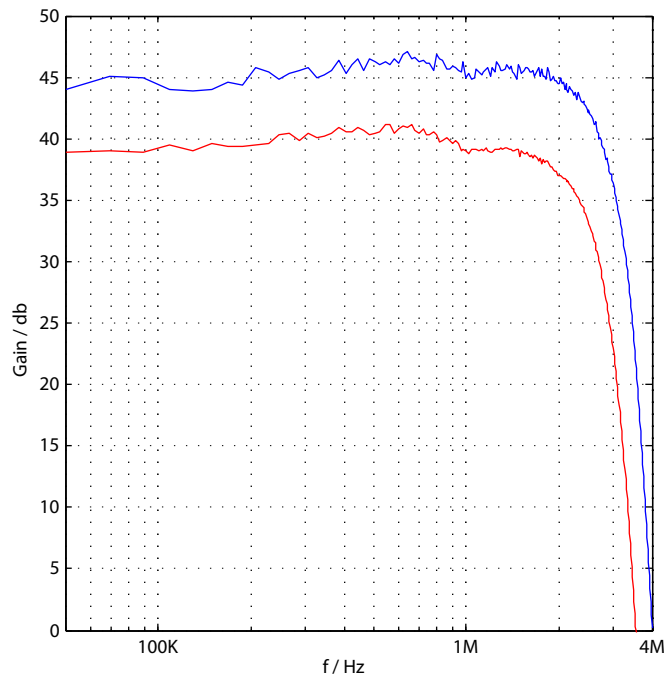


Figure 5.8: Single-ended gain of the amplifier chain

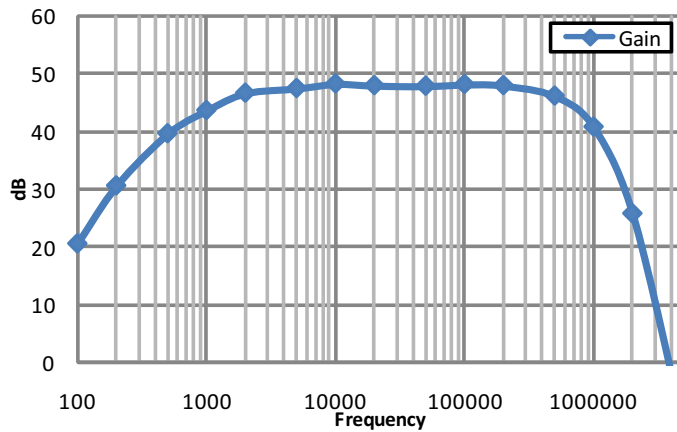


Figure 5.9: Gain and bandwidth of the amplifier chain

chain alone. This measure is done with a spectrum analyzer used with an RMS detector. Figure 5.10 shows two curves: the noise measured at the output of the chain and the noise corrected by the gain as measured and shown in figure 5.9. This represents the equivalent noise source of the circuit calculated as input source. The results show the typical flicker noise of MOS transistors in the lower frequency (represented by a negative coefficient line) that disappears afterwards in a horizontal noise floor. These results match the results given by the simulation tools, proving that the models are good enough to estimate noise levels of the process.

Figure 5.11 shows the same measure results for the amplifier chain that includes also the RF detector, that proves to be very noisy adding at least 10 dB in all the interesting frequency range (i.e. between 10 kHz and 500 kHz). This is a result of the MOS detector being biased with ultra-

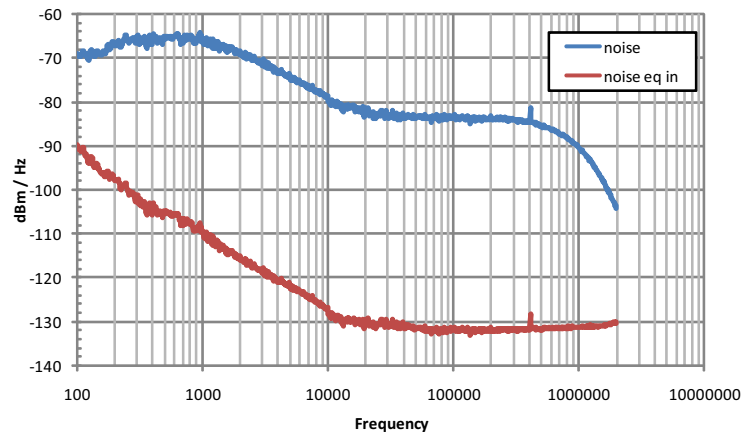


Figure 5.10: Spectral noise density of the amplifier chain

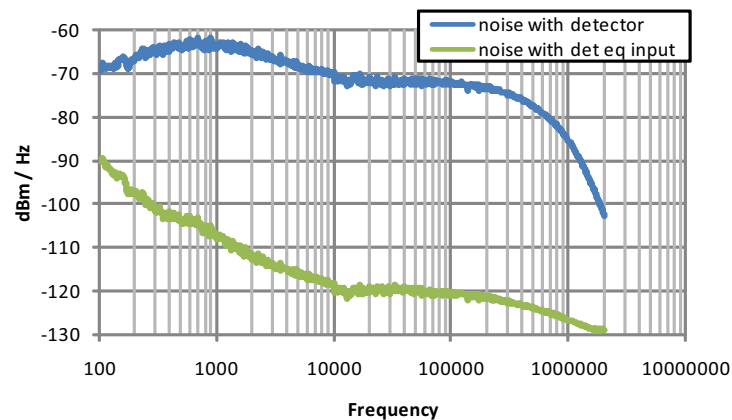


Figure 5.11: Spectral noise density of the detector-amplifier chain

low currents (around 100 nA) and therefore being in weak inversion. This results then in the key factor that influences the sensitivity of the complete receiver. Also in this case, the equivalent input noise shows the typical pattern composed by flicker noise and constant noise as the internal detector is also composed of MOS transistors only. 10 kHz These measures show that the internal MOS rectifier is adding a lot of noise to the analog signal processing. This worsens the sensitivity of the receiver although the efficiency of the detector is higher compared to the much lower noise of the Schottky detector. The measures also show that the signal band below 10 kHz is not appropriate for the wakeup signal, because of the strong noise that populates them. This noise cannot be reduced as it is intrinsic to MOS circuits. The only way to reduce this noise would be replacing the MOS process with other technologies, which in turn are not so economically advantageous.

5.3 Figure of merit for the wakeup receiver

The Bit Error Ratio (BER) is the typical figure of merit to qualify a digital receiver. This error ratio is the number of bits incorrectly received to the total number of bits sent during a specified

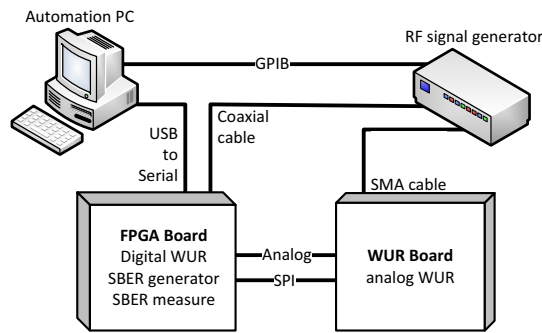


Figure 5.12: Figure of merit measure setup

time interval. For a radio receiver the input mean RF power that produces a BER value of 10^{-3} is usually referenced as the sensitivity limit. The mean RF power is the arithmetical mean of the power of all symbols used by the digital modulation. The BER is computed simply counting the number of wrong bits over a certain significant amount of bits transmitted. To better characterize the WUR, a novel figure of merit is introduced. This figure is called Synchronized Bit Error Ratio (SBER) and is the ratio between the number of wrong bits per detected packet. The outcome is that the synchronization properties of the receiver are included in the figure, giving a better idea of the required power to successfully decode an incoming packet. This is realized with the receiver under test, a device that generates the signal and a device that measures the number of wrong bits. In this case, both the signal generation and SBER measure is done in the Field Programmable Gate Array (FPGA). The system is implemented completely in hardware and a personal computer is then needed for the automation of the measure.

The FPGA contains a block that generates the envelope (i.e. the baseband) signal for the RF generator. The RF generator modulates at 2.4 GHz the baseband signal at a defined power level (e.g. -60 dBm). This signal is fed with an RF cable to the analog WUR realized on chip. The FPGA contains also the digital WUR that demodulates the signals coming from the analog WUR extracting the data from the packet. The extracted data can be compared to data transmitted as everything is generated inside the FPGA. A WUR packet contains 16 bit address and 24 bit data. A complete measure transmits 10^6 packets with same destination address and pseudo-random generated data (each packet contains different bits) such that the resolution is at least a SBER of 10^{-6} . As packet time length is around 1 ms and some delay between two packets must be allowed for the receiver to turn back to the idle condition, a time around 5 minutes is needed for one test. Under these conditions of bit length of the packet, number of transmitted packets and measure time, it is possible to reach a reasonably confident measure of the SBER. The PC is able to automate the measure by controlling both the generator and the FPGA. In this way, no manual control of the repeated measure is needed if the SBER must be recorded in relation to the input RF power. The PC sets the desired power on the generator (via standard measurement instruments' bus), the FPGA generation of packet is started (via serial link to the computer), the computer polls the FPGA to check if all packets are transmitted and finally the PC gets the measured number of failed bits. The whole process is started again for another RF power.

As the WUR is actually asynchronous to every sender, there is no possibility to measure the real SBER without external synchronization of sender and receiver. To overcome this problem, a digital SBER measure device has been developed on the FPGA as a complex block separated from the WUR but with access to it. This measure is actually between a packet error rate and

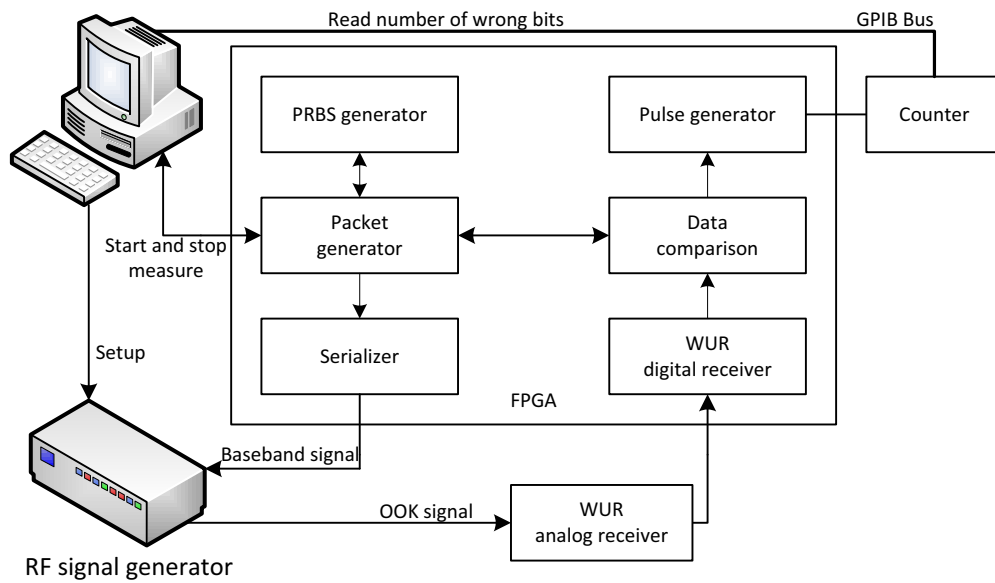


Figure 5.13: Detail of the FPGA SBER measure setup

a pure bit error rate because if the packet does not allow synchronization then the bits are all counted as wrong. This seems to be a better figure of merit of the receiver as the packet error rate because this contain less information on the effective data errors, and it is not a real figure of merit for wireless communication the measure of a pure SBER, because it does not account for the synchronization needed by each packet. The complete measure is regulated by a state machine the repeats the single measure in the following sequence, after the setup of all measure and generator instruments as well as the WUR:

1. Setup frequency and power of the RF signal
2. Generate pseudo-random data
3. Create WUR packet with sync word and data
4. Add FEC bits to packet
5. Add preamble to packet
6. Generate the baseband signal that is needed by the RF generator
7. Wait for transmission completion
8. Read decoded packet from the digital WUR
9. If no packet is received mark all bits as bad
10. If packet was successfully decoded extract data and compare with transmitted data
11. Generate the number of pulses equivalent to the number of bad bits
12. Read from the external counter the number of bad bits
13. Save data in a spreadsheet

14. Start next measure if not yet finished

These measures are accomplished at the best frequency, i.e. at the frequency that produces the best SBER, therefore allows the sensitivity to be measured at its maximum. The WUR was also set up for the SBER measure with high gain and other configurations for the best results.

The results of this repetitive SBER measure can be found in figure 5.14. As it can be seen, the detector using a Schottky detector achieves better performance as the MOS detector equipped WUR. Recalling the efficiency measure shown in figure 5.7, that results in 5 dB better efficiency of the MOS detector over the Schottky detector, this appears to be contradictive. The noise measure shows on the other side that the MOS detector performs at least 10 dB worse (over the significative signal band) of the Schottky detector because of its active nature (although with very low bias current), comparing to the completely passive nature of the Schottky detector. As a result of these two factors, with the noise prevailing over the better efficiency, it is clear that the Schottky detector performance is better than the MOS performance reaching a sensitivity of -54 dBm compared to -50 dBm.

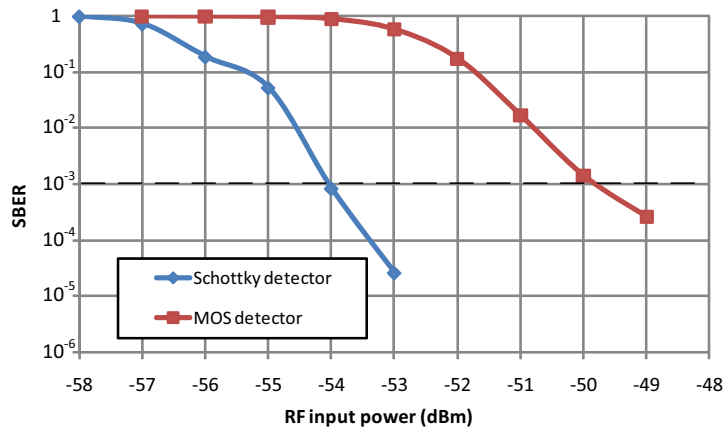


Figure 5.14: WUR SBER results

5.4 Data throughput and latency

The use of the protocol stack presented in section 4.2.2 yield also some experimental results on the potential total transaction time that can be needed by a single channel WUR equipped sensor node. Considering the 250 kbit/s transceiver used, and the Atmel microcontroller, the times for a complete transaction (RTS/CTS and 10 bytes data transmission and 2 bytes acknowledge transmission, considering also additional needed transmission bits) are shown in the following table: This results in a net data rate of 53.334 kbit/s if the channel is used allowing 250 μ s pause between each transaction. At this rate the sensor network could show a best-case latency of 1.5 ms per hop.

Considering the experimental results of the WUR and the usage of an efficient 1 Mbit/s transceiver as in section 3.3, the resulting transaction times are shown in the following table: This results in a total time of 1.84 ms per transaction that realizes a net transmission of 40 kbit/s allowing a 160 μ s pause between transactions. The resulting best-case latency for each hop is then of 2 ms, which if compared to actual scheduling MAC latencies in the rage of the second looks very promising.

Phase	Time (μs)
RTS	288
CTS	288
Data	488
Ack	192

Table 5.2: Latency of the protocol transaction

Phase	Time (μs)
RTS	840
CTS	840
Data	112
Ack	48

Table 5.3: Latency of the implemented WUR transaction

Latency is a function of much more parameters than packet length and therefore it cannot be simply calculated by the single hop delay multiplied by the number of required hops. As a WSN is intended to provide ad-hoc connection between nodes, i.e. the routing is not fixed, but calculated basing on environmental and energy information, the upper bound to the latency value (if it exists) can be calculated thanks to the analysis of the upper layers of the protocol stack, which are not focus of this work.

6 Conclusion and future work

The impact of using Wireless Sensor Network (WSN) in the many fields and applications that need environmental data acquisition will bring many benefits to its users, such as energy saving and better use of resources. The idea behind this is that the sensor node can be embedded in the environment because it does not need any cables to connect it to rest of the system. In this way the node can be freely positioned in the environment that has to be controlled by choosing strategic positions, not constraining the choice by the position of the cables. The concept of WSN allows the presence of many sensors that send different data on different measures to an entity that collects information and acts if necessary. The main task of the sensor network is monitoring, and secondly, taking action if required.

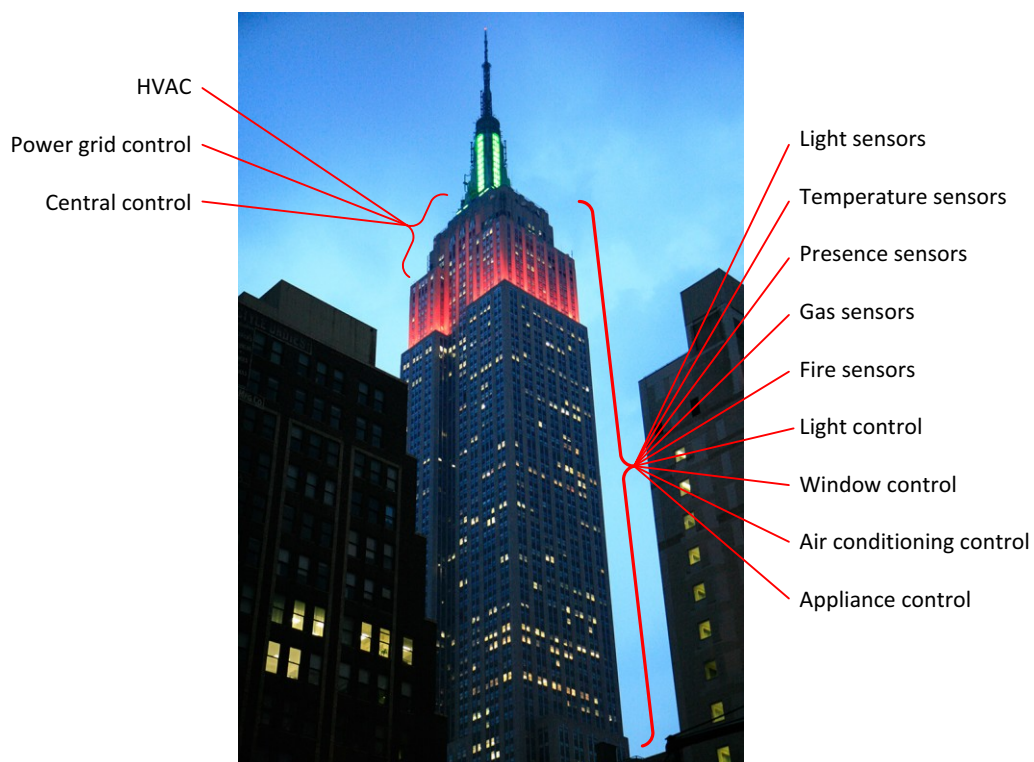


Figure 6.1: Example of building automation

Between the most common tasks that are associated to WSN the main application that could

benefit of WSNs are home or building automation (figure 6.1) due to the possible vastness of the network, car automation because of the many advantages of wireless communication, container tracking, battlefield monitoring and also home and hospital health monitoring. The amount of data that each node generates each measure is considered to be very low and the throughput of more than one generated packet per second can also be considered unusual. Nonetheless, a wireless sensor network can gain a lot in flexibility if each node communicates with the rest of the network in an ad-hoc fashion, meaning that each node can also act as a router to forward information from other nodes to the destination. Considering this and that the number of nodes can be relatively high, at least in applications such as building automation, it is clear that there is a lot of activity in a sensor network, and therefore enough energy is required to sustain it.

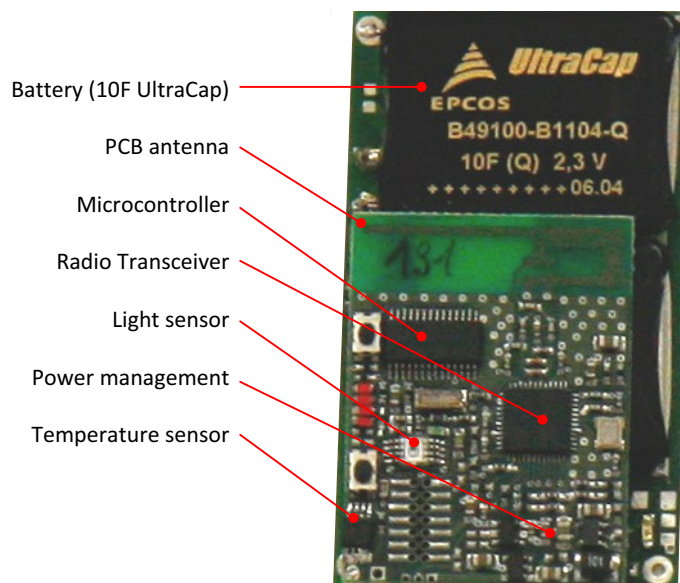


Figure 6.2: Example of wireless sensor node

The “unwired” nature of the sensor nodes (an example can be found in figure 6.2) means that the energy source is enclosed in a battery that can have many forms or different chemical compound, but is finally limited by the technology that is not progressing as fast as the electronic circuits. Other energy sources, known as scavengers, take energy from the environment and transform it in electrical energy. This is a promising field for wireless sensor nodes, but the harvested energy is still very low and therefore the node needs to consume very low energy if the sources have to be used. The energy demands for radio communication do not allow constant listening to the channel; otherwise the battery would drain in days, if not in hours.

The main problem that prevents wireless sensor networks being produced and sold widely is not reliability or robustness of the protocols, but the life expectancy of the node relying on an energy source with reasonable dimensions and costs (i.e. those of the electronics of the sensor node). Of course, the dimensions of the energy source is not a limiting factor for all applications that would use a wireless sensor network, but the most important fields such as building automation or car automation do have strict constraints in matter of weight and physical dimensions. As there is no projected increase in energy density for batteries or harvesting capacity to rely on, the problem must be tackled from the other side: average power consumption must reduce to levels that allow a long life of the single nodes and therefore of the network.

Most of the research in lowering power consumption of sensor nodes focuses exactly on reducing the energy needed for the communication, which is for the radio and its control. The most common strategy to accomplish this goal is to turn on the radio only for the strictly needed time and then to turn it off for the majority of the time. This reduces power consumption of the radio to a fraction of it depending on how long the radio is inactive, such that the ratio between on time and off time is the factor that multiplied to the active power consumption gives the resulting consumption. This is of course a very simple way to reduce power consumption to the required value, but brings a lot of disadvantages too.

Using this periodical strategy, which means controlling the synchronized start and stop of the radios of the nodes following a certain schedule, does require a good precision in timing otherwise the drift of the clocks would prevent after a certain time the communication of two nodes, as their active times would never meet. To prevent this, the strategy is to start the radio (to wake up) often enough, to maintain at least synchronization, if no data needs to be exchanged. Of course, the number of packets that can be processed per wake up period is limited, otherwise the system would not be periodical anymore. Here comes the first disadvantage in such protocols: that is the hop-to-hop delay that is directly related to the period of the protocol and to the maximum number of processed packets per active period (usually limited to a single unit). So if we consider a mean delay of 1 s and the packet must go through 100 nodes to reach its destination, then the general latency will be in the range of the 100s which could not be a very long time, but very long compared to actual transmission times.

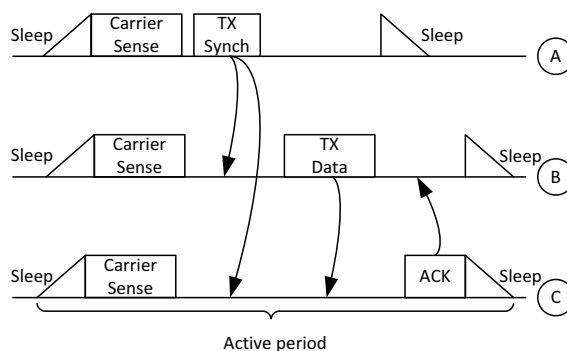


Figure 6.3: Simplified scheduling MAC approach

What is called a scheduling MAC approach is, as described in the previous paragraph and shown in a simplified manner in a three node network in figure 6.3, a way to reduce the power consumption paying in increase of the latency of the system and data throughput. This happens because the periodicity acts as a balance and reduces power consumption only if the latency is increased, which is indeed a limiting factor to the application of wireless sensor networks, at least in some application fields such as building automation. Many publications are available in the literature (see [EHD04], [SS07] and [MB04]), where the synchronization efficiency is maximized and the utilization of the radio is minimized. The power consumption is reduced to very low levels, but still the nodes wake up periodically although no packet must be sent or forwarded, actually wasting energy. This implies that if the traffic is generally low, energy is needed keep response times in a reasonable range.

To prevent the unnecessary periodical wakeup the literature propose to use a radio receiver (see

figure 6.4) that can be always active and consumes ultra-low power ($< 1 \mu\text{W}$ in [LSGR01]). This receiver is used to build remote wake up mechanisms that are able to activate the main radio to communication of a node and is called a wakeup receiver. The advantage of having such a receiver is that the node can be set in a deep sleep mode and woken up only if another node requests communication or if the sensors require a measure. As there is no periodicity in the wake up times the nodes do not need to be synchronized, at least for communication purposes. The wakeup receiver makes the nodes always available to communication supposed that the channel is free. If a node wants to forward a packet to another node, it sends a request on the wakeup channel and then sends the packet over the main data channel, which is more robust and much better performing than the wakeup channel. The latency of the packet and the mean hop time are not bound to the periodicity anymore, but lie in the range of the transmission time. This makes the network much more responsive and opens up the use to much more applications. The resulting throughput also increases because there are no more constraints in the number of processed packets per period. Of course, this means that the upper bound to power consumption can reach high levels if a node is highly active, but a periodic system would create a bottleneck in this case. Considering that a node is projected to be inactive most of the time, the wakeup receiver solution achieves fast response times by consuming ultra-low power consumption.

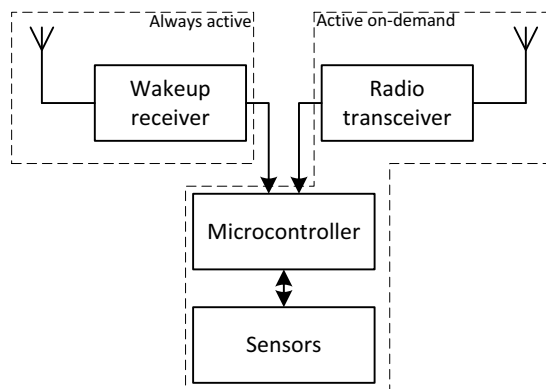


Figure 6.4: Proposed architecture

The goal of power consumption below $1 \mu\text{W}$ is still far to be reached. There are some attempts to realize the wakeup receiver in chapter 2 which are the base upon which this work is built. The fundamental idea is to move back from frequency modulation to amplitude modulation because the latter can be demodulated even with a passive circuit, which is a very interesting starting point if the power consumption is the main factor in the building of the wakeup receiver. After the demodulation, there are several different approaches to the analog and digital processing needed to extract the information of the packet. Some propose to digitize with an Analog to Digital Converter (ADC) and then elaborate with a Digital Signal Processor (DSP). This is complex and not an energy saving choice as the DSP requires a lot of energy if many calculations must be done to decode the incoming signals. If few calculations are needed, then simple logic consumes surely less than a complete DSP core. Other approaches require a simple state machine to decode the signal but then need very strong transmission signals to activate successfully the decoding logic. This is a problem that has not been circumvented yet as the efficiency of passive or nearly-passive amplitude demodulation, actually On-Off-Keying (OOK), does not provide high sensitivity as frequency demodulation could achieve.

The proposed solution is the architecture of the two (the Medium Access Control (MAC) layer

Detector	Power @ 100 kbit/s	Data rate (kbit/s)	Sensitivity (dBm)
MOS	12.5 μW ¹	1...250	-50
Schottky	11 μW ¹	1...250	-54

Table 6.1: WUR measured performance

and the physical layer) lower levels of the protocol stack for the single sensor node. The MAC protocol provides access to the channel by implementing an RTS-CTS mechanism via the wakeup receiver channel, which is always active. The nodes are all addressed and the wakeup mechanisms can wake up a single node or all the nodes in the range of the transmitter by choosing an adequate broadcast address. One additional byte of information can be added to transmit other parameters for the data transmission such as the proposed sending channel. The receiving node answers a CTS request with the confirmed channel and then starts the main transceiver. The physical layer is realized by a main radio capable of receiving and also transmitting large amounts of data in the data channels with high speed and high sensitivity and is capable of transmitting RTS requests on the wakeup channel. The physical layer is extended by the presence of a wakeup receiver which consumes ultra-low power (with a goal around 10 μW) by being always active receiving incoming packets. The information contained in these packets is relegated to source and destination addresses and one additional byte for other handshake information.

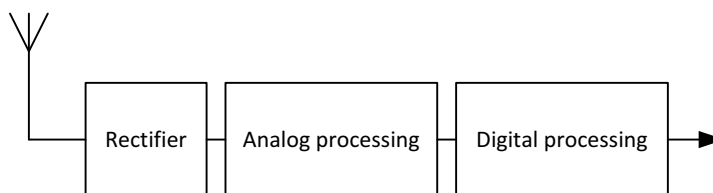


Figure 6.5: Wakeup receiver block diagram

The actual wakeup receiver architecture (as depicted in 6.5) is very simple OOK receiver as this is a very power saving architecture, as any block that handles signals in the Radio Frequency (RF) band are avoided. This receiver does not need mixers or oscillators. The RF signal is down-converted at the very beginning of the signal path directly to base band, by the means of an energy detector circuit. The energy detector is also called envelope detector or rectifier, alluding to its implementation that converts oscillation to DC levels. This stage is very critical to the receiver because the sensitivity and robustness depends primarily on it. The realization is done with a simple diode-like function given by the transistors of the CMOS technology. The signal produced by the rectifier is then processed by an analog chain that has to consume less power as possible. This implies that not much elaboration is done in the analog domain, as the digital domain can achieve much better results in enhancing the overall sensitivity of the design.

The implementation was realized in a 120 nm CMOS technology provided by Infineon Technologies. The output is a stand-alone wakeup receiver design which can be added to existing sensor nodes systems or used as a macro block and inserted in advanced SoC projects. The result of the integration of the Wakeup Receiver (WUR) has been compared to the performance of the other ultra-low power receivers available in the literature. The results are shown in the previous sections as in table 6.1 and show that the proposed WUR consumes way less energy than any competitor but needs improvements in the sensitivity.

¹Equals the measured power of the analog receiver and 5 μW simulated power of the digital receiver

To help the visualization of the results shown in table 6.1, some comparison graphs are presented in figure 6.6 and 6.7. These graphs show a comparison of the proposed architectures as cited in chapter 2 and this work. As power consumption is identified as the key parameter to this work, it is taken as the comparison figure. The first proposed comparison displays the power consumption

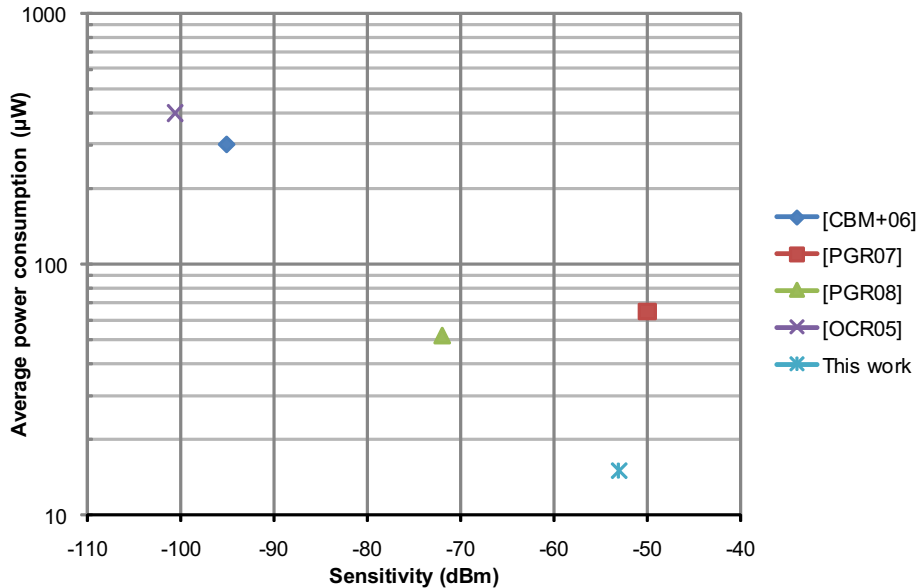


Figure 6.6: Power consumption vs. Sensitivity

related to the sensitivity of the design. This work achieves better power performance as any other receiver, but the sensitivity figure has still to be improved, if the receiver has to be used in real world situations, where a sensitivity of at least -70 dBm is required.

The comparison proposed in figure 6.7 relates power consumption to data rate. This comparison bears in mind that the node sending a wakeup message uses energy that can be saved if the transmitter is used for short times. Very low bit rates imply long use of oscillator and power amplifier that are costly to the power supply.

The current limitations of this work are that the sensitivity is not as high (due to the detector efficiency). The envelope detector is the most important block of the receiver. It converts the RF signals to the baseband directly and is therefore directly responsible of the overall sensitivity of the receiver. The detector must be optimized for bandwidth, efficiency and noise. The first factor can be optimized by using external passive filtering with very high quality factors (such as MEMS resonators). The efficiency is a purely circuital and biasing matter, that must be inspected very carefully, as the power consumption must be kept low but the efficiency must be maximized. Other circuit topologies than the ones used, should be considered to achieve the goal of raising the efficiency of the detector. The noise that the detector generates is also a limiting factor to the overall sensitivity of the receiver. This is both a technological aspect, meaning that the chosen CMOS technology influences very much the result and a circuital aspect because again bias and topology influence the produced noise, which is higher at lower frequencies in CMOS circuits due to Flicker noise.

The analog processing blocks must be optimized in matter of bandwidth, which reduces the overall noise generated by the amplification of the signal of the detector. The bandwidth was left

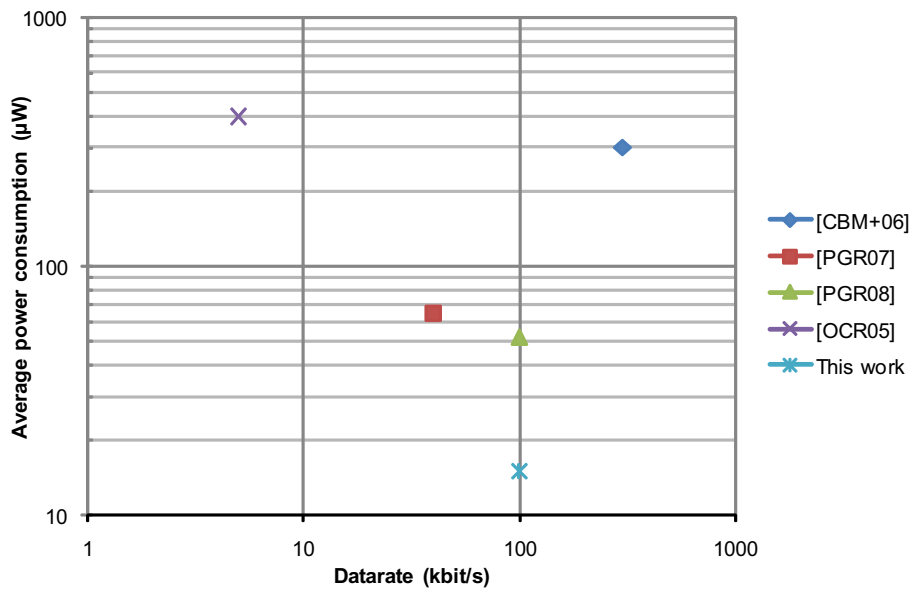


Figure 6.7: Power consumption vs. Data rate

large enough to test with different data rates but in an optimal design it should fit exactly the incoming signals and nothing more, also reducing interference from other transmission in the RF band.

The digital processing can be enhanced to achieve a better correlation if the symbol length is extended or if the number of symbols is increased to 2 or more. This results in a better capacity of the receiver to extract information from the noisy output of the analog chain. This could be an interesting approach if the analog chain could not be further enhanced. Another important point in the digital signal processing is the synchronization to the incoming packet because no data can be retrieved in case of wrong synchronization. The algorithm that governs synchronization is fairly simple in this implementation and therefore is also a good candidate for enhancement.

If the WUR sensibility can be reduced to -90 dBm and below the concept of WUR could fade transforming it to a main receiver. Changes have to be done also to the modulation scheme as OOK is not optimized in bandwidth and robustness. The modulation scheme should move from amplitude modulation to frequency modulation although this implies a great lowering of the power consumption of the building blocks such as Phased Locked Loop (PLL) and mixer which has not been achieved yet. Such a receiver (FSK and power consumption below $10 \mu\text{W}$) could start the revolution of the world of the WSNs because energy costs would be cut to minimum. All the interesting scenarios such as car-to-car communication or intelligent building automation would be achievable at lower costs than with present state of the art technology.

The first scenario in which a wireless sensor network fits well is the home of the future: the intelligent home. The intelligent home, as already imagined by many book and film writers is capable of controlling itself and letting the human being control the whole house in a centralized way. Of course the primary task of the intelligent house would be the reduction of the energy consumption of the house. The control of the air conditioning is the first example where a control on the temperature, humidity and human presence in a room can be used to decide if and how strongly (or weakly) must cool or warm air be pumped. If we consider that the system can direct the air flow there where there is a presence, this can reduce the consumption for all rooms where

a strict control of the climate is not necessary. The same can be done with light, which could be activated and deactivated basing on information that relate to human presence, time of the day (or night). So it would be possible to turn off the light in the garage if the car is parked and no human has been detected in the last few minutes. In the house, there is also a need of tight control on security related issues: if gas is used as energy source for warm water or for cooking, sensors could be spread in the house to detect gas escape, or at least to give pre-warning, if we assume that security sensors would still be wired. Other interesting features of home automation would be the control of all the material that is needed by the inhabitants. The network could control the need of taking the garbage outside, or tell the owners that milk is at the end. It could be even possible that normal appliances embed wireless sensor nodes that notify the users or even the technician is something has to be replaced or repaired. This would require as sort of pairing such as in Bluetooth networks when a new device is brought home. Of course, the main control would be on the power supply of the device, to automatically turn off the television set if it still runs at night and the viewer has fallen asleep on the couch (and does not move, which is a detectable event).

A similar scenario is provided by building automation, where modern skyscraper buildings or offices are meant, but also industrial location. There are some attempts to analyze the industrial application presented in [OPR⁺07],[AMT05] and [SWS04]. The challenge provided by these environments is the vastness of the network because of the many rooms each floor and many floors. Due to the huge surface to be controlled, using a cabled network implies the use of kilometers of copper which is expensive and also heavy. A wireless network would also be easily deployed in already built constructions, as it is not the case for a wired building automation. Between the many tasks that building automation has in common with home automation, there are some tasks that are provided by the large scale of the building. Many rooms and centralized air conditioning could be controlled such that less air conditioning is used where no presence is detected. Another interesting task could be the reduction of the overall energy consumption of the building, based on measures of the consumption or messages from the grid authority. In this way, great peaks of energy consumption can be kept under control. Lighting in a big building is as important as air conditioning control; a network could ease the job of reducing energy consumption. Creating an efficient and flexible system for access control to offices and flats could be easily added to an existing building without the need of new cabling shafts.

In the huge cities of today, the task of controlling the highly complex traffic roads is a task that at the moment is far to be at its optimum, congestions are everyday's experience and this adds to the already high pollution of the air. A sensor network that detects where the major traffic is going and is able to interact with the traffic control could enhance the average speed of transit of the vehicles. This would also help reduce traffic jams and pollution given by the cars traveling at very low speed. Such a network would need a fairly extended amount of sensors particularly near street crossings. Such an extended network would be impossible to realize with cables because of its requirement for kilometers of connections, which is surely economically not reasonable. A wireless network would not have the problem of costs of the cabled connection and could also interact with the sensors equipped in the vehicles.

As the world population is aging and the life expectancy is rising, another interesting scenario for wireless sensor networks is represented by health care. Two interesting applications could make the control of ill patients much easier and efficient. The first would be the embedding of sensors in the houses of the patients, such that patterns can be recognized in ordinary life. If a patient is making coffee each morning at 7 o'clock and the coffee machine is not running, and the sensors in the bed reveal that the patient is still laying, this could prepare the central medical service

for an eventual emergency. On the other hand, many sensors could be hidden in clothing of the patient such that he can move freely and still measure important items, such as pulse rhythm or blood pressure. When the patient is back home, the data could be transferred to data server and forwarded to the medical system, otherwise the patient could go in the hospital and the relevant data could be accessed directly on-site by the medical responsible.

A very high number of containers are moved each day by train, ship or plane, but it is almost equivalently unbelievable how many containers are stolen or emptied of their cargo. This is of course a very important issue for the business of cargo transport. The security of the transportation of goods could be dramatically improved by tracking the trip that each container does and crosschecking it with the planning route. The sensors would of course need to be wireless so that the container is able to connect to the infrastructure where it lies or use a cellular network in the case that no other network is available. The sensors should control the internal temperature or other environmental parameters if it's important for the transported goods. A Global Positioning System (GPS) sensor is required to track the position and of course intrusion detection is also very important. The last presented but still very interesting scenario where wireless sensor networks would bring great improvement in functionality or great energy savings is car-automation. Today's cars are already equipped with a lot of sensors and luxury class models have a lot of sensors for non security critical tasks. The car of the future could be full of this extremely low cost (because of the mass production) sensor to increase the comfort and ease of utilization of the vehicle. One sensor system that has already come to the market is the Tire Pressure Monitoring System (TPMS). This helps to prevent car accidents by advising the pilot of a flat tire or of decreasing tire pressure. There are a lot of other sensors in the cars that could be successfully replaced by wireless sensors. One good example is the sensor for seat presence, which is usually coupled to a message to fasten the seatbelt. Another application would be air conditioning control of the car's cockpit. All these sensors require a lot of cabling (except for TPMS) and are of course consuming energy from the motor to work.

Another interesting scenario in car-automation with wireless sensor networks is represented by car-to-car data exchange. This application could produce unprecedented efficiency in traffic control by letting the cars communicate with each other. If somewhere a traffic jam is identified, the message could be spread from car to car and to or from the traffic management to inform the drivers. Driving on a highway, the cars could pass messages that inform of an accident or crash ahead and tell the drivers to pull-out or to modify their route. Changing lanes is always been a potential accident source and this could be prevented by notifying the presence to other surrounding cars.

All of these possible scenarios are at the moment too expensive to realize either because a wireless sensor network is unable to live long enough or because the utilization of a wired solution is not practical or too expensive. The introduction of the wakeup receiver in the sensor node system allows the sensor nodes to live much longer relying on restricted energy sources such as batteries or solar panels.

This work (a die photograph is presented in figure 6.8) presents a complete solution for lowering power consumption in nodes of wireless sensor networks. The solution is both hardware and software covering the MAC and physical layer of the communication system. The solution is presented bearing in mind that the hardware is integrated in a system-on-chip or at least system in-package. The hardware is a mix between full-custom analog and semi-custom digital circuit. In this way, ultra low power consumption can be reached. The usage of such a receiver has also a very important effect of reducing hop-to-hop delay and therefore overall latency. A MAC protocol

that is paired to the architecture with a main transceiver and a wakeup receiver is also presented. This enables such a system to be integrated seamlessly in existing solutions.

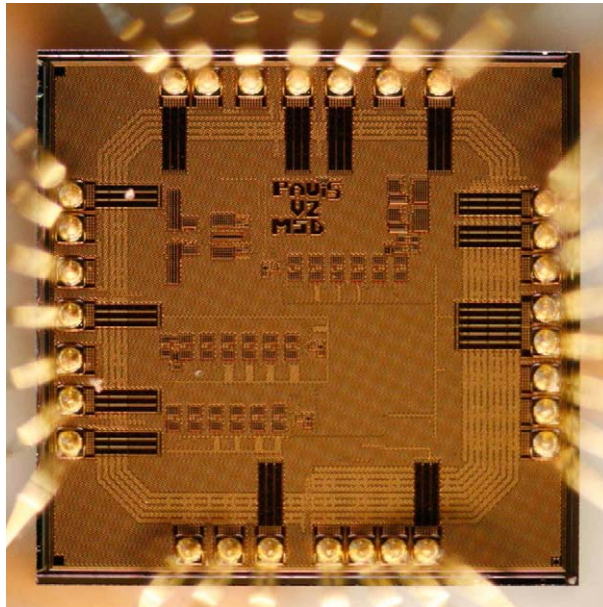


Figure 6.8: Die photograph of WUR

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