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Interface Characterization Methods and Properties of GaN Metal-Insulator-Semiconductor Structures

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Korea, with all its characteristic and cultural facets

Abstract

This work presents a detailed study on the characterization methods of the interface properties of GaN-insulator structures for several dielectric materials. It is an pre-study for the purpose of fabricating inversion metal insulating semiconductor field-effective transistors (MISFETs) based on GaN, which are believe to have higher breakdown and current capability than those of other materials, due to the wide band gap related properties of GaN.

The focus is divided into a theoretical discussion about the characterization methods, the fabrication, the measurement and the analysis of MIS structures based on the interface properties and the field-effective mobility measured by Hall measurement and extract from Schottky transistors. As characterization methods, capacitive measurement with over band gap UV light has been used to study the interface charge induced flatband voltage shift and was compared to conductive AC measurement for extraction of the interface state density. The investigation of p-type and n-type substrates allowed a characterization over the whole band gap. Due to the lack of inversion ability in the samples the field effective mobility was extracted from accumulation in enhancement device structures.

As dielectric materials silicon nitride and silicon oxide deposited by plasma-enhanced chemical vapor deposition (PECVD) where compared to aluminum oxide from atomic layer deposition (ALD) under certain annealing conditions. Amorphous aluminum oxide has several advantages as a high dielectric constant, a high energy barrier and a high breakdown field, but shows a lower thermal stability only up to around 800°C.

The capacitive analysis was based on virtual-ground MIS devices in order to remove any distortion effects by not perfectly rectified ohmic contacts, which was necessary on p-type

GaN. It resulted into symmetric interface state distribution over the band gap with a maximum at the band edges. Aluminum oxide showed the best performance with an interface state density below $2x10^{11}$ $cm^{-2}eV^{-1}$ in the middle of the band gap and below 10^{12} $cm^{-2}eV^{-1}$ at the band edge after thermal treatment in nitrogen ambient. Silicon oxide interfaces showed similar behavior but less effect on annealing.

For p-type substrates high interface density were observed depending on the epitaxially grown substrate. The interface characteristics were generally less dependent on the dielectric or surface treatment due to the defects from the grown bulk material which could be shown by comparison to photoluminescence measurement. Inversion carriers were not observed using Schottky barrier MISFET devices. Further, capacitive study on p-type GaN, which is up to now rarely presented, is discussed with focus on the high series resistance due to the low mobility of holes in GaN. An accurate result was measured using silicon oxide with a minimum interface state density of $4x10^{11}$ $cm^{-2}eV^{-1}$ around the band edge.

The Gated Hall mobility was extracted from the carriers in accumulation and separated from the bulk carriers. The Hall measurement resulted in a field-effective mobility of 150 cm^2/Vs for silicon nitride in a bulk material with mobility around 300 cm^2/Vs. Similar configuration was measured for transistors with Gate lengths of 4 to 30 µm. The channel length dependent resistance was extracted and led to a maximum field-effective conductivity mobility for silicon oxide of 50 cm^2/Vs, while silicon nitride and aluminum oxide showed mobilities around 15 cm^2/Vs.

GaN Metal-Insulator-Semiconductor 구조의 계면 특성화 방법과 특성

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(초록)

본 논문에서는 GaN 절연체 구조의 계면특성 분석을 위한 특성화 방법에 대하여 세부적인 연구를 보여준다. 이 연구는 GaN을 기반으로 한 Inversion MISHFET (metal insulating semiconductor field effective transistors)를 만들기 위한 예습이라고 할 수 있다. GaN를 기반으로 한 물질의 특성은 다른 물질들 보다 넓은 에너지 갭을 가지기 때문에 높은 항복 전압과 전류용량을 가질 것으로 기대된다. 중요내용으로는 특성화 방법에 관한 이론적인 논의, 제작, 계면특성을 기반으로 한 MIS 구조의 측정 및 분석 그리고 홀 측정법으로 구한 Field-effective conductivity로 구성이 되어 있고, Schottky transistors를 이용하여 측정하였다. UV light에 대한 band gap의 용량성 측정 특성화 방법을 위해 flatband voltage shift로부터 야기된 계면 전하와 계면 전하 밀도의 추출을 위해 비교된 전도성 AC 측정에 대하여 연구를 하였다. 측정은 공핍 소자에서 반전의 결핍으로 인하여 향상되었다. 절연물질로서 PECVD (plasma-enhanced chemical vapor deposition)으로 길러진 Silicon nitride와 Silicon oxide는 일정한 조건에서 ALD (atomic layer deposition)로 길러진 Aluminum oxide와 비교 되었다. Aluminum

oxide는 높은 절연상수 같은 많은 장점을 가지고 있지만 800°C에서는 낮은 열적 안정도를 보여주었다. 전기적 용량의 분석을 위하여 가상 접지 MIS 소자를 사용하여 완전하게 정류된 저항성 접촉에 의한 왜곡 영향을 제거 하였다. 결과적으로 밴드 가장자리에서 밴드 갭에 대하여 대칭적인 계면 상태 분포를 보여주었다. Aluminum oxide는 밴드 갭 중앙에서 $2x10^{11}$ $cm^{-2}eV^{-1}$ 이하의 최대 계면상태밀도를 보여주고, 질소 분위기에서 열처리 후에는 밴드 가장자리 부근에서10^{12} $cm^{-2}eV^{-1}$ 의 결과를 보여주었다. Silicon oxide 계면은 비슷한 결과를 보여주지만 열처리 효과가 적은 것으로 보여졌다. 또한 p형 물질에서 계면 밀도는 에피택셜 물질에 따라 변화하는 것이 관측되었다. 보통 계면 특성은 bulk 물질의 결함에 의해 발생하기 때문에 절연물질이나 표면 처리에 의존한다. Schottky barrier 소자에 의하여 테스트 된 반전 전하들은 관측 되지 않았다. 지금까지 소개된 p형 GaN 용량성에 관한 연구는 낮은 홀의 이동도 때문에 나타나는 직렬 저항 문제에 관하여 보여주고 있다. Silicon oxide를 사용함으로서 $2x10^{11}$ $cm^{-2}eV^{-1}$의 최소 계면 상태 밀도의 정확한 결과가 측정 되었다. 마지막으로 field-effective conductivity와 Gated Hall mobility에 대한 결과를 요약하면, 홀 측정은 150 Vs/cm^2 의 Field-effective conductivity의 결과를 보여주었고, Bulk 물질에서는 약 300 Vs/cm^2 의 이동도를 보여주었다. 그리고 4~30um의 Gate길이를 가지는 transistors 에서도 비슷한 형태가 측정되었다. Silicon nitride와 Aluminum oxide가 약 15 Vs/cm^2 의 이동도를 가질 때 채널 길이의 변화에 따른 저항을 구할 수 있었고, 50 Vs/cm^2 의 Silicon oxide에 대한 최대의 field-effective conductivity를 이끌어 내었다.

Contents

Acknowledgement III

Abstract IV

초록 VI

LIST OF FIGURES X

LIST OF TABLES XIV

1. INTRODUCTION 1

1.1. GaN & Modern Semiconductor Devices 1

1.2. History of Inversion MOSFETs in GaN 3

1.3. Thesis Outline 4

2. TECHNICAL BACKGROUND 6

2.1. GaN Properties 6

2.1.1. Crystal Structure 6

2.1.2. Band Structures 8

2.1.3. Piezoelectric and Spontaneous Polarization 9

2.1.4. Typical Compounds of GaN 11

2.2. Gate Dielectrics on GaN 13

2.3. The basic MIS Structure 16

2.3.1. 2-Terminal Behavior of Gallium Nitride 16

2.3.2. Interface Properties 24

3. CHARACTERIZATION TECHNIQUES 26

3.1. CV Measurement in GaN 26

3.1.1. Capacitive Method 26

3.1.2. Conductive Method 29

3.1.3. Dynamic Behavior of Interface States 32

3.2. Hall and Gated-Hall Measurement 35

3.3. Characterization by Schottky Barrier Transistor 40

4. FABRICATION 44

4.1. Technology 44

4.1.1. Metal-Organic CVD 44

4.1.2. Dielectric Deposition 46

4.2. Device Processing 52

4.2.1. MIS Capacitor 52

4.2.2. Gated Hall Pattern 56

4.2.3. Schottky Barrier Transistor 59

5. EXPERIMENTAL RESULTS 61

5.1. Characteristic of CV measurement 61

5.2. Dielectric Characterizations 68

5.2.1. Silicon Nitride (Si_3N_4) 71

5.2.2. Silicon Oxide (SiO_2) 75

5.2.3. Aluminum Oxide (Al_2O_3) 82

5.3. Mobility Characterization from Gated Hall 86

5.4. Characterization by 3-Terminal Gated Device 90

6. SUMMARY & CONCLUSION 94

LITERATURE 99

SCIENTIFIC ARTICLES FROM THIS WORK 106

APPENDIX A: TYPICAL PARAMETERS OF GAN 107

APPENDIX B: MATHCAD CODE FOR CV CALCULATION 110

APPENDIX C: NUMERICAL CV SOLUTION 111

List of Figures

Figure 1.1: Application field of materials based on frequency and power performance 3

Figure 2.1: Crystal structure of wurtzite structure, typically used in GaN. Right side shows the N-polar phase which is exactly turn around of the Ga-polar phase on the left. 7

Figure 2.2: Band energy of conduction bands and valence bands in GaN based on theoretical calculation [22] (left). The right side shows the crystal directions based on the unit lattice cell. 9

Figure 2.3: Unit cell structure of zincblende (left) and wurtzite crystal (right). The polarization can be understood by adding up the vectors from N atoms to GaN atoms (white arrows)..... 10

Figure 2.4: Qualitative graph of the polarization based on the stress in the lattice perpendicular to the [1000] direction. The stress can be introduced by interfaces with III-N alloys. 11

Figure 2.5: Band gap energy versus lattice constant for the basic nitride materials (dots). Along the outside line of the triangle the band gap energy for possible compounds can be seen. 13

Figure 2.6: MIS structure and basic equivalent circuit of capacitors. For the ideal case the interface state capacitor is zero and only the semiconductor and oxide capacitor remain. 17

Figure 2.7: Qualitative band diagram of the MIS structure for accumulation and depletion19

Figure 2.8: Total calculated amount of semiconductor charges versus the surface potential of the semiconductor 21

Figure 2.9: Calculation result of the total Capacitor of the MOS structure (solid line), semiconductor capacitor (dashed line) and the constant oxide capacitor. 21

Figure 2.10: Calculation of the relation between surface potential and the Gate potential. In the depletion region both change linear. From the flatband voltage the surface potential does not change. 22

Figure 2.11: Calculation of the MOS capacitor (deep depletion) versus applied Gate voltage (solid). Again semiconductor capacitor (dashed) and oxide capacitor are additionally shown. 23

Figure 3.1: Energy diagram of the MOS structure at flatband condition (a), depletion

condition with incident UV light (b) and inversion (c). 28

Figure 3.2: Calculated CV Graph showing the Flatband shift induced by oxide constant charges on n-type GaN (right) and p-type GaN (left). 29

Figure 3.3: Equivalent circuit models used for conduction measurement analysis: measurement circuit (a), circuit in accumulation, where the semiconductor capacitance does not play a role (b), simple MOS circuit of extracting the corrected MOS capacitance values Gc and Cc (c) and total equivalent circuit given explicit Gp. 30

Figure 3.4: Comparison between the conductivity of the MOS interface before and after series resistance correction. 32

Figure 3.5: Calculation of the trap emission time versus Trap Energy relative to the band gap (solid line). As a reference the capture time for flatband condition is drawn (dashed line). 33

Figure 3.6: Calculation of the Trap capture time in dependence of the Gate voltage, the surface potential and the surface carrier concentration, respectively. The flatband voltage is at zero Gate voltage assuming ideal case. 35

Figure 3.7: Model of Hall measurement: electric field in x-direction, magnetic field in z-direction, Hall voltage in y-direction. 36

Figure 3.8: Schematic Band diagram of Schottky barrier transistor from Source to Drain for thermal equilibrium (upper), barrier lowering by Gate voltage (middle) and forward current by $V_{DS} > 0$ and turned no channel. 42

Figure 3.9: Modeling of the channel resistance from Schottky barrier transistor by comparing the total Source – Channel – Drain resistance for different Gate lengths. 42

Figure 4.1: Schematic of the MOCVD reactor and its components. 45

Figure 4.2: Schematic view of a planar PECVD reactor 47

Figure 4.3: Schematic view of the chemical reaction in the four cycle atomic layer deposition process for aluminum oxide 49

Figure 4.4: Deposition rate and uniformity of the ALD in dependence of the deposition temperature. 50

Figure 4.5: XRD results of 28 nm aluminum oxide films after annealing in oxygen for 60s at several temperatures 51

Figure 4.6: Leakage current measured for 10 nm and 28 nm aluminum oxide films. The measured current values were taken from the same potential difference starting from the flatband voltage in order to neglect differences in the interface. 52

Figure 4.7: Schematic process flow for MIS capacitors 53

Figure 4.8: Mask used for the fabrication of MIS capacitors (a). The bottom figure (b) shows a schematic view of the cross section of the capacitors with the dielectric (black) on the GaN substrate and the single metal layer on the top for both electrodes. 55

Figure 4.9: Schematic process flow of the Hall pattern 57

Figure 4.10: Schematic Mask design for the Gated Schottky Hall pattern (top right) and the Gated Hall pattern (top left). The bottom figure shows the cross section of the Gated Schottky Hall pattern with overlapping pad and Gate metallization. The normal Gated Hall pattern is same except no overlap is necessary. 58

Figure 4.11: Measurement circuit for Gated Hall measurement. The sample was bonded and connected to the Hall system, with external Gate bias control. 59

Figure 4.12: Mask design (top) and cross section (bottom) of the Schottky Transistor..... 60

Figure 5.1: Measurement of the same capacitor with different common ground contact configurations according to figure 5.2 62

Figure 5.2: Schematic cross-section for standard common ground contact (upper), reduced size common ground contact (middle) and far reduce size contact (lower). 63

Figure 5.3: Schematic description of the current distribution in radial direction in an infinite structure under consideration of the series resistance and the MIS capacitor..... 65

Figure 5.4: Comparison between the same capacitor measured at large and small capacitor pattern. The value of the small pattern is multiplied by the aerial ratio between the two capacitors for normalization. 67

Figure 5.5: $1/C^2$ extraction on deep depletion CV measurement on n-type for SiO_2..... 70

Figure 5.6: $1/C^2$ extraction of deep depletion CV measurement on p-type GaN for SiO_2... 70

Figure 5.7: CV graph of non-annealed Si_3N_4 showing high flatband voltage dependence on frequency. Ideal graph is shown for comparison. The oxide capacitor of the 24 nm dielectric film was 180 pF. 72

Figure 5.8: Hysteresis effect on Si_3N_4 capacitor measured at 1 kHz and indicating a very high interface density close to the conduction band. The oxide capacitor was 180 pF.73

Figure 5.9: CV graph of annealed Si_3N_4 measured at 1 MHz without UV light. The graph shows dispersion and is therefore normalized to its maximum value. (C_{ox} = 61.1 pF/ 72nm Si^3N^4) 73

Figure 5.10: Comparison between n-type CV graphs with annealed and non-annealed Si_3N_4 measured during UV illumination. The threshold shift shows a lower fixed charge density for the annealed dielectric. Both oxide capacitors are 61.1 pF. 74

Figure 5.11: Comparison of p-type CV graphs with Si_3N_4. Upper Graph shows annealed sample measured with UV light illumination at 1 MHz (C_{ox}=61.1 pF) while lower graph (shifted by -20V) shows the non-annealed sample measured without light at 1 kHz (180 pF). 75

Figure 5.12: CV of 40 nm non-annealed SiO_2 on n-type GaN over frequency. C_{ox} = 70 pF. 76

Figure 5.13: CV graph of 40 nm SiO_2 on n-type GaN with and without UV light, measured at 1 MHz. (C_{ox} = 70 pF)..... 77

Figure 5.14: CV graph of annealed SiO_2 (72 nm) with and without UV light. Capacitor shows large dispersion at 1 MHz. 77

Figure 5.15: Interface state density extracted from p-type sample for the lower half and from n-type sample for the upper half of the band gap..... 78

Figure 5.16: Photoluminescence Measurement of Mg doped p-type GaN. The energy is plotted reversely from the conduction band to match it with the valence band. The PL peak from the valence band electrons is drawn light grey, that it can be differed from bulk traps by the viewer's inspection. 79

Figure 5.17: CV graph, measured at 1 MHz of p-type SiO_2 capacitor, with and without UV light. Graph is normalized by its maximum, due to dispersion at high frequency. C_{max}= 14 pF/ SiO_2 40nm. 80

Figure 5.18: Frequency dispersion in p-type GaN with 40 nm SiO_2 (C_{ox} = 70 pF). 81

Figure 5.19: Inversion behavior at white light exposure in p-type GaN with 72 nm SiO_2 after annealing. Measurement was done at 1 MHz. 81

Figure 5.20: CV graphs for Al_2O_3 MOS capacitors for non-annealed (upper, left), 750°C (upper, right) and 850°C (lower) annealed samples. 83

Figure 5.21: Summary of oxide charges, fixed charges and interface charges for different annealing conditions of Al_2O_3 83

Figure 5.22: Extracted and normalized parallel conductivity for the non-annealed sample (upper, left), the 750ºC annealed sample (upper, right) and the 850ºC annealed sample (lower). 84

Figure 5.23: Summary of interface state density plotted over the band energy relative to the valence band. 85

Figure 5.24: CV graph of the 700ºC annealed Al_2O_3 sample with and without UV light. The vertical arrow shows the increased capacitance value due to the incident optical energy. 86

Figure 5.25: Hall measurement result (mobility & sheet carrier concentration) of annealed silicon nitride sample..... 87

Figure 5.26: Sheet resistance result from Hall measurement 88

Figure 5.27: Extracted accumulation charges extracted from Hall measurement in comparison to fitted theoretical data (open holes) using a flatband voltage at 3.8 V and a capacitance of $3x10^{-8}$ F/cm^2. 88

Figure 5.28: extracted field-effective accumulation channel mobility using carrier concentration from the Hall measurement and the theoretical fitted data. 89

Figure 5.29: Id-Vd characteristic of p-type GaN SCHOTTKY BARRIER MOSFET with and without UV light. 91

Figure 5.30: Id-Vg Characteristic of annealed silicon nitride depletion Mosfet for several Gate lengths and 80 µm channel width. The flatband voltage was assumed to be around -1 V, by comparing with Gate-less TLM pattern. 92

Figure 5.31: Total Source-Drain accumulation resistance over channel length for annealed silicon oxide depletion MOSFET. 92

Figure 5.32: Extracted field-effective mobility for annealed silicon oxide, silicon nitride and aluminum oxide over the relative Gate Potential in accumulation. 93

Figure 6.1: Summary of oxide charges in GaN MIS structures. (n.a. = not annealed, silicon oxide and nitride were annealed at 1000°C for 30 min under nitrogen ambient) 95

Figure 6.2: Summary of interface state densities in GaN MIS structures. The arrows mark the expected high interface state density near the band edge. 96

List of Tables

Table 1.1: Comparison of electrical properties of semiconductor materials..... 2

Table 2.1: Spontaneous polarization for AlN, GaN and InN in [0001] direction of the wurtzi te structure given in standard unit and number of charges per cm^2 for comparison to su rface charges. 10

Table 2.2: Summary of dielectirc materials used on GaN. 14

Table 5.1: Summary of succussful fabriacted MOSFET devices 90

1. Introduction

This first chapter provides a low level technical background focusing on the reason of GaN as a material for transistors in general and on inversion metal insulting semiconductor field-effective transistors (MOSFETs) in particular. A brief review about the history of GaN MOSFETs is also presented summarizing the results up to today and gives reasons for this work. A detailed introduction over this work is given at the end of this chapter.

1.1. GaN & Modern Semiconductor Devices

The recent progress in GaN devices [1, 2] is driven by its superior material parameters as wide band gap (3.44 eV), high critical electric field (3 MV/cm), similar thermal conductivity as silicon and high mobility in polarization charge induced two dimensional electron gas (2DEG) due to its polar nature. All those parameters and the fact that prior growth difficulties could be solved, lead to dominance in high power and high voltage operation devices. A comparison of the main material parameters to other materials used for power devices is shown in table 1.1.

Prior to its success in transistors, light emitting diodes (LEDs) where developed emitting blue light according to its high band gap energy. In the standard lattice structure, wurtzite, GaN, AlN and InN form a continuous alloy system whose direct band gaps range from 1.9 eV for InN, to 3.4 eV for GaN and up to 6.2 eV for AlN. Thus the III-nitride family potentially could cover the whole spectra from red to deep ultraviolet. Indeed, this is what recent reports show, even though the crystal quality, which is crucial for effective devices, is still the major problems for those materials [3].

Also, GaN power transistors gain several benefits due to the large band gap. The intrinsic carrier concentration is around 10^{-10} cm^{-3} at room temperature, which allows much higher operation temperatures, until the extrinsic carriers dominate. Indeed device performances at temperatures higher than 1000°C were shown recently at the IWN 2006 [4], which did not result to any degradation in device operation. In achieving the same depletion width in a junction, GaN can be doped higher according to the wide band gap, which improves the on-state resistance of power

device and the on-state power loss. Additional, for the same depletion width GaN shows a better breakdown voltage [5, 6] as it has a ten times higher breakdown field than silicon and 5 times higher than GaAs.

	Si	GaAs	4H-SiC	GaN
e^- saturation velocity	1×10^7 cm/sec	1×10^7 cm/sec	2×10^7 cm/sec	~ 3×10^7 cm/sec
Breakdown field	0.3 MV/cm	0.6 MV/cm	2 MV/cm	3.3 MV/cm
2DEG density	-	~ 10^{12}/cm2	-	~ 10^{13}/cm^2
Bandgap	1.1 eV	1.4 eV	3.3 eV	3.4 eV
Electron Mobility	1400 cm^2/Vs	8500 cm^2/Vs	800 cm^2/Vs	900(H) cm^2/Vs
Thermal conductivity	1.5 W/mK	0.5 W/mK	4.9 W/mK	1.3 W/mK
ε_r	11.8	12.8	10	9

Table 1.1: Comparison of electrical properties of semiconductor materials

Even though GaAs provides a four times higher mobility in 2DEG as GaN it can not be used for high power device due to its low breakdown field. Therefore GaN shows the combination of all benefits making it the leading material in this field. This can also be seen in figure 1.1, describing that the limits for GaN devices cover the whole spectra of LDMOS devices and GaAs power transistors [7, 8]. Indeed, Cree [9] and Nixtronex [10] recently presented their first power transistors products on GaN based on high electron mobility transistors (HEMTs) for output power up to 100 W and frequency range up to 10 GHz. Further high frequency device operation with an output power of 35 dBm at 110 GHz have been shown [11] for RF power MMIC applications.

In summary, GaN provides the highest power device capability based on today's fabrication possibilities. There are still materials as diamond or AlN [12] which provides higher band gaps, but the limits of these materials are simply the difficulties in growth which have to be solved prior to device fabrication.

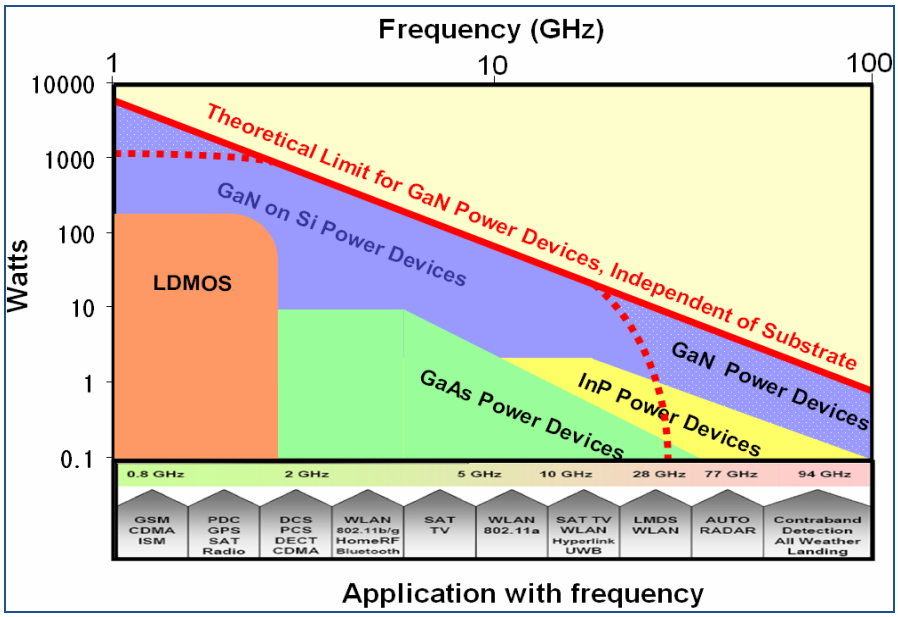

Figure 1.1: Application field of materials based on frequency and power performance

1.2. History of Inversion MOSFETs in GaN

Depletion MOSFETs in GaN have been investigated since Ambacher et al. described the effect of two dimensional carrier gas [13, 14]. However, for real device applications, those transistors suffer from two major issues. First, depletion transistors are normally-on, which is often not accepted for many applications (i.e. in automobiles) regarding safety reasons and second, those devices show always a certain leakage through the buffer in turn-off state and the sub-threshold slope gets horizontal. Therefore the on-state current can achieve high current values but in total the devices often show a low on-off current ratio, which increases the off-state power consumption.

In contrast, inversion MOSFETs include a reverse pn junction in turn-off mode but do suffer from less forward current in turn-on state, since the carrier concentration is less and the mobility is around one order lower than in the 2DEG. First attempts for this were done by Irokawa et al. [15] who showed a non-self aligned device structure with MgO dielectric. Similar to all devices up to today, they used Si for n+ doped Source and Drain regions into Mg doped p-type GaN. Even though, MgO was described to have a good interface quality, the device showed very low

inversion current. At a Gate length of 22 µm the maximum Gate current at 12 V Gate voltage was 20 µA/mm. The threshold voltage was around 6 V. The output characteristic showed only linear behavior up to 5 V. The extracted electron mobility was extremely low, which is not sufficient for reasonable current capability.

One year later Matocha et al. [16] presented a self aligned structure on n-type GaN with silicon oxide as Gate electric. The Gate structure was fabricated by poly silicon. The device showed a maximum Drain current at 34 V of about 12 mA/mm for a 8 µm Gate length and a 3 orders lower off current. The field-effective electron mobility was extracted from the linear region to be 45 cm^2/Vs. Further tests on the breakdown voltages showed that a maximum breakdown voltages could be achieved at a Gate Drain spacing of 9 µm without field plate.

The same group presented on year later by Huang et al. [17] a similar device on p-type substrate. The Drain current was increased up to 15 mA/mm with a lower turn off current. The sub threshold slope was extracted to be 490mV/decade. The field effective mobility was increased to 167 cm^2/Vs, while the Hall mobility showed 200 cm^2/Vs. The small difference was explained to be due to the interface charges, which was proved to be low by CV method.

Another very unconventional idea was pulished by Jang et al. in 2006, trying to make a Source Drain doping by Si diffusion [18]. Using a temperature of 1000°C for long time annealing cycles a reasonable doping could be achieved. However the magnesium oxide interface resulted in lower Drain currents around 22 µA/mm.

Very recently Otake et al. [19] presented a vertical trench structure for GaN MOSFETs with silicon oxide and nitride as Gate dielectric deposited by sputtering. The results were however a bit lower then from Huang et al. and showed a field effective mobility of 133 cm^2/Vs.

All these results show a promising outlook for GaN MOSFETs, since the mobility is comparable to other materials and only a factor two lower than Si. However in comparison to high electron mobilities in two dimensional electron confinements it is still a factor ten below.

1.3. Thesis Outline

As this topic is quite new and only a few groups reported on it, compared to the total research in GaN devices, this thesis focuses not just on the experimental work but also on the theory of the applied methods. Several reports have been presented which did not show an accurate analysis. Therefore I am focusing on the background of the interface characterization.

In the second chapter, a general overview of GaN is given with a review on dielectrics studies. The last part of the chapter provides the basic theoretical background on capacitive measurement and the non-ideal behavior. Since this part is already well known from silicon, I built up on this general knowledge and added the specific characteristics of GaN or wide band gap materials in general.

The third chapter explains the method of capacitive and conductive interface analysis and shows a discussion on the accuracy and errors that can occur. This knowledge is a key issue of this work and most of the actual time was spend in finding the right measurement and analysis condition. Also a short explanation on the Hall mobility and the Schottky Transistor is given to show the basic model that was used in the extraction.

A summary on the whole fabrication processes is given in chapter four with a short introduction into the MOCVD growth and the dielectric deposition. Later one focuses on PECVD, which was used for silicon nitride and oxide, and on atomic layer deposition (ALD), which was used for aluminum oxide. Some process details are also given for each of the used devices, as capacitor, Gated Hall pattern and Schottky barrier transistor.

Chapter five shows the results of several experiments and discusses typical measurement issues of the capacitive methods. The first part focuses on the series resistance problem which occurs mainly in p-type GaN and its effect on the virtual ground contact used in the capacitors. The occurring effects are discussed and some solutions are presented. In a second part, the characteristic given by the measurements methods discussed in chapter 3 are shown for silicon nitride, silicon oxide and aluminum oxide. Finally the results of Hall measurements in n-type and p-type GaN and the transistor characteristics are presented.

2. Technical Background

This chapter presents all the general descriptions necessary to understand later characterization methods or fabrication processes. Starting with the bottom of the MIS structure, the first sub chapter summarizes the most important properties of GaN or related materials from the III-nitride family. Even though, this work implies only non-heterostructures, I use them to explain the effect of polarization charges, which have also relevance in bulk materials. The second part covers a summary of important dielectrics, which are applied on GaN in this work. Finally, I show the simple theoretical calculation used to describe a two terminal behavior as it appears generally for wide band semiconductors. This should help to understand the detailed characteristics of capacitive or conductive studies described in chapter 3. A summary of the most important material parameter is further shown in appendix A.

2.1. GaN Properties

In order to understand the origin for the benefits of GaN, listed in chapter 1.1, the crystal structure and the band structure will be discussed in the following part. Based on this, the spontaneous and piezoelectric polarization can be discussed. Also related to this is the importance of other nitride materials, which will be mentioned at the end of this part

2.1.1. Crystal Structure

GaN as well as other group-III nitrides can crystalline into wurtzite, zincblende and rocksalt structure. Last one is probably least common since it requires very high pressures. The zincblende structure for GaN and InN can be grown by epitaxy of thin films on cubic substrates and shows lower effective mass and less dangling bonds on the surface. However, under ambient conditions, the thermo dynamical stable structure is wurtzite for bulk GaN, AlN or InN. Therefore the most common used crystal structure in devices is wurtzite which has a hexagonal unit cell and thus two lattice constants, c and a. It consists of two interpenetrating hexagonal

closed packed (HCP) sublattices.

The origin for many properties of the III-nitride family lies in the extreme high thermal and chemical stability. This originates from the mixed binding mechanism with covalent and ionic components, due to the difference in electro negativity between the group-III and group-V elements. Therefore these semiconductor materials show a high binding energy per atom (GaN 9.8 eV/atom, AlN 11.5 eV/atom, InN 7.7 eV/atom).

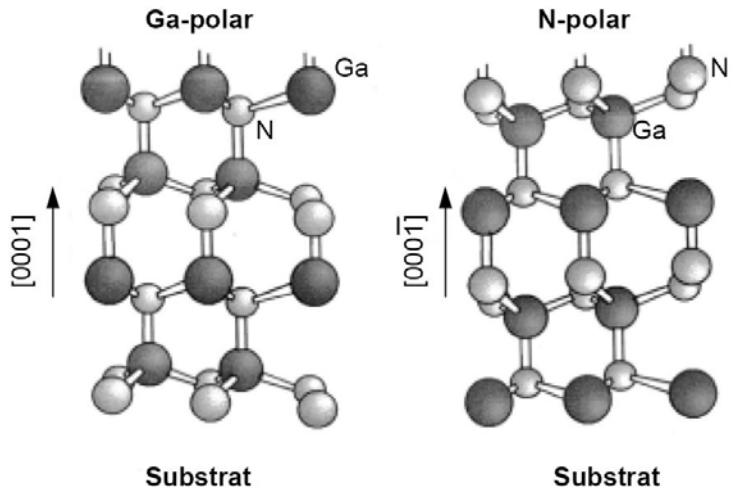

Figure 2.1: Crystal structure of wurtzite structure, typically used in GaN. Right side shows the N-polar phase which is exactly turn around of the Ga-polar phase on the left.

For the wurtzite structure, it is differed between the Ga phase and the N phase. Even though the structures are the same, the order in which the crystal appears is opposite, as can be seen in figure 2.1. The GaN phase is defined as [0001] direction while the N phase is refers as [000/1]. Usually templates grown by MOCVD lead to a Ga-polar substrate, even though N. Fichtenbaum [20] reported very recently an N-polar MOCVD growth by using different orientations of sapphire substrates. In MBE growth both polar structures can be grown, depending on the nucleation layer and the applied MBE (Plasma or NH_3). Differences between the two polarities occur also in physical and chemical surface properties. The Ga-polar phase shows usually more smooth surface morphology and is therefore more resistant against wet etching or oxidation.

It should be noted, that the orientation of an epitaxial GaN layer does not depend on the

termination of the surface. A Ga phase or a N phase can be terminated by either a N layer or a Ga layer, without any change of its phase. Only by flipping around the wafer, the polarity can be changed.

Even though, epitaxial growth is limited by those two polarities for stable wurtzite structure, it was shown that non-polar devices can be fabricated using GaN wafers out of bulk crystal material [19, 21]. The differences for GaN MIS structures using different substrate orientations will be discussed further at the spontaneous polarization effects.

2.1.2. Band Structures

The calculated band structure for the wurtzite phase of GaN is shown in figure 2.2 (left) [22]. In figure 2.2 (right) the crystal orientations are shown for the high symmetrical points of the hexagonal structure. It can be seen that the band gap, resulting from the lowest and highest energy point of the conduction and valence band, respectively, is in the Γ-point, which is the center of hexagonal structure. GaN is, like all other materials of the group III-nitride family, a direct semiconductor and therefore high efficient in transforming electrical energy into optical energy.

Under consideration of the spin-orbit splitting energy and the crystal field splitting energy, the valence band splits into two bands for light holes and heavy holes. The crystal field splitting energy, which occurs only in the wurtzite phase, also depends on the strain of the lattice.

An important issue in GaN is the very low mobility of holes based on a high effective mass. Typical values are found by $m_h/m_0 = 0.8$ [23], even though the results differ quite [24, 25]. It was generally observed that the band gap energy is indirect proportional to the effective carrier mass [26], which also leads to increased masses in other high energy gap materials as GaAs or InP. Additionally, wide band semiconductors show a higher intra band scattering, which further reduces the mobility of holes.

The fundamental material property of low hole mobility and respectively high resistive p-type GaN films, is the main reason why GaN devices focus almost exclusively on electron carriers. Therefore bipolar devices as inversion MOSFETs or heterostructure bipolar transistors (HBTs)

are far behind the development in comparison to unipolar devices as HEMTs.

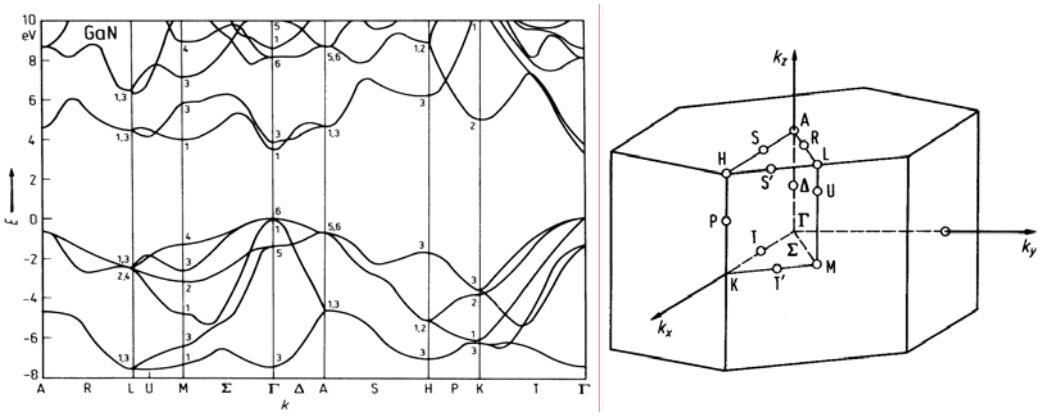

Figure 2.2: Band energy of conduction bands and valence bands in GaN based on theoretical calculation [22] (left). The right side shows the crystal directions based on the unit lattice cell.

2.1.3. Piezoelectric and Spontaneous Polarization

The high number of polarization charges is probably the most important factor of GaN based devices. It causes extremely high carrier concentration called two-dimensional electron gas (2DEG) or its opposite two-dimensional hole gas (2DHG) at the interface to other materials. The polarization charges depend on two independent components; the material dependent spontaneous polarization and the stress dependent piezoelectric polarization.

The spontaneous polarization depends directly on the hexagonal structure on the wurtzite phase. It is called spontaneous, since no external field or force is required. From figure 2.1 can be seen, that Ga layers are followed by N layers or vice versa, depending on the polarity. In order to get the total polarization from the Ga – N binding (with ionic component), the single dipoles in [0001] should be add up. While this leads to a constructive addition in the wurtzite structure, the total sum of polarization charges is zero in the zincblende structure, as can be found from figure 2.3. The diagonal directions are faced in all eight directions and cancel each other.

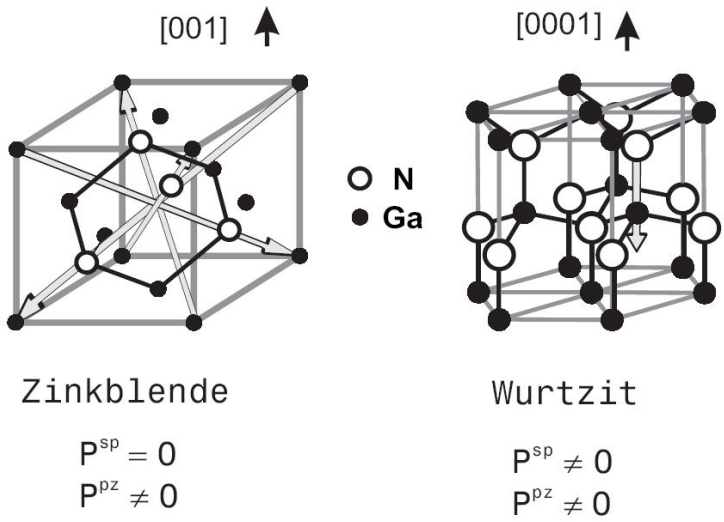

Figure 2.3: Unit cell structure of zincblende (left) and wurtzite crystal (right). The polarization can be understood by adding up the vectors from N atoms to GaN atoms (white arrows).

It should be noted, that inside the crystal the spontaneous polarization is zero (or only appears as a higher order multi pole with neglectable influence) due to the ongoing sequence of atomic layers. Spontaneous charges occur therefore at terminating surfaces, as material interfaces of air interfaces. In terms of material interfaces the net charges depends on the difference between the spontaneous polarization fields the two materials. Theoretical values have been calculated by Bernardini et al. [27] and are listed in table 2.1. The table inlcudes the values for charges per square meter and values normalized for the elementary charge. It appears quite clear that those values are very large, if they represent the carriers in a 2DEG or the surface charge to a dielectric interface. Later one is the reason why several groups try to use non-polar materials [21, 28].

	AlN	GaN	InN
P_{sp} [C/m^2]	-0.081	-0.029	-0.032
P_{sp} [q/cm^2]	-5.06e13	-1.81e13	-2.00e13

Table 2.1: Spontaneous polarization for AlN, GaN and InN in [0001] direction of the wurtzite structure given in standard unit and number of charges per cm^2 for comparison to surface charges.

The second component of polarization charges arises from the fact, that hetero interfaces produce

stress (tensile or compressive), which deforms the crystal structure and causes therefore piezoelectric induced charges. The amount of charges is therefore not constant and depends on the polarity and on the stress, which is material and alloy dependent. A qualitative graph summarizes the effect of stress on the piezoelectric charges and the total polarization charges in figure 2.4. The induce stress on a hetero interface is an almost linear function to the mole fraction of the III-N alloys. A simple limit for piezoelectric charges is the difficulty in growing such stress related interfaces. If materials with a higher lattice constant difference are grown in sequence on top of each other, the critical thickness, until the surface of the upper layer cracks, reduces drastically. Therefore the number of polarization charges is limited by the capability of growing such structures. An exact evaluation of the piezoelectric induced charges depends on the stress tensor and the piezoelectric tensor, which is not discussed further here, as piezoelectric charges do not play a role in single GaN layers.

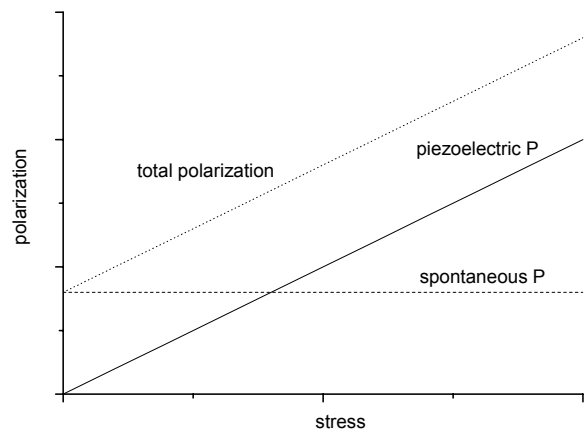

Figure 2.4: Qualitative graph of the polarization based on the stress in the lattice perpendicular to the [1000] direction. The stress can be introduced by interfaces with III-N alloys.

2.1.4. Typical Compounds of GaN

The III-nitride family contains the three basic materials GaN, AlN, InN and there alloys. Not only the high band gap differences, mentioned at the band structures, but also the large

conduction band offsets make devices based on electrons very interesting. The most commonly used alloy is probably AlGaN in High Electron Mobility Transistors (HEMT). Since it was found that there is a minimum thickness that the AlGaN layer requires to form a 2DEG channel [29], the aluminum content is quite limited around 30%. Further increase would lead to higher stress and therefore more piezoelectric charges but also enhances the roughness of the interface, which provides another scattering mechanism to the electron channel [30]. Very recently AlN/GaN HEMTs were demonstrated [31, 32] showing a critical thickness around 7 nm and an optimum, regarding the current flow, at 5 nm. Due to the higher carrier concentration, provided by higher spontaneous charges based on higher difference in polarization field and by higher piezoelectric charges due to increased stress according to the lattice constant difference, this device shows the highest current capability of any state-of-the-art GaN device.

Another newly applied alloy is AlInN (also written as InAlN), which can be grown lattice matched on GaN with an In content of about 17% according to figure 2.5 [33, 34]. For this structure the growth does not provide any stress and therefore less difficultness, but also no piezoelectric charges. Later one is compensated by increasing spontaneous polarization, which makes this device another promising candidate for high current devices.

On the issue of MOSFETs, GaN is commonly applied due the vast amount of growing experience and the high band gap, providing higher breakdown voltages. Using AlN as a bulk material would be another great step in terms of higher voltage drivability, but therefore numerous problems for the device fabrication, as doping and ohmic contacts must be solved. Another approach is to use AlN as a dielectric, which it certainly is, due to its wide band gap. In order to apply larger thicknesses it has to be grown at lower temperatures around 500°C to be relaxed, otherwise interface charges would appear, as described above. In our group we could recently show that AlGaN alloys on p-type GaN showed also relaxation effects, if the p-type layer is thick enough. Also AlN directly grown on p-type layer showed an extremely smooth surface, compared to the same thickness on undoped GaN. This approach might be another step to find better interfaces for dielectric materials on GaN.

The third alloy of the III-nitride family, InGaN, shows the smallest band gap and therefore if used in a stack of the same polarity, shows opposite behavior in polarization charges. This was used in an approach to raise the conduction band on the backside of a 2DEG channel for further

channel confinement [35]. A second approach was shown, using InGaN on the top of the HEMT structure to raise the conduction band before the 2DEG and change the device to enhancement mode [36].

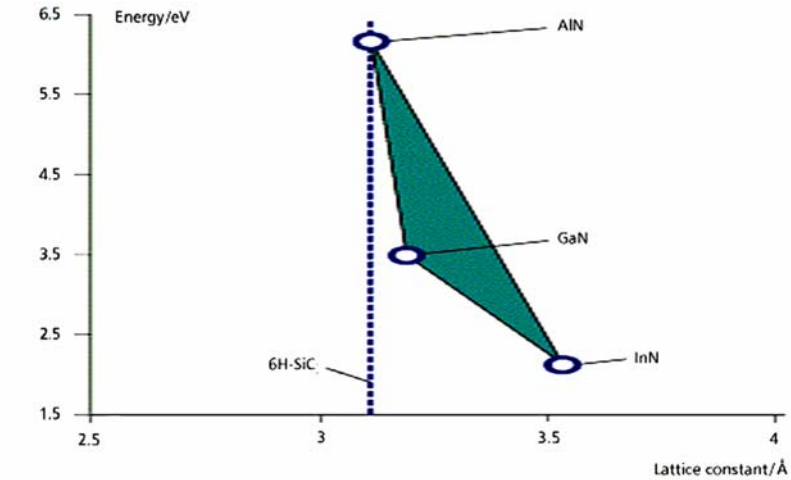

Figure 2.5: Band gap energy versus lattice constant for the basic nitride materials (dots). Along the outside line of the triangle the band gap energy for possible compounds can be seen.

In summary, designing within the III-nitride family heterostructure can be done by crystal structure, crystal orientation, polarity of orientation and the order and type of materials. Several new ideas are therefore potentially possible by using those materials.

In terms of MOSFET devices, those polarity properties are rather unwanted, as they provide additional surface charges. Even though, they can be taken into account to the fixed charges, it should be noted that the polarization charges have a strong dependence on the temperature and therefore cause shifts in the device parameters.

2.2. Gate Dielectrics on GaN

This chapter provides a basic overview over numerous dielectric materials. Several different reports have been shown that it is very difficult to find a good material on GaN. But also the applied measurement methods for characterizing differed a lot in the past, making an accurate comparison difficult. However the dielectric interface seems to be the major reason, why

inversion MOSFETs rarely have been reported, compared to depletion devices. Those need only a Fermi level shift to the mid gap to deplete the conduction band sufficiently. In inversion MOSFETs the Fermi level must sweep through the full gap, which is often prevented by high interface states, which pin the Fermi level and make the minority carrier generation impossible. I will discuss this problem in detail in the experimental chapter of this work.

In table 2.2 the basic parameters, as dielectric constant, the band gap and the conduction band discontinuity ΔEc to GaN, of several dielectrics are listed.

Material	Dielectric constant	Eg (eV)	ΔEc to GaN	Reference
GaN	9.5	3.4	-	
SiO_2	3.9	9	2.3	[37]
Si_3N_4	7.4	4.5	Unknown	[38]
Al_2O_3	8.6-10	9	2	[39-43]
AlN	8.5	9	1.7	[13]
Ga_2O_3	10	5.4	0.9	[44]

Table 2.2: Summary of dielectirc materials used on GaN.

Silicon Oxide was one of the first reported dielectrics on GaN [45], and many reports followed [46-49], showing different pre-dielectric-deposition surface treatments [50] or different deposition techniques. Those methods as PECVD [51], liquid phase deposition [52] and electron beam deposition [53] show all interface charges in the order of 10^{11} cm^{-2} to 10^{12} cm^{-2} close to the conduction band edge. In 2006 Huang et al. report PECVD deposited silicon oxide at 300°C showing a very nice result from 10^{11} cm^{-2} at the upper band edge to 10^{10} cm^{-2} in the midgap [54]. This work includes also a short discussion on the result of p-type GaN MIS capacitors, which were generally less investigated. Huang et al. and Nakano et al. observed both an inversion behavior in p-type GaN without light illumination [55]. A general advantage of SiO_2 is the large conduction band, decreasing tunneling currents through the oxide, but it also has a more than two times lower dielectric constant which causes lower breakdown behavior. From a process technological view point silicon oxide is probably the easiest material and it can be applied in several ways to a fabrication process, which makes it a very useful candidate.

Few works are shown for silicon nitride usually deposited by PECVD [56, 57]. In comparison the results are better than SiO_2 by a factor 10 at the band edge [51]. The result von Nakasaki et al.

was measured by Terman's method [58] and is therefore probably not accurate enough, especially on the band edge. For device surface passivation, most groups use SiNx which is known to reduce the dangling bonds and surface charges, influencing the device [59]. It should be noted that those results are not applicable on inversion MOSFETs since they not only require low fixed charges but also a low interface state density throughout the whole band gap.

A very new approach is aluminum oxide, often deposited by atomic layer deposition (ALD) on GaN, which also this work focuses on. Al_2O_3 depletion devices have been shown with a reasonable performance [60-63], without noticing about the passivation effects on the frequency behavior. A rough estimation of average interface states density for different annealing conditions have been shown by Wu et al [64] for 40 nm thick aluminum oxide, using the total UV shift of the capacitor measured at the inversion capacitor level. The work also showed an improvement of the average interface states for thermal treatment up to 800°C down to 10^{11} cm^{-2}. While Al_2O_3 after deposition is in amorphous phase, it change to polycrystalline phase at thermal treatment around 800°C for very thin films, less than around 5 nm, or lower temperature for thicker film. The reason therefore is simply that a long range order can easier be established in a thicker film rather than very thin film [65]. Therefore thin films around 10 nm change their phase easily to polycrystalline at temperatures below 800°C, which increases the leakage current by several orders of magnitude. Further results on this will be shown in the experimental chapter. In conclusion on this, aluminum oxide shows good results and improvement through annealing. The point is just, that too high annealing temperature might not be possible to be applied, as the phase changes and the material looses its properties of a good Gate dielectric.

Gallium oxide has been also reported as dielectric grown by dry thermal oxidation in oxygen ambient [66-69], but does not provide the same benefits as silicon oxide to silicon. A few reports show higher values than usually on SiO_2 by PECVD.

As mentioned in the previous chapter, AlN can be also applied as a dielectric with its large band gap of 6.2 eV. In order to grow a relaxed AlN film on GaN the growth temperature should be much lower around 500°C. However, the results are not better than from silicon oxide as shown from Hashizume et al., who used thick AlN and characterized them by UV light [70].

In summary many reports on several dielectric show the difficulty of finding a good interface on GaN, but also the critical issue of applying an accurate method to analyze them.

2.3. The basic MIS Structure

The Metal-Insulator-Semiconductor structure has been the reason for the long time success of the integrated circuit era. Most of its study has been done on silicon as a p-type or n-type semiconductor with a SiO_2 oxide layer and there is probably not much, which needs to be developed in this field. In order to describe the ideal case of the MIS structure in GaN, the basic physics known from silicon can be applied but several behaviors of the total structure change due to the wide band gap.

The following to subchapters will review the physical-mathematical background for this field for the ideal case, where the insulator and its interface to the underlying bulk material is supposed to be free of charges or interface states, and later the qualitative effects for the real case. In chapter 3 I will then describe how the interface quality and the charges in the insulator can be determined.

2.3.1. 2-Terminal Behavior of Gallium Nitride

The basic MIS structure consists of a semiconductor bulk material with an insulating material and a metal layer on its top, as shown in figure 2.6. The metal is assumed to have no ohmic resistance so that its thickness is irrelevant for this observation. The insulting material often has a thickness from a few nanometers to hundreds of nanometers, but in any case we want to neglect any vertical current trough this structure. Since the integration density of modern integrated transistors is steadily increasing, this thickness became one of the most crucial factors, as tunnel current increases exponentially and hence makes a low operation current impossible. However, this problem does not yet play a critical role in GaN MOSFETs.

The semiconductor in my model has a sufficient thickness, that any band bending at its surfaces is decayed at least until its bottom end at any bias condition. Also I assume to have no bulk potential. Therefore the bulk semiconductor can be set as a potential reference point somewhere deep inside. For a given surface potential (of the semiconductor) the electric field and the resulting charges in the semiconductor can be calculated using Maxwell equations. On the other side of the dielectric, the Gate voltage can be written as a function of the surface potential and the charges in the semiconductor which again are functions of the surface potential. Therefore the easiest way is to search a parametric function based on the surface potential of the semiconductor. After finding the two equations it can be noticed, that those equations do not have an analytical inverse function. Therefore numerical solutions are necessary to solve the

implicit equation. In appendix B the straight forward parametric solution is presented and appendix B suggests a simple numerical solution for Matlab. The split from the implicit function to two parametric functions can be described as

$$C_{MIS}(V_{Gate}) \quad \mapsto C_{MIS}(V_{Surface})$$

$$\mapsto V_{Gate}(V_{Surface}) .$$

The MIS capacitor can be divided into a series of the insulating capacitor, with a fixed thickness, and a semiconductor capacitor, with a surface voltage dependent depletion thickness. In order to find the thickness of the depletion width we start describing the changes of charges in the surface region of the semiconductor.

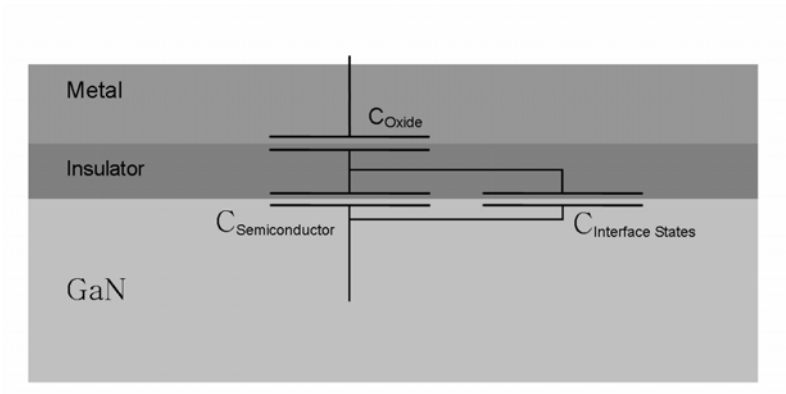

Figure 2.6: MIS structure and basic equivalent circuit of capacitors. For the ideal case the interface state capacitor is zero and only the semiconductor and oxide capacitor remain.

Assuming an n-type GaN material with a doping concentration N, the surface can either be depleted or accumulated. As shown in figure 2.7 a negative voltage causes negative charges at the metal surface and positive charges in the semiconductor. A source of positive charges can either be fixed ionized donors in a depleted surface region or free holes at surface inversion. Later one can only be supplied by external hole sources since the minority carrier response time τ_R is vast too long in wide band materials. A brief calculation can prove this when τ_R is given by

$$\tau_R = \frac{1}{\sqrt{2}}\frac{N}{n_i}\tau_0 = \frac{1}{\sqrt{2}}\frac{10^{17}}{10^{-10}}10^{-8} \cong 10^{19}\, s \cong 3\cdot 10^{11}\, years, \qquad (2.1)$$

where n_i is the intrinsic carriers density and τ_0 is the carrier lifetime. Therefore any capacitive measurement in GaN should result into deep depletion graphs without external carrier supply [71,72].

In accumulation the conduction band bends down and electrons can gather in a certain surface region. The relation between electrons and the band potential is given by

$$n(x) = N \cdot e^{\frac{q\varphi(x)}{kT}}, \tag{2.2}$$

where n is the electron concentration along the x coordinate, which belongs to the depth of the structure and φ is the potential, which is zero at the band edge deep inside the bulk. Assuming that all donor are ionized, Poisson's equation can be written as

$$\frac{\partial^2\varphi(x)}{\partial x^2} = -\frac{q}{\varepsilon} N\left[e^{\frac{q\varphi(x)}{kT}} - 1\right]. \tag{2.3}$$

Unfortunately, this equation can not be solved analytically and an assumption should be made to simplify the problem. Therefore the accumulation width W_a is defined according to figure 2.7, where the electron concentration is higher than N for $x < W_a$ and equal to the bulk concentration for all values $x > W_a$. This includes an assumption as it is used similarly for the depletion assumption. The Poisson equation can now be noted as

$$\frac{\partial^2\varphi(x)}{\partial x^2} \cong -\frac{q}{\varepsilon} N e^{\frac{q\varphi(x)}{kT}} \tag{2.4}$$

including the assumption $n >> N$. Considering that the potential and its first deviation (electric field) is zero at the accumulation width the solution of above equations and the electric field is

$$\begin{aligned} \varphi(x) &= \frac{kT}{q} \ln\left\{\sec^2\left[\frac{Wa - x}{\sqrt{2}L_D}\right]\right\} \\ \vec{E}(x) &= -\frac{2kT}{q}\frac{1}{\sqrt{2}L_D}\tan\left\{\frac{x - Wa}{\sqrt{2}L_D}\right\} \end{aligned}. \tag{2.5}$$

Using the solution of the potential in equation 2.2 gives the carrier concentration of the accumulation region. Further more, the integral of the accumulated electrons defined by

$$n_{acc}(x) = N \cdot \left(e^{\frac{q\varphi(x)}{kT}} - 1\right) \tag{2.6}$$

shows the total amount of accumulated charges

$$Q_{s,acc} = -\sqrt{2 \cdot \varepsilon \cdot V_T \cdot N \cdot q} \cdot \sqrt{e^{\frac{Vs}{V_T}} - 1}, \tag{2.7}$$

where $$V_T = \frac{kT}{q}. \tag{2.8}$$

This result is the first part used for the theoretical capacitance behavior. V_s is the surface potential which belongs to the surface carrier n(x) for x = 0 and can be found by equation 2.5-1.

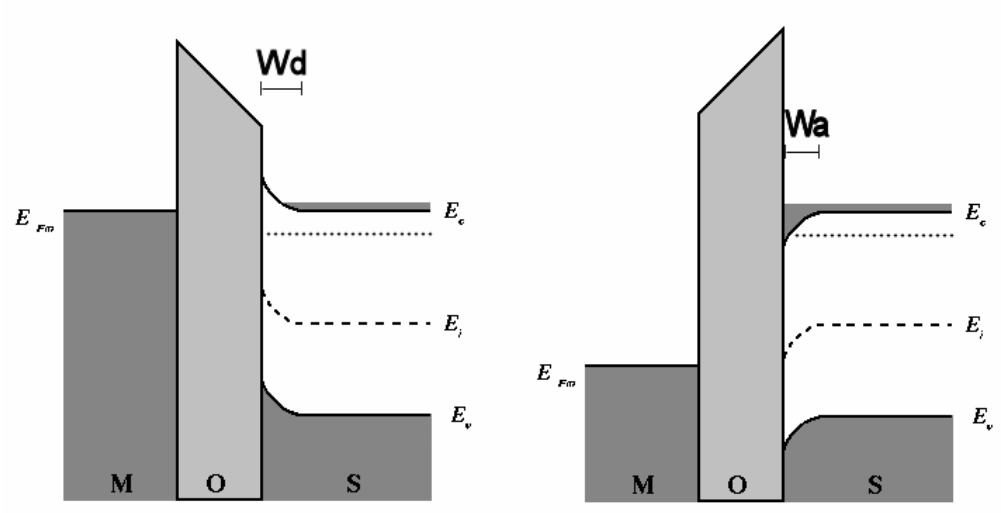

Figure 2.7: Qualitative band diagram of the MIS structure for accumulation and depletion

Looking on the opposite Gate voltage direction, the semiconductor surface will be depleted of electrons. As discussed, no further mobile carriers can reach the surface and the surface depletes deep into the bulk. The description is much easier since only one type of charges is involved and equals a simple diode analysis starting with Poisson's equation

$$\frac{\partial^2 \varphi(x)}{\partial x^2} = -\frac{q}{\varepsilon} N \ . \tag{2.9}$$

Similar to previous analysis a certain depletion width can be assumed. From the potential solution the total amount of depletion charges is

$$Q_{s,dep} = \sqrt{2 \cdot \varepsilon \cdot V_S \cdot N \cdot q} \ . \tag{2.10}$$

With this second solution, all charges, occurring in a wide band gap semiconductor are

numerically described. The total semiconductor charges Q_s is noted as

$$Q_S(V_S) = Q_{S,acc} + Q_{S,dep} = \sqrt{2 \cdot \varepsilon \cdot N \cdot q} \cdot \sqrt{V_T e^{\frac{Vs}{V_T}} - V_T - V_S} \qquad (2.11)$$

and plotted over the surface potential in figure 2.8.

This pre-result tells how many charges are developed in the semiconductor at a surface potential. From that information the capacitance belonging to those charges is simply given by the derivative after the surface potential

$$C_S(V_S) = -\frac{dQ_S}{dV_S} = \frac{\sqrt{2 \cdot \varepsilon \cdot N \cdot q}}{2} \cdot \frac{e^{\frac{Vs}{V_T}} - 1}{\sqrt{V_T e^{\frac{Vs}{V_T}} - V_T - V_S}} . \qquad (2.12)$$

Since the oxide capacitor is constant and in series with the semiconductor capacitor (figure 2.6), the total capacitance is described by

$$C(V_S) = C_{ox} \,||\, C_s(V_S) = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_s(V_S)}} . \qquad (2.13)$$

This result, which is the first function of the parametric function solution, is shown in figure 2.9. It can be seen, that the semiconductor in accumulation reaches a value much higher than the oxide capacitor, which therefore is neglected. On the other side in depletion, the thickness of the ionized donor surface is increasing and dominates the total capacitor.

A final analysis belongs to the second part of the parametric function and develops the relation between the surface potential and the Gate voltage $V_a(V_s)$. As mentioned, the potential has a reference point deep in the semiconductor, which requires adding up all potential changes from the bottom to the top of the structure. The first component is the surface potential, which does not need any description, since it is the parameter of the function. Further, the charges in the semiconductor cause an electric field, which must be supplied by the Gate voltage trough the oxide capacitor. When the semiconductor has totally flat bands (no bending in either direction), which requires no fields in the vertical structure, it is called to be in flatband. For the ideal description this case happens under zero applied voltage. In a real device, the difference in workfunctions, fixed and interface charges (Q_f, Q_{int}) play an additional role [73, 74].

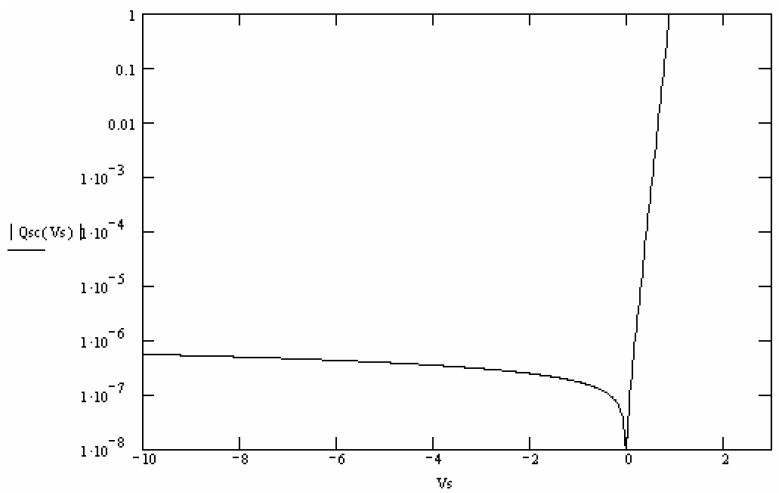

Figure 2.8: Total calculated amount of semiconductor charges versus the surface potential of the semiconductor

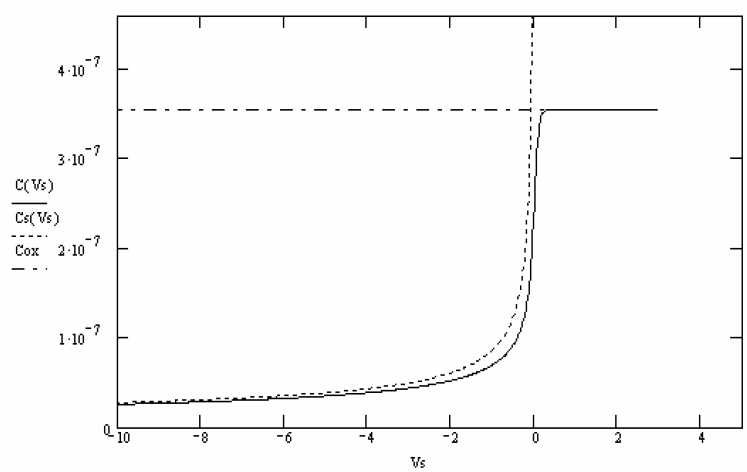

Figure 2.9: Calculation result of the total Capacitor of the MOS structure (solid line), semiconductor capacitor (dashed line) and the constant oxide capacitor.

Those charges will be discussed further in the next chapter. At this point, it should only be mentioned that interface charges are another function of the surface potential.

$$V_{FB} = \Phi_M - \chi_s - \left[\frac{E_g}{2} - \frac{kT}{q}\ln\frac{N}{n_i}\right] - \frac{Q_F}{C_{ox}} - \frac{Q_{INT}}{C_{ox}} \qquad (2.14)$$

where Φ_M is the metal work function, χ_s is the electron affinity of the semiconductor, E_g is the

band gap energy, k is the Boltzmann constant, T is the temperature, q is the elementary charge, N is the doping density, n_i is the intrinsic carrier concentration, Q_F is the density of fixed charges, Q_{INT} the density of interface trap charges and C_{ox} is the oxide capacitor. Except the interface trap density (equal to interface charges if filled), all other components are constant in respect to the surface potential V_s. Any charges within the oxide can be contributed in the fixed charge, but do usually not play a dominant role since the fixed charge at the surface are higher and more effective.

Adding up the discussed components for the applied Gate voltage results to

$$V_a(V_s) = V_s - \frac{Q_s}{C_{ox}} + V_{FB}\,. \tag{2.15}$$

This function is plotted for zero flatband voltage in figure 2.10. It can be seen that, except in accumulation region, the surface potential and the Gate potential increase proportional.

Since both functions are known, also the capacitance-voltage graph can be plotted, as it appears theoretically in wide band gap semiconductors, shown in figure 2.11. This result can be used as a reference for measurements on CV results.

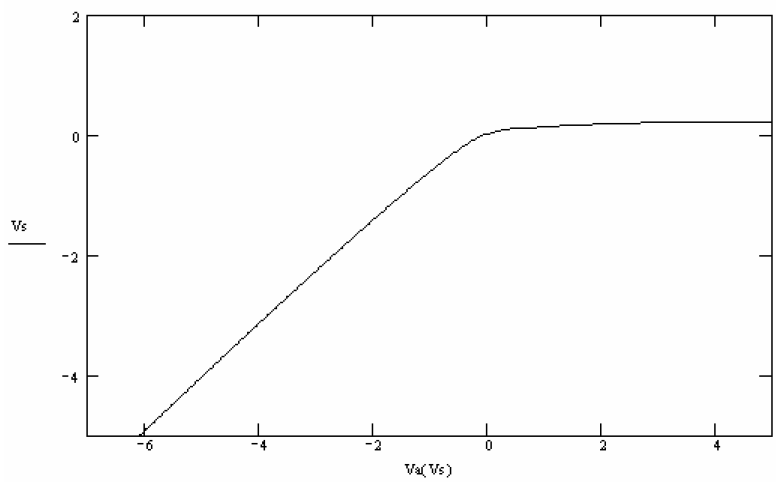

Figure 2.10: Calculation of the relation between surface potential and the Gate potential. In the depletion region both change linear. From the flatband voltage the surface potential does not change.

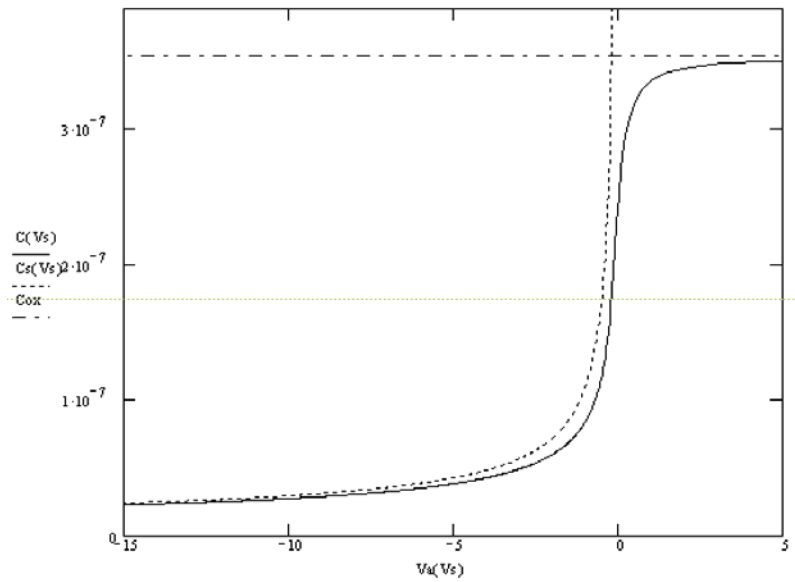

Figure 2.11: Calculation of the MOS capacitor (deep depletion) versus applied Gate voltage (solid). Again semiconductor capacitor (dashed) and oxide capacitor are additionally shown.

Finally, I want to show the basic circuit model of the MIS structure based on this charge model. Even though this model is widely known, it is very important to be understood for the conductive measurement analysis which is based on a slightly more extended circuit including the series resistance of the bulk material.

From above analysis it is shown that the total charge in the MIS structure is given by

$$Q = -Q_s - Q_f - Q_{\text{int}} . \tag{2.16}$$

Based on this charge the total capacitor is

$$C(V_a) = \frac{dQ}{dV_a} = \frac{dQ/dV_s}{dV_a/dV_s} = \frac{\frac{d}{dV_s}\left(-Q_s - Q_f - Q_{\text{int}}\right)}{\frac{d}{dV_s}\left(V_s - \frac{Q_s}{C_{ox}} - \frac{Q_{\text{int}}}{C_{ox}}\right)} . \tag{2.17}$$

By changing the charges to there equivalent capacitors as

$$C_s = -\frac{dQ_s}{dV_s} \quad \text{and} \quad C_{\text{int}} = -\frac{dQ_{\text{int}}}{dV_s}, \tag{2.18}$$

the final capacitance formula is

$$C = \frac{C_s + C_{\text{int}}}{1 + \frac{C_s}{C_{ox}} + \frac{C_{\text{int}}}{C_{ox}}} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_s + C_{\text{int}}}}. \tag{2.19}$$

Equation 2.19 shows the above described circuit in figure 2.6, for neglected interface charges. In chapter 3 this model will be expanded and conductivities will be added for integrating interface traps. In contrast to the real behavior of interface traps, this shows advantages, since the frequency response of a single trap level can be modeled more accurate by a resistive-capacitive circuit.

2.3.2. Interface Properties

In the previous section I already mentioned the flatband voltage shift by the given formula 2.14. Here I will discuss the charges and how they act by simple physical description.

The atoms on the surface of the epitaxial GaN layer can not have the same bonding structure than inner crystal atoms. Therefore bonds of Ga or N atoms are unsaturated and provide different energy states for electrons, which also lie within the band gap. This means that electrons can be placed at energy positions at the surface, where they actually can not exist within the bulk. Therefore those electrons, once trapped in an interface state have a stable position. In an n-type GaN material, electrons can easily fill surface states below the band gap, but those states can not be emptied, since hole carriers, which are necessary for recombination do not exist and the required thermal energy is too high for deep traps. This behavior can be described by the capture and emission time of carriers [75]. The emission time depends on the trap capture cross section σ, the thermal velocity of the carrier, the intrinsic carrier density and the exponential dependence of trap energy E_t to the mid band gap E_i (intrinsic energy level).

$$\tau_e = \frac{1}{\sigma_{trap} v_{th} n_i} \cdot e^{-\frac{E_T - E_i}{kT}} \tag{2.20}$$

In contrast the capture time does not depend on the energy level of the trap, since the electrons fall into the trap from the conduction band.

$$\tau_c = \frac{1}{\sigma_{trap} v_{th} n_s}, \tag{2.21}$$

where n_s is the (volume) carrier concentration at the surface. By describing the number of interface charges, the surface potential first leads to the surface carrier concentration, which than results into a dynamic property of the trap filling mechanism. I will discuss this behavior in detail in section 3.1.3 after the characterization techniques have been described.

Another type of charges are the fixed oxide charges. Their contribution is constant, since they do not change their occupation with the surface potential of the GaN surface. As mentioned in previous chapters, the polar nature of III-N materials provides extra fixed charges, which are strongly depending on the temperature. Additionally, fixed charges occur also in the dielectric itself but in comparison to silicon MOS capacitors this contribution seems to be less significant on nitride materials. Generally the effect of the fixed charges can be modeled as

$$Q_f = \int_0^{W_{ox}} \left(1 + \frac{x}{W_{ox}}\right) \cdot \rho(x) \cdot dx, \tag{2.22}$$

where charges further away from the metal contribute more than those which are closer [76]. In equation 2.22 Wox is the thickness of the oxide and ρ(x) is the distribution function of fixed charges through out the Gate insulator. As we can assume to have most fixed charges at the interface, within an atomic layer the formula can be simplified to

$$Q_f = \rho(x)\big|_{x=0} = Q_{dielectirc} + Q_{polarization}. \tag{2.23}$$

This is simply the sum of fixed charges in the dielectric and the polarization charges. Matocha et al. showed that the second component depends on a pyroelectric charge coefficient of 3.7×10^9 q/cm^{2}K for a silicon oxide interface, causing 1.1×10^{12} q/cm^2 fixed charges at room temperature [28].

3. Characterization Techniques

Before describing the interface results, a detailed introduction about the applied characterization methods based on the theoretical knowledge from the previous chapter is presented. This implies a detailed description of the interface characterization methods, which is divided into two parts. First, the capacitive study shows the characteristic following the derivation in chapter 2.3 of a basic MIS structure and second, a conductive study, which became one of the standard methods in wide band gap semiconductor, due to numerous problems of other CV characterization methods.

Furthermore the characterization of the field effective mobility Gated Hall measurement and Schottky barrier transistor characterization is discussed at the end of this chapter.

3.1. CV Measurement in GaN

The capacitive measurement method is such a well understood and commonly used technique that it can be applied for a wide range of characterizations of the bulk and the interface of a MOS structure. As we apply the knowledge from silicon on GaN, the techniques remain same but the characteristic changes, because of the wide band gap and other compound properties. Therefore the commonly know CV method using high and low frequency measurement is not applicable anymore. Also the common interface state extraction method by Terman does not supply accurate results, even though it is used in several reports [49, 51].

New techniques using UV light illumination, which supplies an over band gap energy for carriers in the semiconductor and allows the generation of electron-hole pairs, appear in several recent reports [21, 54, 64]. For investigations of the interface state distribution over the band gap the AC conduction method is presented in chapter 3.1.2 which provides an extremely sensitive measurement in one half of the band gap [76].

3.1.1. Capacitive Method

One of the basic extraction methods for interface states is to use the hysteresis caused by charged

and uncharged states across the band gap. The idea is simply to compare the flatband voltage between to different measurements, including and excluding interface charges and contribute this shift to the net interface trap concentration. Therefore the capacitive curve is measured in darkness from accumulation to deep depletion. While the Gate potential is kept constant in depletion, UV light which contains photons with over band gap energy is exposed on the capacitance to create electron-hole pairs, emptying the interface traps. After illumination the measurement sweeps back to accumulation. This backwards measurement has to be done fast enough, so that interface traps are not filled during the sweep. As the curve reaches accumulation, electrons fill again the traps at the interface.

The origin of the hysteresis caused by UV light can be explained by figure 3.1. After the capacitance has been in accumulation, electrons have fully filled all interface traps. At flatband voltage (a) a few traps close to the conduction band can be emptied by thermal energy. As the capacitance changes to deep depletion no more traps can be emptied due to the absence of holes in the valence band. Therefore it can be assumed that almost all interface traps are filled during the first measurement sweep. Using the UV light source on the sample, over-bandgap photons are able to create electron-hole pairs in GaN. The created holes can recombine with electrons, collected at the interface, causing the traps to empty (b). After a certain time the interface traps are emptied and the GaN bands are bending further according to the Fermi level shift. If the bending was sufficient inversion carriers are accumulated at the surface. The origin of the inversion hole for this n-type GaN example is again the UV light. The following voltage sweep back to accumulation does not contain charges in the interface trap. In accumulation, a large number of electrons refill the traps and cause the same situation as before the first sweep. Fortunately this time is large enough so that a fast sweep can be done, assuming that no traps are being filled during the measurement.

For analyzing the trap density the flatband capacitor is calculated for the given MIS structure. The thickness of the flatband semiconductor capacitance is equal to the Debye length. Therefore the voltage shift at flatband voltage can be extracted and compared to the theoretical values.

$$V_{FB} = \Phi_M - \chi_s - \left[\frac{E_g}{2} - \frac{kT}{q}\ln\frac{N}{n_i}\right] - \frac{Q_F}{C_{ox}} - \frac{Q_{INT}}{C_{ox}}, \qquad (3.1)$$

The first three terms represent the ideal flatband voltage, comparing the work function of the metal and the Fermi level of the semiconductor. The latter two causes the flatband voltage to shift according to the number of charges and the polarity.

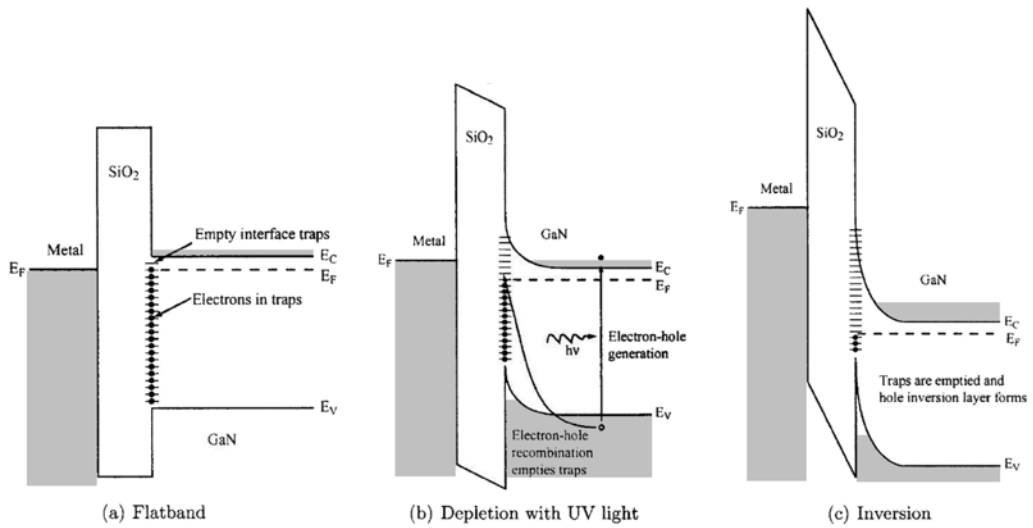

Figure 3.1: Energy diagram of the MOS structure at flatband condition (a), depletion condition with incident UV light (b) and inversion (c).

During the first sweep both interface related charges play a role on the flatband voltage. After emptying the interface traps, Q_{INT} can be neglected which allows the extraction of the interface charges by

$$Q_{INT} = C_{ox}(V_{FB,Inv.\rightarrow Acc.} - V_{FB,Acc\rightarrow Dep.Depl.}) . \qquad (3.2)$$

Taking the same flatband voltage and compare it to the ideal theoretical value leads to the fixed charge density by

$$Q_F = C_{ox}\left\{\left[\Phi_M - \chi_s - \left[\frac{E_g}{2} - \frac{kT}{q}\ln\frac{N}{n_i}\right]\right] - V_{FB,Inv.\rightarrow Acc.}\right\}. \qquad (3.3)$$

If the oxide capacitor C_{ox} includes the area of the capacitor, the interface and fixed charges are normalized.

The mechanism described for n-type GaN works similar for p-type GaN. Since in accumulation a

large number of holes keeps the interface traps empty the first sweep contains only fixed charges. In deep depletion UV light causes electrons in the conduction band, which can fill the interface traps and make them detectable during the reverse sweep back to accumulation. The reverse shifting effect can be qualitative seen in figures 3.2.

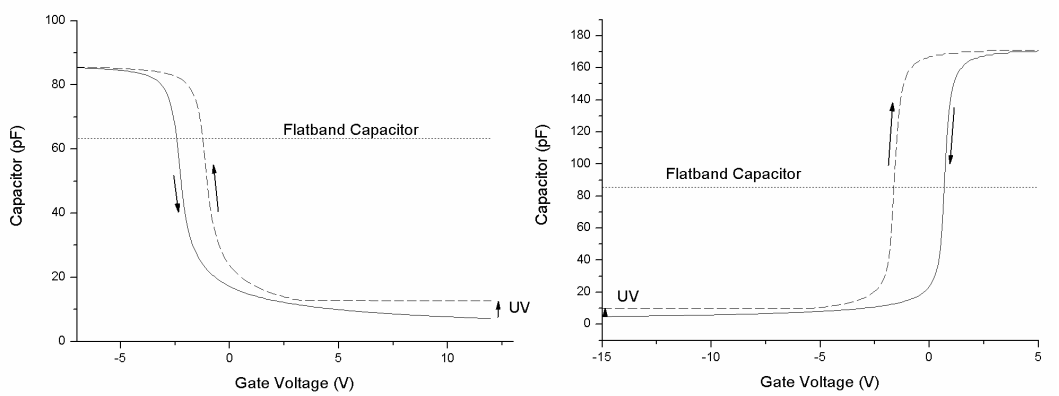

Figure 3.2: Calculated CV Graph showing the Flatband shift induced by oxide constant charges on n-type GaN (right) and p-type GaN (left).

3.1.2. Conductive Method

A very sensitive method is the conductive method for calculating the interface states. The sensitivity is primarily improved by the simple fact that the conductivity directly results into the interface density, while in the capacitive method the interface capacity is parallel to the interface effective capacity. This much smaller subtraction value can often contain large errors.

Nevertheless, also the conductivity method requires several extractions summarized in figure 3.3, where C_m and G_m are the measured values, C_{ox} is the oxide capacitor, R_s is the series resistive component, C_c and G_c are the correct capacity and conductivity and Cp and G_p the final corrected parallel capacity and conductivity of the depletion region. The parallel conductivity indicates the interfaces states during the sweep from flatband to depletion, which will be described after the details of the extraction.

Therefore we start with circuit (a), which shows the measurement circuit of the parallel capacitor and the conductivity measured at several frequencies up to 1MHz by an LCR meter. The theoretical derivation of the capacitive behavior already showed that in the accumulation region the MIS structure reduces itself to the oxide capacitor, resulting into the circuit (b). Therefore it

is a simple method to take measurement values from the accumulation and extract the series resistor, which is a series component of the actual parallel interface states conductivity.

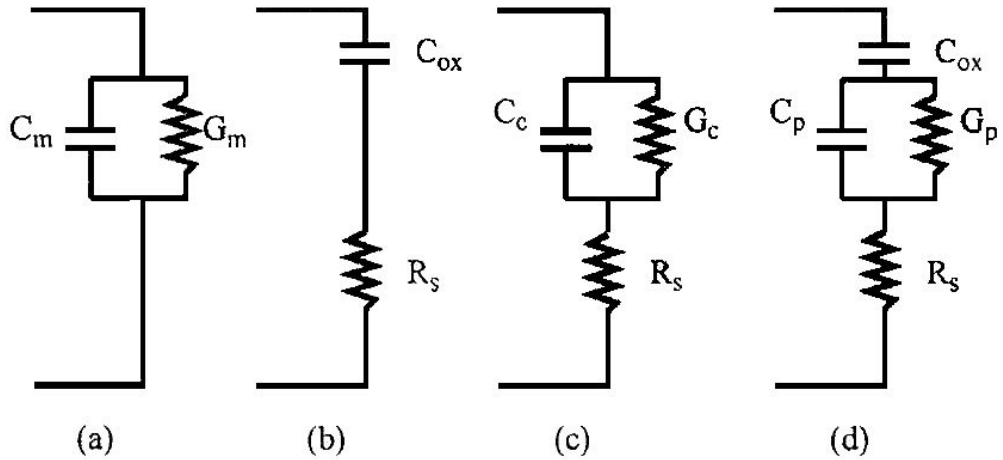

Figure 3.3: Equivalent circuit models used for conduction measurement analysis: measurement circuit (a), circuit in accumulation, where the semiconductor capacitance does not play a role (b), simple MOS circuit of extracting the corrected MOS capacitance values Gc and Cc (c) and total equivalent circuit given explicit Gp.

Using the complex circuit analysis and setting circuit (a) equal to (b) results into

$$R_s = \frac{G_m}{G_m{}^2 + \omega^2 C_m{}^2} \tag{3.4}$$

$$C_{ox} = C_m\left[1 + \frac{G_m}{\omega \cdot C_m}\right] \tag{3.5}$$

for accumulation. Those values are used as constants in the following circuits. The measured capacity and conductivity can be corrected for the series component. The equations are again derived by comparing circuit (a) and (c) and the solution is given by

$$C_c = \frac{(G_m{}^2 + \omega^2 C_m{}^2)C_m}{a^2 + \omega^2 C_m{}^2} \tag{3.6}$$

$$G_c = \frac{(G_m{}^2 + \omega^2 C_m{}^2)a}{a^2 + \omega^2 C_m{}^2} \tag{3.7}$$

with

$$a = G_m - (G_m{}^2 + \omega^2 C_m{}^2)R_s \tag{3.8}$$

A comparison between the corrected and the measured conductivity is plotted in figure 3.4. In general the corrected capacitor differs less on the series resistance ($C_c \approx C_m$) than the conductivity, since the series resistance dominates the accumulation region. However, this extraction is quite simple as the series resistance is an easy to extract value. Also, it should be noticed that in certain cases the series resistance can reduce the capacitive value in accumulation, which will be discussed in chapter 5.1 for high resistive p-type GaN, where the bulk resistance plays a dominant role.

In the next step, the impact of the oxide capacitor should be extracted by setting circuit (c) equal to (d). Additionally, the resulting parallel conductivity is normalized by the radial frequency, which changes its unit to Farad. The solution is given by

$$\frac{G_p}{\omega} = \frac{\omega \cdot C_{ox}{}^2 \cdot G_c}{G_c{}^2 + \omega^2 (C_{ox} - C_c)^2} \tag{3.9}$$

Plotting this function over frequency or the Gate voltage, shows the resonant peak of the interface states according to a certain energy level (surface potential). The normalization by frequency in equation 3.9 is especially necessary for the frequency graph, since no peak can be observed without normalization. The peak value and the peak width are necessary to determine the actual interface states by

$$D_{it} = \frac{\left[\frac{G_p}{\omega}\right]_{peak}}{q^2 A \cdot f_D}, \tag{3.10}$$

where q is the elementary charge of an electron, A is the area of the measured capacity and f_D a function of the standard deviation of the band bending. This value is found by the normalized G_p from equation 3.9 plotted over the dimensionless band bending function

$$v_s = \frac{qV_S}{kT}, \tag{3.11}$$

where V_s is the surface potential according to the Gate voltage (refer to chapter 2.4.1). The width of this graph expresses the standard deviation. Nicollian et al. provided the theoretical background for this theory of a single trap level and described the relation of the parameter f_D on the standard deviation [76]. Typical values for f_D are found between 0.2 and 0.5.

The above described analysis leads to a single point of interface states charges between the flatband potential and the mid band gap of the semiconductor. By varying either the frequency or the temperature, changing interface trap energy levels become dominant. Also, shifting the Gate voltage, changes the surface potential and hence the Fermi level position. Measuring over a wide frequency range the whole density distribution of interface states can be found.

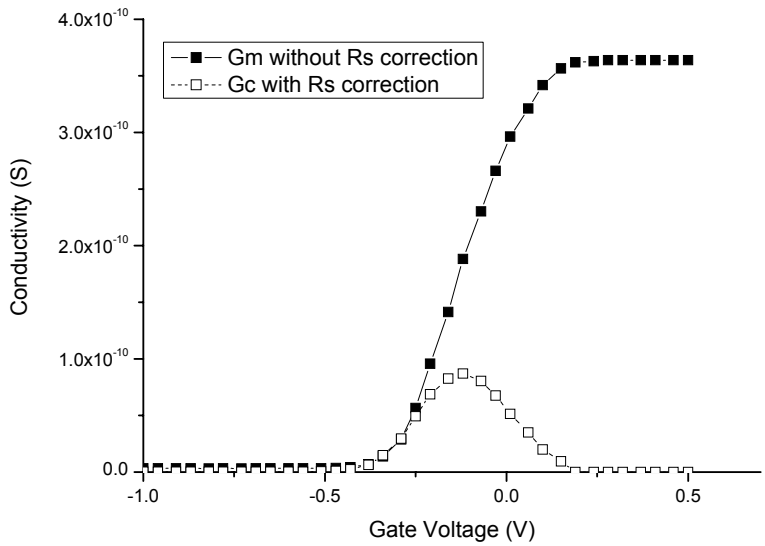

Figure 3.4: Comparison between the conductivity of the MOS interface before and after series resistance correction.

3.1.3. Dynamic Behavior of Interface States

In the previous sections I assumed that the traps always respond to the measurement unless they were emptied by light illumination. In 3.1.1 for the capacitive measurement into deep depletion it was assumed that all interface states are filled, while after UV light illumination the interface states were assumed to be empty for the whole measurement until accumulation. In the

conduction method in 3.1.2, this was a bit more differentiated since the respond of traps at a certain trap energy (respectively the Gate bias) was detected under different frequencies.

A brief introduction into these dynamic behaviors was discussed in section 2.3.2 by the trap capture time (equation 2.21) and the trap emission time (equation 2.20). The trap emission time depends on the thermal energy of an electron and its energy difference to the conduction band (as mentioned earlier, we assume to have no holes in n-type GaN). Therefore traps close to the valence band can emit easier to the conduction band. The calculated plot for this behavior is shown in figure 3.5 for a typical n-type GaN layer with 10^{16} cm^{-3} carrier concentration.

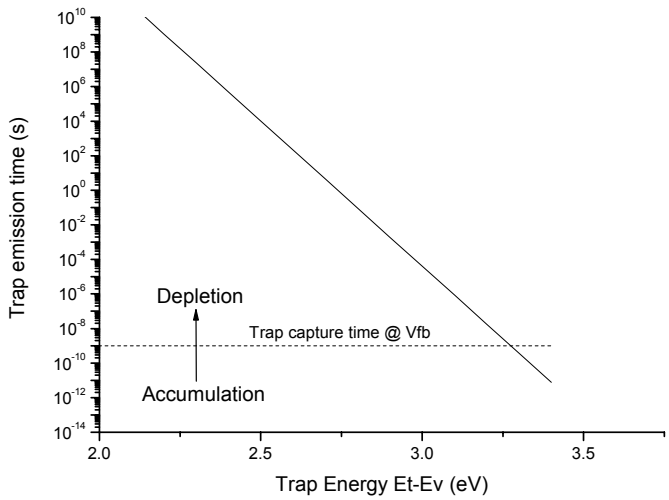

Figure 3.5: Calculation of the trap emission time versus Trap Energy relative to the band gap (solid line). As a reference the capture time for flatband condition is drawn (dashed line).

The capture time, plotted in figure 3.6, depends only on the supplied carriers at the surface, which are able to be captured into traps. The surface carrier concentration in a GaN MIS capacitor can be described by

$$n_s(V_s) = N \cdot e^{\frac{qV_s}{kT}}, \tag{3.12}$$

where V_s is the surface potential, N is the doping concentration and q/kT is the thermal voltage. The relation between the surface potential and the Gate potential was already shown in equation 2.15.

According to the capture and emission process, the interface traps can be filled or emptied. If the capture time is shorter, it dominates the emission and the responding traps are filled. However at the band edge the emission timer is shorter and the interface traps have a higher chance to be empty. Both conditions do not respond to the capacitive measurement, since always empty and always filled traps have no charge transfer (= capacitance). The traps that are mostly responding on the AC Gate amplitude are those with same capture and emission time. This energy level can be found by setting the two equation equal and including the surface carrier concentration from equation 3.12.

$$\frac{1}{\sigma_{trap} v_{th} n_i} \cdot e^{-\frac{E_T - E_i}{kT}} = \frac{1}{\sigma_{trap} v_{th} N \cdot e^{\frac{qVs}{kT}}} \tag{3.14}$$

can be reduce to

$$\frac{N}{n_i} e^{\frac{qVs}{kT}} = e^{-\frac{E_T - E_i}{kT}} . \tag{3.15}$$

Inserting the Fermi level into the equation instead of the ratio between the electrons in the conduction band and the intrinsic carriers, gives the final condition

$$E_F + qV_S = E_T\big|_{\tau_E = \tau_C} . \tag{3.16}$$

The corresponding trap energy is therefore directly depending on the surface potential. Equation 3.16 is directly used for the determination of the trap energies in the conductive measurement. Since equation 3.12 and the assumption in 3.15 included the Boltzmann equation, the result is only valid for energies below the Fermi level (for n-type). For negative surface potential the emission time dominates and the traps can not be measured. The conduction measurement is therefore valid for values below the flatband voltage.

If the surface is depleted the corresponding trap energy gets deeper into the band gap. Since those traps have lower responding times, the resonant frequency decreases. Due to the limit of the measurement the characterization is limited to a certain depth. The frequencies required for certain energies can be seen from time constant in figure 3.5. The sensitivity of the conduction method is therefore only applicable for a quite small range of about 1 eV of both sides of the band gap.

The UV method measures only the overall traps and therefore includes all deep traps to the opposite band edge. However the sweep back into accumulation is accompanied by increasing capture time causing traps to be added in the result. Above flatband voltage, the measurement

sweep is probably to slow to include the fast traps near the band edge. Nevertheless, this method gives a comprehensive comparison for the rest of the bandgap below the flatband voltage.

Terman's method, which was not used in this work, suffers from the fact, that no real low and high frequency performance exists in GaN. Therefore and including the fact that the sensitivity is low in direct capacitive measurement, the applied frequencies should be very high and the capacitive error very small. Otherwise, the result is only valid in a very short range according to the energy in figure 3.5. Even though, this method is applied in several reports with usually better results showing its underestimation.

In conclusion, the dynamic behavior of interface traps and their response behavior to the measurement conditions, as sweeping speed, measurement frequency or Gate voltage, respectively surface potential, are from enormous importance for the qualitative examination of the interface. The fact that the observation is limited to a very small range of the bandgap, makes it clear, at any measurement must be considered very carefully.

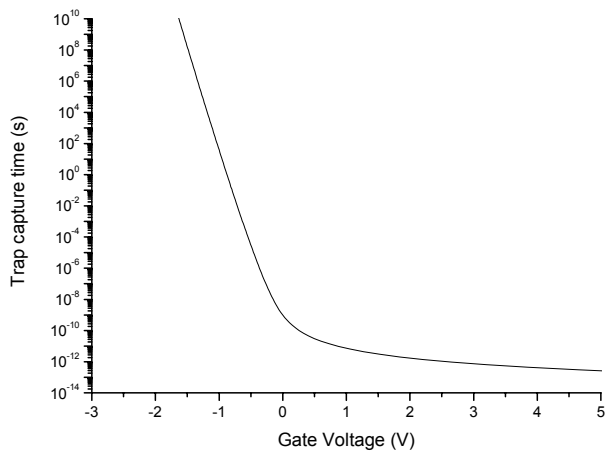

Figure 3.6: Calculation of the Trap capture time in dependence of the Gate voltage, the surface potential and the surface carrier concentration, respectively. The flatband voltage is at zero Gate voltage assuming ideal case.

3.2. Hall and Gated-Hall Measurement

Until this chapter, the main focus of the interface characterization lied on the quantitative amount of oxide charges in the interface. A high interface charge density does not only requires high

switching voltage in order to create the same amount of channel charges, but also provides enhanced scattering for the channel electrons. These electrons, generated directly below the Gate oxide, are affected by the horizontal field for transportation through the crystal and also by the vertical field from the Gate. As electrons are towed toward the Gate electrode, they collide with effective charges on the interfaces. Therefore the field-effective channel mobility is one the most crucial parameters in MISFET devices. It was already discussed, that HEMT have much higher channel mobilities, since they do not require electrons generated by the Gate potential and further are free of ionized doping atoms in the channel region. The following part will explain the standard configuration of the Hall measurement and the theoretical relation between the Hall mobility and the conductivity mobility [77-79].

The Hall effect, discovered by Edwin Hall in 1879, describes the potential difference (Hall voltage) due to the Lorentz force in conductive materials. The configuration, shown in figure 3.7 consists of a horizontal current flow and a horizontal magnetic field in a thin probe. The following derivation for the Hall effect restricts the magnetic field to the z-direction and the current flow due to the applied voltage V_a to the x-direction. The Hall voltage can be measured perpendicular to both directions in y-direction.

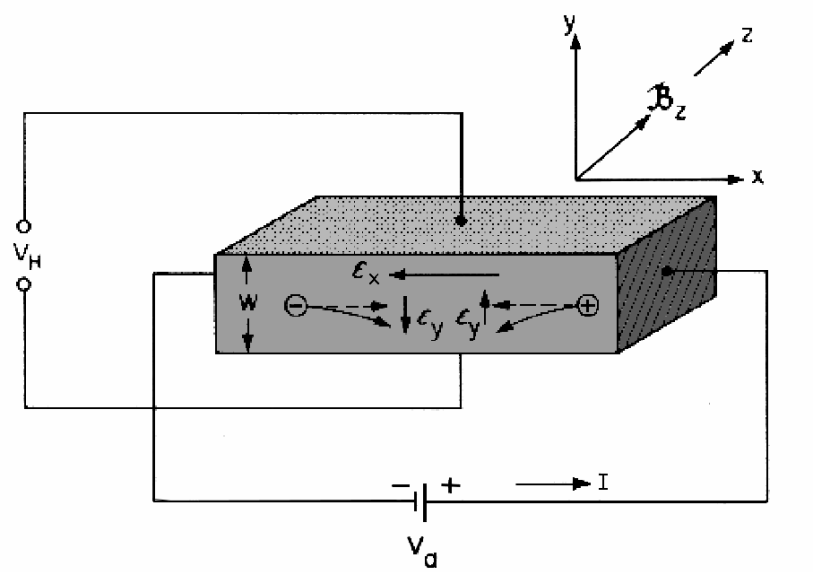

Figure 3.7: Model of Hall measurement: electric field in x-direction, magnetic field in z-direction, Hall voltage in y-direction.

Using the derivation from the Boltzmann Equation, the distribution of states in the k-space can be written as

$$f = f_0 + \frac{\partial f_0}{\partial E}\vec{v}\cdot\vec{G}\,, \tag{3.17}$$

where f_0 is the distribution at thermal equilibrium, E is the Energy, v the velocity of the carriers and G represents a term proportional to the force that acts on the electrons. In equation 3.18 G is defined for electric and magnetic fields but without carrier concentration gradients or temperature gradients, where q is the elementary charge, τ_m is the momentum relaxation time, m* is the effective mass and therefore a tensor and B is the magnetic flux density. The momentum relaxation time describes how fast a change in the distribution function return to the thermal equilibrium.

$$\vec{G} = q\tau_{m\cdot}\left[\frac{\vec{E} - \frac{q\tau_{m\cdot}}{m^*}(\vec{E}\times\vec{B}) + \left(\frac{q\tau_{m\cdot}}{m^*}\right)^2\vec{B}\cdot(\vec{E}\cdot\vec{B})}{1+\left(\frac{q\tau_{m\cdot}}{m^*}\right)^2\vec{B}\cdot\vec{B}}\right]. \tag{3.18}$$

Equation 3.18 involves several terms, where the first in the nominator involves the ohmic contribution, the second describes the field due to the Hall effect and the third one together with the denominator describes the magneto resistive effects. Since those last terms are second order effects of the magnetic field, they will be neglected in the derivation of the Hall effect, which is valid for the assumption that only small magnetic fields are applied. Solving this equation and using the result in equation 3.17 for the Fermi-Dirac statistic shows the electron distribution under applied fields. It is known that in thermal equilibrium the total velocity of the carriers vanishes. This changes after the distribution differs from its equilibrium position as can be shown by solving

$$v = \frac{\int_0^\infty \vec{v}f\cdot dx}{\int_0^\infty f\cdot dx} \tag{3.19}$$

where x is

$$x = \frac{E - E_c}{kT} \tag{3.20}$$

the normalized energy difference from the conduction band energy Ec. Equation 3.19 represents that total integral over the whole carrier distribution in the conduction band. Using the result from equation 3.17 into 3.19 gives the drift velocity of the carriers

$$v_d = \frac{2}{3m^*} \frac{\int_0^\infty \vec{G}\left(-\frac{\partial f_0}{\partial x}\right) x^{3/2} dx}{\int_0^\infty f_0 \cdot x^{3/2} dx}, \tag{3.21}$$

The drift velocity is directly related to the current density by

$$\vec{J} = -qn\langle v \rangle, \tag{3.22}$$

where n is the carrier concentration. Solving equation 3.21 for the vector G from 3.18 results into

$$\begin{aligned} \vec{J} &= \frac{q^2 n}{m^*} \left\langle \frac{\tau_{m\cdot}}{1+(\omega_c \tau_m)^2} \right\rangle \vec{E} - \frac{q^3 n}{m^{*2}} \left\langle \frac{\tau_m^2}{1+(\omega_c \tau_m)^2} \right\rangle \vec{E} \times \vec{B} \\ &\cong \frac{q^2 n}{m^*} \langle \tau_m \rangle \vec{E} - \frac{q^3 n}{m^{*2}} \langle \tau_m^2 \rangle \vec{E} \times \vec{B} \end{aligned}, \tag{3.23}$$

if the magnetoresistive terms are neglected, as mentioned before. The second line of equation 3.23 shows a simplification for the denominator, where

$$\omega_c = \frac{q \cdot \left|\vec{B}\right|}{m^*}, \tag{3.24}$$

is the cyclotron frequency, which is small due to a small assumed magnetic field. The first term in equation 3.23 is the ohmic current due to an external electric field, while the second term shows an additional current due to the Lorentz force, dependent on the ex-product of the magnetic an the electric field. As described in figure 3.7, the electric field is only defined in the vertical direction (z), which can be noted as

$$\vec{B} = B \cdot \vec{e}_z \tag{3.25}$$

Therefore the euclidic components of the current density can be rewritten as

$$\vec{J}_x = \frac{q^2 n}{m^*}\langle\tau_m\rangle\vec{E}_x - \frac{q^3 n}{m^{*2}}\langle\tau_m^2\rangle\vec{E}_y \times \vec{B}_z$$
$$\vec{J}_y = \frac{q^2 n}{m^*}\langle\tau_m\rangle\vec{E}_y - \frac{q^3 n}{m^{*2}}\langle\tau_m^2\rangle\vec{E}_x \times \vec{B}_z \qquad (3.26)$$
$$\vec{J}_z = \frac{q^2 n}{m^*}\langle\tau_m\rangle\vec{E}_z$$

Using the fact that the current flow is restricted to the x direction, allows to express the component E_x out off equation 3.26-2. Finally this result used in equation 3.26-1 and again neglecting the second order magnetic term gives the current density in direction of the external electric field in dependence of the magnetic field and the vertical field due to the Hall effect.

$$\vec{J}_x = -qn\frac{\langle\tau_m\rangle^2}{\langle\tau_m^2\rangle}\frac{E_y}{B_z}\cdot\vec{e}_x \qquad (3.27)$$

This is the final equation for the Hall effect, which can be detected by measuring the Hall potential, due to E_y. Defining a Hall constant

$$R_H = \frac{E_y}{J_x B_z} = -\frac{1}{qn}\frac{\langle\tau_m\rangle^2}{\langle\tau_m^2\rangle} \qquad (3.28)$$

shows that the carrier concentration n can be measured directly out of the measurement relation. If then the Hall constant (resistive) is compared with the conductivity of a semiconductor, it turns out, that the Hall mobility is related to the conduction mobility by

$$\mu_H = \mu_c\frac{\langle\tau_m\rangle^2}{\langle\tau_m^2\rangle}, \qquad (3.29)$$

where r_H is the Hall factor, which can be written as

$$r_H \equiv \frac{\langle\tau_m\rangle^2}{\langle\tau_m^2\rangle} = \frac{3\sqrt{\pi}}{4}\frac{\Gamma[2r+3/2]}{\Gamma[r+3/2]^2}. \qquad (3.30)$$

The factor is used to model the relaxation time utilizing the model function

$$\tau_m = \tau_0 \cdot x^r. \qquad (3.31)$$

The momentum relaxation time depends on the scattering mechanism and therefore shows

different values of r of various mechanisms. The Hall factor can be ~1, which is the case when the Hall mobility and the conduction mobility is almost same. However, for certain scattering the Hall mobility is not representative for the conductivity mobility.
In case of GaN MIS structure, the channel carriers are dominated by the field effective scattering on ionized surface charges. Certain reports showed that in this case the values between channel and Hall mobility do not vary very much [17].

In order to measure the Hall mobility of a normal semiconductor piece, four test points are required, showing an ohmic transfer characteristic. In case of the Hall measurement on the electron carriers in a p-type substrate, the contacts should be low resistive for electrons but blocking for holes. The usual MOSFET structure provides therefore n^+-Source and -Drain regions, which are connected to the channel region below the Gate and provide an ongoing electron channel through the transistor if the channel is turned on. The Schottky barrier transistor, described in the next chapter, simplifies this by using a Schottky barrier to the p-type material with a workfunction similar to the conduction band. Hence, electrons can travel from Source to Drain with a small barrier by thermionic emission. Further discussion on this will be given in the next subchapter. In order to measure the field-effective Hall mobility a Gate metal is placed on top of the structure after a dielectric material for isolation. The fabrication of this structure is explained in chapter 4.2.2. In my work I compared two devices using n-type and p-type substrate. While the p-type structure measured the inverted electrons, the n-type device restricts to the accumulation carriers below the Gate. In order to neglect the bulk carriers, which are measured parallel to the channel, the channel carrier density must be efficiently high.

3.3. Characterization by Schottky Barrier Transistor

Schottky barrier MOSFETs are currently under research for sub 0.1 μm devices and great performances could be already shown down to a few nanometer Gate length [80-82] in silicon. They are usually fabricated in a self-aligned structure using metal silicides as Source Drain region. After Gate definition, instead of Source/ Drain doping, a metal layer is deposited which forms a silicide structure during annealing. This structure can diffuse below the Gate and hence

provides a sufficient connection to the channel. Several short-channel related issues can be improved, since the metal-silicide layer has comparable properties to a highly doped silicon layer. This formation of silicides is a great advantage, which unfortunately does not exist in GaN. Therefore overlapping metal layers must be deposited and isolated by the Gate dielectric [83]. A schematic design is shown in figure 4.10 and discussed in chapter 4.2.3. A disadvantage of this configuration is increasing oxide capacitor in the edges caused by the Source and Drain metal. These areas show a decreased field and therefore a thinner electron channel.

The general concept of the Dual Schottky barrier is pointed out in figure 3.8. The upper band diagram shows the case for zero Gate bias and zero Drain bias. The Schottky barrier of Source and Drain is similar to the bandgap energy, since the metal workfunction (aluminium) is almost same to the electron affinity of GaN and the bulk material is p-type doped. Applying forward (positive) voltage on the Gate electrode increases the energy of the bulk below the Gate and lowers the barriers to Source and Drain. After sufficient Gate bias, electrons are created in the channel at an energy level of the conduction band. Those electrons are at a similar energy than the metal workfunction and can therefore easily be emitted into the metal by thermionic emission. The last band diagram shows the case of positive Drain voltage, providing electron flow from Source to Drain.

The modeling of the transistor was performed using the simple SPICE 1 model for the Drain current approximation. Tested devices had Gate lengths from 3 to 30 µm and therefore no short channel characteristic was predicted. In order to compare the mobility with the results from the Hall measurement, the channel resistance was extracted using a graph similar to the one in figures 3.9. The total resistance based on the Drain current and voltage is plotted for devices with different length assuming a silicon oxide Gate oxide of 12 nm and constant channel mobility for all devices and Gate voltages. Since the total resistance is composed of the Gate length independent Source and Drain resistance and the channel resistance, the channel resistivity can be taken from the slope of the graph while the Source and Drain resistance is equal to half of the crossing point of all the graphs with the y-axis. A similar method is used for Gated-Transmission Line Measurement (TLM) first described by Baier et al. [84].

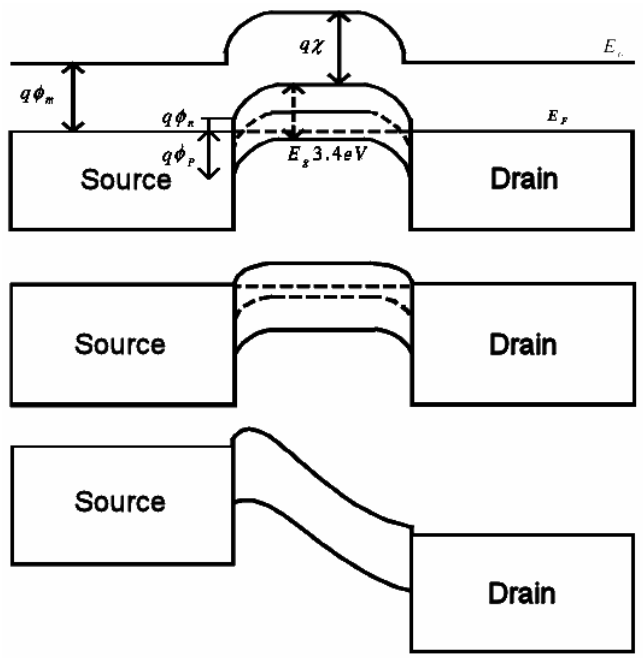

Figure 3.8: Schematic Band diagram of Schottky barrier transistor from Source to Drain for thermal equilibrium (upper), barrier lowering by Gate voltage (middle) and forward current by $V_{DS} > 0$ and turned no channel.

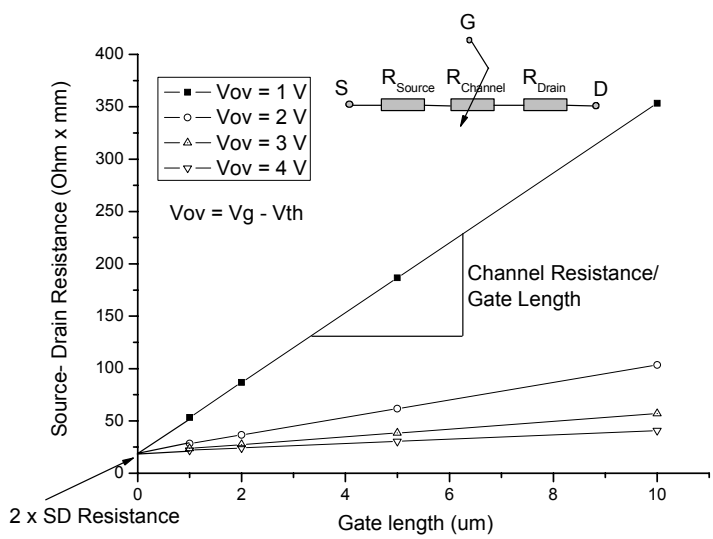

Figure 3.9: Modeling of the channel resistance from Schottky barrier transistor by comparing the total Source – Channel – Drain resistance for different Gate lengths.

From the extracted resistivity, the field-effective mobility is found by comparison with the calculated channel electrons based on the applied Gate bias [85].

In conclusion the Hall measurement was described under the assumption of small electric fields in the channel and relatively large Gate length. In contrast the transistor has a higher channel field, due to the shorter channel and the applied field Source-Drain voltage. Both device are in linear region for the measurement.

4. Fabrication

In this part the details of the processing technology are presented. A first part will focus on the technologies itself and the later one describes each of the used devices individually. In fabricating the devices, several process parameter tests have been done, in order to get acceptable results. However only the final process data are shown, which were used as a standard process technique for our clean room facilities. Further discussion includes the measurement setup based on every device. Those results are discussed in the next chapter.

4.1. Technology

The semiconductor fabrication technology used in this work was mainly related to metal-organic chemical vapor deposition (MOCVD) for growth of the GaN substrates and dielectric deposition by plasma-enhanced PECVD and atomic layer deposition (ALD). Beside, standard optical lithography, electron-beam evaporation for metallization and transducer coupled plasma reactive ion etching (TCP-RIE) on GaN or dielectrics was applied. Later ones are standard processes in today's clean room fabrication and are not further discussed, except the used process parameters in chapter 4.2. The following two parts of this sub chapter will describe the MOCVD system and its functionality on GaN growth. Further the mechanism of dielectric deposition techniques are enclosed with emphasis on the atomic layer controlled ALD.

4.1.1. Metal-Organic CVD

The use of metal-organic chemical vapor deposition (MOCVD) became the optimum tool for high growth quality substrates and a commercially acceptable output. Therefore fabrication of compound epitaxial structures is mainly done by this technique. While MBE had some advantages in the early stage of epitaxy, MOCVD results could show comparable data, including an exact layer transition and low incorporation for high mobility substrates.

The difference from a normal CVD to a MOCVD is the use of metal-organic precursors which

are necessary to provide the metallic components (in case of GaN gallium) in the gas phase for the deposition. Most common used sources for the III-N family are trimethylgallium (TMGa), trimethylauminum (TMAl), trimethylindium (TMIn). Typical grown GaN layer show n-type characteristic, even though the intrinsic carrier concentration is neglectable at room temperature. These electrons in the order of 10^{16} cm^{-3} are provided by dislocations and impurities in the crystal causing donor-like states in the bandgap. In order to achieve higher n-type doping concentrations silane (SiH_4) can be added to the growth, causing additional doping by silicon atoms. As silicon is a group IV element and the fact that it replaces Ga (group III) atoms in the crystals under normal conditions, an additional electron per silicon atom is provided. The growth of p-type GaN layers is done by adding biscyclopenntadienyl-magnesium (Cp_2Mg) into the process, which acts as a deep level acceptor. This deep level behavior of magnesium causes low doping efficiency in the order of 1%.

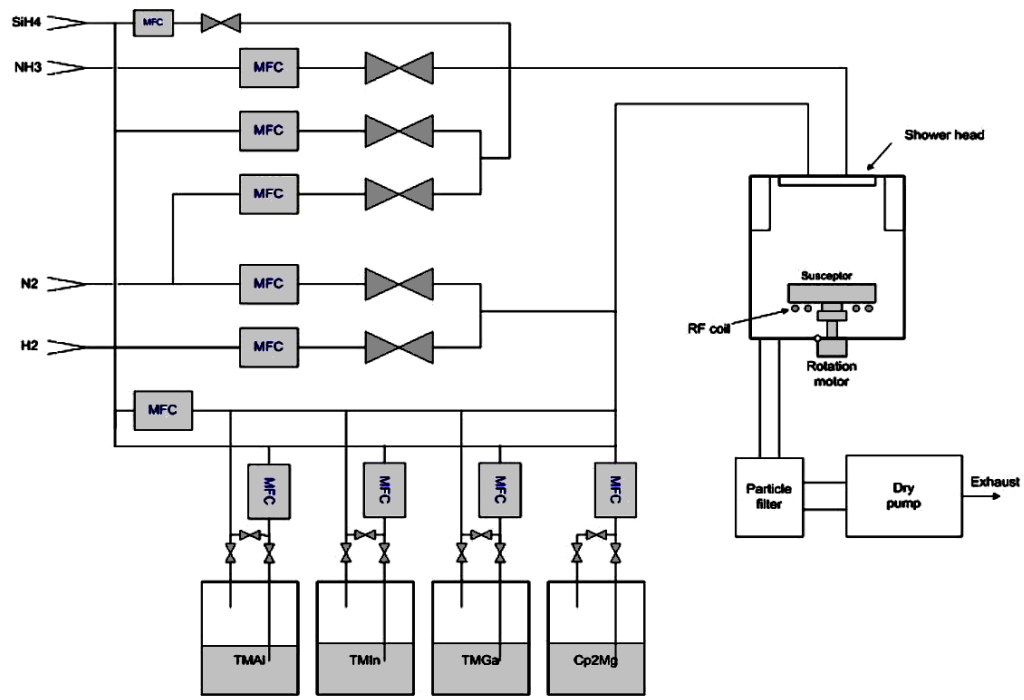

Figure 4.1: Schematic of the MOCVD reactor and its components.

A schematic view of our MOCVD system is shown in figure 4.1. It is a SYSNEX MOCVD LE-260NT with a vertical reactor and separate group V and group III input flows. The reactor itself contains a shower head for the vertical flow input, a graphite susceptor for six 2-inch wafers at

the bottom and an underlying RF coil heater. In the whole outline of the chamber, including the shower head, a cooling system helps to prevent gas reactions on the chamber walls.

The gas line system contains separate control for the carrier gases nitrogen and hydrogen as well as silane (used for doping) and ammonia, which provides the nitrogen atoms during the growth. The precursors are placed in temperature controlled containers and can be transferred into the chamber by either nitrogen or hydrogen.

Our standard growth sequence for GaN epilayer growth started with a thermal etch at 1125°C under nitrogen flow to clean the substrate. This is followed by a first low temperature buffer growth at 545°C and a pressure of 100 torr to provide a nucleation layer. This is followed by another layer of GaN at normal growth temperature of 1060°C but higher pressure of 300 torr causing a very slow growth rate. After this, the final 2.2 µm GaN buffer at the same temperature and a pressure of 100 torr is grown. In case of the growth of p-type GaN layer, additional growth with Mg doping is added afterwards. Typical results on Hall measurements of these substrates show mid 10^{16} cm^{-3} of electron concentration and mobilities in the 400 cm^2/Vs for n-type GaN and mid 10^{17} cm^{-3} of hole concentration with mobilities around 10-20 cm^2/Vs for p-type GaN.

4.1.2. Dielectric Deposition

Plasma Enhanced Chemical Vapor Deposition (PECVD)

Dielectric deposition from PECVD is generally used after metallization deposition, which does not allow high deposition temperatures due to damage of the metal layers. In my case silicon oxide deposition is used after metallization of aluminum, which has a melting point of 660°C and therefore any subsequent processing temperatures must be less than 450°C. If a usual CVD system would be used, the deposition rate would be extremely low since the deposition is surface reaction controlled with exponential temperature dependence. In addition the observed film qualities would be porous and show gaps leading to moisture absorption of the film.

Therefore an additional energy source to the thermal energy is required. In case of PECVD, plasma creates this additional source allowing dielectric deposition even at room temperature. In our case we usually use deposition at chuck temperatures of 300°C. For silicon nitride I generally

deposited ammonia-free films. The chemical reaction taking place in the chamber for the two films can be expressed as

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$$

$$SiH_4 + N_2 \rightarrow SiN_x + 2H_2.$$

In figure 4.2 a schematic view shows the structure of a typical PECVD system. The wafers are placed on the bottom plate, which also provides the thermal energy. The plasma is sustained between the lower and the top plate using a generator with 13.56 MHz. Gases are provided by inlets on the side with a low pressure of a few hundred mtorr. The high-energy electrons in the plasma ionize further atoms and sustain therefore the plasma. Once the energetic species reach the surface the reaction occurs very fast. Additional electron, which could escape from the plasma and strike the surface can break bonds on surface atoms and hence increase the reaction.
The usual benefits of the use of plasma enhanced dielectric deposition are good adhesion, good step coverage and uniformity. However the film quality and characteristic, as dielectric constant, refraction index, dielectric strength and etch rate, depends strongly on the applied process conditions.

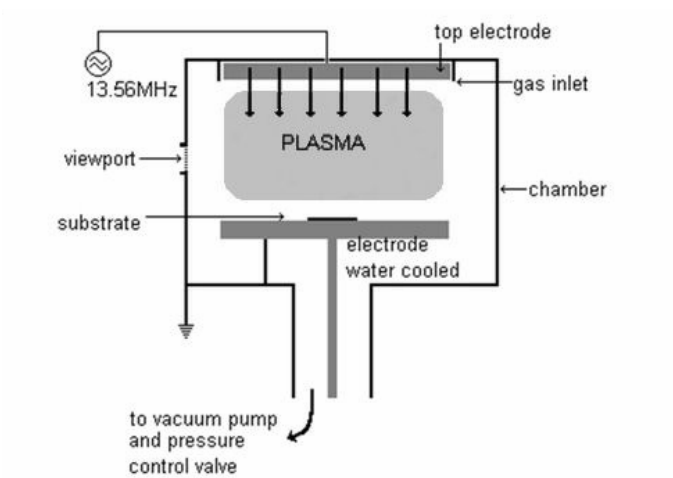

Figure 4.2: Schematic view of a planar PECVD reactor

In this work silicon oxide and nitride was used for the MOS interface on GaN, which is in comparison to the silicon and thermally grown silicon oxide a method with a lot of disadvantages. The interface layer is not as well controlled which increases the number of dangling bonds

causing energetic traps within the bandgap. However PECVD systems are widely used and show several advantages in fabrication which cannot be provided by other techniques.

Aluminum oxide by Atomic Layer Deposition (ALD)

In atomic layer deposition the materials are not grown continuously but in a stepwise process. Using two different mechanisms, which are both self-limited, layer by layer of atoms can be deposited over the whole wafer even for extreme shaped surfaces. Similar to the PECVD, atomic layer deposition is a surface reaction process, but with the difference that the amount of reactive species is limited within one cycle of deposition. Therefore ALD shows the best uniformity and step coverage of all deposition techniques. This is one of the reasons why ALDs are more common used in modern VLSI devices, changing from planar technology to three dimensional structures and requiring deposition on all surface directions.

Several materials from semiconductors to dielectrics and metals can be deposited by atomic layer deposition. One of the major applications are high-k dielectric materials as Al_2O_3, HfO_2, ZrO_2, TiO_2 and there compounds. Using those materials, thin effective Gate materials with high leakage suppression can be provided.

Aluminum oxide can be deposited by using Trimethylaluminum (TMA) and either H_2O or plasma, as it is used in our system. The general advantage of PE-ALD is a lower deposition temperature, a broader range of possible chemistry, denser films and fewer impurities for a higher dielectric constant. Similar to the PECVD additional growth parameter lead to a better process controllability but also make the reaction chemistry and the chamber design more complicated. As mentioned before, precursors used in ALD processes must show self-limited adsorption without self-decomposition in order to guarantee a layer by layer deposition. The reaction occurring in the second step should be aggressive to achieve a fast and full saturation without etching the films or the substrate. The deposition is generally temperature dependent, even though there is a large window (“ALD window”) in which the layer by layer process is possible. For too low temperatures the precursor might either condensate or the thermal energy is no enough to provide full surface reaction. Therefore the growth rate increases or decrease in comparison to the layer by layer process. On the other side of the window, the temperature can

cause decomposition of the precursor which increases the growth rate as the mechanism becomes similar to a CVD or desorption of the precursor leads to loss of species and decreases the growth rate. In our PE-ALD system we could show that the growth rate is quite constant over a wide range of temperature (figure 4.4), but below 450°C the thickness uniformity increases drastically which let assume that the deposition is not layer by layer controlled. Therefore we generally use a deposition temperature of 500°C. In case of sapphire substrate, which shows a very low thermal conductivity, we expected a reduction of the growth rate. However measurements on ellipsometer did not show a noticeable difference.

The deposition cycle for aluminum oxide deposition by PE-ALD is shown in figure 4.3. First TMA is used to adsorb on the surface in a single layer within 200 ms. After a 2 s Ar purge, removing any non absorbed molecules from the chamber ambient, the aluminum atoms are oxidized in a 20s oxygen plasma, followed by another 2 s purge with Ar gas.

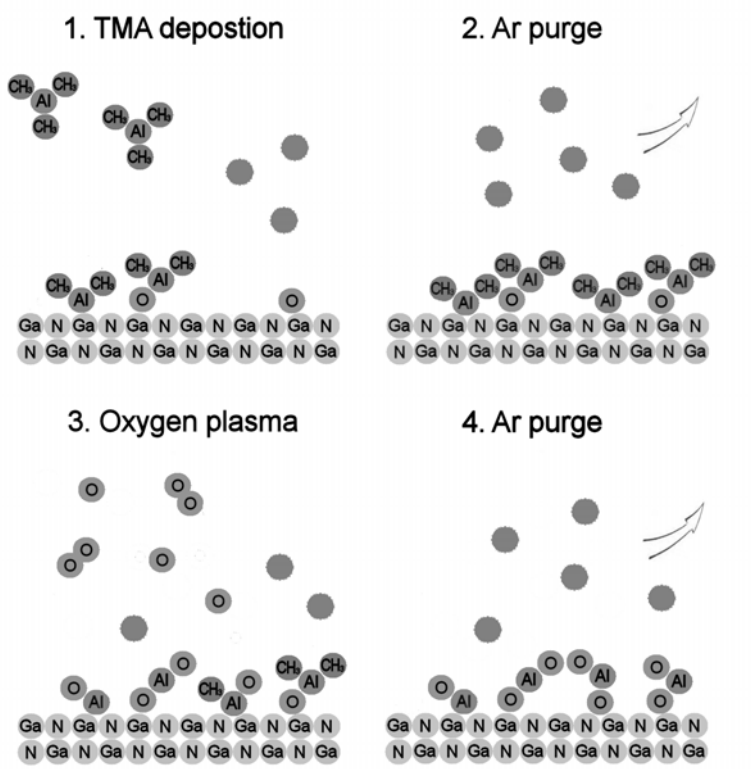

Figure 4.3: Schematic view of the chemical reaction in the four cycle atomic layer deposition process for aluminum oxide

The sequence and the timing show that ALD is a very well controlled process but the deposition rate is extremely low. A measured deposition rate of 0.8Å/cycle refers to 1.9Å/min or ~120 Å/hour, which points out the disadvantages of an ALD system.

Aluminum oxide has to withstand the thermal budget of subsequent process steps. It is known that around 850°C the amorphous film becomes polycrystalline. Even though the dielectric constant of crystalline films is higher at around 12 (compared to 8 for amorphous films), the leakage current increases by a few order of magnitude, which makes the dielectric useless for thin film applications. For thick films of a few tens of nm the leakage current was reported not to increase after high temperature thermal treatment [64]. Jakschik et al. investigated the crystallization behavior of thin films and found that films with thicknesses of 3.5 nm are stable until 1000°C while films of 8 nm change to polycrystalline phase below 850°C [65]. This was contributed to the fact that long range order can easier occur in thick films. Additional time dependence of the annealing cycles was observed showing less significance compared to the temperature.

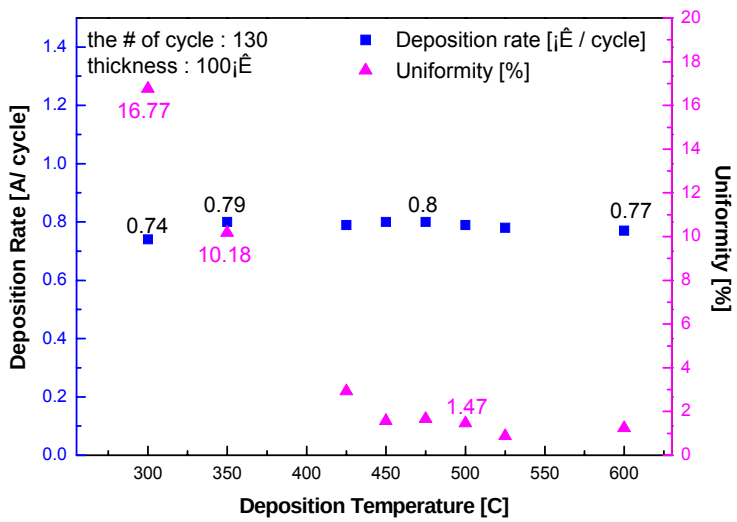

Figure 4.4: Deposition rate and uniformity of the ALD in dependence of the deposition temperature.

Tests on aluminum oxide films from our ALD system with thicknesses of 10 nm and 280 nm showed similar behavior at even lower temperature. From XRD measurements of the thicker sample, shown in figure 4.5, we could find a small peak, indicating long range order of polycrystalline, already after 60s annealing in oxygen at 700°C. This peak becomes clearer at higher temperatures at 800°C and 900°C.

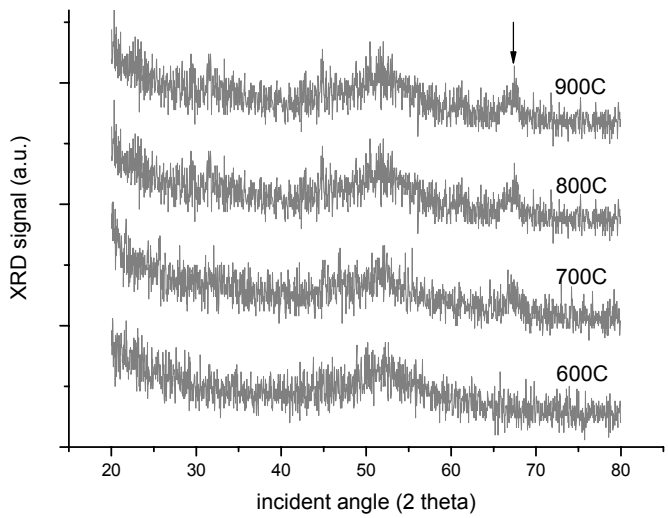

Figure 4.5: XRD results of 28 nm aluminum oxide films after annealing in oxygen for 60s at several temperatures

The samples were patterned with Gate electrodes and the leakage current of the dielectric films was measured, as shown in figure 4.6. The leakage current could be improved by more than two orders for annealing at 600°C for the 28 nm film but increased after the phase changed. Similar behavior was observed for the leakage of the 10 nm thin film, which decreased more than two orders in magnitude until 800°C and then increased. The decreases mainly accounts to the decrease of oxide charges (mainly fixed charges) as presented in chapter 5.2.3. Since we where not able to get accurate XRD results for the thin aluminum oxide film due to the limited power of our XRD signal, we assumed that 800°C is the maximum temperature for 10 nm amorphous aluminum oxide, which also matches with the data from other reports [65].

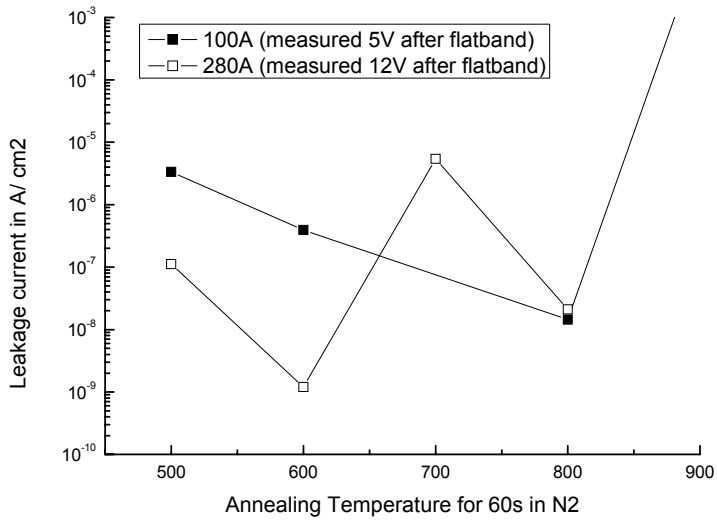

Figure 4.6: Leakage current measured for 10 nm and 28 nm aluminum oxide films. The measured current values were taken from the same potential difference starting from the flatband voltage in order to neglect differences in the interface.

4.2. Device Processing

All devices were fabricated in the clean room facilities of Kyungpook National University, starting from the growth to the final device fabrication. In order to achieve the device patterns, standard optical light lithography was used with commercially fabricated masks. The MIS capacitor required only one very simple mask, while the Hall patterns and the transistors made it necessary to draw and fabricate a new design. The following sub chapters will discuss the layout and process flow of the devices.

4.2.1. MIS Capacitor

Several MIS capacitors were fabricated in this work using several different substrates and dielectrics. The here presented device is therefore an optimized structure which was mostly used including some variations for different insulting materials, according to the previous chapter.
The process flow, shown in figure 4.7, started with a two step surface cleaning of the GaN

samples, which were taken directly from the MOCVD growth and cut into pieces. In the first step the samples were put into H_2SO_4:H_2O_2 (3:1) for 10 min, rinsed and dried by N_2 gas. After that, the native surface oxide was removed by HCl:H_2O (1:2) for 3 min. Directly after surface cleaning the samples were placed in the PECVD or ALD for dielectric deposition. Those process steps were already discussed in chapter 4.1. Annealing of the dielectric film was done in a rapid thermal annealing process (RTA/ RTP) for Al_2O_3, since the maximum thermal budget for amorphous film is comparable low. Silicon oxide can sustain much higher temperatures and was annealed for 30 min in a furnace up to 1000ºC. In order to minimize the interface charges, the first three steps were done directly after each other. The final step before measurement was the metal deposition for the Gate and ground pad areas. Using the mask, which is schematically shown in figures 4.8, a positive photo resist pattern was obtained by standard optical lithography. The resist had a thickness of around 1.5 µm after spinning at a maximum speed of 3500 rpm and was pre-baked at 90ºC for 80s. After light exposure with the mask under contact for 30 s at 4 mW the resist was developed for 20s in AC 300 developer. Even though a positive lithography process was used the lift-off process was successful for large patterns. The samples were then placed into an electron beam evaporator for nickel and gold deposition. During the whole cycle the chamber vacuum was hold below 10^{-6} torr. The metal layer thickness was 400Å for nickel and 500Å for gold. As nickel was directly deposited on the dielectric, it caused the effective workfunction for the MIS capacitor, while the gold layer was used for a good surface conductivity and prevention of surface oxide.

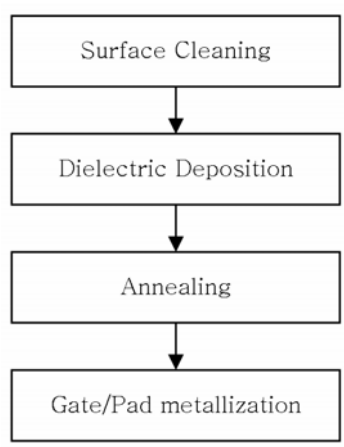

Figure 4.7: Schematic process flow for MIS capacitors

A schematic cross section through the device structure is shown in figure 4.8. It can be noticed

that no ohmic contact was used for the second terminal, opposing to the Gate contact. This method, so called virtual ground contact, can be used under the condition, that the pad contact area is much larger than the actual size of the measured capacitance. In this case the series capacitance from the pad can be neglected during measurement and only the small capacitor defined by the Gate area remains. This method is not only a great advantage in fabrication, since no second metallization step is needed, but also guarantees that no parasitic capacitances of ohmic contacts are included. As can bee seen in figure 4.8, the pad area is extremely large and covers the whole sample except other capacitors and the isolation area. If ohmic contacts would be used as pad, the area is usually smaller, since the contact is not required to be much larger. This works well on n-type GaN where ohmic contacts around 10^{-6} Ωcm^2 can be achieved. But on p-type GaN ohmic contacts are more difficult, resulting into higher resistance and often not perfectly rectified contacts. In this case the ohmic contact can be modeled as a small capacitance with a parallel ohmic resistance. This parasitic capacitance can be shown by capacitive measurement or from a non-linearity in the IV-graph. In either way, it can be recognized that the measured Gate capacitance changes its shape and therefore leads to an additional stretch-out of the graph, which is certainly not acceptable. Therefore the virtual ground contact was used instead. However, also this technique has limits due to the series resistance. These problems are further discussed in the general part of the capacitive measurements.

In comparison to upon described method, designs with ohmic contacts were tested. As mentioned, the ohmic contact on n-type GaN is easier to achieve than on p-type. In general we used a Ta/Ti/Al contact with annealing at 750ºC [86]. It was observed that this contact stack reduces the nitrogen in the surface region during annealing, which leads to nitrogen vacancies and further n-type doping. Therefore the conduction band piles up sufficiently for a perfect rectifying contact. Several stack variations were tested resulting all in perfect linear ohmic contacts from 10^{-6} to 10^{-5} Ωcm^2. On p-type GaN a combination of nickel and gold with very thin thicknesses of less than 100Å was used. Ho et al. explained that the Ni layer changes to NiO during thermal treatment in oxygen for several minutes at temperatures around 500ºC [87]. This thin oxide layer defines a tunneling barrier for holes to the gold metal and leads to rectifying contacts. We could achieve optimum results of high 10^{-5} Ωcm^2 after surface cleaning with HCL:H_2O (1:1) for 60 s but as mentioned above a very small non-linearity was always observed in the IV characteristic. After comparing several p-ohmic results of different doped GaN layers, I concluded, that this might be due to a high density of surface states, which pins the Fermi level a certain energy level and hinder the surface from piling up for rectification.

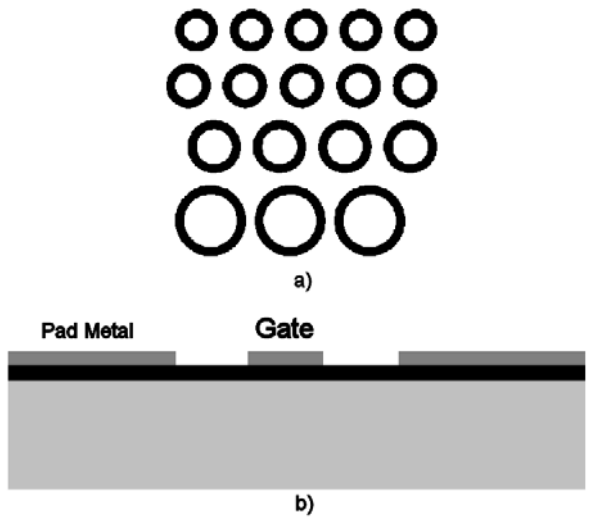

Figure 4.8: Mask used for the fabrication of MIS capacitors (a). The bottom figure (b) shows a schematic view of the cross section of the capacitors with the dielectric (black) on the GaN substrate and the single metal layer on the top for both electrodes.

After fabrication the IV characteristic was measured by HP4156 in order to determine the leakage behavior. Too high leakage values made further analysis impossible since the parallel resistance does not allow an accurate capacitance measurement. Frequency measurement was done by an HP4284 LCR meter for measurements from 200 Hz to 1MHz and a 1 MHz CV meter (HP4084). Even though both devices are able to measure up to 1 MHz the higher frequency results of the LCR meter differed slightly for samples with higher ohmic resistivity due to an higher internal resistance and additional influences of the external wiring of the measurement device, which could not be removed by calibration. Prior to the measurement, the devices were calibrated over all frequencies by shorten and open measurement after connecting the samples to the probe station. Shorten measurement was done by the gold layer of the samples, while for the open measurement both probes where lifted up from the sample surface. The AC measurement amplitude of 30 mV was usually used in order to reduce noise in the resulted graph. Optional 10 mV amplitude often shows a rough graph shape. Most non-time-critical measurements were done with the lowest possible integration time of the measurement device. This was reduced to a few 100 ms in case of the backwards measured capacitance graph, in order to allow the assumption that no electrons from the interface are captured (or emitted) during measurement (at least not in

the inner bandgap).

4.2.2. Gated Hall Pattern

Gated Hall patterns were fabricated to measure the field effective mobility of the carriers below the oxide. This is important since the mobility is of enormous interest in comparison to high mobility electron transistors. Two different type of process flows were used in order to measure the n-type and p-type electron mobility. The hole mobility is much lower in GaN and therefore device based on holes are almost not of any interest. For n-type GaN a simple hole pattern with a large Gate electrode upon the center is sufficient if the bulk carriers can be neglected over the channel carriers. However, in p-type GaN inversion electrons must be created, which requires a bipolar structure. Most reports use silicon implantation into Mg doped GaN for highly n-type doped regions [88-91]. One part of this work was also related to silicon implantation into GaN, but the results are not ready to be included into this work. In substitution I used a Schottky contact on p-type GaN by aluminum, which has almost no barrier to the conduction band and therefore allows electrons to be injected [83].

For both substrate types, the processes started with a MESA etch for isolation which restricts the electrons to the Hall area. Prior to the transformer coupled plasma reactive ion etch (TCP-RIE) a positive lithography step was performed similar to the one described for the MIS structure with the mask shown in figure 4.10. The TCP-RIE etch was done by BCl_3 and Cl_2 gases at a pressure of 10 mtorr, 300 W AC power and 40 W DC power. The resulting etch rate was 200 nm/min. In order to get a good isolation for p-type GaN on the described UGaN buffer structure a minimum etching time of 5 min was required. In case of n-type GaN this was increased until the lower end of the buffer. Since such deep etch processes also require a thick photo resist for masking, an 8 µm thick resist was prepared. After etching the sample were cleaned in acetone and H_2SO_4:H_2O_2, separately, followed by the same procedure as used in the MIS structure. The whole dielectric deposition was performed exactly same as before, in order to be able to compare the results of the interfaces with the mobility measurement. After thermal treatment the samples were patterned with ohmic patterns according to figure 4.10. Prior to metal deposition a short TCP-RIE etch was performed to remove the dielectric at the contact areas. For n-type samples this etch could also be done by wet etch with hydrofluoric acid (HF). However, for p-type samples which require a sharp etch edge at the ohmic pattern for the overlapping Gate, wet etch is not sufficient. The previous described ohmic contact was deposited by electron beam evaporation

and annealed in an RTP cycle for 60 s at 750ºC. The ohmic contact was extracted by linear TLM measurement [92, 93]. For the p-type Schottky Hall pattern the pad to Gate isolation required a second dielectric deposition, which was done by silicon oxide from PECVD, since other deposition techniques would require higher temperatures than being acceptable for the metal layer. This second oxide layer has neglectable influence on the dielectric interface. The final Gate metallization was deposited according to the MIS metal layer. An additional step is required for the p-type samples since the ohmic pad contacts are covered with the second dielectric layer. Therefore a simple mask step and wet etch of the oxide removed the dielectric on the pads.

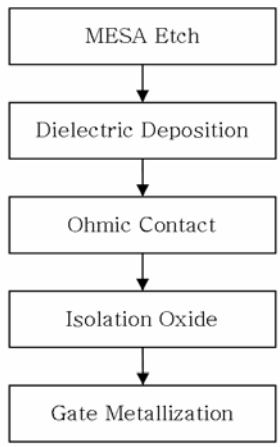

Figure 4.9: Schematic process flow of the Hall pattern

The device dimensions were 100 x 100 μm^2 for the inner Hall region and about 150 x 150 μm^2 for the pads, which was necessary for contacting by the bonding machine. One important factor in the device structure is that the Gate needs to be sufficient isolated from the pads and the channel. Otherwise the Hall measurement shows current through the Gate metallization which is parallel to the GaN area. Therefore the overlapping area in p-type samples and the total area of the Gate metallization has to be small enough that the total leakage current through this area is neglectable in comparison to the horizontal current flow due to the Hall measurement.

After fabricating the samples in the clean room, IV measurement using HP4156 was done to select a device for wire bonding to a printed circuit board (PCB). This sample was then mounted in a HL55WIN Hall measurement. The standard configuration in our laboratory has only a 4-point Hall measurement which required a separate Gate voltage control. Therefore a wire was fixed to the bonding pad of the Gate and connected to an external voltage source. The ground

connection was returned to the ground contact of the Hall measurement device. The Hall measurement supplies symmetrically a maximum amplitude of 20 mV. Therefore, Gate voltages of more than a few Volts can be considered as independent of the pad potentials.

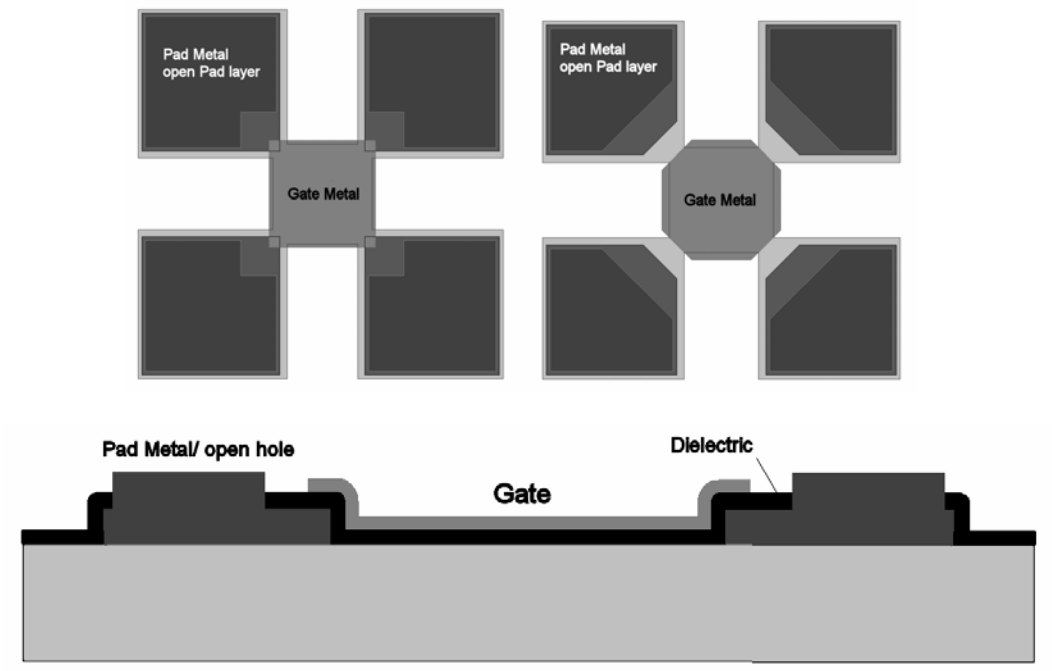

Figure 4.10: Schematic Mask design for the Gated Schottky Hall pattern (top right) and the Gated Hall pattern (top left). The bottom figure shows the cross section of the Gated Schottky Hall pattern with overlapping pad and Gate metallization. The normal Gated Hall pattern is same except no overlap is necessary.

The measurement circuit shown in figure 4.11 includes the samples bonded on a PCB mounted in the Hall system. The fifth connection to the Gate is connected by wire to the external power supply using a 100 kOhm resistance in series and a voltage meter for the adjusting the bias value directly on the sample. The resistance is used to protect the Hall system from the external source in case of a dielectric breakdown. The biased voltage ranged up to 10 V which can cause damage on the internal circuit of the Hall measurement. However the bias voltage was almost not affected by the bias source resistance under normal device operation, since the Gate resistance of the dielectric had several Mega-Ohms.

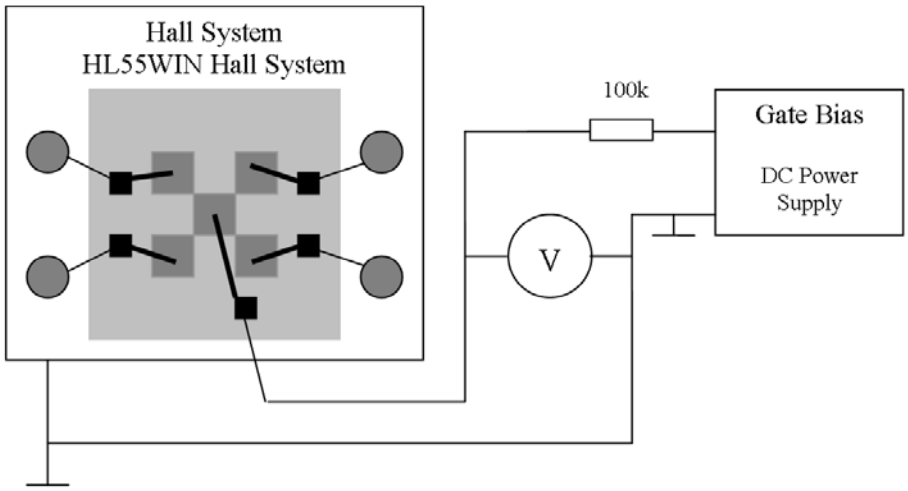

Figure 4.11: Measurement circuit for Gated Hall measurement. The sample was bonded and connected to the Hall system, with external Gate bias control.

4.2.3. Schottky Barrier Transistor

The Schottky Hall pattern and the Schottky transistor used the same idea of Source and Drain contact. By comparing figure 4.10 with figure 4.12 it can be seen that the layer order is same and only the dimensions differ. Therefore the Hall pattern and Schottky transistor could be done in the same fabrication on one sample. However in case of Schottky transistor device isolation could also be performed by Ar implantation, which was tested to have an effective isolation depth of more than 200 nm at 140 keV. Full layer isolation is not required, since the device is a 3-terminal device and the current is restricted to the ohmic current flow from Source to Drain. A major concern in this the device is the narrow gap between the ohmic contact for Source and Drain. Even though the patterns are defined exactly by optical lithograph, they diffuse during the post annealing process for the ohmic contact in n-type devices. Especially aluminum with a lower melting point than the annealing temperature prefers to widen the patterns, leading to non-exact edges. In order to prevent this, a second Ta layer with a thickness of 200Å was inserted after the aluminum layer. The device channel length varied from 3 to 30 μm.

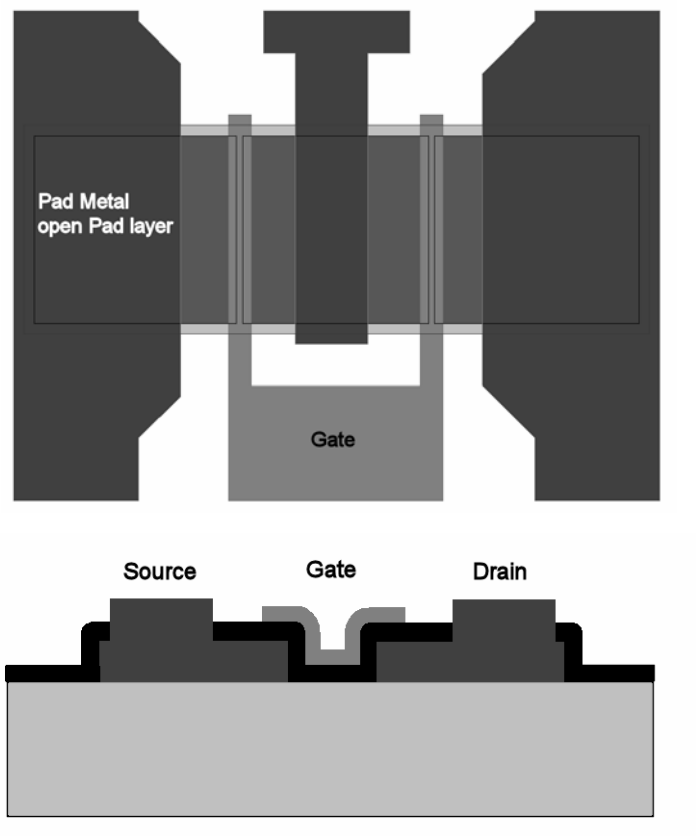

Figure 4.12: Mask design (top) and cross section (bottom) of the Schottky Transistor.

The devices were drawn for dual finger shape which is normally used for RF measurement. However this was not performed on this structure since the performance would not be interesting according to the large Gate capacitance. More interesting was the IV characteristic which was again measured by HP4156 for the Drain current in dependence of the Gate and the Drain voltage.

5. Experimental Results

In this final part of my work, the key measurement results from this topic related research are shown. Since most of the time I spend answering the question, how the capacitive measurement can be done accurately for different type of MIS structures, a large part of this chapter is contributed to those results for silicon nitride, silicon oxide and aluminum oxide. Before, a general summary on the characteristic of CV graphs for MIS structures based on GaN is given. The last two subchapters discuss the Hall and transistor results related to the mobility characterization.

5.1. Characteristic of CV measurement

The basic model of a MIS structure was discussed in chapter 3.1.2 at the conduction method, including the oxide capacitor, the depletion and interface related capacitor and resistance. Further more, the last chapter introduced the virtual ground contact, which was used without any exception throughout this work. This capacitive contact leads to an additional series capacitor, equal to a larger size mirrored Gate capacitor. These two capacitors are connected by the bulk material which includes a series resistance according to the radial shape of the test patterns (figure 4.8). In my previous description, the size of the series resistance, even though unequal from zero, does not influence the capacitive result. Hence it can be extracted by presented method. Also it was assumed, that the pad capacitor for the ground contact is sufficiently larger, that it can be neglected in the result. Further it was mentioned, that the resistivity of GaN bulk material is very low, since the mobility for p-type GaN is below 20 cm^2/Vs and n-type GaN without doping has a usual carrier concentration around 10^{16} cm^{-3}. Further, capacitors were often fabricated on sample from the outer part of the wafer, which shows sometimes lower mobility and few carriers. Hence, the series resistance is often very large, which leads to several effects in the measurement. The following part will describe each of them separately.

First of all, I would like to discuss figure 5.1, where several different measurement

configurations are shown. The configurations are schematically shown in figure 5.2. The first graph is the common ground configuration which shows the expected, ideal CV graph shape of a p-type GaN sample, measured between a small Gate capacitor and a large common ground area with neglectable bulk resistance. If the ground area is reduced as shown in the middle configuration, it appears as a capacitors of same size with a mirrored CV characteristic. It can be seen from the first graph that the flatband voltage is around zero Volts. Therefore the resulting graph is equal to the series capacitor of two original capacitors mirrored at zero Gate voltage. It clearly points out that if the area of the ground contact is too small a reasonable result is not possible and can not be extracted. However if the next configuration is considered, where the ground contact has the same size but further away from the actual Gate capacitor (figure 5.2, bottom), it can be noticed that the measured capacitor shape is similar to the first one but reduced in size. This reduction is not due the second capacitor, rather than due to the additional series resistance. The ground capacitor is still noticeable at the deep accumulation part of the CV graph. However over a wide range the shape is not deformed.

Even though this measurement is just a demonstration, where the values of the capacitor and the resistance were changed geometrically, it clearly shows the dependencies of the results.

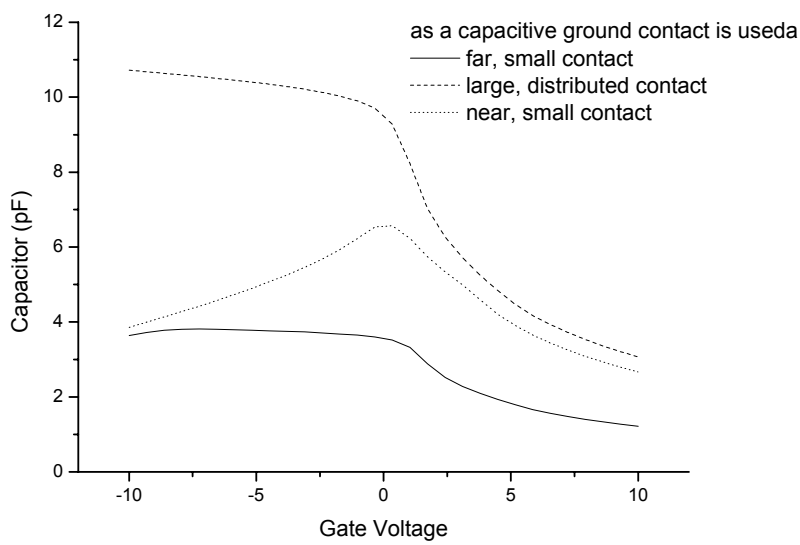

Figure 5.1: Measurement of the same capacitor with different common ground contact configurations according to figure 5.2

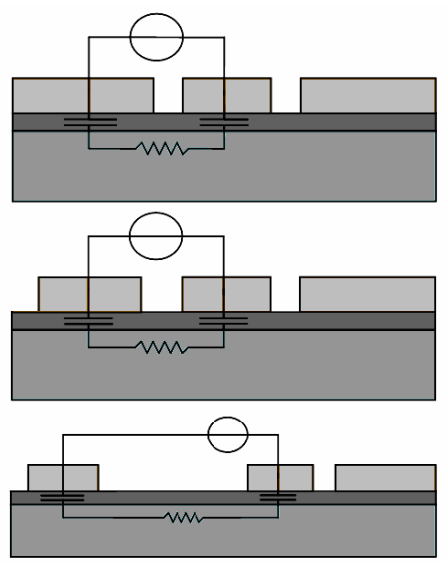

Figure 5.2: Schematic cross-section for standard common ground contact (upper), reduced size common ground contact (middle) and far reduce size contact (lower).

It was noticed that the graph depends on the series resistance and the ground capacitor size. This might seem that the size of the virtual ground contact is a design issue and can be solved by using a larger area. However, this was never the case in my design, where the surrounding area has been almost the whole sample except some small capacitor shapes. Even though, a second parasitic capacitor was noticed for some measurements. This resulted from the fact, that the capacitor size depends not only on the vertical structure, but also on the lateral one, which is accompanied by the series bulk resistance. Simply, it can be said, that capacitive components far away from the Gate capacitance do not play a role and can be neglected. If this non-active area is getting larger, the actual effective ground capacitor size reduces and therefore can not be neglected in the model. More physically, this can be compared to the transfer length model shown in figures 5.3. Along the capacitive interface the radial resistance of the bulk can be written as

$$dR = \rho_{\square} \frac{dr}{2\pi r} \tag{5.1}$$

and the corresponding capacitor

$$dC = \frac{\varepsilon}{t} 2\pi r \cdot dr\,, \tag{5.2}$$

where $\rho_{\square}$ is the sheet resistance of the bulk, ε the dielectric constant of the insulating material, t

the thickness of the insulator and r the radial coordinate. In accordance, the potential drop a long the radial axis can be expressed by the infinitesimal radial resistance and the current, which vanishes by charge exchange with the infinitesimal capacitor as

$$\begin{aligned} dU(r,t) &= dR \cdot I(r,t) \\ dI(r,t) &= dC \cdot \frac{\partial U(r,t)}{\partial t} \end{aligned} \cdot \tag{5.3}$$

This set of equation is sufficient to solve the potential term for U(r,t) and the current term I(r,t). I then insert equation 5.1 and 5.2 into 5.3. and get

$$\begin{aligned} \frac{\partial U(r,t)}{\partial r} &= \frac{dR}{dr} \cdot I(r,t) = \frac{\rho_{\square}}{2\pi r} I(r,t) \\ \frac{\partial I(r,t)}{\partial r} &= \frac{dC}{dr} \cdot \frac{\partial U(r,t)}{\partial t} = \frac{\varepsilon}{t} 2\pi r \frac{\partial U(r,t)}{\partial t} \end{aligned} . \tag{5.4}$$

In order to combine the two equations, the first one can be differentiated with respect to the radial coordinate

$$\frac{\partial^2 U(r,t)}{\partial r^2} = \frac{\rho_{\square}}{2\pi r} \frac{\partial I(r,t)}{\partial r} \tag{5.5}$$

which allows to remove the differential term of the current.

$$\frac{\partial^2 U(r,t)}{\partial r^2} = \frac{\rho_{\square} \cdot \varepsilon}{t} \frac{\partial U(r,t)}{\partial t} \tag{5.6}$$

This is the final equation, which needs to be solved for the potential term. It is quite obvious that the time and the radial coordinate can be separated. Furthermore, the main interest lies on the radial extension. Therefore I use equation 5.7 as a solution term, where $U_0(t)$ involves the time-dependent amplitude.

$$U(r,t) = U_0(t) \cdot e^{-\frac{r}{\lambda}} \tag{5.7}$$

Using the solution term 5.7, equation 5.6 results into

$$U_0(t) \frac{1}{\lambda^2} = \frac{\rho_{\square} \cdot \varepsilon}{t} \frac{\partial U_0(t)}{\partial t}, \tag{5.8}$$

where $U_0(t)$ could not be removed due to the derivation term. In accordance to my measurement, only sinusoidal signals were used, which allows to express the absolute length of the complex potential vector as

$$\left| \frac{\partial U_0(t)}{\partial t} \right| = \omega \cdot \left| U_0(t) \right|, \tag{5.9}$$

where ω is the radial frequency of the current and voltage signal.

Inserting equation 5.9 into 5.8 gives the radial result for equation 5.7 where

$$\lambda = \sqrt{\frac{t}{\rho_{\square} \cdot \varepsilon \cdot \omega}} = \sqrt{\frac{1}{\rho_{\square} \cdot \omega \cdot C_{ox}}} \tag{5.10}$$

is the effective radial extension of the capacitor for sinusoidal signals. The result is schematically inserted in the lower figure of 5.3. It can be seen that the length λ decreases with increasing bulk resistance, as noted before, and with increasing frequency. Second one results from the increasing current through a capacitor at high frequencies.

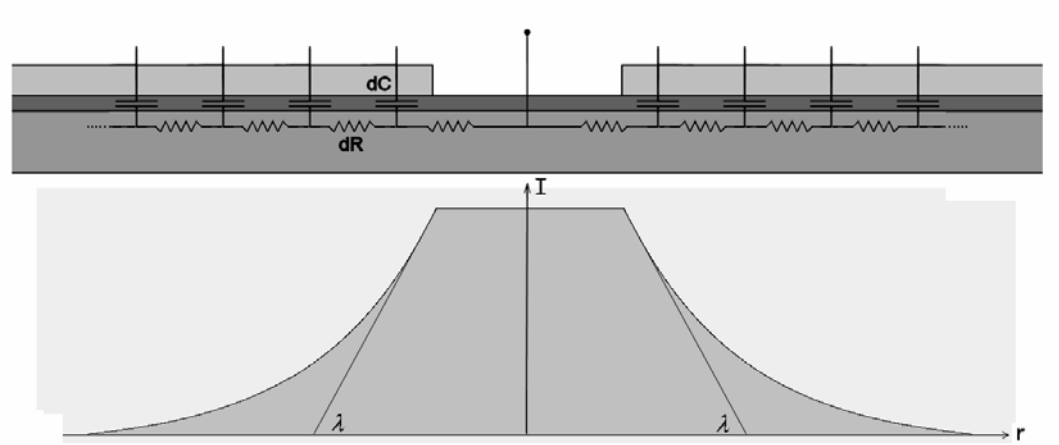

Figure 5.3: Schematic description of the current distribution in radial direction in an infinite structure under consideration of the series resistance and the MIS capacitor

In order to verify this theory, I would like to use an example for a typical MIS structure. Assuming an oxide capacitor of 10^{-7} F/cm^2 and a substrate with 50 kOhm/square sheet resistivity (typical value of a p-type GaN substrate) which is measured at a frequency of 1 MHz, the resulting critical length would be 56.4 μm. Therefore the effective size of the measured capacitor and the ground contact must be smaller this length.

Further, I would like to describe the total virtual ground capacitor in dependence of λ and r_0, which is the inner radius of the circular virtual ground contact. Using equation 5.2 of the effective capacitance area from r_0 to $r_0 + \lambda$ gives

$$C_{Ground} = \int_{C(r_0)}^{C(r_0+\lambda)} dC = \frac{\varepsilon\pi}{t}\left[\lambda^2 + 2r_0\lambda\right] \tag{5.11}$$

In comparison the Gate capacitor is simple expressed as

$$C_{Gate} = \int_{C(0)}^{C(R_0)} dC = \frac{\varepsilon\pi}{t} R_0^2 \ , \tag{5.12}$$

where R_0 is the maximum radius of the circular Gate area. One method which increases the effective area of the ground contact relatively is using smaller Gate capacitors and the same spacing between the Gate capacitor and the surrounding pad metallization (can be expressed as r_0-R_0). If d is the constant spacing between the two metallization, it can be seen that the inner area decreases quadratic wile the outer area does only linear and shows an additional constant term, which improves the ratio for smaller values of R_0.

$$R_0^2 << \lambda^2 + 2r_0\lambda = \lambda^2 + 2(R_0 + d)\lambda \tag{5.13}$$

Therefore the relation between the capacitive areas improves and the measurement result shows less parasitic influence.

Another characteristic of the CV graph is observed in the accumulation region. Similar to silicon MOS structures using poly-silicon as ohmic Gate layer, the capacitor increases with deeper accumulation potential. In silicon this is due to the fact, that the high doped poly silicon can be depleted partially and this slight change in depletion varies the total depletion thickness. However the metal Gate layer does not show a depletion and the effect is therefore noted to the decreasing series resistance of the capacitor in accumulation. The resistive part between the capacitors does not change, but the bulk area below the Gate is accumulated with carriers and therefore its conductivity increase. Hence the capacitor is slightly increased and inner radial capacitive components contribute more to the total capacitor value. This can be easily understood by considering figures 5.1, for the first and last configuration. There only the series resistance is effectively different, changing the absolute value of the capacitor. Another more drastic example for a low resistive n-type sample is shown in figure 5.4. Those two capacitors where measured on the same sample, using a large (D = 300 µm) and a small pattern (D = 140 µm). While the small one is constant in accumulation the large one increases drastically at the same surface potential. This shows how large the influence of the effective area of the Gate capacitor and the ground contact capacitor is. Therefore it is important, to decrease the capacitive area and further

compare the results for different capacitor sizes, in order to find the critical length for a substrate. In case of the numerical example from before, a capacitor with a diameter of 300 µm and a critical length of 50 µm measures only ~55% of its actual value. However if the sheet resistance increases, due to accumulation carriers at the surface, the capacitor might be able increase further. Since this effect appears clearly after depletion, it must be neglected in accumulation from the actual measurement. An example of such a case is shown in figure 5.14. For this capacitor it was not possible to measure an appropriate pattern without disturbance. Nevertheless, the depletion region, which is of main interest for the flatband extraction is not affected by this effect.

However this whole analysis shows that the CV measurement includes lateral components if a back contact is not possible, as in silicon. These lateral components must be carefully included; otherwise the result must be doubted. If high-resistive undoped GaN is characterized by high frequencies, the critical length reaches a micrometer or less. For this case a characterization is in praxis not possible by a lateral configuration. In order to improve such a measurement, additional geometrical confinement can be integrated in the device to channel the current. However the large serial resistant must be taken into account.

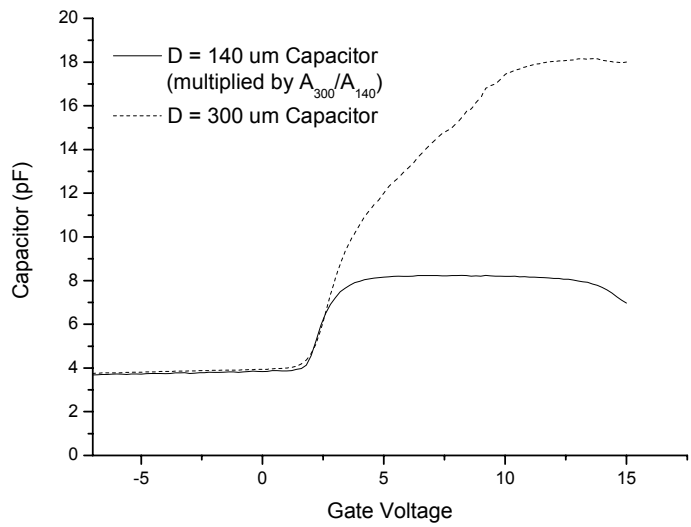

Figure 5.4: Comparison between the same capacitor measured at large and small capacitor pattern. The value of the small pattern is multiplied by the aerial ratio between the two capacitors for normalization.

Another effect, that I want to discuss in general, is the frequency dispersion in p-type GaN

substrates. While it is known from silicon that for frequencies above 1 MHz the ohmic resistance increases, p-type GaN shows this effect already for a few kHz. A good example is shown in figure 5.17 with comparison to figure 5.12. Over a large range of frequencies the n-type capacitance does not change significantly, but the p-type capacitance decreases for increasing frequency and almost disappears for measurement at 1 MHz. I observed that for frequencies below 1 kHz the capacitor reaches the expected value and almost no dispersion occurs. In comparison to above shown examples, it shows that the bulk resistance increases with the frequency which I believe is contributed to carriers trapped in bulk traps, caused by the large magnesium incorporation. With higher frequencies, the trapped hole carrier can not response to the AC signal and do not contribute to the current flow, which increases the resistivity. In order to get the exact CV shape, low frequency measurement is therefore required. However, accepting the decreased capacitive values for the measurement result, allows it to use also higher frequencies, which is basically done in all the reports [54, 55] that were published until today.

5.2. Dielectric Characterizations

The following subchapters discuss quantitatively the interfaces of silicon nitride, silicon oxide and aluminum oxide under different annealing conditions. Further different types of substrates were used, resulting in very different characteristic. The first substrate was characterized to have a low unintentional doping density in the low 10^{16} cm^{-3} characterized by Hall measurement and showed therefore a good quality of GaN films. However those results could not be further produced by our MOCVD systems, which resulted into slightly higher doping densities, probably due to increasing crystal defects or impurities. This second substrate showed a comparable worse interface characteristic for n-type and p-type GaN films.

The used design, described in chapter 4.2.1, has a nickel layer as Gate electrode, which defines the metal workfunction for the flatband voltage. The workfunction of nickel was taken to be 5.15 eV, which is a common value resulting from photo-electric measurements. Using equation 2.14, the ideal flatband voltage for n-type GaN was determined to be

$$V_{FB,N/Ni} = \Phi_M - \chi_s - \left[\frac{E_g}{2} - \frac{kT}{q}\ln\frac{N}{n_i}\right] = 0.95V\,, \qquad (5.14)$$

where χ_s is the electron affinity of GaN, Eg is the band gap energy. The other parameters were

already described earlier. N was measured from above mentioned Hall measurements and confirmed by the depletion capacitance shown in figures 5.5. The slight curvature in the graph occurred from the fact that this graph was measured without UV light, resulting into a deep depletion graph including charged interface traps. Some of those traps can emit during measurement as described in chapter 3.1.3. However, deeper in the bulk the interface traps do not respond due to the lower surface potential and the slope becomes linear and the extracted doping density similar to the Hall result. The linear results prove further the deep depletion characteristic. If the CV graph after UV illumination is characterized in the same way, it would be linear for a short range, showing the same slope as the deep depletion CV graph without interface states.

Similar calculations where done for p-type GaN substrates showing that the doping density varied from low to high 10^{17} cm^{-3}. Those values where again taken from Hall measurement and confirmed by $1/C^2$ graphs of the depletion region from capacitive measurement. It can be noticed, that no curvature appears in figure 5.5 compared to n-type, which is due to the fact that interface traps charges can not be charged in the dark-measured CV graph of p-type GaN. Equation 5.14 changes according to the Fermi level, which is on the opposite side of the intrinsic energy and the flatband voltage becomes

$$V_{FB,P/Ni} = \Phi_M - \chi_s - \left[\frac{E_g}{2} + \frac{kT}{q}\ln\frac{N}{n_i}\right] = -2.3V\,. \qquad (5.15)$$

The difference between the flatband voltages in equation 5.14 and 5.15 is almost the band gap energy of GaN.

In conclusion, the bulk doping density determined by Hall and confirmed by depletion graph is a rough orientation for the following capacitive measurement. While the wafer characterization was usually done in the center position of the 2-inch wafer, for CV characterization all kind of wafer positions were used. Therefore samples with lower resistivity sometimes appeared for certain experiments.

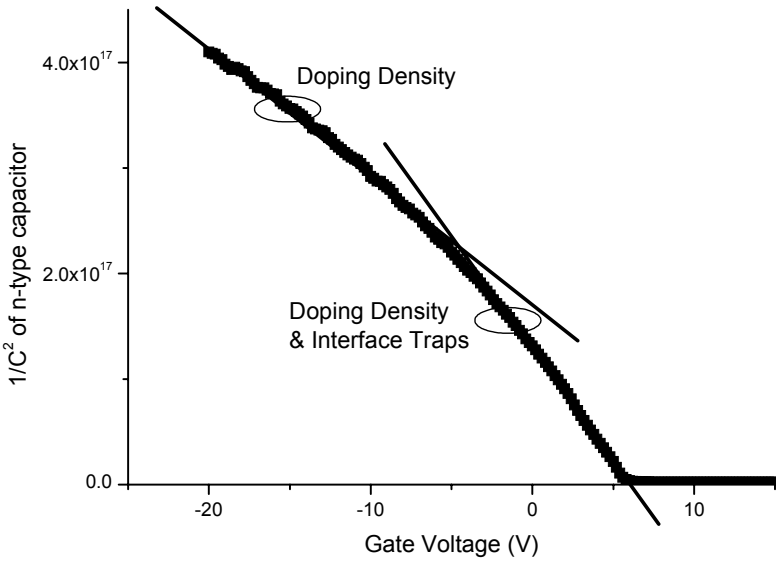

Figure 5.5: $1/C^2$ extraction on deep depletion CV measurement on n-type for SiO_2.

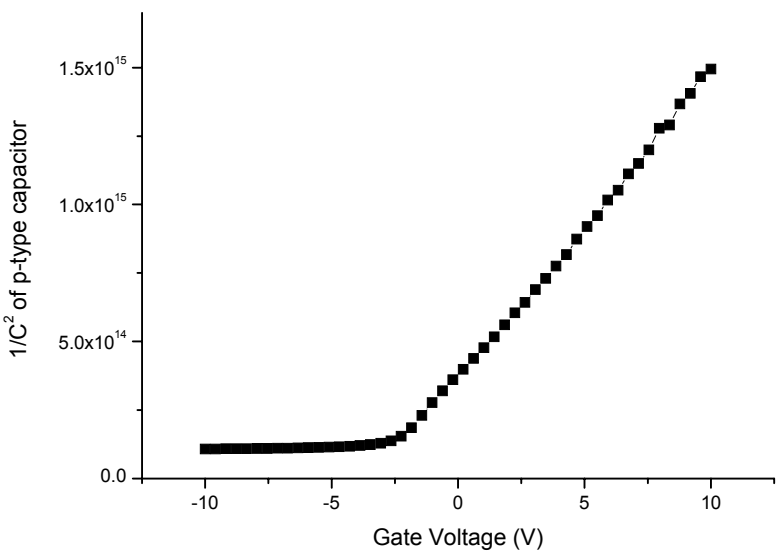

Figure 5.6: $1/C^2$ extraction of deep depletion CV measurement on p-type GaN for SiO_2.

5.2.1. Silicon Nitride (Si_3N_4)

Silicon Nitride was characterized with post deposition annealing at 1000ºC under nitrogen ambient and without annealing. All capacitors showed similar behavior, which includes the highest interface density among the tested dielectrics. This can be also observed from the frequency behavior of the CV graph in figure 5.7, as the flatband voltage drifts backwards for higher frequencies. This unusual behavior is explained by a very high interface density around the band edge (Fermi level). Further, the silicon nitride capacitor shows hysteresis, shown in figure 5.8. As described earlier this is mostly not observed in GaN MIS capacitors and leads to the same conclusion. A rough extraction of the interface state density from figures 5.7 results to 5.8-6.4x10^{13} $cm^{-2}eV^{-1}$ around 3 eV above the valence band. For the calculation I assumed that only states beyond the frequency related trap energy can responds to the measurement. The total oxide charges were determined to be above 1.4x$10^{13}cm^{-2}$. But an accurate value can not be given, since the density is too high at the conduction band edge and those traps can hardly be measured by any technique. The high density around the band edge makes it further difficult to measure the capacitors, since they tend to drift and are extremely sensitive to any external influence as light. In accumulation, the graphs show an increase short after reaching saturation, which is due to leakage current. However this does not affect the actual results from the flatband voltage which depend only on the depletion region.

Representative for many of my results on n-type GaN, the previous graphs show a constant capacitor after depletion instead of deep depletion. Therefore two possibilities can be described. First, in comparison to silicon, this would be contributed to an inversion channel below the nitride layer even though I mentioned earlier that thermal generated carriers do not exist in GaN material. However if this would be the case, also a low-frequency CV graph should be possible at a certain low frequency, where the capacitor increases up to the oxide capacitor. Such a measurement can be done by integrative capacitive measurement for long integration time. However, no difference in the shape was notice using this kind of technique. The second explanation is therefore that this non-deep depletion graph depends on a large interface density lying deep in the half of the lower band gap, which prevents the capacitor from further depletion into the bulk.

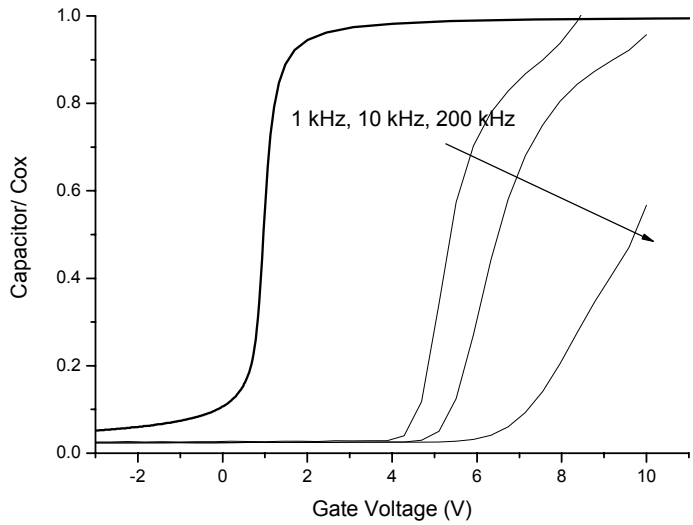

Figure 5.7: CV graph of non-annealed Si_3N_4 showing high flatband voltage dependence on frequency. Ideal graph is shown for comparison. The oxide capacitor of the 24 nm dielectric film was 180 pF.

In comparison, the annealed sample did not show an improvement in terms of the interface density, as can be notice from figure 5.9, showing the CV measurement without UV light into deep depletion. A long stretch-out leads to interface charges around $2x10^{13}$ cm^{-2}, which is similar to previous shown result. It should be noticed that the quantitative voltage shift is not directly related to the charges, since I used different dielectric thicknesses. Further, the graph showed depression of the capacitance value due to higher frequencies (dispersion). Therefore the graph was normalized by its maximum rather than the oxide capacitor (I use the term oxide capacitor as a general term for the insulating capacitor, since it is a very common expression in literature, mainly based on silicon oxide.) The graph shows high deformation in comparison to the ideal graph in shallow depletion, which is again due to a high trap density around the conduction band. However, the depletion behavior of the graph shows deep depletion into the bulk.

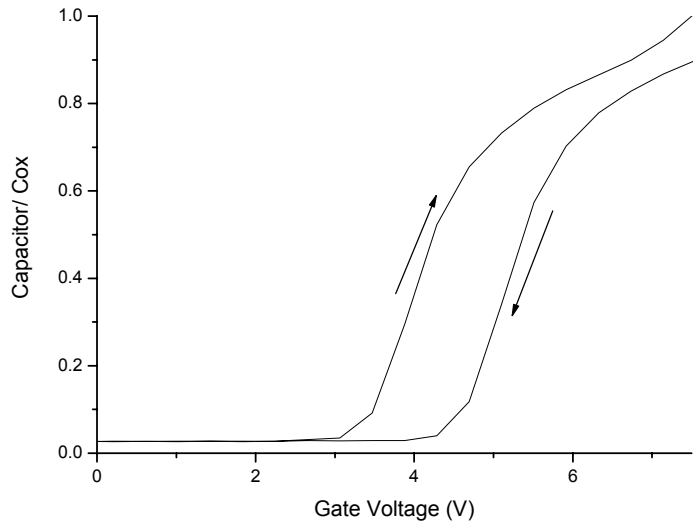

Figure 5.8: Hysteresis effect on Si_3N_4 capacitor measured at 1 kHz and indicating a very high interface density close to the conduction band. The oxide capacitor was 180 pF.

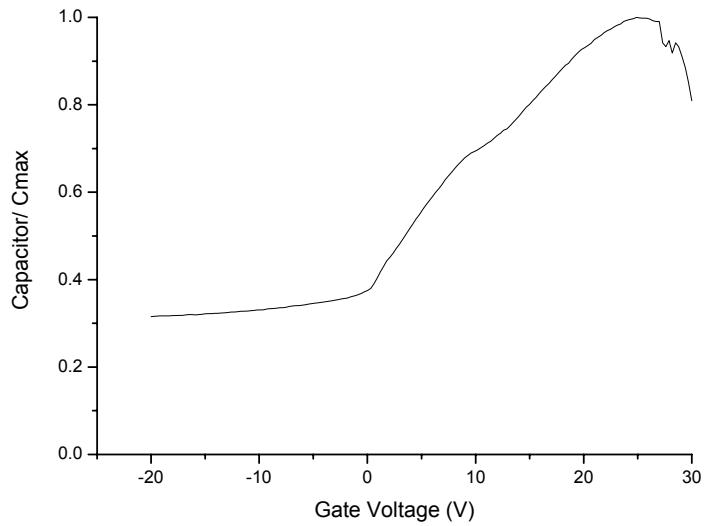

Figure 5.9: CV graph of annealed Si_3N_4 measured at 1 MHz without UV light. The graph shows dispersion and is therefore normalized to its maximum value. (C_{ox} = 61.1 pF/ 72nm Si^3N^4)

In order to derive the fixed charges, samples with and without annealing where measured under UV light. In above considerations I neglected them, since the interface charges dominated the oxide charge. Due to the very high trap density around the band edge, measurement after UV light illumination, as described in 3.1.1, showed similar stretch-out and was therefore not accurate enough. Hence, the result shown in figure 5.10 was measured under UV light illumination during the whole measurement, assuming that the hole generation is higher than the carrier trapping time. Even though this measurement does usually result in a very noisy graph and is often not useful, it showed a good result for the nitride capacitors, due to the high trap density. The calculated fixed charge density for silicon nitride without annealing was $2.2x10^{12}$ cm^{-2} and could be improved to $6.7x10^{11}$ cm^{-2} after annealing at 1000°C.

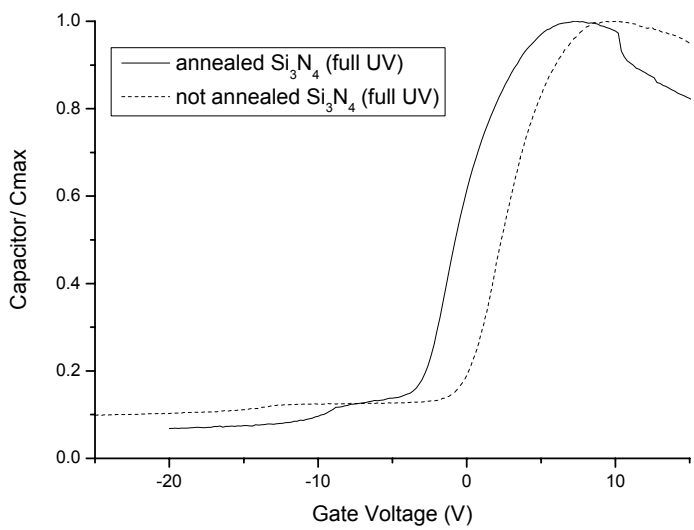

Figure 5.10: Comparison between n-type CV graphs with annealed and non-annealed Si_3N_4 measured during UV illumination. The threshold shift shows a lower fixed charge density for the annealed dielectric. Both oxide capacitors are 61.1 pF.

A final result for silicon nitride compares the annealed and non-annealed result for p-type GaN. The graphs in figures 5.11 are normalized by the maximum values, according the dispersion in p-type samples. As the results are from different substrates, they do not allow a lot of comparison. The non-annealed sample shows a large flatband shift (the graph is shifted by -20V for

comparison) and normal deep depletes without UV light. However, using the substrate with higher crystal defects, no depletion was observed over the whole applied Gate bias range. Only during instantaneous UV illumination the presented depletion result could be measured, showing a similar depletion shape, but less deep and no flatband shift. Later on is probably due to the compensation of fixed charges with interface charges. An accurate quantitative analysis is therefore not possible. Similar to the n-type result inversion was not observed after UV illumination.

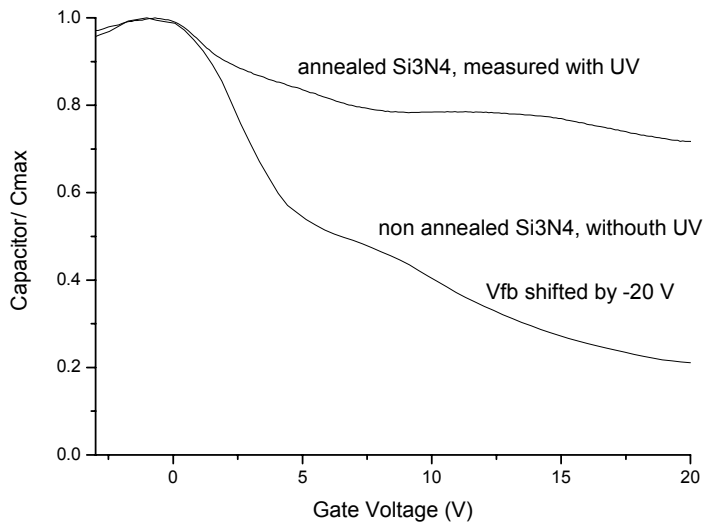

Figure 5.11: Comparison of p-type CV graphs with Si_3N_4. Upper Graph shows annealed sample measured with UV light illumination at 1 MHz (C_{ox}=61.1 pF) while lower graph (shifted by -20V) shows the non-annealed sample measured without light at 1 kHz (180 pF).

5.2.2. Silicon Oxide (SiO_2)

Silicon oxide shows much improved results in comparison to silicon nitride, which can already be seen in figure 5.12, showing the CV graph of an n-type sample measured from 1 kHz to 1 MHz, without noticeable flatband shift. Additionally, no hysteresis was observed for this samples. The measurement included also the conductivity, used for further trap analysis, which will be discussed later.

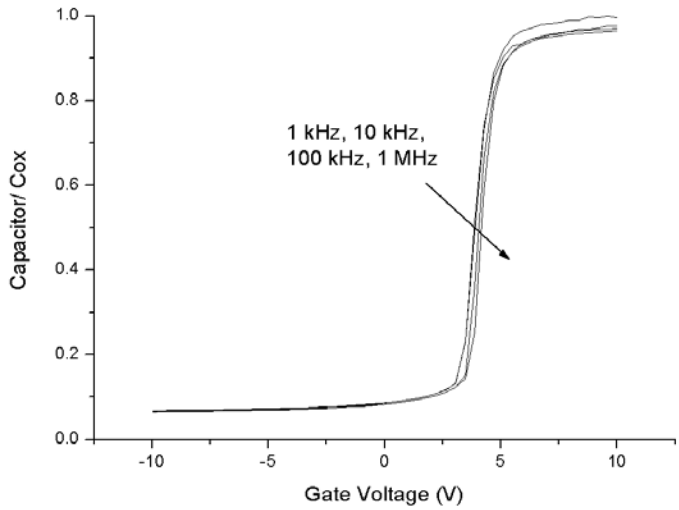

Figure 5.12: CV of 40 nm non-annealed SiO_2 on n-type GaN over frequency. C_{ox} = 70 pF.

While above measurement was done with out light, I compared the UV shift to the dark measurement at 1 MHz and determined a fixed charge density of $3.7x10^{12}$ cm^{-2} and a interface charge density of $6.2x10^{12}$ cm^{-2}. The CV graphs in figure 5.13 measured without light show typical deep depletion characteristic. The increase of the capacitance during UV light illumination is due to the hole generation and let assume inversion carriers in the channel, as usually interpreted [54, 64]. However, it might also be just due to the fact, that the graph is shifted by the difference of the interface charges. The measurement shows very good agreement with the ideal graph.

In figure 5.14 the same measurement was repeated using an annealed sample and the second type of substrate with higher defects. The results for the n-type material did not change significantly and the fixed charges remained around same value, while the interface charges decreased slightly around $5.3x10^{12}$ cm^{-2}. The measurement shows some series resistance effect as described previously. Therefore I normalized the graph to the expected maximum capacitance value and draw schematically the expected graph. The series resistance related measurement should be neglected by the viewer and does not affect the depletion region of the capacitance. It is interesting to note, that for silicon oxide the interface charges dominate the oxide charge, even

though they are a factor 5 lower than in silicon nitride.

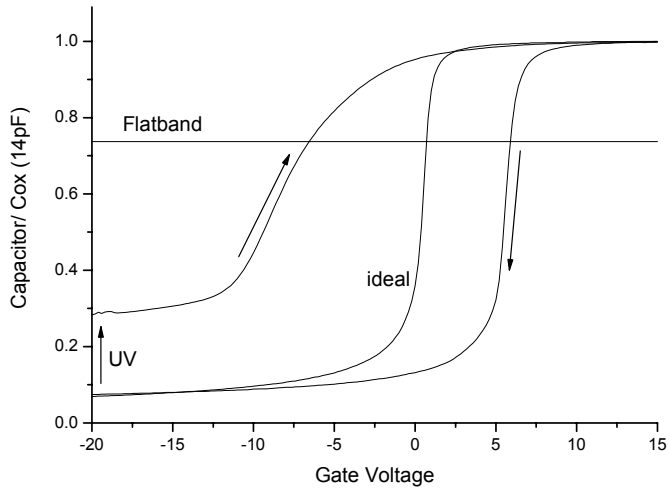

Figure 5.13: CV graph of 40 nm SiO_2 on n-type GaN with and without UV light, measured at 1 MHz. (C_{ox} = 70 pF)

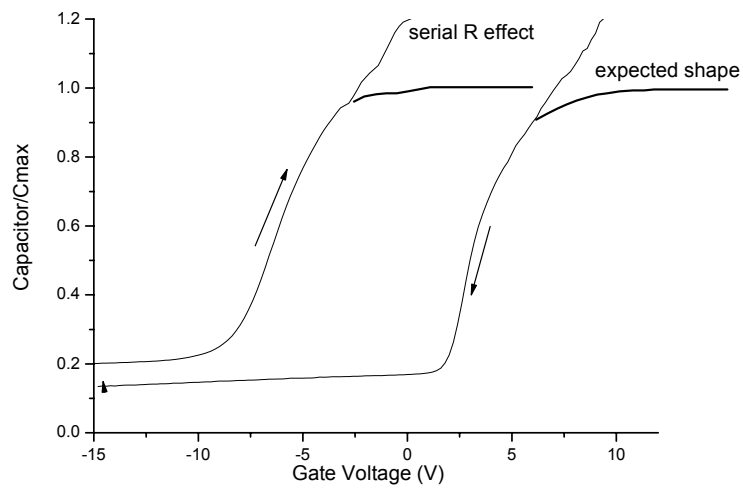

Figure 5.14: CV graph of annealed SiO_2 (72 nm) with and without UV light. Capacitor shows large dispersion at 1 MHz.

The interface state density is summarized in figure 5.15 for n-type and p-type GaN and shows therefore the distribution over the whole band gap. The data were taken from the measurements

according to figure 5.12 for n-type and figure 5.17 for p-type GaN. The series resistance correction was done for every single graph and especially for the p-type result the oxide capacitor value had to be adjusted for every measurement, due to frequency dispersion. The interface density was extracted from peak values of the parallel conductivity with a band bending standard deviation of around 1 for n-type GaN and around 3 for p-type GaN. The corresponding values of f_D for equation 3.10 where 0.33 and 0.2, respectively [76]. The distribution shows quite high symmetry in respect to the intrinsic energy level and peaks again at the band edges. The maximum values from my measurement, correspond to energies below (above) the Fermi level of n-type (p-type) GaN, and therefore give no information about the real quantity of the maximum trap density. It is interesting to note, that in my result the distribution in the lower half shows no higher densities than the upper half, which is in contrast to other reports [54]. The increase is usually noted due to the doping impurities. The values in the inner energy region show a slight increase after a minimum around 0.5-1 eV away from either band edge side. However those results must be seen very critical according to the discussion in 3.1.2 and 3.1.3, since the interface trap coefficients extracted from the parallel conductivity plot where quite constant (similar to figure 5.21 for Al_2O_3), which might be indication that the peak value does not correspond to the actual surface potential, taken from the theoretical graph fitted with the measured one.

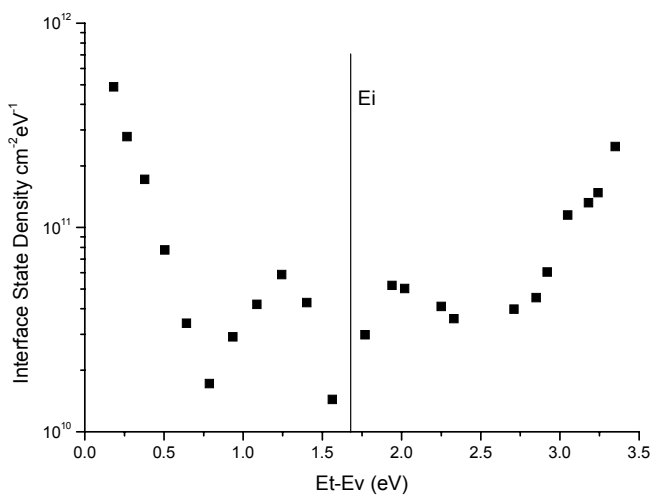

Figure 5.15: Interface state density extracted from p-type sample for the lower half and from n-type sample for the upper half of the band gap.

In order to compare the interface states on the surface to the electron traps in the bulk I inserted our photoluminescence (PL) measurement result from p-type GaN wafer in figure 5.16. The measurement was performed at 1.53 mW from 300 to 700 nm using a 266 nm laser. The graph was drawn over the photon energy and which was plotted reversely, by subtracting the measured energy from the band gap energy, which is described by

$$E_{Bulktrap} = E_g - \frac{k \cdot c}{\lambda}, \tag{5.16}$$

where k is the Boltzmann constant in eV, E_g is the bandgap energy, c is the speed of light and λ is the measured wavelength. Therefore a direct comparison between the bulk trap positions to interface trap positions is possible. The result shows a high correlation repeating the two peaks from the conductive measurement. The PL measurement contains two peaks where the lower one involves the sharp peak from the valence band (it is therefore drawn brighter to be not considered). However the first peak from 0 to 0.7 eV might be related to the magnesium incorporation. It is less recognizable from this graph but gets clearly visible at higher magnesium compositions. The second peak at around 1.25 eV might me stronger related to the bulk impurities. The fact that the bulk impurities seem to dominate the interface traps might be an explanation that the trap density is similar for Mg doped p-type and for the undoped n-type GaN.

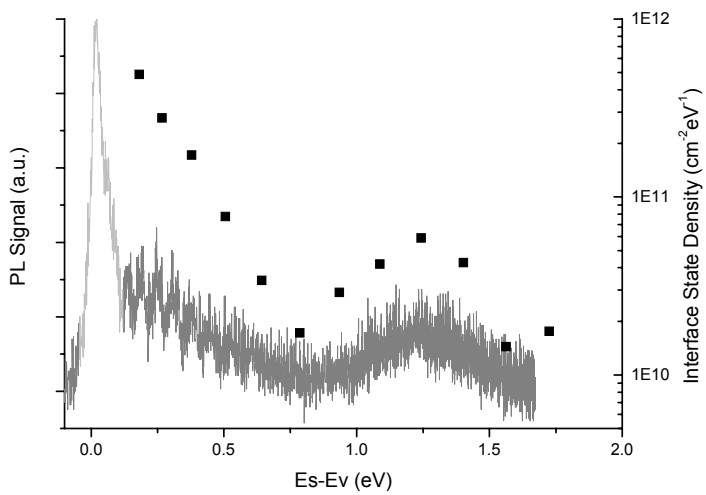

Figure 5.16: Photoluminescence Measurement of Mg doped p-type GaN. The energy is plotted reversely from the conduction band to match it with the valence band. The PL peak from the valence band electrons is drawn light grey, that it can be differed from bulk traps by the viewer's inspection.

In contrast to above discussion, the following part summarizes the results from p-type samples. Figure 5.17 shows the measurement with and without UV light and more clearly points out that no inversions carriers are created during illumination. The graph shifts around 10 V, which results in comparison with the ideal graph to a fixed charge density of $1x10^{12}$ cm^{-2} and a interface charge density of $4.4x10^{12}$ cm^{-2} for the low defect substrate. Even though this is a small improvement compared to the n-type sample, the graph let assume, that no hole carriers could be generated.

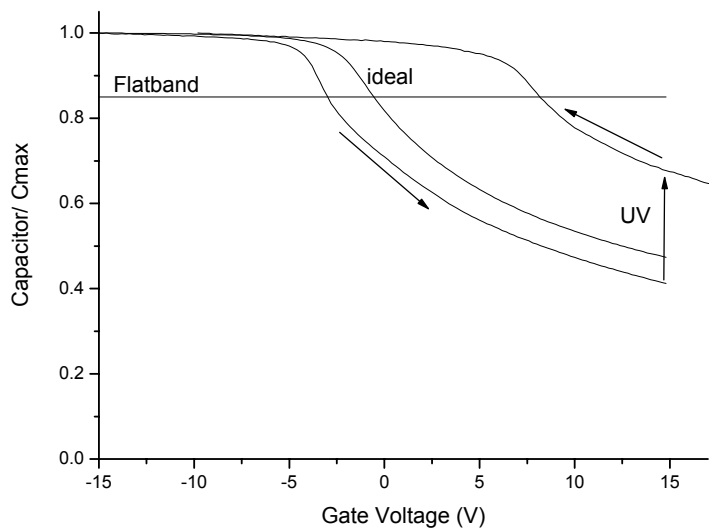

Figure 5.17: CV graph, measured at 1 MHz of p-type SiO_2 capacitor, with and without UV light. Graph is normalized by its maximum, due to dispersion at high frequency. C_{max}= 14 pF/ SiO_2 40nm.

Further, no hysteresis was observed and also no flatband shift for different frequencies as shown in the result of figure 5.18. Additionally, the dispersion effect of p-type GaN appears very clear for all measurement frequencies higher than 1 kHz. Graphs measured below 1 kHz are similar to the ideal shape.

The result changes drastically for the second substrate were no depletion was observed in darkness. Incident light, whether UV or normal white light, could create a shallow depletion and showed a shape similar to inversion for the annealed samples, as presented in figure 5.19. This observation in p-type GaN agrees with the previous reports [54, 55]. However, the following

chapters will prove that the surface could not be inverted. Therefore this observation might be caused by carriers generated during UV light illumination and limited by the oxide capacitor. In fact the interface density on this substrate seemed to be that high, that it prevented the substrate from depletion.

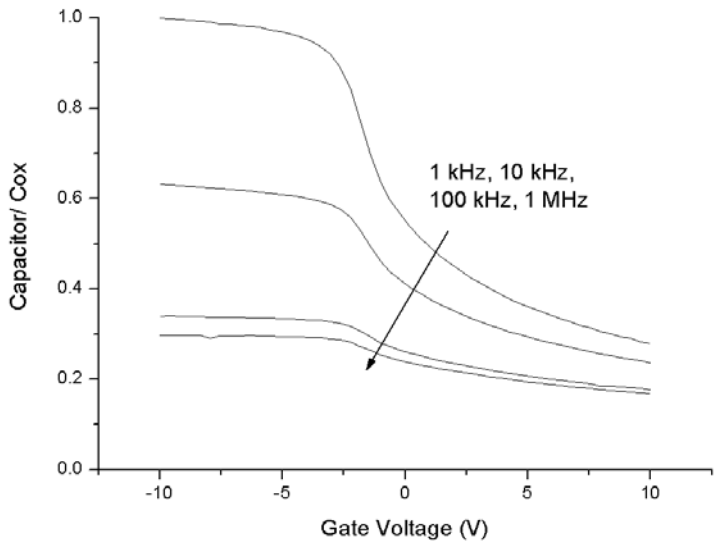

Figure 5.18: Frequency dispersion in p-type GaN with 40 nm SiO_2 (C_{ox} = 70 pF).

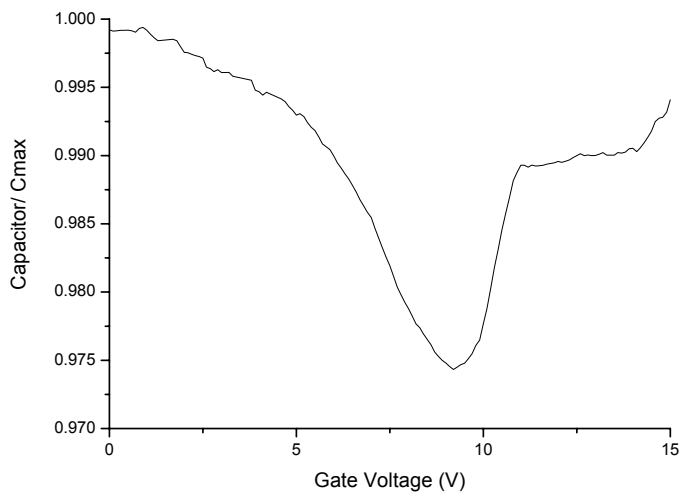

Figure 5.19: Inversion behavior at white light exposure in p-type GaN with 72 nm SiO_2 after annealing. Measurement was done at 1 MHz.

In conclusion, silicon oxide shows an improved interface and the determining factor seems to be the substrate, rather than surface treatment or annealing effects. However the necessary inversion was not observed in any of the used substrates.

5.2.3. Aluminum Oxide (Al_2O_3)

Aluminum oxide shows comparable good results to silicon oxide and a low interface states density for the applied measurement. Figure 5.20 summarized the capacitance measurement with and without UV light exposure during deep depletion. The samples differed in there post-deposition annealing conditions from 750°C and 850°C in oxygen ambient. On sample was used directly from deposition by ALD without any annealing processes. The following graphs also show the ideal CV graph which was calculated for the corresponding substrate background doping density and the oxide capacitor. The oxide thickness varied for every capacitor, due to the annealing. It was tested prior, that a 100Å aluminum oxide film shrinks around 9% in average. This thin thickness and the high dielectric constant resulted into a comparable larger oxide capacitor and explain the different shape of the CV graphs.

The results show that both measured graphs (with and without UV light) shift less from the ideal one, for higher annealing temperatures, which indicates that the fixed charges decrease. However the UV induced shift does not differ a lot, describing quite constant interface charges around $2.6x10^{11}$ cm^{-2}. Both characteristics are summarized in figure 5.21. Additionally the total oxide charges are shown, which represent the sum of fixed and interface charges. As noticed from the large capacitor values the measurement is very sensitive to voltage shifts. Therefore I think that the result of the interface charges is qualitatively correct but the quantities might be slightly different. The extraction of the fixed charges, which are around an order higher than the interface charges, is less sensitivity and they improve from around $6x10^{12}$ cm^{-2} down to below $1x10^{12}$ cm^{-2}.

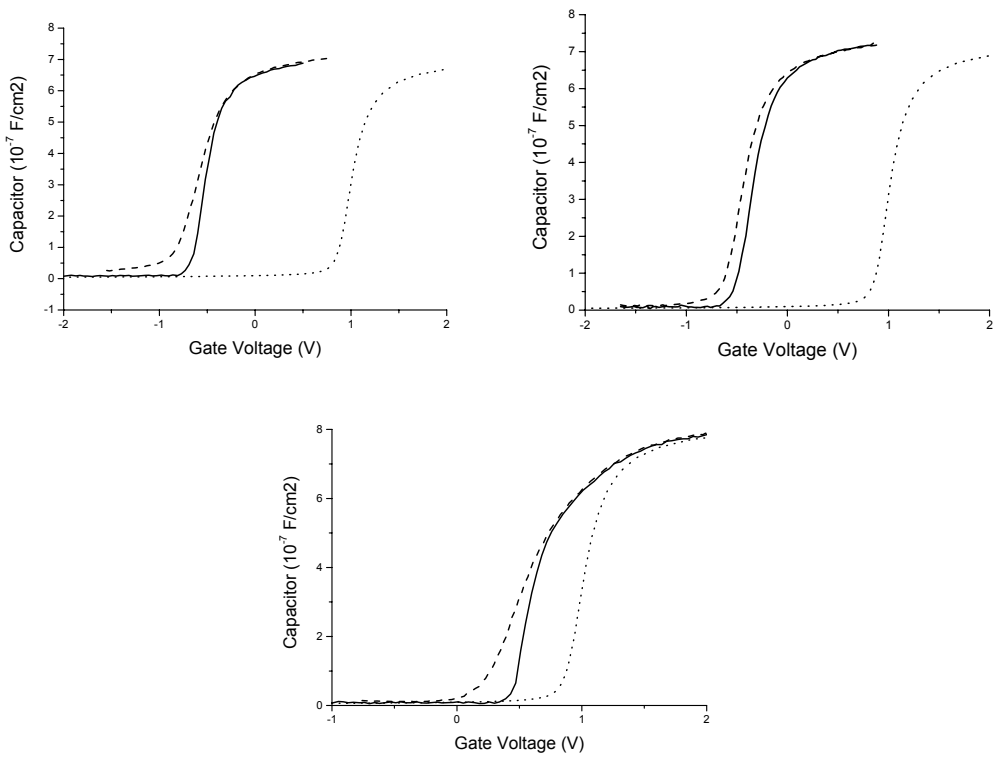

Figure 5.20: CV graphs for Al_2O_3 MOS capacitors for non-annealed (upper, left), 750°C (upper, right) and 850°C (lower) annealed samples.

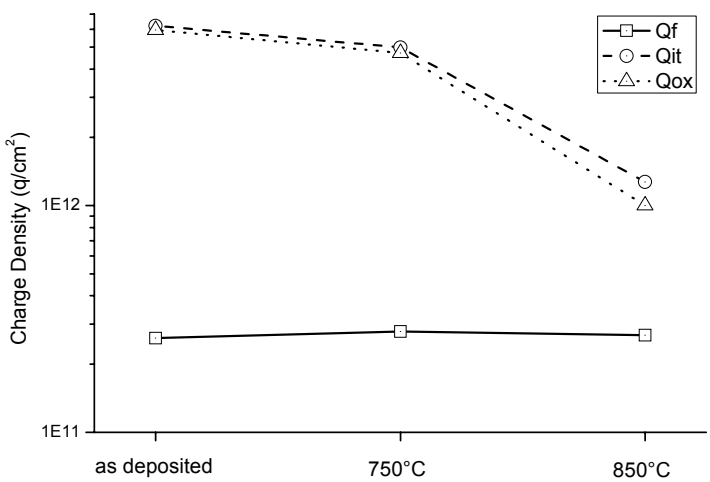

Figure 5.21: Summary of oxide charges, fixed charges and interface charges for different annealing conditions of Al_2O_3

In a second analysis the CV measurement was repeated for the conductivity. The parallel interface conductivity was extracted according to the method described in 3.1.2. The results for the same samples are summarized in figure 5.22. The graphs are shown for constant Gate voltage which is directly related to the surface potential using the theoretic results from chapter 2.3.1. As the capacitive graphs did not show hysteresis or flatband voltage shift for different frequencies, the Gate voltage for same surface potentials can be compared in one graph. All graphs show a peak around 10000 rad/s and some smaller side peaks. Interestingly, the peak value does not differ on the surface potential which is contrary to the theoretical model explained in 3.1.3, assuming that deeper traps (surface potential) correspond to lower frequencies. This constant trap response frequency was also reported from Huang et al. [54] without noticing on that fact.

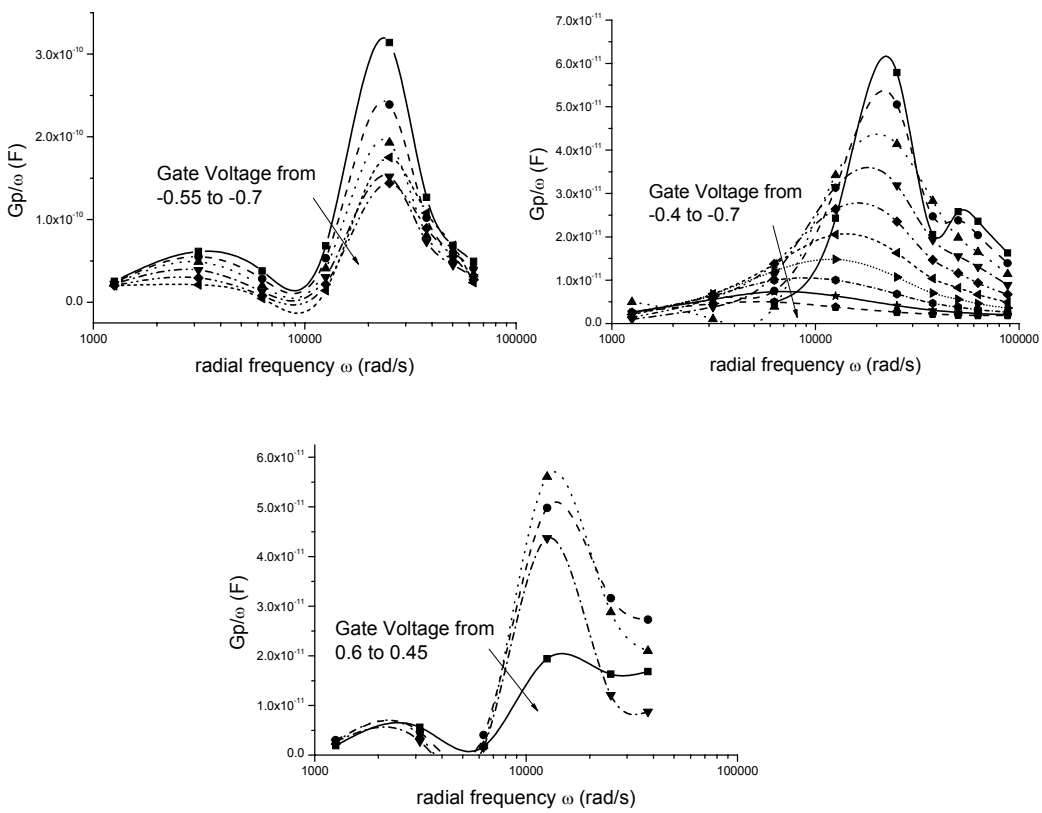

Figure 5.22: Extracted and normalized parallel conductivity for the non-annealed sample (upper, left), the 750°C annealed sample (upper, right) and the 850°C annealed sample (lower).

I assume that this shows that, the response is more or less from the similar surface potential and therefore just vanishes as the Gate voltage biases further into depletion. Under this explanation the resulted interface density in the center region of the band gap would be over-estimated by this measurement. However, using the peak values of the graph from figure 5.22, the interface density summarized in figure 5.23 could be extracted. It shows that the trap density in the middle region of the band gap could be improved by annealing while the density at the edge seems to be quite constant at around $4x10^{11}$ $cm^{-2}eV^{-1}$.

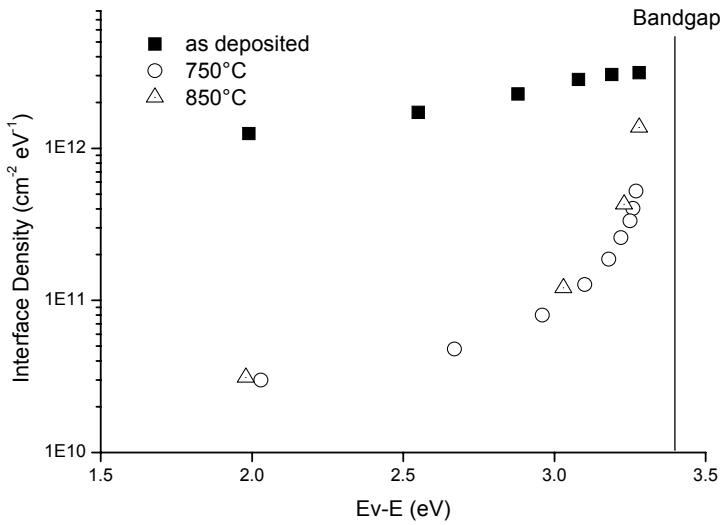

Figure 5.23: Summary of interface state density plotted over the band energy relative to the valence band.

The results from p-type GaN are very similar to the later results of silicon oxide and did not show differences for various annealing conditions. I therefore present only the sample annealed at 700ºC. The behavior was only measured on the higher defect substrate, which seems to be the limiting factor. Without UV light depletion was observed around 10 V after flatband voltage. The UV light increases the amount of electrons and decreases the series resistance which increases the capacitive value in inversion and accumulation. The expected inversion from the graph, even without UV light, could not be proved by the Schottky barrier transistor.

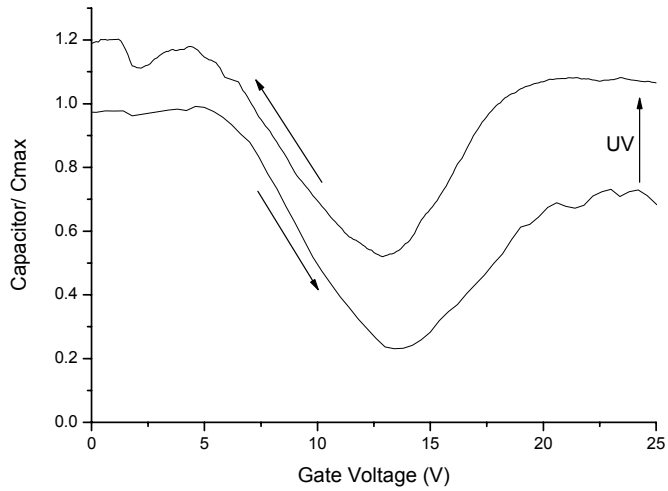

Figure 5.24: CV graph of the 700°C annealed Al_2O_3 sample with and without UV light. The vertical arrow shows the increased capacitance value due to the incident optical energy.

5.3. Mobility Characterization from Gated Hall

In the previous chapter it was shown that most p-type samples showed only slight depletion and no inversion. Therefore the Hall measurement of Schottky barrier devices was not possible. Hence, I focused on the characterization of n-type substrates under accumulation. However the silicon oxide and aluminum oxide sample showed no distinguishable accumulation charges, which made a characterization meaningless. The following part summarizes therefore the silicon nitride interface under accumulation.

Even though the Gated Hall measurement was an improvised measurement method, since our Hall measurement is only set up for four probes, the result were absolute accurate, since no Gate leakage current affected the measurement. This was the most critical issue, since the measurement currents at the Hall device are usually in the micro ampere range and even a low Gate leakage can cause errors in the result. The result is shown for the silicon nitride sample which was annealed at 1000°C after dielectric deposition. The annealed dielectric was only 30 nm thick, but I added another thick Gate dielectric layer in order to decrease the leakage further.

The direct result of the Hall measurement is shown in figure 5.25 for the electron bulk mobility

and the electron density. At the flatband voltage, around 4 V, the carrier concentration increases and the total mobility decreases. The total sheet resistance decreases, as shown in figure 5.26. The flatband voltage differs from the previous chapter because the oxide capacitor is around a factor 3-4 smaller.

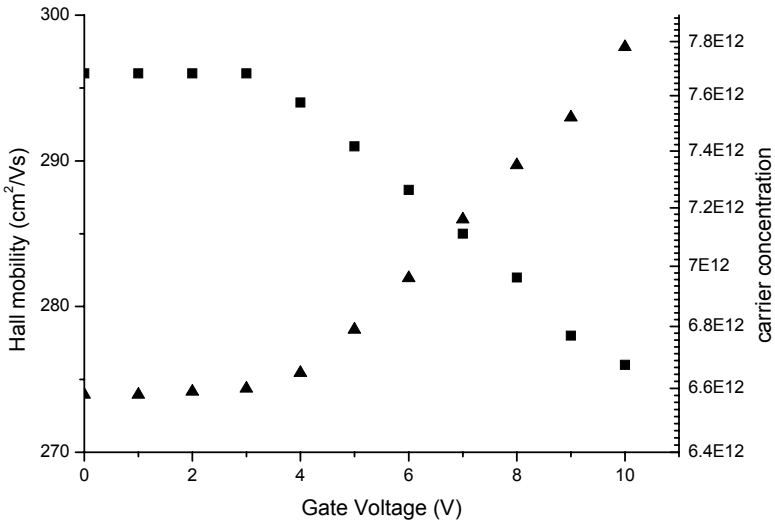

Figure 5.25: Hall measurement result (mobility & sheet carrier concentration) of annealed silicon nitride sample

Below the flatband, the depletion of surface electrons can not be notice, since the measurement sensitivity is low in comparison the bulk charges. However the amount of accumulation charges was large enough to be recognized in the measurement for silicon nitride. I extracting the accumulation charges from the bulk charges, which where taken from the Hall result measured below flatband voltage. This result is shown in figure 5.27 and compared to a theoretical fitted result using a flatband voltage of 3.8 V and an oxide capacitance of $3x10^{-8}$ F/cm^2. This value is very close to the expected one from the fabrication process using a 30 nm silicon nitride and a 150 nm silicon oxide film as Gate dielectric.

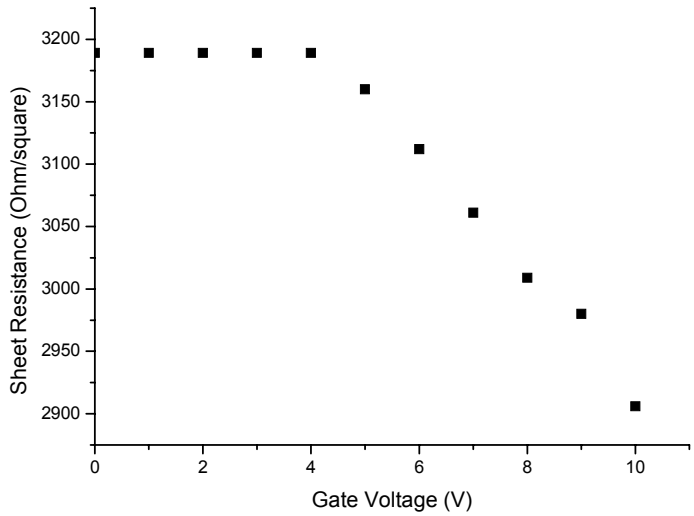

Figure 5.26: Sheet resistance result from Hall measurement

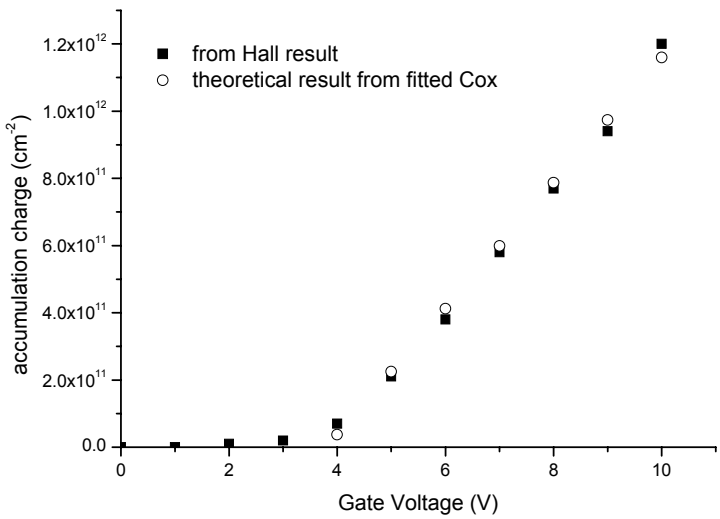

Figure 5.27: Extracted accumulation charges extracted from Hall measurement in comparison to fitted theoretical data (open holes) using a flatband voltage at 3.8 V and a capacitance of $3x10^{-8}$ F/cm^2.

The field-effective mobility was then calculated from the bulk result and the extracted

accumulation charges, assuming that the bulk carrier concentration and mobility do not depend on the Gate voltage and are equal to the Hall result before flatband voltage. Using the fact that the accumulation conductance is parallel to the channel conductance leads therefore to the channel mobility by

$$\mu_{Channel} = \frac{N_{Hall} \cdot \mu_{Hall} - N_{Bulk} \cdot \mu_{Bulk}}{N_{accumulation}}. \qquad (5.17)$$

The resulting graph is shown in figure 5.28 using the accumulation carrier density from Hall measurement and the theoretical result from the fitted data in figure 5.27. The average field effect mobility can be notice around 160 cm^2/Vs. The graph is plotted versus the overdrive voltage. Therefore the first point of the theoretical result varies from the Hall result due to the slower increase of the accumulation charges directly after flatband voltage, where the fitted graph does not match with the measurement.

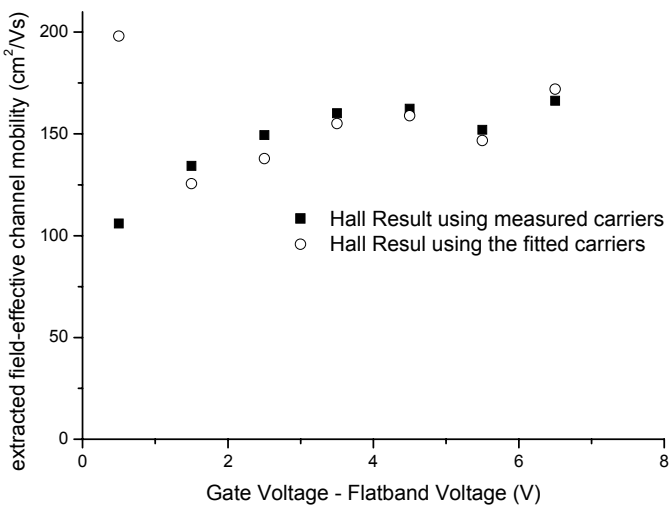

Figure 5.28: extracted field-effective accumulation channel mobility using carrier concentration from the Hall measurement and the theoretical fitted data.

The field-effective mobility saturates at 3 V after flatband voltage and remains quite constant. The first view points lack probably on sensitivity, since the numbers of accumulated charges is too small for an accurate extraction.

5.4. Characterization by 3-Terminal Gated Device

The characterization by transistors was done for depletion and Schottky barrier MOSFET in order to compare the channel behavior. A list of fabricated and compared samples is shown in table 5.1. Silicon Nitride was not tested for Schottky barrier MOSFETs on GaN, due to the insufficient results from the interface characterization. All three dielectric materials where compared for depletion devices, since do not require inversion but even though show effects on the interface charges on the mobility.

However, none of the p-type GaN samples could be proved to be able to invert its surface and create inversion carriers. As a representative device, the measurement results of the annealed silicon oxide interface are shown. The Id-Vg characteristic was as flat as the capacitive result, indication no current modulation in depletion or accumulation according to the shallow depletion observed in the capacitive results.

Schottky Barrier MOSFET			**Depletion MOSFET**		
p-type GaN			Undoped GaN		
SiO_2	SiO_2	Al_2O_3	SiO_2	Si_3N_4	Al_2O_3
no	Furnace	RTP	Furnace	Furnace	RTP
annealing	1000°C	750°C	1000°C	1000°C	750°C
	N_2 gas	O_2 gas	N_2 gas	N_2 gas	O_2 gas

Table 5.1: Summary of succussful fabriacted MOSFET devices

The Id-Vd characteristic is shown in figure 5.29, which was the typical graph for any Gate bias. The forward voltage was only slightly reduced by negative Gate voltage according to an increased number of carriers. However this behavior is far from appropriate device operation. In order to test the electron behavior I illuminated the sample with UV light during the whole measurement, which increased the current, according to the lower energy barrier for electrons. However, the electrons induced by UV light under high positive Gate bias vanished as soon as the light was turned off, shown by the third graph. Therefore it can be assumed that the generated electrons did even not conduct a surface channel.

In conclusion it must be said, that those samples had no ability to create a surface inversion nor

were able to confine light induced carriers at the surface. Therefore it must be doubt, that those p-type GaN wafers are able to create any effective surface depletion. Additionally, Hall measurements could not be examined on p-type sample since the current did not show ohmic characteristic and was not related to the Gate.

The Id-Vg and Id-Vd characteristic of the n-type samples was measured. Since the channel layer was around 2 μm, the devices could certainly not deplete the whole channel. However, this was not required, as the focus lied on the additional accumulated charges for n-type devices. An example of the Id-Vg characteristic is shown in figure 5.30 for annealed silicon oxide. It can be noted, that the surface depletes up to the certain depths and also it is able to accumulate carriers. The leakage current was at least three orders in magnitude lower than the Drain current during measurement and had therefore not influence. The flatband voltage was determined by comparison to a transistor patterns without Gate oxide and allowed to extract the accumulation current.

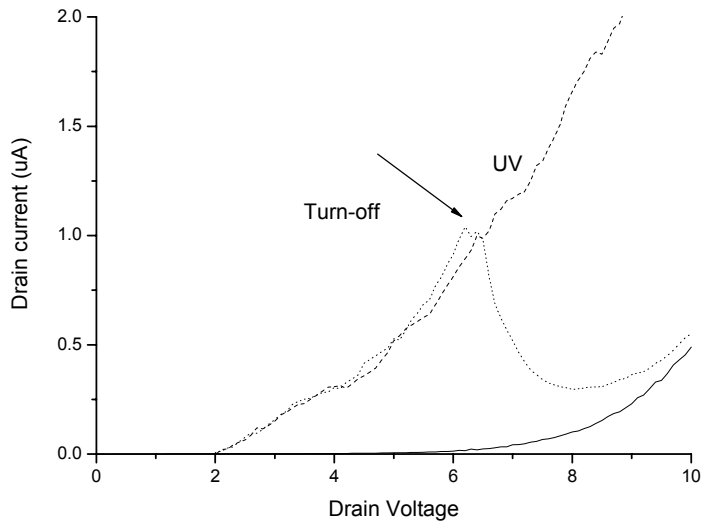

Figure 5.29: Id-Vd characteristic of p-type GaN SCHOTTKY BARRIER MOSFET with and without UV light.

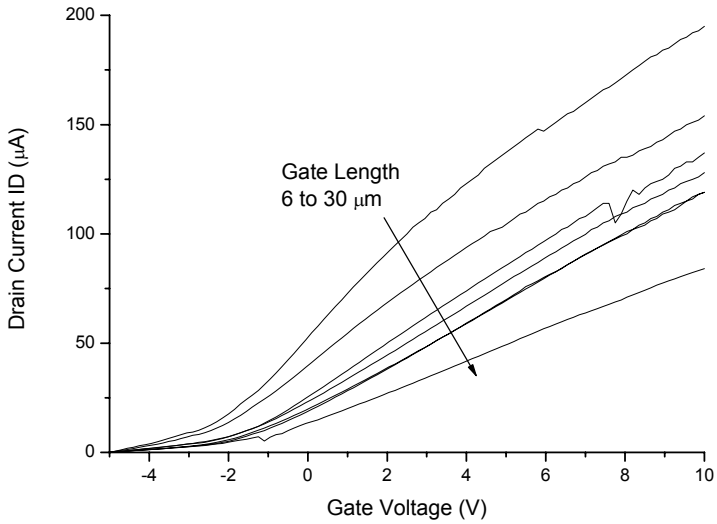

Figure 5.30: Id-Vg Characteristic of annealed silicon nitride depletion Mosfet for several Gate lengths and 80 μm channel width. The flatband voltage was assumed to be around -1 V, by comparing with Gate-less TLM pattern.

These current values were used to calculate the channel resistance according to the accumulation carriers and plotted over the channel length. Another qualitative example is shown in figure 5.31.

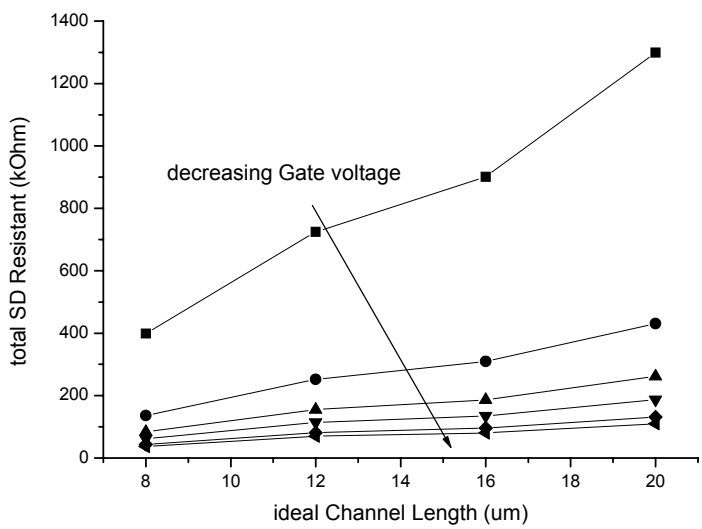

Figure 5.31: Total Source-Drain accumulation resistance over channel length for

annealed silicon oxide depletion MOSFET.

The intersection with the y-axis (at zero Gate length) is negative, which lets assume, that the effective channel length got smaller during thermal annealing of the metallization. This is in accordance to the observation, that the smallest Gate length of 3 μm was shortened. However the applied analysis uses only the slope of the graphs and does therefore only requires the relative channel length. The extracted resistance values were compared to the theoretical expected charge quantities using the theoretical values of the oxide capacitors. The same fitting was used for the Hall measurement. The comparison leads to effective field mobilities expressed by

$$\frac{Rs}{L} = 1/\sigma \cdot \frac{1}{W} = \frac{1}{qN\mu W} \tag{5.18}$$

for every Gate potential above flatband voltage, which is summarized in figure 5.32. Silicon oxide showed the best performance with two times higher mobility values than silicon nitride or aluminum oxide.

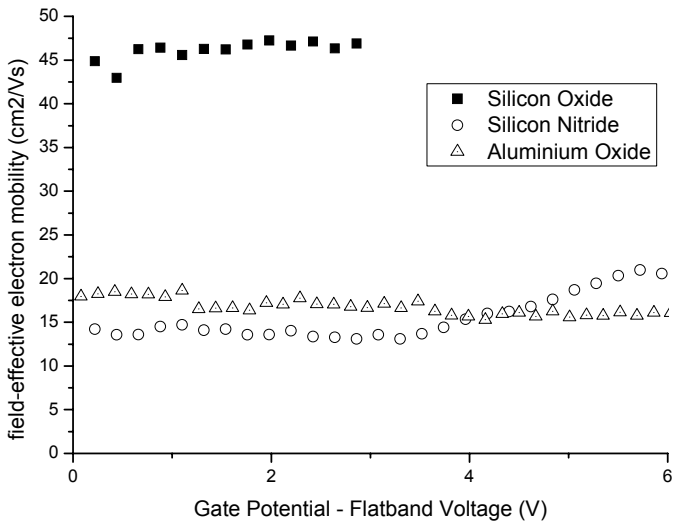

Figure 5.32: Extracted field-effective mobility for annealed silicon oxide, silicon nitride and aluminum oxide over the relative Gate Potential in accumulation.

6. Summary & Conclusion

The aim of this work was to find out the characteristic of GaN MIS structures and their measurement methods in general and the interface properties of certain dielectrics. Unfortunately, no inversion channel current could be proven in the fabricated Schottky barrier transistor design for silicon oxide and aluminum oxide. Therefore the characterization was limited to one half of the band gap for n-type and p-type GaN, respective.

In general the virtual ground concept was successfully integrated in the capacitor design and the series resistance effects in lateral capacitive structure could be described and isolated from the measurement result. Therefore this method allows an accurate and easy measurement design.

The interface charge resulting from the UV induced flatband shifts are summarized in figure 6.1 for all dielectrics under several annealing conditions. The interface condition of silicon nitride was the worst among tested one with an interface charge density higher than 10^{13} cm^{-2}. The results for silicon oxide are generally a factor 5 better regardless the annealing condition. The interface charges for aluminum oxide seem to be extremely low, but the result must be challenged due to the too sensitive and therefore probably inexact measurement. The lowest results of fixed charges are quite same in all dielectrics at around 10^{12} cm^{-2}. The highest annealing effect was achieved in aluminum oxide, which was also proven by a great improvement in the leakage current. Silicon nitride showed also an improvement under thermal treatment, but the high total oxide charge density makes it a weak candidate for MISFET applications. The leakage of silicon nitride was also two orders higher due to its oxide charges. The fact that the minimum achieved fixed charges for any dielectric material are similar is because of the polarization field in GaN. The charges rising from the termination of this field and therefore can not be further reduced by any treatment.

The second interface characterization method led to the interface state density over the bandgap. According to the investigation of n-type and p-type samples, the full bandgap distribution can be shown. However the summary in figure 6.2 neglects results further inside the bandgap than around 1.3 eV from the band edges. As mentioned previously those values are probably not

accurate according to the dynamic trap behavior. The final result for silicon oxide and aluminum oxide shows the typical symmetric distribution and almost same results after thermal treatment of aluminum oxide. The trap density increased to both sides of the band edges. It is therefore difficult to estimate the total number of traps, since an unpredictable amount of traps might be hidden between the Fermi level and the band edge. The lower trap densities of silicon oxide directly at the Fermi level let assume that it might show an improved characteristic in comparison to aluminum oxide. The trap densities within the first 600 meV around the band edge are higher in p-type GaN which is related to the bulk traps according to the comparison with photoluminescence measurement. From several CV results on n-type GaN an inversion-like capacitor shape in depletion was observed in contrast to the expected deep depletion shape. As reported this can be due an enormous trap density which pins the Fermi level. On the other side, several p-type samples showed no depletion at all, which indicates the same high interface density close to the valence band. I therefore believe that those expected traps are the reason for the absence of inversion in both substrates.

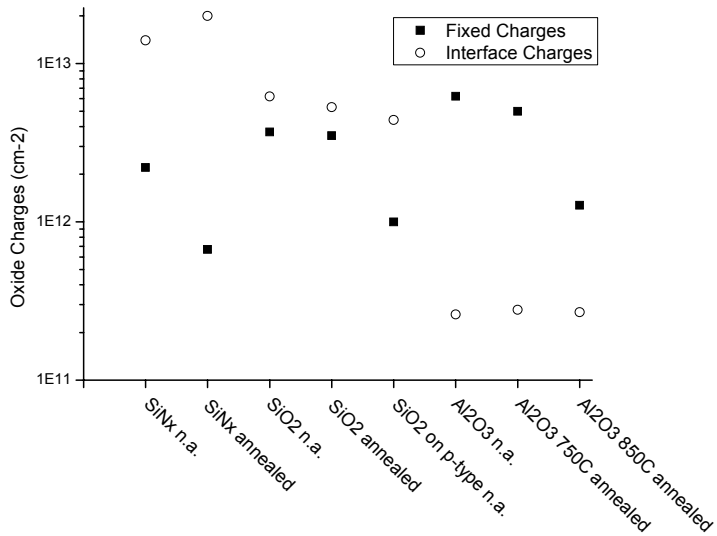

Figure 6.1: Summary of oxide charges in GaN MIS structures. (n.a. = not annealed, silicon oxide and nitride were annealed at 1000°C for 30 min under nitrogen ambient)

The mobility results generally show higher Hall mobilities than conductivity mobilities. The

reason for this might be the theoretical difference due to the scattering mechanism and measurement errors from the transistor analysis due the very simple applied model. The best result was observed for silicon oxide for around 50 cm^2/Vs, while silicon nitride and aluminum oxide showed field-effective conductivity mobilities around 15 cm^2/Vs. In comparison the field-effective Hall mobility for silicon nitride was determined around 150 cm^2/Vs. Both mobilities were extracted from linear device behavior of accumulation n-type transistors. An appropriate device operation could not be observed due to the thick and conductive buffer.

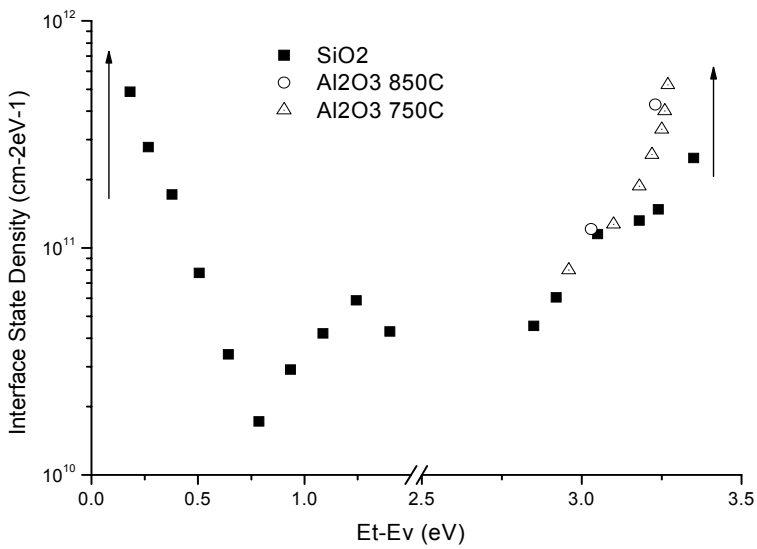

Figure 6.2: Summary of interface state densities in GaN MIS structures. The arrows mark the expected high interface state density near the band edge.

To finally conclude my work, it seems that the limiting parameter of the interface quality is not the dielectric but the epitaxial bulk material. Hence, an optimum result requires low defect and high resistive GaN layers. It should be expected that a decreases in interface trap density allows the Fermi level to invert the material surface. The mobility result from Hall measurement, which is similar to other reports, might not be able to be improved since the oxide charges can not decreased below the fixed charge density, which depends on the internal polarization of GaN.

Outlook and Future Ideas

During reviewing my work, several ideas were suggested to me, mostly from state-of-the-art silicon technologies. In my opinion many concerns which do exist for the Si/SiO_2 interface are not applicable for GaN. For example the oxide charges within the dielectric are not from major interest as long as the polarization induced fixed charges exceed them. Therefore methods as charge pumping might not be used on this kind of structures. However, an interesting idea, which was suggested from Prof. Jong-Ho Lee, might be to compare the interface dependent noise of the channel carrier in accumulation, in comparison for several dielectrics and to the bulk carriers. If a separation between the bulk traps related noise and the interface traps related noise is possible, a more generous statement can be given on the total amount of oxide charges, including all traps of the band gap.

As this work is the starting project of GaN MOSFETs in our laboratory, focusing on the characterization, further work should be done on the epitaxial quality of the GaN substrate. It is absolutely required to reduce the crystal defects as nitrogen vacancies resulting in relatively high conduction bulk material. I believe that the dielectric material issue is less important in Nitride devices since none of them shows an as good result as the silicon/silicon oxide interface. Therefore the contamination of the dielectric seems to be absolute neglectable.

In order to improve the general idea of a GaN MOSFET, I would like to mention my initial idea of this project. Even though I was not able to test the structure, I still believe it has a lot of potential for further research on such devices. The basic idea was to put the channel interface from the GaN surface into the GaN bulk material by growing a second nitride material on the top. A good candidate could be aluminum nitride (AlN) which has a similar band gap to aluminum oxide and a conduction band offset of around 2 eV to GaN. This very thin surface layer would act as a spacer between the channel and the low mobility dielectric and therefore reduces the impact on the channel electrons. This scattering is the main disadvantage of MOSFET devices in comparison to 2DEG channels and the reason why 2DEG mobilities are much higher. However this heterostructure has several problems that need to be solved. First, the standard-known GaN growth by MOCVD results into a wurtzite structure with high polarization fields. Second, in case

of AlN/GaN interfaces an additional stress-related piezoelectric field creates additional interface charges resulting into a 2DEG. Both effects create surface carriers as it is known from depletion devices. In order to prevent those carriers several attempts can be tried. First of all the AlN layer can be grown very thin, which would reduce the stress. Second, a different orientation of GaN can be used instead of the (1000) direction. If another direction is used the polarization field can be decrease or even compensated for spontaneous and piezoelectric polarization. A third possibility is to use cubic GaN with symmetric atomic arrangement. Therefore the spontaneous polarization is zero but stress induced charges still occur at the material interfaces.

However solving this problem by one of those attempts could provide a new type of MOSFET leading to similar current capability then HEMTs but with extremely low off currents. Further, such a device would work in enhancement mode and therefore be an ideal candidate for most applications in industries.

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Appendix A: Typical Parameters of GaN

For Wurzite crystal structure at 300 K

Lattice

Group of symmetry	C^4_{6v}-$P6_3mc$	
Number of atoms in 1 cm^3	$8.9 \cdot 10^{22}$	
Debye temperature	600 K	
Density	6.15 g cm^{-3} @ 300 K	
Lattice constant, *a*	3.160 ÷ 3.190 Å	
	3.189 Å	300 K
Lattice constant, *c*	5.125 ÷ 5.190 Å	
	5.18	300 K
Thermal expansion coefficient, *a*	5.59×10^{-6} K^{-1}	
Thermal expansion coefficient, *c*	3.17×10^{-6} K^{-1}	

Electrical Parameter

Dielectric constant (static)	10.4(3)	$E \| \| c$
	9.5(3)	$E \perp c$
Dielectric constant (high frequency)	5.8(4)	$E \| \| c$
	5.35(20)	$E \perp c$
Breakdown field	~5 x 10^6 V cm^{-1}	
Mobility electrons	=< 1000 cm^2 V^{-1} s^{-1}	
Mobility holes	=< 200 cm^2 V^{-1} s^{-1}	
Diffusion coefficient electrons	25 cm^2 s^{-1}	
Diffusion coefficient holes	5 cm^2 s^{-1}	
Refractive index, *n*	2.29(5)	
Piezoelectric constant		
e_{15}	-0.30 C m^{-2}	
e_{31}	-0.33 C m^{-2}	
e_{33}	0.65 C m^{-2}	

Band Structure

Energy gaps, E_g	3.47 eV	0 K
	3.39 eV	300K

Energy separation between	Γ valley and M-L valleys	1.1 ÷ 1.9 eV
Energy separation between	M-L-valleys degeneracy	6 eV
Energy separation between	Γ valley and A valleys	1.3 ÷ 2.1 eV
Energy separation between	A-valley degeneracy	1 eV

Energy of spin-orbital splitting E_{so}	0.008 eV	
Energy of spin-orbital splitting E_{so}	11(+5,-2) meV	
Energy of crystal-field splitting E_{cr}	0.04 eV	
Energy of crystal-field splitting E_{cr}	22(2) meV	
Effective mass of density of state m_v	1.5 m_0	
Effective electron mass m_e	0.20 m_o	
Effective electron mass $m_{e\perp}$	0.20(2) m_o	
Effective electron mass $m_{e\|\|}$	0.20(6) m_o	
Effective hole masses	0.8 (2) m_o	
Effective hole masses (heavy) m_{hh}	$m_{hh} = 1.4\ m_o$	
	$m_{hhz} = 1.1\ m_o$	
	$m_{hh\perp} = 1.6\ m_o$	
Effective hole masses (light)	$m_{lh} = 0.3\ m_o$	
	$m_{lhz} = 1.1\ m_o$	
	$m_{lh\perp} = 0.15\ m_o$	
Effective hole masses (split-off band) m_s	$m_{sh} = 0.6\ m_o$	
	$m_{shz} = 0.15\ m_o$	
	$m_{sh\perp} = 1.1\ m_o$	
Electron affinity	4.1 eV	
Optical phonon energy	91.2 meV	
Effective Density of States in Conduction band	$N_c \sim= 4.3 \times 10^{14} \times T^{3/2}$ (cm^{-3})	
	2.3×10^{18} cm^{-3}	300 K
Effective Density of States in Valence band	$N_v = 8.9 \times 10^{15} \times T^{3/2}$ (cm^{-3})	
	4.6×10^{19} cm^{-3}	300 K
Band discontinuity		
AIN/GaN(0001)	ΔE_c = 2.0 eV	
	ΔE_v = 0.7 eV	
InN/GaN	ΔE_c = 0.43 eV	
	ΔE_v = 1.0 eV	

Impurities, Donors & Acceptors

Donors, Ionization Energy (Et-Ec)

Si	0.12-0.02 eV	Ga Site
V_N (vacancy)	0.03; 0.1 eV	N Site
C	0.11-0.14 eV	Ga Site
Mg	0.26; 0.6 eV	N Site

Acceptors, Ionization Energy (Ev-Ev)

V_{Ga} (vacancy)	0.14 eV	Ga Site
Mg	0.14-0.21 eV	Ga Site
Si	0.19 eV	N Site
Zn	0.21-0.34 eV	Ga Site
Hg	0.41 eV	Ga Site
Cd	0.55 eV	Ga Site
Be	0.7 eV	Ga Site
Li	0.75 eV	Ga Site
C	0.89 eV	N Site
Ga	0.59-1.09	N Site

Appendix B: Mathcad Code for CV Calculation

Mathcad sheet for CV calculation of n-type GaN MIS structure according to chapter 2.3.1

Constants

$\varepsilon := 8.854187810^{-14}\ \frac{F}{cm}$ $T := 300$ $k1 := 8.6173431 0^{-5}\ \frac{eV}{K}$ $q := 1.602 10^{-19}$ C

$k := k1 \cdot q$ $Vt := \frac{k \cdot T}{q}$ $Vt =$

Material parameter

$Nc := 2.8 \cdot 10^{19}$ $Eg := 3.42$ $N := 10^{17}$ $Wox := 10 \cdot 10^{-7}$ cm $\varepsilon s := \varepsilon \cdot 10$ $\varepsilon ox := \varepsilon \cdot 4$

$L := \sqrt{\frac{\varepsilon s \cdot k \cdot T}{q^2 \cdot N}}$ $ni := Nc \cdot e^{\frac{-Eg \cdot q}{2 \cdot k \cdot T}}$ $Cox := \frac{\varepsilon ox}{Wox}$ $Vsth := \frac{-k \cdot T}{q} \cdot 2 \cdot \ln\left(\frac{N}{ni}\right)$

$L =$ $ni =$ $Cox =$ $\frac{F}{cm^2}$ $Vsth =$

MOS $Vs := -20.01, -19.99 .. 3$

$$Cs(Vs) := \left| \frac{\sqrt{2 \cdot q \cdot \varepsilon s \cdot N}}{-2} \cdot \frac{1 - e^{\frac{Vs}{Vt}}}{\sqrt{Vt \cdot \left(e^{\frac{Vs}{Vt}} - 1\right) - Vs}} \right|$$

$$Qsc(Vs) := \sqrt{2 \cdot q \cdot \varepsilon s \cdot N} \cdot \sqrt{Vt \cdot \left(e^{\frac{Vs}{Vt}} - 1\right) - Vs}$$

$$C(Vs) := \frac{Cs(Vs) \cdot Cox}{Cs(Vs) + Cox}$$

Flatband

$Qss := 0$ $\phi := 0$ $\rho(x) := 0$

$$Vfb := \frac{-1}{Cox} \cdot \left[Qss + \int_{-Wox}^{0} \left(1 + \frac{x}{Wox}\right) \cdot \rho(x)\, dx - \phi \cdot \frac{\varepsilon \cdot 4}{Wox} \right] \qquad Vfb =$$

$$Va(Vs) := Vs + \frac{\frac{Vs}{|Vs|} \cdot Qsc(Vs)}{Cox} + Vfb$$

Appendix C: Numerical CV Solution

In comparison to the previous appendix, this calculation contains a numerical solution for the inverse function of Va(Vs). Therefore the parametric analysis for C(Va) can be directly expressed and does not need the computation of two individual functions. This is not only convenient due to less computation, but also allows matching the calculation with the measurement points and therefore a direct comparison of the Gate voltage with the surface potential. It turns out, that this is a great advantage, as the dependence of the original function becomes exponentially.

The code includes two functions. One defines the original function Va(Vs) for n-type and p-type materials as well as for inversion and non-inversion charges. Later one is used for deep depletion graphs only. At first, the general semiconductor and MIS structure parameters are defined or calculated. The second part derives the inverse function for the required Gate potentials. The last part calculates the capacitor of the MIS structure according to the surface potential. The numerical solution is found by the regula falsi method. The default initial guess is the given Gate voltage. If no solution is found an offset is added on the initial guess and the computation repeats. The offset changes by size and sign for a few more tries attempts until the user is informed that no solution was found. This method was chosen since the low frequency solution contains two exponential function, making a convergence quite difficult if it starts on the wrong side. However it was found out, that most points do not require is safety mechanism. Therefore the calculation is not slowed down.

```
function Result=CV_sekant(curve,substrate,dielectric,Wox,gate,N,sub_type,M_start,M_stop,M_step)

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% curve:          Type of CV graph                    - LF,HF,deep_depletion     %
% substrate:      Substrate Material          - GaN, Si                          %
% dielectric:     Dielectric Material         - SiO2, SiNx, Al2O3                %
% Wox:            Thickness of Dielectric, nm                                    %
% gate:           Gate Material               - Al, Ni, Au                       %
% N:              Sub. Doping Density, cm-3                                      %
% sub_type:       Substrate Doping Type       - n-type, p-type                   %
% M_start:        Measurement Start                                              %
% M_stop:         Measurement Stop                                               %
% M_step:         Measurement Step                                               %
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

global Vt;
global es;
```

```
global N_;
global Vfb;
global Cox;
global ni;

e0=8.8541878e-14;
T=300;
k_eV=8.61734301e-5;
q=1.602e-19;
k=k_eV*q;
Vt=k*T/q;

%-----------------------------------------------------------
%       Parameter Definition
%-----------------------------------------------------------

switch substrate
      case {'GaN','Gallium Nitride','gallium nitride'}
            Nc=2.73e18;
            Eg=3.42;
            es=e0*10.4;
            X=4.31;
      case {'Silicon','silicon','Si'}
            Nc=2.8e19;
            Eg=1.08;
            es=e0*11.8;
            X=4.17;
      otherwise
      error('Unknown Substrate')
end

switch dielectric
      case 'SiO2'
            eox=e0*3.9;
      case {'Si3N4','SiN','SiNx'}
            eox=e0*7.4;
      case 'Al2O3'
            eox=e0*9.1;
      case 'AlN'
            eox=e0*8.5;
      otherwise
      error('Unknown Dielectric')
end

switch gate
      case {'Al','aluminum','Aluminum'}
            Wm=4.08;
      case {'Ni','nickel','Nickel'}
            Wm=5.15;
      case {'Au','Gold','gold'}
            Wm=5.1;
      case {'Cu','copper','Copper'}
            Wm=4.7;
      otherwise
      error('Unknown Gate')
end
```

```
N=abs(N);          %cm-3
Wox=abs(Wox)*1e-7;      %nm->cm

Cox=eox/Wox;
ni=Nc*exp(-Eg/(2*Vt));
switch sub_type
      case 'n'
            Ws=X+Eg/2-Vt*log(abs(N)/ni);
            safe=-2;
      case 'p'
            Ws=X+Eg/2+Vt*log(abs(N)/ni);
            safe=2;
      otherwise
            if(N<0)
                  Ws=X+Eg/2-Vt*log(abs(N)/ni);
                  sub_type = 'n';
            else
                  Ws=X+Eg/2+Vt*log(abs(N)/ni);
                  sub_type = 'p';
            end
end
N=abs(N);          %cm-3
N_=N;
Vfb=Wm-Ws;
L=(es*Vt/q/N)^0.5;

switch curve
      case {'deep_depletion','Deep_Depletion','deepdepletion','DeepDepletion','dd','DD'}
            inv=0;
      case {'LF','lf','lowfrequency','lowF','lowf','HF','hf','highfrequency','highF','highf'}
            inv=1;
end

%-------------------------------------------------------------
%       Fitting Vs to Va
%-------------------------------------------------------------

Va=M_start:M_step:M_stop;
Vs=zeros(1,size(Va,2));
dx=1;
eps=1e-7;
kmax=500;
done=0;
safe=0;s=1;
for i=1:size(Va,2)
      safe=0;s=1;
      y=Va(i);
      while (done==0 || safe>10);
            x=y+s*safe;
            x_last=x+dx;
            for k=1:kmax
                  x_next=x-(Va_func(x,inv,sub_type)-y)*(x-x_last)./(Va_func(x,inv,sub_type)-
Va_func(x_last,inv,sub_type));
                  x_last=x;
                  x=x_next;
                  if(abs(Va_func(x,inv,sub_type)-y)<eps)
                        done=1;
```

```
                    break
                end
            end
            if(done==0)

                safe=safe+1
                if(safe>10)
                    %error('no solution was found');
                s=s*(-1);
            end
        end
        done=0;
        Vs(i)=x;
end
Vs(find(Vs==0))=0.00000001;

%-----------------------------------------------------------
%       Find CV
%-----------------------------------------------------------

switch curve
    case {'deep_depletion','Deep_Depletion','deepdepletion','DeepDepletion','dd','DD'}
        switch sub_type
            case 'n'
                Cs=abs((2*q*es*N)^0.5/(-2)*(1-exp(Vs/Vt))./(Vt*(exp(Vs/Vt)-1)-Vs).^0.5);
            case 'p'
                Cs=abs((2*q*es*N)^0.5/(-2)*(exp(-Vs/Vt)-1)./(Vt*(exp(-Vs/Vt)-1)+Vs).^0.5);
        end
    case {'LF','lf','lowfrequency','lowF','lowf'}
        switch sub_type
            case 'n'
                Cs=abs((2*q*es*N)^0.5/(-2)*(1-exp(Vs/Vt)+(ni/N)^2*exp(-Vs/Vt))./(Vt*(exp(Vs/Vt)-
1)-Vs+Vt*(ni/N)^2*(exp(-Vs/Vt)-1)).^0.5);
            case 'p'
                Cs=abs((2*q*es*N)^0.5/(-2)*(exp(-Vs/Vt)-1-(ni/N)^2*exp(Vs/Vt))./(Vt*(exp(-Vs/Vt)-
1)+Vs+Vt*(ni/N)^2*(exp(Vs/Vt)-1)).^0.5);
        end
    case {'HF','hf','highfrequency','highF','highf'}
        switch sub_type
            case 'n'
                Cs=abs((2*q*es*N)^0.5/(-2)*(1-exp(Vs/Vt))./(Vt*(exp(Vs/Vt)-1)-Vs).^0.5);
            case 'p'
                Cs=abs((2*q*es*N)^0.5/(-2)*(exp(-Vs/Vt)-1)./(Vt*(exp(-Vs/Vt)-1)+Vs).^0.5);
        end
    otherwise
        error('Unknown Curve Type')
end
C=Cs*Cox./(Cs+Cox);

figure; plot(Vs,C); title('CV graph vs Surface Potential');
figure; plot(Vs,Va); title('Applied Voltage vs. Surface Potential');
figure; plot(Va,C); title('Caluclated CV-Graph'); axis([-10 10 0 Cox]);

Result=zeros(2,size(Va,2));
Result(1,:)=Va;
Result(2,:)=C;
```

```
figure; plot(R(1,:),R(2,:)); title('CV');
```

The part shows the sub-function called in the upper code which solves the original Gate voltage for a given surface potential. This function is inverted by the shown regula falsi algorithm. The case involves the functions with and without inversion charges and for n-type and p-type material.

```
function Va=Va_func(Vs,inv,sub)

q=1.602e-19;
global Vt;
global es;
global N_;
global Vfb;
global Cox;
global ni;

switch inv
      case 1
            switch sub
                  case 'n'
                        Va=Vs+sign(Vs)*(2*q*es*N_)^0.5*(Vt*(exp( Vs./Vt)-1)-Vs+Vt*(ni/N_)^2*(exp(-
Vs./Vt)-1)).^0.5./Cox+Vfb;
                  case 'p'
                        Va=Vs+sign(Vs)*(2*q*es*N_)^0.5*(Vt*(exp(-Vs./Vt)-
1)+Vs+Vt*(ni/N_)^2*(exp( Vs./Vt)-1)).^0.5./Cox+Vfb;
            end
      case 0
            switch sub
                  case 'n'
                        Va=Vs+sign(Vs)*(2*q*es*N_)^0.5*(Vt*(exp( Vs/Vt)-1)-Vs).^0.5./Cox+Vfb;
                  case 'p'
                        Va=Vs+sign(Vs)*(2*q*es*N_)^0.5*(Vt*(exp(-Vs/Vt)-1)+Vs).^0.5./Cox+Vfb;
            end
end
```
