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DISSERTATION

Photodiode Modeling and Optoelectronic Integrated Circuits for Optical - Data - Storage Applications

ausgeführt zum Zwecke der Erlangung des akademischen Grades eines
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Die Neugier steht immer an erster Stelle
eines Problems, das gelöst werden will.

Galileo Galilei
(1564 - 1642)

Diese Arbeit wurde unter der Leitung von Univ. Prof. Dr. -Ing. Horst Zimmermann am Institut für Elektrische Mess- und Schaltungstechnik der Technischen Universität Wien durchgeführt. Ich möchte mich an dieser Stelle für die zahlreichen Diskussionen und wertvollen Ratschläge bei den Institutskollegen bedanken. Allen voran gilt mein Dank Herrn Prof. Zimmermann. Seine Unterstützung war ein Grundstein bei der Erstellung der Dissertation.

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Zusammenfassung

In optoelektronischen Bausteinen werden in Sperrrichtung betriebene Photodioden als Lichtsensoren verwendet, welche einfallendes Licht in Photoströme umwandeln. Um die meist sehr kleinen Stromsignale weiterverarbeiten zu können, werden die Photodioden in der Regel mit nachfolgenden Verstärkerschaltungen gekoppelt. Für opto-elektronische Hochgeschwindigkeitsanwendungen auf dem Gebiet der fasergebundenen Kommunikation werden als Photodioden meist spezielle III/V Halbleiter Technologien benutzt. Das bedeutet, das "Multichip-Gehäuse" notwendig sind, in welchen Photodioden und Verstärker-Schaltungen in unterschiedlichen Technologien implementiert und durch "Wire-bond" oder "Flip-Chip" Methoden im Gehäuse verbunden werden. Das verursacht aber großen Aufwand und dadurch hohe Kosten. Für viele "low-cost" Anwendungen im Bereich der Unterhaltungselektronik ist daher ein in eine Standard IC-Technology integrierter Photosensor deutlich kostengünstiger. Diese Art von Schaltungen werden auch "Opto-Elektronische-Integrierte-Schaltungen" (OEIC) genannt. Aber nicht nur aus Kostengründen, sind OEICs interessant. Auch die elektrische Performance kann optimiert werden, da parasitäre Effekte im Gehäuse deutlich reduziert werden können. Aus diesen Gründen wurden OEICs während der letzten 10 Jahre auch für Hochfrequenzanwendungen im Bereich der optischen Datenspeicherung und optischen Datenübertragung über Plastikfasern vermehrt eingesetzt. Die Integration von Photodioden, analogen Verstärker-Schaltungen sowie Signal-Verarbeitungsschaltungen auf einem Siliziumchip bietet für diese Anwendungen einen deutlichen Vorteil bei den Produktionskosten. Natürlich können OEIC Schaltungen nicht die Anwendungen mit höchster Geschwindigkeit von $> 10\,\text{GHz}$ abdecken, da nur Photodioden in Standard Silizium verwendet werden. Auch die Geschwindigkeitsperformance der Standard CMOS oder BiCMOS Transistoren ist für diese Anwendungen zu gering. Typische Anwendungen für OEICs benötigen Bandbreiten von 100 MHz bis einigen GHz bei einer Lichtwellenlänge von 400 nm bis 800 nm. Für diesen Anwendungsbereich bietet die in dieser Arbeit benutzte Silizium BiCMOS Technologie ein Optimum an Performance und Kosten.

In dieser Arbeit wird die Theorie und Entwicklung von Photodetektoren sowie analogen Verstärker-Schaltungen im Bereich optischer Datenspeicherung präsentiert. Sie kann grob in zwei Hauptgebiete eingeteilt werden. Der erste Teil behandelt die Integration und die Modellierung von Photodioden in einer BiCMOS Technologie. Die notwendige Theorie über Reflexion und Transmission von Licht an Halbleiteroberflächen sowie das dynamische Verhalten von optisch generierten Ladungsträgern im Silizium und an pn-Übergängen wird im ersten Kapitel gezeigt. Zusätzlich wird die Integration von Pho-

todioden in eine 0.5 μm Standard-BiCMOS Technologie, sowie die Integration von high-performance PIN-Photodioden beschrieben. Die Integration der PIN-Photodioden Option benötigt zusätzliche Prozeßschritte, die im Rahmen eines EU-Förderprojektes mit Namen "INSPIRED" entwickelt wurden.

Das darauf folgende Kapitel zeigt die Erstellung eines SPICE Modells für eine BiCMOS "Doppel-Photodiode". Das Model berücksichtigt die Modellierung von zeitabhängigen Drift- und Diffusionsströmen, sowie auch eine Beschreibung der wellenlängenabhängigen Photodiodenempfindlichkeit. Zusätzlich wird das 3 - dimensionale Photodiodenverhalten durch eine Netzwerknäherung beschrieben. Ein "Mathematica" Programm wurde entwickelt, um die Photodiodengeometrie zu definieren und die SPICE Netzliste des Photodiodenmodels automatisch zu generieren. Das Model kann bei der Schaltungsentwicklung für analoge transiente Simulationen im Zeitbereich, sowie Kleinsignal AC-Simulationen im Frequenzbereich verwendet werden.

Der zweite Themenbereich der Arbeit behandelt die Theorie und Entwicklung von analogen Verstärker-Schaltungen, die bei OEICs im Bereich optischer Datenspeicherung eingesetzt werden sollen. Eine wichtiger Basisblock für OEICs ist dabei die Transimpedanz-Verstärkerschaltung (TIA). Ein Kapitel behandelt daher die Analyse von Stabilität, Bandbreite und Rauschen von TIA Schaltungen. Weiters werden verschiedene "single-ended" und differentielle TIA Schaltungen präsentiert. Da speziell für TIAs im Bereich optische Datenspeicherung die Eingangs-Lichtintensitäten über weite Bereiche schwanken kann, werden TIA Architekturen mit verstellbarer Verstärkung diskutiert. Weiters wird ein neues TIA Konzept mit variablen Stromverstärker als Eingangsstufe (ITIA) vorgestellt, welches eine Verstärkungsvariation über mehr als 3 Dekaden, bei gleichzeitig hoher Bandbreite von 260 MHz erlaubt.

Ein abschließendes Kapitel präsentiert die Entwickung und Charakterisierung eines OEIC Prototypen, der für "optical-pickup-units" in optischen Speicherlaufwerken eingesetzt werden soll. Die Spezifikation wurde gemeinsam mit der Firma Philips definiert, die auch Partner im Projekt "INSPIRED" war. Der Prototyp sollte die Spezifikation für alle drei zur Zeit (und in nächster Zukunft) aktuellen Standards CD, DVD und "Blu-ray" abdecken. Für die Schaltungsentwicklung wurde die im ersten Kapitel vorgestellte 0.5 μm BiCMOS Technologie mit integrierter PIN-Photodiode verwendet. Neben der OEIC Architektur, werden verschiedene Schaltungskonzepte diskutiert und abschließend noch Meßergebnisse des Prototypen vorgestellt.

Abstract

The first part of this work presents the integration and modeling of high-speed photodiodes in a 0.5 μm BiCMOS process. This includes the necessary theory on light transmission and reflection on silicon surfaces, as well as the dynamic carrier behavior inside silicon and pn-junctions. Two examples for photodiode integration are presented. A "standard" photodiode without process modification and a high-performance PIN photodiode, that requires additional process steps. Finally a photodiode SPICE model is shown that includes time-dependent carrier drift and diffusion effects as well as 3-dimensional behavior by using a network approximation. A "Mathematica" script is used to design the photodiode geometry and automatically generate a photodiode SPICE model netlist.

In the second part of this work an optoelectronic receiver IC for CD, DVD and Blue-Laser optical data storage applications is presented. The IC was developed in a 0.5 μm BiCMOS technology with integrated PIN-photodiodes. It includes a new architecture of high-speed and low-noise variable gain transimpedance amplifiers witch current pre-amplifier input. The amplifier transimpedance gain is programmable over a gain range of 130 Ω to 270 kΩ with a serial interface. The amplifier small-signal bandwidth is 260 MHz for highest gain which gives a gain-bandwidth-product of 70 THzΩ and a sensitivity improvement by a factor of 2 compared to published OEICs. The amplifiers support a special write/clip mode which realizes a nonlinear gain reduction for high input signals. The output voltage buffers are 130 Ω impedance matched for optimized data transmission over a flex cable. The impedance is generated with active - impedance synthesis to increase the output dynamic range.

Contents

List of Constants and Appreviations

Constants

c_0	Vacuum light velocity $3 \cdot 10^8$ m/s
D_n, D_p	Diffusion coefficient for electrons and holes (cm^2/s)
$e(= q)$	Electron charge $1,60 \cdot 10^{-19}$ C
h	Plank Constant $6,63 \cdot 10^{-34}$ Js
k	Boltzmann Constant $1,38 \cdot 10^{-23}$ J/K
N	Complex refractive index
n	Refractive index
n_i	Intrinsic carrier density $1.45 \cdot 10^{10}$ cm^{-3} for silicon
R	Photodiode responsivity
V_T	Thermal voltage ($V_T = kT/q \approx 26mV$ at T=300K)
ϵ_0	Vacuum permitivity $8.854 \cdot 10^{-12}$ F/m
ϵ_{Si}	Relative permitivity of silicon (11.9)
ϵ_{Ox}	Relative permitivity of SiO_2 (3.9)
η	Photodiode quantum efficiency (generated carriers per incident photon)
κ	Optical extinction coefficient
μ_n, μ_p	Mobility of electrons and holes (cm^2/Vs)

Appreviations

ADC	**A**nalog to **D**igital **C**onverter
ARC	**A**nti **R**eflection **C**oating
BER	**B**it **E**rror **R**ate
BiCMOS	**Bi**polar **CMOS**
BIP	**Bip**olar
CD	**C**ompact **D**isc
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
DPD	**D**ouble **P**hoto **D**iode
DVD	**D**igital **V**ersatile **D**isc
DSP	**D**igital **S**ignal **P**rocessing
GaAs	**Ga**llium **A**r**s**enide
Ge	**Ge**rmanium

IC	**I**ntegrated **C**ircuit
IFX	**I**nfineon Technologies
LED	**L**ight **E**mitting **D**iode
OEIC	**O**pto **E**lectronic **I**ntegrated **C**ircuit
OPU	**O**ptical **P**ickup **U**nit
OTA	**O**perational **T**ransconductance **A**mplifier
Pdes	**P**hotodiode **des**igner (Mathematica tool)
PNM	**P**hotodiode **N**etwork **M**odel
POF	**P**lasitc **O**ptical **F**ibers
Si	**Si**licon
SCR	**S**pace **C**harge **R**egion
TIA	**T**rans **I**mpedance **A**mplifier
VGA	**V**ariable **G**ain **A**mplifier

Chapter 1

Introduction

In optoelectronics or photonics devices light is interacting with electrons in semiconductor materials. Such devices can be divided into two groups. The first group are devices that convert electrical energy into optical radiation. For example the LED (light emitting diode) or laser diode (light amplification by stimulated emission of radiation). The second group are devices that convert optical radiation into electrical signals. These cover the group of photodetectors on one hand and also photovoltaic devices like solar cells on the other hand. The scientific investigation and also commercial utilization of optoelectronics devices is ongoing since many decades in the last century and therefore it is as old as microelectronics itself. The most important investigations on the interaction of light with solids go back to the beginning of last century when Albert Einstein presented the photo-electric-effect in 1905 which was the starting point for development of photonics devices. The first LED came up in the 1970's [1] while lasers are even older and go back to the invention of the masers (microwave amplification by stimulated emission of radiation) by Townes in 1954 [2]. The first high-speed photodetectors for optical data communication were published in 1970 [3], [4].

For most high-end optoelectronics applications in the field of optical fiber receivers, special technologies like III/V semiconductors are used. This means a discrete or hybrid solution with wire-bonded silicon circuits in a multi-chip package and therefore high costs and effort. For many low-cost consumer applications an integrated sensor and amplifier solution in a standard IC technology is much more cost efficient. These kind of ICs are also called opto-electronic-integrated-circuits (OEIC). But not only for cost reasons a monolithic photodiode integration is of interest. Also the electrical performance of an OEIC can be optimized compared to a discrete solution, due to reduced parasitics in the photodetector-IC interface. Therefore a lot of research was done during the last 15 years to implement integrated photodiodes in CMOS or BiCMOS IC technologies in combination with pre-amplifiers [5], [6], [7], [8], [9]. A broad variety of applications for OEICs came up in the last few years. For sensor applications with high-sensitivity, low-noise but low-speed performance integrated photodiode ICs are extensively used since about 15 years for example in infrared receivers, light barriers, opto-couplers and various kinds of light-to-voltage converters. Another important and strongly growing OEIC market is the field of integrated CMOS imaging devices. For high-speed OEICs two different fields of applications came up in the last years. On one hand there is the field of optical data transmission in the visible and near - infrared range like plastic - optical - fibers (POF). This application can be used for data links in automotive and optical home area networks. Another possible application for data transmission are optical interconnects. On the other hand the field of optical data storage like CD and DVD read / write optical - pickup - units came up a few years ago. These applications also need OEICs for future product generations like the so called "Blu-ray" standard and therefore show up as potential high volume market.

In this work theory and development of photodetectors in combination with electronic read - out circuits mainly for optical data storage applications are considered. Therefore only silicon based photodiodes are discussed since most low-cost standard IC technologies are based on "pure" silicon. This also means a restriction of light wavelength to visible range from blue (400 nm) to near infrared ($< 1\,\mu$m). In the next chapter the integration of photodiodes into IC technology is discussed. Necessary photodiode theory is presented before introducing an example for a photodiode integration in a standard low-cost BiCMOS technology. The chapter will be finalized by presenting a high - performance PIN photodiode integration which can be used within high-speed applications. Especially for high - speed applications a proper photodiode model is an essential prerequisite for circuit design of OEIC products. Therefore the 3^{rd} chapter will present the development of a novel photodiode SPICE simulation model. The proposed model includes most significant high - speed behavior like carrier drift and diffusion effects as well as light wavelength dependent sensitivity. On the other hand the photodiode model considers 3-dimensional effects by introducing a network approximation. The remaining chapters will focus on theory and design of high-speed circuits for optical data storage applications. New transimpedance amplifier architectures will be presented combining high - speed and low - noise performance with a variable gain functionality. The thesis will be completed with the presentation of a prototype development for an optical pickup unit OEIC for optical data storage drives.

Chapter 2

Photodiode Integration in IC Technologies

2.1 Introduction

In optoelectronics high - speed applications like optical data transmission via fiber networks and optical pickup units in data storage applications high - speed receiver devices are needed that convert the optical input light signals to electrical output signals. In general a photodiode is a perfect device to do this conversion. Operated in reverse direction (positive voltage on n-doped layer and negative voltage on p-doped layer) it converts the incoming light to a current with an excellent linearity, speed, temperature stability and dynamic range. The only drawback of a photodiode is a rather low gain (ratio of output voltage to input light intensity) that is for example $\leq 0.6\,A/W$ for a silicon photodiode with a light wavelength $\lambda = 0.85\,\mu m$. Therefore a combination of a photodiode with an amplifier is necessary in practical all applications. This amplifier can either be a current amplifier or, mostly used, a transimpedance amplifier (TIA) that converts the photodiode current to an output voltage. For most receiver applications these amplifiers needs a high and also programmable gain, high bandwidth, low noise and very low input impedance.

In the past, for high - end applications discrete photodiodes where connected to transimpedance amplifier IC's in multi-chip packages by wire - bonding or in hybrid integrated circuits [10],[11],[12]. The advantage of this solution is that the performance for each device can be optimized separately by using special photodiode and IC technologies. The drawback are high costs due to a complex production and assembly process. Another disadvantage are potential noise sources due to bondwires and package pins.

As an alternative low - cost solution in the visible spectral range the monolithic integration of photodiodes in standard CMOS and BiCMOS IC technologies became more and more popular during the last 10 to 15 years. The reason is mainly the simple process flow of a standard IC technology without any additional process changes (in best case). Therefore these so called optoelectronics integrated circuits (OEIC) are a competitive solution for many low - cost consumer and sensor applications. Another advantage of an OEIC is the high flexibility in integration of logic and data processing functionality in new deep - sub - μm CMOS technologies. An impressive example is the field of single chip CMOS cameras.

The performance of OEIC photodiodes compared to discrete photodiodes was usually lower in most cases. Especially the integration of high - speed photodiodes was a problem for a long time. Only during the last years the speed performance of integrated photodiodes became comparable to optimized discrete silicon photodiodes. The main challenges in high - speed photodiodes integration will be discussed the next sections.

All different applications for silicon based OEICs are limited to the visible or near-infrared light range up to about 850 nm. The reason for this is a high band - band transition voltage (bandgap) of silicon and will be discussed in Section 2.2.

2.2 Theory of Photodiodes

2.2.1 General

When visible light is falling on a semiconductor material like silicon, one part of the light is reflected while the other part is penetrating into the silicon and is absorbed by the semiconductor. The penetration depth of the light is dependent on the light wavelength. Due to absorption of light energy, electron - hole pairs are generated. A photodiode device separates these carrier pairs in a pn - junction electric field and therefore generates a photocurrent. A photodiode can be operated in two different modes. The first mode is the photovoltaic mode where the device is unbiased connected to a load resistor like in solar cells. The second mode is the 'classical' photodiode mode where the device is connected to a reverse voltage. In this mode it is working like a light - dependent current source. Dependent on configuration different photodiode types are known. The pn - junction diode which is normally no high - performance device but nevertheless used for numbers of low - speed sensor applications. The pin - photodiode which has implemented an intrinsic zone between the p and n - doped region. These diodes are optimized in speed and sensitivity performance. The metal - semiconductor (Schottky) diodes reach high speed values but in general at lower sensitivity performance. The avalanche photodiodes shows an internal current gain as result of impact ionization at high internal electric field. This means a very high sensitivity at low speed values. In this work only the theory and implementation of pn - diodes and pin - diodes will be discussed.

The current Section 2.2 should give an introduction in general photodiode characteristics and theory on light absorption in silicon, quantum efficiency, sensitivity, response speed, and light transmission and reflection on the photodiode surface.

2.2.2 The Interaction of Light with Semiconductors

The physical interaction of an electromagnetic wave with a solid is explained by the Maxwell - Theory and therefore well - known since two centuries. Visible light is an electromagnetic radiation in a small wavelength range of approximately 400 nm to 700 nm (see Figure 2.1). Therefore the interaction of light with semiconductor materials is also defined by Maxwell - Equations [13].

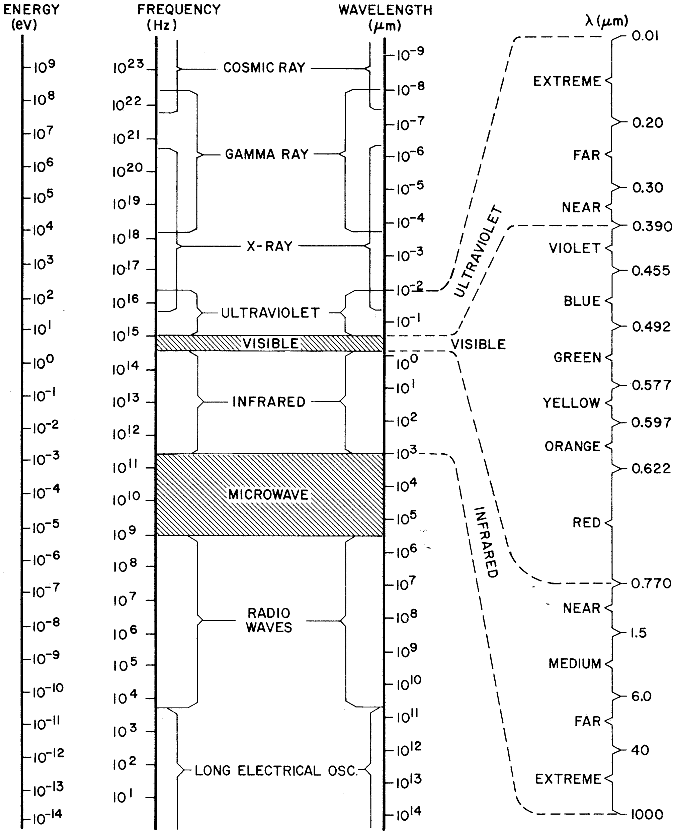


Figure 2.1: Electromagnetic Spectrum

According to quantum mechanics theory, light can be described either as electromagnetic wave with a certain wavelength or as a particle (photon) with a defined energy. The relation between these two representations is given by the Plank Constant h (see Equation 2.1) with E is the photon energy in eV, c_0 is the vacuum light velocity, λ_0 is the vacuum light wavelength in nm and ν is the light frequency in Hz.

$$E = \frac{hc_0}{\lambda_0} = h\nu \approx \frac{1240}{\lambda_0}. \tag{2.1}$$

A typical example for the two "faces" of light is the interaction with a semiconductor material. When light is falling on the surface of a semiconductor, one part of the light is reflected while the other part is absorbed inside the semiconductor. The light reflection and transmission can be explained by Maxwell's wave theory, while the physical light absorption process inside the semiconductor is explained preferably by a particle behavior.

The macroscopic optical behavior of a material is completely given by the complex refractive index N which is

$$N = (n + i\kappa) \tag{2.2}$$

with n is the "classical" optical refractive index and κ is the extinction coefficient which defines the damping of the light wave inside the material. The refractive index n is the ratio of light velocity in vacuum (c_0) and within the material (c)

$$n = \frac{c_0}{c} \tag{2.3}$$

Table (2.1) shows refractive indices of different materials at a defined wavelength.

Material	Refractive Index n	Wavelength
Si	4.18	589 nm
Ge	5.3	547 nm
SiO_2	1.43 ... 1.46	200 nm ... 5 μm
Si_3N_4	2.02	633 nm

Table 2.1: Refractive Indices of different Materials

The optical material parameters n and κ are directly related to the electrical parameters dielectric function $\bar{\epsilon}$ and conductivity σ (see Equation 2.4) and therefore showing the connection between the electromagnetic "wave" theory and the electrical "particle" theory.

$$(n + i\kappa)^2 = \bar{\epsilon} = \epsilon + i\frac{\sigma}{\omega\epsilon_0} \tag{2.4}$$

with ϵ is the material permittivity, $\omega = 2\pi\nu$ is the light frequency and ϵ_0 is the vacuum permittivity.

2.2.3 Light Transmission and Reflection

Integrated photodiodes in IC technologies are preferably realized by using standard layers available in the technology process (see Section (2.3)). In general these layers are not optimized for optical light interactions. Besides the intrinsic photodiode performance, the coupling of light through different oxide and nitride surface layers (used in metallization process) into silicon is a critical performance issue. Two important parameters for IC photodiode development are therefore the light transmission coefficient T and reflection coefficient R of photodiode surface layers which significantly influences the overall photodiode sensitivity. They define the percentage of transmitted and reflected light intensity compared to incident light intensity. Reflections on an integrated photodiode can occur due to different surface layers like silicon oxide (SiO_2) or silicon nitride (Si_3N_4) with different optical parameters (n and κ) compared to silicon.

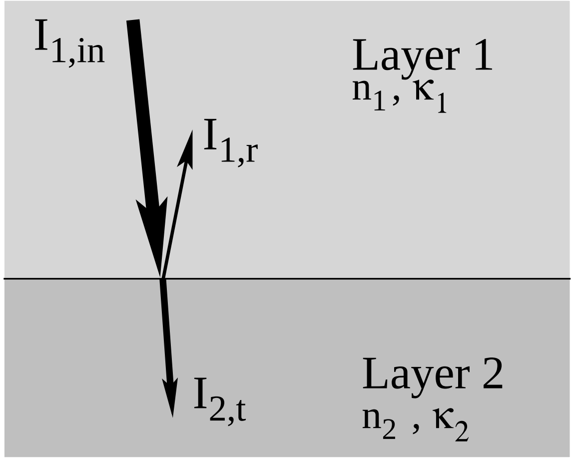


Figure 2.2: Transmission ($I_{2,t}$) and reflection ($I_{1,r}$) of an incident electromagnetic wave ($I_{1,in}$) at the interface of two materials with different optical parameters n and κ

Light transmission and reflection of an electromagnetic wave through a stack of layers with different n and κ are defined by the Fresnel - Coefficients r and t derived from Maxwell's theory [13]. The Fresnel - Coefficients are the ratio of transmitted (t) an reflected (r) electric field $\vec{E}$ at an interface of two materials with different optical constants n and κ. For normal light incidence these parameters only depends on the refractive index N of the two different layers

$$r \equiv \frac{\vec{E}_{1,r}}{\vec{E}_{1,in}} = \frac{N_1 - N_2}{N_1 + N_2} \tag{2.5}$$

$$t \equiv \frac{\vec{E}_{2,t}}{\vec{E}_{1,in}} = 1 - r = \frac{2N_2}{N_1 + N_2} \tag{2.6}$$

where N_1 and N_2 are the refractive indices of layer 1 and layer 2, $\vec{E}_{1,in}$ and $\vec{E}_{1,r}$ are the electric field of incident and reflected wave in layer 1 and $\vec{E}_{2,t}$ is the electric field of transmitted wave in layer 2. For optical transparent layers like oxide and nitride the absorption part κ of N (see Equation 2.2) can be neglected, so that r and t depends on refractive index n only. In practice not the ratio of electric field amplitudes but the ratio of (measurable) light intensities $I \approx |\vec{E}|^2$ is used to define reflection and transmission.

$$R \equiv \frac{I_{1,r}}{I_{1,in}} = \frac{(N_1 - N_2)^2}{(N_1 + N_2)^2} \tag{2.7}$$

$$T \equiv \frac{I_{2,t}}{I_{1,in}} = \frac{(4N_1N_2)}{(N_1 + N_2)^2} \tag{2.8}$$

From Equation 2.7 one can directly derive the reflection R of a simple air - to - material interface with n and κ defined by

$$R = \frac{(1 - n)^2 + \kappa^2}{(1 + n)^2 + \kappa^2} \tag{2.9}$$

The reflection and transmission behavior at integrated CMOS or BiCMOS photodiode surface layers is more difficult to evaluate since there are several layers involved. A typical layer combination for such photodiodes is drawn in Figure 2.3. In almost every IC technology the uppermost layer is silicon nitride (Si_3N_4) for passivation that protects the IC from environmental influences. Below the nitride layer there are different oxide layers (SiO_2) used as inter - metal - oxide to isolate the metal lines. Usually these oxide layers are deposited directly on the silicon surface. New CMOS technologies with Copper metallization have several additional layers distributed in between the oxide layers used as blocking - layers in the metallization process. This makes the optical behavior by far more critical since the variation of transmission T over wavelength becomes significantly higher.

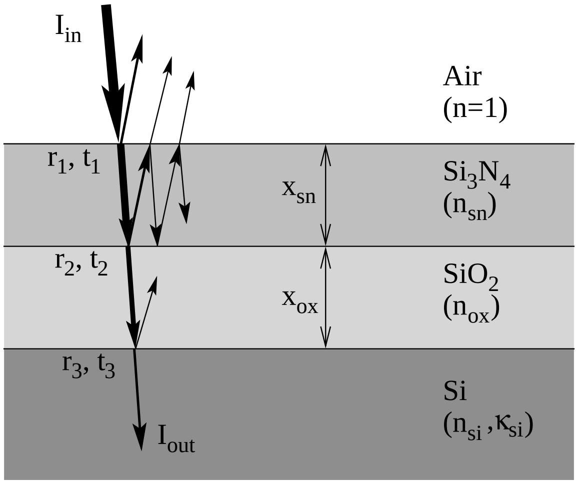


Figure 2.3: Transmission and reflection of an incident electromagnetic wave (I_{in}) at typical CMOS or BiCMOS photodiode Nitride and Oxide surface layers

To calculate the parameters R and T of the layer stack shown in Figure 2.3 at normal incidence, the Fresnel - coefficients for all three interfaces air - Si_3N_4, Si_3N_4 - SiO_2 and SiO_2 - Si must be evaluated. The absorption in Si_3N_4 and SiO_2 can be neglected because $\kappa \approx 0$. Since there is a certain amount of reflection and transmission on every layer interface, the superposition of multiple reflected waves with the incident wave must be considered. The phase shift of a wave entering a layer from topside and reflected back at bottom side interface is given by

$$\delta = \frac{4\pi}{\lambda} n x \tag{2.10}$$

Depending on layer thickness x and refractive index n the superposition of all reflected wave contributions shows minima and maxima at certain wavelengths λ. To calculate the R and T of multiple layer structures, different methods were developed by using matrix algebra mathematics [13]. Applying this mathematics on the layer structure from Figure

2.3 one can achieve the following relation for R and T.

$$r_1 = \frac{1-n_{sn}}{1+_{sn}} \qquad r_2 = \frac{n_{sn}-n_{ox}}{n_{sn}+n_{ox}} \qquad r_2 = \frac{n_{ox}-n_{si}}{n_{ox}+_{si}}$$

$$A_1 = 2\cos\left(\frac{4\pi n_{sn}x_{sn}}{\lambda}\right)$$

$$A_2 = 2\cos\left(\frac{4\pi n_{ox}x_{ox}}{\lambda}\right)$$

$$A_3 = 2\cos\left(\frac{4\pi n_{sn}x_{sn}}{\lambda} - \frac{4\pi n_{ox}x_{ox}}{\lambda}\right)$$

$$A_4 = 2\cos\left(\frac{4\pi n_{sn}x_{sn}}{\lambda} + \frac{4\pi n_{ox}x_{ox}}{\lambda}\right)$$

$$A_5 = \frac{(A_1 r_2(1+r_3^2) + r_3(A_4 + r_2^2 A_3))}{r_2^2 + r_3^2 + r_2 r_3 A_2}$$

$$A_6 = \frac{1 + r_2^2 r_3^2 + r_2 r_3 A_2}{r_2^2 + r_3^2 + r_2 r_3 A_2}$$

$$\boxed{R = \frac{1 + r_1^2 A_6 + r_1 A_5}{A_6 + r_1^2 + r_1 A_5} \qquad T = 1 - R} \tag{2.11}$$

The reflection R and transmission T of the discussed layer stack in Figure 2.3 is given by Equation 2.11. In Figure 2.4 the transmission T of a stack with a nitride thickness $x_{sn} = 550\,nm$ and an oxide thickness $x_{ox} = 1500\,nm$ is shown in dependence on light wavelength λ.

The spectral behavior shows a strong variation of T over λ from very high values of 0.95 (= 95%) down to low values of 0.25 (= 25%). This can be explained by the refractive indices which changes from $n = 1$ for air to a high value of $n_{sn} = 2.5$ for nitride, back to a lower value $n_{ox} = 1.46$ for oxide and again to a high value of $n_{si} = 4.18$ for silicon. To improve the transmission, the refractive indices should increase continuously from one layer to another. So the nitride layer has to be removed from top and instead inserted between oxide and silicon. A risk by doing this is the missing surface passivation. So humidity might permeate into the silicon substrate and change the transistors behavior over lifetime. This effect has to be investigated during photodiode qualification process. The simulation of an improved photodiode surface stack is shown in Figure 2.5. The transmission T over λ is calculated for an air - oxide - nitride - silicon stack with a variation of nitride thickness x_{sn}. The oxide thickness was $x_{ox} = 1500\,nm$. Figure 2.5 shows that the spectral transmission behavior is very sensitive to nitride thickness. It has an optimum

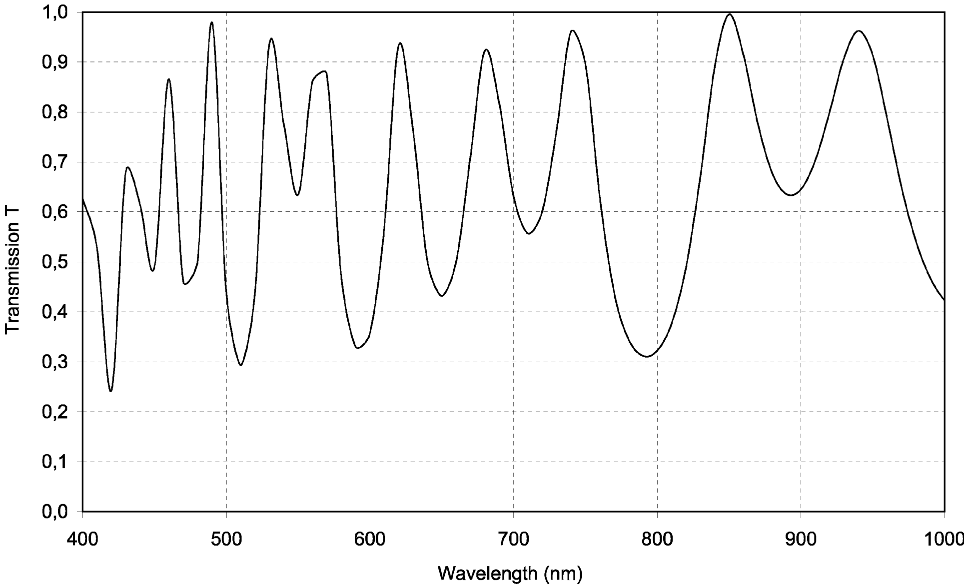


Figure 2.4: Light transmission at a typical CMOS or BiCMOS surface layer stack with nitride and oxide on silicon

with lowest variation for a $x_{sn} = 60\,nm$. Therefore a nitride layer with defined thickness acts as an anti-reflection-coating (ARC) on the photodiode and can dramatically improve the sensitivity performance. The drawback is that additional process steps are necessary resulting in a non-standard IC process flow with higher production costs of approximately 5 %.

2.2.4 Light Absorption and Carrier Generation

An important factor for photodiode sensitivity is the light absorption inside the semiconductor material. The reason for light absorption in semiconductors, is carrier generation due to band-to-band transition. When light (photons) is falling on a semiconductor the electrons in valence band are excited to conduction band by absorption of photon energy defined in Equation (2.1) resulting in a photocurrent. For efficient photocurrent generation the light absorption given by the extinction coefficient κ must be high. Since κ is not easy to measure, a more practical parameter was defined, called absorption coefficient α (see Equation 2.12). It is the penetration depth x of light when an incident light power P_{opt} is decreased to a value of $P(x) = P_{opt}/e$ due to absorption. The absorption coefficient depends on κ and the light wavelength λ.

$$P(x) = P_{opt} exp(-\alpha x) \;\; \text{with} \;\; \alpha = \frac{4\pi\kappa}{\lambda} \tag{2.12}$$

The absorbed photons generates electron-hole pairs inside the semiconductor due to the photo-effect proportional to the photon flux $\phi(x)$ given by Equation (2.13). The carrier

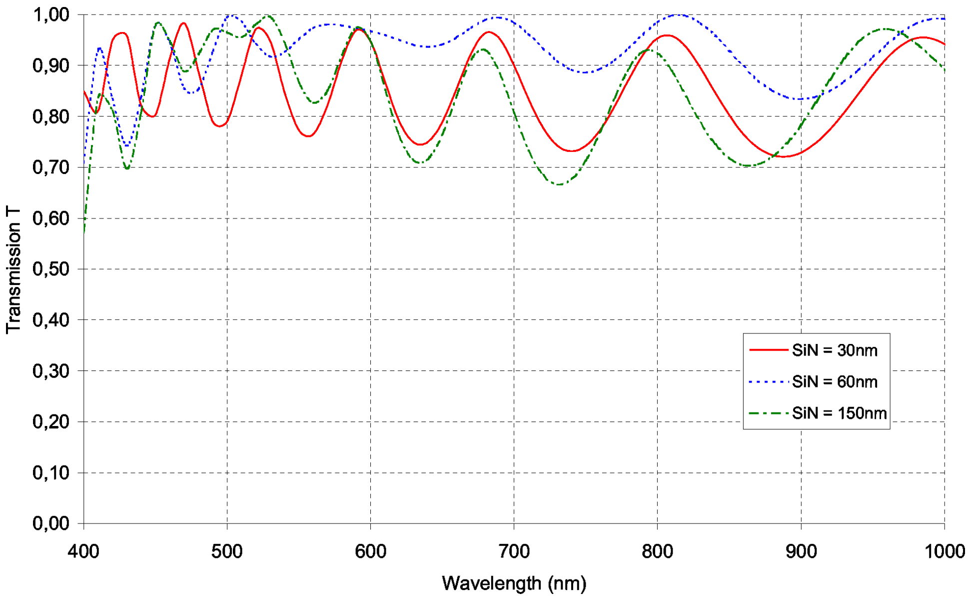


Figure 2.5: Light transmission at an optimized surface layer stack with oxide on a defined nitride layer on silicon

generation rate is defined in Equation (2.14)

$$\phi(x) = \frac{P_{opt}T}{h\nu}(1-\exp(-\alpha x)) \tag{2.13}$$

$$G(x) = \frac{1}{A}\frac{\partial\phi(x)}{\partial x} = \frac{\alpha P_{opt}T}{Ah\nu}\exp(-\alpha x) \tag{2.14}$$

with T is the light transmission into the silicon, discussed in previous section.

Figure 2.6 shows the measured absorption coefficients of various semiconductor materials used for photodiode and laser production at two different temperatures [14]. Out of Figure 2.6 one can see, that α strongly depends on light wavelength. It decreases dramatically for higher wavelengths or lower photon energy. This means that light is penetrating very deep into the silicon substrate. For high absorption the photons energy must be larger than the energy gap between valence and conduction band also called bandgap energy E_g. This is the reason why silicon photodiodes shows a significant absorption (and therefore sensitivity) only for light wavelengths below about 1.1 μm. If on the other hand the wavelength is to low (which means a low penetration depth) the light is absorbed near the surface were the carrier recombination due to surface defects is high. This also reduces the photodiode sensitivity. In Figure 2.7 the absorption of light for different wavelengths is shown. For red light with 650 nm the penetration depth is about 5 μm while light with 780 nm wavelength is penetrating into a depth of about 15 μm.

An analytic model of the absorption coefficient at room temperature, including wavelength dependence, is presented in [15]. This equation is a sufficient approximation for

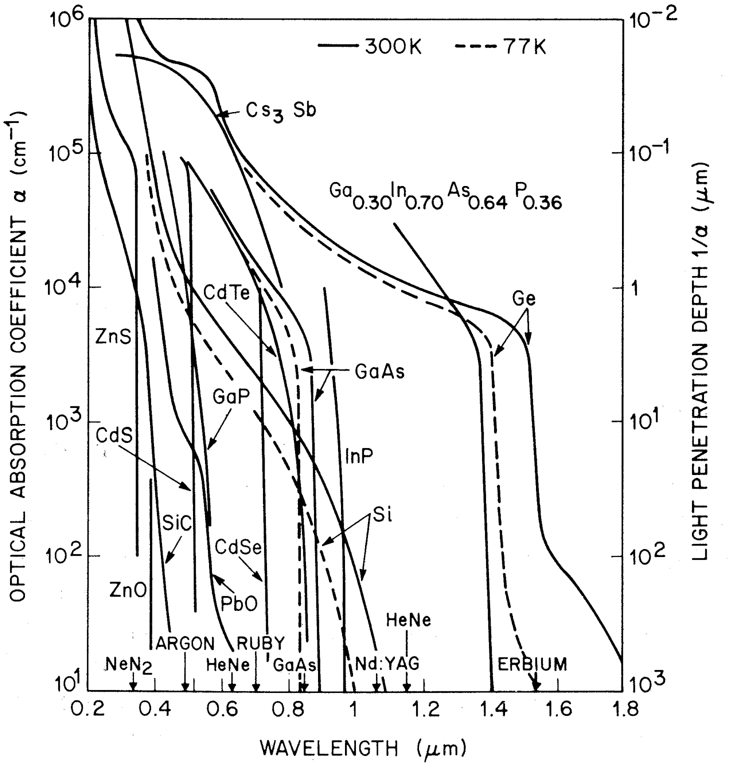


Figure 2.6: Optical absorption coefficients of different semiconductor materials at two temperatures; at bottom scale different laser emission wavelength are indicated [14]

wavelengths of $0.4\mu m < \lambda < 1\mu m$.

$$\alpha(\lambda) = \left(\frac{84.732 \cdot 10^{-6}}{\lambda[m]} - 76.417\right)^2 \cdot 10^2 \left[\frac{1}{m}\right] \tag{2.15}$$

This analytic representation of the absorption coefficient will be used for the photodiode SPICE model, presented in Section (3.2).

2.2.5 Photodiode Quantum Efficiency

The intrinsic photodiode sensitivity is defined by the quantum efficiency η which is the number of electron - hole pairs generated per an incident photon. One part of the quantum efficiency is the light reduction due to optical transmission (T) and reflection (R) on the photodiode surface as discussed in previous section.

$$\eta = \frac{\frac{I_p}{q}}{\frac{P_{opt}(1-R)}{h\nu}} \tag{2.16}$$

where I_p is the photo - generated current, P_{opt} is the incident optical light power, q (=e) is the electron charge and $h\nu$ is the energy of a photon (see Equation 2.1). A more practical

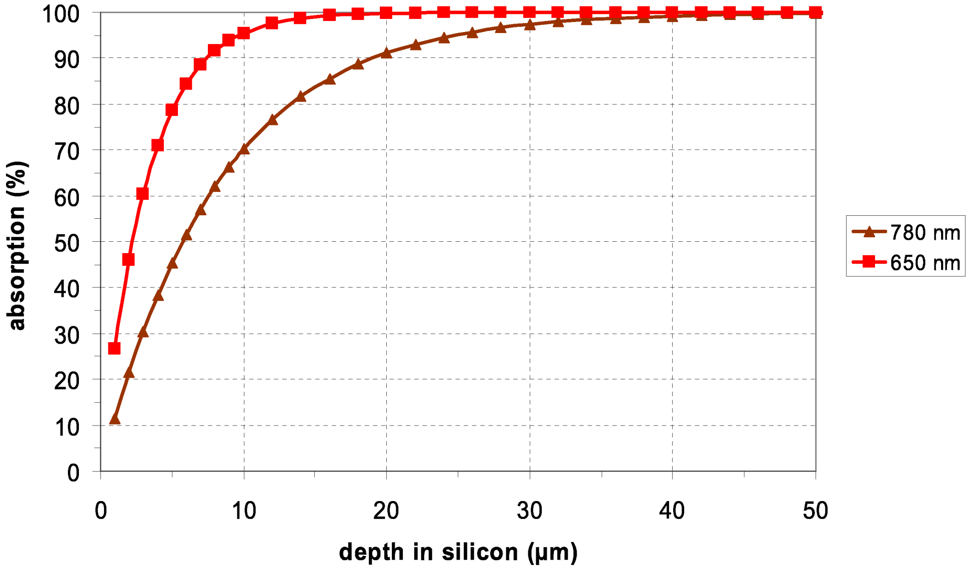


Figure 2.7: Penetration depth of light in silicon for different wavelength

relevant figure of merit for the photodiode sensitivity is the responsivity R_s. This is the ratio of photocurrent per incident optical light power and therefore it can easily be measured.

$$R_s = \frac{I_p}{P_{opt}} = \frac{\eta q}{h\nu} = \frac{\eta\lambda}{1.234} \;\; [A/W] \tag{2.17}$$

The reflection R is included in the η and λ is the wavelength in μm. According to Equation 2.17 the theoretical maximum responsivity increases linearly with the light wavelength λ. The maximum R_s for a photodiode with 660 nm light is $R_{s,660nm} = 0.53\,A/W$ whereas the R_s decreases for blue light of 410 nm to $R_{s,410nm} = 0.33\,A/W$. Especially for higher wavelengths the linear behavior for R_s is not valid as it will be shown in the following sections.

2.2.6 Static and Dynamic Behavior of Carriers in Semiconductors

The carrier transport in semiconductors is mainly given by two basic mechanisms, carrier drift and carrier diffusion. In addition the static and dynamic behavior of carriers under the influence of external fields is described by the Maxwell - Equations [16]. Out of these equations one can derive the current - density equations and the continuity - equations that defines the carrier transport inside semiconductor materials and in pn - junction depletion layers.

2.2.6.1 Carrier Drift and Mobility

Carrier drift occurs when an electric field is present inside the semiconductor, especially in a space-charge-region (SCR) of a pn-junction. For low electric fields the drift velocity of electrons ($\vec{v_n}$) and holes ($\vec{v_p}$) is proportional to the electric field strength (see Equation 2.18). The proportionality factor $\mu_{n,p}$ is called mobility.

$$\vec{v_{n,p}} = \mu_{n,p}\vec{E} \tag{2.18}$$

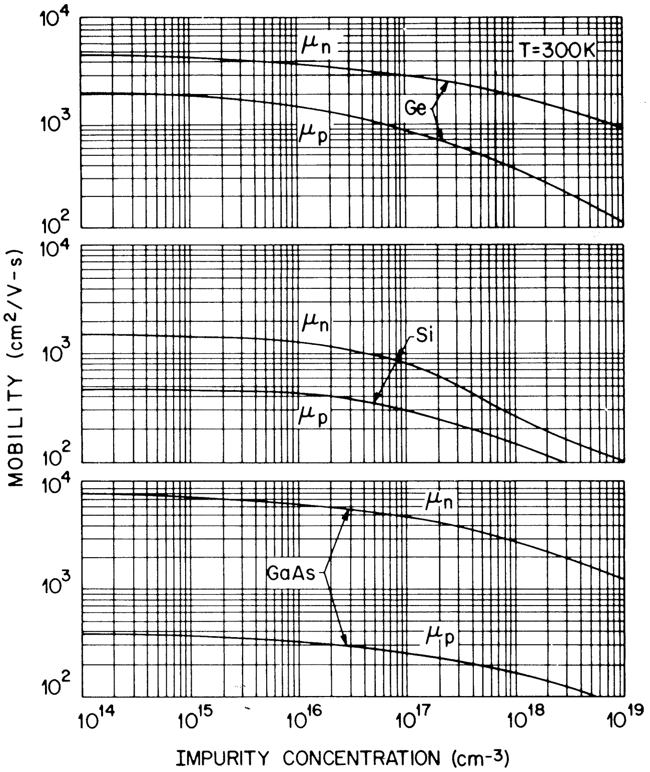


Figure 2.8: Mobility of n and p carriers in Ge, Si and GaAs at 300 K versus doping conentration

The mobility of Si, Ge and GaAs for different doping concentrations at a temperature of 300 K is shown in Figure (2.8). The mobility is decreasing for high carrier concentration. Also for strong electric fields the mobility and therefore also drift velocity is saturating as shown in Figure (2.9) [14, 17]. According to [18, 19] the dependence of carrier mobility on electric field in silicon can be approximated by

$$\mu_n(\vec{E}) = \frac{\mu_{0n}}{1 + (\mu_{0n}\vec{E}/\vec{v}_n^{sat})^2} \tag{2.19}$$

$$\mu_p(\vec{E}) = \frac{\mu_{0p}}{1 + (\mu_{0p}\vec{E}/\vec{v}_p^{sat})^2} \tag{2.20}$$

where $\vec{v}_{n,p}^{sat}$ is the saturation velocity for electrons (n) and holes (p) and is approximately $1.03 \cdot 10^5\,m/s$ for a temperature $T = 300\,K$. The $\mu_{0n,p}$ is the carrier mobility at zero electric field and is shown in Figure (2.8).

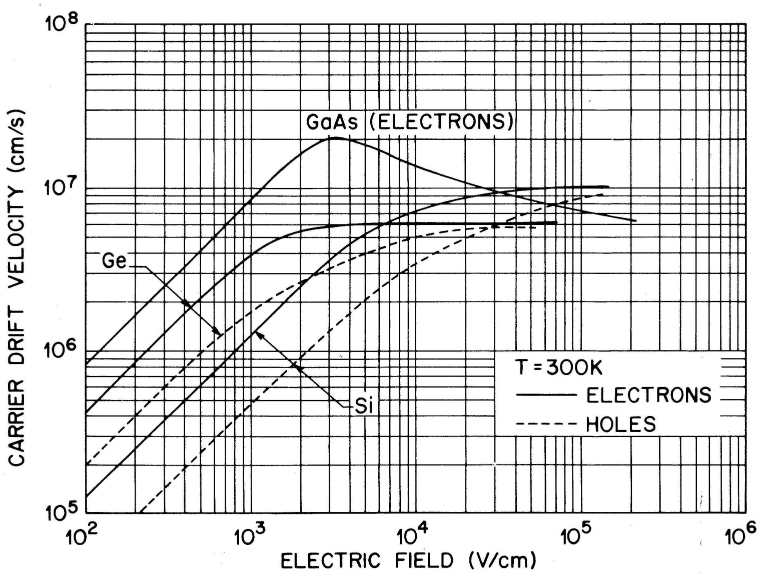


Figure 2.9: Carrier velocity versus electric field for Ge, Si, GaAs

2.2.6.2 Carrier Diffusion

Carrier diffusion in semiconductors occurs in quasi - neutral regions without electric field. Therefore the carrier velocity is much lower compared to carrier drift. To achieve high speed photodiodes, diffusion carriers should be avoided as much as possible, since they contribute to the photocurrent as slow component. An important parameter for carrier diffusion is the diffusion coefficient D_n, D_p (with n for electrons and p for holes). These coefficients are related to the diffusion coefficients μ_n, μ_p by the Einstein relation

$$D_{n,p} = \frac{kT}{q}\mu_{n,p} \tag{2.21}$$

with $kT/q = 0.0259V$ at 300K. The mobilities $\mu_{n,p}$ are also a measure for the electrical conductivity σ which is the reciprocal resistivity ρ and therefore a relation between current density $\vec{j}_{n,p}$ and electrical field $\vec{E}_{n,p}$.

$$\vec{J}_{n,p} = \sigma_{n,p}\vec{E}_{n,p} = \frac{1}{\rho_{n,p}}\vec{E}_{n,p} \tag{2.22}$$

$$\sigma_n = q\mu_n n \quad \sigma_p = q\mu_p p \tag{2.23}$$

with n is the electron concentration in a n-type semiconductor and p is the hole concentration in a p-type semiconductor. The resistivity in dependence on the doping concentration of n and p type silicon is shown in Figure (2.10).

2.2.6.3 Current - Density Equations

The current density J_n and J_p of electrons and holes in silicon for a one - dimensional case are given by Equations 2.24 and 2.25 respectively. These currents consists of two

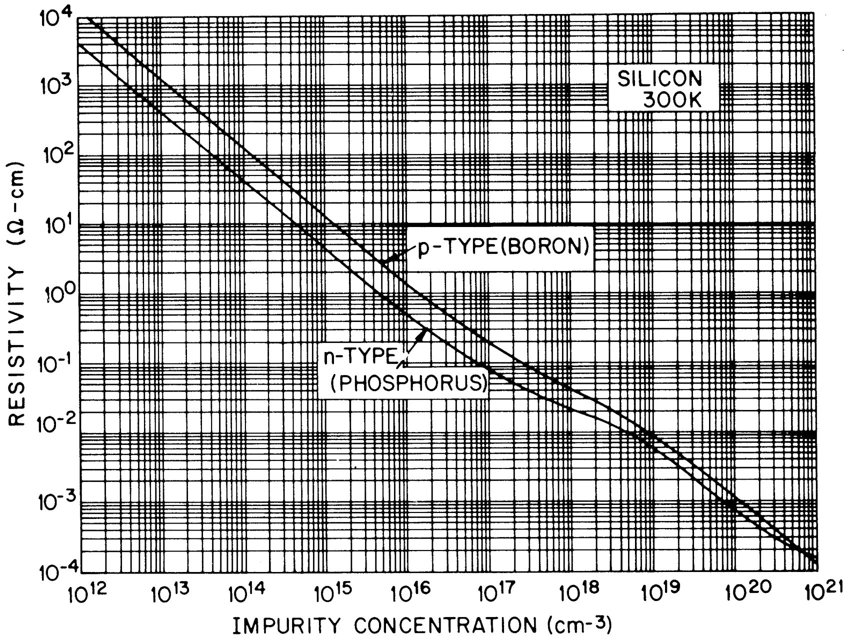


Figure 2.10: Resistivity of p and n - doped silicon depending on doping concentration

components. A drift component for carriers generated inside an electric field $\vec{E}$ according to Equation 2.22 and a diffusion component caused by a carrier doping concentration gradient $\partial n, p/\partial x$.

$$J_n = q\mu_n nE + qD_n\frac{\partial n}{\partial x} \tag{2.24}$$

$$J_p = q\mu_p pE + qD_p\frac{\partial p}{\partial x} \tag{2.25}$$

where μ_n and μ_p are the electron and hole mobility (see Figure 2.8). D_n, D_p are the carrier diffusion coefficient (Equation 2.21). The total current density is therefore given by

$$J = J_n + J_p \tag{2.26}$$

2.2.6.4 Continuity Equations

To describe the dynamic behavior of drift and diffusion carriers in equilibrium, the continuity equations have to be solved (for simplicity only one dimension x is considered):

$$\frac{\partial n_p}{\partial t} = G_n(t) - \frac{n_p - n_{po}}{\tau_n} + \mu_n n_p\frac{\partial E}{\partial x} + \mu_n E\frac{\partial n_p}{\partial x} + D_n\frac{\partial^2 n_p}{\partial x^2} \tag{2.27}$$

$$\frac{\partial p_n}{\partial t} = G_p(t) - \frac{p_n - p_{no}}{\tau_p} + \mu_p p_n\frac{\partial E}{\partial x} + \mu_p E\frac{\partial p_n}{\partial x} + D_p\frac{\partial^2 p_n}{\partial x^2} \tag{2.28}$$

where n_p and p_n is the minority carrier density of electrons n in p - silicon and holes p in n - silicon, n_{po} and p_{no} is the thermal equilibrium minority carrier density and E is the electrical field. G_n and G_p is the electron and hole generation rate (cm^{-3}/s) due to incident light, defined in Equation (2.14) and τ_n and τ_p are the electron and hole minority carrier lifetime in the p- and n-doped region. For further simplification, the continuity equations should only be solved in field-free region ($E \approx 0$) outside the SCR. This simplifies the Equations to

$$\frac{\partial n_p}{\partial t} = G_n(t) - \frac{n_p - n_{po}}{\tau_n} + D_n \frac{\partial^2 n_p}{\partial x^2} \tag{2.29}$$

$$\frac{\partial p_n}{\partial t} = G_p(t) - \frac{p_n - p_{no}}{\tau_p} + D_p \frac{\partial^2 p_n}{\partial x^2} \tag{2.30}$$

The solution of these differential equations including time dependent carrier generation is not straight forward. They can be solved analytically mainly with neglecting carrier generation $G_n(t), G_p(t)$ or with a simple and well-defined generation functions like step-response or impulse response [20, 21].

In following section the solution of the steady-state continuity equations will be presented. In Chapter 3 a method for solving the time dependent continuity equations for arbitrary functions of $G_n(t), G_p(t)$ by introducing a SPICE circuit model will be presented.

2.2.6.5 Solution of Steady-State Continuity Equations

In Figure (2.11) a simplified cross-section of a silicon photodiode is shown, which is a pn-junction with a space-charge-region (SCR). Light is penetrating into the silicon bulk and generates carrier pairs which are drifting or diffusing to the photodiode contacts. With a reverse voltage connected to the p and n-doped region, a significant electrical field, and therefore carrier drift, is only present inside the SCR. The regions outside the SCR are mainly field-free and so only slow minority carrier diffusion occurs. Since photodiode speed is limited by these diffusion effects, an analysis is essential for the development of high-speed photodiodes. As shown before, the diffusion current in the field-free region can be evaluated by solving the differential continuity equations (2.29) and (2.30). For sake of simplicity the solution of idealized equations neglecting the time-dependence will be presented [22, 23]. Also parasitic effects like surface recombination due to charge traps are neglected. These results will be used for a photodiode model including all time dependent effects with arbitrary carrier generation (shown in Chapter (3).

Equation (2.31) and (2.32) shows the simplified steady-state continuity equations for electrons in the p-region and for holes in the n-region respectively.

$$D_n \frac{\partial^2 n_p}{\partial x^2} - \frac{n_p - n_{po}}{\tau_n} + G_n = 0 \tag{2.31}$$

$$D_p \frac{\partial^2 p_n}{\partial x^2} - \frac{p_n - p_{no}}{\tau_p} + G_p = 0 \tag{2.32}$$

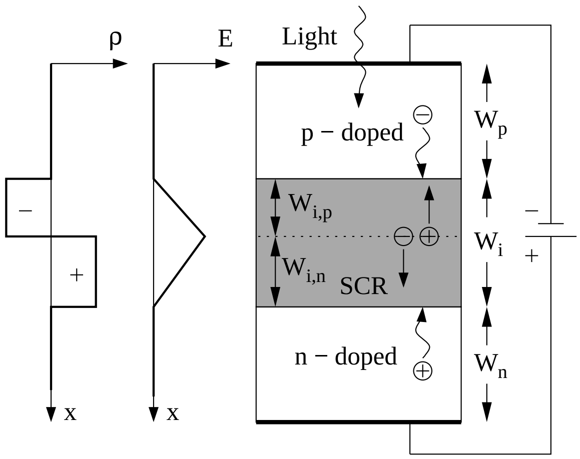


Figure 2.11: Cross-section of a silicon photodiode with a n-doped region, a p-doped region and a Space-Charge-region in between. The idealized electric field E accross the photodiode and the space charge density ρ is indicated in the diagram.

where the electron-hole diffusion coefficient $D_{n,p} = L^2_{n,p}/\tau_{n,p}$ with $L_{n,p}$ is the electron and hole diffusion length. The equilibrium electron and hole density n_{po} and p_{no} is defined by $n_{po} = n_i^2/N_D$ and $p_{no} = n_i^2/N_A$ with N_D is the donor density in the n-region and N_A is the acceptor density in the p-region respectively. According to Equation (2.14) the carrier generation rate for electrons in the p-region G_n and holes in the n-region G_p is given by

$$G_n(x) = \frac{\alpha_p P_{opt} T}{Ah\nu} \exp\left(-\alpha_p x\right) \tag{2.33}$$

$$G_p(x) = \frac{\alpha_n P_{opt} T \exp\left(-\alpha_p W_p - \alpha_i W_i\right)}{Ah\nu} \exp\left(-\alpha_n x\right) \tag{2.34}$$

with α_n is the absorption coefficient of n-doped layer with W_n is the layer width, α_p of p-doped region with width W_p and α_i of the intrinsic region with width W_i.

Solution for p-region The solution of Equation (2.31) for $n_p(x)$ in the p-region under the bounding conditions

$$\begin{array}{ll} x = 0: & n_p = n_p(0) \\ x = W_p: & n_p = 0 \end{array} \tag{2.35}$$

can be calculated as

$$n_p(x) = n_{po} + C_1 \exp(-\alpha_p x) + \cdots \tag{2.36}$$

$$+ \frac{\left[n_p(0) - n_{po} - C_1\right] \sinh \frac{W_p - x}{L_n} - \left[n_{po} + C_1 \exp(-\alpha_p W_p)\right] \sinh \frac{x}{L_n}}{\sinh \frac{W_p}{L_n}}$$

$$C_1 = \frac{P_{in} T \alpha_p L_n^2}{A h\nu D_n (1 - \alpha_p^2 L_n^2)} \tag{2.37}$$

The total number of excess electrons N_p in the p-doped region is therefore

$$N_p = A \int_0^{W_p} (n_p(x) - n_{po})\, dx \tag{2.38}$$

To eliminate the $n_p(0)$, Equation (2.36) is substituted in Equation (2.38). Solving for $n_p(0)$ and substituting in Equation (2.36), the total electron diffusion current is according to Equation (2.24)

$$I_n = -qAD_n \left.\frac{\partial n_p}{\partial x}\right|_{x=W_p} \tag{2.39}$$

.

Solution for n-region For holes in the n-region the solution of Equation (2.32) for $p_n(x)$ is very similar. Under the bounding conditions

$$\begin{aligned} x = 0 :& \quad p_n = 0 \\ x = W_n :& \quad p_n = p_n(0) \end{aligned} \tag{2.40}$$

the solution can be calculated as

$$\begin{aligned} p_n(x) &= p_{no} + C_2 \exp(-\alpha_n x) + \cdots \\ &+ \frac{[p_n(0) - p_{no} - C_2 \exp(-\alpha_n W_n)] \sinh \frac{x}{L_p} - (C_2 + p_{no}) \sinh \frac{W_n - x}{L_p}}{\sinh \frac{W_n}{L_p}} \end{aligned} \tag{2.41}$$

$$C_2 = \frac{P_{in} T \exp(-\alpha_p W_p - \alpha_i W_i) \alpha_n L_p^2}{A h\nu D_p (1 - \alpha_n^2 L_p^2)} \tag{2.42}$$

The total number of excess holes P_n in the n-doped region is

$$P_n = A \int_0^{W_n} (p_n(x) - p_{no})\, dx \tag{2.43}$$

To eliminate the $p_n(0)$, Equation (2.41) is substituted in Equation (2.43). Solving for $p_n(0)$ and substituting in Equation (2.41), the total holes diffusion current is according to Equation (2.25)

$$I_p = -qAD_p \left.\frac{\partial p_n}{\partial x}\right|_{x=0} \tag{2.44}$$

.

The equations for the electron and hole diffusion currents I_n and I_p will be used for a photodiode SPICE model in Chapter (3).

2.2.7 Photodiode Capacitance

An important parameter for the development of high-speed photodiodes is the pn-junction capacitance. To achieve fast photodiode currents, the capacitance must be as small as possible. The reason is a non-zero input impedance of the transimpedance amplifier or current amplifier connected to the photodiode (see Chapter 4). For a reverse biased photodiode, the capacitance is mainly defined by the depletion capacitance of the pn-junction [14]. In the depletion region or space-charge-region (SCR) the minority carrier density is very low and the electrical field is high because of charges due to ionized impurity atoms. The electrical field outside the SCR can be neglected. Therefore the pn-junction can be seen as a capacitor with parallel plates in a distance of the depletion layer width.

$$C_{pn} = \epsilon_0 \epsilon_r \frac{A}{W_i} \tag{2.45}$$

with A is the pn-junction area and W_i is the SCR width. According to Figure (2.11), the SCR width W_i (sum of $W_{i,p}$ and $W_{i,n}$) of an abrupt pn-junction can be calculated as

$$W_{i,p} = \sqrt{\frac{2\epsilon_0\epsilon_r(\phi_i + V_{pn})}{qN_A\left(1+\frac{N_A}{N_D}\right)}} \tag{2.46}$$

$$W_{i,n} = \sqrt{\frac{2\epsilon_0\epsilon_r(\phi_i + V_{pn})}{qN_D\left(1+\frac{N_D}{N_A}\right)}} \tag{2.47}$$

$$W_i = \sqrt{\frac{2\epsilon_0\epsilon_r}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(\phi_i + V_{pn})} \tag{2.48}$$

$$\text{with} \qquad \phi_i = V_T ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{2.49}$$

with N_A is the acceptor density in p-doped region and N_D is the donor density in the n-doped region, ϕ_i is the diffusion voltage (typical 0.8 V for silicon), ϵ_0 is the vacuum permitivity, ϵ_r is the relative permitivity(11.9 for silicon) and V_{pn} is the junction reverse voltage in positive values, V_T is the thermal voltage ($V_T = kT/q \approx 26mV$ at T=300K) and n_i is the intrinsic carrier density ($1.4 \times 10^{-10} cm^{-3}$).

In Figure (2.12) the SCR width of a pn-junction is shown in dependence on the reverse voltage for different doping concentration N_d of the n-doped region. The p-region is highly doped, so the SCR in the p-region can be neglected which is the case for a typical integrated photodiode in an IC technology (see Section 2.3).

According to Equation (2.45), the pn-junction capacitance is shown in Figure (2.13) in dependence on the reverse voltage for different resistivities of the n-doped silicon. Since the resistivity is indirect proportional to the doping concentration, the junction capacitance is decreasing with increasing resistivity.

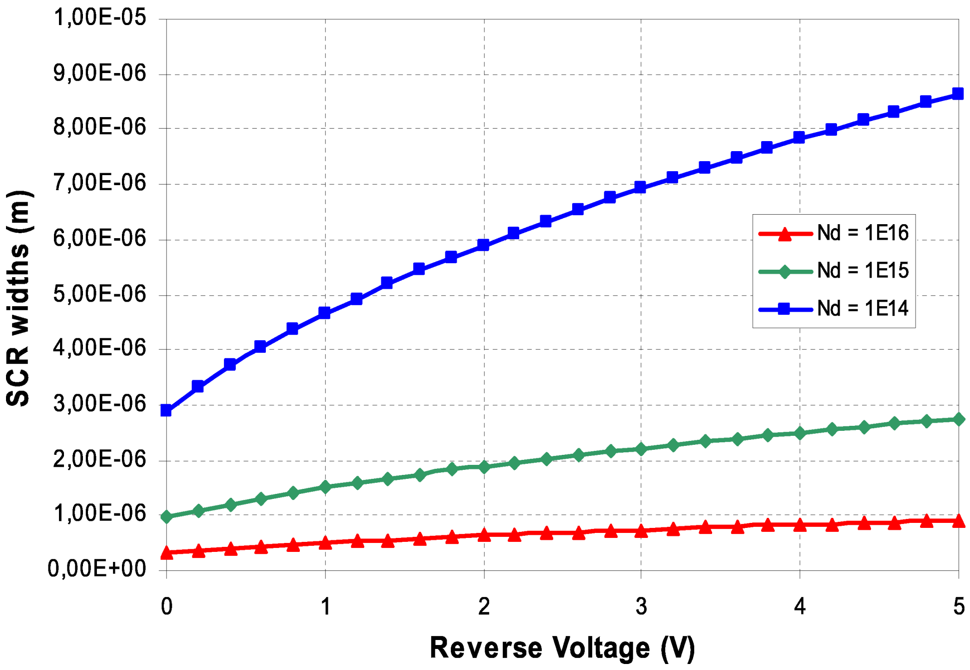


Figure 2.12: Width of a Space - Charge - Region (SCR) in dependence on the pn-junction reverse voltage for different doping conctrations N_d of the n-region. The p-region doping concentration is significantly higher.

2.3 Integration of Photodiodes in Standard BiCMOS Technologies

2.3.1 Introduction

The integration of photodiodes in IC technologies is nowadays an extensively used method to realize optical sensors including analog signal processing mainly for low cost applications. In IC technologies there are several layers with different doping concentration available like the drain/source and bulk of MOS transistors, or the buried collector layer and the base layer of BIP transistors. All these layers can be combined for photodiode realization. Mainly two different technology options are available for IC products. On one hand the pure CMOS technology, which is the cheapest IC technology. Another popular option is the BiCMOS technology which combines CMOS transistors with bipolar transistors. This option provides a higher flexibility for photodiodes and also for the analog circuit design. The drawback is higher costs of about 10% to 15% for the BiCMOS technology compared to a pure CMOS with the same technology feature size. For applications in the field of optical data storage, we decided to use an IFX 0.5 μm BiCMOS technology called B6CA. The reason is, that the product specification requests for high speed with low power consumption and a strong output driver strength (as shown in Section 5). Together with higher flexibility in the photodiode design, the BiCMOS technology shows

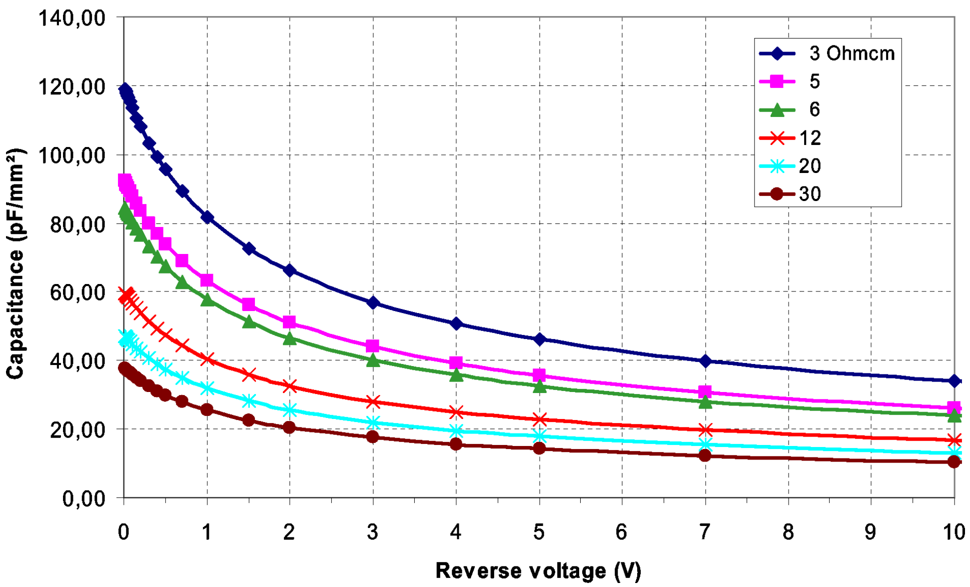


Figure 2.13: Capacitance of a Space - Charge - Region (SCR) in dependence on the pn-junction reverse voltage for different resistivities of n-silicon.

several advantages due to the BIP transistor performance.

In this section we will present the photodiode integration in standard B6CA BiCMOS technology without any process modification. We will show the technology implementation of a so called double photodiode (DPD) structure which combines a reasonable speed performance for 660 nm as well as for 780 nm, with a reasonable high responsivity, even for large photodiode areas [24]. Measurement results will be shown, which indicates the performance limits for this kind of low cost photodiodes.

2.3.2 Photodiode Implementation

A photodiode can be implemented as a p-n-junction with applied reverse voltage. As discussed in Section 2.2, incident light penetrates into photodiode silicon and generates electron-hole pairs. The penetration depth of light in silicon strongly depends on the light wavelength. For 650 nm light 90% is absorbed in a silicon depth of about 7 μm. For 780 nm light (as used in CD applications) the penetration depth increases to about 20 μm (see Figure 2.7). To optimize the photodiode sensitivity, most of generated carriers inside the absorption region have to be collected as photodiode current. Depending on local electrical field the carriers are diffusing or drifting to the photodiode p-n-junction and contribute to the photo current. To realize a high photodiode speed only carrier drift in an electric field is allowed because diffusion carriers are much slower and therefore they decrease photodiode speed. Since only inside the p-n-junctions space-charge-region (SCR) there is significant electrical field, the photodiode SCR must be as wide as possible.

Preferably as wide as the light penetration depth. A wide SCR also reduces the photodiode junction capacitance which is necessary for high-speed OEIC circuits (Figure (2.13)). A low photodiode junction capacitance is also beneficial for a low noise level (conversion of voltage noise via the photodiode capacitance to current noise). The SCR width W of a p-n-junction is defined by Equation (2.48). To achieve a wide SCR the reverse voltage $-V_{pn}$ can be increased or the silicon doping concentrations N_A, N_D can be decreased. Figure 2.12 shows the SCR width in dependence on reverse voltage $-V_{pn}$ for different doping concentrations.

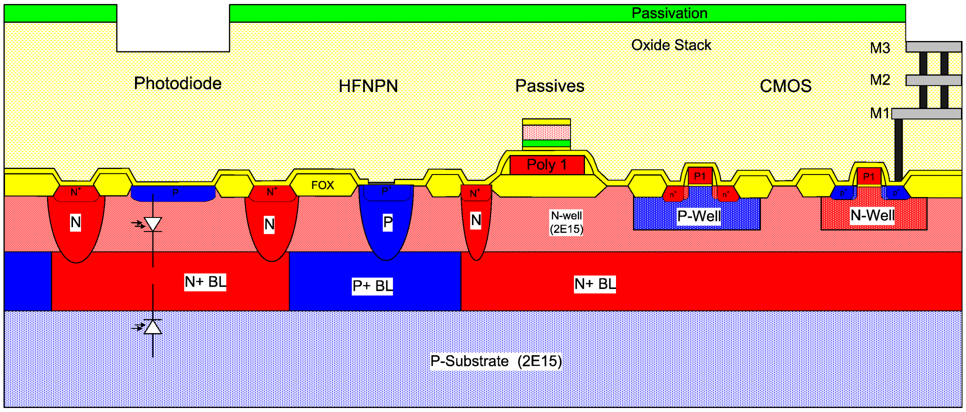


Figure 2.14: Cross-section of a silicon photodiode with a n-doped region, a p-doped region and a Space-Charge-region in between. The idealized electric field E accross the photodiode and the space charge density ρ is indicated in the diagram.

The cross section of the proposed DPD photodiode is shown in Figure (2.13). On left-hand side the photodiode area is shown. The circuit region including CMOS transistors and passive devices (BIP transistors are not shown) can be seen on the right-hand side. We implemented the DPD with a stack of p^+-S/D layer / n-epi layer / n^+-buried layer / p-substrate. Therefore two pn-junctions were formed named "upper" photodiode (UPD) and "lower" photodiode (LPD). The UPD is situated between the flat an highly doped p^+-S/D layer ($N_A \approx 10^{20} cm^{-3}$) as anode and the quite low doped n-epitaxial layer ($N_D \approx 10^{15} cm^{-3}$) as cathode, which acts as intrinsic zone. To avoid a large RC time constant, the high ohmic n-epi layer is connected by a low ohmic n^+-buried layer ($N_D \approx 10^{20} cm^{-3}$). The space charge region is taking up the whole n-epi layer, causing a high electric field inside, which means high carrier drift velocity. Figure (2.15) shows the simulated distribution of the electric field in a B6CA double photodiode structure. We clearly see the two peaks of the electric field in the SCR of the UPD and LPD. Due to its high doping concentration, the n^+-buried layer has no space charge region inside. Only a small electric field is build up at the edges of the n^+-buried layer, due to a gradient in the doping concentration. The electric field in the center is vanishing. Nevertheless, the high doping concentration in the p^+-S/D layer and the n^+-buried layer reduces the carrier diffusion length to below 0.3 μm. Figure (2.16) shows a calculation of the carrier diffusion length in a n-doped silicon semiconductor. So the low electric field in the p^+-S/D layer and in the center of the n^+-buried layer in depths of 0 - 0.3 μm and 3 - 4 μm, respectively, (see Figure (2.15)) does not cause a strong diffusion part in the resulting photodiode current. Both simulations of the electric field and of the carrier diffusion length were performed with the device simulator MEDICI [25].

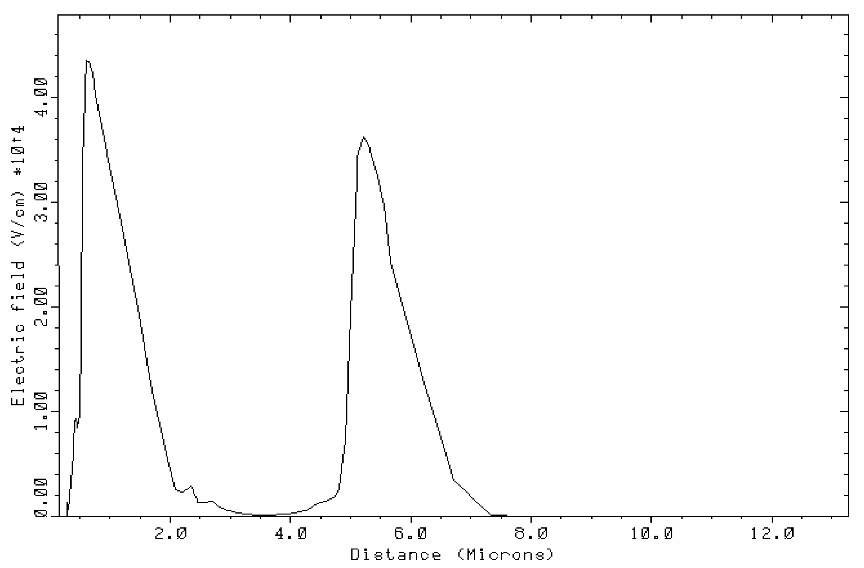


Figure 2.15: Distribution of the electric field (absolute values) in the DPD for a reverse bias voltage of 3V (reference for the distance is the silicon surface).

The second, "lower" photodiode (LPD) consists of the low ohmic n^+-buried layer as cathode and the high ohmic p-substrate ($N_A \approx 10^{15} cm^{-3}$) as anode. The space charge region appears in the p-substrate only, causing a high electric field in a depth of 4.7 - 7 μm. The LPD is more sensitive for 780 nm, because a higher percentage of carriers is generated in the substrate due to the large penetration depth of 780 nm light (see Table (2.2)). Nevertheless the carrier diffusion part in the photodiode current is not very strong, because the space-charge region of the substrate is extending to a depth of about 7.5 μm. The capacitance of the photodiodes is also low, due to the wide space-charge regions (C_{UPD}=0.16 pF, C_{LPD}=0.12 pF for $50 \times 50 \mu m^2$ photodiodes with a reverse voltage of 3 V).

2.3.3 Photodiode Characterization

For the characterization photodiode test-chips were die bonded directly on a PCB. To avoid a bandwidth limitation due to the RC-time constants of the measurement setup in

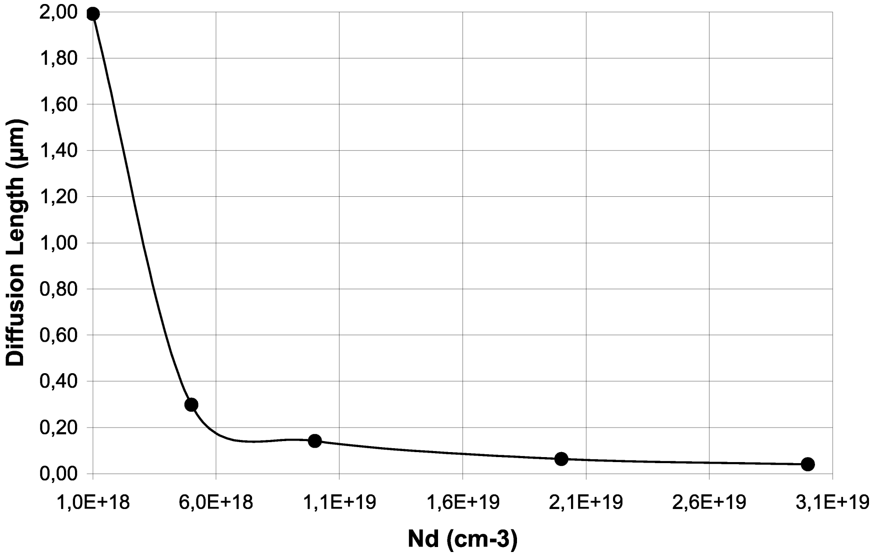


Figure 2.16: Minority carrier diffusion length in n-doped silicon in dependence on the doping concentration

combination with the photodiode capacitance, we integrated a SMD resistor of 50 Ω on the PCB board near to the photodiode. The PCB strip lines were matched to 50 Ω, to minimize wave reflection losses. As light source we used laser diodes with a wavelength of 660 nm and 780 nm. The light was coupled into the $50 \times 50\,\mu m^2$ photodiodes with a single mode optical fiber. The RF-signal of a pulse generator Agilent 81130A was coupled into the laser diode through a bias-tee network with a bandwidth of 1 GHz. The transient response of the photodiodes was measured with a digital sampling scope Tektronix TDS7054 on the 50 Ω input. The measurements of the photodiode small signal bandwidth were performed with a network analyzer Rohde&Schwarz FSEA30 modulating the laser light and measuring the AC output signal. For the transient measurements and small signal bandwidth measurements, the photodiode reverse voltage was 3 V. The photodiode responsivity measurements were performed on $200 \times 200\,\mu m^2$ photodiodes with the wavelengths of 660 nm and 780 nm to ensure, that the total laser light of the optical fiber is focused on the photodiodes. A reference measurement was performed on the Coherent LabMaster Ultima light power meter.

2.3.3.1 Photodiode Responsivity

The measured photodiode responsivity of the two photodiodes UPD and LPD for 660 nm and 780 nm can be seen in Table (2.2). In a practical application the two photodiodes can be used in parallel, with a high responsivity of 0.4 A/W for 660 nm and 0.5 A/W for 780 nm. For high speed applications, only the UPD might be used with an acceptable high responsivity of 0.23 and 0.14 A/W for 660 nm and 780 nm.

Wavelength (nm)	Responsivity (A/W) UPD	Responsivity (A/W) LPD
660	0.23	0.17
780	0.14	0.36

Table 2.2: B6CA photodiode responsivity at 660 nm and 780 nm.

2.3.3.2 Transient and AC Behavior for 660 nm

Figure (2.17) shows on upper graph the transient behavior of the photodiodes UPD and LPD at a wavelength of 660 nm. The rise time and fall time of the UPD was found to be 1.3 ns. For the LPD we measured 1.8 ns for the risetime and 1.9 ns for the fall time. The overshoot, especially for 660 nm is an effect of laser modulation. The transient response shows no diffusion component for the UPD, as well as for the LPD.

The AC small signal response of the two photodiodes UPD and LPD at a wavelength of 660 nm can be seen in Figure (2.17) on bottom graph. Bandwidths of about $f_{-3db} = 250$ MHz and 150 MHz were found for UPD and LPD. The small increase of gain up to approximately 50 MHz can be explained with a non-optimum measurement calibration. The high bandwidth at 660 nm makes the two photodiodes suitable for high speed applications up to data rates of approximately 300 Mbit/s. An application of the two photodiodes in parallel gives a high responsivity performance of 0.4 A/W.

2.3.3.3 Transient and AC Behavior for 780 nm

The measured transient and AC behavior of the photodiodes for a wavelength of 780 nm can be seen in Figure (2.18). The risetime and falltime of the UPD was measured to be t_r=1.4 ns and t_f=1.8 ns, respectively. For the LPD we found t_r=7 ns and t_f=10 ns. The transient response for the lower photodiode LPD shows a slow component of approximately 10% to 15% of the total amplitude, caused by carrier diffusion in the p-substrate. Nevertheless in other approaches a comparable small risetime of about 7 ns at a wavelength of 780 nm was only published in a BiCMOS process with a modification of the epitaxial substrate material [26]. In contrast, this approach uses an unchanged low cost BiCMOS process with standard substrate material. The bottom graph of Figure (2.18) shows the small signal bandwidth measurements of the two photodiodes at 780 nm wavelength. Values of $f_{-3db} = 250$ MHz and 100 MHz were found for UPD and LPD.

If a higher responsivity at 780 nm is necessary, both photodiodes UPD and LPD can be used in parallel, which results in a responsivity S = 0.4 A/W. The resulting rise time for 780 nm is still only 4 - 5ns and therefore very fast, for a photodiode with absolutely no

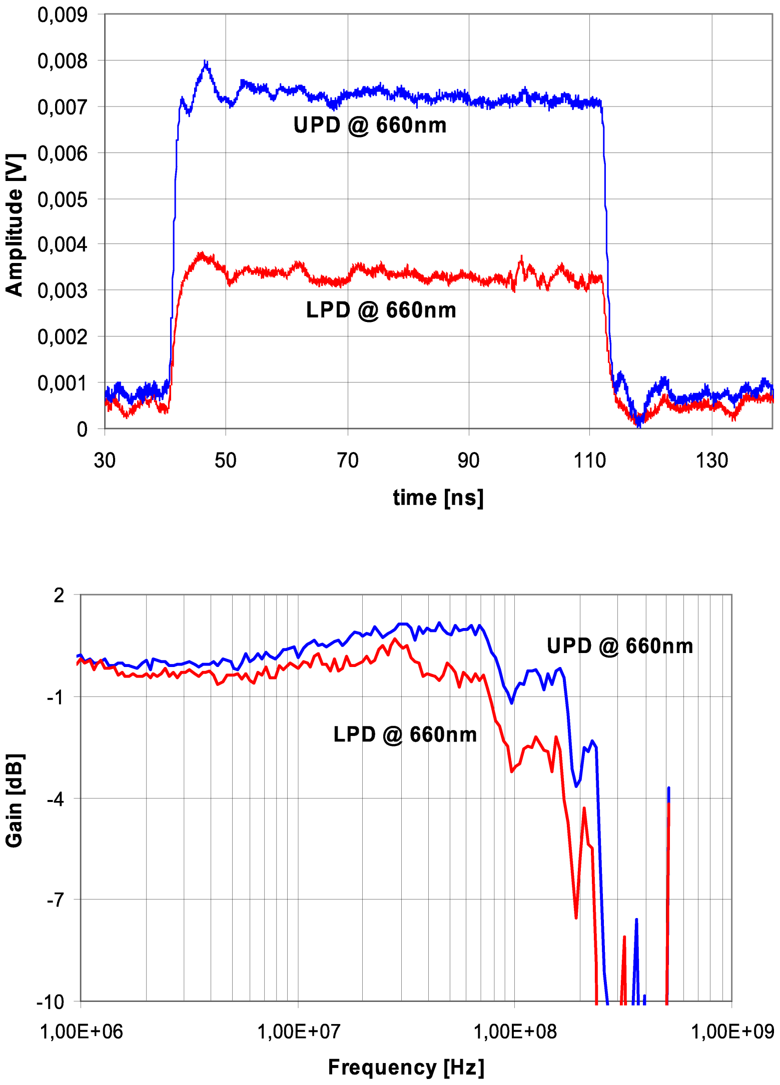


Figure 2.17: Transient response (top) and small signal bandwidth (bottom) of the B6CA photodiodes UPD and LPD at 660nm wavelength.

process modification. The DPD gives high flexibility in terms of responsivity and speed for several applications (eg. in the field of fiber communication OEICs).

An analytical representation of the presented measurements will be shown in Section (3.2.4) (see also Figures (3.7)and (3.8)).

2.3.4 Summary

In this section we presented an example for the integration of a double photodiode structure in a 0.6 μm BiCMOS technology. Looking on the doping layers available in the B6CA technology, one can see, that neither the sensitivity nor the speed will be an optimum for high performance photodiodes. Nevertheless a number of applications in the field of sen-

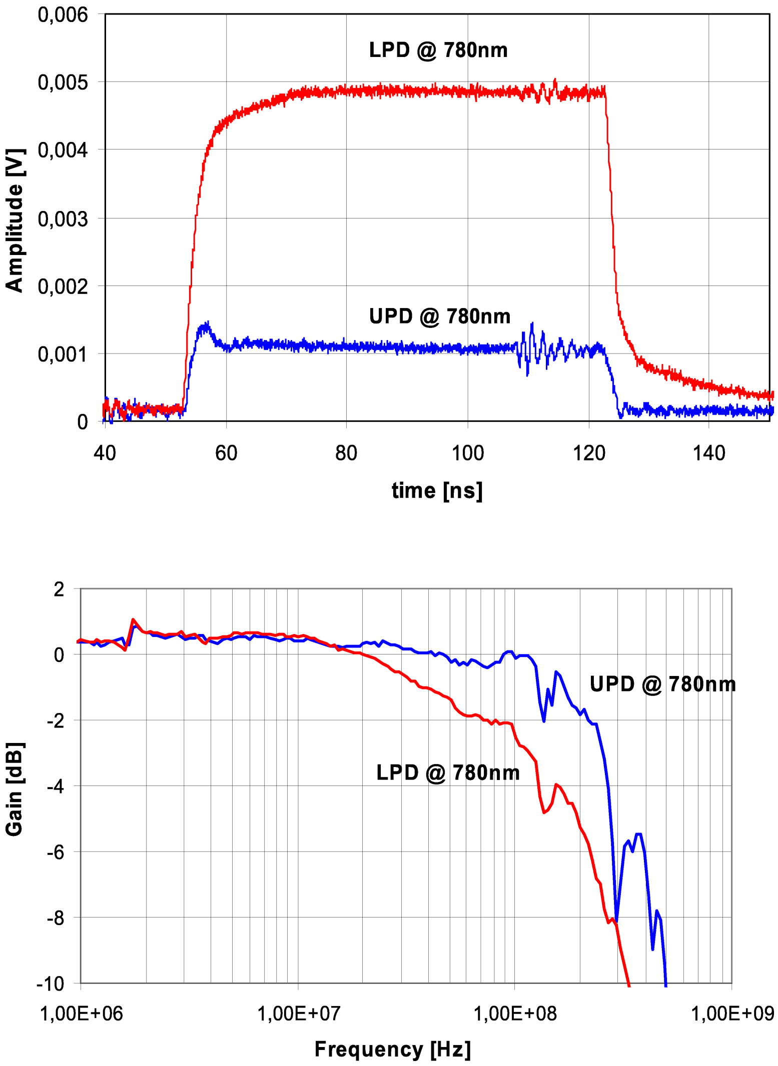


Figure 2.18: Transient response (top) and small signal bandwidth (bottom) of the B6CA photodiodes UPD and LPD at 780nm wavelength.

sors for optical data storage and fiber communication for medium speeds up to 100 MHz can be realized with these low cost photodiodes.

2.4 Integration of PIN Photodiodes

2.4.1 Introduction

For high speed ICs in next generations optical data storage applications, like blue laser DVD, new high performance photodiode structures are necessary. In this Section (2.4) we will present the development of high speed, high sensitivity PIN-photodiodes within the B6CA technology [27]. This technology option (called B6CP) needs process modifications which means higher process costs of about 15% compared to standard BiCMOS process

B6CA. Nevertheless the B6CP technology is a cost efficient solution for high speed OEIC‘s in the field of optical data storage or plastic optical fibers compared to a discrete IC with external PIN-photodiode connected by wire bonding. The B6CP process development was done within an EC funded IST-project called ”INSPIRED”.

2.4.2 Photodiode Implementation

Figure 2.19 shows a B6CP technology cross section with the PIN-photodiode on left-hand side and BiCMOS devices on right-hand side. The available devices are a single-poly NPN bipolar transistor with $f_t = 20\,GHz$, a vertical PNP bipolar transistor with $f_t = 1\,GHz$, standard $0.5\,\mu m$ CMOS and passive devices like capacitors, resistors and laser fuses. The integrated PIN-photodiode is optimized to high-speed and high-sensitivity for light wavelengths from 400 nm up to 800 nm.

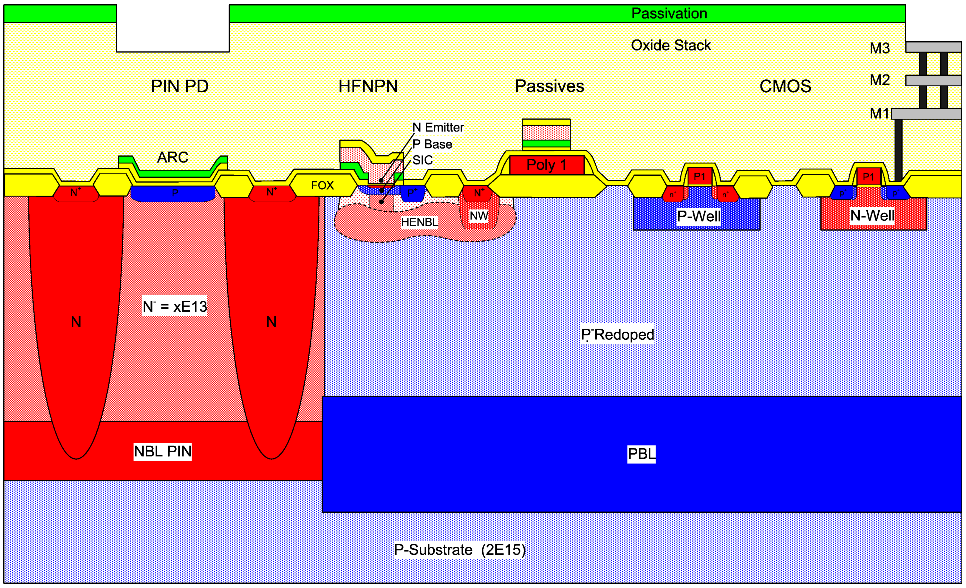


Figure 2.19: B6CP technology cross - section. On left hand side the PIN-photodiode and on right hand side the BiCMOS part can be seen, including bipolar NPN transistor, CMOS transistors and capacitances.

For the PIN-photodiode integration we implemented a SCR width of $10\,\mu m$ to realize a large sensitivity and high speed for the light wavelengths 410 nm, 650 nm and 780 nm used in the data storage applications for blu-ray, DVD and CD. In Figure 2.19 the photodiode anode is a shallow and highly doped P^+ layer at the surface. Below the anode there is a $10\,\mu m$ deep n-epitaxial layer with low doping concentration as almost intrinsic zone. The photodiode cathode is realized as highly doped N^+ buried-layer below the intrinsic layer. The buried-layer is connected with N^+ buried-contacts at the photodiode edge. With applied reverse voltage between anode and cathode the SCR spreads through the whole epitaxial layer down to the N^+ buried-layer. As we use a low epitaxial doping concentration this can be achieved for a small reverse voltage $<$ 2V. To reduce the light reflection due to silicon-oxide and nitride layers on top of the photodiode surface a special anti-reflexion-coating (ARC) layer is implemented on the silicon. Therefore high intrinsic speed and a large quantum efficiency are achieved with the integrated PIN-photodiode which is necessary for future OEIC requirements in optical data storage applications.

2.4.3 Characterization Results

The measured photodiode sensitivity of the integrated PIN-photodiode is shown in Figure 2.20.

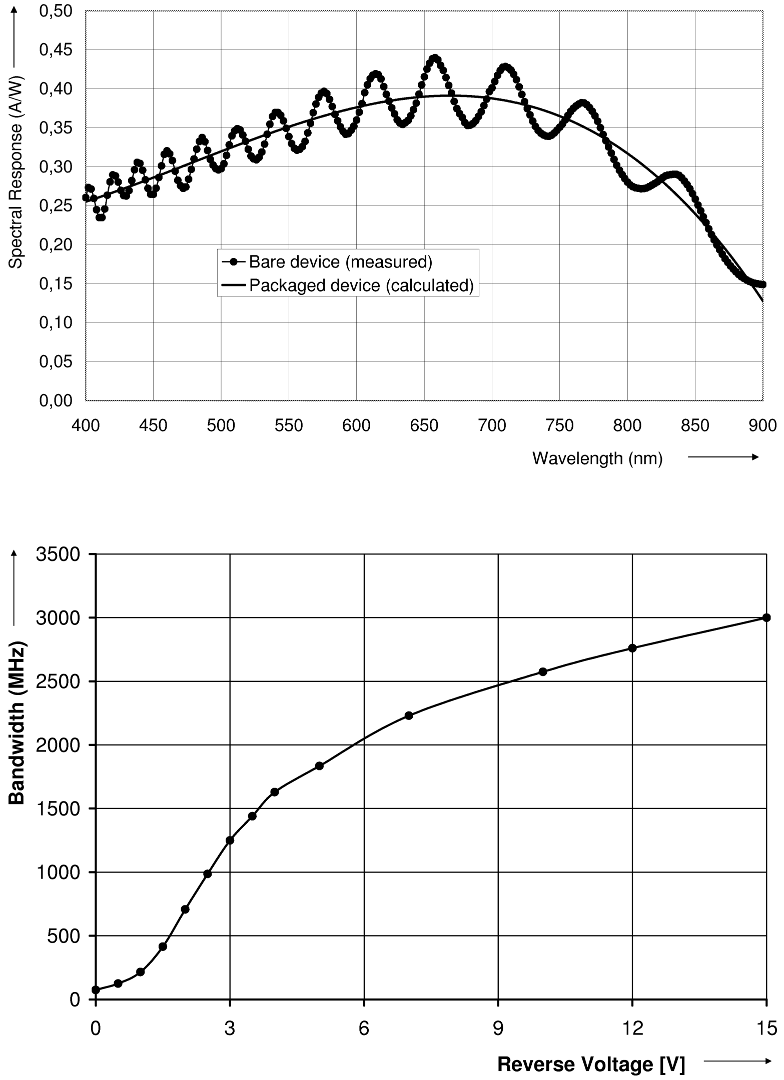


Figure 2.20: Spectral responsivity (top) and small signal bandwidths for different photodiode reverse voltages (bottom) of B6CP photodiodes [28].

The spectral response, which is the ratio of photocurrent to incident light power, is measured in dependence on the light wavelength from 400 nm to 900 nm. The photodiode demonstrates a high sensitivity of 0.25 A/W for 400 nm, 0.4 A/W for 660 nm and 0.35 A/W for 780 nm. The measurement for a bare photodiode without package shows a modulation in the sensitivity measurement of about 10% over the whole spectral range which is small due to the ARC layer. This modulation disappears completely on a packaged device. This is because the refractive index of the package epoxy material is matched to the silicon-oxide stack on the photodiode. Therefore the optical thickness of layers on the photodiode is large compared to light wavelength, which inhibits interference effects. The measured 3 dB small signal bandwidth of a 50 μm x 50 μm PIN photodiode is above 1 GHz without any diffusion effects with a reverse voltage of only 2.5 V. For higher reverse voltages the photodiode speed is even higher as shown on bottom graph of Figure 2.20 [28].

For photodiode characterization we developed a teschip with bare 50 μm x 50 μm photodiode structures as well as photodiodes including TIA circuits for characterization. The measurement setup is the same as explained in Section (2.3). The testchip silicon and the evaluation PCB is shown in Figure 2.21. The small signal bandwidth measurements shown in Figure 2.20 were performed at the Vienna University of Technology [28].

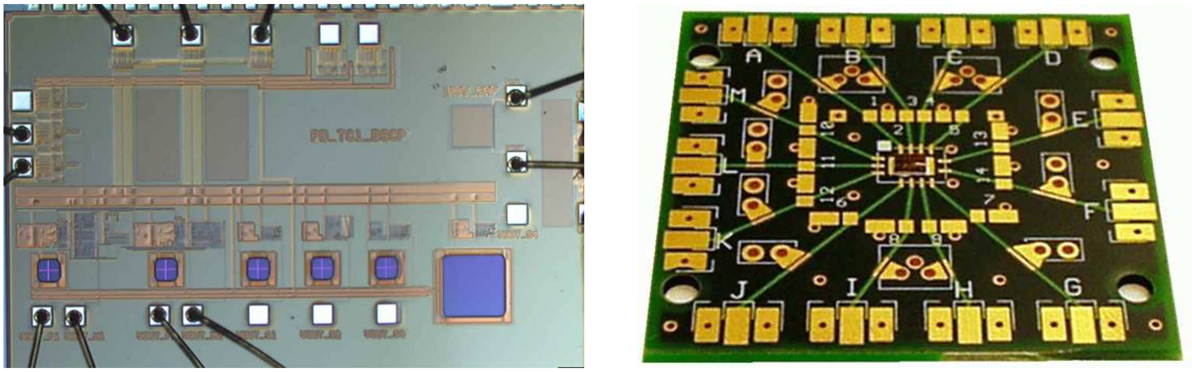


Figure 2.21: Photograph of the photodiode testchip with different photodiode geometries and read-out circuits. PCB for characterization of the photodiode testchip.

2.4.4 Summary

For high-speed optoelectronics applications with bandwidths above 100 MHz up to approximately 2 GHz at light wavelengths from 400 nm to 800 nm, special PIN - photodiode structures are necessary. Therefore process modifications has to be implemented within standard CMOS or BiCMOS technologies. On one hand this increases the process costs for about 15%. On the other hand, the combination of cheap CMOS / BiCMOS technologies together with high performance PIN-photodiodes enables the development of cost effective optoelectronics frontends for optical data storage and plastic optical fiber communication.

Within the EC funded project "INSPIRED" we developed the so called B6CP technology option, that integrates a high performance PIN-photodiode within a standard IFX $0.5\,\mu$m BiCMOS technology. With the B6CP technology we were able to design OEIC circuits for optical data storage applications up to 260 MHz bandwidth with a superior sensitivity of $100\,\mathrm{mV}/\mu\mathrm{W}$ as shown in Section (5). For optical data communication, data rates up to 5 Gbit/s can be achieved using B6CP PIN-photodiodes in combination with voltage-up-converters, as presented in [29].

Chapter 3

Photodiode Modeling

3.1 Introduction

The integration of photodiodes in silicon IC technologies is widely used since many years. Resent applications for OEIC's in the field of optical data storage or optical fiber communication, requests high - speed performance up to several 100 MHz. Since for these applications the IC performance is mainly limited by photodiode speed, an accurate photodiode model is essential for circuit design. Such model should include on one hand the sensitivity behavior over light wavelength, and on the other hand an accurate speed modeling including carrier drift and diffusion effects for arbitrary AC input light signals. For large photodiode areas, the speed behavior is often determined by drift and diffusion effects, and also by 3 - dimensional resistive and capacitive electrical behavior including photodiode contact geometry. As described in Section (2.2) a complete analytical solution of these photo-electronic effects is more or less impossible. Of course numerical calculations with device simulation tools (like MEDICI) can be performed up to very high accuracy levels. But simulation time becomes incredible high, even for 2 - dimensional simulations. Furthermore the results from device simulations can not be used within circuit simulations, since the model needs an analytical descriptions of the significant photodiode behavior.

In the literature there are only few publications presenting photodiode models for SPICE based circuit simulators [23, 30, 31]. In the following section an equivalent circuit SPICE model for an integrated double - photodiode (DPD) as presented in Section (2.3) will be introduced. The model includes most significant physical effects, like

- One dimensional minority carrier diffusion and drift through the photodiode layers.
- Arbitrary time dependent carrier generation due to incident light. The incident optical light power can be applied to the model, by an independent voltage source connected to an "optical" pin.
- Voltage dependence of carrier drift and diffusion effects.
- Wavelength dependent transmission and reflection due to photodiode surface layers.

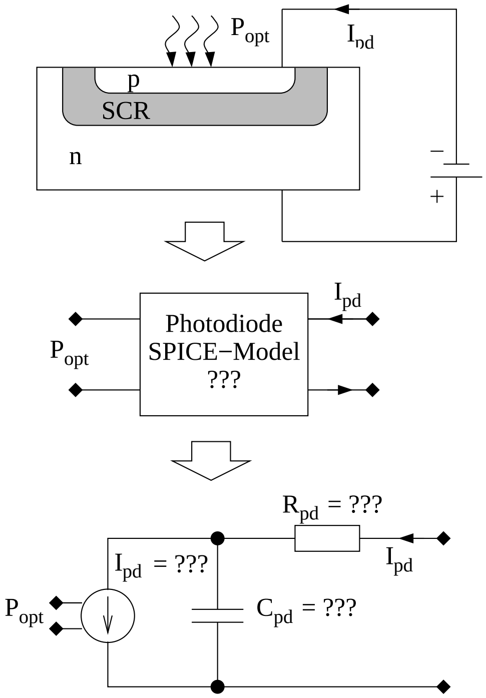


Figure 3.1: Photodiode SPICE model. The 3 - dimensional physical behavior is modeled by a simple R-C network with a controlled currentsource

- 3 - dimensional photodiode behavior by introducing a so called photodiode network model (PNM). This enables modeling of the photodiode speed dependence on photodiode geometry (photodiode dimensions and electrical contacts) which is, as far as we know, new for photodiode SPICE models. The photodiode geometry, including PNM as optimized SPICE netlist can be generated by a Mathematica script.

- Fast simulation speed due to simple photodiode equivalent circuit using SPICE primitives only.

- The model can be used for DC, transient time domain and small - signal AC simulations.

In Figure (3.1) the basic idea of the photodiode model is shown. The physical effects mentioned above, should be modeled with a simple SPICE circuit by only using SPICE primitive elements. This allows high simulation speed and good convergence for analog simulator algorithms.

The photodiode current, defined by drift and diffusion currents in the photodiode layers and generated from incident light power, is indicated by a controlled current source. The input pins P_{opt} can be connected to a variable voltage source and defines the time dependent incident light power. The light power reduction due to reflections at oxide and nitride photodiode surface layers is also included in the photo current model.

In Chapter (3.2) the solution of the time dependent continuity and carrier generation rate equations will be shown. The solution is based on the one-dimensional steady - state solution presented in Subsection (2.2.6.5). The time dependency within the continuity and rate equations can be described by an equivalent circuit using electrical elements like capacitors, resistors and controlled current sources. The electrical circuit model is indicated as current source in Figure (3.1).

The resistor R_{pd} and capacitor C_{pd} shown in Figure (3.1) is an equivalent circuit for the photodiode sheet resistance and capacitance, depending on photodiode area, geometry, SCR width, light beam diameter and contact resistances. Therefore this R-C circuit defines the 3 dimensional photodiode behavior. The calculation of R_{pd} and C_{pd} will be shown in Chapter (3.3). They can be extracted from an equivalent photodiode network model (PNM), by pole - zero analysis with additional reduction algorithm.

3.2 Analytical Drift and Diffusion SPICE Model

In this section the solution of time dependent continuity and rate equations will be presented, describing minority carrier generation, drift and diffusion through the different photodiode layers. This will be done by converting the analytical equations presented in Subsection (2.2.6.5) into an electrical equivalent circuit, also proposed by Chen and Liu [23], extended to an integrated BiCMOS double - photodiode (DPD) (presented in Section (2.3)). In addition the photo current dependency on photodiode reverse voltage as well as the wavelength dependent light transmission and absorption coefficient is implemented in this sub-circuit model.

The cross section of the BiCMOS integrated double photodiode (DPD) is shown on left hand side of Figure (3.2). The two photodiodes PD1 and PD2 are stacked. The upper diode is between a shallow and highly doped p+ region laying in a low doped n- region. The n- region is contacted by a highly doped n+ buried layer acting as cathode for the 2 photodiodes PD1 and PD2. The lower photodiode PD2 is between the n+ buried layer and the lower doped p- substrate. Between the photodiode layers a space - charge - region (SCR) is indicated, also called as intrinsic region or i-region. In the center of the picture, the doping concentration N_A, N_D of the photodiode layers as well as the absolute value of the electrical field is shown. It can be seen, that the SCR is mainly occurring in the lower doped regions, while the higher doped regions are acting as low ohmic photodiode contacts. The electrical field reaches high values only inside the SCR. For simplicity we assume, that the electric field is uniformly distributed in the SCR and zero outside the SCR. On right hand side of Figure (3.2) the decreasing light intensity inside the silicon is shown. When light with a certain certain energy $h\nu$ is falling onto the photodiode, only a smaller percentage T is transmitted into the silicon. Inside the silicon, the light

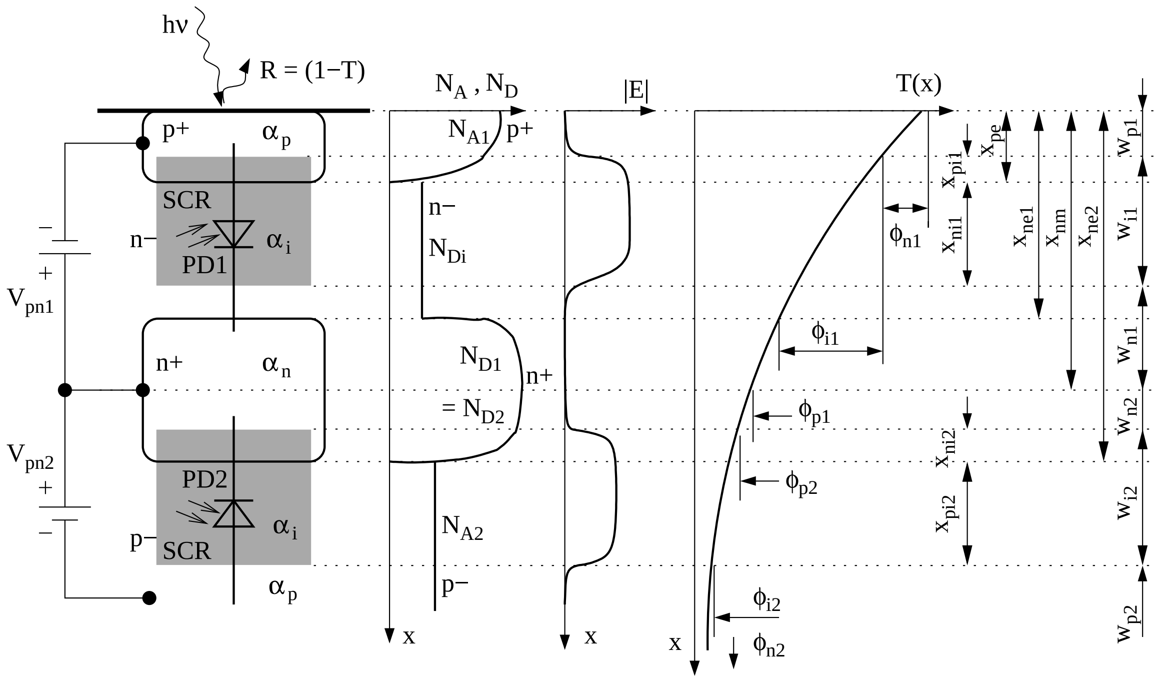


Figure 3.2: Cross section of a double photodiode with an upper photodiode PD1 and a lower photodiode PD2. The doping concentration N_A, N_D of the different layers, as well as the absolute electrical field |E| and light transmission $T(x)$ is shown.

intensity is decreasing due to absorption, depending on light wavelength. For following calculations the number of absorbed photons is important, which is approximately the number of generated carriers (carrier flux $\phi(x)$). It is proportional to the absorbed light power $P(x)$ as shown in Equations (2.13) and (2.14).

For the solution of continuity equations for the n and p - regions, the Equations (2.29) and (2.30) are modified by introducing the number of excess electrons and the photon flux. This leads to the rate-equations. As an example this modification is shown for the p-region Equation (2.29).

$$\frac{\partial n_p}{\partial t} = G_n(t) - \frac{n_p - n_{po}}{\tau_n} + D_n \frac{\partial^2 n_p}{\partial x^2} \tag{3.1}$$

By substituting the carrier generation $G_n(t)$ with $\partial\phi_n/\partial x$ and integration on both sides of Equation (3.1) we get

$$\int_0^{W_p} \frac{\partial n_p}{\partial t}\, dx = \phi_n - \int_0^{W_p} \frac{n_p - n_{po}}{\tau_n}\, dx + D_n \frac{\partial n_p}{\partial x} \tag{3.2}$$

With $N_p = \int (n_p - n_{po})\, dx$ and $I_n = -qD_n \frac{\partial n_p}{\partial x}|_{x=W_p}$ the rate equation for the p-region has the form

$$\frac{\partial N_p}{\partial t} = \phi_n - \frac{N_p}{\tau_n} - \frac{I_n}{q} \tag{3.3}$$

and identically for the n-region

$$\frac{\partial P_n}{\partial t} = \phi_p - \frac{P_n}{\tau_p} - \frac{I_p}{q} \tag{3.4}$$

with N_p is the number of excess electrons in the p-region and P_n is the number of excess holes in the n-region, ϕ_n and ϕ_p is the number of absorbed photons in the n-region and p-region respectively. I_n and I_p is the diffusion current from the p-region and n-region into the SCR.

Now the time dependent rate equations (3.3) and (3.4), which are equivalent to the continuity equations, must be solved for the two photodiodes PD1 and PD2 shown in Figure (3.2). This will be done by following steps

- Write the rate equations for the n-region, p-region and i-region of PD1 and PD2
- Calculate the generation rates ϕ_n, ϕ_p, ϕ_i for the n-region, p-region and i-region
- Converting the number of excess carriers P_n, N_p to voltage sources by introducing a parameter C_0 equivalent to an electrical capacitor.
- Converting the generation rates ϕ_n, ϕ_p, ϕ_i to electrical currents
- Converting the carrier life times τ_p, τ_n to electrical R-C time constants
- Substitute all electrical equivalent terms into the rate equations
- Substitute the diffusion currents I_n, I_p by the solution of the steady state continuity equations shown in Subsection (2.2.6.5).
- Connect all equivalent resistors, voltage and current sources to a photodiode SPICE model.

3.2.1 Solution of Rate Equations for Photodiode PD1

In this section, the rate equations for photodiode PD1 are solved according to the steps mentioned above

3.2.1.1 Rate equations for the n-region, p-region and i-region

For photodiode PD1, shown in Figure (3.2), the following rate equations can be derived

$$\text{p-region:} \qquad \frac{\partial N_{p1}}{\partial t} = \phi_{n1} - \frac{N_{p1}}{\tau_{n1}} - \frac{I_{n1}}{q} \tag{3.5}$$

$$\text{n-region:} \qquad \frac{\partial P_{n1}}{\partial t} = \phi_{p1} - \frac{P_{n1}}{\tau_{p1}} - \frac{I_{p1}}{q} \tag{3.6}$$

$$\text{i-region:} \qquad \frac{\partial P_{i1}}{\partial t} = \phi_{i1} - \frac{P_{i1}}{\tau_{pr1}} - \frac{P_{i1}}{\tau_{pt1}} - \frac{I_{p1}}{q} \tag{3.7}$$

The third equation for the intrinsic i-region is valid under neutral conditions ($P_{i1} = N_{i1}$), without electrons and holes impact ionization. The total current of the i-region (SCR) consists of holes current from the n-region I_{p1}, reduced by a recombination and drift term (defined by τ_{pr1} and τ_{pt1}). The τ_{n1} and τ_{p1} are the electrons and holes lifetime in the p-region and n-region. τ_{pr1} is the recombination lifetime of holes in the SCR (given by technology) and τ_{pt1} is the holes transit time through the SCR. The transit time depends on SCR width W_{i1} (see Equation (3.14)) and the hole velocity v_{p1} according to

$$\tau_{pt1} = \frac{W_{i1}}{v_{p1}} \tag{3.8}$$

The holes velocity v_{p1}, due to an electrical field inside the SCR, can be approximated by [17]

$$v_{p1} = \frac{E_1 \mu_{po}}{1 + \frac{\mu_{po} E_1}{V_{sp}}} \tag{3.9}$$

with μ_{po} is the holes mobility without electrical field (see Figure (2.8)) and v_{sp} is the holes saturation velocity for very high electrical fields (above $10^4\,V/cm$). v_{sp} is approximately $10^5\,m/s$ as shown in Figure (2.9). The electrical field E_1 inside the SCR is given by $E_1 = (-V_{pn1} + \phi_i)/W_{i1}$ with V_{pn1} is the reverse voltage applied to PD1 and ϕ_i is the diffusion voltage (approx. 0.8V).

3.2.1.2 Generation rates ϕ_n, ϕ_p, ϕ_i for the n-region, p-region and i-region

The minority carrier generation rates ϕ_n, ϕ_p, ϕ_i in the n-region, p-region and i-region, used in Equations (3.5) to (3.7), can be calculated as (see Equation (2.13)).

$$\text{p:} \qquad \phi_{n1} = \frac{P_{opt}T}{h\nu}(1 - \exp[-(\alpha_p W_{p1})]) \tag{3.10}$$

$$\text{i:} \qquad \phi_{i1} = \frac{P_{opt}T}{h\nu}\exp[-(\alpha_p W_{p1})](1 - \exp[-(\alpha_i W_{i1})]) \tag{3.11}$$

$$\text{n:} \qquad \phi_{p1} = \frac{P_{opt}T}{h\nu}\exp[-(\alpha_p W_{p1} + \alpha_i W_{i1})](1 - \exp[-(\alpha_n W_{n1})]) \tag{3.12}$$

with

$$W_{p1} = X_{pe} - X_{pi} \;\; \text{with} \;\; X_{pi} = \sqrt{\frac{2\epsilon_o \epsilon_r[\phi_i - V_{pn1}]}{qN_{A1}[1 + \frac{N_{A1}}{N_{D1}}]}} \tag{3.13}$$

$$W_{i1} = \sqrt{\frac{2\epsilon_0\epsilon_r}{q}\left(\frac{1}{N_{A1}} + \frac{1}{N_{D1}}\right)(\phi_i - V_{pn1})) \quad \text{see Eq.(2.48)} \tag{3.14}$$

$$W_{n1} = X_{nm} - W_{p1} - W_{i1} \tag{3.15}$$

The doping layer thicknesses X_{pe}, X_{ne1}, X_{nm} are defined by technology process.

3.2.1.3 Converting the number of excess carriers P_{n1}, N_{p1}, N_{i1} to equivalent voltage sources

To convert the generation rate Equations (3.5) to (3.7) to electrical equivalents, the excess carriers are substituted by electrical voltages. This can be done by introducing a constant C_{01} which is equivalent to a capacitor (this is correct, since voltage is the ratio of charge over capacitance)

$$P_{n1} = \frac{1}{q}C_{01}V_{p1} \quad N_{p1} = \frac{1}{q}C_{01}V_{n1} \quad P_{i1} = \frac{1}{q}C_{01}V_{i1} \tag{3.16}$$

3.2.1.4 Converting the generation rates ϕ_n, ϕ_p, ϕ_i to electrical currents

The carrier generation rates ϕ_n, ϕ_p, ϕ_i can be seen as electrical currents by introducing equivalent voltages V_{on1}, V_{op1} and V_{oi1}. Therefore Equations (3.10) to (3.12) can be written as

$$\text{p:} \qquad \phi_{n1} = \frac{P_{opt}}{V_{on1}} \equiv I_{on1} \;\; \text{with} \;\; V_{on1} = \frac{h\nu}{qT(1-\exp[-(\alpha_p W_{p1})])} \tag{3.17}$$

$$\text{i:} \qquad \phi_{i1} = \frac{P_{opt}}{V_{oi1}} \equiv I_{oi1} \;\; \text{with} \;\; V_{oi1} = \frac{h\nu \exp[(\alpha_p W_{p1})]}{qT(1-\exp[-(\alpha_i W_{i1})])} \tag{3.18}$$

$$\text{n:} \qquad \phi_{p1} = \frac{P_{opt}}{V_{op1}} \equiv I_{op1} \;\; \text{with} \;\; V_{op1} = \frac{h\nu \exp[(\alpha_p W_{p1} + \alpha_i W_{i1})]}{qT(1-\exp[-(\alpha_n W_{n1})])} \tag{3.19}$$

3.2.1.5 Converting the carrier time constants $\tau_{p1}, \tau_{n1}, \tau_{pr1}, \tau_{pt1}$ to electrical R-C time constants

The carrier life times τ_{p1}, τ_{n1} and the transit and recombination time τ_{pt1}, τ_{pr1} can be expressed by an electrical circuit model as R-C products. Equivalent electrical resistors R_{n1}, R_{p1}, R_{pr1} and R_{pt1} were introduced

$$\begin{aligned} \tau_{n1} &= R_{n1}C_{01} & \qquad \tau_{pr1} &= R_{pr1}C_{01} \\ \tau_{p1} &= R_{p1}C_{01} & \qquad \tau_{pt1} &= R_{pt1}C_{01} \end{aligned} \tag{3.20}$$

3.2.1.6 Substitute all electrical equivalent terms into the rate equations

The electrical equivalent sources and devices calculated in previous paragraphs, can now be substituted into the generation rate Equations (3.5) to (3.7)

$$\text{p:} \qquad I_{on1} = \frac{P_{opt}}{V_{on1}} = C_{01}\frac{\partial V_{n1}}{\partial t} + \frac{V_{n1}}{R_{n1}} + I_{n1} \tag{3.21}$$

$$\text{n:} \qquad I_{op1} = \frac{P_{opt}}{V_{op1}} = C_{01}\frac{\partial V_{p1}}{\partial t} + \frac{V_{p1}}{R_{p1}} + I_{p1} \tag{3.22}$$

$$\text{i:} \qquad I_{oi1} = \frac{P_{opt}}{V_{oi1}} = C_{01}\frac{\partial V_{i1}}{\partial t} + \frac{V_{i1}}{R_{pr1}} + \underbrace{\frac{V_{i1}}{R_{pt1}}}_{I_{i1}} - I_{p1} \tag{3.23}$$

These are the time dependent carrier rate equations, converted to electrical representation with voltages, currents, resistors and capacitors. A SPICE circuit model can be generated out of these equations. Only for the carrier diffusion currents I_{n1}, I_{p1} of the p-region and n-region a representation is still missing. Assuming the time dependent behavior is included in the arbitrary light input power P_{opt} and the excess carrier densities V_{p1}, V_{n1} and V_{i1} only, then currents I_{n1}, I_{p1} can be expressed as time in-depended functions of P_{opt}, V_{p1} and V_{n1}. Therefore I_{n1}, I_{p1} can be calculated from the solution of the steady state continuity equations presented in Section (2.2.6.5).

3.2.1.7 Substitute the diffusion currents I_{n1}, I_{p1} by the solution of steady state continuity equations

The steady state continuity equations for the p-region and n-region of photodiode PD1 can be written as presented in Equations (2.31) and (2.32).

p-region:

$$D_{n1}\frac{\partial^2 n_{p1}}{\partial x^2} - \frac{n_{p1} - n_{po1}}{\tau_{n1}} + G_{n1} = 0 \tag{3.24}$$

$$\text{with} \quad D_{n1} = \frac{L_{n1}^2}{\tau_{n1}} \quad \text{and} \quad n_{po1} = \frac{n_i^2}{N_{A1}}$$

$$G_{n1}(x) = \frac{P_{opt}T}{Ah\nu}\alpha_p \exp[-\alpha_p x]$$

n-region:

$$D_{p1}\frac{\partial^2 p_{n1}}{\partial x^2} - \frac{p_{n1} - p_{no1}}{\tau_{p1}} + G_{p1} = 0 \tag{3.25}$$

$$\text{with} \quad D_{p1} = \frac{L_{p1}^2}{\tau_{p1}} \quad \text{and} \quad p_{no1} = \frac{n_i^2}{N_{D1}}$$

$$G_{p1}(x) = \frac{P_{opt}T\exp[-(\alpha_p W_{p1} + \alpha_i W_{i1})]}{Ah\nu}\alpha_n \exp[-\alpha_n x]$$

Similar as shown before, the solution for I_{n1}, I_{p1}, presented in Equations (2.39) and (2.44), can be converted to electrical parameters. This leads to

$$I_{p1} \;=\; \frac{V_{p1}}{R_{pd1}} + \beta_{p1}P_{opt} + I_{po1} \tag{3.26}$$

$$I_{n1} \quad = \quad \frac{V_{n1}}{R_{nd1}} + \beta_{n1} P_{opt} + I_{no1} \tag{3.27}$$

with

$$R_{pd1} = R_{p1} \left[\cosh\left(\frac{W_{n1}}{L_{p1}} \right) - 1 \right] \tag{3.28}$$

$$R_{nd1} = R_{n1} \left[\cosh\left(\frac{W_{p1}}{L_{n1}} \right) - 1 \right] \tag{3.29}$$

$$I_{po1} = \frac{q p_{no1} A L_{p1} \left[\cosh\left(\frac{W_{n1}}{L_{p1}} \right) + 1 \right]}{\tau_{p1} \sinh\left(\frac{W_{n1}}{L_{p1}} \right)} \tag{3.30}$$

$$I_{no1} = \frac{q n_{po1} A L_{n1} \left[\cosh\left(\frac{W_{p1}}{L_{n1}} \right) + 1 \right]}{\tau_{n1} \sinh\left(\frac{W_{p1}}{L_{n1}} \right)} \tag{3.31}$$

$$\beta_{p1} = \frac{q T \alpha_n L_{p1}^2 \exp[-(\alpha_p W_{p1} + \alpha_i W_{i1})]}{h\nu (1 - \alpha_n^2 L_{p1}^2)} \times \tag{3.32}$$

$$\times \left\{ \frac{\cosh\left(\frac{W_{n1}}{L_{p1}} \right) + 1}{L_{p1} \sinh\left(\frac{W_{n1}}{L_{p1}} \right)} + \frac{\exp[-\alpha_n W_{n1}] - 1}{\alpha_n L_{p1}^2 \left[\cosh\left(\frac{W_{n1}}{L_{p1}} \right) - 1 \right]} - \alpha_n \right\}$$

$$\beta_{n1} = \frac{q T \alpha_p L_{n1}^2}{h\nu (1 - \alpha_p^2 L_{n1}^2)} \left\{ \frac{\left[\cosh\left(\frac{W_{p1}}{L_{n1}} \right) + 1 \right] \exp[-\alpha_p W_{p1}]}{L_{n1} \sinh\left(\frac{W_{p1}}{L_{n1}} \right)} + \right. \tag{3.33}$$

$$\left. + \frac{\exp[-\alpha_p W_{p1}] - 1}{\alpha_p L_{n1}^2 \left[\cosh\left(\frac{W_{p1}}{L_{n1}} \right) - 1 \right]} + \alpha_p \exp[-\alpha_p W_{p1}] \right\}$$

The total photodiode current of PD1 can now be calculated as

$$I_{pd1} = I_{n1} + I_{i1} + I_{d1} \tag{3.34}$$

This current I_{pd1} is the sum of p-region diffusion current I_{n1} and current I_{i1} flowing from SCR into the p-region. I_{i1} is mainly the sum of drift current inside the SCR, plus the diffusion current of the n-region flowing through the SCR into the p-region. An additional current I_{d1} is included in Equation (3.34), which is the dark current. This is due to tunneling of majority carriers from the n-region through the SCR to the p-region, against the electrical field. I_{d1} is in the range of few pA's dependent on photodiode size, temperature and technology process quality. Since I_{d1} is quite small for small photodiodes, this term can usually be neglected for high speed applications.

Now all terms of the time dependent continuity equations for PD1 are solved and converted to electrical components. By using these components and relations, a SPICE circuit model can be created. This will be demonstrated in Section (3.2.3). But first the electrical circuit representation for photodiode PD2 will be calculated same as for PD1.

3.2.2 Solution of Rate Equations for Photodiode PD2

In this section, the rate equations for photodiode PD2 are solved identically as shown for PD1 in Section (3.2.1. The results are mainly summarized. For more detailed explanations see Section (3.2.1).

3.2.2.1 Rate equations for the n-region, p-region and i-region

For photodiode PD2 as shown in Figure (3.2), the rate equations can be derived as

$$\text{p-region:} \qquad \frac{\partial N_{p2}}{\partial t} = \phi_{n2} - \frac{N_{p2}}{\tau_{n2}} - \frac{I_{n2}}{q} \tag{3.35}$$

$$\text{n-region:} \qquad \frac{\partial P_{n2}}{\partial t} = \phi_{p2} - \frac{P_{n2}}{\tau_{p2}} - \frac{I_{p2}}{q} \tag{3.36}$$

$$\text{i-region:} \qquad \frac{\partial N_{i2}}{\partial t} = \phi_{i2} - \frac{N_{i2}}{\tau_{nr2}} - \frac{N_{i2}}{\tau_{nt2}} - \frac{I_{n2}}{q} \tag{3.37}$$

The τ_{n2} and τ_{p2} are the electrons and holes lifetime in the p-region and n-region. τ_{nr2} is the recombination lifetime of electrons in the SCR and τ_{nt2} is the electrons transit time through the SCR. The transit time depends on SCR width W_{i2} (see Equation (3.14)) and the electrons velocity v_{n2} according to

$$\tau_{nt2} = \frac{W_{i2}}{v_{n2}} \tag{3.38}$$

The electrons velocity v_{n2} inside the SCR is

$$v_{n2} = \frac{E_2 \mu_{no}}{1 + \frac{\mu_{no} E_2}{V_{sn}}} \tag{3.39}$$

with μ_{no} is the electrons mobility without electrical field (see Figure (2.9)) and v_{sn} is the electrons saturation (approximately $10^5\, m/s$). The electrical field E_2 inside the SCR is given by $E_2 = (-V_{pn2} + \phi_i)/W_{i2}$ with V_{pn2} is the reverse voltage applied to PD2.

3.2.2.2 Generation rates ϕ_n, ϕ_p, ϕ_i for the n-region, p-region and i-region

The minority carrier generation rates ϕ_n, ϕ_p, ϕ_i in the n-region, p-region and i-region, used in Equations (3.35) to (3.37) is

$$\text{n :} \qquad \phi_{p2} = \frac{P_{opt} T}{h\nu} \exp[-(\alpha_p W_{p1} + \alpha_i W_{i1} + \alpha_n W_{n1})] \times$$

$$\times(1-\exp[-(\alpha_n W_{n2})]) \tag{3.40}$$

$$\text{i}: \quad \phi_{i1} = \frac{P_{opt}T}{h\nu}\exp[-(\alpha_p W_{p1}+\alpha_i W_{i1}+\alpha_n W_{n1}+\alpha_n W_{n2})] \times$$

$$\times(1-\exp[-(\alpha_i W_{i2})]) \tag{3.41}$$

$$\text{p}: \quad \phi_{n2} = \frac{P_{opt}T}{h\nu}\exp[-(\alpha_p W_{p1}+\alpha_i W_{i1}+\alpha_n W_{n1}+\alpha_n W_{n2}+\alpha_i W_{i2})] \times$$

$$\times(1-\underbrace{\exp[-(\alpha_p W_{p2})]}_{W_{p2}\approx\infty\,\Rightarrow\,0}) \tag{3.42}$$

with

$$W_{n2} = X_{ne2}-X_{nm}-X_{ni2} \text{ with} \tag{3.43}$$

$$X_{ni2} = \sqrt{\frac{2\epsilon_o\epsilon_r[\phi_i - V_{pn2}]}{qN_{D2}[1+\frac{N_{D2}}{N_{A2}}]}}$$

$$W_{i2} = \sqrt{\frac{2\epsilon_0\epsilon_r}{q}\left(\frac{1}{N_{A2}}+\frac{1}{N_{D2}}\right)(\phi_i - V_{pn2}))} \tag{3.44}$$

$$W_{p2} \approx \infty \tag{3.45}$$

3.2.2.3 Converting the number of excess carriers P_{n2}, N_{p2}, N_{i2} to equivalent voltage sources

The excess carriers are substituted by electrical voltages by introducing a capacitor C_{02}.

$$P_{n2} = \frac{1}{q}C_{02}V_{p2} \quad N_{p2} = \frac{1}{q}C_{02}V_{n2} \quad P_{i2} = \frac{1}{q}C_{02}V_{i2} \tag{3.46}$$

3.2.2.4 Converting the generation rates ϕ_n, ϕ_p, ϕ_i to electrical currents

The carrier generation rates ϕ_n, ϕ_p, ϕ_i were converted to electrical currents by introducing equivalent voltages V_{on2}, V_{op2} and V_{oi2}. Therefore Equations (3.40) to (3.42) can be written as

$$\text{n:} \quad \phi_{p2} = \frac{P_{opt}}{V_{op2}} \equiv I_{op2} \text{ with} \tag{3.47}$$

$$V_{op2} = \frac{h\nu\exp[\alpha_p W_{p1}+\alpha_i W_{i1}+\alpha_n W_{n1}]}{qT(1-\exp[-(\alpha_n W_{n2})])}$$

$$\text{i:} \quad \phi_{i2} = \frac{P_{opt}}{V_{oi2}} \equiv I_{oi2} \text{ with} \tag{3.48}$$

$$V_{oi2} = \frac{h\nu \exp[\alpha_p W_{p1} + \alpha_i W_{i1} + \alpha_n W_{n1} + \alpha_n W_{n2}]}{qT(1 - \exp[-(\alpha_i W_{i2})])}$$

$$\text{p:} \qquad \phi_{n2} = \frac{P_{opt}}{V_{on2}} \equiv I_{on2} \ \text{ with} \tag{3.49}$$

$$V_{on2} = \frac{h\nu \exp[\alpha_p W_{p1} + \alpha_i W_{i1} + \alpha_n W_{n1} + \alpha_n W_{n2} + \alpha_i W_{i2}]}{qT(1 - \exp[-(\alpha_p W_{p2})])}$$

3.2.2.5 Converting the carrier time constants $\tau_{p2}, \tau_{n2}, \tau_{nr2}, \tau_{nt2}$ to electrical R-C time constants

The carrier life times τ_{p2}, τ_{n2} and the transit and recombination time τ_{nt2}, τ_{nr2} can be expressed by introducing electrical resistors R_{n2}, R_{p2}, R_{nr2} and R_{nt2}

$$\begin{aligned} \tau_{n2} &= R_{n2}C_{02} & \qquad \tau_{nr2} &= R_{nr2}C_{02} \\ \tau_{p2} &= R_{p2}C_{02} & \qquad \tau_{nt2} &= R_{nt2}C_{02} \end{aligned} \tag{3.50}$$

3.2.2.6 Substitute all electrical equivalent terms into the rate equations

The electrical equivalent sources and devices can now be substituted into the generation rate Equations (3.35) to (3.37)

$$\text{n:} \qquad I_{op2} = \frac{P_{opt}}{V_{op2}} = C_{02}\frac{\partial V_{p2}}{\partial t} + \frac{V_{p2}}{R_{p2}} + I_{p2} \tag{3.51}$$

$$\text{p:} \qquad I_{on2} = \frac{P_{opt}}{V_{on2}} = C_{02}\frac{\partial V_{n2}}{\partial t} + \frac{V_{n2}}{R_{n2}} + I_{n2} \tag{3.52}$$

$$\text{i:} \qquad I_{oi2} = \frac{P_{opt}}{V_{oi2}} = C_{02}\frac{\partial V_{i2}}{\partial t} + \frac{V_{i2}}{R_{nr2}} + \underbrace{\frac{V_{i2}}{R_{nt2}}}_{I_{i2}} - I_{n2} \tag{3.53}$$

These are the time dependent carrier rate equations, converted to electrical representation with voltages, currents, resistors and capacitors for photodiode PD2. After calculating the steady state carrier diffusion currents I_{n2}, I_{p2} of the p-region and n-region, a SPICE circuit model can be generated. I_{n2} and I_{p2} can be calculated from the solution of the steady state continuity equations presented in Section (2.2.6.5).

3.2.2.7 Substitute the diffusion currents I_{n2}, I_{p2} by the solution of the steady state continuity equations

The steady state continuity equations for the p-region and n-region of photodiode PD2 can be calculated as presented in Equations (2.31) and (2.32).

n-region:

$$D_{p2}\frac{\partial^2 p_{n2}}{\partial x^2} - \frac{p_{n2} - p_{no2}}{\tau_{p2}} + G_{p2} = 0 \quad \text{with} \tag{3.54}$$

$$D_{p2} = \frac{L_{p2}^2}{\tau_{p2}} \quad \text{and} \quad p_{no2} = \frac{n_i^2}{N_{D2}}$$

$$G_{p2}(x) = \frac{P_{opt}T}{Ah\nu}\alpha_p \exp[-(\alpha_p W_{p1} + \alpha_i W_{i1} + \alpha_n W_{n1})] \exp[-\alpha_n x]$$

p-region:

$$D_{n2}\frac{\partial^2 n_{p2}}{\partial x^2} - \frac{n_{p2} - n_{po2}}{\tau_{n2}} + G_{n2} = 0 \quad \text{with} \tag{3.55}$$

$$D_{n2} = \frac{L_{n2}^2}{\tau_{n2}} \quad \text{and} \quad n_{po2} = \frac{n_i^2}{N_{A2}}$$

$$G_{n2}(x) = \frac{P_{opt}Tx}{Ah\nu} \exp[-(\alpha_p W_{p1} + \alpha_i W_{i1} + \alpha_n W_{n1} + \alpha_n W_{n2} + \alpha_i W_{i2})]\alpha_p \exp[-\alpha_p x]$$

The solution for I_{n2}, I_{p2} presented in Equations (2.39) and (2.44) can be converted to electrical parameters

$$I_{p2} = \frac{V_{p2}}{R_{pd2}} + \beta_{p2}P_{opt} + I_{po2} \tag{3.56}$$

$$I_{n2} = \frac{V_{n2}}{R_{nd2}} + \beta_{n2}P_{opt} + I_{no2} \tag{3.57}$$

with

$$R_{pd2} = R_{p2}\left[\cosh\left(\frac{W_{n2}}{L_{p2}}\right) - 1\right] \tag{3.58}$$

$$R_{nd2} = R_{n2}\left[\cosh\left(\frac{W_{p2}}{L_{n2}}\right) - 1\right] \tag{3.59}$$

$$I_{po2} = \frac{qp_{no2}AL_{p2}\left[\cosh\left(\frac{W_{n2}}{L_{p2}}\right) + 1\right]}{\tau_{p2}\sinh\left(\frac{W_{n2}}{L_{p2}}\right)} \tag{3.60}$$

$$I_{no2} = \frac{qn_{po2}AL_{n2}\left[\cosh\left(\frac{W_{p2}}{L_{n2}}\right) + 1\right]}{\tau_{n2}\sinh\left(\frac{W_{p2}}{L_{n2}}\right)} \tag{3.61}$$

$$\beta_{p2} = \frac{qT\alpha_n L_{p2}^2 \exp[-(\alpha_p W_{p1} + \alpha_i W_{i1} + \alpha_n W_{n1})]}{h\nu(1 - \alpha_n^2 L_{p2}^2)} \times$$

$$\times\left\{\frac{\left[\cosh\left(\frac{W_{n2}}{L_{p2}}\right)+1\right]\exp[-\alpha_n W_{n2}]}{L_{p2}\sinh\left(\frac{W_{n2}}{L_{p2}}\right)}+\right.$$

$$\left.+\frac{\exp[-\alpha_n W_{n2}]-1}{\alpha_n L_{p2}^2\left[\cosh\left(\frac{W_{n2}}{L_{p2}}\right)-1\right]}+\alpha_n\exp[-\alpha_n W_{n2}]\right\} \tag{3.62}$$

$$\beta_{n2}=\frac{qT\alpha_p L_{n2}^2\exp[-(\alpha_p W_{p1}+\alpha_i W_{i1}+\alpha_n W_{n1}+\alpha_n W_{n2}+\alpha_i W_{i2})]}{h\nu(1-\alpha_p^2 L_{n2}^2)}\times$$

$$\times\left\{\frac{\cosh\left(\frac{W_{p2}}{L_{n2}}\right)+1}{L_{n2}\sinh\left(\frac{W_{p2}}{L_{n2}}\right)}+\right.$$

$$\left.+\frac{\exp[-\alpha_p W_{p2}]-1}{\alpha_p L_{n2}^2\left[\cosh\left(\frac{W_{p2}}{L_{n2}}\right)-1\right]}-\alpha_p\right\} \tag{3.63}$$

The total photo diode current of PD2 can now be calculated as

$$I_{pd2}=I_{p2}+I_{i2}+I_{d2} \tag{3.64}$$

This current I_{pd2} is the sum of n-region diffusion current I_{p2} and current I_{i2} flowing from SCR into the n-region. I_{i2} is mainly the sum of drift current inside the SCR, plus the diffusion current of the p-region flowing through the SCR into the n-region. The dark current I_{d2} is quite small for small photodiodes, so this term can usually be neglected for high speed applications.

In this Section all terms of the time dependent continuity equations for PD1 an PD2 are solved and converted to electrical components. Now a SPICE circuit model can be created. This will be demonstrated in next Section (3.2.3).

3.2.3 SPICE Model for Photodiode PD1 and PD2

The one-dimensional drift- and diffusion current model for a double photodiode (DPD) structure shown in Figure (3.2) and Section (2.3) will be presented in this Chapter. The calculation results shown in previous Sections (3.2.1) and (3.2.2) can be expressed by electrical circuit components. The SPICE model shown in Figure (3.3) is a circuit representation of Equations (3.21), (3.22), (3.23), (3.26), (3.27) and (3.34) for PD1 and Equations (3.51), (3.52), (3.53), (3.56), (3.57) and (3.64) for PD2.

The light depending photocurrent of PD1 is I_{pd1} and for PD2 it is I_{pd2}. The input light intensity can be applied via a voltage source between P_{opt} and Ground. The photodiode

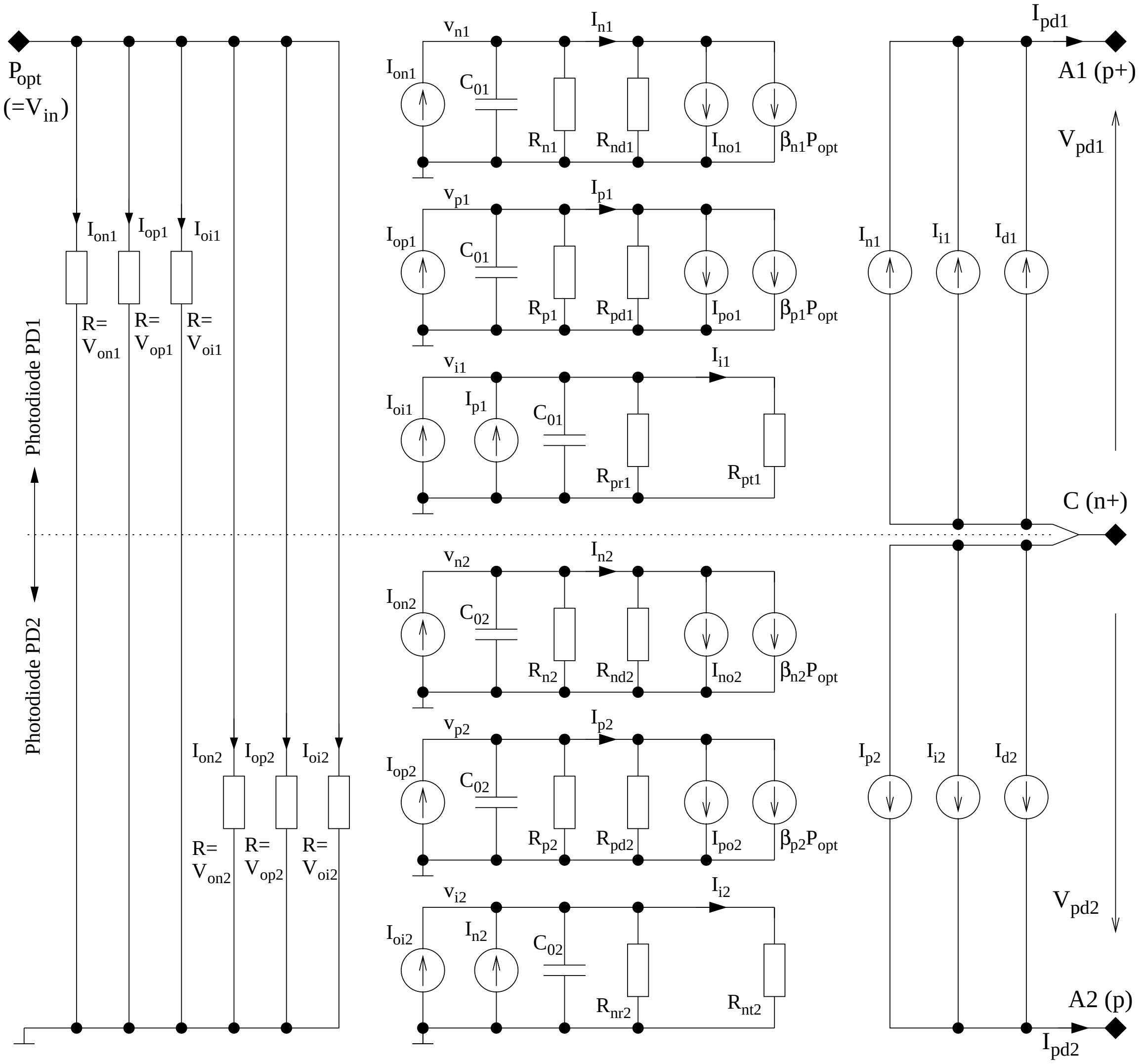


Figure 3.3: SPICE circuit model for a double photodiode (DPD) with an upper photodiode PD1 and a lower photodiode PD2. The light dependent photodiode current for PD1 is I_{pd1} and for PD2 is I_{pd2}. The input light intensity can be applied via a voltage source between P_{opt} and Ground. A1 and A2 are the photodiode anodes of PD1 and PD2 and C is the common cathode for PD1 and PD2

pins A1 and A2 are the photodiode anodes and C is the common cathode for PD1 and PD2.

Now we have defined a model of the light dependent, one-dimensional photodiode drift and diffusion current of a double photodiode structure. This current is indicated in the simplified model of Figure (3.1) as controlled current source. What is still missing in a realistic photodiode model, is the 3 dimensional behavior due to sheet resistance and capacitance, indicated as R-C components in Figure (3.1). The calculation of the R-C values will be presented in Section (3.3). But first we will show simulation results of the photodiode drift and diffusion SPICE model in next section.

3.2.4 Simulation Results for Photodiode SPICE Model

In this section simulation results of drift and diffusion current behavior, performed with the SPICE model from Figure (3.3) will be shown. The simulations where done with a SPICE based Infineon in-house simulator, called Titan. The full simulation SPICE netlist for Figure (3.3) is attached in Appendix B. The netlist starts with the definition of necessary parameters. After this, all equations for the SPICE netlist components of photodiodes PD1 and PD2 are listed. In addition to the SPICE model of Figure (3.3), the netlist contains the wavelength dependent light transmission Equation (2.11), presented in Section (2.2.3). The absorption coefficient is calculated according to Equation (2.15). After this, the circuit netlist for PD1 and PD2 is listed, using standard SPICE primitives like resistors (R), capacitors (C), voltage and current-sources (V, I), current-controlled-current-sources (F) and voltage-controlled-current-sources (G). The input light is applied by a voltage source on pin Vin.

In Figure (3.4) the simulated photodiode responsivity (ratio of photodiode current per input light power in [A/W]) is shown in dependence of light wavelength. The three graphs are the responsivity for photodiode PD1, PD2 and the sum of PD1+PD2 of a double photodiode (DPD) structure. The maximum responsivity for PD1 is at lower wavelengths (550 nm) compared to PD2 (850 nm). This is because PD1 is located near to the silicon surface. Therefore mainly light with lower wavelengths is absorbed, due to low penetration depth. Light with longer wavelength is penetrating deep into the silicon bulk and the resulting diffusion current is mainly collected by photodiode PD2. This is the reason for a higher sensitivity of PD2 at higher wavelengths. Figure (3.4) also shows significant sensitivity variation over wavelength of up to 60%, due to light interference inside the nitrid-oxide-silicon stack. To reduce these spectral variations, the nitride layer at the top of the photodiode can be removed as discussed in Section (2.2.3). Figure (3.5) shows the simulation results of the same DPD structure, but without passivation nitride layer covering the photodiode area. The variations are reduced significantly down to about 15%.

Figure (3.6) shows the measured responsivity values of a DPD test structure without nitride layer. Comparing these graphs with Figure (3.5), demonstrates a good correlation between measurement and simulation results. The basic responsivity characteristic over wavelength is very similar for simulation and measurement. Also the responsivity modulation amplitude over wavelength due to surface layer reflections is almost the same at lower wavelengths. Only at higher wavelengths above 800 nm the model accuracy becomes worse. One reason is that the responsivity modulation is very sensitive to layer thickness variations. The second reason is, that the model is not accurate enough to show a good

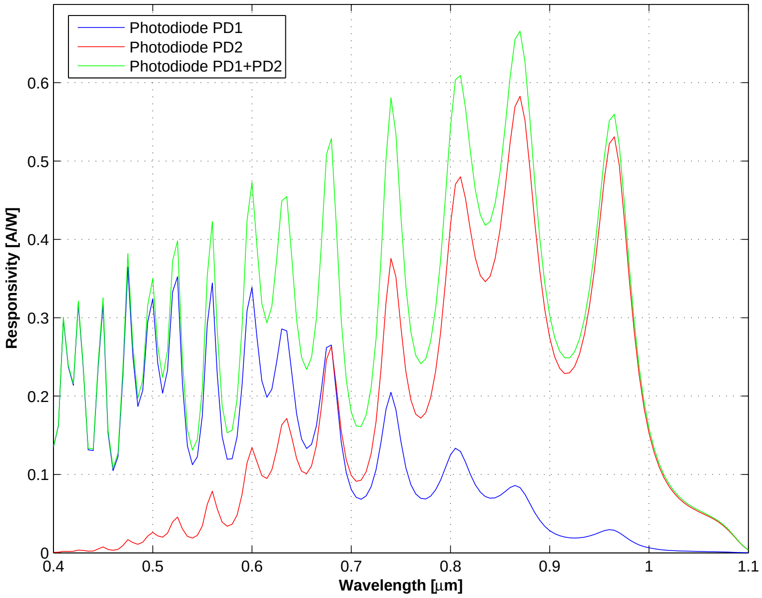


Figure 3.4: Simulated wavelength dependent photodiode responsivity in [A/W] for photodiode PD1 and PD2. The photodiode is covered with silicon nitrid.

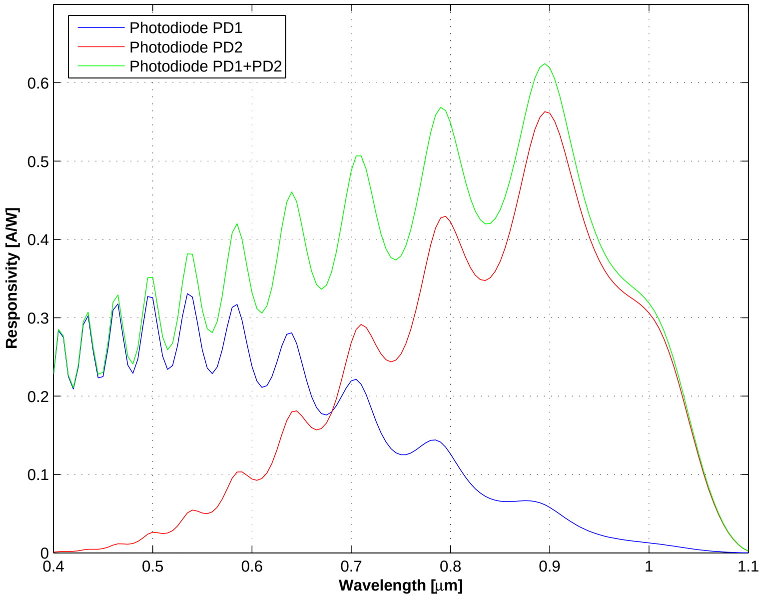


Figure 3.5: Simulated wavelength dependent photodiode responsivity in [A/W] for photodiode PD1 and PD2. The silicon nitrid is removed from photodiode surface.

representation of the responsivity drop at higher wavelength (near the band-gap energy). Therefore the responsivity drop above 850 nm is too steep with the simulation model.

The simulation results of a DPD pulse response is shown in Figure (3.7) and Figure (3.8) for 660nm and 780nm light wavelength. The y-axis shows the absolute photocurrent for

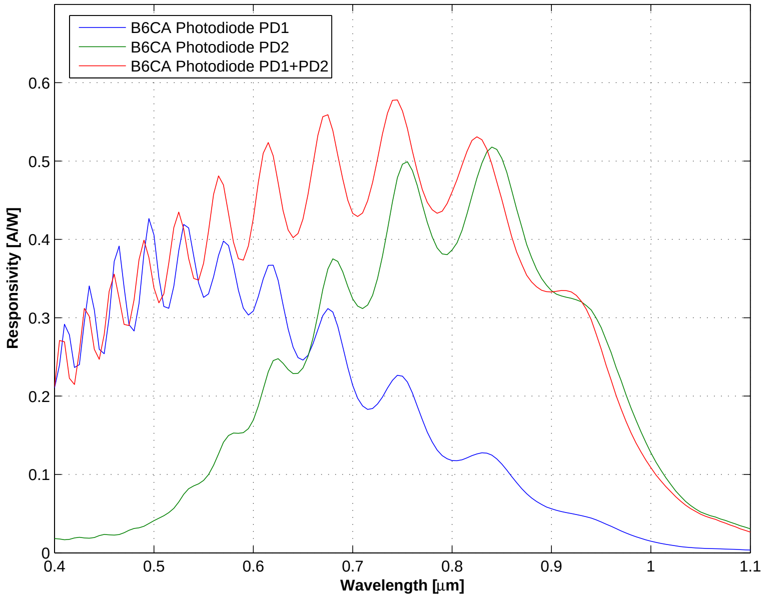


Figure 3.6: Measured wavelength dependent photodiode responsivity in [A/W] for a B6CA BiCMOS double photodiode structure. The silicon nitrid was removed from photodiode surface.

an input light pulse amplitude of 1 mW. It can be seen, that for 660nm light wavelength, the PD1 is more sensitive than PD2. Furthermore, PD1 and PD2 show no significant contribution of slow diffusion carriers. In difference to 660nm, at 780nm the PD2 has a major diffusion current contribution with a very slow rise-time of about 20ns. The simulation results of Figures (3.7) and (3.8) are matching very well to the measured DPD pulse responses, presented in Figures (2.17, 2.18).

Finally the Figure (3.9) shows the simulated pulse response for PD1 and PD2 at 660nm light, at different pn-junction reverse voltages. The rise-time of photodiode PD1 becomes slow at low reverse voltages. The reason is, that for low V_{pd} the SCR becomes smaller and therefore the slow diffusion current component is increasing.

These simulation and measurement results concludes the section of photodiode drift and diffusion current models. In next section a three dimensional R-C network model will be introduced.

3.3 Photodiode Network Model

3.3.1 Introduction

In previous Section (3.2), an analytical solution for a 1-dimensional drift and diffusion photodiode model, including light dependent carrier generation, was presented. In reality, a 1-dimensional model is not representative, especially for large photodiode structures.

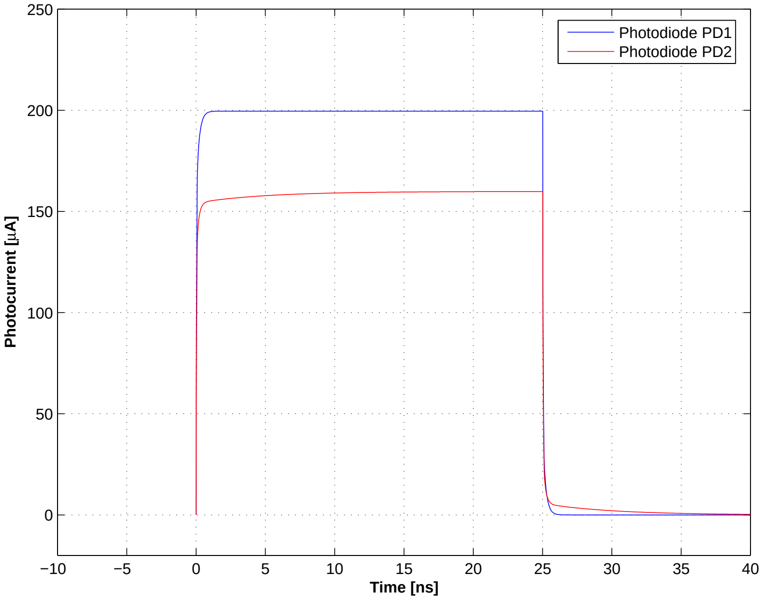


Figure 3.7: Simulated pulse response of a double photodiode PD1 and PD2 for 660nm light wavelength.

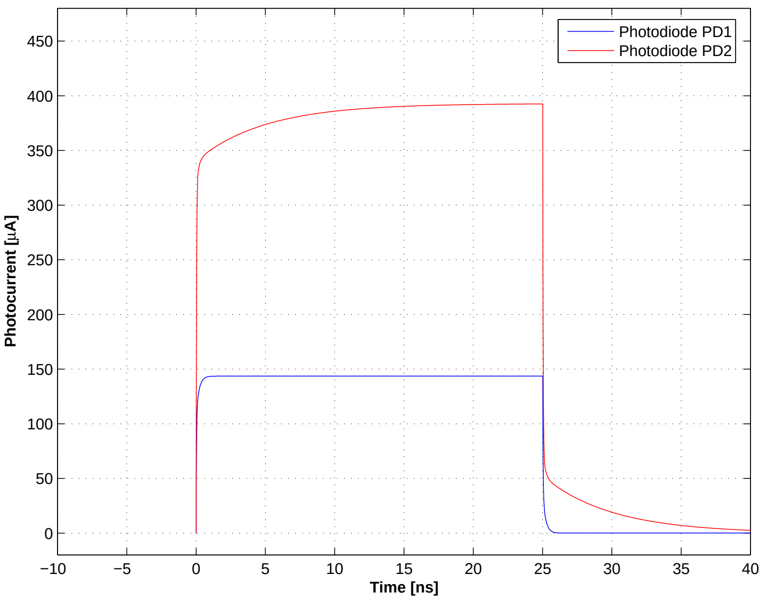


Figure 3.8: Simulated pulse response of a double photodiode PD1 and PD2 for 780nm light wavelength.

The analytical solution of time dependent diffusion and rate equations for 2 or even 3 dimensions is significantly more complex, and therefore not feasible. In this section, an alternative method for modeling the 3-dimensional photodiode behavior will be presented. The idea is, to use the 1-dimensional photodiode model and expand it to a 3-dimensional model, by building up a network. Every sub-cell of this network, is a photodiode SPICE model, as presented in previous section. In addition, the electrical sheet resistance of the

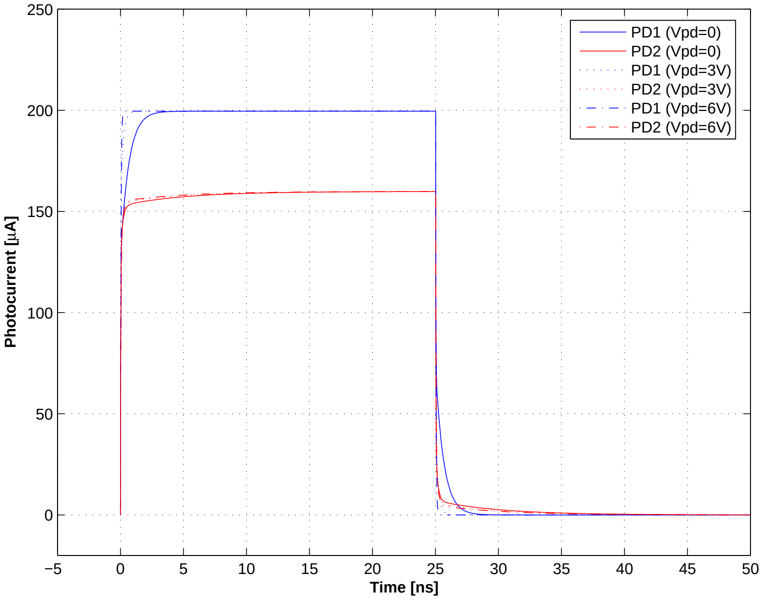


Figure 3.9: Simulated pulse response of a double photodiode PD1 and PD2, for 660nm light wavelength, in dependence on the photodiode pn junction reverse voltage

different photodiode layers and the pn-junction capacitance of the photodiode must be considered. It turns out, that for large area diodes, the photocurrent is most likely not limited by diffusion effects, but simply by the R-C time constant of sheet resistance and photodiode capacitance.

In next section, the realization of this photodiode network model (PNM) is described. A Mathematica script will be used, to define, generate and simplify the PNM. It generates a resistor-capacitor-current source (R-C-I) network as circuit model, representing the 3-dimensional photodiode behavior.

3.3.2 Realization of the Photodiode Network Model

For the PNM, the 3-dimensional photodiode structure is split into a network of small (1-dimensional) sections, as shown in Figure (3.10). Every section can be modeled as an R-C-I circuit. R is the layer sheet resistance ($R_{p,s}, R_{n,s}$) of p-doped and n-doped photodiode layers, C is the junction capacitance of the small photodiode section ($C_{pd,x}$) and I is the light dependent drift/diffusion photocurrent ($I_{pd,x}$) as presented in previous Section (3.2). To reduce the complexity of the R-C-I network, a simple equivalent circuit will be generated as shown in Figure (3.10). The single current source I_{pd} represents the total photodiode current, C_{pd} is the photodiode capacitance and R_{eff} is an equivalent resistor. The photodiode capacitance C_{pd} is well defined by the SCR-width as presented in Section (2.2.7). The photodiode current I_{pd} and the equivalent photodiode series resistor R_{eff} depends on the photodiode and light beam geometry and will be calculated via the

PNM. For higher accuracy, the simple R_{eff}, C_{pd} low-pass model can be extended to a more complex circuit. As an example a circuit model including 3 capacitors and 2 resistors will be presented.

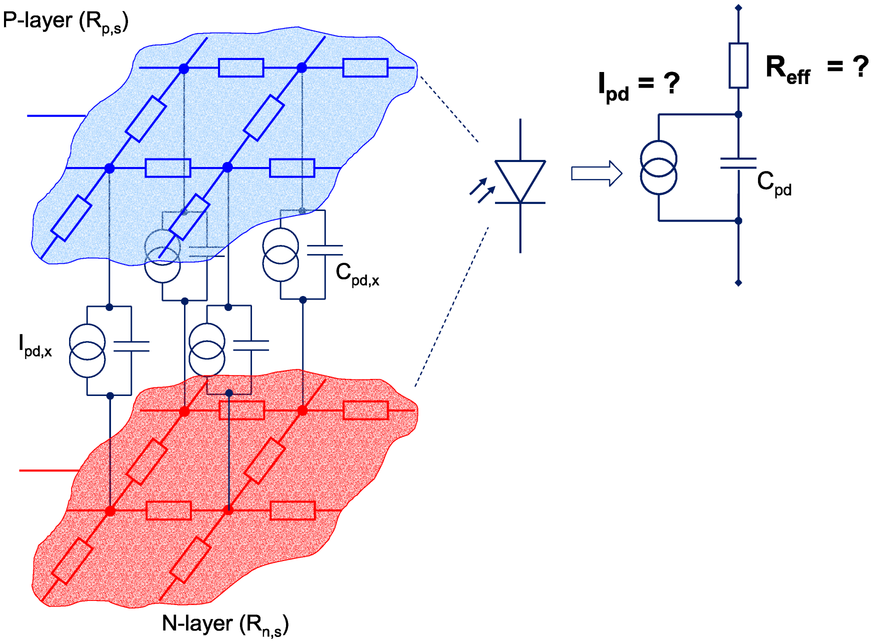


Figure 3.10: The 3 - dimensional dynamic behavior of the photodiode PD1 from a BiCMOS double photodiode structure can be described with a distributed R-C-I network

In the following section, the PNM of a BiCMOS double photodiode structure as presented in Section (2.3) will be described. The photodiode network depends on the photodiode dimensions, the electrical photodiode contacts and also the geometry and position of the incident light beam. To define the photodiode geometry, a Mathematica script was written called *"Photodiode Designer" (PDes)*. The script performs the following operations:

- With a graphical user interface, the photodiode can be designed. The photodiode dimensions can be defined. It also allows to draw electrical contacts for the anode of the upper photodiode PD1. The common cathode for PD1 and PD2 is a low ohmic contact ring around the photodiode (as implemented in the presented BiCMOS DPD structure). The anode of the lower photodiode PD2 is modeled as a single low-ohmic series resistor (approximately 20 Ω representing the resistor of substrate bulk silicon. Also the light beam size and location can be defined with the user interface. In Figure (3.12) two photodiode examples are shown. The left-hand photodiode 1 has anode contacts in the upper left corner and the right-hand photodiode has a contact ring around the whole photodiode area (indicated as 'X'). A light beam is indicated as "$*$" in the center of the photodiode. The photodiode is divided into a network of 20x20 segments. Every one of the 400 segments is modeled as a R-C-I circuit as shown in Figure (3.10).

- Out of this interactive drawing, a SPICE netlist of the R-C-I network is generated.
- Out of this netlist, a simplified model with few R's and C's is extracted by following steps:
    - Calculate the poles and zeros of the R-C-I network. In the *PDes* tool this is done by using a mathematica extension package called *"Analog Insydes"* [32]. This package allows numerical analysis of SPICE circuits, by solving the Kirchhoff equations. Most important circuit analysis methods like AC-analysis, pole-zero analysis and also transient analysis can be performed, using the analytical solutions of circuit equations. The pole-zero calculation can also be done with a standard analog simulator by loading the results into the *PDes* tool.
    - Reduce the number of poles and zeros by a reduction algorithm. The reduction algorithm cancels out pole/zero pairs with a similar frequency (defined by a deviation factor). This reduces the total number of approximately 400 poles and 400 zeros to about 20.
    - Take the first dominant poles p_1, p_2 and zeros z_1, z_2 at lowest frequency
    - Generate a simple R-C circuit model for PD1, representing these first poles and zeros. The dominant pole p_1 can be expressed by a simple R-C first order low-pass filter (see Figure (3.11a)). The capacitor of this low-pass is the photodiode capacitance C_{pd1}. The effective resistor R_{pd1} can be simply calculated from the pole p_1 with $R_{pd1} = 1/p_1 C_{pd1}$. For higher accuracy, a model representing the first two poles and two zeros can be used. The spice circuit for this model is shown in Figure (3.11b). The evaluation of the capacitor values for C_1, C_2, C_3 and the resistor values R_1, R_2 out of the first 2 poles p_1, p_2 and zeros z_1, z_2 is done with the *PDes* tool. In both circuits the photodiode PD2 is modeled as single pole low-pass filter with C_{pd2} is the capacitance of PD2 and R_{pd2} is the series resistor containing the bulk resistance and contact resistance. R_{pd2} is quite small ($< 20\Omega$). The substrate photodiode PD2 is in first order independent on the photodiode geometry.
    - Generate a netlist for the two simplified photodiode models, including extracted resistors, capacitors and current sources.
    - The photocurrent I_{pd1} and I_{pd2} is represented by the drift/diffusion SPICE model shown in Figure (3.3).
    - Generate two SPICE netlists for the two different photodiode models. One netlist contains a simple R-C photodiode representation and the other netlist is the more accurate model with C_1, C_2, C_3 and R_1, R_2 as well as photodiode

currents I_{pd1} and I_{pd2}. The photodiode netlists are defined as SPICE subcircuits and can therefore be included in other circuit schematics. All standard analog simulations like AC and transient simulations can be performed with the photodiode SPICE model.

- The printout of the photodiode designer *PDes* Mathematica code is shown in Appendix (A). An example for a single pole photodiode model netlist, containing all technology parameters necessary for I_{pd1} and I_{pd2} calculation, is shown in Appendix (B)

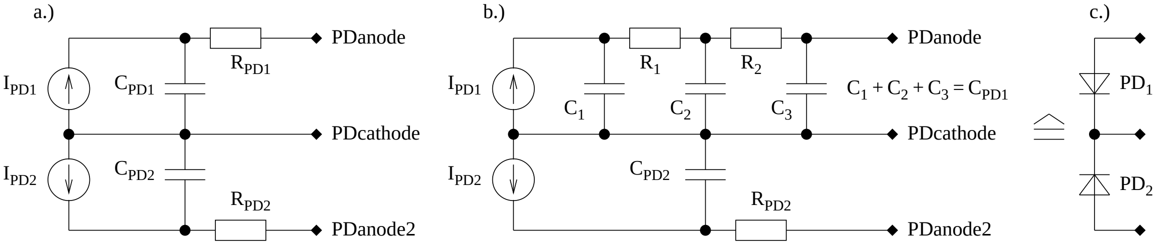


Figure 3.11: Simplified SPICE circuit models of a BiCMOS double photodiode structure. PD1 is the upper photodiode and PD2 is the lower substrate photodiode. In a.) the simple model of one dominant pole for PD1 is shown. In b.) a circuit model for PD1 representing 2 dominant poles and two zeros is shown. c.) shows the photodiode representation.

3.3.3 Simulation Results of the Photodiode SPICE Model

The following section presents simulation results from the discussed photodiode SPICE model of a BiCMOS double photodiode. The *PDes* tool was used to generate the photodiode model. This model includes all presented photodiode characteristics like drift and diffusion currents, wavelength dependent sensitivity and geometry dependent transient behavior. The generated SPICE sub-circuits are used to perform analog transient and small-signal AC simulations.

To demonstrate the influence of photodiode geometry on the speed performance, the SPICE models of two different photodiodes are generated with *PDes* as shown in Figure (3.12). Both photodiodes have a size of 0.7mm x 0.7mm. The two photodiodes differ in the anode contact geometry, where the left-hand photodiode 1 has anode contacts in the upper left corner and the right-hand photodiode 2 has a contact ring around the whole photodiode. A light beam is indicated as '$*$' in the center of the photodiode. In the simulation test-bench, the photodiode anodes are connected to 3V and the cathode to 0V. As input signal, an ideal light pulse is used. Therefore a voltage pulse source is applied to

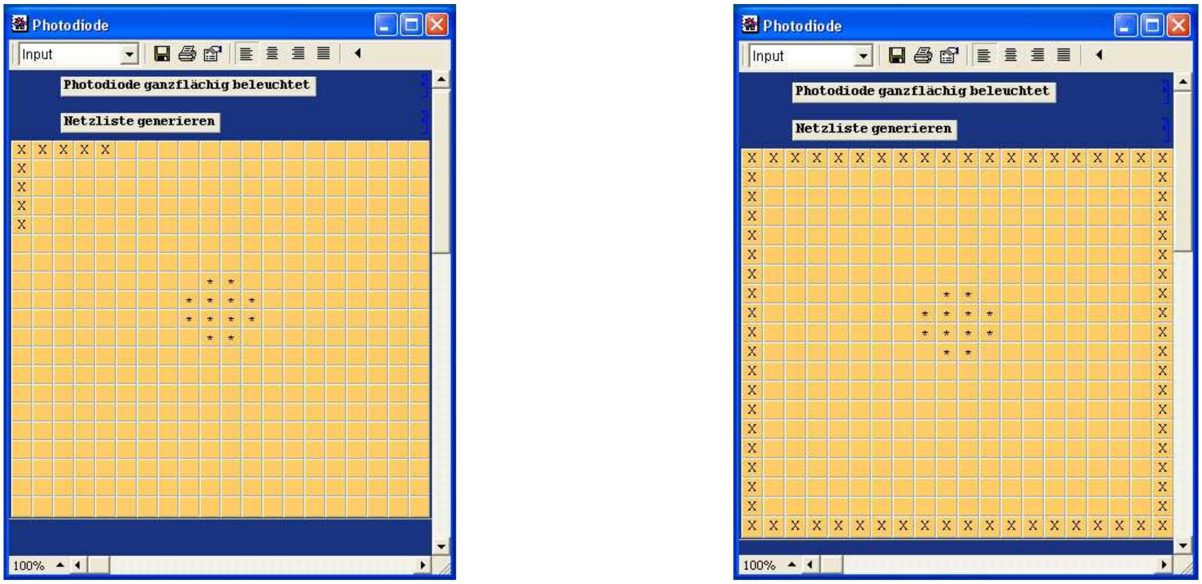


Figure 3.12: Two different photodiode designs. The left hand photodiode 1 has a contact only in one corner (indicated as 'X'). The right hand photodiode 2 has a contact ring around the whole photodiode. The light beam is in the center of both photodiodes 1 and 2 (indicated as '∗').

the photodiode model via pin "vin". The simulations were done with an analog simulator called TITAN.

In Figures (3.13, 3.14, 3.15) a transient simulation of the photodiode current is shown for three different models. One graph shows the (most accurate) full network model including all 400 nets as described before. The other two graphs are showing the simplified models including one dominant pole on one hand or 2 poles and 2 zeros on the other hand.

Figure (3.13) shows the results of photodiode 1, while Figures (3.14, 3.15) are from photodiode 2. It can be seen, that the most significant difference between the two photodiode designs is the speed. While photodiode 1 has a slow risetime of about 150ns, the photodiode 2 is much faster with about 10ns risetime. The reason is the higher contact resistance for photodiode 1, since the contacts are only located in one corner. But even the risetime of photodiode 2 is significantly higher, as the photocurrent simulations presented in Section (3.2.4) and shown in Figure (3.7). Due to the large photodiode area (0.7mm x 0.7mm) the photocurrent speed is always limited by R-C time constants and not necessarily by slow diffusion currents.

Comparing the simulations of the two simplified models with the full network model, it can be seen, that even the 1p model is already an accurate representation. For photodiode 1 it is even better as the more complex 2p-2z model (which is not true for photodiode 2). Therefore the simple one pole model is well suited for the design of OEIC's, since it has the fastest simulation speed with reasonable accuracy.

In Figures (3.16, 3.17) the small-signal AC simulation of photodiode 1 and photodiode 2 is shown. These simulations show, that the simplified 1p and 2p-2z models are accurate models for the photodiode bandwidth, but become inaccurate at frequencies higher as approximately 10 times the bandwidth.

Not only the photodiode contact geometry but also the light beam position has a big influence on photodiode speed. In Figure (3.18) two different photodiode models were generated. The geometry of both photodiodes is equal to photodiode 2 presented before. The only difference is, that the light beam on the right-hand graph is located in the center and on the left-hand graph in a corner of the photodiode. Figure (3.19) shows the transient pulse response simulation results for the two setups. It can be seen, that the photodiode with the light beam in the center is much slower compared to the one with light beam in the corner. The reason is once more the higher R-C time constant for currents generated in the photodiode center compared to the edge.

3.4 Summary and Conclusion

The verification results of a real BiCMOS double photodiode testchip, compared to the proposed photodiode SPICE model, concludes the section of photodiode modeling. These simulation and measurement results, shows a very good correlation for most significant photodiode effects. On one hand the photodiode drift and diffusion currents are modeled as SPICE circuit model including the dependence on input light intensity, light wavelength and photodiode reverse voltage. On the other hand a photodiode network model is used to extract a simplified SPICE model for the three dimensional dynamical photodiode behavior. A "Mathematica" tool called *PDes* was developed that simplifies the photodiode design and generates a full photodiode SPICE sub-circuit model. As far as we know, the presented photodiode SPICE model is outstanding in accuracy in combination with high simulation speed for this kind of integrated photodiodes.

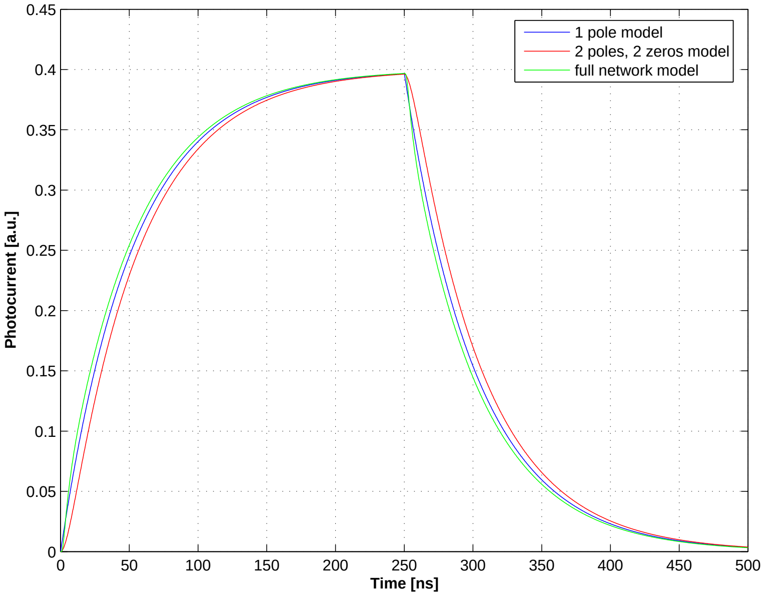


Figure 3.13: Transient simulation of a light pulse response with photodiode 1. The three graphs show the photodiode network model and the simplified 1-pole model and the 2-poles / 2-zeros model.

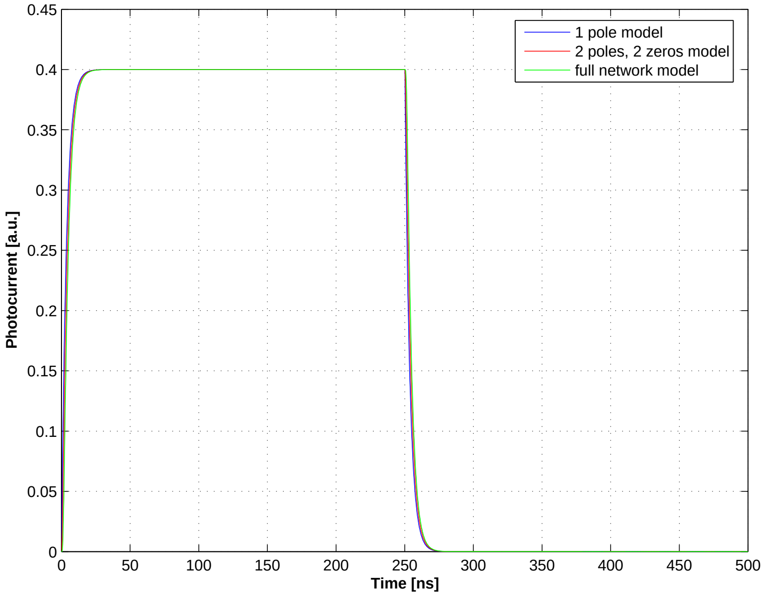


Figure 3.14: Transient simulation of a light pulse response with photodiode 2. The three graphs show the full photodiode network model and the simplified 1-pole model and the 2-poles / 2-zeros model.

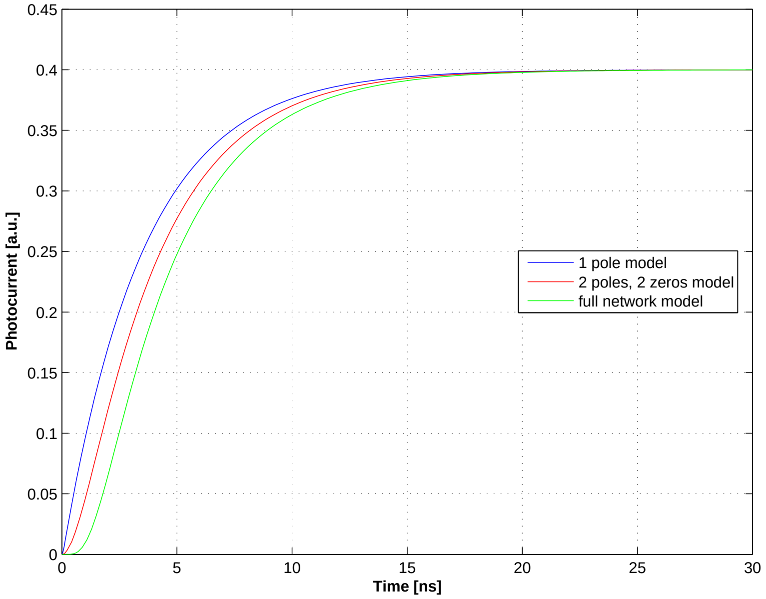


Figure 3.15: Transient simulation of a light pulse response with photodiode 2. Detail of figure 3.14.

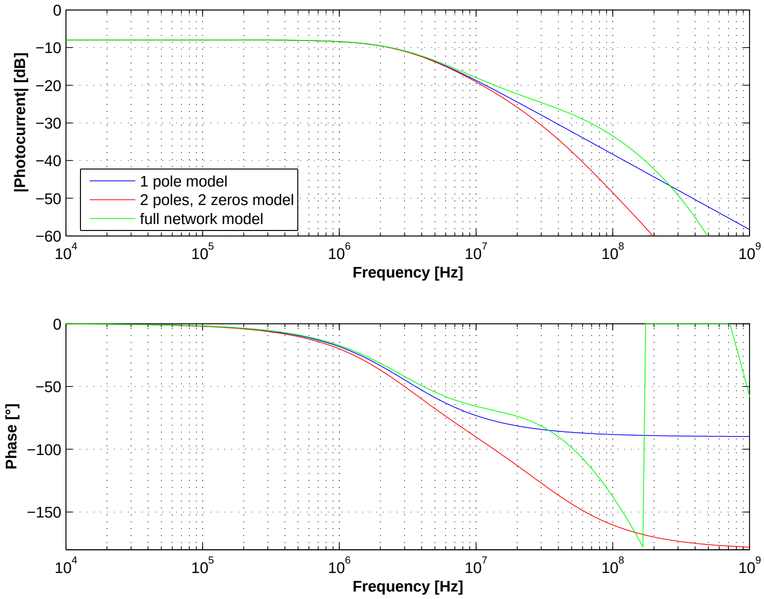


Figure 3.16: Small-Signal AC simulation of photodiode 1. The three graphs show the full photodiode network model and the simplified 1-pole model and 2-poles / 2-zeros model.

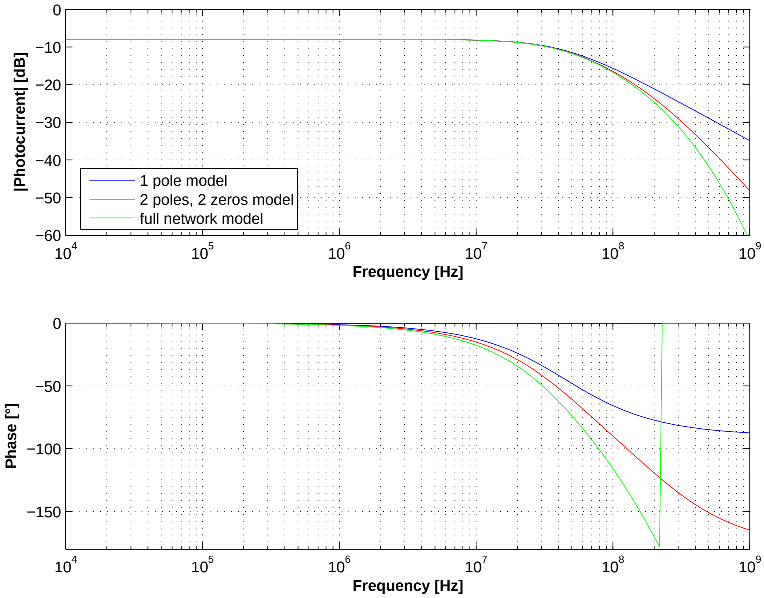


Figure 3.17: Small-Signal AC simulation of photodiode 2. The three graphs show the full photodiode network model and the simplified 1-pole model and 2-poles / 2-zeros model.

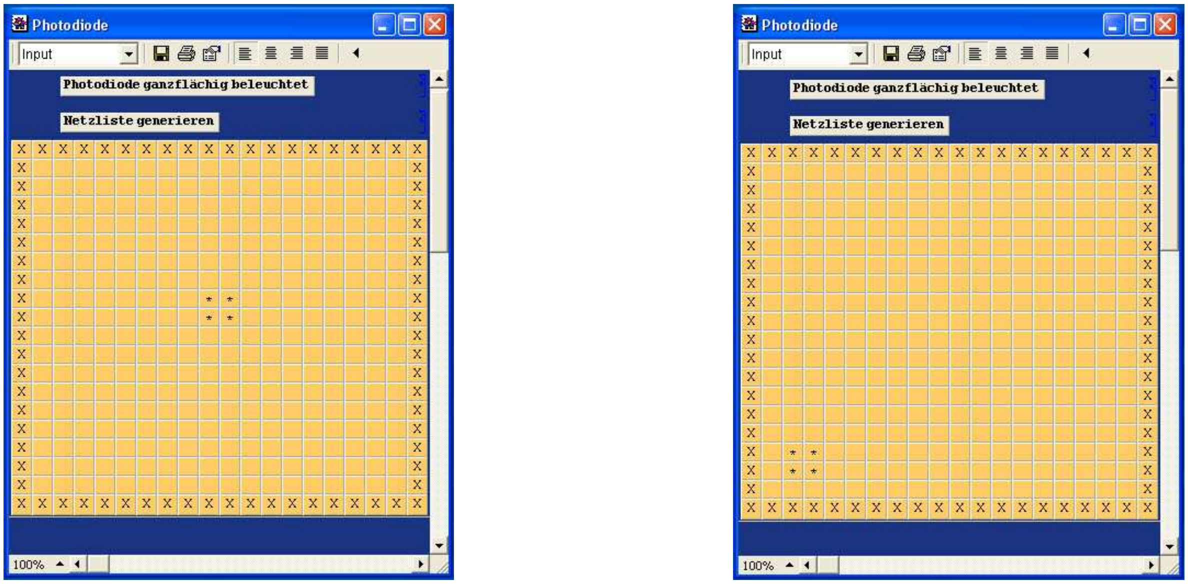


Figure 3.18: Models of photodiode 2 with different light beam positions in the center and in the corner.

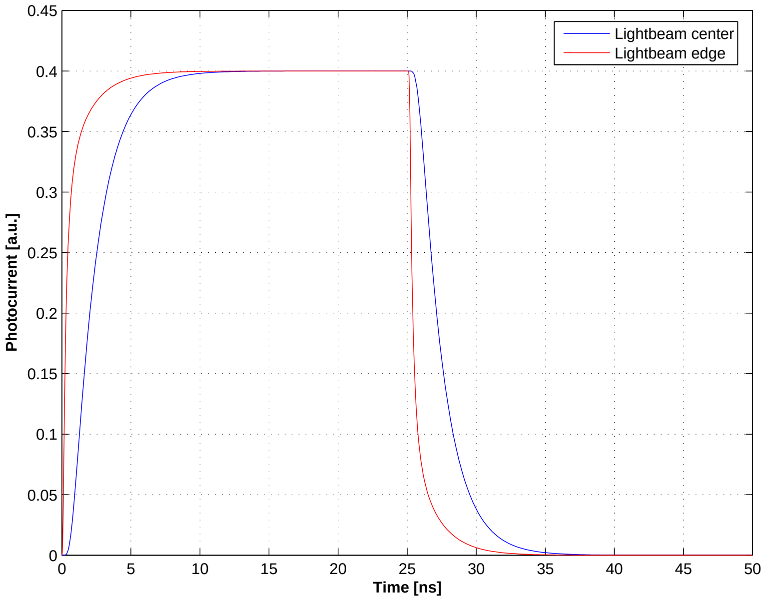


Figure 3.19: Transient simulation of a light pulse response from photodiode 2 with the lightbeam in the center and in the corner of the photodiode.

Chapter 4

Transimpedance Amplifier (TIA)

4.1 Introduction

As discussed in previous chapters, a photodiode converts light photon energy into an electrical signal by generating minority carriers within the semiconductor. For most optical sensor and data communication applications, the photodiodes are used as current sources with a reverse bias voltage applied to the photodiode pn-junction. As an alternative solution, the photodiode can be used as voltage source like in solar cells. However, this operating mode produces a highly non-linear output response with a very low bandwidth and is therefore not used in optical sensor and data communication applications. In next chapters we will restrict our discussion to reverse biased photodiode setups only. A photodiode has an excellent linearity, dynamic range and temperature stability. The main drawback of a reverse biased photodiode is a low sensitivity defined by the ratio of input light power over output current. Therefore in almost all applications an analog post-processing of the photocurrent is necessary. For sensor applications the photocurrent is amplified with very high gains, filtered or processed by an analog-to-digital converter (ADC) for further digital signal processing (DSP). Most optical data transmission applications, are using high-speed variable gain amplifiers (VGA) in combination with analog equalizers, and clock-and-data-recovery circuits. But for almost all applications, a transimpedance amplifier (TIA) circuit is used as first pre-amplifier stage. A TIA converts the photodiode current into a voltage signal which is more convenient for following signal processing.

Figure (4.1) shows a simple block diagram of a TIA with a photodiode connected to the input. The basic principle of a TIA is the conversion of the photodiode current i_{pd} to a voltage v_{pd} over a resistor R_t. Figure (4.1 a.) shows a simple current-to-voltage converter with only one resistor connected to the photodiode. As it will be explained in next section, this solution has a lot of disadvantages especially for high speed applications. A more complex but often used TIA structure is shown in Figure (4.1 b.). It uses an operational amplifier (opamp) with a feedback resistor to realize a current-to-voltage conversion. Due to high amplifier gain, the photodiode is now connected to a low impedance node at the TIA input. This isolates the photodiode capacitance from the voltage swing. Therefore

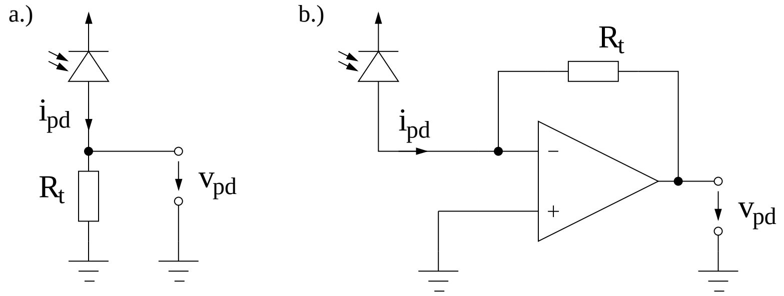


Figure 4.1: Basic block diagram of a transimpedance amplifier (TIA) connected to a photodiode. a) shows a simple resistor R_t as TIA and b.) shows an opamp with feedback resistor R_t as TIA.

this structure improves the TIA's speed performance significantly, as it will be shown in next section. While the basic structure of the opamp TIA is very simple, the circuit shows significant effort in design optimization, especially for high-speed applications. The main advantage of a TIA is flexibility in gain and bandwidth optimization compared to a standalone photodiode implementation.

Since the TIA is a key building block for most optoelectronics applications, the following sections of this chapter will give an introduction to TIA theory and should provide guidelines for the TIA design, especially for high-speed circuits. The next section will investigate TIA's bandwidth and stability behavior while following sections will point out the noise performance optimization. Also different architectures of single-ended and differential TIAs will be presented. All discussed TIA circuits were implemented in OEICs within standard low-cost CMOS and BiCMOS technologies.

4.2 TIA Basics

In this section some important TIA properties like gain and bandwidth will be investigated for two basic TIA structures as shown in Figure (4.1). This should give a first glance of the issues in TIA design which will be further investigated in following sections. The gain of a TIA, also called as transimpedance, is defined as ratio of output voltage over input current v_o/i_{in}. (see Figure (4.2)). The current i_{in} is the photodiode current flowing into the TIA. The voltage v_o is the TIA output voltage. Z_i is the effective input impedance of the TIA circuits, which defines together with C_i the impedance of the input node and so the bandwidth of the circuit. The capacitor C_i in Figure (4.2) is more or less given by the photodiode capacitance and therefore defined by application requirements. For high sensitivity, the photodiodes might be very large, which means a high capacitance C_i. $A_0(s)$ is the frequency dependent amplifier open-loop gain. In a first estimation, the gain A(s) can be assumed as constant over frequency. This is true, if the amplifier bandwidth is high compared to the TIA input node pole frequency.

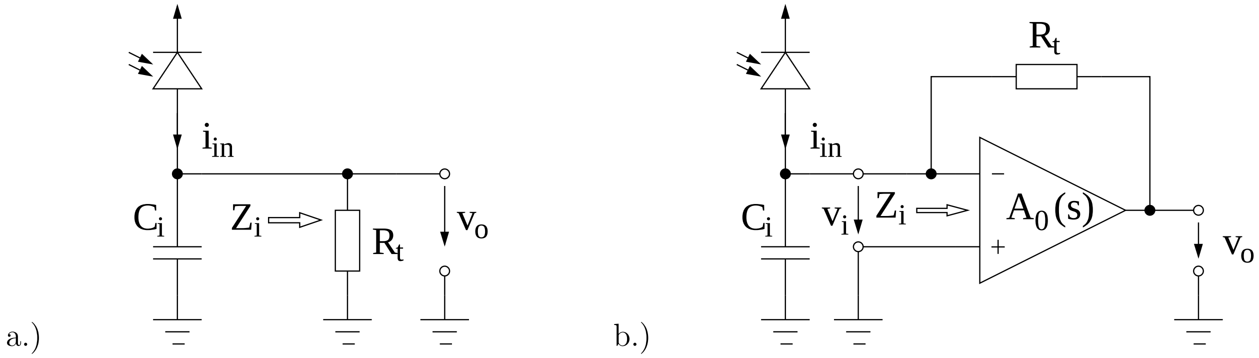


Figure 4.2: Two basic TIA structures (as also shown in Figure (4.1)), with a.) a simple resistor and b.) with an opamp TIA.

Lets compare the small signal transfer functions of the two structures in Figure (4.2 a.) and (4.2 b.), which is the transimpedance gain v_o/i_{in}.

Figure (4.2 a.):

$$\frac{v_0}{i_{in}} = \frac{R_t}{1 + sC_iR_t} \tag{4.1}$$

Figure (4.2 b.):

$$\frac{v_0}{i_{in}} = \frac{R_t\frac{A_0}{A_0+1}}{1 + sC_i\frac{R_t}{A_0+1}} \tag{4.2}$$

The DC-gain for the simple TIA in 4.2 a.) is the transimpedance resistor value R_t. For high amplifier gains A_0 this is also the case for 4.2 b.). Comparing the frequency behavior, the dominant pole which defines the small signal bandwidth f_{BW} for the two circuits are defined by:

Figure (4.2 a.):

$$f_{BW} = \frac{1}{2\pi C_iR_t} \tag{4.3}$$

Figure (4.2 b.):

$$f_{BW} = \frac{A_0 + 1}{2\pi C_iR_t} \tag{4.4}$$

Equation 4.3 shows, that the bandwidth of the simple resistor TIA is completely defined by a given transimpedance and photodiode capacitance. Equation 4.4 shows, that the opamp TIA has an approximately A_0 times higher bandwidth f_{BW}, compared to a simple resistor TIA. The amplifier gain A_0 is design dependent and higher than 1 for frequencies up to the amplifiers transit frequency f_t. Therefore the increased bandwidth for the same transimpedance value, is one of the most important advantages of an opamp TIA compared to a simple resistor solution. On the other hand, the simple resistor TIA has the lowest possible noise.

Comparing the equivalent input impedance Z_i of the two different TIA circuits, we get

Figure (4.2 a.):

$$Z_i = \frac{v_i}{i_{in}} = R_t \qquad (4.5)$$

Figure (4.2 b.):

$$Z_i \approx \frac{R_t}{A_0(s)} \approx \frac{R_t}{\frac{A_0}{1+s/p_A}} = \frac{R_t}{A_0} + \frac{R_t}{A_0 p_A} s \qquad (4.6)$$

Equation 4.6 shows the input impedance of the opamp TIA, which is equivalent to an inductance $L_{eq} \approx R_t/A_0 p_A$ and a series resistor $R_{eq} = R_t/A_0$. In combination with the photodiode capacitance C_i, the opamp TIA is therefore a resonance circuit, which might cause significant stability issues. This circuit configuration produces a double pole instead of a single pole behavior. Stability problems might occur, when the amplifier bandwidth is smaller, as the pole generated by the photodiode capacitance. The high impedance, for frequencies above amplifier bandwidth, often makes the TIA circuits oscillating. As an example we assume an opamp TIA, with a photodiode capacitance of C_i=10 pF, a transimpedance resistor of R_t=10 kΩ, an amplifier gain of A_0=50 and an amplifier bandwidth of p_a=200 MHz. According to Equation 4.4, this TIA has a small-signal bandwidth of about f_{BW}=78 MHz. A simple resistor TIA with same transimpedance, would have a low bandwidth of only 1.6 MHz. The equivalent inductance for the opamp TIA circuit is L_{eq}=1 μH. This gives a resonance frequency of $f_{res} = 1/\left(2\pi\sqrt{L_{eq}C_i}\right) = 50\,\text{MHz}$ which is inside the signal bandwidth of the TIA. These simple estimations should indicate, that stability is an important issue in TIA design.

In next section, the TIA transfer function will be investigated in more detail. Stability and bandwidth behavior will be analyzed, and design guidelines for bandwidth optimization will be presented.

4.3 TIA Bandwidth and Stability

In this section the bandwidth and stability behavior of an opamp TIA will be further investigated. As mentioned above, the opamp TIA forms a two-pole system, which can act as L-C tank that makes a careful stability analysis necessary. Theoretically the opamp provides a virtual ground node to the photodiode capacitance, which of course is not perfect due to the finite amplifier gain. Therefore it defines the first pole of the system. The second pole is given by a finite amplifier bandwidth, which further increases the impedance of the input node for high frequencies.

For a detailed analysis of the opamp TIA bandwidth and stability, the transfer function from Equation 4.2 is rewritten in Equation 4.7 by introducing a frequency dependent feedback factor $\beta(s)$.

$$\frac{v_0}{i_{in}} = -\frac{R_t}{1 + \frac{1}{A_0(s)\beta(s)}} \quad \text{with} \quad \beta(s) = \frac{1}{1 + sC_iR_t} \qquad (4.7)$$

The feedback factor $\beta(s)$ has a low-pass behavior with a pole at the frequency $f_{p\beta} = 1/2\pi R_t C_i$. Looking for the total phase of the transfer function, one gets a phase shift at dc of -180° from the inverting amplifier and additional -90° phase shift from the amplifier gain $A_0(s)$ above the -3 dB bandwidth frequency. The third phase shift contribution comes from $\beta(s)$, which is also -90° for frequencies higher $f_{p\beta}$. This sums up to a total phase shift of -360° which means positive feedback and therefore oscillation if the loop gain is higher than 1. The loop gain of Equation 4.7 is defined by $1/A_0(s)\beta(s)$. The critical frequency is therefore when $A_0(s) \leq \beta^{-1}(s)$.

A Bode-plot representation of the TIA feedback loop can be used to visualize the stability behavior [33] as shown in Figure (4.3). The blue graph in Figure (4.3) shows the amplifier open-loop gain $A_0(s)$ with an (assumed) 20 dB roll-off and a transit frequency (gain-bandwidth) at f_t. The red curve shows the inverse feedback factor $\beta^{-1}(s)$ with a zero (= pole for $\beta(s)$) at the frequency $f_{p\beta}$. The green curve is the overall TIA-gain as shown in Equation 4.7. As mentioned before, the critical frequency is at the crossing point of $A_0(s) = \beta^{-1}(s)$. At this frequency f_i the overall phase shift exceeds -360° if $\beta^{-1}(s)$ is further increasing (uncompensated). The TIA-gain is peaking at this frequency (instability) and shows a 2-poles -40 dB roll-off for higher frequencies.

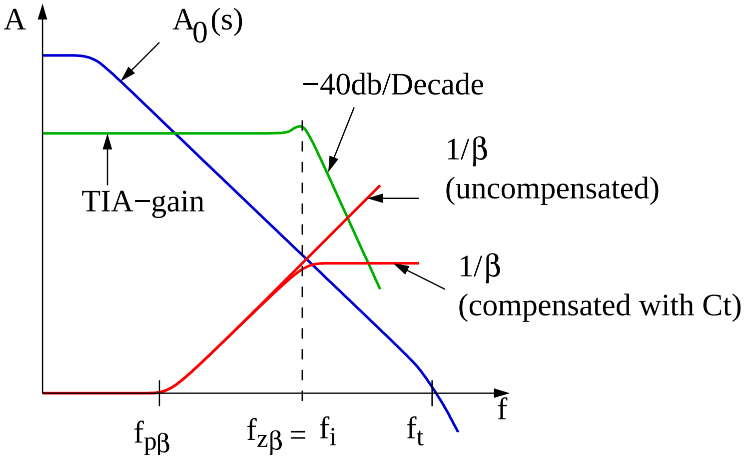


Figure 4.3: Frequency representation of the opamp TIA small signal transfer function with the overall TIA gain (green), the amplifier gain $A_0(s)$ (blue) and the inverse feedback factor β^{-1} (red).

There are mainly three possibilities to compensate the two poles stability issue. The first way is to define a proper photodiode capacitance C_i to ensure stability, which is not feasible in real applications. The second possibility is to optimize the amplifier bandwidth for stability. This would mean a reduction in the overall TIA bandwidth. Therefore the third and only feasible way to ensure stability is to implement an additional zero in the feedback path of $\beta(s)$. This zero should avoid a further decrease of $\beta(s)$ (increase of $\beta^{-1}(s)$) at the crossing point of $A_0(s) = \beta^{-1}(s)$. The red $\beta^{-1}(s)$ curve in Figure (4.3) is now snapped off due to the zero at frequency $f_{z\beta}$ and stops increasing. The zero in the feedback path can easily be realized with a capacitor C_t in parallel to the transimpedance resistor R_t. This is shown in Figure (4.4).

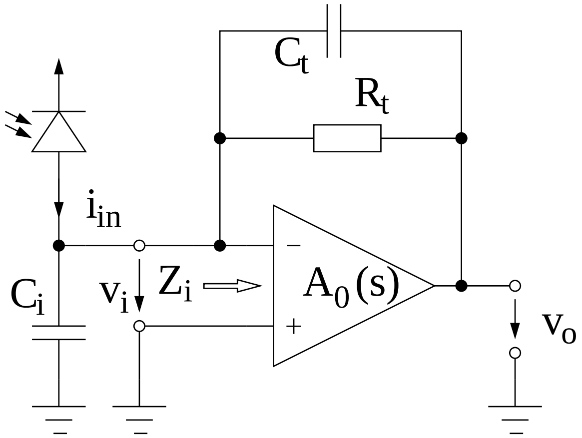


Figure 4.4: Block diagram of an opamp TIA with a compensation capacitor C_t implemented in parallel to the feedback resistor R_t.

The transfer function of the compensated TIA circuit including the capacitor C_t in the feedback path can be derived from Equation 4.7 as

$$\frac{v_0}{i_{in}} = -\frac{R_t}{(1+sC_tR_t)\left(1+\frac{1}{A_0(s)\beta(s)}\right)} \tag{4.8}$$

$$\text{with} \quad \beta(s) = \frac{1+sR_tC_t}{1+sR_t(C_i+C_t)} \tag{4.9}$$

Compared to Equation 4.7, the feedback factor $\beta(s)$ now includes a pole $f_{p\beta}$ and an additional zero $f_{z\beta}$ at following frequencies

$$f_{p\beta} = \frac{1}{2\pi R_t(C_i+C_t)} \tag{4.10}$$

$$f_{z\beta} = \frac{1}{2\pi R_tC_t} \tag{4.11}$$

The pole $f_{p\beta}$ is now slightly shifted to lower frequencies due to the additional capacitor C_t. But in many applications the capacitor C_t can be neglected compared to the photodiode capacitance C_i.

Now the compensation capacitor C_t must be dimensioned for proper circuit stability. As mentioned before, the zero $f_{z\beta}$ should be located at the critical frequency f_i, at the intersection of $A_0(s) = \beta^{-1}(s)$. The estimated phase margin at this frequency sums up to -180° (inverting amplifier) - 90° ($A_0(s)$) - 90° (pole $f_{p\beta}$) + 45° (zero at $f_{z\beta} = f_i$). This gives a total TIA phase margin of 45° [33]. With the following estimation

$$A_0(s) \approx \frac{f_t}{f} \quad \text{and} \quad \beta^{-1}(s) \approx \frac{f}{f_{p\beta}} \tag{4.12}$$

the frequency f_i can be calculated as

$$\frac{f_t}{f_i} = \frac{f_i}{f_{p\beta}} \quad \text{which gives}$$

$$f_i = \sqrt{f_{p\beta} f_t} = \sqrt{\frac{f_t}{2\pi R_t (C_i + C_t)}} \tag{4.13}$$

For the calculation of C_t the mentioned constraints can now be used

$$f_{z\beta} = f_i \quad \text{or} \quad \frac{1}{2\pi R_t C_t} = \sqrt{\frac{f_t}{2\pi R_t (C_i + C_t)}} \tag{4.14}$$

Solving Equation (4.14) gives a quadratic relation for C_t

$$2\pi R_t f_t C_t^2 - C_t - C_i = 0 \tag{4.15}$$

Out of Equation (4.15) two solutions can be calculated. The first approximated solution is valid, if the photodiode capacitance C_i is much larger than the compensation capacitor C_t. This simplifies the solution to

$$C_t \approx \sqrt{\frac{C_i}{2\pi R_t f_t}} \tag{4.16}$$

The exact, but more complex solution of Equation (4.15) can be used, if the approximation $C_i \gg C_t$ is not valid.

$$C_t = \frac{1 + \sqrt{1 + 8\pi R_t C_i f_t}}{4\pi R_t f_t} \tag{4.17}$$

Equations (4.16) and (4.17) are estimations for the compensation capacitor C_t. These equations assume a phase margin of 45° for the closed-loop TIA transfer function, which means a gain peaking of 2.4 dB at frequency f_i. Therefore this circuit is slightly undercompensated, compared to an optimum flat transfer function, which means a phase margin of about 69°. Nevertheless this estimation is feasible, since TIA bandwidth has to be optimized as much as possible for most applications. An overcompensation with capacitor C_t also reduces the TIA bandwidth dramatically. With the assumed phase margin of 45° and a gain peaking of 2.4 dB, the TIA's -3 dB bandwidth frequency is increased to

$$f_{BW,TIA} = 1.4 f_i = 1.4 \sqrt{\frac{f_t}{2\pi R_t (C_i + C_t)}} \tag{4.18}$$

The presented relations for C_t (Equations (4.16) and (4.17)) and for the TIA bandwidth $f_{BW,TIA}$ (Equation (4.18)) are simplified estimations and only valid, if there are no additional poles and zeros near the intersection frequency f_i. Nevertheless these methods provide an easy-to-use TIA design guideline for bandwidth and stability optimization.

4.4 TIA Noise

The noise performance of opto electronic receiver circuits is a key design parameter, since it is directly related to the receivers sensitivity and also to the bit-error rate (BER). The BER defines the number of corrupted bits in a data-stream, divided by the total number of bits. A typical BER requested in serial data links is 10^{-12}. To achieve a high BER, the ratio of receivers peak-to-peak output voltage $v_{r,pp}$ to integrated RMS output noise voltage $\overline{v}_{n,out}$ must be as high as possible. The reason for this is, that usually the receiver output pins are connected to a decision circuit (comparator) with a certain threshold, that determines if a bit is a zero or a one (see Figure (4.5)). With a high receiver output noise voltage, the probability for a threshold violation (and therefore a wrong decision) increases significantly. For a BER of 10^{-12}, a ratio of $v_{r,pp}/\overline{v}_{n,out} = 14$ is necessary. If the ratio decreases to $v_{r,pp}/\overline{v}_{n,out} = 7$, the BER is already below 10^{-4} [34]. Looking on this from the other way round, for a receiver with bad noise performance, the signal amplitude must be very high, to achieve a certain BER. This requires a high receiver gain and photodiode sensitivity, which results on the other hand in lower speed performance. As a conclusion, the noise performance must be optimized for competitive optical receivers.

4.4.1 Input-Referred Noise in Optical Receiver Circuits

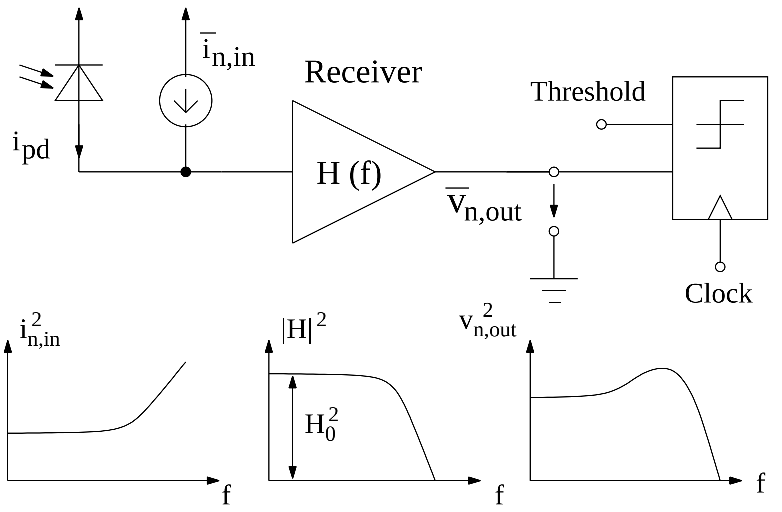


Figure 4.5: Receiver block diagram with input refered noise current source $i_{n,rms}$ and receiver output noise voltage $v_{n,rms}$. The bottom graphs show the sprectral behavior of the input and output noise due to the receiver transfer function H(f).

For a typical receiver circuit, the main noise sources are the photodetector noise and, even more important, the TIA noise. This means, that the TIA circuit more or less determines the optical receivers sensitivity and noise performance. Therefore, in this section a detailed TIA noise analysis will be presented. But lets start with a general view on the noise behavior of a receiver circuit. Figure (4.5) shows a basic block diagram including photodiode, receiver and digital decision circuit [34]. The receiver has a complex transfer function $H(f)$ that relates the output voltage to the input current i_{pd}. The decision circuit works as comparator which compares the receiver output voltage with a threshold voltage and is latched with a clock signal. All receiver noise sources including photodiode noise can be translated to a single input referred noise current source $\overline{i}_{n,in}$ connected to a noiseless receiver. This input noise current $\overline{i}_{n,in}$ generates the same output noise voltage $\overline{v}_{n,out}$ as all noise sources in the receiver circuit. The left-hand bottom graph in Figure (4.5) shows an example for an input referred power spectrum $i^2_{n,in}(f)$ of the receiver noise. As it will be shown later, the $i^2_{n,in}(f)$ increases with frequency due to a f^2 component of the input referred noise current. This input noise current is filtered by the receiver transfer function $H(f)$ and results in a frequency bounded output noise voltage power spectrum $v^2_{n,out}(f)$. The total RMS receiver output noise voltage $\overline{v}_{n,out}$ can now be calculated with

$$\overline{v}_{n,out} = \sqrt{\int_0^\infty |H(f)|^2 \, i^2_{n,in}(f) \, df} \tag{4.19}$$

by integration of the shaped spectral input noise current $i^2_{n,in}(f)$. An integration up to ∞ is actually not necessary, since the roll-off due to $H(f)$ is very step.

On the other hand, the total input referred RMS noise current $\overline{i}_{n,in}$ is an important factor for receiver sensitivity. It can be calculated by $\overline{i}_{n,in} = \overline{v}_{n,out}/H_0$ where H_0 is the receiver DC-gain in the transfer function $H(f)$. Therefore $\overline{i}_{n,in}$ can be calculated from the spectral input referred noise current $i_{n,in}(f)$ by

$$\overline{i}_{n,in} = \frac{1}{H_0}\sqrt{\int_0^\infty |H(f)|^2 \, i^2_{n,in}(f) \, df} \tag{4.20}$$

Since the analytical solution of Equation (4.20) is not straight forward, we will look for an estimation of Equation (4.20), that can be used during circuit design phase. As it will be shown later in Equations (4.30) and (4.31), the input referred noise spectrum can be written in a very general form as

$$i^2_{n,in}(f) = A + B \cdot f^2 \tag{4.21}$$

The noise current contains a constant factor A and a f^2 dependent part B. An 1/f dependent noise part, coming from MOS-transistor input stages, is neglected in this equation. By inserting the Equation (4.21) into Equation (4.20), we get a relation

$$\overline{i}_{n,in} = \sqrt{A \cdot BW_n + B \cdot BW^3_{n2}} \tag{4.22}$$

with

$$BW_n \;=\; \frac{1}{H_0^2}\int_0^\infty |H(f)|^2 \, df \tag{4.23}$$

$$BW_{n2}^3 = \frac{1}{H_0^2}\int_0^\infty |H(f)|^2 \cdot f^2\, df \qquad (4.24)$$

The bandwidths BW_n and BW_{n2}^3 are only dependent on the receiver transfer function $H(f)$. They are also known in the literature as Personick Integrals [34, 35]. Table (4.1) shows numeric values for BW_n and BW_{n2} for different basic receiver transfer functions $H(f)$. The values of BW_n and BW_{n2} from the table can now be used together with Equation (4.22) to calculate the total RMS input referred noise current $\bar{i}_{n,in}$ for different receiver transfer characteristics.

H(f)	BW_n	BW_{n2}
1^{st}-order lowpass	$1.57\cdot BW_{3dB}$	∞
2^{nd}-order lowpass, real (Q=0.5)	$1.22\cdot BW_{3dB}$	$2.07\cdot BW_{3dB}$
2^{nd}-order lowpass, Bessel (Q=0.577)	$1.15\cdot BW_{3dB}$	$1.78\cdot BW_{3dB}$
2^{nd}-order lowpass, Butterworth (Q=0.707)	$1.11\cdot BW_{3dB}$	$1.49\cdot BW_{3dB}$

Table 4.1: numeric values for BW_n and BW_{n2} for different transfer functions $H(f)$ [34]

4.4.2 TIA Noise Analysis

In previous section we pointed out that the input referred noise current has a big impact on the receivers sensitivity. In particular the photodiode and the receiver input stage are the main contributors to receiver noise. In most applications, the input stage is a transimpedance amplifier (TIA). Therefore we will investigate the TIA noise performance in more detail. In Figure (4.6) the main noise sources of a TIA are shown.

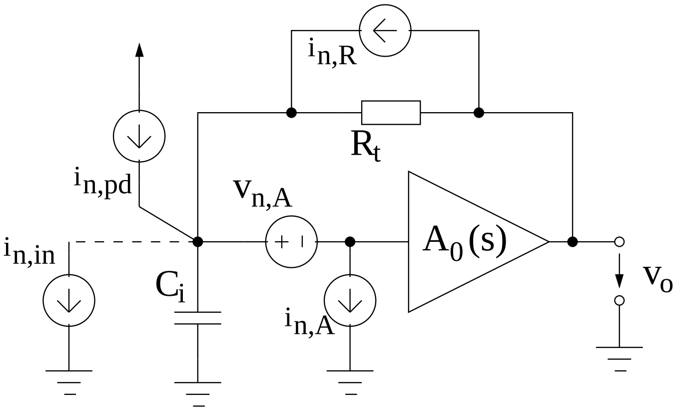


Figure 4.6: TIA block diagram with equialent noise sources included.

The photodiode shot noise can be modeled by a current source $i_{n,pd}$, directly connected to the input node. The TIA noise can be specified by mainly three noise sources. On one hand, the noise of transimpedance resistor R_t can be expressed by a current source $i_{n,R}$ in parallel. On the other hand, all amplifier noise sources can be mapped to a noise current source $i_{n,A}$ and noise voltage source $v_{n,A}$ at the amplifier input. All these noise sources can be converted to a single input referred current source $i_{n,in}$. This leads to following equations

$$\begin{aligned} \frac{i^2_{n,in}}{df} &= i^2_{n,pd} + i^2_{n,R} + \frac{v^2_{n,A}(1+sR_tC_i)^2}{R_t^2} + i^2_{n,A} \\ \Rightarrow \frac{i^2_{n,in}}{df} &= 2qI_{pd} + \frac{4kT}{R_t} + \frac{v^2_{n,A}(1+sR_tC_i)^2}{R_t^2} + i^2_{n,A} \qquad (4.25) \end{aligned}$$

Equation (4.25) shows the input referred noise current power density, with f is the frequency. The photodiode shot noise $i^2_{n,pd} = 2qI_{pd}$ with $q = 1.6 \times 10^{-19}$As is proportional to the photodiode current I_{pd}. The thermal noise of the resistor R_t is defined by $4kT/R_t$. The amplifier noise voltage $v_{n,A}$ is converted to a current by the impedance of the input node, given by C_i and R_t and the amplifier noise current $i_{n,A}$ directly contributes to the input referred noise current.

As next step we will compare the noise performance of a TIA input stage, designed with MOS-transistors on one hand and with bipolar transistors on the other hand. A simplified schematic is shown in Figure (4.7). As an example a common source (common emitter) stage is used at the TIA input with a DC bias current I_D (I_C).

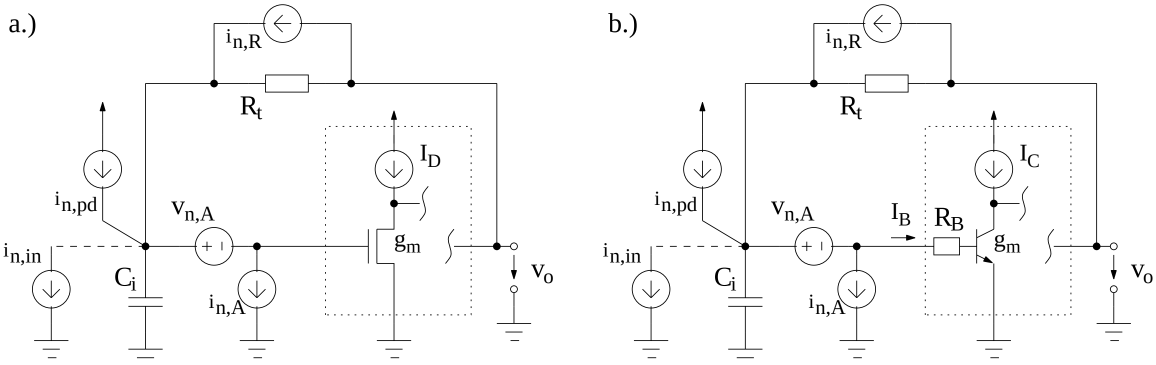


Figure 4.7: Noise sources of a TIA circuit with MOS input stage (a) and bipolar input stage (b).

Looking on a MOS transistor (see Figure (4.7 a.)), the input referred noise voltage source shown in Equation (4.26), mainly consists of two parts. The first part is the thermal channel noise due to drain current I_D that is transferred to an input voltage $v_{n,A}$ via transconductance g_m. A second noise source is the 1/f dependent flicker noise, which is significant for low frequencies up to few MHz. It is proportional to a constant K and the drain current I_D. For high frequency applications, the 1/f-noise can be neglected. The TIA input referred current noise $i_{n,A}$ can be neglected for MOS transistors (see Equation (4.27)).

$$\frac{v_{n,A}^2}{df}_{MOS} = \underbrace{4kT\frac{2}{3}\frac{1}{g_m}}_{Thermalnoise} + \underbrace{K\frac{I_d}{f}}_{Flickernoise} \tag{4.26}$$

$$\frac{i_{n,A}^2}{df}_{MOS} \approx 0 \tag{4.27}$$

The input referred noise voltage and current sources for a BIP transistor input stage (see Figure (4.7 b.)), are shown in Equations (4.28) and (4.29). The input referred noise voltage $v_{n,A}$ is defined by the thermal noise of the base resistance r_B on one hand and the shot noise of the current I_C flowing through the collector pn-junction and transferred to an input voltage via g_m on the other hand. The shot noise part can be simplified by the relations $g_m = I_C/V_t$ with thermal voltage $V_t = kT/q$. The input referred current noise source $i_{n,A}$ is mainly defined by the base current shot noise, while the 1/f flicker noise can be neglected.

$$\frac{v_{n,A}^2}{df}_{BIP} = \underbrace{4kTr_B}_{Thermalnoise} + \underbrace{\frac{2qI_c}{g_m^2}}_{Shotnoise} = 4kT\left(r_B + \frac{1}{2g_m}\right) \tag{4.28}$$

$$\frac{i_{n,A}^2}{df}_{BIP} = 2qI_B \tag{4.29}$$

Equations (4.30) and (4.31) represent the input referred spectral noise current $i_{n,in}$ for MOS transistors and BIP transistors by substituting the terms of Equation (4.25) with (4.26), (4.27) and (4.28) as well (4.29) respectively. For both transistors, the noise current can be split into one frequency independent factor and a second term, that shows a f^2 frequency dependence.

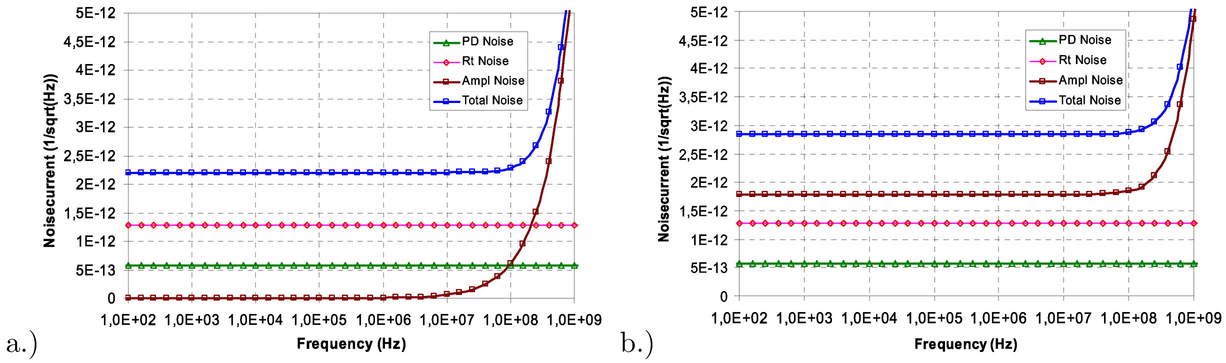
$$\frac{i_{n,in}^2}{df}_{MOS} = 2qI_{pd} + \frac{4kT}{R_t} + \frac{32kT\pi^2 C_i^2 f^2}{3g_m} \tag{4.30}$$

$$\frac{i_{n,in}^2}{df}_{BIP} = 2qI_{pd} + \frac{4kT}{R_t} + \frac{16kT\pi^2\left(r_B + \frac{1}{2g_m}\right)C_i^2 f^2}{3g_m} + 2qI_B \tag{4.31}$$

As an example, Figure (4.8) shows the different components of the spectral noise behavior for a TIA with MOS transistor input in comparison to a TIA with BIP transistor input. This calculation was done with following parameters:

- Photodiode current $I_{pd} = 1\mu A$

- Transimpedance resistor $R_t = 10k\Omega$
- Input capacitance $C_i = 500fF$
- BIP base resistance $r_B = 100\Omega$
- BIP base current $i_B = 100\mu A$ (which means a current gain $\beta \approx 50$)
- Transconductance of MOS transistor $g_{m,MOS} = 3 \cdot 10^{-3} A/V$ (assuming a drain current $I_D = 500\mu A$, a MOS gain factor $K' = 80\mu A$ and a $W/L = 100$)
- Transconductance of BIP transistor $g_{m,BIP} = 2 \cdot 10^{-2} A/V$ (assuming a collector current $I_C = 500\mu A$)



a.) b.)

$$\frac{i^2_{n,in}}{df}_{MOS} = \overbrace{2qI_{pd}}^{PDnoise} + \overbrace{\frac{4kT}{R_t}}^{Rtnoise} + \underbrace{\overbrace{\frac{32kT\pi^2C_i^2f^2}{3g_m}}^{AmplNoise}}_{\downarrow withI_d}$$

$$\frac{i^2_{n,in}}{df}_{BIP} = \overbrace{2qI_{pd}}^{PDnoise} + \overbrace{\frac{4kT}{R_t}}^{Rtnoise} + \overbrace{\underbrace{\frac{16kT\pi^2\left(r_B+\frac{1}{2g_m}\right)C_i^2f^2}{3g_m}}_{\downarrow withI_C} + \underbrace{2qI_B}_{\uparrow withI_C}}^{AmplNoise}$$

Figure 4.8: Spectral noise behavior for a TIA with MOS transistor input (a.) and BIP transistor input (b.). The total noise is splitted into photodiode noise (PD noise), R_t resistor noise and amplifier noise.

The graphs in Figure (4.8) show, that for the same drain/collector current of $500\mu A$, the total noise values are similar. Due to the base current noise, the BIP transistor noise is slightly higher. For low noise applications, the g_m of a MOS amplifier and therefore the drain current I_D should be as high as possible. For a TIA with BIP input stage, a high g_m also decreases the noise at high frequencies. But for the low frequency range, the noise even increases with a high collector current (high g_m), due to the higher base current. For noise optimization, a BIP TIA needs therefore a low base resistance r_B, high g_m and a high current gain β to reduce the base current I_B.

4.5 TIA Realization Examples

In the previous section, we discussed basic TIA properties like bandwidth, stability and noise. To show how the discussed TIA structures can be implemented in real circuit topologies, different state of the art TIA implementations will be shown in the following section. All presented circuits are dedicated to broadband applications in the field of optical data communication and optical data storage. The main focus on these kind of circuits is on high bandwidth in combination with low noise performance. The circuits are designed in either pure CMOS or BiCMOS technologies.

4.5.1 Single-Ended TIA

The circuit shown in Figure (4.9) presents a TIA, realized in a BiCMOS technology [36]. The single ended TIA input stage mainly consists of a common-emitter amplifier with transistor Q_4. To increase the input resistance of the circuit, a Darlington configuration of transistor Q_1 and Q_4 is used. The photodiode is directly connected to the input node. The TIA output voltage is buffered with an emitter follower Q_3. The transimpedance resistor R_t is connected from the TIA output to the input node. For stability reasons, a capacitor C_t is in parallel to R_t (as described in previous section). A small resistor in the emitter path of Q_4 is implemented to improve the noise performance. At the TIA output node a differential amplifier with Q_6, Q_7 is connected to convert the single-ended signal to a differential output A, B. Preferably the second differential amplifier input V_{ref} can be connected to a properly matched replica of the TIA circuit. Nevertheless the output offset voltage is an issue with this kind of circuit implementation. The gain linearity of the output differential pair is improved with two emitter degeneration resistors. With this circuit a good noise performance with medium bandwidths up to 128 MHz was achieved. Additionally the transimpedance gain was programmable in the range from R_t <100Ω up to 100kΩ as presented in [36].

Another single-ended TIA implementation is shown in Figure (4.10) [37]. As the previous circuit, this is implemented in a BiCMOS technology. Instead of using a common-emitter amplifier, this circuit uses a common-base input stage, defined by transistor Q_1. The output of the common-base amplifier is connected to the actual TIA input. This is (as before) a common-emitter stage, using the MOS transistor M_1 as amplifier, the BIP transistor Q_2 and Q_3 as output buffers and the resistor R_t as transimpedance. The main advantage of this circuit is, that the capacitance of the input node is decoupled from the TIA input by the common-base stage. Therefore the TIA bandwidth can be optimized, since it is independent from the photodiode capacitance, which can be large and vary for different applications. Compared to the realization in Figure (4.9), this circuit shows an improved speed performance. On the other hand, the common-base input stage is an

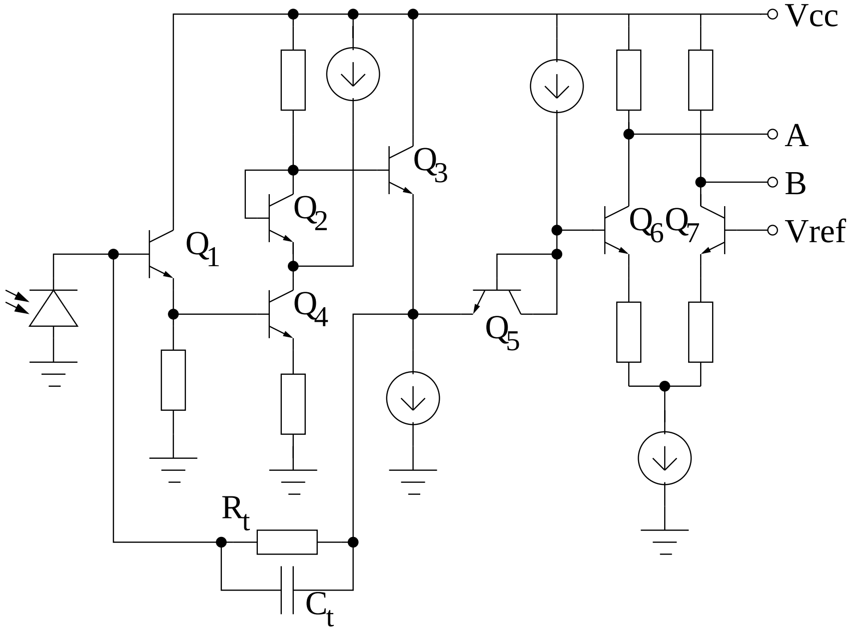


Figure 4.9: Single-ended TIA circuit with common-emitter Darlington input stage.

additional significant noise source, which is the main drawback of this circuit. Also the current consumption of this architecture will be higher, due to the additional input stage.

The circuit shown in Figure (4.11) is a single-ended TIA in pure CMOS technology, which means a low-cost implementation [38]. In difference to the solutions presented before, this circuit uses a 3-stage amplifier to achieve the necessary gain. The output of the 3^{rd} stage is connected to the TIA input via the transimpedance resistor R_t. Every one of the three amplifier stages consists of 3 MOS transistors (like the first stage are M_1, M_2 and M_3). The gain of every stage is defined by the transconductances of the three transistors, as for the first stage $A_1 = (g_{m,M1} + g_{m,M3})/g_{m,M2}$. This equation shows, that the gain is given by a g_m ratio, and is therefore mostly defined by transistor matching. A significant advantage of this circuit is the high amplifier gain, which means also a high TIA bandwidth according to Equation (4.4). In reference [38] a transimpedance-bandwidth product of 18 THzΩ was reported. Another advantage is the low supply voltage the circuit needs. The main disadvantage of this circuit is the sensitivity to power supply noise. Another critical design issue is the stability behavior due to the multi-stage amplifier feedback.

The TIA shown in Figure (4.12) is a single-ended TIA, with a differential input stage [39]. The differential pair Q_1, Q_2 is connected to the photodiode on one side and to a biasing reference voltage V_{ref} on the other side. The TIA output is buffered with an emitter-follower Q_5. The transimpedance resistor is R_t with a compensation capacitor C_t. The base current of the BIP transistor Q_1 always creates an output offset voltage, which can vary over a wide range. To avoid this offset, a compensation circuit is implemented, which is adding the base current into the input node, by mirroring a replica current. This is

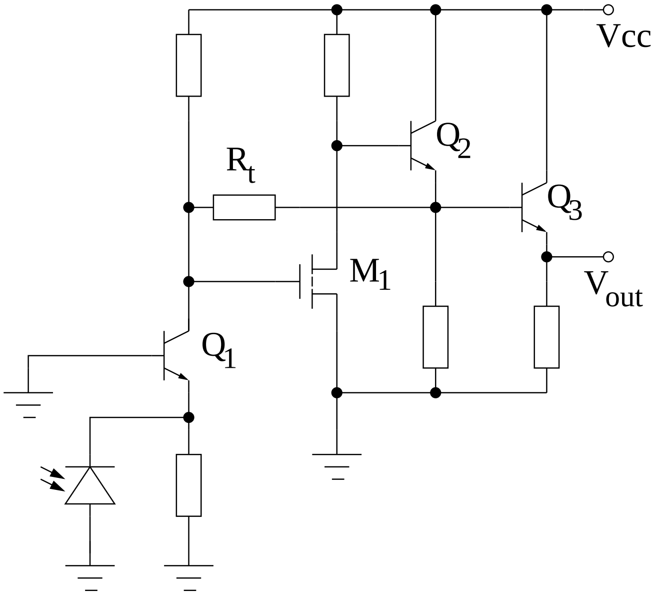


Figure 4.10: Single-ended TIA circuit with common-base input stage.

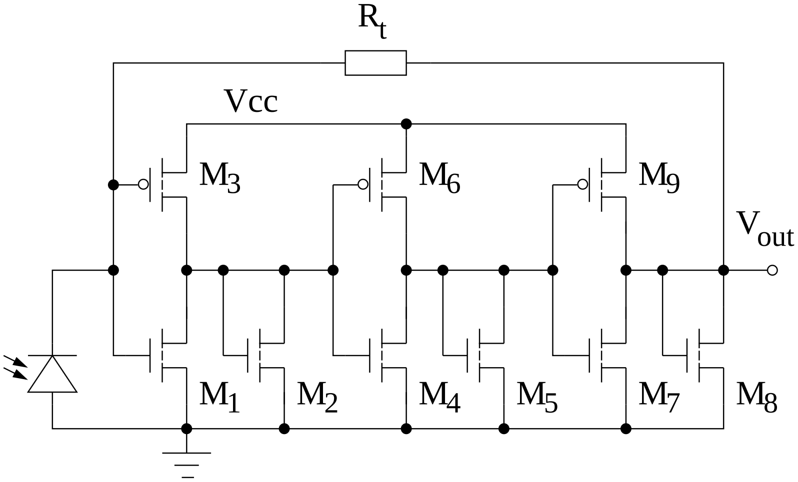


Figure 4.11: Single-ended CMOS multi-stage TIA circuit.

coming from dummy transistors Q_3 and Q_4 which have the same collector current as the main transistors Q_1, Q_2. Nevertheless this compensation can remove the offset error only partially, since it relies on the β-matching of BIP transistors, which is not well defined.

4.5.2 Differential TIA

All presented circuits up to now, were single-ended TIAs. On one hand this is convenient due to the photodiode, which in general can only provide a single-ended current signal. On the other hand, a TIA with differential output would be preferable since it is less sensitive to cross-talk and power supply noise which would mean a significant advantage. Figure (4.13) shows basic topologies, how the single-ended photodiode input current can

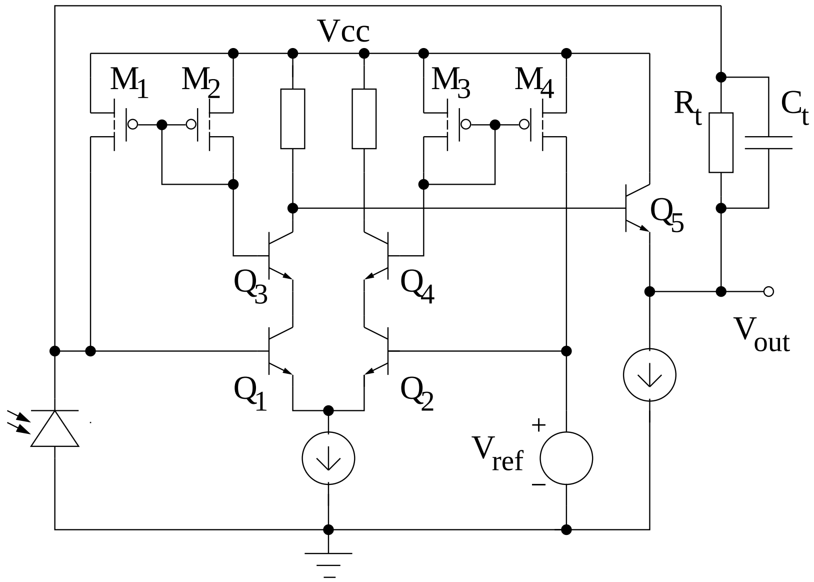


Figure 4.12: Single ended TIA circuit in BiCMOS technology with differential input stage and base current compensation.

be converted to a differential output voltage. Figure (4.13 a.) shows a standard single ended TIA with a reference voltage V_{cm} that defines the common-mode level. Since the input signal is only single ended, for a fully differential amplifier the second input must be connected properly. Figures (4.13 b.) and (4.13 c.) show two different possibilities for realizing a differential TIA. The first possibility is to connect a large capacitor C_r to the second input pin, as shown in Figure (4.13 b.) (ideally the capacitor should be ∞). For AC signals this means a ground connection like using a constant voltage source. The output common-mode voltage is defined by a reference voltage source V_{cm}. The circuit will more or less behave like a standard single-ended TIA. The differential transimpedance gain for this configuration is two times the feedback resistor. In Figure (4.13) the gain (differential and single-ended) of all three circuits is equivalent. Therefore in version (4.13 b.) the feedback resistor is drawn as $R_t/2$. Unfortunately the power-supply rejection ratio (PSRR) of version b.) is the same as for a single-ended TIA. Summarizing there is no significant advantage of the differential amplifier version b.), compared to a single-ended TIA. The second possibility for realizing a fully differential TIA is shown in Figure (4.13 c.). There the capacitance C_r is matched to the photodiode capacitance. This makes the circuit fully symmetrical which means a significantly optimized PSRR. On the other hand, the differential transimpedance gain is as high as one single feedback resistor R_t. This means a gain loss of two compared to a single-ended TIA, if using the same number for the sum of the two feedback resistors. Another significant disadvantage for the differential solutions compared to the single-ended TIA is the noise performance. Comparing the noise of the three circuits in Figure (4.13) it turns out, that the single-ended solution has the best noise performance for the same single-ended and differential gain. According to Equation (4.25) the spectral noise of the feedback resistor R_t is $i_{n,Rt} = \sqrt{4kt/R_t}$. Comparing the noise performance of the two differential circuits, we can see that for version (4.13 b.) only one of the two feedback resistors contributes to the noise. This is because the high capacitance is shorting out the noise for the second feedback resistor. But since the value of one feedback resistor is only $R_t/2$, the resistor noise contribution for this circuit is $\sqrt{2}$ higher compared to a single-ended TIA. In the differential circuit of Figure (4.13c), both feedback resistors contribute to the noise current, due to the small capacitance value C_r. This means, that the feedback resistor noise current for this circuit is actually two times worse compared to a single-ended TIA. Taking all these considerations into account, the benefit of a differential TIA has to be analyzed carefully and strongly depends on the application.

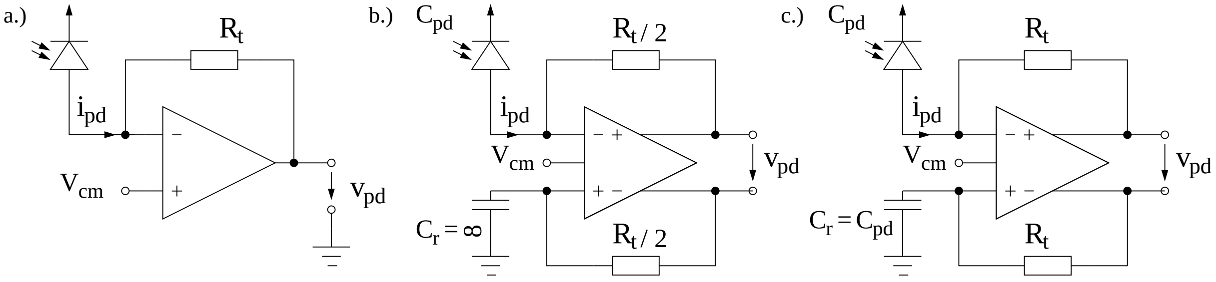


Figure 4.13: Comparison of single ended vs. differential TIA stage. Figure a.) shows a single-ended TIA, Figure b.) is an unbalanced and c.) is a fully balanced differential TIA.

An example for a differential TIA implementation is shown in Figure (4.14) [11]. The circuit is implemented in a BiCMOS technology. The differential pair is realized with the BIP transistors B_1 and B_2. The transimpedance is indicated as R_t. The capacitor C_r can either be matched to the photodiode or can be very large, as explained just before. The output pins are buffered with BIP transistors as emitter followers B_3 to B_6. High bandwidths up to 9 GHz with a transimpedance of 55 dBΩ were shown in [11] by using additionally shunt peaking techniques and filter termination at the TIA input.

4.5.3 Variable-Gain TIA

Most applications in the field of optical data storage and fiber communication requires a variable-gain TIA to cover the wide range of input light intensity. Looking to typical TIA implementations with a transimpedance amplifier at the input connected to the photodiode and a post amplifier as output stage implies two possibilities for gain variation. On one hand the transimpedance R_t of the TIA input stage can be tuned as shown in Figure (4.15a.) and on the other hand a variable gain voltage post amplifier (VGA) can be implemented after the TIA, as in Figure (4.15b.).

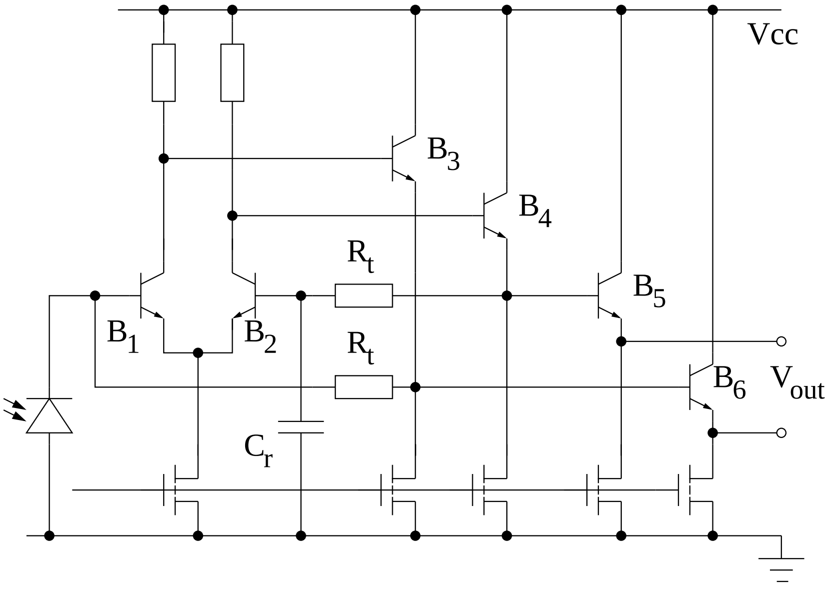


Figure 4.14: Differential TIA circuit in BiCMOS technology.

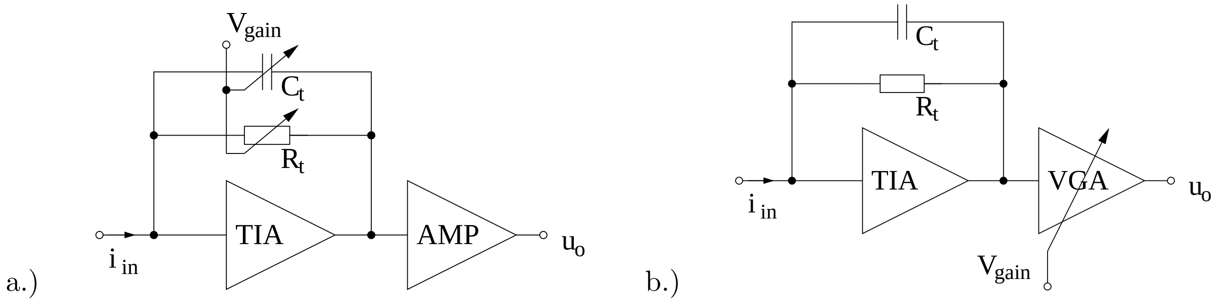
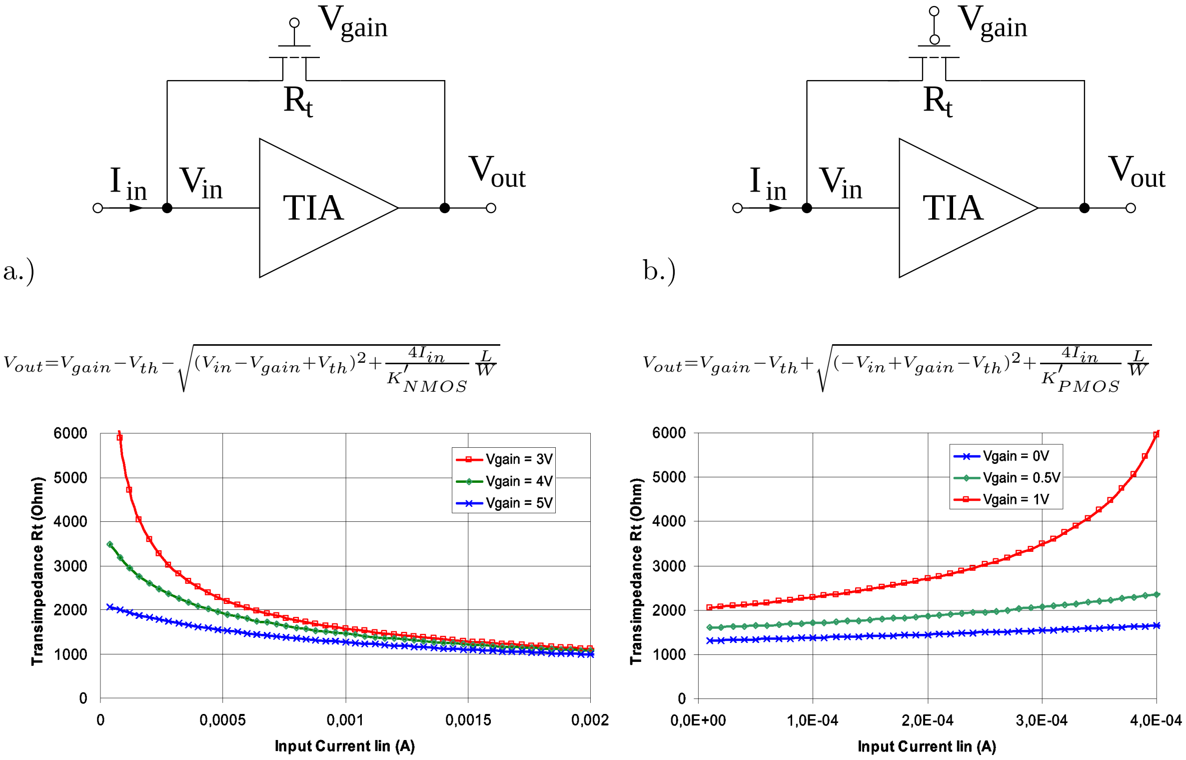


Figure 4.15: Variable-gain TIA implementations. Figure a.) shows a TIA with variable transimpedance R_t and Figure b.) a variable-gain voltage amplifier with a constant transimpedance TIA.

4.5.3.1 TIA with variable transimpedance

A variable transimpedance as in Figure (4.15 a.) has the advantage of a high input current overload level which means also a high dynamic range. The transimpedance R_t is tuned as high as possible (achieving required bandwidth), which means an optimum of noise performance. The disadvantage of version a.) is the direct variation of the signal path via TIA feedback R_t which is critical for stability and requires sophisticated control circuits for the compensation capacitor C_t. A simple implementation for a tunable transimpedance is a MOS transistor in the linear region as shown in Figure (4.16). It shows the TIA circuit with a NMOS transistor (a.) and a PMOS transistor (b.) as feedback resistor as well as the relation of the output voltage V_{out} as function of the input current I_{in} in dependence on gate voltage V_{gain}. The input voltage V_{in} is constant at 2 V. The transistor geometries are (W/L) = 5 for the NMOS and W/L) = 20 for the PMOS transistor.

The bottom graphs of Figure (4.16) show the transimpedance value as function of the input current I_{in} for different V_{gain} settings. The photodiode current is flowing into the TIA. Both graphs show a strong dependence on R_t on the input current. For the NMOS transistor the transimpedance is strongly non-linear for small input currents and R_t decreases for higher currents. The reason is, that for a NMOS the R_t mainly depends on $1/g_m$ which is decreasing for higher drain-source currents. Therefore a NMOS is acting as limiting amplifier since gain compression occurs for high input currents. A PMOS transistor in the TIA feedback path (b.) shows the opposite behavior. The transimpedance increases with higher input current. The reason is that R_t mainly depends on $1/g_{ds}$ which is increasing for high drain-source currents. So the PMOS transimpedance shows a lower dynamic range. A critical issue for both circuits is stability, since the transimpedance is strongly non-linear. For practical applications a gain control circuit for V_{gain} is necessary.



$$V_{out}=V_{gain}-V_{th}-\sqrt{(V_{in}-V_{gain}+V_{th})^2+\frac{4I_{in}}{K'_{NMOS}}\frac{L}{W}}$$

$$V_{out}=V_{gain}-V_{th}+\sqrt{(-V_{in}+V_{gain}-V_{th})^2+\frac{4I_{in}}{K'_{PMOS}}\frac{L}{W}}$$

Figure 4.16: TIA with variable transimpedance R_t using a NMOS transistor (W/L)=5 (a.) and a PMOS transistor (W/L)=20 (b.) with input voltage V_{in}=2V.

4.5.3.2 TIA with variable-gain post amplifier

A VGA circuit as post amplifier as shown in Figure (4.15 b.) is widely used in receiver architectures. Several circuits are well suited for this application enabling a continuous gain variation over a wide gain range without switching of signal paths or feedback. But this architecture does not provide a noise optimum. It also has a low input dynamic range, since the TIA circuit has a fixed (not optimized) gain.

One of the most famous VGA circuits is a Cherry-Hooper stage [40, 41, 42, 10] combined with a four-quadrant mixer (Gilbert cell) [43] as shown in Figure (4.17). The Cherry-Hooper stage is built up as differential pair with emitter degeneration resistors R_e (bottom of Figure (4.17)) and a transimpedance amplifier (top of Figure (4.17)). Between these two building blocks of the Cherry-Hooper stage, a 4-quadrant current mixer also called Gilbert cell is implemented for gain tuning. With the gain control voltage of the current mixer, the amplifier gain can be tuned continuously between 0 (V_{gain}=0) and a maximum gain value of R_t/R_e for a high V_{gain}. V_{gain} must always be positive, since the signal is inverted for the other polarity, which means instability of the amplifier. Since only 2 quadrants of the Gilbert cell are used for gain tuning, a simple current divider can be used instead. Unfortunately the common-mode output current is then varying with gain setting, which makes an offset control circuit necessary.

The bandwidth of this circuit is high, since the emitter degeneration reduces the input capacitance and therefore increases the frequency of input pole of the differential pair. Furthermore the capacitor C_e, which is in parallel to the emitter resistors R_e, introduces a zero for high frequency boosting. Also the transimpedance amplifier (TIA) speeds up the circuit bandwidth, because of the low impedance of the TIA input node, as explained in Equation (4.6). To increase the amplifier driving strength, the TIA output nodes V_{out} must be buffered accordingly (not shown in Figure (4.17)).

All discussed variable-gain TIA circuit implementations use a TIA input stage directly connected to the photodiode. Several advantages and disadvantages were discussed within this section. An alternative TIA architecture with a current amplifier as TIA input stage will be discussed in next section. This alternative circuit architecture overcomes most of the discussed issues.

4.5.4 TIA with Current Pre-Amplifier (ITIA)

For optical data storage applications there is a strong demand for high-bandwidth and low-noise transimpedance amplifier circuits. Due to the broad variety of operating conditions (CD, DVD, Blu-ray, read, write, single or double layer disc...) the transimpedance amplifiers must be programmable over a wide range of gains. The input light intensity for such applications can vary over several orders of magnitude, from below 1 μW for Blu-ray read, up to 30 mW for CD write applications. Therefore the TIA must be programmable over a wide range of gains.

We used an alternative architecture to classical variable gain TIA's (presented in previous section), that combines a TIA with a variable gain input current preamplifier (ITIA)

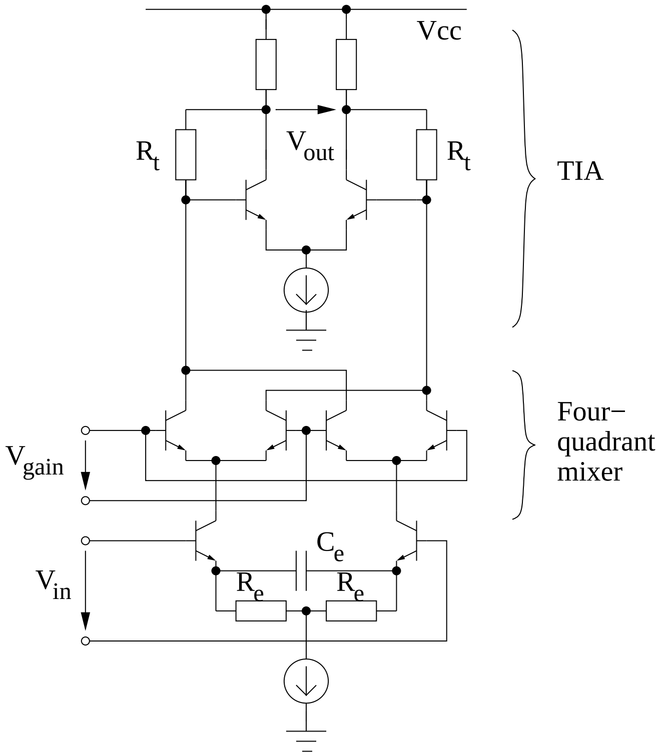


Figure 4.17: Variable gain amplifier. Cherry-Hooper stage combined with a four-quadrant current mixer.

as shown in Figure (4.18)). This architecture allows a continuous variable gain over a wide range in combination with high-speed and low-noise performance. Since the gain is programmed already in the input stage, the circuit has a high input dynamic range. The TIA circuit as output stage of the ITIA is a classical implementation with or without a programmable gain.

In this section we will introduce circuit implementations for a variable gain current amplifier. A circuit stability and bandwidth analysis and a comparison to a standard TIA concerning noise performance will be presented.

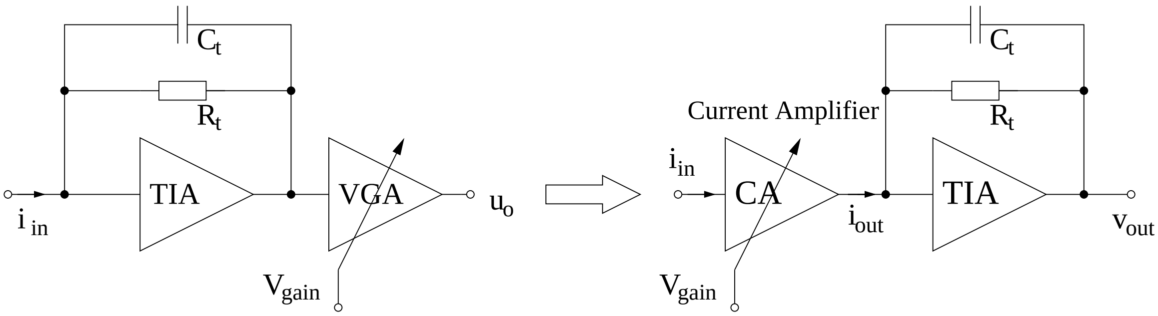


Figure 4.18: Classical TIA with post variable gain amplifier on left hand side, compared to an ITIA with variable gain current amplifer as input stage on right hand side.

4.5.4.1 Current amplifier implementation

The most simple current amplifier is a current mirror structure. A MOS current mirror is shown in Figure (4.19). A lot of different implementations are discussed in books for analog circuit design [44, 45].

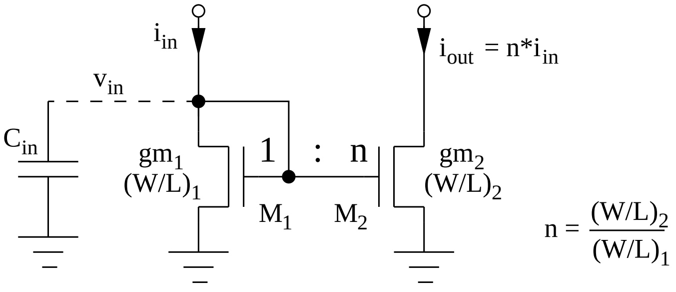


Figure 4.19: Classical current mirror with a current amplification of $n = (W/L)_2/(W/L)_1$.

The current gain of a MOS current mirror circuit is defined by the ratio of the transistor geometries

$$\frac{i_{out}}{i_{in}} = \frac{(W/L)_2}{(W/L)_1} \tag{4.32}$$

neglecting the output impedance of transistor M_2. The current gain of a BIP transistor mirror is given by the ratio of emitter areas of the two mirror transistors. An additional error source of BIP mirrors is the transistor base current. Another way to make the gain of a current mirror programmable, is to use source (emitter) degeneration resistors. Therefore the gain is approximately defined by a resistor ratio. The disadvantages are a smaller dynamic range due to the resistor voltage drop and the additional resistor noise source degrading the sensitivity.

To implement a variable gain amplifier by using standard current mirrors, switches has to be implemented that adds or remove additional transistors (or resistors) within the current mirror. Therefore a variable gain is not really applicable.

The speed performance of a current mirror is defined by a pole at the current mirror input node v_{in} which is given by the transconductance of transistor M_1 and the capacitance of the input node C_{in}

$$f_p = \frac{g_{m1}}{2\pi C_{in}} \tag{4.33}$$

Since the capacitance of the input node is low, the current mirror can be operated up to high frequencies.

An alternative current amplifier structure is a regulated current mirror. A circuit implementation using BIP transistors is shown in Figure (4.20).

The current mirror is given by the BIP transistors T_1 and T_2. The emitters of T_1 and T_2 are regulated by an operational transconductance amplifier OTA. The input node dc-voltage of the current mirror v_{in} is defined by the voltage source V_{dc}. The amplifier gain

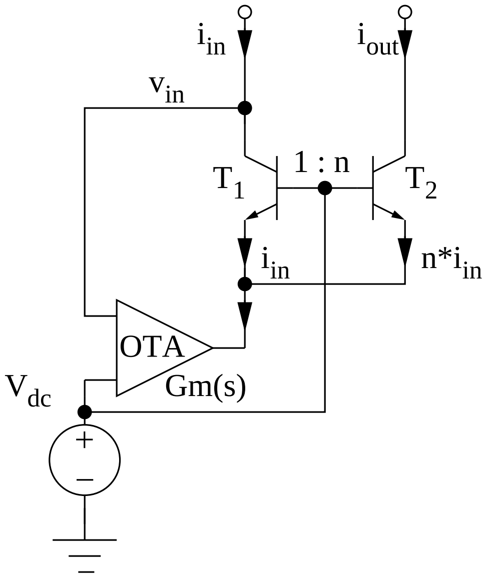


Figure 4.20: Current amplifier implemented as regulated current mirror.

is given by the ratio n of BIP emitter areas. The speed of this circuit is high and limited by the OTA speed. Like for a simple current mirror, the input pole is defined by the OTA transconductance Gm(s) according Equation (4.33).

4.5.4.2 Regulated current mirror stability

A critical issue with this kind of circuits is stability. The impedance of the amplifier input node v_{in} can be calculated as

$$\begin{aligned} v_{in} &\approx \frac{i_{in}+ni_{in}}{Gm(s)} \approx \frac{i_{in}(n+1)s}{\omega_T} \quad \text{with} \quad Gm(s) \approx \frac{\omega_T}{s} \\ \frac{v_{in}}{i_{in}} &\approx s\frac{n+1}{\omega_T} \end{aligned} \tag{4.34}$$

with ω_T is the OTA gain-bandwidth.

Equation (4.34) shows an inductive behavior of this regulated current mirror circuit. In combination with the parasitic capacitance at the input node, this gives an L-C tank which can lead to stability issues. The equivalent inductance is given by $L_{in} = (n+1)/\omega_T$. A simple estimation with an input capacitance (including photodiode) of C_{in}=1 pF, an amplifier gain n=10 and an OTA transit frequency of ω_T=10 GHz gives an inductance of L_{in}=1.1 nH. Together with the input capacitance this gives a resonance frequency of $f_r = 1/(2 * \pi\sqrt{L_{in} * C_{in}}) = 4.8\,\text{GHz}$. Therefore the resonance frequency might cause stability problems.

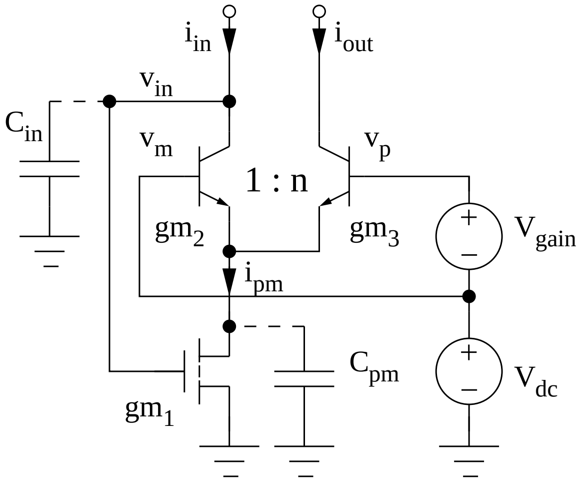


Figure 4.21: Implementation of a variable-gain regulated current mirror.

4.5.4.3 ITIA variable-gain current amplifier

In next paragraph we will present a variable gain regulated current mirror structure that can be used within an ITIA implementation. Figure (4.21) shows a more detailed circuit implementation of a regulated current mirror discussed before. The current mirror includes the bipolar NPN transistors T_1 and T_2 that are regulated with a n-MOS transistor as OTA. The OTA has a transconductance $g_{m1} = \frac{i_{pm}}{v_{in}}$ which regulates the input node to a defined and low-ohmic potential V_{in}. The current mirror gain n is the current ratio $n = \frac{i_{out}}{i_{in}}$. This current amplifier architecture has the advantage of a simple continuous gain adjustment with a variable voltage source $V_{gain} = V_p - V_m$. Compared to other solutions [46] no switching in the current signal path is necessary. The current gain n is defined by the Equation (4.35) where V_T is the thermal voltage of 26mV.

$$n = \frac{I_{out}}{I_{in}} = \exp\left(\frac{V_p - V_m}{V_T}\right). \tag{4.35}$$

The small-signal transfer function of the circuit is shown in Equation (4.36). The AC behavior is more or less defined by two poles P_1 and P_2 with P_1 is associated to the input node impedance at V_{in} and P_2 to the common emitter node of the current mirror. An approximation of the pole frequencies can be seen in Equation (4.37 and 4.38)

$$\frac{i_{out}}{i_{in}} \approx \frac{n}{1 + s\frac{C_{in}}{g_{m1}}(1+n) + s^2\frac{C_{pm}C_{in}}{g_{m1}g_{m2}}} \tag{4.36}$$

$$P_1 \approx \frac{g_{m1}}{C_{in}(n+1)} \tag{4.37}$$

$$P_2 \approx \frac{g_{m2}(n+1)}{C_{pm}} \tag{4.38}$$

For circuit stability the two poles have to be split away from each other. On the other hand both poles should be as high as possible for amplifier speed. To shift the P_1 to high frequencies the g_{m1} of the OTA can be increased to high values. The input capacitance C_{in} is more or less defined by the photodiode capacitance. The pole P_2 increases with g_{m2} of the current mirror NPN transistors and decreases with a high parasitic capacitance C_{pm} in the common emitter node. An additional input DC-current through the current mirror with NPN transistors T_2 and T_3 increases g_{m2} and g_{m3} and therefore shifts the pole P_2 to high frequencies. Higher values of amplifier gain n also splits the poles and increases stability. Dependent on the photodiode capacitance and the gain n one has to decide which pole P_1 or P_2 is the dominant and therefore the bandwidth limiting pole. For our application the pole P_1 is the dominant pole. So this current amplifier input stage can be optimized to even higher speed values compared to a classical TIA implementation with a resistive feedback amplifier as input stage. The bandwidth of a classical TIA input stage is approximately determined by the value of $A_0/R_t(C_t + C_{in})$ with A_0 is the TIA-amplifier gain, R_t is the transimpedance resistor connected to the input node and C_t is the compensation capacitor in parallel to R_t. As in our implementation the TIA is located in the output stage, the capacitances and the R_t can be minimized to achieve an overall higher bandwidth.

The noise performance of the circuit is dominated by the shot noise of the transistors T_2 and T_3. To minimize the input referred noise current, the input DC current $I_{in,dc}$ must be as low as possible. On the other hand the small-signal-bandwidth of the circuit depends on the transconductance g_{m1} of OTA transistor T_1 (see Figure (4.21)) and therefore decreases with lower $I_{in,dc}$ as mentioned before. This can be solved by applying a DC-current source connected to the drain of the NMOS-OTA T_1. Figure (4.22) shows the dominant noise sources of the ITIA variable gain current amplifier.

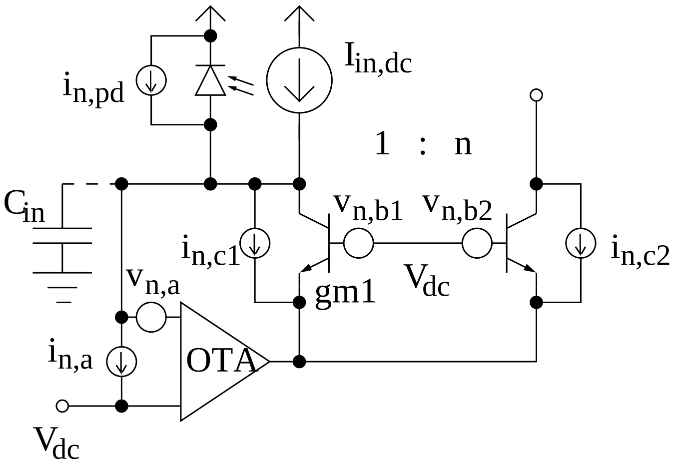


Figure 4.22: Noise sources of a variable-gain regulated current mirror.

Looking into more detail for the noise performance of our current amplifier ITIA architecture one can find that the noise can be reduced compared to a classical TIA implementation. In Equation (4.39) the input-referred noise current $i_{n,TIA}$ of a classical TIA is shown (see also Section 4.4.2)

$$\frac{i^2_{n,TIA}}{df} \approx 2qI_{in} + \frac{4kT}{R_t} + \frac{v^2_{n,A}(1+sR_tC_{in})^2}{R_t^2} + i^2_{n,A} \tag{4.39}$$

where $2qI_{in}$ is the photodiode shot noise, $4kT/R_t$ is the thermal noise of transimpedance resistor R_t, $v_{n,A}$ and $i_{n,A}$ are the amplifier input noise voltage and noise current. In Equation (4.40) the input referred noise current $i_{n,ITIA}$ of the current amplifier (Figure 4.22) is shown. $4qI_{in,dc}$ is the shot noise of transistors T_2 and T_3, r_B is the base resistance of transistor T_2 and T_3 and $v_{n,A}$ and $i_{n,A}$ are the OTA input referred noise voltage and noise current.

$$\begin{aligned}\frac{i^2_{n,ITIA}}{df} &\approx i^2_{n,pd} + i^2_{n,c1} + \frac{i^2_{n,c2}}{n} + (v^2_{n,b1} + v^2_{n,b1})gm_1^2 + v^2_{n,A}(sC_{in})^2 + i^2_{n,A} \\ \frac{i^2_{n,ITIA}}{df} &\approx 2qI_{in} + 4qI_{in,dc} + \frac{8q^2r_BI^2_{in,dc}}{kT} + v^2_{n,A}(sC_{in})^2 + i^2_{n,A} \qquad (4.40)\end{aligned}$$

Comparing Equations (4.39) and (4.40) the noise behavior is approximately the same except for a few terms as shown in Equation (4.41). Figure 4.23 shows a comparison of these different noise terms in dependence on transimpedance resistor R_t on one hand and different input DC-currents $I_{in,dc}$ on the other hand. These graphs demonstrate that for low $I_{in,dc}$ values the ITIA shows a better noise performance compared to a TIA input stage.

$$\underbrace{\sqrt{\frac{4kT}{R_t}}}_{TIA} \Longleftrightarrow \underbrace{\sqrt{4qI_{in,dc} + \frac{8q^2r_BI^2_{in,dc}}{kT}}}_{ITIA} \tag{4.41}$$

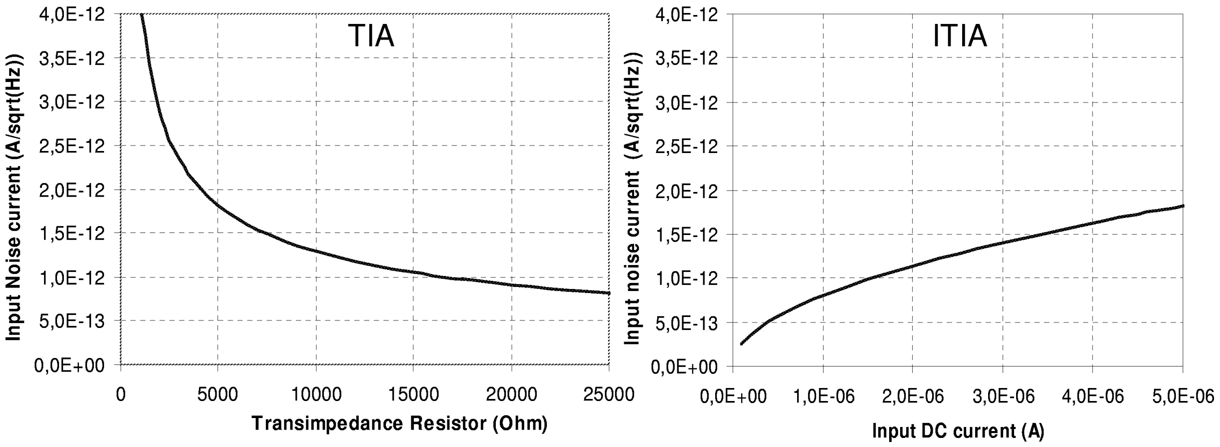


Figure 4.23: Comparison of significant ITIA input noise and standard TIA input noise terms.

4.6 Summary and Conclusion

For OEIC's in the field of optical data storage there is a strong demand for variable gain transimpedance amplifiers. These amplifiers should have a high bandwidth up to approximately 150 MHz but also low noise in combination with variable gain over a wide range of more than 3 decades. An example for such data storage OEIC will be presented in Chapter (5). We have shown within this section, that a TIA architecture with variable gain current amplifier input stage (ITIA) shows significant advantages to fulfill these requirements. It combines a high bandwidth with low noise and continuously variable gain.

Chapter 5

OEIC for CD/DVD/Blue-laser Optical-Data-Storage Applications

5.1 Introduction

The optical pickup unit (OPU) is a key component implemented in modern optical data storage systems like CD, DVD or future applications with blue laser light ("Blu-ray"). Figure (5.1) shows the basic optical setup for a pickup unit in Figure a.) and a photograph of a modern multi-standard optical pickup unit in b.) presented by Philips Semiconductors. The OPU is a complex optoelectronic system including several optical devices like lenses, beam-splitters and mirrors. Since the three standards (CD, DVD and "Blu-ray") are using different light wavelengths, three laser diodes are integrated in an OPU. A CD laser at 780 nm, a DVD laser with 660 nm and a blue laser with 410 nm wavelength. All three laser beams are focused onto the disk media and reflected back to the optoelectronic detector IC (OEIC). In this section we will present a prototype OEIC that covers all three standards. The OEIC converts the reflected light from the storage disc to a proportional electrical output signal. On one hand the data rates in optical storage applications like Blu-ray increase rapidly up to 500 Mb/s and on the other hand the reflected light intensity for read application is decreasing below $1\mu W$. Therefore there is a strong demand on OEICs including integrated photodiodes with high-speed and sensitivity performance combined with high-bandwidth and low-noise transimpedance amplifier circuits. Due to the broad variety of operating conditions (CD, DVD, "Blu-ray", read, write, single or double layer disc...) the transimpedance amplifiers must be programmable over a wide range of gains.

In the presented prototype IC the circuits are implemented in the novel $0.5\,\mu m$ BiCMOS technology called B6CP including an integrated PIN-photodiode with a high speed and light sensitivity for all 3 wavelengths used for optical data storage like CD (780 nm), DVD (660 nm) and "Blu-ray" (410 nm). As presented in Section (2.4) the measured photodiode sensitivity is 0.35 A/W for 780 nm, 0.4 A/W for 660 nm and 0.25 A/W for 410 nm wavelength. The 3dB small-signal-bandwidth of the photodiode is above 1 GHz without slow diffusion effects of photo-generated minority carriers. A detailed description of the

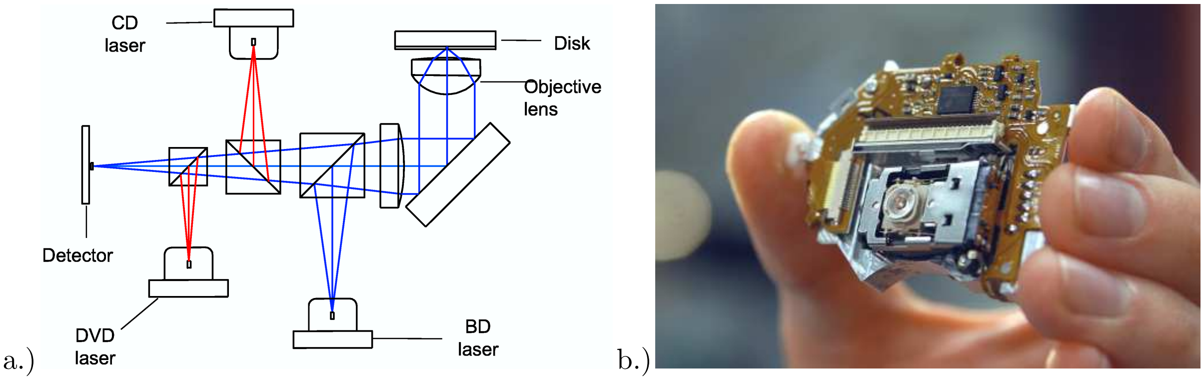


Figure 5.1: Basic optical setup (a.) and photograph of an optical picup unit for a multi standard CD, DVD and Blue-Laser drive (Source: Philips).

B6CP technology can be find in Section (2.4). The technology as well as OEIC prototype development was done within a EC funded Project called "INSPIRED" under reference IST-2000-28013.

The photodetector configuration on the OEIC is the typical 8-photodiode arrangement (see Figure (5.12) and (5.2)) used by most of the OPU manufacturers [47]. It consists of 4 central segments (A...D) and 4 satellite segments (E...H). The central segments are used for data detection as well as laser beam focussing and tracking for DVD and "Blu-ray". The CD operation additionally requires so called satellite segments to the left and right of the central segments. They are used for CD tracking.

Each photodiode segment is connected to a programmable transimpedance amplifier (TIA) stage. Compared to classical solutions for the transimpedance amplifiers [48] we used a new architecture that combines a classical TIA with an input current preamplifier (ITIA) as discussed in Section (4.5.4). This architecture allows a very flexible gain programming in combination with high-speed and low-noise performance. The prototype OEIC has 12 different gain settings for read and write applications and additional 17 gain settings in a special write/clip mode programmable with a serial interface. Another critical issue for an OEIC in OPUs is the data transmission over the flex cable to the controller unit. We implemented an impedance matching of the output driver stage to the 130 Ω cable impedance to avoid signal reflections. To increase the output dynamic range the impedance is generated by active impedance synthesis.

5.2 OEIC Architecture and Building Blocks

The IC architecture is shown in Figure (5.2). The 8 photodiode segments (4 central segments A to D and 4 satellite segments E to H) are located in the center. Left and right to the segments the 8 amplifier channels can be seen. Every single photodiode current is amplified to a single-ended output voltage V_A to V_H. In addition a differential signal RFP and RFM for the RF-data output is implemented which is a summation of the central photodiode signals (A to D). Every amplifier channel consists of a current preamplifier (CA to CH) as input stage, followed by a transimpedance amplifier (TA to TH) and an output buffer (Buf). All stages are programmable with a serial I^2C-interface. A DC output reference voltage between 2V and 2.4V can be applied to an external pin V_{ref}. To avoid channel crosstalk and stability problems, every channel has its own decoder (Dec) with reference voltage and current generation and a power supply filter network is implemented.

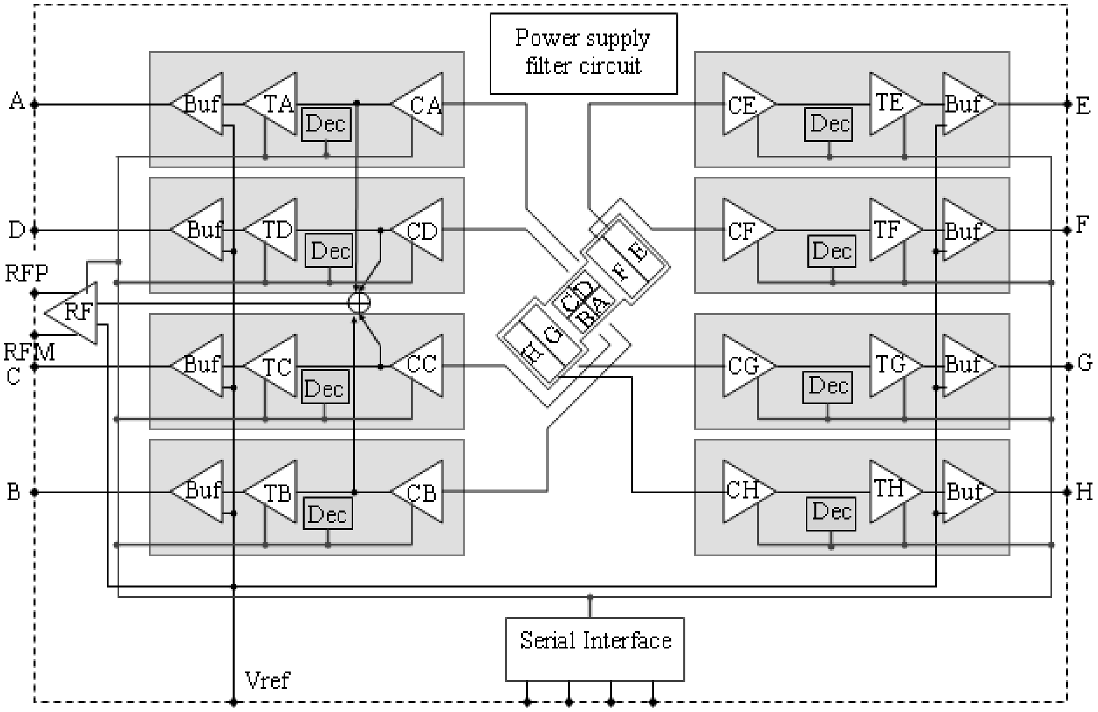


Figure 5.2: OEIC architecture with integrated photodiodes (A to H) connected to a current amplifier (CA to CH), a transimpedance amplifier (TA to TH) followed by an output buffer (Buf). RF is a differential transimpedance amplifier for the current CA+CB+CC+CD. The gain is programmable with a serial interface in combination with a gain decoder (Dec).

Due to the high range of input signal levels for the different operating conditions as read, write and write/clip we implemented a large number of different transimpedance gain settings. The gains in read and write operation for the central segments A to D can be programmed between 130Ω and 270kΩ in steps of two. The gain for the satellite segments is even 4 times higher and the differential RF gain is 2/5 of the central segments gain. For the so called write/clip mode additional 17 gains can be programmed. The objective for the write/clip mode is to use a much higher central segments gain as RF-gain compared to the standard write mode. This allows a 'low' level measurement during write with a high central segment gain which is used for tracking calculation. During the write 'high' level a gain clipping circuit for the central segment becomes active. This circuit adaptively reduces the central amplifier gain at the input stage when the input current becomes too high for maximum central segment output voltage swing. The central segment output voltage swing is reduced to nearly 0 during the 'high' phase. This dramatically decreases the current consumption during write mode.

5.2.1 Transimpedance Amplifier Architecture

To implement the required number of different gains and operating modes we used a new multistage transimpedance amplifier (TIA) architecture. The TIA for one central segment and the differential RF-amplifier is shown in Figure (5.3).

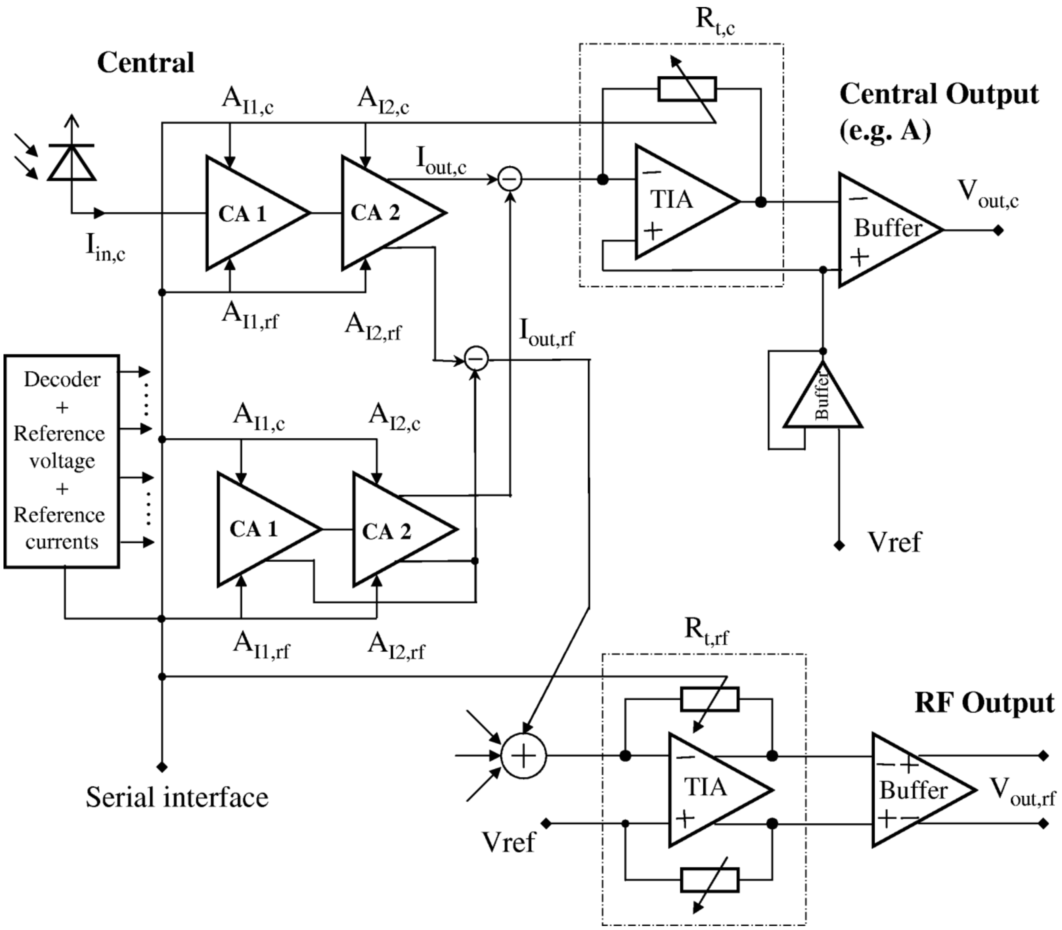


Figure 5.3: ITIA architecture for central and RF channel.

In difference to a classical TIA solution we used a 2-stage current preamplifier (CA1 and CA2) as input stage followed by a classical TIA stage and a buffer at the output (ITIA). The input current $I_{in,c}$ coming from a central segment photodiode is preamplified in the

	Central Segments	Satellite Segments
A_{I1}	0.375/1.5/6	0.9/4/16
A_{I2}	0.25/0.5/1/2/4	0.5/1/2/4/8
$A_{I1,rf}$	0.375/1.5/6	
$A_{I2,rf}$	0.25/0.5/1/2/4	
$R_{t,c}$	1.4kΩ /11kΩ	1.4kΩ /11kΩ
$R_{t,rf}$	530Ω /4kΩ	

Table 5.1: Gain values of the OEIC TIA gain stages

current amplifiers CA1 and CA2 with a gain of $A_{I1,c} * A_{I2,c}$. For the offset compensation of output current $I_{out,c}$ a matched replica of amplifiers CA1 and CA2 are implemented without input current. The output offset current of the replica amplifiers is subtracted from current $I_{out,c}$ by a precise current mirror circuit. The offset compensated current is then fed into a classical TIA with programmable transimpedance $R_{t,c}$. Finally the TIA output voltage is buffered to an output voltage $V_{out,c}$. The output reference voltage V_{ref} is applied to the TIA and buffer amplifier inputs from an external pin.

Also a differential TIA is implemented as shown in Figure (5.3). The input current of this TIA is the sum of the 4 central segment currents $I_{out,rf}$ coming from a second path in current amplifier CA2. The common-mode output voltage of the differential output buffer is defined by V_{ref}.

The main advantage of this TIA implementation is a high flexibility in gain programming since we have designed a variable gain current amplifier as input stage with a high gain-bandwidth and low noise (see Section (5.2.2)) compared to classical TIA implementations.

All amplifier stages are programmable with the serial interface. The gains of the amplifier stages are shown in Table 5.1.

5.2.2 Current Amplifier Circuit

The input current preamplifier stage was presented in Section 4.5.4. A simplified schematic of the current amplifier is shown in Figure (4.21). The amplifier consists of a gain programmable regulated current mirror. The current mirror includes 2 bipolar NPN transistors that are regulated with a n-MOS transistor as Operational Transconductance Amplifier (OTA). The OTA has a transconductance $g_{m1} = \frac{i_{pm}}{v_{in}}$ which regulates the input node V_{in} to a defined and low-ohmic potential V_{in}. The current mirror gain n is the current ratio $n = I_{out}/I_{in}$. This current amplifier architecture has the advantage of a simple continuous gain adjustment with a variable voltage source $V_{gain} = V_p - V_m$.

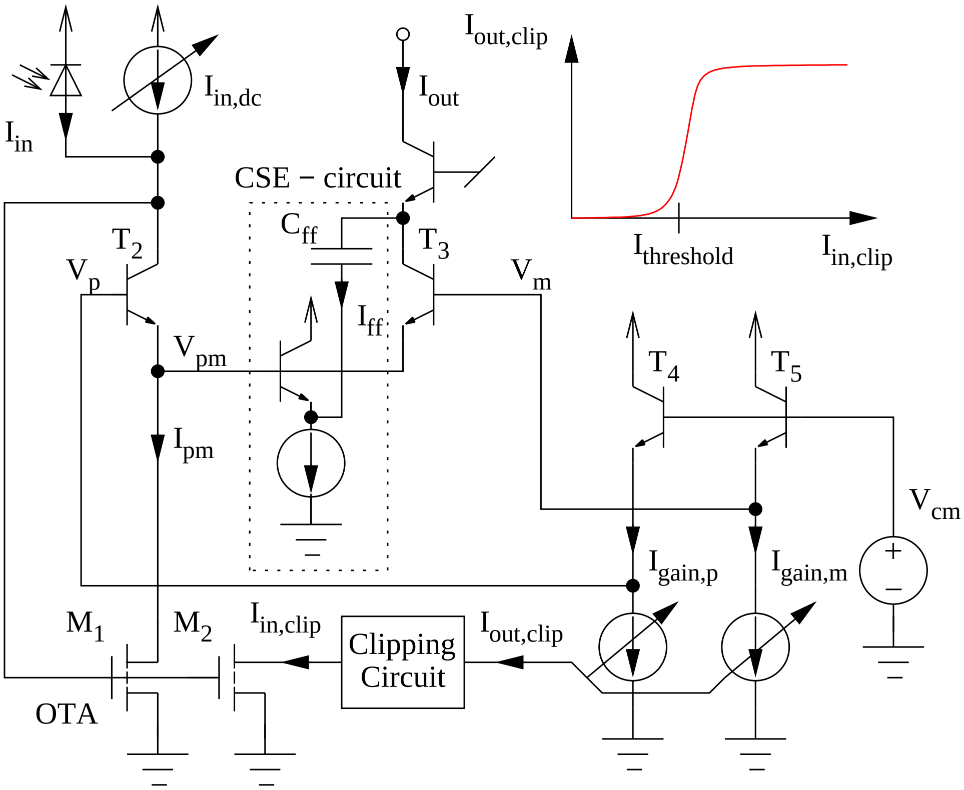


Figure 5.4: OEIC implementation of current amplifier including capacitive-speed enhancement (CSE) and clipping circuit.

The final current amplifier implementation for our OEIC is shown in Figure (5.4). It consists of two NPN current mirror transistors T_2 and T_3 and a NMOS transistor M_1 acting as OTA. For current mirror biasing a dc voltage source V_{cm} and a current source $I_{in,dc}$ was used. As mentioned before, the current gain of this amplifier can be tuned by the NPN current mirror base voltage difference ($V_p - V_m$). This was implemented by transistors T_4 and T_5 which are matched pairs to transistors T_2 and T_3. Therfore the current mirror gain $n = I_{out}/I_{in}$ is equivalent to the ratio of currents $I_{gain,p}/I_{gain,m}$, which realizes simple gain programming.

To enable the clipping functionality described in Section 5.2 an additional clipping circuit block is included in our application. This circuit non-linearly reduces the amplifier gain in the input stage via current sources $I_{gain,p}/I_{gain,m}$ after reaching a defined input current level ($I_{in} > I_{threshold}$). Therefore the high input currents up to 5 mA in write operation are only flowing through the input NPN transistor T_2 and the OTA M_1 to ground. There is no amplified signal current flowing through the following circuit blocks anymore. This results in a lower current consumption for the write/clip mode compared to the normal write mode. The circuit implementation for the clipping circuit is shown in Figure (5.5). It works as fast current comparator which compares the input current $I_{in,clip}$ with a

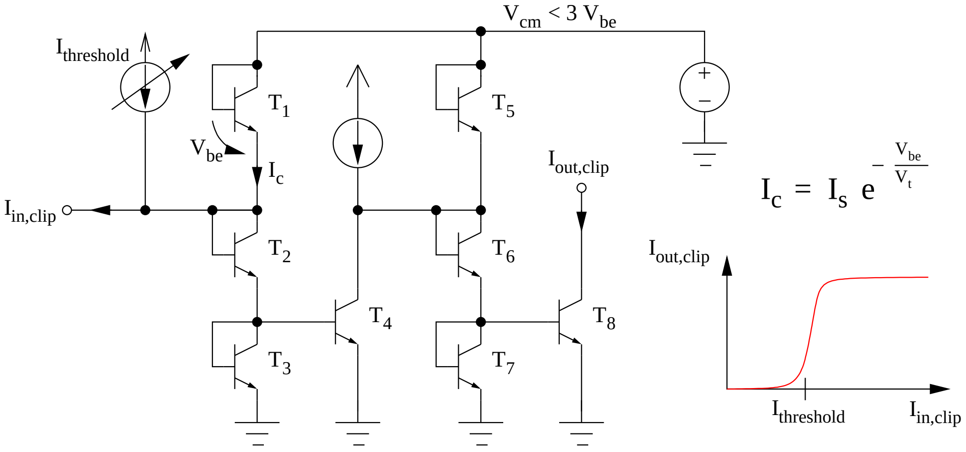


Figure 5.5: Clipping circuit implentation.

reference current $I_{threshold}$. The basic parts of the comparator are three NPN-diodes T_1, T_2 and T_3 in series which are powered by a voltage V_{cm} smaller than three times the base-emitter voltages V_{be}. Depending on the input current direction the transistors T_2, T_3 and therefore T_4 are switched on or off. To increase the comparator gain an identical 2^{nd} stage is implemented. Since all nodes in the circuit are low impedant and there is also no direct feedback included, the comparator speed is high. The comparator characteristic is indicated in Figure (5.5).

The noise performance of the circuit was discussed in Section (4.5.4). There it was shown, that for low input dc-currents $I_{in,dc}$ the input referred noise current decreases to very low values. On the other hand, the bandwidth of the current amplifier also decreases with lower $I_{in,dc}$ current. To optimize the noise as well as the speed performance, we reduced the $I_{in,dc}$ to low values of about $1\,\mu A$. Additionally we introduced a capacitive speed enhancement circuit also shown in Figure (5.4). This circuit by-passes the current mirror transistor T_3 by adding a fast feed-forward current I_{ff} to the output current. The forward current is generated by a buffered capacitor C_d which is connected to a low ohmic node (NPN cascode transistor) at the mirror output. The feed-forward current is approximately defined by the relation

$$I_{ff} = AC_{ff}\frac{dV_{pm}}{dt} \tag{5.1}$$

with A is the buffer gain. In our case we used an emitter follower circuit as buffer, which means a gain of about 1. Depending on the dynamic behavior of node V_{pm} the output current risetime can be optimized via feed-forward buffer gain and C_{ff} value.

Another important parameter especially in data communication systems is the circuit jitter performance. This is defined by the amplifier output signal phase difference between the minimum and maximum transmitted data frequency. Therefore a good jitter performance requires high linearity (constant gradient) in the phase response. A measure for the phase linearity is the group delay τ_d which is related to the phase φ by $\tau_d = -d\varphi/df$

with f is the frequency. An alternative method for jitter investigation is shown in Figure (5.6). It is defined by the maximum deviation of a real amplifiers phase response from ideal phase behavior with constant gradient. The simulated phase response of the ITIA output voltage from Figure (5.3) is shown as solid line in Figure (5.6). The doted line indicates the ideal phase response, which is the tangent at frequency f=0. The maximum simulated amplifier phase gradient deviation between f = 0 and 250 MHz is 12°. With an 250 MHz input signal this relates to an effective group delay of about 130 ps.

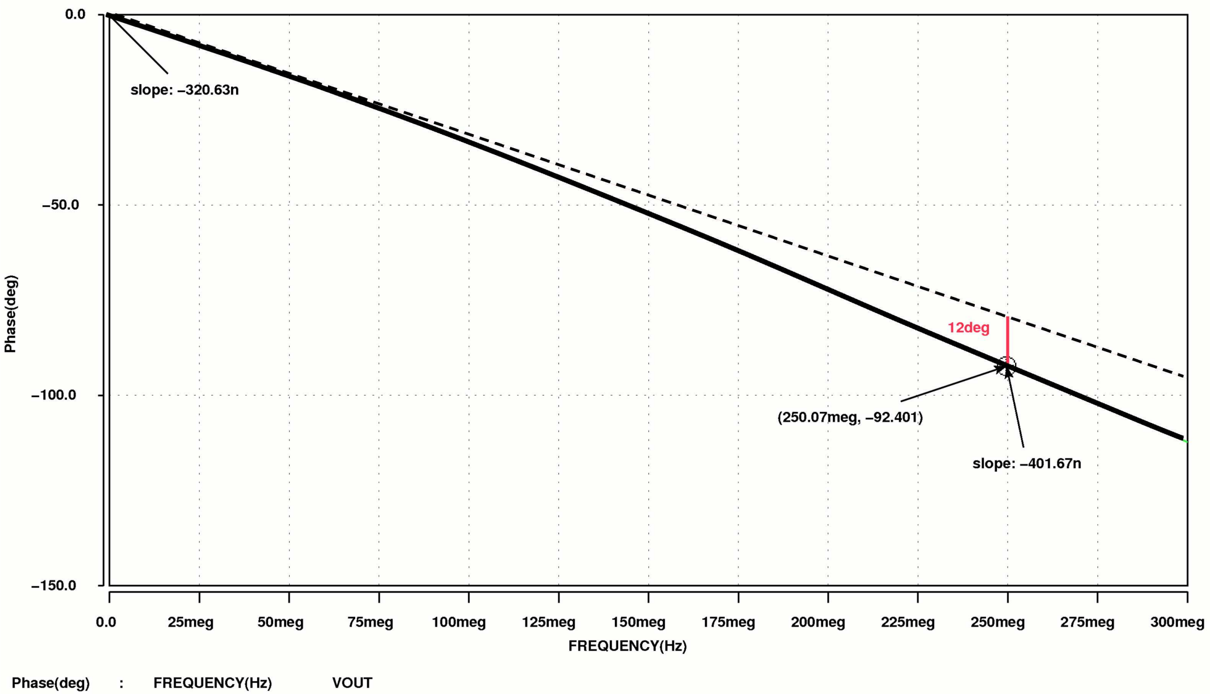


Figure 5.6: Simulated phase response of the ITIA from Figure (5.3)(solid line). The doted line shows an ideal phase response with a constant gradient.

5.2.3 Output Buffer

For RF data transmission over a flex cable an impedance matching is necessary for signal frequencies above 200 MHz. Therefore the output buffer stage has a $130\,\Omega \pm 15\,\Omega$ output impedance matched to the flex cable. The $130\,\Omega$ impedance is generated with active impedance synthesis. Figure 5.7 show the circuit concept for a single ended output buffer with a positive feedback path. The resistor values for the buffer feedback circuit can be calculated according to Equation (5.2) with a synthesis factor m and Equation (5.3) showing the amplifier gain G including load. The factor k defines the value of m and therefore the value of G. Hence the integrated output resistor R_0/m can be m times smaller than the effective output resistance R_0 which matches to the load impedance Z_L. This increases the output voltage dynamic range by a factor of m. In our IC the synthesis factor m=2 and gain G=1.5. The factor m was designed to optimize the output voltage dynamic range with respect to the limited supply voltage headroom for the output buffer. The maximum buffer output voltage swing is 0.8V. The gain G was dimensioned to optimize gain and bandwidth for the combination of TIA and buffer in the output stage.

$$m = \frac{k+1}{k-1} \tag{5.2}$$

$$G = \frac{m+1}{2} \tag{5.3}$$

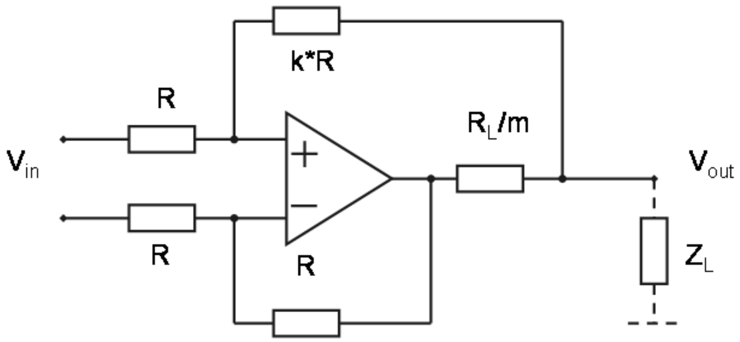


Figure 5.7: Output buffer with active impedance synthesis.

5.2.4 Noise Shielding for Sensitive Amplifier Stages

An important issue for high gain amplifier circuits in general is the signal-to-noise ratio (SNR). An improvement of SNR is essential for a low bit-error-rate in data transmission systems. We discussed in previous sections how to reduce the input referred noise current due to circuits shot noise and thermal noise contributions. The circuits noise performance is determined mainly by the amplifier input stage. But especially for high gain and high bandwidth opto-electronic applications another noise source might be significant. Substrate cross coupling from high power amplifier output stages to sensitive low-current amplifier input stages might be a dominant factor. Minority carriers are capacitively injected into the substrate and may cause noise currents. Also parasitic light that is reflected to analog circuit areas generates minority substrate currents. An effective noise shielding is therefore essential to increase SNR. The presented BiCMOS technology B6CP offers an efficient possibility for noise shielding. The deep PIN-photodiode n^+-buried layer together with the n^+-buried layer contacts can be used to generate a shielding diode as shown in Figure (5.8). This shielding diode is enclosing sensitive circuit parts completely and acts as a guard ring. For an efficient shielding the guard ring needs a low ohmic connection to power supply VDD while the p-substrate bulk is connected to ground VSS. Since the n^+-buried layer is about $10\,\mu m$ deep the sensitive circuit components can be integrated within the shielding structure with a standard process flow without changing the transistor parameters.

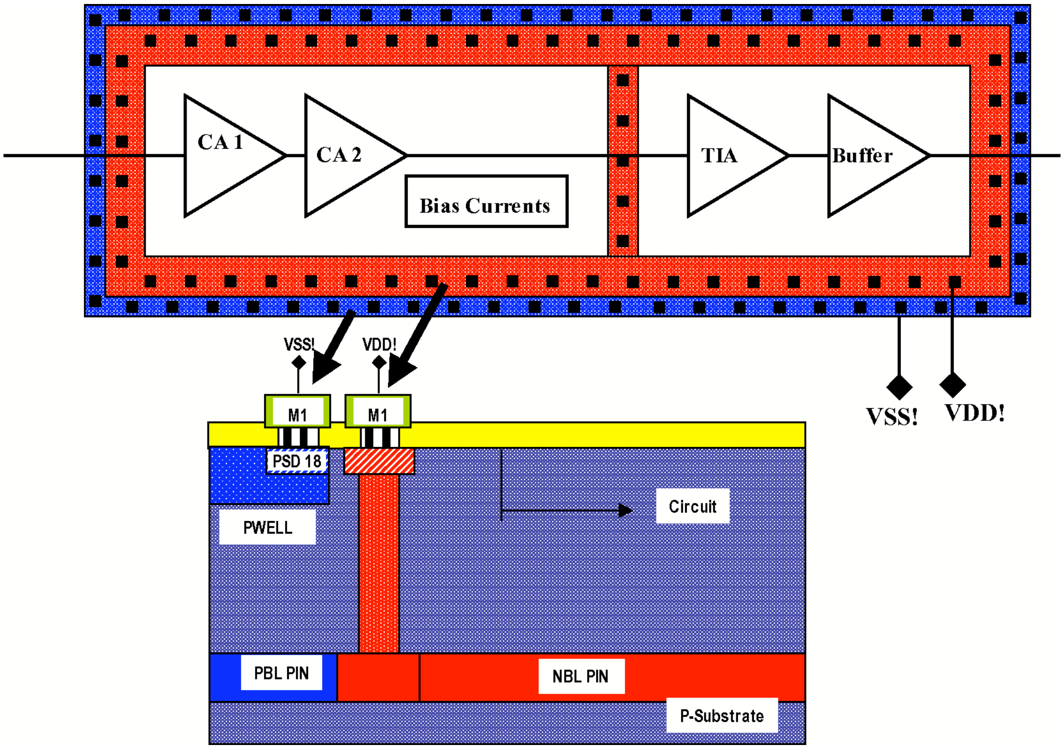


Figure 5.8: Technology option for enhanced noise shielding of sensitive analog blocks by using PIN photodiode technology steps. The circuits are shielded by photodiode buried layers.

5.3 Measurement Results

The IC is mounted in an optically open LGA type package including supply filter caps. For characterization a PCB was developed with external $130\,\Omega$ load resistor simulating a flex-cable. The measurement setup is fixed on an optical bench. As light source we used laser diodes with a wavelengths of 650 nm and 780 nm focused on the chip with optical lenses. The laser diode current is modulated with a pulse generator over a bias-tee circuit. The transient output voltages are measured on the external load resistors with a high impedance probe.

Figure (5.9) shows a transient pulse of the central segments signal with highest gain value of $270\,\mathrm{k}\Omega$. The measured rise/falltime is 1.3 ns. This means a small-signal bandwidth of approximately 260 MHz. The eye diagram of the differential RF signal at highest gain is

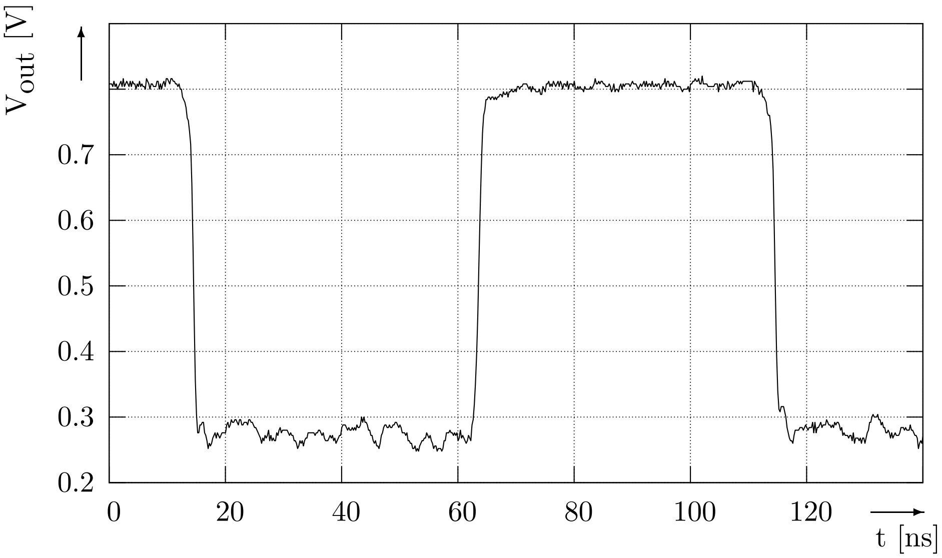


Figure 5.9: Transient signal of central channel with highest gain setting at 650nm wavelength.

shown in Figure (5.10). The diagram shows a well opened eye with a 200 Mbit/s pseudo random data signal with a length of $2^{31} - 1$. Due to the rise/fall times of 1.3 ns even a higher data rate up to 400 Mbit/s is possible even with the highest transimpedance gain value.

The write/clip mode behavior is shown in Figure (5.11). The diagram includes the input light signal and the clipped central channel output signal. During the 'low' phase of the input signal the output is amplified with a high gain. After input signal is switching to 'high' state the amplifier gain is reduced to a very low value. Therefore the output voltage is decreasing to approximately 0 which decreases the IC current consumption during the write.

The maximum output voltage swing for the single-ended signals and for the differential output signal is 800 mV. The power consumption of the ASIC is 300 mW with a supply voltage of 5 V.

Figure (5.12) shows a photograph of the OEIC. In the center the 8 photodiodes can be seen. The whole chip except the photodiodes is covered with a metal plane for light shielding.

5.4 Conclusion

An optical receiver IC for the data storage applications CD, DVD and "Blu-ray" has been realized. The IC consists of integrated PIN-photodiodes connected to programmable transimpedance amplifiers (TIA). The PIN-photodiode shows a superior high-speed and sen-

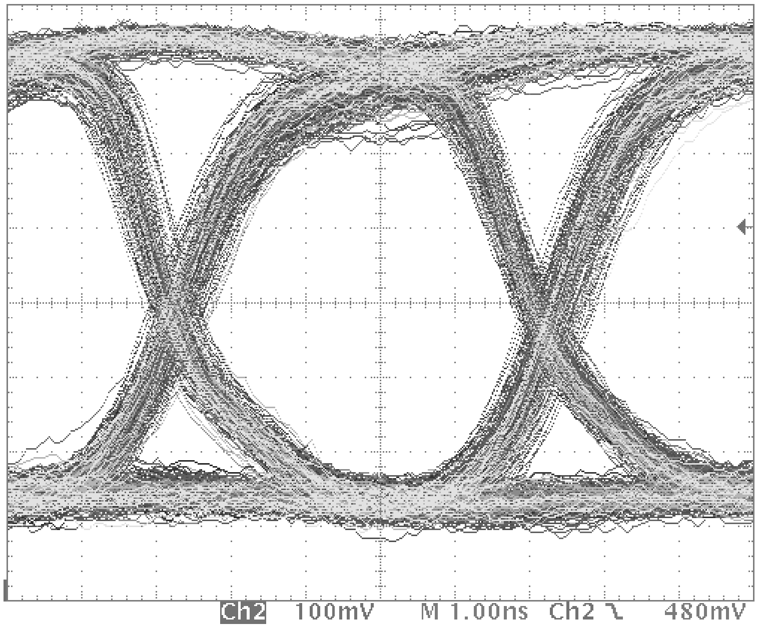


Figure 5.10: Eye diagram at 200 Mbit/s of differential RF output signal at 650nm wavelength.

sitivity performance for all three wavelength needed for CD, DVD and "Blu-ray" applications (780 nm, 660 nm and 410 nm) without any slow diffusion effects. The new multistage TIA architecture with a current pre-amplifier stage (ITIA) gives a high flexibility in gain programming for read, write and write/clip operation mode with 29 different gain settings. A special write/clip mode with active gain control in the input stage is implemented. The rise/fall time for the central segments is 1.3 ns which means a small-signal-bandwidth of 260 MHz for the highest gain of 270 kΩ. In combination with the photodiodes this leads to a sensitivity of $100\frac{mV}{\mu W}$ for 650nm wavelength which is an improvement by a factor of 2 compared to other publications [46]. For an optimized RF data transmission the amplifier output buffers are matched to the 130 Ω flex cable impedance. To improve the amplifier output dynamic range the impedance is generated by an active impedance synthesis with a synthesis factor of 2.

Therefore the OEIC was a fully functional prototype for optical data storage applications, that covers all three standards CD, DVD and Blu-ray. Nevertheless the prototype needs some improvements to bring it to a final product quality. One optimization is necessary to decrease the power consumption, which is at the moment 300 mW. The specification requests for values below 200 mW. This can be reached by reducing a number of gain settings that are not needed within a final product implementation. Another improvement has to be done on amplifier offset. Actually the measured amplifier offset can reach values up to 150 mV, which is to high for a final product. This can be solved by including an offset compensation circuit using laser-fuses for offset compensation during production wafer test.

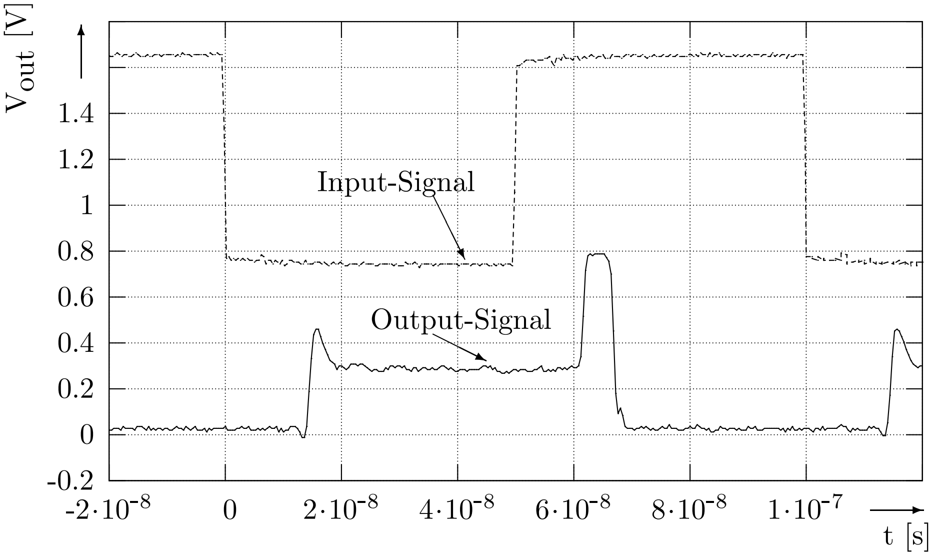


Figure 5.11: Input signal and clipped output signal of central channel in write/clip mode.

To solve the mentioned problems, an OEIC redesign was started called "Demonstrator" [49]. The Demonstrator design can be seen as optimized version of the described prototype OEIC. It has implemented a reduced number of gain settings as well as lower bandwidth compared to the prototype. On the other hand an offset compensation circuit was realized that reduces the output offset voltage to below 20 mV. Also the power consumption was reduced to about 150 mW, which is significantly lower compared to the prototype. Therefore an optimized competitive product version was developed that covers the standards CD, DVD and Blu-ray.

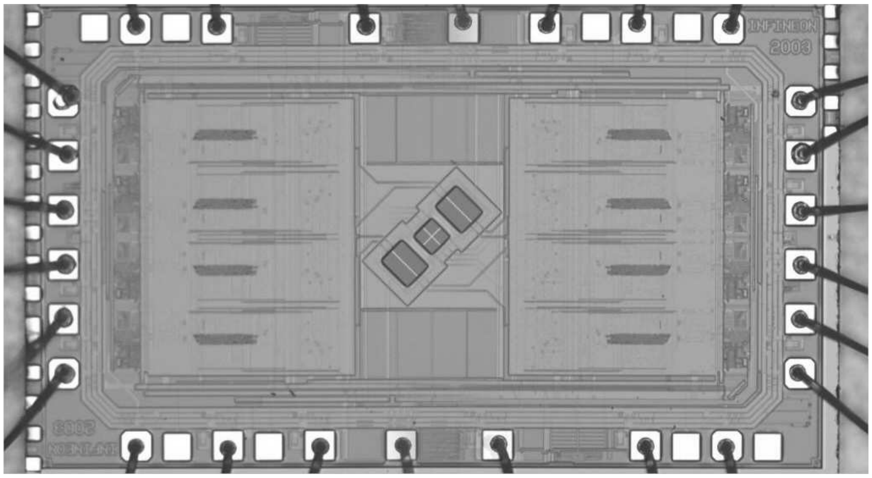


Figure 5.12: OEIC photograph.

Chapter 6

Summary and Conclusion

Optoelectronics integrated circuits became more and more popular within the last 10 years also for high speed applications especially in the field of optical data storage and optical fiber communication. The two driving forces behind this trend are technical performance and production costs. Integrated solutions offers a better speed and noise performance compared to discrete solutions assuming same kind of low-cost PIN photodiodes. On the other hand the integration of photodiodes, analog amplifiers and signal processing circuits on one piece of silicon also provides an advantage in production costs. For sure the OEIC applications can not cover the highest speed applications up to 10^{th} of GHz, since the integrated photodiodes are based on silicon and therefore they can only be used for light wavelengths below $1\,\mu m$. Also the analog circuit performance of the used low-cost IFX BiCMOS technology B6CP is not as high compared to special Si-Ge double poly transistor based BIP technologies. But a lot of low cost applications requests for bandwidths of 100 MHz up to few GHz with light wavelengths from 400 nm up to about 800 nm where the used technology option shows an optimum in performance and costs.

This work can be divided into two main areas related to optical data storage OEIC's. The first part covers the integration and modeling of high-speed photodiodes in BiCMOS technology. Necessary photodiode theory like light transmission, absorption and reflection at semiconductor surfaces, as well as the dynamic carrier behavior including the solution of steady-state continuity equations is presented in Chapter (2). An additional section of Chapter (2) shows the integration of photodiodes in a standard $0.5\,\mu m$ BiCMOS process flow as well as integration of high performance PIN photodiodes that requires additional process steps. The PIN-photodiode BiCMOS process development was done within an EC funded project called "INSPIRED". In Chapter (3) a detailed description of a SPICE model for the BiCMOS double photodiodes is presented. The model includes time dependent photodiode drift and diffusion carrier effects with arbitrary input light transient. Additionally the 3-dimensional photodiode behavior is modeled by using a network approximation. A "Mathematica" tool called *PDes* was developed to design the photodiode geometry and automatically generate a SPICE netlist for analog circuit simulations. The proposed photodiode model provides high accuracy and simulation speed for this kind of integrated photodiodes.

The second part of this work is introduced by Chapter (4). It presents the theory of the transimpedance amplifier (TIA) which is an important building block for all optoelectronics integrated circuits. This chapter mainly covers the analysis and optimization of TIA bandwidth, stability and noise. Another section of Chapter (4) presents different single ended and differential TIA realization examples. Especially for optical data storage OEIC's variable gain amplifiers are needed. Therefore variable gain TIA's were discussed. A new TIA concept was presented, that uses a variable gain current pre-amplifier stage (ITIA) that reaches a very wide gain range with high bandwidth. The following Chapter (5) presents the development of a prototype OEIC used in pick-up units for optical data storage drives. The specification was defined together with the company Philips who was a partner within the project INSPIRED. The prototype was specified to cover all optical data storage standards CD, DVD and also the new "Blu-ray" standard within one OEIC. This prototype should investigate the performance limits using the B6CP technology option with integrated PIN photodiodes. The gain is programmable from 130 Ω to 270 kΩ for the RF central segment photodiodes. A special write/clip mode is implemented with additional 17 gain settings used for write operation. The different operation modes and gains can be programmed with a I^2C serial interface. Despite the high gain values a small-signal bandwidth of 260 MHz was reached at highest gain. This bandwidth is sufficient for next generations Blu-ray discs. In combination with the high PIN photodiode performance this leads to a sensitivity of $100\,mV/\mu W$ for 650 nm light wavelength which means an improvement by a factor of 2 compared to other publications. The output driver stage is matched to 130 Ω flex cable impedance. Active impedance synthesis is used to increase output dynamic range. To summarize, the prototype was a fully functional OEIC for optical data storage, that covers all three standards CD, DVD and Blu-ray. Nevertheless two issues came up with the prototype OEIC. On one hand the output offset voltage was about 150 mV and therefore to high. On the other hand, the OEIC power consumption was above the specified 200 mW. A redesign called "Demonstrator" was started, that solves the mentioned problems. It reduces the power consumption to about 150 mW and the output offset voltage to below 20 mV. Additionally the demonstrator was simplified by reducing the number of gain settings and also bandwidth requirements. Therefore an optimized competitive OEIC was developed that covers all three optical data storage standards CD, DVD and Blu-ray.

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Appendix A

”Photodiode Designer”

The following pages are showing the printout of a developed Mathematica tool *’Photodiode Designer’ (PDes)*. This tool enables the graphical design of photodiodes including the generation of a photodiode SPICE circuit model netlist.

Photodioden - Designer

by J.Sturm (09.2005)

Confidential

1. Allgemeines

Das Script generiert die Spice Netzliste eines vereinfachten Ersatzschaltbildes für eine Double-Photodiode Struktur in der Technologie B6CA. Weiters enthält die Netzliste ein Spice Modell für die Drift- und Diffusionsströme.

2. Generierung des Photodioden Netzwerk Modells / Spice Netzliste

In diesem Abschnitt wird die Photodiode definiert indem die Abmessung, die Anodenkontaktierung (p), sowie die Beleuchtung der Photodiode grafisch designt werden. Aus der definierten Photodiode mit Beleuchtung wird anschließend eine Spice-Netzliste des R-C- Netzwerk Modells mit den zugehörigen Photodiodenströmen generiert. Anschließend werden die Pole und Nullstellen des Netzwerk Modells berechnet. Nach einer Extraktion der aktiven Pole und Nullstellen, werden 2 vereinfachte Spice Ersatzschaltungen für das Photodioden Netzwerk Modell generiert. Die erste modelliert nur einen dominanten Pol. Die zweite modelliert 2 dominate Pole und 2 Nullstellen. Die generierten Netzlisten enthalten neben dem vereinfachten R-C Ersatzschaltbild, auch ein SPICE Model für die Drift und Diffuissions Ströme.

Beschreibung der einzelnen Funktionen

Mit der Funktion "makephotodiode[ ]" werden in einem eigenen Notebook "thenotebook" die Buttons mit dem Titel "Photodiode ganzflächig beleuchten" und "Netzliste generieren" sowie aus der Table "buttontable" eine Buttonmatrix mit der Größe pdcols *pdrows erzeugt, bei der alle Buttons leer sind. Diese Buttonmatrix entspricht den Photodiodenabmessungen. Durch drücken eines Buttons der "buttontable" wird die Funktion "buttonmatrixneu[ ]" aufgerufen und das Notebook "thenotebook" überschrieben. Dabei ändert sich allerdings der gedrückte Buttoninhalt von "leer" auf "*" wird der selbe Button ein zweites Mal gedrückt, ändert sich der Button inhalt von "*" auf "X". Dabei bedeuted "*", daß die Photodiode in desem Netzknoten beleuchtet wird, und "X", daß die Photodiodenanode in diesem Netzknoten kontaktiert ist. Wird der Button "Photodiode ganzflächig beleuchten" gedrückt, werden alle Buttons geleichzeitig auf "*" gestellt. Dabei ruft sich die Funktion buttonmatrixneu[ ] bei jedem Drücken wieder selbst auf, und überschreibt im Notebook"thenotebook" den Inhalt mit den neuen Werten. Ist die Photodiode fertig definiert, so wird durch drücken des Buttons "Netzliste generieren" aus der Photodiode die Titan-Netzliste mit den R,C und Stromquellen generiert.

```
In[1]:=
```

Setze das Directory in dem dieses Notebook liegt, zum Arbeits Directory.

```
In[2]:= $NotebookDirectory =
          ToFileName@First["FileName" /. NotebookInformation[EvaluationNotebook[]]];
        SetDirectory[$NotebookDirectory];
```

```
In[4]:= makephotodiode[] := (
          (* Photodiodengröße definieren und Anzahl der Zellen berechnen. Gesamtzahl ca. 400 *)
          pdlength = Input["Geben Sie die Photodiodenlänge in mm ein:"];
          pdwith = Input["Geben Sie die Photodiodenbreite in mm ein:"];
          pdcols = IntegerPart[Sqrt[400 * pdlength / pdwith]] // N;
          pdrows = IntegerPart[400 / pdcols] // N;
          areapd = pdlength * pdwith;

          (*Photodiodentable generieren *)
          buttontable = Table[" ", {i, pdrows}, {j, pdcols}];

          (* Button, um die ganze Photodiode zu beleuchten *)
          ButtonPDganzfl =
           ButtonBox["Photodiode ganzflächig beleuchtet", ButtonEvaluator → Automatic,
            Active → True, ButtonFunction :> (buttontable = Table["*", {i, pdrows}, {j, pdcols}];
              NotebookFind[ButtonNotebook[], "DieNeuePhotodiode", All, CellTags];
              NotebookWrite[ButtonNotebook[], buttonmatrixneu[]]), ButtonSource → ButtonContents];

          (* Button, um die Netzliste zu generieren *)
          GenNet = ButtonBox["Netzliste generieren", ButtonEvaluator → Automatic, Active → True,
            ButtonFunction :> (GenerateNetlist[]), ButtonSource → ButtonContents];

          (* Notebook generieren, in der die Photodiode bearbeitet wird *)
          thenotebook = NotebookPut[Notebook[{ButtonPDganzfl, GenNet, buttonmatrixneu[]},
             WindowElements → {"HorizontalScrollBar", "VerticalScrollBar", "MagnificationPopUp"},
             WindowToolbars → "EditBar", WindowFrameElements → {"CloseBox", "ZoomBox", "ResizeArea"},
             WindowSize → {Fit, 500}, WindowClickSelect → True, WindowFrame → "Normal",
             WindowTitle -> "Photodiode", Active → True, Background → RGBColor[0.1, 0.2, 0.5]]];
          SelectionMove[thenotebook, Before, Notebook];
         )
```

```
In[5]:= buttonmatrixneu[] := (Cell[ButtonPDganzfl];
          Cell[GenNet]; Cell[
           BoxData[GridBox[Table[ButtonBox[buttontable[[x, y]], Background → RGBColor[1, 0.8, 0.4],
               ButtonEvaluator → Automatic, Active → True, ButtonFunction :→
                ({buttontable[[#2[[1]], #2[[2]]]] = #2[[3]]; NotebookFind[ButtonNotebook[],
                    "DieNeuePhotodiode", All, CellTags]; NotebookWrite[ButtonNotebook[],
                    buttonmatrixneu[], AutoScroll → True]} &), ButtonSource → ButtonData, ButtonData ->
                {x, y, If[buttontable[[x, y]] == " ", "*", If[buttontable[[x, y]] == "*", "X", " "]]}],
              {x, pdrows}, {y, pdcols}], ColumnSpacings → 0, RowSpacings → 0,
             ColumnWidths → 1.5, RowMinHeight → 1.5]],
           NotebookDefault, CellMargins → {{0, 0}, {0, 0}},
           ShowCellBracket → False,
           Active → True,
           CellTags -> "DieNeuePhotodiode"])
```

Eine Netzliste wird aus der aktuellen Photodiodenmatrix "buttontable" generiert, in der die Netzknoten mit den Strömen und Anschlüssen definiert sind. Der Name der Netzliste sowie die Bezeichnung der Photodioden Anode und Kathode wird eingegeben.

Die erste Netzliste (Variable=Netzliste) dient zur Berechnung der Übertragungsfunktion (Eingangsphotodiodenstrom / Ausgangsphotodiodenstrom). Der Eingangsstrom wird mit spannungsgesteuerten Spannungsquellen realsiert, die auch AC Quellen sind. Der gesamte Phtodiodenströme (Summe aller Netzknotenströme) ergibt sich aus der eingestrahlten Lichtleistung (entspricht der angelegten Spannung an der gesteuerten Stromquelle) multipliziert mit der Photodiodenempfindlichkeit Spd.

```
In[6]:= GenerateNetlist[] :=
         (
          (* Parameter *)
          RsqAn = 1000;  (*Square Widerstand der p-Anode (p-Basis oder p-S/D) *)
          RsqKat = 100;    (*Square Widerstand der n-Kathode (n-buried layer) *)
          Spd = 0.4;    (* Empfindlichkeit d. Photodiode in A/W *)
```

```
LightPower = 1;  (* Eingangslichtintensität für die berechnung des PD-Stromes *)
Cpd = pdlength * pdwith * 70 * 10^-12;  (* Kapazität der Photodiode;
 nur geschätzter Wert, der aktuelle Wert wird in der Netzliste definiert  *)
CpdNet = Cpd / (pdcols * pdrows);

(* Eingeben des Netzlistennamens
  und der Photodiodenanschlussnamen für Kathode und Anode *)
Netzliste = InputString["Geben Sie den Netzlistennamen ein"];
PDanode = InputString["Geben Sie einen Namen für die Anode von PD1 ein:"];
PDanode2 = InputString["Geben Sie einen Namen für die Anode von PD2 ein:"];
PDcathode = InputString["Geben Sie einen Namen für die Kathode von PD1+PD2 ein:"];

(* Generieren der Photodiodenstrommatrix und der Anschlussmatrix *)
PDcurrentTable = buttontable /. {"X" → 0, " " → 0};
PDcontactTableP = Table[buttontable[[i, j]] /. {"*" → SequenceForm["p", i, "p", j],
    " " → SequenceForm["p", i, "p", j], "X" → PDanode}, {i, pdrows}, {j, pdcols}];
PDcontactTableN = Table[If[(i == 1 || i == pdrows || j == 1 || j == pdcols),
   PDcathode, SequenceForm["n", i, "n", j]], {i, pdrows}, {j, pdcols}]

(* Schreiben der Netzliste des gesamten Photodioden Netzwerkmodells in ein Textfile. Die
  Netzliste liegt dabei in einem Subcircuit mit den Anschlüssen Anode,
 Kathode und 2 Steuerleitungen für die eigestrahlte Lichtstärke *);
pdmodelname = ToString[SequenceForm["PDmod_", Date[][[1]], "_",
   Date[][[2]], "_", Date[][[3]], "_", Date[][[4]], "_", Date[][[5]]]];
FullNetlist = "Full_" <> Netzliste;
outputstream = OpenWrite[FullNetlist];

WriteString[outputstream,
 "*##############################################################\n",
 "*########## Titan-netlist of the photodiode Model ##########\n",
 "*##############################################################\n",
 "* by J.Sturm (2002)\n",
 "* The photodiode model is a subcircuit with 4 external Pins:\n",
 ToString[SequenceForm["* ", PDanode, "  =  Photodiode anode     ",
   PDcathode, "  =  Photodiode cathode", "\n"]],
 "* PdLightP, PdLightM  =  input pins for light intensity in W\n", "*\n",
 "* The light intensity falling on the photodiode is the voltage\n",
 "* between the pins PDLightP and PDLightM. The pins must be\n",
 "* connected to an external voltage source.\n", ToString[
  SequenceForm["* The size of the photodiode is ", pdlength, " x ", pdwith, " mm.\n"]],
 ToString[SequenceForm["* The photodiode model is an R/C/I network with ",
   pdcols * pdrows, " nodes.\n"]], "*\n", "*\n"];

WriteString[outputstream, "* The name of the subcircuit is ", pdmodelname,
 "\n", "\n", "* The netlist:\n", "\n", ToString[SequenceForm[".SUBCKT ",
   pdmodelname, " ", PDanode, " ", PDcathode, " PdLightP PdLightM\n", "\n"]]];

(* Schreiben der Widerstände der p-Schicht in die Netzliste *)
WriteString[outputstream, "* p layer resistors of photodiodemodel\n"];
Do[(WriteString[outputstream, ToString[
    SequenceForm["R_", j, "p", i, "_", j, "p", i + 1, " ", PDcontactTableP[[j, i]], " ",
     PDcontactTableP[[j, i + 1]], " ", RsqAn, "\n"]]]), {i, 1, (pdcols - 1)}, {j, 1, pdrows}];
Do[(WriteString[outputstream, ToString[SequenceForm["R_", j, "p", i, "_", j + 1,
     "p", i, " ", PDcontactTableP[[j, i]], " ", PDcontactTableP[[j + 1, i]],
     " ", RsqAn, "\n"]]]), {i, 1, pdcols}, {j, 1, (pdrows - 1)}];

(* Schreiben der Widerstände der n-Schicht in die Netzliste *)
WriteString[outputstream, "* n layer resistors of photodiodemodel\n"];
Do[(WriteString[outputstream, ToString[
```

```
    SequenceForm["R_", j, "n", i, "_", j, "n", i + 1, " ", PDcontactTableN[[j, i]], " ",
     PDcontactTableN[[j, i + 1]], " ", RsqKat, "\n"]]]), {i, 1, (pdcols - 1)}, {j, 1, pdrows}];
Do[(WriteString[outputstream, ToString[SequenceForm["R_", j, "n", i, "_", j + 1,
     "n", i, " ", PDcontactTableN[[j, i]], " ", PDcontactTableN[[j + 1, i]],
     " ", RsqKat, "\n"]]]), {i, 1, pdcols}, {j, 1, (pdrows - 1)}];

(* Schreiben der Kapazitäten in die Netzliste *)
WriteString[outputstream,
 "* Capacitances of photodiodemodel between the anode and cathode nets\n"];
Do[(WriteString[outputstream, ToString[
    SequenceForm["Cpd_", j, "x", i, " ", PDcontactTableP[[j, i]], " ",
     PDcontactTableN[[j, i]], " ", MantissaExponent[CpdNet // N][[1]], "E",
     MantissaExponent[CpdNet // N][[2]], "\n"]]]), {i, 1, pdcols}, {j, 1, pdrows}];

(* Schreiben der Photodiodenströme in die Netzliste, wenn Sie ungleich 0 sind *)
WriteString[outputstream,
 "* Photodiode net currents. Voltage-controlled-current-sources\n",
 "* with G = (Photodiodesensitivity Spd / number of currentnodes)\n"];
Do[(WriteString[outputstream, If[PDcurrentTable[[j, i]] == 0, Continue[],
    ToString[SequenceForm["GIpd_", j, "x", i, " ", PDcontactTableN[[j, i]],
      " ", PDcontactTableP[[j, i]], " PdLightP PdLightM ",
      (Spd / Count[buttontable, "*", 2]), "\n", "\n"]]]]), {i, 1, pdcols}, {j, 1, pdrows}];

WriteString[outputstream, ToString[SequenceForm["R_cathode ", PDcathode, " 0 1g", "\n"]],
 ToString[SequenceForm["R_anode ", PDanode, " 0 1g", "\n"]]];
WriteString[outputstream, ".ENDS\n", "\n"];
WriteString[outputstream,
 "* Subcircuit call of photodiodemodel. Name of subcircuit is: XPD\n",
 ToString[SequenceForm["XPD ", PDanode, " ", PDcathode,
   " PdLightP PdLightM ", pdmodelname, "\n", "\n"]]];
WriteString[outputstream, "*######### End of the photodiode model ###########\n"];

Close[outputstream];

(* Schreiben der Netzliste für die AC-Analyse des Photodiodenstromes in ein
   Textfile. Dabei liegt die AC-Quelle an der Photodioden stromquelle *);
TFNetlist = "TF_" <> Netzliste;
DeleteFile[TFNetlist];
CopyFile[FullNetlist, TFNetlist];

outputstream = OpenAppend[TFNetlist];

WriteString[outputstream, "*\n", "*########### Titan Runset ############\n",
 "* This is a TITAN runset for simulation of the AC photodiode transfer function \n",
 "* The AC source is located in the photodiode current sources. \n",
 "*\n", ToString[SequenceForm["V_cathode ", PDcathode, " 0 dc 3", "\n"]],
 ToString[SequenceForm["V_anode ", PDanode, " 0 dc 0\n"]], ToString[SequenceForm[
   "V_light PdLightP PdLightM PULSE(0 ", LightPower, " 0 100p 100p 25n 50n) AC 1\n"]],
 "Rpdlightp PdLightP 0 1g\n", "Rpdlightm PdLightM 0 1g\n",
 "******** Analysis ************\n", ".tran 20p 50n\n", ".op\n", ".ac dec 50 10 100g\n",
 ".pz V_light i(V_anode) dec 20 1000 100g\n", "********* Output ***********\n",
 ".plot tran level=1 v(*) i(V_anode,np)\n", ".plot ac level=0 i(V_anode)\n",
 ".SAVE pdmod FORMAT=SCOPE\n", "**********************************\n", ".END\n"]

Close[outputstream];



(* Schreiben der Netzliste für die AC-
```

```
    Analyse zur Bestimmung der Photodiodenimpedanz. Dabei liegt die AC-
    Quelle an der Photodioden Kathode. Der Name der Netzliste ist Z_xxxx *);
  ZNetlist = "Z_" <> Netzliste;
  DeleteFile[ZNetlist];
  CopyFile[FullNetlist, ZNetlist];

  outputstream = OpenAppend[ZNetlist];

  WriteString[outputstream, "*\n", "*########## Titan Runset ############\n",
   "* This is a TITAN runset for simulation of the photodiode Output inpedance \n",
   "* The AC source is the photodiode cathode voltage source. \n", "*\n",
   ToString[SequenceForm["V_cathode ", PDcathode, " 0 dc 3 AC 1", "\n"]],
   ToString[SequenceForm["V_anode ", PDanode, " 0 dc 0\n"]],
   ToString[SequenceForm["V_light PdLightP PdLightM PULSE(0 ", LightPower,
     " 0 100p 100p 25n 50n)\n"]], "Rpdlightp PdLightP 0 1g\n", "Rpdlightm PdLightM 0 1g\n",
   "******** Analysis ************\n", ".tran 20p 50n\n", ".op\n", ".ac dec 50 10 100g\n",
   ".pz V_light i(V_anode) dec 20 1000 100g\n", "********* Output ***********\n",
   ".plot tran level=1 v(*) i(V_anode,np)\n", ".plot ac level=0 i(V_anode)\n",
   ".SAVE pdmod FORMAT=SCOPE\n", "*********************************\n", ".END\n"]

  Close[outputstream];
  NotebookWrite[thenotebook, Print["Die Netzliste ", Netzliste, " wurde erstellt."]];
 )
```

```
In[7]:= makephotodiode[]
```

3. Generierung eines vereinfachten Photodiodenmodels

```
In[8]:=
```

In diesem Abschnitt werden die 2 Titan-Runset Files mit der Netzliste des Photodiodennetzwerks für die Bestimmung der Ausgangsimpdenzin sowie für die Bestimmung der Photodiodenübertragungsfunktion in Analog Insydes eingelesen.

Mit den 2 Netzlisten wird eine AC-Analyse sowie eine Pol/Nullstellen Analyse durchgeführt. Aus der Pol/Nullstellen Liste werden die signifikanten Pole und Nullstellen herausgefiltert. Mit den signifikanten Polen und Nullstellen wird nun eine einfache Ersatzschaltung mit Spice-Primitives generiert. Die Ersatzschaltung wird in ein Titan Runset geschrieben und kann anschließend entweder mit Titan simuliert werden. Zur Verifikation des vereinfachten Modells wird die Netzliste der Ersatzschaltung wieder ins *Mathematica* geladen, eine AC sowie Polnullstellen Analyse durchgeführt und mit der vollständigen Photodioden Ersatzschaltung verglichen.

Initialization

Einige Warnings ausschalten

```
In[9]:= Off[General::spell, General::spell1];
```

Loading and Configuring Analog Insydes

Analog Insydes laden.

```
In[10]:= << AnalogInsydes`
```

```
In[11]:= ReleaseInfo[AnalogInsydes]
```

Default Option settings für einige Graphic Funktionene.

```
In[12]:= SetOptions[{BodePlot, NicholPlot}, PlotPoints → 200, ImageSize → 500];
```

■ Photodioden Übertragungsfunktion

Hier wird die Übertragungsfunktion der Photodiode berechnet (AC-Analyse sowie Pole/Zero Analyse) sowie daraus ein Ersatzschaltbild in spice generiert. Für die Berechnung wird das Runset mit der Variablen Netzliste eingelesen. Die AC Quelle liegt dabei am Eingang der spannungsgesteuerten Stromquellen, die dem Photodiodenstrom entsprechen.

Einlesen des Titan Runset-Files mit der Photodioden Netzliste. Der Name ist in der Variable "Netzliste" definiert

```
In[13]:= tivnetTF = ReadNetlist[TFNetlist, Simulator → "Titan"];

In[14]:= (* tivnetTF//DisplayForm *)
```

Circuit Equations, AC Analysis

Erstellen der Schaltungsgleichungen

```
In[15]:= Clear[s];

In[16]:= tiveqsTF = CircuitEquations[tivnetTF, AnalysisMode → AC, Protocol → {All, All, All}];

In[17]:= (* tiveqsTF // DisplayForm *)
```

Numerische AC-Analyse mit den Schaltungsgleichungen

```
In[18]:= (* acsweepTF=ACAnalysis[tiveqsTF,{f,1,10^10},PointsPerDecade→20,Protocol→All]; *)
```

Numerical Pole/Zero Analysis

Numerisch Pole und Nullstellen des Verstärkers berechnen.

```
In[19]:= Clear[s];

In[20]:= pzTF = PolesAndZerosByQZ[tiveqsTF, I$V$ANODE];
```

Darstellen der Pole und Zeros in einem Root-Locus-Plot

```
In[21]:= rloc2 = RootLocusPlot[Evaluate[pzTF],
           LinearRegionLimit → Infinity, PlotRange → {{-2 * 10^8, 1}, {-1, 1}}]
```

Extrahieren der aktiven Pole und Zeros

Pole und Zeros aus pz extrahieren und nach der Größe sortieren. Das Zero bei 0, das von der Kapazität kommtsoll entfernt werden

```
In[22]:= poTF = Sort[(Poles /. pzTF), Re[#2] < Re[#1] &];
         zeTF = Sort[(Zeros /. pzTF), Re[#2] < Re[#1] &];

In[24]:=

In[25]:= (* poTF>>"PdPoles_TF.m"
            ze>>"PdZeros_TF.m" *)

In[26]:= (* poTF=<<"PdPoles_TF.m"
           zeTF=<<"PdZeros_TF.m" *)
```

Absolutwert der Pole und Zeros ausrechnen und nach der Größe sortieren

```
In[27]:= AbsPoTF = Sort[Abs[poTF], Re[#2] > Re[#1] &];
         AbsZeTF = Sort[Abs[zeTF], Re[#2] > Re[#1] &];

In[29]:= Length[AbsPoTF]
         Length[AbsZeTF]
```

Toleranzbereich innerhalb dessen ein Pol und ein Zero sich aufheben: wenn (Zero -Pol<Zero*tol)

```
In[31]:= tolTF = 0.1;
```

Active Poles (ActPoles) und active Zeros (AcatZeros) suchen:

```
In[32]:= ActPolesTF = poTF;
         zerTF = zeTF;
         ActZerosTF = {};
         j = 0;
         While[Length[zerTF] > 0,
          (
           mark = 0;
           For[i = 1, i ≤ Length[ActPolesTF], i ++,
            If[(Abs[Re[Extract[ActPolesTF, i] - First[zerTF]]]) < (tolTF * Abs[Re[First[zerTF]]]) ∧
              (Abs[Im[Extract[ActPolesTF, i] - First[zerTF]]]) ≤ (tolTF * Abs[Im[First[zerTF]]]),
             mark = 1; (ActPolesTF = Delete[ActPolesTF, {i}]; Break[])]
           ];
           If[mark == 1, zerTF = Delete[zerTF, {1}],
            (ActZerosTF = Append[ActZerosTF, First[zerTF]]; zerTF = Delete[zerTF, {1}])]
          )
         ]
```

Absolutwert der aktiven Pole und Zeros ausrechnen und nach der Größe ordnen:

```
In[37]:= AbsActPolesTF = Sort[Abs[ActPolesTF], Re[#2] > Re[#1] &]
         AbsActZerosTF = Sort[Abs[ActZerosTF], Re[#2] > Re[#1] &]

In[39]:= RedAbsActPolesTF = Take[AbsActPolesTF, 2]
         RedAbsActZerosTF = Take[AbsActZerosTF, 2]
```

Berechnen von R und C für den erten dominaten Pol, wobei C der Photodiodenkapazität Cp entspricht:

```
In[41]:= rpol1 = ToString[SequenceForm["'1/(", CForm[Abs[poTF[[1]]]], "*Cphd1)'"]]
```

Berechnen der 2 Rs und 3 Cs des vereinfachten Ersatzschaltbildes für 2 Pole und 2 Nullstellen:

```
In[42]:= Clear[r1, r2, c1, c2, c3]

In[43]:=
         gl1 = (1 / RedAbsActPolesTF[[1]]) + (1 / RedAbsActPolesTF[[2]]) == r1 * c1 + r2 * c2 + r2 * c1;
         gl2 = 1 / (RedAbsActPolesTF[[1]] * RedAbsActPolesTF[[2]]) == r1 * c1 * r2 * c2;
         gl3 = (1 / RedAbsActZerosTF[[1]]) + (1 / RedAbsActZerosTF[[2]]) ==
            (r1 * c1 * c2 + r2 * c1 * c3 + r2 * c2 * c3 + r1 * c1 * c3) / (c1 + c2 + c3);
         gl4 = 1 / (RedAbsActZerosTF[[1]] * RedAbsActZerosTF[[2]]) == (r1 * c1 * r2 * c2 * c3) / (c1 + c2 + c3);
         gl5 = c1 + c2 + c3 == Cphd1;

         Zelems = Solve[{gl1, gl2, gl3, gl4, gl5}, {r1, r2, c1, c2, c3}]

In[49]:= r1 = r1 /. First[Zelems];
         r2 = r2 /. First[Zelems];
         c1 = c1 /. First[Zelems];
         c2 = c2 /. First[Zelems];
         c3 = c3 /. First[Zelems];

In[54]:= r1 = ToString[SequenceForm["'", CForm[r1], "'"]]
         r2 = ToString[SequenceForm["'", CForm[r2], "'"]]
         c1 = ToString[SequenceForm["'", CForm[c1], "'"]]
         c2 = ToString[SequenceForm["'", CForm[c2], "'"]]
         c3 = ToString[SequenceForm["'", CForm[c3], "'"]]
```

Schreiben einer Netzliste für den vereinfachten Photodioden Subcircuit der Übertragungsfunktion.

Es werden 2 Netzlisten geschrieben:

1. PDsubckt_1p: Subcircuit mit einem dominanten Pol (Photodiodenkapazität + Widerstand)
2. PDsubckt_2p_2z: Subcircuit der Übertragungsfunktion mit 2 Polen und 2 Nullstellen von RedAbsActPoles bzw. RedAbsActZeros.

```
In[59]:= Clear[postr];
         postr = {};
         For[i = 1, i ≤ 2,
           postr = Append[postr, ToString[SequenceForm[MantissaExponent[RedAbsActPolesTF][[i, 1]],
               "E", MantissaExponent[RedAbsActPolesTF][[i, 2]]]]]; i ++];
         Clear[zestr];
         zestr = {};
         For[i = 1, i ≤ 2,
           zestr = Append[zestr, ToString[SequenceForm[MantissaExponent[RedAbsActZerosTF][[i, 1]],
               "E", MantissaExponent[RedAbsActZerosTF][[i, 2]]]]]; i ++];

In[65]:= postr
         zestr
```

Schreiben einer Netzliste eines Subcircuit Modells mit 2 Polen und 2 Nullstellen :

```
In[67]:= outputstream = OpenWrite["PDsubckt_TF_2p_2z"];

         WriteString[outputstream,
           "*########################################################################\n",
           "*# SPICE Subcircuit of B6CA Double-Photodiode with 2 pole and 2 zeros   #\n",
           "*########################################################################\n",
           "* by J.Sturm (2005)\n",
           "* The SPICE model of the double photodiode consists of a simplified R-C-I model ",
           "\n",
           "* The R-C Model for the upper photodiode PD1 is
             extracted from the photodiode network model.", "\n",
           "* It models two dominant poles and two zeros with resistors
             R1,R2 and capacitors C1,C2,C3.", "\n",
           "* The Model for the lower (substrate) photodiode PD2 is a
             single fixed resistor Rpd2 and capacitor Cpd2.", "\n",
           "* The photodiode current for Pd1 and PD2 is represented by a
             SPICE model for the drift and diffusion currents. ", "\n",
           "* The 2 poles and 2 zeros of the transferfunction are:\n", "\n",
           ToString[SequenceForm["* Poles: ", postr, "\n"]],
           ToString[SequenceForm["* Zeros: ", zestr, "\n"]], "\n",
           "* Input pins:\n",
           "* vin  =  input pin for light intensity in W\n",
           "* The vin pin must be connected by an external voltage source to 0.\n", "\n",
           "* Output pins:\n",
           ToString[SequenceForm["* ", PDcathode, ", ", PDanode, " ", PDanode2,
             " = Photodiode cathode and anode1 (PD1) and anode2 (PD2)"]], "\n",
           "\n",
           "* The photodiode model in this netlist is given as subcircuit:", "\n",
           "* .SUBCKT PDsubckt_TF_2p_2z vin PDcathode PDanode PDanode2", "\n",
           "* XPD vin PDcathode PDanode PDanode2 PDsubckt_TF_2p_2z", "\n",
           "\n",
           "************************************************* ", "\n",
           "**** SPICE Model of Drift/Diffusion currents *** ", "\n",
           "************************************************* ", "\n",
           "\n",
           "******************************", "\n",
           "*Parameters", "\n",
         "******************************", "\n",
           ToString[SequenceForm[".param A=", areapd, "e-6 *photodiode area in m2"]], "\n",
         ".param xpe=0.3e-6", "\n",
         ".param xne1=2e-6", "\n",
         ".param xne2=4e-6", "\n",
         ".param xnm=3e-6", "\n",
```

```
".param Na1=1e24 *p-Base doping concentration", "\n",
".param Na2=2e21 *p-Substrate doping concentration", "\n",
".param Nd1=2e21 *n-Epi doping concentration", "\n",
".param Nd2=2e25 *n-BL doping concentration", "\n",
".param phi=0.8", "\n",
".param epsilon0=8.85e-12", "\n",
".param epsilonr=12", "\n",
".param q=1.6e-19", "\n",
".param Vpn1=-3 *pn-junction reverse voltage of pd1", "\n",
".param Vpn2=-3 *pn-junction reverse voltage of pd2", "\n",
".param mun1=1300e-4", "\n",
".param mun2=1300e-4", "\n",
".param mup1=500e-4", "\n",
".param mup2=500e-4", "\n",
".param Eth=3.5e5", "\n",
".param vsn=1e5", "\n",
".param vsp=1e5", "\n",
".param taun1=1e-6", "\n",
".param taun2=1e-6", "\n",
".param taup1=1e-6", "\n",
".param taup2=1e-6", "\n",
".param taupr1=1e-6", "\n",
".param taunr2=1e-6", "\n",
".param Dn1=10000e-4", "\n",
".param Dn2=10000e-4", "\n",
".param Dp1=30e-4", "\n",
".param Dp2=30e-4", "\n",
".param ni=1.5e16", "\n",
".param lambda=780e-9 *light wavelength", "\n",
".param c=3e8", "\n",
".param h=6.626e-34", "\n",
".param C01=1e-12", "\n",
".param C02=1e-12", "\n",
".param Id1=100e-12", "\n",
".param Id2=100e-12", "\n",
".func sinh(x)='(exp(x)-exp(-x))/2'", "\n",
".func cosh(x)='(exp(x)+exp(-x))/2'", "\n",
  "**************************************", "\n",
  "*Absorption coefficient", "\n",
"*in (1/m) mit lambda in (m)", "\n",
"**************************************", "\n",
  ".param alphasi='((84.732e-6/lambda)-76.417)*((84.732e-6/lambda)-76.417)*1e2'", "\n",
".param alphan=alphasi", "\n",
".param alphap=alphasi", "\n",
".param alphai=alphasi", "\n",
"**************************************", "\n",
  "*Light transmission T", "\n",
"**************************************", "\n",
  ".param nsn=2.5", "\n",
".param nox=1.46", "\n",
".param nsi=4.18", "\n",
".param xsn=0*500e-9 *thickness of silicon nitrid", "\n",
".param xox=2300e-9 *thickness of oxid", "\n",
".param r1='(1-nsn)/(1+nsn)'", "\n",
".param r2='(nsn-nox)/(nsn+nox)'", "\n",
".param r3='(nox-nsi)/(nox+nsi)'", "\n",
".param A1='2*cos(4*3.14*nsn*xsn/lambda)'", "\n",
".param A2='2*cos(4*3.14*nox*xox/lambda)'", "\n",
".param A3='2*cos((4*3.14*nsn*xsn/lambda)-(4*3.14*nox*xox/lambda))'", "\n",
```

```
".param A4='2*cos((4*3.14*nsn*xsn/lambda)+(4*3.14*nox*xox/lambda))'", "\n",
".param A5='(A1*r2*(1+(r3*r3))+r3*(A4+(r2*r2*A3)))/((r2*r2)+(r3*r3)+(r2*r3*A2))'",
  "\n",
".param A6='(1+(r2*r2*r3*r3)+(r2*r3*A2))/((r2*r2)+(r3*r3)+(r2*r3*A2))'", "\n",
".param T='1-((1+(r1*r1*A6)+(r1*A5))/(A6+(r1*r1)+(r1*A5)))'", "\n", "\n",
  "*************************************", "\n",
  "*Photodiode 1", "\n",
"*************************************", "\n",
  "\n",
".param pn01='ni*ni/Nd1'", "\n",
".param np01='ni*ni/Na1'", "\n",
"\n",
  ".param Ln1='sqrt(Dn1*taun1)'", "\n",
".param Lp1='sqrt(Dp1*taup1)'", "\n",
"\n",
  ".param Wp1='xpe-sqrt((2*epsilon0*epsilonr*(phi-Vpn1))/(q*Na1*(1+(Na1/Nd1))))'", "\n",
".param Wi1='sqrt((2*epsilon0*epsilonr*(phi-Vpn1)*((1/Na1)+(1/Nd1)))/q)'", "\n",
".param Wn1='xnm-Wp1-Wi1'", "\n",
"\n",
  ".param E1='(-Vpn1+phi)/Wi1'", "\n",
".param vvn1='((E1*mun1)/(1+((mun1*E1)/vsn)))'", "\n",
".param vvp1='((E1*mup1)/(1+((mup1*E1)/vsp)))'", "\n",
"\n",
  ".param taunt1='Wi1/vvn1'", "\n",
".param taupt1='Wi1/vvp1'", "\n",
"\n",
  "*******", "\n",
  ".param Von1='(h*c)/(lambda*q*T*(1-exp(-alphap*Wp1)))'", "\n",
".param Vop1='(h*c*exp((alphap*Wp1)+
    (alphai*Wi1)))/(lambda*q*T*(1-exp(-alphan*Wn1)))'", "\n",
".param Voi1='(h*c*exp(alphap*Wp1))/(lambda*q*T*(1-exp(-alphai*Wi1)))'", "\n",
"\n",
  ".param Rp1='taup1/C01'", "\n",
".param Rn1='taun1/C01'", "\n",
".param Rpr1='taupr1/C01'", "\n",
".param Rpt1='taupt1/C01'", "\n",
"\n",
  ".param Rpd1='Rp1*(cosh(Wn1/Lp1)-1)'", "\n",
".param Rnd1='Rn1*(cosh(Wp1/Ln1)-1)'", "\n",
"\n",
  ".param Ipo1='(q*pn01*A*Lp1*(cosh(Wn1/Lp1)+1))/(taup1*sinh(Wn1/Lp1))'", "\n",
".param Ino1='(q*np01*A*Ln1*(cosh(Wp1/Ln1)+1))/(taun1*sinh(Wp1/Ln1))'", "\n",
"\n",
  ".param betap1='((lambda*q*T*alphan*Lp1*Lp1*exp(-(alphap*Wp1)-(alphai*Wi1)))/(h*
    c*(1-(alphan*alphan*Lp1*Lp1))))*(((cosh(Wn1/Lp1)+1)/(Lp1*sinh(Wn1/Lp1)))+
    ((exp(-alphan*Wn1)-1)/(alphan*Lp1*Lp1*(cosh(Wn1/Lp1)-1)))-alphan)'", "\n",
"\n",
  ".param betan1='((lambda*q*T*alphap*Ln1*Ln1)/(h*c*(1-(alphap*alphap*Ln1*Ln1))))*
    ((((cosh(Wp1/Ln1)+1)*exp(-alphap*Wp1))/(Ln1*sinh(Wp1/Ln1)))+((exp(-alphap*Wp1)-
    1)/(alphap*Ln1*Ln1*(cosh(Wp1/Ln1)-1)))+(alphap*exp(-alphap*Wp1)))'", "\n",
"\n",
  "*************************************", "\n",
  "*Photodiode 2", "\n",
"*************************************", "\n",
"\n",
  ".param pn02='ni*ni/Nd2'", "\n",
".param np02='ni*ni/Na2'", "\n",
"\n",
  ".param Ln2='sqrt(Dn2*taun2)'", "\n",
```

```
".param Lp2='sqrt(Dp2*taup2)'", "\n",
"\n",
  ".param Wn2='xne2-xnm-sqrt((2*epsilon0*epsilonr*(phi-Vpn2))/(q*Nd2*(1+(Nd2/Na2))))'",
  "\n",
".param Wp2=100e-6", "\n",
".param Wi2='sqrt((2*epsilon0*epsilonr*(phi-Vpn2)*((1/Na2)+(1/Nd2)))/q)'", "\n",
"\n",
  ".param E2='(-Vpn2+phi)/Wi2'", "\n",
".param vvn2='((E2*mun2)/(1+((mun2*E2)/vsn)))'", "\n",
".param vvp2='((E2*mup2)/(1+((mup2*E2)/vsp)))'", "\n",
  "\n",
  ".param taunt2='Wi2/vvn2'", "\n",
".param taupt2='Wi2/vvp2'", "\n",
"\n",
  "*******", "\n",
  ".param Vop2='(h*c*exp((alphap*Wp1)+(alphai*
    Wi1)+(alphan*Wn1)))/(lambda*q*T*(1-exp(-alphan*Wn2)))'", "\n",
".param Von2='(h*c*exp((alphap*Wp1)+(alphai*Wi1)+(alphan*Wn1)+(alphan*
    Wn2)+(alphai*Wi2)))/(lambda*q*T*(1-exp(-alphap*Wp2)))'", "\n",
".param Voi2='(h*c*exp((alphap*Wp1)+(alphai*Wi1)+(alphan*Wn1)+
    (alphan*Wn2)))/(lambda*q*T*(1-exp(-alphai*Wi2)))'", "\n",
"\n",
  ".param Rp2='taup2/C02'", "\n",
".param Rn2='taun2/C02'", "\n",
".param Rnr2='taunr2/C02'", "\n",
".param Rnt2='taupt2/C02'", "\n",
"\n",
  ".param Rpd2='Rp2*(cosh(Wn2/Lp2)-1)'", "\n",
".param Rnd2='Rn2*(cosh(Wp2/Ln2)-1)'", "\n",
"\n",
  ".param Ipo2='(q*pn02*A*Lp2*(cosh(Wn2/Lp2)+1))/(taup2*sinh(Wn2/Lp2))'", "\n",
".param Ino2='(q*np02*A*Ln2*(cosh(Wp2/Ln2)+1))/(taun2*sinh(Wp2/Ln2))'", "\n",
"\n",
  ".param betap2='((lambda*q*T*alphan*Lp2*Lp2*exp(-(alphap*Wp1)-(alphai*
    Wi1)-(alphan*Wn1)))/(h*c*(1-(alphan*alphan*Lp2*Lp2))))*((((cosh(Wn2/
    Lp2)+1)*exp(-alphan*Wn2))/(Lp2*sinh(Wn2/Lp2)))+((exp(-alphan*Wn2)-1)/
    (alphan*Lp2*Lp2*(cosh(Wn2/Lp2)-1)))+(alphan*exp(-alphan*Wn2)))'", "\n",
"\n",
  ".param betan2='((lambda*q*T*alphap*Ln2*Ln2*exp(-(alphap*Wp1)-
    (alphai*Wi1)-(alphan*Wn1)-(alphan*Wn2)-(alphai*Wi2)))/(h*c*(1-(alphap*
    alphap*Ln2*Ln2))))*((((cosh(Wp2/Ln2)+1))/(Ln2*sinh(Wp2/Ln2)))+((exp(
    -alphap*Wp2)-1)/(alphap*Ln2*Ln2*(cosh(Wp2/Ln2)-1)))-alphap)'", "\n",
"\n",
  "**************************************", "\n",
  "*Photodiode capacitance", "\n",
"**************************************", "\n",
  ".param Cphd1='(epsilon0*epsilonr*A)/Wi1'", "\n",
  ".param Cphd2='(epsilon0*epsilonr*A)/Wi2'", "\n",
  "\n",
  "************************************************* ", "\n",
  "* Subcircuit of the double photodiode model:", "\n",
  "************************************************* ", "\n",
  ToString[SequenceForm[".SUBCKT PDsubckt_TF_2p_2z vin ",
    PDcathode, " ", PDanode, " ", PDanode2, "\n"]], "\n",
  "******************************************", "\n",
  "*Circuit Modell for Photodiode 1", "\n",
"*******************************************", "\n",
  "\n",
  "Vion1 vin on1 dc 0", "\n",
```

```
"Viop1 vin op1 dc 0", "\n",
"Vioi1 vin oi1 dc 0", "\n",
"\n",
  "Rvon1 on1 0 Von1", "\n",
"Rvop1 op1 0 Vop1", "\n",
"Rvoi1 oi1 0 Voi1", "\n",
  "\n",
  "Fon1 0 n1 Vion1 1", "\n",
"Cn1 n1 0 C01", "\n",
"Virn1 n1 n1a dc 0", "\n",
"Rn1 n1a 0 Rn1", "\n",
"Vin1 n1 n1x dc 0 *vsource for CCCS", "\n",
"Virnd1 n1x n1xa dc 0", "\n",
"Rnd1 n1xa 0 Rnd1", "\n",
"Vino1 n1x n1xb dc 0", "\n",
"Ino1 n1xb 0 Ino1", "\n",
"Vibetan1 n1x n1xc dc 0", "\n",
"GIbetan1 n1xc 0 vin 0 betan1", "\n",
"\n",
  "Fop1 0 p1 Viop1 1", "\n",
"Cp1 p1 0 C01", "\n",
"Vrp1 p1 p1a dc 0", "\n",
"Rp1 p1a 0 Rp1", "\n",
"Vip1 p1 p1x dc 0 *vsource for CCCS", "\n",
"Vrpd1 p1x p1xa dc 0", "\n",
"Rpd1 p1xa 0 Rpd1", "\n",
"Vipo1 p1x p1xb dc 0", "\n",
"Ipo1 p1xb 0 Ipo1", "\n",
"Vibetap1 p1x p1xc dc 0", "\n",
"GIbetap1 p1xc 0 vin 0 betap1", "\n",
"\n",
  "Foi1 0 i1 Vioi1 1", "\n",
"Fip1 0 i1 Vip1 1", "\n",
"Ci1 i1 0 C01", "\n",
"Vrpr1 i1 i1a dc 0", "\n",
"Rpr1 i1a 0 Rpr1", "\n",
"Vii1 i1 i1x dc 0 *vsource for CCCS", "\n",
"Rpt1 i1x 0 Rpt1", "\n",
"\n",
  ToString[SequenceForm["Fin1 ", PDcathode, " a1x Vin1 1"]], "\n",
ToString[SequenceForm["Fii1 ", PDcathode, " a1x Vii1 1"]], "\n",
  ToString[SequenceForm["Id1 ", PDcathode, " a1x Id1"]], "\n",
  "\n",
  ToString[SequenceForm["Vimess a1xxx ", PDanode, " dc 0"]], "\n",
  "\n",
  "*******************************************", "\n",
  "*Circuit Modell for Photodiode 2", "\n",
"*******************************************", "\n",
  "\n",
  "Vion2 vin on2 dc 0", "\n",
"Viop2 vin op2 dc 0", "\n",
"Vioi2 vin oi2 dc 0", "\n",
"\n",
  "Rvon2 on2 0 Von2", "\n",
"Rvop2 op2 0 Vop2", "\n",
"Rvoi2 oi2 0 Voi2", "\n",
"\n",
  "Fon2 0 n2 Vion2 1", "\n",
"Cn2 n2 0 C02", "\n",
```

```
"Vrn2 n2 n2a dc 0", "\n",
"Rn2 n2a 0 Rn2", "\n",
"Vin2 n2 n2x dc 0 *vsource for CCCS", "\n",
"Virnd2 n2x n2xa dc 0", "\n",
"Rnd2 n2xa 0 Rnd2", "\n",
"Vino2 n2x n2xb dc 0", "\n",
"Ino2 n2xb 0 Ino2", "\n",
"Vibetan2 n2x n2xc dc 0", "\n",
"GIbetan2 n2xc 0 vin 0 betan2", "\n",
"\n",
  "Fop2 0 p2 Viop2 1", "\n",
"Cp2 p2 0 C02", "\n",
"Virp2 p2 p2a dc 0", "\n",
"Rp2 p2a 0 Rp2", "\n",
"Vip2 p2 p2x dc 0 *vsource for CCCS", "\n",
"virpd2 p2x p2xa dc 0", "\n",
"Rpd2 p2xa 0 Rpd2", "\n",
"Vipo2 p2x p2xb dc 0", "\n",
"Ipo2 p2xb 0 Ipo2", "\n",
"Vibetap2 p2x p2xc dc 0", "\n",
"GIbetap2 p2xc 0 vin 0 betap2", "\n",
"\n",
  "Foi2 0 i2 Vioi2 1", "\n",
"Fin2 0 i2 Vin2 1", "\n",
"Ci2 i2 0 C02", "\n",
"Virnr2 i2 i2a dc 0", "\n",
"Rnr2 i2a 0 Rnr2", "\n",
"Vii2 i2 i2x dc 0 *vsource for CCCS", "\n",
"Rnt2 i2x 0 Rnt2", "\n",
"\n",
  ToString[SequenceForm["Fip2 ", PDcathode, " a2x Vip2 1"]], "\n",
ToString[SequenceForm["Fii2 ", PDcathode, " a2x Vii2 1"]], "\n",
  ToString[SequenceForm["Id2 ", PDcathode, " a2x Id2"]], "\n",
"\n",
  "Vimess_pd2 a2x a2xx dc 0", "\n",
"\n",
  "******************************************************** ", "\n",
  "**** SPICE Model of simplified network model         *** ", "\n",
  "******************************************************** ", "\n",
  "\n",
  "***** Photodiode PD1:", "\n",
  "\n",
  ToString[SequenceForm["C1 ", PDcathode, " a1xx ", c1]], "\n",
  ToString[SequenceForm["R1 a1x a1xx ", r1]], "\n",
  ToString[SequenceForm["C2 ", PDcathode, " a1xx ", c2]], "\n",
  ToString[SequenceForm["R2 a1xx a1xxx ", r2]], "\n",
  ToString[SequenceForm["C3 ", PDcathode, " a1xxx ", c3]], "\n",
  "\n",
  "***** Photodiode PD2:", "\n",
  ToString[SequenceForm["Cphd2 ", PDcathode, " a2x Cphd2"]], "\n",
  ToString[SequenceForm["Rphd2 a2xx ", PDanode2,
    " 20  * estimated series resistor for anode of PD2"]], "\n",
  "\n",
  ".ends", "\n",
  "\n",
  "******************************************************************", "\n",
  "* Subcircuit call of photodiode model. Name of subcircuit is: XPD\n",
  "******************************************************************", "\n",
  ToString[SequenceForm["XPD vin ", PDcathode, " ",
```

```
    PDanode, " ", PDanode2, " PDsubckt_TF_2p_2z", "\n", "\n"]], "\n", "\n"
];
Close[outputstream];
```

Schreiben einer Netzliste eines Subcircuit Modells mit einem dominanten Pol :

```
In[70]:= outputstream = OpenWrite["PDsubckt_TF_1p"];

WriteString[outputstream,
  "*#################################################################\n",
  "*# SPICE Subcircuit of B6CA Double-Photodiode with 1 pole       #\n",
  "*#################################################################\n",
  "* by J.Sturm (2005)\n",
  "* The SPICE model of the double photodiode consists of a simplified R-C-I model ",
  "\n",
  "* The R-C Model for the upper photodiode PD1 is
    extracted from the photodiode network model.", "\n",
  "* It models one dominant pole with a resitor Rpd1 and Cpd1.", "\n",
  "* The Model for the lower (substrate) photodiode
    PD2 is a single fixed resistor Rpd2 and capacitor Cpd2.", "\n",
  "* The photodiode current for Pd1 and PD2 is represented by a
    SPICE model for the drift and diffusion currents. ", "\n",
  "* The pole of the transferfunction is:\n",
  ToString[SequenceForm["* Pole: ", CForm[Abs[poTF[[1]]]]]], "\n",
  "* Input pins:\n",
  "* vin  =  input pin for light intensity in W\n",
  "* The vin pin must be connected by an external voltage source to 0.\n", "\n",
  "* Output pins:\n",
  ToString[SequenceForm["* ", PDcathode, ", ", PDanode, " ", PDanode2,
    " = Photodiode cathode and anode1 (PD1) and anode2 (PD2)"]], "\n",
  "\n",
  "* The photodiode model in this netlist is given as subcircuit:", "\n",
  "* .SUBCKT PDsubckt_TF_1p vin PDcathode PDanode PDanode2", "\n",
  "* XPD vin PDcathode PDanode PDanode2 PDsubckt_TF_1p", "\n",
  "\n",
  "************************************************ ", "\n",
  "**** SPICE Model of Drift/Diffusion currents *** ", "\n",
  "************************************************ ", "\n",
  "\n",
  "******************************", "\n",
  "*Parameters", "\n",
"******************************", "\n",
  ToString[SequenceForm[".param A=", areapd, "e-6 *photodiode area in m2"]], "\n",
".param xpe=0.3e-6", "\n",
".param xne1=2e-6", "\n",
".param xne2=4e-6", "\n",
".param xnm=3e-6", "\n",
".param Na1=1e24 *p-Base doping concentration", "\n",
".param Na2=2e21 *p-Substrate doping concentration", "\n",
".param Nd1=2e21 *n-Epi doping concentration", "\n",
".param Nd2=2e25 *n-BL doping concentration", "\n",
".param phi=0.8", "\n",
".param epsilon0=8.85e-12", "\n",
".param epsilonr=12", "\n",
".param q=1.6e-19", "\n",
".param Vpn1=-3 *pn-junction reverse voltage of pd1", "\n",
".param Vpn2=-3 *pn-junction reverse voltage of pd2", "\n",
".param mun1=1300e-4", "\n",
".param mun2=1300e-4", "\n",
```

```
".param mup1=500e-4", "\n",
".param mup2=500e-4", "\n",
".param Eth=3.5e5", "\n",
".param vsn=1e5", "\n",
".param vsp=1e5", "\n",
".param taun1=1e-6", "\n",
".param taun2=1e-6", "\n",
".param taup1=1e-6", "\n",
".param taup2=1e-6", "\n",
".param taupr1=1e-6", "\n",
".param taunr2=1e-6", "\n",
".param Dn1=10000e-4", "\n",
".param Dn2=10000e-4", "\n",
".param Dp1=30e-4", "\n",
".param Dp2=30e-4", "\n",
".param ni=1.5e16", "\n",
".param lambda=780e-9 *light wavelength", "\n",
".param c=3e8", "\n",
".param h=6.626e-34", "\n",
".param C01=1e-12", "\n",
".param C02=1e-12", "\n",
".param Id1=100e-12", "\n",
".param Id2=100e-12", "\n",
".func sinh(x)='(exp(x)-exp(-x))/2'", "\n",
".func cosh(x)='(exp(x)+exp(-x))/2'", "\n",
  "*************************************", "\n",
  "*Absorption coefficient", "\n",
"*in (1/m) mit lambda in (m)", "\n",
"*************************************", "\n",
  ".param alphasi='((84.732e-6/lambda)-76.417)*((84.732e-6/lambda)-76.417)*1e2'", "\n",
".param alphan=alphasi", "\n",
".param alphap=alphasi", "\n",
".param alphai=alphasi", "\n",
"*************************************", "\n",
  "*Light transmission T", "\n",
"*************************************", "\n",
  ".param nsn=2.5", "\n",
".param nox=1.46", "\n",
".param nsi=4.18", "\n",
".param xsn=0*500e-9 *thickness of silicon nitrid", "\n",
".param xox=2300e-9 *thickness of oxid", "\n",
".param r1='(1-nsn)/(1+nsn)'", "\n",
".param r2='(nsn-nox)/(nsn+nox)'", "\n",
".param r3='(nox-nsi)/(nox+nsi)'", "\n",
".param A1='2*cos(4*3.14*nsn*xsn/lambda)'", "\n",
".param A2='2*cos(4*3.14*nox*xox/lambda)'", "\n",
".param A3='2*cos((4*3.14*nsn*xsn/lambda)-(4*3.14*nox*xox/lambda))'", "\n",
".param A4='2*cos((4*3.14*nsn*xsn/lambda)+(4*3.14*nox*xox/lambda))'", "\n",
".param A5='(A1*r2*(1+(r3*r3))+r3*(A4+(r2*r2*A3)))/((r2*r2)+(r3*r3)+(r2*r3*A2))'",
  "\n",
".param A6='(1+(r2*r2*r3*r3)+(r2*r3*A2))/((r2*r2)+(r3*r3)+(r2*r3*A2))'", "\n",
".param T='1-((1+(r1*r1*A6)+(r1*A5))/(A6+(r1*r1)+(r1*A5)))'", "\n", "\n",
  "*************************************", "\n",
  "*Photodiode 1", "\n",
"*************************************", "\n",
  "\n",
".param pn01='ni*ni/Nd1'", "\n",
".param np01='ni*ni/Na1'", "\n",
"\n",
```

```
  ".param Ln1='sqrt(Dn1*taun1)'", "\n",
".param Lp1='sqrt(Dp1*taup1)'", "\n",
"\n",
  ".param Wp1='xpe-sqrt((2*epsilon0*epsilonr*(phi-Vpn1))/(q*Na1*(1+(Na1/Nd1))))'", "\n",
".param Wi1='sqrt((2*epsilon0*epsilonr*(phi-Vpn1)*((1/Na1)+(1/Nd1)))/q)'", "\n",
".param Wn1='xnm-Wp1-Wi1'", "\n",
"\n",
  ".param E1='(-Vpn1+phi)/Wi1'", "\n",
".param vvn1='((E1*mun1)/(1+((mun1*E1)/vsn)))'", "\n",
".param vvp1='((E1*mup1)/(1+((mup1*E1)/vsp)))'", "\n",
"\n",
  ".param taunt1='Wi1/vvn1'", "\n",
".param taupt1='Wi1/vvp1'", "\n",
"\n",
  "*******", "\n",
  ".param Von1='(h*c)/(lambda*q*T*(1-exp(-alphap*Wp1)))'", "\n",
".param Vop1='(h*c*exp((alphap*Wp1)+
    (alphai*Wi1)))/(lambda*q*T*(1-exp(-alphan*Wn1)))'", "\n",
".param Voi1='(h*c*exp(alphap*Wp1))/(lambda*q*T*(1-exp(-alphai*Wi1)))'", "\n",
"\n",
  ".param Rp1='taup1/C01'", "\n",
".param Rn1='taun1/C01'", "\n",
".param Rpr1='taupr1/C01'", "\n",
".param Rpt1='taupt1/C01'", "\n",
"\n",
  ".param Rpd1='Rp1*(cosh(Wn1/Lp1)-1)'", "\n",
".param Rnd1='Rn1*(cosh(Wp1/Ln1)-1)'", "\n",
"\n",
  ".param Ipo1='(q*pn01*A*Lp1*(cosh(Wn1/Lp1)+1))/(taup1*sinh(Wn1/Lp1))'", "\n",
".param Ino1='(q*np01*A*Ln1*(cosh(Wp1/Ln1)+1))/(taun1*sinh(Wp1/Ln1))'", "\n",
"\n",
  ".param betap1='((lambda*q*T*alphan*Lp1*Lp1*exp(-(alphap*Wp1)-(alphai*Wi1)))/(h*
    c*(1-(alphan*alphan*Lp1*Lp1))))*(((cosh(Wn1/Lp1)+1)/(Lp1*sinh(Wn1/Lp1)))+
    ((exp(-alphan*Wn1)-1)/(alphan*Lp1*Lp1*(cosh(Wn1/Lp1)-1)))-alphan)'", "\n",
"\n",
  ".param betan1='((lambda*q*T*alphap*Ln1*Ln1)/(h*c*(1-(alphap*alphap*Ln1*Ln1))))*
    ((((cosh(Wp1/Ln1)+1)*exp(-alphap*Wp1))/(Ln1*sinh(Wp1/Ln1)))+((exp(-alphap*Wp1)-
    1)/(alphap*Ln1*Ln1*(cosh(Wp1/Ln1)-1)))+(alphap*exp(-alphap*Wp1)))'", "\n",
"\n",
  "*************************************", "\n",
  "*Photodiode 2", "\n",
"*************************************", "\n",
"\n",
  ".param pn02='ni*ni/Nd2'", "\n",
".param np02='ni*ni/Na2'", "\n",
"\n",
  ".param Ln2='sqrt(Dn2*taun2)'", "\n",
".param Lp2='sqrt(Dp2*taup2)'", "\n",
"\n",
  ".param Wn2='xne2-xnm-sqrt((2*epsilon0*epsilonr*(phi-Vpn2))/(q*Nd2*(1+(Nd2/Na2))))'",
  "\n",
".param Wp2=100e-6", "\n",
".param Wi2='sqrt((2*epsilon0*epsilonr*(phi-Vpn2)*((1/Na2)+(1/Nd2)))/q)'", "\n",
"\n",
  ".param E2='(-Vpn2+phi)/Wi2'", "\n",
".param vvn2='((E2*mun2)/(1+((mun2*E2)/vsn)))'", "\n",
".param vvp2='((E2*mup2)/(1+((mup2*E2)/vsp)))'", "\n",
  "\n",
  ".param taunt2='Wi2/vvn2'", "\n",
```

```
".param taupt2='Wi2/vvp2'", "\n",
"\n",
  "*******", "\n",
  ".param Vop2='(h*c*exp((alphap*Wp1)+(alphai*
    Wi1)+(alphan*Wn1)))/(lambda*q*T*(1-exp(-alphan*Wn2)))'", "\n",
".param Von2='(h*c*exp((alphap*Wp1)+(alphai*Wi1)+(alphan*Wn1)+(alphan*
    Wn2)+(alphai*Wi2)))/(lambda*q*T*(1-exp(-alphap*Wp2)))'", "\n",
".param Voi2='(h*c*exp((alphap*Wp1)+(alphai*Wi1)+(alphan*Wn1)+
    (alphan*Wn2)))/(lambda*q*T*(1-exp(-alphai*Wi2)))'", "\n",
"\n",
  ".param Rp2='taup2/C02'", "\n",
".param Rn2='taun2/C02'", "\n",
".param Rnr2='taunr2/C02'", "\n",
".param Rnt2='taupt2/C02'", "\n",
"\n",
  ".param Rpd2='Rp2*(cosh(Wn2/Lp2)-1)'", "\n",
".param Rnd2='Rn2*(cosh(Wp2/Ln2)-1)'", "\n",
"\n",
  ".param Ipo2='(q*pn02*A*Lp2*(cosh(Wn2/Lp2)+1))/(taup2*sinh(Wn2/Lp2))'", "\n",
".param Ino2='(q*np02*A*Ln2*(cosh(Wp2/Ln2)+1))/(taun2*sinh(Wp2/Ln2))'", "\n",
"\n",
  ".param betap2='((lambda*q*T*alphan*Lp2*Lp2*exp(-(alphap*Wp1)-(alphai*
    Wi1)-(alphan*Wn1)))/(h*c*(1-(alphan*alphan*Lp2*Lp2))))*((((cosh(Wn2/
    Lp2)+1)*exp(-alphan*Wn2))/(Lp2*sinh(Wn2/Lp2)))+((exp(-alphan*Wn2)-1)/
    (alphan*Lp2*Lp2*(cosh(Wn2/Lp2)-1)))+(alphan*exp(-alphan*Wn2)))'", "\n",
"\n",
  ".param betan2='((lambda*q*T*alphap*Ln2*Ln2*exp(-(alphap*Wp1)-
    (alphai*Wi1)-(alphan*Wn1)-(alphan*Wn2)-(alphai*Wi2)))/(h*c*(1-(alphap*
    alphap*Ln2*Ln2))))*((((cosh(Wp2/Ln2)+1))/(Ln2*sinh(Wp2/Ln2)))+((exp(
    -alphap*Wp2)-1)/(alphap*Ln2*Ln2*(cosh(Wp2/Ln2)-1)))-alphap)'", "\n",
"\n",
  "***************************************", "\n",
  "*Photodiode capacitance", "\n",
"***************************************", "\n",
  ".param Cphd1='(epsilon0*epsilonr*A)/Wi1'", "\n",
  ".param Cphd2='(epsilon0*epsilonr*A)/Wi2'", "\n",
  "\n",
  "*************************************************** ", "\n",
  "* Subcircuit of the double photodiode model:", "\n",
  "*************************************************** ", "\n",
  ToString[SequenceForm[".SUBCKT PDsubckt_TF_1p vin ",
    PDcathode, " ", PDanode, " ", PDanode2, "\n"]], "\n",
  "******************************************", "\n",
  "*Circuit Modell for Photodiode 1", "\n",
"******************************************", "\n",
  "\n",
  "Vion1 vin on1 dc 0", "\n",
"Viop1 vin op1 dc 0", "\n",
"Vioi1 vin oi1 dc 0", "\n",
"\n",
  "Rvon1 on1 0 Von1", "\n",
"Rvop1 op1 0 Vop1", "\n",
"Rvoi1 oi1 0 Voi1", "\n",
  "\n",
  "Fon1 0 n1 Vion1 1", "\n",
"Cn1 n1 0 C01", "\n",
"Virn1 n1 n1a dc 0", "\n",
"Rn1 n1a 0 Rn1", "\n",
"Vin1 n1 n1x dc 0 *vsource for CCCS", "\n",
```

```
"Virnd1 n1x n1xa dc 0", "\n",
"Rnd1 n1xa 0 Rnd1", "\n",
"Vino1 n1x n1xb dc 0", "\n",
"Ino1 n1xb 0 Ino1", "\n",
"Vibetan1 n1x n1xc dc 0", "\n",
"GIbetan1 n1xc 0 vin 0 betan1", "\n",
"\n",
  "Fop1 0 p1 Viop1 1", "\n",
"Cp1 p1 0 C01", "\n",
"Vrp1 p1 p1a dc 0", "\n",
"Rp1 p1a 0 Rp1", "\n",
"Vip1 p1 p1x dc 0 *vsource for CCCS", "\n",
"Vrpd1 p1x p1xa dc 0", "\n",
"Rpd1 p1xa 0 Rpd1", "\n",
"Vipo1 p1x p1xb dc 0", "\n",
"Ipo1 p1xb 0 Ipo1", "\n",
"Vibetap1 p1x p1xc dc 0", "\n",
"GIbetap1 p1xc 0 vin 0 betap1", "\n",
"\n",
  "Foi1 0 i1 Vioi1 1", "\n",
"Fip1 0 i1 Vip1 1", "\n",
"Ci1 i1 0 C01", "\n",
"Vrpr1 i1 i1a dc 0", "\n",
"Rpr1 i1a 0 Rpr1", "\n",
"Vii1 i1 i1x dc 0 *vsource for CCCS", "\n",
"Rpt1 i1x 0 Rpt1", "\n",
"\n",
  ToString[SequenceForm["Fin1 ", PDcathode, " a1x Vin1 1"]], "\n",
ToString[SequenceForm["Fii1 ", PDcathode, " a1x Vii1 1"]], "\n",
  ToString[SequenceForm["Id1 ", PDcathode, " a1x Id1"]], "\n",
  "\n",
  "Vimess_pd1 a1x a1xx dc 0", "\n",
  "\n",
  "*******************************************", "\n",
  "*Circuit Modell for Photodiode 2", "\n",
"*******************************************", "\n",
  "\n",
  "Vion2 vin on2 dc 0", "\n",
"Viop2 vin op2 dc 0", "\n",
"Vioi2 vin oi2 dc 0", "\n",
"\n",
  "Rvon2 on2 0 Von2", "\n",
"Rvop2 op2 0 Vop2", "\n",
"Rvoi2 oi2 0 Voi2", "\n",
"\n",
  "Fon2 0 n2 Vion2 1", "\n",
"Cn2 n2 0 C02", "\n",
"Vrn2 n2 n2a dc 0", "\n",
"Rn2 n2a 0 Rn2", "\n",
"Vin2 n2 n2x dc 0 *vsource for CCCS", "\n",
"Virnd2 n2x n2xa dc 0", "\n",
"Rnd2 n2xa 0 Rnd2", "\n",
"Vino2 n2x n2xb dc 0", "\n",
"Ino2 n2xb 0 Ino2", "\n",
"Vibetan2 n2x n2xc dc 0", "\n",
"GIbetan2 n2xc 0 vin 0 betan2", "\n",
"\n",
  "Fop2 0 p2 Viop2 1", "\n",
"Cp2 p2 0 C02", "\n",
```

```
"Virp2 p2 p2a dc 0", "\n",
"Rp2 p2a 0 Rp2", "\n",
"Vip2 p2 p2x dc 0 *vsource for CCCS", "\n",
"virpd2 p2x p2xa dc 0", "\n",
"Rpd2 p2xa 0 Rpd2", "\n",
"Vipo2 p2x p2xb dc 0", "\n",
"Ipo2 p2xb 0 Ipo2", "\n",
"Vibetap2 p2x p2xc dc 0", "\n",
"GIbetap2 p2xc 0 vin 0 betap2", "\n",
"\n",
  "Foi2 0 i2 Vioi2 1", "\n",
"Fin2 0 i2 Vin2 1", "\n",
"Ci2 i2 0 C02", "\n",
"Virnr2 i2 i2a dc 0", "\n",
"Rnr2 i2a 0 Rnr2", "\n",
"Vii2 i2 i2x dc 0 *vsource for CCCS", "\n",
"Rnt2 i2x 0 Rnt2", "\n",
"\n",
  ToString[SequenceForm["Fip2 ", PDcathode, " a2x Vip2 1"]], "\n",
ToString[SequenceForm["Fii2 ", PDcathode, " a2x Vii2 1"]], "\n",
  ToString[SequenceForm["Id2 ", PDcathode, " a2x Id2"]], "\n",
"\n",
  "Vimess_pd2 a2x a2xx dc 0", "\n",
"\n",
  "******************************************************** ", "\n",
  "**** SPICE Model of simplified network model         *** ", "\n",
  "******************************************************** ", "\n",
  "\n",
  "***** Photodiode PD1:", "\n",
  ToString[SequenceForm["Cphd1 ", PDcathode, " a1x Cphd1"]], "\n",
  ToString[SequenceForm["Rphd1 a1xx ", PDanode, " ", rpol1]], "\n",
  "\n",
  "***** Photodiode PD2:", "\n",
  ToString[SequenceForm["Cphd2 ", PDcathode, " a2x Cphd2"]], "\n",
  ToString[SequenceForm["Rphd2 a2xx ", PDanode2,
    " 20  * estimated series resistor for anode of PD2"]], "\n",
  "\n",
  ".ends", "\n",
  "\n",
  "******************************************************************", "\n",
  "* Subcircuit call of photodiode model. Name of subcircuit is: XPD\n",
  "******************************************************************", "\n",
  ToString[SequenceForm["XPD vin ", PDcathode, " ",
    PDanode, " ", PDanode2, " PDsubckt_TF_1p", "\n", "\n"]], "\n", "\n"
];
Close[outputstream];
```

Appendix B

SPICE Netlist for Drift and Diffusion Model

Following pages show a SPICE netlist for a double photodiode drift and diffusion circuit model. The netlist is automatically generated by the *'Photodiode Designer' (PDes)* tool. It is defined as SPICE subcircuit and can directly be used for simulation with an analog simulator.

```
******************************************************
* Photodiode circuit model including
* photodiode pins:
* vin = voltage source representing input light intensity
* k = photodiode cathode
* a1 = anode of photodiode PD1
* a2 = anode of photodiode PD2
*
* sth, 04.2005
******************************
* Parameters
******************************
.param A = 1e-6  * photodiode area in m2
.param xpe = 0.3e-6
.param xne1 = 2e-6
.param xne2 = 4e-6
.param xnm = 3e-6
.param Na1 = 1e24 *p-Base doping concentration
.param Na2 = 2e21 *p-Substrate doping concentration
.param Nd1 = 2e21 *n-Epi doping concentration
.param Nd2 = 2e25 *n-BL doping concentration
.param phi = 0.8
.param epsilon0 = 8.85e-12
.param epsilonr = 12
.param q = 1.6e-19
.param Vpn1 = -3  *pn-junction reverse voltage of pd1
.param Vpn2 = -3  *pn-junction reverse voltage of pd2
.param mun1 = 1300e-4
.param mun2 = 1300e-4
.param mup1 = 500e-4
.param mup2 = 500e-4
.param Eth = 3.5e5
.param vsn = 1e5
.param vsp = 1e5
.param taun1 = 1e-6
.param taun2 = 1e-6
.param taup1 = 1e-6
.param taup2 = 1e-6
.param taupr1 = 1e-6
.param taunr2 = 1e-6
.param Dn1 = 10000e-4
.param Dn2 = 10000e-4
.param Dp1 = 30e-4
.param Dp2 = 30e-4
.param ni = 1.5e16
.param lambda = 780e-9  *light wavelength
.param c = 3e8
.param h = 6.626e-34
.param C01 = 1e-12
.param C02 = 1e-12
.param Id1 = 100e-12
.param Id2 = 100e-12

.func sinh(x) = '(exp(x)-exp(-x))/2'
.func cosh(x) = '(exp(x)+exp(-x))/2'

**************************************
* Absorption coefficient
* in (1/m) mit lambda in (m)
**************************************
.param alphasi='((84.732e-6/lambda)-76.417)*((84.732e-6/lambda)-
76.417)*1e2'

.param alphan = alphasi
```

```
.param alphap = alphasi
.param alphai = alphasi

**************************************
* Light transmission T
**************************************
.param nsn=2.5
.param nox=1.46
.param nsi=4.18
.param xsn=0 *500e-9   *thickness of silicon nitrid
.param xox=2300e-9     *thickness of oxid

.param r1='(1-nsn)/(1+nsn)'
.param r2='(nsn-nox)/(nsn+nox)'
.param r3='(nox-nsi)/(nox+nsi)'
.param A1='2*cos(4*3.14*nsn*xsn/lambda)'
.param A2='2*cos(4*3.14*nox*xox/lambda)'
.param A3='2*cos((4*3.14*nsn*xsn/lambda)-(4*3.14*nox*xox/lambda))'
.param A4='2*cos((4*3.14*nsn*xsn/lambda)+(4*3.14*nox*xox/lambda))'
.param A5='(A1*r2*(1+(r3*r3))+r3*(A4+(r2*r2*A3)))/((r2*r2)+(r3*r3)+
(r2*r3*A2))'
.param A6='(1+(r2*r2*r3*r3)+(r2*r3*A2))/((r2*r2)+(r3*r3)+(r2*r3*A2))'

.param T='1-((1+(r1*r1*A6)+(r1*A5))/(A6+(r1*r1)+(r1*A5)))'

*************************************
* Subcircuit of photodiode model
*************************************
.SUBCKT pd_mod_subckt vin k a1 a2

**************************************
* Photodiode 1
**************************************
.param Cpd1 = 1p

.param pn01 = 'ni*ni/Nd1'
.param np01 = 'ni*ni/Na1'

.param Ln1 = 'sqrt(Dn1*taun1)'
.param Lp1 = 'sqrt(Dp1*taup1)'

.param Wp1 = 'xpe - sqrt((2*epsilon0*epsilonr*(phi-Vpn1))/(q*Na1*(1+
(Na1/Nd1))))'
.param Wi1 = 'sqrt((2*epsilon0*epsilonr*(phi-Vpn1)*((1/Na1)+
(1/Nd1)))/q)'
.param Wn1 = 'xnm - Wp1 - Wi1'

.param E1 = '(-Vpn1 + phi) / Wi1'
.param vvn1 = '((E1*mun1)/(1+((mun1*E1)/vsn)))'
.param vvp1 = '((E1*mup1)/(1+((mup1*E1)/vsp)))'

.param taunt1 = 'Wi1 / vvn1'
.param taupt1 = 'Wi1 / vvp1'

*******

.param Von1 = '(h*c) / (lambda*q*T*(1-exp(-alphap*Wp1)))'
.param Vop1 = '(h*c*exp((alphap*Wp1)+(alphai*Wi1))) / (lambda*q*T*(1-
exp(-alphan*Wn1)))'
.param Voi1 = '(h*c*exp(alphap*Wp1)) / (lambda*q*T*(1-exp(-
alphai*Wi1)))'

.param Rp1 = 'taup1 / C01'
.param Rn1 = 'taun1 / C01'
```

```
.param Rpr1 = 'taupr1 / C01'
.param Rpt1 = 'taupt1 / C01'

.param Rpd1 = 'Rp1*(cosh(Wn1/Lp1) - 1)'
.param Rnd1 = 'Rn1*(cosh(Wp1/Ln1) - 1)'

.param Ipo1 = '(q*pn01*A*Lp1*(cosh(Wn1/Lp1)+1))/(taup1*sinh
(Wn1/Lp1))'
.param Ino1 = '(q*np01*A*Ln1*(cosh(Wp1/Ln1)+1))/(taun1*sinh
(Wp1/Ln1))'

.param betap1 = '((lambda*q*T*alphan*Lp1*Lp1*exp(-(alphap*Wp1)-
(alphai*Wi1)))/(h*c*(1-(alphan*alphan*Lp1*Lp1)))) * (((cosh(Wn1/Lp1)+
1)/(Lp1*sinh(Wn1/Lp1))) + ((exp(-alphan*Wn1)-1)/(alphan*Lp1*Lp1*(cosh
(Wn1/Lp1)-1))) - alphan)'

.param betan1 = '((lambda*q*T*alphap*Ln1*Ln1)/(h*c*(1-
(alphap*alphap*Ln1*Ln1)))) * ((((cosh(Wp1/Ln1)+1)*exp(-alphap*Wp1))/
(Ln1*sinh(Wp1/Ln1))) + ((exp(-alphap*Wp1)-1)/(alphap*Ln1*Ln1*(cosh
(Wp1/Ln1)-1))) + (alphap*exp(-alphap*Wp1)))'

**************************************
* Photodiode 2
**************************************
.param Cpd2 = 1p

.param pn02 = 'ni*ni/Nd2'
.param np02 = 'ni*ni/Na2'

.param Ln2 = 'sqrt(Dn2*taun2)'
.param Lp2 = 'sqrt(Dp2*taup2)'

.param Wn2 = 'xne2 - xnm - sqrt((2*epsilon0*epsilonr*(phi-Vpn2))/
(q*Nd2*(1+(Nd2/Na2))))'
.param Wp2 = 100e-6
.param Wi2= 'sqrt((2*epsilon0*epsilonr*(phi-Vpn2)*((1/Na2)+
(1/Nd2)))/q)'

.param E2 = '(-Vpn2 + phi) / Wi2'
.param vvn2 = '((E2*mun2)/(1+((mun2*E2)/vsn)))'
.param vvp2 = '((E2*mup2)/(1+((mup2*E2)/vsp)))'


.param taunt2 = 'Wi2 / vvn2'
.param taupt2 = 'Wi2 / vvp2'

*******

.param Vop2 = '(h*c*exp((alphap*Wp1)+(alphai*Wi1)+(alphan*Wn1))) /
(lambda*q*T*(1-exp(-alphan*Wn2)))'
.param Von2 = '(h*c*exp((alphap*Wp1)+(alphai*Wi1)+(alphan*Wn1)+
(alphan*Wn2)+(alphai*Wi2))) / (lambda*q*T*(1-exp(-alphap*Wp2)))'
.param Voi2 = '(h*c*exp((alphap*Wp1)+(alphai*Wi1)+(alphan*Wn1)+
(alphan*Wn2))) / (lambda*q*T*(1-exp(-alphai*Wi2)))'

.param Rp2 = 'taup2 / C02'
.param Rn2 = 'taun2 / C02'
.param Rnr2 = 'taunr2 / C02'
.param Rnt2 = 'taupt2 / C02'

.param Rpd2 = 'Rp2*(cosh(Wn2/Lp2) - 1)'
.param Rnd2 = 'Rn2*(cosh(Wp2/Ln2) - 1)'

.param Ipo2 = '(q*pn02*A*Lp2*(cosh(Wn2/Lp2)+1))/(taup2*sinh
```

```
(Wn2/Lp2))'
.param Ino2 = '(q*np02*A*Ln2*(cosh(Wp2/Ln2)+1))/(taun2*sinh
(Wp2/Ln2))'

.param betap2 = '((lambda*q*T*alphan*Lp2*Lp2*exp(-(alphap*Wp1)-
(alphai*Wi1)-(alphan*Wn1)))/(h*c*(1-(alphan*alphan*Lp2*Lp2)))) *
((((cosh(Wn2/Lp2)+1)*exp(-alphan*Wn2))/(Lp2*sinh(Wn2/Lp2))) + ((exp(-
alphan*Wn2)-1)/(alphan*Lp2*Lp2*(cosh(Wn2/Lp2)-1))) + (alphan*exp(-
alphan*Wn2)))'

.param betan2 = '((lambda*q*T*alphap*Ln2*Ln2*exp(-(alphap*Wp1)-
(alphai*Wi1)-(alphan*Wn1)-(alphan*Wn2)-(alphai*Wi2)))/(h*c*(1-
(alphap*alphap*Ln2*Ln2)))) * ((((cosh(Wp2/Ln2)+1))/(Ln2*sinh
(Wp2/Ln2))) + ((exp(-alphap*Wp2)-1)/(alphap*Ln2*Ln2*(cosh(Wp2/Ln2)-
1))) - alphap)'

******************************************
* Circuit Modell for Photodiode 1
*******************************************
****** model *******
Vion1 vin on1 dc 0
Viop1 vin op1 dc 0
Vioi1 vin oi1 dc 0

Rvon1 on1 0 Von1
Rvop1 op1 0 Vop1
Rvoi1 oi1 0 Voi1


Fon1 0 n1 Vion1 1
Cn1 n1 0 C01
Virn1 n1 n1a dc 0
Rn1 n1a 0 Rn1
Vin1 n1 n1x dc 0 * vsource for CCCS
Virnd1 n1x n1xa dc 0
Rnd1 n1xa 0 Rnd1
Vino1 n1x n1xb dc 0
Ino1 n1xb 0 Ino1
Vibetan1 n1x n1xc dc 0
GIbetan1 n1xc 0 vin 0 betan1

Fop1 0 p1 Viop1 1
Cp1 p1 0 C01
Vrp1 p1 p1a dc 0
Rp1 p1a 0 Rp1
Vip1 p1 p1x dc 0  * vsource for CCCS
Vrpd1 p1x p1xa dc 0
Rpd1 p1xa 0 Rpd1
Vipo1 p1x p1xb dc 0
Ipo1 p1xb 0 Ipo1
Vibetap1 p1x p1xc dc 0
GIbetap1 p1xc 0 vin 0 betap1

Foi1 0 i1 Vioi1 1
Fip1 0 i1 Vip1 1
Ci1 i1 0 C01
Vrpr1 i1 i1a dc 0
Rpr1 i1a 0 Rpr1
Vii1 i1 i1x dc 0 * vsource for CCCS
Rpt1 i1x 0 Rpt1

Fin1 k a1x Vin1 1
Fii1 k a1x Vii1 1
Id1 k a1x Id1
```

```
Cpd1 k a1x Cpd1

******************************************
* Circuit Modell for Photodiode 2
*******************************************
****** model *******
Vion2 vin on2 dc 0
Viop2 vin op2 dc 0
Vioi2 vin oi2 dc 0

Rvon2 on2 0 Von2
Rvop2 op2 0 Vop2
Rvoi2 oi2 0 Voi2

Fon2 0 n2 Vion2 1
Cn2 n2 0 C02
Vrn2 n2 n2a dc 0
Rn2 n2a 0 Rn2
Vin2 n2 n2x dc 0 * vsource for CCCS
Virnd2 n2x n2xa dc 0
Rnd2 n2xa 0 Rnd2
Vino2 n2x n2xb dc 0
Ino2 n2xb 0 Ino2
Vibetan2 n2x n2xc dc 0
GIbetan2 n2xc 0 vin 0 betan2

Fop2 0 p2 Viop2 1
Cp2 p2 0 C02
Virp2 p2 p2a dc 0
Rp2 p2a 0 Rp2
Vip2 p2 p2x dc 0  * vsource for CCCS
virpd2 p2x p2xa dc 0
Rpd2 p2xa 0 Rpd2
Vipo2 p2x p2xb dc 0
Ipo2 p2xb 0 Ipo2
Vibetap2 p2x p2xc dc 0
GIbetap2 p2xc 0 vin 0 betap2

Foi2 0 i2 Vioi2 1
Fin2 0 i2 Vin2 1
Ci2 i2 0 C02
Virnr2 i2 i2a dc 0
Rnr2 i2a 0 Rnr2
Vii2 i2 i2x dc 0 * vsource for CCCS
Rnt2 i2x 0 Rnt2

Fip2 k a2x Vip2 1
Fii2 k a2x Vii2 1
Id2 k a2x Id2
Cpd2 k a2x Cpd2

Vimess_pd1 a1x a1 dc 0
Vimess_pd2 a2x a2 dc 0

.ends

****************************************************************
* Subcircuit call of photodiodemodel. Name of subcircuit is: XPD
****************************************************************
XPD vin k a1 a2 pd_mod_subckt
```

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Curriculum Vitae

Name: Dipl.-Ing STURM Johannes Karl

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Education:

1982 - 1987	Höhere Technische Lehranstalt für Elektrotechnik Klagenfurt - Austria
1988 - 1995	Technological University of Graz - Technical Physics Dipl.-Ing degree from department of Solid-State-Physics: "*Optoelektronische Eigenschaften konjugierter Polymere*"
01. - 04.1995	Research at University of Leipzig
07. - 09.1995	Research Center of France Telecom (CNET), Paris

Work Experience:

1996 - 1999	Siemens Semiconductors, Villach Process engineer for plasma-etching
Since 1999	Infineon Technologies, Villach Analog and mixed signal IC design for integrated sensor IC's Concept engineering for high-speed CMOS mixed signal circuits

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