ADVANCED ELECTRONIC MATERIALS

Supporting Information

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Reconfigurable Complementary and Combinational Logic Based on Monolithic and Single-Crystalline Al-Si Heterostructures

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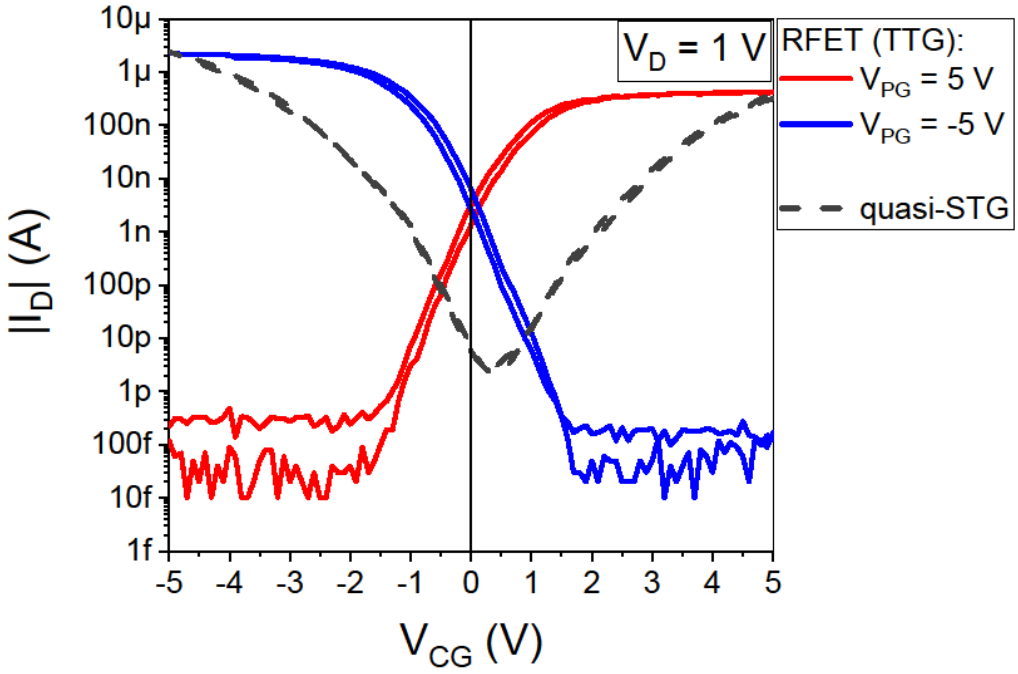

Figure S1. *The three top-gate RFET operated as a quasi-single top-gate (STG) SBFET by electrically connecting the control- and polarity gates (V_{CG} = V_{PG}) in black dashed lines, showing that the three top-gate RFET (red, positive V_{PG} and blue, negative V_{PG}) architecture promotes the suppression of undesired charge carriers, showing the V_{CG} sweep in both directions.*

Evaluation of transfer characteristic at positive and negative bias polarity V_D:

Figure 1c in the manuscript shows the transfer characteristic for positive biases ranging from V_D = 250 mV to 1 V in 250 mV steps. Increased biases result in a "fanning" of the transfer characteristic in p-type operation. This is a typical characteristic of SBFETs, as the charge carrier injection mechanism relies on tuning the incorporated energy landscape of the semiconductor and thus on the band bending mechanism.[1] Applying negative drain biases, leads to such a fanning in the n-type operation regime. Thus, leading to higher threshold voltages at higher V_D due to a stronger band bending.

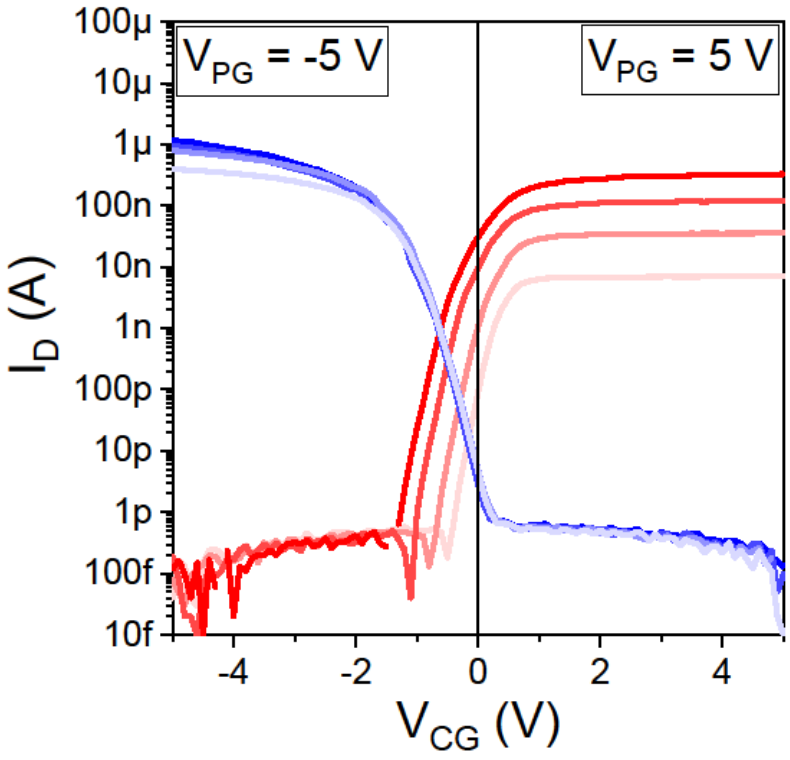

Figure S2. *Transfer characteristic of a three top-gate RFET with negative drain biases ranging from V_D = -250 mV to -1 V in -250 mV steps. Biasing the device with negative V_D, results in a fanning with increasing drain bias of the transfer characteristic in n-type operation mode.*

	p-Ion (µA/µm)	p-Ioff (µA/µm)	n-Ion (µA/µm)	n-Ioff (µA/µm)	p-Jon (A/cm²)	n-Jon (A/cm²)	p-Vth (V)	n-Vth (V)	p-S (mV/dec)	n-S (mV/dec)
NiSi-Si [3]	94	1.50E-07	5.3	1.50E-07	6.00E+05	3.40E+04	-	-	90	220
NiGe-Ge [4]	5.56	5.60E-04	0.47	1.67E-03	3.80E+04	3.50E+03	-0.2	0.4	150	215
Al-Si (this work)	35	1.39E-06	3.34	4.09E-06	5.13E+04	4.99E+03	-0.72	0.36	289	280
Al-Ge [5]	52.8	6.00E-05	0.02	5.00E-05	9.20E+05	3.30E+03	-1.4	1	700	800

Table S1. *Comparison of the most important transistor parameters of silicide/germanide and Al-based NW RFET concepts for Si and Ge channel materials.*

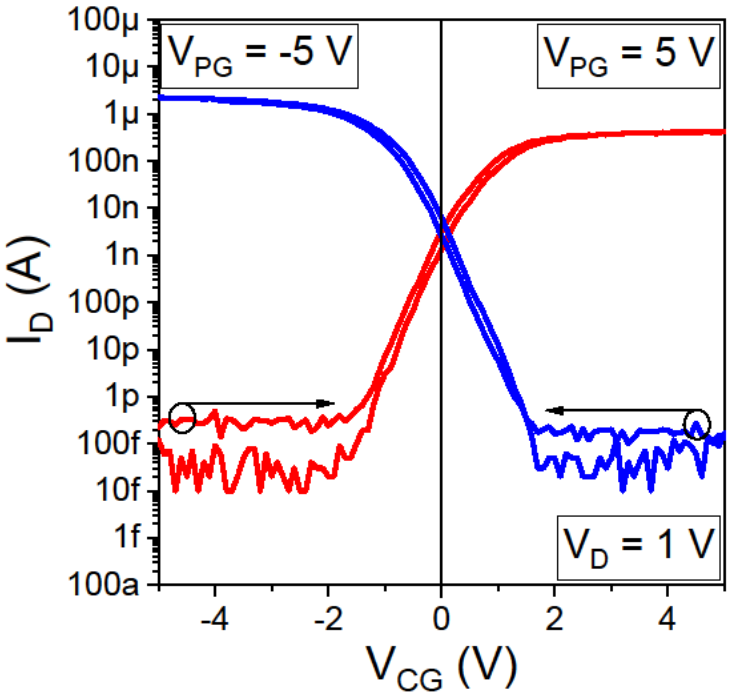

Figure S3. *Forward and backward measured transfer characteristic, where the forward measured transfer characteristics are always measured from the off- to on-state. The arrows indicate the measurement direction. Remarkably, the hysteresis remains low due to a relatively low number of traps states in the thermally grown SiO_2 gate dielectric.*

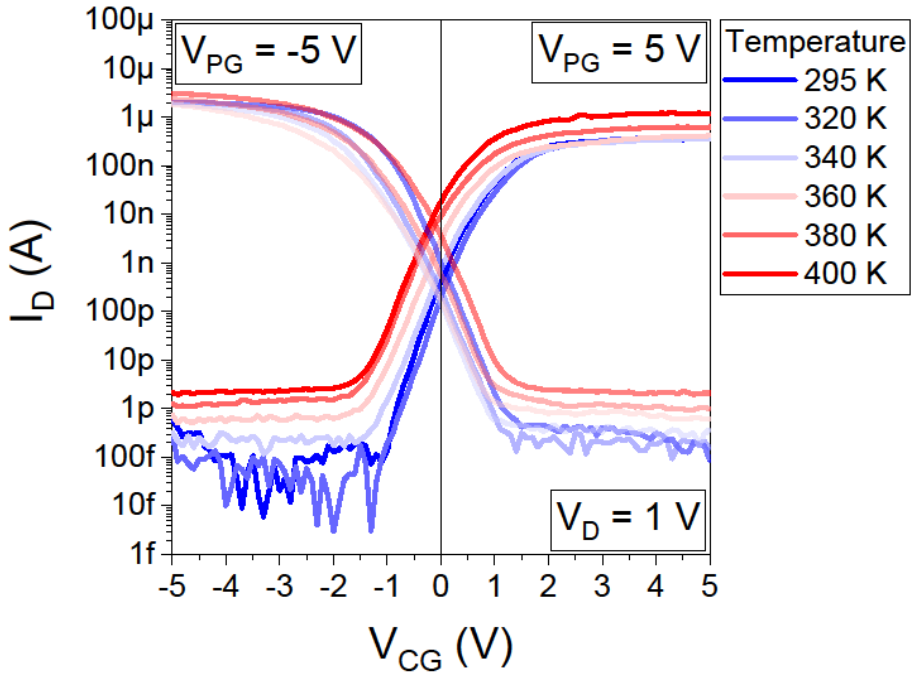

Figure S4. *Transfer characteristic of a three top-gate Al-Si NW RFET for elevated temperatures. Due to excited charge carriers, the off-current increases gradually with higher temperatures by about one to two orders of magnitude, whereas the on-current also increases, supporting well-defined operation even at temperatures up to 400 K.*

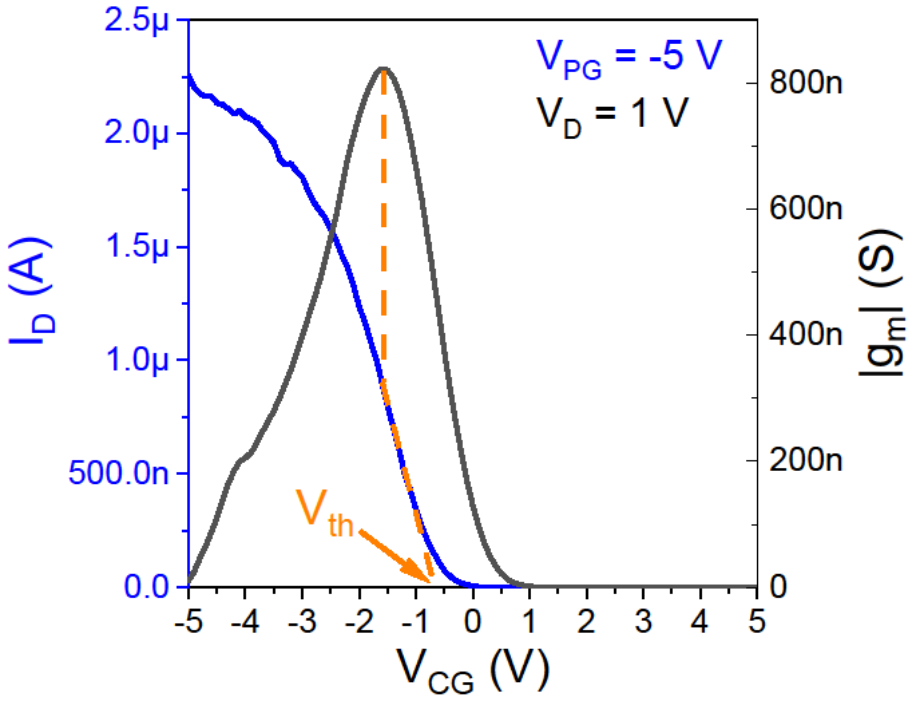

Figure S5. *Extraction of the threshold voltage V_{th} of the p-type transfer characteristic. The evaluation is done by the transconductance method.[2] The same procedure is applied for the transfer characteristic of the n-type operation mode.*

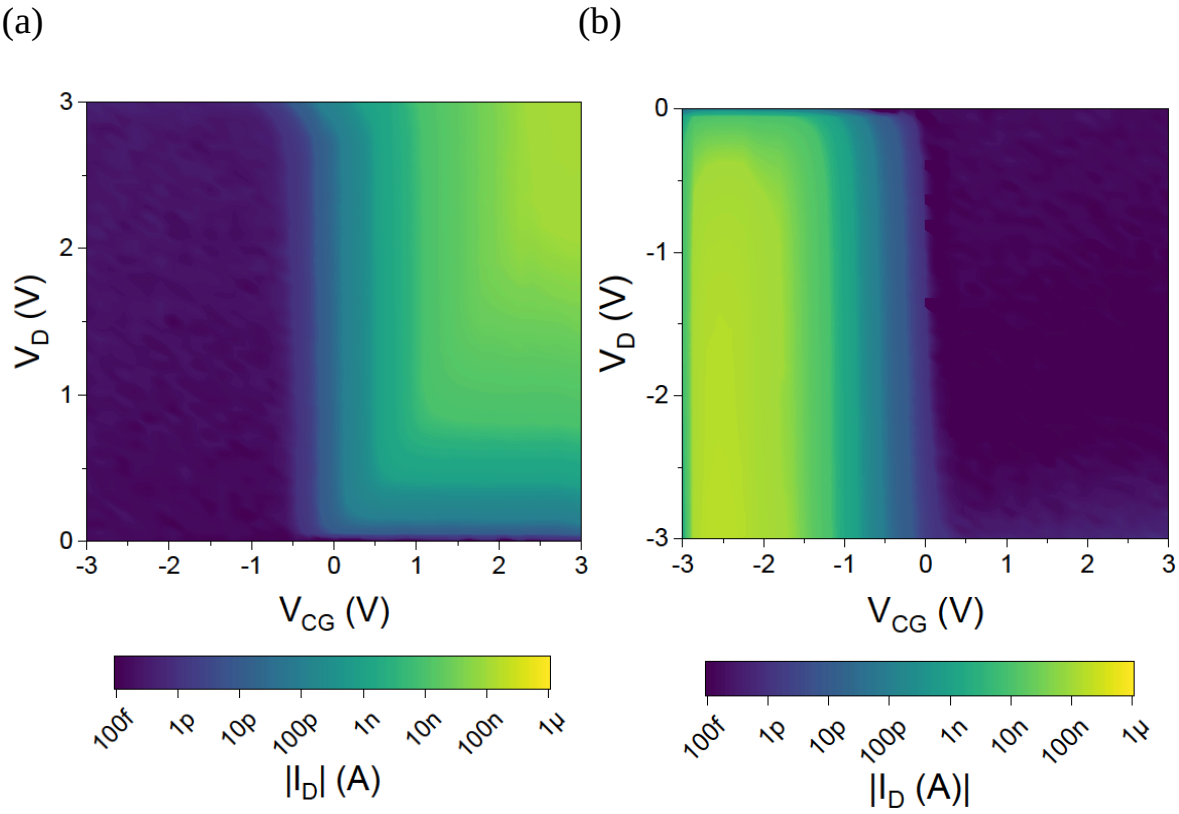

Figure S6. *Conductance maps for (a) V_{PG} = 3 V (n-type operation) and (b) V_{PG} = -3 V (p-type operation), allowing to determine appropriate operation points of the bias as well as top-gate voltages (here: 3 V).*

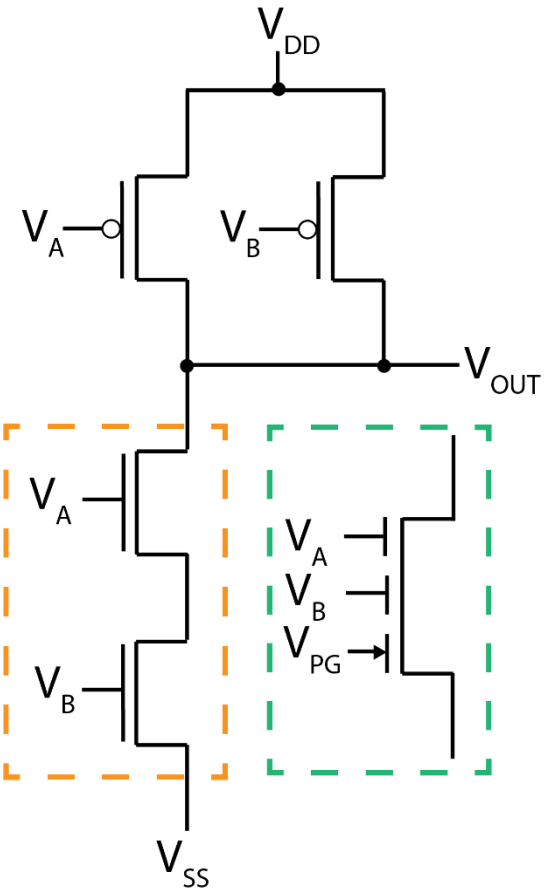

Figure S7. *NAND logic gate realized with FETs. The orange path shows the realization with conventional MOSFET technology, whereas the green path illustrates the use of a wired-AND gate replacing the lower two MOSFETs.*

References

[1] Weber, W. M., & Mikolajick, T. (2017). Silicon and germanium nanowire electronics: physics of conventional and unconventional transistors. *Reports on Progress in Physics*, *80*(6), 066502.

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[3] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, W. M. Weber, *Nano Letters* **2012**, *12*, 119.

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