DIPLOMA THESIS

Power Supply Unit for Wireless Sensor Networks

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Kurzfassung

Energieautarke Funksensornetzwerke bestehen aus Netzwerkknoten, die die benötigte Energie entweder aus ihrer Umgebung oder von Batterien beziehen. Daher liegt das Hauptaugenmerk beim Betrieb von Sensorkonten auf deren Energieeffizienz. Durch einen hohen Wirkungsgrad erzielt man lange Batterielaufzeit beziehungsweise benötigt nur kleine Energieumsetzer. Diese Arbeit beschäftigt sich mit dem Wirkungsgrad von Spannungswandlern für Funksensorknoten. Ziel ist die Entwicklung eines Energieversorgungssystems, das speziell auf die Anforderungen eines Sensorknotens zugeschnitten ist. Die wichtigsten Aspekte sind ein hoher Wirkungsgrad auch bei kleinen Ausgangsströmen, ein schnelles Ausregeln von Lastsprüngen und gleichzeitig eine flexible Erzeugung von auf- oder abwärts gewandelten Ausgangsspannungen. Kommerzielle Spannungsregler sind für hohe Ausgangsströme optimiert und weisen lediglich in diesem Bereich einen hohen Wirkungsgrad auf. Diese treten bei typischen Lastprofilen in Funksensoren jedoch nur für kurze Zeiträume auf. Weiters wird durch Verwendung eines Konzeptes zur Steuerung mehrerer Ein- und Ausgängen mittels einer einzigen Induktivität eine Erhöhung der Integrationsdichte und eine Kostenreduktion erreicht. Die Messergebnisse des diskret aufgebauten Prototypen validieren die Simulationsergebnisse und die erwartete Funktion des innovativen Reglerkonzeptes. Der Eigenstrombedarf der Schaltung wurde, im Vergleich zu kommerziellen Spannungsreglern, von 15 µA auf weniger als 1 µA reduziert. Diese Verbesserung wirkt sich vor allem bei kleinen Lasten aus und steigert den Wirkungsgrad enorm.

Abstract

Self-sufficient wireless sensor networks consist of network nodes that are powered by either the environment using energy harvesters or by batteries. Hence, power efficiency is important for sensor nodes. A high efficiency extends battery lifetime or reduces the size of energy harvesters. This thesis focuses on the power efficiency of voltage regulators used in wireless sensor nodes. The goal is to design a power supply unit that is fitted to the special requirements of a wireless sensor node. The most important aspects are high power efficiency even at low output currents, handling of fast load steps and a combined step-up and step-down operation. Off-the-shelf voltage regulators are optimized for high load currents which occur only during short time slots in typical load profiles of sensor nodes. Furthermore the regulator concept increases the integration density using a single inductor that supports multiple input and output channels. Due to the reduced size and the low off-chip component count, a cost reduction is achieved. Measurement results of the discretely implemented prototype confirm with simulation and expected function of the innovative switching regulator concept. When compared to off-the-shelf regulators, a reduction of the quiescent current from 15 µA to less than 1 µA was achieved. This enhancement has its highest impact at low output currents and gains power efficiency enormously.

Acknowledgments

My thanks go to my advisor, Prof. Dr. Dietmar Dietrich and Dr. Christian Hambeck who supported me with technical information and feedback through the course of my thesis. Special thanks go to my parents, family and friends who supported me during my study period. Especially, I would like to thank Melanie and Andreas who helped me to keep eye on the important things in life.

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[1] http://www.chosen.eu/

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List of Abbreviations

AC	Alternating Current
ADC	Analog Digital Converter
AODV	Ad-hoc On-Demand Distance Vector
ASIC	Application Specific Integrated Circuit
BAS	Building Automation Systems
DC	Direct Current
DSDV	Destination-Sequenced Distance-Vector
ESR	Equivalent Series Resistance
FET	Field Effect Transistor
FFT	Fast Fourier Transformation
GSM	Global System for Mobile Communication
IC	Integrated Circuit
IP	Internet Protocol
IR	Infrared
IT	Information Technology
LDO	Low Drop Out Regulator
LED	Light Emitting Diode
MAC	Media Access Control
MIMO	Multiple Input Multiple Output
MOS	Metal Oxide Semiconductor
OS	Operating System
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation
PSU	Power Supply Unit
PWM	Pulse Width Modulation
RAM	Random Access Memory
RF	Radio Frequency
SEPIC	Single Ended Primary Inductor Converter
SNMP	Simple Network Management Protocol
TCP	Transmission Control Protocol
TTL	Transistor Transistor Logic
USB	Universal Serial Bus
VDHL	Very High Speed Integrated Circuit Hardware Description Language
WLAN	Wireless Local Area Network
WSN	Wireless Sensor Network

1 Introduction

The idea of wireless sensor networks is to establish an ad hoc radio network to monitor environmental sensor data of typically large areas. The wireless communication links of the sensor nodes make distribution flexible because of the omission of wiring. Compared to wired nodes, a significant cost reduction can be achieved by avoiding expensive installation and connection of network nodes. Furthermore, the wireless concept can be more resistant against single node failures. First, this chapter gives an overview over wireless sensor networks. The physical communication, routing concepts, power supply and maintenance is discussed. Section 1.2 outlines the application field for wireless sensor networks and gives some examples where wireless sensor networks can be used. The topic of section 1.3 are different components which are needed to set up a wireless sensor node. This includes sensors, communication modules, micro controllers and energy storage. In the end of this chapter, tasks of the power supply unit and the problem with state-of-the-art are described, as well as the objectives of a possible solution are discussed.

1.1 Wireless Sensor Networks

Wireless sensor networks (WSNs) contain of up to thousands of single network nodes. These nodes are placed in a certain area and typically provide simple measurement, routing, storage or control tasks. The nodes within the network communicate via wireless technology. As communication method radio frequency (RF) or infra red (IR) light is used. One goal of wireless networks is to provide ad hoc creation of the radio link topology. Nodes are distributed within an area either specifically or randomly and the nodes are searching for their neighbors and form the wireless network automatically.

The network nodes contain sensors to provide tasks such as measuring the environmental temperature or humidity. Different application examples are discussed in 1.2. Each node performs measurements in certain time slots and stores the information until the next datagram is sent to a neighbor node or the network gateway node. Furthermore, basic calculation tasks can be provided by the network node itself. Information from each node is passed through the network to the gateway that collects measurement results and provides the information to the user, another network, a computer system or generates alarm messages. For instance, an alarm is raised when

the average temperature exceeds a specified threshold. In contrast to wireless communication protocols, such as IEEE 802.11 - WLAN (Wireless Local Area Network), the communication within a wireless sensor network is done hop by hop using network nodes as routers. The next forwarding node is determined by the shortest distance to the sender node. By shortening the transmission distance for each node, the needed transmission energy is reduced compared to long transmission distance communications. The routing protocol has to determine the optimum path from each node to the gateway. The used routing protocol has major impact to delivery time of datagrams and to the energy efficiency. The optimal routing protocol is different for each application because of various requirements. Figure 1.1 illustrates a schematic diagram of a wireless sensor network. When node A wants to send a datagram, the packet is sent hop-by-hop along the red (wireless) path to the gateway. From there, the data is distributed to the external application.

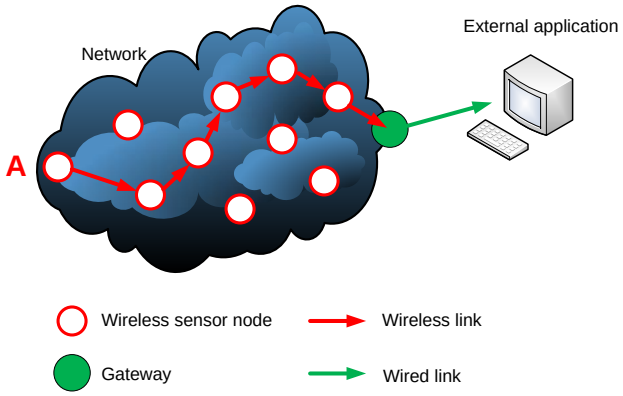


Figure 1.1: Schematic structure of a wireless sensor network

The development or even the selection of the routing protocol is a big challenge in WSNs. In general, the network nodes can be moved easily because of their wireless character. Furthermore, a breakdown of a network node should not degrade the whole network operation. So it is important to support topology changes within the network. There are many routing protocols available that face this problem. A proactive routing protocol, for example, is the destination-sequenced distance-vector (DSDV) and the ad hoc on-demand distance vector (AODV) is listed as example for a reactive one. As mentioned in [ZT05] and [SZ05], many considerations for developing power saving routing protocols are done.

An important objective is a long lifetime of each network node and of the network service itself without maintenance. Most network nodes are battery powered to be aware of power lines. Batteries only contain a limited amount of electrical energy, so it is important to ensure that the network nodes operate as power efficient as possible. In addition to permanently powered components with low consumption, some components can be switched off or put into sleep mode if they are not used. For example, the temperature typically changes slowly. So a measurement interval of ten milliseconds is not necessary. One measurement every ten seconds is sufficient for most applications. The rest of the time, the processor and the communication module are not used and can be switched off to save energy. This extends battery lifetime enormously.

Assuming the application of measuring temperature and humidity in a forest, the sensor nodes are placed on trees. Then replacement of the batteries of each network node is a time and cost

intensive effort. If the nodes are mounted on the treetop, maintenance is even dangerous for the employees. In a network with more than thousand nodes, the maintenance costs would be high, and costs are a limiting factor for the success of wireless sensor networks. So it is important to achieve an extended lifetime of the sensor with a single battery or to include energy harvesting components such as solar panels or electromechanical harvesters to make battery replacement more infrequent or even obsolete.

1.2 Application Field for Wireless Sensor Networks

Wireless sensor networks cover a wide application field that ranges from home and building automation to military applications. Wireless sensor nodes are typically powered by a primary or secondary battery, or an energy harvester and use radio communication links. So no wiring of the node is necessary. This makes the network flexible because the nodes can be moved very easy at any time as long the node is still in link range to the other nodes in the network. The network topology can be easily changed to optimize the application or to adapt it for a different purpose. Furthermore, adding, removing and replacement of network nodes is easy and also deployment and installation of the nodes is cheaper when compared to wired sensor nodes. Wireless networks can also be used if cabling is impossible. In hazardous areas for instance, cable isolation would be damaged.

An example of wireless sensors in home automation is in alarm systems. Application domain for such systems are the detection of intrusion into buildings as well as the detection of fire or water ingress. Complex routing algorithms are not necessary, due to the small network size, but in some cases repeaters are used to extend the link range of the network. The most common sensors are movement- and magnetic sensors to check if a door or a window is opened. Additional sensors to detect breaking glass, fire, water or gas can be included. In the application domain of home users, the benefits of a wireless system are easy to understand. Alarm systems are often assembled when the building is already made up and inhabited. In case of a wired network the walls would have to be opened to install the wires. This makes installation longsome, expensive, and stressful for the inhabitants. Moreover, a later extension to more sensors or to a greater area would repeat this installation process. In that sense, wireless components are much more flexible and cheaper compared to their wired counterparts.

The CMC-TC system [1] from Rittal[1] includes sensors for temperature, humidity and access control. The system provides warning messages using TCP/IP (Transmission Control Protocol/Internet Protocol) and SNMP (Simple Network Management Protocol) in case of a temperature alarm, when water ingress is detected, or when a person enters the room. There are also nodes with digital inputs available which allow to connect alternate sensors. So there are many more monitoring tasks possible. Some of them are power breakdown, cable break, movement or fire. Because of the wireless components, it is easy to expand the system using more or other types of sensors. Furthermore, the mobility of sensors allows optimization of the actual sensor location for temperature measurement. Figure 1.2 shows the floor plan of a fictitious IT server

[1] `http://www.rittal.com/`

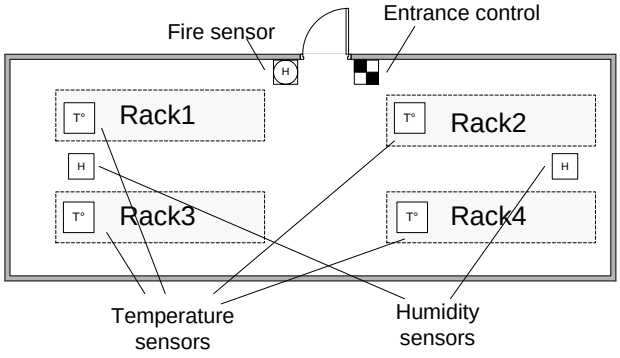


Figure 1.2: Example floor plan of a fictitious IT server room

room containing four racks. Especially if the size and the count of the racks are not known at design time, a wireless sensor network lowers the difficulties in the network setup of the room. On the Rittal homepage also an overall price example is given that presents a higher component price for the wireless components but an overall cost reduction when including installation. Furthermore, the time to setup the system is short and reduces the interruption of the IT system.

A common application field for a large amount of sensors and actuators are building automation systems (BAS). Traditionally, wired components are used, but there are many considerations to replace wired sensors with wireless ones. In [SK02], a combination of wireless sensors such as mobile user terminals, and wired sensors for static components like radiators is proposed. The wireless components provide high flexibility which is important for modern room concepts. Heaters or air condition systems are connected via wired network nodes though static energy supply, by wires or pipes, is needed anyway. The considerations of the paper result in a combination of wired and wireless components and a wired backbone that provides higher data throughput and lower error rate than the wireless links. In [RKNG07], considerations for abdication of wires are made because of aesthetic needs in all-glass architectures or historical buildings. Using wireless links, no cables are visible and no walls have to be opened. In terms of costs [Gut04] demonstrates that installation cost of electrical switches are 10 to 30 times higher than the switch cost itself which illustrates a cost reduction in deploying electrical switches when the lighting system is controlled by wireless switches. Furthermore, sensors for safety and security can be included into modern buildings to detect fire or to check access authorization. Because of the large number of sensors, the network becomes often tolerant against single node failures.

Wireless networks are even possible in vehicles. Modern cars have a high amount of sensors and actuators inside. Wireless links are more sensitive to disturbances from outside than wired ones, if the interference is randomly injected. Even if the wireless links are limited to non safety critical functions, the reduced amount of wires is enormous. The consequence is reduced installation cost and weight and hence, less fuel consumption. Some non-critical functions are the remote control for the audio system, air condition temperature sensors, seat heating and mirror control. This list can be extended to many more applications where wired communication links can be replaced by wireless ones. Another application inside cars is the measurement of the tire pressure where the sensor is placed inside the rubber of the tire. The correct tire pressure is important to grant the minimum stopping distance and fuel consumption. Thus, a pressure sensor increases safety

and efficiency of a car. Figure 1.3 illustrates such non safety critical sensors and actuators inside a car.

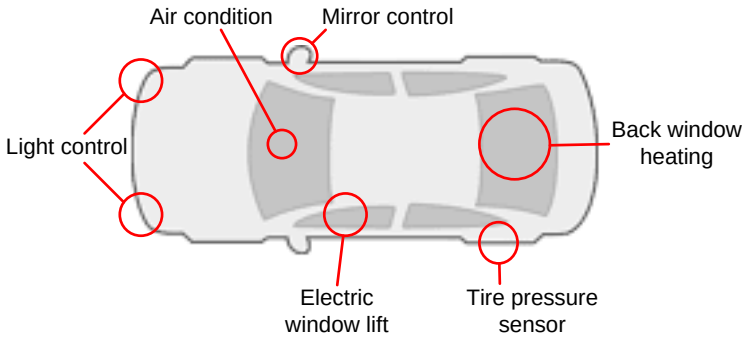


Figure 1.3: None-critical sensors and actuators in a vehicle

Health care systems become more and more important especially for weak and seriously ill people. By wearing sensors on the body, the quality of life of these people can be increased. For example, a pulse sensor can be located in a watch that communicates with the cell phone of the patient. In case of an emergency, the phone gives an emergency call via GSM (Global System for Mobile Communication) or the Internet. Several types of different sensors can be included in this system. For instance, sensors which monitor the heartbeat or tracking the body's temperature of the patient can be deployed. Figure 1.4 illustrates a concept plan for a health care system with wireless body sensors. Acceleration sensors are used to detect a person's accident. Furthermore, long time observations for health check or pharmaceutical studies can lead to better objectivity and accuracy. Wireless sensors make the monitoring more comfortable for the patient and simplify analysis of the data by medical staff.

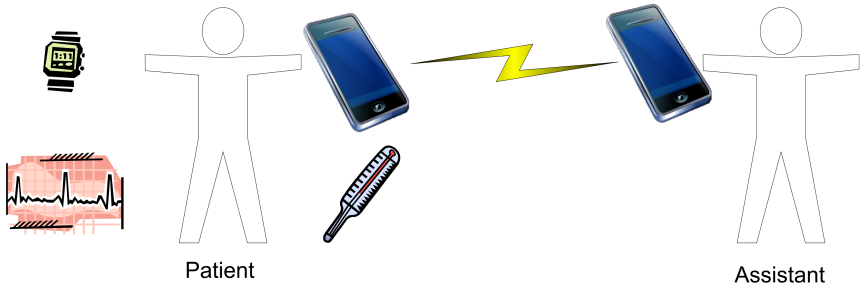


Figure 1.4: Health care system with wireless body sensors

As outlined in this section, there are many applications for wireless sensor networks, even more applications will be developed in future. A lot of research is going on currently in the topic of wireless sensor nodes and networks to further reduce size, decrease cost, increase computing power, and especially minimize power consumption of the manifold components.

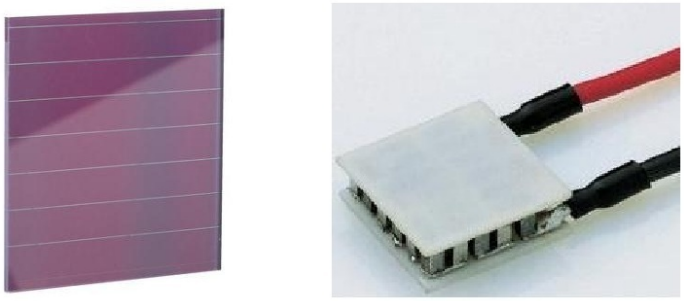
1.3 Components of Wireless Sensor Nodes

As discussed in section 1.1 a WSN consists of many, sometimes heterogeneous network nodes. The used components of a sensor node depend on the vendor and the function that has to be handled. In sensor nodes that provide a simple temperature measurement every minute, different components are used than for magnetic field sensors or sensors that require significant computing tasks. Heavily depending on the application of the specific node, different components are necessary to provide an optimal balance between operation and energy efficiency. A sensor node basically consists of a communication module, a micro controller, memory, at least one sensor and an energy storage device. The most common energy supplies are primary and secondary batteries with high energy density. Because of the different supply voltages that are needed for the node's components, voltage regulators are necessary to provide the appropriate voltage levels. The main component that includes the voltage regulators and provides additional supply-related power management functionality is called power supply unit (PSU).

The actual function of a sensor device is to convert a physical value such as temperature or light intensity to an electrical quantity first for later analog-to-digital conversion. Main task of the micro controller is to filter and check the sensor's measurement data, and to prepare it for transmission via the communication module. Simple calculations like averaging of measurement results are typically performed. Depending on the application, the measurement results are stored in the micro controller's memory or in an external non-volatile memory until the node transmits the data. The PSU includes management functions beside the actual voltage regulation to indicate, if the output voltage is already stable. As mentioned before, the energy supply itself can be, either a primary battery or a rechargeable secondary battery together with energy harvesters such as solar panels or piezoelectric modules.

Energy harvesting is a method to gather energy from the environment and convert it to electrical energy to supply electronic components. A well known harvesting transducer is a solar cell. It converts electrical current out of light intensity. Another type of energy harvester is a (micro) mechanical component that converts vibrations to electrical energy by using piezoelectric crystals. Peltier elements use the Seebeck effect for converting a temperature gradient between the two plates of the element into electrical energy. Figure 1.5 shows two energy harvesting transducers, a solar panel and a peltier element and the accordant power densities of state-of-the-art devices.

Depending on the node vendor, application, and environment, distinct components are used within a wireless sensor node. Therefore it is not possible to generalize how a node is designed and built. Three different sensor nodes from different vendors are briefly introduced and a more detailed description of these wireless sensor nodes is given in section 2.1. The sensor node MICA2 from Crossbow [3] includes a micro controller, flash memory, a radio communication module as well as a carrier for batteries. Sensors can be attached via an expansion connector. A more basic node is produced by Amber Wireless. The module AMB2520 [4] contains only a wireless module and a processor to manage the radio communication protocol stack. Application processor, memory, sensors, as well as the supply system have to be connected externally. The third example is a commercial product from E-Senza. The node includes processor, memory, radio communication module, energy supply and sensors. So for every measurement application, different types



(a) Solar panel: 15 mW/cm^2 (b) Peltier element: 40 µW/cm^3

Figure 1.5: Energy harvesting components
(Pictures from [2], Data from [RKH+05])

of nodes are available. The module SB110-T [5] includes a PT 100 element for temperature measurement. The benefit is therefrom that each node is optimized for its specific application.

WSNs communicate with external computer systems using a gateway node that has special characteristic and is often wired. For example, the gateway nodes from Crossbow offer three possibilities to implement gateway functionality. Figure 1.6 displays the main components that can be used. The serial interface of each network node can be used to connect the node to a computer and form a network gateway. In this case the interface hardware has to be installed external as shown in figure 1.6(a). The gateway board MIB520 from figure 1.6(b) includes an universal serial bus (USB) interface for communication with a personal computer. MIB600 from figure 1.6(c), offers an Ethernet interface that supports TCP/IP and provides a web interface for sensor data access.

(a) MICA2 sensor node [3] (b) MIB520 - with USB interface [3] (c) MIB600 - with Ethernet interface [6]

Figure 1.6: Gateway nodes for wireless sensor networks

1.4 Impact of Power Supply Systems

The function of the power supply system is to convert energy of a given power source to one or more output voltages that fit to the component's demand and to handle power management. An overview over components of a wireless sensor node is given in section 1.3. In the easiest case, no extra voltage regulation is necessary when all connected components can be operated with

the given input voltage, but in most cases, this is not possible because different supply voltages are needed for various building blocks and also maximum power efficiency has to be taken into account. Some components, especially the digital ones, can deal with a wide range of the supply voltage. Modern electronic components are forced to tolerate a wide range of supply voltages. The output voltage of a battery with nominally 1.5 V is almost constant most of the time, but can also fall down to around 1.0 V depending on the load condition and battery type [7]. In some cases it is even necessary to provide a higher voltage to the component than provided by the voltage source. This is achieved with adequate converter circuits such as switching voltage regulators. A challenging requirement for PSUs is the dynamic switching from down-conversion to up-conversion mode and vice versa according to the available input- and the required output voltage.

The energy supply system is important for the overall performance considerations to achieve maximum lifetime with limited amount of energy. There are several different types of voltage regulators available. Each one has its special characteristics. The power efficiency of the sensor node is significantly reduced when a suboptimal voltage regulator is chosen. The efficiency of the PSU depends on the actual load conditions and on the deployed regulator concepts within the PSU. A more detailed discussion of the tradeoff between linear voltage regulators versus switched mode regulators is given in section 2.3. The typical characteristic of linear regulators is a better efficiency at low output currents and low voltage drop. At high currents and large voltage differences between input and output, switched regulators have better power efficiency. Considering this circumstance, it is not energy efficient to supply low voltage circuits using a linear regulator-based PSU. Another important regulator characteristic is the control speed. If the load of the connected component changes very fast and the controller of the PSU is too slow, the output voltage reaches an undesired voltage level that makes the supplied component not working properly or the component is even destroyed. On the other hand, fast controllers typically have significant higher power consumption and should be used only if absolute necessary. For choosing an adequate regulator, application details have to be known previously.

It can be concluded that the selection of the optimal voltage regulator is not a trivial task and needs information about the component characteristics that are supplied by the regulator, as well as knowledge about the application and possible load conditions that will appear in the field. When the regulator does not fit to the rest of the components, the considerations concerning energy efficiency, performance, and reliability are in danger.

1.5 Problem Description and Objectives

Wireless sensor nodes are forced to be as small as possible to make an easy deployment possible. Furthermore, a compact design supports low price because of a high integration factor and low power consumption. All these points have to be considered when designing a wireless sensor node. An important part to achieve a high integrated solution, is the power supply unit of the sensor node. Most voltage regulators are designed for high performance applications where high currents of 100 to 500 mA and a large energy budged is available. In wireless sensor nodes, load

steps occur by switching from active to low power mode of the supplied components. The limited energy budget forces the node to operate at low power consumption in microwatt range. Mobile applications such as cell phones have been a driving force for low-power components. In contrast for wireless sensor nodes, the level of power demand is much lower and thus, efficiency of the voltage conversion has to be as high as possible even when the connected component is in power down or sleep mode with current consumption of less than one micro ampere. It is not helpful to have a regulator that has a good efficiency during the active periods and a bad one during sleep mode. It has to be considered that the components will stay in power down or sleep mode for most of the time and only wake up when a measurement is performed or data is transmitted or received. Figure 1.7 shows a typical power profile of a wireless sensor node. Because of the high ratio of sleep time to active time, a high power efficiency at low output currents is required. As mentioned in the previous sections, it is likely that all the components of the node need different supply voltages, so the support of various output voltages of the PSU is often an useful feature. Adjustable output voltages are necessary to grant flexible operation of the component and a

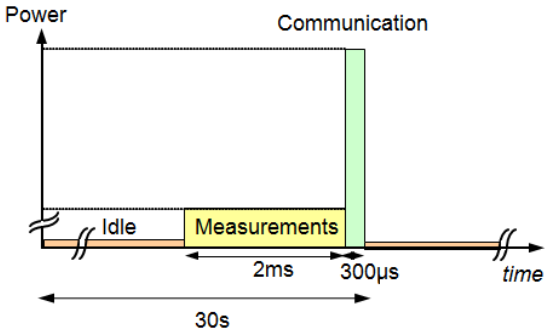


Figure 1.7: Typical power consumption profile of a wireless sensor node

wide application range. Available PSUs do not only consist of the regulator itself but also include additional features such as output voltage monitoring or a shutdown capability. Depending on the vendor and component type, there are furthermore other additional circuits included. According to the control rate, a tradeoff between speed and current consumption has to be chosen. Methods for the dynamic change of the control speed according to the actual load profile helps to balance the performance at different load conditions. Without any kind of maintenance, a sensor node that has to operate for tens of years, can only be powered by batteries in rare cases. Only a solar cell is also no solution, because sufficient exposure to ambient light is not guaranteed all the time. Similar considerations can be made for other harvesting components. As a consequence, a combination of energy source and energy buffer has to be used. For example, a secondary battery is charged by an energy harvester to provide power when no energy is available from the transducer. When the secondary battery is charged directly by a solar panel, the designer is forced to match the voltages of the solar panel with the used energy storage device for high efficiency. This limits the components that can be used in combination. For instance, using a 5 V solar panel combined with a 1.5 V AA battery is not useful. So a solution to this voltage matching problem increases flexibility.

One goal of this thesis is to compare the characteristics of the most common concepts for voltage

regulators and to determine the application field where each concept fits best. The optimal solution for wireless sensor network nodes should be figured out of all the evaluated concepts. There are multiple challenging considerations that have to be taken into account when developing a low power circuit. The most promising architectures and concept combinations should be evaluated and discussed. As a result, a set of the most powerful and compatible concepts should be found and applied to the proposed regulator circuit. To determine the function and estimated quality of the developed circuit, simulations should be performed at first. After that, a discrete prototype of the proposed and optimized PSU is assembled and set up. Its performance should be compared to the simulation results and state-of-the-art. Main focus is on optimization of the designed voltage regulator for high power efficiency and bandwidth of the control loop. Off-the-shelf components archive the best power efficiency at high output currents. Because wireless sensor nodes mostly operate under low output power condition, the efficiency in this range is of major importance. In this case, the loss due to own consumption of the regulator circuit itself has increased impact to the overall efficiency. So it is important to switch off all unneeded circuits. Because of unpredictability of the load current, a short resume time is important. In other words, the regulator enters its low power mode as often as possible, but without any external information and switches to active mode again as fast as possible. Response times below about hundred nanoseconds are required typically to guarantee sufficient quality of the output voltage. Another task is to optimize the combination of primary and backup power supplies. In the worst case - at the highest output current - switching between power sources has to be performed without drastic impact to the output voltage. In this context, the support of multiple output voltages and also an integrated power management for charging the backup battery should be provided. Furthermore, the number of off-chip components should be minimized to achieve high efficiency and low cost.

The methodology to achieve and prove an appropriate design for the proposed PSU is described in this paragraph. The LTSpice[2] simulation tool is used mainly for circuit simulation and concept evaluation. It is a free simulation tool customized by Linear Technologies and it supports simulation of analog circuits and components, but also simulation of digital circuits is possible with limited accuracy. For most switching regulators from Linear Technologies, LTspice macro models are available. Furthermore, a large number of models for operational amplifiers, transistors, etc. are available. This makes comparison of the proposed regulator and the commercially available voltage regulators - at least from Linear Technologies - comfortable. When developing prototypes, an ASIC implementation is very time and cost intensive. So the prototype of the PSU is assembled as a scalable prototype with mostly PCB mounted components in a first step. This means that instead of a fully integrated power stage, discrete power transistors are used. These non-integrated components have slightly different electrical characteristics than the integrated counterparts, but function is equivalent and component size, power consumption, leakage current, etc. can be scaled. So estimations concerning performance of an integrated circuit implementation are possible with sufficient accuracy. The digital control parts of the regulator are integrated into a field programmable gate array (FPGA) to minimize development time without tradeoff in functional performance. The PCB prototype contains surface mounted components

[2] `http://www.linear.com/designtools/software/ltspice.jsp`

to achieve a circuit performance that is almost close to those of an integrated solution. Detailed circuit design of auxiliary components such as transistor drivers and a startup circuit for the regulator are not covered down to transistor level. The focus of this work is put on an innovative architecture with a novel operating principle.

2 Related Work

The main topic of this chapter are related work and state-of-the-art of concepts with relevance for this thesis. In section 2.1, a set of off-the-shelf wireless sensor nodes is described. The main components of the nodes are listed together with their most important electrical characteristics. A closer look is taken on the current consumption at the nominal supply voltage to get an overview over the power consumption of a typical wireless sensor node. Section 2.2 exemplary presents components that are used in a wireless sensor node. Examples of processors, communication modules, sensors, and supplying components are given. A more detailed look is taken on the power consumption of the components in different power modes. This information is necessary to determine the requirements for the power supply unit of a network node. The subsequent section 2.3 describes and compares different regulator concepts and control mechanisms for switching voltage regulators. Based on this information, a regulator concept is chosen for the proposed design which is concluded afterwards.

2.1 Sensor Network Nodes

In order to determine the requirements for the power supply unit of a wireless sensor node, the characteristic of off-the-shelf nodes is analyzed. There are many ways to set up a sensor node in terms of complexity, number of used parts, size, weight, energy consumption and much more. Therefore it is not possible to generalize how a sensor node is built. Depending on the used components, the electrical characteristics can be very different. For example, a 2.4 GHz transceiver with ZigBee[1] protocol stack has higher power consumption and different timing characteristics than a simple 916 MHz radio module without protocol function. The characteristics of typical sensor nodes from different vendors are outlined to show target application platforms for the anticipated power supply unit.

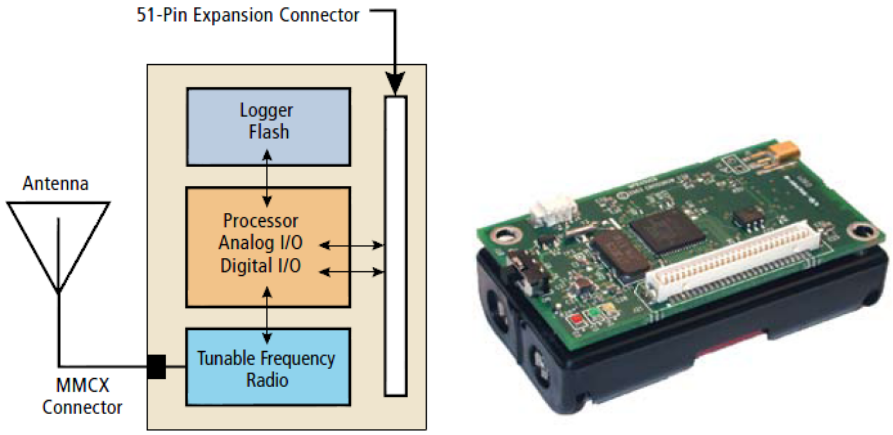
One example node is the MICA2 node from Crossbow. It basically consists of a ATmega128L processor, 512 K bytes of flash memory, a radio communication module with 868/916 MHz radio frequency and an extension connector for external sensors. Figure 2.1 illustrates a block diagram (a) and a photograph (b) of the MICA2 node. As illustrated in sub-figure (b), the required

[1] `http://www.zigbee.org/`

space for the batteries is as high as the required space for the components of the node. Task of the microcontroller is management of the communication protocol stack and the sensor data as well as execution of the application itself. The node uses the operating system (OS) MoteWorks[2] that is developed as a derivate of TinyOS[3]. The OS provides methods for automatically setting up the mesh network and methods for remote reprogramming. There are no sensors on the board included, but they could be added using the extension connector. The node is powered with two AA batteries and provides a lifetime greater than one year when sleep modes are used. The most important power ratings of the node are given in table 2.1. [3]

Table 2.1: Electrical characteristics of MICA2 at 3 V[3]

Component	Active Current	Sleep Current
Processor	8 mA	<15 µA
Radio Module	27 mA	<1 µA



(a) Block diagram with main components (b) Node photo with 2 x AA energy storage

Figure 2.1: Wireless sensor node MICA2 from Crossbow [3]

The module AMB2520 from Amber Wireless[4] contains a RF transceiver (CC2500 from Texas Instruments) that uses a transmission frequency of 1.4 GHz, a communication micro-processor (MSP430F1232 also from Texas Instruments), and an integrated antenna. The application processor is not needed to manage communication protocol related computations because of the separate communication module. The application processor is connected via a serial peripheral interface. Figure 2.2 presents a photo of the sensor module. It cannot be used as a standalone wireless sensor node, because at least additional sensors are necessary. There are further modules available that support different transmission frequencies or include a complete Bluetooth or ZigBee protocol stack[5]. The main power characteristics are listed in table 2.2. [4]

[2] `http://www.xbow.com/support/wSoftwareDownloads.aspx`
[3] `http://www.tinyos.net`
[4] `http://amber-wireless.de`
[5] `http://amber-wireless.de/15-0-Ready-made-RF-Modules.html`

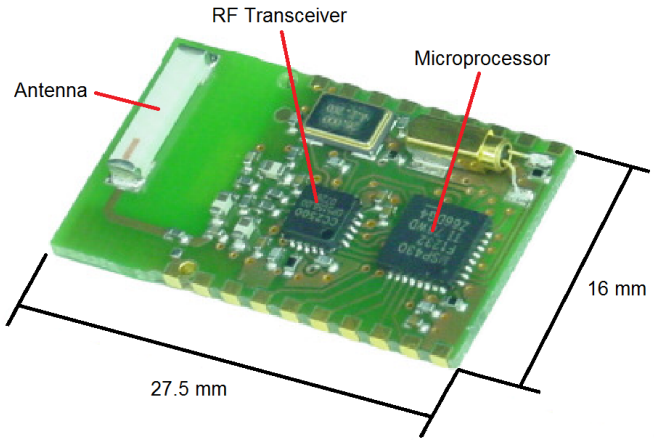


Figure 2.2: Wireless transceiver module AMB2520 from Amber Wireless [4]

Table 2.2: Current consumption of AMB2520 at 2.7-3.6 V supply [4]

Transmit	Receive	Low Power
25 mA	21 mA	6 µA

The module AMBZ210 from Amber Wireless works similar to the module 2520 with the difference that a ZigBee protocol stack with a 2.4 GHz physical layer is implemented on board. Because of the complex protocol and the large transmission range, the energy consumption of the module is higher when compared to other communication modules. [8]

E-Senza[6] products use a specific network protocol using a 2.4 GHz IEEE 802.15.4 compliant physical layer and a power source of two AA batteries or an external 12 - 24 V power supply. For many measurement applications, different sensor modules are available. The module SB110-T for example, includes a PT100 element for temperature measurements. The current consumption at different load conditions is given in table 2.3. [5]

Table 2.3: Electrical characteristics of sensor node SB110-T at 3 V supply [5]

Transmit	Receive	Active Measurement	Low Power
55 mA	50 mA	2 mA	20 µA

A widely common power supply for network nodes are two AA batteries with a nominal voltage of 3 V. The power consumption of the module mainly depends on the node complexity, protocol and frequency of the communication module, and the used power mode. Table 2.4 compares the power consumption of the nodes that have been discussed in this section. Depending on the module, different current profiles with power values are given in the data sheet for transmit, receive, sleep and low power operating modes. Due to the different current profiles and the versatile components, the comparison of the modules is difficult. For a better clarity, only the minimum and maximum values are listed. The consumed power of a wireless sensor node ranges from

[6] `http://www.e-senza.de/`

Table 2.4: Comparison of power consumption of different sensor nodes

Vendor	Module	Max. Power	Min. Power
Crossbow	MICA2	105 mW	48 µW
Amber	AMB2520	90 mW	16 µW
Amber	AMBZ210	457 mW	1.8 µW
E-Senza	SB110T	165 mW	60 µW

almost 500 mW down to some micro watt in power saving mode. There is a ratio of active power over stand-by power consumption from 2,000 up to 250,000. During power mode switching, the resulting load steps have to be compensated by the power supply unit without causing significant voltage drop or voltage overshoot.

2.2 Node Component Characteristics

The most important components of a wireless sensor node and its main characteristics are described in this section. Special attention is put on power consumption, supply voltage and supply current in different power saving modes of each component. This data is necessary to obtain basic knowledge of the demands on voltage regulators that are specialized for wireless sensor nodes. Only the main components are used for discussion and comparison to limit complexity.

Wireless Modules

Wireless communication modules from different vendors are compared, and the main focus is put on the power supply ratings of the modules that also include sleep or power down modes. Furthermore, the dependency of the energy consumption versus throughput and protocol complexity is given. As example modules, the 2.4 GHz transceiver CC2500, the 2.4 GHz transceiver CC2520 with included ZigBee protocol stack - both developed by Texas Instruments[7] and the module MAX7031 from Maxim[8] are used. All wireless modules can operate in different power modes for optimal energy efficiency.

The module CC2500 uses a carrier frequency of 2.4 GHz. The chip itself includes hardware support for packet handling but no protocol stack. It contains transmit and receive FIFOs, and a packet handler. The chip can handle supply voltages from 1.8 - 3.6 V while the current consumption in transmit or receive mode depends on the actual data rate. As maximum current consumption in transmission mode, a current consumption of 21.5 mA at a data rate of 500 kBaud is given in its data sheet. The current consumption is sleep mode is 400 nA. These values do not include the consumption of the external components such as a crystal oscillator or antenna components. [9]

The second module is also developed by Texas Instruments. CC2520 uses similarly to CC2500, a 2.4 GHz physical layer and is compliant to IEEE 802.14.4 with its media access control (MAC)

[7] `http://www.ti.com/`
[8] `http://www.maxim-ic.com/`

layer. The wireless link is capable of data rate of 250 kb/s. The modules main feature is the integrated ZigBee protocol stack. It includes a protocol processor that reduces the programming effort of the application processor. The supply voltage ranges from 1.8 to 3.6 V. The supply current demand in different operation modes is 18.5 mA in receive mode and a signal strength dependent value between 25.8 mA and 33.6 mA in transmit mode. There are three power modes supported by the module and not all functionality is supported in each mode. The minimum supply current is given with 30 nA, but current consumption of the external clock and the antenna components are not considered nor mentioned. [10]

The third module that is discussed is the MAX7031. It supports communication frequencies of 308, 315 and 433.91 MHz with a maximum data rate of 66 kbit/s. This module only supports modulation and demodulation of transmit data and does not include any communication protocol. It uses a supply voltage between 2.1 V and 3.6 V and has a current consumption of 12 mA in transmit mode and less than 800 nA in shutdown mode. [11]

The current consumption of the module depends on the complexity of the chip, the performance of the on-chip micro controller, transmission range, bit rate, physical layer, and application usage. Table 2.5 shows a comparison of the mentioned wireless modules according to their electrical attributes. The power consumption of the different modules ranges from less than 1 µW to

Table 2.5: Power rating comparison of different wireless communication modules

Vendor	Chip	Supply Voltage	P_{min}	P_{max}
TI	CC2500	1.8 - 3.6 V	1.2 µW	64 mW
TI	CC2520	1.8 - 3.6 V	90 nW	100 mW
Maxim	MAX7031	2.1 - 3.6 V	2.4 µW	36 mW

100 mW which illustrates the high dynamic range that has to be covered by the power management unit.

Micro Controller

Exemplarily, the power consumption of three often used low power micro controllers is analyzed. These are Atmega 128A from Atmel[9], MSP430F1232 from Texas Instuments and PIC16F72X from Microchip[10]. The controller Atmaga 128A can operate with a clock frequency of up to 16 MHz. The speed depends on the supply voltage and covers a range of 2.7 V to 5.5 V. A supply current of 19 mA is given in the datasheet at a clock frequency of 8 MHz. [12]

MSP430F1232 is an ultra low power processor with different power save modes. This micro controller is also used in the sensor node AMB2520 from section 2.1. The supply voltage is defined within a range of 1.8 V to 3.6 V. The current consumption is given at a clock frequency of 1 MHz and a supply voltage of 2.2 V. Altogether five low power modes are available. The current consumption is 200 µA in active mode, 0.7 µA in stand-by and 0.1 µA in power-down or RAM retention mode. [13]

[9] `http://www.atmel.com/`
[10] `http://www.microchip.com/`

The PIC16F72X could use a supply voltage of 1.8 V to 5.5 V. Different power saving modes are available. For example, current consumption is less than 0.6 mA at 3 V supply voltage and 4 MHz clock frequency. In sleep mode, the current consumption is about 20 nA. [14]

In summary, the current consumption and the minimal supply voltage depend on the architecture of the micro controller. The minimal supply voltage, for low power architectures, is around 1 V lower than for standard high speed processors. Table 2.6 shows a comparison of the micro controllers described before with their power supply ratings where especially minimum, maximum and normalized power consumption is listed. Compared to wireless communication modules, printed in table 2.5, the standard application processors can use a higher supply voltage.

Table 2.6: Comparison of micro controller power ratings

Vendor	**Chip**	**Supply Voltage**	$\mathbf{P_{min}}$	$\mathbf{P_{max}}$	**Normalized power**
Atmel	Atmega 128A	2.7 - 5.5 V	25 µW	95 mW	11.875 mW/MHz
TI	MSP430F1232	1.8 - 3.6 V	220 nW	720 µW	720 µW/MHz
Microchip	PIC16F72X	1.8 - 5.5 V	60 nW	1.8 mW	450 µW/MHz

Sensors

This clause discusses the load characteristics of different sensor components. The requirements for the supply voltage of sensors that basically operate in analog domain are more strict than for sensors with integrated voltage regulator. An input voltage ripple can cause errors in the actual measurement quantity. Also if a good power supply rejection ratio is provided by the sensor, the ripple should be kept small to grant high sensor accuracy. Digital circuits or ASICs with integrated regulator are not that prone to voltage ripple. The sensors that are analyzed are the temperature sensor AD22103 and the magnetic field sensor AD22151 from Analog Devices[11] and the absolute pressure sensor KP123 from Infineon[12].

The sensor AD22103 basically consists of a temperature dependent resistor and an operational amplifier. Figure 2.3 illustrates a simplified schematic of the sensor circuit. The current source I in the figure is proportional to the supply voltage and creates a supply voltage dependent intermediate measurement result until this dependency is compensated via the voltage divider at the inverting input of the amplifier. The sensor is designed for a single supply voltage of 3.3 V with the limits of 2.7 V and 3.6 V. The quiescent current is given with maximal 600 µA. [15]

The sensor AD22151 is designed for measuring magnetic fields and generates an output voltage proportional to the field strength. To increase the accuracy of the sensor, a temperature measurement circuit is included on chip. The sensor is designed to be powered by a single 5 V supply voltage while the boundaries of the supply voltage are between 4.5 V and 6 V. A typical current consumption of 6 mA and a maximal value of 10 mA is specified. [16]

The third sensor example presented is the pressure sensor KP123. It is based on a capacitive sensing principle with a nominal supply voltage of 5 V and a supply voltage range from 4.5 V to

[11] `http://www.analog.com`
[12] `http://www.infineon.com`

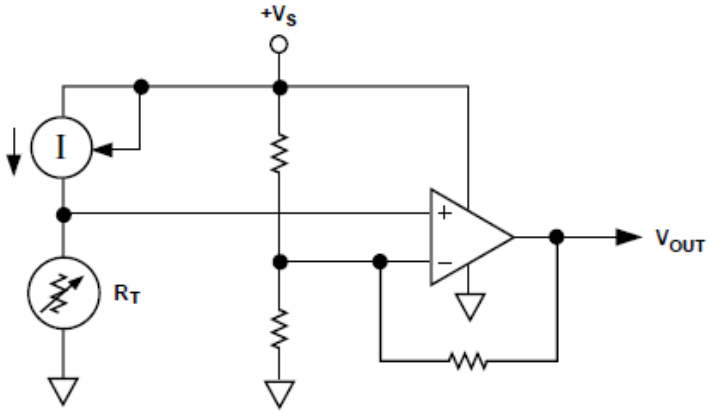


Figure 2.3: Simplified schematic of temperature sensor AD22103 from Analog Devices [15]

5.5 V. The output voltage of the sensor is radiometric which means that the output voltage is proportional to the supply voltage. The current consumption ranges from 8 mA to 10 mA. [17]

It can be concluded that sensors have different requirements to the quality of supply voltage when compared to micro controllers (see table 2.6). For micro controllers, the voltage ripple is not very important except for the integrated analog to digital converter (ADC). Most sensor outputs depend on the supply voltage at least partly and that forces the supply voltage to provide a low voltage noise to achieve an adequate accuracy. Furthermore, the supply voltage range is smaller than for digital circuits. The supply current is mainly defined by the quiescent currents. Table 2.7 shows a comparison of the electrical power values for the outlined sensor types.

Table 2.7: Supply voltage range and power consumption of sensor modules

Vendor	Chip	Supply Voltage	P_{nom}
Analog Devices	AD22103	2.7 - 3.6 V	1.98 mW
Analog Devices	ADD22151	4.5 - 6 V	30 mW
Infineon	KP123	4.5 - 5.5 V	50 mW

Energy Sources

Energy sources can be distinguished between primary and secondary batteries, and energy harvesters such as solar panels or for example electro-mechanic scavengers. This section introduces some most common components to store or harvest electrical energy.

Batteries

The most common primary or secondary batteries used in wireless sensor nodes are the AA or AAA formats. For example, the Energizer[13] L91 AA lithium battery has a nominal output

[13] `http://www.energizer.com`

voltage of 1.5 V. A discharge down to 0.9 V is possible where the voltage decreases non-linear. The maximal output current is limited to 2 A for a single cell and its capacity is 3 Ah. [7]

An interesting secondary battery from Leclanché[14] is the LiPo cell of the series 904301. It features a total thickness of just 0.2 mm and provides a nominal capacity of 1.1 Ah at an output voltage range from 3 V to 4.2 V. The nominal voltage is given with 3.7 V. Discharging to less than 3 V as well as output currents of more than 3.3 A have to be avoided to prevent cell damage. LiPo cells require a more complex charging circuit if their maximum performance should preserved as long as possible. [18]

Another possibility for supplying an electrical circuit is usage of a storage capacitor. Depending on the physical size and the maximum voltage, capacitances of up to 70 F are available in commercial products. Panasonic[15] produces capacitors with 70 F in their HW series for an operating voltage of 2.1 V [19]. The amount of electrical energy that can be stored in a capacitor is much less when compared to secondary batteries. On the other hand, lifetime, number of recharge cycles, and the maximum output current are much higher. Furthermore, charging of a capacitor is very easy using a voltage or current source.

Harvester

Compared to primary and secondary batteries, energy harvester are typically cost intensive components with low energy output. This section focuses on solar panels and piezo-electric components. As example for piezo harvester the component Volture V21b by MIDÉ[16] is outlined. It converts vibrational energy into electrical energy. Depending on the frequency of the vibration, an output power of up to 6 mW is achieved. Piezoelectric components produce an AC voltage that requires a rectification. For optimal results, the harvester has to be tuned to a specific vibration frequency. Using the harvester over a wide frequency range is not effective in terms of output power. Furthermore the device size of $91 \times 17\,mm$ is huge compared to the size of primary batteries with comparable amount of energy, but lifetime may be much longer. [20]

In contrast to the piezo electric harvester, solar panels are much easier to use. There are a great amount of different panels available with a wide spread output voltages and peak power. Document [21] gives an overview over some solar panels from Solarbotics[17]. Another benefit of solar panels is the almost constant output voltage over the output current and light intensity [Böh, p. 328f]. Figure 1.5 on page 7 illustrates the comparison of the power density of a solar panel and a peltier element that is also a type of thermoelectric energy harvester.

Conclusion

The discussed components in this section give an overview over the variety of available components. For every application field, dedicated and optimized components are available. The power

[14] `http://www.leclanche.eu`
[15] `http://www.panasonic.com/`
[16] `http://www.mide.com/`
[17] `http://www.solarbotics.com/`

consumption of radio communication modules highly depends on the data rate and transmission range while the needed energy of micro controllers is proportional to the clock frequency and very dependent from application. Furthermore, the requirements for the power supply unit are different for each module. While micro controllers are not vulnerable to input voltage ripple, such noise can reduce the accuracy mainly of analog circuits and sensors.

The easiest method for supplying a wireless sensor node with electrical energy is to use batteries. In terms of power density, batteries are a better choice than energy harvesters. A standard NiCd accumulator provides an energy density of about 180 $\frac{mWh}{cm^3}$ while a solar panel provides a typical power density of 15 $\frac{mW}{cm^2}$ [RKH+05] [Pow00]. Secondary batteries have the disadvantage that a charging circuit is needed. Energy harvesters are expansive and have large physical dimensions. On the other hand, a power aware network node could only be realized using some kind of energy harvesting if lifetime has to be more than 10 years because of the self-discharge effect of batteries. Solar panels could only operate when sufficient light is available and piezoelectric components could only be used when vibration in a defined frequency range exists. So the best fitting energy supply highly depends on the actual application. Issues that have to be considered are the environment, the power demand and the ratio of cost versus output power.

2.3 Voltage Regulator Concepts

There exist various concepts for generation of a stabilized output voltage. In this section, the most important concepts for voltage conversion and regulation are discussed. The selection is limited to methods for converting DC voltages to DC voltages. Concepts for AC to DC conversion such as rectifier circuits are not core topic of this thesis and are omitted for simplicity. Off-the-shelf voltage regulators are briefly described that implement the main different regulator concepts. The compared voltage regulators are chosen according to the following boundary characteristics.

- Tunable output voltage
- Input voltage smaller than 12 V
- Output voltage smaller than 12 V
- Output current smaller than 1 A
- Multiple output voltages (if available)

2.3.1 Linear Regulators

Linear voltage regulators basically consist of a transistor that is connected between input and output of the regulator, where the transistor operates as a variable resistor. The control loop itself works in the way that the difference between input and desired output voltage is dropped as the collector emitter voltage of the power transistor. The linear dissipated electrical energy is converted into thermal energy within the transistor. Figure 2.4 illustrates a simple regulator

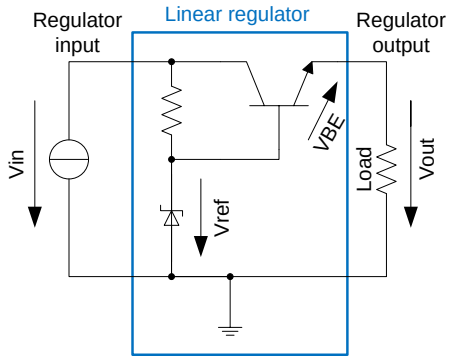


Figure 2.4: Linear voltage regulator with bipolar transistor and Zener diode as voltage reference

circuit that uses a Zener diode as voltage reference. The breakdown voltage of the Zener diode defines the output voltage of the regulator. The regulator output voltage is defined as $V_{Out} = V_{Ref} - V_{BE}$. V_{BE} of the transistor is not constant - it depends on the collector current with logarithmic function - and so the output voltage of the regulator varies according to the actual output current. A big issue for linear regulators is to minimize the dropout voltage. The dropout voltage is the minimum voltage difference between input and output at which the regulator is still working properly [Böh, p. 319]. The regulator operates in a high power efficiency region when the difference between input and output voltage is close to the dropout voltage. The efficiency - the quotient of output power over input power - depends only on the voltage drop at the transistor and is mostly independent of the output current. As a consequence, high efficiency is only achieved, if the voltage difference and the own consumption of the regulator are low [TS, p. 965]. In an other functional concept, a linear regulator can be used to decrease the ripple of the input voltage. Reducing the ripple voltage is a task where a linear regulator has to support high bandwidth and power supply rejection ratio in the high efficiency region with low voltage drop. In [YSZY08], a low drop out regulator (LDO) with a dropout voltage of 160 mV and a quiescent current of 20 µA is introduced.

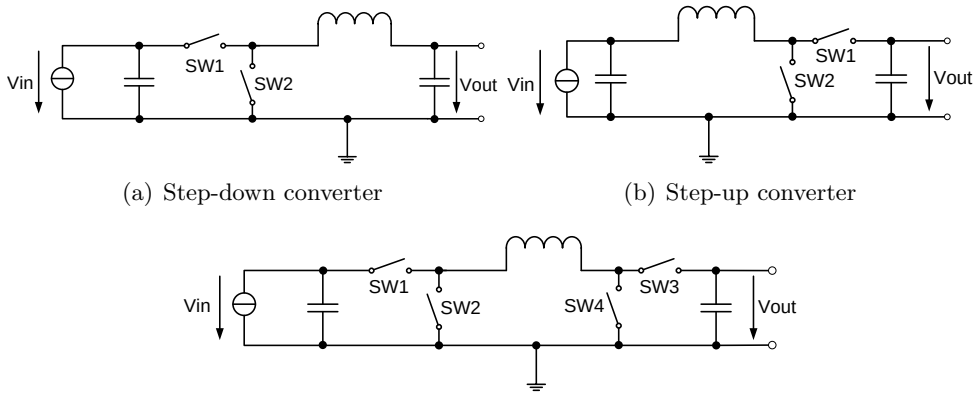
As example for a linear regulator, the MAX1705 is described. In fact it is a combination of a switched mode boost converter and a linear voltage regulator. Both voltage outputs can be used separately with the limitation that the LDO is cascaded with the switching regulator. The minimum and maximum input voltages are 0.7 respectively 5.5 V. The output voltages are programmable via a voltage divider and can be adjusted from 2.5 to 5.5 V for the step up converter and from 1.25 to 5.0 V for the linear regulator. The maximum output currents are 1 A respectively 200 mA. The switching regulator supports operation in pulse width modulation (PWM) mode and pulse frequency modulation (PFM) mode to increase power efficiency at low output current. PWM and PFM modes are discussed in detail in section 2.3.4. The overall efficiency is given in the data sheet with maximal 96 % at 100 mA, about 75% at 1 mA and around 40 % at output currents of 100 µA. [22]

The great benefit of linear voltage regulators is the low output noise voltage and the high efficiency at low voltage drops and low output currents. Combined with a switched-mode regulator, a LDO opens the way for various applications with requirements for high efficiency and high quality of supply voltage. The output ripple of the switching regulator can remain and is reduced afterwards

by the LDO. So the LDO operates in its high efficiency region and the switching regulator guarantees high power efficiency. For example, the switching frequency, and the values of the inductor and blocking capacitors can be reduced. This makes supplying of sensitive components possible combined with a high overall efficiency.

2.3.2 Inductor-based Switching Regulators

Switching voltage regulators achieve the goal of regulating the output voltage via switching the source - the input voltage - on and off. The output voltage is further defined by the duty cycle of the switching regulator. For a proper function, an energy storage is needed temporarily. The regulators discussed in this section use an inductor for energy storage. By varying the duty cycle for the switches, the output voltage is adjusted. In contrast to linear voltage regulators, which are topic of section 2.3.1, switched regulators have a theoretical power efficiency of up to 100 %, if lossless components are assumed. Via switched-mode regulators, step-up and step-down voltage conversion of the input voltage is possible. Figure 2.5 illustrates one possible concepts for implementing step-up, step-down and a combined step-up-/down converter.



(a) Step-down converter

(b) Step-up converter

(c) Step-up-/down converter

Figure 2.5: Switching concepts for inductor-based DC/DC converters

Step-Down Converter

Switching regulators that provide a lower output voltage when compared to their supply voltage, are called step-down converter or buck converter. The operation concept involves two steps. In the first step, the device for temporary energy storage is charged, while it is connected in series to the output (figure 2.5(a) - SW1 closed). In the second step, the converter input is disconnected via SW1 and the inductor is discharged into the output terminal (figure 2.5(a) - SW2 closed). The output voltage is defined by the duty cycle of these two steps and the input supply voltage. It is calculated by $V_{out} = \frac{t_{on}}{t_{on}+t_{off}} V_{in}$ where t_{on} is the time where SW1 is closed and during t_{off}, SW2 is closed. The duty cycle has to be adapted to fit to the actual values of output voltage and current [TS, p. 980f][Böh, p. 331]. The output ripple voltage of the regulator is defined by the

value of the inductor, the value of the output blocking capacitor, the actual load impedance and the input- and output voltage. Decreasing the ripple voltage would result in increased inductor and capacitor values that would also increase the physical dimensions, loss and cost. State-of-the-art step-down converter achieve power efficiencies of up to 97 % at output currents of several hundreds of mili-ampers [CHH10].

Step-Up Converter

Switching regulators with a higher output voltage than input voltage are called step-up converters or boost converters. Similar to the buck converter, the regulator operates using a two-step approach. In the first step the storage element is charged and the output is disconnected (figure 2.5(b) - SW2 closed, SW1 open). In the second step, the charged inductor is connected in series to the input voltage and that results in a boost of the output voltage (figure 2.5(b) - SW1 closed, SW2 open). The output voltage depends on the duty cycle of the switches and is defined as $V_{out} = (1 + \frac{t_{on}}{t_{off}})V_{in}$ where t_{on} is the time where SW1 is closed and during t_{off}, SW2 is closed. [Sch, p. 29ff]

Step-Up-/Down Converter

A buck-boost converter is a combination of a step-up and step-down converter. Depending on the voltage conditions for the regulator, it either operates in buck or boost mode. Such a buck-boost converter is illustrated in figure 2.5(c). Switching between the different modes of operation is only performed when the input voltage or the desired output voltage changes. There are several ways how a buck-boost converter can be implemented. In [CME01], different methods for setting up buck-boost converter are discussed. In general a buck-boost converter includes the combination of the switches of a buck and a boost converter. The capability of providing up and down conversion is paid with additional number of switching transistors which results in slightly decreased efficiency because of the additional on-resistance of the additive switches.

A typical example for a buck-boost converter is the regulator LTC 3522 from Linear Technology. It is a combination of a step-up and a step-up-down converter within a single package and provides two different output voltages. A combination of a buck-boost and a buck converter with 400 mA and 200 mA output current are implemented on the chip. The output voltages are independently configurable while each regulator requires a separate inductor. To achieve high power efficiency under low and also under high current conditions, an operation in PWM or PFM mode is supported. The magnitude of output current where the switching from PWM to PFM mode and reverse occurs, depends on the input and output voltage. The regulator uses the continuous conduction mode and this results in high efficiency and reduced noise. Continuous conduction mode means that the inductor current is controlled to omit the zero state. The output voltages are defined via a resistive voltage divider network. Allowed input voltages range from 2.4 to 5.5 V and the output voltages can be configured from 2.2 to 5.25 V in the buck-boost converter, and from 0.6 V to V_{DD} for the step-down converter. A quiescent current of 25 µA is given in the data sheet for both converters in burst (PFM) mode. The efficiency of the regulator depends on the

input voltage, output voltage, output current and the used control mode. The peak efficiency is listed with 95 % with decreased values at low output currents. Components for gate control and current measurement are implemented twice and completely independent for each sub-regulator. Only the bandgab voltage reference and the oscillator circuit is used by both sub-regulators [23].

Buck-boost converters provide the advantage of an enlarged input voltage range. Regulators with output currents less than 1 A can be implemented on a single chip without off-chip switching transistors. The external components are reduced to the inductor and the blocking capacitors. The capability of using PWM or PFM control mode provides high efficiencies over a large range of output current. The control functionality for such a converter concept could be implemented in digital logic. A combination of these two control concepts combined with a driver logic for switch control should be feasible without difficulties. The mentioned points make the use of this concept a very interesting candidate for the proposed and novel design to reach the goal of this thesis. By using the buck-boost concept illustrated in figure 2.5, an optimization trade off between peak efficiency and efficiency over an almost large load range has to be considered.

SEPIC

A single ended primary inductor converter (SEPIC) is a complex voltage regulator that offers generation of output voltages higher, equal or lower than the input voltage. As pumping component, the SEPIC uses a combination of two inductors and one capacitor. As switching components one switch and one diode are sufficient for the proper SEPIC operation. Calculation of the circuit behavior is complex because of the large component count [24]. Switch control can only be performed by a PWM circuit that causes similar problems at low output currents like an inductor-based step-up or step-down converter. Furthermore, the loss of the SEPIC are higher by design because of the three passive pumping components. Larger physical dimensions are needed and caused by the increased component count. A more detailed description of the SEPIC can be found in [24].

The voltage regulator TPS61130 from Texas Instruments is a combination of a SEPIC converter and a LDO. The input voltage range of the SEPIC is defined from 1.8 to 5.5 V and the output current is limited to 200 mA. The output voltage is programmable via an external voltage divider from 2.5 to 5.5 V independent from the input voltage. Efficiencies of up to 90 % are given in the data sheet. The LDO can eigher be used in series to the SEPIC or may also be powered directly by the supply voltage. The output voltage of the LDO is also programmable. Its output current is limited to 300 mA. The most important special feature of the regulator is a low battery comparator with programmable threshold voltage and user connectable pins. [25]

SEPIC converters have the main drawback that two inductors and a capacitor is needed for energy pumping. The additional components cause increased energy loss compared to other concepts. This limits the benefit that only one switching transistor and a diode is needed for proper function of the regulator. Furthermore the peak efficiency is defined over a small range of output currents which makes usage of this type of regulator unpractical for handling load steps. State-of-the-art technical papers show that the concept of the SEPIC converter can be used for output voltages

up to several hundreds of volts and up to more than 100 W of output power [PMY10], but this is not necessary for wireless sensor networks, where low voltage and low power consumption is of interest.

2.3.3 Capacitor-based Switching Regulators

In this section, switched voltage regulators are discussed that use capacitors for energy pumping. The capacitor is used as a temporary energy storage device and the energy is pumped from the input to the capacitor first and is then forwarded to the output capacitor. In switched capacitor circuits, direct voltage conversion to any user defined output voltage is not possible. By altering the regulator topology, addition or subtraction of voltages can be provided.

Voltage Multiplier

A voltage multiplier or a more specialized voltage doubling circuit can be realized only via capacitors and switches. The main concept is to add voltages to get a higher output voltage. The concept is to charge two parallel connected capacitors to the input voltage first. When the capacitors are charged fully, the circuit topology is changed in a way that the capacitors are connected in series, and the connection to the input is broken. So the series connected capacitors double the input voltage and provide it at the output. By connecting more than two capacitors in series/parallel and adding further switches or by cascading several stages of voltage doublers, further boosted output voltage can be reached. [Sch, p. 9f][Böh, p. 330]

Voltage Divider

Voltage divider are circuits where the output voltage is $1/n$ of the input voltage, where n is a natural number. Such circuits can be implemented similarly to voltage multipliers, only using capacitors and switches. The main concept of a divider is to split the input voltage into two or more equal parts via series connection of two or more capacitors. In [PLS04, p. 5], a voltage divider with $V_{out} = 1/2V_{in}$ and eight switches is introduced. In principle, a voltage divider can also be implemented using five switches and three capacitors. The concept is similar to the concept of voltage multipliers, but only the capacitor chain is more or less operated in the opposite direction. First, the capacitors are connected in a serial way. After charging, they are connected in parallel and all capacitors provide the output voltage.

Multiplier, Divider Combination

In the previous clauses, electrical circuits that double or half the input voltage have been discussed. By extending the control concept of the switches, a combined voltage multiplication/voltage division circuit can be implemented. If the desired output voltage is not twice or half of the input voltage, additional stages have to be added. Achieving fine-graded user-defined output voltages

is only possible via a complex set of capacitors and switches where the high amount of switches increases the switching loss [RC07].

ON Semiconductor[18] produces DC-DC converters using a charge pump with an adjustable output voltage. The component CAT3200HU2 supports an input voltage of 2.2 to 4.5 V and an output voltage from 2.7 to 6 V. The regulator uses a voltage doubling circuit that limits the output voltage to twice the input voltage or less. The output voltage is adjusted via an external resistive voltage divider. The control loop works in the way that the charge pump output current is modulated according to the sensed output voltage. The output current is limited to 100 mA while the efficiency highly depends on the ratio of output to input voltage. A voltage ratio close to 2 achieves high efficiency. This results in an efficiency of 73 % at a ratio of 1.5 and an efficiency of 55 % at a ratio of 1.1 (at 50 mA output current). For lower currents the efficiency is decreased further. [26]

Voltage regulators with charge pumps have the benefit that no costly inductor is needed. Using small capacitors and high switching frequencies make an implementation into a single chip solution possible without further off-chip components. This benefit it limited due to the fact that on-chip capacitors inhere parasitic stray capacitance to the substrate that cause additional switching loss. This type of voltage regulator needs a high amount of on-chip capacitors and consumes therefore a large amount of chip-area. All these facts limit the maximal output current of such regulators to several milli amperes. Another point is the peak current when charging capacitors via a voltage source ($I_c = C\frac{dV}{dt}$). High currents result in high loss in the switching transistors. In [SN07] a method is introduced where a combination of a capacitor and a inductor is used to limit the peak currents through the switches. The regulator is optimized for a specific output voltage that is defined via the component´s values. But when the desired output voltage is different to the optimized value, the efficiency decreases rapidly.

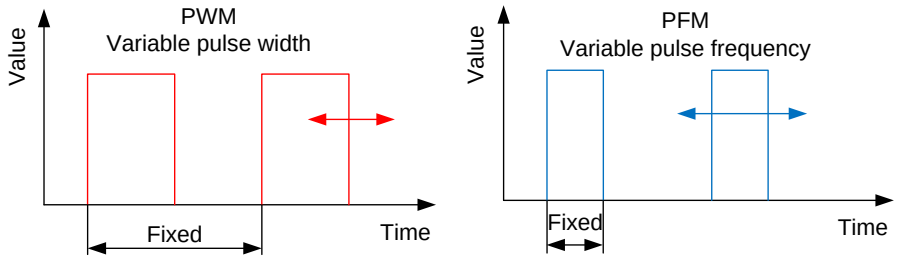
2.3.4 Switch Control Principle

This section discusses the methods for controlling the switches in converters with inductor-based power stage. The output voltage mainly depends on the duty-cycle of the switching states. Adjustment of the duty cycle of switch control is necessary when the output current is low and if a changing of the output voltage should be performed. Choosing the optimal control mechanism is important if efficiency is considered. Significant loss in switching transistors only occur at the transition from the low resistive to the high resistive state and vice versa - at switching operations. Reducing the amount of switching cycles also reduces switching loss therefore.

PWM

Pulse width modulation (PWM) is used to regulate the average output voltage via switching the source on and off. Via a change of the duty cycle, the mean value is changed too. Figure 2.6(a) illustrates the concept of a PWM signal. PWM in relation with switching regulators describes

[18] `http://www.onsemi.com`



(a) Pulse width modulation (b) Pulse frequency modulation

Figure 2.6: Simplified concept of PWM and PFM

the method of how the switches are controlled. It describes the time ratio of how long a switching state is taken. Generation of the PWM signal can be performed by comparing a saw tooth voltage with an adjustable voltage threshold using a comparator. Depending on the desired value, the duty cycle of the PWM signal is then controlled easily. The PWM controlling scheme for voltage regulators is efficient if the output current is high. In the case of low output currents, the on time (pulse length) of the PWM signal gets shorter and shorter. In the worst case, the on-times are that short that the switching transistors cannot be switched on/off completely. Then most of the transferred energy is lost in the switching transistors. [WX10][23][Böh, p. 338f]

PFM

In contrast to pulse width modulation, where the pulse width of a control signal is variable and its frequency is fixed, the pulse frequency modulation (PFM) uses fixed length pulses. The higher the value that should be represented by the modulation, the higher is the frequency of the pulses and thus the shorter is the time between these pulses. A PFM signal is shown in figure 2.6 (b). Similar to the PWM technique, the modulation controls the behavior of the switching states in the power circuit where the corresponding switches are opened or closed alternatively. Consequently, during one pulse of the PFM technique a small energy packet is delivered to the output. The PFM switching technique provides an efficiency boost, in contrast to PWM signals when the regulator output power is low. In contrast to PWM, the granularity of energy is defined by one pulse length. Because of this fixed minimum amount of energy, the voltage ripple depends partly on the load impedance. When high output current is required, the PFM controlling technique is not adequate. The time between the pulses gets shorter and shorter and results in a similar problem like for PWM coding in light load conditions. [Böh, p. 332f][23]

2.3.5 Multiple Input / Multiple Output Concepts

Although there are no off-the-shelf regulators available that use multiple input and multiple output (MIMO) concepts, MIMO regulators are an upcoming topic in regulator research. By simply adding additional input and output transistors the hardware demand on a MIMO system are met (compare with figure 2.5) [BBM08, JL09]. There are several different methods for controlling the MIMO system. In [BBM08], two separate PWM signals are used, and the PWM values are

calculated via the sum respectively the difference of two intermediate voltage error values. Depending on the PWM values, the output switching times are determined and the inductor current values are set. [JL09] introduces a dual output buck-boost regulator that operates in a pseudo DCM/CCM mode and overlays energy pulses by a predefined but adaptable direct current (DC) value for a better fit into high output power conditions. In [HC09], a similar control mechanism is discussed, but with separate buck and boost outputs and load dependent peak currents. The peak efficiency is reached at output currents above 100 mA.

2.4 Conclusion

A wireless sensor node can be build-up in various ways. Depending on the desired application, a large set of components such as micro controllers, communication modules and sensors are available. The requirements for the power supply of these components regarding quality and bandwidth is highly distinct. Points to consider are the power-saving modes of the different components. A power efficient application can only be achieved by extensive usage of the available power saving functions. This produces high load steps that have to be handled by the power supply circuitry. There are several different voltage regulators available on the market that use different conversion concepts. The optimal concept depends on the application. Linear regulators provide high efficiency under certain conditions while switching regulators provide high efficiency over a wide range of input and output voltages, and output currents. Furthermore, up and down voltage conversion is possible. Inductor based regulators are more expensive and have larger physical dimensions than capacitor based charge pump regulators, but can operate in a more dynamic way at a higher efficiency. Several additional features such as input voltage comparators as well as short circuit protection and thermal overload protection are included on the regulator chip. In order to provide different output voltages via a single voltage regulator device, two or more separate voltage regulators are packed into a single package. This results in a higher amount of off-chip components, more connection pins of the chip and a larger chip area. There currently are no voltage regulators available on the marked that provide the possibility to generate multiple output voltages via a single core-regulator. Multiple input/multiple output concepts are limited to prototypes in research activity. MIMO concepts increase the performance of the overall regulator especially when weak loads are connected to the regulator. No off-the-shelf voltage regulator has been found that supports utilization of a primary and backup voltage source. For standard architectures of primary and backup voltage, the harvester and the secondary battery have to provide an almost equal nominal voltage. Otherwise, an additional charging circuit and therefore voltage regulator is required.

3 Design and Simulation

Based on the sensor node characteristics and available control mechanisms, the power supply unit is designed. Development approach and considerations are the main topic of this chapter. The voltage regulator is implemented as a combination of analog and digital parts. To achieve a highly efficient solution, the number of analog components is reduced to a minimum. Section 3.1 discusses the starting point of the design process via selection of the regulator concept / architecture as well as additional desired features. Section 3.3 comprises the description of the digital control mechanisms and section 3.2 describes the analog design approach. In the end of this chapter, the simulation results of the proposed design are presented and discussed.

3.1 Pre-design Considerations

To define the origin of the design process, the requirements for a voltage regulator and the most promising regulator concepts are recapitulated in this section. The boarder conditions of the design and the most important properties of the desired voltage regulator are defined and the chosen regulator concept and the designated features are outlined.

3.1.1 Application Field for Proposed Design

Several state-of-the-art wireless sensor nodes and components of a sensor node have been discussed in chapter 2 and are used to define the requirements for the power supply unit and the application field of the design. From the electrical power characteristics of these components, the boarder conditions for the proposed voltage regulator are concluded.

- Output power of less than 300 mW per output
- Output voltage range of 1 to 3.3 V
- Stable operation also for capacitive loads and over full current range
- Maximum output current of 100 mA

- Input voltage range of 1 to 3 V
- Fast compensation of large load steps

Goal of this design is to implement a switching voltage regulator that is optimized for applications where low output power is required. The design should be optimized for wireless sensor nodes that are discussed in the previous chapters. An important characteristic of wireless sensor nodes is the implementation of an extensive power management. Energy management is necessary to optimize battery lifetime and response time of the network node. Components within a wireless sensor node operate at low-power mode for most of the time. On a specified condition, the components wake up to perform their measurement or communication tasks and are powered down again as fast as possible afterwards. The transitions from active mode to low-power mode and vice versa result in load steps that must not disturb quality of output voltage. Through the low duty cycle, the components of a wireless sensor node operate at low output currents most of the time. Hence, power efficiency at low output current is more important than in high current conditions. Although the power supply unit is not implemented as an integration solution in this first step, considerations for a possible chip integration are important for extrapolation. External components should be avoided and connection pins need to be reduced to a minimum to decrease physical dimensions and production costs of the chip solution. In other words, a solution with high capability for integration density should be found.

3.1.2 Design Approach

Figure 3.1 illustrates the block diagram of the proposed voltage regulator. The black lines illustrate the analog components such as inductor and switches of the power stage. This analog part is controlled by a digital logic block (blue). Analog and digital blocks communicate via proper driver interfaces. As initial point of the analog design, a combined buck-boost converter with four switches and an inductor for energy buffering is used to achieve an almost flexible regulator concept for the needs of a wireless sensor node supply. This decision is made by comparing the available regulator concepts, that have been discussed in section 2.3, as well as the requirements for state-of-the-art components from section 2.2. Figure 3.2 illustrates the conceptual structure of the chosen architecture with ideal components. To provide high power efficiency at low loads, the PFM control mechanism is selected. Some variations of the pulse frequency modulation are compared to develop the optimal switching method.

Multiple Output Voltages via Time Domain Multiplexing

As mentioned in section 2.2, different types of components are used within a wireless sensor node. It is likely that parts of the wireless sensor node needs to be supplied by different supply voltages. Various, and separately configurable output voltages provided by a single voltage regulator open a new way for creation of small and power efficient sensor nodes.

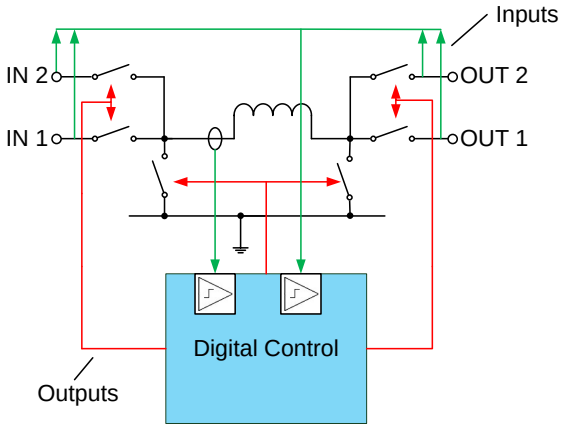


Figure 3.1: Block diagram of proposed design

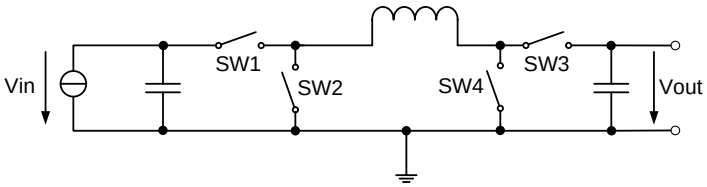


Figure 3.2: Schematic of the designed buck-boost converter power stage

Figure 3.3 illustrates a method to extend the concept of figure 3.2 to multiple outputs. This hardware-enlargement is also reported in state-of-the-art designs from research [BBM08][JL09][HC09]. Via controlling the switches SW3A and SW3B, either the first or the second output is operated via a time-division multiplexing principle. Charging of both output capacitors at the same time is not intended. This way different output voltages can be provided at the different outputs. The outputs are accessed via time division multiplexing with priority management. The low priority output - output 2 - is only supplied with energy when the high priority output voltage - of output 1 - is already stable.

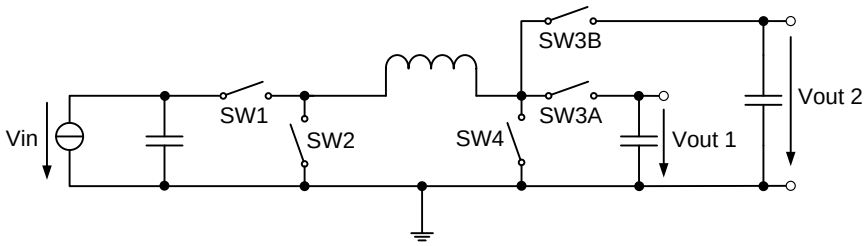


Figure 3.3: Dual output buck-boost converter

Benefit of the presented method is, that multiple outputs are realized only by adding one additional switching transistor and the obvious smoothing capacitor. Considering low output currents and PFM as control technique, the outputs operate completely independent of each other. In high current conditions, the increased load will lead to an increased output ripple at the low priority output. The higher the load on the high priority output, the longer is the time until the low priority output is served. It has to be considered that this may result in increased voltage

ripple at the second output, if the whole regulator is overloaded. It is not intended to implement a dynamic priority management feature, where the priority chain can be programmed. An implicit relation (output 1 = high priority; output 2 = low priority) increases regulator usability for the developer. Changing the priority sequence during runtime is only needed in some special cases when for instance, the priority of the components depends on external conditions. Priority management implies some kind of boot sequence of the outputs. Figure 3.4 illustrates the behavior that the low priority output is provided with energy after the high priority output holds its desired voltage value. Furthermore, every output can be shut down via disabling the corresponding output switch. When compared to a design with multiple voltage regulators, the required quiescent current is reduced, since all control circuitry is implemented only once.

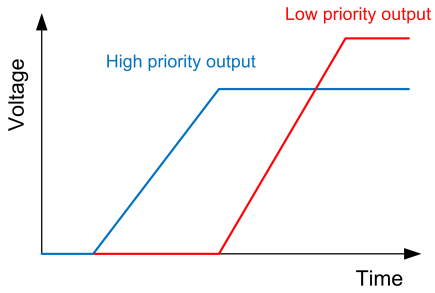


Figure 3.4: Desired startup behavior for dual output operation with priority management

Multiple Input Voltages via Time Domain Multiplexing

Off-the-shelf voltage regulators are designed for the support of one input voltage. In case of multiple regulators within a single package, the different regulators can have independent inputs. This is not suitable for nodes of a power aware network. Power awareness defines that the node is supplied by energy harvesters that depend on the availability of light, vibration or any other kind of usable energy source. The gathered energy is stored in a secondary battery or capacitor to bypass an energy gap if the harvester is not able to deliver sufficient power. A voltage regulator with several inputs combined with priority management provides the advantage of the possibility to use a primary and a backup supply voltage. Electrical energy is taken from the high priority input when energy is available, and the used voltage input is changed when no electrical power is available at the high priority input. The backup supply is used until the high priority input provides energy again. Figure 3.5 illustrates the concept of a multiple input buck-boost converter

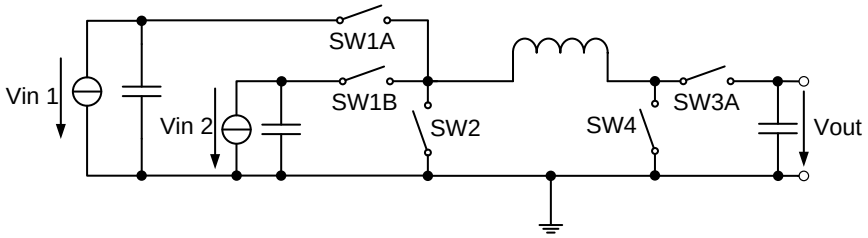


Figure 3.5: Dual input buck-boost converter

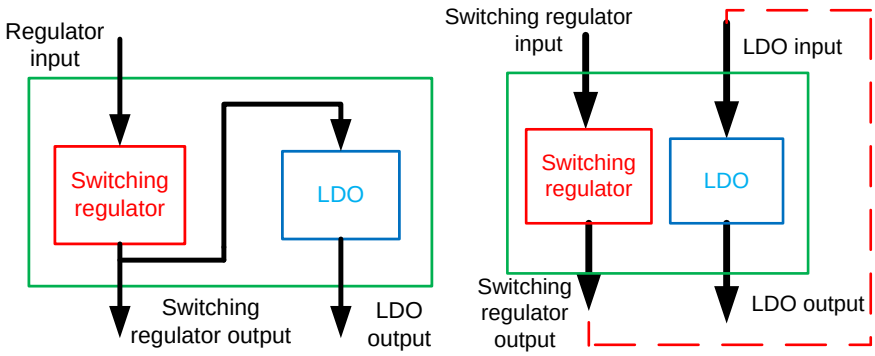
as outlined in section 2.3.5. The extra components for the second voltage source are an input blocking capacitor and a switching transistor. The main concept is that the inputs are used in a time division multiplexing manner combined with priority management provided by the control circuit. The selection of the actual voltage source is handled via the switches SW1A and SW1B. Similar to the multiple output regulator concept from section 3.1.2, the priorities of the inputs are set in an implicit way. When the PFM controlling mechanism is used, the input voltage source can be changed each time an energy packet is delivered from the regulator input to the output.

The concepts of multiple inputs and multiple outputs can be combined without problems. This way special use-cases such as a combination of an energy harvester together with a backup battery can be implemented easily.

On-chip LDO

As mentioned in section 2.3.2, a common solution is to integrate a low drop-out linear voltage regulator (LDO) into the same package together with the switching regulator. When the LDO operates at its intended field of operation, high efficiency as well as a low output ripple is achieved. This is the case when the difference between the input and output voltage and the output current is low. Especially a combination of switching regulator and LDO provides several benefits. The LDO can provide a low ripple voltage and the switching regulator can be designed with less focus on the output ripple. So a lower switching frequency as well as smaller external components can be used and offer low cost and small size.

There are mainly two ways to connect the LDO. Either the LDO can be connected internally to the output of the switching regulator, or it uses a separate input pin. Figure 3.6 illustrates the two methods. Sub figure (a) illustrates the possibility to connect the LDO to the output of



(a) Static connection to switching converter output

(b) Separate input and output pin

Figure 3.6: Connection options for an internal LDO

the switching regulator. Two different output voltages are possible with the restriction that the output voltage of the LDO is smaller than the voltage of the switching regulator. Sub figure (b) contains the block diagram of the second method. The LDO is integrated onto the same chip but operates completely independent from the switching regulator. Any input voltage can be

chosen for the LDO. Using a trivial electrical connection (red dashed line in figure 3.6 (b)), the same function compared to sub figure (a) is achieved. This method has the advantage of higher flexibility to fit to the user requirements, bit increases pin count.

3.2 Power Stage

The power stage contains the power switched on the one hand as well analog voltage comparators and a current amplifier and accordant comparators on the other hand. The demands and requirements for these analog components are discussed and the physical implementation of the switches is described in this section.. Auxiliary topics such as power-up circuits, the actual voltage feedback implementation with reference voltage generation and driver circuits for the switching transistors are excluded for simplicity in this first step. For these analog parts a wide range of state-of-the-art products and literature is available and therefore, detailed design of these components is not core of this thesis.

3.2.1 Power Switches

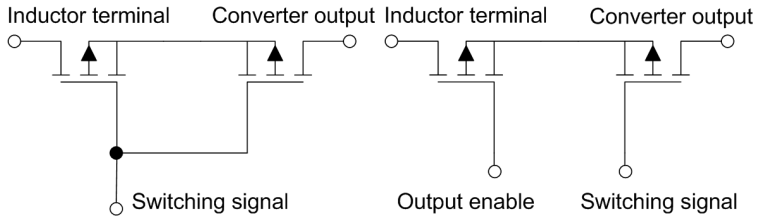
In the previous design considerations, ideal switches have been used. This section discusses issues of non-ideal switching devices in case of metal oxide semiconductor (MOS) field effect transistors (FETs). Referring to figure 3.2 and to the electrical characteristics of N and P channel power MOS FETs, the switches SW2 and SW4 are replaced with N channel FETs. The input and output switches SW1 and SW3 are built with P channel FETs.

Due to the characteristics of the power MOS FETs, a parasitic diode is located between drain and source. It is called body diode. When the drain-source voltage exceeds the forward voltage of the parasitic diode, the FET cannot be disabled. To grant proper function of a switching regulator, the source terminal of the input transistor (SW1) hast to be connected to the input voltage source and the source of the output transistor (SW3) must be connected to the load output. Otherwise, the input and output cannot be isolated from the regulator hardware. [TS, p. 212f]

When the multiple input and multiple output scheme is included into the design, an additional problem occurs regarding the switching transistors. Using one switching transistor is only possible for a single input and a single output topology. When using two different outputs, an electrical connection between the multiple outputs can occur via the body diodes of the power MOS transistors. For example, if two output voltages are considered and the output switch of one channel is closed during normal operation, then the other output switch has to be open in case that the second output voltage is either lower than the first one and also in case that the second output voltage is higher. This means that the second switch has to isolate positive and negative voltage drops. Consequently, the body diode is disturbing operation, because it would short at least one direction. Because of symmetry, similar effects occur when using the other output channel vice versa.

To solve this problem, two switch assemblies are developed. Figure 3.7 illustrates both connection schemes for the output transistors that can handle the described mode of operation properly where

the inner connection is connected to the inductor and the outer connection is connected to the input or output.



(a) Equal transistors

(b) Output enabled switching transistor

Figure 3.7: Two proposed concepts for the switching transistors

Sub figure (a) shows the scheme with two identical transistors that use the same control output. The benefit of this method is that these two transistors isolate the circuit in both directions in spite of the FET's body diode, but it has the drawback that twice the on-resistance and twice the gate charge is present when compared to a single transistor switch. This results in increased switching loss as well as longer switching times. Method (b) uses two control inputs for the transistors. One for the switching control itself and one for enabling the accordant output/input channel. The benefit of this method is that for enabling/disabling of the input/output a large and slow transistor with a low R_{DSon} value and a high gate charge can be used. The gate charge has no significant impact to the efficiency because of the low switching frequency. Drawback of method (b) is that the parasitic body diode is active for every enabled output which is not the case in method (a).

In the actual design, the method from figure 3.7 (a) is used because the drain-source diode of the transistor causes energy loss that has a great impact to the overall performance because of the low voltage values used. The described body diode difficulty only occurs when discrete power transistors are used. In case of an integrated solution, the bulk connection of the transistor is free accessible. Then, the bulk can be connected to the highest available electrical potential. So the body diode is permanently disabled and the usage of the double transistor scheme becomes obsolete. So power efficiency is further increased. Only for the discrete solution of the prototype, the double transistor concept is used.

3.2.2 Current Amplifier

The current amplifier is a main component of the proposed voltage regulator architecture. Inductor current measurement is implemented via a shunt resistor. The voltage drop across the shunt resistor is too small to be connected directly to a voltage comparator, so pre-amplification is necessary. For proper function, the current amplifier has to offer low power consumption and high bandwidth. High speed is needed to get correct measurement of the inductor current that has a bandwidth of up to 10MHz, depending on the used inductor value and the actual current limit. To save electrical energy, it is possible to turn off the amplifier when the inductor current

is zero by design. This increases power efficiency especially at low output current and excessive PFM operation. When powering up the amplifier again, sufficient short setup time has to be ensured in order to guarantee the correct output voltage until the first current threshold (I_L) is reached. This time is about some hundred nanoseconds and depends on the used inductor.

To minimize power consumption of the current measurement circuit, a simple difference amplifier consisting of one operational amplifier and its peripheral components is used. The basic concept is illustrated in figure 3.8.

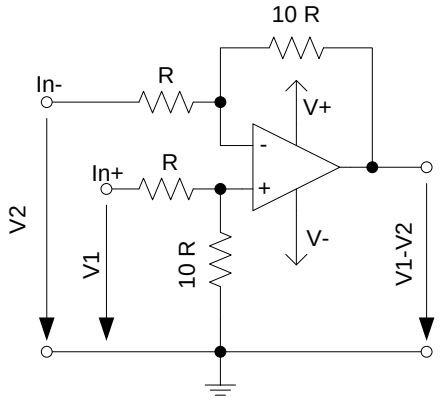


Figure 3.8: Current sense preamplifier with differential inputs

3.2.3 Voltage Comparators

Other critical analog components of the proposed design are the voltage comparators. Comparators are used to determine current thresholds as well as for monitoring of input voltage and output voltage. Depending on the purpose of the comparator within the design, the speed requirements are different. For example, the input voltage changes its value comparably slow because of the blocking capacitors, so the speed of the comparator for detection of sufficient input voltage is not as important. The comparators for supervisory of the output voltages are more time critical. The delay of the comparator has an impact to bandwidth of the control loop and the ripple voltage of the output. The comparators who determine the inductor current thresholds have the most strict timing requirements. A variation of the delay results in inaccurate current thresholds and therefore in a variation of switching frequency and output ripple. It has to be ensured that the maximum peak current is not exceeded significantly. Zero current threshold detection is also critical. When this threshold is reached the regulator is switched to idle state. The remaining energy that is stored within the inductor when switching off the power stage is lost. So the propagation delay of this comparator has direct impact to the regulator efficiency. Under low output current conditions, the zero current threshold is used more frequently than in high output current conditions, and so this effect is more important when the output current is low.

As proposed in section 3.2.2, the high speed comparators for the current thresholds are powered down if the regulator is in idle mode. In combination with the current amplifier, the outputs of the comparators have to provide the correct states when the first current threshold is reached. In

order to prevent the digital system from wrong comparator outputs during idle mode, comparator outputs must not be computed in idle times.

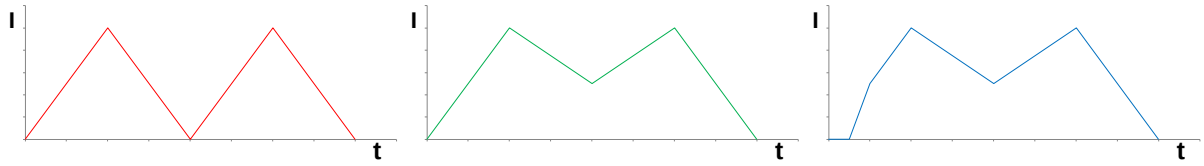
3.3 Digital Control

This section discusses the digital design and the control mechanism that are the main innovative part of this thesis. The converter architecture has already been discussed in section 3.1. It also includes the proposed topology of the power switches. Now, the digital implementation of the control circuit is in focus. First of all, the concept of the control of the inductor current and the method of buck-boost switching is discussed. The developed concepts lead to the design of a state machine. Later section 3.3.4 describes the concepts for control of multiple input and output channels as well as the hard coded priority management for the inputs and outputs. The last sections address considerations for practical implementation and covers cross-conduction avoidance and the clock generation concept for minimizing power consumption.

3.3.1 Modes of Operation

PFM Implementation

There are even different implementations of the PFM modulation possible for the usage in switching regulators. These result in different waveforms for the regulated inductor current. Figure 3.9 illustrates three energy pulses in different operation modes where step-down conversion is assumed. One possible implementation is to define a maximum inductor current. The inductor is charged until the peak current is reached. Then it is discharged via the converter output until the current becomes zero. The inductor current remains zero until an additional energy packet is started and delivered to the output. The maximum energy throughput is reached when the time between the energy packets is zero, as illustrated in figure 3.9 (a). This implementation is used in the switching regulator of the LTC3522 (Linear Technology) in PFM mode. The implementation from figure 3.9 (b) illustrates the a current mode control scheme with continuous conduction and PFM. The inductor current is regulated within the range between I_{min} and I_{max}. The current profile is similar to the current profile of the pulse width modulation. The current remains within the current window until the output voltage reaches its designated value. Depending on the voltages and currents, the number of cycles can vary. The maximum energy throughput is reached when the inductor current does not get zero. Compared to sub figure (a) the average of the inductor current is higher and that results in higher maximal energy throughput and thus higher efficiency because of the reduced crest factor. Figure 3.9 (c) illustrates the continuous current implementation with additional fast start-up state. It works mainly equivalent to the continuous current implementation but with the difference that the transition from stand-by to active mode is accelerated. The inductor is directly connected to the input voltage and charged while the load is disconnected and this results in a fast rise of the inductor current. The high current slope reduces the regulator start-up time especially when the first current slope is slow. This is the case when the voltage drop at the inductor is low.



(a) Return to zero (b) Continuous conduction (c) Continuous conduction with fast start

Figure 3.9: Time domain illustration of inductor current waveform for different PFM implementations in step-down conversion mode

The current waveform of 3.9(c) illustrates such a condition for buck-mode operation. When operating in boost mode, the so-called fast stop method is used similarly to discharge the inductor faster. Then the fast current slope is at the end of each energy packet.

Fast Start Implementation

The benefits of the continuous current implementation compared to the return to zero method Are easy to explain. The higher energy throughput within the same time extends the power range for operation and increases the control loop bandwidth. The fast start feature brings additional complexity when compared to the continuous current implementation. Because of the higher slope of the inductor current in the beginning of the energy pulse, the on-time of the regulator decreases. This increases the time where the components within the regulator (comparators, amplifiers, etc.) can remain in a power saving mode. The time reduction depends on the value of the inductor that defines the maximum slope of the inductor current. Furthermore, it depends on the actual values of the difference between the input and output voltage The maximum gain appears at low voltage drop at the inductor. The amount of the saved energy therefore is related to the amount of saved time, and the power consumption of the components in active mode can be reduced. The main drawback of this concept is that the amount of transported energy is lower than without fast start due to the reduced are in the current-over-time diagram . Furthermore, the loss from the on-resistance of the switching transistors is marginal higher because of the slightly higher inductor current. The influence to power efficiency depends on numerous facts and conditions, so general prediction is impossible, but the impact to efficiency is not very strong.

A great improvement of the regulator behavior occurs when the fast start method is combined with the multiple output concept from section 3.3.4. An important case for fast start principle is the multiple output system where the outputs can be multiplexed at each state machine transition, and one output voltage is almost equal to the input voltage. The very slow current slope of one output would block the other regulator output channel for a long time until the accordant current threshold is reached and this prevents output channel switching. So the other output would miss its control goal. The significant time reduction increases the bandwidth of the control loop and makes the behavior much more predictable. In the case of a multiple input and a single output system, the fast start method can provide similar benefits when the energy output of the harvester is limited to short time slots. The usage of the multiple input/output architecture in

combination with other PFM controlling mechanisms is possible with the drawback of possibly low speed. Because of the digital implementation of the control circuit, a configurable version of the control algorithm is possible for maximum flexibility and without major drawbacks.

Sources of Loss

An important task for optimization of power efficiency is identification and reduction of main sources of loss. Power loss is generated by the digital and the analog circuitry. It can be divided into static loss - mainly leakage - and dynamic loss that is caused by the state transitions of for example digital logic. The static loss is mainly dependent from semiconductor technology and temperature, while the dynamic loss depends at first on the switching frequency of the digital parts. Static loss of the switching transistors is caused by the on-resistance where the power loss also depends on the current value ($P_L = I^2 \cdot R_{DS}$). Dynamic loss of the switching transistors is caused by charging and discharging the MOS transistor gates. The power consumption of the analog components such as comparators and the current amplifier can be separated to active consumption and stand-by power consumption. In general, the calculation or estimation of the loss that is caused by the inductor is much more difficult. The equivalent serial resistance (ESR) is in general frequency dependent and contains the resistance of the copper wire, frequency dependent resistance from the skin effect, and loss of magnetic inductor core. These values are proportional to $\sqrt{f}$ where f is the switching frequency of the inductor current. So, a reduction of the high frequency components of the inductor current spectrum also reduces the inductor's loss. The impact of the AC loss of the inductor can be neglected for frequencies up to 1 MHz [BRK94][27]. Higher frequency values occur when a small inductor is used to force a high switching frequency for high integration density.

3.3.2 Buck-Boost Mode Transition

The changeover between buck and boost switching mode is a non-trivial task for DC-DC regulators. A non-ideal step-down converter is not able to provide an output voltage that is equal to the input voltage. This is caused by the ESR loss in the transistors, inductor. Furthermore, the maximum output voltage of a step-down converter depends on the output current and thus the actual load condition. So, the optimal voltage threshold for buck-boost switching is variable. Transitions from boost to buck mode cause similar problems. The proposed solution determines the buck-boost switching decision with the help of current thresholds. Figure 3.10 illustrates the behavior of the inductor current profile for the two mode transition possibilities. For the proposed implementation of smooth transitions between both modes of operation, two additional current thresholds are required. One above the maximal current I_H and one below the minimal current I_L. The new thresholds are called I_{HH} and I_{LL}. The left part of figure 3.10 illustrates the current waveform for transfer of a single energy packet in buck mode (red line). When the converter operates in buck mode and the output voltage is higher than the input voltage, the inductor current does not increase any more to follow the expected characteristic for buck conversion. Instead, after reaching I_L, the inductor current decreases because of the opposite polarity

of the inductor voltage. When the threshold ILL is crossed instead of the expected I_H threshold, the converter recognizes a required change of the operating mode and it switches from buck to boost operation. Then, the power switches are controlled to operate in boost mode further on (see blue line). The boost-buck transition works in a similar way. On the right part of figure 3.10, the transition from boost to buck mode is illustrated. Again, after reaching I_H, the current is expected to decrease because of the negative voltage difference across the inductor (see red line),if the converter works in boost mode. Instead, the input voltage is higher than the output voltage, and the current increases further. When the threshold I_{HH} is exceeded, the converter detects a boost-buck mode change and controls the power stage accordant to buck mode from now on. Figure 3.11 in section 3.3.3 illustrates the transitions in the state chart of the designed digital state machine. It implements 4 states and additional state transitions for the buck-boost mode changeover. This is necessary to react to the modified conditions. The concept works equally when multiple concatenated energy pulses are delivered.

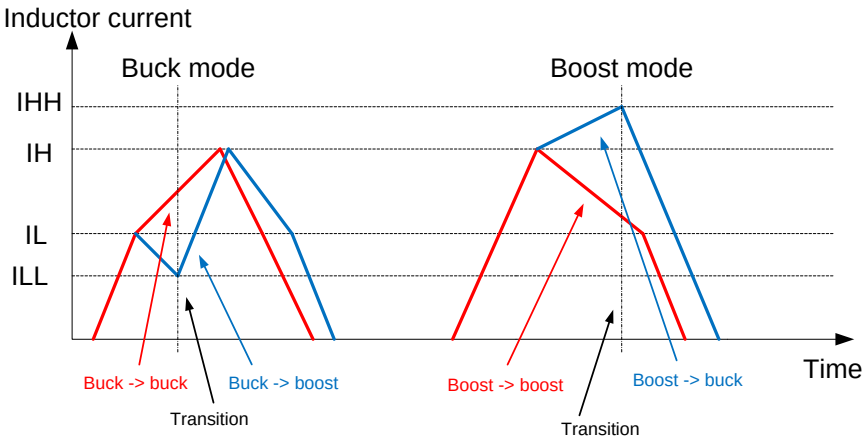


Figure 3.10: Time domain illustration of inductor current at step-up/down transitions

3.3.3 Digital State Machine

The main core of the digital control circuit implementation is a state machine. It is designed as a Moore machine which means that the output values only depend on the actual state. Figure 3.11 illustrates the state chart of the introduced design. The drawings within the figure show the accordant status of the switching transistors in each state and define the output values of the state machine. The design describes a buck-boost converter with one input and one output. State transitions are mainly based on threshold crossings of the inductor current. The two thresholds I_H and I_L define the maximum and minimum current for nominal operation. The thresholds I_{HH} and I_{LL} are needed for the change of the operating mode from buck to boost conversion and vice versa. I_z is used to determine the zero current state of the inductor. V_m monitors the output voltage and indicates a necessary charging of the output channel. The *boost* signal determines the actual operation mode. It is managed by the state machine without external events from the analog circuitry.

After the asynchronous reset, the state machine is in state 0 and the internal boost signal is 0 as well (buck-mode). When the V_m signal gets high, state 1 is reached in the next clock period. This state represents the fast start method of the buck-converter of the proposed design (compare with section 3.3.1). When I_L is exceeded, state 2 is entered. In state 2, the normal operation of the buck converter starts and toggles between state 2 and state 3 until the configured output voltage is reached. The inductor current is controlled to remain between I_L and I_H in a constant conducting mode. If the nominal output voltage is reached, the state machine stays in state 3 until the inductor current becomes zero. Finally, the transition to state 0 (idle state) is performed until energy is required again at the output. When the buck converter resides in state 2, it expects that the inductor current rises because of the usually higher input voltage when compared with the output voltage. But if the inductor current decreases further, this is an indication that the output voltage is higher than the input voltage. Then, a mode switch to boost mode and a transition to state 1 is performed. The boost converter also forces the inductor current between the thresholds of I_L and I_H while toggling between state 1 and state 2. When the programmed output voltage is reached, the inductor is discharged in state 3. This is the implementation of the fast stop method of the boost converter. Considering the boost converter in state 2, the inductor current is expected to decrease. If the current increases further and exceeds I_{HH}, this is an indication that the input voltage is higher than the output voltage. Then a mode switch to buck conversion and a transition to state 3 is performed.

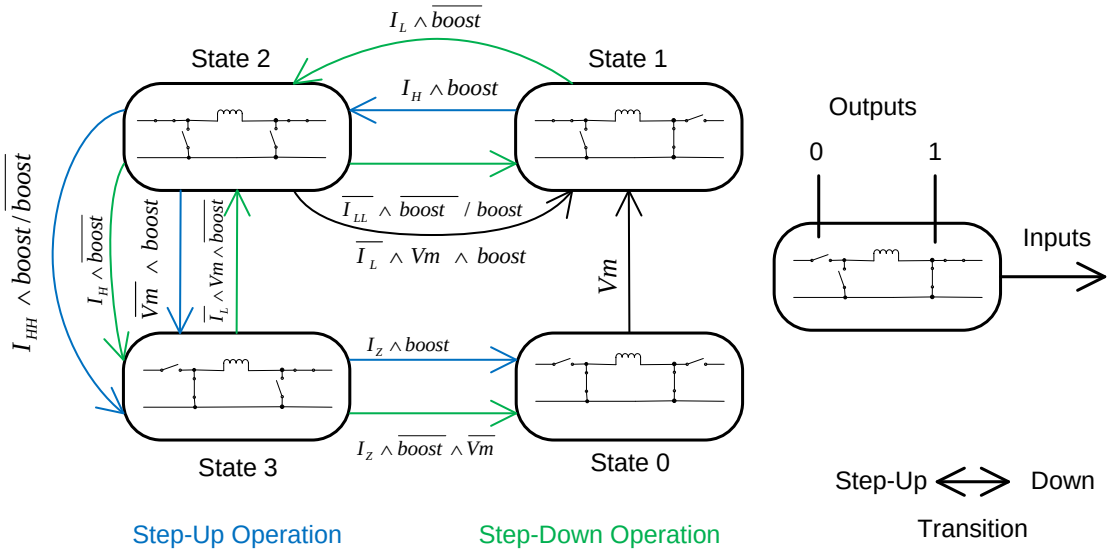


Figure 3.11: State chart of proposed design with single in- and output

One possible implementation of the multiple input and multiple output concept is via inclusion of the input and output channel switching as well as the priority management into the state machine. Considering two independent inputs and two independent outputs, five additional states are required to cover any allowed power switch constellation in a separate state. Figure 3.12 illustrates a state chart for two inputs and outputs with nine different states. In this case, not only the state changes and the buck-boost switching has to be considered, but also the channel switching between the two inputs and the two outputs. This results in typically more than 40

useful transitions in the state chart is not shown in figure 3.12 due to clarity reasons. Additional inputs or outputs would result in exponential growth of states and transitions and complicates the design and would decrease abilities for debugging and extension. Therefore, another method for the support of multiple inputs and outputs is necessary.

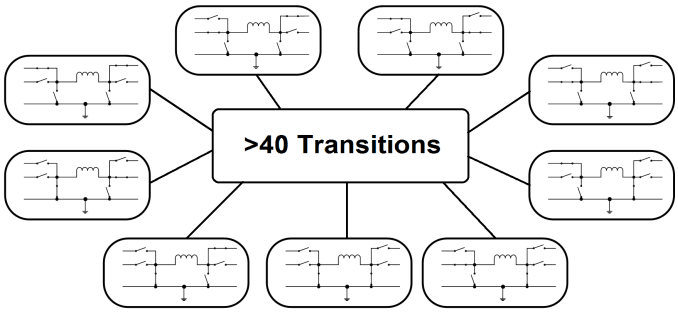


Figure 3.12: Complex state chart for dual input and dual output control

An alternative concept is to use a multiplexer/demultiplexer scheme for the multiple input/output management. The state machine is the same like in figure 3.11 and supports single I/O. The control of the different inputs and outputs is provided by additional digital parts. The switches SW1 and SW3 are converted to virtual switches that are not present in the physical design. The control signals for these switches are connected to the output switch and the input switch logic that perform multiplexing/demultiplexing as well as the priority management. Control signals for SW1A, SW1B, SW3A and SW3B are connected to the gates of the physical switching transistors (compare with figures 3.5 and 3.3). The control signals for SW2 and SW4 are not affected by this extension. The benefit of this concept is that the state machine has a limited complexity and is therefore less complicated to implement and the design offers better modularity. The behavior of the state machine can be changed independently of the priority management and adding/removing of inputs and outputs is comparably trivial. This also increases the maintainability of the system.

Event Triggered Control

The main power loss within a digital circuit is caused by state changes of the digital logic. Switching loss dominate over the static loss that is caused by leakage currents because of the low gate count. So transitions between the logic levels have the highest impact to digital loss. In case of information storage components such as flip-flops, loss is not only caused due to logic state transitions on the output but also when a clock event reaches the flip-flop. The energy consumption is almost unchanged independent from a state change [MNB01]. In other words, a clock triggered state machine would consume the same amount of power even when a state change is performed or not. Considering this fact, the main loss is caused because of the clock signal. The energy demand of the digital implementation can be lowered significantly via reduction of the number of clock events. In the case of a switching regulator at low load condition, the regulator remains in idle mode, and the reduction of clock events is simple and reasonable. The consequence is an event triggered state machine that changes its state only via external events and does not need a separate clock frequency. Such events are for example the crossing of a current threshold

or any other input signal from analog domain. Then , there is just a single clock event per state change and power consumption is reduced to a minimum. An additional benefit of omitting a permanent clock signal is that neither an external (or internal) crystal is needed nor an oscillator circuit for clock generation. The determination, if a clock event must be generated is done via comparison of the current and the future state of the state machine. A simple clock generation circuit can be implemented via combination of the flip-flop input D_n with the output Q_n by XOR and combining the results of each flip-flop by an OR gate.

$$C = Q_0 \oplus D_0 \vee Q_1 \oplus D_1 \vee \ldots \vee Q_N \oplus D_N \tag{3.1}$$

The equation above shows how the clock signal can be generated for N flip-flops. Figure 3.13 illustrates a conceptual schematic of the clock generation circuit. The illustrated flip-flops represent the states of the state machine and the combinatory logic block contains the digital logic for state transitions. The clock signal at the output of the OR gate has the defined length of the latency of three logic gates (flip-flop, XOR gate, OR gate). It has to be assured that every clock-sensitive component in the design can detect this short clock peaks. Otherwise, the peaks have to be extended by an additional circuit.

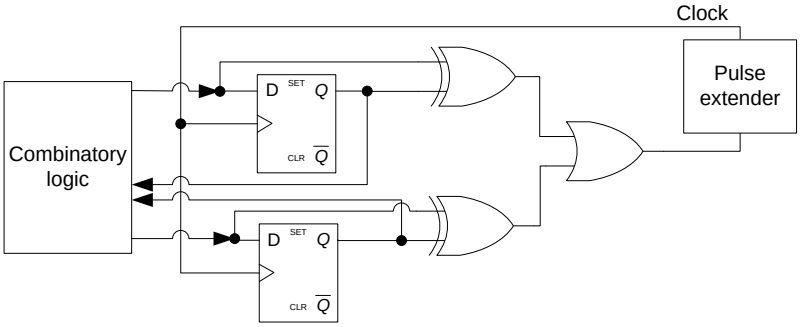


Figure 3.13: Introduced clock generation circuit

3.3.4 Multi Channel Operation

As illustrated in figure 3.1, the digital parts control the switches according to the input and output voltages and the inductor current. Figure 3.14 shows the block diagram of the digital control. Beside the state machine and the enable logic, the digital control consists of output and input multiplexing circuit, which is topic of this section.

Output Multiplexing

The output channel switching circuit provides several tasks. Multiplexing of one control signal to two switching signals, priority management and avoidance of overlapping of complementary switching transistors. The input of the circuit is connected to the state machine and the outputs are connected to the transistor driver or directly to the transistor gates. Figure 3.15 illustrates

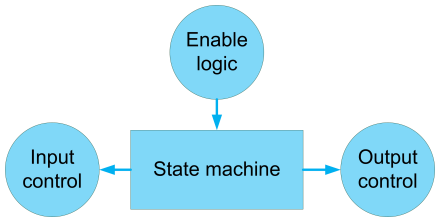


Figure 3.14: Block diagram of digital control

the schematic of the proposed design for the output switching circuit. The concept of the output multiplexing is, that a change of the used output channel can be performed only when a state transition of the state machine occurs. As mentioned in section 3.3.3 and figure 3.11, each state represents a different switch setting. So a change of the output channel at a state transition does not have any feedback to the behavior of the actual state machine. For any other part of the digital design it is not important if for example SW3A or SW3B is closed. The output channel switching is related to the priority management and handled by the priority management section in figure 3.15. The signals *Output 1* and *Output 2* determine which output needs to be charged. They are synchronized and change only at state transitions. and when any of the outputs requests energy. The priority management is implemented via a simple method. If Output 1 is high, the high priority output is charged and SW3A is closed. If Output 1 is low and Output 2 is high, the low priority output is charged and SW3B is closed. For safety reason, at least on output channel is selected. Otherwise, abnormal discharge if the inductor can cause a voltage peak and can damage the connected components. The illustrated circuit only becomes active when the virtual switch SW3 (either SW3A or SW3B)is closed. The shoot through protection part illustrated in figure 3.15 ensures that the corresponding complementary switching transistors are not closed at the same time. The affected switches are SW3A, SW3B and SW4. Such a behavior would result in a short circuit of the outputs channels or an unwanted short cut of the two outputs channels. In any case the resulting loss would be unacceptably high. To simplify the adjustment of the timing of the switching signals, each MOS driver output is also connected to a digital input. These signals are called the feedback signals S3A Feedback, S3B Feedback and S4 Feedback. The signals indicate if the transistor gate has already switched correctly and assure that a switch cannot be closed until the corresponding ones are open.

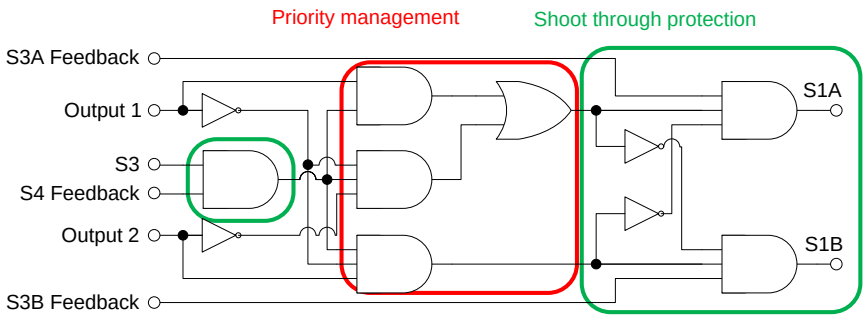


Figure 3.15: Proposed output multiplexing circuit with two outputs, shoot through protection and priority management

Input Multiplexing

The proposed input control circuit provides similar tasks such as the output control circuit. These are input multiplexing, priority management and shoot through protection The input signal comes from the state machine and the outputs directly control the driver of the switching transistors. Figure 3.16 illustrates the schematic of the designed input control circuit. The concept of input multiplexing allows for channel control independently from actual state machine implementation. The functionality is very similar when compared with the output control circuit. Again, state-synchronized channel switching is performed according to priority management from figure 3.16. The signal *Input 1* indicates availability of the primary voltage source. Extra inclusion of the backup voltage source into the priority decision is not necessary. In case that none of the input voltage sources is available, the DC/DC converter is not started. When the primary voltage source is available it is used, otherwise the backup source is used. This decision is made for every energy packet that should be delivered, so very fast input channel switching is possible. The signal overlap avoidance part of figure 3.16 is necessary to ensure that the corresponding complementary input switches are not closed at the same time. The affected switches are SW1A, SW1B and SW2. Such a behavior would result in a short circuit of the power sources and waste energy. The input switching circuit uses the same circuit for overlap avoidance such as the output control. The feedback signals from the gate drivers are S1A Feedback, S1B Feedback and S2 Feedback. These signals indicate if the transistor gate is already in its final state to detect the real latency.

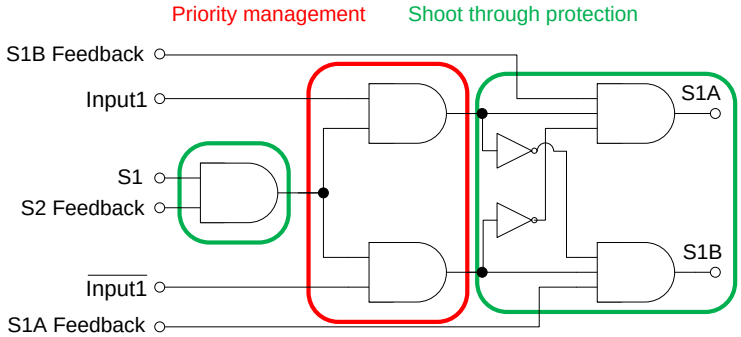


Figure 3.16: Proposed input multiplexing circuit with two inputs, shoot through protection and priority management

Shoot Through Protection

When the proposed concept with four switches is used, timing and latency is more important than for architectures with switches and diodes. Even small timing violations can result in high power loss and decreased power efficiency. Due to the switches, the inductor current is not limited into any direction. When the inductor is completely discharged ($I_L = 0$) and it is still connected to the output, the inductor is charged again, but in opposite polarity by the output buffer capacitor. The current changes its direction and the output is discharged. On the other hand, when the inductor is not discharged completely and is disconnected from the output, voltage peaks can occur and destroy components of the voltage regulator, and the remaining energy in the inductor

is lost. So it is important to disconnect the output from the inductor as accurate as possible at $I_L = 0$. Another important timing constraint is accurate control of the complementary switches. The switches at the input and the output are controlled complementary in pairs. Because of the limited speed of the switching transistors, the switching takes a specific amount of time in nanosecond range. When both switches are closed at the same time, the input or the output is shorted to ground. High currents across the switching transistors are the consequence and waste lots of energy. Timing has to be considered also in the digital logic parts of the implementation. Every logic gate has a specific propagation delay. Different delays of multiple signals have to be considered in combination with the behavior of the analog components to guarantee synchronized operation.

Timing considerations have also be done for the input signals. Some signals have to be processed as fast as possible. For example, the signal used to activate the converter from idle state is important for the overall regulator bandwidth and must have minimum delay. On the other hand, these comparators for voltage monitoring should have ultra-low power consumption during standby. When the comparators are switched off to save energy ,it is important that the values of the last output state are available to the digital logic without interruption to guarantee correct behavior of the logic functions. To prevent the digital implementation from glitches, the coding of the states should be done in gray-code.

3.4 System Simulation

Careful simulation of intended functionality of analog as well as digital circuit parts is mandatory. This section discusses the performed simulations and simulation results. The main issues for determination of the circuit components, simulation models and general considerations about the realistic simulation are presented. The final subsections show and discuss the simulation results of the time domain behavior and power efficiency for typical operation conditions.

3.4.1 Simulation Models

As mentioned in section 1.5, the PSpice derivative LTSpice tool from Linear Technology is used for simulation. The description of the used simulation models is the major topic of this section. Simple models of logic gates are available as almost ideal components without supply voltage or input current. Specific parameters such as delay time, output resistance and voltage levels can be configured. The implementation of the digital design includes state machine and input/output control circuit and is simulated with these idealized component models, but with a delay time of 1 ns each. The MOS transistor drivers are simulated with realistic output resistance and voltage levels according to the parameters of the Field Programmable Gate Array (FPGA) that is targeted as measurement platform. The comparators are replaced step by step from ideal components to almost real simulation models. In the simulation as well as in the prototype, the MAX975 from Maxim is used [28]. The comparator is configured to operate in high speed mode. Switching the speed modes is not reasonable because of the large delay times. These times are

significantly longer than for ASICs because of the buffer amplifier for off-chip loads. Because of the straight timing guidelines, the power saving modes are not implemented for the discrete setup. The MAX975 is used for every comparator in the circuit because of its excellent tradeoff between propagation delay and supply current. The P-channel switching transistor is CPH331 from Sanyo. It has a gate charge of 1.25 nC and an on-resistance of 0.4 Ω. The N-Channel FET FDV305N from Fairchild has a gate charge of 0.75 nC and an on-resistance of 0.15 Ω. The simulation models of the switching transistors have been adapted as good as possible to these transistors used for the prototype setup. The most critical part, the operational amplifier for current signal gain is chosen with the help of an available simulation model on the one hand and the availability from a distributor on the other hand. Although the design is not vulnerable to parameter variations of the components, the current amplifier is an important part with many competing component requirements. In simulation and for the prototype, the OPA LTC6247 from Linear Technology is used. The simulation model of the inductor includes beside the actual inductance also the equivalent series resistance. The frequency dependent sources of loss of the inductor are hard to determine especially because of the non-constant inductor current spectrum of up to some megahertz.

3.4.2 Startup Behavior

The support of multiple output voltage channels is one of the key features of the proposed voltage regulator. This section presents the simulation results of the regulator startup characteristic with for dual output voltage. This is illustrated in figure 3.17. The unusual high ripple voltage is a consequence of the low inductance and the very small blocking capacitors. These values are chosen for simulation only to show behavior more concisely. Much lower ripple voltage is intended for the prototype assembly. The timing diagram illustrates the priority management, continuous current operation mode during output channel switching, dependency of output voltage ripple during channel switching as well as the behavior of the regulator during normal operation for a dual output configuration at light loads. Between 30 and 40 µs, the high priority output rises to its nominal output voltage first. When the primary output voltage has reached its targeted level, the low priority output is served. Because of the priority management, the charging of the low priority output is interrupted as soon as the high priority output needs energy. This behavior is shown in the time interval from 40 to 47 µs. During this period, the ripple of output voltage 1 is significantly lower because of the constant minimum amount of transported charge from the regulator that is partitioned between the two outputs. At any time, both outputs request energy, and the energy packets are partitioned between the outputs. This results in a lower ripple voltage at both output voltages and is illustrated at the 52 µs time point. Otherwise, the two outputs are charged alternating and do not have interdependency.

Channel switching between the outputs can be performed at any trigger event of the control state machine so that at least one output needs to be charged (see also section 3.3.4). This behavior allows the regulator to comply with the priority setting at any time. The priority management consists of only a few logic gate stages that keep the circuit overhead low. The regulator can operate in continuous current mode even during output channel switching. This is

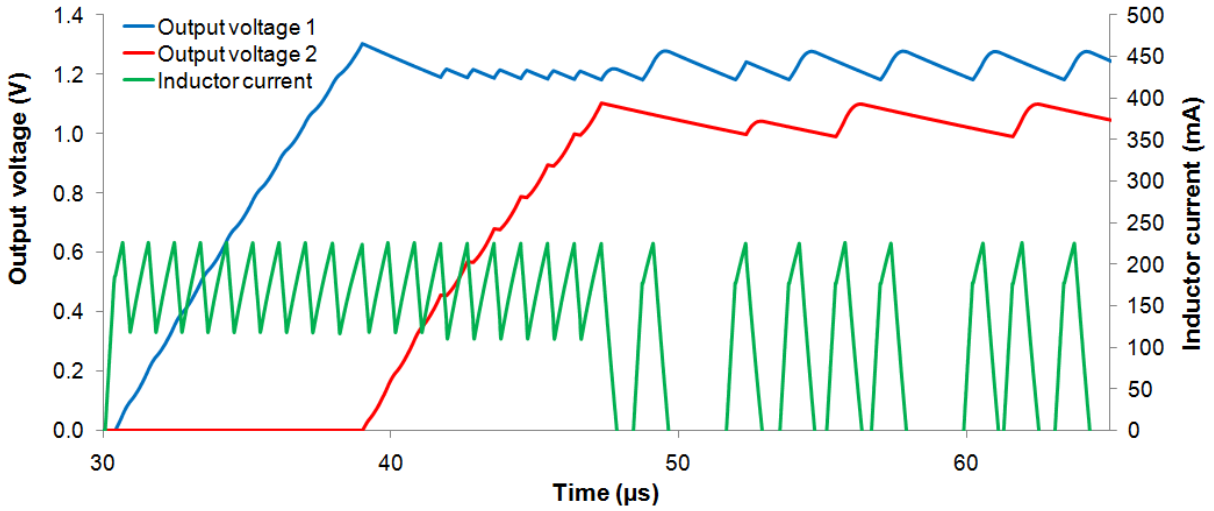


Figure 3.17: Output voltages in single input/multiple output configuration with $V_{refHigh} = 1.2\,V$ and $V_{refLow} = 1\,V$

a main condition for high switching speed and maximum efficiency gain in multiple input/multiple output (MIMO) mode.

3.4.3 Power Efficiency

Efficiency versus Output Current

Figure 3.18 illustrates the simulation results of the efficiency versus output current. The boarder conditions for this simulation are an input voltage of 3.1 V and an output voltage of 2.4 V. The DC/DC converter operates in step-down mode. The simulation curve for the pure power stage illustrates the efficiency of the converter when own consumption of the comparators and the amplifier is neglected. The efficiency characteristic is almost constant and does not depend from the output current. This result is extrapolated also down to micro ampere range, because the energy loss scales directly with the operating frequency and therefore, the efficiency remains constant for each energy pulse. In other words, each energy packet that is delivered from the input to the output causes a specific loss at the on-resistance of the transistors, at the inductor, and also the shunt resistor. A lower mean output current corresponds to less delivered energy packets. Because the leakage current of the transistors is low, the efficiency is constant. The second curve in figure 3.18 illustrates the overall efficiency that includes the quiescent current of the operational amplifier, the voltage comparators and current comparators. The efficiency decreases when the output current/the output power decreases. At low output current, the quiescent consumption of the analog components dominates the overall loss. Although the quiescent power of the simulated components is much higher than for low-power integrated version of the auxiliary components, this efficiency drop occurs at comparable large current values. The integrated version would consume much lower power, so the characteristic is similar for the low load condition, but only at much reduced load current. This leads to another benefit of the proposed design. In applications

with different voltage levels, the combined output power is higher than those of two separate converters with single output. This increased output power increases the overall efficiency of the multiple output voltage regulator as well. In other words, the multiple loads increase the utilization and thus the mean current, so the efficiency of the regulator is increased too.

For example, if a combination of a 1.2 V output @ 4 mA combined with a 2.4 V output @ 1 mA is used, the equivalent output current related to 2.4 V is 3 mA. In this case (compare with figure 3.18) the overall efficiency is increased from 15 % to 35 %. Please note that the power consumption of the simulated amplifier and comparators is huge compared to quiescent power of equivalent integrated components. Furthermore, no stand-by mode was simulated for the components and this increases the quiescent loss dramatically. The illustrated effect can be lowered by decreasing the quiescent loss but it can never be neglected completely. So, the multiple output concept is an improvement almost independent of the used regulator concept.

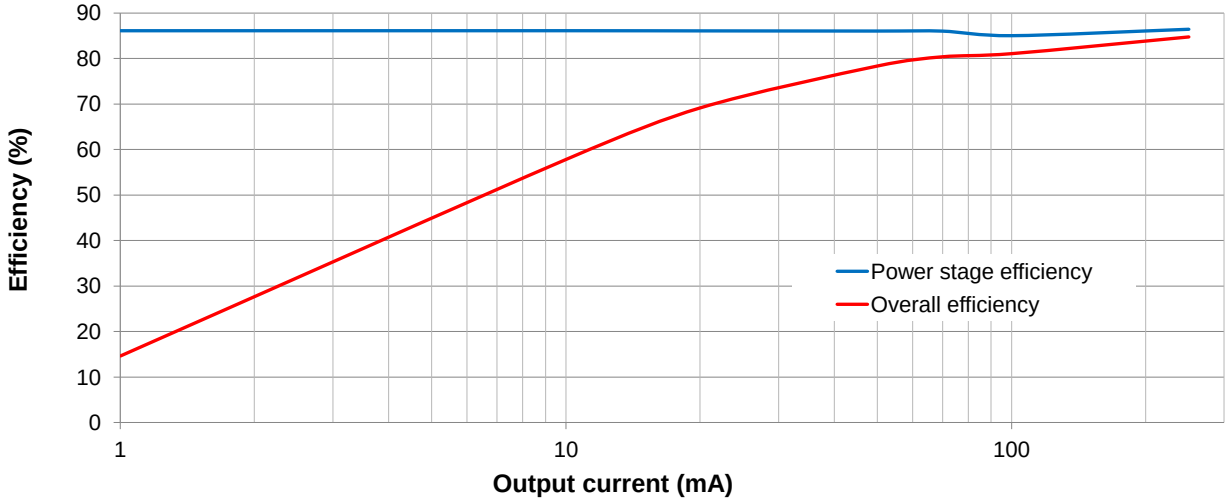


Figure 3.18: Simulation results of efficiency for power stage only and with inclusion of own-consumption of analog circuitry for control; $V_{in} = 3.1\,V$,$V_{out} = 2.4\,V$

Efficiency and Input Voltage

Figure 3.19 shows simulated regulator efficiencies and output voltage ripple depending on the input voltage. As boarder conditions for the simulation, an output voltage of 2.4 V and an output current of 45 mA are assumed. The figure shows the implementation of two slightly different state machine versions. The graphs of the initial state machine illustrates the implementation of the initial design of the regulator (compare to section 3.3.3 and figure 3.11). The transition from step-up to step-down mode is provided for different input voltage. The step in the efficiency indicates the mode switching. To increase the efficiency, especially in step-up mode, different implementations have been tested. The graphs of the updated state machine in figure 3.19 offers an increased efficiency over the whole input voltage range. This implementation differs from the initial one in only two transitions.

1. In buck mode, transition from state 1 to state 2: $I_{LL} \wedge \overline{boost}$ instead of $I_L \wedge \overline{boost}$, so the transition from state 1 to state 2 is performed earlier.

2. In boost mode, transition from state 2 to state 3: $\overline{Um} \wedge boost \wedge \overline{I_L}$ means that the regulator remains longer in state 2 before it changes to state 3.

Although the efficiency is increased by design, is not practical for every application because of the huge ripple voltage of more than 25 % (for these unusual small blocking capacitors). By using different transition conditions, multiple implementations can be implemented that have an efficiency and a ripple voltage between these two implementations from figure 3.19. Furthermore, via usage of a much larger output blocking capacitor, the ripple voltage is reduced significantly. A further reduction of the output ripple combined with an increased efficiency can be achieved when the amount of transported energy per single energy packet is reduced or finally via connection of a LDO after the switching regulator. So a sufficient tradeoff between efficiency and ripple voltage can be found for most applications. Another advantage of this approach is that the changes only affect small digital control parts of the regulator. So basically even a design with configurable efficiency versus ripple voltage is possible.

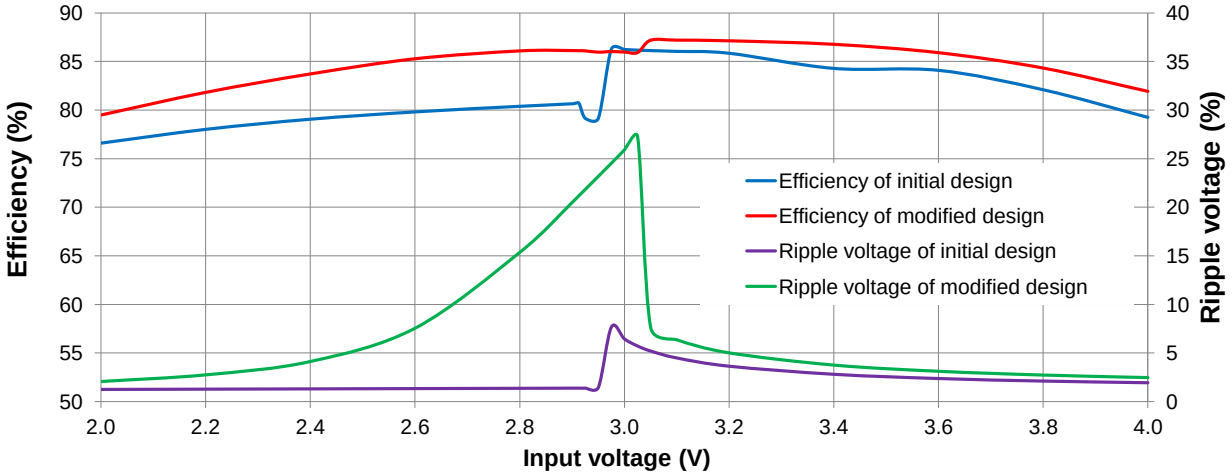


Figure 3.19: Simulation results for efficiency and ripple voltage of different state machine implementations. $V_{out} = 2.4\,V$, $I_{out} = 45\,mA$

4 Implementation

The main topic of this chapter is the physical implementation of the discrete prototype assembly of the proposed power converter for wireless sensor networks. First, the digital development platform is introduced and the setup of the prototype for the complete supply unit is presented. Section 4.2 deals with the implemented functionality of the prototype assembly and includes PCB design issues, and section 4.3 presents the implementation of the digital design for the PFGA platform using a hardware description language. At the end of this chapter, the deviations of the final prototype from the initial design, as well as function tests are discussed.

4.1 Development Platform

Goal of the CHOSeN (Cooperative Hybrid Objects Sensor Network) research project is the development of smart sensor network applications for automotive and aeronautic domain. In the course of the project, several different hardware and software components are designed and developed. The hardware includes an application processor module (µC), a RF transmitter module, a RF receiver module, a wake-up receiver module and the power management module that is topic of this thesis. For development purposes, a development board was designed to carry the mentioned hardware modules. Figure 4.1 illustrates a photograph of the development board and its main components. Beside the connectors for the modules, the development board contains a FPGA core module, power supply, USB interface, LEDs, buttons, switches, further external connectors and a JTAG interface for programming. The FPGA module is the central part of the board. Direct connections between the plug-in modules are possible via the FPGA. The development board provides a 3.3V supply voltage to the modules. [29]

The utilized FPGA is a Xilinx Spartan 3 device that is clocked with a 25 MHz oscillator. The implementation of the proposed converter's digital design is intended within the FPGA and the used hardware description language is Very High Speed Integrated Circuit Hardware Description Language (VHDL). Although the propagation delay of the FPGA gates is worse than those of an Application Specific Integrated Circuit (ASIC), the implementation works sufficient accurate. Analog and passive parts of the design such as switching transistors, inductor, amplifier and comparators are mounted on an external Printed Circuit Board PCB) that is connected to the

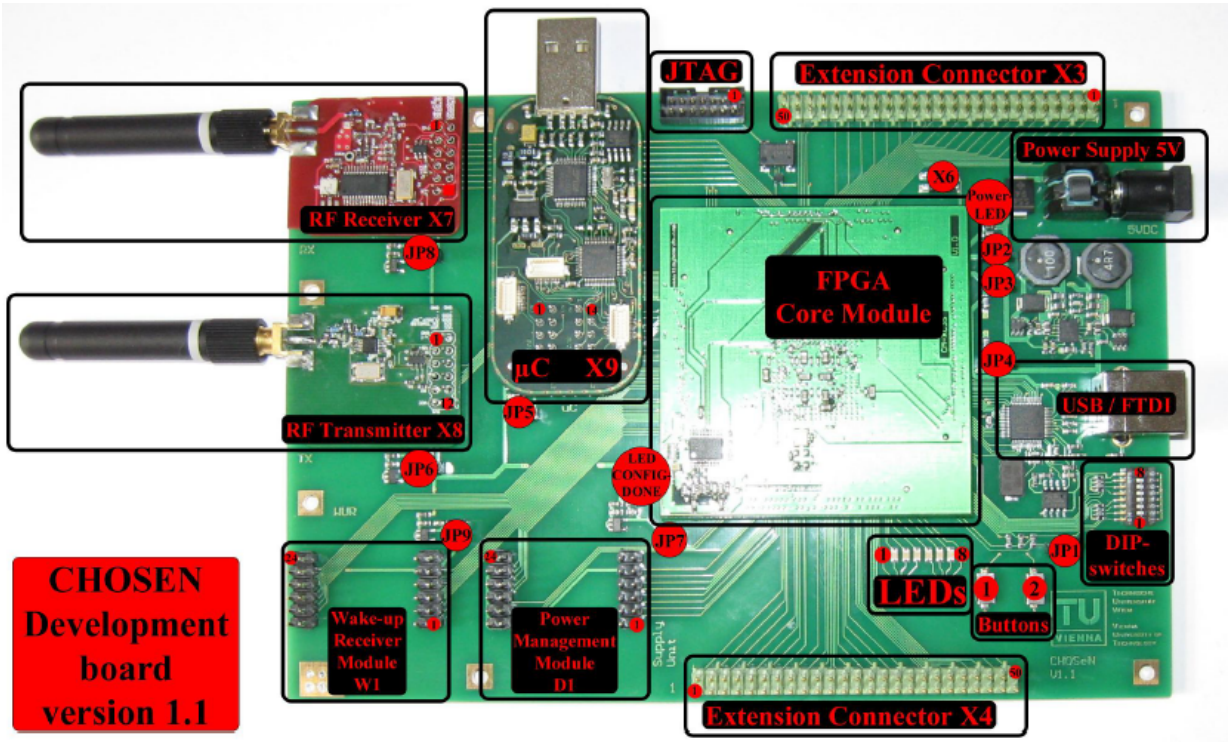


Figure 4.1: Development board of the CHOSeN research project [29]

development board using extension connectors. The functionality of the prototype is validated with the help of discrete components, while the behavior of a full integrated solution is determined using simulation results, performance data of scientific literature and experience gained from the discrete setup.

Interfaces

Although there is a set of connectors defined for the power supply plug-in unit from figure 4.1, an additional set of connectors is used for the implemented prototype. Because of the high amount of needed connections to the FPGA, two connector blocks are insufficient. Because of the insufficient pin count and the physical dimensions of the prototype, the two connectors for the wake-up receiver module and one connector of the power management module are used.

They contain single ended digital inputs and outputs as well as the +3.3 V board supply voltage and the ground connections to the development board. According to the assigned pin numbers in figure 4.2, table 4.1 lists the pinning of the actual analog connections for the designed DC/DC converter.

4.2 Hardware Design

In this section, the used hardware components for the discrete converter prototype are discussed. Furthermore, basic information about the PCB design and the used analog components is given.

Table 4.1: Pin number, pin name and description of analog voltage inputs and outputs of the prototype

Pin Number	Pin Name	Description
1	GND	Ground
2	V_{OUT1}	High priority output voltage
3	V_{OUT2}	Low priority output voltage
4	V_{-}	Negative supply voltage for the current amplifier
5	V_{IN2}	Low priority input voltage
6	V_{IN1}	High priority input voltage
7	GND	Ground

Discrete Prototype

The hardware implementation of the designed prototype provides the possibility to operate the DC/DC converter in step-up or step-down mode. Two independent output voltages as well as two independent input source voltages are supported by the prototype hardware. This design requires the implementation of six independent switching transistors. Further configuration signals that are connected directly to the FPGA are chip select, enable signals for both outputs as well as an accu-mode selector option that is described in detail later in section 4.3. The digital design is implemented on the FPGA using VHDL entry. The complete schematic of the designed PCB is shown in figure 1 in the appendix. Reference voltages for the input and output comparators are generated on board via a voltage divider, but can alternatively be injected from an external source. All input voltages, except the +3.3 V supply for the amplifier and comparators have to be applied externally. On-board load circuits are available for each output, but can also be disconnected if off-board loads are used. Generation of the switch control signals is done directly by the digital outputs of the FPGA module without additional driver circuit on the PCB. The range for possible input and output voltages of the prototype converter are limited by the driver output voltage range. The high level voltage is limited to 3.3 V and directly drives the gates of the P-channel transistors. If the output voltage would exceed 3.3 V significantly, the P-channel FETs cannot be turned off completely, so the maximum output voltage then becomes around 3.3 V. On the other hand, a low level of the driver output has to turn on the PMOS transistor fully, so also if a device with low threshold voltage is used, the lower boundary of the converter output voltage is some 1.8 V. Further reduction of the output voltage would firstly decrease efficiency due to high static power loss, and later influence operability of the converter.

PCB

Figure 4.2 illustrates a photograph of the regulator prototype PCB. The main parts of the implementation are labeled. In this section, the practical circuit design and auxiliary components that are necessary for proper operation of the proposed prototype are discussed.

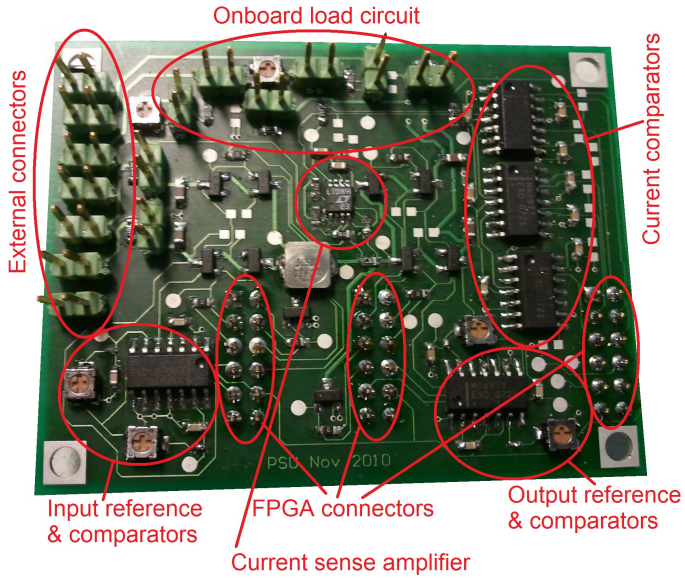


Figure 4.2: Implemented voltage regulator prototype with two independent inputs and two outputs: The main components are labeled

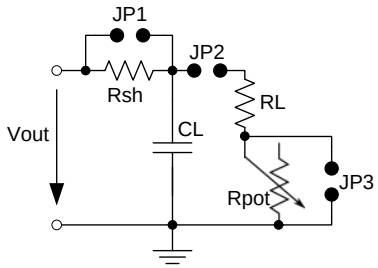


Figure 4.3: Implemented on-board load circuit for easy measurements

On-board Load Circuit

In order to integrate a practical test environment, load circuits for each output are included on the PCB. Figure 4.3 shows the schematic of the on-board load. R_{sh} is a $0.1\,\Omega$ shunt resistor that is connected in parallel to the jumper pins of JP1 to allow output current measurements. Using jumper JP2, the on-board load can be enabled or disabled. It consists of a low value resistor in series to a potentiometer. This way, various loads can be emulated. Via shortening the potentiometer with jumper JP3, load steps can be generated. The output is also connected to an external connector to supply off-board loads. The load capacitor CL is equipped optionally to model capacitive load impedance.

Reference Voltage Generation

The proposed voltage regulator is designed to use one voltage monitor comparator for each input and output pin. The output comparator is needed to check if the output requires energy. At

the input, the comparator is needed to determine if the input voltage is available. To reduce the amount of external connectors, a separate on-board reference generation circuit for each in- and output is added. The circuit contains a potentiometer, soldering bridge and a test pad. When the soldering bridge is closed, the reference voltage is defined via the potentiometer, and the actual value can be measured at the test pad. When the soldering bridge is opened, an external reference voltage may be injected via the pad. The actual value is compared with the desired output value without a voltage divider. So, if an output voltage of 2 V is desired a 2 V signal has to be applied for reference.

Switching Transistor Bypass

In contrast to common switching voltage regulators, the proposed design uses two series connected input and output transistors in the discrete assembly. Optionally, one of these transistors can be bridged via additional pads. So, the design can be changed to a single IO system that uses only a single transistor at the input and output. This increases debugging capabilities and power efficiency.

Test Pads

Additional test pads are inserted onto the PCB at several important locations for efficient debugging and measurement gathering. Test pads are added at the supply voltage, each transistor gate, at the shunt resistor and the current amplifier output. A test pad consists of a small SMD pad without soldering stop. So a probe can be connected easily.

Current Sense Amplifier

The operational amplifier for the current measurement is one of the main and most critical components of the implementation. The amplifier has to provide the following characteristics:

- Low power consumption for high efficiency
- High bandwidth for amplification of the high frequency current spectrum as well as high common mode rejection ratio to handle large common mode steps at the inputs properly
- High speed and high slew rate for a small propagation delay
- Rail to rail operation for efficient usage of the full supply voltage range.

In the implemented design, the operational amplifier LTC 6247[1] from Linear Technology is used. This device provides all needed functionality and furthermore, the available simulation model supports efficient development and low deviation of simulation from prototype characteristic.

[1] `http://www.linear.com/`

Comparators

The comparators for the prototype have to provide high speed and a combination of low delay and low rise time. This is needed to minimize the overall delay from current threshold crossing and initiation of a reaction within the digital part. Furthermore, low power consumption is needed to achieve high power efficiency. On the prototype PCB, mainly two different types of comparators are used. The current threshold comparators and the reference voltage comparators for input and output voltages. Although the speed requirements are much lower for the voltage comparators, equal devices are used for both tasks for simplicity. The used comparator is the MAX 977[2] from Maxim. Compared to other comparators, it provides the best ratio of current consumption to delay time.

Switching Transistors

The most important characteristics of the switching transistors are a low static on-resistance, low gate charge, switching times, maximal drain-source voltage and drain current. The optimal operating point for the switching transistors is when the static loss due to the on-resistance ($P_R = I_D^2 \cdot R_{DSON}$) is equal to the dynamic loss that is caused by the gate charge of the transistor at switching events ($P_S = V_G \cdot Q_G \cdot f_{sw}$ where f_{sw} is the switching frequency). To find the optimal transistors for the prototype, various switching transistors have been tested in the prototype and in simulation. One major challenge for transistor selection is that a transistor with a low gate charge for fast switching has a large on-resistance. This positive impact on the regulator functionality results in a negative impact on the power efficiency. Transistors with a low resistance have larger transition times and that increases voltage overshoot at the transistors. Especially at the shunt resistor for current measurement, this behavior results in measurement errors that disturb the regulator functionality. Figure 4.4 illustrates timing diagrams for such a characteristic. The blue line is the common mode voltage at the shunt resistor terminals. The steps from inductor switching cause overshoot and undershoot at the output of the high-bandwidth current measurement amplifier (green line). The higher the over- and undershoot, the larger are the current measurement errors. A wrong output value of the amplifier may result in a wrong behavior of the regulator for excessive impact. Especially the buck-boost switching concept is vulnerable to this type of error, because it checks the inductor current for unexpected current slopes.

Because the shunt resistor is connected in series to the inductor and is located at the output side of the regulator, the power transistors at the output have to provide fast switching speed to minimize these errors. At the regulator input, larger transistors with longer switching times and lower on-resistance can be used without significant impact to the regulator's operating reliability. This has been determined in an iterative design process via comparison of refined simulation results and prototype measurements.

[2] `http://www.maxim-ic.com/`

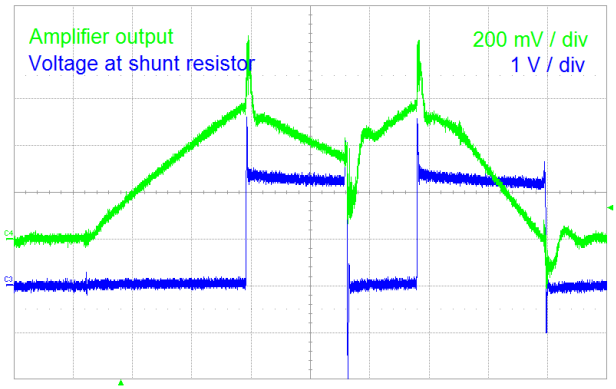


Figure 4.4: Impact of the shunt resistor's common mode voltage over- and undershoot to the current sense amplifier output

4.3 FPGA Design

The digital design for control of the power supply unit is implemented within a FPGA via VHDL entry. Figure 4.5 illustrates the block diagram of the implemented digital design. The implementation is separated into different functional parts that are described in this section. Due to proper partitioning, the design complexity is limited and open to enhance its capabilities with low effort. Main parts of the digital implementation are the state machine, the input and output channel switching blocks and the enable logic.

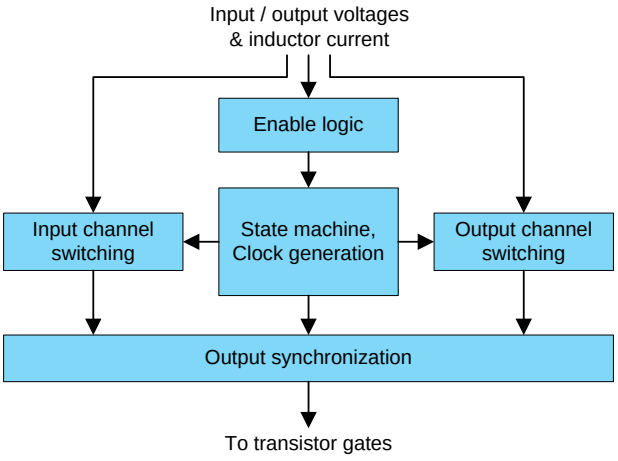


Figure 4.5: Block diagram of digital implementation in VHDL

FPGA I/O Drivers

Xinlinx Spartan 3 provides several properties to configure the input and output drivers of the FPGA. The IO-Standard defines the used voltage levels for a bank of IOs. For the actual implementation, the default value (low power CMOS 3.3 V) is used. The switching transistors are connected directly to the FPGA outputs without additional MOS transistor drivers. This default configuration limits the maximum output current - the drive strength - of each output to 12 mA.

To further reduce switching time of the transistors, an alternate value raises the limit to 24mA for each driver that is connected to a transistor gate. Furthermore, the slew rate of the output pins can be selected. The standard value is 'SLOW', but to reduce switching time further, the value is set to 'FAST' for each pin that drives a switching transistor. Signal delay can be used for shoot through protection, but the programmable delay constraints are in pico seconds range and therefore not suitable [30]. For this purpose, delay times of nanoseconds are required.

State Machine

The state machine has been implemented using the VHDL state machine design pattern. As designed, the state machine operates with a single converter input channel and a single output channel. Clock signal generation is also integrated into the state machine and works via a state comparison scheme that generates a clock event when the next state is evaluated (see section 3.3.3).

Enable Logic

Task of the enable logic block is proper control of the state machine's and the voltage regulator's operating mode. It can activate the converter or put it to idle mode. Depending on the states of the input and output voltage monitors and configuration signals, this logic block evaluates the enable signal for the state machine. Beside the enable signals for the multiple outputs, also the accu-mode signal and the chip select signal are processed. The accu-mode supports a secondary battery for energy buffering. It must be connected to the secondary output channel for charging and also to the secondary input channel for discharge, if the primary energy source does not deliver sufficient power. When accu-mode is enabled, the constellation of charging the secondary output via the secondary input make no sense and hence, is avoided and the regulator is not enabled in this case.

Input / Output Channel Switching

The input and output channel switching logic is implemented as combinatoric logic. Beside the virtual switching signals from the state machine, also the priority management and the shoot through protection schematic is handled by this logic block.

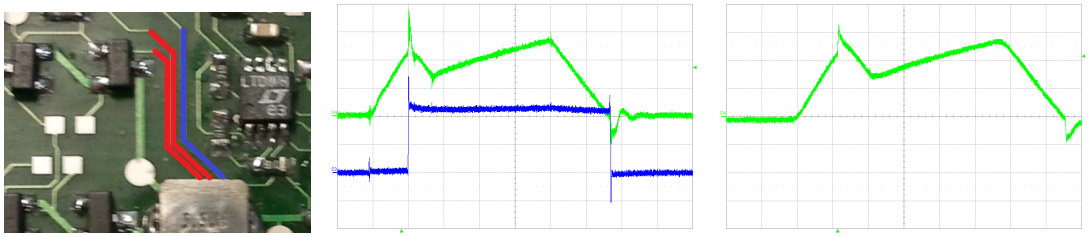
4.4 Difficulties

As expected, physical implementation of the previously simulated design brings deviation from simulation results and additional noise because of the high frequency spectrum of voltage and current signals. So this section addresses difficulties and problems that had to be solved during circuit development and testing. Layout impact and other non-modeled effects necessitate adaption of the initial analog and digital implementation to improve regulator reliability and power efficiency.

Common mode error of the current amplifier

The current amplifier is a key component for proper function of the implementation. The output voltage of the current amplifier has direct impact to the behavior of the digital implementation. Errors at the output of the operational amplifier (OPA) can result in a wrong behavior of the whole control circuit. The main causal problems according to the OPA errors has been injection of high frequency noise, and the high frequency ringing and the high magnitude of the shunt resistor's common mode voltage at a comparably low desired differential voltage.

High frequency signal injection occurred because the high frequency switching signal and feedback signal of an input switch (see red lines in figure 4.6 (a)) run in parallel to the negative supply voltage of the amplifier (blue line in figure 4.6 (a)). The switching signal contains very high frequency components because of the short transition times of the switching signal for the transistors. The impact of these disturbances has been reduced via connection of an additional filter capacitor to the negative OPA supply. The error that comes from the operational amplifier and is caused by the common mode voltage steps at the inputs, cannot be compensated completely via external components. Figure 4.6 (b) illustrates the voltage at one amplifier input and the corresponding output voltage of the OPA. A common mode step in the input voltage causes an unwanted peak at the amplifier output. An additional problem visible in figure 4.6 (b) is that the common mode step in combination with very short over- and undershoot of the input signal beyond the supply voltages (3.3 V/-1 V) of the OPA boosts this amplifier error even more. Via connection of a ferrite bead in series to each input of the amplifier, the over- and undershoot is reduced and the slope of the common mode step is decreased. Figure 4.6(c) illustrates the amplifier output after this procedure. The amplitude of the amplifier error is reduced significantly.



(a) Capacitive disturbance injection (red) into supply voltage (blue)

(b) Initial impact of a common mode steps (blue) to the current amplifier output

(c) Reduced impact of common mode step

Figure 4.6: Causation, impact and performance of advanced design for practical current sense amplifier error

Track Inductance

In high frequency circuits, the track length on the PCB represent distributed parasitic capacitors and inductors. In general, any track should be kept as short as possible. The introduced prototype has a comparably long track from the shunt resistor to the N-channel FET that connects the shunt resistor to ground potential. This is shown as red marked track in figure 4.7. In combination

with the capacitance of the track, the test pads, and the P-channel FETs, a parasitic LC tank is built. This forces ringing effects, pushes additional disturbance onto the shunt resistor's voltage potential, as well as into the amplifier input. So the initial design was not operable. To damp these oscillations, a ferrite bead was inserted into this trace.

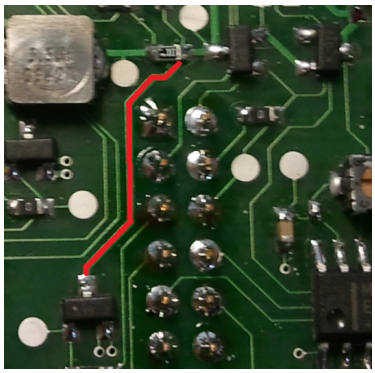
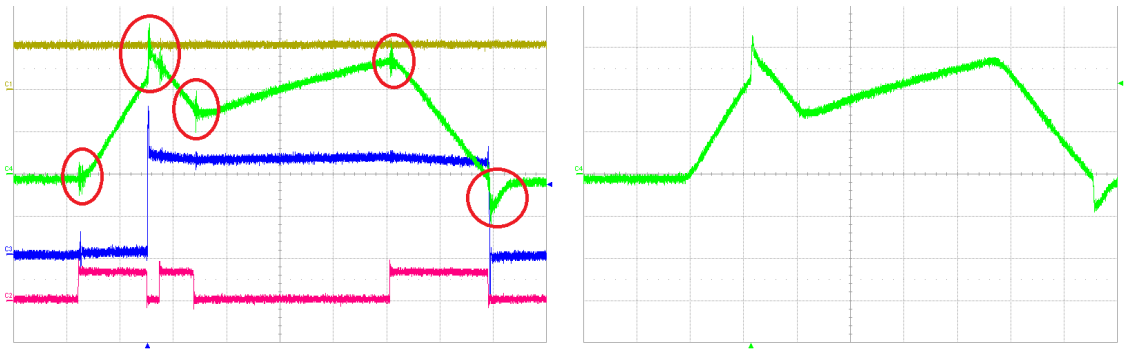


Figure 4.7: PCB trace with disturbing parasitic inductance

Oscilloscope Effects

Because of the finite input impedance and the input capacitance of the oscilloscope probe, the measurement method has an impact to the measured voltage value especially at high frequencies. Furthermore, measurements of different channels on the oscilloscope lead to crosstalk. Figure 4.8 (a) illustrates the measurement of the analog amplifier output in combination with measurements on all three other channels. Figure 4.8 (b) shows the same measurement when all other channels are disconnected. The main differences are clearly visible and marked in sub figure (a). The reason for that is crosstalk between the oscilloscope channels and can lead to misinterpretation of the gathered results.



(a) Measurement of multiple channels

(b) Measurement of single channel

Figure 4.8: Crosstalk between oscilloscope channels

5 Measurement Results and Comparison

Measurement results of the implemented prototype as well as the comparison to simulation results and state-of-the-art voltage regulators are topic of this chapter. In section 5.1, an overview over the used test setup is given and the main sources of regulator loss are discussed. Section 5.2 discusses measurement results of the prototype under certain load conditions. Topic of section 5.3 is the comparison of the measurement results to the simulation and to state-of-the-art products and research prototypes. At the end of this chapter, efficiency estimations for an equivalent integrated solution of the implemented design are presented.

5.1 Test Setup

As mentioned in section 4.2, the analog components such as amplifier and comparators are implemented as discrete components. Discrete components have inferior performance in terms of propagation delay, cutoff frequency and power consumption, when compared to integrated components. Furthermore, the power consumption of the digital logic implemented in the FPGA, is magnitudes higher than for an ASIC version. In order to get a closer relation to the integrated solution, the values for the power consumptions of

- Digital implementation (static and dynamic loss)
- Operational amplifier
- Current and voltage comparators
- Gate drivers

are calculated or simulated, and combined with the prototype measurement results. Characterization of the prototype is performed via measuring the input and output voltage as well as the input and output currents. The measurement includes loss of the switching transistor's on-resistance, the inductor, leakage current, the shunt resistor loss as well as the loss caused by auxiliary components for the current sense amplifier.

Power consumption of the operational amplifier and the current comparators are determined by comparing state-of-the-art integrated components with similar performance such as the discrete components, that are used within the prototype. In [ZL07], a low-power, high-speed operational amplifier with a unity-gain bandwidth of 160 MHz and a power consumption of 587 µW is introduced. A low power asynchronous comparator is introduced in [LP00], which provides an overall delay of 19 ns while consuming 161 µW. This comparator has even a better performance than the comparators used for the prototype. For the voltage comparators, a comparator delay of 19 ns is not necessary. [LP00] further introduces a formula to calculate the power consumption with respect to propagation delay. Power consumption is halved when the propagation delay is doubled. So the value of the power consumption of the voltage comparators can be scaled via $P_{VCMP} = 161\,\mu W/6 = 26.8\,\mu W$, which results in a latency time of 114 ns. Considering very light loads (several micro watt), the loss of four voltage comparators with 26 uW each, would dominate the overall regulator loss. Because of the special requirements to these voltage comparators, an ultra-low-power comparator is designed and simulated in 120nm CMOS technology. It is optimized for the needed requirements.

The simulated voltage comparator is illustrated in figure 5.1. It is implemented as a two stage amplifier with differential input stage (M1, M2) and active load (M3, M4). Transistor M5 is included to limit the maximum voltage at the gate of M6 which decreases switching time from low to high at the output. The output stage is powered using a cascode current mirror (M7, M8) to reduce power consumption. The characteristics of the designed comparator are

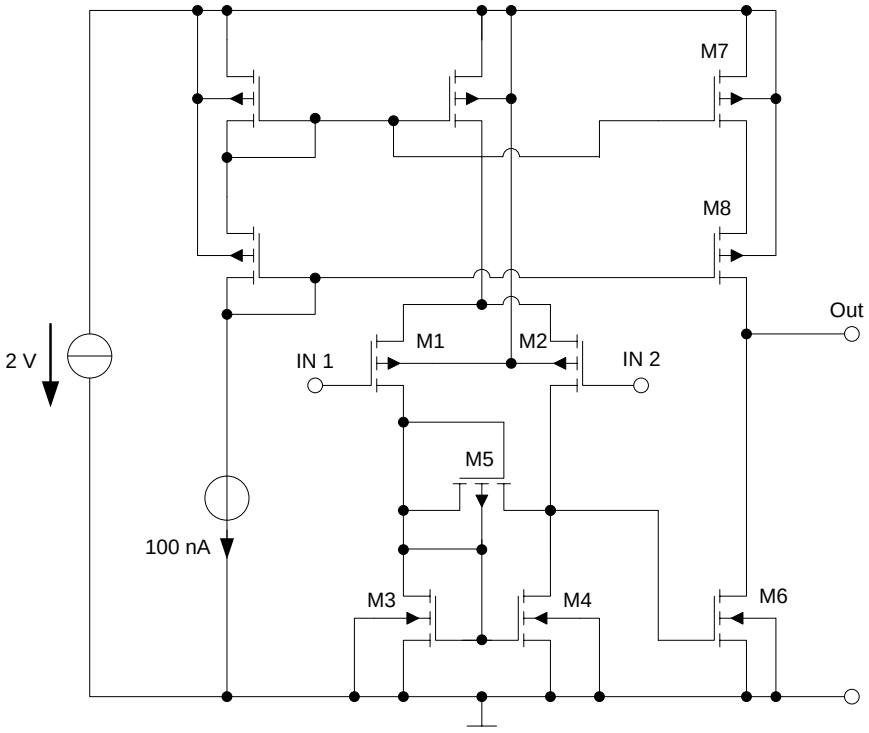


Figure 5.1: Designed and simulated ultra low power comparator for input and output voltage monitoring

- Supply voltage = 2 V
- Current consumption of 150 nA for each comparator + 100 nA for the current reference
- Delay time = 120 ns.

Effects of layout are already considered in these results.

To further decrease idle-loss, the current amplifier and current comparators can be set to a power saving mode by switching the bias currents off. Enabling and disabling is provided by the digital control. In this case, the loss is reduced to the leakage currents of values between 1 and 10 nA.

Static loss of the digital implementation is calculated using [HN97], where the leakage current of a logic gate at different input patterns is listed. The calculated average value is about 100 fW per gate. Multiplied by the estimated number of gates of the proposed design, a power consumption of less than 6 nW is estimated. The presented design includes an event triggered digital control state machine that performs state transitions without an extra clock signal. Considering this and the loss calculation introduced in [MNB01], a flip-flop with clock gating consumes 52 fJ per clock cycle in average. Multiplied with the number of flip-flops in the design and the switching frequency, the dynamic loss of the digital implementation is estimated. Loss that is caused due to the gate charge of the power transistors is calculated via $Q = I \cdot \frac{1}{f} \Rightarrow P_l = Q_G \cdot f \cdot V$ where Q_G is the gate charge of the transistor, f the mean switching frequency and V the maximum gate voltage.

5.2 Measurement Results

As mentioned in section 5.1, the measurement results are combined with estimated values of state-of-the-art products and with calculated values that can not be measured directly. The following figures illustrate efficiency measurements of the introduced voltage regulator versus output current and versus input voltage.

Figure 5.2 illustrates the regulator efficiency versus output current. The input voltage is 3 V and the output voltage is 2.4 V. The figure consists of two diagrams. Diagram "Power stage efficiency" illustrates the measured efficiency and includes static transistor loss, loss of shunt resistor, inductor and leakage loss). The efficiency is almost constant over a wide load range because of the PFM operation and the constant efficiency of each delivered energy packet within a single switching cycle. The static leakage loss is nearly negligible. Diagram "Overall efficiency" additionally includes the calculated loss of the comparators, the current sense amplifier, gate-charge and the digital circuitry. As illustrated, the efficiency decreases with decreasing output current. This is because the desired output power decreases, but the idle loss of the comparators and amplifier remains constant and dominate the overall regulator loss. The higher the quiescent currents of the components, the more rapid the efficiency decreases at low output currents. The loss that is caused by the voltage comparators at each input and output channel of the regulator has the biggest impact to the overall efficiency during low load condition because they have to

operate in an always-on mode to recognize a threshold crossing of the input and output voltages immediately. The maximum efficiency or peak efficiency is limited by the on-resistance values of the transistors and the current values through the transistors.

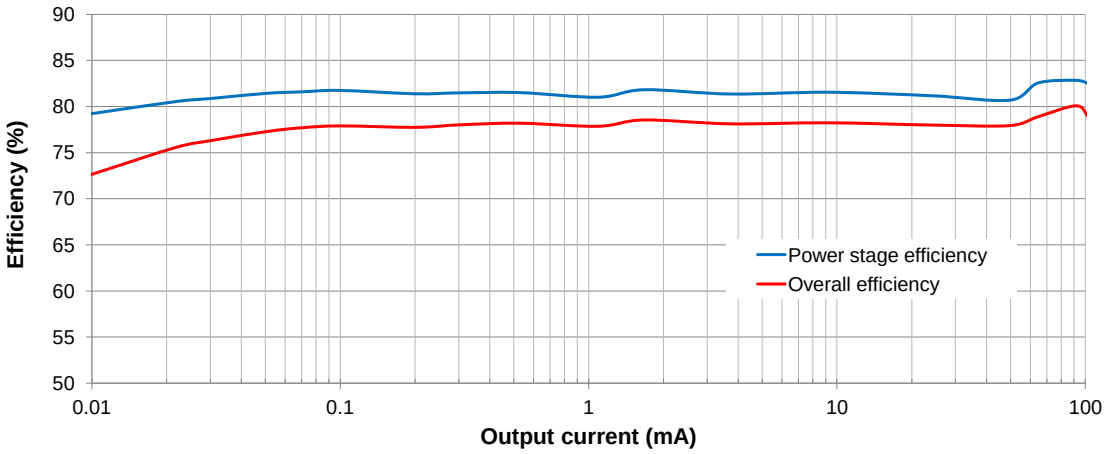


Figure 5.2: Measured prototype efficiency of power stage only and with inclusion of estimated analog component loss versus output current ($V_{in} = 3.1\,V$, $V_{out} = 2.4\,V$)

Figure 5.3 illustrates regulator efficiency versus input voltage at an output voltage of 2.4 V and an output current of 45 mA. Similar to figure 5.2, this figure contains two graphs. "Power stage efficiency" illustrates the efficiency when only loss of transistor, shunt resistor, inductor, and leakage loss are considered. "Overall efficiency" additionally includes loss of the amplifier, the comparators and the digital implementation. The two graphs are almost identical because of the relatively high output power. In this case, the amplifier and the comparator loss do not have a big impact to the overall efficiency. Furthermore, the voltage range where the transitions from step-down to step-up mode occur (green line) and from step-up to step-down mode (red line) are performed, are illustrated. The graph shows that there is a hysteresis between the buck-boost transitions. The benefits of this behavior are that fast toggling between the modes is avoided and the regulator automatically operates in a defined operation mode without the need of a complex operating mode-selection circuit. The efficiency drop-off at high input voltages (3.8 V and above) is caused by the maximum gate voltage of the P-Channel FETs that is limited to 3.3 V only by this implementation. At high input voltages the P-Channel FETs cannot be switched off completely, which drastically increases leakage current and decreases efficiency, cut there is principally no limitation of this DC/DC conversion concept. The drop-off at around 3.05 V appears close to the switching threshold from step-up to step-down mode and is caused by the small slope of the the inductor current. This effect is gained at the high current values - caused by the high threshold values - which are needed to provide an accurate current measurement.

As discussed in section 3.3.4, the multiple output channel concept has a positive impact to the overall efficiency of the voltage regulator. Figure 5.4 illustrates an efficiency comparison of a single and dual output regulator at low output currents. The sections of the diagram show the behavior when

- Both outputs operate in step-down mode

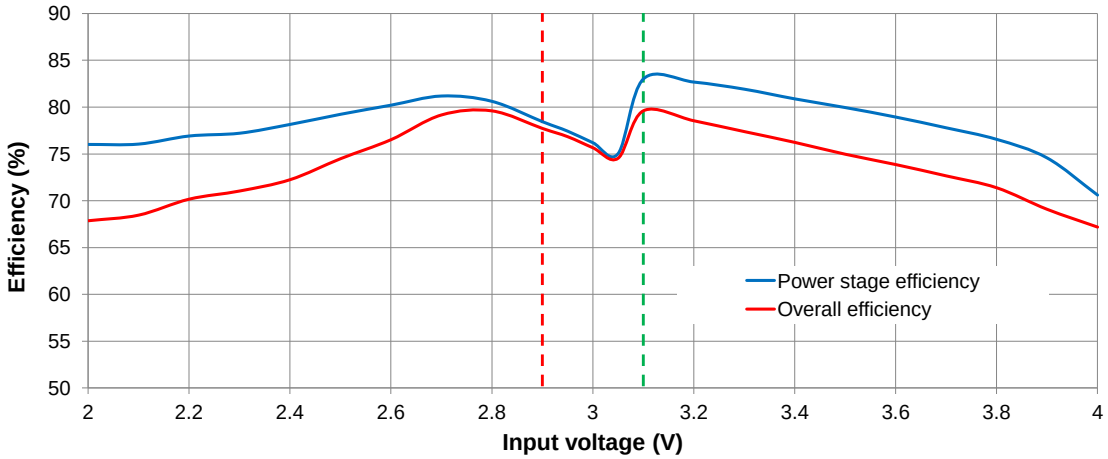


Figure 5.3: Prototype efficiency of power stage only and with inclusion of analog component loss versus input voltage ($V_{out} = 2.4\,V$, $I_{out} = 45\,mA$)

- One output operates in step-down and one in step-up mode
- Both outputs operate in step-up mode.

The different bars illustrate the efficiency of the single high priority output (Out 1), the single low priority output (Out 2), the mean efficiency of the two single output cases and the efficiency when using dual output operation under equal conditions.

The edge conditions of the measurement are

- Buck-Buck: $V_{in} = 3.2\,V; V_{Out1} = 2.4\,V; V_{Out2} = 2\,V; I_{Out1} = I_{Out2} = 100\,\mu A$
- Buck-Boost: $V_{in} = 2\,V; V_{Out1} = 2.5\,V; V_{Out2} = 1\,V; I_{Out1} = I_{Out2} = 100\,\mu A$
- Boost-Boost: $V_{in} = 2\,V; V_{Out1} = 2.5\,V; V_{Out2} = 2.2\,V; I_{Out1} = I_{Out2} = 100\,\mu A$

As shown in figure 5.4 , the combined efficiency is higher when compared to the case of single output regulators. In dual output operation, the regulator works at a higher overall output power which decreases idle time. The difference between the 'Average' and the 'Dual Output' value depends on the idle loss of the used components. The lower the idle loss, the smaller is the difference between the values. In the case of ideal components (idle loss = 0) the two bars would have an equal value, but in praxis, this idle loss is the main efficiency limiting factor at light load condition.

As shown in diagram Buck-Boost, the regulator operates with one output in step-up and one output in step-down mode simultaneously. The proposed design allows a complete automatic and dynamic mode selection. This means that no output is fixed to an operation mode nor has to be configured.

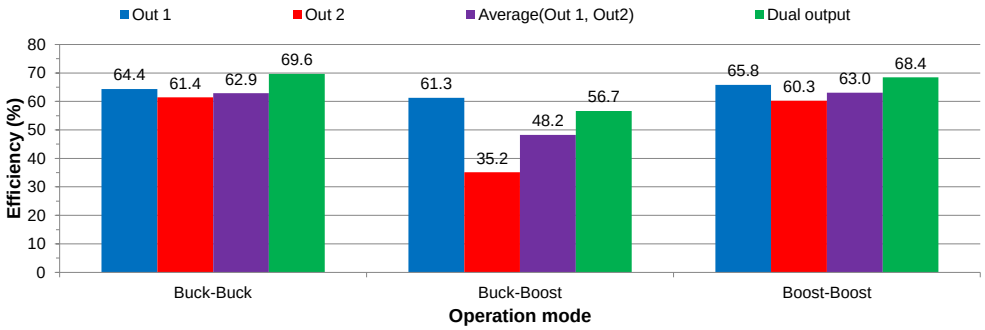


Figure 5.4: Efficiency comparison of regulators with two single outputs and with dual outputs in buck-boost mode combinations

5.3 Comparison

Figure 5.5 illustrates power efficiency versus input voltage diagram and compares simulation and measurement results. This figure includes graphs of figure 3.19 and 5.3. As shown, the state machine implementation can have significant impact to regulator efficiency and ripple voltage. Graph 2 and 3 illustrate simulation results with different state machine implementations. Diagram 1 presents measurement results of a different implementation of the state machine with a power efficiency/ripple voltage among the simulated ones. The diagrams are comparable, with the difference that the efficiency of the measured curve is about 5 % below the simulated one. Deviations in the magnitude are caused by

- Tolerances/deviations from simulation models of transistors, shunt resistor and inductor
- More simple capabilities to adjust zero-current and shoot through protection in the simulation
- Applied ferrites to improve prototype functionality
- Non-modeled parasitic PCB effects such as wiring resistance, capacitance, and inductance

The efficiency dent in the buck-boost transition region is caused by the higher inductor current in boost mode and the increased active time when the input voltage is nearly equal to the output voltage. The loss is proportional to the square of the load current and dominates at the high current range.

Figure 5.6 is a combination of the graphs from figure 3.18 and 5.2. Similar to the comparison illustrated in figure 5.5, the deviation of the simulated and measured power stage efficiency is about 5 % and remains constant over the full range of the output current (graph 1a and 2a). Graph 1b also includes the simulated loss of the auxiliary components from the discrete prototype setup, while in graph 2b, the loss of an equivalent integrated solution is estimated with the help of low-power state-of-the-art components from literature and ASIC simulation.. When comparing diagram 1b and 2b, the big impact of the idle loss is clearly visible. The simulation of the efficiency versus output current is provided down to 1 mA. Smaller output currents are not simulated due to very long execution times for the simulation.

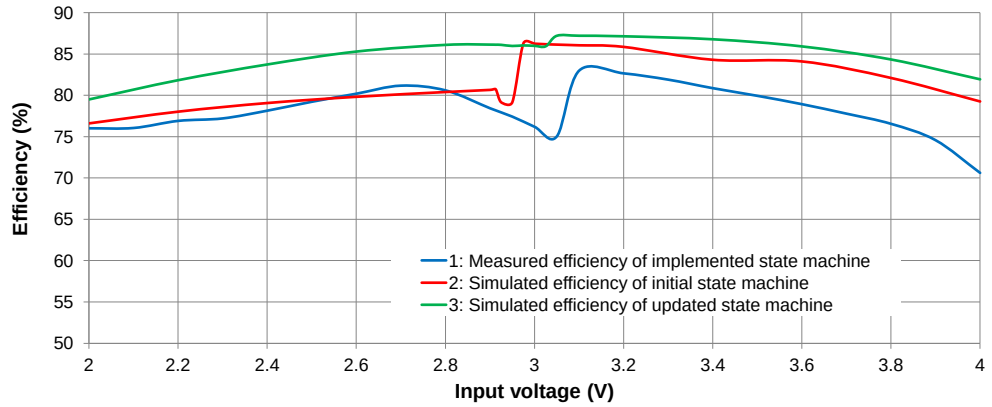


Figure 5.5: Comparison of simulated and measured efficiency at $V_{out} = 2.4\,V$ and $I_{out} = 45\,mA$

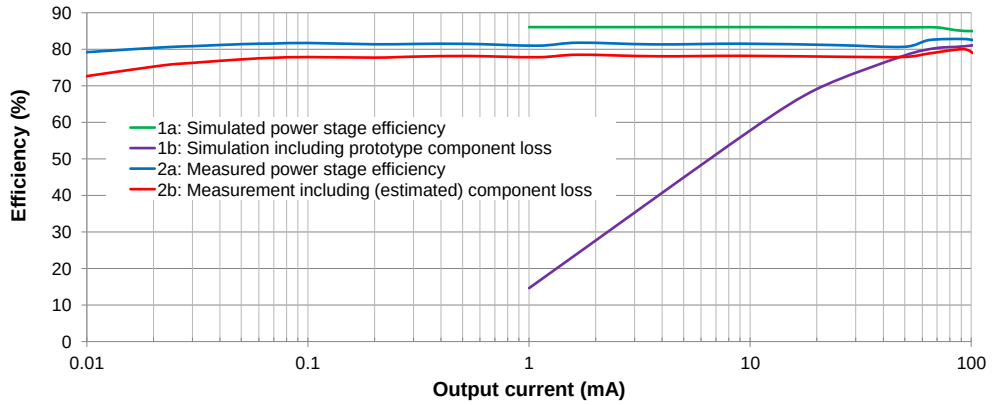


Figure 5.6: Comparison of simulated and measured efficiency depending on the output current and with different current sense amplifiers and comparators at an input voltage of $3.1\,V$ and an output voltage of $2.4\,V$

Comparison to State-of-the-art Products

Figure 5.7 illustrates the measurement results of the presented design together with a similar characteristic of the commercial voltage regulator LTC3531 from Linear Technology[1]. The diagram illustrates the power efficiency versus the voltage difference between inputs and outputs. The graph of the implemented regulator uses a 10 % efficiency offset in scale when compared to the LTC3531. For a discrete prototype assembly, efficiencies are in general lower than in integrated circuits because of parasitic circuit elements. In contrast to the presented design, the LTC3531 uses three operation modes. Buck, boost, and the so called 4-switch mode that is used in the region between buck and boost mode. To determine mode transitions, input and output voltage are compared. The drawback of this concept is that the transition from step-up to step-down not only depends on the input and output voltage, but also on the actual load. Therefore, the LTC 3531 needs the 4-switch mode to cover the region where the buck or boost mode cannot be clearly determined. In this mode, an additional timer is used to force state transitions. The actual design transitions from boost to buck mode and vice versa via principle that monitors the

[1] `http://www.linear.com/`

inductor current has already been introduced in section 3.3.2. It makes comparison of input and output voltage as well as a third operation mode obsolete. Rather two additional thresholds of the inductor current are needed (two additional comparators). In the presented design, the efficiency gap of buck and boost mode is decreased when compared to state-of-the-art regulators. The decreased efficiency at high voltage differences is caused by the limited gate voltage for the power transistors (PFGA output = 3.3 V). So the P-channel FETs cannot be turned off completely at high input voltages.

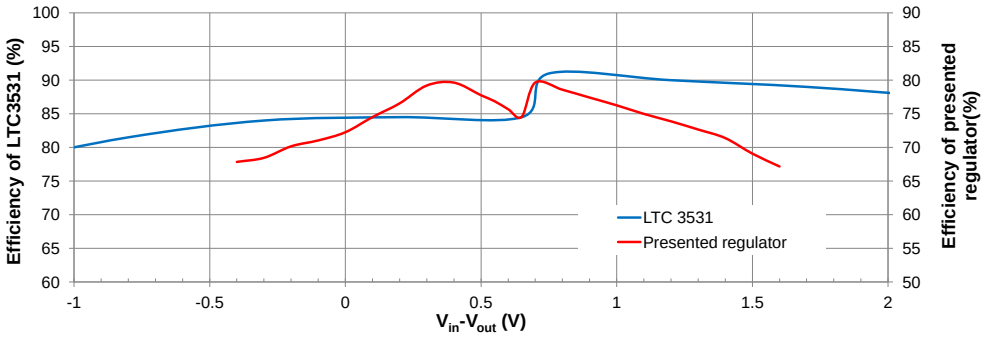


Figure 5.7: Comparison of prototype efficiency and state-of-the-art regulator LTC3531 from Linear Technologies versus voltage difference between input to output

Figure 5.8 illustrates comparison of power efficiency versus output current of the introduced design with the LTC3531 converter. The curve "Simulated Integrated Solution" has been discussed in section 5.4 and the results from the presented design show output currents down to 10 µA while the characteristic of the LTC3531 ranges down to a minimum output current of 0.1 mA. As shown in the figure, the proposed voltage regulator provides a better efficiency at ultra low power loads than today's off-the-shelf products. This benefit is offered by the novel power management algorithm of the digital and analog implementation. As discussed in chapter 3, the main applied power saving concepts are

- An event triggered digital control to minimize dynamic loss of the digital implementation as well as the absence of a clock generation circuit
- Minimization of always-on analog components
- Reduced regulator active time in combination with a multiple input multiple output channel concept
- Control of sleep-modes of the analog components via the digital control circuit

In [CRaM07], a Power Mixer-Charger-Supply System that provides the capability of a limited multiple input multiple output concept is introduced. It uses a fuel cell as primary source and supplies the actual load and a secondary battery with energy. The output is sourced by the fuel cell or the secondary battery. The limiting factor of this concept is that the converter could only operate in boost mode when the load or the battery is charged by the fuel cell, and only operates in buck mode when the load is supplied by the battery. In contrast, the presented design

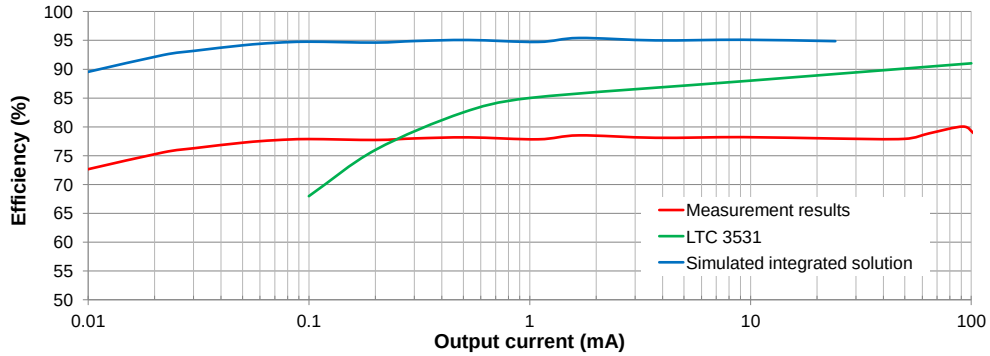


Figure 5.8: Comparison of prototype with state-of-the-art regulator LTC3531 in a power efficiency versus output current diagram.

provides possibilities to use a multiple input/multiple output system, where any combination of step-up and step-down operation is possible. Furthermore, the used input and output voltages are allowed to vary dynamically during operation. Multiple input and output concepts are not yet available in off-the-shelf components.

Unfortunately, neither in data sheets of off-the-shelf regulators nor in technical papers, the clock generation or clock management is discussed. Regulators that operate in PWM mode use a fixed clock frequency for operation. In burst mode and especially at low output currents, a permanent clock has a negative impact to the regulator's own-consumption. Main considerations about the event triggered digital control are to remove the common clock generation circuit from state-of-the-art implementations to save energy, as well as reduction of the dynamic loss of the digital state transitions flip-flops (compare with literature [MNB01]). Furthermore, the reaction on an event (reaching a current value) is performed faster via usage of the event triggered state machine approach than using a permanently clocked circuit. With the event triggered concept, the clock frequency is direct proportional to the frequency of the transferred energy pulses from the input to the output of the converter. So the clock frequency is variable and depends on the load conditions and thus, efficiency is high also during light load condition.

5.4 Extrapolation to Integrated Solution

When moving to an integrated solution with the introduced design, some changes and adoptions are required of the implemented discrete prototype to improve functionality and first of all power efficiency. The presented double transistor scheme discussed in section 3.2.1, is not needed within an integrated solution because the bulk connection of a FET is free accessible. When connecting the bulk connectors of the P-channel FETs to a high voltage level (the maximum potential of all input and output voltages), the double transistors at the regulator inputs and outputs can be reduced to single transistors. The high voltage level at the bulk connection disables the body diode and the transistor can block currents in both directions. This improves regulator efficiency drastically via reduction of the static on-resistance values as well as decreasing the gate charge of the input and output switching transistors. The lower gate charge increases switching speed

which has a positive impact to the shoot through protection and therefore also to efficiency. An integrated solution is less vulnerable to noise and interference because of compactness. This enables capabilities of a smaller shunt resistor as well as lower consumption of the auxiliary voltage dividers for the current sense amplifier (see also section 3.2.2). Furthermore, the current thresholds of the inductor current can be decreased. The introduced prototype operates with a peak current I_H of 200 mA. By decreasing the current thresholds, the maximum output current (power) is reduced as well and the static loss of the transistors is decreases. Because of the relation $P_L = I^2 \cdot R$, a reduction of the peak current has disproportionate high impact to the transistor's loss. Additionally, the peak current reduction reduces the amount of energy of a single transfer pulse. This decreases the ripple voltage at the output capacitor and solves the drawback of the prototype version from [MNB01].

According to the considerations of this section, the converter simulation model was updated to achieve results that are almost close to a real ASIC implementation. At a maximum average output current of 35 mA (a peak value I_H of 55 mA) and equal analog components from section 5.1, a peak efficiency of 94.9 % is reached. At an output current of 1 mA, still an efficiency of 93.4 % is provided at a ripple voltage of less than 0.2 %. Border conditions of the simulation are an input voltage of 3 V, an output voltage of 2.4 V (step-down mode) and the consideration of a single I/O system. The simulated graphs are also presented in figure 5.8. When compared to state-of-the-art, this an enormous performance gain especially in the low load region below 100 µA. Consequently, the proposed solution has very high potential to save lots of energy in WSN nodes during standby operation.

6 Conclusion and Outlook

Finally, this chapter gives a summary over the main findings of this thesis, presents the most important results and gives an outlook over possible enhancements. Section 6.1 gives a resume over problem description, design phase and results. Section 6.2 discusses some possible enhancements for future developments such as implementation of a serial interface for configuration and an alternative concept of measuring the inductor current. At the end of the chapter, future prospects of using the presented voltage regulator are made.

6.1 Summary

A concept for a switched-mode voltage regulator for the special requirements of wireless sensor nodes has been presented. The proposed regulator concept was designed under consideration of low price, high integration density, small outline and high power efficiency, especially at low load currents. To reach the high efficiency goal, a sophisticated energy management was implemented. The presented voltage regulator supports operation in step-up and step-down mode as well as dual input and dual output operation with a single off-chip inductor. The introduced design is expendable to a user-defined number of inputs and outputs. The proposed method for a fast start and a fast stop technique makes usage of the multiple output concept more practical and gains power efficiency. The introduced multiple input/multiple output concept provides possibilities for cost and size reduction, and further increases the DC/DC converter's efficiency. Cost and size reduction is achieved via reduction of the number of off-chip components when compared to single output regulators. Off-the-shelf regulators require separate inductors for each of the regulated output voltages. Because inductors are the external components that require most of the PCB space and dominate the overall power supply cost, a multiple output channel regulator is highly beneficial and moreover, multiple subsystems of a wireless sensor node can be supplied simultaneously which reduces the number of necessary voltage regulators and passive components. The efficiency boost in multiple output mode operation is reached via increase of the mean regulator load, so it reduces the impact of the quiescent current of the regulator. This behavior is illustrated in figure 3.18. With the help of the presented concept of multiple inputs, the sensor node can be supplied directly via a combination of energy harvester and secondary battery or other types of energy storage devices. With the possibility to feed one output channel

back to an input, the voltage regulator can work additionally as charging circuit. In contrast to designs presented in technical papers, any possible input/output combination can be used and each converter channel can operate in step-up mode or in step-down mode. The integrated priority management of inputs and outputs provides a defined startup behavior, and can prioritize the supplied loads.

To achieve the goal of high efficiency, some considerations for energy saving have been made. Digital circuits are often implemented as state machines. Typical implementations use a clock signal for synchronizing state transitions, or inputs and outputs. Clock signals cause energy loss at generation as well as in flip-flops also without state transitions or logic level change. During low output-power conditions, the clock-caused loss has a big impact to the converter efficiency. Therefore, an event triggered digital control was introduced to minimize dynamic loss of the digital implementation. Most analog components of the converter circuit can be switched powered down, when the regulator operates in idle mode. So a big issue in energy saving is achieved. The main part of quiescent loss is caused by the voltage monitors for the input and output voltage. In contrast to the rest of the analog regulation components, these voltage comparators have to operate in always-on mode. Since no state-of-the-art low speed and low power comparator was available, a comparator adapted to the needed requirements was designed and simulated. So a significant reduction of the quiescent current was achieved.

For evaluating the proposed concept and estimating possible problems of an integrated build-up, a prototype, with discrete analog components and a digital implementation using a FPGA, was implemented. The prototype confirmed the function of the design. It gave information about that the switching transistors at the shunt resistor has a significant impact to the regulator functionality. Even short overlapping of the switching transistors at the regulator output - at the shunt resistor - cause disturbances in the current measurement circuit and compromises regulator functionality. In contrast, overlapping at the input decreases the efficiency but does not have an impact to the main function. Another important point is that the circuit is in general very error-sensitive at the shunt resistor. Parasitic capacitances and inductances have a much higher impact than at nodes that are not connected to the shunt. The achieved efficiency of the prototype is about 10 % lower than for off-the-shelf buck-boost converter. An efficiency gain of up to 95 % can be reached by using integrated switching transistors. Estimated results of an integrated solution are only provided by simulations. By using the presented design, a reduction of the quiescent current from 15 µA, of off-the-shelf regulators, to less than 1 µA can be achieved. The introduced multiple output concept provides a further efficiency gain by increasing the regulator utilization while the multiple input concept provides the possibility to use multiple supply voltages. The single-inductor concept decreases regulator outline as well as the overall price. The possibility to use each output in step-up and step-down mode with dynamic mode-switch capabilities, provides a wide application-area and efficient operation.

In summary, the designed concepts provide the following advantages:

- Independent operation of each output channel in step-up or step-down mode.
- Reduction of the quiescent current from 15 µA to less than 1 µA compared to off-the-shelf voltage regulators. This results in an efficiency gain from 68 % to 95 % at 100 µA output current.
- Reduction of required off-chip components and PCB outline in wireless sensor nodes via the multiple input/multiple output concept, which means a reduction from 6 capacitors and 3 inductors to 4 capacitors and a single inductor when 3 outputs are assumed.
- Innovative digital control method for smooth buck-boost operating mode transition: Low voltage ripple and low power consumption via a novel event triggered approach.

6.2 Enhancements

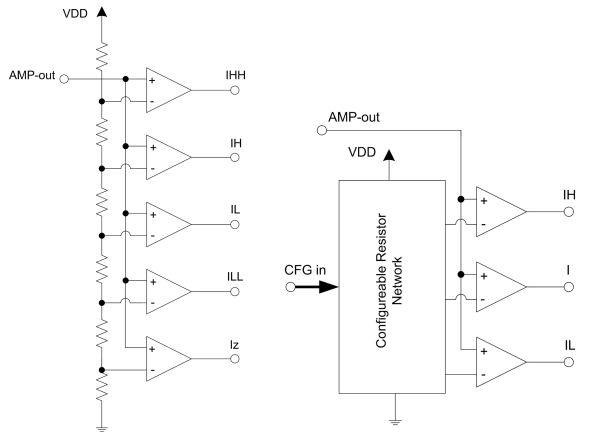
The actual core of the proposed voltage converter concept has been investigated and tested within the course of this thesis. There are a number of extensions and enhancements possible to further boost functionality and efficiency, or save effort and silicon area and cost. As mentioned in the previous chapters, the voltage comparators of the outputs do not require a fast response time but have to operate in always-on mode. When a specific output is disabled, the corresponding output voltage comparator is not needed and can also be turned off to further save energy.

To decrease the number of needed analog components, the comparator array, used within the design can be advanced. In the actual design, a single comparator for each current level is used as illustrated in figure 6.1(a). Because the inductor current does not have discontinuities, the current typically increases or decreases linear. For this reason, the number of current comparators can be reduced from five (I_{HH}, I_H, I_L, I_{LL}, I_z) to three (I_H, I, I_L) via adaption of the configurable resistor network from figure 6.1(b). Using the CFG-input, the recently crossed current level can be switched to the middle output and the other two outputs represent the next higher respectively the next lower current level threshold. The interpretation of the output signals and the controlling of the resistor network is performed by the digital control unit. When using the components introduced in section 4.2, the energy consumption of the current measurement circuit can be reduced by 23 %. Due to the implementation with transistors and comparators where the ratio of the resistor values at the comparator inputs define the current levels, the actual current thresholds can be changed by altering the resistor values of the voltage divider. This is used to adapt or switch the thresholds for output current sensing. At low load conditions, the current thresholds can be decreased dynamically during operation to reduce the loss of the on-resistance of the switching transistors. When the output current exceeds a specific value, the current thresholds can be changed to increase the maximum possible output current. The average load can be determined either via the duty cycle of the switch control signals or either via the mean value of the current amplifier output signal. A power-mode transition is performed then, if a specific average value is exceeded.

In general, the digital control state machine of the regulator provides extendability in many design aspects. Some possible enhancements for the digital implementation are:

- Flexible configuration via serial peripheral interface
  - output voltage
  - state machine version
  - load modes
- Supervisory information
  - utilized input
  - output voltage stability/quality
  - priority configuration and status
  - regulator utilization
  - chip temperature

A possible subsequent work may be the implementation of a fully integrated ASIC version.



(a) Comparator array used within design and prototype

(b) Possible enhancement of a comparator array to reduce the amount of needed comparators

Figure 6.1: Different versions of the comparator array for current threshold evaluation

6.3 Vision

The DC/DC converter concepts presented and evaluated within this thesis provides advantages especially for low power applications and wireless sensor networks. Multiple output voltages increase the flexibility for the design of wireless sensor nodes because the selection of used components is not limited to components with a specific input voltage range. Each component can

be supplied by its optimal voltage to operate within its optimal efficiency range and performance point. Beside the efficiency boost, a cost and size reduction is achieved with the proposed and novel design.

With the help of the following example, the effect of the introduced concept is shown. In a medium-class auto, cables with a total length of up to 2 km are used. When the amount of wired sensors is reduced, and only the system critical ones remain, a significant reduction in wire length can be reached. In this example 1 km is assumed This results in a weight reduction of the car of about 60 kg which is about 3 % of the overall weight. As a consequence, also the fuel consumption of the car is lowered. For a typical CO_2 emission of 190 g/km, this means a reduction of 5.7 g/km caused by the decreased weight. Considering 3 million cars with an average of 13,497 km p.a. in Austria, this marginal reduction is accumulated to more than 200,000 tons of CO_2 reduction per year. This amount is equally produced by a coil-fired power plant if 380 GWh of electrical energy is produced. So far small and lightweight and less expensive nodes, this scenario can become possible.

In a second example, a sensor network for temperature measurement within a building may be used for air conditioning. It can consist of at least 100 network nodes. The node remains in idle mode for 99 % of the time. In this idle period, a current consumption of 10 µA is assumed. The efficiency of a typical state-of-the-art voltage regulator is about 40 % at 10 µA load. This own consumption increases the supply current by the factor of 2.5 to 25 µA. The proposed regulator provides an efficiency of 80 % at 10 µA load current and increases the overall supply current only to 11.1 µA. This means a reduction of more than 50 % respectively a doubled lifetime in case of a battery powered application. Consequently, the service interval for battery replacement is doubled, or alternatively, half the batteries are required for the full service duration. So lots of energy, resources, and environmental pollution could be saved.

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Appendix

Schematic

Figure 1 illustrates the complete schematic of the implemented discrete prototype assembly. The schematic is divided into three main parts. The left upper corner shows the actual the power stage with switching transistors, inductor, shunt resistor, as well as the voltage monitoring circuits for input and output supervisory and the reference voltage generation. In the right upper corner, the current sense amplifier circuit with current threshold detection is illustrated. At the bottom of the schematic, the load circuits and external connectors are shown.

PCB Layout

The PCB was designed as a dual layer board where the bottom layer was implemented as ground plane to minimize signal disturbance via interference and noise. Signals are routed on the top layer. Figure 5 illustrates the bottom layer. The homogeneous ground plane is a precondition for low signal distortion because the frequency spectrum of the signals ranges up to gigahertz range. On the top layer, two different track widths are used. For signal lines a width of 0.15 mm and for power tracks a width of 0.4 mm is used. This reduces the resistance and inductance of the high current paths. Figure 2 illustrates the combination of top-, bottom- and component outline layers. The input and output comparators are located at the bottom of the PCB, while the current comparators are placed at the right side. The current amplifier is centered on the PCB to keep the track distance from the shunt resistor to the amplifier input as short as possible. The load circuits are placed on the upper side of the PCB. Figure 3 illustrates the outlines of the used components on the top layer. The bottom side is does not contain any components.

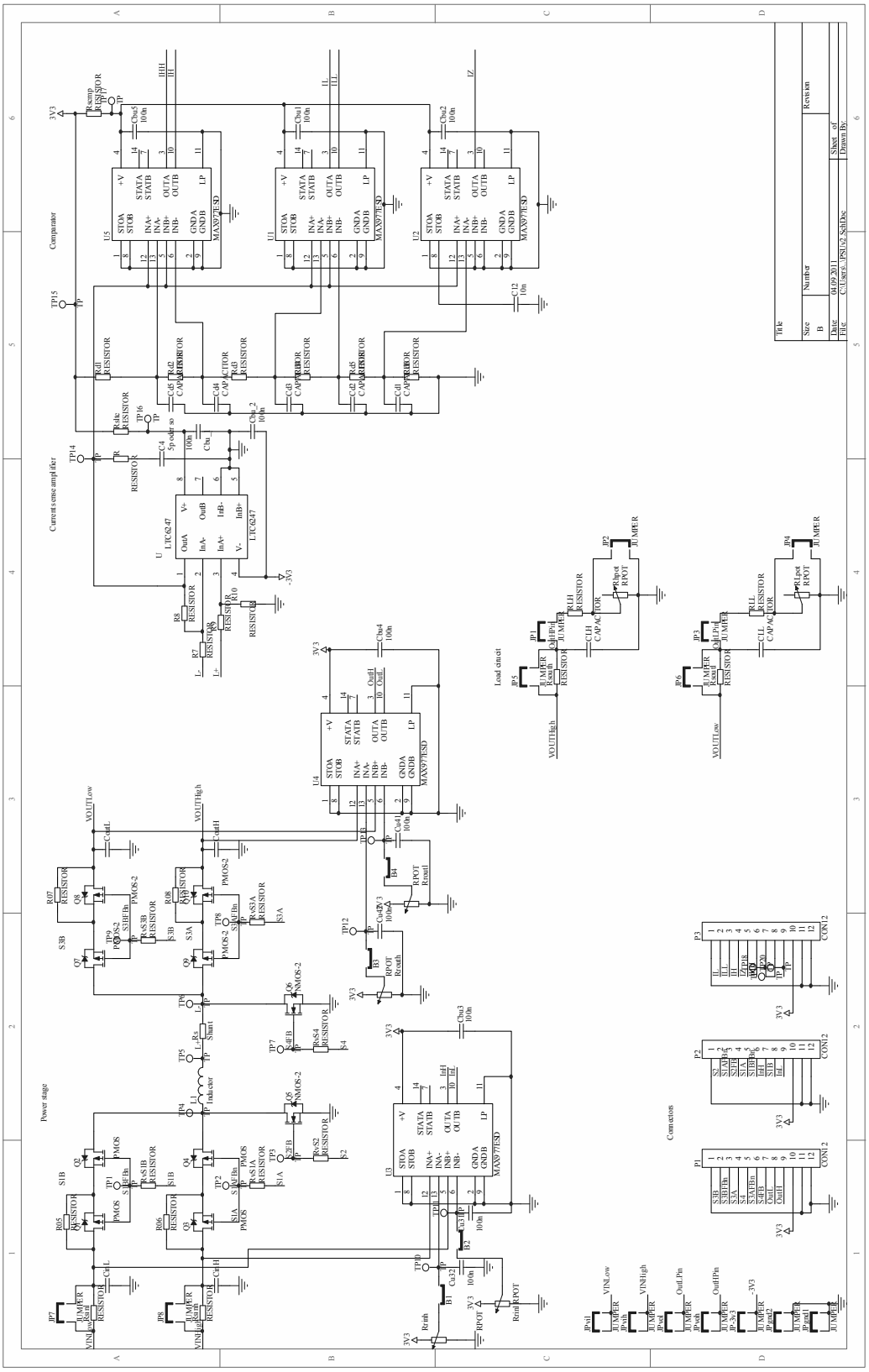

Figure 1: Full schematic of the designed prototype assembly

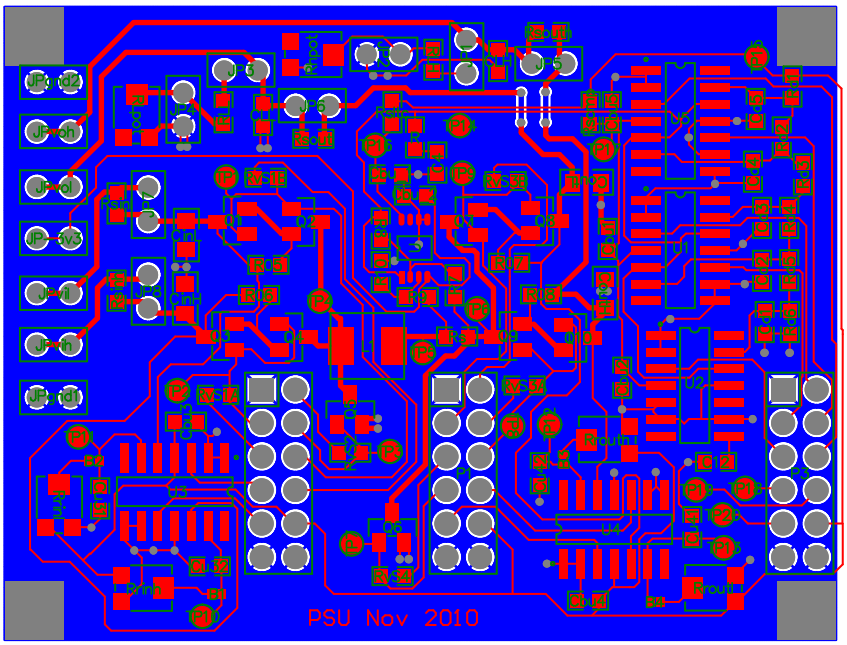

Figure 2: PCB layout with top layer, bottom layer, and component overlay drawing

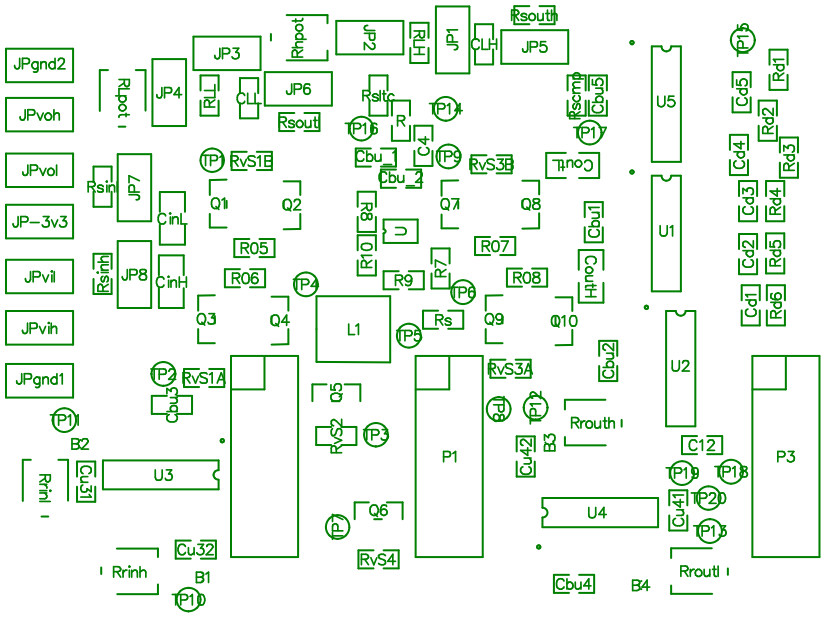

Figure 3: Component outline layer of PCB layout

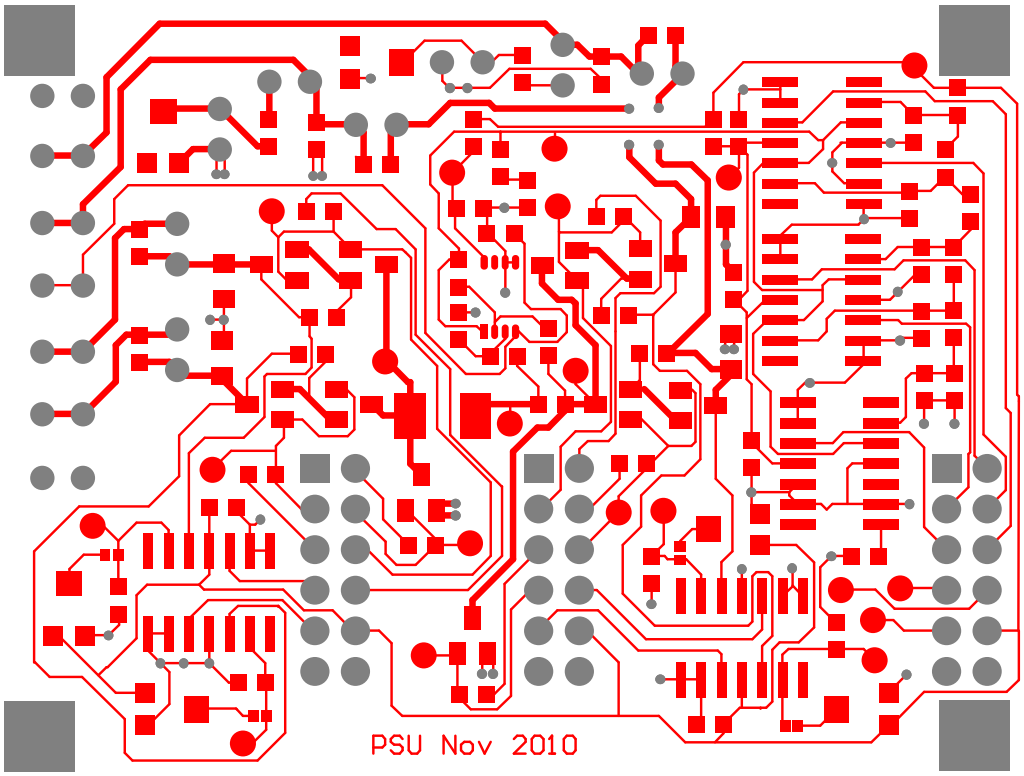

Figure 4: PCB layout: top layer

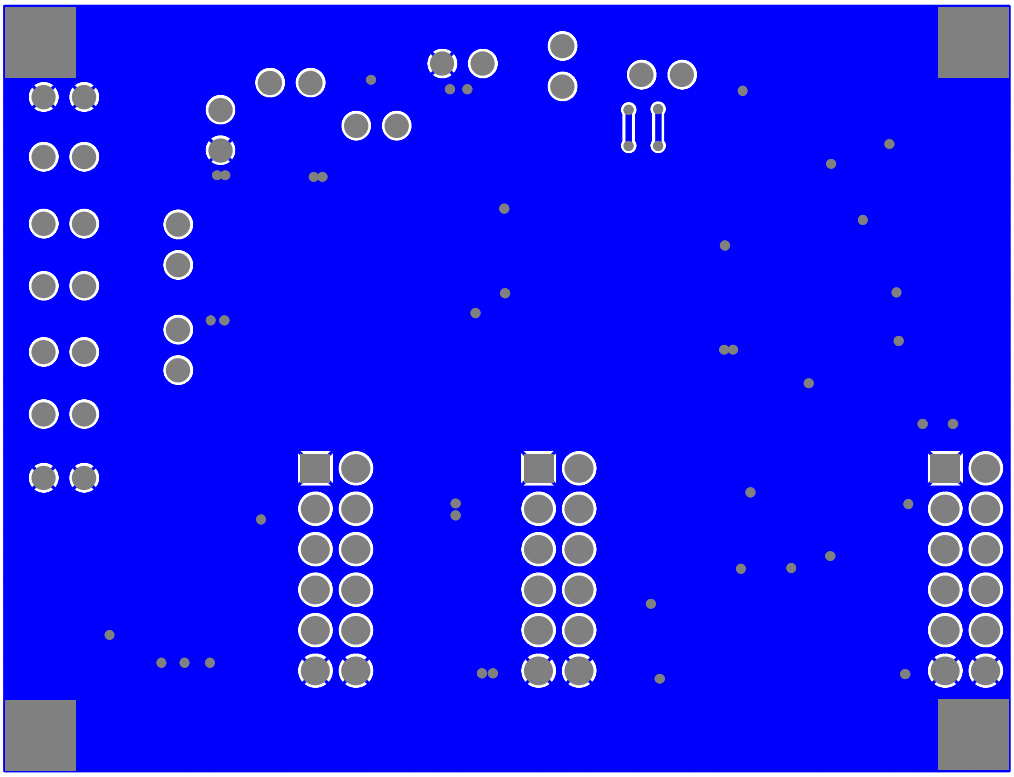

Figure 5: PCB layout: bottom layer