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# Double Quantum Dots in Germanium Hut Nanowires: Fabrication and Characterization

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# Foreword

Every thesis starts with a foreword to thank all the people who were somehow included in the process. Not to break the tradition I will also mention some of the people I'm thankful to.
First of all, I would like to thank my mentor Georgios Katsaros for accepting me into his group. It has been my pleasure to work on such a exciting research topic with a highly motivated group.
Thanks Lada,Josip and Marian for teaching me how to operate the cleanroom machines and conduct the experiments. Daniel, Alesandro and Andrea thanks for all the discussions on the spin blockade. Luka, thanks for helping me with python (and thanks for bringing the couch in the office). Marco and Kushagra, the superconducting twins, thanks for showing nice looking plots I completely do not understand.
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Most part of my life in Vienna I have spent with my two great friends, Martin and Dominik. Thanks for teaching me Tiroler Dialekt and making me company in good and bad times.
Of course my studies would not be possible without the help of my family and relatives. Thanks on all the support during these years.

*In memory of Milan Soče (1960-2017†)*

# Abstract

Since the first theoretical work on quantum computation scientists have considered various systems for the implementation of a large scale qubit system. One of them are electron spins confined in quantum dots. In the past few years, hole spin states were also suggested as promising qubits, because of their strong spin-orbit coupling which allows fast all-electrical spin manipulation. In 2018 the first germanium hole spin qubit was demonstrated in a double quantum dot device made out of a hut wire and it showed record manipulation times of $140 MHz$.
However, obtaining reproducible and stable double quantum dots in this material system proved to be a difficult task. In the presented work, various fabrication recipes have been developed and tested for achieving this goal. Using four different samples, devices are characterised and a significant improvement in terms of charge-noise and tunability is reported. The presented results enable further and more complex spin qubit research in this material system.

# Kurzfassung

Seit den ersten theoretischen Arbeiten über Quantenrechner haben Wissenschaftler verschiedene Systeme für die Implementierung eines solchen Quantenprozessors in Angriff genommen. Eine davon besteht darin einzelne Elektronen in einem Quantenpunkt einzufangen. In den letzten Jahren wurden auch Spin Zustände von Löchern als vielversprechende Kandidaten für Qubits vorgeschlagen da sie eine starke Spin-Bahn Kopplung besitzen welche wiederum eine komplett elektrische Manipulation des Spins ermöglicht. In 2018 wurde das erste Germanium Loch-Spin Qubit in einem Doppelquanten Punkt in einem hut wire gezeigt. Eine Rekordmanipulationsfrequenz von 140$MHz$ wurde hierbei demonstriert.
Nichtsdestotrotz erwies sich die Reproduzierbarkeit und Stabilität der Doppelpunkte in diesem Material als äußerst schwierig. In der vorliegende Arbeit, verschiedene Fabrikationsrezepte wurden zur Optimierung dieser Eigenschaften getestet. Mit vier verschiedenen Proben, die Charakterisierung is gemacht und eine deutliche Verbesserung des Elektrischen Rauschens und der Stimmbarkeit wird gezeigt. Die präsentierten Resultate ermöglichen weitere und komplexere Forschung zu spin qubits in diesem Materialsystem.

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# List of Abbreviations

**ALM** - Atomic Force Microscope
**ALD** - Atomic Layer Deposition
**CIM** - Constant Interaction Model
**DAC** - Digital-Analog-Converter
**DMSO** - Dymethyl Sulfoxide
**DQD** - Double Quantum Dot
**EBL** - Electron Beam Lithography
**EDSR** - Electron Dipol Spin Resonance
**GtG** - Gate to Gate
**HF** - Hydrofluoric Acid
**HH** - Heavy Hole
**HV** - High Vacuum
**HW** - Hut Wire
**IPA** - Isopropanol
**LH** - Light Hole
**mG** - Middle Gate
**ML** - Monolayer
**NW** - Nanowire
**PCB** - Printed Circuit Board
**PMMA** - Polymethyl Methacrylate
**PSB** - Pauli Spin Blockade
**RTA** - Rapin Thermal Annealing
**SEM** - Scanning Electron Microscopy
**SOI** - Spin Orbit Interaction
**SQD** - Single Quantum Dot
**UHV** - Ultra High Vacuum
**QC** - Quantum Computer
**QD** - Quantum Dot

**QM** - Quantum Mechanics
**QIS** - Quantum Information Science

# 1 Introduction

At the start of the 20th century physicists were struggling to understand the interaction between light and matter. The photoelectric effect (Einstein 1905) proved that light is not a wave as believed at the time but rather a particle with a finite, discrete amount of energy. In 1924 De-Broglie proposed that all matter has wave properties which was experimentally confirmed by Thomson in 1927. The wave-particle duality along with other quantum effects such as the uncertainty principle (Heisenberg 1927) opposed the known laws of classical mechanics. The intellectual discussions on the nature of matter and light yielded a completely new theory in physics which was referred to as Quantum Mechanics (QM).
By applying the laws of QM to semiconductors, physicist invented the first semiconductor transistor (Shockley,Pearson 1946). With each transistor representing the state of a logical bit, the transistor became the backbone of classical computers. The metal-oxide-silicon (MOS) transistor proved to be the most scalable path and started dominating the industry of semiconductor electronics. Enormous efforts in fabrication techniques doubled the number of transistors per chip approximately every two years, commonly known as Moor's law. Today modern electronic devices contain billions of transistors per chip with each transistor having a length of around 10 nanometers (Fig. 1.1) Supercomputers have the power to do several quadrillion ($10^{15}$) floating point operations per second (FLOPS). However, using classical computation it is still impossible to solve certain problems, namely to simulate many-body QM systems, like complex chemical molecules. The simulation of quantum systems requires a completely different approach to computation.

The first proposal of a quantum computer (QC) was formulated in 1982 by Richard Feynman[1]. Since then a lot of theoretical works on which quantum

[1] Feynman, 1982.

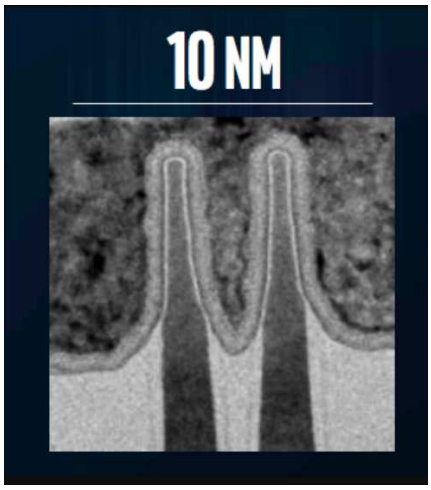


Figure 1.1: Cross section of a modern transistor (IEEE, 2017) .

computation can base have been done. It has been proven that a QC could outperform the classical computers not only in QM simulations[2] but also in certain type of algorithms used in cryptography[3] and database search[4]. A whole new field of Quantum Information Science (QIS) arose but a QC out-preforming the classical one has still not been reported[5]. The reason lays in the very fragile nature of the qubits, which are the basic carriers of information in a QC. A qubit is in principle any two level QM system, which can be written as:

$$|\psi >= \alpha|1 > +\beta|0 > (\alpha, \beta \in \mathbb{C}) \tag{1.1}$$

Where the state $|\psi >$ is in a superposition of states $|1 >$, $|0 >$ with each state having a probability of $\alpha^2$ and $\beta^2$, respectively. Exploiting the quantum

[2]Deutsch, 1985.
[3]Shor, 1997.
[4]Grover, 1996.
[5]During the writing of this thesis Google reported a calculation performed using 53 superconducting qubits, which outperforms the classical computers in a random state preparation (Arute et al., 2019). However, it is still debatable whether quantum supremacy is reached.

effects of superposition and entanglement is what gives quantum computation an advantage over the classical computation. (A rigorous proof why this is true is part of QIS and won't be covered in this thesis). For a QC to work, the qubit manipulation must be fast and nearly error free which is the main focus of the current experimental research. The two limiting qubit factors are the relaxation time $T_1$ and the decoherence time $T_2$. The relaxation time $T_1$ refers to the time upon which the qubit will spontaneously relax to the ground state while decoherence $T_2$ is the expected lifetime of a previously prepared superposition.
Many different systems are being investigated as possible qubits, such as cold- ion traps[6], optical lattices[7], nuclear spins[8], superconducting circuits[9] etc. In each of the above systems, scalabillity and decoherence challenges still exist.

## 1.1 Quantum Dots for Quantum Information Processing

One of the proposed implementations for realising a qubit is using the spin of a single electron confined in a Quantum Dot (QD)[10]. The Electron spin 1/2 is a natural two-level quantum system where the state of the spin is in superposition of 'up' and 'down' states. Since the spin state is not perturbed by electric potential fluctuations, for systems with low spin orbit coupling, long coherence times are expected. Further on, in the original *Loss* proposal it was suggested that two electrons sitting in neighboring quantum dots (also called Double Quantum Dot) can be electrically coupled and decoupled by the barrier in-between. This can affect the time evolution of their spin states via the Heisenberg exchange coupling, which can be implemented as a Quantum XOR gate. The XOR gate together with a single qubit operation is a sufficient basis for an universal QC[11].

[6] Cirac and Zoller, 1995.
[7] Brennen et al., 1999.
[8] Chuang, Gershenfeld, and Kubinec, 1998.
[9] Nakamura, Pashkin, and Tsai, 1999.
[10] Loss and DiVincenzo, 1998.
[11] Barenco et al., 1995.

As QDs can be formed in semiconductor materials and can be fully electrically controlled, they have attracted interest for the experimental realisation of such a qubit. The first spin state read-out has been reported in a 2DEG GaAs/AlGaAs QD structure in 2004[12]. Two years later, in the same material system, the first coherent oscillation of a spin 1/2 confined in a QD was reported[13]. However one of the major issues with GaAs is the presence of nuclear spin which shortens the qubit's coherence time through the hyperfine interaction. Research then focused on finding a more suitable QD host platform, mainly in group IV materials, silicon and germanium. Silicon can be isotopically purified by leaving only $Si^{28}$ which has almost no nuclear spin and it's coherence time has been demonstrated to be close to a second[14].

## 1.2 Interest in Germanium holes

Interest in holes started gaining ground as theory suggested that holes should have reduced hyperfine interaction[15] and strong spin-orbit interaction (SOI) which implies fast and pure electrical manipulation of the spin-states[16] without the use of micro-magnets. In addition holes do not have nearly degenerate ground states which eliminates the valley splitting problem. The first qubit which demonstrated coherent hole-spin rotations using electron dipole spin resonance (EDSR) has been reported in a p-type Si FinFET[17].

Germanium as a natural host of hole spins, due to the theoretically predicted much stronger and tunable SOI[18], started emerging as an alternative material for spin qubit research.

In 2018 the first Ge hole spin qubit[19] has been reported. Earlier this year

[12] Elzerman et al., 2004.
[13] Koppens et al., 2006.
[14] Muhonen et al., 2014.
[15] Testelin et al., 2009.
[16] Bulaev and Loss, 2007.
[17] Maurand et al., 2016.
[18] Kloeffel, Trif, and Loss, 2011.
[19] Watzinger, Kukučka, et al., 2018.

(2020) a quantum CNOT gate was reported in a DQD Ge/SiGe heterostructure[20]. It's fair to say that Ge has positioned itself as an exciting material for spin qubit research and a possible candidate for future scale-up which could lead to a quantum processor.

## 1.3 Outline of the Thesis

The first Germanium hole spin qubit was formed in a Ge hut-wire (HW) DQD and showed record manipulation time of $140MHz$, presumably due to the strong spin orbit coupling in Ge. However the spin-qubit research in hut wire DQDs has since then halted. Obtaining reproducible and clean DQD devices has proven to be an experimental research bottleneck.
In this thesis, first the semi-classical theory of hole transport through quantum dots at cryogenic temperatures will be discussed. In the following chapter, experimental methods for fabricating DQD devices in a Ge HW are described and fabrication recipes are revealed. In the measurement chapter, the characterisation of the fabricated devices is done and the results are presented. As a conclusion, main results of the thesis are summarized and an outlook is given.

[20] Hendrickx et al., 2020.

# 2 Hole Transport in Single and Double Quantum Dots

A QD is a nanometer scale potential box in which a single charge carrier can be confined. With confining the carrier it is meant, that the carrier is trapped in a potential well in all the three spatial dimensions, just like an electron trapped in an atom by the nucleus potential. Since the electron shell filling in a QD can follow Hund's rule[1], a QD is often referred to as an artificial atom.
In semiconductors, a vacant electron state in the valence band is defined as a quasi-particle with an opposite charge ($+e$) called *hole*. In an analogous way, holes can also be confined in QDs with a use of a confinement potential.
In our material system, the Fermi level is close to the valance band due to the high work function of Pt used for the contacts. (see Chapter 3.0.1). Therefore, at cryogenic temperatures, just holes are localised in Ge. There are many different approaches for the experimental realisation of a semiconductor QD (self-assembled, lateral, nanowire based). This thesis focuses on QDs formed in a nanowire (NW). The diameter of a NW is in order of the electron De-Broglie wavelength.

$$\lambda = \frac{h}{m^* v} \sim (10 - 100nm) \tag{2.1}$$

Where $m^*$ represents the effective mass of a quasi-particle. For heavy-holes in germanium and for the parallel transport direction it is $\approx 0.04 m_0$it [2] ,[3].

[1] Ashoori, 1996.
[2] $m_0 = 9.11x10^{-31}kg$ is the free electron rest mass.
[3] G. Katsaros et al., 2011.

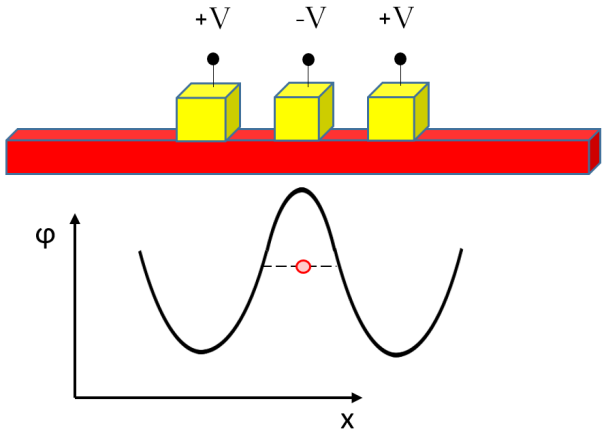


Figure 2.1: Schematic illustration of a hole confined in a NW based QD. Positive voltages applied at the neighboring gates build potential barriers to the dot.

Such a confinement implies quantized energy level spacing in two of the dimensions. By adding top gates and by applying an electric field, confinement in all the three spatial dimensions is possible (see Fig. 2.1).

The following chapter, will be focused on a semi-classical model which describes hole transport spectroscopy through a single and double QD at cryogenic temperatures.

## 2.1 Single Quantum Dot

To investigate the electronic transport properties of a single quantum dot (SQD) a three terminal device is studied as depicted in Figure 2.2. The QD energy spectrum is probed by measuring the current flowing through the device. The tunneling barriers $(R_L, R_R)$ have to be sufficiently transparent to allow electron tunneling and thus the observation of an experimentally measurable current. However they need to be opaque enough so that short tunnelling time $\Delta t$ does not influence the energy broadening of the levels due to the Heisenberg uncertainty 2.3 relation. Here $\Delta t$ translates to as the

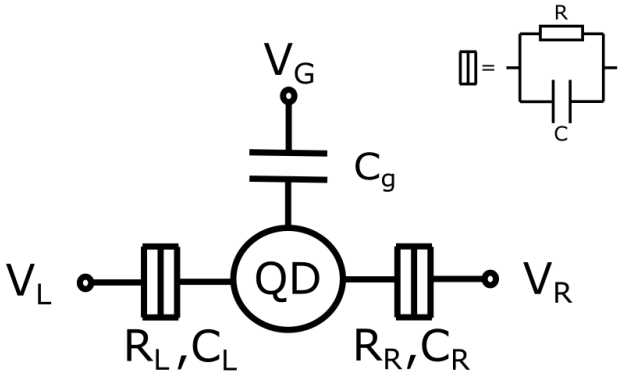


Figure 2.2: Semi-classical model of a SQD

typical time it takes to charge and discharge the dot[4]; $R$ is tunneling barrier resistance and $C$ is the capacitance of the dot.

$$\Delta t = RC \tag{2.2}$$

$$\Delta E \Delta t > \frac{\hbar}{2} \tag{2.3}$$

The gate terminal $V_G$ is ideally purely capacitively coupled[5] to the dot and it is used to tune the electrochemical potentials.

### 2.1.1 Constant Interaction Model

The main electrostatical features of a SQD system can be described using the semi-classical Constant Interaction Model[6] (CIM). I begin the study using the common known equation for the electrostatic energy of a capacitor :

$$U = \frac{CV^2}{2} = \frac{QV}{2} \tag{2.4}$$

[4]Kouwenhoven and McEuen, 1999.
[5]Pure capacitive coupling implies zero leakage current flowing to the terminals $V_L, V_R$
[6]Beenakker, 1991.

The capacitance $C$ and the charge $Q$ of a QD are assumed to be

$$C = C_L + C_g + C_R \tag{2.5}$$

$$Q = C_L(V - V_L) + C_g(V - V_g) + C_R(V - V_R) = n|e| \tag{2.6}$$

where $n$ is total, quantized number of charges on the QD.
Combining the above equations, an expression for the electrostatic energy is obtained

$$U_n = \frac{[n|e| + C_L V_L + C_g V_g + C_R V_R]^2}{2C} \tag{2.7}$$

In order to be consistent with a semiconductor QD picture, the orbital spacing energy $\xi_n$ must be introduced. It comes from a quantum-mechanical single particle spectrum and it is assumed to be independent of the electrostatical interactions.

$$U_n = \frac{[n|e| + C_L V_L + C_g V_g + C_R V_R]^2}{2C} + \sum_{t=1}^{n} \xi_t \tag{2.8}$$

If one is to approximate the QD with a infinite potential well, $\xi_n$ is strongly correlated with the level and size of the QD [7].

$$\xi_n \propto \frac{n^2}{L^2} \tag{2.9}$$

When studying transport properties, it is specially useful to define the electrochemical potential $\mu_n$. It represents the energy needed to add the $n$-th charge considering there are already $n-1$ charges on the dot.

$$\mu_n = U_n - U_{n-1} \tag{2.10}$$

Further on, the *addition energy* is defined as a difference between neighbouring electrochemical potentials

[7] In our QDs, the shape, the size, the effective mass etc. of the QD is not exactly known, therefore no analytical calculations for the single-particle spectrum can be made

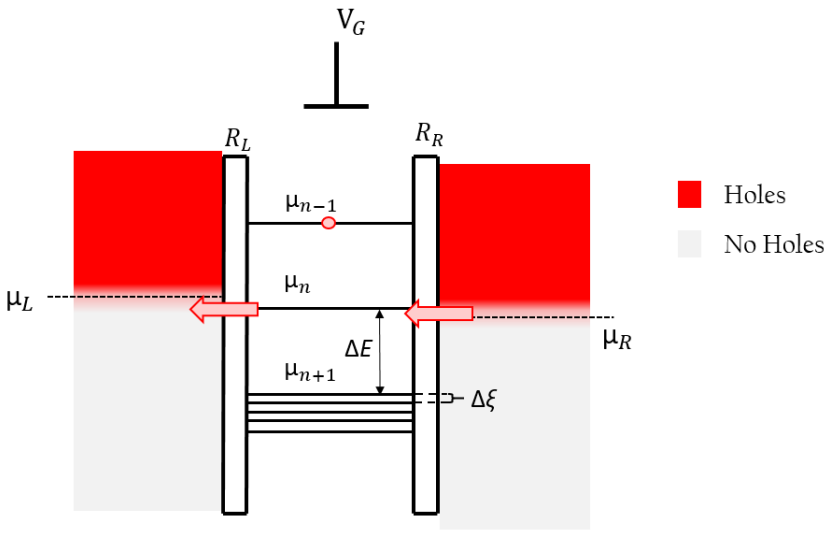


Figure 2.3: Electrochemical potentials diagram for a SQD device

$$\Delta E = \mu_{n+1} - \mu_n = \frac{e^2}{C} + \Delta\xi_n \tag{2.11}$$

where $e^2/C$ comes from a purely classical model of a QD and is referred to as *charging energy* .

### 2.1.2 Transport spectroscopy of a SQD device

Let us consider a situation in which a voltage is applied so that

$$\mu_R < \mu_n < \mu_L \tag{2.12}$$

for some $n-th$ level of the QD. The electrochemical potential $\mu_n$ is aligned in a small bias window $V_b = \mu_R - \mu_L \to 0$. The system is in non-equilibrium and resonant hole tunneling occurs ($\mu_R \to \mu_n \to \mu_L$) as depicted in Figure 2.3.

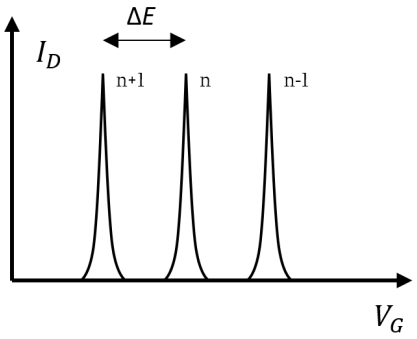


Figure 2.4: $I_D$ vs $V_G$ characteristic line of a SQD device

The next electrochemical potential $\mu_{n+1}$ is energetically at a distance given by the addition energy :

$$\Delta E = \mu_{n+1} - \mu_n = \frac{e^2}{C} + \Delta\xi_n \tag{2.13}$$

Due to the Fermi distributions at cryogenic temperatures ($< 1K$)

$$f_h = 1 - f_e(\mu_{n+1}) = 1 - \frac{1}{e^{\frac{-\Delta E}{k_B T}} + 1} \tag{2.14}$$

$$k_B T << \Delta E \tag{2.15}$$

the probability $f_h$ that the hole, coming from a lead, will overcome the addition energy is practically zero. Transport through the $n-th$ QD level is thus the only one allowed, with one hole tunneling at a time.
In QDs of $\approx 100nm$ size, the addition energy is mainly due to the charging energy while the single-particle term has a considerably smaller influence. Since the charging energy effectively comes from the electrostatical repulsion of a QD charge, this phenomenon is often refered to as *Coulomb blockade* .
As the voltage $V_G$ is sweeped, different electrochemical potentials get aligned in the bias window. Lorentzian shaped spectral lines -*Coulomb peaks* are measured in the current transport. From the position of the spectral lines the addition energy can be calculated.

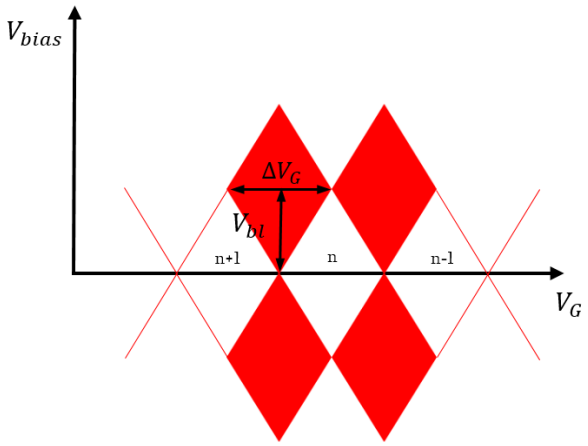


Figure 2.5: Stability diagram of a SQD showing the characteristic *Coulomb Diamonds* pattern

Making a two-dimensional sweep $V_b$ *vs* $V_G$ builds a pattern known as stability diagram as shown in Figure 2.5 with red color presenting the region where transport can take place.
The relationship between the bias voltage $V_b$ and the electrochemical potentials $(\mu_L, \mu_R)$ is assumed to be.

$$eV_b = (\mu_R - \mu_L) \tag{2.16}$$

With a careful sweep of the gate voltage, the capacitive coupling to the gate can be extracted.

$$\Delta\mu_n = \alpha(e\Delta V_G) = (\mu_R - \mu_L) \tag{2.17}$$

It reveals the linearity between $V_g$ and the electrochemical potential $\mu_n$ commonly known as *level arm*.

$$\alpha = \frac{\partial\mu}{\partial V} = \frac{V_{bl}}{\Delta V_G} \tag{2.18}$$

$V_{bl}$ and $\Delta V_G$ are explained in Figure 2.5.

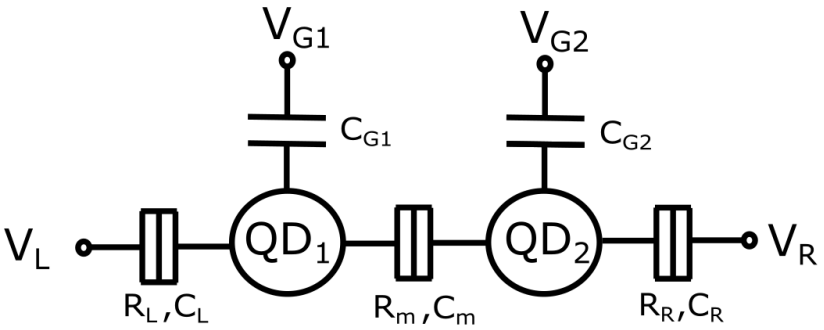


Figure 2.6: Semi-classical model of a DQD

## 2.2 Double Quantum Dot

A DQD consists of a two QDs coupled by a tunneling barrier, characterised by a resistivity $R_m$ and a capacitance $C_m$ as shown in Figure 2.6. Using the assumptions from the CIM 2.1.1, the electrochemical potentials are defined as (full derivation for electrons in[8])

$$\begin{aligned}\mu_1(n,p) &= U(n,p) - U(n-1,p) \\ &= (n-\frac{1}{2})E_{C1} + pE_{Cm} + \frac{1}{|e|}(C_{G1}V_{G1}E_{C1} + C_{G2}V_{G2}E_{Cm})\end{aligned} \tag{2.19}$$

$$\begin{aligned}\mu_2(n,p) &= U(n,p) - U(n,p-1) \\ &= (p-\frac{1}{2})E_{C2} + nE_{Cm} + \frac{1}{|e|}(C_{G1}V_{G1}E_{Cm} + C_{G2})\end{aligned} \tag{2.20}$$

$$E_{C1} = \frac{e^2}{C_1}\left(\frac{1}{1-\frac{C_m^2}{C_1C_2}}\right) \tag{2.21}$$

[8] Wiel et al., 2002.

$$E_{C2} = \frac{e^2}{C_2}\left(\frac{1}{1-\frac{C_m^2}{C_1 C_2}}\right) \tag{2.22}$$

$$E_{Cm} = \frac{e^2}{C_m}\left(\frac{1}{\frac{C_1 C_2}{C_m}-1}\right) \tag{2.23}$$

where $n$ is the number of holes on $QD_1$ and $p$ is the number of holes on $QD_2$

Important to emphasise is the influence of the electrostatic coupling energy $E_{Cm}$ which strongly depends on the inter-dot capacitance $C_m$ and substantially influences the DQD transport properties. It represents a change in the electrostatical energy of a one dot if a charge is added to the other.
In practice, tunable inter-dot coupling controlled by a gate is desirable and will be demonstrated further in the thesis.

### 2.2.1 Low Bias Regime

The low bias regime assumes a finite bias close to zero, $V_b = \mu_L - \mu_R \approx 0$ (Experimentally it's usually $\approx 100\mu V$). Transport occurs only if both of the DQD electrochemical potentials are aligned in the bias window (see Fig. 2.7)

$$\mu_R < \mu_{1,n} \approx \mu_{2,p} < \mu_L \tag{2.24}$$

By sweeping both gate voltages and measuring the transport, a *charge stability* diagram is constructed. The characteristic lines of the diagrams reveal the coupling between the dots as shown in Figure 2.8 .
For $C_m \to 0$ $(a)$, the dots are in a completely decoupled regime. The voltage applied at dot $QD_1$ (or electrostatic energy) and the hole occupation number has no influence on the dot $QD_2$ and vice versa. The rectangle corners

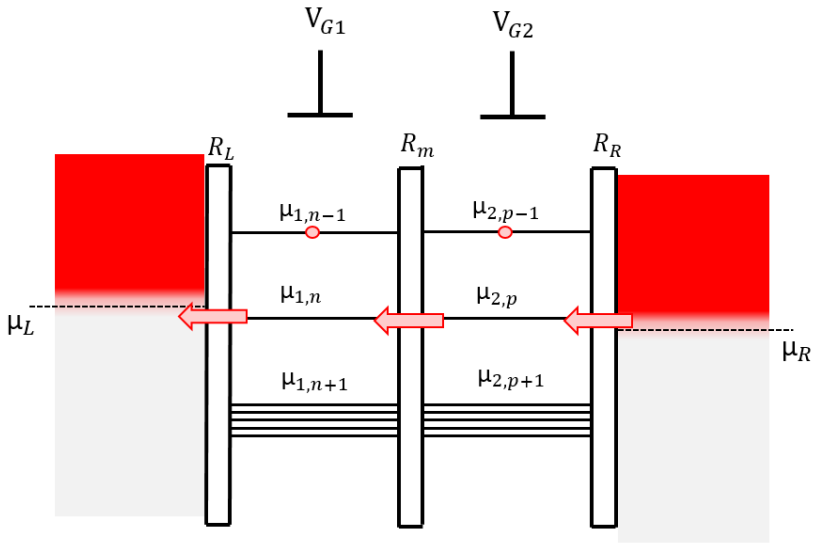


Figure 2.7: Electrochemical potentials diagram for a DQD

represent the situation when the electrochemical potentials are aligned in the bias window and transport occurs.
On the contrary, for strong inter-dot coupling $(c)$, the DQD effectively behaves as a one big SQD.
An interesting situation appear for an intermediate coupling $(b)$. The electrochemical potentials are coupled by the electrostatical coupling constant $E_{Cm}$ given by equation 2.23. The charge stability diagram reveals a hexagon pattern where two types of transport cycles occur, as shown in Figure 2.9 .

Upper right triple point : $(n,p) \rightarrow (n,p+1) \rightarrow (n+1,p) \rightarrow (n,p)$
While for the lower left : $(n+1,p+1) \rightarrow (n,p+1) \rightarrow (n+1,p) \rightarrow (n+1,p+1)$.
By reducing the inter-dot coupling two of the triple points merge into the one. Whence, a similar diagram like the one shown in 2.8$(a)$ would be observed.

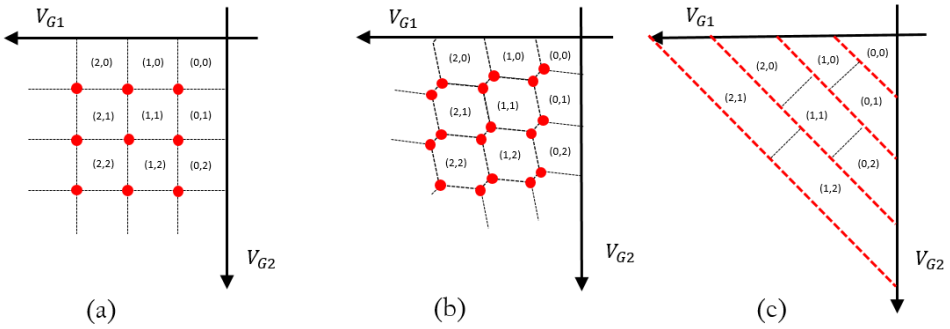


Figure 2.8: Illustration of a charge stability diagram for a a) decoupled b) intermediately coupled and c) strongly coupled DQD

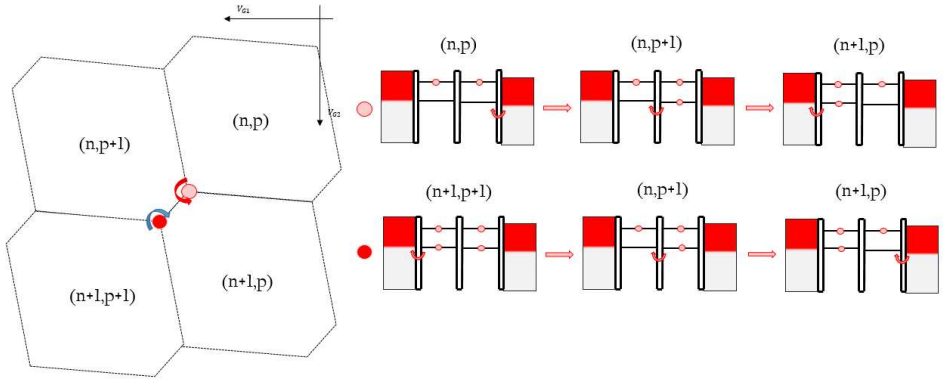


Figure 2.9: Illustration of the transport cycles for intermediate coupling together with the corresponding electrochemical potential diagrams

### 2.2.2 High Bias Regime

If the bias is increased, triple-points evolve into triangles as shown in Figure 2.10. Since a bias window is opened, transport can occur for different types of electrochemical potential alignments in the dots. The detuning parameter $\epsilon$ is introduced as a measure of misalignment between the electrochemical potentials of the two dots.

$$\epsilon = \mu_{1,n} - \mu_{2,p} \tag{2.25}$$

The maximal detuning for which transport occurs is equal to the applied bias $\epsilon_{max} = V_b$. On the charge stability diagram it represents the tip of the triangle as depicted in the purple window of Figure 2.10. Even though levels are misaligned there is still a measurable current since transport is induced by phonon scattering (indicated with a dashed line). With the same logic, the base of the triangle represents the situation for which the detuning is zero.
From the triangle dimensions, the level arm of each of the gates is extracted.

$$\alpha_1 = \frac{V_{bias}}{\Delta V_{G1}}; \qquad \alpha_2 = \frac{V_{bias}}{\Delta V_{G2}} \tag{2.26}$$

With a sufficiently large bias, multiple energy levels align in the bias window and participate in the transport. However, one has to be aware that transport occurs only through one of the states at a time, since Coulomb blockade prohibits parallel transport channels. The new levels introduced into the bias window come from the single-particle QD spectrum and are referred to as *excited states*. In Figure 2.11 different colors are used to denote transport through ground state (brown) and excited state (red). Pink color is used to point out the region of current induced by phonon absorption/emission. The overlapping of the triangles point out that in respect to Figure 2.10, the DQD is slightly more decoupled.

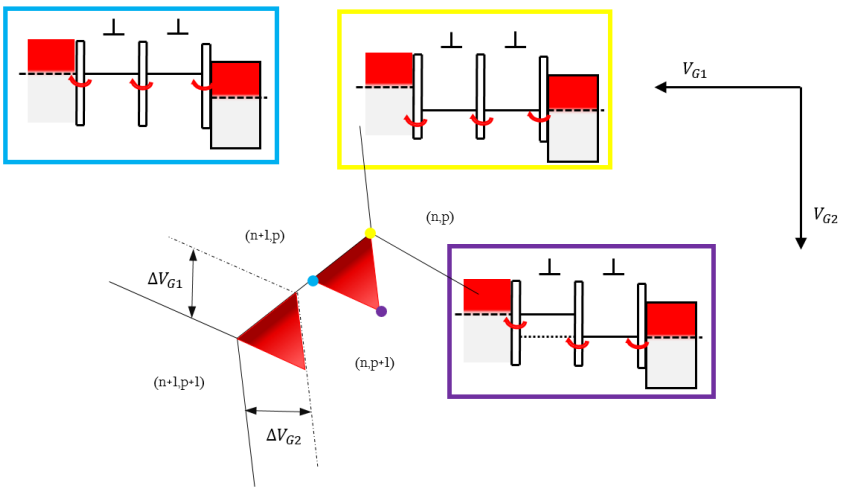


Figure 2.10: Illustration of bias triangles measured at triple points for the high bias regime.

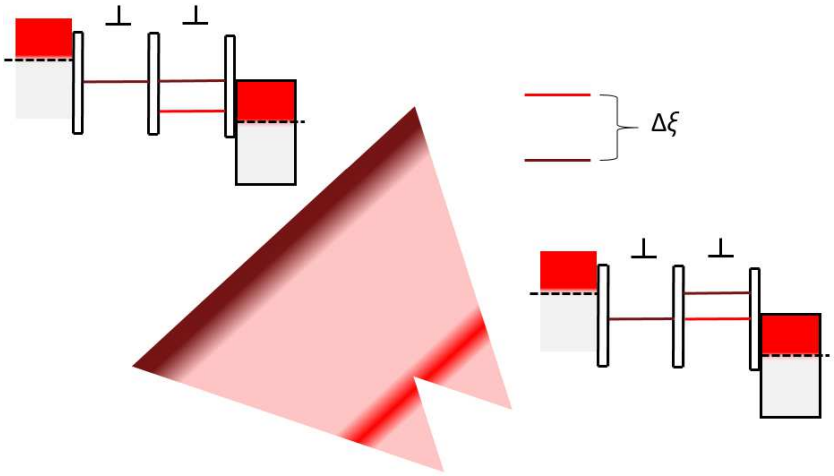


Figure 2.11: Bias triangles illustrating transport through the ground and excited state

### 2.2.3 Spin dependent transport

The Spin is an intrinsic property of an electron(hole) coming from it's angular momentum and can obtain two values which we write as a spin-up $|\uparrow\rangle$ and spin-down $|\downarrow\rangle$. In a DQD device two particle spin interaction are of interest. The spatial wave-function describing the two particle state has two solutions, a symmetric and an anti-symmetric one. For a symmetric spatial distribution the spin distribution is anti-symmetric and the formed state is called *singlet*. In an analog manner, asymmetric spatial distribution has symmetric spin states, leading to the three *triplet's* states. In a singlet state the net spin of a system is zero, while the triplet states have a final total spin momentum equal to one.
Initially degenerate, the triplet energy state splits under the influence of a magnetic field [9].The singlet and triplet states are summarized below.

$$|S\rangle = \frac{|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle}{\sqrt{2}}, |T_0\rangle = \frac{|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle}{\sqrt{2}}, \ |T_+\rangle = |\uparrow\uparrow\rangle, \ |T_-\rangle = |\downarrow\downarrow\rangle \quad (2.27)$$

Tunneling from a singlet to a triplet is a forbidden process (when hyperfine interaction and spin-orbit are ignored) due to Pauli exclusion principle. The electrochemical potentials of a DQD can be aligned in a way to favor the exclusion principle so that current flowing through the device is blocked. By now, it's a commonly observed phenomena refereed to as *Pauli Spin Blockade* (PSB).

An example of PSB for zero detuning is shown in at Figure 2.12 (a). To simplify, I denote the starting charge configuration to be $(n, p) = (1, 0)$.
$QD_2$ has no charge and it can host both triplet and singlet states of charge configurations $T(1,1), S(1,1)$ respectively. When a triplet state $T(1,1)$ is loaded into $QD_2$ transport is blocked since tunneling to a $S(2,0)$ is not allowed. There is still a reduced current flowing due to spin leakage but a significantly smaller current will be measured. The reduced baseline current is represented by a bleached pink color (see Fig. 2.12 (a)). At higher detuning,

[9]It's important to point out, that very recently, triplet splitting at zero magnetic field has been reported in Ge Hut wire system (Georgios Katsaros, 2019). For the purpose of this thesis it is however not relevant and spin triplet degeneracy is assumed.

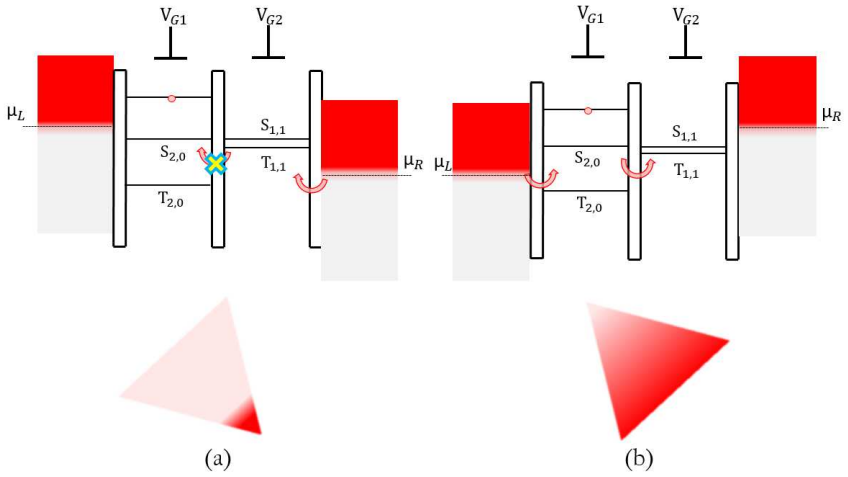


Figure 2.12: Schematic of electrochemical alignments resulting in a spin blockade a) When PSB takes place the current at the base line of a triangle is reduced. For the opposite bias direction b) PSB is lifted.

close to the tip of triangle, $T(2,0)$ might enter the bias window and blockade is lifted. If the bias is reversed as shown in Figure 2.12 (b), holes tunnelling from the lead to the $QD_1$ will by definition go through the $S(2,0)$ state, as the T(2,0) is much higher in energy and thus transport is not blocked. At higher detuning there will be slightly less current due to the misalignment of the electrochemical potentials.

The mechanism described makes a DQD device an efficient system for realising a spin qubit. The spin state of holes can be coherently manipulated by using a microwave electrical field via the EDSR mechanism which has been demonstrated using holes in both Si and Ge.
The demonstration of a qubit in a DQD device is still a major research challenge and is not the purpose of this Thesis. More interested readers are instructed to read ref.[10].

[10]Watzinger, Kukučka, et al., 2018.

# 3 Fabrication and Measurement Setup

Since DQDs are nanometer size devices, a cleanroom environment is essential for the device fabrication. Therefore, the DQDs reported in this thesis are fabricated in the IST Austria Nanofabrication facility ranging from class 10000 to 100.

### 3.0.1 Si-Ge Epitaxy

Silicon and Germanium are group IV semiconductors; they both occur in a diamond-like lattice structure with Si having a lattice constant of $0.543nm$ and Ge of $0.568nm$. Their similar physical and chemical properties make them a good match for epitaxial crystal growth[1].
Epitaxialy grown Si-Ge-Si material leads to a type-II energy band alignment[2]. The confinement potential for holes is created in the Ge while electrons are localised in the Si conduction band as illustrated in Figure 3.1. Ignoring the split-off band, for bulk material, the Ge valence hole band is double degenerate. Transport can occur through two different types of holes - heavy holes (HHs) and light holes (LHs), distinguished by a different in the effective mass. The HH, LH band degeneracy is lifted by inducing strain and carrier confinement (see Fig. 3.4); both of which are present in HW material system. It has been shown[3] that localised holes in HWs are almost of pure HH character.

[1] SiGe alloys are common material in industrial CMOS applications (Takagi, 2011)
[2] Yakimov et al., 2006.
[3] Watzinger, Kloeffel, et al., 2016.

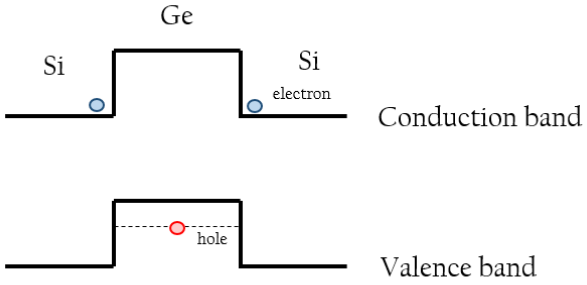


Figure 3.1: Si-Ge-Si energy band alignment

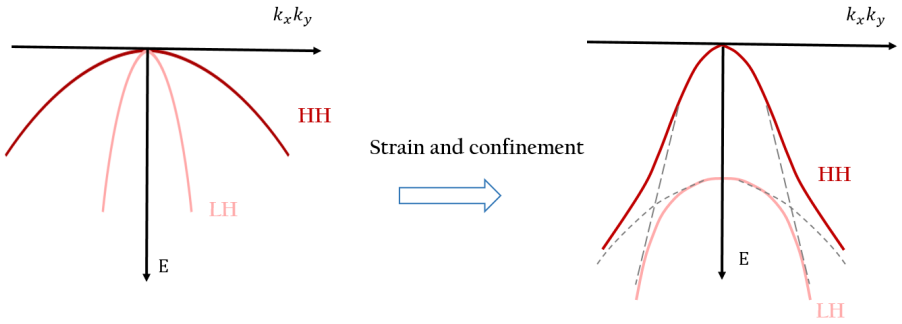


Figure 3.2: Illustration elucidating the lifting of the valence band degeneracy in Ge

## 3.1 Germanium Hut Nanowires

Germanium Hut Wires are grown on a Si Wafer using Molecular Beam Epitaxy (MBE). MBE machines are capable of achieving ultra high vacuum (UHV) environments , needed for mono-layer precision material growth. HWs used in the thesis were grown by the group of J.J Zhang from the Chinese Academy of Sciences in Beijing; more details about the material system can be found in ref.[4]

The silicon wafer is loaded into the MBE chamber and is kept heated at temperature of $\approx 500°C$. Vaporised Ge is introduced into the chamber

[4]Zhang et al., 2012.

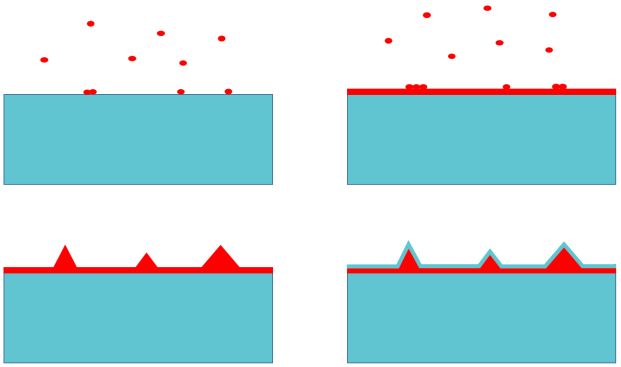

Figure 3.3: Schematic visualisation of Stranski-Krastanov growth, Ge (red) forms clusters during the deposition due to the lattice mismatch. After the formation of the Ge nanostructures a thin layer of Si (blue) is grown in order to protect Ge from oxidation.

and it starts to accumulate at the Si surface by matching it's lattice constant. After reaching the critical thickness of a 2-3 monolayers (MLs), growth continues in the form of 3D Ge islands, the so called *hut clusters*. This is a well known process called *Stranski–Krastanov growth*, physically coming from the strain effect due to the different lattice constants[5]. In the next step, the substrate is *in-situ* annealed during which clusters evolve into the wires along the [001] or the [010] crystallographic direction. The typical length and density of the HWs depends strongly on the annealing time and temperature. Needless to say, the uniformity also varies across the wafer. Typical HWs used in the thesis are around a micrometer ($\approx 1\mu m$) long. By using Transmission Electron Microscopy (TEM) for their height and a width was estimated to be $1.8nm$ and $18nm$, respectively[6].

After the growth, several nanometers of a Si capping layer are deposited to prevent Ge from oxidation when exposed to the atmosphere.

During the writing of the thesis, pre-pattern grown HWs have been reported[7]. Such site controlled HWs might open the path to more scalable devices.

[5] Baskaran and Smereka, 2012.
[6] Watzinger, 2018.
[7] Gao, 2020.

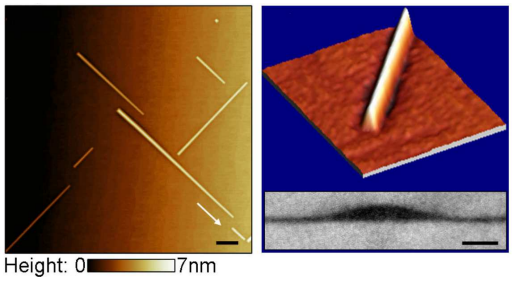


Figure 3.4: AFM scan and TEM image of a Ge hut wires as seen in [4]

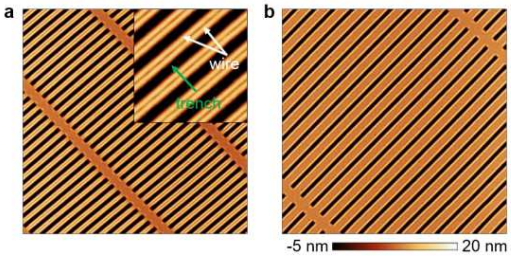


Figure 3.5: AFM image of pre-pattern grown hut HWs as seen in [7]

## 3.2 Device Fabrication Process

The fabrication starts with imaging the sample, on top of which HWs are located. Imaging is done using a Scanning Electron Microscope (SEM) with an electron beam of $2kV$ and $6.3pA$ of current. Since HWs are exposed to the electron beam, this step could contribute to the observed *charge noise* in a finished device. Therefore the shortest possible scanning times are desired (dwell time of $\approx 10\mu s$). In future research, SEM imaging could be avoided by using an Atomic Force Microscopy (AFM) instead.

From the SEM image, the HW location is determined by using position markers which have been previously created. Using the *K-layout* computer software, a DQD device layout is designed and routed subsequently to the bonding pads. Figure 3.6 shows a SEM image of HWs and a DQD layout aligned with one of the HWs. The process of the design layout can be abbreviated by an using Auto-routing software currently developed at IST.

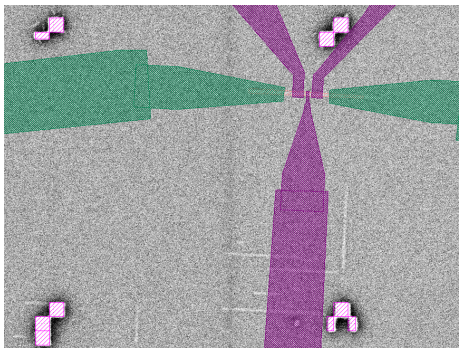

Figure 3.6: Snapshot of a device designed in a K-layout software and aligned with one of the HWs using the position markers visible in the four corners of the SEM picture. The green structures will become the source and drain contacts, the purple the gates.

### 3.2.1 Source/Drain - Ohmic Contacts

To prepare the sample for the electron-beam lithography (EBL) step, it is coated with a 2% 950K polymethyl methacrylate (PMMA) resist and spinned at 4000 $rpm$ for 60 $seconds$[8]. At the hot plate the sample is baked at 180°$C$ for 5 $minutes$ in order to harden the resist.
EBL exposure is done by using the RAITH EBPG5150 machine with a beam voltage of 100$kV$ and a dose of 540$\mu C \setminus cm^2$ [9]. The resist development consists of dipping the sample for 30 seconds in a mixture of distilled water ($H_2O$) and isopropanol (IPA), $H_2O : IPA = 30 : 70$. To stop the development, the sample is dipped in pure IPA solution for a period of $\approx$ 40 seconds. After drying the sample with a nitrogen gun, the source-drain pattern should be visible even with the naked eye.
Since the sample is in the contact with the atmosphere, few nanometers of natural Si oxide build on top of the Si cap. The Si oxide acts as a insulator and it prohibits the formation of low resistance contacts. To remove the Si oxide, the sample is dipped in a buffered hydrofluoric acid (HF) for a period of 10 $seconds$. 10 $seconds$ of a dip in a distilled water are afterwards needed

[8] Variations with recipes using 3% and 4% PMMA were also tried. However, the recipe with 2% PMMA was most successful in achieving fabrication accuracy of 20$nm$ which is close to the EBL limit.

[9] A dose of 600$\mu C \setminus cm^2$ was used for structures bigger than a 2$\mu m$

to remove the highly acid HF traces on the sample.
To prevent the formation of a new natural oxide, the sample is loaded in a high vacuum (HV) evaporator immediately after the HF dip. Using the Plassys MEB 550S evaporator, 25$nm$ of Platinum is deposited. Lift-off is done in the dimethyl sulfoxide (DMSO) solution which is heated in a hot bath at 75°$C$ for a period of 60 $minutes$. In Figure 3.7 fabrication steps are schematically shown to give the reader a better overview. Successful source-drain fabrication can be inspected down to 500$nm$ using the optical microscope.

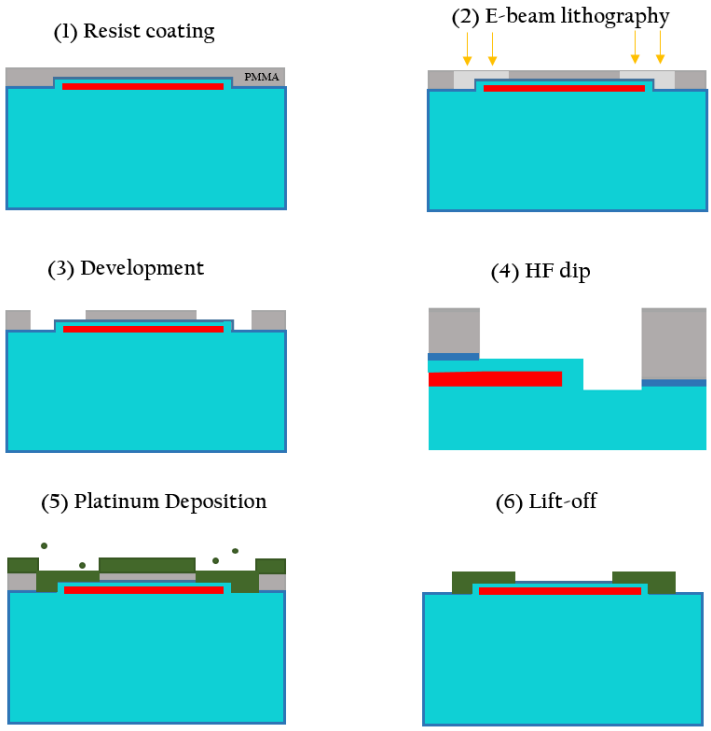


Figure 3.7: Source drain fabrication steps. The red color presents Ge hut wire, blue the Si, dark blue the Si native oxide, gray the PMMA and green the deposited Pt.

### 3.2.2 Gate contacts

The formation of the gate oxide has been implemented with two different approaches. In the first approach aluminium oxide $Al_2O_3$ is formed using the atomic layer deposition (ALD) machine while in other approach the aluminium gate oxide is formed thermally. The thermal oxide approach has shown to be more successful in obtaining good quality DQD devices, therefore all of the measurements presented in the thesis are done with this approach.

In the same way as for the source/drain recipe, the sample is coated with a PMMA 2% resist and the gate layout is exposed via the EBL machine. After development, 25$nm$ of Al is deposited. The average lift-off time used was 90$minutes$, however it can vary from sample to sample. To form the thermal Al gate oxide, the sample is baked at 150°$C$ for 5 $minutes$ on a hot plate.

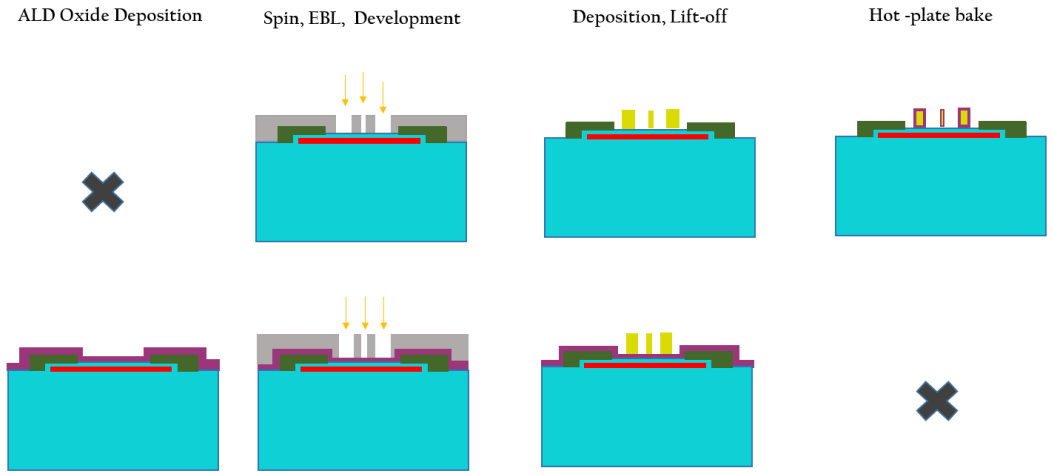


Figure 3.8: Schematic showing the fabrication steps for the two different oxide approaches. In a top row, aluminum gates are colored yellow and thermally formed Al oxide is colored purple. In a bottom row, Al gates are colored yellow and ALD deposited oxide is colored purple.

In the ALD oxide approach, the oxide is deposited before the gate exposure. Since the EBL exposure is done using a 100kV electron beam it could lead to substantial defects in the oxide. It is believed that the thermal oxide showed

more successful results because the oxide formation is done after the EBL exposure step and oxide charging is avoided. However such a strong claim need a stronger evidence, which is why some of the samples where sent to an external partner to investigate a hot tip type of lithography where no electron beam is used. No results have been so far obtained with this technique.
To enhance the device quality, in a last step, the sample is loaded in a MILA-5000 MINI-LAMP rapid thermal annealing (RTA) machine. It is annealed for 15 *minutes* at 300°C with under flow of N2, H2 gas mixture. The RTA step was introduced recently and the optimal tuning of the temperature, duration and gas mixture parameters is not yet clear. So far there is an indication that annealing at 400°C leads to higher leakage currents.

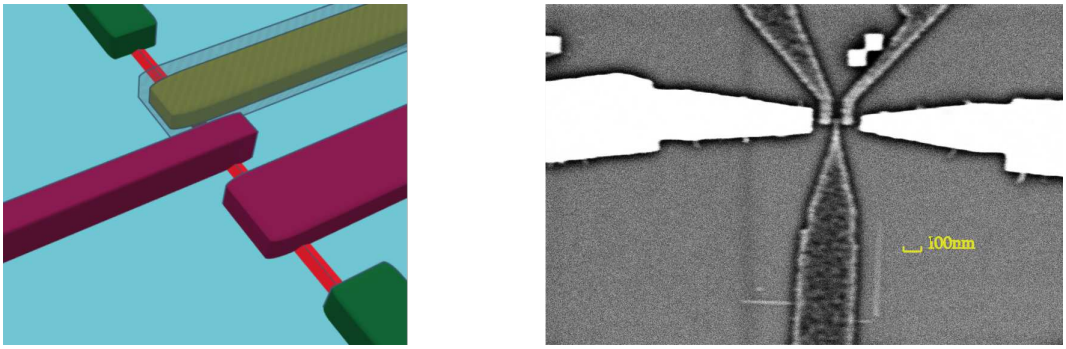


Figure 3.9: On the left, artistic rendering of a finished device with coloring corresponding to the Figure 3.8. On the right, SEM scan of a finished device.

## 3.3 Measurement Setup

The presented measurements were done using two different types of cryostats, depending on the availability and confidence in the sample quality. Both of the cryostats use helium isotopes $He^3$ and $He^4$ to reach temperatures below $1K$.

### 3.3.1 Heliox He3 refrigator

The Oxford Heliox Helium 3 refrigerator is capable of achieving temperatures down to $250mK$. It is based on a single shot pumping of $He^3$ . The gaseous $He^3$ is brought in thermal contact with liquid $He^4$ at about $1.5 - 2K$. Liquid $He^4$ base temperature is $4K$ and it can be cooled to $\approx 1.5K$ by reducing it's the pressure using a scroll pump. At $1.5K$, $He^3$ undergoes a phase transition to a liquid phase and starts to accumulate in the $He^3$ pot. Using a sorption pump, the pressure of the liquefied $He^3$ is reduced and thereby temperatures of $250mK$ are obtained. After $\approx$ 12h of pumping on $He^3$, all of the $He^3$ gets back in gaseous form and the whole cycle must be repeated.

### 3.3.2 Blue Fors Dilution Refrigerator

The BlueFors LD-250 EO He- 3/He-4 dilution refrigerator uses a $He^3/He^4$ mixture and it is capable of achieving a base temperature of $10mK$. It is based on a principle in which $He^3$ floats on diluted $He^4$ having a small percentage of $He^3$. By removing the $He^3$ from the diluted mixture using a turbo pump , pure $He^3$ is forced to go from the concentrated phase to the dilute phase. It is a endothermic process which removes heat from the mixing chamber environment. After leaving the mixing chamber $He^3$ is purified, condensed and the whole cycle repeats. Cooling down a sample to base temperature can last up to 12h. However, once cooled the sample can stay at the base temperature for very long periods of time, with minimal temperature oscillations.

Figure 3.10: HelioxVL refrigerator used for the reported measurements.

Figure 3.11: Blue-fors dilution refrigerator used for the reported measurements

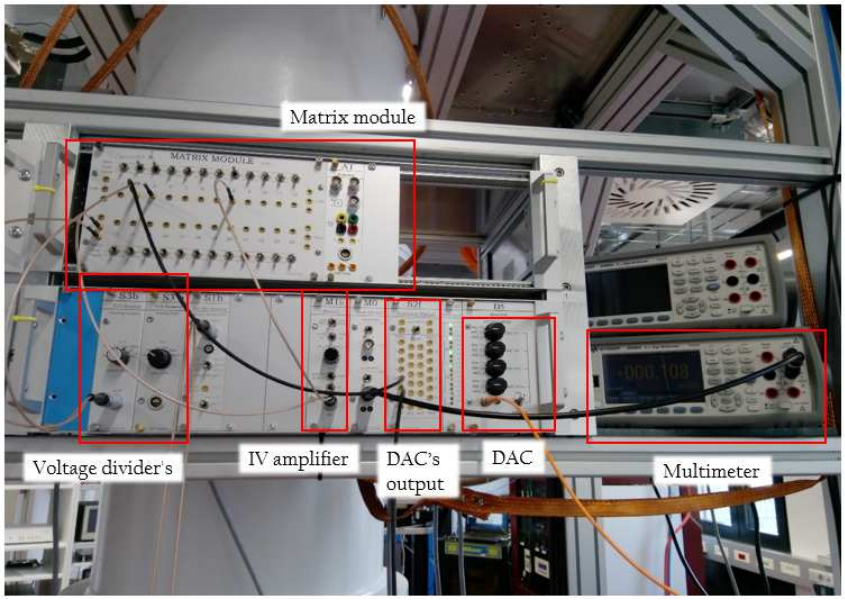


Figure 3.12: Electronic setup used for the measurements

### 3.3.3 Electronics

The sample is glued on a printed circuit board (PCB) (designed at IST) with a silver paste and it is bonded using the 5330 thin wire wedge bonder. The PCB is connected to the control and measuring units, through purely DC lines using a fisher cable. The matrix module is used as an electronic jumper for choosing the wanted measurement lines. The applied voltage signals are controlled through a digital-analog-converter (DAC) system developed at TU Delft. The DAC resolution is initally $61\mu V$ and it can be reduced to the $nV$ range by voltage dividers. The measured current is amplified using a current to voltage (IV) amplifier with a gain up to $10^9$ after which the voltage is measured using the Keysight 34465A digital multimeter. The electronics are controlled through a personal computer connected to the DACs with a fibre optical cable and with the multimeter through a USB bus. The measured data is recorded using commercially available *Labber* and free *Qcodes* softwares.

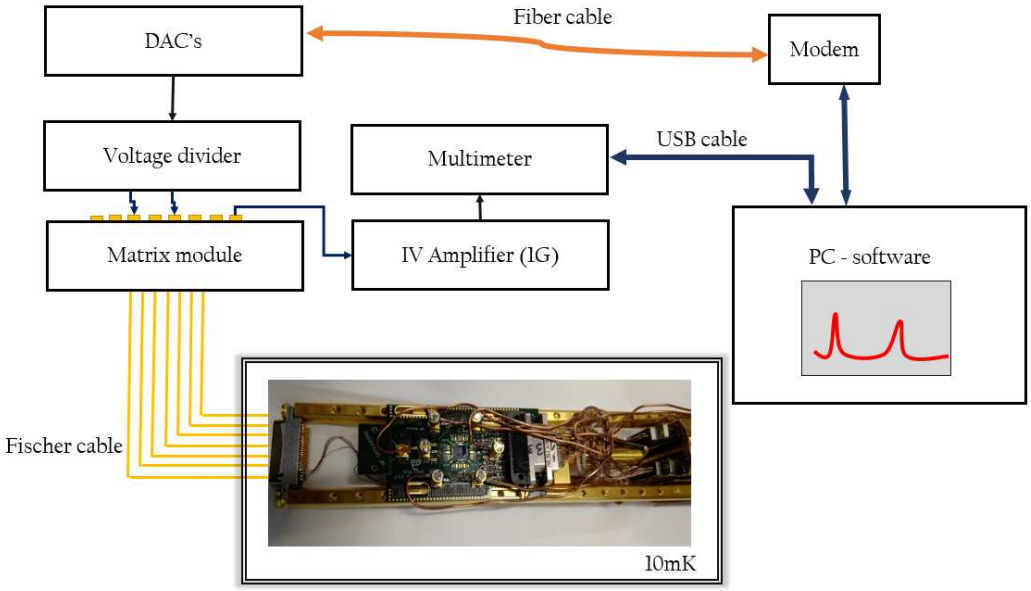


Figure 3.13: Schematics explaining the measurement setup

# 4 Measurement Results

## 4.1 Device design

My starting DQD device design is a follow-up of a design previously realized by Hannes Watzinger. It allows the realisation of a DQD in a HW with the use of only two gates. No additional barrier gates are needed as the dots form below the gates, thus making the layout look very simple. Such a sample allowed the realisation of the first hole spin qubit in Ge.
In Figure 4.1 the starting device layout studied in this thesis is presented. The gate width of $75nm$ was taken from Hannes Watzinger's design and was not altered. The gate to source/drain (S/D) lengths of $50 - 60nm$ are used as tunneling barriers and are also not investigated in detail. The gate to gate (GtG) distance represents the electrostatical barrier in between the QDs and it will be investigated in terms of inter-dot coupling and charge noise.

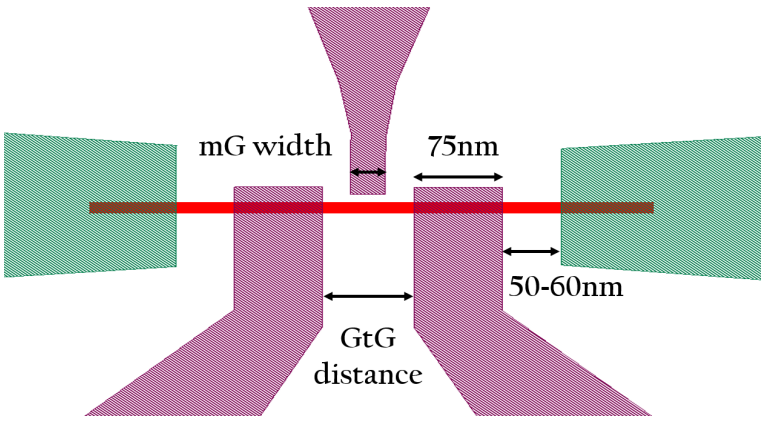


Figure 4.1: Layout of a general case DQD device. The S/D contacts are colored green and the gates purple.

The middle gate (mG) is introduced in an effort to demonstrate tunable inter-dot coupling. The width and positioning of the mG will be altered and measurement results will be discussed.

## 4.2 Gate to Gate distance investigation

### 4.2.1 Sample MJ_3_S32

Here the first success in implementing a DQD using an Al thermal oxide as gate material is demonstrated. Triangles appear at the corners of a rectangular grid (see Fig. 4.3), denoting the decoupled behaviour for a GtG distance of $110nm$.

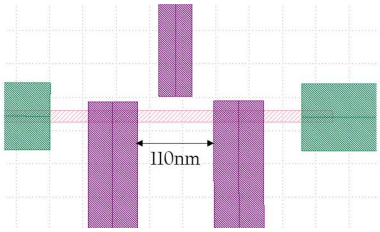


Figure 4.2: DQD layout device used for the measurement shown in Figure 4.3. The middle gate influence was not investigated and therefore its dimensions are not relevant.

The rectangle size can vary from one charge configuration state $(n, p)$ to the next $(n, p+1)$, implying that the capacitance and therefore the charging energy (eq. 2.11) is function of the charge configuration. The relatively ordered structure of the stability diagram on the left figure gives an indication to continue using the thermal oxide approach. However, the considerable amount of charge noise revealed at finer scans (right figure) makes such a DQD device inadequate for inspecting the excited states which are important for further experiments.

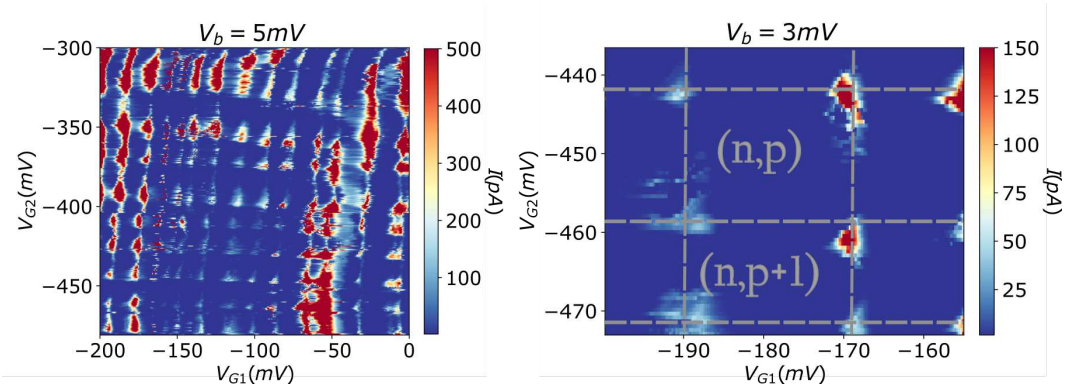


Figure 4.3: Charge stability diagrams of a device fabricated from the sample MJ_3_S32. The plots show the current flowing through the DQD versus the gate voltages $V_{G1}$ and $V_{G2}$. VG2. On the left, the stability diagram taken for a wide range of gate voltages is shown. On the right, the measurement taken on a smaller range is shown, where with a finer gate sweep a poor device stability can be concluded. $T = 250mK$

### 4.2.2 Sample Chi2_P1_12

To improve the device in terms of charge noise, the GtG distance is reduced to $50nm$ in the next sample. Due to a statistical nature of defects in semiconductors, a smaller GtG distance should yield a more stable device. In addition, a RTA step[1] is introduced as a experimental approach to enhance the semiconductor crystal quality.

The charge stability diagrams in Figure 4.5 show clear evidence of charge noise reduction.

In the left figure, two inter-dot coupling regimes are observed. The coupled and decoupled regime, depending on the charge configurations (n,p). For a smaller number of charges in the QDs, the two dots are largely decoupled. When a higher voltage (in absolute value) is applied, the QDs carry more charges and strong inter-dot coupling is observed. This indicates that voltage applied at the gates influences the capacitance of the inter-dot barrier. A potential profile of the mentioned assumption is shown schematically in Figure 4.6.

[1] Annealling at $300°C$ for 15 minutes under 100% $N_2$ flow at 100 sccm.

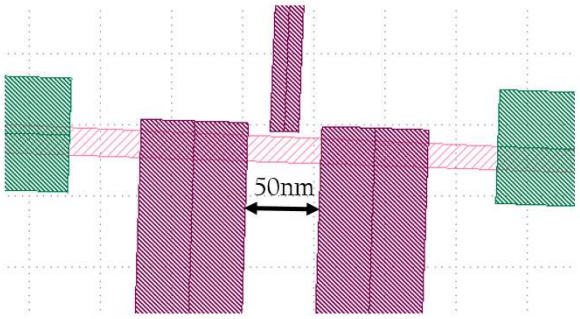


Figure 4.4: Layout of a DQD device used for a measurement shown in Figure 4.5.

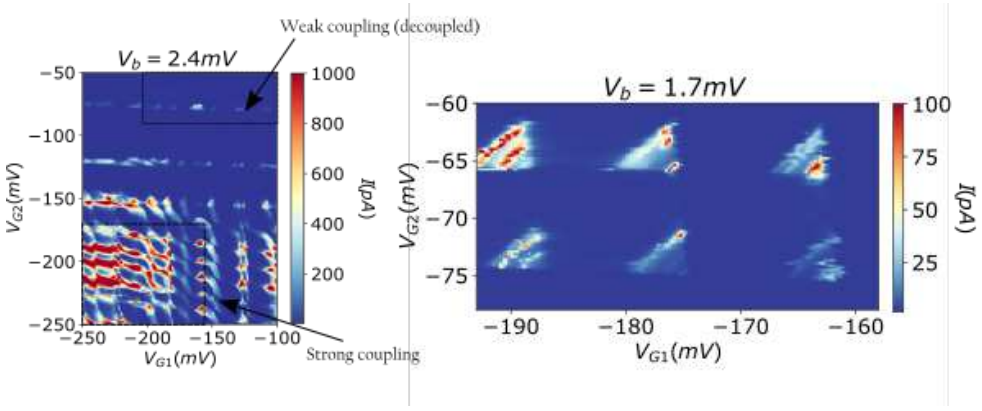


Figure 4.5: Charge stability diagrams of a device fabricated from the sample Chi2_P1_12. Wide range scan is shown on the left and a zoomed in scan of a decoupled area on the right. A clear reduction of charge noise in comparison to Figure 4.3 can be seen. $T = 250mK$

The finer scan reveals rather stable triangles in which excited states can be observed and level arms extracted. Using equation 2.26 and extracting the $\Delta V_{G1}, \Delta V_{G2}$ from Figure 4.7, level arms are calculated:

$$\alpha_1 \approx 0.34 \; \alpha_2 \approx 0.425$$

The detuning line is taken so that $\epsilon$ is zero at the current baseline.

$$\epsilon(V_{G1}, V_{G2}) = (\mu_1 - \mu_{1g}) - (\mu_2 - \mu_{2g}) = e[\alpha_1(V_{G1} - V_{G1g}) - \alpha_2(V_{G2} - V_{G2g})]$$

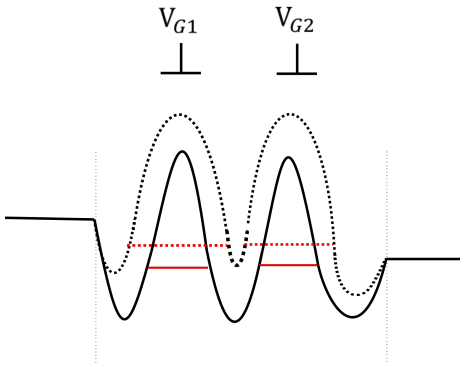


Figure 4.6: Schematic of a DQD potential profile for different gate voltage configurations. The dotted line represents the strong coupling regime. By applying more (absolute) voltage at the gates, inter-dot coupling is influenced as shown in a measurement in Figure 4.5

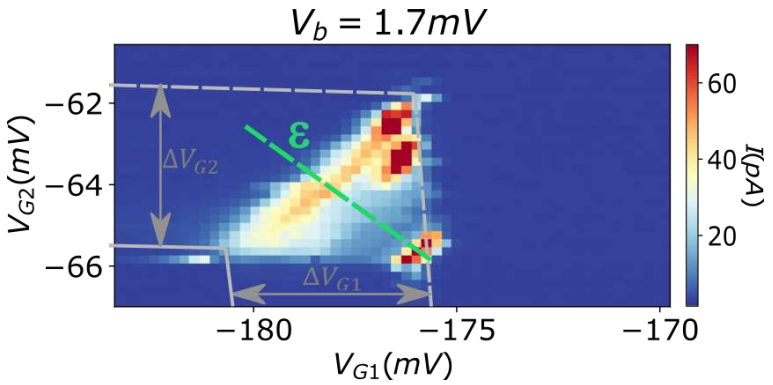


Figure 4.7: Current vs $V_{G1}$ vs $V_{G2}$ showing a pair of merged bias triangles. It was used to extract the level arm factors and extract the detuning line cut.

where $\mu_{1g}$ and $\mu_{2g}$ represent the electrochemical potentials at the baseline of the triangle. From Figure 4.8, the energy difference of $\approx 1.4meV$ between the ground and excited state is obtained.

This sample was measured in the HelioxVL system where the measurement time is limited and therefore the middle gate influence was not investigated.

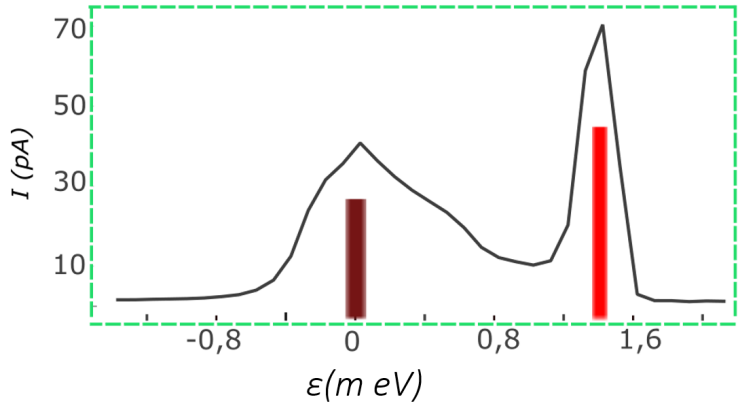


Figure 4.8: The detuning line for the triangle shown in Figure 4.7. The brown color corresponds to transport through the ground state while the red color corresponds to transport through the excited state.

## 4.3 Tuning the Middle Gate

### 4.3.1 Sample Chi2_P1_11

The next sample was measured in a dilution fridge and the measurements were oriented towards the investigation of the middle gate influence on the inter-dot coupling[2]. As Figure 4.9 suggests, the device with the $GtG$ distance of $50nm$ and $mG$ width of $30nm$ is measured. The $mG$ was not placed above the wire to avoid the formation of an unwanted triple QD. However, it's close enough so that it can electrostatically influence the inter-dot coupling $C_m$.

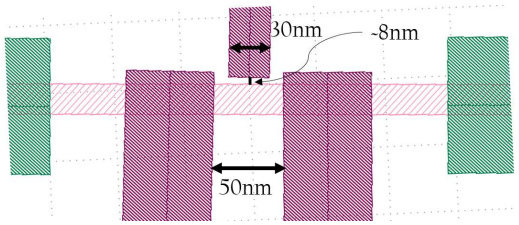


Figure 4.9: Layout of a DQD device used for the measurement shown in Figure 4.10. The GtG distance is $50nm$, the middle gate width is $30nm$ and it is located $8nm$ in distance from the HW as indicated in the Figure.

To investigate the influence of the middle gate on the inter-dot coupling, the stability diagram is measured for five different middle gate voltages; $V_m = (-1000, -500, 0, 500, 1000)mV$, as shown in Figure 4.10. One would expect that applying a voltage at $mG$ would influence the coupling constant $C_m$ and therefore the inter-dot coupling could be tuned. Although the current passing through the device is altered, there is no clear sign of tuneabillity between the coupled and decoupled regime.
It is believed that the mG is capacitively coupled to the QDs which is an unwanted effect coming from the device dimensions as shown in Figure 4.11. This has the consequence of $V_m$ influencing the potential profile of a QD together with the inter-dot capacitance which is ineffective for achieving a highly tunable DQD inter-dot barrier.

[2]Unfortunately, the sample was not annealed since at the time of fabrication, the RTA step was not yet introduced into the recipe.

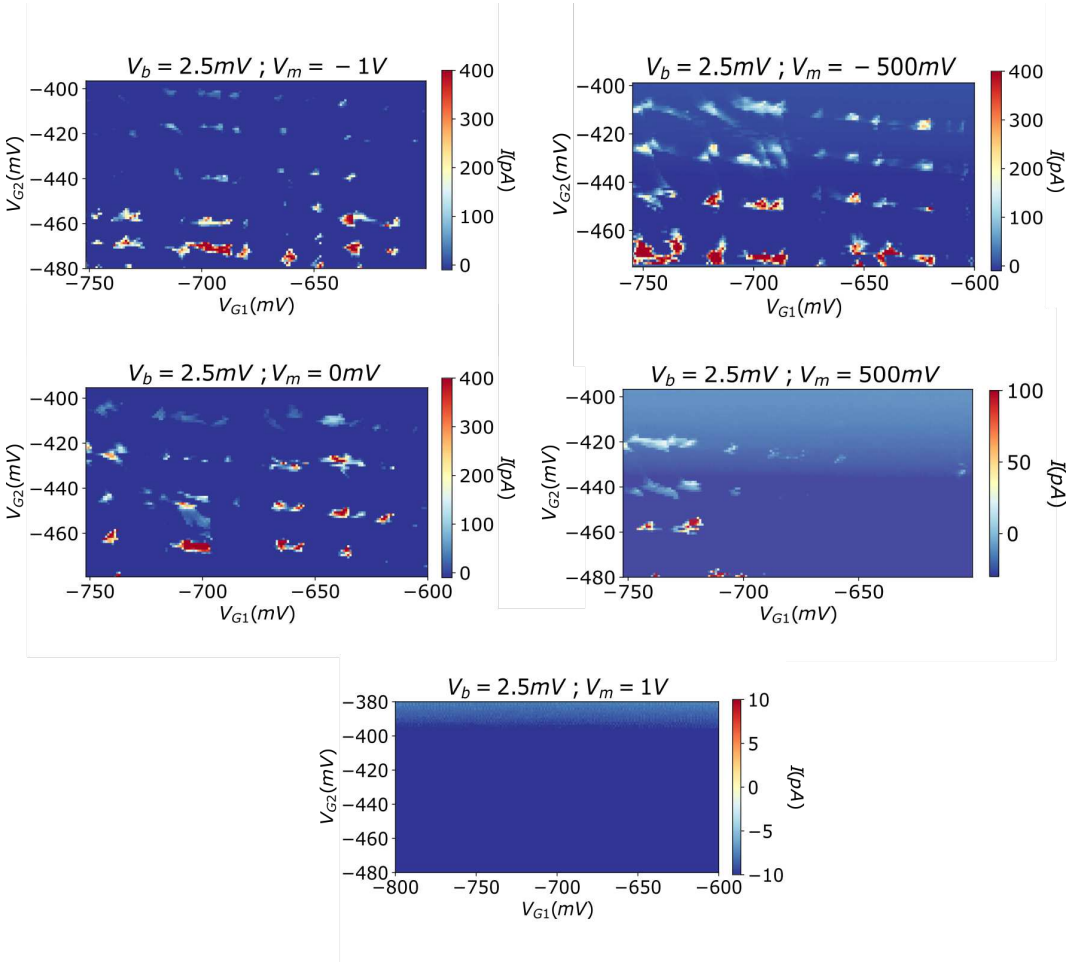


Figure 4.10: Charge stability diagrams for different middle gate voltages in a range from $-1V$ to $1V$. Sweeping the middle gate shows no clear sign of inter-dot coupling tunability. The blue gradient in the background of the diagrams is due to a leakage current of around $\approx 20pA$ flowing from the gate to the drain. $T = 10mK$

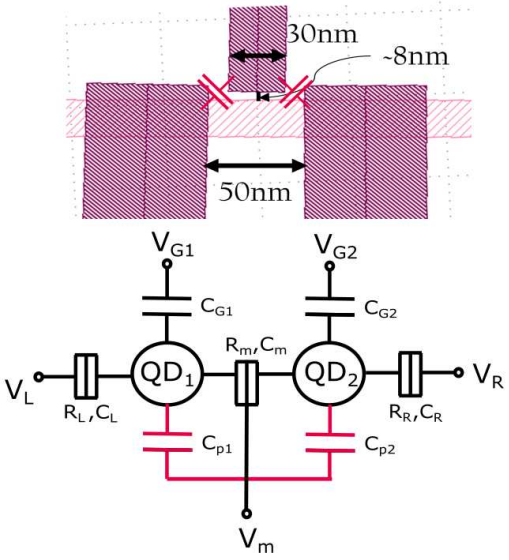


Figure 4.11: On top, the device layout used for measurements shown in Figure 4.10. It's corresponding electrostatics schematic with parasitic capacitance in red is shown at the bottom

### 4.3.2 Sample Chi2_P1_22

In the previous sample it was suspected that the middle gate is capacitively coupled to the QDs which is an unwanted effect for inter-dot tunability. To avoid it in the following sample, a different middle gate design is used as shown in Figure 4.12. The GtG width is increased from 50 to 60$nm$. Further on, the mG width is decreased from 30 to 20$nm$ and placed above the wire in order to directly influence the barrier between the QDs [3].

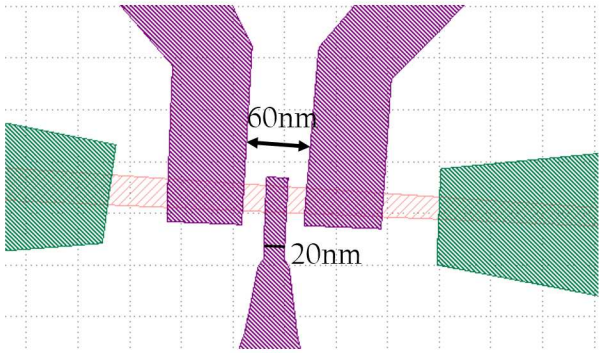


Figure 4.12: Layout of a device fabricated from sample Chi2_P1_22 and used for measurement in Figure 4.15. The middle gate is placed over the wire in order to tune the inter-dot capacitance.

The measurement is started for a middle gate value of $V_m = 0V$. The gates $V_{G1}$ and $V_{G2}$ are swept and show Coulomb peaks even for positive voltages (see Fig. 4.13) which means that the QDs are formed not only due to gate voltage confinement [4]. This behaviour was also observed in a previous work[5], where it was argued that the hole confinement might be induced by the strain from the deposited gates.

To avoid the formation of a QD below the middle gate, it is swept to positive voltage in order to deplete any formed dot below. The device is turned off at $V_m \approx 1.3V$ ( see Fig. 4.14) and the middle gate influence is inspected in that range.

[3] RTA step is used, 300C for 15min with flow 100sccm of $N_2$ and $H_2$ gas mixture.

[4] Holes are confined by negative voltages. Positive gate voltage Coulomb peaks prove QDs formation already for zero gates voltage.

[5] Watzinger, 2018.

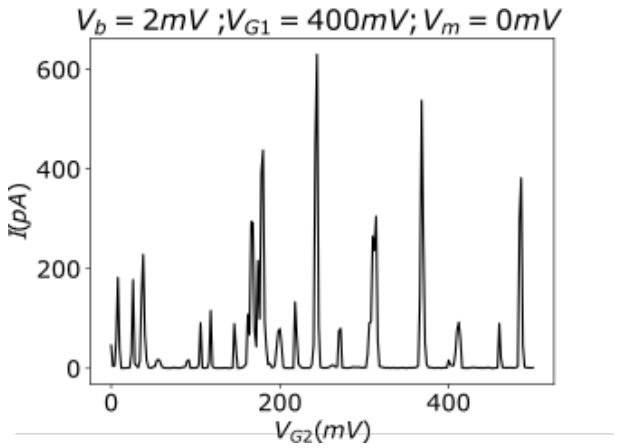


Figure 4.13: Current vs gate voltages showing Coulomb peaks for positive gate voltages.

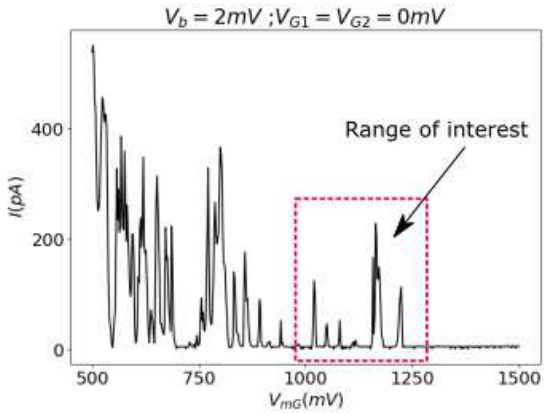


Figure 4.14: $I$ vs $V_m$ characteristic showing peaks due to mG sweep. By applying sufficient positive voltage, the device is turned off at $1.3V$ and further measurements are done.

The bias voltage is set to $200\mu V$ and charge stability diagrams are measured for different mG voltages. In Figure 4.15, the tuning between coupled ($V_m = 0.95V$) and decoupled ($V_m = 1.35V$) regime is obvious and inter-dot tunability is proven. In the decoupled regime the bias is increased to $V_b = 1.5mV$ and high bias triangles are revealed. By extracting the values from the triangle (lower right), the level arms are calculated to be

$$\alpha_1 \approx \alpha_2 \approx 0.375 \tag{4.1}$$

Which together with the measurement from the sample *Chi*2_*P*1_12 prove reproducible properties of the thermal oxide.
Further inspection of the triangles reveals indication of Pauli spin blockade as shown in Figure 4.16. Note that the neighboring triangle (at the bottom) is given for comparison. The indication of spin blockade makes the reported DQD adequate for the further spin qubit experiments.

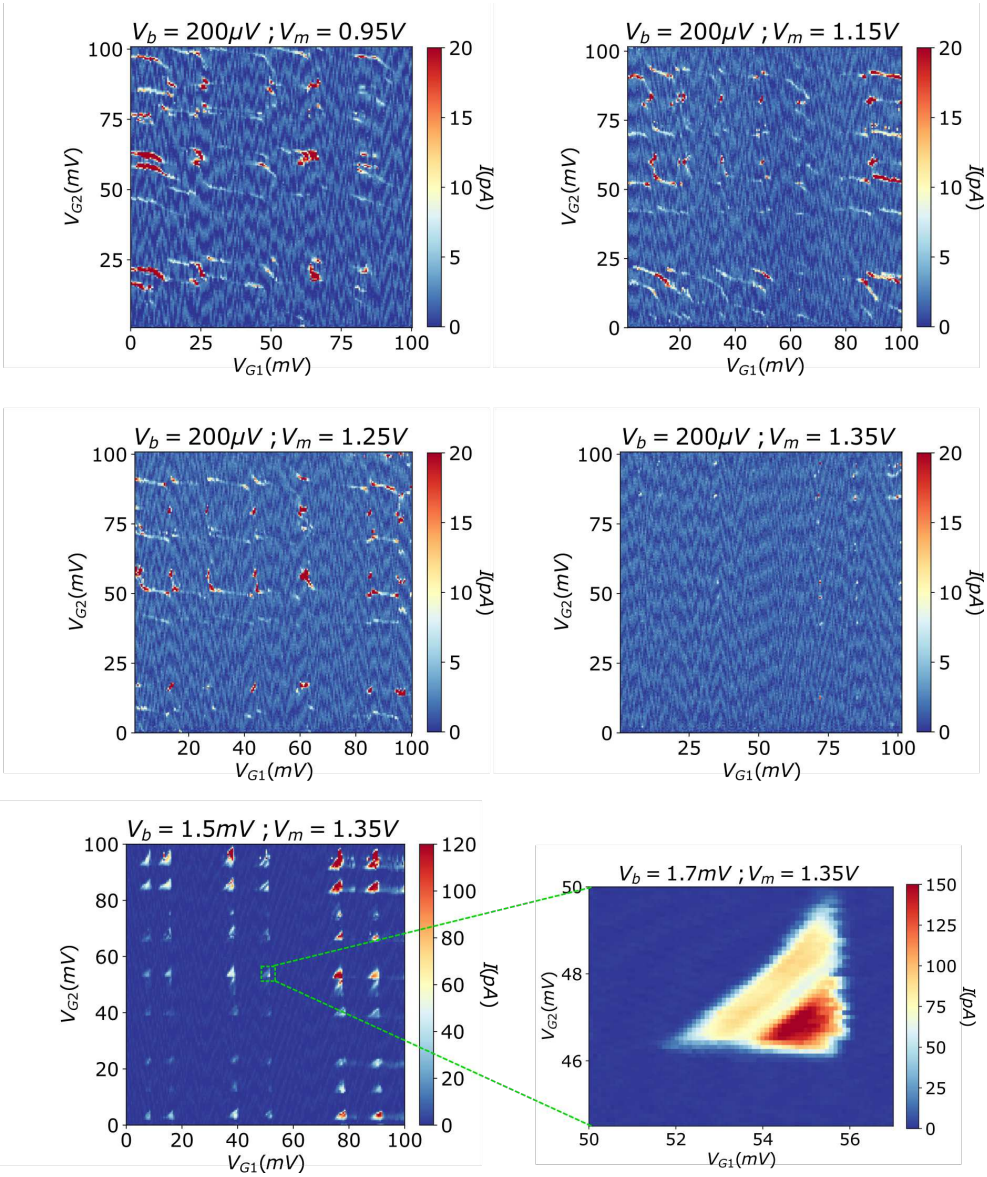


Figure 4.15: Charge stability diagrams of the same gate voltage range for different middle gate voltages. On the upper left diagram characteristic lines show strong coupling between the dots. When the mG voltage is increased from $0.95V$ to $1.15V$ a hexagonal structure starts forming. With the further increase to mG $1.25V$ a hexagonal structure is obvious. At $1.35V$ the DQD dot is in the decoupled regime (middle right) and transport is observed at the corners of a rectangular grid where triangles form when the bias is increased (lower left). The lower right image is a high resolution scan of one of the triangles. The periodic blue gradient seen in the background is noise of several $pA$ due to imperfect grounding. $T = 10mK$

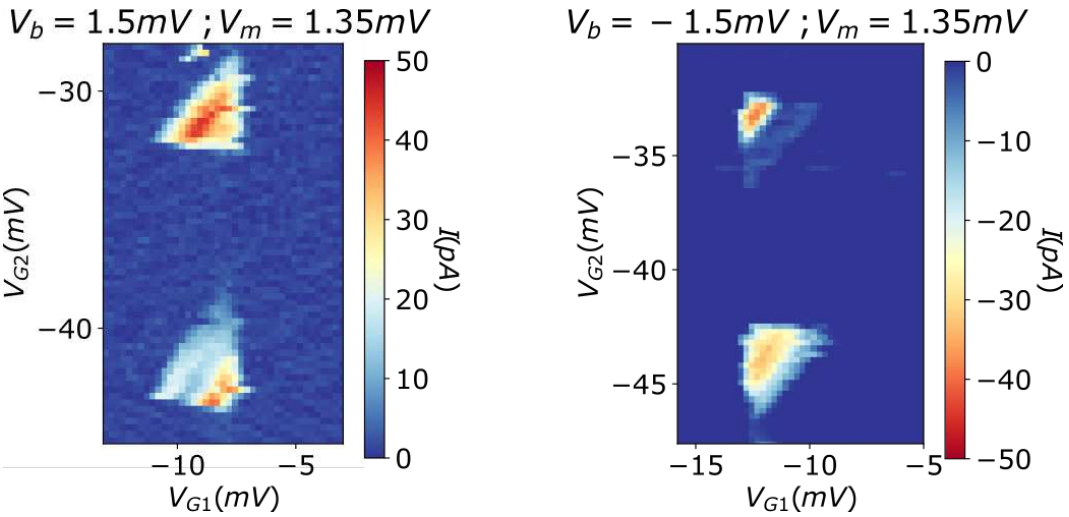


Figure 4.16: Stability diagrams indicating Pauli Spin Blockade for the top triangle pair for negative bias.

# 5 Conclusion

A successful demonstration of stable and tunable DQDs is reported. The main difference from previously reported DQDs in hut wires is the use of a thermal oxide instead of the ALD deposited oxides. It is argued that EBL machines induce unwanted charges in the ALD oxide while writing the top-gates. The thermal oxide avoids this issue, since it's formed after the gate deposition. However, more work is needed to investigate the EBL influence on the oxide quality and therefore on the charge noise. The regular charge stability diagram together with noise -free triangles shown in Figure 4.15, imply that a qubit formed by a described fabrication recipe should be within reach. Future work will orient towards reaching the last hole regime and implementing tunable gate to source/drain barriers.
A tunable inter-dot coupling was achieved by depositing a $20nm$ thick middle gate over the hut wire and in-between the two QDs. It opens a possibility of implementing a quantum CNOT gate, which has not yet been reported in these structures.
Fast spin manipulation times, no use of micromagnets, CMOS compatibility, simple device design and possibility to pre-pattern hut wires, places the Ge hut wires as a promising material platform for moving towards multiple qubit devices.

This document is set in Palatino, compiled with pdfLaTeX2e and `Biber`.

The LaTeX template from Karl Voit is based on KOMA script and can be found online: https://github.com/novoid/LaTeX-KOMA-template

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# 6 Declaration

Hiermit erkläre ich, dass die vorliegende Arbeit gemäß dem Code of Conduct – Regeln zur Sicherung guter wissenschaftlicher Praxis (in der aktuellen Fassung des jeweiligen Mitteilungsblattes der TU Wien), insbesondere ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel, angefertigt wurde. Die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet. Die Arbeit wurde bisher weder im In– noch im Ausland in gleicher oder in ähnlicher Form in anderen Prüfungsverfahren vorgelegt.

Marin Soče

März 2020, Wien