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Characterization Studies of 65nm Radiation-Tolerant Pixel Readout Chip for CMS Outer Tracker

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unter der Anleitung von

DI Dr. Marko Dragicevic

und

Priv.-Doz. DI Dr. Christoph Schwanda

durch

Anvesh Nookala, BSc

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Abstract

The Large Hadron Collider (LHC) is the largest accelerator laboratory in the world and is operated by CERN, an international organization dedicated to particle physics research. To fully utilize its physics potential, the High-Luminosity upgrade (HL-LHC) aims to increase the instantaneous luminosity of the accelerator by a factor of 5 to 10. The consequent increases in collision rate, particle track density and radiation dose call for an extensive upgrade of the particle tracking system ("silicon tracker") of the general-purpose CMS detector. The increase in collision events requires an enhanced discrimination towards interesting events. A new discrimination strategy is introduced to the CMS Outer Tracker, where individual modules correlate signals of two closely-spaced sensor layers to filter for high-momentum particle hits. High energy hits are provided continuously at 40 MHz as coarse tracking information to the detector Level-1 trigger system, which uses the information to decide if the collision event is to be further processed or discarded. The Macro-Pixel ASIC (MPA) and Short-Strip ASIC (SSA) are 65 nm CMOS-technology based silicon detector read out-chips designed to satisfy the heightened performance requirements while implementing a fast on-chip particle momentum discrimination logic. The development of the two chips has progressed towards their final prototypes, respectively named MPA2 and SSA2.1. Extensive testing on various stages, ranging from wafer-level probing, single chip characterization on carrier-boards to total ionizing dose (TID) and single event upsets (SEU) irradiation testing have been conducted. Within the scope of this thesis and regarding its future operation in the CMS Outer Tracker, the performance of the MPA2 was characterized and studied. Probe station tests on a sample size of over 3550 MPA2 chips from 17 wafers show that over 90% of them are fully functional. Chip characterization studies in respect to temperature and radiation indicate a good general functionality and show effectiveness of radiation effect mitigation and low-power techniques used in the design of the chip.

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Zusammenfassung

Der Large Hadron Collider (LHC) ist das größte Beschleunigerlabor der Welt und wird vom CERN betrieben, einer internationalen Forschungsorganisation, die sich der Teilchenphysik widmet. Um dessen physikalisches Potenzial weiter ausschöpfen zu können, soll mit dem High-Luminosity-Upgrade (HL-LHC) die momentane Luminosität des Beschleunigers um einen Faktor 5 bis 10 erhöht werden. Die sich daraus ergebende Erhöhung der Kollisionsrate, der Teilchenspurdichte und der Strahlendosis erfordert ein umfangreiches Upgrade des Teilchentrackers ("Silicon-Tracker") des CMS Detektors. Die Zunahme der Kollisionsereignisse erfordert auch eine verbesserte Diskriminierung von interessanten Ereignissen. Im Zuge dessen, wurde für den CMS Outer Tracker eine neue Strategie eingeführt, bei der einzelne Module die Signale von zwei eng aufeinander liegenden Sensorschichten korrelieren, um somit Treffer von hochenergetischen Teilchen zu selektieren. Hochenergetische Treffer werden kontinuierlich mit 40 MHz als grobe Tracking-Information an das Level-1-Trigger-System des Detektors geliefert, das anhand dieser Informationen entscheidet, ob das Kollisionsereignis weiterverarbeitet oder verworfen werden soll. Der Macro-Pixel-ASIC (MPA) und der Short-Strip-ASIC (SSA) sind 65 nm CMOS-Technologie basierende Auslesechips für Siliziumsensoren. Sie wurden entwickelt, um die erhöhten Leistungsanforderungen zu erfüllen und gleichzeitig die hochfrequente On-Chip-Logik zur Unterscheidung von Teilchenimpulsen zu implementieren. Die Entwicklung der beiden Chips ist bis zu ihren endgültigen Prototypen, dem MPA2 und dem SSA2.1, vorangeschritten. Im Rahmen dieser Arbeit, wurden umfangreiche Tests in verschiedenen Stadien durchgeführt, reichend von Tests auf Waferebene über die Charakterisierung einzelner Chips auf Trägerplatinen bis hin zu ionisierenden Bestrahlung (TID) und Single-Event-Upset (SEU) Charakterisierungen. Im Hinblick auf dessen zukünftigen Betrieb im CMS Outer Tracker, wurde die Leistungsfähigkeit des MPA2 charakterisiert und untersucht. Wafertests anhand einer Stückzahl von über 3550 MPA2-Chips von 17 Wafern haben gezeigt, dass über 90% voll funktionsfähig sind. Messungen zur Charakterisierung des Chips in Bezug auf Temperatur und Strahlung weisen auf eine gute allgemeine Funktionalität hin und untersteichen die Wirksamkeit von Design-Techniken hinsichtlich Strahlungsresistenz und Energieeffizienz in der Implementierung des Chips.

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1 Introduction

Particle accelerators play a major role in the field of high energy physics (HEP), with new discoveries driven by either the emergence of larger and more powerful accelerators or their continuous improvement. The Large Hadron Collider (LHC) is todays largest accelerator laboratory in the world and is operated by CERN, an international organization dedicated to particle physics research. Following many years of design, planning, and commissioning for the LHC, the discovery of a new particle was announced after only two years of its operation in 2012 [1]. The observation of the Higgs boson was a milestone discovery for the HEP field and represents a long sought-after conclusion for the Standard Model (SM).

The SM still leaves many questions to be answered and has opened the field for Beyond Standard Model (BSM) theories to be proposed and investigated. However, the statistical gain of running the accelerator will become marginal after the current Run 3 has concluded in 2025 and continued operation will necessitate a reduction in the statistical uncertainty of the data, i.e., an increase in data rates will be imperative. In an effort to maintain scientific progress and fully exploit the potential of the LHC, the High-Luminosity at LHC (HL-LHC) upgrade aims to increase the luminosity available to experiments to 5 - 7 $\times$ $10^{34}\text{cm}^{-2}\text{s}^{-1}$ by 2029 [2]. The HL-LHC upgrade will increase the data sample available to experiments by up to one order of magnitude. This will allow experiments such as the Compact Muon Solenoid (CMS) and A Toroidal LHC Apparatus (ATLAS) detectors to support extended studies of Higgs bosons and searches for new particles, which could help solve currently investigated open questions in HEP [3].

The luminosity increase of the HL-LHC upgrade will cause increases in collision rates, particle track density, and radiation doses. It will require comprehensive upgrades of a wide range of components and systems across the LHC and its detectors. The tracker system ("silicon tracker") of the general-purpose CMS detector employs multiple layers of silicon sensor modules to measure the trajectories of particles emerging from the beam collisions. It will undergo a complete replacement in the scope of its so-called Phase-2 upgrade [4]. To handle increased data rates, the p_{T}-module concept was introduced to the outer layers of the CMS tracker (CMS Outer Tracker). The p_{T}-module concept consists of two parallel sensor layers which are spaced a few millimeters apart. A magnetic field permeates the tracker and bends trajectories of charged particles traversing the sensor layers. The degree of curvature is dependant on the particle momentum, thereby by correlating particle hits between its two sensor planes, the p_{T}-module is able to discriminate particles based on their transverse momentum p_{T}. If the subsequent particle hit occurs

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in a certain narrow region above the the primary hit, that particle is ascribed a certain p_{T}. The sensor signals are digitized and a so-called stub event is generated.

Two flavors of p_{T}-modules will be implemented for the CMS Outer Tracker (CMS OT): The 2S consists of two strip sensor layers and the PS module consists of one strip and one pixel sensor layer. The signals of the PS-module pixel sensors (PS-p) and strip sensors (PS-s) are read-out and processed by the Application Specific Integrated Circuits (ASICs), the Macro-Pixel ASIC (MPA) and Short-Strip ASIC (SSA) respectively. Both chips are fabricated in 65 nm Complementary Metal-Oxide Semiconductor (CMOS) technology. The MPA has undergone multiple prototype design and fabrication iterations: the MPA-light, MPA1, and finally the MPA2.

In the scope of this master thesis, test routines were developed and testing was performed in various stages with the overall goal to verify the functionality and characterize the performance of the MPA2. The MPA2 was tested at a wafer level and its behavior in respect to variation of temperature and radiation was studied in depth.

This document is structured as follows. The basic concepts of silicon detectors and radiation effects are described in Chapter 2. The CMS Outer Tracker, its Phase-2-Upgrade and the thereby formulated requirements to the MPA2 are discussed in Chapter 3. Chapter 4 provides a description on the MPA2 chip architecture and its various functionalities. Chapter 5 presents the used testing methodology and reports the functional testing data gathered through probing of the MPA2 wafers. In Chapter 6, more in-depth studies of the MPA2 in respect to temperature, X-ray and heavy ion irradiation characterization are reported, in an effort to verify its readiness for operation in the CMS Outer Tracker.

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2 Silicon Particle Detectors

Silicon is the most widely accessible semiconductor and a preferred sensor material for particle detectors [5]. This is owed to it's fast signal generation, high read out rate, and energy resolution capabilities. Additionally, silicon sensor performance is comparatively resistant to radiation damage. Advances made within the semiconductor industry have allowed for the mass-production of high quality affordable silicon. Particularly, the ease of integration of silicon dioxide into silicon devices for usage as dielectric, insulation, gate-oxide, passivation, etc., provides a large technological benefit. The signals generated by silicon sensors are directly available in electric form, ready for analog and digital processing.

In this chapter the basics of particle interaction with matter pertinent to silicon detectors are discussed. Following that, the working principle of silicon detector technology, their read out systems and the effects of radiation on CMOS technology are summarized.

2.1 Particle Interactions with Matter

Particles are detected by their interaction with matter. The amount of energy deposited by an incident particle is dependent on the type of particle, its energy, charge, and the material of the detector. The energy loss (or also stopping power) of an incident charged particle is based on Coulomb forces toward shell electrons of the material (i.e., ionization). For heavy charged particles, the average energy loss $-\frac{\mathrm{d}E}{\mathrm{d}x}$ is expressed by the Bethe-Bloche function [5]:

$$-\left(\frac{\mathrm{d}E}{\mathrm{d}x}\right) = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A}\frac{1}{\beta^2}\left[\frac{1}{2}\ln\left(\frac{2m_e c^2\beta^2\gamma^2 T_{\max}}{I^2}\right) - \beta^2 - \frac{\delta(\gamma)}{2}\right] \tag{2.1}$$

The material properties of the detector are described by Z - the atomic number, A - the atomic mass, and I - the mean excitation energy. The incident particle is described by z - its charge, T_{max} - its maximum kinetic energy, and factor $\beta\gamma$ - representing the particle momentum. The other symbols are the constants c - the speed of light, N_A - the Avogadro constant, m_e - the electron mass, and r_e - the electron radius.

The Bethe-Bloche formula is valid for a certain range of incident particle energies and is applicable to the detection of heavy charged particles such as muons and hadrons. Figure 2.1 shows the average stopping loss in respect to incident particle energy. The value

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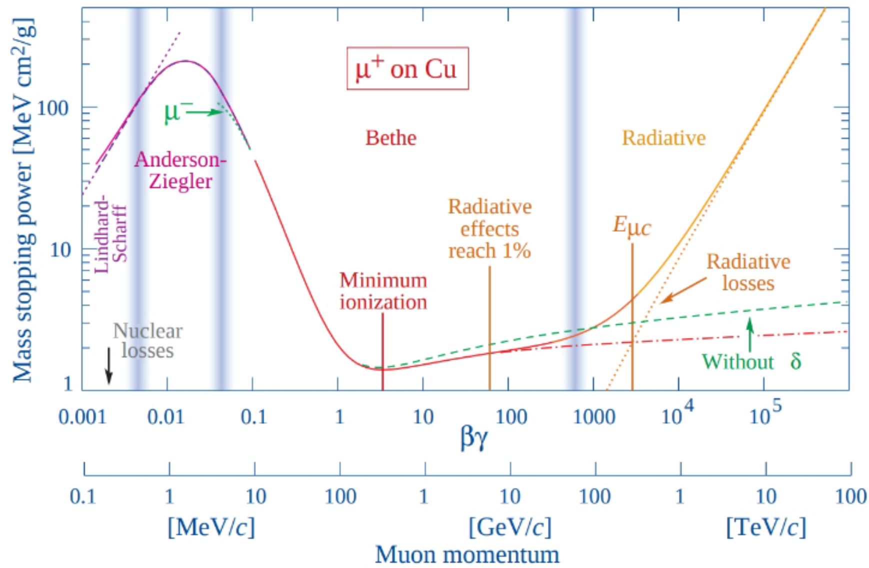

Figure 2.1: Average energy loss of a charged particle traversing a material, e.g. copper [5]. The Bethe region is shown in red and the minimum ionization level is marked. Particle energy is quantified with its momentum in $\frac{\mathrm{eV}}{c}$ [6]. For particle momentum beyond the Bethe region, various other interactions exist which are not considered for the particles discussed in this work.

of the minimum (seen at around $\beta\gamma \approx 3-4$) depends on the square of the particle charge and very weakly on the particle mass. Particles with energies around this minimum (1 to 100 GeV) are called Minimum Ionizing Particle (MIP). MIPs are considered the worst case in regards to energy levels a particle detector needs to be capable of detecting and also happen to be the most common particle energies that occur in HEP. As such, particle detector design is tasked with clear distinguishment of MIPs and constraining noise signals to well below this level.

If the incident charged particle is an electron or positron, the Bethe-Bloche relation does not apply, but ionization still remains the primary mode of energy loss. At higher energies, electric forces with shell electrons bend an incident electron trajectory and generate photons, an effect known as Bremsstrahlung, which can then further result in secondary ionization effects [7].

Due to the absence of charge and mass, photons do not interact with matter through direct ionization. For highly energetic photons (e.g., X-ray and γ-rays) effects such as the photo-electric effect, Compton scattering and pair-production can result in the generation of free charge carriers in matter [7].

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2.2 Working Principles of Silicon Detectors

The ionization of material by incident energetic particles is exploited in many materials particle detection. Before the availability of high-quality silicon, usage of gaseous detectors was widespread for example. One of the chief advantages of silicon is that only 3.6 eV are required to ionize silicon atoms and generate electron-hole pairs (e-h pairs), compared to 30 eV for gas molecules [5].

Other semiconductors materials such as Diamond or Galium may exhibit even better characterisics in terms of signal generation speed, signal-to-noise ratios or radiation hardness [8]. However, the as-of-yet high cost and complexity of the fabrication of these materials compared to the wide availability and capabilities of silicon manufacturing make it the clear choice as a sensor material.

When an ionizing particle traverses silicon, it generates e-h pairs along its path. The likely amount of a generated e-h pairs in Silicon can be described through a Landau distribution. For an incident MIP momentum of $E \approx 3\,\mathrm{GeV/c}$ and its mean energy loss in silicon of 390 eV/µm, the most probable value is 76 and the average is 108 e-h generated pairs per micrometer [5]. In the presence of an electric field, the electrons and holes diffuse towards the respective electrodes to form the basis of the signal to be amplified and processed. However, in intrinsic or single doped silicon the amount of thermally-excited e-h pairs is by orders of magnitude higher than those generated by an ionizing particle. Without any depletion of the excess charge carriers the silicon device would be insensitive to incident particles and therefore not usable as a particle detector. The solution is to deplete charge carriers by introducing diode structures operated in reverse bias.

2.2.1 pn-Junctions as Basis for Detection

The fundamental working principle of a silicon particle detector is based on highly doped silicon slices placed on a resistive silicon substrate of the opposite polarity to form a pn-junction [5]. Figure 2.2 shows the cross-section of a typical silicon particle detector with multiple pn-junctions. Excess electrons and holes diffuse into the oppositely doped region establishing a space-charge-region (SCR) around the interfaces between the n- and p-doped semiconductor. By applying a reverse bias voltage the SCR can be expanded throughout the full silicon volume to deplete all excess charge carriers throughout the silicon bulk. In this p-in-n type sensor, holes generated by an incident ionizing particle drift to the p+ doped strips while the electrons drift to the n++ backplane. By segmenting multiple pn-junctions across the length of the sensor, individual charge collection and measurement of the spatial coordinates of a particle trajectory becomes possible.

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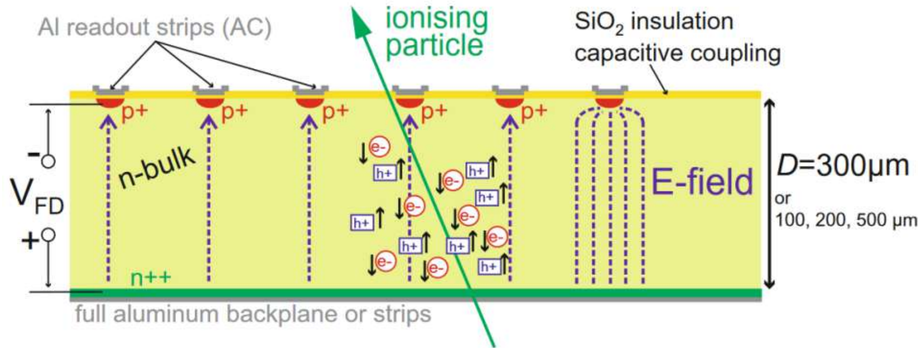

Figure 2.2: Typical working principle of p-in-n silicon strip sensor [5]. Segmented pn-junctions allow for charge collection through small individual strips. V_{FD} refers to the depletion voltage necessary to expand the SCR throughout the full sensor volume.

2.2.2 Standard Sensor Layout

Figure 2.3 shows a schematic of one corner of a modern baseline silicon sensor for use in a particle detector tracking system [5]. The n-in-p type sensor has a silicon base that consists of p-bulk and a p++ backside implant. The highly doped backside implant ensures an ohmic contact to the aluminum backplane. The n+ strip implants are placed on the top of the sensor to establish the pn-junctions. A thin high-quality SiO_2 layer separates the strip implants and aluminum readout strips on the top, forming a capacitative coupling between the two, while a thicker oxide separates the individual strips. The capacitative coupling formed by the coupling oxide is necessary to prevent leakage currents from being drained by the read-out electronics and is also called AC[1] read-out. Another oxide layer, the passivation layer, is processed on the full surface of the sensor for insulation and includes metal openings for the contact to the read-out chip through the AC pad. The DC pad[2] is typically added as conductive contact to the implants through vias and is only required for testing purposes.

The implants are surrounded by a bias ring which establishes a ground potential. A conductive decoupling to the bias ring is required in order to prevent loss of signal currents from the implants. As such, in the case of AC readout, the standard technique to establish the biasing contact between bias ring and the individual implants is through polysilicon resistors. The backplane functions as opposite terminal for application of the reverse bias voltage.

Each individual implant is further isolated by a p+-stop. These p+-stops are added as a counter-measure to conductive paths between implants which may form at the Si-SiO_2

[1] Alternating Current
[2] Direct Current

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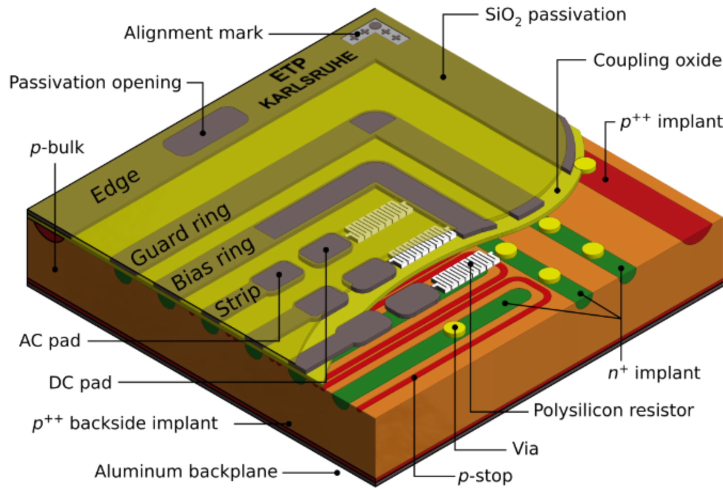

Figure 2.3: Illustration of an n-in-p type strip sensor [5]. It represents the baseline layout for silicon sensors used for the CMS Outer Tracker HL Upgrade, from which the pixel sensor layout is also adapted.

interface. Conductive paths may arise through trapped positive charges in the oxide layer which attract electrons from the silicon bulk. The p+-stop dissipates accumulated electron layers at the Si-SiO_2 interface, isolating the strips from each other.

Finally, all implants are encircled by one or more guard rings and the sensor edge. The sensor edge is a p-doped implant, providing a conductive path between sensor frontside, bulk and the backside. While the n+ bias ring is grounded, a n+guard ring is added in between to provide a more continuous electric potential drop to the sensor edge, thereby protecting the sensors in the center from high voltages.

2.2.3 Strip and Pixel Detectors

Strip sensors are obtained by spatially segmenting the doped implants into strips over the length of the detector (see Figure 2.2) [5] . The connection of the sensors to adjacent read-out electronics can be established by wire-bonding them together. Such a configuration allows for sensor and read-out electronics to be developed independently from each-other based on their respective requirements and is often termed as a "hybrid" detector. In the strip sensor case, the resolution of the detection is limited by the size and pitch of the segmented strips themselves. For a higher resolution in a second axis, the implants can be segmented in two dimensions, becoming small isolated squares called pixel sensors. The amount of read-out channels presented by a two-dimensional pixel sensor array makes wire-bonding impractical however. As an alternative, the read-out chip is placed on top of the pixel sensor and electrically connected to individual pixels through small solder balls (often referred to as bump bonding). Figure 2.4 shows a typical bump bonding scheme

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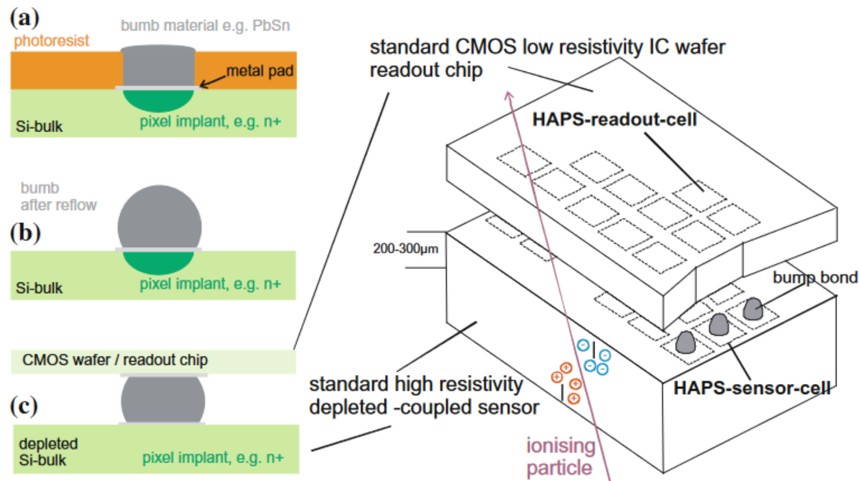

Figure 2.4: Bump bonding for a Hybrid Active Pixel Sensor (HAPS), where pixels of a low-resistivity readout chip are electrically connected to high-resistivity sensor cells [5].

for a Hybrid Active Pixel Sensor (HAPS). With Figure 2.3 the baseline layout for a strip sensor is described. The most notable modification for a pixel sensor is that the implants are DC coupled to the read-out electronics instead of AC coupled. This is due to the reduced amount of leakage current originating from smaller pixel implants. DC coupling therefore also does not have to rely on costly high quality and uniform processing of a large oxide layer. DC coupling does not require a bias ring, as the bias potential to the pixel implants is provided by the conductively connected read-out chip. However, bias rings are occasionally still added for testing and characterization purposes (fas was done for the pixel sensor of the PS-module). To bias each individual pixel implant, so called Punch-through-Structures (PTS) connected to the grounded bias rail are used [6].

2.3 Sensor Read-out Electronics

In the following, the generic building blocks of a typical pixel detector read-out architecture is presented according to Rossi et. al. [9]. When a pixel sensor and its read-out chip are produced separately they can be designed and optimized independently from each other. Modern read-out chips are commonly of mixed-signal designs leveraging standard analog and digital CMOS technology design processes. Each pixel sensor is read out by an analog front-unit which amplifies, discriminates and prepares charge signals from the sensors for digitization. The digital read-out architecture fulfills storage, data-encoding and transmission tasks while providing configurability toward potential variation in the application circumstances.

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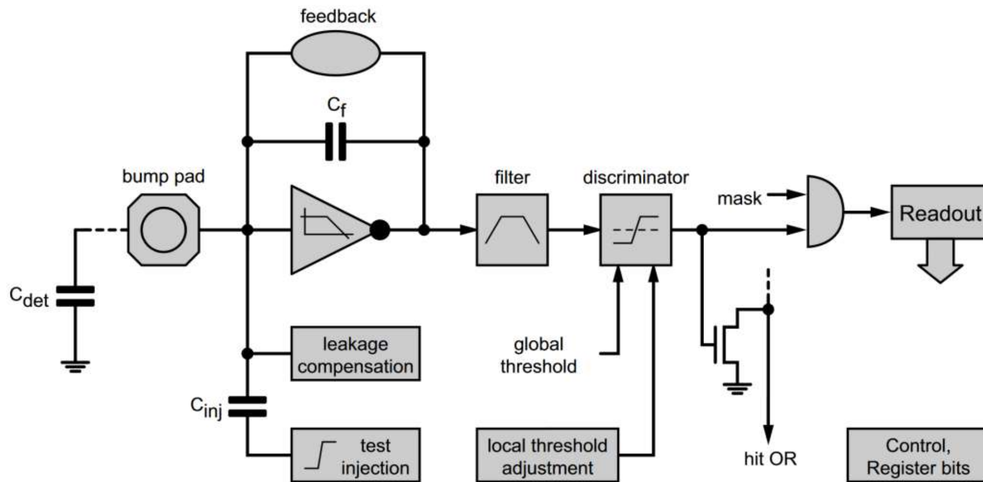

Figure 2.5: Schematic blocks of a generic analog front-end circuit and its connection to the digital read out structure [9].

2.3.1 Analog Front-End

The standard blocks of an analog front-end (FE) circuit to read-out a single pixel cell are shown in Figure 2.5. Signals generated by silicon sensors of 100 to 500 μm width are in the order of $10^4\,e^-$ charge and incur collection times in the nanosecond range. The capacitance C_{det} models the sensor behavior and is connected to a bump pad to which the analog FE is bump-bonded to.

The charge-sensitive amplifier reads out and converts an input charge to a voltage using a high open loop gain and capacitive feedback C_f. Ideally, the amplifier behaves like an integrator with the open loop gain set by C_f. In a real amplifier the gain will also be affected by C_{det}. An additional feedback circuit sets the DC operating point and depletes charge from C_f so that the voltage pulse may return to zero after an amplifier response. Leakage compensation is added as a sink for leakage currents of up to a few nA, as leakage occurs in the case of DC coupling to the sensor.

A band-pass filter, also referred to as the shaper, sets the bandwidth of the amplifier output. It suppresses high and low frequency noises, improving the signal-to-noise ratio.

The discriminator compares the shaper output voltage with a reference threshold. The result is available in 1-bit resolution, as a digital HIGH or LOW signal, depending on if the threshold was surpassed by the signal voltage or not. In typical implementations, a global threshold can be set for the entire two-dimensional array of analog FEs of a read-out chip.

ASICs which implement analog FEs based on the typical scheme presented here are, e.g., the TimePix4, a hybrid pixel detector for Time-over-Threshold and Time-of-Arrival

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measurement [10], the ISPA, for Gamma Ray Imaging [11], or the RD53A, a demonstrator chip for the HL-LHC [12].

S-Curve

As the analog output of a pixel FE can often not be directly measured, the S-curve is an important figure of merit for the characterization of the response behavior of an analog pixel FE [9]. It can be determined by plotting the response ratio of the discriminator with a set threshold against multiple charge injections with increasing amplitude. An example of this shown in Figure 2.6. The higher the input charge amplitude, the more likely it is for a discriminator to respond. The measured threshold is defined at the mid-point where 50 % of the injections fire the discriminator.

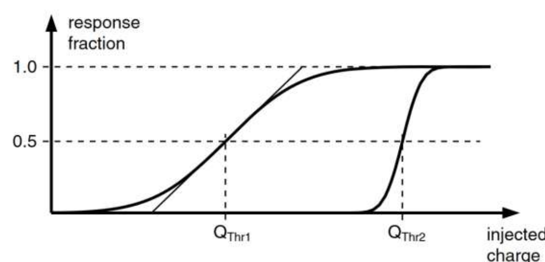

Figure 2.6: 'S-curve' response of two discriminators [9]. The slope quantifies the noise level of the analog channel.

In the ideal case, the S-curve would be a stepping function. However in real devices, a front-end noise is introduced by the analog circuit and causes noise hits. The equivalent noise charge (ENC) is the root-mean-square noise at the input of the discriminator expressed in input charge, i.e., the noise output voltage divided by the gain of the amplifier. The output of the analog front-end cannot be directly measured, but the ENC can still be determined by the slope of the S-Curve and is quoted in units of charge (or electrons). When referring to noise of the analog FE channel throughout this thesis, the ENC determined by through the S-curve is meant.

Ideally, all thresholds across a pixel array are the same. In practice, the thresholds between analog pixel FEs will vary due to slight variations in the quality of the lithographic fabrication process. The threshold variation needs to be finely balanced in order to guarantee a consistent hit efficiency across a pixel array in trade-off with the noise performance. A fine-tunable local threshold can be provided on a per-pixel basis to compensate for variations between the analog FE characteristics across one chip. These type of threshold tuning techniques make use of injection of known test charges provided by a calibration capacitance C_{inj}.

After trimming, the fluctuations of the per-pixel thresholds will be reduced and a lower limit for the average threshold should be defined to keep the noise hit rate low [9]. A

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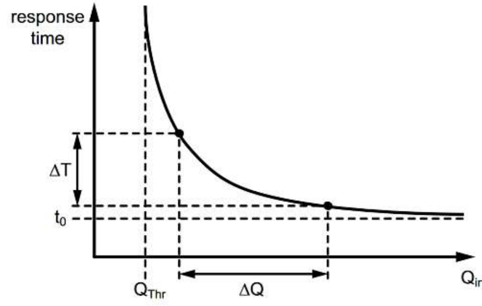

Figure 2.7: Response time of an analog FE circuit as a function of injected charge [9]. ΔT indicates the timewalk.

minimum recommended threshold can be determined, with the threshold spread σ_{thr} and noise σ_{noise} by the estimation

$$Q_{\text{thr}} \gtrsim 5-6 \times \sqrt{\sigma_{\text{thr}}^2 + \sigma_{\text{noise}}^2}. \tag{2.2}$$

For the input charge generated by a MIP in a 250 µm-thick sensor material, a conservative goal should be to keep σ_{noise} and σ_{thr} in the order of $\sim 200\,\text{e}^-$.

Timewalk

Another mechanism to consider is the response time between pulse injection and hit detection of the circuit: compared to high amplitude pulses, lower amplitude pulses will arrive later in time to the discriminator input. In other words, higher charge pulses are "faster", as illustrated in Figure 2.7. Incident particles with low input charges may thereby be associated to a subsequent discrete point in time. This effect is termed timewalk and the extent of its delay should be determined and limited to a certain minimum.

2.3.2 Digital Read-out

The further processing and digital read-out architecture is then strongly dependant on the requirements of the application. In high-event rate HEP applications, many events are not relevant for physics analyses. As such, the need of implementing on-chip data reduction techniques, while satisfying requirements in power consumption and radiation tolerance, drives the design of read-out architectures.

Important indicators are the hit rate [$\text{s}^{-1}\text{cm}^{-1}$] and the occupancy [$\text{s}^{-1}$]. The hit rate defines the number of particle hits over the sensor during a time period. It implies the amount of events a digital read-out architecture needs to be able to process. The occupancy describes the ratio of utilization of the read-out channels with hit information

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during a defined time period. In the case of the LHC, the reference period is the 25 ns bunch crossing rate.

Read-out architectures often employ zero-suppression to reduce size of buffers and satisfy power requirements. In zero-suppression, detector signals are only processed when they surpass the set discriminator threshold.

When continuous transmission of particle hit data is not feasible, a triggered read-out can be implemented. Triggered read-out refers to a functionality, where the read-out ASIC[3] stores the event information for a set duration (latency) until a trigger signal is received and the data is transmitted. If no trigger signal is received the event information is discarded. This requires sufficiently sized data buffers in the read-out chips to store event data for a certain latency.

2.4 Radiation Effects in CMOS Electronics

Irradiation effects on electronics encompass any modification of the electrical properties of the device through interaction of an incident particle. Effects can be detrimental to the device performance or even cause unrecoverable failures. The study of radiation-induced effects is of particular importance in HEP, as high radiation doses pose a key challenge in the design and the reliability of the highly integrated electronics used in experiments.

In the scope of this master thesis, radiation-induced effects on CMOS-technology-based read-out electronics of silicon particle detectors will be discussed. Relevant radiation-induced effects on the underlying MOSFETs[4] are categorized into displacement damage of silicon lattice, ionization of oxides and single event effects. Only the latter two will be discussed as MOSFETs are less sensitive to displacement damage effects [13].

2.4.1 Total Ionizing Dose Effects

Total Ionizing Dose (TID) effects in MOSFETs consist of radiation-induced ionization in silicon dioxide structures and the generated charges being accumulated as "traps" near or at the interface to silicon [14]. The magnitude of TID is expressed as absorbed radiation dose using the SI[5] unit Gray (Gy). The unit rad is also used frequently, with a conversion of $100\,\mathrm{rad} = 1\,\mathrm{Gy} = 1\,\frac{\mathrm{J}}{\mathrm{kg}}$. Contributions toward a deposited dose can originate from various incident particles. At certain energies, photons may cause ionization in silicon dioxide mainly through the photoelectric effect. Later in this thesis, the results of using an x-ray source to study TID effects in the MPA2 chip will be presented.

[3] Application Specific Integrated Circuit
[4] Metal Oxide Semiconductor Field Effect Transistors
[5] *SI*, International System of Units

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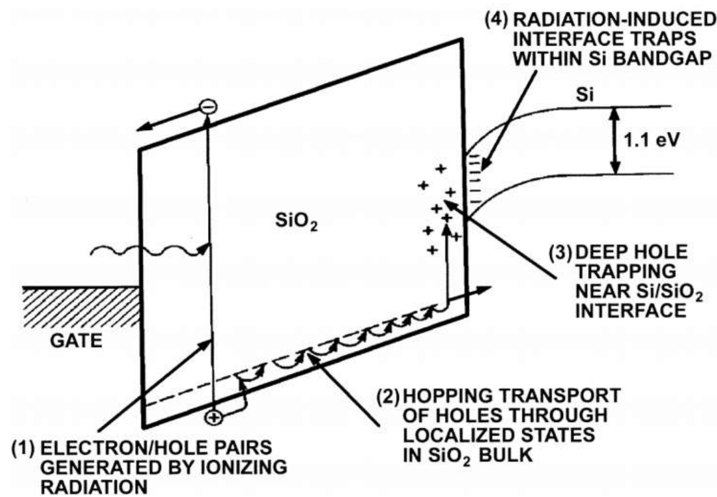

Figure 2.8: Schematic of energy band diagram of a MOSFET gate oxide interface and generation of interface traps induced by radiation [14].

The basic process of the emergence of TID effects is illustrated in Figure 2.8. Induced by incident ionizing particles, e-h pairs are generated in the SiO_2 material [14]. A large fraction of the pairs quickly recombine depending on the charge carrier mobility of the oxide. The remaining free charge carriers are transported in the oxide in the presence of a positive-bias electric field: electrons diffuse towards the gate electrode, while holes are transported to the Si-interface via "hopping" through localized energy states. Hole transportation can result in the formation of trapped positive charges around pre-existing defects within the oxide. Another effect of transported holes is the reaction with hydrogen atoms and generation of hydrogen ions. Hydrogen ions may further react with Si-H bonds at the SiO_2-Si interface where then negatively-charged interface traps are formed. Traps in the oxide are quicker to form but may also be recovered through thermal energy (annealing). Traps formed at the interface however are formed slowly over time and require temperatures of 400 °C to anneal.

The extent of high dose-rate effects in 28 nm, 65 nm and 128 nm CMOS technology nodes was studied in [15]. Gate oxide layers in modern CMOS technologies are only few nm thick, and typically produced in high quality processes. The reduced scale and lack of defects have made TID-induced effects in gate oxide layers negligible. As such, TID effects are limited to occurring in lateral oxides such as shallow trench isolation (STI) used to isolate adjacent transistors and oxides used in spacers for the gate in lightly-doped drain (LDD) transistors. STI oxides are much thicker and richer in defects than gate oxide layers, so TID effects can remain significant.

Trapped charges in the trench oxides are positive. Therefore, radiation-induced effects are distinguished between pMOS and nMOS devices. Generally speaking, in nMOS devices, positive charges trapped at the oxide interfaces result in a shift of the transistor

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threshold voltages and increases in leakage currents[6]. For pMOS devices, the trapped positive charges in oxide result in the degradation of the transistor on-current I_{ON} at high TID levels ($>$ 100 Mrad). The degradation of the device performance varies depending on the dimensions of the gate, the technology node, the operating temperature and the applied bias voltages.

To study and qualify TID effects in MOS devices, the ionization of oxides is preferentially induced by photon irradiation. Photons do not cause other effects such as displacement damage or single-event effects, and so these effects are excluded when studying device degradation towards TID [16].

2.4.2 Single Event Effects

Single-Event Effects (SEE) are events which are caused by transient energetic single particles [7]. The incident particle experiences energy loss through the process of Coulomb scattering, ionization and generation of e-h pairs. While TID effects occur in the oxides, SEEs are local to pn-junctions of MOSFETs where the charges are collected as transient pulses. The pulses may give rise to different types of errors at a circuit node.

An Single-Event Upset (SEU) may occur in memories of digital circuits, such as latches and flip-flops. In an SEU, one or more stored bits are overwritten by the collected charge of an incident charged particle. In a classic CMOS inverter, the output node is most sensitive to particle hits as it is connected to the drains of the nMOS and pMOS devices. A transient positive or negative charge at the output node may lead to a reversing of the stored state, i.e., a bit is flipped. The flipped bit may propagate to other modules, corrupting data in memories or altering state of FSMs[7]. A Single Event Transient (SET) is an error that might occur within setup and hold times of sequential digital electronics, where a temporary wrong value is transmitted and causes incorrect logical states. In combinatorial logic circuits, SETs might lead to SEUs. A Single-Event Latchup (SEL) occurs through the parasitic combined PNPN structure in CMOS devices. The transient current spike can trigger a latch up such that a short circuit between supply and ground is established.

The above errors are considered non-destructive soft errors. A recovery is often possible through re-writing the flipped bits or power cycling of the device. When shorted circuit currents in SELs are very high, they might burn through the device resulting in permanent damage and causing a hard error.

The probability of an SEU occurring is dependent on the energy transferred by the incident particle and the minimum charge needed to flip the state of a storage element. The Linear Energy Transfer (LET) of a particle is used to express the transferred amount

[6]Leakage current is defined as the transistor drain-to-source current I_{DS} while the transistor is in off-state.

[7]Finite State Machine

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of energy by per unit of distance. If put into relation with electronic devices through silicon density, LET is typically expressed in units MeV cm^2 mg^{-1}.

LET can also be expressed as deposited energy E_{dep} for a considered material volume. For silicon and a sensitive volume of 1 µm × 1 µm × 1 µm, E_{dep} is calculated by

$$E_{dep} = LET \cdot d \cdot \rho_{Si}, \tag{2.3}$$

where $d = 1\,\mu m$ is the depth of the SV and $\rho_{Si} = 2.32\,g/cm^3$ is the density of silicon.

To be able to relate the radiation-induced effects caused by different particles, a normalized measure for irradiation is used. The 1 MeV neutron equivalent fluence Φ_{eq} is used to scale the energy of a certain particle energy to the equivalent irradiation by 1 MeV neutrons. The unit of the measure is n_{eq}/cm^2.

The cross-section σ is a measured value to specify the probability of an error occurring during irradiaton. Cross-section is expressed in units of cm^2 and can be thought of as the sensitive area that a particle needs to hit to cause an error. It is calculated by

$$\sigma = \frac{N_{errors}}{\Phi_{eq}}. \tag{2.4}$$

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3 LHC and the CMS Experiment

The Large Hadron Collider (LHC) is part of an accelerator complex that has been steadily added upon since the founding of CERN in 1954. With a circumference of 27 km it is the worlds largest particle accelerator. It was built between 1998 and 2008 in a collaborative effort between institutes originating from over 100 countries. Among many accomplishments, the discovery of the Higgs boson is counted as the chief scientific breakthrough facilitated by the LHC. The LHC has undergone multiple phases of operation and shutdowns performed to upgrade its components. On April 22, 2022 the LHC became operational again commencing the so-called Run 3 which is expected to last until the end of 2025.

The Compact-Muon-Solenoid (CMS) experiment is one of the four larger detectors situated around the LHC beam crossing points. The ATLAS and CMS detectors are both considered general-purpose detectors, as they share similar objectives in further studying the Higgs boson and investigating BSM theories. The two detectors however vary in their technical implementation in order to provide corroboration for their respective findings.

This chapter provides a short introduction to characteristics of the LHC and the structure of the CMS experiment. The functionality of the CMS tracker and trigger system is described and the requirements given by the Phase-2 Upgrade are highlighted.

3.1 LHC Characteristics

The LHC is a synchrotron that accelerates two proton beams in a counter-rotation to each other within its accelerator complex. The beams are brought to collision at four respective interaction points at which the detectors CMS, ATLAS, A Large Ion Collider Experiment (ALICE), and Large Hadron Collider beauty (LHCb) are situated.

Each proton beam can be accelerated up to an energy of 6.8 TeV[1] through a chain of accelerators of which the LHC is the last. The CERN accelerator complex is shown in Figure 3.1. The proton-proton collisions in the LHC can reach a center-of-mass-energy $\sqrt{s}$, of up to 14 TeV [18]. The various resulting sub-atomic particles that are produced by the collisions are observed and, if considered as an interesting physics event, recorded by the detectors. Protons are accelerated in bunches with each bunch containing 1.15×10^{11}

[1] 1 eV is the amount of kinetic energy an electron gains when accelerated by a voltage of 1 V.

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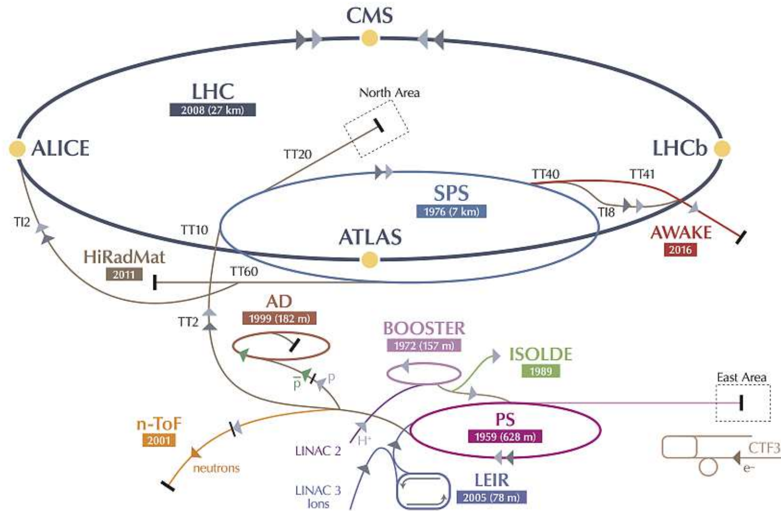

Figure 3.1: The CERN accelerator complex. The four interaction points are marked in yellow. Adapted from [17].

protons. An interaction between two proton bunches is called bunch crossing (BX). As the injection of bunches is spaced 25 ns apart, the resulting collision or bunch crossing rate (BX rate) is 40 MHz.

A key indicator of the performance of the LHC and a measure of the amount of the particle interactions is the instantaneous luminosity

$$l := \sigma^{-1}\frac{\mathrm{d}N}{\mathrm{d}t}, \tag{3.1}$$

where $\frac{dN}{dt}$ is the interaction rate and σ is the cross-section of the process. The integrated luminosity

$$L := \int l\mathrm{d}t \tag{3.2}$$

is a measure of the total amount of expected or observed events over a time period. In 2018 the instantaneous luminosity of the LHC reached $2.1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and an integrated luminosity of 66 inverse femtobarn (fb^{-1}) for proton-proton collisions was delivered.

3.2 The CMS Detector

The CMS detector is situated around Interaction Point 5 and is structured in layers with its central feature and namesake, the superconducting solenoid [19]. The solenoid provides a 3.8 T strong magnetic field that bends trajectories of charged particles traversing

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the detector. Figure 3.2 shows an overview of the detector. Each layer encloses the interaction point and represents a sub-detector system tasked with collecting information on particles produced by the collisions.

Within the solenoid structure is the silicon tracker, the Electromagnetic Calorimeter (ECAL) and the Hadron Calorimeter (HCAL). All three systems are composed of a barrel and two end cap sections. Both calorimeter sub-detectors are based on scintillators[2] to measure the energy of particles. The ECAL concerns itself with the energy measurement of electrons and photons, while for the HCAL the energy of Hadrons[3] is of interest.

Closest to the interaction point, the tracking system based on silicon detectors records paths of charged particles. Momentum is measured and tracks of particles are reconstructed by correlating measured particle hits from multiple locations within the tracker.

Surrounding the solenoid, muon chambers are interleaved with the solenoid return yoke. The muon system is based on gaseous chambers to detect the energy of muons, heavy charged particles which are not absorbed by the calorimeters in the inner part of the detector.

A cartesian right-handed coordinate system is adopted for CMS. Its origin is around the center of the detector where the interaction point lies, with the x-axis pointing toward the center of the LHC, the y-axis pointing upwards to the surface, and z-axis pointing in the direction of the particle beam. The xy-plane is called the transverse plane, with p_{T} referring to the transverse momentum of a particle in the xy-plane. Due to the cyclindrical shape of the detector, polar coordinates are also often used: r is the radial distance from the beam (or z-axis), the azimuthal angle φ is taken from the x-axis in the xy-plane, and the polar angle Θ is the angle measured in the rz-plane from the z-axis. The pseudorapidity η is often used instead of the polar angle, with $\eta = -\ln \tan(\frac{\Theta}{2})$.

3.2.1 Silicon Tracking System

The CMS tracker consists of two types of silicon detector devices: the inner pixel and outer strip detectors [19]. The dimensions of the sensors and sensor pitches vary depending on the radial distance of a sensor module to the interaction point. In total, the silicon tracker consists of 66 million pixels that cover a sensitive area of $1.1\,\mathrm{m}^2$. The strip detector has 10 million channels and covers an area of $206\,\mathrm{m}^2$. The strip detector modules are located between $20\,\mathrm{cm} < r < 120\,\mathrm{cm}$ from the interaction point, whereas the pixel detector modules are closer to the interaction point at $r < 20\,\mathrm{cm}$.

The tracker modules were designed for a instantaneous luminosity of $1 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ and an average pile-up[4] of 25. After upgrades to the LHC, the luminosity and pile-up

[2] *Scintillator*, a material that emits light when excited by ionizing radiation.
[3] *Hadrons*, particles made up of quarks and gluons e.g. protons, neutrons, pions and kaons.
[4] *Pile-up*, simultaneous collisions which occur during one bunch crossing.

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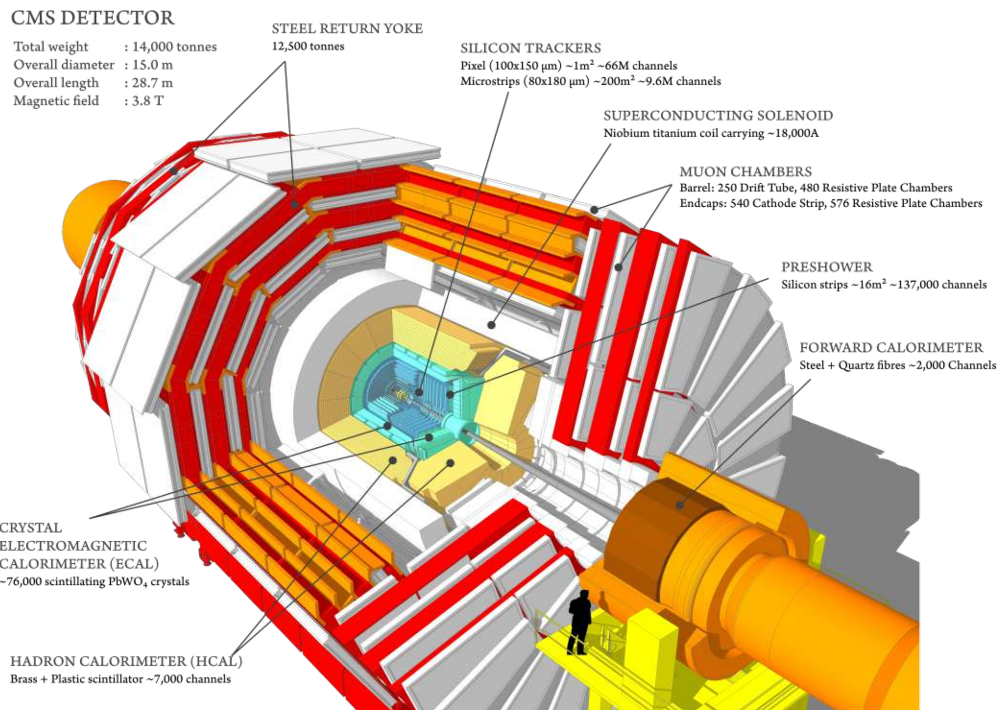

Figure 3.2: View of the current CMS detector [20]. The tracker composed of silicon strip and pixel sensors is highlighted in blue.

more than doubled in their original values [21]. The original pixel detector was replaced during the year-end technical stop of the LHC in 2016/2017 to handle the increased requirements [**adamCMSPhase1Pixel2021b**]. The strip detectors have remained the same since their installation.

The read-out chips of the pixel and strip detectors were designed using 0.25 μm CMOS technology. The read-out chip for the strip sensors is called APV25 [22], a fully analog chip featuring a triggered read-out mode to reduce data rates across the read-out channels. Triggered read-out refers to a functionality, where the read-out Application Specific Integrated Circuits (ASIC) stores the event information for a set duration (latency) until a trigger is received and the data is transmitted. If no trigger is received, the event information is discarded.

3.2.2 Triggering System

Considering a BX rate of 40 MHz and a pile-up of 25 to 40, over 1×10^9 events per second are generated in the CMS interaction point. As only a fraction of this generated data can be recorded, the CMS trigger system is designed to selectively read-out only interesting

events and suppress data rates by a factor of 10^6 [19]. The trigger system is comprised of two levels of triggers: the Level 1 Trigger (L1) and the High Level Trigger (HLT).

The L1 trigger is based on custom hardware processors that receive coarse event data from the calorimeter and muon systems after a collision. Using these so-called trigger primitives as input, track finding and p_T assignment algorithms are computed. Within $4\,\mu$s and with a maximum rate of 100 kHz, the L1 trigger must then decide to generate a Level-1 Accept (L1A) signal. The L1A signal triggers a read out of full resolution event information from the detector front-end electronics such as the APV25. The hardware implementation of the L1 trigger algorithm is based on several Field Programmable Gate Array (FPGA) boards which are located outside of the detector and transmit or receive data via high speed optical links.

The HLT is based on more elaborate software algorithms running on commercially available computing hardware to take events accepted by the L1 for further classification. The HLT further reduces the data rate to ∼1 kHz, a sustainable value for storage and physics analysis.

3.3 Phase-2 Upgrade of the CMS Tracker

The statistical gain of operating the LHC in its current state diminishes increasingly beyond 2020. To reduce the statistical error of generated physics data, the HL-LHC upgrade aims to increase the instantaneous luminosity to 5 to $7 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ with an accompanying increase of pile-up up to 200 [2]. The CMS Phase-2 Upgrade refers to the upgrades which the CMS detector will require for it to exploit the increased luminosity that HL-LHC will provide.

An increase in luminosity is accompanied by several increased requirements to the performance of the detector and its many sub-detectors. The upgrade of the CMS Tracker and the new strategies developed for it are of special interest to this thesis. The planned upgrades are described in the Technical Design Report of the Phase-2 Upgrade of the CMS Tracker [4].

3.3.1 L1 Trigger Requirements for the new Tracker

A key challenge to be addressed by the Phase-2 Upgrade is an improved trigger capability necessary to maintain a sustainable trigger rate for the higher pile-up environment. The enhancement of the trigger performance consists of an improved discrimination of event selection and higher output rate of those interesting events [4].

The improvement in discrimination ability to the L1 trigger will be achieved by providing tracking information for the trigger decision and increasing the latency to allow for the

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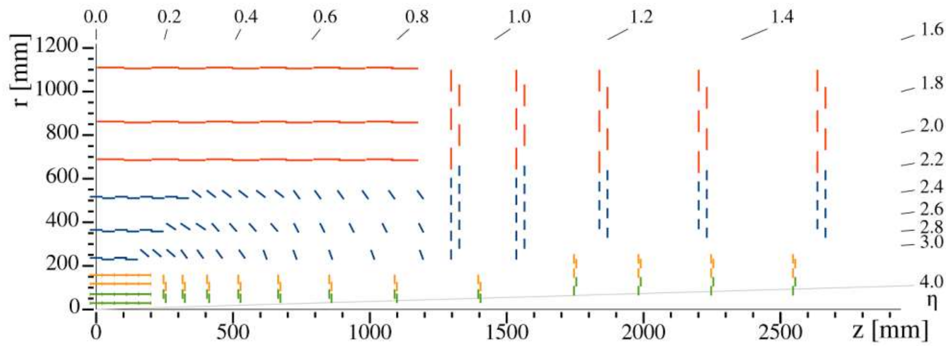

Figure 3.3: One quarter of the Phase-2 tracker layout [4]. The Outer Tracker p_T-modules are represented by the red and blue lines, which are the 2S and PS modules respectively. Green and orange lines are the Inner Tracker modules.

additional processing time. This means that the tracker must provide continuous tracking information to the L1 trigger system at a 40 MHz rate.

While the two-tiered triggering concept of L1 trigger and HLT will remain, the L1 trigger rate will be enhanced from 100 kHz to 750 kHz. The latency, i.e., the maximum duration available for an L1 trigger decision to be made, will be increased from 3.2 µs to 12.5 µs.

The provision of track information to the L1 trigger will be implemented in the outer layers of the tracker referred to as CMS Outer Tracker. The Outer Tracker will be populated by layers of p_T-modules, which have the capability to reject signals from particles based on their transverse momentum.

3.3.2 Tracker Upgrade

A larger pile-up and particle density calls for higher detector granularity in order to provide a good track reconstruction. The higher granularity will be achieved through the use of shorter strip lengths and increasing the amount of sensor modules.

A view of the tracker layout and its modules can be seen in Figure 3.3. The Inner Tracker, the section within $r < 20$ cm from the interaction point and populated with pixel sensors, will use smaller pixels and thinner sensor substrates. The coverage of the Inner Tracker will be improved to pseudorapidity $|\eta| < 4$ through the spatial arrangement of its sensor modules. The Outer Tracker will feature pixel sensors in one of its two p_T-module types for the first time. The two module types will both implement the L1 trigger functionality and in total 5616 units of the PS module and 15 360 units of the 2S module are planned to be installed in the Outer Tracker.

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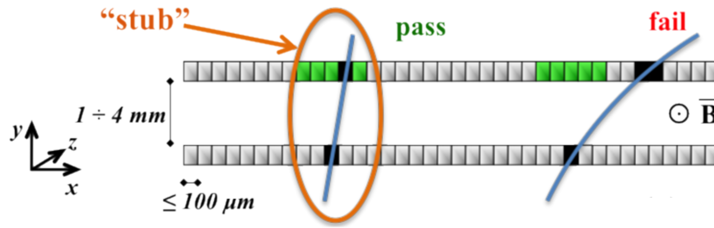

Figure 3.4: Concept of the stub finding process [4]. Tracks of charged particles are deflected in the transverse xy-plane by lorentz-force interaction with the magnetic field.

p_T-module Concept

The requirement of providing tracking information to the L1 trigger and local data reduction at the stage of the front-end electronics are the main drivers of the design for the p_T-modules [4]. These tasks are accomplished through the correlation of signals from two single-sided closely-spaced sensors: sensor hits are correlated into hit pairs which are discriminated by the particle p_T. Pairs of hits which fulfill the p_T-threshold are called "stubs". The concept of the p_T-modules is illustrated in Figure 3.4.

A charged particle p_T is correlated with the distance between two hits in the transverse plane, as tracks of charged particles are bent in the transverse x-z plane by the 3.8 T magnetic field. The curvature of the track is inversely proportional to the particle transverse momentum p_T, i.e, the higher the momentum, the straighter the trajectory. As a particle passes the first sensor plane, a narrow search window is applied in the second sensor plane. If a second hit is measured within the window above the first, the stub event is generated and its coordinates are transmitted for processing to the L1 trigger. The full event information is stored for the duration of the latency and transmitted upon request by an L1 trigger signal (L1 data). The bending threshold that is set for p_T-discrimination is tunable to a certain degree and corresponds to around 2 GeV [4].

The two p_T-module types, the PS and 2S modules, populate the Outer Tracker layers [4]. The PS modules combine a macro-pixel and strip sensor and will be deployed in the layers closer to the interaction point, between $20\,\mathrm{cm} < r < 60\,\mathrm{cm}$. The 2S modules use two strip sensors and will be located in the outer layers of the Outer Tracker, between $60\,\mathrm{cm} < r < 120\,\mathrm{cm}$. The use of a pixelated sensor in the PS module is explained by the fact that the strip sensors are aligned in the z-axis direction, which limits the resolution of the $z(r)$ component of the particle trajectory to the length of the strip. Using pixelated sensors in the inner layers of the Outer Tracker provides a sufficiently precise z measurement to discriminate primary vertices between simultaneous particle tracks.

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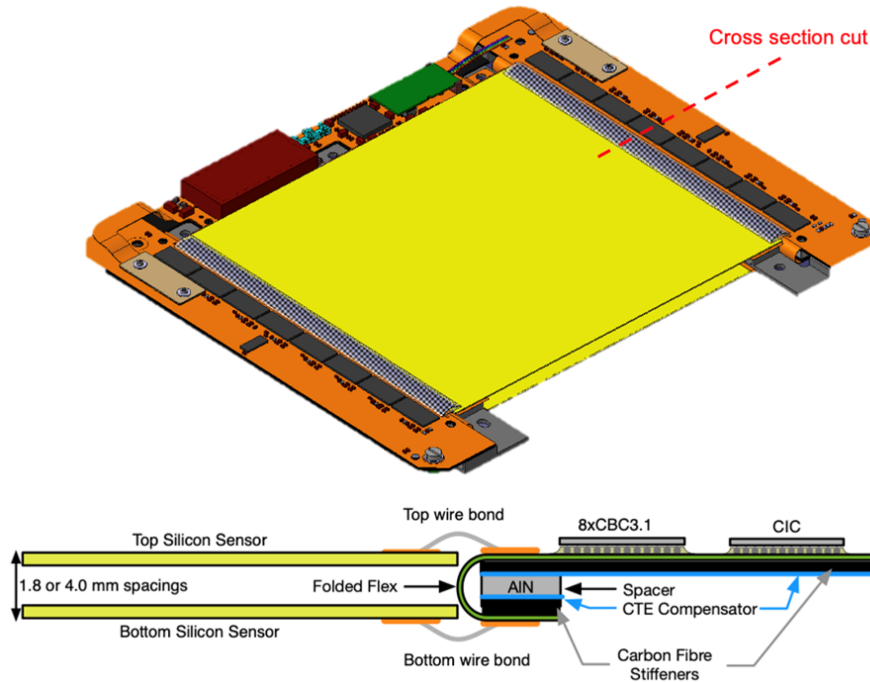

Figure 3.5: Rendering of the assembled 2S module (top), and sketch of the cross-section cut showing the connectivity of the assembly (bottom) [25].

2S Module Structure

The 2S (two-strip) module is shown in Figure 3.6. It consists of two strip sensors spaced a few millimeters apart. Each strip sensor consists of two rows of strips, each with a length of 5 cm and pitch of 90 μm. This results in 2032 strips per sensor with a total sensor size of 10 cm $\times$ 10 cm. The strips are read out by the CMS Binary Chip (CBC), which processes signals from 254 strips per chip and implements the L1 trigger functionality, i.e. provides stub (trigger) data and L1 data [23]. Each CBC is connected to both sensors with wire-bonds being connected alternatingly to top and bottom sensor. On two sides of the modules a PCB sub-assembly, called the FE-Hybrid, features 8 CBCs and one Concentrator ICs (CIC) each. The CIC aggregates data from the 8 CBCs and further transmits them to the so-called service hybrid [24]. For further reduction of the stub data rates, the CIC implements sorting algorithms to select stubs based on their bending value before transmission to the detector back end. The service hybrid hosts the modules for high speed optical link transmission to the detector back-end.

PS Module Structure

The PS (Pixel-strip) module is shown in Figure 3.6 featuring the strip and macro pixel sensors and their respective read-out ASICs. The strip sensor (PS-s) consists of 2 $\times$ 960 strips, each strip with a size of 2.4 cm $\times$ 100 μm. The pixel sensor (PS-p) consists of a

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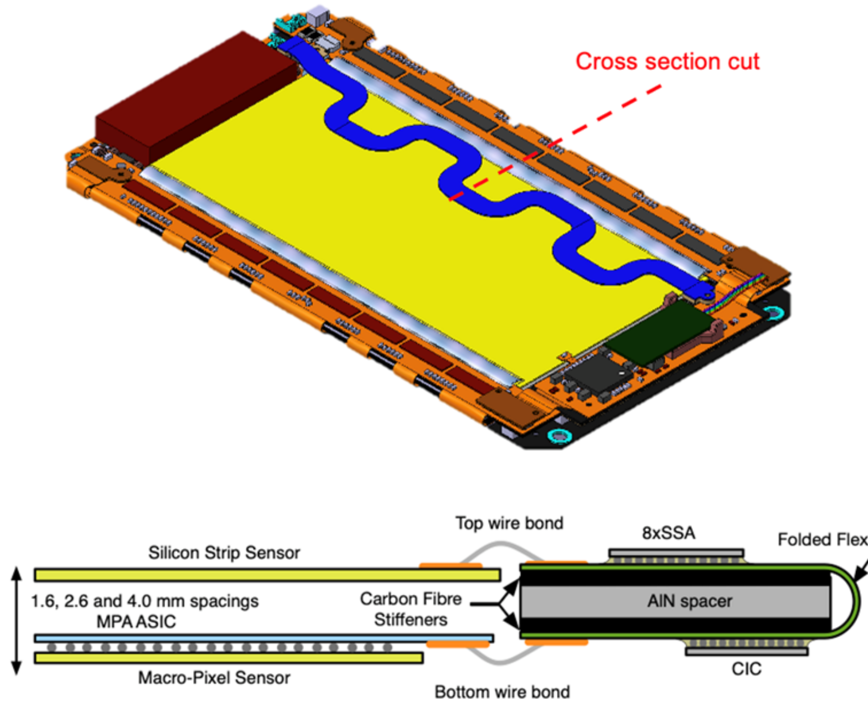

Figure 3.6: Rendering of the assembled PS module (top), and sketch of the cross-section cut showing the connectivity of the assembly (bottom) [25].

sensor array of 32×960 pixels, each pixel with a size of 1.5 mm $\times$ 100 μm. The sensor planes are spaced apart in three different configurations (1.6 mm, 2.6 mm and 4.0 mm) depending on the location of the specific PS module in the Outer Tracker layout. The total size of both sensors is 10 cm $\times$ 5 cm, only half the surface size of the 2S sensor. The signals of each sensor are read-out and processed by two different read-out ASICs: the Short-Strip ASIC (SSA) [26] is connected via wire-bonds to the strips of the PS-s and the Macro-Pixel ASIC (MPA), described in Chapter 4) is bump-bonded to the pixels of the PS-p. Both read-out ASICs directly interface with each other. The SSA transmits centroid hit coordinates from 120 strip cells to the MPA continuously, while storing detailed event information. The MPA correlates particle hits into stubs and transmits these as trigger data to the L1 trigger. Upon reception of an L1 trigger signal, a full event read-out from the SSA and MPA is triggered, where the MPA encodes raw data from both chips into so-called L1 packets. The CIC is used in the PS module for data aggregation as well. Two CICs aggregate data (stub and raw hit information) from 8 MPAs respectively and interface data towards optical link transmission modules.

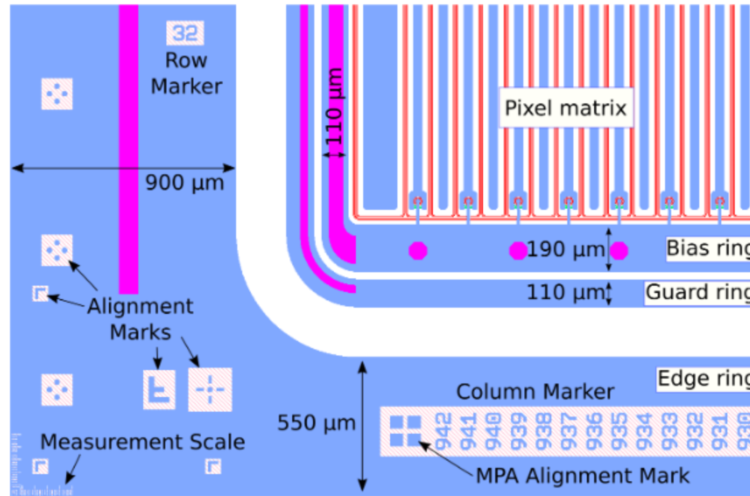

Figure 3.7: Edge of the PS-p sensor layout. [6]. The blue aluminum layer contains various identification and alignment markings. Passivation openings for contact purposes are marked in purple. In the pixel matrix, pixels surrounded by p-stops and their PTS to establish the bias potential are visible.

Pixel Sensor

The development and design choices for the macro pixel sensor of the PS module, named PS-p, are described in [6]. Multiple prototypes and layout variations of the PS-p were produced and studied. The layout of a standard PS-p is shown in Figure 3.7. It is similar to the baseline sensor layout shown in Figure 2.2, however with DC-coupled pixel cells instead of strips and biasing accomplished through PTS. The PS-p is processed on float zone silicon material. The choice of the sensor polarity is based on studies showing a higher charge collection and robustness after irradiation compared to p-in-n sensors. The thickness of the sensor was initially targeted to be 200 µm, as it would exhibit reduced leakage currents, require smaller depletion voltages and incur less radiation-induced degradation of its charge collection. However, it was observed that 200 µm-thick sensors are very sensitive to scratches and early breakdown, so the final sensor PS-p thickness was decided to be 320 µm. The target PS-p operating bias voltage will be 600 V. Even after irradiation of up to $1.5 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$, the PS-p is able to provide a most probable collected charge signal of $\sim$8000 e^- for MIPs to the MPA pixel FEs [27].

Material Budget and Power

The quantity of the material used in the Tracker represents a limiting factor in the detection efficiency, as particles lose energy by the volume of material they cross. Therefore, strict material budgets are levied on the construction of the detector systems. These material budgets particularly constrain the capabilities of and the material allowed for power distribution and cooling systems. Transposed as power budget requirements for

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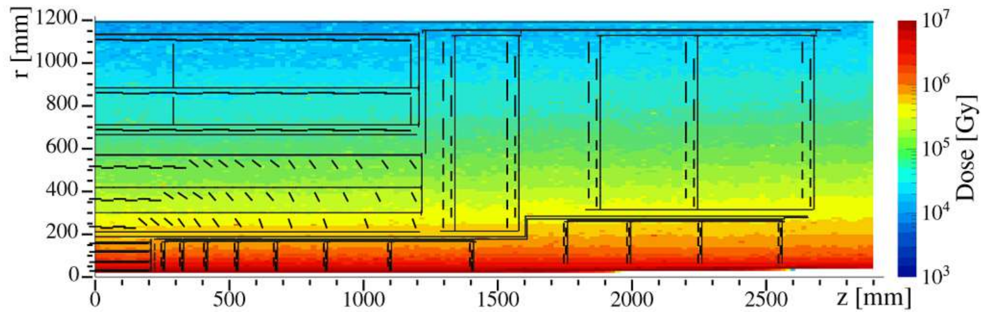

Figure 3.8: TID for the Phase-2 tracker [4]. These estimations were generated using the CMS FLUKA simulation software.

the PS module ASICs, the MPA and SSA are allowed a power consumption of 200 mW and 80 mW respectively [4].

Radiation Levels

The upgraded tracker is required to function nominally up to an integrated luminosity of 3000 fb^{-1}, which is expected to be reached after around 10 years of HL-LHC operation [2]. No maintenance or replacement of the Outer Tracker is possible during this period. Thereby, the TID delivered to modules in the tracker will reach unprecedented irradiation levels for integrated electronics, e.g., up to 1200 Mrad (12 MGy) for modules in the Inner Tracker [4]. The expected radiation levels are a key challenge to be addressed in the design of all electronics within the tracker.

Depending on the radial distance to the interaction point, the Outer Tracker p_T-modules will experience different levels of TID over their lifetime. Figure 3.8 shows the expected TID as function of the location in the tracker. The expected maximum TID levels for the PS modules in the Outer Tracker are around 100 Mrad. As such, electronics to be deployed in the Outer Tracker are designed using radiation-hardening techniques. Furthermore, their functionality in such harsh environments needs to be guaranteed and verified through testing in appropriate irradiation studies.

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4 MPA - Hybrid Pixel Readout Chip

The Macro Pixel ASIC (MPA) is the pixel read-out ASIC for Phase-II CMS Outer Tracker upgrade. As described in 3.3, the MPA and SSA fulfill the p_T-module concept for the PS-module. The MPA reads out hit data from the macro-pixel sensor, digitizes it and stores the pixel L1 data. It processes input strip trigger data from the SSA and pixel trigger data, rejects low-p_T hits and transmits stub events synchronously with the 40 MHz BX rate. The L1 pixel data is stored for a latency of 12.8 μs and, upon request by an L1 trigger signal, is encoded and transmitted together with the L1 strip data to the detector back-end systems. While defined at 750 kHz, the MPA is able to accommodate a L1 trigger signal rate of 1 MHz. Due to the harsh radiation environments and stringent material budget of the Outer Tracker, the MPA is expected to operate under a TID of up to 100 Mrad and is allowed a maximum power consumption of 200 mW.

Both, the MPA and SSA, are implemented in 65 nm CMOS technology with radiation-tolerant and low-power design techniques in mind. In the case of the MPA, an initial silicon prototype with a reduced pixel-array size, named the MPA-light, was developed to study the analog front-end architecture and binary read-out chain [28]. Based on the learnings, a full-size prototype, the MPA1, was developed and characterized [29]. After expanding the functionality with additional features, improving the radiation-tolerance, and solving previously uncovered issues, a final prototype named MPA2 was developed.

This chapter aims to describe the various functionalities of the MPA in order to support the reasoning for the testing and characterization procedures performed for the MPA2 (presented in Chapter 5). As the specification of the CMS Phase-2 upgrade poses strict requirements for the performance and capabilities of the MPA, important aspects in the design and implementation towards low-power usage and radiation-tolerance will be highlighted.

Figure 4.1 shows the top level architecture of the MPA chip as a block diagram. It illustrates the various partitions of the chip, e.g., in terms of the analog and digital processing paths, the various clock domains, the pixel array and the periphery block. Key functionalities are shown as blocks connected by the input/output paths and explained in the following sections. The available input and output channels for control signals and data transmission of the chip are shown in the IO[1] block on the bottom.

[1] Input/Output

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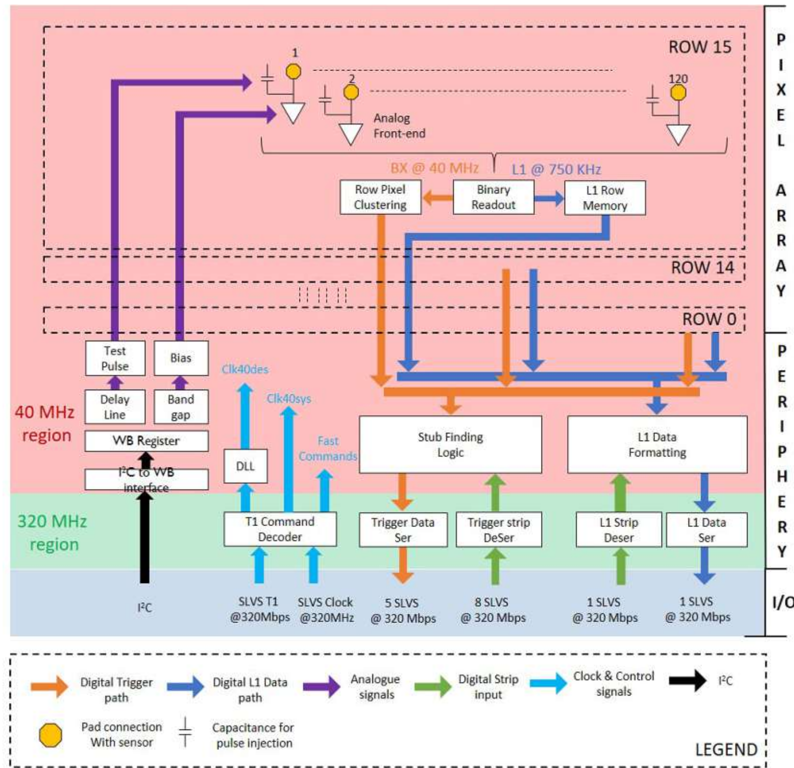

Figure 4.1: Block diagram of the top level architecture of the MPA [4].

4.1 Dimensions and Floorplan

Figure 4.2 shows an image of the MPA2 and its dimensions. The physical dimensions of MPA1 and MPA2 are equal. Due to the large size of the PS-p pixel sensor, 16 MPA ASICs are required to read out a single sensor. The total size of an individual MPA ASIC is $11.9 \times 25.2\,\mathrm{mm}^2$. The chip is divided into the periphery part and the pixel array region. The pixel array has 16 rows with 118 columns with a pixel cell size of $100 \times 1447\,\mu\mathrm{m}^2$. While the size of a standard pixel cell is limited by the granularity requirement, the maximum size of the ASIC is constrained by the maximum reticle size limit of the manufacturer. Each pixel cell contains an individual read-out circuit for initial sensor signal processing and a staggered bump pad to connect to the sensor. The periphery block extends beyond the sensitive pixel array. It contains input/output pads and many global functionalities of the chip, such as configuration, hit processing, and bias circuitry.

Considering the orientation of an untilted PS module in the tracker barrel of the CMS detector, the MPA rows are aligned to the x-axis and the columns to the z-axis (i.e., the beam direction) of the coordinate system. The pixel size aspect ratio is considered untypical for pixel detectors, as the available resolution differs drastically between the

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two axes.

Due to spacing between the individual chips, the first and last column of the pixel sensors will not be connected to the read out cells. These unconnected pixel sensors are shorted to their neighbouring pixel sensor cell. This way, no active sensor area is lost. However, the pixel at the edge of the each row is doubled in size.

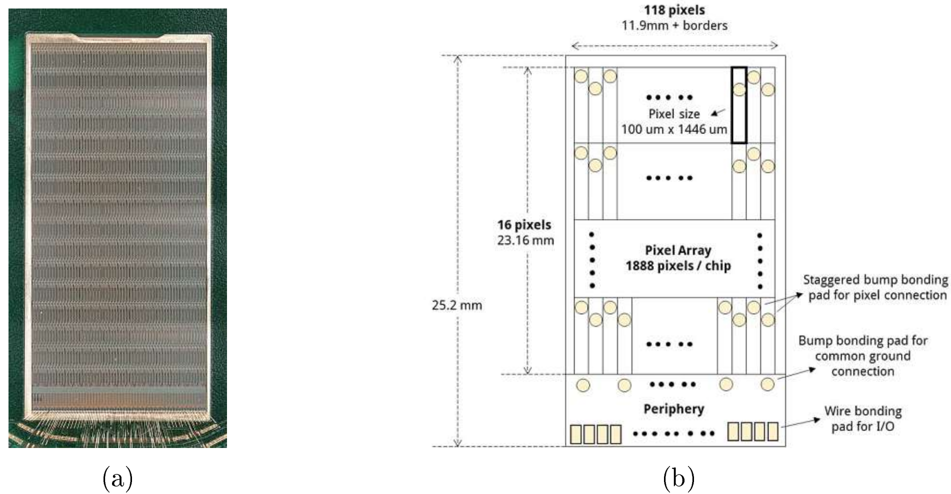

Figure 4.2: Image of the MPA2 wire-bonded to a carrier board (a) and a schematic showing its dimensions and electrical connections (b).

4.2 Chip Control Architecture

The MPA offers two interfaces for the control and configuration of the chip. These are the I2C configuration and the fast control of which the functionality is described here. The reception and decoding of the I2C and fast control interface is located in the periphery of the MPA2, as shown respectively by the black and light-blue paths in Figure 4.1. The input clock and the clock architecture is also described here.

I2C Configuration

The MPA uses an I2C serial communication bus for the addressing and monitoring of its configuration registers. The I2C interface for the MPA is a communication bus standard which follows the Philips Semiconductor I2C specification. However, it implements only a subset of those features. It was devised to be used by all ASICs for the CMS Outer Tracker and can be used to address individual components across the PS module. The implemented I2C interface is specified in detail in [30].

For the access to internal configuration registers, the chip implements an I2C Slave-Wishbone master which allows to further control the various wishbone slaves (e.g., pe-

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riphery, row and pixels) per chip [**SoCInterconnectionWISHBONE**]. The implemented Wishbone protocol addressing scheme is based on 16-bit addressing and 8-bit data for read/write access to internal registers of the chip. The configuration registers of specific rows or pixels can be addressed individually or chip-wide. Configuration registers are available for read and write operations, whereas certain registers are implemented exclusively for monitoring purposes and are therefore set as read-only. I2C transactions to the MPA can be issued by up to 1 MHz.

Fast Control

The MPA fast control interface provides inputs for a reference clock and fast commands necessary for the basic operation and synchronisation of the chip. To facilitate this, the following signal inputs are available:

- A differential clock with a nominal frequency of 320 MHz
- A differential command line for encoded fast commands at 320 Mbps

Both, the fast command and reference clock differential lines are provided by the PS module. Due to the structure of the module, these signals are physically routed through the SSA before arriving at the MPA. The fast commands, also called T1 commands after their input line, are 8-bit encoded words which can be provided to the MPA at a 40 Mhz frequency. The four main commands and their functions are listed in Table 4.1.

T1 commands	Description
Resync (or Fast Reset)	Clears memories and resets control states
L1-Trigger	Triggers read-out of the L1 data
CalPulse	Initiates a test pulse
Counter Reset	Resets the L1 Counter and the BX counter

Table 4.1: Available fast commands for the operation of the MPA.

Clock Distributions

The MPA implements four clocks for different domains of the chip. The communication domain uses a 320 MHz, called Clk320c, that is externally provided through the fast command interface.

From the Clk320c clock signal, the chip generates three 40 MHz clocks for various purposes, called Clk40, Clk40s and Clk40d. The first, Clk40, is used for the I2C bus transactions and data transmission lines. Clk40d is used for the core internal logic of the chip and its phase can be adjusted through I2C configuration. Clk40s is used exclusively for the sampling of the pixel FEs and originates from Clk40d. In order to move the sampling point of the analog FE pulse, the phase of Clk40s is controlled by a configurable delay-locked loop (DLL) with a range of 0 ns to 25 ns. This adjustability of the sampling phase is provided in order to adjust for chip-to-chip variations and time-of-flight compensation to provide a uniform sample time in the tracker operation.

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Power Supply Domains

The MPA is specified to use three different supply voltages for its operation. The three are referred to as analog (AVDD), digital (DVDD) and periphery (PVDD). VDD signifies the positive drain voltage provided to the CMOS transistors. The supply voltages and their minimum, maximum and typical levels are listed in Table 4.2.

Domain	**Name**	**Min.** (V)	**Typ.** (V)	**Max.** (V)
Digital	DVDD	0.9	1	1.32
Analog	AVDD	1.2	1.25	1.32
I/O	PVDD	1.2	1.25	1.32

Table 4.2: MPA voltage domains and their typical levels.

AVDD is provided to the the analog front-end circuits in each of the pixel cells, while DVDD encompasses complete digital architecture, i.e., the binary read-out, hit processing, control/configuration, I/O serializers of the chip. Finally, PVDD drives the I/O pads.

4.3 Pixel Front End Electronics

The Front-End (FE) circuitry is implemented for each cell in the pixel array of the MPA. Each FE processes the analog pulse signals originating from a respective pixel sensor and digitizes them as hit information for further processing.

Analog FE unit

The analog chain of the FE is shown as a block diagram in Figure 4.3. It resembles closely the generic analog FE circuit for pixel detectors described in Section 2.3.1. As such, its main component blocks are the pre-amplifier, a shaper and a discriminator. The complete schematic and design of the analog FE unit is described in more detail in [28].

The pre-amplifier is a charge sensitive amplifier (CSA) with a Krummenacher feedback loop, which is capable of compensating a sensor leakage current of up to 200 nA and has a nominal gain of 95 mV/fC. The shaper stage is a differential amplifier and integrator. The discriminator consists of a high-gain differential amplifier followed by a differential to single ended stage. The global threshold for the discriminator is provided by a high impedance current source which mirrors the output current from the 8-bit Threshold DAC[2] (ThDAC). Similarly, the local per-pixel 5-bit Trimming DAC is connected to the second differential input of the discriminator.

[2] DAC, Digital-to-Analog Converter

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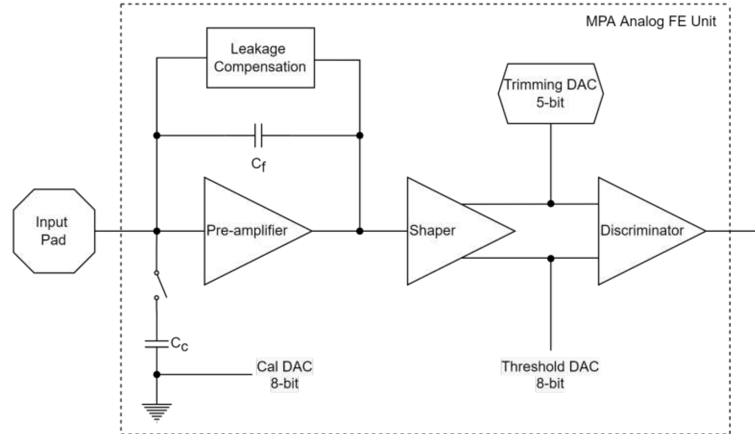

Figure 4.3: Block diagram of the MPA per pixel analog FE unit, composed of the pre-amplifier, shaper and discriminator blocks. Its circuit remains identical between the different MPA prototypes.

The calibration circuit provides the control of test charges to be injected. The calibration capacitor C_c allows for the transmission of the test charges (analog CalPulse) to the front-end input through a CMOS switch. This switch can be individually controlled per pixel FE. The C_c capacitance is 20 fF and the amplitude of the injected charge is set with the voltage applied by the 8-bit calibration DAC (CalDAC) by $Q_{inj} = C_c V_{CalDAC}$. The gain of the CalDAC is expressed in terms of input LSB of the DAC and the resulting charge injected. Based on simulation of the analog FE during its design, it is around $0.035\,\mathrm{fC/LSB_{CalDAC}}$. Thereby the calibration circuit allows injected charge amplitudes of up to $45 \times 10^3\,\mathrm{e}^-$.

Charges in the order of $14\,000\,\mathrm{e}^-$ are considered for an MIP hit in the PS-p pixel sensor under optimal conditions and a bias voltage of 600 V [27]. The MPA analog pixel FEs are designed around a minimum threshold of $Q_{thr} = 0.5\,\mathrm{fC}$ ($\sim$3000 e^-) referred to as nominal threshold. Its value is based on possible charge-sharing of a particle hit between pixel cells and an expected radiation-induced degradation of the charge collection efficiency of the sensor. The conservative estimates indicate that the nominal threshold set in the MPA should meet a hit efficiency of 99.5 %. The threshold of the discriminator is set by the ThDAC, which has a simulated gain of $1.4\,\mathrm{mV/LSB_{ThDAC}}$. As an example, to set the nominal discriminator threshold for charges of 0.5 fC and by taking into account the pre-amplifier gain, the corresponding ThDAC value would be 32 LSB. However, by setting this threshold globally across all pixels, the actual thresholds of the individual pixel analog FEs will vary between each other. This threshold variation can be equalized by a threshold tuning technique, which is further detailed in Section 5.2.4.

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Binary Read-out

For each pixel, the discriminator output is further processed by a digital pixel back end. This block implements the binary read-out (BR) of the pixel sensors and acts as the interface between the pixel FEs and the digital hit processing architecture. Its schematic is shown in Figure 4.4. Although only 118 analog FE units exist per row, there are still 120 binary read-out channels per row. The read-out of the edge pixels (pixel 1 and 118) is duplicated per row in order the match the 120 channels of the SSA.

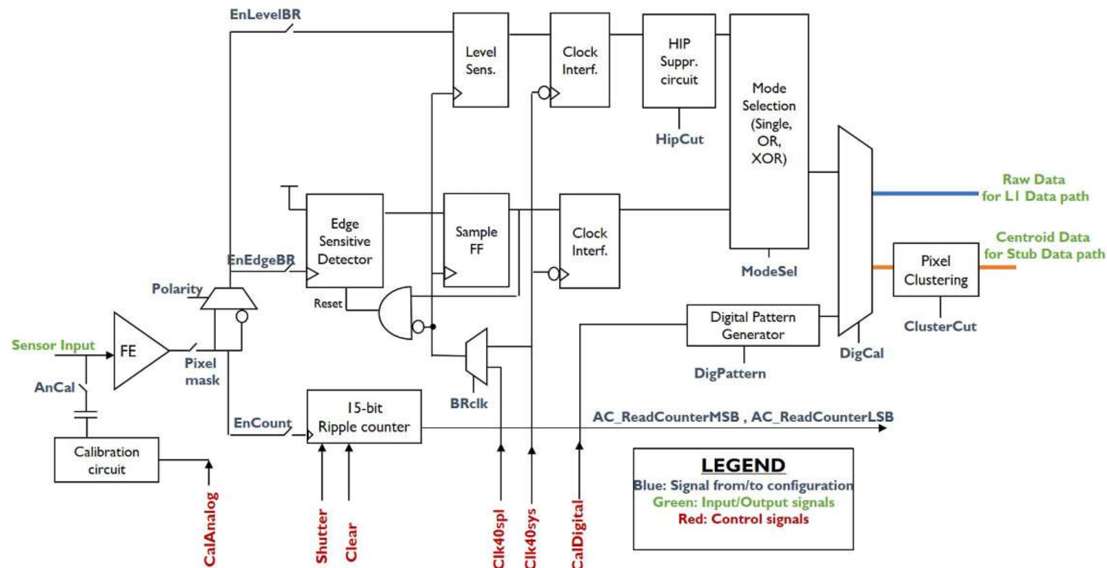

Figure 4.4: Schematic of the MPA digital pixel back end [31]. The binary read-out is possible by three acquisition methods: the asynchronous ripple counter (EnCount) or the edge and level sensitive synchronous readout paths (EnLevelBR and EnEdgeBR). The input signal is either provided by an attached sensor or by the calibration circuit.

First, a pixel mask can be applied to rectangular pulses of analog FE output to enable/disable the channel. Three distinct acquisition modes are available:

- Asynchronous 15-bit Ripple Counter ('EnCount'): Counts every rising edge of the discriminator output. This asynchronous readout is started by opening a shutter controllable by a fast command which starts the ripple counter. Once the shutter is closed, the counter value can be read out by the I2C wishbone interface. This mode is required for the calibration and testing purpose of the analog FE unit, e.g., by the threshold trimming process (see Chapter 5).
- Synchronous Edge Sensitive ('EnEdgeBR') and Level Sensitive ('EnLevelBR') read-out: Both these read-out modes sample the discriminator output at a 40 MHz sampling rate and associate the ToA of the pulse with the appropriate Bunch

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Crossing Identification Data (BX ID). The difference between the two modes is found at the first stage of their signal digitization. As long as the threshold is crossed by the analog pulse, the discriminator outputs digital HIGH. This signal is sampled against the Clk40s sampling clock and the level sensitive read-out goes to HIGH for the amount of clock cycles that the discriminator output is HIGH as well. The edge sensitive read-out generates a single cycle HIGH pulse at the rising edge of the sampling clock. In the case of the level sensitive mode, an optional highly-ionizing-particle (HIP) suppression circuit can be enabled to limit the output signal for a set number of cycles ('HipCut').

Every acquisition method can be enabled independently through the chip configuration and is executable simultaneously. The edge and level sensitive binary read-out modes are selected independently by OR-ing or XOR-ing the output depending on the mode selection configuration value (ModeSel). The binary read-out data is then further passed to the hit processing architecture (the L1 data and stub data paths are described in Section 4.5).

For the testing purposes of the hit processing architecture, the binary read-out modes can also be completely disabled in favor of injecting 8-bit digital patterns. This is done by enabling the digital pattern generator and setting a pattern through the chip configuration ('DigPattern'). The digital injection sequence lasts 8 BX cycles and is started by sending the digital calibration pulse command (digital CalPulse).

4.4 Bias Structure

The bias structure of the chip is split into seven identical bias blocks which each provide bias levels to 16 or 18 pixel columns at once. The replication is done due to the large size of the MPA and to ensure the bias values are as consistent as possible across the pixel array. The individual bias blocks provide reference signals in form of several voltages and currents required by analog pixel FEs. Among others, these include reference and bias signals for the analog FE, for the Calibration or Trimming DAC. The individual biases and nominal values are listed in Table 4.3.

A schematic of the MPA bias block structure is shown in Figure 4.5. A bandgap reference circuit provides the bandgap reference voltage [32]. The generated voltage is temperature compensated. Furthermore, the used extraction circuit is designed to be as robust as possible towards variations process, voltage, temperature (PVT) as well as radiation. The generated bandgap reference voltage is around 285 mV, from which the bias levels are then further derived. In each individual bias block, the bandgap voltage is distributed to six voltage-to-current converters (V2I) which in turn each supply a 5-bit DAC. These DACs are used to further adjust the bias levels to their nominal values, as they may deviate due to PVT variations as well.

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TEST n	DAC	Bias Description	Nominal value (mV)
0	A	Krummenacher feedback (80 nA)	82
1	B	Pre-amplifier (15 µA)	82
2	C	Trimming DAC range 48/108/172	48/108/172
3	D	DAC for voltage biases	82
4	E	DAC for current biases	82
5	E	Threshold DAC (ITH)	−10 to 370
6	E	Calibration level	0 to 450
7	/	Local reference (GND)	−10 to 10

Table 4.3: Bias DACs names, purpose and nominal values. Nominal values are listed as they are expected to be measured at the test pad.

An analog multiplexer in each bias block allows to probe the voltage levels of the individual DACs on an external I/O pad (also referred to as test pad measurement). This can be used to calibrate the individual DACs to their nominal value and also calculate the DAC resolution, i.e., the least significant bit (LSB) fo the DAC. This functionality is part of the monitoring block, which is further described in Section 4.6

4.5 Data Processing

The read-out architecture for hit processing in the MPA is characterized by the two distinct data paths: the L1 and stub finding path. Both paths process the binary read-out information from the 1920 channels of the pixel array at a 40 MHz rate. Figure 4.6 shows the fundamental blocks of the two read-out paths of the PS module. In this section, the stub finding and L1 data process are described as implemented in the MPA. Description of the data processing blocks in the SSA are not explicitly handled in this work and can be found in [33].

4.5.1 Stub Finding Path

The stub finding path continuously provides high-p_T hit information in form as stubs to the L1 trigger (therefore, also referred to as trigger data). The stub data includes the hit position coordinate of a particle in the pixel array and a p_T estimation. This p_T estimation is based on the bending value of the particle hit between strip and pixel sensor planes. As such, the stub finding logic comprises numerous computations, all operating at a 40 MHz frequency, making it a power intensive process where trade-offs between reduction of data transmission versus the stub efficiency are considered.

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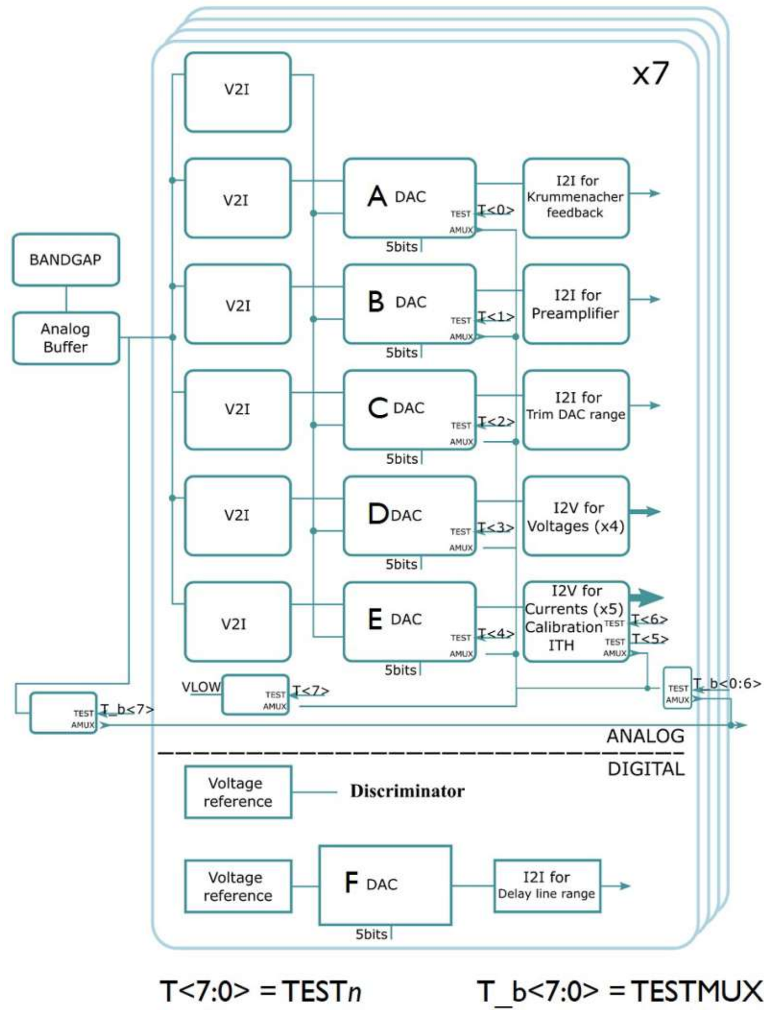

Figure 4.5: MPA Bias block structure [31].

Row Pixel Clustering

The first step towards the generation of stubs following the binary read-out is the row-local pixel clustering (shown by Figure 4.6 in the orange path of the MPA). Clusters are pixel hits which are adjacent. They may occur across a pixel row by low-p_T particles with a strongly bent trajectory that passes through multiple pixels. Clusters also may occur by high-p_T particles which cause cross-coupling between two pixels. To prevent further processing of uninteresting larger clusters caused by low-p_T particles, the row pixel clustering is able to reject clusters which exceed a configurable size. The real incident coordinates, the centroids, which are defined as the center of a pixel in the single cluster case, are extracted and passed on as binary matrix for clusters which are not rejected. As for cluster sizes of even numbers, the centroid falls between two pixels. To handle

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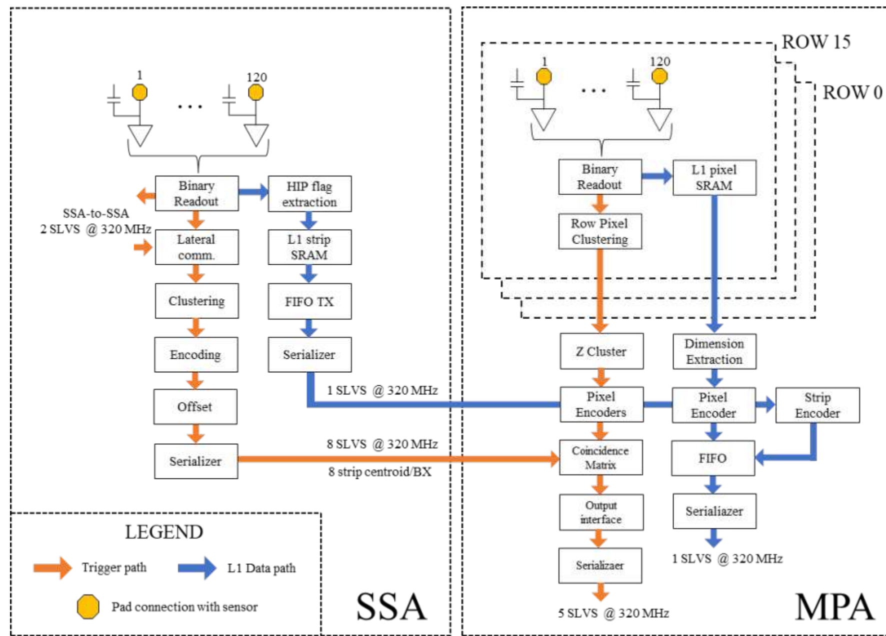

Figure 4.6: L1 data (blue) and stub finding (orange) read-out paths of the MPA and SSA [4].

these cases, an additional bit is added per two pixels to indicate that the centroid falls between the two. With that, the per-row 120 bit vector indicating the centroid positions is expanded to 180 bit which includes the so-called "half-pixel" resolution.

Z Cluster and Pixel Encoding

The periphery logic receives the unsparsified 180×16 pixel centroids a as binary matrix, amounting to total a data rate of 76 Gbps. As a first step, Z clustering is performed, where column clusters larger than two are rejected. For a cluster of size two, the coordinate closer to the periphery of the chip is selected as column centroid out of convention. From this stage onwards, the binary hit matrix is sparsified and encoded into coordinates. A per-row pixel encoder encodes the column coordinate of the centroid based on a binary tree of OR-gates inspired by the MEPHISTO chip [34]. It takes the 180 bit long centroid vector as input and extracts up to four centroid column positions per BX, encoding each in an 8 bit value. These centroids are totalled over the rows, amounting to 64 centroids per BX being passed to a priority encoder. The priority encoder selects up to 8 pixel centroids with priority to centroids with closer proximity to the periphery out of convention, each encoded as 12 bit value (4 bit for the row, 8 bit for the column position). The 8 pixel centroids per BX are passed to correlation logic, the characterizing feature of the stub finding process.

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Stub Correlation Logic

Before hit correlation can be performed, the strip trigger data needs to be received. Strip trigger data is transmitted by the SSA to the MPA as 8 strip centroids per BX. A strip centroid, the center coordinate of a strip cluster, is one of the 120 available strip coordinates encoded as 8 bit value[3]. The coincidence logic accepts the 8 pixel and 8 stub centroids per BX. The bending of the hit pairs, defined simply as x-axis distance between pixel and strip centroids, can now be computed. This computation is performed by a coincidence matrix, where each possible combination of the 8 pixel and strip centroid distances are computed in a matrix multiplication fashion. Finally, a maximum threshold for the x-axis differences is applied in order to select stub events. This bending window, or also called stub window, is configurable to compensate for the position and orientation of the PS module within the detector. Simulations for the selection of the stub window and the relation between bending and particle momentum can be found in [4].

The resulting stub information is packaged and serialized for transmission at a rate of 5 stubs regrouped over two consecutive BX. Selected stubs are comprised of the row coordinate of the pixel centroid (representing the z-information) and the strip centroid coordinate (representing the x-information.). The bend information is included as the x-axis difference. The averaging of five stubs over two BX is necessitated by the capabilities of the MPA and CIC stub processing. Given by the fact that 15 bit are needed to encode the stub information, the MPA may only transmit up to two stubs per BX with the available stub lines, whereas the CIC can process up to three stubs per BX per MPA. To optimize the available bandwidth, averaging of stubs over two BX is done while still being a sufficient rate of transfer for the CIC stub sorting process. The MPA indicates the BX a stub belongs to by an additional bit provided in the total stub data packet. The stub data format and transmission rates are described in Section 4.5.3.

Besides the normal operation, additional debug modes are available for the stub processing logic. A pixel-pixel mode allows to operate the MPA without the strip input, where the output stubs include only pixel centroids and no bending information or strip coordinates are included. Alternatively, the strip-strip mode, allows to bypass the coincidence logic to verify the received strip input. In the latter case, the MPA sends stubs packets containing only strip centroid positions and no pixel centroids or bending information. This mode of operation can be used for data alignment purposes between the SSA and the MPA.

4.5.2 L1 Data Path

The L1 data path is the triggered read-out path which stores pixel hit events for the L1 latency. Upon reception of the L1 trigger signal, the zero-suppressed raw hit information of pixel and strips are transmitted to the detector back end. The functionality can be seen as divided into two main functionalities, namely event storing and processing.

[3] The full strip cluster information is stored in the L1 memory in case of an L1 trigger reception.

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L1 Memory

Each pixel row includes an L1 memory. The L1 memories, which are implemented as static random-access memory (SRAM), store the unsparsified hit data of all 120 pixels of the respective row. Figure 4.7 shows the SRAM circuit schematic implemented in the MPA. The SRAM can store up to 512 events where one event per BX is stored as a 128 bit word. The depth of the SRAM accounts for the maximum L1 trigger latency of 12.8 µs.

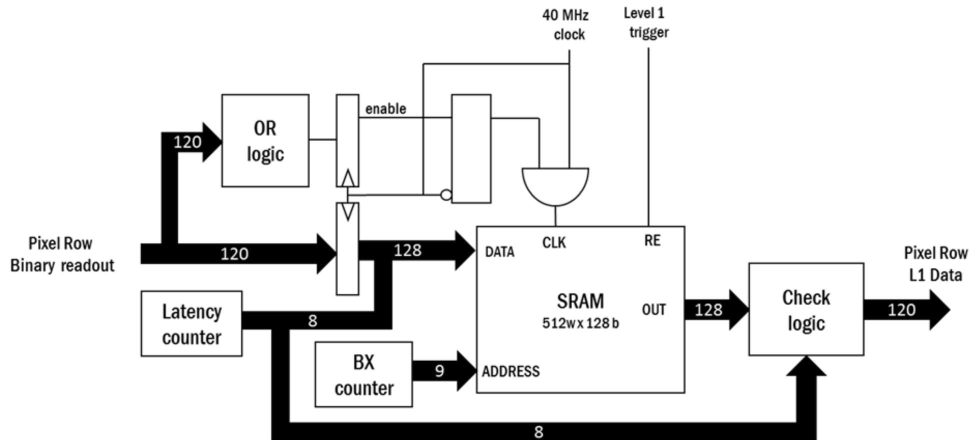

Figure 4.7: Schematic of the SRAM circuit implemented to facilitate L1 event storage per pixel row [28].

Considering the average particle occupancy for the MPA of around 1 %, the SRAM would be filled with a majority of zero events. To prevent this and on the other hand reduce the power consumption, a memory gating technique is implemented. For this, an OR-logic applied to the event data results in the SRAM only being enabled and written when a pixel hit is present.

Based on the fixed L1 latency of 12.8 µs, the SRAM can be operated in a cyclical fashion by the BX counter that provides the address to be written. The 9-bit BX counter increments for each BX and resets after reaching the value 512, which in turn increments the latency counter. The read address pointer is offset in respect to the BX write pointer by the L1Offset value that represents the L1 latency period. Each event word is expanded by the latency counter value (L1 ID) when written into the memory. As soon as the chip receives an L1 trigger, the event at the read pointer is read and its latency value is checked against the current latency counter value. If they match, i.e., the event was generated within the L1 latency period in which the trigger was received, the event is passed on to the periphery. An event with all zeros is sent if the latency values do not match. The checking is performed due to the memory gating, as consecutively stored events possibly may not have consecutive L1 counter values. A stored event is discarded if no trigger is received within the 12.8 µs L1 latency, as the BX counter simply overwrites older events.

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L1 Data Encoding

On the reception of an L1 trigger signal, the MPA periphery collects the data of all 16 row memories, encodes the hits and composes a L1 data packet together with the L1 strip hit data for the transmission to the CIC.

In the first stage, a first-in-first-out (FIFO) memory reads out all pixel row L1 memories into the periphery. Concerning the depth of this raw pixel FIFO memory, the study in [35] examines FIFO memory sizing based on the data size and input/output rate. It is concluded that a depth of 8 is sufficient to fulfill a maximum L1 trigger rate of 1 MHz.

In the next step pixel and strip data is encoded. Up to 31 pixel clusters are encoded. The SSA has stored the strip cluster information in its own L1 strip memories (see Figure 4.6). The strip L1 data is deserialized from the transmission by the SSA and encoded in up to 24 strip clusters. The two cluster types are encoded in the following way:

- Pixel Cluster (14 bit): Column address of first pixel coordinate in cluster (7 bit), Cluster width (3 bit), Row address (4 bit)
- Strip Cluster (11 bit): Column address of first strip coordinate in cluster (7 bit), Cluster width (3 bit), HIP flag (1 bit)

For both cluster types the maximum cluster width is 8. Clusters which exceed the maximum size are encoded as two consecutive clusters. Encoded strip and pixel clusters, together with the respective L1 ID are packaged into a L1 data packet.

The L1 data packet is stored into an L1 FIFO memory in the periphery awaiting transmission to the CIC. The sizing of the L1 FIFO is given by the expected occupancy and amount of pixel-strip clusters during operation in the CMS Outer Tracker. Based on simulations for high PU events occurring for 14 TeV pp collisions, the chance of the L1 data size reaching a length of 500 bit (corresponds to a cluster multiplicity of 40) is 1 in 10×10^6 [28]. As such, an L1 FIFO width of 512 bit is sufficient for a lossless transmission in almost all cases.

4.5.3 Data Transmission

All output data lines make use of Scalable Low-Voltage Signalling (SLVS) differential links which transmit data at a single data rate of 320 Mbps. The SLVS link drivers are a custom design based on 65 nm CMOS technology intended for use in the PS module [36]. The radiation-hardness is based on the use of a thin-gate oxide transistors and a voltage supply of 1.2 V. The output lines of the SSA toward the MPA make use of the same SLVS drivers to transmit the strip data. As such, the SLVS drivers and necessary data serializers and de-serializers are implemented in the 320 MHz domain of the MPA chip periphery.

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Input Lines

The input bus of the MPA consists of 9 parallel SLVS lines, which are further split into 8 lines for the strip trigger data and one line for the L1 strip data packet. The strip centroids are transmitted as an 8 bit coordinate of the strip cluster selected by the SSA. Consequently, with a rate of 320 MHz, up to 8 strip centroids per BX can be transmitted. In the MPA periphery, an input line sampling clock can be adjusted to be synchronized with the phase of the transmitted strip data ('LatencyRx'). After the L1 and trigger strip data is received successfully, a 8-to-1 deserializer buffers and converts the 8 single data lines of 320 MHz into 8×8 bit strip cluster coordinates at 40 MHz.

The L1 strip data is transmitted by one SLVS line after the SSA receives an L1 trigger signal. This L1 strip data packet has a fixed length of 168 bit and contains the L1 ID and BX counters for consistency checking, the 120-bit unsparsified strip event data and the SSA HIP flag. The received L1 strip data packet is also buffered and deserialized in the MPA for further encoding into the complete L1 packet.

Output Lines

The six MPA output lines are split into five lines for stub data transmission and one line for the L1 data transmission to the CIC Concentrator ASIC.

The five stub lines transmit up to 5 stubs averaged over two BX. A complete stub packet of five stubs is therefore transmitted at a rate of 20 MHz. The 15-bit stub data word contains the following stub information:

- Row Address (4 bit): Indicates the row coordinate of the stub in the pixel array.
- Column Address (8 bit): Indicates strip coordinate of the stub. Alternatively, also pixel centroids can be sent in pixel-pixel read-out mode.
- Bending (3 bit): Estimation of the high-p_T particle curvature based on its bending value.

The L1 data output line transmits the sparsified raw hit data. The L1 data packet is divided into a fixed size header and a variable size payload. An illustration of its structure is shown in Figure 4.8. The header contains a unique start sequence, an error field, the L1 ID, the multiplicities of the strip and pixel clusters contained in the payload. The payload is a list of the encoded pixel and strip clusters which occurred during the L1 ID.

Figure 4.8: Header and payload structure of the L1 data packet [28].

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4.6 Monitoring Block

Multiple monitoring features were added to the MPA2 to provide real-time information on the operating conditions (e.g., temperature, power, radiation dose) of the chip. The read-out of these monitoring values is based on I2C read transactions of the respective registers. From a CMS Outer Tracker point-of-view, this chip-level monitoring data may be used to develop a tracker monitoring tool which can be used to optimize and guarantee the adequate performance of the whole detector .

4.6.1 Monitoring by Analog-to-Digital-Converter

A 12-bit Analog-to-Digital-Converter (ADC) based on the successive approximation principle is implemented in the periphery block of the chip. A schematic of the ADC monitoring block is shown in Figure 4.9. The ADC uses a reference voltage of 850 mV that is adjustable towards PVT variation by a 5-bit DAC, referred to as VREF DAC. The ADC provides a digital measurement of the all the internal bias points listed in 4.3, a temperature sensor and additional voltage monitoring resistors. The additional voltage measurements include the bandgap reference voltage and supply voltages. The duration for the conversion is specified at 14 clock cycles.

The ADC monitoring feature was newly added to the MPA2. As such, its characteristics in the MPA2 toward irradiation and temperature measurement is first investigated in Chapter 6 of this work. The ADC design was provided by [37] .

4.6.2 PVT Monitoring by Ring Oscillators

The MPA implements two types of ring oscillators (RO) for the monitoring of variations in the fabrication process of the chips, the temperature and also the accumulated radiation dose on the chip. ROs are circuits which generate an oscillating frequency. Two types of ROs are implemented: the inverter-cell type and the delay-cell type and variations of their oscillation frequency can be measured. The periphery block and each pixel row includes a RO of each type. The two types show a different sensitivity either to the temperature of the chip or to the TID.

This is based on the usage of faster, minimum size transistors for the inverter-type RO which show a higher degradation with radiation. For the delay-type RO transistors, a transistor cell with larger gate-length is used, making it slower in switching, more temperature sensitive but also more robust towards TID. This circumstance should allow the use of the ROs for the monitoring of the operating conditions of the PS module. The behavior of the ROs in respect to temperature and TID is studied in Chapter 6.

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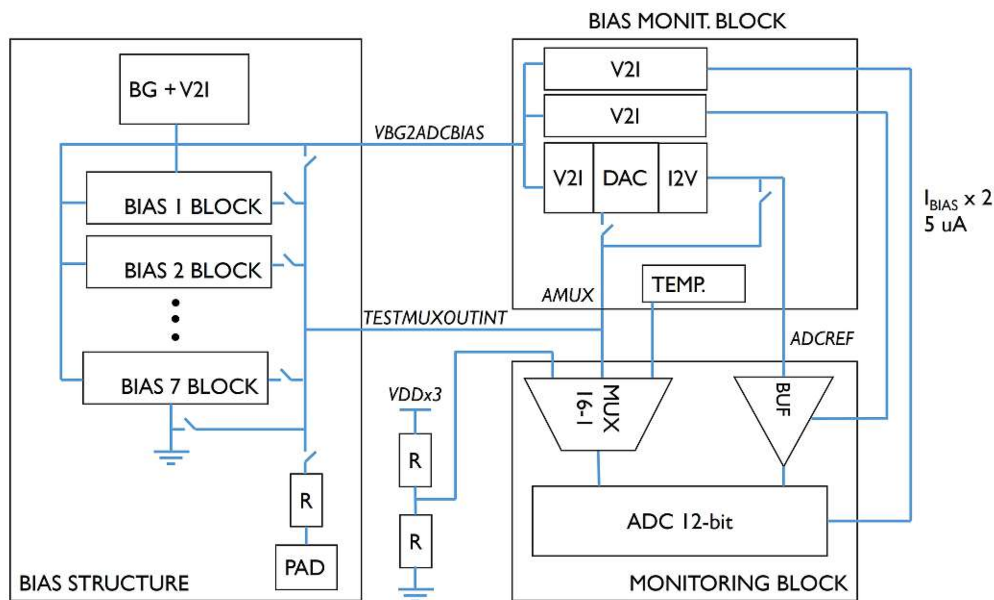

Figure 4.9: Structure of the ADC monitoring feature for bias points, temperature sensor and [28]. Also shown is the connection to the test pad (PAD) which allows the measurement of the bias values through an external instrument, e.g., a multimeter.

4.7 Design for Testability

Generally speaking, functional testing of the silicon chips, as is covered throughout this thesis, consists of invoking the functionality of the ASIC by applying combinations of different inputs and comparing the outputs to expected values. Due to the complexity of the MPA2, functional testing can become very expansive in terms of time consumed and developing cost. When considering the large amount of production units of the MPA2 ASIC that will be required for the CMS Outer Tracker, a full functional test of every chip is no longer considered feasible.

Three different Design for Testability (DFT) solutions were added to the MPA2, each performing structural testing of a specific digital logic region:

- Scanchain, for of the periphery block.
- Memory Built-in Self-Test (BIST), for the SRAM memories.
- Row BISTs, for the pixel row logic.

The scanchain is based on Automatic Test Pattern Generation (ATPG) binary vectors which are input through dedicated scanchain pads and shifted ("scanned") through the digital logic in the periphery of the block. Multiple sets of scan patterns are generated, to

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target known types of faults. The Row Logic BIST operates similarily to the scanchain, by shifting ATPG-generated test vectors through the digital logic. The Memory BISTs implement memory testing based on a March C- algorithm, where a specific set of write and read operations are performed in the memory with various patterns [38].

The DFT features are based on structural- rather than functional testing of the digital logic, by which physical defects in the gate-level logic can be detected. This drastically speeds up the testing time with respect to the covered faults. The detailed description of the DFT features and an analysis for the fault coverage is given in [39]. Only a summary of the functionality was given here.

The DFT blocks are implemented using radiation-hardening techniques and their functionality is first silicon proven for the MPA2 in Chapters 5 and 6.

4.8 ASIC Implementation

In this section, certain design aspects of the MPA2 ASIC driven by the need to satisfy the radiation hardness requirements and power consumption are described. Choices to reduce power consumption and improve radiation tolerance vary across various levels of the chip design, such as the logic design, selection of transistor technology and layout of the ASIC.

4.8.1 Technology Choice

The MPA and SSA, as well as other ASICs for the CMS OT, consist of large digital processing paths which consume the majority of the available power budget for the chip. The choice of 65 nm technology reduces the power dissipation per transistor. The technology node is also known to have reduced gate oxide thicknesses, improving the TID tolerance compared to larger feature sizes. This constitutes the main motivations to move to the smaller 65 nm technology node to benefit from down-scaling effects.

SOI[4] technology, although promising less power dissipation, is not feasible due to radiation damage induced in the oxides. Furthermore, design techniques and radiation behavior of 65 nm technology are well understood by the design community. The technology choice encourages reusability of "rad-hard" design blocks, such as the SRAM block, bandgap circuit or SLVS drivers in the MPA. This reduces prototyping and development costs while supporting collaboration in the design.

[4]SOI, Silicon On Insulator

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4.8.2 TID Tolerance

The radiation-induced degradation of 65 nm MOS transistor performance is dependant on the gate length (L) and threshold voltage. Borghello et. al. [16] show that shorter gate-length transistors experience a higher degradation in leakage currents and threshold voltage (V_T) at very high radiation doses. It is shown that these degradation effects are also strongly temperature dependent and reduced at lower temperatures.

As the design of the MPA2 is based on transistor cells provided by the manufacturer, the dimensions of the transistor in term of gate width to length (W/L) is not freely customizable. Instead, different sets of standard digital cells are provided as libraries to be used for the design. The standard cell libraries vary in their minimum device dimensions (W and L), the transistor threshold voltages (V_T) (high-V_T, low-V_T and normal-V_T). In [40] the standard cell libraries for the 65nm technology node are studied through the DRAD demonstrator chip. While transistors with larger dimensions show less degradation toward radiation, their power consumption is increased. As such, for the design of the MPA2, the choice of standard cell library fell on the '9-tracks' library[5] where the minimum size transistor has $W = 190\,\text{nm}$ and $L = 60\,\text{nm}$.

Also shown in [16] is the circumstance that not only the accumulated TID, but also the irradiation dose-rate affects the performance of 65 nm MOS transistors. In particular, for the same TID, devices exhibited a worse degradation after irradiation with low dose rates compared to higher dose rates. As it is not feasible to test devices with dose rates mirroring the actual radiation rates expected in the accelerator environments, a so-called safety factor for the TID of $\times 2$ is advised. In other words, for the TID characterization of the MPA2, a TID of up to 200 Mrad needs to be investigated considering the maximum expected dose of 100 Mrad in the CMS Outer Tracker.

4.8.3 SEU Hardening

SEU hardening is typically based on redundancy. A common approach selected for electronics in HEP environments is Triple Modular Redundancy (TMR), where each memory or flip-flop is triplicated and a voting cell decides on the output based on majority. While triplication has proven effective in the fault-tolerence against SEUs, the cost in increased area usage and power does not permit the full triplication of the entire digital logic of the MPA. To guarantee at least the fault-tolerant operation of the MPA, TMR was implemented exclusively for the its control paths, the related control clock signals, and the configuration registers.

Figure 4.10 shows TMR applied at the register transfer level (RTL). An exemplary FSM in the control path is fully triplicated. A combinatorial logic (abbreviated as "Comb Logic" in the figure) generates a state value which is stored into a register. As the

[5] N-track numbers for libraries indicate the number of draw lines used in the design tools for the standard cells. A higher track number incurs larger average channel W/L.

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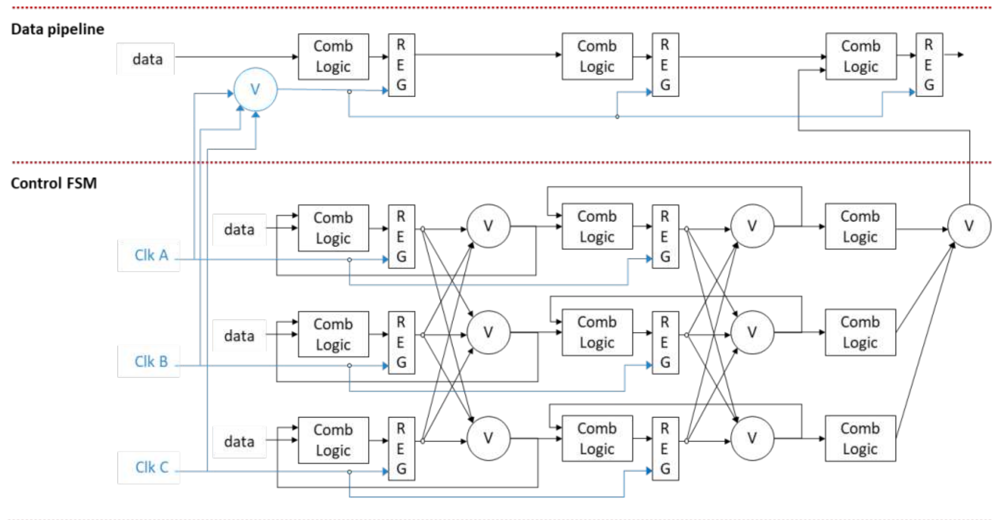

Figure 4.10: TMR for SEU fault-tolerance as implemented in the control paths for MPA and SSA [41].

combinatorial logic is susceptible to SET and the register may experience SEUs, the output of the registers is propagated to a voting cell. The voting cell itself is also triplicated in case of SEUs occurring here. A feedback loop is implemented to correct an error by periodically refreshing the voted state to the combinatorial logic. This can be repeated for however many stages the FSM may have. The clock signal is also fully triplicated within the control path.

TMR is also applied to the MPA configuration registers. However, as the amount of configuration registers is numerous, a periodic refresh to correct errors would be too power intensive. The stored values are therefore only refreshed if an error has been corrected. This is done by gating[6] the clock signal for the registers with an enable signal from the error detection logic, thereby providing an asynchronous refresh of the stored values in case of an error.

For TMR to be effective, the registers need to be physically spaced from each other by 15 µm to prevent SEUs occurring on multiple nodes of the triplicated block by a single incident particle [42].

Soft errors caused by SEUs in the data are not critical as they do not affect the system functionalities. However, the track reconstruction can be affected if the bit error rate is greater than a few parts per million. Apart from simulations, irradiation tests of devices can provide estimation of error rates. In the scope of this thesis, a heavy ion irradiation campaign was performed for the MPA2 and is described in Section 6.1.

[6]Clock gating, a power dissipation reduction technique where the clock signal can be disabled if the circuit is not in use.

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5 Experimental Setup and Functional Testing

A custom setup is used to test and characterize silicon prototypes of the CMS Outer Tracker ASICs (which includes SSA, MPA, CIC and CBC). It allows the functional testing of silicon prototypes on the wafer level, as well as the extensive testing on various stages, ranging from single chip characterization on carrier-boards for temperature, Total Ionizing Dose (TID), and Single Event Upset (SEU) testing. Before the results of characterization and related studies are presented in Chapter 6, this chapter aims to introduce the test bench setup and provide an outline of the testing procedures performed for the MPA2. A selection of results acquired through functional testing of the MPA2 at the wafer-level is also presented and preliminary estimations on the resulting yield are made.

5.1 Testbench

A block diagram of the custom testbench system is shown in Figure 5.1 and its laboratory setup is shown in Figure 5.2. The system is based on an host PC running software routines with use of an FPGA data acquisition board. An interface board is connected to a carrier board which hosts the wire-bonded MPA2. Test procedures are scripted and run on the UNIX-based host PC which communicates with the firmware of the FPGA board over an TCP/IP ethernet connection, while the interface board routes the MPA2 pad signals and regulates the power supply to the chip. An ethernet-enabled voltmeter allows the measurement of signals directly from the MPA2 test pad.

5.1.1 FC7 FPGA Board

The core module of the testbench is the FC7 FPGA board. The FC7 is a flexible, µTCA compatible Advanced Mezzanine Card (AMC) developed for data acquisition (DAQ) and control applications of electronics in HEP experiments [43]. It hosts a Xilinx Kintex-7 FPGA which supports the interfacing of up to two FPGA Mezzanine Cards (FMC) for the communication to further modules.

The FC7 is driven by the d19c firmware which forms the base for test setups across many CMS tracker electronics and is maintained by the CMS Tracker DAQ community [44].

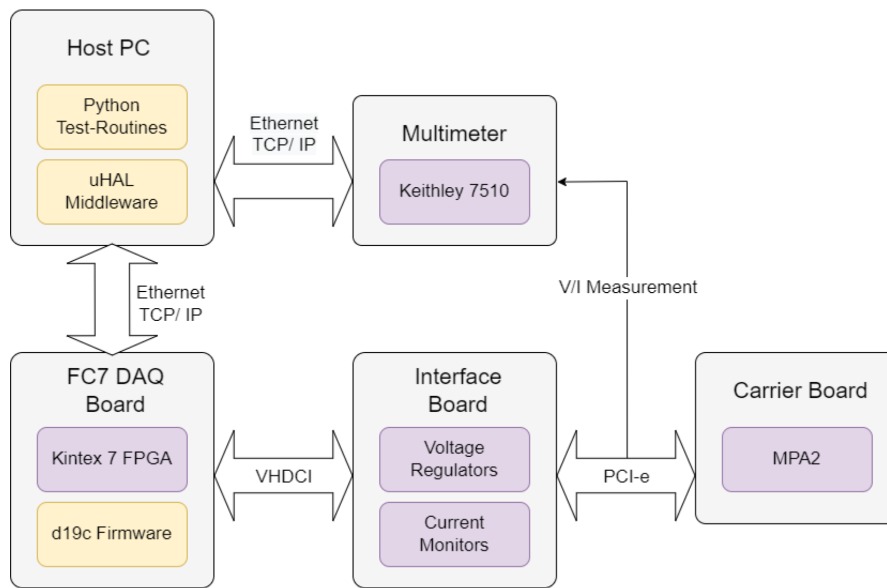

Figure 5.1: Block diagram of MPA-SSA test system and its components.

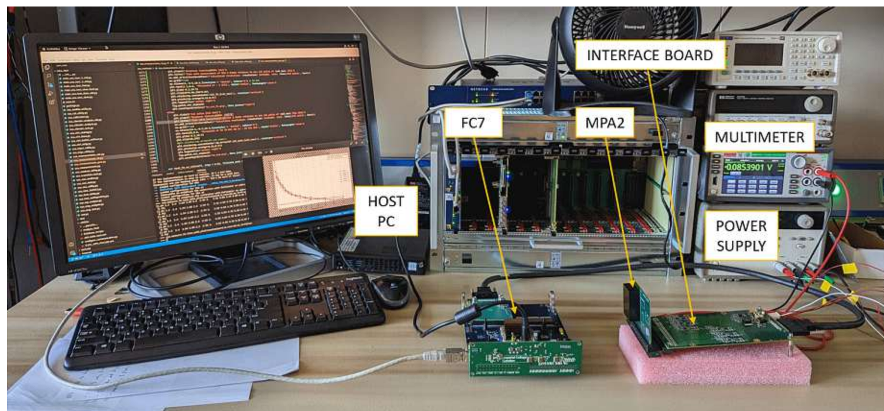

Figure 5.2: Image of the laboratory setup of the MPA-SSA testbench. The MPA2 is covered to protect the delicate wire-bonds to carrier board.

It is used for testing of a range of single CMS ASICs such as the CBC, RD53, SSA and MPA, but also for testing of multiple chips in parallel or sub-assemblies of the modules. In the case of the MPA, it provides direct hardware interfacing with the control, clock and data interfaces of the chip. The firmware includes a wide range of state machines which facilitate the control of the chip in various read-out modes, emulation of input data, read-out of trigger and L1 data among various other procedures. Figure 5.3 provides an overview of the d19c code structure and its main blocks.

The Fast Command Block provides the generation of fast commands for the chip, such as trigger or reset signals, while the Command Processor Block handles I2C transactions to

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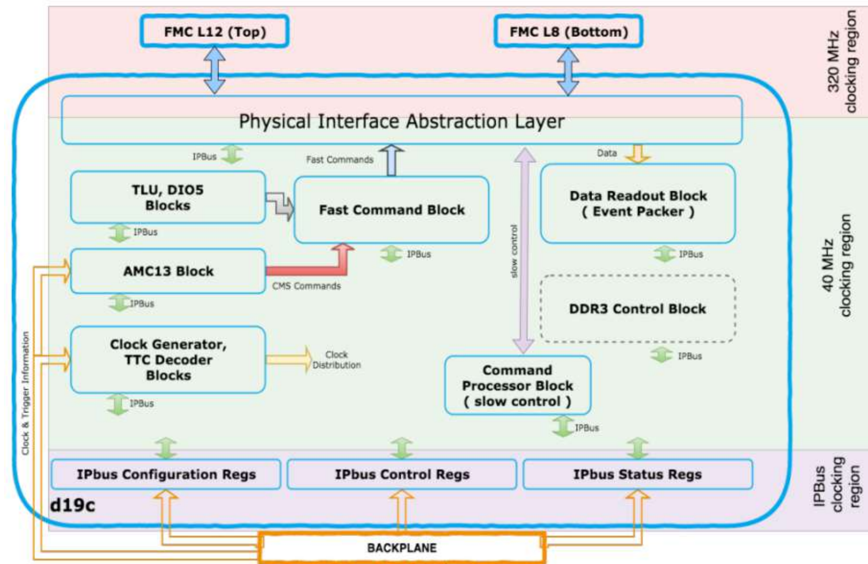

Figure 5.3: General structure of the d19c firmware hosted by Kintex-7 FPGA of the FC7 DAQ board. [44].

the configuration registers. The clock generator provides the different clocks, such as the Clk320c control clock for an MPA under test. The Readout Block handles the read-out of strip and L1 data, supports the associated header information and counter values (L1 and BX), and stores the read-out data in a FIFO memory block of the FC7.

A user interacts with the firmware (e.g., sending fast commands or I2C write transactions) through the IPBus layer. The IPBus provides the configuration and control of the d19c in form of register address spaces for the different blocks. A user may configure and control the d19c blocks by sending configuration commands to these registers based on TCP/IP transaction over an ethernet interface connected to the FC7 [45].

The above described blocks are mostly agnostic to the specific hardware that is being tested. The Physical Abstraction Layer handles lower level communication to the chip under test, and as such, it is here where the d19c handles the address schemes for the fast and I2C commands of the MPA. The read-out data deserialization is processed according to the output data formats and transfer rates of the MPA. As this part of the d19c operates at a 320 MHz rate, the sampling rate of the FC7 needs to be aligned to the phase of the MPA output. Automatic phase tuning methods based on a tuning FSM that uses a synchronisation pattern are provided for the user.

The electrical connection to the MPA chip pads are routed through an FMC socket of the FC7, which are further routed through an FMC-to-VHDCI adapter board to the interface board.

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5.1.2 Interface Board and Carrier Boards

The interface board is a custom design by Rutgers University. It serves I2C addressable linear voltage regulators for the power supply to the chip and allows measurement of these voltages through current monitors. The interface boards is connected to the FC7 by a Very-High-Density Cable Interconnect Cable (VHDCI) and routes all MPA2 signals to a PCI-Express connector. Its power supply requires a 4.5 V and 2.5 V DC voltage.

Figure 5.4: MPA2 mounted on carrier board with wire-bondings. The MPA2 pins are exposed to a PCI-E connector.

The MPA2 chip is mounted by wire-bonding on a carrier board shown in Figure 5.4. Additional variants of a mezzanine card can be plugged into the interface board via PCI-Express connector, allowing to adapt the orientation of the MPA chip for the specific need of the test setup. For the voltmeter measurement of the bias values, a wire is soldered on to the corresponding pin that leads to the test pad of the MPA.

5.1.3 Host PC and Python Test Software

The host PC runs a CentOS 7 operating system and is used to run the MPA2 testing software routines. Through the utilization of various interfaces, APIs[1] and tools described below, a comprehensive testing suite for the MPA and SSA was developed. Python is used as the scripting and programming language to compose various test and characterization routines as well as conduct analysis and visualization of the acquired measurement data. Python encourages a simple and comprehensible coding style with an object oriented focus. A wide range of freely usable APIs for hardware interfacing, data collection and analysis further favor this choice. The drawback of the python is that clock-cycle accurate

[1]Application Programming Interface

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control of configuration and data parsing operations is difficult to achieve due to the software processing and ethernet communication overhead. As the sychronisation of control and high-rate data injection and read-out to the MPA2 is handled by the FC7 anyway, the software overhead on the host PC can be disregarded.

In order to interface with the hardware of the test system, the µHAL API is available for the handling of IPBus commands to the d19c firmware in python [46]. It instantiates a TCP/IP ethernet socket enabling read and write operations to the address space of the d19c accessible through the IPBus protocol. The addresses of the d19c configuration registers are provided by CMS Tracker DAQ.

Voltage measurements are necessary for various calibration and measurement procedures performed for the chip. The Keithley Digital Multimeter 7510 was used in the test system as it allows the control and acquisition of voltage measurements by transmission of Standard Commands for Programmable Instruments (SCPI) over the multimeter ethernet interface. A National Instruments General Purpose Interface Bus (GPIB) is also availabe for the same SCPI commands and was used occasionally.

The rough structure and hierarchy of the testing code is illustrated in Figure 5.5 as a block diagram. Higher level testing methods (further described in Section 5.2) make use of common methods, such as basic chip configurations, data read-out, configuration of the pixel array, fast commands for trigger and calibration pulse injection or powering sequences. Underlying those, are classes which encode the respective control commands in either a fast command or an I2C read/write transaction. For the encoding and issuing of I2C transactions, the addresses of the MPA2 I2C configuration space, also called the I2C address table, are stored in the test software. The same is required in the address table of the d19c for IPBus transactions to the FC7. In fact, the I2C bus protocol transactions are also handled through the FC7.

Listing 5.1 shows a simplified code snippet showing how the sending of an L1 trigger signal is initiated in the test software.

```
1 def send_trigger(la_en = 1):
2     # encode L1 trigger bit with fast command bit mask
3     encode_l1a = self.fc7AddrTable.getItem("fc7_daq_ctrl.fast_command_block
      .control.fast_trigger").shiftDataToMask(l1a_en)
4     # IPBus write to the Fast Command Block of d19c
5     FC7.write("fc7_daq_ctrl.fast_command_block", encode_l1a)
```

Listing 5.1: Python code to initiate an L1 trigger signal.

For the trigger or test pulse commands, a variety of configurations can be set in the associated FSM of the d19c. Examples include the amount of triggers/pulses, frequency of triggers or waiting periods between triggers to be sent.

Another code example is given in Listing 5.2, showing how an analog calibration pulse is injected for a specific pixel FE. I2C command encoding is used to enable and configure

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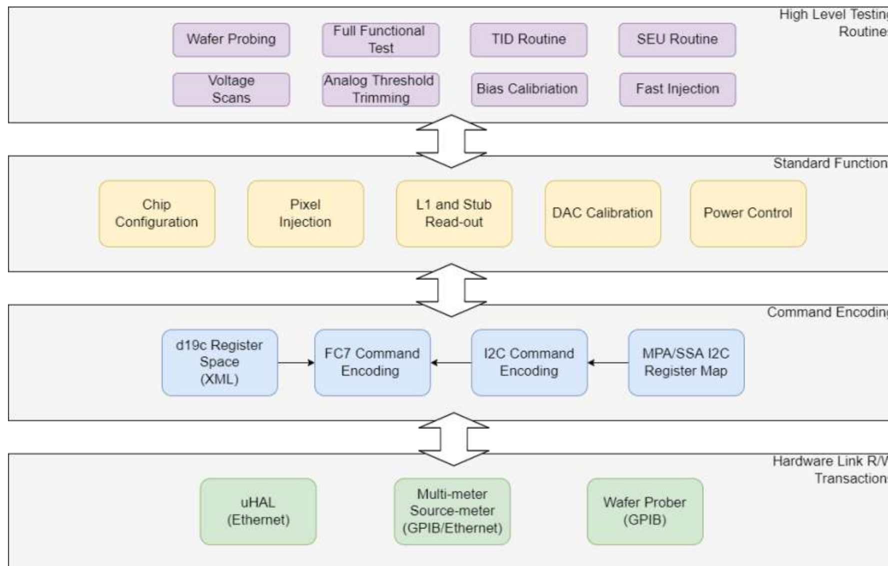

Figure 5.5: General code structure of the python-based test software.

the pixel binary-readout mode, while the test pulse is sent with the use of the FC7 fast command block.

```
def test_pp_analog(row, pixel):
    # enable pixel-pixel read-out mode
    mpa.ctrl_base.activate_pp()

    # enable edge-sensitive synchronous BR for specific row
    I2C.row_write('PixelControl', row, 0x14)
    # enable calibration pulse for specific pixel
    I2C.pixel_write('PixelEnables', row, pixel, 0x57)

    # send test pulse fast command from FC7 for 8 BX duration
    FC7.send_test(8)

    # return the parsed stub data after reading them from the MPA
    return mpa.rdo.read_stubs(fast = 1)
```

Listing 5.2: Python code of analog CalPulse injection in a specific pixel.

5.2 Functional Testing Routine

The basic routine verifies most MPA2 functionalities and collects initial characterization data of a chip. It is intended for the relatively quick assessment of the chip functionality during its wafer-level testing (∼3 min per chip). The core group of higher level testing methods that are considered to classify an MPA2 chip as functional are described in the following.

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5.2.1 Power and Chip Initialization

The power on of the MPA is initiated by I2C commands to the interface board which regulates the MPA supply voltages. A power enable signal is sent to the interface board, which enables the voltage regulators for the three power domains of the chip. Each voltage regulator can be set individually with the voltage level of the respective power domain.

When the supply voltages are provided to the MPA2, the chip configures itself into a start-up state with default values for its configuration. In the initialization procedure for the test bench, the MPA2 is set into to the standard read-out mode (pixel-strip mode) and the phase alignment procedure is started. The phase and word alignment procedures synchronize the FC7 sampling rates to the data output rate of the MPA with the help of the available phase alignment FSMs of the d19c firmware. If the phase alignment is not possible, the chip is possibly erratic in its output line phase or there is no output data present.

The consumed power is measured in form of the current consumed by each of the power domains. If the monitored current is outside the expected range, it indicates that the chip under test is faulty and that electrical shorts are present.

Transistor leakage current is an important value to assess as it can vary significantly against temperature and radiation dose of the chip. The leakage current is measured by putting the chip in a reset stage, thereby disabling the complete digital logic. As the analog pixel FEs cannot be disabled this way, the leakage current is only measured for the digital domain (DVDD).

5.2.2 Measurement of Reference Voltages

An I2C command is sent to the bias structure of the MPA to multiplex one of several bias values to the test pad. The respective bias structure and monitoring circuit is shown in Section 4.6. Through the external voltmeter, the bandgap voltage and digital ground are measured and recorded. The digital ground is the potential difference between the digital LOW value of the chip and the external ground of the test system. It represents a voltage drop across the wire or probing contact to the chip and can indicate the quality of the contact. The bandgap reference voltage is the most stable reference voltage on the MPA2 from which other reference values are derived from. As such, it is a characteristic value, which through comparison can inform on variations in the wafer fabrication process of the chip.

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5.2.3 Bias Calibration

The calibration of the bias blocks in the MPA is an essential step to ensure the uniform distribution of bias values across a chip. At the chip startup, the bias DACs are set with default values. For the bias calibration, the test software sweeps through all available bias DAC input codes and measures their output through the external voltmeter over the test pad. The corresponding DAC input code which is closest to the nominal values listed in 4.3 are then set in the DAC configuration registers.

This is done for all DACs A-E of bias blocks 1-7 shown in Figure 4.5. In addition, the 5-bit VREF DAC for the reference voltage control of the monitoring ADC is set to its nominal value by the same procedure.

5.2.4 Analog Front End Characterization

With the utilization of the asynchronous read-out mode and the pixel FE internal calibration circuit described in 4.3, the pixel analog FE characteristics, such as the gain and channel noise can be measured even without an attached sensor. The S-curve measurement is done to describe the response behavior of a pixel analog FE, as described in Section 2.3.1. It is obtained by comparing the number of registered hits against multiple test charges with increasing amplitude.

S-Curve extraction

For the S-curve routine in the MPA2, the CalDAC controls the amplitude of test charges injected into the analog FE circuit. On the other hand, the ThDAC sets the threshold of the discriminator that needs to be surpassed by the injected charge to be registered as hit. 1000 test charges are injected for each of the 256 available CalDAC amplitudes against a globally set discriminator threshold. The nominal threshold set is around $38\,\mathrm{LSB}_{\mathrm{ThDAC}}$ (0.5 fC). The amount of discriminator hit responses is then counted in the 15-bit ripple counter and acquired via I2C read-out to obtain the pixel S-curve.

A random distribution is assumed for the noise in the S-curve. As such, the S-curve can be seen as a cumulative distribution function (CDF) of a randomly distributed charge value, where the expected value μ is the threshold and its standard deviation σ is the the channel noise. A CDF of shape

$$\frac{1}{2} + \frac{1}{2}\,\mathrm{erf}\left(\frac{\mu - x}{\sigma\sqrt{2}}\right) \tag{5.1}$$

is fitted against the pixel S-curves by means of least squares fitting, delivering the parameters μ and σ of the fitted function. In this way, the noise and threshold of an analog pixel FE are extracted from an S-curve in terms of $\mathrm{LSB}_{\mathrm{CalDAC}}$. If done across all pixel FEs, the average noise of the chip and the distribution of the thresholds can be obtained for the set nominal threshold. Both values are expressed as charge in terms of $\mathrm{LSB}_{\mathrm{CalDAC}}$.

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Threshold Trimming Procedure

The variation of the individual thresholds is defined through its standard deviation, referred to as threshold spread, and the expected value, referred to as threshold mean. The threshold spread is minimized through the threshold trimming (or also equalization) procedure to guarantee the uniform response behavior of pixel FEs. The trimming procedures is based on balancing the per-pixel 5-bit Trimming DAC (TrimDAC) to tune the threshold voltage provided to the discriminator against the injected CalDAC charges.

Before the trimming procedure is started, the LSB gain of the ThDAC and CalDAC are quantified through the bias calibration. Typical gain values are $1.4\,\mathrm{mV/LSB_{ThDAC}}$ for the ThDAC and $35 \times 10^{-3}\,\mathrm{fC/LSB_{CalDAC}}$ for the CalDAC. For both DACs, three parameters are defined to constrain the optimization, namely `high`, `nominal` and `low`. These parameters are based on previous trimming runs known to yield a good trimming performance. Figure 5.6 shows an example of the pixel thresholds obtained by S-curves over the different stages of the trimming procedure. As the software procedure involves many steps, only an outline is given below:

1. A first S-Curve set with ThDAC `nominal` is run (for all pixels) to obtain the pre-trim threshold spread and mean for the pixel array. All S-Curves in the procedure use an injected test charge range of 1 to $250\,\mathrm{LSB_{CalDAC}}$.

2. Two S-Curves sets at ThDAC `high` with the TrimDAC set once to its minimum of 0 and maximum of $31\,\mathrm{LSB_{TrimDAC}}$ are run. A high ThDAC setting will minimize the effect of noise on the min. and max. trim thresholds received.

3. Based on the minimum trim and maximum trim thresholds acquired in the previous step, the TrimDAC LSB resolution in terms of $\mathrm{LSB_{CalDAC}/LSB_{TrimDAC}}$ for each pixel is calculated.

4. The half-point between the means of the minimum trim and maximum trim thresholds is calculated. With this, a target trimming threshold value in terms $\mathrm{LSB_{CalDAC}}$ is now defined for each pixel.

5. With the TrimDAC resolution and the target threshold, each pixel is configured with the TrimDAC value that should shift its threshold to the target threshold. Some pixels may have a trimming range which is not able to cover the target trimming threshold, they are therefore considered 'not-trimmable.'

6. A trimmed S-Curve set with ThDAC `nominal` is run to check the trimming performance.

7. Based on thresholds received from the previous step, a fine-tuning of the TrimDAC value around `nominal` CalDAC is performed.

8. A nominal S-curve set with ThDAC set to `nominal` is run.

9. A final S-curve set with ThDAC `low` is run to acquire post-trim channel noise, threshold spread and mean, averaged over the pixel array.

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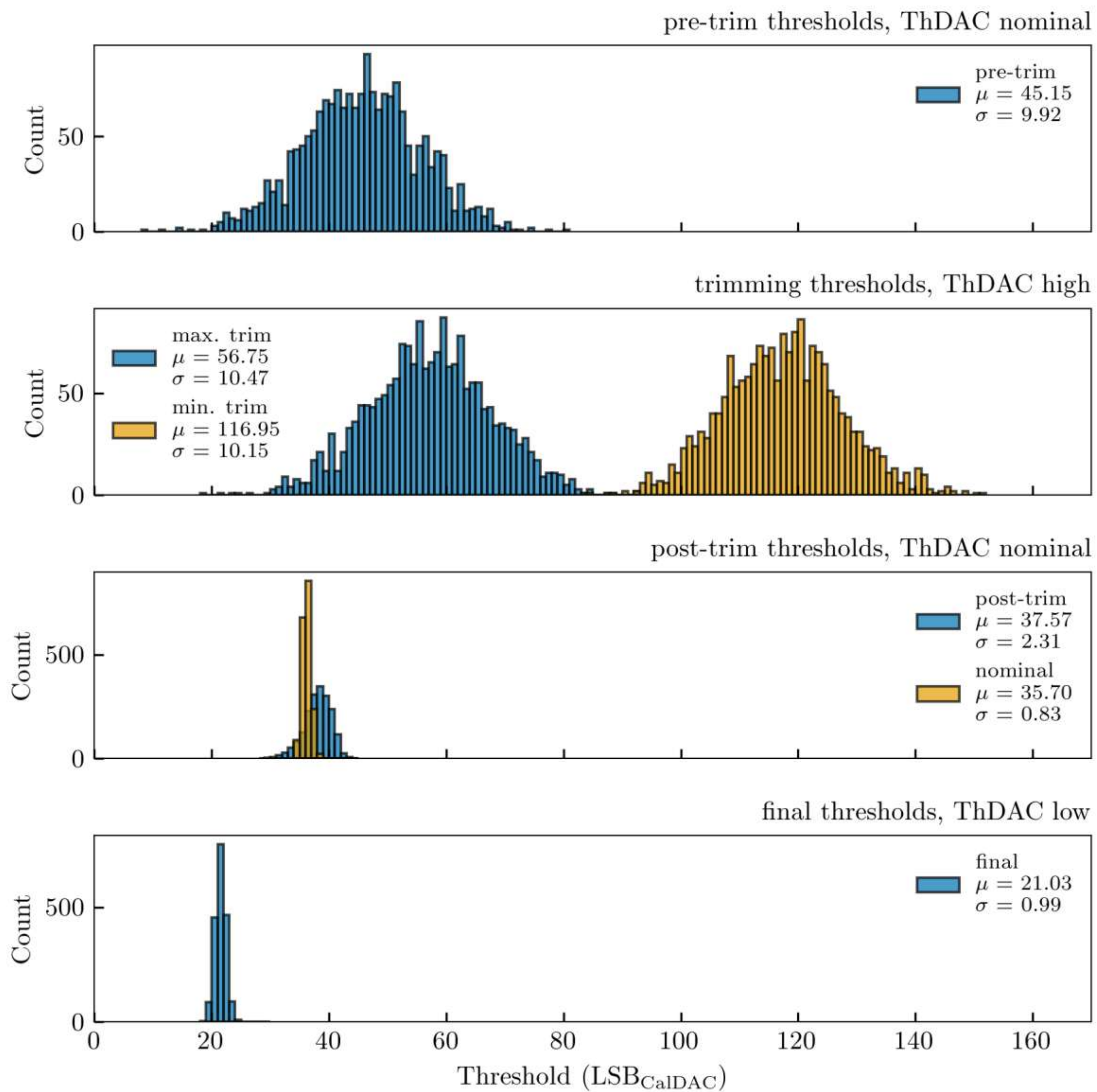

Figure 5.6: Thresholds obtained by per-pixel S-curve at each stage of the threshold trimming procedure.

With the `nominal` and final `low` thresholds and their respective S-curve responses acquired in the last two steps, two points with the input charge and output threshold voltage have been measured and are averaged. By calculating the slope between the two points, the gain of the FE pre-amplifier is evaluated across the chip in terms of mV/fC.

To be noted is that the threshold trimming procedure presented here is just one approach in order to demonstrate the ability to trim threshold variations towards a calibration pulse in the MPA2. Trimming procedures for an MPA2 combined with the PS-p sensor will

likely be adjusted and optimized for pulse amplitudes and noise behavior of the sensor.

Timewalk

As the discriminator output of the analog FE cannot be directly measured electrically, the timewalk is determined in an indirect way. The timewalk of the analog FE circuit is theoretically described in Section 2.3.1. For its measurement in the MPA2, analog calibration pulses are sent to a pixel FE in pixel-pixel mode and the BX ID of the output stub packet is read. Higher amplitude pulses should arrive sooner at the discriminator input than smaller pulses. However, the resolution of the BX ID is only 25 ns and therefore too large to distinguish a delay between calibration pulses of different amplitudes.

The timewalk measurement is accomplished with use of a 5-bit line delay DAC implemented in the bias structure of the MPA2 (DAC-F in Figure 4.5). It can provide an additional delay to the calibration pulse in the range of 0 to 25 ns. By sweeping the delay DAC codes for a given calibration pulse and observing at which delay input the output stub switches from one BX ID to the next, the delay resolution of the delay DAC can be determined. The BX ID switch occurs at different delay inputs proportional to the input calibration pulse amplitude. By calculating the delta between the BX shift between two pulses in terms of delay DAC inputs, a timewalk measurement is obtained.

The timewalk characterization can take a long time depending on the number of charge amplitudes for which it is to be measured. In general, the specification requires the timewalk to be below 15 ns for all pulses above the nominal threshold (0.5 fC). As the analog FE block in the MPA1 is identical to the MPA2, and the timewalk requirement has been validated for the MPA1 in the past, the measurement is not considered as part of the basic functional testing routine of the MPA2. In the scope of this thesis, the timewalk measurement was performed as part of the temperature characterization of the MPA2 reported in Section 6.3.

5.2.5 Strip Input Integrity

The strip input lines (9 SLVS input lines in Figure 4.1) of the MPA2 are tested for their signal integrity and functionality to pass input data to the MPA2 output lines. For this test, the strip-strip read-out mode of the chip is activated, where the strip centroids transmitted to the strip lines are used as stub seeds through the MPA stub data path. The strip centroids are generated by a d19c FSM that emulates trigger data to the MPA. During the test procedure, a strip centroid is sent to each input line of the MPA. The input line sampling rate phase of the MPA is sweeped to verify if it can be matched to the phase of the input data stream. After the matching phase delay is found, the strip centroids are processed in strip-strip mode and the resulting output stubs are checked against the input strip centroids. This procedure is repeated for different centroid coordinates covering the range of possible strip coordinates.

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5.2.6 Pixel Injection and Hit Processing

Two types of test routines were implemented to test the functionality of the available binary read-out modes and data injection methods in the pixel FEs (refer to Section 4.3). For both of the test methods described below, the chip is configured in pixel-pixel mode and every available pixel FE is tested individually.

The 'analog pixel test' injects analog test charges into a pixel FE using the calibration circuit and the edge-sensitive binary read-out mode. For this test, the calibration pulse in the pixel analog FE is set to $200\,\mathrm{LSB}_{\mathrm{CalDAC}}$ and the discriminator threshold to $200\,\mathrm{LSB}_{\mathrm{ThDAC}}$. After test charges are sent for a certain amount of BX cycles, the generated stub events are loaded into the FC7 and parsed by the test routine. The test routine checks if the centroid coordinate in the stubs corresponds to the coordinate of the injected pixel FE.

A 'digital pixel test' validates the digital debug mode of the BR in the pixel FEs in level-sensitive mode and the L1 data path. For that purpose, it injects a digital pattern with digital CalPulse functionality. The L1Offset, the duration the raw hit information is stored in the L1 row memories, is set to 255 BX cycles and a single test pulse and L1 trigger are generated. The received L1 data packet is parsed by the testing routine and checked for the correctly encoded pixel centroid coordinate.

5.2.7 Fast Injection Routine

The previously described pixel injection routines only verify the hit processing of the chip in pixel-pixel mode for each individual pixel FE. Thereby, the actual stub finding and coincidence logic needed for the p_T discrimination is still left out. Furthermore, the individual test pulse injection of a single pixel and read-out of the resulting stub or L1 data cannot not be done at high rate due to overhead caused by the I2C transactions.

As such, the fast injection routine leverages a d19c FSM to configure the periodic transmission of test pulses and L1 triggers at a high rate while injecting strip data. Concerning the injected data, the test routine generates 8 random strip and pixel centroids every two BX. The d19c is configured to emulate the transmission of the 8 strip centroids in form of trigger data as well as L1 strip data. Meanwhile, the 8 pixel centroids in the MPA are generated by digital test pulses. With the MPA stub finding configured in normal operation mode (pixel-strip) and L1 triggers generated at a 1 MHz rate, injected events are read-out as stub data and as full event L1 data frames.

The injection and read-out timeframe of the fast injection routine can be configured to be as long as required. As the generated data rates are very high, the d19c implements specific FIFOs and FSMs which allow real-time checking of the read-out L1 and stub data against the injected centroids. The d19c firmware can be configured to store only events which do not match the input data and stop the procedure if the the related memory for erroneous events overflows.

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5.2.8 Measurement of Monitoring Values

As part of the PVT monitoring functionality, the oscillation of ring oscillators can be initiated and recorded. For the measurements included in this thesis, ring oscillators were pulsed for a duration of 1016 BX cycles. A counter accumulates the oscillation count per RO and can be read-out via I2C. To produce the oscillation count as frequency, one needs to apply the simple conversion

$$RO_{Hz} = \frac{RO_{Count}}{1016 * 25\,\text{ns}}. \tag{5.2}$$

The read-out of the ADC monitor occurs via I2C as well. The ADC block is first enabled and the conversion is started through an ADC control register. A selection register can be configured for the multiplexers of the ADC monitoring block to select the desired parameter for ADC read-out.

5.2.9 Design for Testability (DFT)

The DFT features of the MPA, briefly described in Section 4.6.2, are also performed as part of its functional testing routine.

For the Memory and Row Logic BISTs, the execution is straight-forward from the perspective of the testing software. Both tests are configured and their execution in the digital logic is initiated by I2C transactions. The Memory and Row BIST are performed in sequence, as the Memory BIST sets the SRAM outputs to specific values which are then used for the Row BIST. The Memory BIST merely needs to be executed for each row through I2C operation to the dedicated registers. For the Row BIST, the relevant BIST controller block is configured consecutively over I2C with the various ATPG test vectors, the scan operation is performed and the response vector is immediately compared. The comparison result is stored in I2C registers and are read by the testing software.

The scanchain for the periphery block requires an external FSM implemented in the d19c firmware. The d19c scanchain controller sets the MPA2 into a dedicated test mode where its general functionality is disabled. A test vector, provided to the d19c by IPBus commands by the testing software, is shifted through the periphery logic through the dedicated scanchain pads of the MPA2. The response vector is simultaneously captured through another dedicated output pad and directly compared against expected outputs by the FSM. The result is again retrievable to the testing software through an IPBus read transaction to the respective d19c register.

Table 5.1 lists optimal testing durations based on simulations reported by [39] against the time required to perform the tests with the test system (which includes significant additional overhead due to the test system).

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DFT Feature	f(MHz)	Test Vector Size	Simulation	Test System
Memory BIST	40	-	7 ms	0.22 s
Row Logic BIST	40	300 × 16 bit	40 ms	0.9 s
Scanchain	20	695 × 23 kbit	760 ms	102 s

Table 5.1: DFT operating frequency and execution time on the test system and during design simulation [39].

5.3 Functional Testing at Wafer Level

The MPA2 design was submitted for production in March 2021. The first MPA2 wafers were received at CERN in Summer 2021 subsequently. Within the scope of this thesis, the functional testing routine discussed in Section 5.2 was applied for the first electrical characterization of the MPA2 at the wafer level. The acquired probing data was analyzed and presented to CMS Outer Tracker electronics working groups to inform on the progress of the development and commissioning of the chip. Based on the initially probed wafers, MPA2 chips which were assessed as functional where selected for dicing and mounting on the carrier boards. In addition, the collected data provides statistics on how certain parameters may be chosen to asses a chip as "good" and how those parameter cut-offs may affect the yield in view of the large-scale production testing of the chip. The wafer probing setup and a selection of the acquired testing data is presented in this section.

The MP2 is processed on 300 mm wafers, each with 187 MPA2 dies. At the time of writing, a total of 3552 MPA2 chips over 19 wafers were were tested using the wafer probing station. The lot-specific names and wafers probed are listed in Table 5.2. The amount of testing data provides a large amount of statistics for the electrical characterization of the MPA2 and allows to quantify chip-to-chip and process variations. This testing data is also made accessible to CMS collaborations through a Phase-2 Tracker component database, in an effort to inform on MPA2 characteristic values in preparation for the assembly and further testing of the assembled PS modules.

Lot name & size	Probed Wafers	No. of chips
N6Y215 (17)	1 to 18	3178
NAFR48 (25)	1	187
NAFR49 (25)	1	187

Table 5.2: Lot names and wafers/chips probed.

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5.3.1 Wafer Probing Setup

The same test setup described in Section 5.1 is also used for the wafer probing of the MPA2. However, instead of a carrier board, the MPA2 chip to be probed must be contacted through a custom designed probe card. The probe card is installed into the Cascade Microtech CM300xi, a wafer probing station for wafers of up to 300 mm diameter pictured in Figure 5.7.

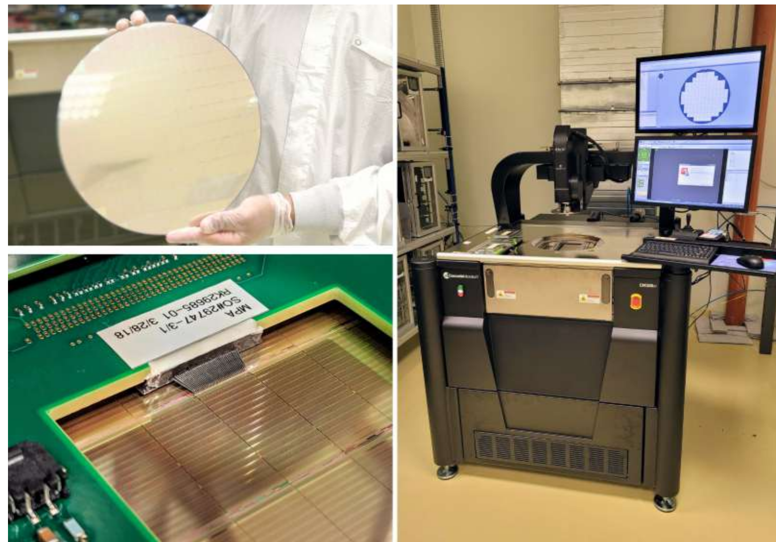

Figure 5.7: MPA2 dies processed on a 300 mm wafer (left top). Custom probe card tips in contact with the pads of an MPA2 die (left bottom). Cascade Microtech CM300xi wafer probing station (right).

A MPA2 wafer is loaded into the machine by placing it on the wafer chuck. Through an alignment procedure, the position of the scope and tilt of the probe tips can all be precisely adjusted to ensure a good contact between the probing tips of the probe card and the pads of a die. After the alignment has been completed and the probe station has been programmed with the MPA2 wafer map, including the locations, exact size and pitch of the dies processed on the wafer, the probe station can be remotely controlled through a GPIB interface connected to the host PC. The remote interface involves the automatic stepping between dies as well as the compensation of any spatial drift of the nominal probe contact position. A wafer testing routine was developed, which leverages the remote interface of the probe station to fully automate the probing of a wafer, initiates the functional testing routine and records the per-die measured data.

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5.3.2 Pass and Fail Rates

In this section the acquired data from the probing of the MPA2 wafers is reported and a few considerations on the estimation of the total yield, i.e., ratio of chips which are considered "good", are presented.

The calculation of yield for the probed wafers is based on pass or fail criteria imposed on certain chip results acquired by the functional test routine. These criteria were defined preliminarily and may be adjusted for the still outstanding large-scale production testing of the MPA2. The statistical results for each criteria and for the different lots probed by August 2022 are listed in Table 5.3 and sorted into categories. Based on these criteria, the total yield is above 93 %.

Test Name	**Criteria**	**Pass rate (%)**		
		N6Y215 ($n_{chips} = 3178$)	NAFR48 ($n_{chips} = 187$)	NAFR49 ($n_{chips} = 187$)
Data Alignment				
Initialization	pass/fail	99.53*	100	98.93
Phase Alignment	pass/fail	99.28	100	98.93
Digital Hit Processing				
Digital Pix.	pass/fail	96.19	98.40	97.33
Strip Input	pass/fail	99.09	100	98.93
Analog Pix.	$<$ 5 errors	96.44	97.89	95.57
Analog				
Threshold Spread	$<$ 2 LSB	95.00	98.93	94.65
Noise	$<$ 2 LSB	97.92	98.93	95.72
DFT				
Mem. BIST	pass/fail	98.55	98.93	98.93
Row BIST	pass/fail	97.01	98.40	97.86
Scanchain	pass/fail	99.37**	98.93	98.93
Total Yield		93.11	95.72	94.65

Table 5.3: Success rate of tests/criteria used for the yield calculation of the probed MPA2 wafers. *init test was recorded for all Wafers of Lot N6Y215 except N6Y215_6 (2991 chips). **Scanchain testing of Lot N6Y215 was done on Wafers 7 to 18 (1870 chips).

Figure 5.8 shows how the selection of the cut-off value for analog FE threshold spread or noise affects the resulting yield rate. The data taken into account excludes Wafer 1 to 5 from Lot N6Y215 as the threshold trimming procedure used for these wafers was set with different parameters, therefore making the threshold spread and noise values not directly comparable.

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The selected cut-off values of 2 $\mathrm{LSB_{CalDAC}}$ for the analog FE threshold spread and noise is on the condition shown in Equation 2.2. With the nominal threshold of $\sim$3000 e^- (0.5 fC) for the MPA, one arrives to 430 e^- or 2 $\mathrm{LSB_{CalDAC}}$ for the maximum threshold spread and noise. Considering the change in the yield against the measured values shown in Figure 5.8, the cut-offs could be lowered. As the connected PS-p sensor will add additional noise levels and as the nominal threshold is still low enough for efficient MIP detection, the additional margin was decided to be kept.

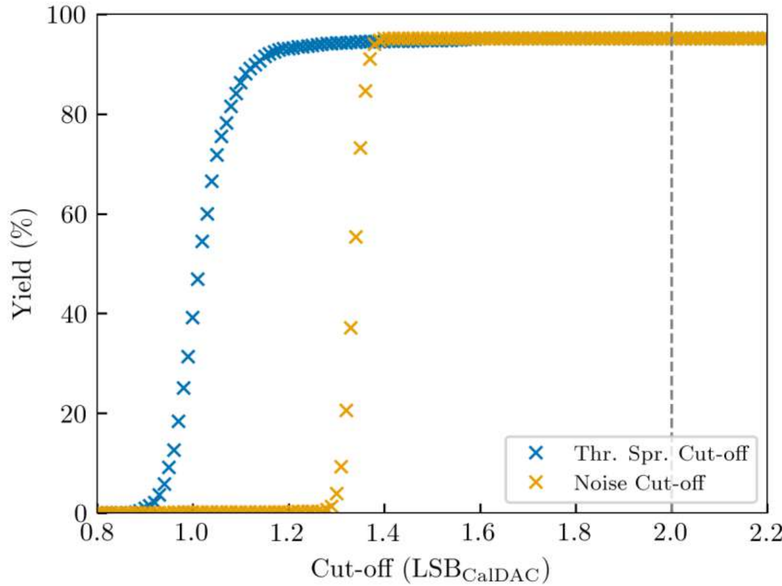

Figure 5.8: Resulting yield in respect to variation of the threshold spread or noise criteria (n_{chips} = 2244).

Desing for Testability (DFT)

The three tests, Row BIST, Memory BIST and scanchain make up the DFT features of the MPA2. Their pass or fail rates are individually listed in Table 5.3. The Pixel Row and Memory BIST was performed on all 3550 tested chips, but the scanchain test was only performed on 2244 of those. For this subset of the probed chips, Table 5.4 lists the digital failure rate compared to the rate of chips which fail one of the DFT features. The digital failure rate is based on failure of one or more criteria with exception of the Analog tests listed in 5.3. Of 103 chips failing any digital test, 63.89 % of them also fail for one of the DFT tests.

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Fail type	**Rate** ($n = 2244$)
Dig. fail rate	4.59 % ($n = 103$)
DFT fail rate	3.07 % ($n = 69$)

Table 5.4: Failure rate of digital tests compared to DFT failure rate. DFT failures are chips which fail one or more of the Row BIST, Memory BIST or Scanchain test.

5.3.3 Variability

The variability of probing data can yield information on the lithographic process quality between lot-to-lot or wafer-to-wafer. This can further be of interest to operators of the CMS Outer Tracker and PS Modules who may wish to understand variation in the MPA2 chip performances and operating conditions stemming from process variation.

To note is that variation between wafers within a lot was found to be minimal. As the variation between measured values are expected to be higher between lots, the measurements capable of indicating process variations are listed in Table 5.5 for the three lots. The measurement mean and standard deviations are computed across all chips of a wafer lot. Lots NAFR48 and NARF49 have only a small amount of data points compared to N6Y215 but should still show any significant deviations. The results reveal that process variations remain low even between the wafer lots. In the following, a few distributions of key measurements are provided to visualize the variability between the wafer lots.

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Measurement	**Value** (Mean (SD))		
	N6Y215 ($n_{chips} = 3178$)	NAFR48 ($n_{chips} = 187$)	NAFR49 ($n_{chips} = 187$)
Current Consumption			
Analog (mA)	59.22 (1.25)*	60.36 (0.95)	59.58 (0.90)
Digital (mA)	77.50 (2.56)	78.58 (1.09)	77.82 (1.04)
IO (mA)	8.62 (0.13)	8.76 (0.09)	8.55 (0.08)
Leakage (mA)	11.19 (0.23)	11.49 (0.23)	11.34 (0.23)
Analog FE			
Threshold Spread (LSB)	1.14 (0.2)	1.02 (0.07)	1.06 (0.08)
Noise (LSB)	1.34 (0.06)	1.32 (0.02)	1.35 (0.08)
Gain (mV/fC)	81.30 (2.35)	81.40 (1.69)	80.03 (2.13)
PVT			
RO Del. (MHz)	21.22 (0.2)	20.89 (0.13)	20.76 (0.16)
RO Inv. (MHz)	228.79 (8.27)	232.45 (6.66)	227.75 (5.99)
Reference Values			
Bandgap (mV)	283.86 (2.56)	283.86 (2.56)	283.72 (2.26)
ADC VREF DAC (LSB)	7.9 (2.2)	7.33(1.77)	7.24(2.02)

Table 5.5: A selection of measured values after wafer probing, averaged over all chips of one lot. *Values are slightly skewed, due to different threshold trimming parameters chosen for five wafers.

Bandgap

Measurements of the bandgap voltage distribution measured per chip are shown in Figure 5.9 per lot. The bandgap voltage variation between lots is minimal, which indicates a good control in the fabrication process of the wafers.

ADC Reference DAC

The necessary LSB value for the VREF DAC to establish the ADC reference voltage of 850 mV is shown in Figure 5.10 over all the chips for each lot. The distribution is similar between lots, owing to the fact that the ADC reference voltage is derived from the bandgap voltage.

Ring Oscillators

Distributions of the measured RO oscilliation counts are shown in Figure 5.11 and 5.12 for delay and inverter type respectively. Variability for the delay-type RO between wafers and lots is small, whereas it is higher for inverter-type RO. Lot N6Y215 seems to incur slightly higher standard deviations for the measured RO oscillations for both cell types due to the larger sample size. Figure 5.13 and 5.14 shows location-dependant variability of the RO oscillation of one wafer per lot as example. Again, a higher variability for inverter-type RO is visible.

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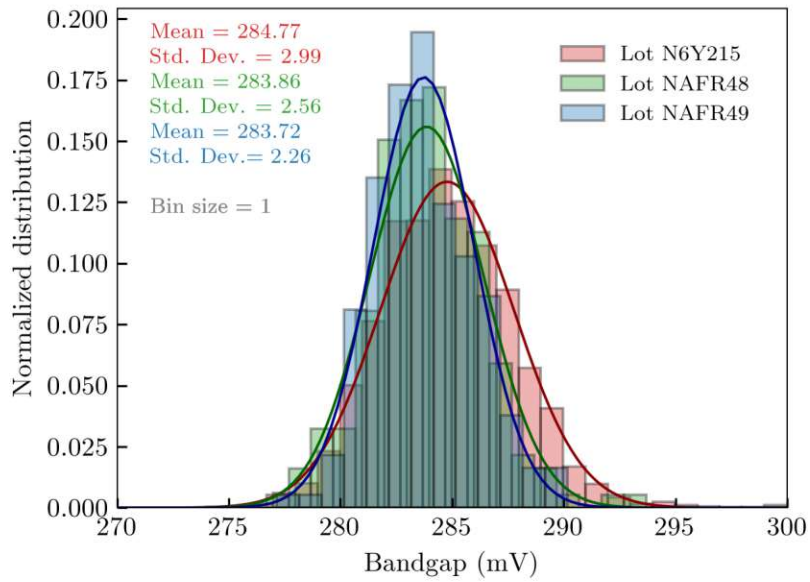

Figure 5.9: Distribution of per-chip bandgap voltage across all wafers of each lot.

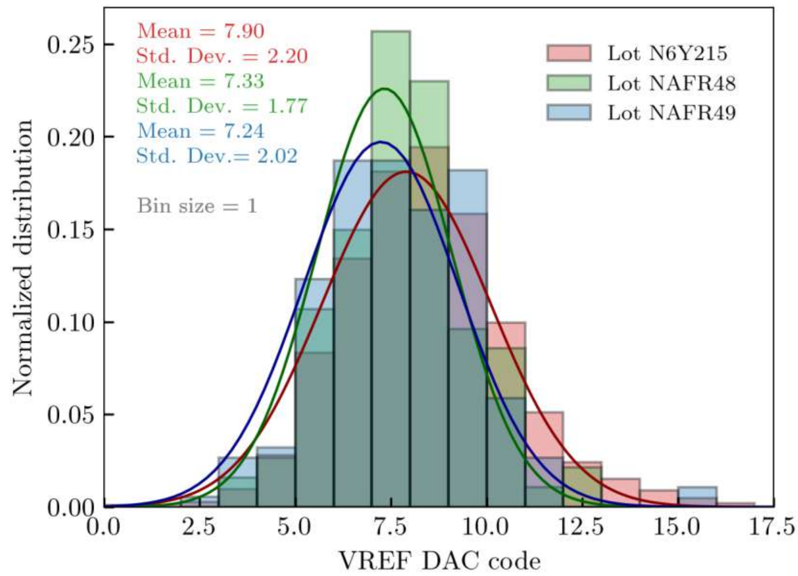

Figure 5.10: Distribution of per-chip calibrated DAC code for ADC reference voltage across all wafers of each lot.

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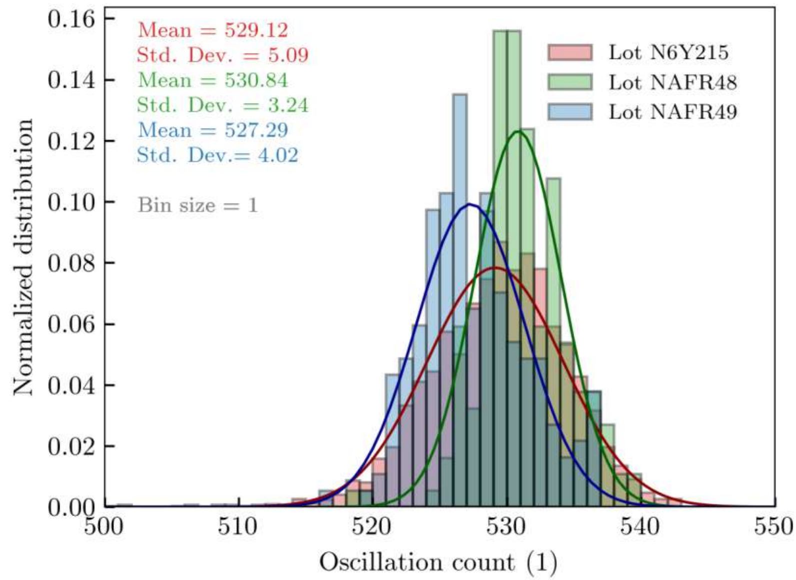

Figure 5.11: Distribution of per-chip delay-type RO oscilliation count across all wafers of each lot.

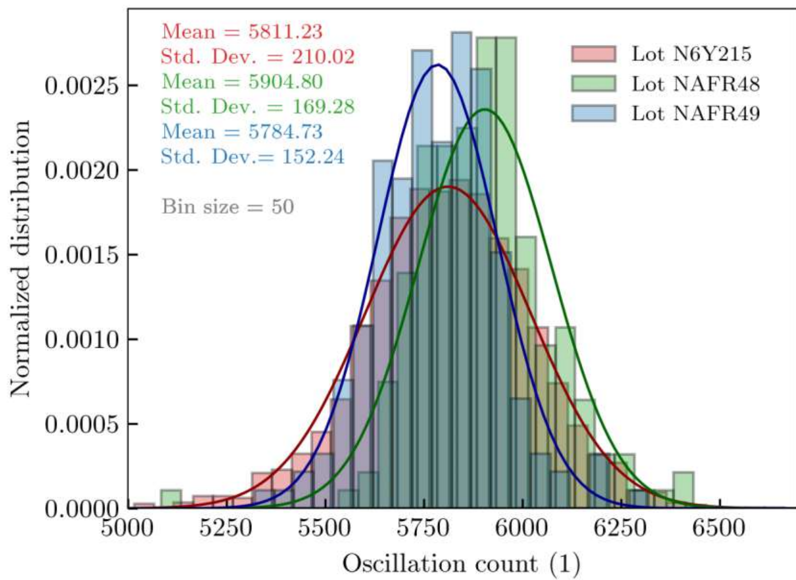

Figure 5.12: Distribution of per-chip inverter-type RO oscilliation count across all wafers of each lot.

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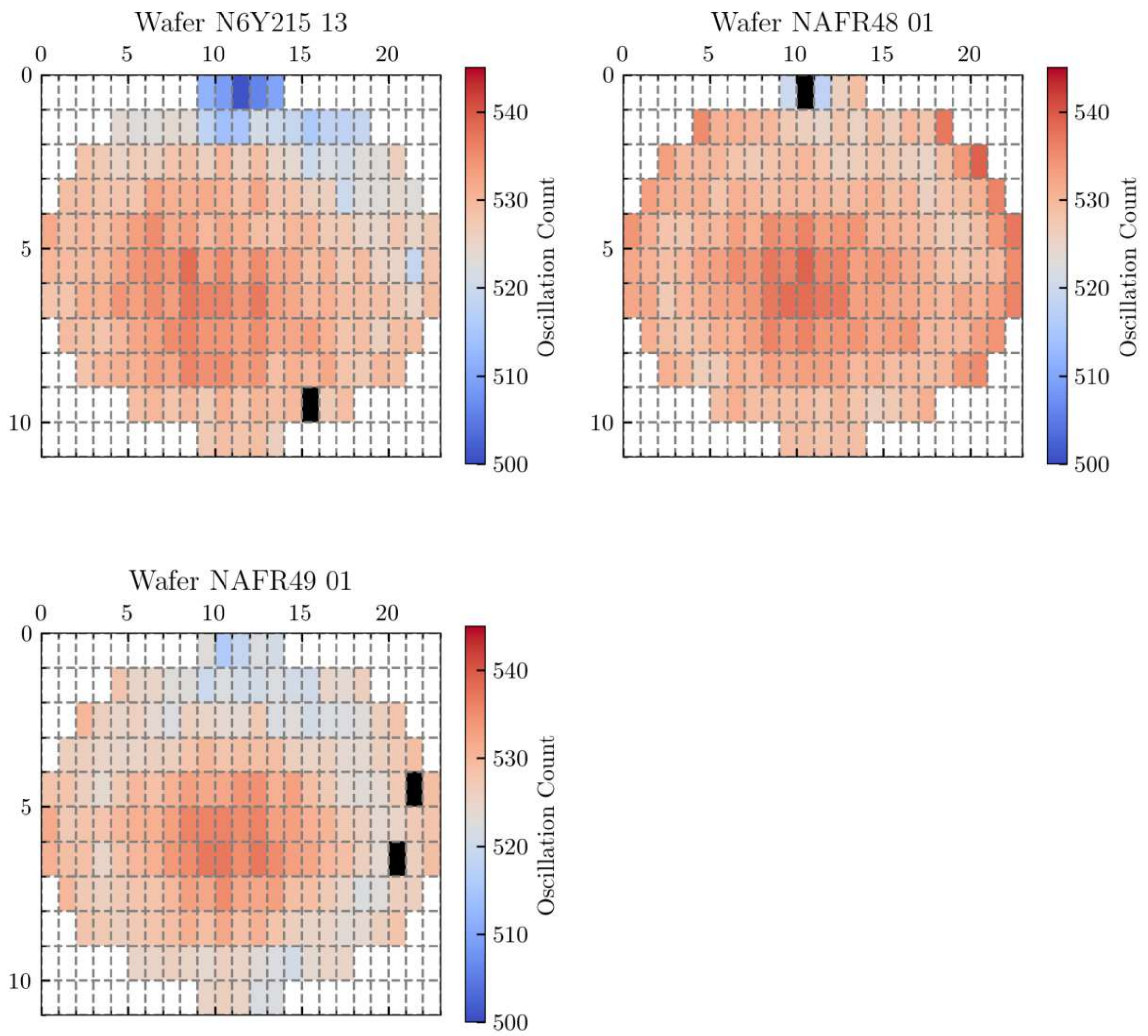

Figure 5.13: Location-dependant variability of the delay-type RO oscillation of one wafer per lot. Chips marked in black are failing or have measurement outside of the indicated range.

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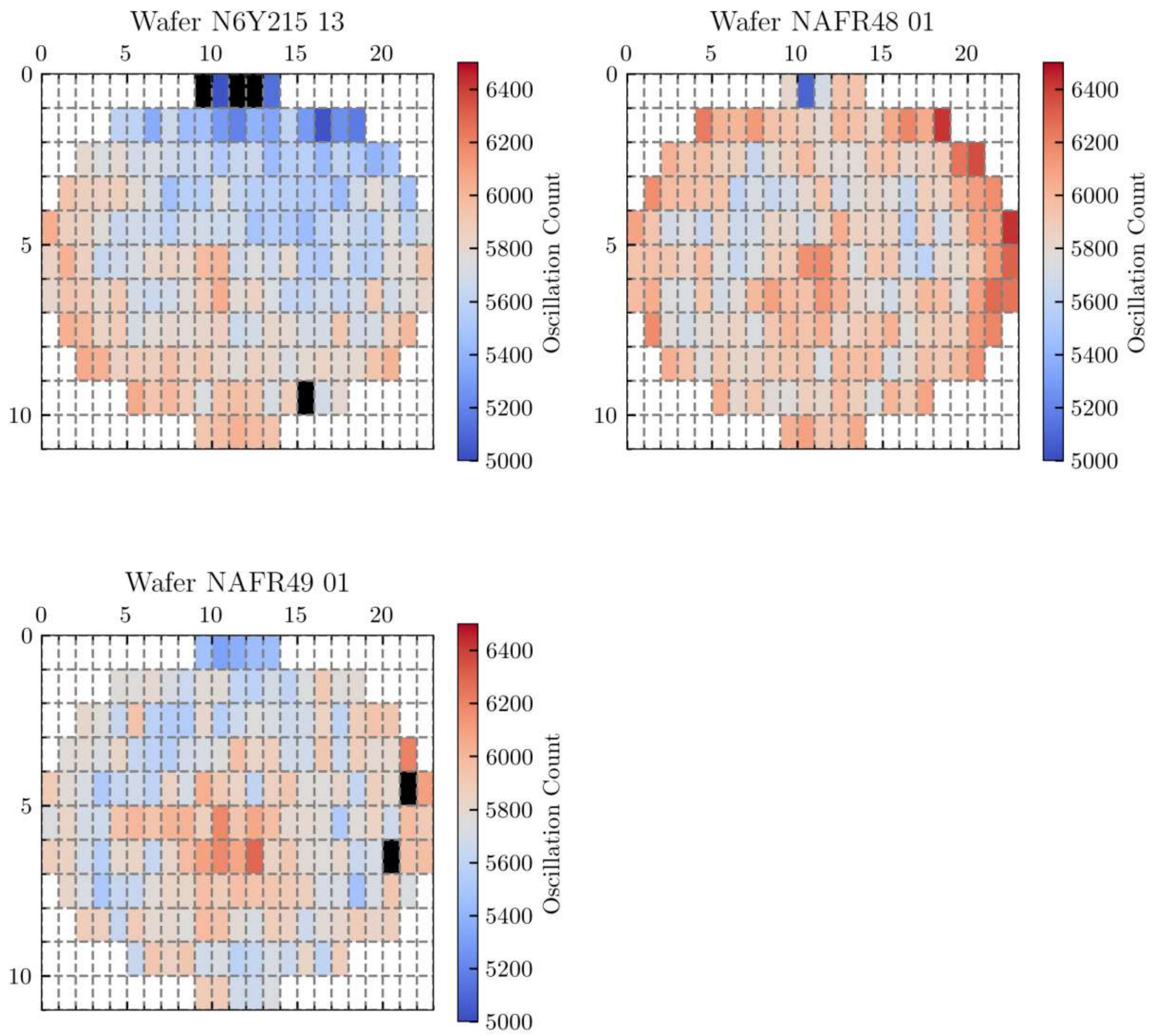

Figure 5.14: Location-dependant variability of the inverter-type RO oscillation of one wafer per lot. Chips marked in black are failing or their measurement is outside of the indicated range.

5.3.4 VDD Variation

Additional probing passes were undertaken for Wafer NAFR49_01 with different VDD profiles to understand how this may affect the performance of the chip and also its yield. VDD values were set to 10 % below and above the nominal values (see Table 5.6). The resulting wafer probing data can be considered in the case of deviating supply voltages within the PS module.

Voltage Profile	Analog (V)	Digital (V)	Periphery (V)
Standard	1.2	1.0	1.2
High VDD	1.32	1.1	1.32
Low VDD	1.08	0.9	1.08

Table 5.6: Voltage profiles applied for wafer testing of NAFR49_01.

Figure 5.15 shows yield values and locations of failing chips for each VDD profile. The yield rate is slightly reduced for the high and low VDD profiles, owed to individual chips failing the threshold trimming procedure and missing the $<$ 2 LSB yield cut-off for the threshold spread.

Figures 5.16 shows distributions of threshold trimming performance as threshold spread for each VDD profile. An increase of threshold spread variation can be seen for the low VDD profile, indicating that thresholds trimming capability is reduced. The lower supply voltages to the analog FE or bias DACs no longer allows the individual pixel thresholds to be trimmed to the target threshold for some pixels. However, since the cause is the software trimming procedure, the procedure could be better optimized for this case of deviating supply voltage causing greater variation in the thresholds.

Figure 5.17 shows distributions of the inverter-type RO oscillation for each VDD profile. As expected of RO oscillation behavior, the oscillation counts are affected by the driving supply voltage. At higher VDD, the standard deviation of the oscillation count increases.

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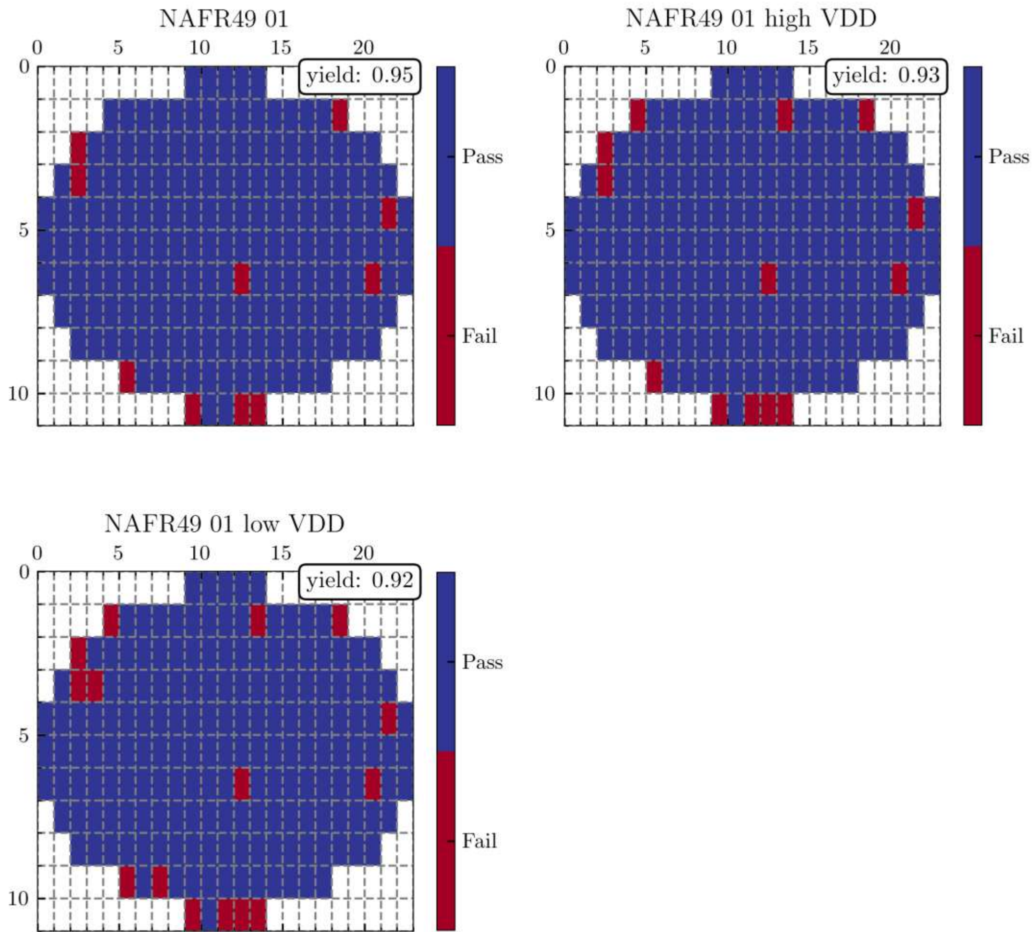

Figure 5.15: Yield variabililty and failing chips across wafer NAFR49_01 for each VDD profile.

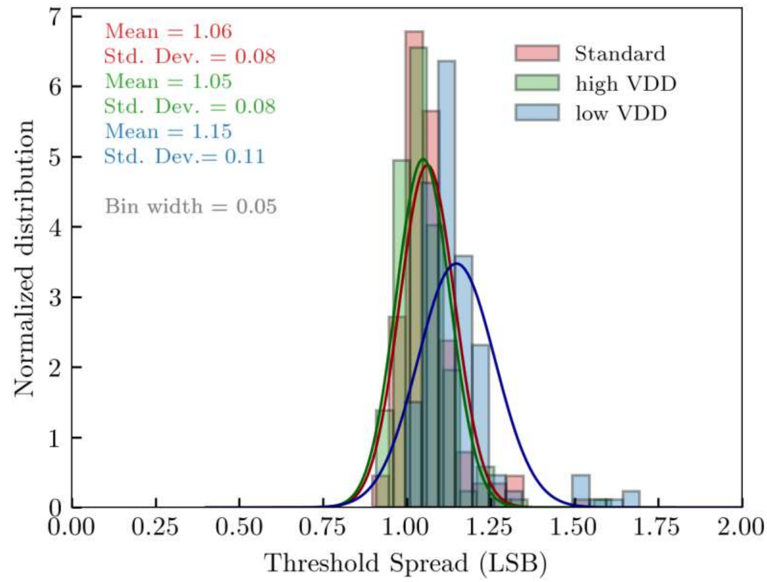

Figure 5.16: Distribution of analog FE trimmed threshold spread across wafer NAFR49_01 for each VDD profile.

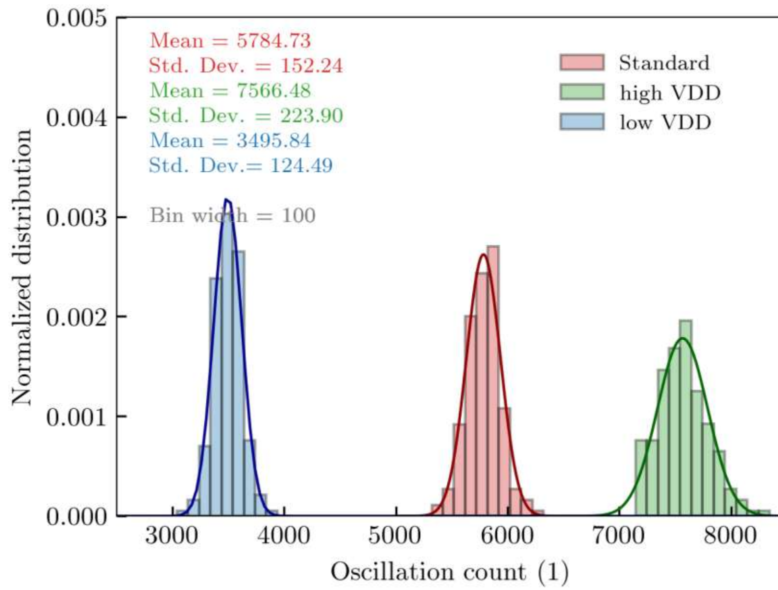

Figure 5.17: Distribution of inverter-type RO oscilliation count across wafer NAFR49_01 for each VDD profile.

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6 MPA2 Characterization Results

With Chapter 5 the procedure for the baseline functionality assessment of a given MPA2 chip was presented. However, to complete its full characterization and qualify if the MPA2 design and the processed chips are ready for the operation in the actual tracker, more detailed studies need to be considered. A readiness qualification for single ASICSs intended for the CMS Tracker typically consists of the irradiation testing of the chip (with respect to TID and SEU) and a climatic chamber test where the chip behavior to temperature variation is assessed. Based on these results, further testing of sub-assemblies and complete assemblies of modules are performed.

In this chapter, the setups and procedures for SEU, TID, and temperature testing conducted for the MPA2 within the scope of this thesis are discussed. The respective results are presented and linked with expectations formulated during the design phase of the chip.

6.1 SEU Testing

As described in Chapter 4, the MPA2 implements fault-tolerance towards SEUs in its circuit implementation and logic design. The capabilities of the SEU fault-tolerance can be experimentally tested and measured by irradiation of an MPA2 chip with heavy ions. The SEU irradiation testing and measurements for the MPA2 were carried out at the Cyclotron Resource Centre (CRC) of UCL[1] in Belgium. The CRC provides access to their Heavy Ion Facility (HIF) for radiation hardness testing of electronic devices [47]. This section describes the irradiation facility, test setup and procedures used for the MPA2 SEU irradiation. Based on these results, error rate estimations for radiation in the CMS Outer Tracker environment are made.

6.1.1 CRC Heavy Ion Facility

At the CRC, the Cyclone-110 cyclotron produces ion beams which are further used in various sub-facilities for neutron, proton, gamma, heavy ion and light ion irradiation [47]. At the HIF, a range of heavy ions are offered for irradiation testing by coupling of the cyclotron with an ECR[2] ion source. The thereby produced various heavy ions are

[1]Université Catholique de Louvain
[2]Electron Cyclotron Resonance

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accelerated towards a target device located in a vacuum chamber. Table 6.1 lists the different ions and their characteristic LET available at the HIF. The maximum achievable LET is 62.5 $\mathrm{MeV\,cm^2\,mg^{-1}}$ through Xenon ion beams.

Ion	**Energy** MeV	**LET** $\mathrm{MeV\,cm^2\,mg^{-1}}$	**Range (Si)** μm
$^{13}C^{4+}$	131	1.3	269.3
$^{22}Ne^{7+}$	238	3.3	202.0
$^{27}Al^{8+}$	250	5.7	131.0
$^{36}Ar^{11+}$	379	10.0	120.5
$^{53}Cr^{16+}$	513	16.0	107.6
$^{58}Ni^{18+}$	582	20.4	100.5
$^{84}Kr^{25+}$	769	32.4	94.2
$^{103}Rh^{31+}$	927	45.8	88.7
$^{124}Xe^{35+}$	995	62.5	73.1

Table 6.1: Available ions and corresponding LET in silicon for irradiation at HIF in UCL.

6.1.2 Test Setup and Procedure

Hardware Setup

For the SEU irradiation test setup, an MPA2 on a carrier-board was connected to the interface board and placed inside the vacuum chamber. Figure 6.1 shows the interface board fixed on a cooling plate before insertion into the vacuum chamber. As the irradiation takes place in vacuum, a water-cooled aluminum plate is provided within the chamber to affix and cool the device under test. The FC7 DAQ board is placed outside the chamber and connected to the interface board using long FMC cables. The FMC and power supply cables are passed through into the vacuum chamber using a custom flange with the respective cable sockets affixed to the chamber lid.

Located outside the chamber is the Host PC with the software testing routines, normally interfacing to the FC7 DAQ board over Ethernet. For the operation of the HIF, a graphical user interface is provided, which displays various monitoring values such as fluence levels and flux rates. Irradiation can also be started with this interface. The switching of the ion beams however is managed by a technical operator, who is also present during the testing.

SEU Fast Injection Routine

The MPA data paths are not directly protected against SEUs due to the strict power budget. During an irradiation window, L1 and stub data payloads are generated through the fast injection testing routine, described in 5.2.7, which checks output data against

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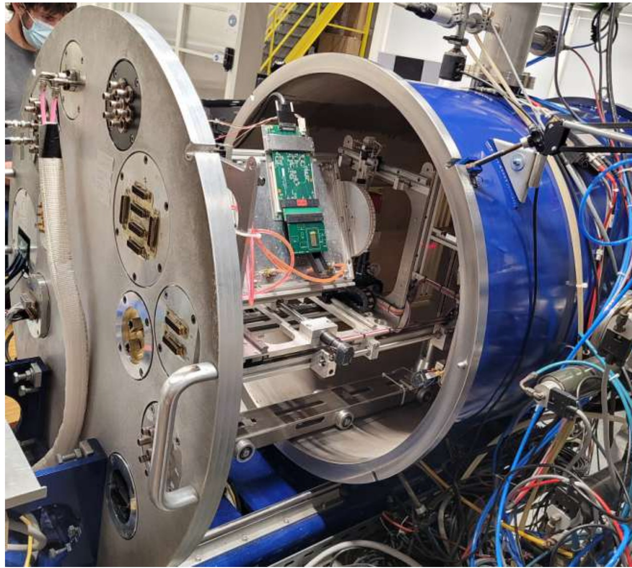

Figure 6.1: MPA2 and interface board fixed on the cooling plate and scaffolding to be inserted into the vacuum chamber. Also visible on the chamber lid are flanges with connections for the pass-through for power and FMC cables.

expected patterns and tracks bit-flips due to SEUs in real-time. 8 random strip and pixel centroids are injected at 20 MHz (every two BX) and L1 triggers are sent at 1MHz.

An SEU comparison state machine is implemented in the d19c firmware. It checks the read-out of L1 and stub data frames against the expected input. Events which do not match the input event are stored in FC7 memory blocks and are later read-out by the testing routine after the irradiation has concluded. Mismatched events are checked for the flipped bit and are summed as SEUs for the respective data path.

As for the configuration/control domain and the related clock signal distribution of the chip, the MPA2 implements a self-correction logic based on triplicated logic (see Chapter 4). Errors which are self-corrected are counted in dedicated SEU counter registers and are recorded through I2C read out by the SEU testing routine. These counts of self-corrected errors are summed under the *SEU Counters* value.

To summarize, the fast injection routine modified for SEU detection is able to assess the following error types:

- SEU Counter: self-corrected bit-flip occurring within the triplicated control and configuration domain of the Chip.
- L1 Error: bit-flip occurring within payload of the L1 data packet. The L1 data packet header is generated by triplicated logic and is not expected to experience errors.

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- Stub Error: bit-flip occurring within a stub packet of the trigger data stream.

Angle and Latency variation during Irradiation

For each ion irradiation, the angle of the MPA2 under test within the vacuum chamber was varied between 0 and 30 degrees in respect to the beam. Since LET is a measure of transferred energy per unit of distance travelled, a particle which crosses material at an angle transfers proportionally more energy in the volume. This variation of the angle thereby provides irradiation at one additional LET point per ion.

Additionally, the L1 latency in the MPA2 is varied between a high (500 cycles) and low (40 cycles) latency setting to evaluate the importance of the SRAM on the SEU cross-section. The latency set in the L1Offset register regulates how many entries are stored in SRAM. It is equivalent to the number of clock cycles for which the L1 data is stored. At a clock period of 25 ns, the latency setting of 40 cycles corresponds to 1 µs and the setting of 500 cycles to 12.5 µs (roughly the L1 latency). During an irradiation, a higher latency setting should incur increased amount of errors within the L1 data, as a higher latency results in longer storage periods and therefore increased probability for SEUs to occur.

For each set of ion, latency and angle, the MPA2 under test was irradiated up to a fluence of 5×10^6 particles/cm^2. All error values are read out immediately after completion of each irradiation set, which occurs after the depletion of the respectively available fluence.

6.1.3 Irradiation Results

For the range of LET and irradiation with available ions, variation of angle and latency, no hard errors of the MPA2 were observed, i.e. no loss of control or data synchronisation occurred. Over a total fluence of 170×10^6 particles, no uncorrected errors where detected for the I2C control of the chip. This indicates that the triplication of control and configuration logic is robust toward heavy ion irradiation and capable to correct SEUs.

According to Equation 2.4, the SEU cross-section for each ion is calculated by dividing the amount SEUs by the the irradiation fluence for which they occurred. The calculation of cross-section is also separated between the data paths and control/configuration logic to assess the variability between these domains. In the following, the resulting SEU cross-sections are shown in respect to LET for the control and configuration domain (i.e., *SEU counter* value) in Figure 6.2, for the stub data path in Figure 6.3, and L1 data path in Figure 6.4.

6.1.4 Estimation of Upset Rates for CMS Phase-2

This estimation of upset rates for the CMS tracker environment is based on the procedure described by Faccio et. al. [48].

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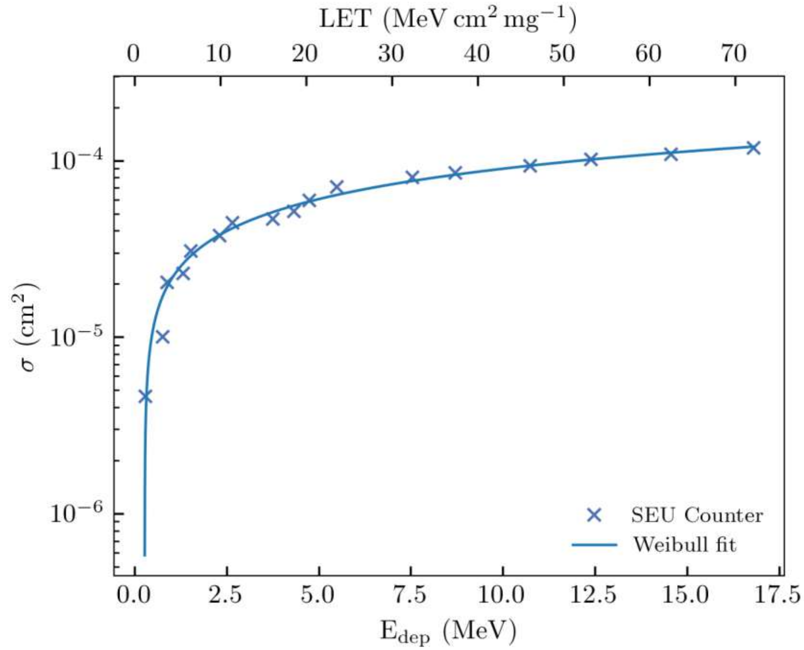

Figure 6.2: Resulting SEU cross-sections in respect to LET and E_{dep} for self-corrected errors. A Weibull function is fit to the data.

To evaluate the cross-section specifically for the CMS outer-tracker region and for 13 TeV proton-proton collisions, the cross-section functions from 6.1.3 are convoluted with the energy deposition probabilities for Hadrons above 20 MeV in the CMS outer tracker environment. Only higher energy hadrons may be considered, as their contribution to the upset rates dominates lower energy hadrons by one order of magnitude. The data for hadron energy deposition probabilities is provided by FLUKA simulations of the tracker environment and is provided by [48].

For each available energy bin i and the energy deposition probability P_i, the increase of sensitive area in this energy interval can be calculated from the Weibull function: $\Delta\sigma_i = (\sigma_{i+1} - \sigma_i)/\sigma_0$. The convolution operation to calculate the SEU cross-section Σ is then given by

$$\Sigma = \sum_i P_i \Delta\sigma_i \frac{\sigma_0}{A}, \tag{6.1}$$

where A is the the cross-sectional area of the considered sensitive volume ($1\,\mu\text{m} \times 1\,\mu\text{m}$).

The resulting SEU cross-sections for each domain as estimated for Hadrons above 20 MeV are listed below in Table 6.2.

Based on the cross-sections, the error rates can be estimated for particle flux magnitudes expected for the CMS Phase-2 Outer Tracker. The magnitudes of particle flux is strongly

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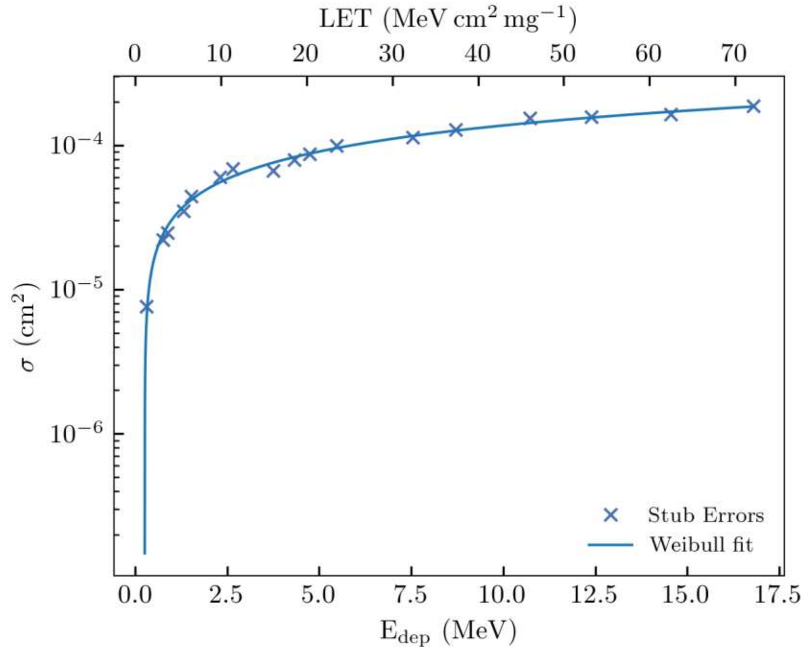

Figure 6.3: Resulting SEU cross-sections in respect to LET and E_{dep} for errors in *stub* data path. A Weibull function is fit to the data.

SEU domain	**Cross-section Σ** (cm^2)
L1 (low latency)	4.89×10^{-11}
L1 (high latency)	7.19×10^{-11}
Stubs	1.38×10^{-10}
SEU Counter	8.36×10^{-11}

Table 6.2: MPA2 Cross-sections for hadrons > 20 MeV.

dependant on r and z coordinate in the tracker barrel. As the error rate estimates are made for the worst-case, the location with the highest particle flux rates is considered for the calculation.

Expected flux rates for CMS are taken from the Radiaton Simulation Plotting (RSP) Tool provided to CMS users by the BRIL Radiation Simulation Team [49]. The simulation profile selected was `CMS_Phase2_TDR_pp_7TeV_FLUKA_v3.7.18.0` for an instantaneous luminosity of $10 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ and Hadrons above 20 MeV. According to the RSP tool, the maximum flux rate of $3.8 \times 10^{7}\,\mathrm{s^{-1}cm^{-2}}$ occurs closest to the interaction point at $r = 20\,\mathrm{cm}$ and around $z = 150\,\mathrm{cm}$ for untilted PS-modules ($\eta < 3.2$). The flux rate variation over the z coordinate is assumed as roughly uniform.

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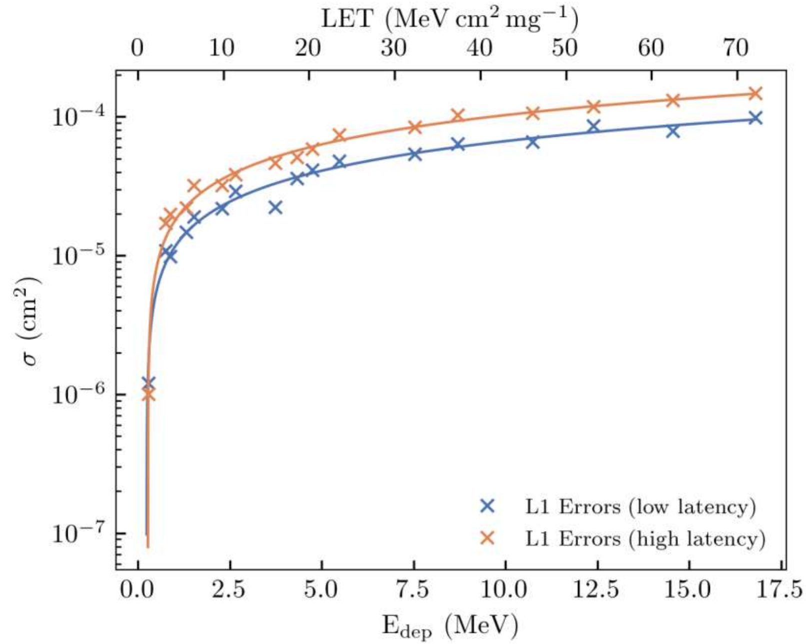

Figure 6.4: Resulting SEU cross-sections in respect to LET and E_{dep} for errors in *L1* data path for high and low latency setting. Weibull functions are fit to the data.

The error rates per SEU domain are calculated as the product of particle flux and the respective cross-section. The hadron flux rates for $r = 20\,\text{mm}$ and $r = 60\,\text{mm}$ and the resulting error rates are listed in Table 6.3. The increased amount of stub error rates is given by the fact that the error rates are shown as rate per second and not normalized per event. In other words, the read-out rate of the stub data is 40 times higher than that of the L1 data, so more errors are observed in the stub data per second.

r (cm)	**Flux** ($\text{s}^{-1}\text{cm}^{-2}$)	**L1 (low lat.)** (s^{-1})	**L1 (high lat.)** (s^{-1})	**Stubs** (s^{-1})	**SEU Counter** (s^{-1})
20	3.8×10^7	1.86×10^{-3}	2.73×10^{-3}	5.24×10^{-3}	3.18×10^{-3}
60	2.32×10^6	1.13×10^{-4}	1.67×10^{-4}	3.2×10^{-4}	1.93×10^{-4}

Table 6.3: Estimated SEU rates for the MPA2 in the PS module region. Flux rates are based on FLUKA radiation simulation of CMS Phase-2 for an instantaneous luminosity of $10 \times 10^{34}\,\text{cm}^{-2}\text{s}^{-1}$ and hadrons $E > 20\,\text{MeV}$.

6.2 TID Testing

The TID characterization of the MPA2 is performed by photon irradiation based on x-rays. This section describes the irradiation facility and the testing procedure used to qualify TID effects in the MPA2. The results and an interpretation are presented subsequently.

6.2.1 X-Ray Irradiation Facility

The high TID levels expected for the HL-LHC require an irradiation facility capable of high dose rates in order to keep the duration of the irradiations tests within reasonable time frames. Typically, photon irradiation is performed using either of two sources: γ-rays or X-rays [50]. As X-rays allow higher dose rates and are less energetic (therefore safer to handle) compared to γ-rays, they are the preferred radiation source for qualification of electronics for the HL-LHC.

The irradiation facility at the CERN Electronics Systems for Experiments (ESE) section makes use of a Seifert R149 X-ray machine [51]. The machine uses a 10 keV X-ray irradiation source and is capable of providing a maximum dose rate of 10 Mrad/h. It consists of an X-ray tube and an adjustable positioning frame, placed within an irradiation cabinet to prevent X-rays from scattering into the environment. The enclosable inside of the cabinet with an MPA2 under test is shown in Figure 6.5. A cooling plate is available to irradiate devices under controlled temperatures. Cables and wires needed for a test-bench placed within the chamber are passed through a metal-shielded opening on the side of the cabinet.

A positioning frame allows the orientation of a device under test against the X-ray beam. The delivered dose rate and the X-ray beam profile are regularly measured with the use of positive intrinsic negative (PIN) photo-diodes, which have a pre-calibrated current behavior proportional to the dose rate. A precise spatial distribution map of the beam's dose rate is available, showing that the X-ray beam profile is not uniform in terms of its dose rate, whereas some sections of the beam show less variability than others (see Figure 6.6). As such, a device under test needs to be positioned with mm-precision in order to guarantee its irradiation with minimal variability across the device's physical dimensions.

6.2.2 Irradiation Setup and Procedure

Three irradiation runs on three different MPA2 chips were conducted, differing in their dose rates and the achieved TID. The irradiation runs are listed in Table 6.4. For all runs, a TID of over 200 Mrad was targeted to study the MPA2 behavior towards expected tracker radiation doses with an additional safety factor of $\times 2$. Run 1 was completed first in time but without any cooling applied to the chip. Run 2 was not completed, due to

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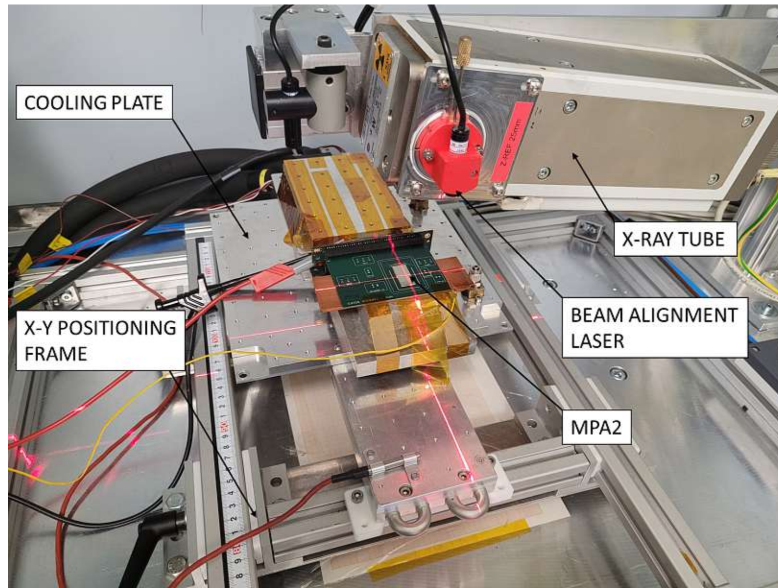

Figure 6.5: View of the cabinet inside of the X-ray irradiation machine at CERN ESE. An MPA2 carrier-board connected to the interface board (hidden by metal for shielding) is fixed on the cooling plate and positioned against the X-ray beam using the alignment laser.

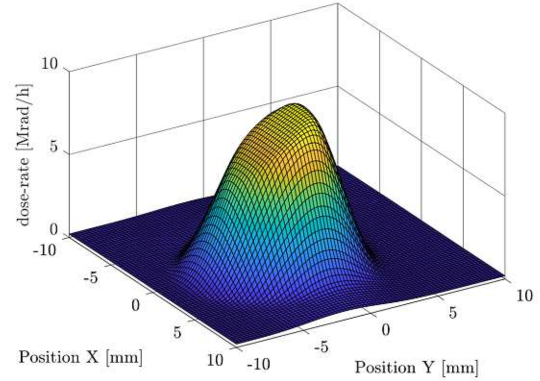

Figure 6.6: Example map of the X-ray beam profile and its location-dependent dose-rate generated moving a PIN diode in steps of 0.1 mm with the beam placed 2 cm from the diode [15].

a malfunction in the interface board which occurred during the irradiation. Run 3 was completed with the chip under test cooled directly through a aluminum cooling plate during the entire course of the irradiation.

Due to the comparatively large size of the MPA2, the dose rate was initially limited to

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Run Name	Dose Rate (Mrad/h)	Max TID (Mrad)	T-control (°C)
Run 1	1.34 ±10 %	200	None
Run 2	1.34 ±10 %	40	0
Run 3	2.37 ±10 %	224.5	6

Table 6.4: Details on TID testing runs performed on the MPA2.

1.34 Mrad/h. After a re-calibration of the X-ray Machine, a dose rate of 2.37 Mrad/h was attained. For all measurement runs, the beam was placed 10 cm away from the target MPA2, thereby achieving a maximum variability of ±10 % in the dose rate across the chip. This means, that for the target 225 Mrad, one part of the chip is irradiated to an actual 202 Mrad at minimum while the other is irradiated to 247 Mrad at maximum. Both dose rates achieved are in the range of Mrad/h and are therefore considered high dose rates [15]. As such, dose-rate-dependent variation between the measurements of the irradiation runs presented here can be excluded.

During the entire irradiation procedure, the logic was kept in an actively biased state with the use of the fast injection routine described in Section 5.2. This is a general recommendation for irradiation testing in order to avoid unrealistic bias-dependent effects on the devices. The testing routine runs the full functional testing and measurement suite at periodic intervals to monitor and record power consumption, analog front-end performance and digital functionality against the current TID level. Additional read-out of ADC monitored values was added to assess the performance of the monitoring block during the irradiation. A selection of the TID irradiation results in the MPA is listed in the following sections.

Note: The following figures presenting measurements made in respect to TID include dashed vertical lines which indicate the end of the X-ray irradiation and start of the annealing period for Run 1 and Run 3. Due to errors in the software procedure during the irradiation in combination with a repeated malfunctioning of the interface board, there are gaps in the data for Run 1 between 10 Mrad to 30 Mrad, and for Run 3 between 25 Mrad to 50 Mrad. The interface board malfunction is attributed to overheating of a specific component that handles the voltage level of the RESET input pad of the MPA, therefore putting the chip in an unrecoverable reset mode.

6.2.3 Digital Tests

The MPA2 digital functionalities include all tests with exception of the analog tests listed in Table 5.3. In the Run 1 uncontrolled temperature irradiation, the MPA2 under test exhibits the first failures in its digital functionality at around 160 Mrad with a failure of the Row BIST test. After 180 Mrad, further capabilities such as phase alignment and

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injection tests are lost at which point the chip is considered no longer functional. The I2C control and configurability of the chip is finally lost after around 200 Mrad but recovers after around 8 h of annealing at room temperature. The other digital functionality is recovered after an annealing period of around 20 h.

In contrast, during the Run 3 irradiation with a low-temperature controlled chip, the digital functionality is preserved for the full course of the irradiation. This result underlines the strong temperature dependency of radiation-induced degradation effects in the 65 nm technology used for the MPA2.

6.2.4 Power Consumption

During the irradiation, the current consumption of the different MPA2 power domains was measured with the supply voltages set to their typical values (see Table 4.2). Figure 6.7 shows an increase in leakage current of the digital domain of the chip with respect to TID. A fast rise is exhibited during early TID levels for both runs. This is due to the expected behavior of nMOS transistors with increasing TID levels in 65 nm technology. The leakage current is reduced to ~5 % in the low temperature run.

Figure 6.8 shows the consumption of the analog domain decreasing in respect to TID for all runs. While increasing leakage current should also be occurring in the analog domain, the decrease in consumption seems to be dominated by I_{ON} current degradation of pMOS transistors. Once again, the degradation effect is reduced in the temperature controlled measurement.

Both the IO and digital domain are not shown, as the variation of their current consumption remains within ±2 % for all temperature scenarios. The digital power consumption however increases for Run 1 and decreases for Run 3. Figure 6.9 shows the total current consumption with a decrease of less than 10 % for both temperature scenarios. It appears that the degree of degradation of the total current consumption does not strongly vary with the temperature, but this is due to the decreased consumption of Run 1 being offset by a most likely heat-induced increase over the course of irradiation. In general, the measurements indicate a good robustness of the powering domain in the MPA2 toward high TID levels.

6.2.5 Analog FE Performance

Figures 6.10, 6.12 and 6.11 respectively show the analog FE performance in terms of average threshold spread, noise and gain averaged across the chip during irradiation.

Very noticeable is the increased scattering of trimmed threshold spreads shown in Figure 6.10 after around 50 Mrad in the Run 1 irradiation. This indicates that the threshold procedure is no longer performing well, due to the upper and lower bounds for trimmed

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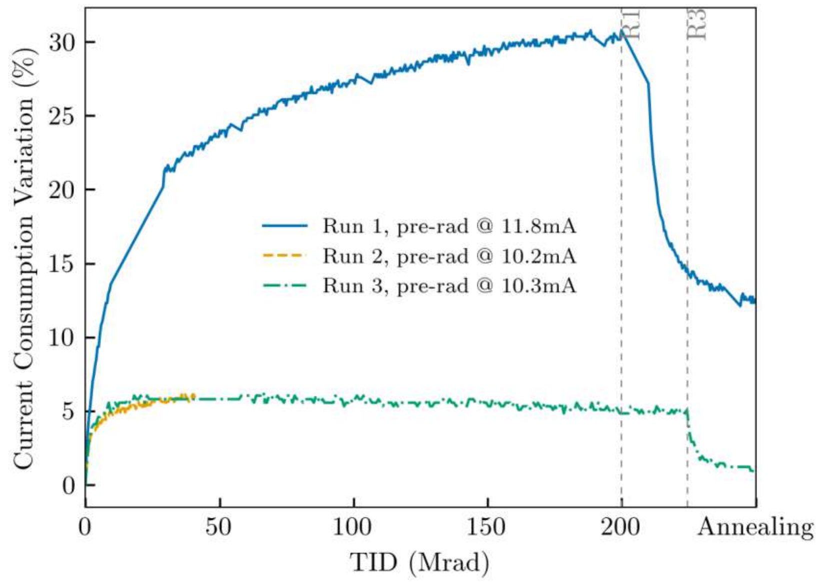

Figure 6.7: Leakage current variation in respect to TID.

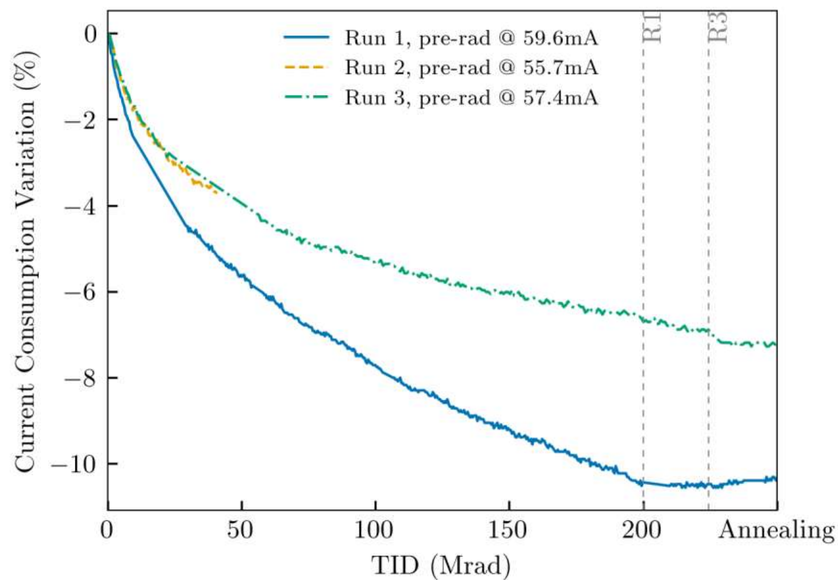

Figure 6.8: Analog current variation in respect to TID.

thresholds in the procedure being set manually based on old parameters. The trimming procedure was subsequently improved to automatically select an appropriate midpoint for threshold trimming during each trimming procedure, thereby compensating the threshold variations induced by the radiation dose. This results in the very stable

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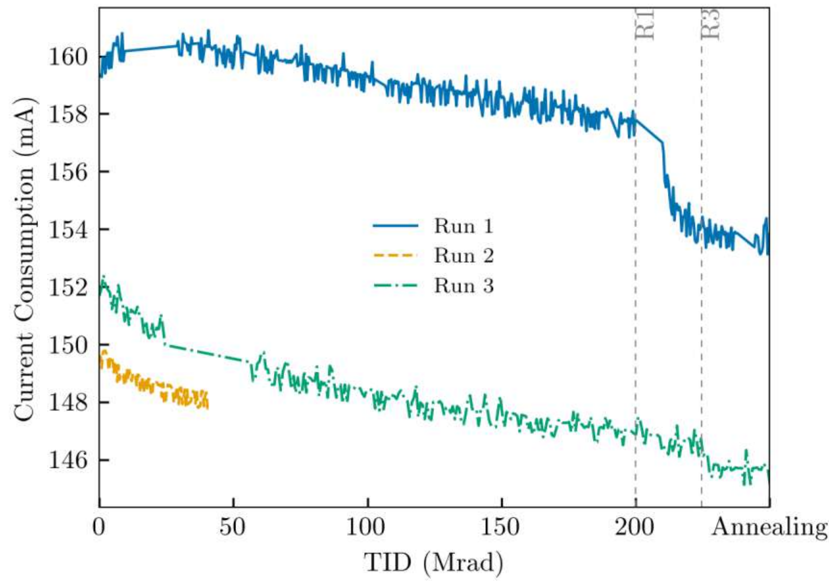

Figure 6.9: Total current consumption in respect to TID. The offsets between the total consumptions stems from variations between the tested chips and the quality of the test setup connection established in each measurement run.

threshold spread toward increasing TID seen for Run 3. Consequently, the noise and gain extracted from the trimmed S-curves remain stable during Run 3, whereas they are more erratic for Run 1 (see Figures 6.11 and 6.12).

The average gain of the amplifiers in the analog FEs also shows a slightly rising slope with respect to increasing TID seen in Figure 6.11. This can be explained by the TID-induced reduction of the current available to the ThDAC and the consequent reduction of its output voltage per input LSB (from initially 1.445 to 1.410 $\mathrm{mV/LSB_{ThDAC}}$ at the end of irradiation in Run 3). Thereby, the global thresholds that are set for all pixels by the manual parameters for the trimming procedure are slightly decreasing with increasing TID. As the gain is determined based on the output response of the discriminator, which now has a reducing threshold against the injected calibration charges, its value is increasing over TID. Although the increase is not high, this indicates that the S-curve-based extraction of the gain could be improved to also compensate for the shift in the ThDAC resolution.

The results show that the variations in the thresholds of the analog pixel FE and their drift during irradiation can be equalized depending on the trimming procedure algorithm. Furthermore, the functionality of the required calibration components in the analog FE are proven to be robust to high levels of TID.

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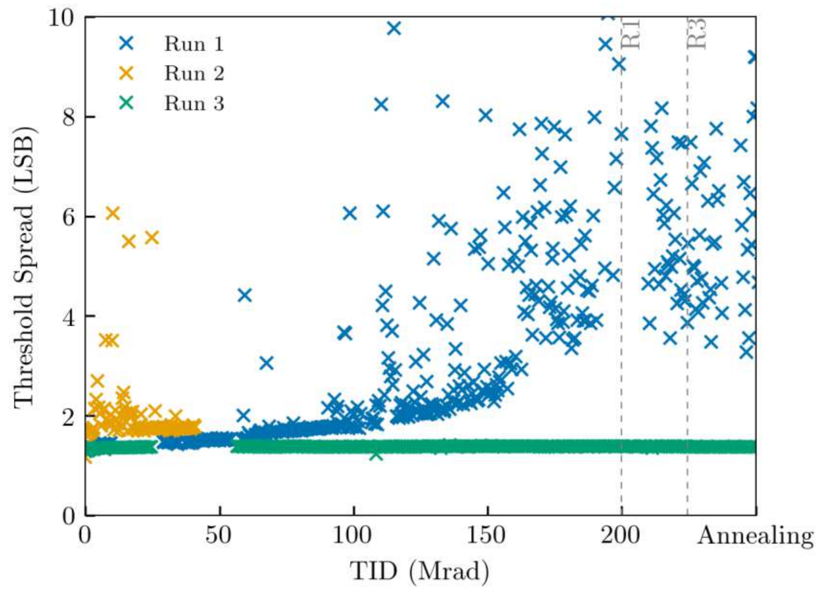

Figure 6.10: Analog FE trimmed threshold spread in respect to TID.

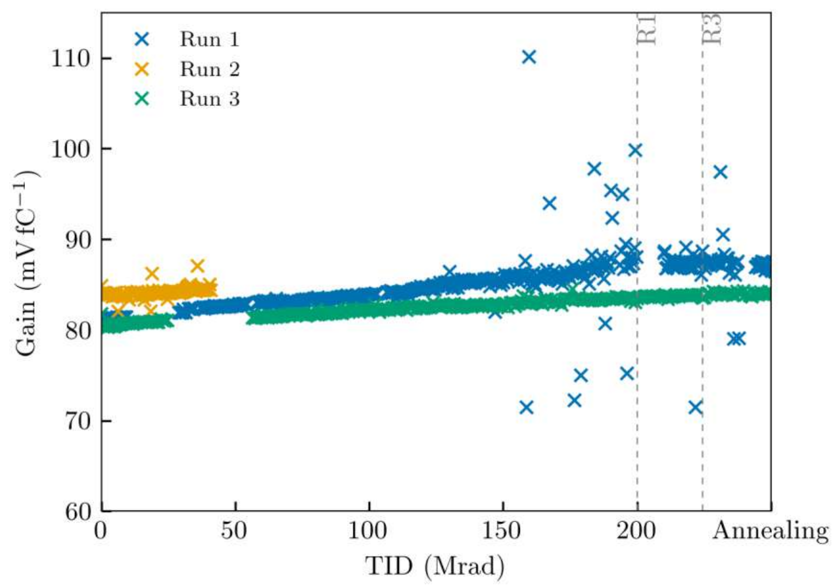

Figure 6.11: Chip-average analog FE gain in respect to TID.

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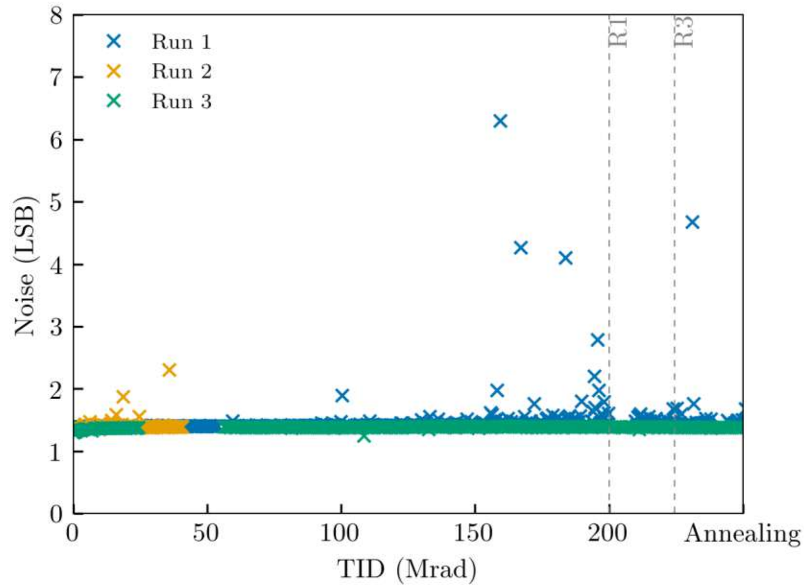

Figure 6.12: Average analog FE noise in respect to TID.

6.2.6 Ring Oscillators

The measurement of the RO oscillation behavior toward TID is shown in Figure 6.13. In general, the oscillation frequency degrades with respect to TID, but it can be seen that the sensitivity is different between inverter-type and delay-type RO based on the different transistor sizing used for the two types (see Section 4.6.2). This difference of sensitivity is the intended mechanism by which the inverter-type RO could be utilized as on-chip monitor of the radiation dose. The oscillation degradation is however reduced for both types in the temperature controlled measurement, owed to the increase in electron mobility for cooled devices. The degree of TID sensitivity still remains distinguishable between the two RO types.

6.2.7 ADC Reference DAC

A shift of the ADC Reference DAC code in respect to TID for the controlled and uncontrolled temperature measurement is shown in Figure 6.14. The depicted offset between the pre-rad DAC codes does not stem entirely from the temperature difference, as at room temperature the Run-3 chip had a pre-rad DAC code of 10 LSB. The offset rather comes from variation between the two chips under test and the quality of their electrical contact in the test system.

The DAC is seen to shift its code to maintain the 850 mV ADC reference voltage over the course of the irradiation. This effect occurs for most of the DAC units used on the

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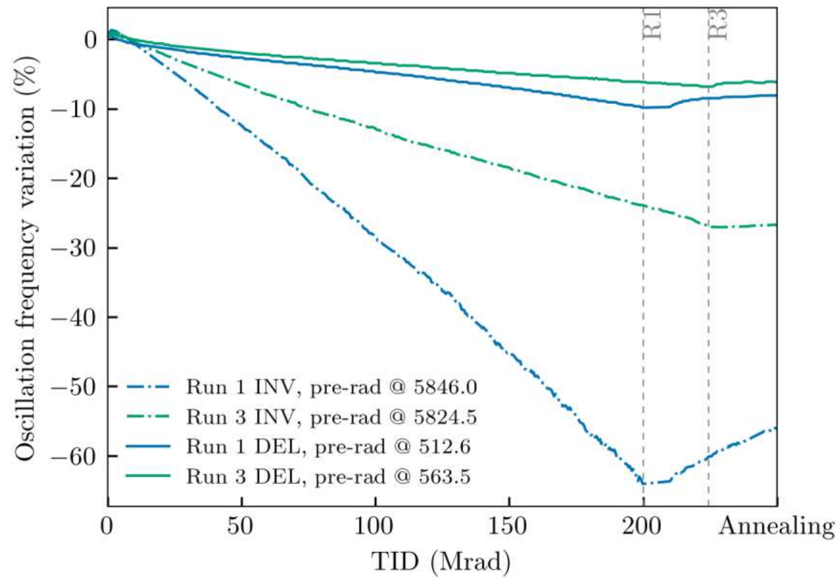

Figure 6.13: Ring oscillator variation over TID.

chip. Due to degradation of I_{ON} currents of pMOS transistors in high TID levels, the current range supplied to the DACs is decreased with rising TID. As such, the LSB resolution decreases and the DAC code needs to be shifted up to maintain the same level of bias voltage. In the case of the MPA2 DACs, the required quantization shift remains well within the range of the 5-bit DAC range (0 to 31 LSB). In the temperature controlled measurement, the number of quantization shifts required is reduced, due to less TID-induced current degradation experienced by the transistors in lower operating temperatures.

6.2.8 ADC Monitoring

The 12-bit ADC was measured for its TID robustness in terms of the digital measurement of the bandgap reference voltage and read-out of the on-chip temperature sensor. Figure 6.15a shows the Run 1 measurement for uncontrolled temperature. For comparison, the bandgap reference voltage measured by the external multimeter is shown in the blue dashed line. The externally measured bandgap voltage exhibits a very stable variation towards TID, whereas the same measurement read-out by the ADC monitor seems to exhibit an offset and also degrades with increasing TID[3].

By plotting only the delta to the pre-rad values in Figure 6.15b, the degree of degradation becomes more clear and the steps in the measurements can be associated with the quan-

[3]For the ADC read-out in voltage values, the binary ADC output code is converted with the gain factor 0.22 mV/LSB.

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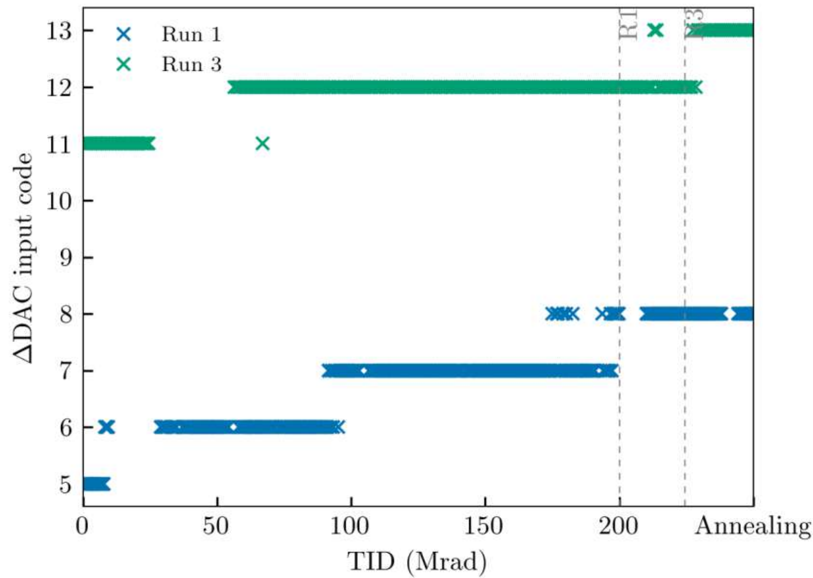

Figure 6.14: Variation of the VREF DAC input code in respect to TID.

tization shifts occurring for the ADC Reference DAC shown in Figure 6.14. The ADC bandgap measurement follows quite closely the temperature sensor measurement, showing that the effect is based on radiation-induced degradation of I_{ON} currents. In general, the temperature sensor has a negative voltage slope with increasing temperatures, as is shown in the temperature testing section (see Figure 6.23). When the irradiation is stopped around 200 Mrad, the temperature measurement increases during the room temperature annealing, due to falling temperatures on the chip in the absence of the X-ray beam. The bandgap measurement remains at its degraded level.

In the temperature-controlled measurement, the ADC measurement is more stable towards TID as can be seen in Figure 6.16b. A temporary drop of the ADC bandgap measurement is seen starting around 180 Mrad. At this point it is not clear as to what this can be attributed to.

6.2.9 Additional Remarks

The TID irradiation runs conducted for the MPA2 show that the chip is robust towards high TID levels as no early breakdown of its functionality occurs. As the expected doserates for the tracker are in the order of three magnitudes lower, the MPA2 was irradiated to a factor 2 beyond the worst-case 100 Mrad dose expected for 10 years of HL-LHC operation. TID-induced degradation of variations of the MPA2 were characterized and are shown to be significantly reduced for the chip operated at lower temperature.

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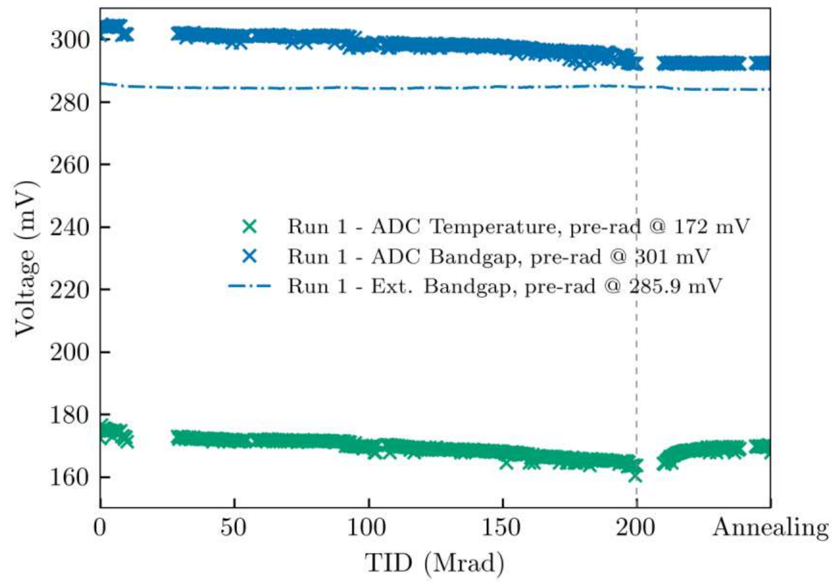

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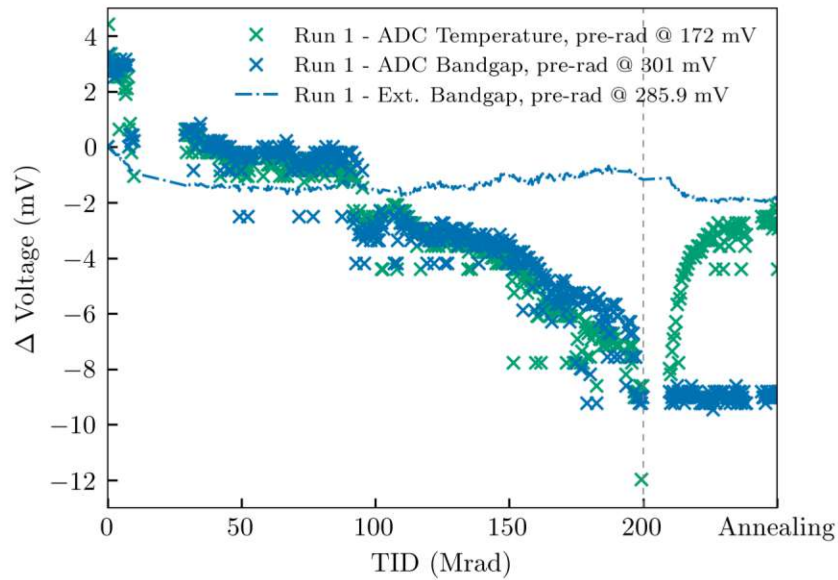

(b)

Figure 6.15: ADC measurement of the bandgap voltage and temperature in respect to TID for Run 1. In absolute values (a) and delta values (b). The externally measured bandgap by the multimeter is added as a blue dashed line. The grey dashed line represents the end of the irradiation and beginning of annealing.

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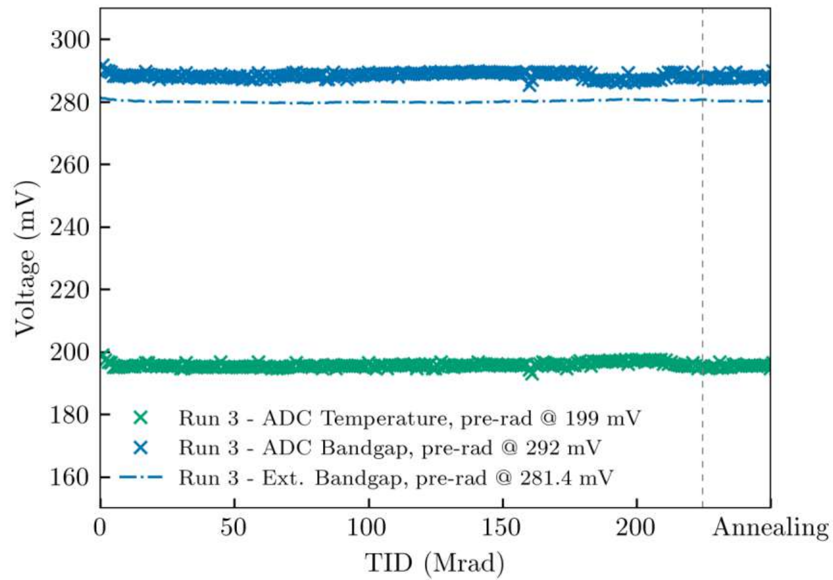

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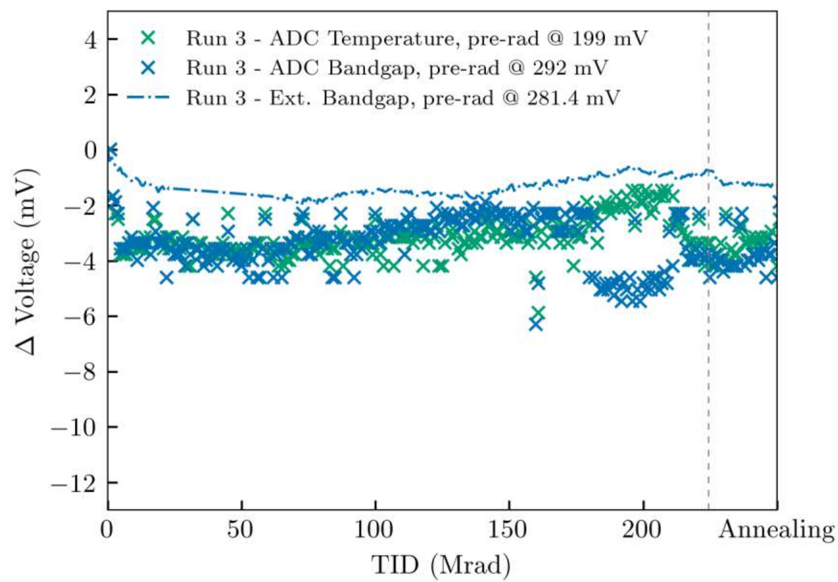

(b)

Figure 6.16: ADC measurement of bandgap and temperature in respect to TID for Run 3. In absolute values (a) and delta values (b). The externally measured bandgap by the multimeter is added as a blue dashed line. The grey dashed line represents the end of the irradiation and beginning of annealing.

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6.3 Temperature Testing

Temperature testing of the MPA2 was performed to characterize its performance against variation of the ambient operating temperature with the Climats EXCAL 1423-HA climatic chamber provided by CERN ESE [52]. The CMS Outer Tracker cooling system aims to maintain silicon sensor temperature at $-20\,^{\circ}\mathrm{C}$ or lower. In the PS Module, cooling will be applied by a carbon fibre reinforced polymer baseplate attached to the PS-p sensor. The final operating temperature to be achieved for the MPA2 in the tracker is still to be exactly determined and will be subject to further testing of the assembled tracker and its modules. As such, the temperature testing conducted for the the MPA2 in this thesis serves to inform on the chip functionality and drift of its characteristics toward a wide range of temperatures.

6.3.1 Test Procedure

The carrier-board mounted MPA2 and the interface board are placed within the climatic chamber as shown in Figure 6.17. A compressed air dryer prevents humidity damage to the electronics in sub-freezing temperatures. Apart from the temperature control provided by the machine, an additional temperature sensor is attached directly on the carrier-board with adhesive to accurately monitor the chip temperature.

Figure 6.17: MPA2 carrier board and interface board within the ESE Climats EXCAL 1423-HA climatic chamber.

The software test procedure used is very similar to the TID testing routine described in Section 6.2. Temperature range performed for the test starts from $-40\,^{\circ}\mathrm{C}$ to $40\,^{\circ}\mathrm{C}$ with a rate of the temperature increase set to $0.2\,\frac{^{\circ}\mathrm{C}}{\mathrm{min}}$. To collect temperature-based datapoints, the functional testing routine and additional measurements were scheduled to run in fixed intervals of 3 minutes. In general, the MPA2 stays functional for the full range of the tested temperatures. All digital functionalities for the MPA2 (data alignment, hit

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processing and DFT features) are passed for each temperature point. Nevertheless, the chip exhibits some temperature-dependant variation in its power consumption, analog FE response and bias values.

The main contributor by which a variability to temperature occurs, is by the temperature dependance of the electron mobility μ and threshold voltage V_t in the drain current of MOS transistors. In general μ increases and V_t decreases with rising temperatures. Depending on the polarity of the transistor and its inherent V_t however, its drain current can decrease (μ dominated) or increase (temperature inversion effect due to high V_t) with higher temperature.

6.3.2 Power Consumption

Figure 6.18 shows the variation of the static current consumption of the three voltage domains (analog, digital and periphery), the total consumption and the leakage current of the digital domain. The supply voltages are set to their typical values listed in Table 4.2.

The digital domain consumption increases by up to 5 % (+3.7 mA). This increase consists almost entirely of its leakage current increase, which increases by up to 40 % at +40 °C (+3.5 mA). For the analog domain, the increase is more difficult to distinguish. On top of leakage current increases, the bandgap reference voltage also increases, convoluting the current consumption increase over various bias levels for the analog FEs. In any case, the consumption of the full chip and its three voltage domains increases by less than 10 % for the tested temperature range. Converted to the static power consumption, the consumption goes from 146 mW at −40 °C to 159 mW at +40 °C.

The dynamic current consumption, i.e., the current consumption during high rates of injected pixels/strips and sent L1 triggers, was not measured against temperature variations. The dynamic power consumption measured at room temperature in Section 6.4.1 indicates that, even at higher temperatures, there should be more than enough margin in the allocated power budget of the MPA2 (∼ 200 mW).

6.3.3 Reference Voltages

Figure 6.19 shows the variation of reference voltages toward temperature. Shown here, are the ADC reference voltage, bandgap voltage, and the ground contact voltage as measured by the external voltmeter. To be noted is that the ADC reference voltage depicted here is the uncalibrated value (set by the default input code of the reference DAC).

The bandgap voltage increases by a slope of $\approx 160\,\frac{\mu V}{°C}$. The temperature coefficient measured here is higher than the $\sim 130\,\frac{\mu V}{°C}$ measured for an isolated and best-performing bandgap circuit sample reported in [32]. Nevertheless, the bandgap reference voltage in

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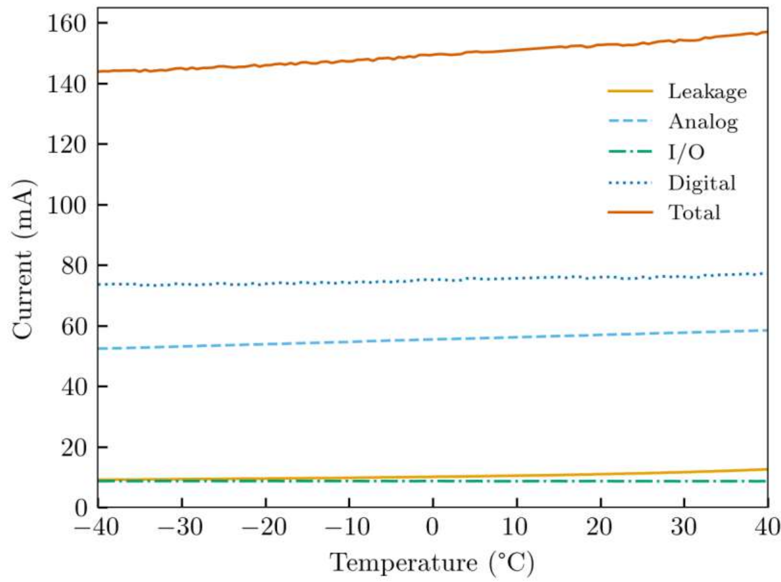

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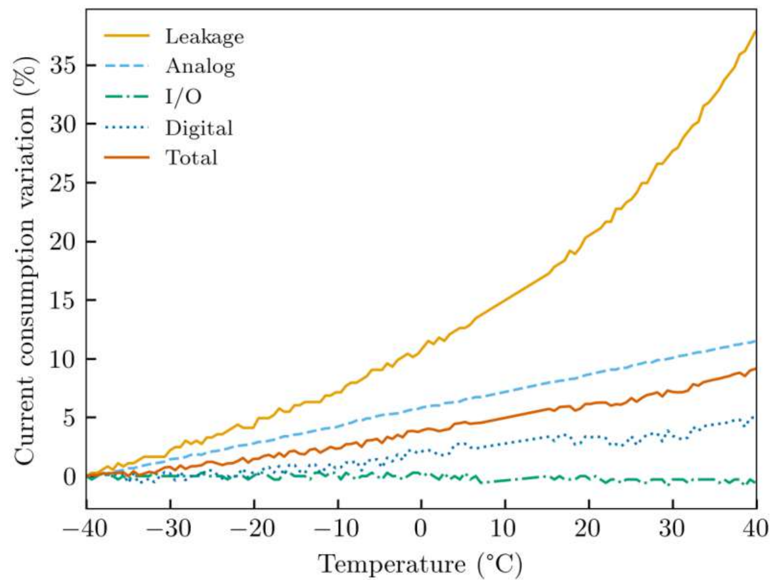

(b)

Figure 6.18: Current consumption in respect to temperature in absolute values (a) and relative values (b). The variation of the total current consumption relative to consumption at $-40\,^{\circ}\mathrm{C}$ remains less than $10\,\%$.

the MPA2 is considered sufficiently stable towards temperature variation in the tested range.

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The ADC reference voltage set by a default ADC Reference DAC value of 15 increases based on the effect described in the next section.

6.3.4 ADC Reference DAC

Figure 6.20 shows the behavior of the required DAC input code to maintain the 850 mV ADC reference voltage in respect to temperature. The required DAC input shifts down in higher temperatures, a behavior which is not immediately apparent. The DACs used for the MPA2 are based on weighted pMOS current sources switched for the individual binary inputs. This pMOS transistor is based on a high V_t cell library, so it is assumed that the higher temperature causes an increase in the drain current (temperature-inversion effect), thereby reducing the LSB input needed to establish the nominal ADC reference voltage.

At room temperature, the mean DAC code set by the MPA2 calibration procedure is around 7 to 8 LSB as seen for the chips tested during wafer probing (see Figure 5.10). A few chips also exhibit a calibrated DAC code of 2 LSB or less. Considering the quantization shifts seen from 20 °C to 40 °C it would suggest, that those DACs might not be able to calibrate to the 850 mV nominal ADC reference voltage in high temperature scenarios. This degree of high temperature should however not occur in the tracker under any nominal operating circumstance.

6.3.5 Analog FE Performance

The chip-average analog FE performance was measured against temperature. The result is shown in terms of threshold spread and noise in Figure 6.21a and gain in Figure 6.21b. As expected, the noise levels increase with higher temperatures. The gain of the pre-amplifiers is reduced in high temperature scenarios presumably due to the higher currents provided to the ThDAC. Thereby the global thresholds are increased, as they are set by fixed values in the threshold trimming procedure. In other words, an opposite effect is seen for the gain compared to the TID behavior (see Figure 6.11), as in the case of temperature testing, the ThDAC is suspected to being supplied more current due to the temperature-inversion effect in its input transistors.

In the case of threshold spread, it is seen to be improving at higher temperatures. This effect should be attributed to the threshold trimming procedure which was originally parametrized for room temperature threshold variation. By modification of the trimming procedure to automatically calculate a target threshold trimming based on current threshold variation (as was used for Run 3 of the TID irradiation), a more constant trimmed threshold spread in respect to temperature variation would be expected.

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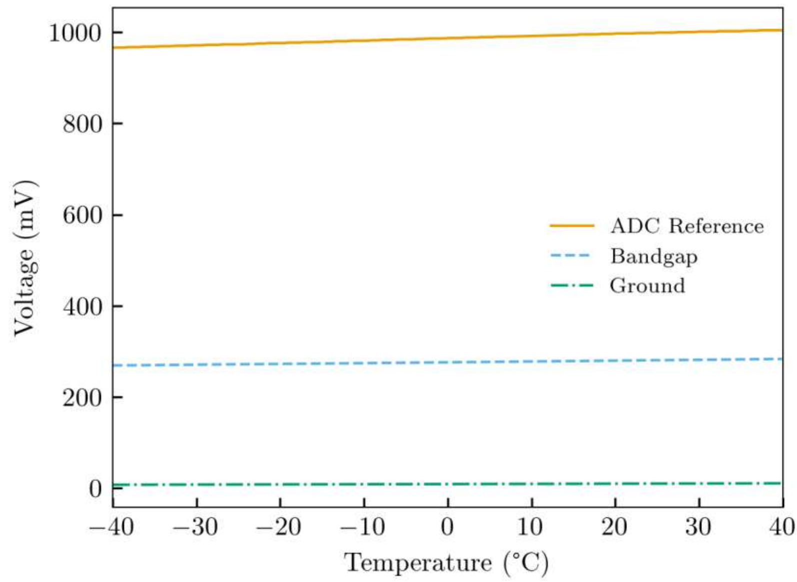

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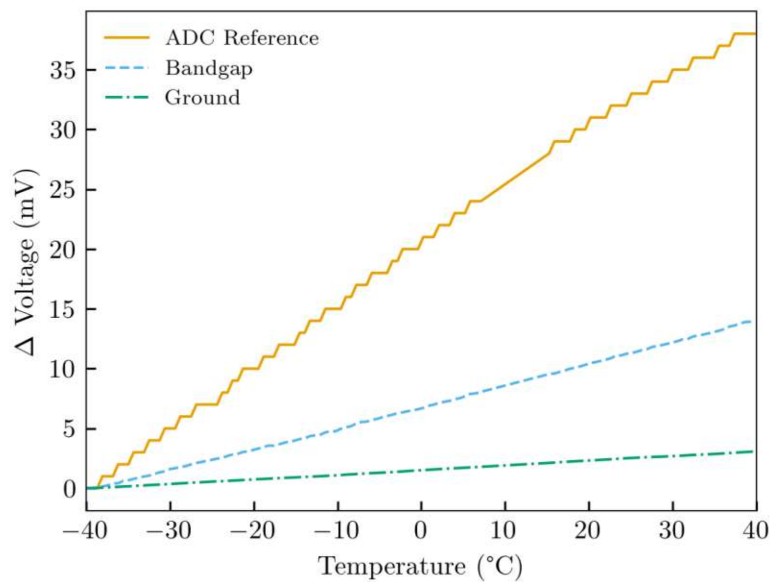

(b)

Figure 6.19: Variation of analog reference voltages in respect to temperature in absolute values (a) and delta values (b). The ground voltage is provided as a comparison to account for an increasing voltage drop incurred by the electrical contact to the chip in rising temperatures.

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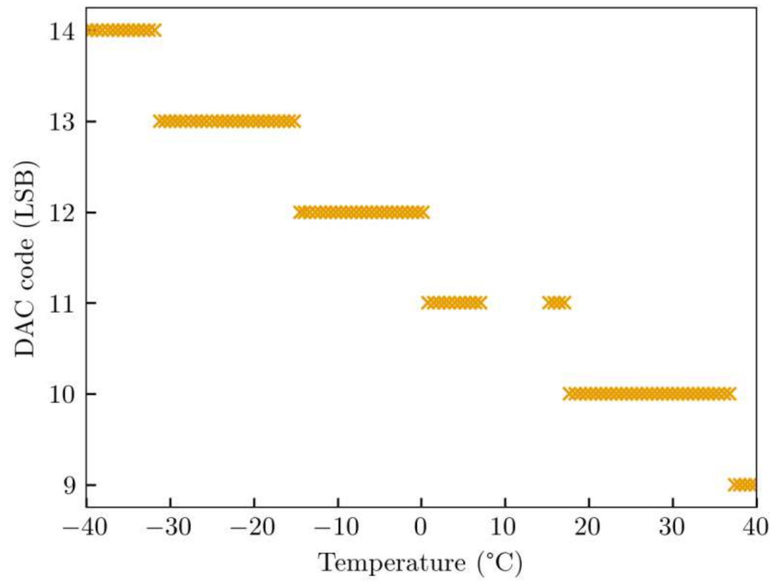

Figure 6.20: DAC input code to maintain a 850 mV reference voltage for the ADC monitoring block in respect to temperature.

6.3.6 Ring Oscillators

Figure 6.22 shows the variation of the RO oscillation count in respect to temperature. The inverter- and delay-based cells exhibit an inverse temperature proportionality compared to each-other. The delay-type oscillators degrade significantly for higher temperatures, while the inverter-type oscillation slightly increase. The increase in the inverter-type RO frequency can be attributed to the usage of high-V_t transistors, which exhibit increased switching speed in higher temperatures. Compared to the behavior seen during TID testing (Figure 6.13), this sensitivity difference should be usable for the concurrent monitoring of TID and temperature independent of each-other during tracker operation of the MPA2.

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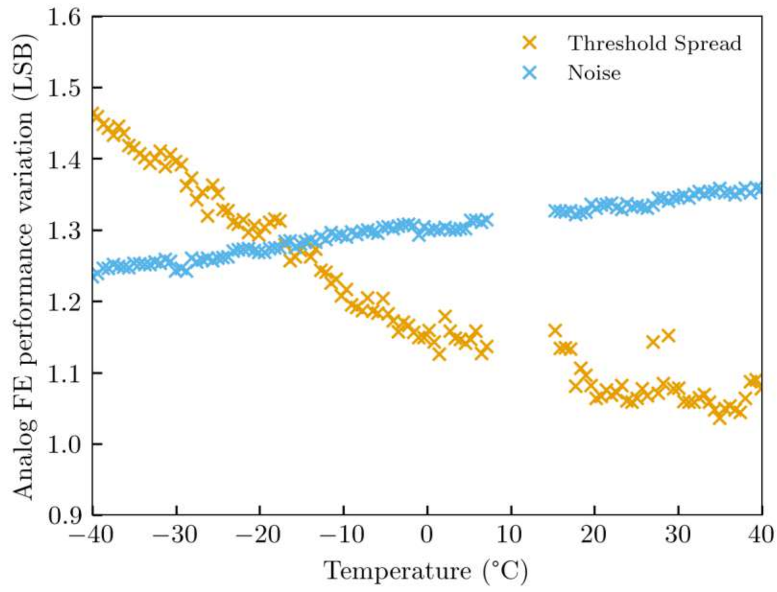
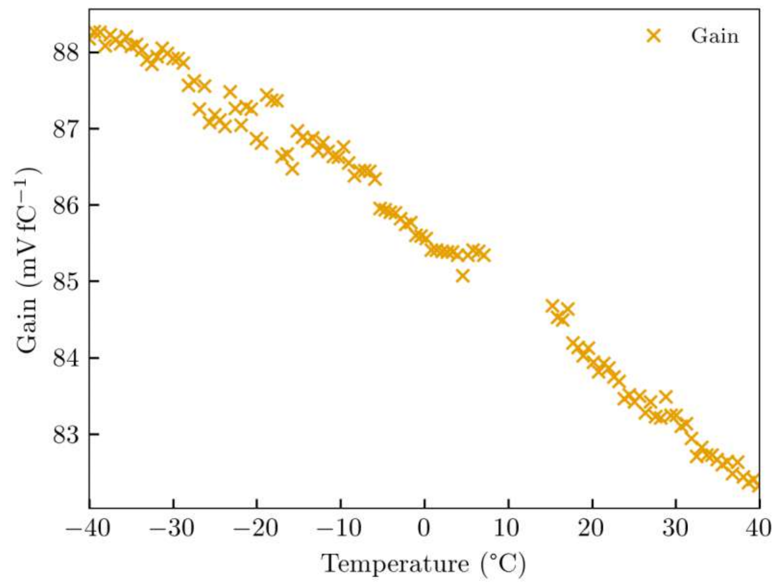


(a)



(b)

Figure 6.21: Variation of average Analog FE Threshold Spread and Noise (a) and Gain (b) in respect to temperature.

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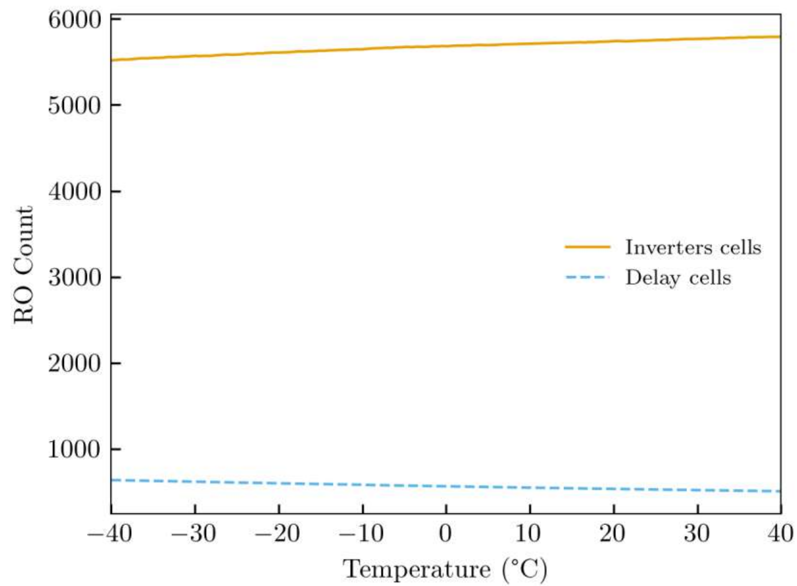
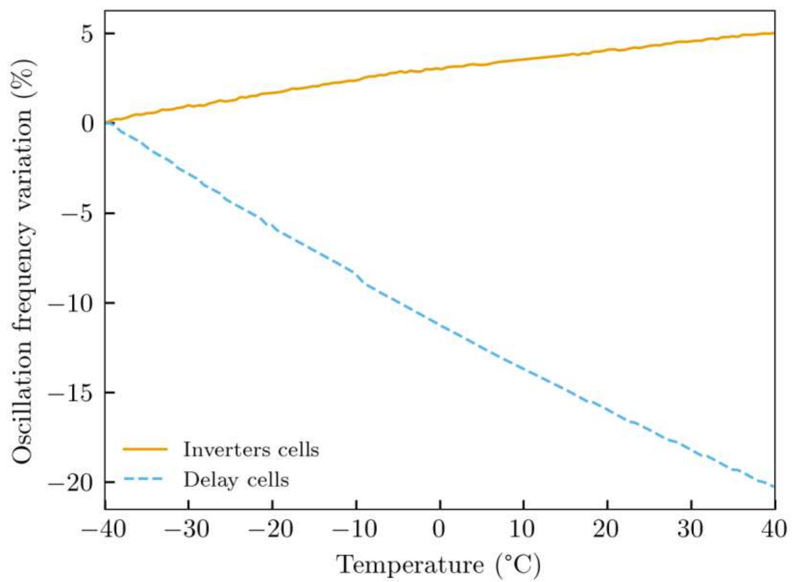


(a)



(b)

Figure 6.22: Ring Oscillator oscillation count for inverter and delay cells in absolute values (a) and relative variation (b) in respect to temperature.

6.3.7 ADC Monitoring

The variability and accuracy of the digital measurement by the internal ADC monitoring in respect to temperature is shown in Figure 6.23. Depicted, are the measured values for the bandgap reference voltage and temperature sensor voltage. For comparison, the bandgap reference voltage measured by the external multimeter is shown in the blue dashed line. Based on simulations, the temperature sensor shows a gain of $-1.4\,\frac{\text{mV}}{^{\circ}\text{C}}$, with an offset that can vary by $\pm 40\,\text{mV}$. Assuming an equal offset, the slope of a simulated temperature sensor is also provided in Figure 6.23 as a yellow dashed line. The ADC temperature measurement follows the expected temperature measurement accurately, with slight exception at the lower and higher ends of the tested temperature range.

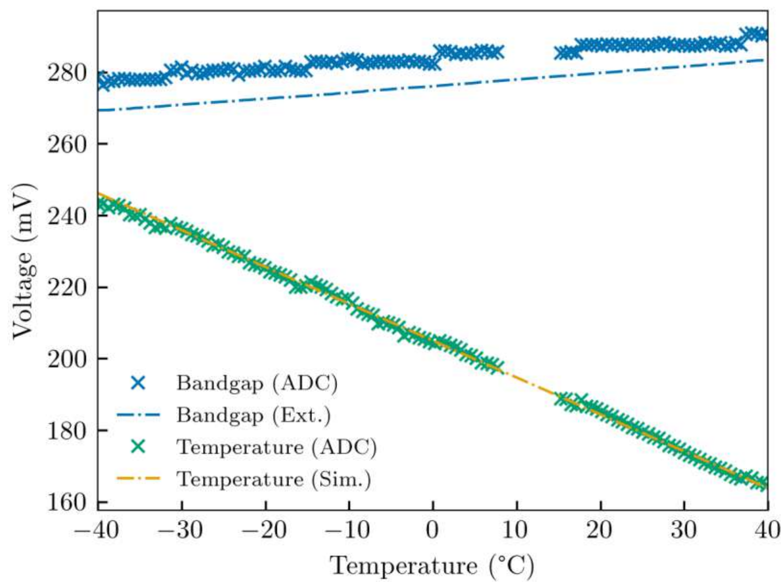


Figure 6.23: Bandgap and temperature sensor voltage measured by the ADC. The externally measured bandgap voltage and simulation-based temperature sensor slope are added for comparison.

An offset is seen for the ADC bandgap measurement that seems to decrease slightly at higher temperatures. This indicates that the ADC measurement degrades in higher temperature due to a decrease in the available current range. Following the course of the ADC measured values, a stepping behavior can be seen. These quantization steps coincide with points in Figure 6.20 where calibration of the ADC Reference DAC shifts the input code to maintain the ADC reference value.

Figure 6.24 shows the ADC measurement of the supply voltages. Not only is there a variable offset between the ADC measured values and actual voltages, but also an increased degradation in the measurement is again seen for higher temperatures.

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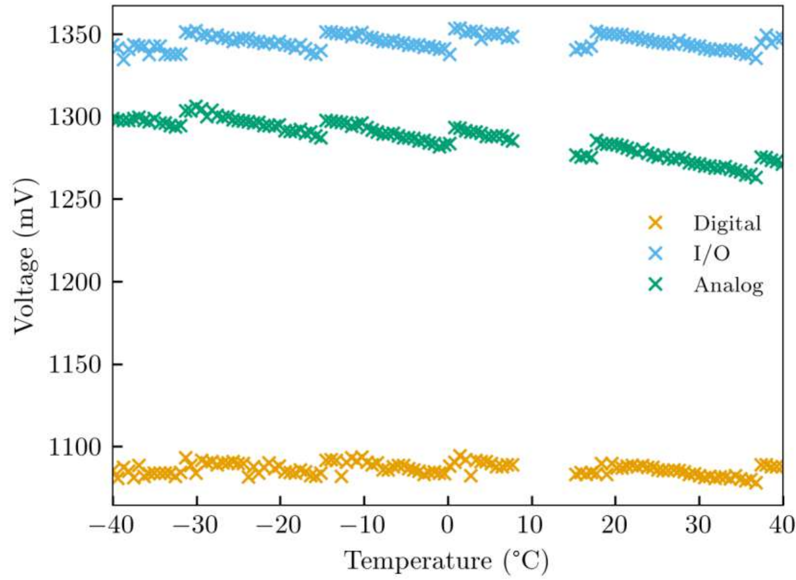

Figure 6.24: ADC measurement of the three supply voltages.

The results indicate that the ADC measurement generally degrades for higher temperatures. As the ADC is intended for monitoring of operating conditions of the MPA2 in the tracker, a calibration procedure would be required that considers chip-individual offset of the ADC measurement and also compensates measurement errors against temperature.

6.3.8 Time-walk

To understand the effect of temperature and the response time of the analog FE in the MPA2, the timewalk was measured according to the procedure outlined in Section 5.2.4. Figure 6.25 shows the timewalk measurement for a single pixel and for four operating temperatures. The measurement itself is somewhat noisy, as the threshold of the pixel was set to below the nominal threshold to show the falling response times against higher charges. As expected, lower pulse amplitudes accrue higher time-walk durations. Exponential curves were roughly fit to the timewalk series measured at each temperature. The trend shows that lower temperatures seem to favor the response time of the analog FE circuits. In all measured temperature scenarios, time-walk remains below the specified 15 ns for a nominal threshold of 0.5 fC.

6.3.9 Additional Remarks

Two MPA2 chips were measured against temperature to account for chip-to-chip variability in its temperature behavior. No large variation between the chips was seen. While the

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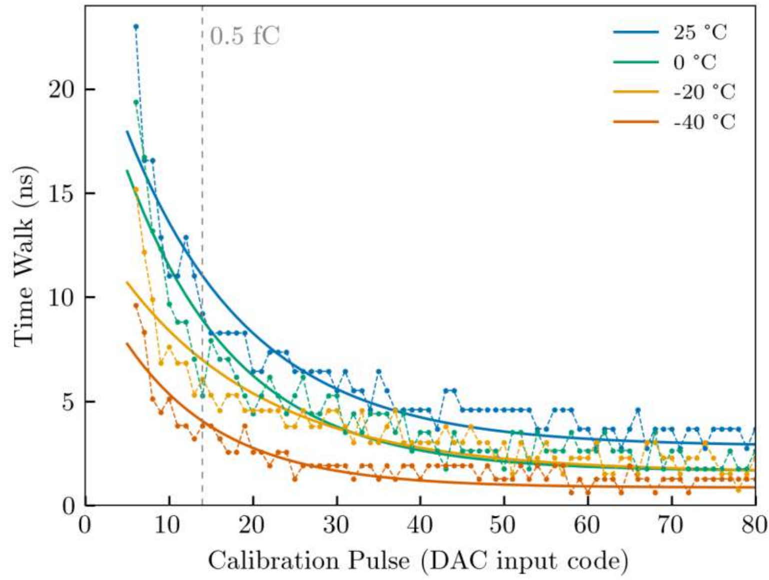

Figure 6.25: Timewalk measurement of a single pixel taken at different temperatures in respect to calibration pulse amplitude. The nominal threshold is marked by the dashed grey vertical line. The threshold of the pixel was set to 80 $\mathrm{LSB_{ThDAC}}$ (untrimmed).

quality of the ADC measurement is temperature-dependent (and also TID-dependent as shown in Section 6.2), the two ADC measurements of the two chips behave similarly. This is positive result, as a calibration procedure devised to correct the offset and temperature-dependent error in the ADC measurement will be necessary for its utilization in tracker monitoring tasks. This calibration procedure should be equally applicable for all MPA2s deployed to the tracker.

6.4 Additional Measurements

6.4.1 Dynamic Power Consumption

All power measurements shown thus far in the thesis were made with the MPA2 in a static state. An initial dynamic power consumption study by injection of pixel hits to stimulate the digital hit processing logic of the MPA2 is shown in Figure 6.26. Pixel hits are injected every two BX by the fast injection routine and the measurement was repeated for various digital supply voltages. The digital consumption increases linearly with increasing pixel centroids injected, with hits spread across the chip rows. At 8 injected centroids, the consumption saturates due to the stub centroid priority encoding selecting only 8 centroids to be further processed. For the nominal DVDD of 1 V, the

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maximum increase in the dynamic power consumption for the digital domain is around 12 mW. The analog and I/O power domains are independent of the pixel hit activity.

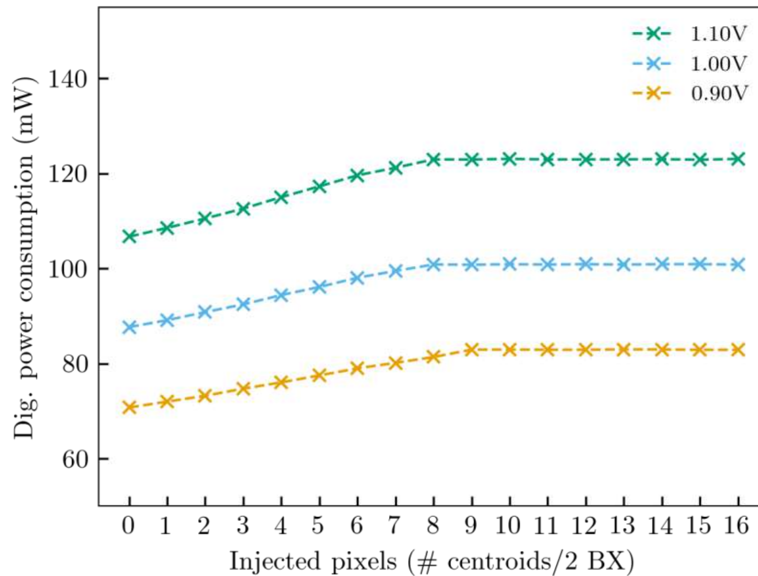

Figure 6.26: Digital power consumption in respect to injected pixels for multiple DVDD levels. The MPA2 is set to pixel-pixel processing mode and the L1 trigger rate is 1 MHz.

This test was done in pixel-pixel mode and with no L1 triggers sent. As such, the coincidence logic and the L1 data path are not fully stimulated. As the stub hit processing logic and transmission consume a majority of the digital power budget based on the 40 MHz operating frequency, this test can still be taken as an indication that the MPA2 power consumption will remain below its 200 mW power budget also for high PU scenarios.

6.4.2 Row BIST Voltage Scan

The Row BIST was characterized in respect to the digital supply voltage to explore its minimum required operating voltage. According to simulation results, the minimum digital voltage supplied should be at least 810 mV[39]. As shown in Figure 6.27, the Row BISTs are successful for a DVDD voltage down to 810 mV in all cases. The first Row BISTs start to fail around 800 mV. Also visible, is that the individual BISTs stop functioning at varying voltage levels, with BISTs of higher indexed rows failing closer to the minimum operating voltage. This is explained by the greater physical distance of higher index rows to the periphery block, as they incur higher voltage drops compared to pixel rows closer to the periphery. While this result is not directly applicable for the operation of the MPA2 in the tracker, it indicates that the digital functionalities of

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the chip should be able to function at supply voltages close to the minimum voltages suggested by simulation.

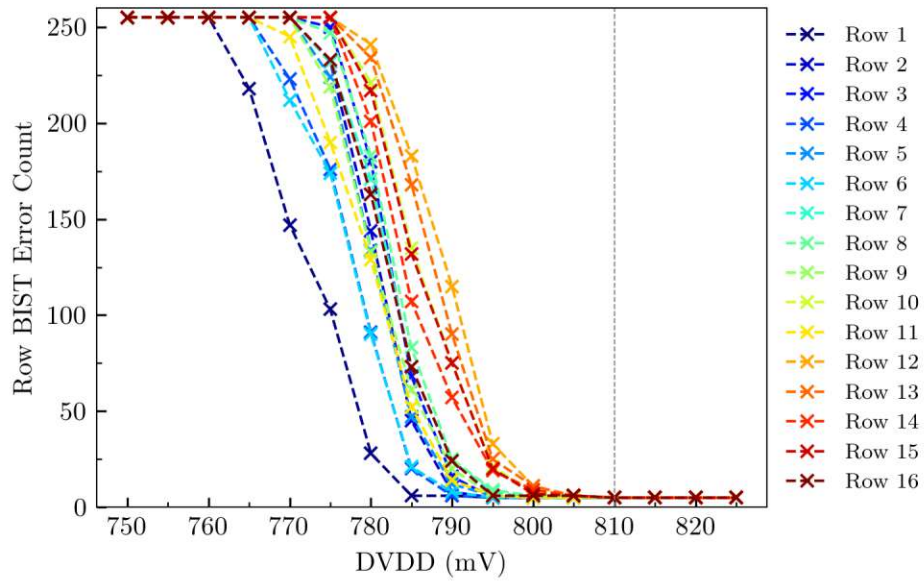

Figure 6.27: Row BIST error count in respect to digital voltage for each row. The Row BISTs were designed according to a specified minimum operating voltage of 810 mV (grey vertical dashed line).

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7 Conclusions

The aim of this thesis was to perform the bare-die characterization of the readiness of the MPA2 chip for its operation in the CMS Outer Tracker. Within this scope, functional test routines were devised to confirm and characterize the wide array of the chip functionalities. The full functionality was tested at the wafer-level for over 3500 chips. The resulting wafer probing data was then analysed to formulate preliminary criteria for a yield assessment accounting for chip-to-chip variation. The developed test procedures and the results presented in this thesis will be drawn upon in view of large scale production testing at an external test house.

Subsequently, single-chip carrier-board based testing allowed to run extensive studies to verify if the MPA2 fulfilled stringent power and radiation-tolerance requirements which have informed the chip implementation.

Based on a heavy ion irradiation campaign, the control logic of the MPA2 was found to be robust toward SEUs, while data sensitivity towards SEU was measured and error rates were estimated to be within acceptable ranges. X-ray irradiation was performed to simulate the chip operation for radiation doses expected for its long-term operation in the HL-LHC. The MPA2 was found to stay operational for TID levels of up to 200 Mrad while staying within the allowed power budget margin.

Through the conducted temperature characterization, it was shown that the MPA2 is robust toward potential changes in its final operating temperature in the tracker. In combination with the TID characterization, the variability of the performance degradation in the chip was measured and found to be within the expected margins.

Based on the tests and characterizations presented, the MPA2 is considered fully characterized for nominal operating conditions in the tracker. Additional testing of the single MPA2 is planned to study its behavior in certain edge cases, such as deviation of nominal supply voltages, L1 data packet management or dynamic power consumption in high PU scenarios. The ADC monitoring block characterization is also on-going, in an effort to formulate a calibration procedure, which can adequately compensate measurement errors against variation of radiation dose and temperature in the tracker.

Further testing of the MPA2 and its integration with the other components of the PS module is planned. As such, the acquired testing data serves as an initial baseline for the MPA2 in the testing of the sub- and fully assembled PS modules in face of the commissioning effort for the CMS Phase-2 tracker upgrade in the next years.

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Glossary

ALICE	A Large Ion Collider Experiment.
ASIC	Application Specific Integrated Circuits.
ATLAS	A Toroidal LHC Apparatus.
ATPG	Automatic Test Pattern Generation.
BIST	Built-in Self-Test.
BR	binary read-out.
BSM	Beyond Standard Model.
BX	Bunch Crossing.
CMOS	Complementary Metal-Oxide Semiconductor.
CMS	Compact Muon Solenoid.
CSA	charge sensitive amplifier.
DAQ	data acquisition.
DFT	Design for Testability.
FE	Front-End.
FMC	FPGA Mezzanine Cards.
FPGA	Field Programmable Gate Array.
HEP	high energy physics.
HL-LHC	High-Luminosity at LHC.
HLT	High Level Trigger.
L1	Level 1 Trigger.
LHC	Large Hadron Collider.
LHCb	Large Hadron Collider beauty.
MPA	Macro-Pixel ASIC.
PTS	Punch-through-Structures.
PVT	process, voltage, temperature.
SEU	Single-Event Upset.

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SM	Standard Model.
SSA	Short-Strip ASIC.

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