Built-in Self-Test Based Phase Noise Measurement

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Marija Ćulibrk

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Kurzfassung

Da die integrierten Schaltkreise immer kleiner werden, wird die Durchführung von Tests immer mehr zu einer aufwendigen, zeitintensiven und kostspieligen Aufgabe. Das Testen erfolgt in verschiedenen Phasen des Lebenszyklus des Geräts, um dessen ordnungsgemäße Funktionsfähigkeit zu gewährleisten und sicherzustellen, dass die vom Kunden festgelegten Vorgaben erfüllt werden können. Eingebaute Selbsttests sind ein probates technisches Mittel, die durch die Ausstattung des integrierten Schaltkreises mit zusätzlicher Hardware ermöglichen, dass der eigene Betrieb regelmäßig selbst getestet wird. Durch den Einsatz solcher Tests lassen sich die Testkosten beträchtlich senken, da der Bedarf an automatisierten Testgeräten entfällt und die Testzeit zudem erheblich verkürzt wird.

Ein Phasenregelkreis ist ein Regelsystem mit negativer Rückkopplung, das häufig in Hochfrequenzsendern und Empfangsgeräten, die aus einem festen Niederfrequenzsignal ein stabiles, in der Regel hohes, Ausgangsfrequenzsignal generieren, verwendet wird. Es gibt verschiedene Leistungsparameter, die geprüft werden müssen, um die ordnungsgemäße Funktionsweise sicherzustellen, darunter das Phasenrauschen. Ein hoher Beitrag des Phasenrauschens wirkt sich negativ auf die Gesamtleistung eines Phasenregelkreises aus, da es unerwünschte Schwankungen in der Phase des Ausgangssignals verursacht. Zu den unerwünschten Effekten, die durch Phasenrauschen verursacht werden, gehören gegenseitige Vermischung, Erhöhung der Bitfehlerrate und Kanalstörungen. Daher ist die Modellierung des Phasenrauschens in Phasenregelschleifen bei der Entwicklung von Hochfrequenzsystemen von entscheidender Bedeutung. Mit Hilfe von Tests kann

sichergestellt werden, dass das Phasenrauschen innerhalb der Spezifikationswerte bleibt. Herkömmliche Methoden zum Testen des Phasenrauschens sind jedoch suboptimal, so dass eine Marktlücke für neue und von modernen Herangehensweisen geprägten Testmethoden vorliegt.

Ziel dieser Arbeit war es, das Phasenrauschen zu modellieren und festzustellen, ob ein eingebauter Selbsttest zur Erleichterung der Testbarkeit eines solchen Bauteils verwendet werden kann. Die Ergebnisse wurden durch die Simulation des Phasenrauschens mit einem MATLAB-Modell erzielt. Zuerst wurde, das Phasenrauschen vor und nach dem spannungsgesteuerten Oszillator modelliert und die Ergebnisse für verschiedene Frequenzbereiche miteinander verglichen. Nach einer Analyse der im Rahmen dieser Arbeit erstellten Diagramme ließ sich feststellen, welche Rauschbeiträge in welchem Frequenzbereich dominant waren. Um möglichst zuverlässige Ergebnisse erzielen zu können, wurde außerdem ermittelt, welche Parameter die Funktionalität einer solchen Messung einschränken könnten und welche Komponenten hinzugefügt oder entfernt werden sollten. Vorgeschlagene Werte für diese Parameter sowie die entsprechenden Berechnungen wurden ebenfalls im Rahmen dieser Arbeit thematisiert. Des Weiteren zeigt sich in dieser Arbeit, dass nicht alle Informationen durch eine solche Messung erfasst werden können, einige gehen dauerhaft verloren. In der Schlussfolgerung dieser Arbeit wurde näher dargelegt, welche Störquellen im Rahmen einer solchen Testmethode ausfindig gemacht werden könnten und welche konkreten Informationen verloren gehen würden.

Abstract

As integrated circuits are becoming smaller and smaller, testing them has become a more tedious, time consuming and costly task. Testing occurs throughout various stages of the device life-cycle, guaranteeing its proper functioning and ensuring it meets certain specifications determined by the customer. Built-in self-tests are a design for testability technique which includes additional hardware on the integrated circuit, allowing it to periodically test its own operation. The use of such tests considerably reduces the testing cost since the need for automated test equipment is eliminated and additionally significantly improves the test time.

A phase lock loop is a negative feedback control system which is frequently included in high-frequency transmitters and receivers generating a stable, usually high, output frequency signal from a fixed low frequency signal. There are several different performance parameters which must be tested to ensure proper functionality, one of these being the phase noise. Phase noise negatively effects the overall performance of a phase lock loop by causing undesired variations in the phase of the output signal. Some undesired effects caused by phase noise include reciprocal mixing, increase bit error rate and channel interference. Therefore, modeling the phase noise in phase lock loops is critical when designing radio frequency systems. Testing helps to ensure that the phase noise remains within the specification values. However, conventional methods for testing phase noise are suboptimal, since the parameters which are currently being used are not always accurate predictors of performance, causing an opening in the market for new testing techniques

using modern approaches.

The objective of the thesis was to model the phase noise and to determine if a built-in self-test could be introduced to ease the testability of such a component. The results were obtained via simulating the phase noise via a MATLAB model. In the first step, the phase noise was modeled before and after the voltage controlled oscillator and compared for different frequency ranges. From these plots it was possible to determine which noise contributions are dominant in which frequency range. Additionally, it was determined which parameters could limit the functionality of such a measurement system and what components should be added or removed to ensure the most reliable results. Suggested values for these parameters, as well as their respective calculations, are provided in this thesis. Furthermore, it was shown that not all information can be retained via such a measurement, some would be permanently lost. The conclusion provided in this work states which noise contributors would be visible via such a measurement and which exact information would be lost.

Contents

CHAPTER 1

Introduction

1.1 Motivation

The economics of electronics manufacturing require that Integrated circuits (ICs) be of very high quality before they are soldered onto circuit boards or into multichip modules. In such a situation, functional testing alone is inadequate. The manufacturer therefore wishes to be able to trim devices for performance or filter them out once they fail a test. Full functionality of the ICs is extremely important. The manufacturer must ensure, with a high degree of confidence, that the devices are working properly. However, the ever decreasing size of chips poses a vital threat. This reduction in size increases the probability of manufacturing defects. Detecting these defects is crucial since even a single failure can cause a large deviation from the expected performance. As traditional test approaches are becoming more difficult and less reliable, new techniques need to be proposed to keep up with the constant demand.

Built-In self-test (BIST) is a technique of Design for testability (DfT) which are designs that eliminate the need for expensive external test equipment and can reduce the testing time considerably. Generally speaking, a DfT technique needs to be considered at an early stage in the design process. The hardware added to the chip to perform the

self-testing could impact the operation of the device [1]. These types of test are extremely convenient. By introducing testing hardware in the design phase of ICs production, ICs can perform self-testing. However, some of these performance tests are not that trivial to build. One such performance test is Phase lock loop (PLL) phase noise.

PLLs are electronic circuits which generate an output signal whose phase is related to the phase of an input signal, called the 'reference signal'. They are generally used in many Radio frequency (RF) or wireless applications. In fact, PLL synthesizers are one of the main building blocks found in wireless transcievers used to convert RF band signals to baseband signals and vice versa. It is not a singular component, rather a block of multiple components in a closed loop system which locks the output phase to the phase of the input reference signal, giving the name phase lock loop. The major advantage is that they are stable, programmable and convenient to use. However, PLLs are highly sensitive to parametric deviations and process defects which can cause them to malfunction, this is why testing them is essential [1]. With this said, testing PLLs is rather complex since it requires high measurement precision and access to the external nodes. This leads to high test costs and increased test time.

Phase noise is one of the key performance parameters in PLLs. For proper functionality, it is crucial that the phase noise is minimal and falls within the specification range. Each of the individual components in the feedback system contributes to the overall phase noise at the output. The impact of the noise from any one element in the loop is dependent on its position in the system and therefore each contributes differently towards the output. If the noise does not comply to the requirements, the performance might be compromised and failures can occur. Phase noise is considerably impacted by process, voltage and temperature variations. It is therefore of great importance to measure phase noise during Wafer test (WT) and Final test (FT). During validation, one is able to use expensive and accurate spectrum analyzers on IO pins, but this cannot be done during FT. Currently, during FT, devices are filtered for noise performance by measuring Direct current (DC) parameters that strongly correlate with PLL phase

noise (parameters such as the gain of the oscillator K_{VCO} and charge pump current). These parameters vary with process and temperature. Information regarding these parameters is already collected, making it easy and fast to verify. However, sometimes it is not possible to identify the correlation of the noise to these parameters since they are not always accurate predictors of performance, especially on higher Complementary metal-oxide-semiconductor (CMOS) nodes. In the Ultra-wideband (UWB) project, they make use of PLL phase noise measurements during FT which requires an external RF source.

It is the target of this master's thesis to investigate possible alternatives that would rely fully on internal input and output signals. A BIST is proposed to remove all external cables and interaction with external testing equipment.

The BIST does not need the external RF tone, but instead would rely on capturing the PLL V_{tune} during locking (tunes linear part of oscillator and corrects for frequency and phase). The V_{tune} is the Voltage controlled oscillator (VCO)'s control voltage. The captured V_{tune} time domain signal would be sent via a buffer and then to an Analog to digital converter (ADC). The captured data would be used for later post processing. The task of the thesis is to identify the limitations of this phase noise measurement and to propose adequate solutions for the case when the performance is compromised.

1.2 Research Questions

The objective of the project is to identify the limitations of the phase noise measurement (i.e. weak signal, Low noise amplifier (LNA) gain, analog test bus bandwidth, ADC specifications) and to try and find solutions (i.e. resolution improvements, low noise amplifier, high pass filter). The following research questions are discussed in more detail throughout this thesis:

- R1: Use the PLL model to produce the noise spectrum before and after the VCO

- R2: Theoretically, would the V_{tune} noise measurement be able to capture output noise or would we miss contributors which would impact the measurement itself?
- R3: Which parameters (non-idealities) would limit the accuracy of such a noise measurement?
- R4: How would parameters such as the analog test bus bandwidth, LNA/ADC specifications, which are necessary for a satisfactory measurement (provided some boundary conditions), influence the calculations?

1.3 Approach

The approach used to solve the research questions would be to simulate the phase noise via a MATLAB model. To begin with, the resulting noise towards the output/input of the VCO needs to be calculated via the corresponding transfer functions. These transfer functions must be added to the model to plot the phase noise spectrum. Once this is achieved, the spectral plots at the VCO input and output need to be compared. The goal of the thesis is to create a BIST which senses at the input of the VCO and to conclude if there is the possibility to get representative information concerning the phase noise at the output of the PLL. The frequency is divided up into different ranges (low, mid and high) to see which noise contributions are dominant in which frequency range. According to the VCO input, it is possible to draw conclusions about the noise at the output.

Afterwards, the noise from the ADC and LNA need to be considered. Their corresponding noise contributions should not overpower the phase noise measurement, otherwise it would defeat the purpose of the BIST. It will be shown that a high pass filter needs to be added to the setup. Modeling how this high pass filter effects the noise spectrum is also a necessary step. Other specifications for the LNA and ADC need to be taken into account, such as the gain of the amplifier and the number of bits of the converter. Once all the results are added to the model, it is necessary to conclude if such a measurement makes sense. Would the V_{tune} noise measurement really be able

to capture the phase noise at the output? Does the measurement get drowned out by the other noise contributors in the setup? What are the necessary specifications of the components for an satisfactory measurement? These are all questions which need to be answered throughout the thesis.

1.4 Structure

This thesis is split up into five chapters. After the introduction, chapter 2 provides a basic overview of the main topics which are presented in the thesis. The main information regarding the PLL structure and its basic operation is given. Each block component and its functionality is described in detail. Additionally, information concerning BIST and phase noise is thoroughly explained. Chapter 3 presents the necessary equations/formulas which are used in the MATLAB model. The transfer functions which are necessary to calculate the noise from the individual noise sources towards the output are introduced. Also, there is a detailed analysis on the LNA/ADC parameters such as gain, input referred noise, quantization noise, noise power spectral density, etc. Next, chapter 4 introduces the results in which the equations from chapter 3 were used to extend the MATLAB model. The phase noise spectral plots are discussed in detail and various conclusions are drawn based on them. Lastly, in chapter 5 the main conclusion is given. It also provides suggestions for future work.

CHAPTER 2

Background

2.1 Built-In Self-Tests

In the past, testing electronic circuits was an extremely time consuming and costly task. As ICs started becoming smaller and smaller, following Moore's law (which states that the number of transistors in a dense ICs doubles about every two years), testing became a more cumbersome task. Testing the functionality of electronic devices is necessary for detecting component failures when device specifications are not met. These defects can result in undesired functioning of the circuit and should be screened out during the testing process. Testing is performed at various stages during the life-cycle design. WT and FT are two steps which are used in semiconductor device fabrication. A WT is the first step in the process and it is carried out on production level. It is done to make sure that no damage was inflicted on the material during fabrication. This type of test is done via the help of Automated test equipment (ATE). ATE is computer-controlled equipment which uses automation to test devices for performance and capabilities. The goal of ATE is to quickly perform the necessary measurements and conclude whether the device is functioning properly. The second type of test, FT, is a type of board level testing, it is done once the device packaging is completed. It screens out any chips which

were damaged during the packaging processes and gauges the performance of each device. Additionally, the ICs are tested depending on their expected use. The manufacturer must ensure that the devices meet certain specifications and that the performance is up to par with the consumers expectations. For example, chips which are going to be used in a high temperature environment will be tested by exposing the device to elevated temperatures for a certain period of time. In figure 2.1, the testing life cycle is shown. Design verification looks for design errors, correcting these errors occurs prior to fabrication. The remaining tests target manufacturing defects, these need to be screened out before being sent to the customer [2].

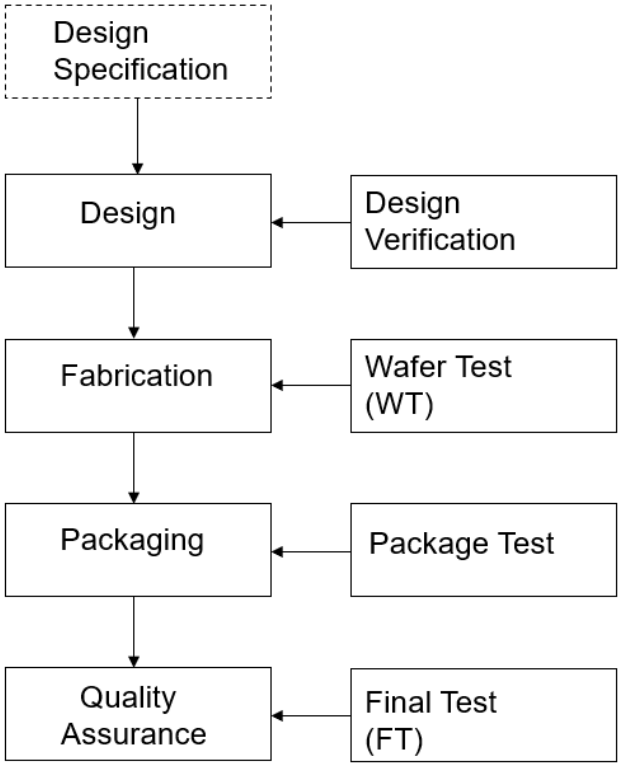


Figure 2.1: Testing life cycle of ICs [2]

Even only preparing the ICs for proper testing is an inconvenient task since a lot of hardware needs to be added to the chip to ensure suitable testability. This task has

only proven to be more complex with the ever decreasing size of the circuits. Special design techniques have to be introduced to make a chip fully testable. DfT is the field which focuses on finding an efficient way to test the circuits and decide which additional hardware must be added to improve the testability. A focal point is improving the observability and controllablity of the internal nodes such that they can be easily accessed. For the best results, testing must be considered at an earlier point in the design process to make the design as efficient as possible. Furthermore, the role of DfT should be used as a mean to fully replace traditional functional tests.

BIST is one of the testing techniques proposed by DfT. The basic idea is that a small testing circuit is integrated inside the ICs which allows them to perform self testing. It is able to test its own operation for functionality, parametrics, etc. Since the test circuitry resides within the circuit under test, BIST can be used at all levels of testing, such as WT or FT, which is what makes it extremely convenient. Its main advantage is that it can significantly lower the cost of testing, since it does not rely on the expensive external test equipment, such as ATE. BIST are particularly useful for those blocks in the ICs which have no direct connection with external pins since traditional test equipment could not be used in such a scenario.

In what follows, the general functionality of a PLL will be described. Even though the basic principle is fairly simple, there is a vast range of specifications that are crucial to the stability and performance of the PLL that need to be thoroughly tested. One of these parameters is phase noise. Combining the BIST technology into the PLL is a major step forward when it comes to testing its functionality. The task itself is not simple, some of the challenges include:

- ensuring that the additional test hardware causes minimum to no impact to the PLL functionality
- contributing minimally to power consumption

- taking up minimal area on the chip
- fault detection can be caught either with direct or indirect measurement of key specification values [3].

Figure 2.2 illustrates the BIST strategy proposed for the PLL. It should measure the phase noise found at the V_{tune} and based on that, draw conclusions about the noise at the output. This would ensure that the phase noise specifications for the PLL are met.

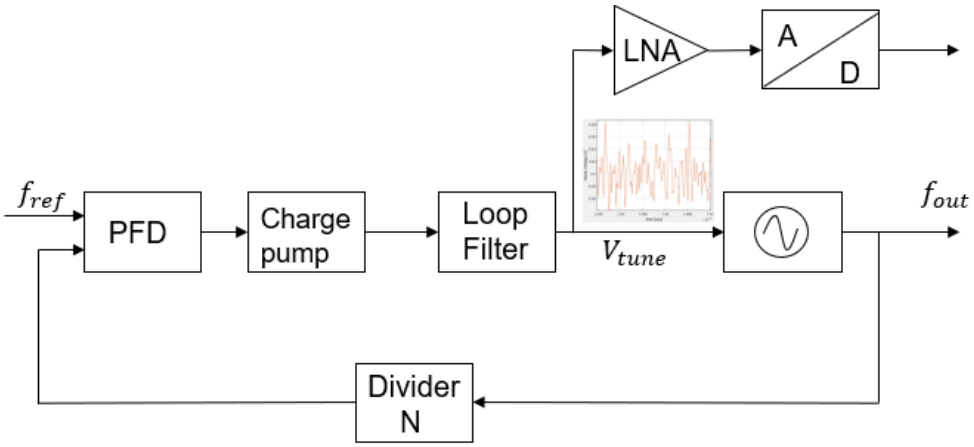


Figure 2.2: BIST strategy for PLL to measure phase noise

2.2 Phase Lock Loop

A PLL is an electronic circuit which is frequently used in communication systems. One of the most common applications of PLLs is as frequency synthesizers, where they are used to generate a range of frequencies from a single reference frequency. This is often done by placing a frequency divider between the VCO and the phase frequency detector. These types of synthesizers are known as indirect frequency synthesizers. However, a basic PLL has various other applications, such as carrier/clock recovery, modulation/demodulation of frequency as well as phase and filter tuning.

A PLL is a negative feedback loop that locks the output of the oscillator to the

reference input. Phase is an important concept to grasp when considering PLLs. Taking the same point on two different wave forms and looking at the angle between them yields the phase difference. When this difference changes, the wave forms are on different frequencies. When the phase difference remains constant, the frequencies are equal. This concept is crucial to the functioning of PLLs.

The PLL causes the phase difference between its input and output signal to become constant. In this way it produces a signal on exactly the same frequency as a 'clean' crystal oscillator. This operation is immensely useful in various applications.

The PLL operates in one of the following three modes:

- Free running mode: when there is no input signal applied to the PLL it operates in this mode.
- Capture mode: as soon as some input is applied, the output at the VCO frequency will begin to change, producing an output frequency used for comparison.
- Lock mode: the VCO frequency continuously changes until the output signal frequency is the same as the input signal frequency, then the PLL is said to be in 'lock'. The loop tracks any change in the input frequency through its repetitive feedback action. Mathematically this can be written as:

$$\phi_{out}(t) - \phi_{in}(t) = constant \tag{2.1}$$

and hence

$$\frac{d\phi_{out}(t)}{dt} = \frac{d\phi_{in}(t)}{dt} \tag{2.2}$$

Figure 2.3 shows the basic components found in a (type-II) PLL. In a type-II PLL there are two integrators. Each of these building blocks and their functionality will be described in this chapter.

The general principle is explained as follows. The Phase frequency detector (PFD) compares the input frequency f_{ref} to the feedback divided frequency f_{div}. The output of the detector generates an error signal which is the difference between the phases of the two input signals. The output error is then sent to a Charge pump (CP) which produces current that loads/empties the capacitors of the Loop filter (LF) accordingly. The primary purpose of the LF is to convert the current spikes stemming from the CP into voltage. Its secondary task is to suppress the high frequency noise component, leaving only the DC voltage behind. The high frequency noise results from the additional summation of f_{ref} and f_{div} at the phase detector output, as opposed to just the subtraction representing the phase difference between the two signals, which is the desired component. The DC V_{tune} is the control voltage of the VCO, this filtered signal is then applied to the VCO as the tuning voltage. The voltage at the VCO input is directly proportional to the output frequency f_{out}. The signal f_{out} is then sent to a divider to produce f_{div}. This process is then repeated until the input and feedback divided frequency are equal and the PLL is in phase lock mode. When this occurs, a steady state error voltage is produced. Since the error is constant the phase difference of the two signals does not change, from this it is concluded that the two signals are on exactly the same frequency. The loop then tracks any change in the input frequency through its feedback path.

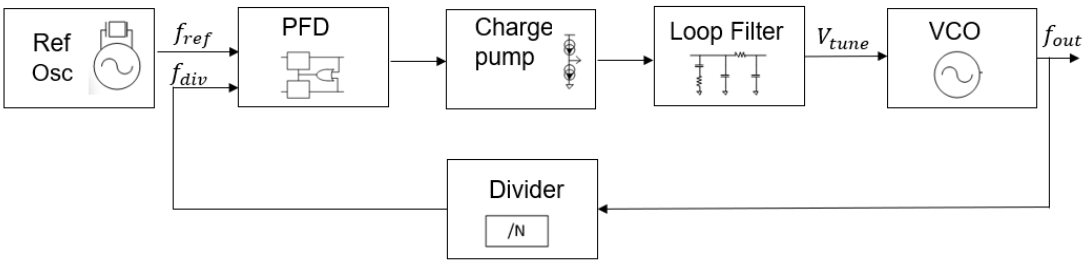


Figure 2.3: PLL block diagram

2.2.1 Phase Frequency Detector

The PFD is used to compare the phase of the reference signal (the crystal oscillator) to the phase of the feedback signal (coming from the divider). It generates an output error

according to the phase difference. The error phase goes through the gain of the PFD K_D, to convert the phase difference to a series of pulses which is proportional to the error. The error voltage is calculated via the following equation:

$$v_e(t) = K_D(\phi_{div}(t) - \phi_{ref}(t)) \tag{2.3}$$

The functionality of the PFD is explained in [4] via a state machine diagram which is depicted in figure 2.4. The output of the PFD can only have three states *up*, *down or zero*. If the rising edge of the reference is leading that of the divider output (coming from the VCO), it produces 'up' pulses which causes more current to be injected into the loop filter. As a result, the loop filter output voltage increases and therefore also the VCO output frequency and phase. Similarly, if the divider output is leading the reference, it will generate 'down' pulses, which causes current to be drawn out of the capacitor resulting in a voltage drop [4].

Basically, a pulse is created which indicates if the oscillator signal needs to catch up with the reference signal or if it is going too fast and needs to slow down. In doing so, it adjusts the voltage of the VCO such that output frequency has a known phase relationship with the input signal.

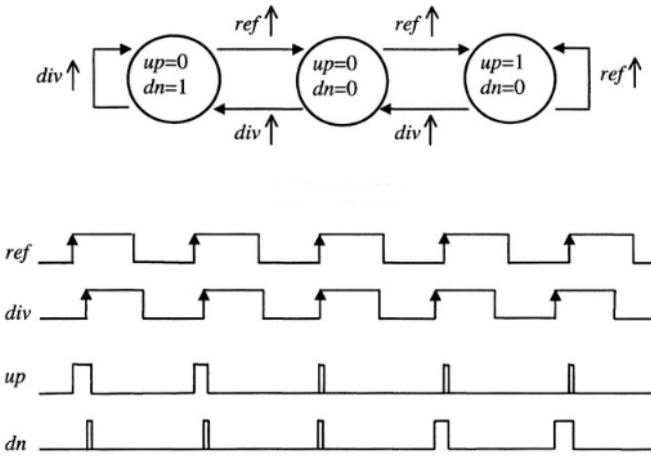


Figure 2.4: Functionality of PFD explained with state machine and signal waveforms [4]

There are different types of phase detectors. The type typically used in frequency synthesizers is a tri-state PFD depicted in figure 2.5. It is constructed by using 2 D-type flip flops, an AND logic gate and a delay. The inputs of the PFD, ref and div, serve as clocks for the flip flops. Both data inputs, D, are always held high. One Q output enables a positive current source, the 'up' signal, while the other Q output enables a negative current source, the 'down' signal. Both outputs are used in conjunction with an AND gate and the delay to reset the two flip flops. The idea is that the flip flops are triggered by a rising edge of either ref or div. Analogously to figure 2.4, a rising edge of ref causes the flip flop output signal 'up' to go to the high state. Likewise, a rising edge on div, will cause the 'down' signal to go to the high state as well. If both inputs of the AND gate are high, the reset signal goes to 'high' and both flip flops are reset, i.e. their 'up' and 'down' signals are brought to back to the low state.

The additional delay element is there to ensure that the so called 'dead zone' effect does not occur. This effect happens if there is very little phase difference between the signals, meaning that the pulses are very narrow, resulting in pulses that are too short for the CP to react to. This implies that the switches on the CP do not turn off and on, causing the current at the output to remain zero. This indicates that there exists some region near the zero phase error at the input of the PFD for which the PLL does not appropriately correct for. Thus, the error becomes so low that the PLL does not correct for small phase errors [4]. One way to overcome this is to make sure the pulses are either in an up or $down$ state long enough to turn on the switches of the CP, this minimum time period is referred to as t_{min}. Such an action is achievable with the addition of the delay component in the phase detector reset path which causes the reset pulse to be delayed, forcing a minimum pulse length.

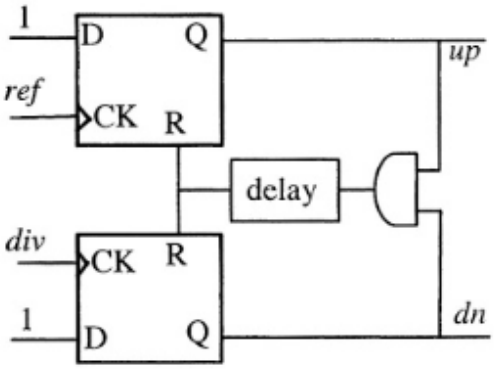


Figure 2.5: Tri-state PFD [4]

2.2.2 Charge Pump

In its most basic form, the PLL only constists of three main components: the PFD, the LF and the VCO. The charge-pump PLL is an extension of the basic PLL. A CP can be integrated into the circuit between the PFD and LF. This type of PLL is considered in the thesis. The PFD in conjunction with the CP is used to simplify the interfacing to the LF.

The CP is responsible for converting the series of pulses, which are proportional to the phase error at the PFD output, to positive and negative current pulses. It is used as a mean to sink or source current for a limited period of time. It takes as an input the *up* and *down* pulses and converts them into current pulses which then directly change the voltage drop V_{tune} on the LF impedances.

In figure 2.6 a schematic of the CP is shown. It consists of two switched current sources which are driven by the PFD. One of the sources is connected to the positive supply while the other is connected to the negative supply. In between the current sources there are 2 switches. It is important to note that the switches are never on at the same time. Depending on whether the PFD is sending 'up' and 'down' pulses, it will turn on S_1 (switch for 'up') or S_2 (switch for 'down') accordingly. For the case when 'up' is high, S_1 is on and S_2 off, causing current from I_1 to flow out of the CP and into the LF,

charging the capacitor C_1 [5]. On the other hand, when 'down' is high, then S_2 is on and S_1 is switched off, resulting in current flowing out of the LF and into the CP [6].

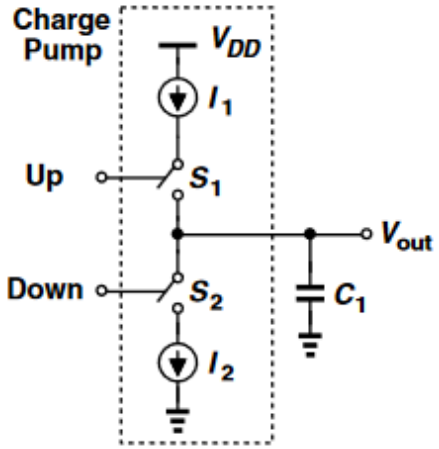


Figure 2.6: CP schematic from [5]

2.2.3 Loop Filter

It will be shown that noise is one of the most crucial design performance parameters when it comes to PLLs. The control voltage, V_{tune}, which is fed into the VCO, is extremely important when considering the noise performance of the closed loop system. Any noise present on the V_{tune} will cause unwanted frequency jitter at the PLL output signal f_{out}, making it extremely sensitive. In its simplest form, the loop filter is a low pass passive filter which is used to reduce the high frequency noise.

Generally speaking, a PLL can also function without a loop filter. These types of PLLs are called 'first order PLL's. They tend to produce large frequency jitter on the output of the loop deeming them intolerable for most applications. The solution to this unwanted jitter is to include a loop filter component into the scheme [7]. Generally, a PLL is always at least a first order feedback system.

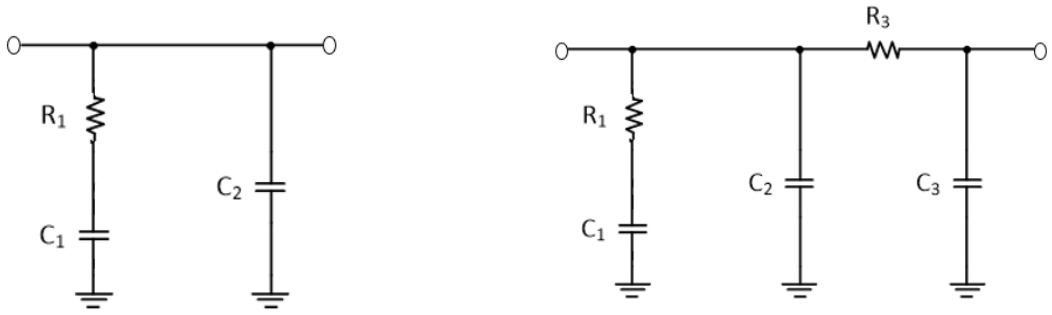
The LF performs two operations on the CP output. First it converts the discrete output current of the CP to a continuous DC voltage used for the VCO operation.

Secondly, it attenuates the high frequency noise on the control voltage signal. It is necessary to eliminate noise on the control voltage because it is represented as jitter on the PLL output signal. The higher the order of the filter, the better the attenuation of this jitter is [8].

Many forms of the LF exist. Ordinarily, passive filters are chosen over active ones, since they produce less noise which then has less influence on the PLL output. As mentioned, the noise performance of the LF can be enhanced by increasing the order of the filter. However, this has the negative effect of increasing the loop complexity and potentially reducing the stability. Choosing the right loop filter is one of the key components in PLL design [7].

The simplest type of LF can be constructed by using a simple Resistor-Capacitor (RC) low pass filter. The standard second and third order passive LF configuration for a PLL are shown in figure 2.7. These LF are commonly used in most PLL circuits in RF and wireless communication systems mostly due to their better noise cancellation.

Generally, the loop filter is crucial for the proper functioning of PLLs, since it governs many of the loop characteristics. It is the component that gives the designer freedom to shape the loop. Its characteristics affect multiple aspects of the PLL performance such as loop stability, transient response and phase noise. In fact, the LF directly determines the PLL loop bandwidth. For larger loop bandwidths, the LF will allow more noise to pass through the filter and vice versa. This is due to the poles that the LF introduces in the PLL transfer function, which directly determines the bandwidth of the PLL [9]. However, a LF bandwidth which is too narrow will result in a PLL which locks slowly. Choosing different LF topologies or different parameters can greatly affect the loop dynamics of the PLL.



(a) Second order filter

(b) Third order filter

Figure 2.7: Passive loop filters used in PLLs

2.2.4 Voltage Controlled Oscillator

As the name implies, voltage controlled oscillators are oscillator circuits where the output frequency is controlled by the input voltage. In the PLL, the VCO is the block component which uses the LF output to generate an output signal with a frequency of f_{out}. Naturally, the output frequency is proportional to the voltage input. As the control voltage increases the frequency of oscillation will also increase and vice versa. The mathematical equation of the ideal VCO output frequency is given by:

$$f_{out} = f|_{V_{tune}=0} + K_{VCO}V_{tune} \tag{2.4}$$

where K_{VCO} is the gain of the oscillator and $f|_{V_{\text{tune}}=0}$ is the so called 'free-running frequency' which is the output frequency for $V_{tune} = 0$ [7].

The VCO design varies greatly depending on its purpose in the circuit. Typically, there are two types of VCOs used in PLLs. The first one is a chain of ring oscillators which uses an odd number of inverters connected in a feedback loop. The second type is a LC tank oscillator, these are often used since they have the best (smallest) phase noise performance.

As far as the phase is concerned, the VCO behaves like an ideal integrator. This is

due to the fact that the impulse response of an oscillator (input current or voltage vs output phase) is a step function. It should be noted that every PLL contains at least one integrator, which is the VCO. The relationship between the input control voltage and the frequency oscillation of the output frequency is called the gain of the VCO and is denoted with K_{VCO}. The transfer function of the VCO is given as:

$$H_{VCO}(s) = \frac{\varphi_{out}(s)}{V_{tune}} = \frac{K_{VCO}}{s} \tag{2.5}$$

2.2.5 Divider/ ΣΔ Modulator

The divider is the component of the PLL that allows the output frequency to be a multiple of the input frequency. The objective is to amplify frequencies to higher frequencies by inserting a divider between the VCO and the PFD. The output frequency coming from the VCO gets divided and then is fed back into the PFD. This is crucial since crystal oscillators only go up to about 300MHz, any frequencies higher than that must involve a divider when using a PLL.

Additionally, there are integer-N PLLs and fractional-N PLLs. Integer-N PLLs, as the name implies, only allow the output frequency to be an integer multiple of the reference frequency, which can be seen in the equation below:

$$f_{out} = f_{in}N \tag{2.6}$$

N is referred to as the 'loop frequency divide ratio' and is an integer value. Such PLLs have some major disadvantages. These disadvantages were thoroughly described in the paper [10]. The authors explained that the main problem with integer-N PLLs is the trade-off between the channel spacing, also known as the frequency resolution, and the loop bandwidth. Generally, a small channel spacing (which corresponds to a high frequency resolution) requires that reference frequency, f_{ref}, needs to the small. However, using a small reference frequency leads to two main issues. The first one being that, a low reference frequency implies a small loop bandwidth which in return results in

slow switching time. The seconds disadvantage is, that the reduction of the reference frequency leads to an increase in the phase noise because of the high division ratio. The fractional-N PLL is proposed in the paper to solve the trade-off issue which occurs in the integer-N PLL. The fractional-N PLL is advantageous since it offers a higher frequency resolution, a lower phase noise and a larger loop bandwidth. The larger loop bandwidth results in a faster switching time. In contrast to the integer-N PLL (seen in equation 2.6), the output frequency of the fractional-N PLL is given as:

$$f_{out} = f_{in}(N\alpha) \tag{2.7}$$

where N is again an integer and α is any fraction. Generally speaking, the basic principle behind a fractional-N PLL is similar to a integer-N PLL, however it includes additional digital circuitry that allows it to accurately interpolate between integer multiples of the reference frequency [11]. Most fractional-N PLLs are based on using $\Sigma\Delta$ modulators. Nevertheless, the fractional-N PLL also has drawbacks as it suffers from fractional spurs [10].

For the general phase noise considerations, the phase noise performance of integer-N may even out-perform that of fractional-N PLLs, but only if a high resolution in frequency is not needed. If this is not the case, then fractional-N PLLs generally give an improved phase noise performance since a lower value of N is being used compared to an integer-N PLLs. However, the fractional synthesizer is more complex.

2.3 Phase Lock Loop Bandwidth

The bandwidth of a PLL is an extremely important parameter which determines how fast the PLL follows the input phase and how long it will remain in the lock condition [12].

The bandwidth of a PLL depends on the characteristics of the PFD, VCO and the LF. Generally, in linear model of a PLL like the one shown in figure 2.8, the PFD has a gain of K_D , the LF has a transfer function $F(s)$, and the VCO has a gain of K_{VCO}.

The bandwidth of the PLL is dependent on all of these parameters. However, the one of most importance is the LF transfer function, as it allows the designer to determine the bandwidth by adjusting the poles in the transfer function. In comparison, the gains of the PFD and VCO, K_D and K_{VCO}, are not as easily adjustable and are limited by other constraints [12].

The forward loop gain, $G(s)$, can be written as:

$$G(s) = \frac{K_D F(s) K_{VCO}}{s} \tag{2.8}$$

While the closed loop gain is given as:

$$\frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{G(s)}{1 + G(s)H} \tag{2.9}$$

where H represents the divider in the feedback path.

$$H = \frac{1}{N} \tag{2.10}$$

The loop bandwidth, ω_c, is defined as the frequency at which $|G(s)H| = 1$

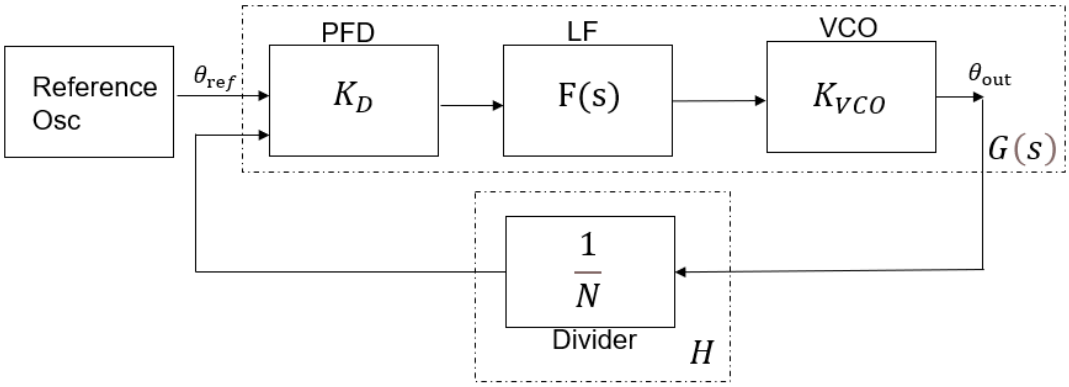


Figure 2.8: PLL linear model

For the phase noise frequencies inside the loop bandwidth, hence $G(s)H >> 1$, the reference oscillator, PFD, divider and LF dominate the overall phase noise of the PLL.

However, for the phase noise frequencies outside the loop bandwidth, $G(s)H << 1$, the VCO noise dominates [13]. This will be discussed in detail in chapter 4.

As mentioned previously, there are trade-offs which exist when choosing the loop bandwidth. Usually, smaller loop bandwidth is desirable since the total noise in such a scenario is minimized. However, such a system results in slower frequency acquisition. This means that more time is needed to obtain the required frequency [14].

2.4 Phase Noise

2.4.0.1 Basic Concept and Mathematical Formulation

Phase noise is an important parameter when it comes to PLLs. It is usually characterized in the frequency domain and describes the frequency stability of a signal. The following equations and their meanings are taken from [4].

Assuming a pure ideal sine wave (which is the expected output of an ideal synthesizer) given as:

$$V(t) = V_o sin(2\pi f_o t) \tag{2.11}$$

In reality, such a signal does not get transmitted. Instead, a signal with amplitude and phase variations appears, given as the following:

$$V(t) = (V_o + v(t))sin(2\pi f_o t + \phi(t)) \tag{2.12}$$

Here, $v(t)$ and $\phi(t)$ are seen as the amplitude and phase fluctuations respectively. Since it is possible to remove the amplitude fluctuations, these are not of significant importance, phase fluctuations however are not as simple to deal with. There are two different types of phase fluctuations, namely periodic and random variations. These are modeled as:

$$\phi(t) = \Delta\phi \sin(2\pi f_m t) + \varphi(t) \tag{2.13}$$

The first term represents the periodic phase variation, which produces a tone at an offset frequency of f_m from the carrier frequency f_o. The second term, $\varphi(t)$, represents the random variations and it is the cause of phase noise. Ideally, this phase noise will be small.

The spectral density is given as the following:

$$S_\varphi(f) = \int_{-\infty}^{+\infty} R_\varphi(\tau) e^{-j2\pi f\tau} d\tau \tag{2.14}$$

With $R_\varphi(\tau)$ being the auto-correlation of $\phi(t)$.

An important term when considering phase noise is the Single-sideband (SSB) phase noise. Since the phase noise falls at frequencies further from f_o it needs to be specified at certain "frequency offset", i.e a certain difference with respect to f_o [5]. SSB phase noise specifies how phase noise is quantified and is defined as the ratio of the noise power in 1Hz bandwidth at a frequency offset ($\Delta f = f - f_0$) from the carrier to the carrier power. The unit of phase noise is given in dBc/Hz [4].

The mathematical formulation of the SSB phase noise is:

$$£(\Delta f) = 10 \log \frac{P_{\text{noise}}\ (1\ \text{Hz at}\ f)}{P_{\text{carrier}}} \text{dBc/Hz} = 10 \log \frac{S_\varphi(\Delta f)}{2} \text{dBc/Hz} \tag{2.15}$$

where the nominator in the first expression, P_{noise}, represents the noise power in 1 Hz bandwidth and the denominator, $P_{carrier}$, denotes the carrier power. Note that S_φ, represents the Double-sideband (DSB) phase noise. The SSB, £, is simply half of the DSB.

In the frequency domain this effect presents itself as the following. Instead of having a single dirac delta in the frequency domain (the shape of a single impulse), there are now additionally 'skirts' created on either side of the carrier frequency causing the spectrum

to broaden since the signal's energy is spilled in the vicinity of the impulse. Instead of having the pure carrier, the phase noise produces the pure carrier and additional side bands. The larger random frequency fluctuations occur with lower probabilities because the oscillator tries to maintain $f = f_o$ (for the most part), this also explains the declining shape of the spectrum as $|f - f_o|$ increases [15]. Figure 2.9 illustrates the phase noise of a signal of frequency f_0:

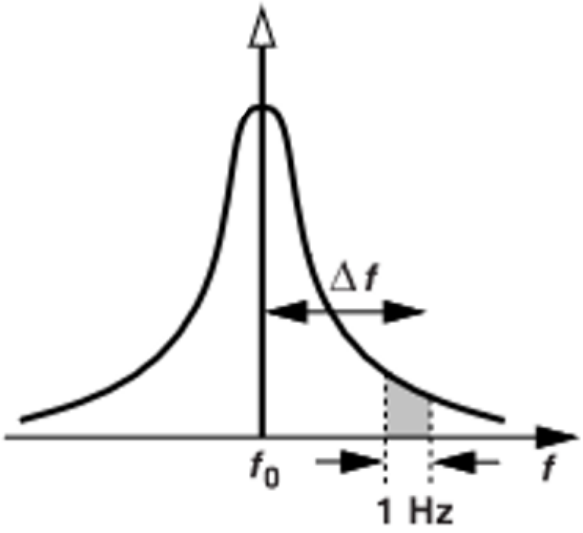


Figure 2.9: Spectrum indicating how phase noise is specified [15]

2.4.0.2 Effect of Phase Noise

One effect of phase noise is called 'reciprocal mixing', it describes why the presence of phase noise in a signal is undesired. At the receiver, the desired signal is convolved with a local oscillator which results in a Intermediate frequency (IF) signal at an angular frequency $\omega_{IF} = \omega_{in} - \omega_{LO}$. However, every oscillator produces some amount of phase noise, the local oscillator is no different. This phase noise will present itself as sidebands on both sides of the Local oscillator (LO) signal, as was shown in figure 2.9. The signal itself can be accompanied by a large interferer. If the phase noise from the LO is superimposed onto the interferer, it can mask out a much lower level desired signal. This

results in a broadened downconverted interferer whose noise skirt corrupts the desired IF signal [5].

Figure 2.10 was taken from [5], it illustrates this scenario perfectly:

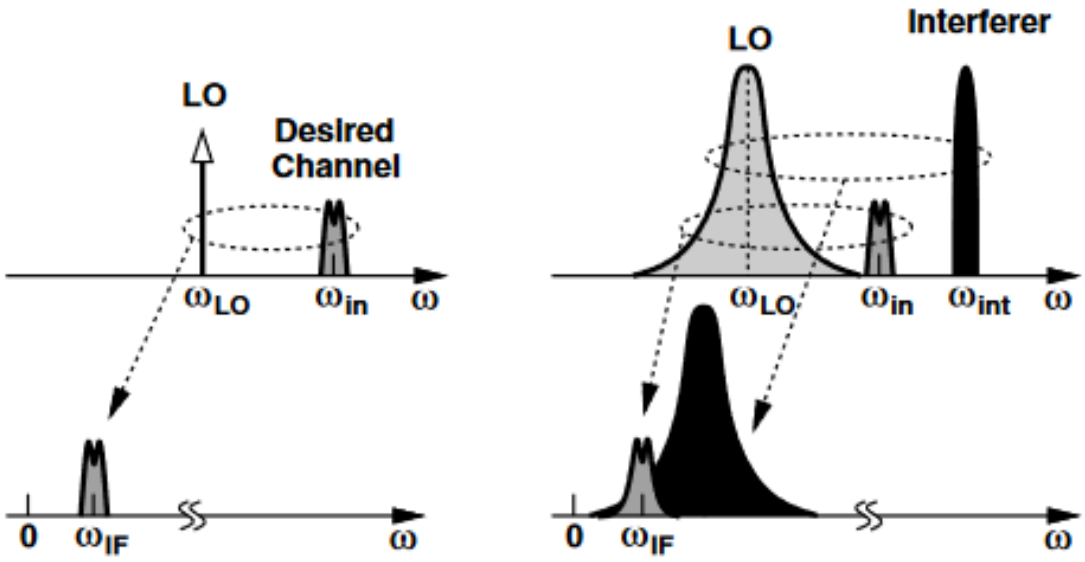


Figure 2.10: Reciprocal mixing [5]

The left hand side shows the ideal scenario when the LO does not produce phase noise and the signal of interest is not accompanied by an interferer. Through a down conversion a 'clean' IF signal is created. On the right hand side, the effect of reciprocal mixing is shown. The adjacent channel power is much higher than the desired signal. The down conversion with a noisy LO limits the receivers effective sensitivity and dynamic range.

Reciprocal mixing is just one effect that the phase noise has on a system. Another common effect of phase noise is the significant increase in bit error rate. With increased phase noise, both in the transmitter and receiver, can lead to an increase in the occurrence of bit errors. However, regardless of the effect caused, it is crucial that for all applications the phase noise on the signal is known and within the required specification limits [16].

CHAPTER 3

Methodology

In this chapter, the mathematical equations used in the MATLAB model are explained in detail. Firstly, the PLL transfer functions are introduced, they are the foundation for producing the phase noise spectrum in the model. Apart from the transfer functions, it is also necessary to analyze certain parameters for the amplifier, ADC and analog test bus in more detail since these are the components which are included in the BIST setup. It is important that their specifications are correct in order to obtain a meaningful measurement.

3.1 Continuous-Time Linear Phase Analysis

3.1.1 Transfer Functions Referred to the VCO Output

As discussed previously, the phase noise significantly effects the performance of the PLL. The total phase noise of the PLL is a contribution coming from each component in the loop.

In figure 3.1 the noise contributions are modeled in a linear phase model. It shows all the equivalent noise sources for each individual contributor. The phase noise is added to the output of the components. The phase noise contributions coming from the reference,

VCO, divider and ΣΔ modulator are represented by θ_{ref}, θ_{vco}, θ_{div} and $\theta_{\Sigma\Delta}$ respectively. Similarly, i_{pole}, i_{zero} are the current noises coming from the charge pump and v_n is the noise voltage from the loop filter [17]. The symbol θ_{out} represents the phase noise at the output of the PLL which is influenced by each of the individual block components.

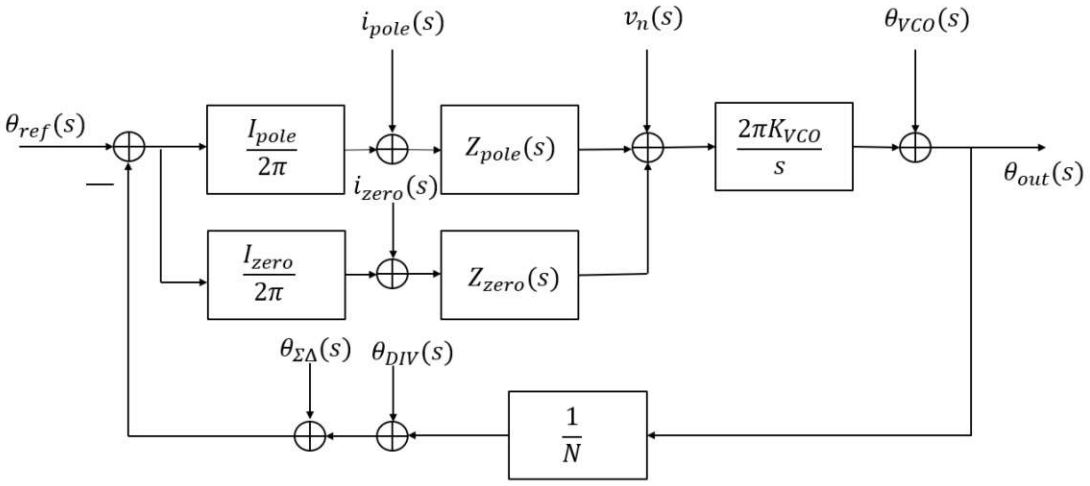


Figure 3.1: PLL block diagram including the individual noise contributions

In order to properly analyze the phase noise in the PLL, the closed loop and open loop transfer functions must be introduced. When the PLL is in the locked state, the phase at the output of the divider tracks the phase of the reference signal, this means that the open loop transfer function is given when the feedback loop is disconnected from the input junction. This implies that the open loop transfer function is a product of the individual loop gains, given by the following formula:

$$H_{OL}(s) = \frac{1}{N}\frac{K_{VCO}}{s}\left[Z_{pole}(s)I_{pole} + Z_{zero}(s)I_{zero}\right] \tag{3.1}$$

This open loop transfer function is a characteristic of a closed loop system. The closed loop transfer functions determine the behaviour of a feedback system. These closed loop transfer functions relate signals around the loop (for e.g. the output) to external signals injected into the loop (which in our case are the individual noise contributors).

This concludes that it is necessary to view a single noise contributor at a time, in this way the transfer functions from each noise source to the output are obtained [17].

It follows that the transfer function of the output to the input reference noise is given as:

$$H_{REF}(s) = \frac{\theta_{out}(s)}{\theta_{ref}(s)} = N\frac{H_{OL}(s)}{1 + H_{OL}(s)} \tag{3.2}$$

Next, it is also possible to write the transfer functions of the output to the charge pump current noises i_{pole} and i_{zero}:

$$H_{POLE}(s) = \frac{\theta_{out}(s)}{i_{pole}(s)} = \frac{2\pi K_{VCO}}{s} Z_{pole}(s)\frac{1}{1 + H_{OL}(s)} \tag{3.3}$$

$$H_{ZERO}(s) = \frac{\theta_{out}(s)}{i_{zero}(s)} = \frac{2\pi K_{VCO}}{s} Z_{zero}(s)\frac{1}{1 + H_{OL}(s)} \tag{3.4}$$

The transfer function of the output with respect to the loop filter equivalent noise source is given as:

$$H_{LF}(s) = \frac{\theta_{out}(s)}{v_n(s)} = \frac{2\pi K_{VCO}}{s}\frac{1}{1 + H_{OL}(s)} \tag{3.5}$$

The PLL output to the VCO noise gives the following transfer function:

$$H_{VCO}(s) = \frac{\theta_{out}(s)}{\theta_{VCO}(s)} = \frac{1}{1 + H_{OL}(s)} \tag{3.6}$$

Lastly, the transfer functions that describe the PLL output to the divider noise and $\Sigma\Delta$ modulator noise are the same:

$$H_{\Sigma\Delta}(s) = H_{DIV}(s) = \frac{\theta_{out}(s)}{\theta_{DIV}(s)} = \frac{\theta_{out}(s)}{\theta_{\Sigma\Delta}(s)} = -N\frac{H_{OL}(s)}{1 + H_{OL}(s)} \tag{3.7}$$

Up until now, each individual noise source was considered by itself, in order to calculate the total noise at the PLL output, all the block noise contributions are added together in an Root mean square (RMS) sum. This is possible since the noise sources are uncorrelated, the total output noise power is given as:

$$\begin{aligned}&\theta_{out}^2(s) = (\theta_{ref}(s)|H_{REF}(s)|^2)+\\&(i_{pole}(s)|H_{POLE}(s)|^2) + (i_{zero}(s)|H_{ZERO}(s)|^2) + (v_n(s)|H_{LF}(s)|^2)+\\&(\theta_{VCO}(s)|H_{VCO}(s)|^2) + (\theta_{DIV}(s)|H_{DIV}(s)|^2) + \left(\theta_{\Sigma\Delta}(s)|H_{\Sigma\Delta}(s)|^2\right)\end{aligned} \tag{3.8}$$

3.1.2 Transfer Functions Referred to the VCO Input

The first task in this thesis is to use the PLL model in MATLAB to produce the phase noise spectrum before and after the VCO. Using the equations from the previous section, it is possible to produce the phase noise spectrum at the output of the PLL. In order to produce the phase noise spectrum before the VCO, it is necessary to rewrite the transfer functions in such a way as to redefine a new output (which is the VCO input). The transfer functions from the individual noise sources towards the input of the VCO will provide the resulting phase noise spectrum.

For the sake of simplicity, the PLL components are grouped together to recreate a traditional feedback loop used in control system theory. This gives a better overview in the sense that it is easier to overlook the equations and check their correctness. The block diagram with the redefined output can be seen in figure 3.2. Here, A_1 represents the PFD,CP and the LF, A_2 represents the VCO and B represents the divider and $\Sigma\Delta$ modulator. The phase noise contributions coming from the reference are expressed via Nin, N_{a1} defines the noise from the PFD,CP and the LF. Additionally, N_{a2} stands for the injected noise source from the VCO. The divider and $\Sigma\Delta$ modulator noise contribution are denoted as N_b. In chapter 3.1, the transfer functions were calculated towards the output of the VCO, namely Out_1. Note that now with the redefined output, Out_2, the VCO noise becomes part of the feedback loop itself. First, the simplified noise transfer functions will be derived with this method.

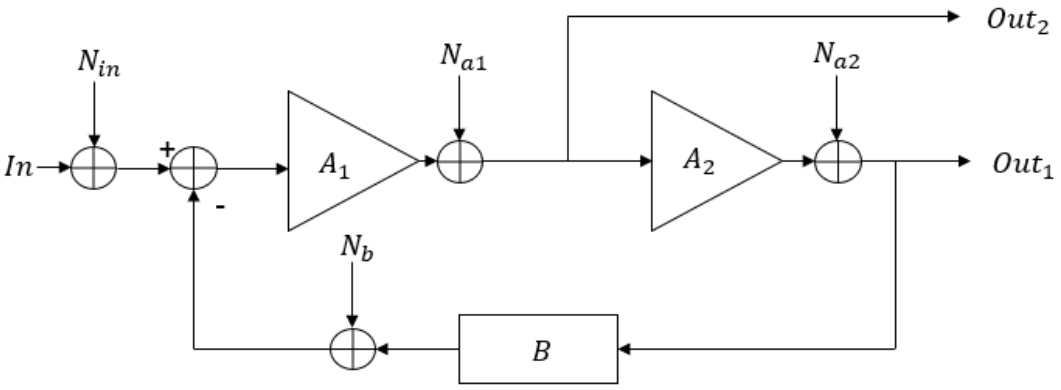


Figure 3.2: Simplified traditional feedback system

The simplified transfer functions lead to:

$$H_{Nin} = \frac{Out_2}{N_{in}} = \frac{A_1}{1 + A_1 A_2 B} \tag{3.9}$$

$$H_{Na2} = \frac{Out_2}{N_{a2}} = \frac{-A_1 B}{1 + A_1 A_2 B} \tag{3.10}$$

$$H_{Na1} = \frac{Out_2}{N_{a1}} = \frac{1}{1 + A_1 A_2 B} \tag{3.11}$$

$$H_{N_b} = \frac{Out_2}{N_b} = \frac{-A_1}{1 + A_1 A_2 B} \tag{3.12}$$

The gain of the charge pump is:

$$G_{CP}(s) = \left[Z_{pole}(s) \frac{I_{pole}}{2\pi} + Z_{zero}(s) \frac{I_{zero}}{2\pi} \right] \tag{3.13}$$

The following equations are analogous to the ones in the previous chapter, except now the individual noise sources are referred to the VCO input instead of the output and are given as the following:

$$H_{REF}(s) = \frac{\theta_{VCO_{IN}}(s)}{\theta_{ref}(s)} = G_{CP} \frac{1}{1 + H_{OL}(s)} \tag{3.14}$$

$$H_{POLE}(s) = \frac{\theta_{VCO_{IN}}(s)}{i_{pole}(s)} = Z_{pole}(s)\frac{1}{1+H_{OL}(s)} \tag{3.15}$$

$$H_{ZERO}(s) = \frac{\theta_{VCO_{IN}}(s)}{i_{zero}(s)} = Z_{zero}(s)\frac{1}{1+H_{OL}(s)} \tag{3.16}$$

$$H_{LF}(s) = \frac{\theta_{VCO_{IN}}(s)}{v_n(s)} = \frac{1}{1+H_{OL}(s)} \tag{3.17}$$

$$H_{VCO}(s) = \frac{\theta_{VCO_{IN}}(s)}{\theta_{VCO}(s)} = \frac{\theta_{VCO_{IN}}(s)}{\theta_{out}(s)} = -\frac{1}{N}G_{CP}\frac{1}{1+H_{OL}(s)} \tag{3.18}$$

$$H_{DIV}(s) = \frac{\theta_{VCO_{IN}}(s)}{\theta_{DIV}(s)} = \frac{\theta_{VCO_{IN}}(s)}{\theta_{\Sigma\Delta}(s)} = -G_{CP}\frac{1}{1+H_{OL}(s)} \tag{3.19}$$

The total noise is calculated by adding all the block noise contributions in an RMS sum just like in equation 3.8. In the next chapter these equations are used in the MATLAB model to produce the spectral plots with the total noise before and after the VCO. The results will be shown and analyzed in that section.

3.2 Low Noise Amplifier

Next, it is necessary to consider the LNA in more detail. Two parameters are of specific importance when it comes to the amplifier, namely the gain and the input-referred noise, these will be discussed in this section.

3.2.1 Amplifier Gain

The amplifier plays a key role in the setup, since it must amplify the small noise voltage sufficiently for it to fit into the Full scale range (FSR) of the ADC. The question then becomes, how large does this gain provided by the LNA need to be to boost such a small noise voltage, in the range of 10^{-4}-10^{-5}, to the FSR of the ADC converter?

The voltage gain is given via the following formula:

$$\text{Voltage Gain } (A_v) = \frac{\text{Output Voltage}}{\text{Input Voltage}} = \frac{V_{out}}{V_{in}} \tag{3.20}$$

Calculating the gain in terms of decibels leads to:

$$A_v = 20\log(A_v)\text{dB} \tag{3.21}$$

The exact values proposed for the BIST setup are considered in chapter 4.

3.2.2 Input-Referred Noise

There are many different types of amplifiers, the one being used in the setup is called a 'Low Noise Amplifier' which is used to amplify a low-power signal without significantly degrading its Signal-to-noise ratio (SNR). The amount of noise coming from the LNA is the second aspect that has to be determined. The LNA does not only amplify the signal and the noise which is present at the input, but the amplifier itself will also introduce some of its own noise which will further contribute to the signal degradation. Evaluating how large this LNA noise is, is crucial for conducting a meaningful measurement.

Resistor thermal noise refers to the random motion of electrons in a conductor which introduces fluctuations in the voltage measured across the conductor even if the average current is zero. Thus, the spectrum of thermal noise is proportional to the absolute temperature [18]. For a resistor with a value R_s, the generated thermal noise voltage is equal to:

$$\overline{V_n^2} = 4kTR_s \tag{3.22}$$

where k is the Boltzmann constant and T represents the absolute temperature. The noise is modeled as a voltage source in series with the resistor and its spectrum is white since it carries equal power at all frequencies [15].

The concept of 'input-referred noise' is used to represent the effect of all noise sources in a circuit by a single source, $\overline{V_{n,in}^2}$ at the input. Figure 3.3 illustrates this concept, a noisy circuit with multiple noise sources is replaced by a noiseless circuit with

a single input-referred voltage source where the output noise of both the circuits, $\overline{V_{n,out}^2}$, is equal [18].

(a) Noisy circuit with multiple noise sources

(b) Noiseless circuit with input-referred voltage

Figure 3.3: Input-referred noise voltage [18]

It should be mentioned that the input-referred noise voltage is in fact a fictitious quantity that cannot be measured at the input of the circuit. It is only mathematically equivalent to a noisy circuit. Additionally, the input-referred noise indicates how much of the input signal is corrupted by the circuit's noise [18].

Another important concept is that of the 'noise figure', which is another metric of noise performance. The noise figure provides an easier measurement than the input-referred noise source, especially at high frequencies.

The SNR is defined as the signal power divided by the noise power and is an quality metric which compares the strength of a desired signal to the strength of background noise which is present.

$$SNR = \frac{P_{signal}}{P_{noise}} \tag{3.23}$$

If the circuit is noiseless, the SNR at the input and the output are the same. To measure how noisy the circuit is, the noise figure is defined as the following:

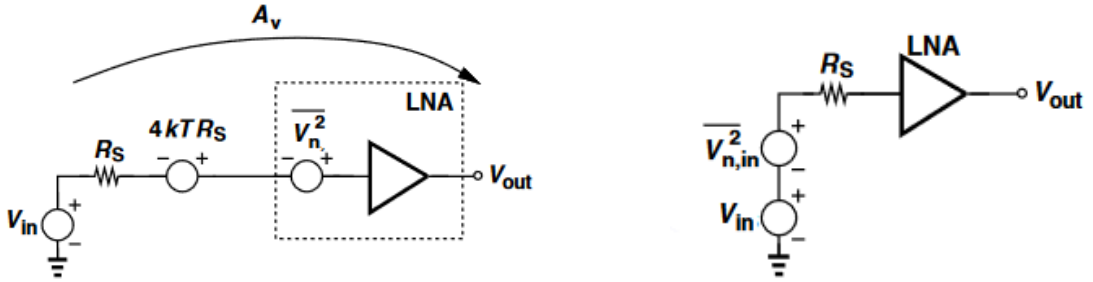
$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{3.24}$$

In the previously mentioned noiseless circuit, the noise figure would be 1. The noise figure can also be expressed in terms of decibels:

$$NF = 10 \log \frac{SNR_{in}}{SNR_{out}} \text{dB} \tag{3.25}$$

It is important to note that the noise figure depends on the source impedance. This means that the noise figure needs to be specified with respect to a source impedance, which typically is 50 Ω. Equation 3.22 shows that the resistor thermal noise is also temperature dependent. From the equation it can be seen that larger resistances and higher temperatures generate more noise. However, in practice reducing the temperature is typically not done, since a large degree of cooling is required to achieve a significant reduction in noise.

The model provided in [5] is considered in this thesis and can be seen in figure 3.4, where in the simplified circuit the noise of the LNA is represented solely by one voltage source:



(a) Noisy circuit

(b) Noiseless circuit with input-referred voltage

Figure 3.4: LNA with input-referred noise voltage and the simplified circuit, slightly modified from [5]

The noise figure in this scenario becomes:

$$NF = \frac{\overline{V_{n,out}^2}}{A_v^2} \frac{1}{4kTR_s} = 1 + \frac{\overline{V_{n,in}^2}}{4kTR_s}. \tag{3.26}$$

The source impedance from the resistor causes thermal noise which is equal to $4kTRs$. The LNA with a gain A_v and a NF can then be represented by a noiseless LNA with gain A_v and added input noise power spectral density and in this way separating the noise from the noisy circuit. The effect of the independent noise sources in figure 3.4 a) towards the output are combined in a single voltage source, $\overline{V_{n,in}^2}$.

As mentioned, the formulas and concepts in this chapter will be used in chapter 4 to calculate certain specifications of the LNA in regards to the gain and the noise figure.

3.3 Analog to Digital Converter

The ADC also plays a crucial role in the setup since the results at the ADC output are used for further digital post processing. An ADC is used to convert a continuous time analog input signal into a discrete digital output signal. This process of converting analog values to digital ones consists of 3 main tasks, namely sampling, quantizing and coding, each of which will be considered in this chapter. Storing a value in the digital domain has several advantages such as using digital signal processing techniques, easier storage, use of computers and robust transmission. In the BIST setup used in the thesis, the ADC is used as the last step to store the phase noise information coming from the VCO input. The results will then undergo further post processing in an attempt to draw conclusions concerning the phase noise at the VCO output.

Figure 3.5 shows the basic block diagram of a ADC.

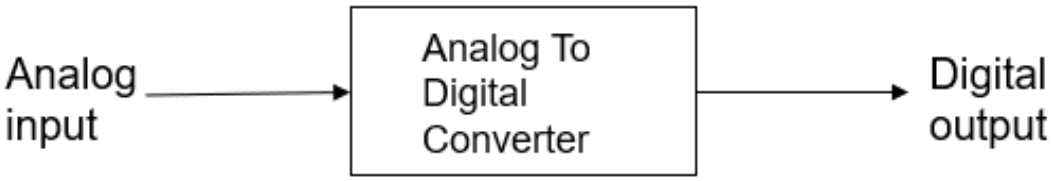


Figure 3.5: Basic principal of an ADC

As can be seen in figure 3.6, a basic ADC consists of three main blocks, namely:

- Sampler: A continuous-time signal is sampled at integer multiples of the sampling instant to obtain a discrete-time signal
- Quantizer: The discrete-time output of the sampler is sent through a quantizer to represent each value as a discrete-valued digital signal. The quantizer replaces each sample with an approximation from a finite set of discrete values
- Coder: The discrete values obtained during the process of quantization are converted into digital code. Each amplitude level is represented as a sequence of binary digits.

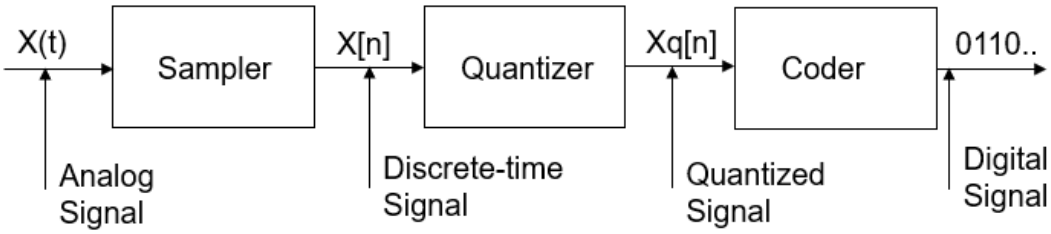


Figure 3.6: ADC block diagram

The input of an ADC is an analog signal which contains an infinite amount of values, the goal is to map these values to a specific number of digital values. The process of how this works will be described in detail in the following sections.

3.3.1 Sampling and Nyquist Theorem

Sampling the input signal is necessary to inspect the value of an analog signal at regular time intervals. This gives an accurate representation of how the signal is changing over time. The process of sampling is described mathematically via the following formula:

$$x[n] = x(nT_s), -\infty < n < \infty \tag{3.27}$$

The time between samples is a quantity referred to as the 'sampling period', while the number of samples taken per second is called the 'sampling frequency'. The sampling period and sampling frequency are related to each other via the following equation:

$$f_s = 1/T_s \tag{3.28}$$

A crucial aspect of sampling is the so called 'Nyquist sampling theorem' which states how often the sampling should occur in order to accurately reconstruct an analog signal from its samples. If only a few samples are taken the original signal may not be reconstructed correctly (especially for fast varying, high frequency signals). On the other hand, if too many samples are taken the cost of equipment increases as well as the memory needed to store a large volume of data. The Nyquist sampling theorem states that the sampling frequency must be at least twice the maximum frequency of the signal in order to perfectly reconstruct the original signal from its samples. This indicates that sampling does not result in a loss of information as long as the following holds:

$$f_s \geq 2f_{max} \tag{3.29}$$

If the sampling frequency is not being met, the original signal may be reconstructed into another waveform which occurs due to an effect called 'aliasing'. This effect is highly undesirable.

3.3.2 Quantization Error and its Noise Power Spectral Density

After the signal has been appropriately sampled, it needs to be sent through the quantizer. The approximation or rounding effect in an ADC is known as quantization [19].

In an ADC, the range of possible input values is divided up into equally sized intervals and each of the sampled inputs is mapped to a discrete level. The values which are allowed in the digital signal are called the 'quantization levels'. In a N bit quantizer, each quantization level is represented with N bits, such that the number of levels equals

2^N. The quantizer then rounds each sampled value to the nearest quantization level [20]. An important term used for ADCs is the so called 'resolution', it defines the smallest voltage change that can be measured by the ADC. Resolution is closely tied to precision, as it is the smallest variation in analog signal that will result in a variation in the digital output and is mathematically defined as:

$$\Delta = \frac{V_{max} - V_{min}}{2^N} \tag{3.30}$$

where V_{max} and V_{min} are the maximum and minimum input voltage that can be applied to the ADC respectively. Their difference defines the input voltage range. The resolution, Δ, is equal to the value of the Least Significant Bit (LSB).

Simply put, the resolution can be thought of as the accuracy of the measurement. An increase in resolution results in more precise measurement values. However, dealing with very high resolution comes with its own drawbacks, since it is difficult to measure with such high accuracy consistently and the amount of storage capacity grows immensely. Determining the right resolution is important since it directly impacts the amount of noise present in the digital signal. As the number of quantization levels increase, the quantization step size decreases which in turn increases the accuracy of the quantizer [20].

Quantization is often most easily explained via an example. Assume that a sinusoidal signal from 0-1V needs to be quantized with a 3 bit ADC. This will result in a total of $2^3 = 8$ levels. The distance between the levels or resolution is (1-0)/8=0.125V. Each level needs to be represented as a binary sequence, for e.g: 000 for 0V up to 111 for 1V. As the number of bits of the ADC increases, the signal will be represented more accurately.

Another important term often used in conjunction with ADCs is the 'dynamic range' which is defined as the ratio between the highest and lowest values that the ADC can reliably measure. The dynamic range of the ADC is determined by the number of bits and is defined as:

$$DR = 20 \log \left(\frac{A_{RMSmax}}{A_{RMSmin}} \right) \text{dB} \tag{3.31}$$

where A_{RMSmax} and A_{RMSmin} are the maximum and minimum RMS amplitude values of the signal respectively.

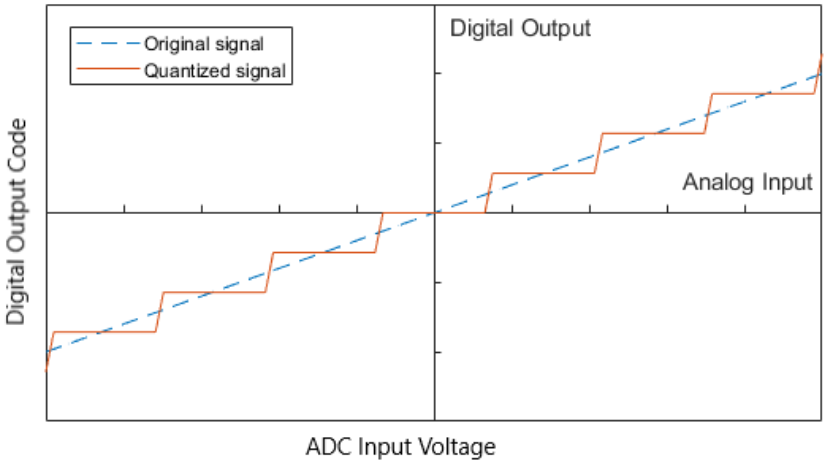
For a constant DC input within its FSR, an ideal N bit ADC can measure the maximum and minimum RMS amplitudes of FSR and $FSR/2^N$, respectively. Therefore, the dynamic range of the ADC is [21]:

$$DR = 20 \log \left(\frac{FSR}{FSR/2^N} \right) \text{dB} \approx 6.02\text{dB} \cdot N \tag{3.32}$$

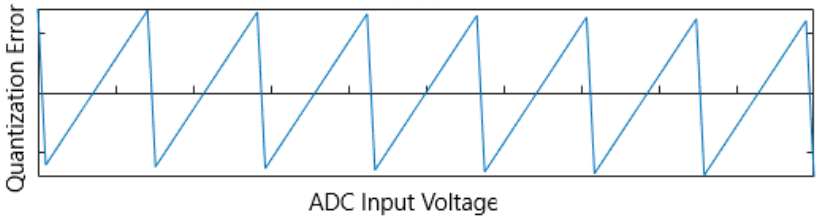
To achieve the maximum possible ADC precision, it is favorable that the ADC dynamic range fully matches the maximum amplitude of the signal. Using the example before assume that the 0-1V sinusoidal signal enters a 3 bit ADC which maximum input voltage is 2V. The maximum signal value converted by the ADC is 1V and it is being represented by 4 bits instead of the available 8. This means that there are 4 unused transitions, which results a loss in the converted signal accuracy. This is the main reason why the LNA is placed before the ADC to match the dynamic range to the maximum signal amplitude.

Additionally, it is important to mention that many signals consist of both large and small voltage components. In such an instance, a high resolution ADC which has a large dynamic range is necessary to accurately measure the signal.

The input/output characteristic curve can be seen in figure 3.7 a), it shows the analog values of the input on the x-axis and the digital values of the output on the y-axis.



(a) ADC input/output characteristic curve



(b) ADC quantization error

Figure 3.7: Ideal ADC quantizing analog input to digital output including error

The higher the resolution, the more bits are used to quantize the signal, which in return results in a better quantized signal. However, regardless of the number of bits used to represent the signal, some error will always be present, since a infinite amount of analog values are being represented by a finite amount of digital ones. The process of quantization results in a loss of information which is irreversible since all samples in a distance $\Delta/2$ about a certain quantization level are assigned the same value [20]. The error that is caused by this phenomenon is called the 'quantization error'. The quantization error, $e[n]$, is defined as the difference between the analog input, $x[n]$, and the digitized output, $x_q[n]$, at each sampling instant.

$$e[n] = x[n] - x_q[n] \tag{3.33}$$

The quantization error is described via a saw-tooth behaviour in figure 3.7 b) and its statistical characterization will be defined. The quantization error which occurs through the process of rounding is bounded between -$\Delta/2$ ≤e[n]≤$\Delta/2$.

The quantization error introduces additional noise to the output which is termed as the 'quantization noise'. Obviously, the more bits being used to represent the analog signal, the more accurate the representation in the digital domain and therefore the smaller the effect of the quantization noise which is distorting the signal.

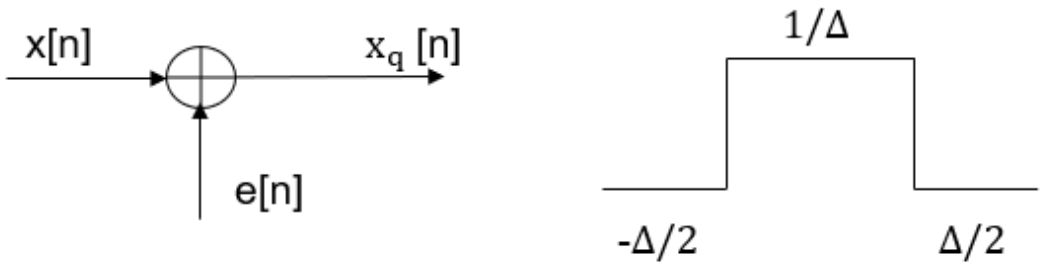


Figure 3.8: Quantization error statistics

Figure 3.8 illustrates the additive noise model for quantization on the left hand side. On the right side figure 3.8 shows how the quantization noise can take on any value between $-\Delta/2$ and $\Delta/2$, resulting in a probability density function which has an uniform distribution. Considering that the integral of the probability density function is equal to one, its value will be $1/\Delta$ for this range of values.

The quantization error has specific properties and can be modeled, with the following assumptions:

- the noise is modeled as stationary random process, which implies that the characteristics of the error will not change over time

- it is uniformly distributed between the extremes -$\Delta/2 \leq e_q[n] \leq \Delta/2$, this means it is equally likely for the error to take any value in that range
- the values in the sequence are uncorrelated between each other
- the error is independent of the input signal, there is no obvious pattern between the error and the input.

These characteristics are reasonable if x[n] appears to be random and if Δ is small enough.

A very important parameter concerning the quantization noise is the noise power spectral density. It indicates how the noise power spreads throughout the frequency bands. To find the power spectral density, the Fourier transform of the auto-correlation function of the noise needs to be calculated. Assuming that the noise samples are not correlated with one another, it is possible to approximate the auto-correlation function with a delta function in the time domain. Since the Fourier transform of a delta function is equal to one, the power spectral density will be frequency independent. Therefore, the quantization noise is white noise with total power equal to [22]:

$$\sigma_e^2 = \frac{\Delta^2}{12} \tag{3.34}$$

This means that the noise power of the error is defined as the variance and is the quantization interval squared divided by 12. These results will be used in the next chapter to quantify the error used in the setup.

The term Signal-to-quantization-noise ratio (SQNR) is defined as the ratio of the signal power $A^2/2$ of a sinusoid at full ADC range to the noise power (3.34). The SQNR indicates how much larger the signal is on average relative to the noise,

$$SQNR = 6.02\text{dB} \cdot N + 1.76\text{dB}. \tag{3.35}$$

According to the formula, the SQNR increases about 6dB for every bit. This simplified expression is accurate enough to be used for most applications.

Since digital devices work by using binary signals, it is necessary to use encoders as a last step in an ADC. The digital signal which is a discrete value in time and amplitude is coded to a unique binary number.

CHAPTER 4

Results

The models with all the corresponding plots were created in MATLAB. The results will be presented in this chapter and the findings will be interpreted and analyzed.

4.1 Use the PLL model to produce the noise spectrum before and after the VCO

The first research question was to use the model to produce the spectrum before and after the VCO and to compare the results between the two. As mentioned in the introduction, the BIST senses at the input of the VCO and therefore it is necessary to conclude if there is the possibility to get representative information concerning the phase noise at the output of the PLL. The analysis of the different transfer functions from the previous chapter were used as a foundation for the phase noise model. By using the different transfer functions and the corresponding injected noise sources it is possible to plot the phase noise at different points in the closed loop system and examine them for different frequencies.

In figure 4.2 the open-loop phase noise profiles for all PLL block components are given.

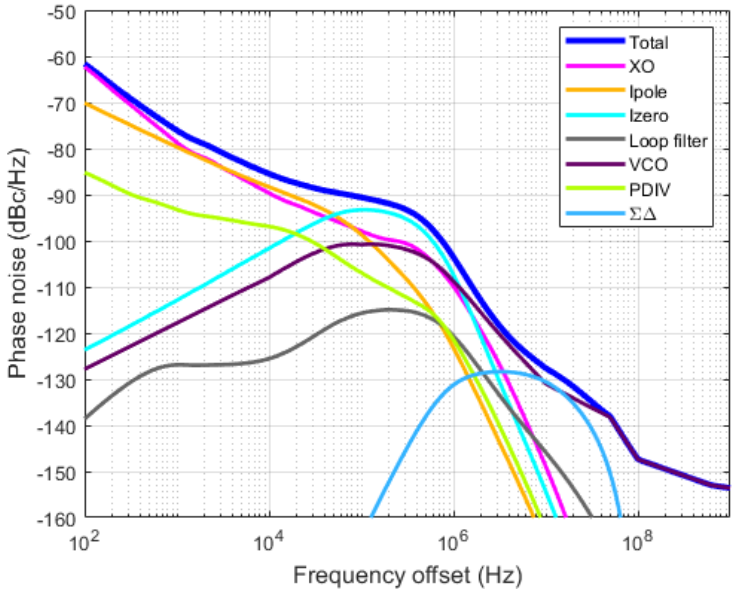


Figure 4.1: Closed loop phase noise profiles seen at the VCO output

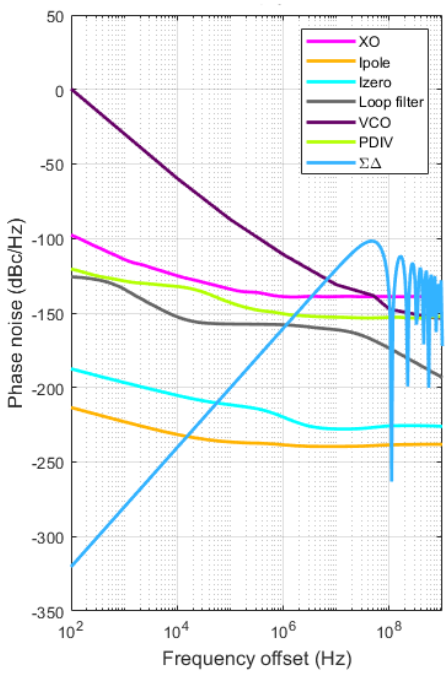


Figure 4.2: Open loop phase noise profiles seen at the VCO output

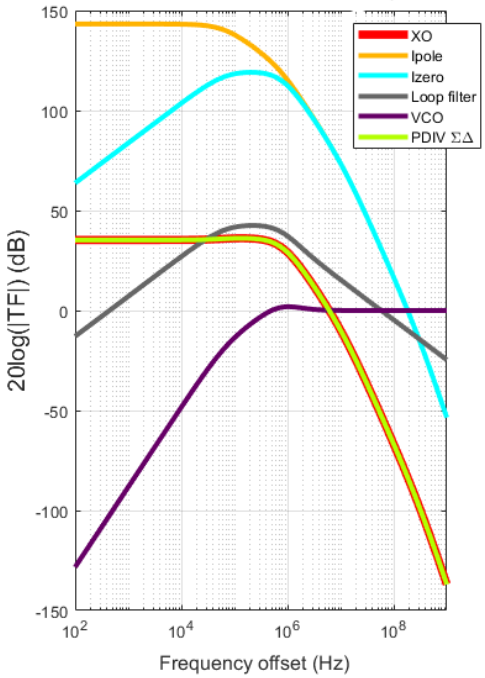


Figure 4.3: Noise transfer functions seen at the VCO output

It is interesting to look at the magnitude of the transfer functions as well as the individual noise sources at the injection points, which then get multiplied with each other correspondingly. Lastly they are combined as a quadratic sum to get the resulting total phase noise at the output as seen in equation 3.8. This indicates that the open-loop phase noise profiles in figure 4.2 are passed through the noise transfer functions in figure 4.3 to produce the output closed loop noise profiles seen in figure 4.1.

The behaviour of the phase noise at the output matches the results often found in literature. A specific example similar to the one provided in this thesis can be seen in the following paper [23]. At different offset frequencies, the noise sources have various contributions towards the output. The total noise is plotted via the dark blue line in figure 4.1.

According to the transfer functions for the reference (crystal) oscillator and divider, the noise sources experience the low pass response of the PLL with a gain of 20log(N)dB at frequencies below the loop bandwidth. The divider ratio used in the model is 58.78, which results in the reference/divider phase noise being increased by 20log(58.78) = 35.38dB. This indicates that the input noise power coming from the reference and divider is, at low frequency offset, being referred to the output (due to the low pass behaviour) and amplified by the divider ratio while being suppressed at high offset frequencies.

The VCO noise is one of the main sources of phase noise in the PLL. The PLL output phase noise due to the VCO is equal to the magnitude squared of the transfer function $H_{VCO}(s)$ multiplied by the injected VCO noise. The transfer function from the VCO to the output exhibits a high pass behaviour. This implies that the low frequency VCO noise that lies within the PLL bandwidth can be, to some extent, filtered out. However, for fast variations, the loop is not fast enough and cannot provide much correction [5]. This can be seen in figure 4.1, at frequencies above 1MHz there is little to no impact from the feedback loop, the VCO noise is not being suppressed anymore by the loop.

The third order loop filter used in the model has band pass characteristics. At the

VCO output, the loop filter noise is not very dominant. However it does increase in the region around the loop bandwidth. Additionally, the charge pump noise is also important. It is split up into two parts, one for the pole current and one for the zero current. The model contains charge pump settings which allows the current that is being injected to be configurable. In return, this changes the noise coming from the charge pump. By adjusting these settings, it is possible to control the amount of current coming out of the charge pump which effectively impacts the gain of the charge pump. The current settings also influence the loop gain and therefore also the PLL bandwidth.

In figures 4.4 and 4.5, the model was altered to show the closed loop phase noise contributions from the individual noise sources, as well as the noise transfer functions, towards the VCO input. By sensing at different positions in the loop and redefining a new output, the noise contributors become dominant in different frequency regions.

A very interesting realization is that the phase noise level at the VCO input is significantly lower than that at the output, this is due to the absence of integration coming from the VCO. The gain of the VCO block, $2\pi K_{VCO}/s$, is dropping with frequency. There is a frequency where the gain of the VCO becomes 0dB (hence $2\pi K_{VCO}/s = 0\text{dB}$). This is approximately 60MHz. At low frequencies there is a lot of gain which explains why the levels at the VCO input are in fact so much lower than the ones at the VCO output (seen by comparing the 'Total´ phase noise in figure 4.1 and 4.4).

In figure 4.1 the VCO is not dominating at the low frequencies since it is being suppressed by the loop gain. However, at the VCO input in figure 4.4, the loop tries to compensate the noise coming from the VCO. This explains why it is visible at low frequencies for the input but not the output. This compensation means that it has an opposite phase at the input clarifying why it is not visible at the output, since the feedback loop is trying to suppress the in-band noise it sees at the output of the VCO.

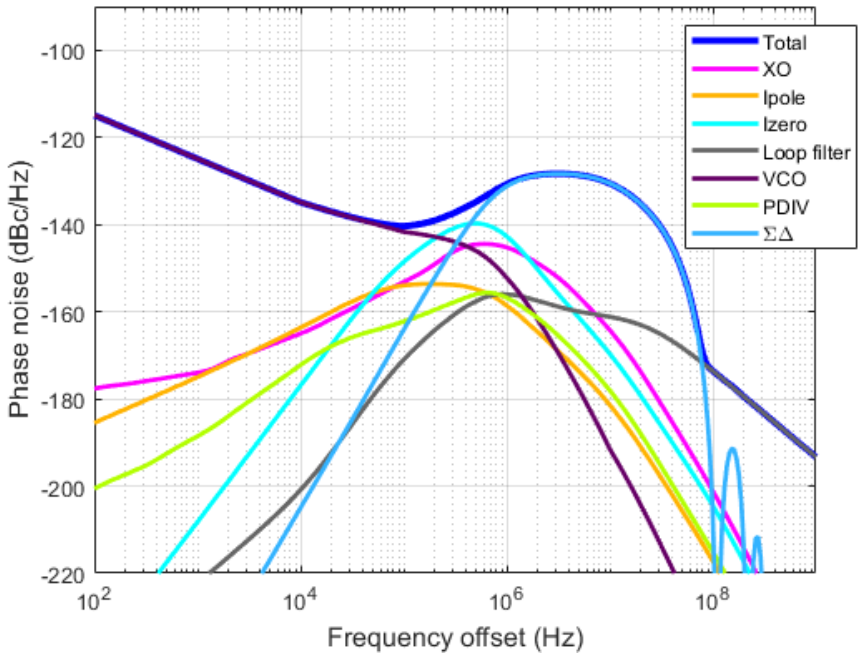


Figure 4.4: Closed loop phase noise profiles seen at the VCO input

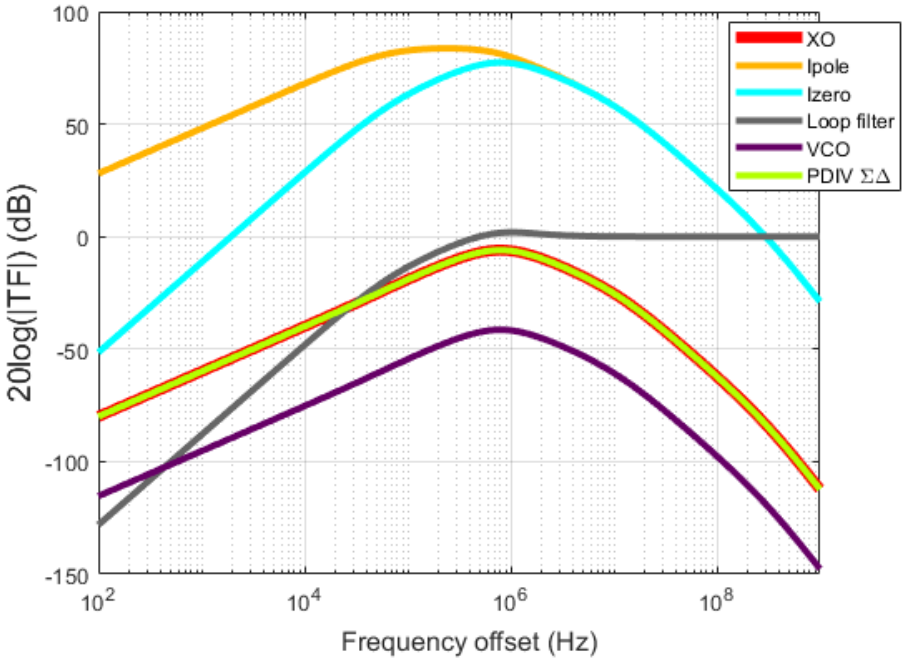


Figure 4.5: Noise transfer functions seen at the VCO input

An important aspect in this whole process was making sure that the model is indeed plausible and the results coincided with what is theoretically expected. Important sanity checks were made to make sure that the results aligned with the expected values. One way of double checking the modeling setup is to open the loop by making the divider ratio extremely large (letting it go to infinity) and by doing so, disabling the feedback loop. In an open loop it is more straightforward to imagine how the noise sources appear at the output. This type of experimentation ensures more confidence that the model is working correctly. At high frequencies the closed and open loops have the same behaviour, because the loop gain becomes very small. Also, in the open loop the phase noise was higher since in a closed loop system the noise gets suppressed. Another method used for checking the model, is to multiply all noise contributions at the VCO input by the gain of the VCO. This should result in the same plot as the VCO output. This type of sanity check is possible for all the noise sources except the VCO noise itself, since it is being suppressed by the feedback loop.

In principle, the $\Sigma\Delta$ modulator can be removed since the analysis can be done at an integer frequency. This was done by simply operating at the closest frequency that allows an integer operation. By eliminating it from the plots, a better overview of the other noise contributors is achieved, the results can be seen in figure 4.6. Going forward, it is assumed that the $\Sigma\Delta$ modulator is disabled.

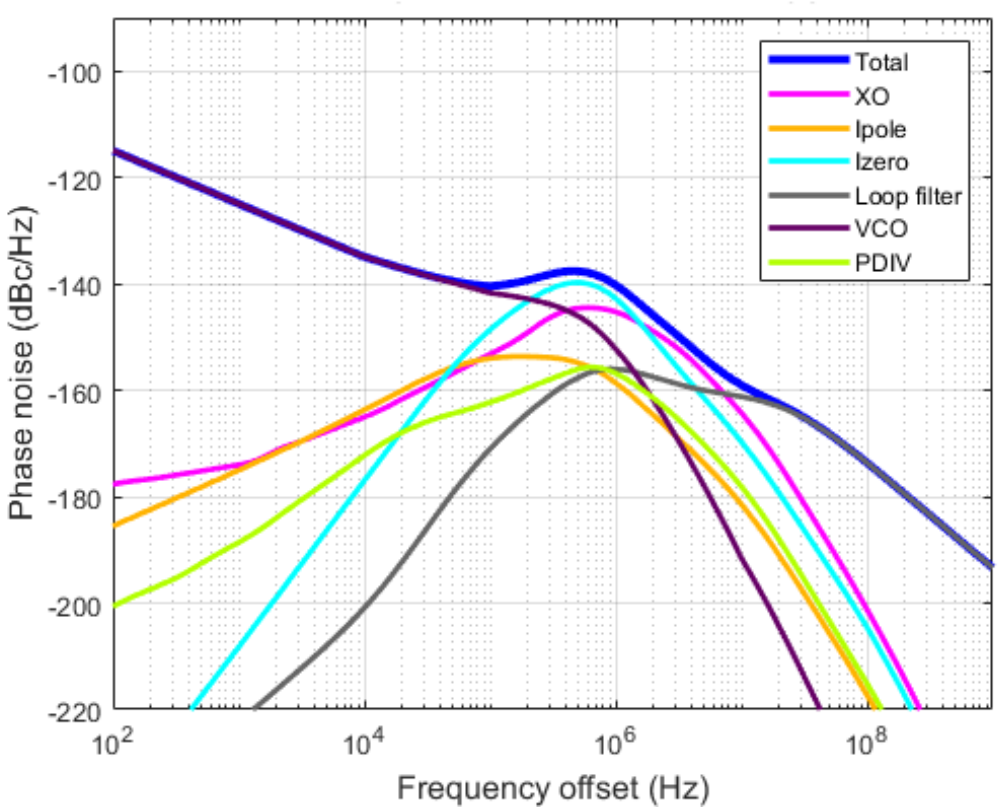


Figure 4.6: Closed loop phase noise profiles seen at the VCO input - Integer mode (without $\Sigma\Delta$ modulator contribution)

4.2 Could the V_{tune} measurement capture the output noise or would crucial contributors be overlooked, impacting the overall measurement?

It is important to analyze which noise sources are dominant in which frequency regions to see if capturing the V_{tune} noise would make sense in such a scenario. For this, the frequency range is split up into three categories: low, mid and high frequencies. This allows for a simpler interpretation of the results. Which noise sources dominate in which frequency range is given in the table below and is seen as a direct interpretation following from figures 4.1 and 4.6.

Frequency Range	at VCO Input	at VCO Ouput
Low : 100Hz-100kHz	VCO	Ipole, XO
Mid : 100kHz-10MHz	Izero, XO	Izero, VCO
High : 10MHz-10GHz	Loop Filter	VCO

Table 4.1: Table showing the noise components dominating in different frequency ranges

From table 4.1 it is visible that only the Izero noise dominates in the same frequency region at the input as well as the output of the VCO. With this information it is possible to indirectly draw conclusions about the Ipole noise, since the two come from the same charge pump. In terms of testability, they will have similar results. A major drawback is that, when looking at the phase noise at the VCO input, the VCO dominates in the low frequency range, however, such a measurement is not desirable since at the output the VCO noise is not dominant in this range. At high frequencies at the VCO input, the

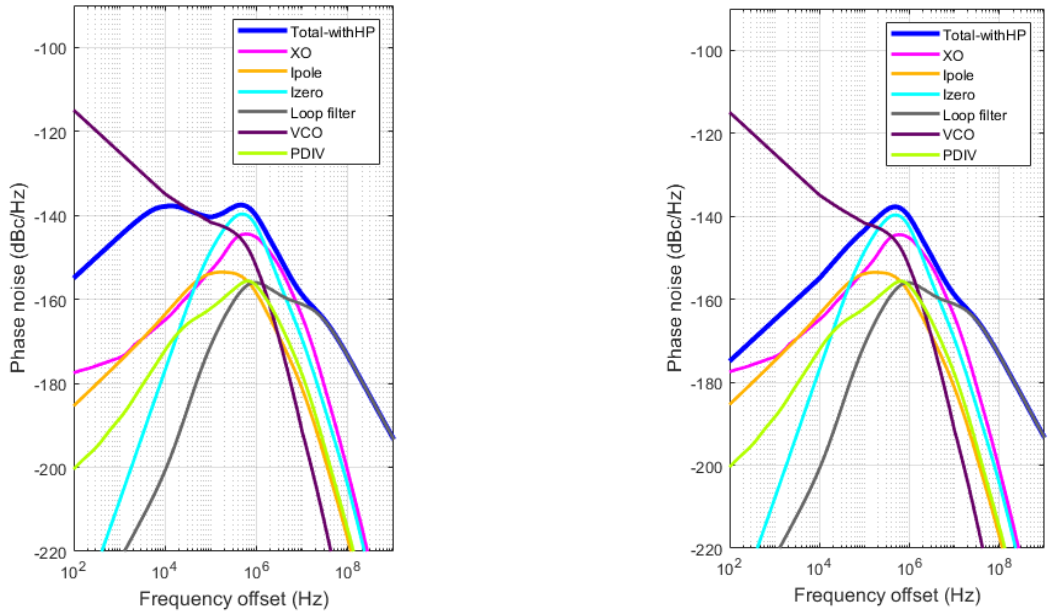
total noise is governed by the loop filter, which occurs because the noise of the loop filter does not get much reshaping (since the noise of the loop filter is simply the thermal noise of its resistors which is shaped by the transfer functions of the resistor itself to the loop filter output). Unfortunately, this does not provide much additional information because the noise coming from the loop filter is fairly predictable already, since it comes from the thermal noise of the resistors.

Additionally, a high pass filter must be integrated in the measurement setup before measuring the total noise, which results in the suppression of the low frequency noise coming from the VCO. This method increases the visibility of the other contributors. Nevertheless, such an approach still does not solve the difficultly of measuring the high frequency VCO noise, as this region would remain unaffected by the high pass filter.

For the model, an ideal first order high pass filter was considered. The cutoff frequencies taken into account were 10kHz and 100kHz, their effects are illustrated in figure 4.7 a) and b) respectively. The value of the cutoff frequency leads to a trade off. In order to measure more of the VCO phase noise, a cutoff of 10kHz is desirable. However, the lower the cutoff frequency, the more time it takes to measure the low frequency components which in return increases the settling time of the measurement. Obviously, it is preferable to reduce test time but the cost would be the loss of information near the cutoff frequency of the filter.

It can be argued that measuring more of the VCO at low frequencies is not of much relevance, since at the VCO output the noise does not dominate in the low frequency region. However, this is not necessarily the case. Seeing how the VCO operates, even at low frequencies at the VCO input, could give information on defects which occur during the manufacturing process of the chip. For example, if the measured VCO noise level is far beyond that what is expected in this frequency range, one can reasonably expect that some defect is present, it can be used as a mean to see if the VCO is working properly. It would be possible to clearly link the defect to the VCO itself, since it is the most

dominant contributor to the overall PLL phase noise in that frequency region.



(a) 10 kHz cutoff frequency

(b) 100 kHz cutoff frequency

Figure 4.7: Closed loop phase noise profiles seen at the VCO input including the high pass filter

It is not enough to look at only the noise sources coming from the PLL components, one has to take into account the quantization noise from the ADC as well as the thermal noise coming from the amplifier. The values of the noise were calculated with the formulas in the previous chapter and the information was added to the phase noise plots for an easier overview, the results can be seen in figure 4.8.

At first an ideal amplifier was considered which generates no noise. This implies that the SNR at the output and input are the same. However in practice this is not the case. In order to model the noise coming form the LNA, an assumption was made which adds a resistor in series such that it produces a noise equivalent with 1kΩ. This results in an equivalent input noise density that is around -168dB/Hz. Generally speaking, increasing the value of the resistor causes the noise level to increase.

The noise coming from the ADC is also modeled as white noise. The noise power was calculated via the formula 3.34 and is around -180dB/Hz. For the ADC noise, as the number of bits increase the noise power decreases. Note that the amplifier noise dominates over the quantization noise coming from the ADC.

It is possible to measure contributions which are around 10dB higher than the noise coming from the amplifier. Information below this flat noise cannot be measured anymore (denoted via the dashed line in figure 4.8). This is a crucial aspect, as this entails that the noise at high frequencies cannot be properly measured because the total noise is dropping with frequency. This information will be lost and cannot be regained via post-processing. In figure 4.8 it can be seen that it is possible to measure until approximately 10MHz, since the total noise is still reasonably above the noise floor. Afterwards the measurement will be drowned out by the noise.

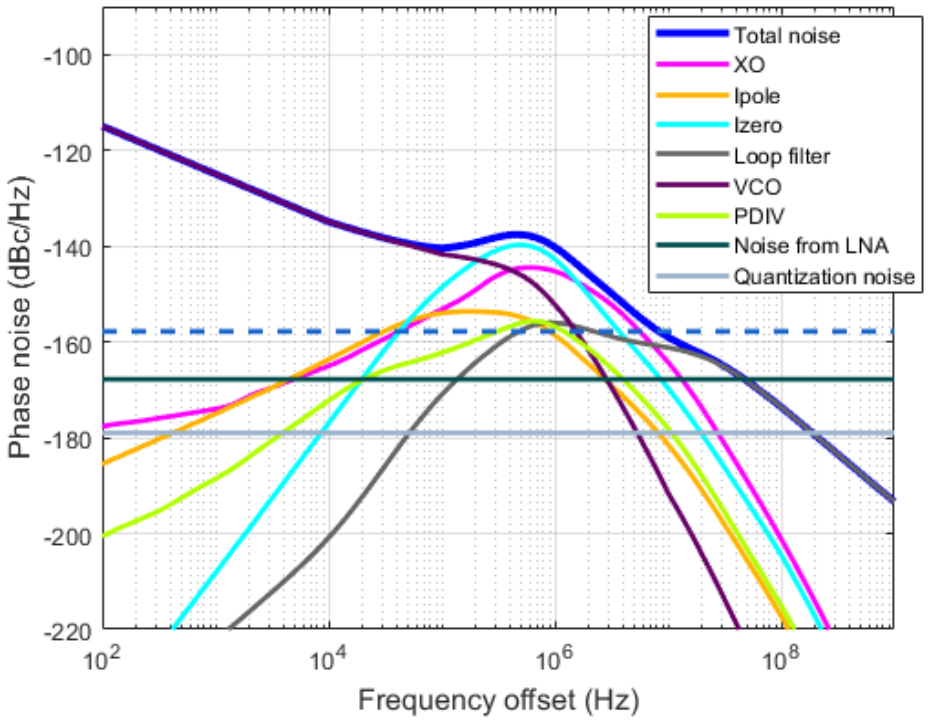


Figure 4.8: Closed loop phase noise profiles seen at the VCO input including ADC and LNA noise densities

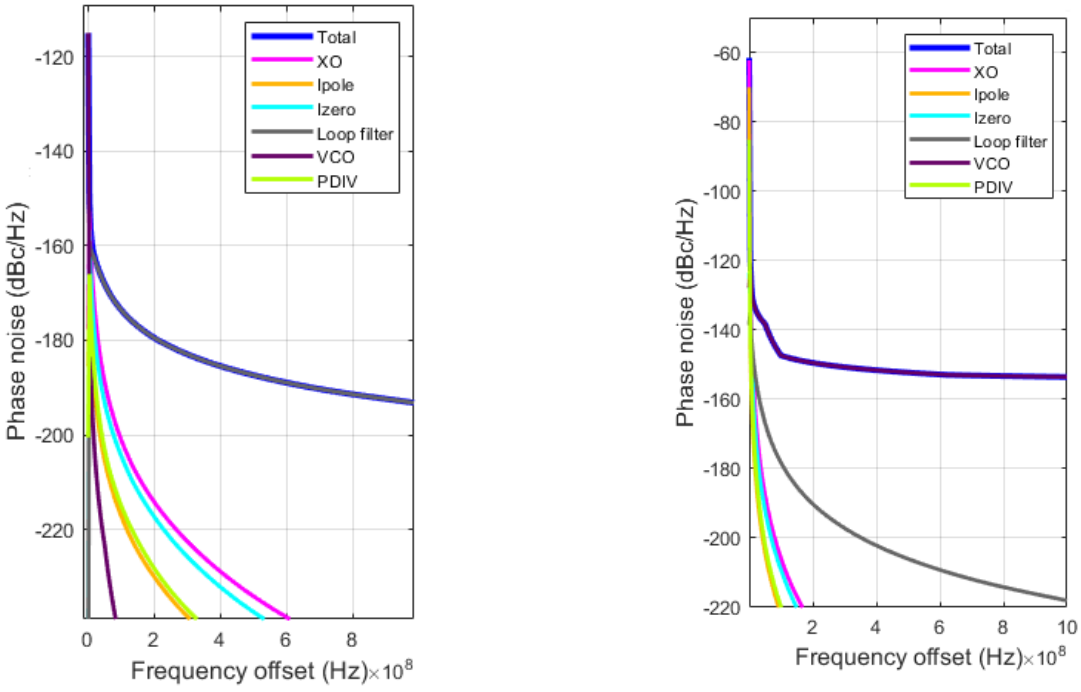
It should be noted that sensing at different points in the loop was also considered. Theoretically, the probe can be placed at any other part in the closed loop system. Obviously, sensing at the output of the VCO would be ideal. However, the output value is a frequency which is extremely high making the measurement demanding. On one hand, this is due to the fact that electronic circuits behave very differently at high frequencies. On the other hand, the equipment used for the measurement cannot support high frequencies and yields inaccurate results. Also, adding a probe at the input of the loop filter was discussed since the high frequency noise is being suppressed by the loop filter. So sensing at the Ipole output and then using a high pass to suppress the low frequency components but passing the high frequencies was also considered as a valid option. While this is plausible in theory and can be modeled by changing the transfer functions, in reality it is not ideal. At the input of the loop filter there are spikes of current coming from the charge pump, measuring this would yield tedious results.

4.3 Proposing parameters for the analog test bus bandwidth, LNA and ADC specifications necessary for a satisfactory measurement

In order to achieve the most accurate measurement possible, the ideal specifications of the analog test bus, LNA and ADC components need to be identified. These parameters should, provided some boundary conditions, yield a satisfactory measurement. To calculate these values, it is necessary to transform the frequency domain phase noise signal into the time domain, which can be done via the help of the Inverse Fast Fourier Transform (IFFT).

The VCO control voltage, V_{tune}, is a DC voltage in the range of 400 - 750 mV. The signal being sensed at the probe is the V_{tune} with a noise being superimposed on it. As discussed previously, a high pass filter needs to be placed before the amplifier, not only to suppress the VCO noise at low frequencies, but also to filter out the DC component and leave only the noise behind. Removing the high pass filter limits the amount of amplification which can be done to the signal.

The first step of converting the spectrum into a time domain plot involves changing the axis. To correctly apply the IFFT in MATLAB, the logarithmic axis needs to be transformed into a linear one, such that all samples are equally spaced. Figure 4.9 a) and b) illustrate the closed loop phase noise profile, seen at the VCO input and output, on a linear scale respectively. From these figures the 'skirts' that the phase noise creates in the frequency domain (as discussed in chapter 2) can be seen. This is because the x-axis is extremely compressed on the left side. The model contains a SSB phase noise around the fundamental frequency, to get the DSB the results simply need to be mirrored. Changing the axis also yields a different perspective. In the logarithmic plot, it seems as though the high frequencies are more compressed and that there is not much energy present in this region. However on the linear scale it can be seen that this is in fact not that case.



(a) Noise seen at VCO Input

(b) Noise seen at VCO output

Figure 4.9: Closed loop phase noise profile on a linear scale

The Fourier Transform takes a continuous time domain signal and transforms it to the frequency domain. Similarly, the Discrete Fourier Transform (DFT) is a linear transform which takes as an input a discrete time complex signal with N data points and gives as an output the corresponding complex signal in the frequency domain with the same length. The Fast Fourier Transform (FFT) is a collection of algorithms which allows the DFT to be computed in a fast and computationally efficient manner. The computational complexity it takes to perform a DFT is equal to $O(N^2)$, on the other hand performing a FFT takes only $O(NlogN)$ operations, which is the main reason why FFTs are used to compute DFTs. The formula for the conversion from time to the frequency domain is is given by:

$$X[k] \triangleq \sum_{n=0}^{N-1} x[n] e^{-j\frac{2\pi}{N}kn} \tag{4.1}$$

where $x[n]$ is the discrete-time input signal, N is the number of samples, n represents the current sample and k is the current frequency where $k \in [0, N-1]$. The output of the transform, $X[k]$, is a sequence of N coefficients which are generally complex numbers and include information of both amplitude and phase.

IFFT is the inverse operation to the FFT that renders the time response of a signal given its complex spectrum and is mathematically represented via the following equation:

$$x[n] \triangleq \frac{1}{N} \sum_{k=0}^{N-1} X[k] e^{j\frac{2\pi}{N}kn} \tag{4.2}$$

MATLAB contains functions and packages which perform the FFT/IFFT transformations. In order to correctly apply the functions, the data first needs to be prepared appropriately. The reconstruction of the original signal from the frequency domain requires the knowledge of both the amplitude and the phase information of the samples. If all of this information is known, the signal can be perfectly represented both in the time and frequency domain. However, in the model only the amplitude information is present, therefore it is no longer possible to uniquely reconstruct the original signal. This is because the data provided for the model only relies on the magnitude information to plot the phase noise, no additional phase information is given. Instead, it is necessary to include random phases for each data point ranging from 0 to 2π. It should be noted that, due to this random phase addition, the original waveform and the reconstructed one are not a one-to-one match. The reason being, that there are many signals which fulfill the same spectral plot if the phase information is unknown.

The steps which were necessary to perform an appropriate transformation were:

- the first component of the FFT is the DC component. Since the DC component is of no interest in this particular case (only the noise is of use), it needs to be

removed from the calculation

- applying the IFFT function in MATLAB requires the entire double-sided spectrum which means that the spectrum in figure 4.9) a) needs to be mirrored
- afterwards the random phases were applied to half of the samples in the spectrum by multiplying each data point by $e^{(1j\theta)}$, here θ takes on uniformly distributed random values from the interval [0;2π]. The remaining half need to be chosen such that the data points of the frequency domain signal (the input to the IFFT) are conjugate symmetric. This means that the remaining half are chosen as negative conjugates of the first half of random phases.

Fourier theory relies on the assumption that any continuous periodic signal can be represented as the sum of properly chosen sinusoidal waves in the time domain. This implies that the IFFT calculates for each point in the spectrum equivalent points in the time domain. Each frequency point is an equivalent sine wave with a random phase, the amplitude of the sine wave is the amount of energy per unit of bandwidth present. The waves are then added together to form the total signal.

In an attempt to check the results, Parseval's theorem was used. It states that the energy of a signal in the time domain equals the energy of the transformed signal in the frequency domain. This implies that the energy of the signal is preserved when using the DFTs/FFTs. Mathematically, Parseval's theorem is stated as:

$$\sum_{n=0}^{N-1} |x[n]|^2 = \frac{1}{N} \sum_{k=0}^{N-1} |X[k]|^2 \tag{4.3}$$

The theorem itself can be proven easily by using equation 4.1 for the FFT.

$$\begin{aligned} &\frac{1}{N} \sum_{k=0}^{N-1} |X[k]|^2 = \frac{1}{N} \sum_{k=0}^{N-1} X[k]X^*[k] = \frac{1}{N} \sum_{k=0}^{N-1} \left[\sum_{n=0}^{N-1} x[n] \exp\left(-j\frac{2\pi}{N}kn\right) \right] X^*[k] = \\ &\frac{1}{N} \sum_{n=0}^{N-1} x[n] \left[\sum_{k=0}^{N-1} X^*[k] \exp\left(-j\frac{2\pi}{N}kn\right) \right] = \frac{1}{N} \sum_{n=0}^{N-1} x[n] \left(Nx^*[n]\right) = \sum_{n=0}^{N-1} |x[n]|^2 \end{aligned} \tag{4.4}$$

Once the signal is reconstructed in the time domain, the worst case scenario needs to be modeled. This is achieved by looping over the function numerous times and finding the results for the 'worst case'. An example of the modeled noise is given in figure 4.10. The noise itself is quite small, in the range of 10^{-4}-10^{-5}V. The goal of the amplifier is to amplify the signal such that it fits into the FSR of the ADC.

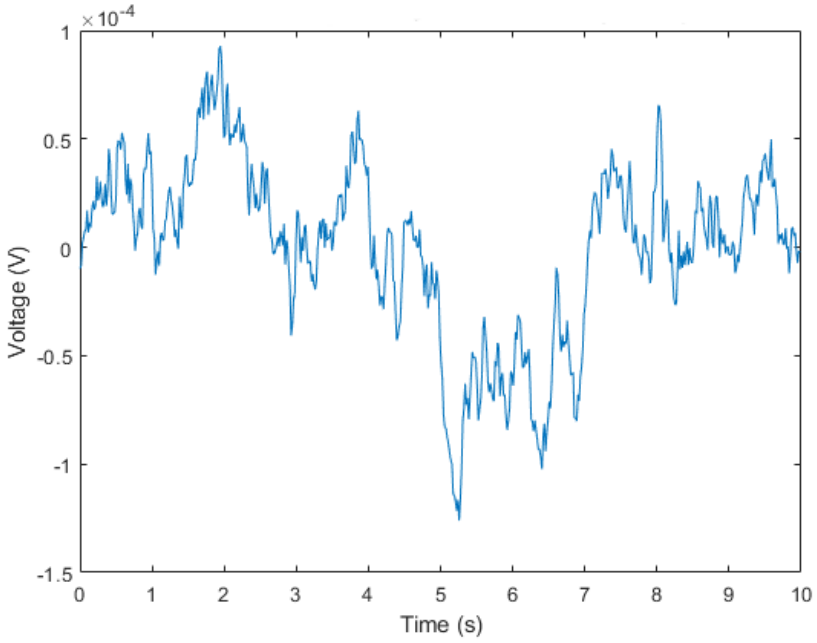


Figure 4.10: Time domain signal reconstructed from the spectral plot

The simulations in the MATLAB model describe the typical performance of the PLL. However, it is necessary to measure the PLL performance at a point where it is not fulfilling the specification anymore. The question then becomes, what is the necessary amplification such that even in the worst case scenario, the signal stays within the range of what the ADC can quantify? To reach the full ADC range with the worst acceptable noise, a margin needs to be considered for the amplification input, it must be a factor of 2 smaller than the full scale amplification as to ensure reasonable results. If the margin is taken into account, the gain will be smaller since the noise from the PLL is worse, considering it is undesirable to saturate the ADC with the maximum noise possible.

There are other reasons why this margin is necessary, one of them being that the loop filter dominates at high frequencies at the VCO input. The noise of the loop filter is predictable, it is mostly the thermal noise of the two resistors, this implies that measuring at cold and hot temperatures will result in different levels of noise. Due to this, it is important to back off on the gain of the amplifier to ensure proper results for different environmental settings.

Subsequently, the ADC needs to be added to the model. The function used to model the ADC takes as an input the amplified signal and the number of bits and produces at the output the quantized signal according to the formulas mentioned in chapter 3. The input range of the ADC is $+/-0.675$V. The model also calculates the quantization error. The signal should be 20dB higher than the noise, this means that a 5 bit ADC should be used and the gain of the amplifier needs to be 2238dB. While the gain of the amplifier is very large, it is possible to reduce it by increasing the number of bits, this will be thoroughly explained during the next research question. Figure 4.11 shows the amplified signal, the quantized version and the quantization error.

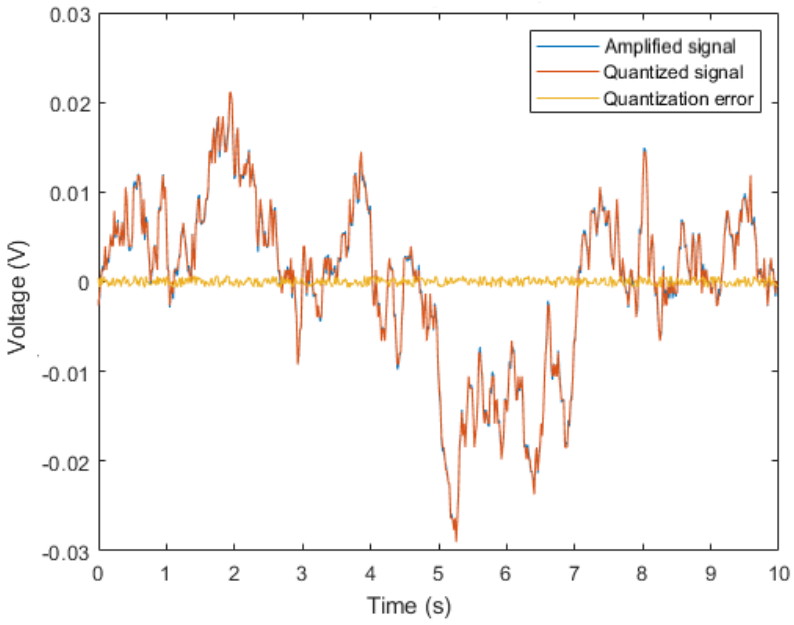


Figure 4.11: Signal being quantizated by ADC including quantization error

Lastly, the bandwidth of the analog test bus needs to be considered. It is important to note that the LNA should be placed closely to the PLL itself, as to prevent the interconnect from adding a non-negligible contribution to the 1kΩ noise from the LNA. The analog test bus is modeled as an additional series RC, acting as a parasitic low pass. For the time being, it is assumed that there is a direct path for the analog test bus, later on a distributed model will be taken into account. The resistor itself will add some noise, however the LNA will ensure that it does not contribute significantly to the overall total noise. The recommended values of the first order RC model are based on what can be reasonably measured at the input of the VCO. It was mentioned previously, that due to the noise coming from the LNA and ADC, the measurement of the high frequencies would be buried in noise. Realistically, it is possible to measure up to a frequency of 10MHz. In order to retain the small portion of the phase noise measurement at high frequencies, the cutoff frequency of the analog test bus should be chosen such that it is beyond 10MHz. Assuming values of R= 2kΩ and C=1pF, gives a cutoff frequency of $1/(2\pi RC)$=80MHz, which is beyond what can be measured and is therefore ideal in such a case. Figure 4.12 shows what the total noise at the input of the VCO would look like, including the high pass and low pass filters.

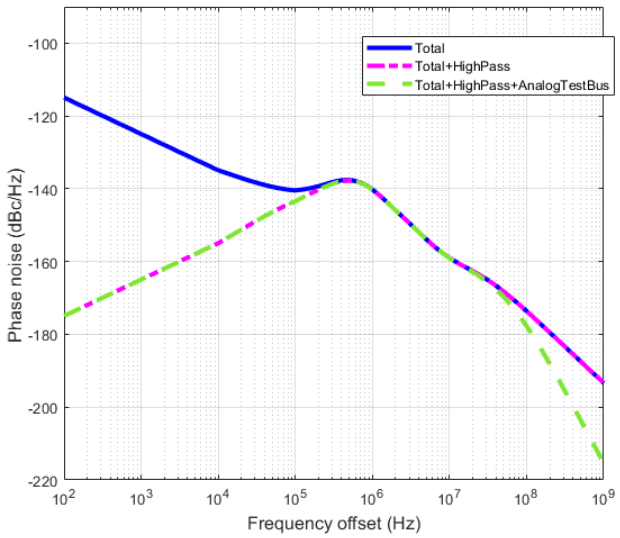


Figure 4.12: Total noise at the VCO input including high pass and low pass

4.4 Which parameters (non-idealities) would limit the accuracy of such a noise measurement?

There are multiple parameters that limit the precision of such a phase noise measurement. The ones discussed in more detail here are the gain of the LNA and the number of bits used for the ADC. Additionally, a distributed analog test bus scheme will be considered to make the model more realistic, as the parasitics along the test bus are by nature distributed along its length.

Figure 4.10 shows that the noise voltage in the time domain is quite small. The goal of the amplifier is to scale the input signal level to fit into the input voltage range of the ADC. The input voltage range is also known as the full scale range and spans from -$Vref$ to $Vref$. If the signal is larger than the voltage range of the ADC, then a saturation error occurs. Which means that for all values beyond $Vref$, the ADC returns the maximum value. Therefore, the analog signal at the input should span as much of the ADC input voltage range as possible, without saturating the ADC, because this causes an increase of the signal to noise ratio [24]. It should be noted that this is one reason why the margin was added to the LNA, as to not saturate the ADC with the maximum noise coming form the PLL. Similarly, if the voltage of input signal is significantly smaller than the FSR of the ADC, the signal should be amplified before entering the ADC input. Theoretically, the analog input should be scaled such that the peak voltage $Vp = Vref$, which would in return maximize the signal to noise ratio. This scenario is illustrated in figure 4.13.

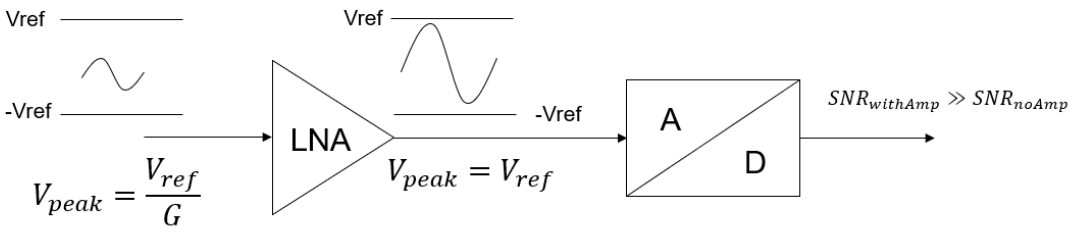


Figure 4.13: Amplifying signal to FSR of ADC

Unfortunately, the SNR at the output of figure 4.13 is not the maximum possible SNR, since the amplifier itself adds noise (as seen in the previous results). However, if the noise of the amplifier is kept relatively small, the SNR with the amplifier will still be larger than the SNR for the case where the input signal does not reach FSR of the ADC [25].

The number of bits in an ADC defines how large the voltage steps are which quantize the analog input. By increasing the number of bits, the resolution increases and the step size is decreased which leads to a more exact representation of the input signal.

An insightful observation is that by increasing the number of bits used for the ADC the gain of the LNA can be lowered proportionally. This would make the high gain of the amplifier less demanding. Assuming then that a 10-bit ADC is being used (instead of the 6-bit one), the gain of the amplifier can be lowered by $G/2^4$, since only the lower 4 bits are being used, which results in a gain of 140dB.

Another aspect which needs to be considered is that, in reality the analog test bus acts more like a distributed network rather than a first order series RC (which is seen in figure 4.14). For the distributed model the resistors and capacitors are split up into equal values. An example of what this looks like can be seen in figure 4.15.

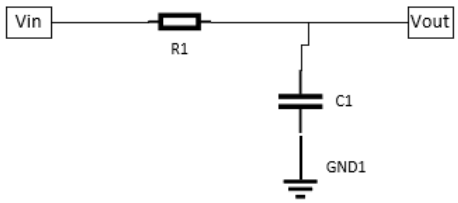


Figure 4.14: Simple analog test bus

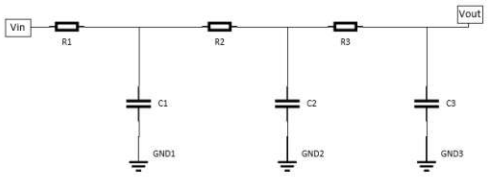


Figure 4.15: Distributed analog test bus with 3 stages

In figure 4.16, a resistor of 2kΩ and a capacitor of 1pF were used. For each stage, the resistor and capacitor were split into equal parts accordingly. As the number of stages increase, the more the low pass filter behaves like an ideal low pass filter (rectangular

pulse). After the cutoff, the steep decline between each stage is reduced by -20dB per decade. Although the cut off frequency does not change between the different stages, the more distributed the circuit is, the more bandwidth there is (as opposed to using a simple RC circuit). Generally speaking, the higher the resistance, the lower the capacitance because the interconnect lines inside the ICs are thinner. If they are thinner there is less lateral parasitic capacitance with the rest of the circuit. The conclusion is that a distributed scheme would be more realistic as opposed to using a first order low pass filter. However, it does make the calculations more complex and since it was shown that the measurement at high frequencies is buried in noise anyway, a more simplistic representation is sufficient to approximate the results.

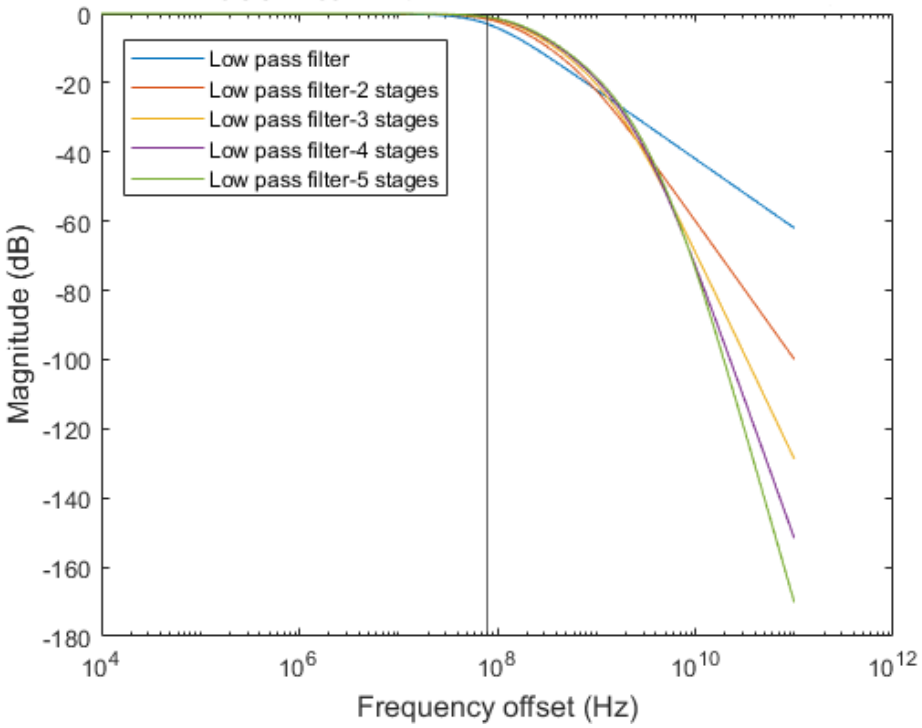


Figure 4.16: First order RC model vs distributed model

According to all these results which were collected in this chapter, the final setup considered for the BIST can be seen in figure 4.17.

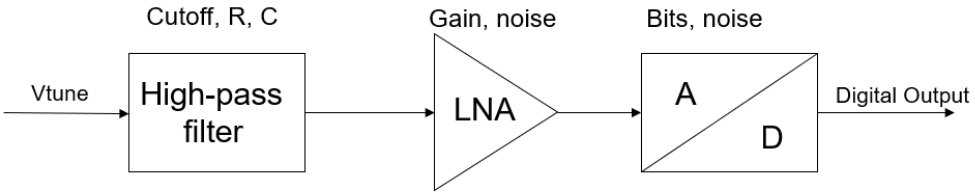


Figure 4.17: BIST setup

The following specification values are proposed for the LNA, ADC and analog test bus parameters:

- LNA gain: 140dB
- LNA noise contribution: -168dB/Hz
- ADC number of bit: 10 bits
- ADC noise contribution: -179dB/Hz
- High pass cutoff frequency: f_{cutoff}= 10kHz
- Low pass cutoff frequency: R= 2kΩ, C=1pF, f_{cutoff} frequency = 80MHz

The conclusion of results are described in the following chapter.

CHAPTER 5

Conclusion

To summarize, the BIST measurement was taken on the control voltage of the VCO, namely the V_{tune}, to measure the phase noise in a PLL. The high pass filter then separated the noise from the DC component, the LNA amplified this noise to fit into the FSR of the ADC and lastly the ADC saved this information in digital form. The information in question would then be digitally post processed for further analysis.

This BIST concept considerably eases the testing of phase noise in a PLL. Allowing the PLL to perform self-testing eliminates the use of additional ATE and significantly reduces test costs in the long run while additionally decreasing the testing time. Although this concept is feasible in theory, it also comes with its drawbacks, since it leads to a loss of certain measurement data. Some of this specific information cannot be reconstructed anymore at a later time and it is considered to be permanently lost. This is the main downside of using this technique. Figure 5.1 shows the entire BIST scheme necessary to perform such a measurement.

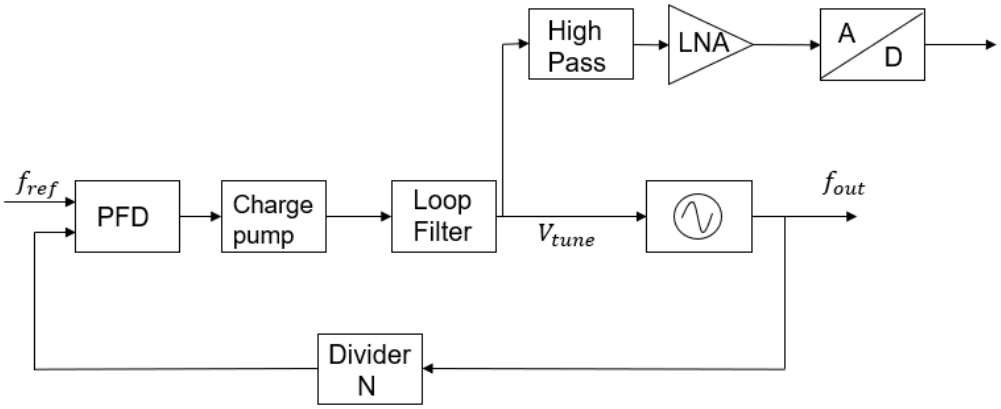


Figure 5.1: Final setup for BIST phase noise measurement

In conclusion, it was shown that a direct measurement of the mid-frequency range was the most plausible, since only this frequency region remained completely unaffected by the components in the setup. From 100kHz to 10MHz, the dominating components which contributed to the overall phase noise of the PLL were the I_{zero} noise coming from the CP as well as the reference noise from the oscillator. This indicated that the model was a good mean to measure the phase noise in the mid-frequency range, as it provided information concerning the the CP noise and the oscillator noise.

Additionally, the low frequencies which were suppressed by the high pass filter could be recovered to some extent via digital post processing. Obviously, the choice of the cutoff value of the high pass filter directly influenced the measurement. Smaller cutoff values measured more of the VCO noise at low frequencies, however it also increased the settling time of the measurement. This was a direct trade-off which needed to be taken into account. Two cutoff values were considered in this work, namely 10kHz and 100kHz.

Furthermore, it was shown that the high frequency components were not visible in such a BIST measurement and this was the biggest limitation found in this thesis. The noise coming from the LNA and ADC drowned out the high frequency phase noise contribution from the PLL. A measurement up until approximately 10MHz was considered

plausible, since the total noise at this frequency was still reasonably above the noise coming from the LNA. The measurement that proceeded after 10MHz was drowned out by the noise produced from the LNA and ADC. Nevertheless, such a BIST technique has proven to carry more advantages than disadvantages and its further development is the key to modern successful testing of electronic circuits.

Phase noise is only one specification parameter which is crucial for the overall proper functionality of PLLs. This proposed BIST could be the springboard to similar techniques used to test other parameters. Such parameters would include lock time, reference spurious levels, etc. This concept could widely improve the testability of PLLs in general, resulting in better functionality and improved customer satisfaction.

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List of Algorithms

Acronyms

ADC Analog to digital converter. xii, 3, 4, 5, 27, 32, 36, 37, 38, 39, 40, 41, 43, 44, 54, 55, 57, 59, 61, 62, 63, 64, 65, 67, 69, 70, 71, 73, 74

ATE Automated test equipment. 7, 9, 69

BIST Built-In self-test. 1, 3, 4, 5, 9, 10, 27, 33, 36, 45, 66, 67, 69, 70, 71, 73, 74

CMOS Complementary metal-oxide-semiconductor. 3

CP Charge pump. 12, 14, 15, 16, 30, 70, 73

DC Direct current. 2, 12, 16, 40, 57, 59

DfT Design for testability. 1, 9

DFT Discrete Fourier Transform. 58, 60

DSB Double-sideband. 23, 57

FFT Fast Fourier Transform. 58, 59, 60

FSR Full scale range. 32, 40, 61, 64, 65, 69, 74

FT Final test. 2, 3, 7, 9

ICs Integrated circuits. 1, 2, 7, 8, 9, 66, 73

IF Intermediate frequency. 24, 25

IFFT Inverse Fast Fourier Transform. 57, 59, 60

LF Loop filter. 12, 15, 16, 17, 18, 20, 21, 30

LNA Low noise amplifier. xii, 3, 4, 5, 32, 33, 35, 36, 40, 54, 55, 57, 59, 61, 63, 64, 65, 67, 69, 70, 71, 73, 74

LO Local oscillator. 24, 25

LSB Least Significant Bit. 39

PFD Phase frequency detector. 12, 13, 14, 15, 19, 20, 21, 30, 73

PLL Phase lock loop. xii, 2, 3, 4, 5, 9, 10, 11, 12, 14, 15, 16, 17, 18, 19, 20, 21, 22, 27, 28, 29, 30, 45, 47, 48, 49, 51, 54, 61, 63, 64, 69, 70, 71, 73

RC Resistor-Capacitor. 17, 63, 65, 66, 74

RF Radio frequency. 2, 3, 17

RMS Root mean square. 30, 32, 40

SNR Signal-to-noise ratio. 33, 34, 54, 65

SQNR Signal-to-quantization-noise ratio. 43, 44

SSB Single-sideband. 23, 57

UWB Ultra-wideband. 3

VCO Voltage controlled oscillator. xii, 3, 4, 10, 11, 12, 13, 15, 16, 18, 19, 20, 21, 22, 27, 28, 29, 30, 31, 32, 36, 45, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 62, 63, 69, 70, 74

WT Wafer test. 2, 7, 9

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