DISSERTATION

High-κ/metal-gate devices for future CMOS technology

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I declare in the lieu of oath that I did this dissertation in hand by myself using only literature cited at the end of this volume.

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Abstract

For almost forty years technological progress and economic benefit drives the scaling of CMOS-technology. The use of silicon dioxide as the gate dielectric on one hand, and highly-doped poly-silicon as the gate electrode on the other hand, offers several simplifications in processing, while maintaining excellent device characteristics. However, the continuative scaling by using this material combination leads to quantum-mechanical effects that result in dramatically increased gate leakage currents. By the implementation of new materials with a high dielectric constant – if necessary in combination with metal-gate electrodes instead of poly-silicon electrodes – this problem can be preliminary solved and ongoing scaling of CMOS-devices can be enabled.

The present work addresses the investigation of high-κ dielectrics and their applicability in CMOS-devices, using metal-gate electrodes. The contents firstly include the deposition of zirconium dioxide and hafnium dioxide from the gas phase, using organometallic precursors, and their physico-chemical characterization. In the following, MOS-capacitors are fabricated by the selective deposition of gate electrodes made from aluminium, molybdenum, nickel, or titanium-nitride, and characterized regarding their electrical behaviour. Furthermore, these material systems are investigated regarding their thermodynamical stability.

Results within this work demonstrate that well balanced and correctly applied annealing of the devices clearly improves electrical behaviour. However, the processed oxides do not exhibit the necessary thermodynamical stability in contact with silicon, which limits the achievable "electrical thickness". Nickel, molybdenum, and titanium-nitride behave as mid-gap metals regarding to silicon. We attribute these metals high potential to be applied in near-future CMOS-technology, if doped with the proper nitrogen content, or implemented as silicides.

Kurzfassung

Seit beinahe vierzig Jahren treiben technologischer Fortschritt und wirtschaftlicher Nutzen die Skalierung der CMOS-Technologie voran. Die Verwendung von Siliziumdioxid als Gate-Dielektrikum einerseits, und von hochdotiertem Polysilizium als Gate-Elektrode andererseits, spielt hierbei eine zentrale Rolle, und ermöglichte prozesstechnische Vereinfachungen unter Beibehaltung hervorragender Bauelementeigenschaften. Allerdings führt die fortschreitende Skalierung unter Verwendung dieser Materialkombination zu quantenmechanischen Effekten, die sich in einem dramatischen Anstieg der Gateleckströme bemerkbar machen. Durch die Einführung neuer Materialien mit hoher Dielektrizitätskonstante – gegebenenfalls in Kombination mit metallischen Elektroden anstelle von Polysilizium Elektroden – kann dieses Problem vorerst behoben, und so eine weitere Skalierung der CMOS-Bauelemente ermöglicht werden.

Die vorliegende Arbeit beschäftigt sich mit der Herstellung und Charakterisierung hochpermittiver Dielektrika, und deren Einsetzbarkeit in CMOS-Bauelementen unter Verwendung metallischer Elektroden. Der Inhalt umfasst zunächst die Abscheidung von Zirkonium-, und Hafniumdioxid aus der Gasphase, unter Verwendung von metallorganischen Vorläufersubstanzen, und deren physikalisch-chemischer Charakterisierung. Des Weiteren werden, durch das gezielte Aufbringen von Gate-Elektroden aus Aluminium, Molybdän, Nickel oder Titan-Nitrid, MOS-Kondensatoren erzeugt und bezüglich ihrer elektrischen Eigenschaften charakterisiert. Darüber hinaus werden diese Materialsysteme bezüglich ihrer thermodynamischen Stabilität untersucht.

Die erbrachten Ergebnisse zeigen, dass gut abgestimmte, und richtig angewandte thermische Nachbehandlung der Bauelemente, zu eindeutig verbesserten elektrischen Eigenschaften führt. Dennoch zeigen die prozessierten Oxide keine ausreichende Stabilität in Kontakt mit Silizium, was

die erreichbare 'elektrische Dicke' limitiert. Nickel, Molybdän und Titan-Nitrid zeigen "Mid-gap"-Verhalten in Bezug auf Silizium. Diesen Materialien – wenn entsprechen mit Stickstoff dotiert, oder als Silizid ausgeführt – schreiben wir gute Aussichten zu, in der nahen Zukunft in der CMOS-Technologie Anwendung zu finden.

"High-κ/metal-gate devices for future CMOS technology"

PART I: INTRODUCTION

PART II: FUNDAMENTALS

PART III: EXPERIMENTAL WORK

PART IV: RESULTS AND DISCUSSION

PART V: REFERENCES AND APPENDIX

PART I: INTRODUCTION

According to the Semiconductor Industry Association (SIA), worldwide sales of semiconductors set a new record at $227.5 billion in 2005. From 1960 to 2003 the world market for semiconductors grew about 14 percent per year. This enormous increase is mainly due to the technological advance of microtechnology, a successful progress that is based on the systematically investigation of the material-, physical-, and chemical properties of silicon - the most important and universal semiconductor - and its processing abilities.

I.1 From Micro- to Nanotechnology

It is no great surprise that government-financed Research & Development (R&D) institutions, as well as market-oriented companies change their prefix from “micro” to “nano”. Now that the semiconductor industry scales the key dimensions of its functional components into regions where they are already partially quantum-mechanical controlled, the era of *microelectronics* passes into an era of *nanoelectronics*.

The remarkable success of the worldwide semiconductor industry principally results from its ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. This lead to principal categories of improvement trends that are shown in table 1.A, with examples of each [1]. Of course, the most famous trend listed below is “integration level”, which is usually cited as *Moore’s Law* formulated by Intel co-founder Gordon Moore in 1965. It predicts the number of components per chip to be doubled every 24 months. An important step for carrying this issue into the 21st century was the implementation of Complementary Metal-Oxide-Semiconductor (CMOS) technology.

However, we have reached a point where planar bulk CMOS faces grand challenges, and to overcome these, invention of new processes, materials, or even completely new device concepts are indispensable.

Table I.A: Improvement trends for ICs enabled by minimal feature scaling.

Trend	Example
Integration level	Components/chip, Moore’s Law
Speed	Microprocessor clock rate, GHz
Power	Laptop or cell phone battery life
Compactness	Small and light-weight products
Functionality	Non-volatile memory, imager
Cost	Cost per function

I.2 Motivation of this work

The *International Roadmap for Semiconductors* (ITRS) in its 2005 Edition classifies the reduction of Equivalent Oxide Thickness (EOT) as the most difficult challenge associated with future device scaling [1]. The gate stack system silicon (Si)/ silicon dioxide (SiO_2)/polysilicon (poly-Si) has for a long time successfully played the key role in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) technology, and its era has continued with silicon oxynitride (SION) as the gate dielectric. Nevertheless, the strong leakage restrictions in low-power applications will make the introduction of a higher dielectric constant (high-κ) material, in which the tunneling current can be suppressed while maintaining the drain current, necessary.

The implementation of such a new class of gate oxides additionally necessitates the introduction of metal gate electrodes. On one hand, this will avoid polysilicon depletion which becomes significant in the use of polysilicon gate electrodes and ads to the equivalent oxide thickness, while on the other hand it prevents boron in-diffusion and lowers the gate resistance. Therefore, metal gate materials that offer an appropriate work function - either as mid-gap metal for both, p-, and n-bulk MOSFETs, or in dual-work-function-gate technology - have to be found.

These material changes address key steps to be taken in future MOSFET-technology, and such new high-κ and metal gate stacks are expected to be fundamental structures used within future CMOS devices, such as fully-depleted Silicon On Insulator (SOI) devices, or multi-gate MOSFETs. These issues attracted immense interest within the worldwide semiconductor-R&D-community during the last years and also bear the motivation of this work.

I.3 Objectives of this work

This work is partially supported by the *Network of Excellence SINANO* (Silicon-based Nanodevices), which is funded by the *European Commission* under the *6th Framework Programme,* and topically embedded within workpackage 2:*'Non-classical nano-MOSFET architectures'*. The main objective of this workpackage is to study the scientific challenges related to the fabrication and characterisation of experimental SOI, SON and double-gate (e.g.: FinFET, GAA) ultimate MOS devices that show performances and technological achievements as required by the ITRS roadmap beyond the 45 nm node, i.e. the end of this decade [2].

This work addresses the investigation of new metal gate/high-κ dielectric/silicon stacks that fulfil the requirements for future device-technology. The contents herein include the complete area of interest, from the fabrication of various MOS-capacitors, via their physical-chemical and electrical characterization, to the investigation of their thermodynamical behaviour.

This thesis is structured into 5 parts: Part I very generally introduces the topic, by giving information about background and motivation. Part II contains all fundamentals that to the author appear necessary to seriously discuss the given topic. The content of this part is based on established and actual literature. In part III, the experimental work performed within the duration of this thesis is described successively. All obtained results and their scientific discussion is presented in part IV. Finally, part V closes with references and appendix.

PART II: FUNDAMENTALS

II.1 Current CMOS (Complementary MOSFET) technology

The CMOS (Complementary MOSFET) technology, which employs both n-MOS and p-MOS to form logic elements, was proposed by Wanlass and Saw [3] in 1963. Its advantage is that the logic elements draw significant current only during the transition from one state to another, offering power consumption to be minimized. Since the early 1980s, silicon-gate CMOS is the dominant technology for Very/Ultra Large Scale Integration (VLSI/ULSI) designs [4,5]. Figure II.1 shows a cross-sectional view of a "state-of-the-art" CMOS device. More details on the applied materials are presented in chapters II.2.1 and II.2.2.

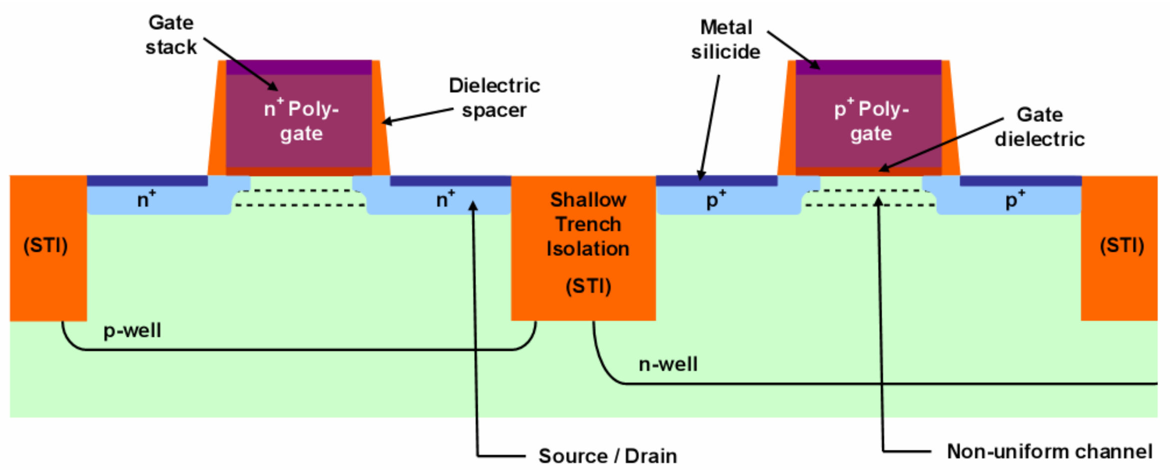

Figure II.1: Cross-sectional schematic view of a "state-of-the-art" CMOS device, showing n-, and p-MOSFETs, separated by shallow trench isolation. Lightly doped source and drain are indicated (adapted from Wong et al. [18]).

II.1.1 Basic MOS semiconductor fabrication processes

This chapter summarizes the basic processing steps that are widespread in MOS fabrication, whereas it mainly follows the textbook by Allen and Holberg [6]. In a separately discussed paragraph, a common n-well silicon-gate CMOS process will be described in detail.

All CMOS processing starts with single-crystal silicon material, which is mainly grown by the “Czochralski-method”, named after its developer Jan Czochralski. A second method, the so-called “float zone technique”, produces crystals of high purity, and is often used for power devices. The crystals are usually grown in either a ⟨100⟩- or a ⟨111⟩ crystal orientation, and are then doped with n-type or p-type impurities to form an n- or a p-substrate, respectively.

The five basic processing steps applied to the doped silicon wafer to fabricate semiconductor components are oxidation, diffusion, ion implantation, deposition, and etching, and will be described in the following paragraphs.

A) Oxidation

“Oxidation” is the first basic processing step, during which a layer of SiO_2 is formed on the surface of the silicon wafer. Thereby, the oxide grows into, as well as out of the silicon surface. Typically about 56 % of the oxide thickness are above the original surface, while about 44 % are below. There are two main techniques applied, “dry“, or “wet oxidation”, which take place at temperatures ranging from 700 °C to 1100 °C, with the resulting oxide thickness proportional to the growth-temperature and the growth-time. The grown oxide thickness t_{ox} varies from less than 15 nm for gate oxides to more than 1000 nm for field oxides.

B) Diffusion

“Diffusion” is the movement of impurity atoms from sites of high concentration to sites of low concentration and takes place at temperatures in the range of 800 °C to 1400 °C. The concentration profile of the impurities within the semiconductor is a function of the impurity-concentration at the semiconductor surface and the amount of time for which the semiconductor is placed in a high-temperature environment.

There are two basic types of diffusion, the “infinite-source-” and the “finite-source diffusion”, distinguished by the time-dependent concentration of the impurity at the surface. These two types are typically of “pre-deposition”- and “drive-in diffusion”-types, respectively. The object of a pre-deposition diffusion is to place a large concentration of impurities near the surface of the material. The maximum concentration that can be diffused into silicon depends on the type of impurity and is, due to the solid solubility limit, in the range of $5x10^{20}$ atoms/cm^3 to $2x10^{21}$ atoms/cm^3. The drive-in diffusion usually follows a pre-deposition, and is used to drive the impurities deeper into the semiconductor.

C) Ion implantation

By “Ion implantation”, ions of a particular dopant (impurity) are accelerated by an electric field to a high velocity, and shot into the semiconductor material. The average depth of penetration, depending on the velocity and angle of the impinging ions, varies typically from 100 nm to 600 nm. The ion implantation process causes damage to the semiconductor crystal lattice, leaving most of the implanted ions electrically inactive. This damage can be repaired by an annealing process, in which the semiconductor temperature is raised to around 800 °C after implantation, allowing the ions to move to electrically active locations. Ion implantation can substitute diffusion, since in both cases the object is to insert impurities into the semiconductor material.

D) Deposition

This fourth basic process includes the deposition of films of various materials. This may be done by using several techniques, including “Evaporation”, “Sputtering” and “Chemical Vapour Deposition (CVD)”.

In evaporation deposition, a solid material is placed in a vacuum and heated until it evaporates. The evaporated molecules strike the cooler wafer and condense into a solid film on the wafer surface.

The sputtering technique uses positive ions to bombard the cathode, which is coated with the deposition material, and this dislodged target-material is deposited on the wafers that are placed on the anode.

CVD uses a process, in which a film is deposited by a chemical reaction or pyrolytic decomposition in the gas phase, which occurs at the surface of the silicon wafer.

For further details on thin film deposition techniques, the reader is referred to chapter II.2.3.

E) Etching

"Etching" is a process that removes exposed (unprotected) material. The means by which exposed- and unexposed material is structured is usually defined by "Photolithography", and will be discussed in the next paragraph. A protective layer – a so-called "mask" – covers the film, except in the area that is to be etched. The etching process has to satisfy two important properties: *selectivity* and *anisotropy*. "Selectivity" quantifies the ratio of the etch rate of the desired layer to the undesired one; "anisotropy" is the property of the etching process to manifest itself in one direction. In practice, neither perfect selectivity nor perfect anisotropy can be achieved, thus undercutting effects and partial removal of the underlying layer can be significant. There are two basic types of etching techniques, "wet etching" that uses chemicals to remove the material to be etched, and "dry etching", or "plasma etching" that uses ionized gases that are rendered chemically active by generated plasma.

F) Photolithography

Each of the basic semiconductor fabrication processes discussed above is only applied to selected parts of the semiconductor, with the exception of oxidation and - in most cases - deposition. “Photolithography” refers to the complete process of transferring an image from a photomask or a computer database to a wafer. Its basic components are the “photoresist” material and the “photomask”, which is used to expose some areas of the photoresist to UltraViolet (UV) light while shielding the rest. The photoresist is classified into “positive-” and “negative photoresist”, whereby a positive photoresist is used to create a pattern where the photomask is opaque to UV light and a negative photoresist creates a pattern where the photomask is transparent to UV light. The resist itself can be removed with organic solvents or plasma ashing.

G) CMOS fabrication steps

In the following paragraph, the fabrication steps of a common “n-well silicon-gate CMOS process” will be described in detail, whereby the mayor steps are summarized in figure II.2.

The first step of the n-well silicon gate CMOS process is to grow a thin silicon dioxide (SiO_2) layer on a p-doped silicon wafer. The first lithographic step defines the regions where the n-wells are to exist. The n-type impurities are implanted into the wafer, as illustrated in figure II.2(a). After a high-temperature oxidation/drive-in process, the oxide is removed, and a thin pad oxide layer is grown to protect the substrate from stress due to the difference in the thermal expansion of silicon and silicon nitride (Si_3N_4) (figure II.2(b)). Next, a global n-, and p-type field (channel stop) implant is performed, respectively, as illustrated in figure II.2(c). Its purpose is to ensure that parasitic p/n-channel transistors do not turn on under various interconnect lines. To achieve isolation between active regions, a thick SiO_2 layer is grown over the entire wafer, except where

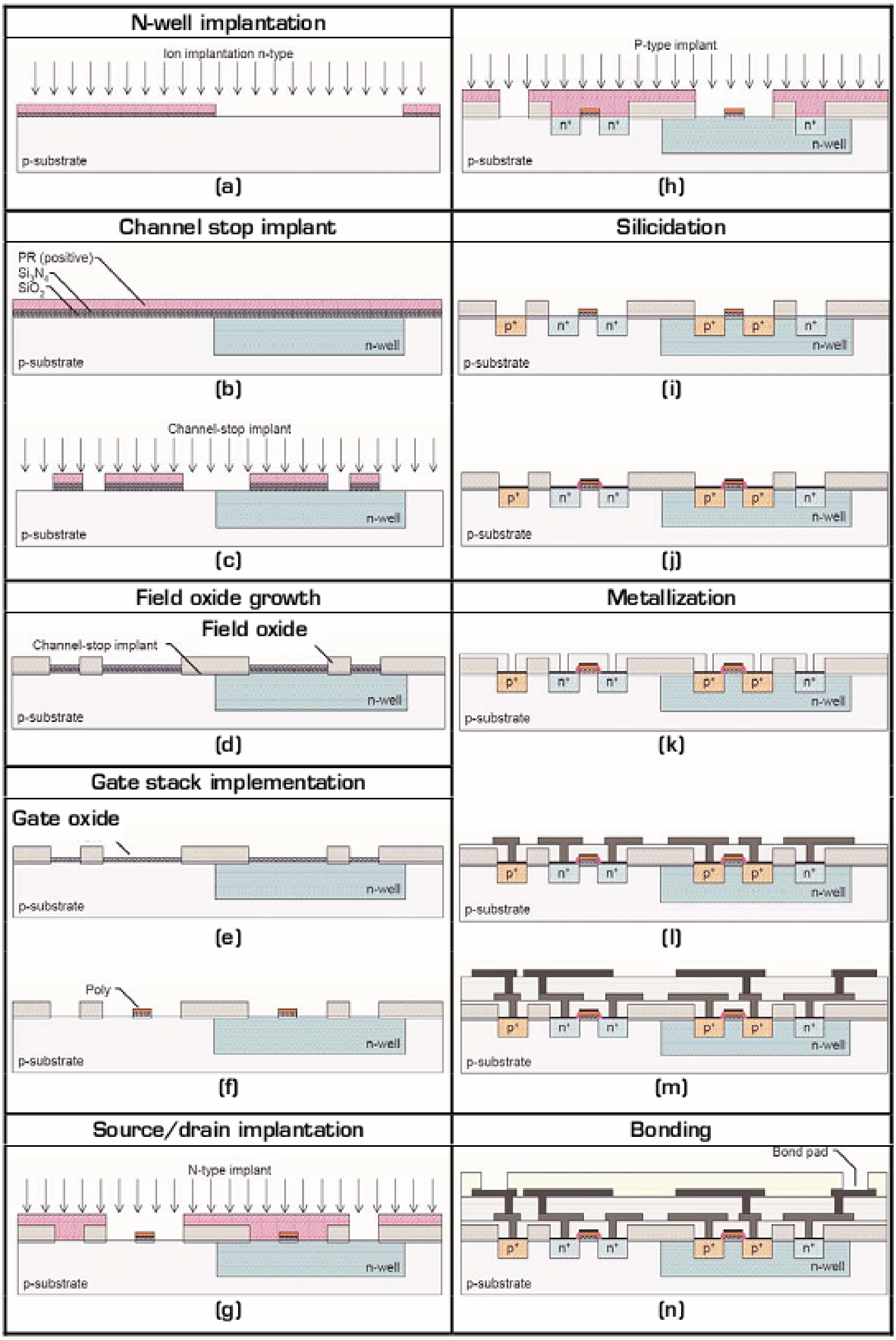

Figure II.2: Mayor CMOS fabrication steps (adapted from [7]).

Si_3N_4 exists (Si_3N_4 impedes oxide growth). This process is called “LOCOS isolation”, resulting in a thick Field Oxide (FOX). Figure II.2(d) shows the result of this step.

Following, the remaining Si_3N_4 is removed and the very critical growth of the gate oxide, serving as the gate dielectric, is performed by a slow low-pressure CVD process (figure II.2(e)). Its thickness t_{ox} determines a multitude of parameters of MOSFETs (e.g. drain current, trans-conductance, and reliability). Polysilicon is then deposited, patterned and etched, leaving the required areas to accomplish transistor gates. The result of this process step is illustrated in figure II.2(f).

Now the drain and source areas have to be diffused into the substrate. Ion implantation forms the source/drain regions of n-MOS transistors and n-well contacts (figure II.2(g)). After photolithography has been applied, the areas that consist of source- and drain-junctions of p-MOS transistors and the substrate ties are implanted by p-type ions (figure II.2(h)). These two implantation steps additionally dope the polysilicon layer, reducing its sheet resistance. The following silicidation process begins with creating an oxide spacer at the edges of the polysilicon gate, so that the deposition of the silicide will not short the gate to the source/drain regions. During the silicidation, active areas (source/drain regions, substrate and well ties) are covered with a thin layer of highly conductive material (e.g. titanium-, or tungsten silicide) by a CVD process (figure II.2(i) and figure II.2(j)).

The wafer is now covered with a thick layer of oxide and is again photolithographically patterned. The areas where the contacts are to be made are etched down to the surface of the silicon, whereby for increased reliability, contacts to the polysilicon gate are not placed on top of the gate area (figure II.2(k)). Metal (e.g. aluminium) is deposited over the entire wafer, photolithographically defined and subsequently etched, leading to a cross section shown in figure II.2(l). To prepare for a second metal, another interlayer dielectric is deposited. Intermetal connections (vias) are in principle defined the same way as metal 1, and the result is illustrated in figure II.2(m). In order to protect the wafer from chemical intrusion or scratching, a passivation layer of SiO_2 or Si_3N_4 is applied over the whole wafer. Pad regions – areas where wires will be bonded between the integrated circuit and the circuit package – are then defined. Figure II.2(n) summarizes a cross section of the final circuit.

It is important to note that there are many other details with CMOS processes that have not been mentioned here, and furthermore there are different variations of the CMOS process just described. There is a wide variety, and the worldwide semiconductor R&D is continuously improving and re-inventing this highly-developed technology.

II.1.2 MOSFET and MOSCAP device physics

In the previous chapter, we looked at the basic CMOS process steps, and how a MOSFET is typically processed. This chapter will give an overview about the “ideal” MOSFET characteristics. During the progression of this chapter, we will focus on the MOSCAP device as the controlling component of the MOSFET device characteristics. At a first glance, it might look uncommon to start with the more complex topic and progress to the simpler one. But the focus of this work lies on MOSCAP device structures, and therefore the aim of this approach is a stepwise approximation to the relevant fundamentals by “zooming” deeper and deeper into the device, until we get to the “heart” of every MOSFET, the *gate/oxide/semiconductor transition*. All derivations are made at the example of the poly-Si/SiO_2/Si device, with the contents mainly taken from the excellent textbooks Sze [8], Chang and Sze [9], and Nicollian & Brews [10].

II.1.2.1 MOSFET device physics

Figure II.3 shows the cross section of an n-channel MOSFET with the voltage terminals and the space coordinates defined. The substrate voltage V_B is arbitrarily set to be the voltage reference. The one-dimensional energy-band diagram perpendicular to the Si/SiO$_2$ interface is shown in figure II.4. Assuming that the current flow is essentially one-dimensional from the source to the drain (this assumption will be inadequate for short channel devices), the drain current including both, drift and diffusion, is described by

$$J_n(x,y) = q\mu_n n\mathrm{E} + qD_n \frac{dn}{dy} \qquad \text{II.1}$$

where μ_n is the electron mobility, E is the electric field, and D_n is the diffusion coefficient. Assuming a Boltzmann-distribution for the minority carriers (electrons for n-channel and holes for p-channel),

$$n = n_{pB} e^{q(\phi - V - V_{SB})/kT}, \qquad \text{II.2}$$

where n_{pB} is the electron concentration in a p-type semiconductor in the bulk and

$$\frac{dn}{dy} = \frac{q}{kT} n \left(\frac{d\phi}{dy} - \frac{dV}{dy} \right). \qquad \text{II.3}$$

Together with the Einstein relation $(kT/q)\mu_n = D_n$, equation II.1 reduces to

$$J_n(x,y) = -q\mu_n n \frac{dV}{dy}. \qquad \text{II.4}$$

After integrating over the spatial dimensions and with the mobility approximated by a weighted average, the drain current can be written as [11,12]:

$$I_D = -\left(\frac{W}{L}\right) \int_0^{V_{DS}} dV(y)\mu_n(y)Q_n(y), \qquad \text{II.5}$$

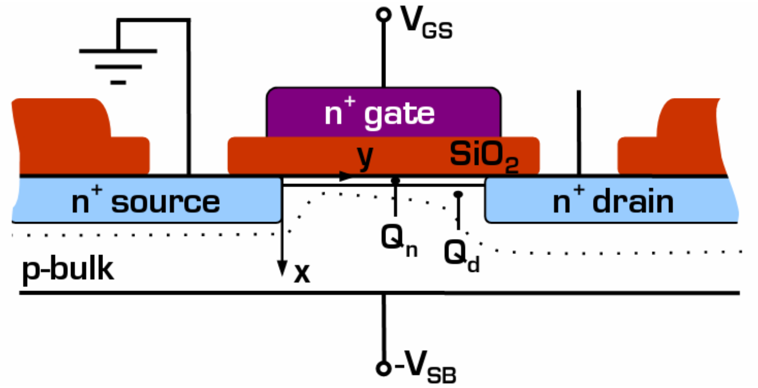

Figure II.3: Cross section (schematic) of an n-channel MOSFET with the voltage terminals and the space coordinates defined (adapted from [9]).

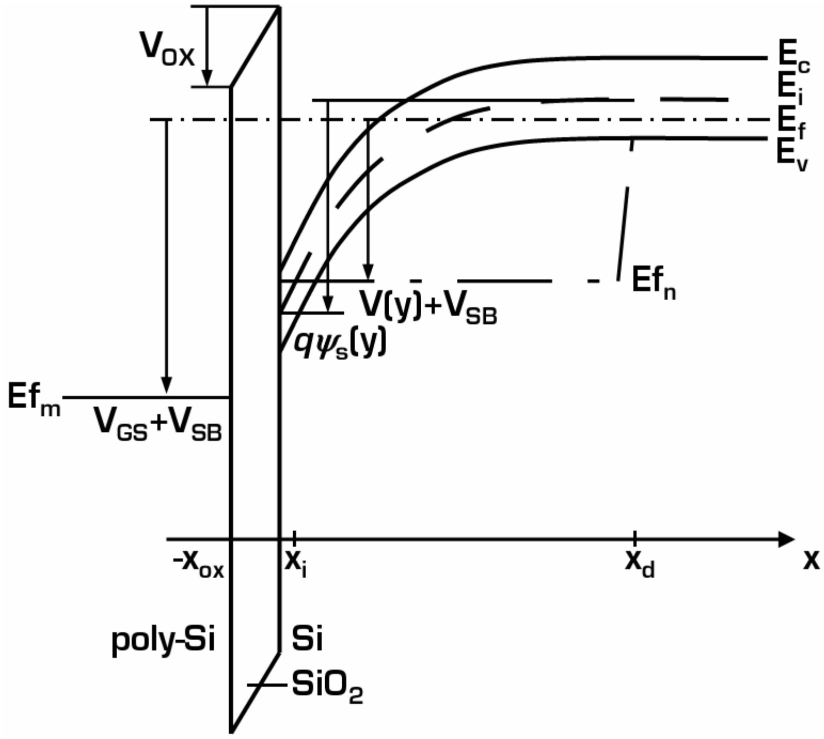

Figure II.4: Energy-band diagram in the direction perpendicular to the Si/SiO_2 interface corresponding to figure II.3 (adapted from [9]).

with the electron mobility μ_n, and the characteristic dimensions channel length L and channel width W, where

$$Q_n(y) = -q \int_0^{x_W} n(x,y)\,dx \qquad \text{II.6}$$

is the two-dimensional (2D) charge density. To obtain the drain current, we need to know Q_n in equation II.5, which is derived using the solution of the Poisson equation,

$$\nabla^2\phi(x,y,z) = \frac{-\rho(x,y,z)}{\varepsilon_S} \qquad \text{II.7}$$

(electric charge density $\rho(x,y,z) = q(N_D - N_A + p_p - n_p)$), II.8

where ε_S is the dielectric permittivity of the semiconductor, the subscript p in the electron density (n_p) and the hole density (p_p) refers to the respective quantity in a p-type semiconductor, N_A is the ionized acceptor-dopant density, and N_D is the ionized donor-dopant density. Assuming a three-dimensional (3D) density of states and the Maxwell-Boltzmann statistics for the carrier density, and after applying boundary conditions, assuming charge neutrality, and different mathematical transformations (for details, the reader is referred to [8],[9]), we obtain the mobile charge in the inversion layer Q_n:

$$Q_n = -\frac{1}{2}\lambda C_{ox}\sqrt{\frac{q}{kT}}G(\phi, V, V_{SB}, \phi_F), \qquad \text{II.9}$$

where $\lambda = \sqrt{2\varepsilon_S q N_A}/C_{ox}$, C_{ox} is the gate oxide capacitance, and the function G is dependent on applied voltage V, and the location-dependent potential ϕ.

The total charge of the semiconductor Q_S and the mobile charge in the inversion layer Q_n has to be related to the applied terminal voltages in order to relate the terminal currents to their corresponding voltages. Referring to figures II.3 and II.4 and taking an one-dimensional slice along the x direction, the terminal voltages and the potential at the Si/SiO$_2$ interface ψ_S can be brought into context as:

$$\begin{aligned} V_G - V_B - V_{FB} &= V_{OX}(y) + \psi_S(y) \\ V_{GB} &= V_{FB} + V_{OX}(y) + \psi_S(y) \end{aligned} \qquad \text{II.10}$$

and

$$Q_s(y) = Q_n(y) + Q_d(y) = -V_{OX}(y)C_{OX} \text{ ,} \qquad \text{II.11}$$

where V_{FB} is the flatband voltage, V_{OX} is the voltage drop across the gate oxide, and Q_d is the charge per unit area in the depletion region of the semiconductor.

We can now obtain the drain current in strong inversion. Therefore, we have to obtain the depletion charge Q_d by solving the Poisson equation. The drain current can then be obtained by integrating equation II.5 (for details, the reader is referred to [8],[9]. If we ground the source and substrate terminals ($V_S = V_B = 0$), and with the threshold voltage, we obtain for the linear region ($V_D << V_G - V_T$):

$$I_D = \mu_n \left(\frac{W}{L} \right) C_{OX} (V_G - V_T) V_D \text{ .} \qquad \text{II.12}$$

As the drain voltage is increased, the channel will be pinched off. If we set $Q_n(y = L) = 0$, when $V(y = L) = V_{Dsat}$, we get (by additionally assuming a large V_G or a small N_A):

$$I_D = \frac{1}{2} \mu_n C_{OX} \left(\frac{W}{L} \right) (V_G - V_T)^2 \text{ .} \qquad \text{II.13}$$

Summarizing, figure II.5 shows idealized drain characteristics of a MOSFET. In the subthreshold region ($\phi_F + V + V_{SB} < \psi_S < 2\phi_F + V + V_{SB}$), the drain current is mainly a diffusion current, in contrast to a drift current in the strong-inversion region [8].

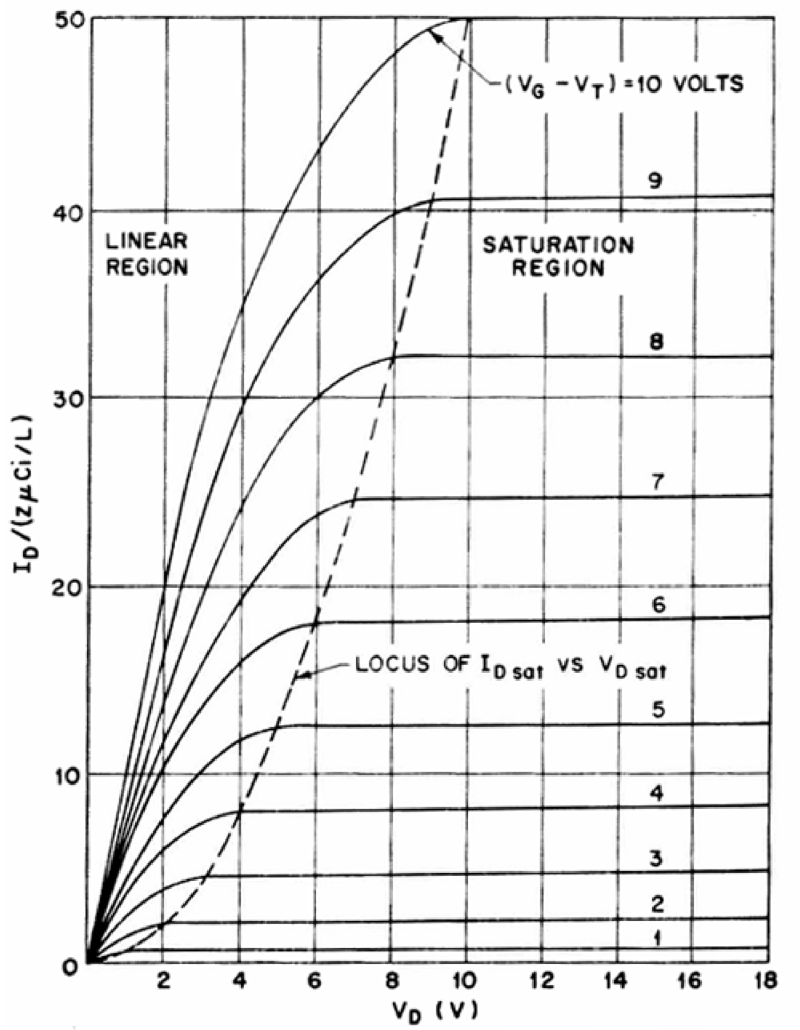

Figure II.5: Idealized drain characteristics (I_D versus V_D) of a MOSFET. The dashed line indicates the locus of the saturation drain voltage (V_{Dsat}). For $V_D > V_{Dsat}$, the drain current remains practically constant [8].

II.1.2.2 MOSCAP device physics

In the previous paragraphs, we showed that the functionality of a MOSFET can be controlled by the central Metal/Insulator/Semiconductor (MIS, or commonly: MOS) structure. Therefore, the MOS is a very useful device to study, and for this reason the fabrication and characterization of such MOS devices builds the core of this work. In this chapter, we will summarize the fundamental device physics, whereas we will follow of the contents the excellent textbook from Nicollian and Brews [10].

A MOS capacitor (MOSCAP) consists of a parallel plate capacitor with one electrode, the “gate”, and the other electrode, the “silicon”. The two electrodes are separated by a thin insulating layer (“oxide”) of (conventionally) SiO_2. Such a structure is shown in figure II.6(a). Figure II.6(b) illustrates the corresponding energy band diagram (ideal case) for a p-type semiconductor at zero applied bias ($V = 0$); E_{fm} is the metal work function, χ the semiconductor electron affinity, χ_{ox} the oxide electron affinity, E_g the bandgap, ϕ_b the potential barrier between the metal and the insulator, and ψ_b the potential difference between the Fermi level E_{fs} of the semiconductor and its intrinsic Fermi level E_i. In these conditions the energy bands are flat (“flatband condition”).

We now discuss the silicon surface charge layer for such a MOSCAP. Applying a negative bias to the gate causes the holes to be attracted to the Si/oxide interface, where they form an *accumulation layer*. Its thickness is comparable to a “Debye length” (typically 10 nm - 100 nm, depending on bias and doping density). If we increase the gate bias, holes leave the accumulation layer. At the flatband voltage V_{FB}, the silicon will be neutral everywhere. As the gate bias is made positive with respect to flat bands, holes are repelled from the silicon surface. The positive gate charge is balanced by negative acceptor ions within the silicon *depletion layer*, so-called because holes have been depleted from the surface region. As the gate bias increases, the depletion layer widens to provide more acceptor ions to balance the gate charge (0.1 μm - 10 μm deep, depending on bias and doping density).

Finally, we increase positive gate bias until electrons appear at the silicon surface in great numbers. These electrons then form a thin *inversion layer*, located at the Si/oxide interface, in a region 3 nm - 30 nm thick. Once inversion occurs, any further increase in positive gate charge is almost entirely balanced by the addition of electrons to the inversion layer. Consequently, the depletion layer no longer increases much in width.

For a mathematical description of this picture of the silicon surface charge layer and its variation with bias, we need to solve Poisson's equation, whereby we assume the MOSCAP to be in thermal equilibrium under applied bias. The whole system will be in thermal equilibrium only, when the Fermi level E_f is the same in both parts, because all quantum levels at a given energy must have equal occupation probabilities at thermal equilibrium. If E_f is not equal before contact, electrons will flow from higher to lower E_f until equality is achieved. After the initial transient, no current flows through the system, because the current flow is blocked by the large energy barriers between the oxide and each electrode. Only for oxide layers remarkably thinner than 5 nm, thermal equilibrium can be disturbed by tunnelling through the oxide. We solve the Poisson equation with certain simplifying conditions:

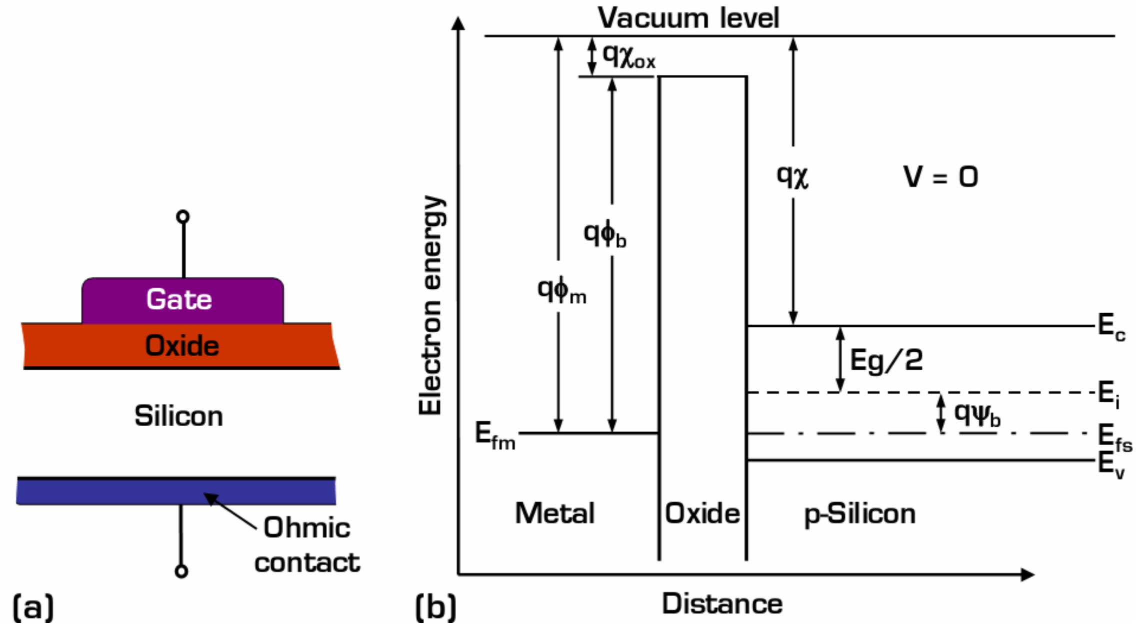

Figure II.6: (a) Cross section of a p-MOS capacitor. (b) Energy band diagram (ideal case) of an MOS capacitor as shown in figure (a) for a p-type semiconductor at zero applied bias (V = 0).

1) Poisson equation will be solved in one dimension. (The field under the gate is uniform and perpendicular to the silicon surface)
2) Impurity concentration in the silicon is uniform. This assumption does not apply, but is a good introduction.
3) The equation is solved for the non-degenerate case.
4) The Poisson equation will be solved using an approximate charge density. Each electron or hole is treated as if it moved in an average field. Thus, each electron or hole can be treated as an independent particle.
5) Surface quantization (carriers are trapped in a narrow potential well at the Si-surface) is neglected.

The “band bending approximation” assumes that the density of states in the conduction- and the valence band is not changed by the applied electric field. The only effect of an electric field is to shift all energy levels in the conduction- and valence band by a constant amount, determined by the potential at each given point in the silicon. This approximation is valid over temperature- and electric field ranges of interest in many device applications and MOSCAP measurements; but it fails in surface quantization and very heavy doping. We now calculate the hole and electron density distribution at the silicon surface under applied bias. Free carrier concentrations are functions of distance and therefore calculated as a function of x, measured in a direction perpendicular to the interfacial plane into the silicon bulk. For the electron density $n(x)$ in the conduction band, in the presence of an electric field, we obtain

$$n(x) = N_D \exp\left(\frac{q\psi(x)}{kT}\right), \qquad \text{II.14}$$

and similarly the hole density $p(x)$ in the valence band is

$$p(x) = N_A \exp\left(-\frac{q\psi(x)}{kT}\right), \qquad \text{II.15}$$

where $\psi(x)$ is the band bending and N_D/N_A are the donor/acceptor densities per unit volume, respectively.

Figure II.7 shows the energy diagram for n/p-type silicon in accumulation and depletion-inversion, respectively. An arrow pointing down denotes a positive potential, an arrow pointing up a negative one. The potential $\phi(x)$ is defined by the equation

$$q\phi(x) \equiv E_{fs} - E_i(x)\,, \qquad \text{II.16}$$

where E_{fs} is the extrinsic Fermi level and $E_i(x)$ is the intrinsic energy level. Deep in the silicon ($x \to \infty$), $\phi(x)$ is called the “bulk potential” $\phi_B(x)$, and at the silicon surface ($x \to 0$), $\phi(x)$ is called the “surface potential” $\phi_S(x)$. The band banding $\psi(x)$ is defined as

$$\psi(x) \equiv \phi(x) - \phi_B\,, \qquad \text{II.17}$$

where $\psi(x)$ represents the potential at any point x in the depletion layer with respect to its value in the bulk. In particular, the barrier height $\psi_S(x) = \phi_S(x) - \phi_B$ is the total potential difference between the silicon surface and the bulk; that is, $\psi_S(x)$ is the total band bending.

The sign conventions for the potentials for n-type silicon in figure II.7 are:

- accumulation: $\phi_B > 0, \psi_S > 0, \cdot and \cdot \phi_S > 0$
- flat bands: $\psi_S = 0 \cdot and \cdot \phi_S = \phi_B$
- intrinsic point ($n_S = p_S$): $\psi_S = -\phi_B < 0$
- inversion: $\psi_S \le -2\phi_B < 0$.

The sign conventions for the potentials for p-type silicon in figure II.7 are:

- accumulation: $\phi_B < 0, \psi_S < 0, \cdot and \cdot \phi_S < 0$
- flat bands: $\psi_S = 0 \cdot and \cdot \phi_S = \phi_B$

- intrinsic point ($p_S = n_S$): $\psi_S = -\phi_B > 0$

- inversion: $\psi_S \geq -2\phi_B > 0$.

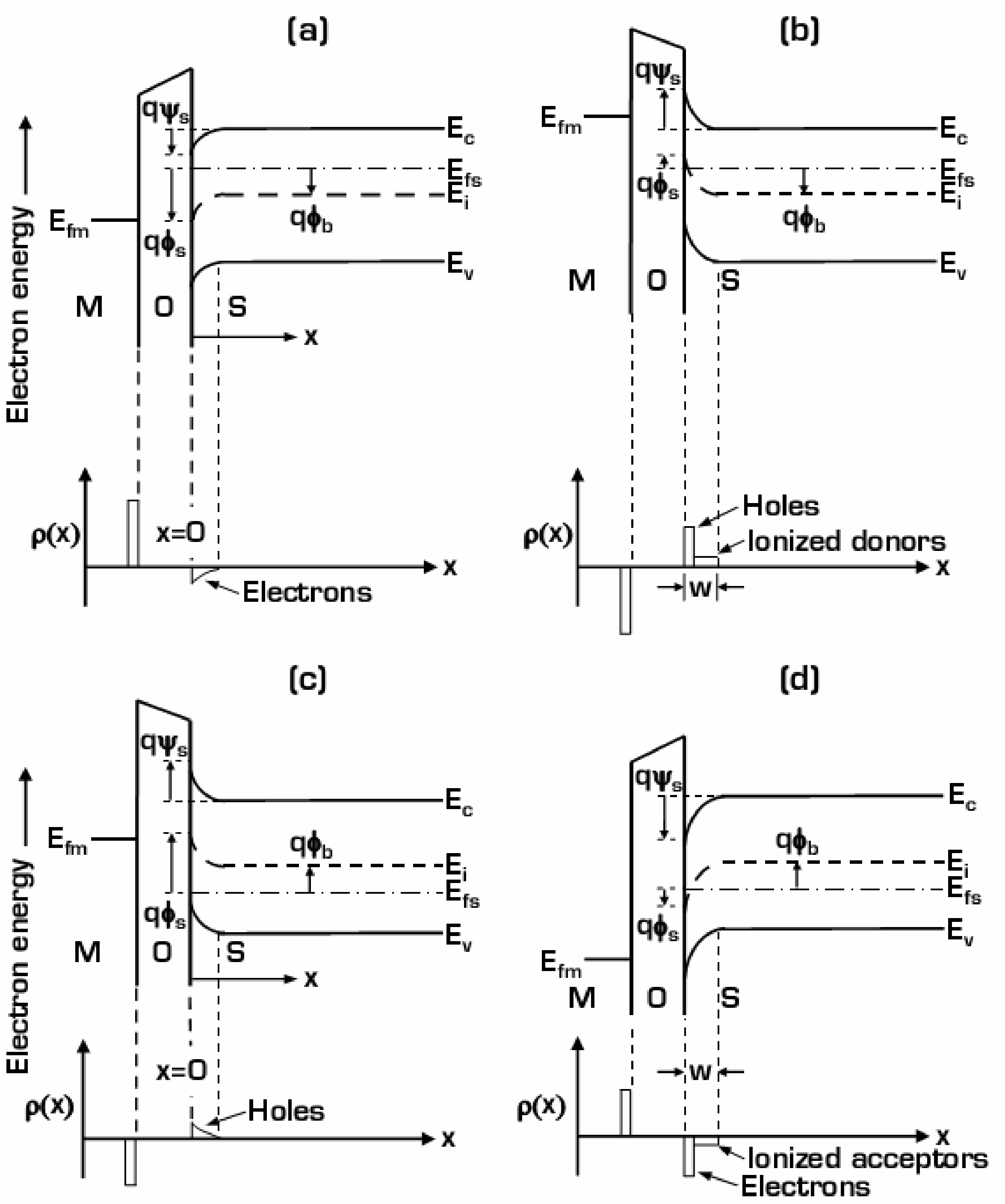

Figure II.7: (a) Energy- and corresponding charge density diagram of the MOS system for n-type silicon in accumulation. An arrow pointing down denotes positive potential. (b) Same as (a), except depletion-inversion is shown. (c) and (d) are same as (a) and (b), but for p-type silicon.

We are now ready to discuss the surface charge region quantitatively. This problem is one dimensional, so that potentials are functions of x only. The Poisson's equation will be solved under the simplifying conditions listed above, and where the band-bending approximation is valid (for a review, see [13]):

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_S}, \qquad \text{II.18}$$

where $\rho(x)$ is the charge density composed of immobile ionized donors, acceptors, mobile holes, and electrons ($\rho(x) = q\left(p(x) - n(x) + N_D - N_A\right)$) and ε_S is the dielectric permittivity of silicon. The condition of charge neutrality has to exist in the bulk; that is, far from the surface where $\phi(\infty) = \phi_B \cdot and \cdot \rho(x) = 0$. Integrating the Poisson equation from the surface to the bulk, we get the field of a semiconductor at the surface, and to get the total charge per unit area, one can use the Gaussian law:

$$Q_S = \varepsilon_S F_S = \mathrm{sgn}(u_B - u_S) C_o \left(\frac{kT}{q}\right) F(u_S, u_B), \qquad \text{II.19}$$

where F_S is the field at the semiconductor surface, $u(x) = q\phi(x)/kT$ is the dimensionless potential in the bulk (index $_B$) and at the surface (index $_S$), $C_o = \varepsilon_S / \lambda_i$ is an effective semiconductor capacitance per unit area with the intrinsic Debye length λ_i defined as

$$\lambda_i = \left(\frac{\varepsilon_s kT}{2q^2 n_i}\right)^{1/2} [cm] \text{ [14]}, \qquad \text{II.20}$$

and $F(u_B, u_S)$ is the dimensionless electric field. Figure II.8 gives a plot of relation II.19.

The "depletion approximation" approximates the free carrier distribution in the transition region between the depletion region and the neutral bulk by a step function. This step function greatly simplifies the

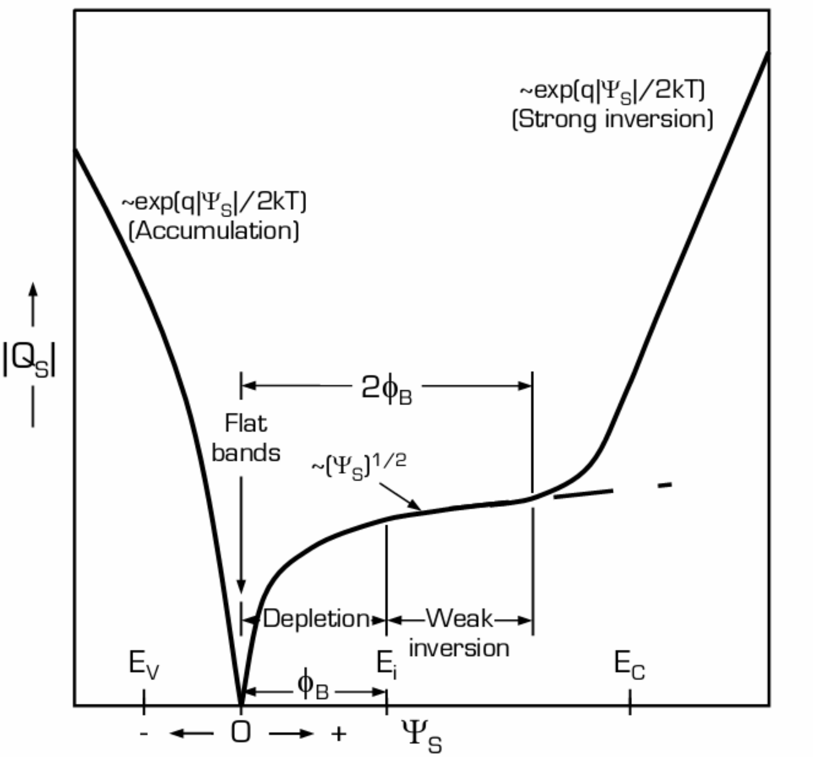

Figure II.8: Plot of relation II.19, showing the silicon surface charge density $|Q_S|$ as a function of barrier height ψ_S for p-type silicon (adapted from [8]).

solution of Poisson's equation in depletion and is widely used. Figure II.9 shows total charge density as a function of distance from the silicon surface. That is, if $p = n = 0$ in the depletion layer and charge neutrality prevails beyond the depletion layer edge. As doping concentration increases, the transition from the depletion region to the neutral bulk region becomes more abrupt.

For the general case of a non-uniform impurity distribution (e.g. diffused or ion implanted surface, or impurity redistribution), the depletion layer charge density in the depletion approximation is

$$\rho(x) = q\left[N_D(x) - N_A(x)\right]. \qquad \text{II.21}$$

After obtaining Poisson's equation and integration, we get:

$$F(x) = \frac{q}{\varepsilon_S}\int_w^x \left[N_A(x') - N_D(x')\right]\cdot dx'. \qquad \text{II.22}$$

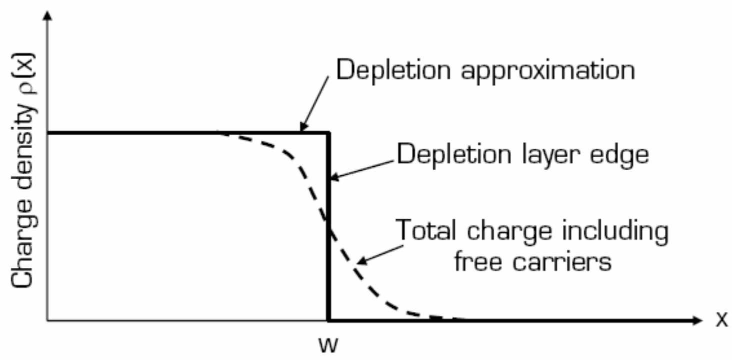

Figure II.9: Silicon surface charge density in the depletion layer (width is w) approximation. Total charge density including free carriers is shown as dotted curve. The sign of majority carriers is always opposite the sign of ionized impurities, so that the total charge is the difference between the two (adapted from [10]).

The potential in the depletion layer is obtained by integrating again:

$$\psi(x) = \frac{q}{\varepsilon_S}\int_w^x dx'(x-x')\left[N_A(x') - N_D(x')\right]. \tag{II.23}$$

Assuming the specific case of a uniform impurity distribution ($\mathrm{q(N_A - N_D) = constant}$), equation II.22 can be written

$$F(x) = \frac{q}{\varepsilon_S}(N_A - N_D)(x-w). \tag{II.24}$$

Integrating equation II.24, substituting the obtained relation into equation II.23 and integrating once more from the bulk to the surface, yields

$$\psi(x) = \frac{1}{2}\frac{q}{\varepsilon_S}(N_A - N_D)(x-w)^2. \tag{II.25}$$

For n-type $N_D > N_A$, so that $\psi_S < 0$, whereas for p-type $N_A > N_D$, so that $\psi_S > 0$. Finally, we can write:

$$\psi(x) = \psi_S\left(1 - \frac{x}{w}\right)^2, \tag{II.26}$$

where we can see from equation II.26 that the band bending in the depletion layer has a parabolic shape as it varies from ψ_S at the surface to zero in the bulk.

The depletion layer width increases with applied bias until the silicon surface becomes strongly inverted. With further increases in bias, the depletion layer width then increases only slowly, because the inversion layer shields the silicon from further penetration of the applied field. We have to keep in mind, that equations II.22 and II.23 are not exact, since the depletion approximation ignores some important facts that will not be mentioned here (please see [10] for further information). But for gradual profile variations, such as thermal redistribution effects, the errors are small, and the depletion approximation can be used with confidence.

In the previous three chapters, we worked out the basic processing steps in CMOS technology, as well as the fundamental device physics of its dominant component, the MOSFET. We have shown that the central MOSCAP structure - with its most critical part, the gate dielectric - of a MOSFET determines and controls the functionality of the device. In the following part, we will once more dare the balancing act between semiconductor physics and technology by discussing the basic concepts of device scaling.

II.1.3 Device scaling

The first concise concept of device scaling was introduced by Dennard et al. [15] and further developed in the 1980s [16]. Figure II.10 illustrates the concept of device scaling, whereby the larger device is scaled down by a factor α to yield the smaller device. The theoretical basis of scaling is formulated by considering the Poisson- and the current continuity equations, which will not be shown here in detail (for further information, the reader is referred to [16]). Table II.A summarizes the scaling relations for various scaling scenarios.

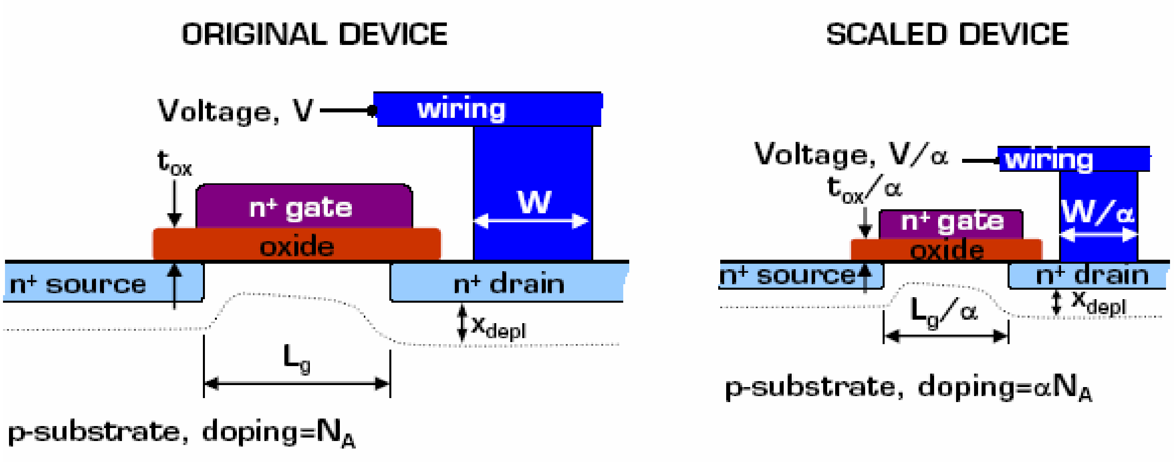

Figure II.10: Schematic illustration of CMOS scaling technology by a factor α (adapted from [9]).

The first case in table II.A summarizes scaling relations for constant electric field scaling ($\varepsilon = 1$). In practice, because of the difficulties with standard voltage supplies, the voltage is seldom scaled as rapidly as the linear dimensions. Thus, an additional scaling factor ε ($\varepsilon > 1$) for the electric field is introduced, as summarized under "generalized scaling" in table II.A. Increasing the electric field requires increasing the amount of doping, and also increases the power dissipation. The disadvantage of this scaling is that the increasing electric field increases the energy of the carriers, resulting in such undesirable effects as "hot-carrier injection" into the gate oxide, or "impact ionization", which affects device reliability. Indeed, this reliability concern forces the use of lower supply voltages for smaller devices, even if power dissipation is not an issue [17]. In recent technology generations (Gate length $L_g < 0.5$ µm), the wiring is not scaled to the same extend as the gate length, since this improves the wiring yield without degrading the gate delay. This "selective scaling" approach is shown in the third column of table II.A, and has two spatial dimension scaling parameters, α_d for scaling the gate length and device vertical dimensions, and α_w for scaling the device width and wiring.

Table II.A: Technology scaling rules for three cases.

Physical parameter	Constant electric field scaling factor	Generalized scaling factor	Generalized selective scaling factor
Channel length, insulator thickness	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Wiring width, channel width	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Electric field in device	1	ε	ε
Voltage	$1/\alpha$	ε/α	ε/α_d
Doping	α	$\varepsilon\alpha$	$\varepsilon\, \alpha_d$
Area	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha_w^{\,2}$
Capacitance	$1/\alpha$	$1/\alpha$	$1/\alpha_w$
Gate delay	$1/\alpha$	$1/\alpha$	$1/\alpha_d$
Power dissipation	$1/\alpha^2$	ε^2/α^2	$\varepsilon^2/\ \alpha_w\, \alpha_d$
Power density	1	ε^2	$\varepsilon^2\alpha_w/\alpha_d$

α is the dimensional scaling parameter, ε is the electric field scaling parameter, and α_d and α_w are separate dimensional scaling parameters for the selective scaling case. α_d is applied to the device vertical dimensions and gate length, while α_w applies to the device width and the wiring. After Wong et al. [18].

Despite the aim of increasing the number of components/chip, an improvement in performance by reducing the average switching time drives ongoing device scaling. The switching time τ of a MOSFET results from the charging and discharging of a capacitive load, where

$$\tau = \frac{C_{Load} V_D}{I_D}, \tag{II.27}$$

with the load capacitance C_{Load}, the drain voltage V_D, and the drive current I_D. The load capacitance reduces to the gate capacitance C_G, if we ignore parasitic contributions, such as junction and interconnect capacitance. For a device scaled by a factor α the switching time (in the case of constant field scaling; see table II.A) is given by

$$\tau_{scaled} = \frac{C_G V_D}{I_D} \cdot \frac{1}{\alpha}. \tag{II.28}$$

Scaling therefore leads to higher clock speeds and faster devices. To achieve this improved clock speed, also the gate capacitance has to be scaled by the factor α. If we keep in mind that the area of the gate is scaled in both lateral dimensions by the factor α, the capacitance per area C/A has to rise by the amount of the scaling factor. In this case we consider a parallel plate capacitor:

$$\frac{C}{A} = \frac{\kappa \varepsilon_0}{t}, \qquad \text{II.29}$$

where κ is the relative dielectric constant of the material, ε_0 is the permittivity of free space, and t is the thickness of the gate dielectric. To maintain the relation in equation II.29 constant, we have to reduce the thickness t of the gate dielectric by the factor α.

However, a reduction of the oxide thickness is not endlessly possible, as will be shown in the following chapter, and therefore the only alternative to solve this problem is a raise of the relative dielectric constant of the insulating material.

II.1.4 Parasitic effects and future trends

This chapter focuses on several parasitic effects that are crucial for MOSFETs in the ULSI era. These non-ideal effects were ignored in the first-order models in chapters II.1.1 and II.1.2, but are of utmost importance for device design. Hereby, we intentionally don’t treat important issues, such as short-channel effects or transport properties coming along within the ULSI era, since this would go beyond the scope of this work. The reader therefore is once more referred to the previously mentioned references, which provide an excellent insight.

In the progress of this section, we will then figure out some future trends in MOSFET device technology to overcome these difficulties.

Therefore, this final section of chapter II.1 bridges the gap to chapter II.2, where we will introduce high-κ/metal-gate devices.

A) Hot carriers:

Because of the desire to keep the power supply voltage high compared to the threshold voltage to improve performance, the electric fields typically rise as devices are scaled. Carriers in the channel gain energy as they travel from the source to the drain, and this energy is increased by an increasing electric field. These high-energy carriers are called "hot carriers" [19,20]. Due to a redirection scattering some carriers gain enough energy and momentum, so that they may surmount the interfacial Si/SiO_2 energy barrier and be injected into the gate oxide as gate current [21]. Currents through the gate insulator create interface traps, which in turn cause degradation of the device performance [22].

The most effective way to reduce hot-carrier degradation effects, apart from reducing the power supply voltage, is to use lightly doped drain (LDD) structures [23]. The basic concept behind the LDD is to drop the drain voltage in a lightly doped drain region between the channel and the heavily doped drain, and thereby reducing the maximum lateral electric field experienced by channel carriers.

B) Gate-Induced Drain Leakage (GIDL):

The "gate-induced drain leakage (GIDL) current" is attributed to band-to-band tunneling in the high-field regions in the silicon [24]. This effect is to be avoided in MOSFET design, to limit the transistor OFF-current. Band-to-band tunneling occurs in the high-field depletion region under the gate-drain overlap region. Figure II.11 illustrates the process for n- and p-channel devices. For n-channel devices, electrons tunnel from the valence band to the conduction band when the applied gate-to-drain bias results in band bending beyond the silicon band gap (similarly for holes in p-channel devices).

The generated electrons travel laterally in the depleted drain and these carriers may be amplified by impact ionization if the carriers attain enough energy in the high-field region (as in a large drain bias).

Band-to-band tunneling can be used to generate hot carriers for injection into the gate insulator, for programming of nonvolatile memory devices [25]. Reference [25] introduces a band-to-band tunneling model.

C) Gate capacitance degradation

The gate capacitance is an important determinant for the trans-conductance and the current drive, attainable by a MOSFET. For MOSFETs scaled to small dimensions, the gate capacitance is no longer simply the specific gate oxide capacitance $C'_{ox} = \varepsilon_0 \kappa / t_{ox}$ based on the oxide thickness t_{ox}, but can best be described by an equivalent electrical thickness $t_{eq} = \varepsilon_0 \kappa / C_{inv}$, where C_{inv} is the gate capacitance at inversion. Figure II.12 shows the calculated electrical equivalent oxide thickness t_{eq} versus the physical oxide thickness t_{ox} [26]. The calculation compares the classic (Maxwell-Boltzmann (MB)- and Fermi-Dirac (FD)-distribution) assumptions and the more accurate quantum-mechanical (QM) description.

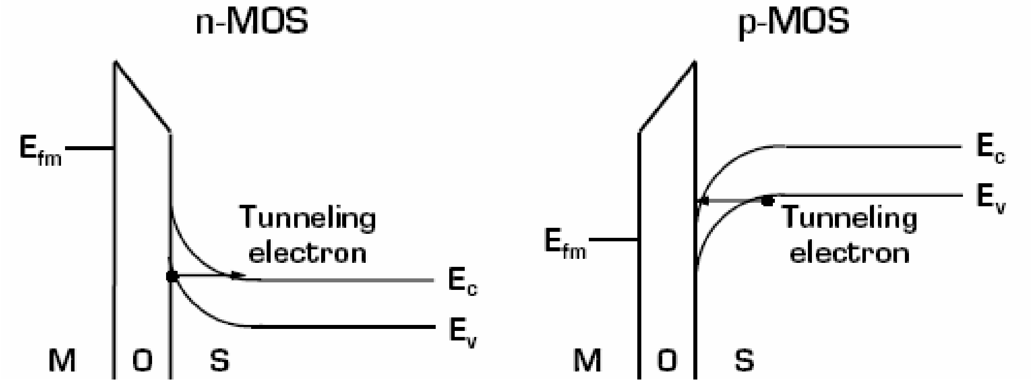

Figure II.11: Energy-band diagram illustrating the band-to-band tunnelling process in silicon in the gate-drain overlap region. Electron-hole pairs are generated by the tunnelling of valence-band electrons into the conduction band and collected by the drain and the substrate separately (adapted after [27]).

For thin physical oxide thickness, the discrepancy between physical oxide thickness and the electrical thickness is significant. The gate capacitance is degraded by two effects:

1. Inversion-layer broadening due to quantum confinement of the 2D electron gas [28,29].
2. Depletion of the polysilicon gate [30].

The inversion-layer capacitance C_{inv} becomes non-negligible compared to the gate oxide capacitance, as gate oxides are scaled below 10 nm, or when the temperature is lowered. The channel charge is reduced by quantum-mechanical broadening of the inversion layer [29].

For MOSFETs with a heavily doped poly-silicon gate, the polysilicon is either depleted or accumulated, depending on the gate bias. In either case, the finite thickness of the depletion-accumulation region contributes to a reduction of the gate capacitance, because the depletion-

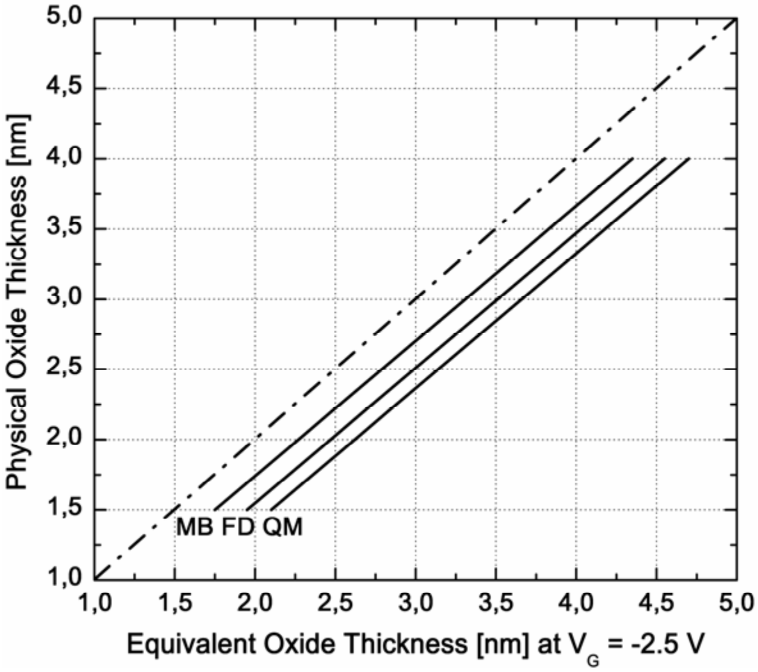

Figure II.12: Calculated (QM) t_{ox} - t_{eq} curves for n^+-poly-Si/p-Si MOS devices. Two other groups are based on the classical model with Fermi-Dirac (FD) and Maxwell-Boltzmann (MB) statistics, respectively, for comparison. Each group summarizes four curves (adapted from [26]). The dash-dotted line represents the unaffected reference for SiO_2.

accumulation capacitance of the poly-silicon gate is in series with the gate oxide capacitance [31]. This effect becomes significant as the gate oxide becomes thinner in the ULSI regime. As it is common to employ an n^+-gate polysilicon doping for n-channel MOSFETs and a p^+-gate polysilicon doping for p-channel MOSFETs, the polysilicon gate is inverted when the MOSFET channel is in inversion.

Figure II.13 shows the ratio of gate capacitance to gate oxide capacitance as a function of the doping of the polysilicon gate. It highlights that the total gate capacitance is degraded for thin gate oxides due to polysilicon depletion effects, and that it is extremely important to control the doping of the polysilicon gate, to provide uniformity of the electrical gate oxide thickness. It is particularly difficult to achieve high doping for p^+-polysilicon gates, because of the segregation of boron into the gate oxide and the possible penetration of the boron into the channel during high-temperature activation anneals.

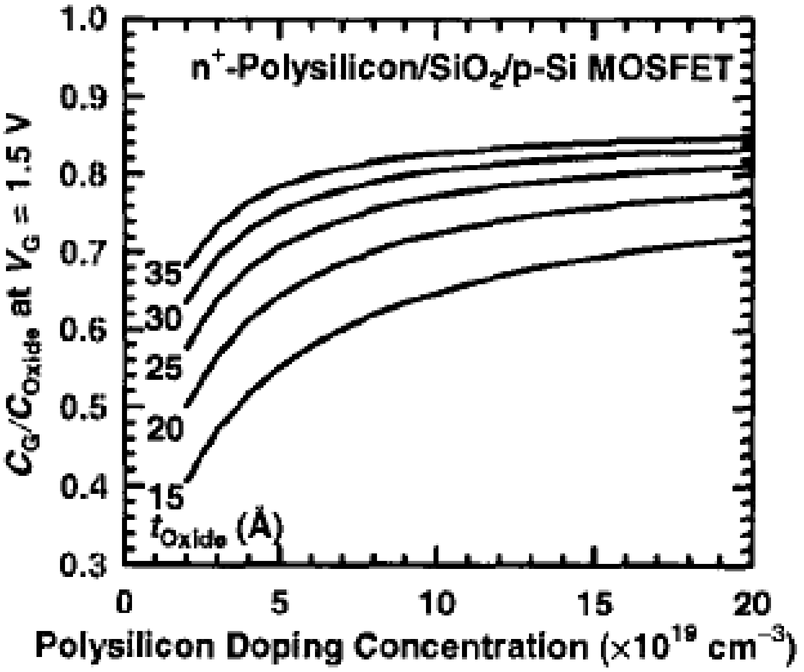

Figure II.13: Calculated gate capacitance to oxide capacitance ratio versus polysilicon doping concentration with oxide thickness as a parameter [26].

D) Gate tunneling current

As the physical thickness is scaled below ~ 3 nm in ULSI devices, significant direct tunneling occurs under high gate biases between the MOSFET channel and the gate. Figure II.14 shows the experimental and calculated gate tunneling current for various gate oxide thicknesses used in ULSI MOSFETs. The direct-tunneling current increases exponentially with decreasing gate oxide thickness and will impose a lower limit of standby-power dissipation and an upper limit of the number of active FETs on a chip for a given standby-power specification. For ULSI systems, a gate tunneling current of about 1 A/cm² is usually considered acceptable for high-performance microprocessor applications [31].

E) Output resistance

The drain current saturates (output resistance tends to infinity) when the drain voltage is larger than the drain saturation voltage. In practice, *Channel Length Modulation (CLM)* will limit the output resistance

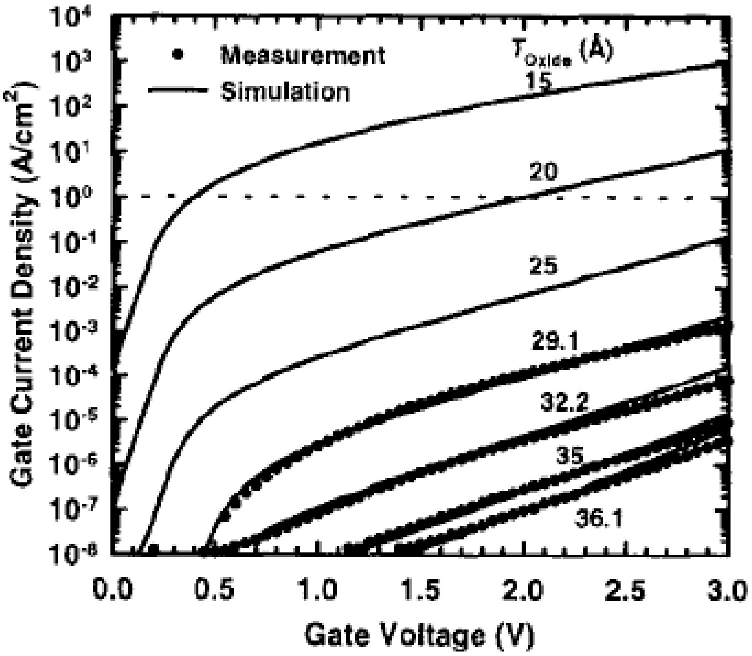

Figure II.14: Measured and simulated gate tunnelling current (I_G - V_G) characteristics of a MOSFET under inversion conditions. The dotted line indicates the 1 A/cm² limit for leakage current [26].

($r_0 = (\partial I_D / \partial V_D)^{-1}$) to a finite value at the low-drain-voltage region, while *drain-induced barrier lowering (DIBL)* and *substrate-current-induced body effect (SCBE)* limit the output resistance at moderate and high-drain-voltage regions [32]. A typical drain current and output resistance characteristic is illustrated in figure II.15, in which the regions where these effects dominate are marked. The finite output resistance has important consequences for analog signal processing applications, where the small-signal voltage gain is determined to a great extend by the output resistance [33]. Huang et al. [32] derived the output resistance in the presence of drain-induced barrier lowering and substrate-current-induced body effect and compared these results with experimental data.

F) Future trends:

Ever since the concept of MOSFET device scaling has been introduced, and especially in the late 1990s, there have been predictions and speculations of when MOSFET scaling will reach a limit. After

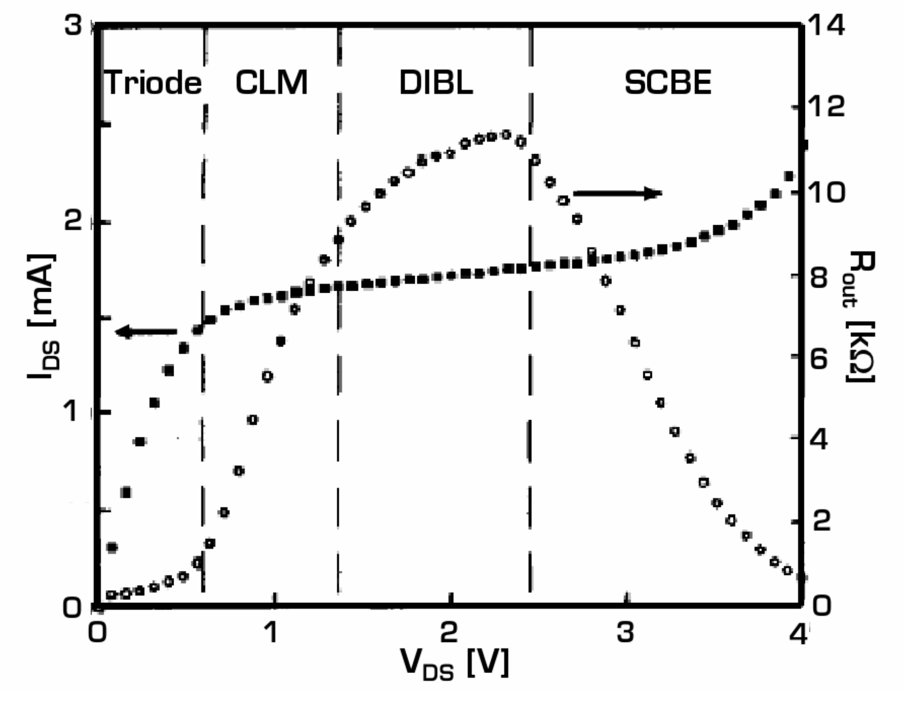

Figure II.15: Typical drain current and output resistance of a MOSFET. W/L = 10/0.43, t_{ox} = 7.5 nm (adapted from [32]).

the publication of the widely referenced *SIA National Roadmap for Semiconductors* [1], there has been much discussion about being near the limit of CMOS device scaling due to fundamental physics (Meindl [34] summarized the limits of CMOS scaling into a hierarchy of limits due to (1) physics, (2) materials, (3) devices, (4) circuit, and (5) system).

The critical dimensions that need to be engineered are the *gate length* L_g, the gate *oxide thickness* t_{ox}, the *depletion depths under the gate* x_{depl}, the *source-drain junction depth* x_j, and the *steepness of the source-drain junction*. All these parameters have to be scaled together. The gate length is the smallest feature of the MOSFET, patterned by lithography and etching. Employing light with a wavelength shorter than 193 nm presents many difficulties. Currently, there is much debate about how the lithographic requirements will be met; with X-ray, extreme UV, and electron beam, all being considered. Sublithographic feature size may be obtained by etching techniques or sidewall image-transfer techniques. The development of a reliable, manufacturable cost-effective lithographic technique is absolutely essential for the progress in CMOS technology.

As previously mentioned, the electrical thickness of the gate insulator has to decrease with the channel length. Studies of tunneling through thin oxides have shown that silicon oxy-nitride (SiON), which is the current standard gate dielectric, can potentially be thinned down to around 1 nm equivalence oxide thickness (EOT) before the leakage current and the associated dissipation becomes to large to be acceptable [1]. For equivalent thicknesses below this value, thicker gate insulators with a higher dielectric constant than SiO_2 and accordingly SiON, are being considered, to reduce the tunneling current through the gate insulator. However, reliability, thermodynamical stability, and insulator-semiconductor interface properties remain the most important concerns for such new materials.

Depletion depths and junction depths, as well as random fluctuations of device properties, are additional difficulties that have to be faced with ongoing device scaling. Nevertheless, we will not discuss these topics in detail, for the scope of this works lies on the challenge of integrating new materials with a higher dielectric constant than SiO_2 and accordingly SiON. This opens the door to the next topic of fundamentals within this thesis, where the reader will be introduced into “high-κ/metal-gate devices”.

II.2 High-κ/metal gate devices

One key element that made the scaling of Si-based MOSFET-technology for decades possible is SiO_2. The use of amorphous, thermally grown SiO_2 as the gate dielectric offers several advantages in processing, including a stable (thermal, chemical and electrical), high-quality Si/SiO_2 interface, as well as superior electrical isolation properties. In modern CMOS processing, defect charge densities are in the order of $10^{10}/cm^2$, and midgap interface state densities are around $10^{10}/cm^2\cdot eV$. Hard breakdown fields of 15 MV/cm are routinely obtained, and are therefore expected regardless of the device dimensions. These outstanding electrical properties pose a significant challenge for any alternative gate dielectric candidate [35].

Regarding content, chapter II.2 and chapter II.3 follow the excellent textbook *"High Dielectric Constant Materials"* [36], edited by H. R. Huff and D. C. Gilmer. In chapter II.2.3 the author will address "Thin film technology", since this is one of the key processes that will have to be controlled to successfully introduce metal-gate/high-κ/silicon capacitors, as well as the experimental basis of this work.

II.2.1 High-κ gate isolator

To overcome the problems summarized in chapters II.1.3 and II.1.4, much work has been done on so-called "high-κ dielectrics" that are hoped to feature a reliable alternative to the SiO_2/SiON systems. Their fundamental advantage is that they provide a physically thicker dielectric for reduced leakage and improved gate capacitance (Review equation II.29: A higher relative dielectric constant κ allows a higher physical thickness t, by keeping the capacitance per area C/A, constant). The commonly used variable in this case is the “Equivalent Oxide Thickness (EOT)”, which is defined as

$$EOT = t_{eq} = \frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} \cdot t_{high-\kappa}\,, \qquad \text{II.30}$$

and sets the high-κ material and SiO_2 in context. Here, $t_{high\text{-}\kappa}$ is the physical thickness of the high-κ material, and κ_{SiO2} and $\kappa_{high\text{-}\kappa}$ are the relative dielectric constants of SiO_2 (= 3.9) and the high-κ material, respectively.

In the following paragraphs, we will discuss in detail the most important requirements that have to be met to successfully substitute SiO_2/SiON systems. The requirements can be summarized as follows:

A) Permittivity, band gap and barrier height

Of course, the dielectric constant κ of the considered dielectric should be noticeably higher than that of SiO_2. Table II.B lists relative dielectric constants of most commonly investigated oxides and compares them to SiO_2 and Si_3N_4. In most cases the values of the permittivity cover a range, because the measurements or calculations can be influenced by many factors, such as film thickness, method of film deposition, and local electronic, or chemical structure within the dielectric. It can be seen that in general, atoms with a high atomic number exhibit more electron dipole response to an external electric field, because there are more electrons to respond. Electronic and ionic dipoles, which give rise to the polarizability, are the two main contributions to the dielectric permittivity, and due to this fact the permittivity for oxides with higher atomic number tends to increase with increasing electronic contribution.

Addressing the tunneling process, the permittivity additionally has to be balanced against the barrier height. This is, because the leakage current increases exponentially with decreasing barrier height (and thickness) for electron “direct tunneling transport” [8,35]:

$$I_{DT}=\frac{A}{t_{OX}^{2}}\exp\left[-2t_{OX}\sqrt{\frac{2m^{*}q}{\hbar^{2}}\left(\phi_{B}-\frac{V_{OX}}{2}\right)}\right], \qquad \text{II.31}$$

where A is a constant, t_{OX} is the physical thickness of the dielectric (oxide), V_{OX} is the voltage drop across the dielectric, and m^{*} is the electron effective mass in the dielectric. For electrons tunneling from the Si substrate to the gate, the barrier height is the conduction band offset $\Delta E_{C}\cong q[\chi-(\phi_{m}-\phi_{b})]$, and for electrons tunneling the opposite direction, this is ϕ_{b} (see figure II.6).

Concerning materials with a low barrier height, at applied voltages near the working-voltage, the tunneling current might be dominated by "Fowler-Nordheim tunneling", where a triangular shape of the barrier is assumed [8,9,10].

For highly defective films with electron trap energy levels in the insulator band gap, the current will instead be governed by trap-assisted mechanisms, such as "Frenkel-Poole emission" [8,9]:

$$I_{FP}\cong E\exp\left[-\frac{q}{kT}\left(\phi_{B}-\sqrt{\frac{qE}{\pi\varepsilon_{i}}}\right)\right]. \qquad \text{II.32}$$

Here, E is the electric field and ε_{i} is the insulator permittivity.

In order to obtain low leakage currents, it is evident to find a gate dielectric that has a large conduction band offset value to Si and ideally to other gate materials that might be used. Table II.B summarizes energy band gap E_{G}-values, conduction band offset ΔE_{C}-values, and valence band offset ΔE_{V}-values for potential high-κ gate dielectric materials. If we compare the values for κ and E_{G}, one can observe a trade-off (although there are departures from this trend). In contrast to the general trend of increasing permittivity with increasing atomic number, the band gap of the metal oxides tends to decrease. An intuitive explanation for this phenomenon is that the band gaps of the transition metal oxides, which all

Table II.B: Comparison of κ-, E_G-, ΔE_C-, and ΔE_V-values for potential high-κ gate dielectric materials.

Material	**Dielectric constant: κ [–]**	**Energy band gap: E_G [eV]**	**Conduction band offset to Si: ΔE_C [eV]**	**Valence band offset to Si[a]: ΔE_V [eV]**
SiO_2	3.9	8.9	3.1	4.7
Si_3N_4	7.4	5.1	2.2	1.8
Al_2O_3	9 - 11	6.2[b], 8.8[c]	2.2[b], 2.8[c]	2.9, 4.9
Gd_2O_3	9 - 14	5.2	-	-
Dy_2O_3	11 - 13	-	-	-
Y_2O_3	12 - 18	5.9	2.2[d]	2.6[d]
ZrO_2	14 - 25	5.5, 5.8	2.0[b], 1.6[d]	2.4, 3.3[d]
$Zr_xSi_{1-x}O_y$	11[e]	8.9, 5.5	3.1[f], 1.6[g]	4.7[f], 2.8[g]
HfO_2	15 - 26	5.6, 5.9	2.0[b], 1.3[d]	2.5, 3.4[d]
$Hf_xSi_{1-x}O_y$	12[e]	8.9, 5.6	3.1[f], 1.3[g]	4.7[f], 3.2[g]
Ta_2O_5	26	4.4	0.77[h], 0.3[d]	2.55, 3.0[d]
La_2O_3	21 - 30	6.0	2.3[d]	2.6[d]
TiO_2	50 - 80	3.5, 4.5	1.0[i]	1.4, 2.4

[a] Calculated from the Conduction band offsets and energy band gap values
[b] Experimental, Afanas'ev *et al.*
[c] Experimental, Ludeke *et al.*
[d] Calculated, Robertson *et al.*
[e] Typical value for x = 0.35
[f] Corresponding value for x = 0
[g] Corresponding value for x = 1
[h] Experimental, Lai *et al.*
[i] Experimental, Campbell *et al.*

have five d-electron orbitals and other non-bonding p-orbitals, can be significantly decreased by the presence of partially filled d-orbitals (For a detailed explanation the reader is referred to [35]). This general band gap reduction for high-κ materials is a limitation that has to be taken into account when selecting a suitable gate dielectric.

In earlier considerations, researchers assumed a dielectric with κ > 25 to be necessary to replace SiO_2. Taking into account more relevant considerations, such as device performance, including off-state (leakage) current, and reliability characteristics, it seems more appropriate to find a material, which provides a moderate increase in κ, but also produces a large tunneling barrier and high-quality interface to Si. A material with $\kappa \sim 12$ to 20 will allow to obtain the required EOT values for 45 nm CMOS and beyond.

B) Thermodynamic stability on Si and interface quality

A key requirement for a MOSFET is that the applied field is able to modulate the carrier transport in the Si-channel. Therefore, any potential high-κ dielectric has to be stable in contact with Si, whereas the dielectric/channel interface has to offer low defect-densities, and also withstand CMOS processing conditions while in contact with Si. Most of the high-κ oxide systems - investigated thus far - react with Si under equilibrium conditions, forming an undesired interfacial layer. This interface with Si plays a key role and is often a dominant factor at the determination of the overall electrical properties. In such cases, an interfacial reaction barrier can produce relief [37]. By using SiO_2 as the layer at the Si interface of a stack, the quality of the Si/SiO_2 interface may reduce the extent of reaction between the high-κ dielectric and the Si, as well as to help maintain high channel carrier mobility.

Nevertheless, a *single-layer dielectric* is preferred, which will be explained at the example illustrated in figure II.16. In the left case of figure II.16, a 0.5 nm thick film of SiO_2 (κ = 3.9) has been deposited at the Si-interface as the lower layer, and afterwards a 3 nm thick dielectric with κ = 25 has been grown as the upper layer. The overall gate stack capacitance (Two dielectrics in series: $1/C_{tot} = 1/C_1 + 1/C_2$) or EOT, can be calculated by simply adding the single layer components:

$$EOT = \frac{\kappa_{SiO_2}}{\kappa_{IL}} \cdot t_{IL} + \frac{\kappa_{SiO_2}}{\kappa_{High-\kappa}} \cdot t_{High-\kappa} \cdot \qquad \text{II.33}$$

In our example the overall EOT is 1 nm, where κ_{IL} and t_{IL} are relative dielectric constant and thickness of the interfacial layer, respectively. In the right case of figure II.19, the same EOT can be achieved with 4 nm (physical thickness) of a material that only has a moderate permittivity of κ = 16. This physical thickness is greater than the physical thickness of the stack in the earlier case (3.5 nm), even though the permittivity of the

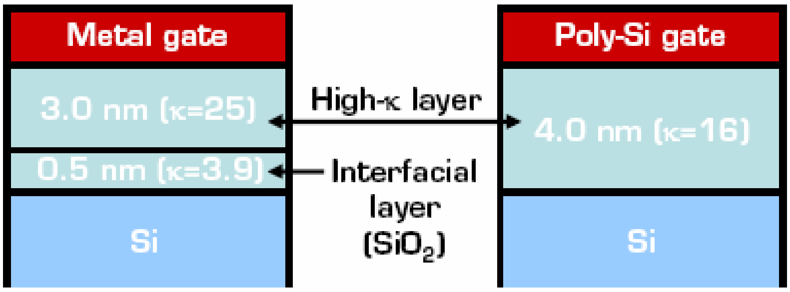

Figure II.16: Schematically comparison of stacked and single layer gate dielectrics. Either structure results in the same overall gate stack capacitance or equivalent oxide thickness (EOT = 1 nm).

single layer gate dielectric is much lower. From equation II.33 it can easily be seen that, if the structure contains several dielectrics in series, the layer exhibiting the lowest capacitance will dominate the overall capacitance and the minimum achievable EOT will never be less than that of the lowest-κ layer.

In addition, a dielectric-dielectric interface is a potential site for charge trapping, since the interface between such stacked dielectrics may almost certainly contain a large density of traps. (This topic will be discussed in detail in chapter II.3.2.1). Further, one can imagine the difficulties that an interfacial layer of unknown chemical composition and thickness brings up. For all these reasons, it is highly desirable to employ an advanced high-κ dielectric that is stable in contact with Si, and exhibits an interface with Si comparable to that of SiO_2. This would avoid the need for an interfacial layer, and additionally the high permittivity of the material could be fully used.

Summarizing, it seems difficult that any material may create a better interface with Si than SiO_2, since typical production SiO_2 gate dielectrics have midgap interface state densities of $D_{it} \sim 2\text{x}10^{10}$ states/cm². Most of the high-κ materials investigated so far show $D_{it} \sim 10^{11}$ states/cm² - 10^{12} states/cm², and in addition exhibit a substantial flat band voltage shift ΔV_{FB}, which is possibly due to fixed charge density in the oxide. It is crucial that an optimal high-κ/Si interface is obtained and preserved during the whole process flow.

In the previous paragraphs, we showed that it is important to understand the thermodynamics of the treated systems and thereby attempt to control the interface with Si. An important approach toward predicting and understanding the relative stability of a particular three-component system for device applications can be explained through ternary phase diagrams [38,39,40]. To evaluate the stability of two materials in contact, the *Gibbs free energy* has to be analysed for the relevant chemical reactions. The resulting change of the Gibbs free energy indicates direction and spontaneity of the respective reaction. Gibbs free energy analysis in the temperature range from 700 C° to 900 °C for the systems Tantalum-Silicon-Oxide (a), Titanium-Silicon-Oxide (b), and Zirconium-Silicon-Oxide (c) are shown Figure II.17. The tie lines in figures 2.17(a) and 2.17(b) indicate that Ta_2O_5 and TiO_2 (or mixtures with Si), respectively, are not stable to SiO_2 formation when placed next to Si, rather they will tend to separate into SiO_2-, metal oxide (M_xO_y, M = metal)-, and possibly silicide (M_xSi_y)-phases. In contrast, the tie lines in phase diagram of figure 2.17(c) indicate that the metal oxide ZrO_2 and the compound silicate $ZrSiO_4$ will both be stable in direct contact with Si up to ~ 900 °C. The grey shaded area denotes a large phase field of $(ZrO_2)_x(SiO_2)_{1-x}$ compositions, which are expected to be stable. These area is preferable, since it is desirable to prevent any Zr-Si bonding. This behaviour is expected to be the same for the Hafnium-Silicon-Oxide system, based on coordination chemistry arguments. These facts support HfO_2, ZrO_2, and their silicates as potential candidates, for they may solve one of the key problems addressing the control of the Si interface.

Nevertheless, the progress of this work will show that the topic concerning thermodynamic stability is more complex and not solved that easy.

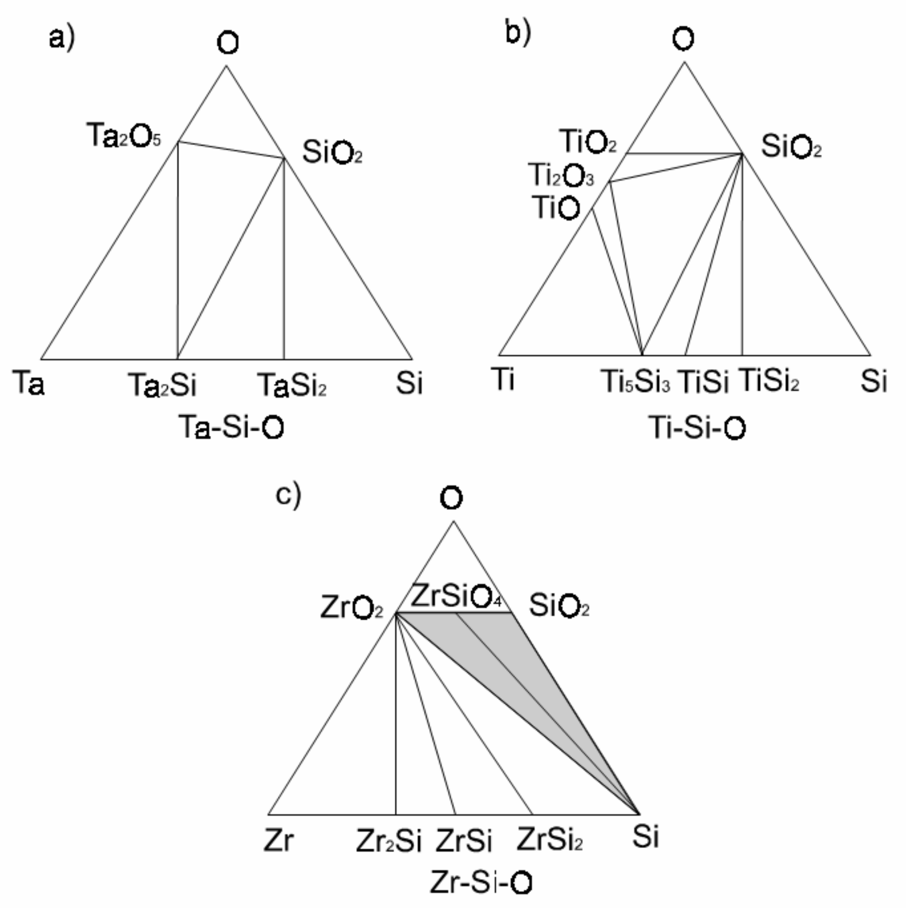

Figure II.17: Ternary phase diagrams for (a) Ta-Si-O, (b) Ti-Si-O, and (c) Zr-Si-O compounds (adapted from [38,40]).

C) Film morphology

Most of the potential candidates to be considered as future gate dielectric so far are either polycrystalline or single crystalline films. SiO_2 and also SiON however, offer an amorphous phase, which is highly desirable. Polycrystalline gate dielectrics are problematic because grain boundaries may serve as leakage paths. Additionally, grain size and orientation changes throughout a polycrystalline film can cause significant variations in the resulting electrical properties up to a locally varying permittivity ε. A gate dielectric stack, with the high-κ film on top of an amorphous layer can overcome these problems, as shown by Houssa *et al.* [41] and Perkins *et al.* [42], but as previously mentioned such an interfacial layer limits the minimum achievable EOT.

Single crystalline oxides grown by Molecular Beam Epitaxy (MBE) methods [43] are in principle free of grain boundaries while providing a good interface, but these films require sub-monolayer deposition control. In contrast, amorphous films exhibit isotropic electrical properties and they are not affected by grain boundaries. Another advantage is that they can be easily deposited by manufacturable techniques.

Summarizing, an amorphous film structure of the gate dielectric appears desirable. As shown in paragraph B, a single amorphous dielectric film appears to be required to achieve the necessary minimum EOT demanded by future ULSI device scaling.

D) Gate compatibility

From the beginning of advanced gate dielectric research, Si-based gates have been applied. They can be tuned by dopant implantation to create the desired threshold voltage V_T for both n-, and p-MOS. Also process integration schemes are well established in industry.

However, nearly al potential new gate dielectric materials investigated to this point require metal gates. This is mainly due to the observed instability that occurs at the interface in contact with poly-Si gate electrodes. Another advantage implementing metal gates lies in the elimination of dopant depletion effects and sheet resistance constraints [35].

To underline the importance of gate electrode material research, this key issue will be discussed in detail in chapter II.2.2.

E) Process compatibility

Final thin film properties and quality are strongly dependent on the deposition method by which the dielectrics are formed. This deposition process has to be compatible with the present or expected CMOS processing scheme, as well as with cost-, and throughput requirements.

As high-κ/metal-gate thin film technology is the main-part within the experimental work of this thesis, this topic is addressed here for the sake of completeness, and will be discussed in detail in chapter II.2.3.

F) Reliability

High-κ materials show novel reliability phenomena related to the asymmetric gate band structure and the presence of fast and reversible charging [44]. Reliability of high-κ structures can be influenced by both, by an interfacial layer as well as the high-κ layer. G. Ribes et al. [44] give a comprehensive review on reliability issues by focusing on Hf-based dielectrics, which are so far the most intensively studied systems.

Threshold voltage (V_{TH}) stability during operation is one of the main challenges. Its shift is attributed to trapping (and de-trapping) of charges in pre-existing traps. These mechanisms can be observed and characterized in so-called "hysteresis phenomena", whereat special fast measurement techniques (e.g.: "Charge pumping technique") are required.

"Bias temperature instability (BTI)" is a degradation phenomenon in MOSFETs, already known with SiO_2 dielectrics [45]. It is assumed that under a constant gate voltage at elevated temperatures, a build-up of charges occurs, either at the interface or within the oxide layer, which leads to a shift of V_{TH}. N-MOS (*Positive bias temperature instability (PBTI)*) and p-MOS (*Negative bias temperature instability (NBTI)*) show a different behavior, but both mechanisms present serious issues in reliability.

Oxide lifetime is usually measured by the first occurrence of the "dielectric breakdown (BD)". Since some MOS-devices remain functional, the separate consideration of *soft (SBD)*-, *progressive (PBD)*-, and *hard (HBD)* breakdown is necessary, whereat PBD usually is a forerunner for a following SBD or HBD. Figure II.18 illustrates the different breakdown occurrences. The breakdown can be provoked by gate-, or substrate injection mechanisms,

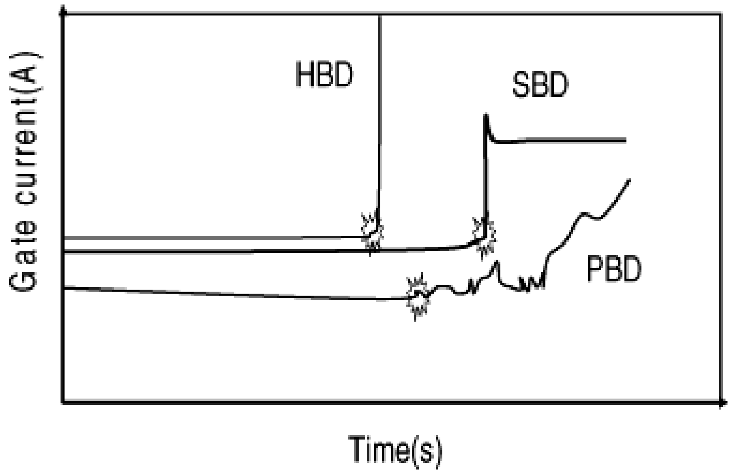

Figure II.18: Schema illustrating the three different occurrences of the breakdown (*soft (SBD)*-, *progressive (PBD)*-, and *hard (HBD)* breakdown) (adapted from [44]).

and in the first case the breakdown is most likely started by an interfacial layer breakdown.

Summarizing, *time-dependent dielectric breakdown (TDDB)* results indicate that the above mentioned mechanisms do not pose fundamental limitations, but need to be better understood. It seems reasonable that there is a link between the performance and the reliability of high–κ devices, and that the continuous improvements of the process steps will bring along improved reliability and lifetime characteristics.

G) Conclusions and potential material systems

In the previous paragraphs, we outlined the key considerations, including (a) permittivity, band gap and barrier height, (b) thermodynamic stability on Si and interface quality, (c) film morphology, (d) gate compatibility, (e) process compatibility, and (f) reliability that have to be made to successfully integrate a new gate dielectric into CMOS technology.

Taking all facts into account, it seems that especially HfO_2, ZrO_2, and their silicates promise superior potential. Due to this, immense research effort has been taken during the last years addressing these systems (for a review, see [35,36,52]). However, there are still some fundamental problems - especially thermodynamical stability and interface integrity - that have not been solved satisfactory. Addressing thermodynamic stability concerns, various rare-earth and ternary rare-earth metal oxides attracted increased interest in recent time [46,47], because these materials show amorphous structures up to the necessary CMOS processing temperatures, and as well fulfil the fundamental criteria containing permittivity, band gap and barrier height. Also aluminates [57] or stacks of the above mentioned materials, incorporating Al_2O_3 that forms a sharp interfacial layer-free interface in contact with Si, are being considered. Tantalum oxide (Ta_2O_3) is still under consideration, especially as tantalum-aluminate for DRAM applications. Titanates (e.g.: lanthanum-titanate) will always be a task, especially because of the high permittivity of TiO_2.

The reader may already see that it appears difficult to figure out one single candidate, superior fulfilling all needs, as it was the case at SiO_2 for over forty years. The author of this thesis believes that we will experience a diversification of the implemented materials due to requirements and device application. This work includes experimental work on ZrO_2 and HfO_2, which is argued by the conclusions of this chapter.

As already addressed, not only the compatibility of the gate dielectric with the Si-substrate is from fundamental importance, but also the compatibility with any potential gate material. For this reason, also the gate material deserves special attention and will be discussed in the following chapter.

II.2.2 Metal gate electrode

Not only the silicon system's insulator SiO_2 offers some beneficial advantages, also its gate material highly doped poly-silicon brings along useful advantages. On one hand it withstands heat treatments during processing that are necessary to activate the source- and drain dopants, and on the other hand patterned poly-Si is used as a mask when implanting the source and drain regions[i].

There are three main reasons that consider metal gates to be incorporated in future-generation MOSFETs. First, they can circumvent the polysilicon depletion effect, and second, they avoid boron diffusion from the aggressively doped gates into the dielectric. These two issues have already been addressed in chapter II.1.4. Finally, along with the upcoming discussion about introducing high-κ dielectrics, since a huge majority of results indicate that poly-Si gates are not chemically stable in contact with these materials. Metals, due to their metallic bond, supply excess electrons, and therefore show low resistivity and do not require doping.

In the following paragraphs, we will discuss in detail the most important requirements that set the course for any material selection. The requirements can be summarized as followed:

A) Work function

Two main concepts are investigated to implement metal gate electrodes into bulk silicon CMOS devices incorporating high-κ dielectrics: "Single mid-gap metal gate"- and "Dual-work-function metal gate"-technology. Figure II.19 summarizes the two concepts by their corresponding energy diagrams.

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[i] If one is using the self-aligned approach. Still, later process schemes implemented dual work function doped polysilicon gates to control the short channel effects and achieve specific threshold voltages.

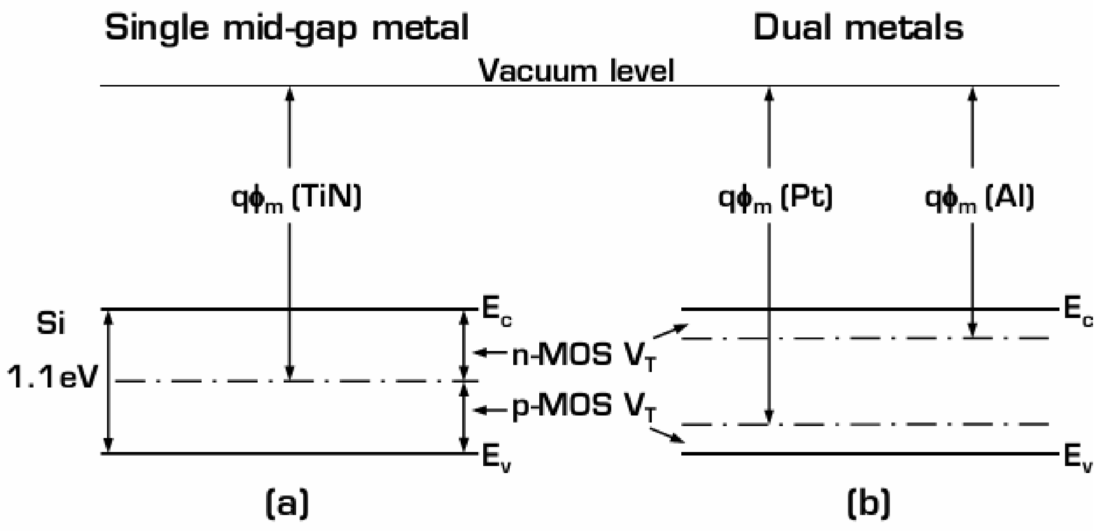


Figure II.19: Energy diagrams of bulk silicon p-, and n-MOS devices using (a) single mid-gap metal gates and (b) dual-work-function metal gates technology (adapted from [35]).

To maintain the performance of scaled bulk CMOS devices, low threshold voltages and good short channel characteristics are required. Therefore, it is necessary to identify pairs of metals with work functions that are near the conduction band and valence band edges of Si, respectively [48]. This means that gate electrodes for n-MOS and p-MOS devices respectively require work functions near 4.1 eV and 5.2 eV. Works [49] report that mid-gap work function metals (e.g. TiN or W) lead to too large threshold voltages for low-voltage operation, and to severely degraded short channel characteristics. For these reasons they appear inadequate for advanced bulk silicon CMOS devices. Still, investigations on mid-gap metals are numerous, because they are in consideration for fully depleted SOI devices [36] and - in the author's view - beyond that, offer an ideal ability to be used as reference electrode, to evaluate and compare different high-κ dielectric materials. In addition, these metals could be used as compounds (especially nitrides and silicides) for *single-metal tunable dual-work-function technology* by changing the composition rate of the elements (e.g. N, Si). Here, the following anticipated trends can be drawn:

1) Work functions of metals increase as the electronegativity of the metal (compound) increases.
2) Si has a higher electronegativity than many transition metals and therefore, metal silicide work functions are generally in the lower half of the Si-band gap.
3) Work functions of the oxides and nitrides are in general higher than those of their corresponding elemental metals.

At this point it is important to note that the techniques that can be used to measure the work functions of electrodes on dielectrics may suffer from errors, due to present charge in the bulk of the dielectric, or due to interface induced gap states [50,51,52]. This issue will be addressed in chapter II.3.2.4.

B) Thermal and chemical interface stability

In general, material properties, such as free energy of oxide formation, oxygen solubility diffusion barrier properties, and film microstructure, can be used to predict the thermal stability. The free energy of oxide formation is inversely related to the electronegativity and therefore, elemental metals with a low work function (= low electronegativity) will exhibit stability problems. This trend implies that n-MOS-compatible elemental metals might likely suffer from high-temperature instability and reactions with the underlying dielectric [53]. For example, metals with work functions less than 4.3 eV, such as Ta, Ti, Al, Zr, and Hf, tend to react with the underlying dielectric, affecting insulating and/or conducting properties, and thereby changing the resulting EOT and V_{FB} of the device.

On the other hand elemental metals with larger work functions tend to provide intrinsic stability. However, they often do nod exhibit appropriate adhesion, since this is impacted by the formation of chemical bonding between the metal gate and dielectric interface. In the case of SiO_2 as the dielectric for example, high work function metals such as Pt or Au do not react with the oxide and therefore do not form a good adhesion layer [54].

C) High carrier concentration

High carrier concentration is a must to avoid gate depletion. For the elemental metals, carrier concentrations exceeding 10^{23} electrons/cm² are common, but metal nitrides and metal silicon nitrides may have lower carrier concentrations due to the presence of non-metallic bonding [55]. This - again - may create gate depletion issues. The resistivity of the gate electrode, which is a function of grain size and impurity levels (e.g. oxygen), should also be kept at a minimum value. However, in practice it might be useful to deposit a thin film of a high-resistivity material to 'tune' the work function, and to deposit a lower-resistivity metal on top of the first material to reduce the sheet resistance of the gate electrode stack.

D) Process compatibility

In the case that *dual work function metals* will have to be incorporated, the expected necessity of two metal deposition steps will greatly increase integration complexity. On one hand the underlying dielectric might be damaged, because the first metal will have to be partly removed, and on the other hand additional photolithographic steps will have to be implemented. These difficulties might be overcome by applying alternative integration schemes. If a metal can be implanted with a certain species that alters its work function to the desired value, then a process flow similar to poly-Si may be obtained. In the case of molybdenum (Mo) for example, it has been demonstrated that the work function can be raised by implanting nitrogen (N) [56]. Another possibility is the deposition of a metal stack that includes the metals A and B, whereat metal B is partly removed from one of the well regions. Subsequently, a controlled reaction (diffusion [57], or intermixing [58]) between the two metals can lead to the desired work function.

E) Conclusions and potential material systems

As outlined in the previous paragraphs, the mayor challenge lies in finding metals with the correct work function that additionally offer good thermodynamic stability.

Metal alloys that are already used in CMOS processing, such as diffusion barriers like titanium-nitride (TiN_x), or tantalum-nitride (TaN_x) may be potential gate electrode candidates, especially for n-MOS devices. Moreover, the work function of these alloys could be tuned by the amount of nitrogen (N) [59]. A similar concept has been shown in the case of molybdenum (Mo) that can be modified using N^+ implantation [60]. Another option that allows work function modulation is “FUSI gate technology” [61], which is basically a metal silicide that is created by capping a previously deposited poly-Si layer with a metal layer and annealing this stack, which yields to a certain silicide phase. Especially nickel (Ni) in form of Ni_xSi_y is in consideration for this approach [62]. As mentioned above, the larger work function materials such as ruthenium (Ru), platinum (Pt), iridium (Ir), nickel (Ni), or cobalt (Co) are predicted to be thermodynamically stable on many gate dielectrics of interest.

Concluding, the work functions of the above mentioned systems draw the bow from near mid-gap to near band-edges, and offer suitability for bulk silicon devices. Still, evaluation regarding their compatibility with potential gate dielectrics, as well as their ability to reliably integrate them into CMOS technology, has to be done.

Beside the exploration of an applicable high-κ gate dielectric for future bulk silicon CMOS technology, also the impact of various gate metals on these dielectrics is a central topic of this work.

II.2.3 Thin film technology

So far we almost exclusively honoured silicon and its nature oxide to be responsible for the formidable progress of bulk CMOS technology. But of course mankind had its share. As a start J. Czochralski in 1916 had to invent his method to grow single crystalline material, J. Bardeen, J. Brattain, and W. Shokley in 1947 had to build the first transistor, and *Fairchild* in 1956 had to develop photolithography, and one year later the planar process.

Nature offers us unique resources, but without the possibility to use and manufacture them, to make them to materials, no progress would be possible. For this reason, to find an applicable, reliable, and profitable deposition process that offers homogeneous thin film deposition in the nm- and even sub-nm range over a wafer of 300 nm to 450 mm in diameter is absolutely indispensable. We want to face this challenge within the next three chapters.

II.2.3.1 Overview and comparison

As already outlined in the previous chapter, the deposited gate dielectric has to exhibit excellent thickness uniformity and superior interfacial-, and bulk properties to meet the high electrical demands.

There are a number of different technologies suitable for depositing high-κ dielectrics, each with its specific advantages and disadvantages. The most common techniques are listed below:

1. Atomic Layer Deposition (ALD)
2. Chemical Vapour Deposition (CVD)
    Metal-organic Chemical Vapour Deposition (MOCVD)

3. Plasma Enhanced Atomic Layer Deposition (PE-ALD)
4. Plasma Enhanced Chemical Vapour Deposition (PE-CVD)
5. Physical Vapour Deposition (PVD)
    a. Sputter Deposition
    b. Evaporation
6. Pulsed Laser Deposition (PLD)
7. Molecular Beam Epitaxy (MBE)
8. Sol-gel Deposition

Taking the following key requirements:

- Thickness uniformity
- Film density
- Step coverage
- Interface quality
- Low temperature deposition
- Deposition rate
- Industrial applicability

for the deposited film into account, MOCVD and ALD emerge as the most promising candidates, and will therefore be discussed in detail in the following chapter. Detailed description of the remaining thin film technologies can be found in many excellent text books, such as [36] or [63].

II.2.3.2 MOCVD & ALD

MOCVD

Chemical vapour deposition, especially in its low-pressure (LPCVD) version, is widely used for thin film deposition [64]. Here the used precursor substances typically are inorganic chemical complexes, which require rather high process temperatures. In the case of the growth of ZrO_2 on silicon for example, the reaction

$$ZrCl_4 + 2\ CO_2 + 2H_2 \rightarrow ZrO_2 + 2\ CO + 4\ HCl \qquad 2.34$$

takes place at process temperatures of 900 °C – 1200 °C [65]. However, the use of metal-organic precursor substances, the so-called Metal-organic Chemical Vapour Deposition (MOCVD), offers the possibility to reduce the process temperatures, what is strongly desired in industry. Especially the improvements of the process technology and tailored precursor-design within the last years make MOCVD a potential candidate for future CMOS technology [66,67]. Further information on MOCVD can be found in [68,69].

A typical CVD process can be divided into the following transport-, and reaction steps:

1. Introduction of (a) precursor substance(s) and/or reaction gas into a reaction chamber
2. Transport of the precursor substance(s) to the preheated substrate
3. Adsorption of the reactants on the substrate surface with subsequent
4. Pyrolytic dissociation(s) on the surface and simultaneous reaction of the reactants
5. Migration of the film-forming products on the substrate surface to form a continuous layer
6. Desorption and evacuation of the gaseous by-products of the reaction

Figure II.20 summarizes the above mentioned process steps by means of one precursor substance and one reaction gas (e.g.: O_2, O_3, NH_3). Since the reaction is thermally activated, either the reaction

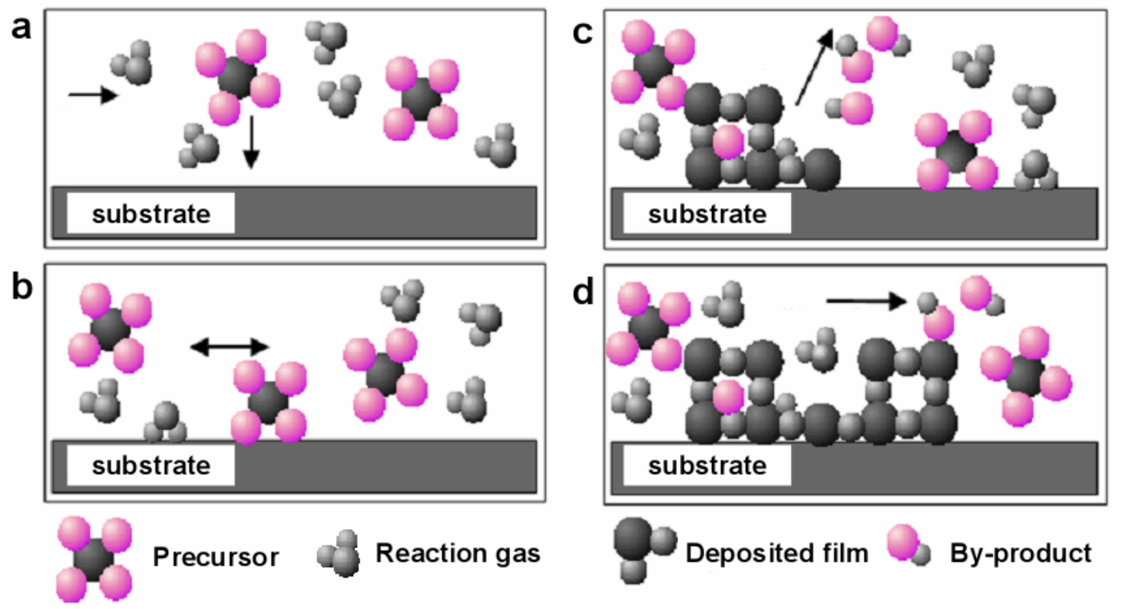


Figure II.20: Schematic, stepwise summary of a CVD process. In figure (a) the precursor substance and the reaction gas are introduced into the chamber, where they adsorb on the surface (figure (b)). The precursor substances dissociate on the surface and react chemically (figure (c)). Migration at the surface forms a continuous thin film, and the resulting by-products desorb and are evacuated (figure (d)).

chamber or the substrate itself has to be heated. The reaction rate increases with the process temperature until it exceeds the rate at which reactant species arrive at the surface. In this case the reaction is limited by the rate at which the reactant gases are supplied to the substrate by mass transport. At lower temperatures however, the surface reaction rate is reduced and therefore limits the process. Therefore, a CVD process can be divided into two mayor reaction regimes:

- Mass-transport limited regime at high temperatures
- Surface reaction limited regime at low temperatures

This correlation is shown in figure II.21 by means of an “Arrhenius-plot” of the logarithmic growth rate *log (x)* and the inverse absolute temperature *1/T*. To obtain morphologically uniform films within the surface reaction limited regime, a constant process temperature is of particular importance. Achieving temperature-stable growth processes

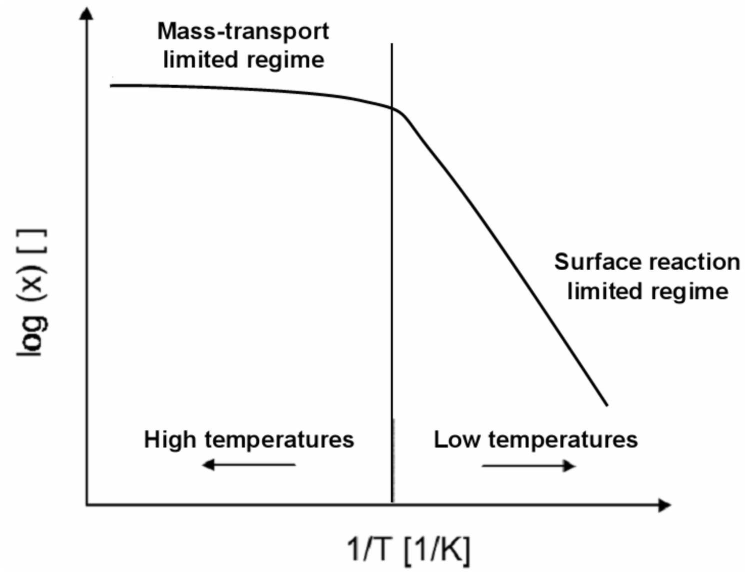


Figure II.21: Arrhenius-plot of the logarithmic growth rate log (x) and the inverse absolute temperature 1/T for a MOCVD process.

appears much easier than transport-optimized ones and is therefore preferable. Nevertheless, in practice both phenomena interact with each other and therefore influence the resulting film morphologies[i].

Commonly used CVD reactors include horizontal and vertical systems, where multiple wafers can be processed simultaneously. For chemical delivery, in most cases a bubbler system or an evaporator is used to introduce the chemical vapour into the process chamber. The vaporized precursors are usually mixed with the reactant at an injection point near the reactor. Figure II.22 shows the schematic of such a bubbler system. Since the reactor design is very critical to the film uniformity of the deposited film, we addressed this challenge by performing numerical simulations, and modelling of the MOCVD process within this work. Details on these topics will be presented in chapters III.2.1 and III.2.2.

Metal-organic precursor substances that are mainly used for the MOCVD of high-κ oxides can be categorized into:

- Metal alkoxides [70]

---

[i] Within this work, we will show that transport-phenomena even within the surface reaction limited regime have a strong impact on the resulting film thickness uniformity.

- β-diketonates [71]
- Metal alkyl amides [72]
- Metal nitrates [73].

The composition and microstructure of the deposited films largely depend on the purity of the precursors and additionally on the deposition conditions. In general, most dielectric materials obtained by CVD tend to be amorphous or have at least a very small grain microstructure. The films typically incorporate some carbon impurities, which can be reduced by adapting the O_2-flow rate, like the nature of a CVD structure can be controlled by the manipulation of the basic deposition parameters.

Details on the physico-chemical properties (like chemical composition, topography, and morphology) of the MOCVD-grown thin dielectrics obtained within this work will be presented in chapter IV.1.

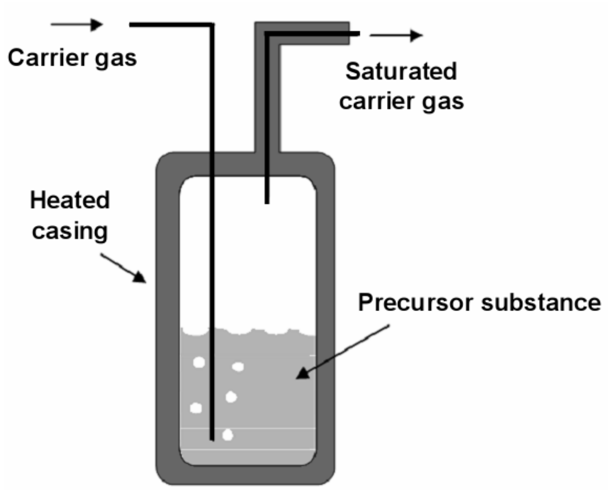


Figure II.22: Schematic of a bubbler system used for metal-organic precursor delivery.

ALD

Atomic Layer Deposition (ALD), also known as Atomic Layer Epitaxy (ALE), was developed by T. Suntola and co-workers in 1977 [74,75]. It is a self-limited layer-by-layer deposition technique with atomic layer accuracy at relatively low temperatures (typically < 400 °C). This deposition process is described here in detail, because it gained much importance within the last years, and the author of this work is convinced that it will be the dominating deposition process for future thin film applications.

By keeping the precursors separate throughout the coating process, each atomic layer formed within one process sequence is a result of saturated surface-controlled chemical reactions. Such a process sequence is schematically shown in figure II.23 by the example of ZrO_2, and can be divided in the following steps.

1. The Zr-precursor ($ZrCl_4$) is injected into the reaction chamber
2. A saturated $ZrCl_4$-layer is formed on the substrate
3. The chamber is evacuated and this continuous layer is exposed to the second precursor H_2O
4. One monolayer of ZrO_2 is formed by the chemical reaction of the two precursors, whereat the excess of precursors and the reaction by-products are removed by evacuating.

This sequence is repeated to grow films of the desired thickness. Thus, ALD offers excellent control over film thickness in the Å-range, high uniformity, and excellent conformality over complex 3-D substrate

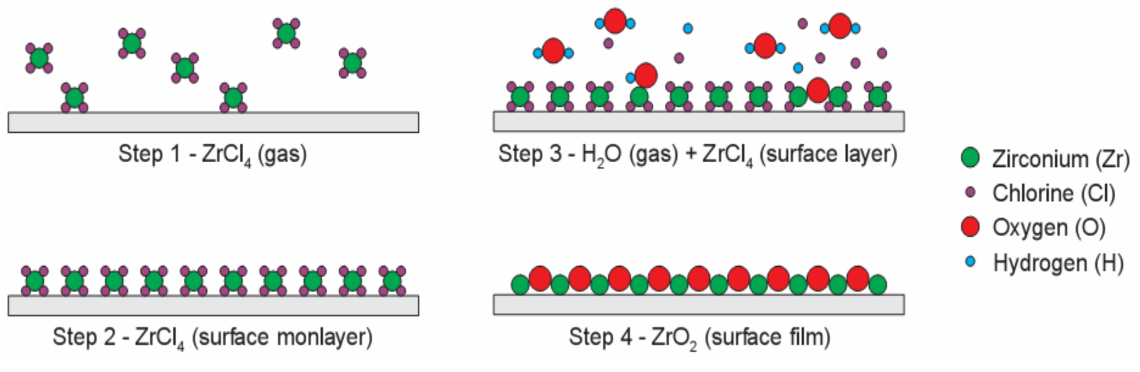


Figure II.23: Schematic of a typical ALD process by the example of ZrO_2. The precursor is injected into the reaction chamber (step 1) and forms a saturated $ZrCl_4$-layer on the substrate (step 2). Subsequently, the chamber is evacuated and this continuous layer is exposed to the second precursor H_2O (step 3), whereat one monolayer of ZrO_2 is formed (step 4).

topologies. Interface continuity might be achieved if a layer-after-layer growth mechanism is achieved starting from the very first layer. ALD is recently gaining huge impact on thin film technology and numerous papers are published, certifying ALD to be a versatile and reliable deposition process for ultra-thin films of all kinds [76,77,78,79,80].

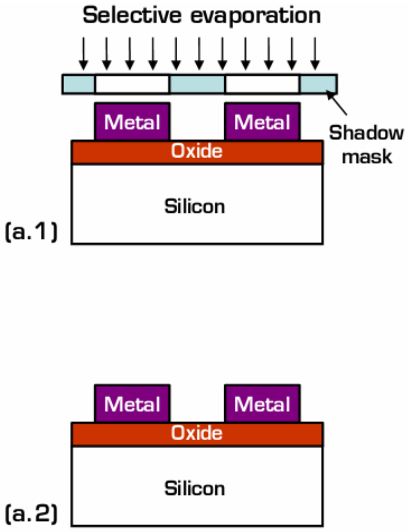
II.2.3.3 Metal gate electrode: Deposition and patterning

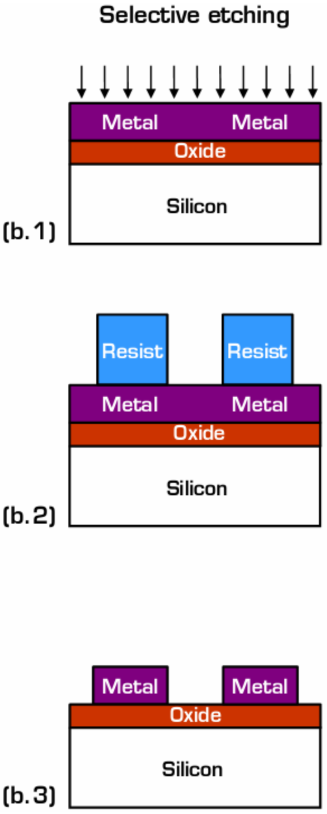
To complete MOS capacitors, a metal gate electrode has to be deposited onto the gate dielectric and patterned. Additionally, to enable electrical characterization, an ohmic backside contact has to be fabricated. In principal, metals are deposited by PVD or by CVD. The most common forms of PVD are evaporation, e-beam evaporation, plasma spray deposition, and sputtering. By CVD, the metals or metal compounds are deposited by chemical reaction or thermal decomposition of precursors. Within this work, the metals have been deposited by evaporation and sputtering (including reactive sputtering). The author abdicates to explain these processes in theoretical detail, since they are described in many excellent textbooks (e.g. [81], whereat continuative information on fundamentals can be found in [82]). Details on the experimental processing of this task will be given in chapter III.3.

The patterning of gate electrodes can be done already in between the deposition process, by evaporation of the metal through a shadow mask, or by photolithography. The latter one can be divided into two methods, selective etching and lift-off process. All three methods are schematically shown in figures II.24(a)-(c). The evaporation of a metal through a shadow mask (figure II.24(a.1)-(a.3)) is only applicable for simple geometrical structures, such as circles or squares. Nevertheless, if the process is reproducible, this is adequate for conventional MOSCAPs.

The main difference between the selective etching (figure II.24(b.1)-(b.3)) and the lift-off method (figure II.24(c.1)-(c.3)) is that in the first case the deposition of the metal is done before the definition of the structure (figure II.24(b.1)), whereat in the latter case it is the other way round (figure II.24(c.2)). Anyone of the two processes has its advantages and disadvantages, and if properly performed, both deliver excellent and reproducible results.

In this work, patterning has been done by selective etching and lift-off processing; details will be given in chapters III.3.1 and III.3.2





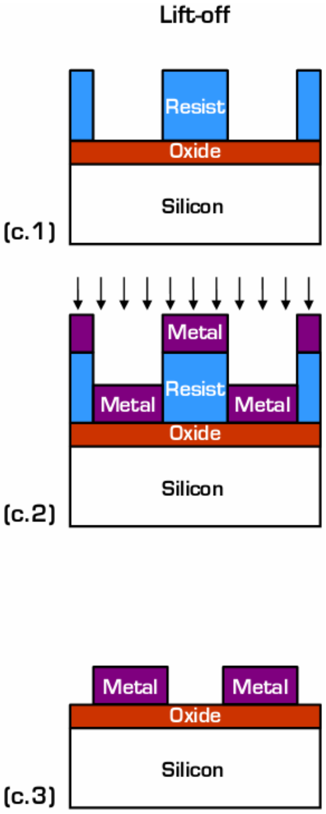


Figure II.24(a): Evaporation of a metal through a shadow mask.

Figure II.24(b): Gate electrode patterning by selective etching.

Figure II.24(c): Gate electrode patterning by lift-off method.

II.3 Characterization methodology

In the following two chapters, the fundamentals of the characterization methods that have been used in the course of this work are summarized. Physico-chemical methods take a supporting role and are only described rudimentary with given references for continuative information, since numerous excellent literature regarding these topics exists. This should not devaluate the applicability and eligibility of these methods, but the focus of this work lies on electrical characterization methodology, and therefore, this topic will be discussed in more detail.

II.3.1 Physico-chemical methodology

The resulting film thickness of the MOCVD-grown films has been obtained by spectroscopic ellipsometry (SE). Auger-electron spectroscopy (AES) has been applied to obtain the chemical composition of the deposited oxides, and atomic force microscopy (AFM) has been used to perform surface-, and roughness analysis. The morphology of complete MOS gate stacks has been revealed by a high-resolution transmission electron microscopy (HR-TEM) including an energy dispersive x-ray (EDX) analysis system to map the chemical composition.

II.3.1.1 Spectroscopic ellipsometry (SE)

Ellipsometry is an optical method for the characterization of thin films. By determining the optical parameters *index of refraction, absorption-*, and *transmission coefficient*, one can suggest the film thickness. The optical parameters are not determined directly, but indirectly by comparing the measurement results with simulated data from a pre-defined model. For this purpose a model that highly approximates the real conditions is mandatory to obtain an exact as possible and reliable result.

The measurement principle of ellipsometry is based on the changing polarization properties of light that is reflected from a film system, compared with the incident light. Reflection and transmission of a single film system are schematically depicted in figure II.25. As long as the amount of the intensity of the reflected light is high enough, also multilayer systems can be analyzed. The principle of the functionality of an Ellipsometer as it has been used within the experimental part of this work is shown in figure II.26. In the polarizer arm, light of a specific wavelength gets circularly polarized. After the reflection on surface and interfaces of the sample, the remaining intensity of the light, which changes its polarization, gets into the analyzer arm. Here, a rotating analyzer detects the resulting polarization of the reflected light by the variation of its intensity. The change of the polarization is usually detected by the change of two defined polarization-angles. In the case of "spectroscopic ellipsometry" the wavelength can be varied, whereat measurements can be done either by keeping the angle of incidence constant and changing the wavelength, or vice versa. For further information the reader is referred two [83].

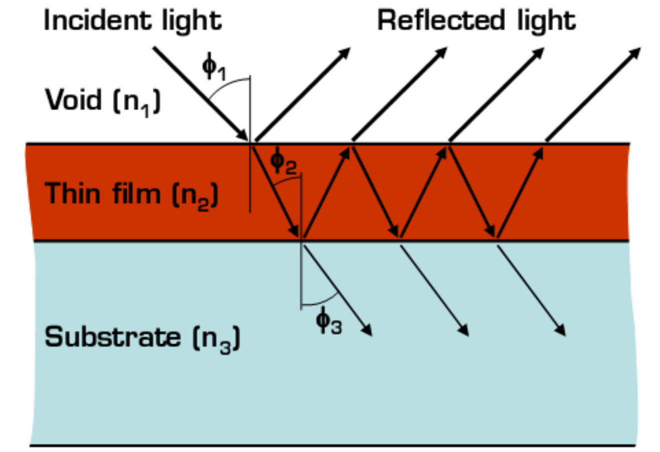


Figure II.25: Reflection and transmission of a single film system on a substrate, where ϕ is the respective incident-, and abusive-angle, and n is the respective index of refraction.

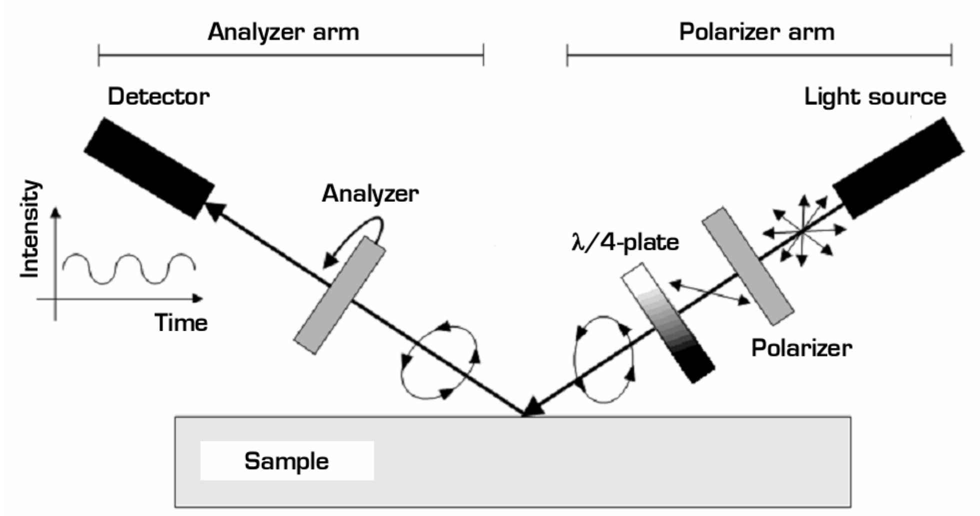


Figure II.26: Schematic principle of functionality of an Ellipsometer, used within the experimental part of this work, containing a rotating analyzer.

II.3.1.2 Auger-electron spectroscopy (AES)

Auger-electron spectroscopy is a surface-sensitive method to characterize the chemical composition of a material. The measurement principle is based on the detection of energy and number of secondary electrons that are emitted during the bombardment of the sample by a focused electron beam. The small mean free path of these secondary electrons of only a few nanometers is the cause for the surface-sensitivity, which qualifies this method for the investigation of very thin films.

The energy of the primary electrons of the focused electron beam in the concrete case within this work is 10 keV. If electrons hit the sample, they sputter an electron from an orbital close to the core. Consequently, an electron from a higher orbital takes the free place, and thereby a so-called “Auger-electron” is emitted. This mechanism is outlined in figure II.27. The kinetic energy of these Auger-electrons is characteristic for the respective Auger process and enables an exact identification of the involved elements. Beside the qualitative analysis, a quantitative extraction of the stoichiometric composition by the amount of the respective signal is possible, but the sensitivity of the system is strongly dependent on the

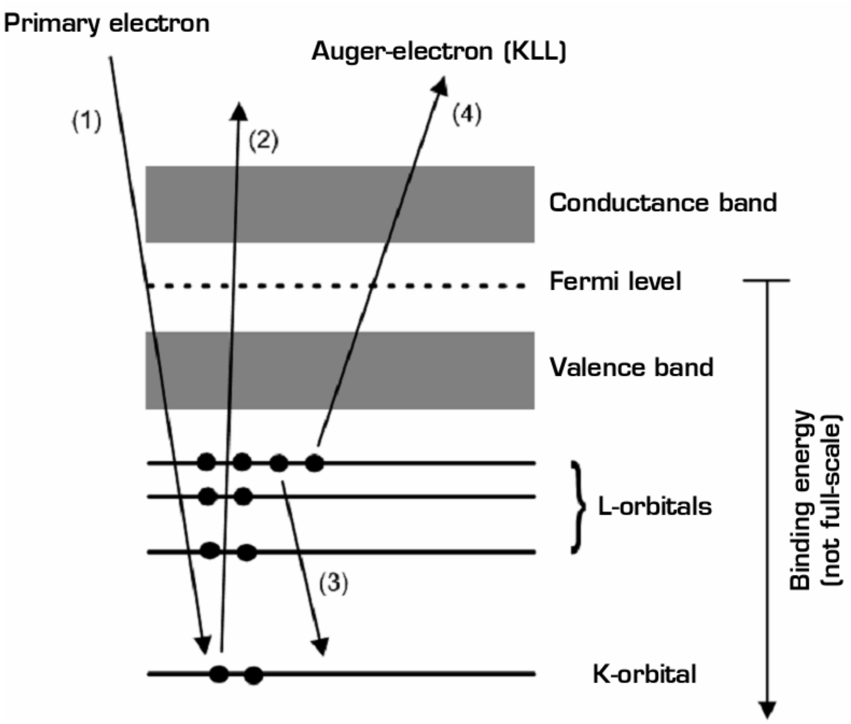


Figure II.27: Schematic illustration of an Auger process: (1) Sputter-ionization by primary electron; (2) Emission of a core-near electron; (3) Decline of an electron from a higher orbital; (4) Emission from an Auger-electron. The denotation in brackets of the process origins from the involved orbitals.

observed Auger-process and -element. For this purpose, an exact known reference sample, with a chemical composition similar to the investigated sample, is necessary. If one is lacking such reference samples, still a semi-quantitative analysis on the basis of standardized sensitivity-factors with an accuracy of a few atomic percents can be done. Comprehensive information on surface characterization can be found in [84].

II.3.1.3 Atomic force microscopy (AFM)

Atomic force microscopy (AFM) is mainly used to characterize the surface morphology of all kinds of materials by nearly achieving atomic resolution. It uses a sharp tip combined with a soft cantilever to probe the force between tip and surface sample. Depending on the amount of this force, the tip is bent up and down, which leads to the deflection of a laser beam that is aimed on the cantilever. This deflection is detected, and over a feedback loop the force is kept constant, and thereby the morphology of the surface is "redrawn".

But not only can the surface morphology be investigated, by using different derivations of AFM, additionally many surface- and interface properties such as mechanical, magnetic, optical, thermal, or chemical properties, can be investigated. All these different methods based on AFM are summarized within the term "scanning probe microscopy (SPM)". The system we used in this work is additionally equipped with a capacitance bridge that offers the possibility to apply scanning capacitance microscopy (SCM), a very interesting alternative to "conventional" capacitance-voltage measurements that has been addressed at this institution within two former theses [85,86]. The scheme of such a measurement setup is shown in figure II.27. It shows the SPM, the capacitance bridge, switching-, and external circuits. Additional information on SPM can be found in [87].

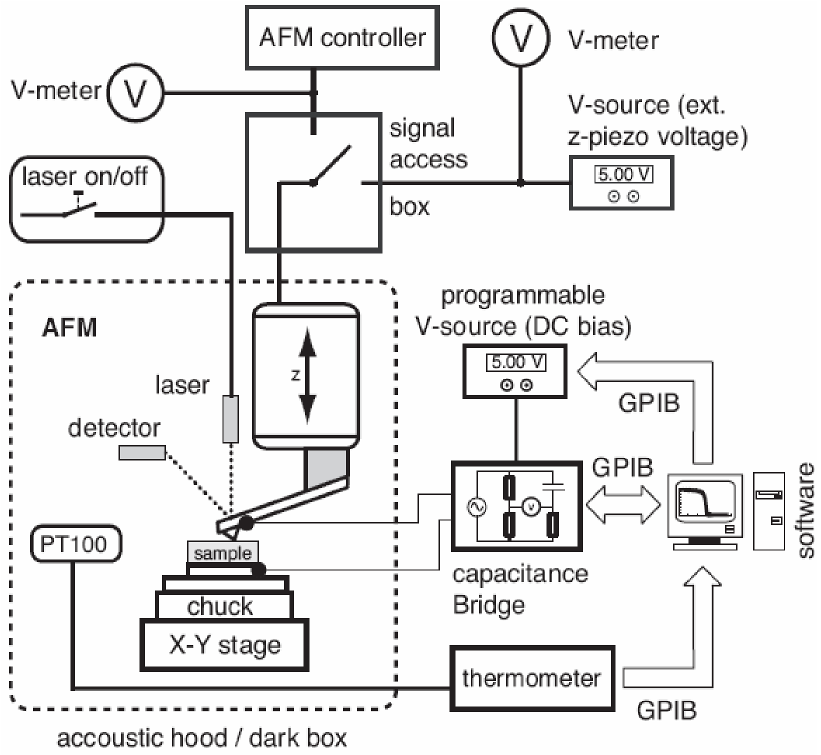


Figure II.28: Measurement scheme of SPM, including switching circuits and capacitance bridge to perform SCM measurements. GPIB denotes a bus system for bidirectional communication.

II.3.1.4 Transmission electron microscopy (TEM)

The technological need for films of only a few nanometers thickness at the same time is a big hurdle for the morphological characterization of such films or stacks along its vertical axis (also called "cross-section"). To obtain exact information about film thickness, homogeneity, and crystal structure of such layer - including possible, sub-nm thick interfacial layers - an investigation by transmission electron microscopy (TEM) is necessary. To receive this very significant information, a time-, and work-consuming sample preparation is required, to obtain the mandatory electron-transparent thickness of thinner than 300 nm.

A transmission electron microscope works similar to an optical light microscope, whereat the light source is substituted by an electron source. This is either a glowing tungsten tip, a heated LaB_6 single-crystal, or a field emitter. The ejected electrons are accelerated to approximately 2/3 of the velocity of light, fast enough to traverse the specimen. The image of the specimen is projected by magnetic lenses (similar to the optical lenses in a light microscope) onto a phosphor screen, a CCD camera, a photographic negative, or an image plate. According to the quantum theory, the high velocity v and the mass m of electrons yield to quite small wavelengths ($\lambda = h/m \cdot v$) and make it possible to achieve atomic resolution. Additionally, X-ray detectors and energy filters can provide element-specific signals that may allow chemical microanalysis on a scale of < 1 nm with a sensitivity < 10 atoms [88]. Figure II.28 shows a typical system setup.

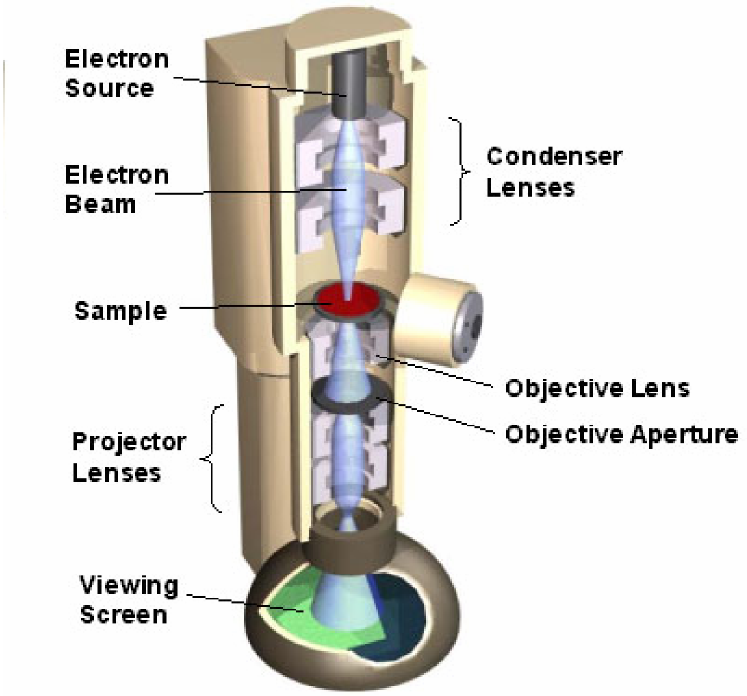


Figure II.29: Typical system setup of a transmission electron microscope (TEM), from [89].

II.3.2 Electrical methodology

The electrical investigation of MOS capacitors by capacitance-voltage (C-V) and current-voltage (I-V) characterization yields information on equivalent oxide thickness (EOT), flatband voltage, barrier heights, doping, and work function of the metal. In detail, C-V measurements reveal information on fixed- or mobile oxide charge within the gate oxide, as well as on interface trapped charge. I-V measurements give information on leakage currents, current typology, and breakdown stability of the oxide [8,10,90] (The basis of chapter II.3.2 can be found in these three references, actual results will be cited additionally).

II.3.2.1 Oxide and interface trapped charges

As already mentioned in chapter II.2.1, good bulk-, interface-, and surface characteristics of the gate oxide are indispensable. Therefore, it is very important to have the possibility to characterize the amount of the different possible charges within the oxide. Qualitatively, and – up to a certain extent – quantitatively, this can be done by C-V measurements.

There are four general types of charges that have been standardized in 1978 for the SiO_2/Si system, but are applicable to all oxide-semiconductor systems [92]. Figure II.27 shows all four types of charges and their most likely location, adapted for a Si/high-κ/metal-gate stack, including a possible interfacial Si_xO_y-layer. The charges are described in the following, whereat for each case, Q is the net effective charge per unit area (C/cm²), and D_{IT} is given in [number/cm²·eV] [91].

1. Interface trapped charge (Q_{IT}, D_{IT}):

Positive or Negative charges due to structural defects, oxidation-induced defects, metal impurities, or others caused by radiation or similar bond-breaking processes (e.g. hot electrons). They are located at the Si/oxide interface. Interface trapped charges are in electrical communication with the underlying silicon and can be charged or discharged, depending on the surface potential. Most of the interface trapped charge can be neutralized by low-temperature (~450 °C) hydrogen or forming gas (hydrogen-nitrogen mixture) anneals.

2. Fixed oxide charge (Q_f, Q_{OX}):

This is a predominantly positive charge, primarily due to structural defects (ionized silicon) in the oxide layer less than 2 nm from the Si/oxide interface. The origin comes from the oxidation process, and its density depends on oxidation ambient and -temperature, cooling conditions, and silicon orientation. It cannot be determined unambiguously in the presence of moderate densities of interface trapped charge, and therefore is only measured after hydrogen- or forming gas anneals, which minimize interface trapped charge. The fixed oxide charge is not in electrical communication with the underlying silicon and can be reduced by annealing in nitrogen or argon ambient.

3. Oxide trapped charge (Q_{ot}):

Oxide trapped charge can be positive or negative due to holes or electrons trapped in the bulk of the oxide. Trapping may result from ionizing radiation, avalanche injection, Fowler-Nordheim tunnelling, or other mechanisms. Unlike fixed charge, oxide trapped charge is sometimes annealed by low-temperature (< 500 °C) treatments, although neutral traps remain.

4. Mobile oxide charge (Q_m):

This charge is primarily caused by ionic impurities such as Na^+, Li^+, K^+, and possibly H^+. Negative ions and heavy metals may contribute to this charge even though they are typically not mobile below 500 °C.

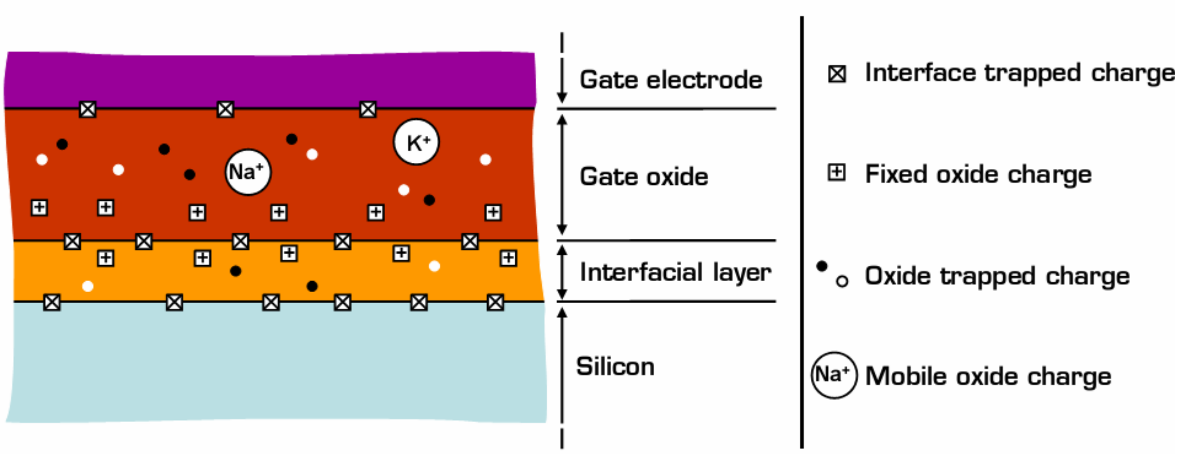


Figure II.30: Charges and their most likely locations in a MOS gate stack system incorporating a possible interfacial layer.

II.3.2.2 Capacitance-Voltage (C-V) measurements

Grove et al. [92] established the MOS capacitor as the mayor tool in the study of the MOS system. The most popular method is the C-V measurement of such a capacitor. To measure the capacitance as a fraction of bias in steady state[i], a small alternating component of voltage (ac-voltage) is superimposed on the gate bias. Figure II.31 shows the cross section of an MOSCAP as it is measured, and the addressed measurement principle. The amplitude of this ac-voltage has to be within the "small-signal range" (for explanation and further information the reader is referred to [10,90]).

By reminding the fundamentals that we worked out in chapter II.1.2.2, we obtain the total capacitance per unit area from the change of the gate charge dQ_G with the change of the applied gate voltage dV_G, after:

$$C = \frac{dQ_G}{dV_G} . \qquad \text{II.35}$$

Since the total charge in a device has to be zero and assuming no oxide charge, we get:

$$Q_G = -(Q_S + Q_{IT}) . \qquad \text{II.36}$$

Q_S is the charge corresponding to the semiconductor and Q_{IT} is the charge due to interface traps. The gate voltage V_G is partially dropped across the oxide (V_{OX}) and partially across the semiconductor. This leads to the relation

$$V_G = V_{FB} + V_{OX} + \psi_S , \qquad \text{II.37}$$

where V_{FB} is the flatband voltage, and ψ_S is the semiconductor voltage or the surface potential. By means of equations II.36 and II.37, equation II.35 can now be rewritten as:

$$C = -\frac{dQ_S + dQ_{IT}}{dV_{OX} + d\psi_S} \qquad \text{II.38}$$

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[i] Here "steady state" means that the macroscopic parameters of a system are either time independent, or varying sinusoidally in time with time independent amplitudes.

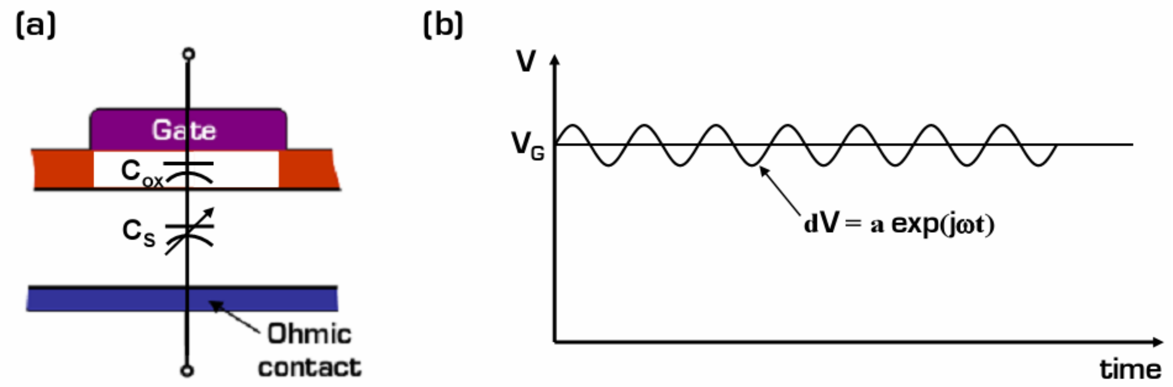

Figure II.31: (a) Cross section of an MOSCAP (compare Figure II.6). Capacitance-contributions of the oxide C_{OX} and the semiconductor C_S shown. (b) C-V measurement principle: Small ac voltage of amplitude a superposed on the gate bias V_G that is applied to the terminals of the MOSCAP.

The reader is reminded on figure II.7, to clarify the equations, figure II.32 once more shows the potential band diagram of a p-MOS capacitor for (a) flatband conditions and (b) in depletion. The semiconductor charge can be split into by

$$Q_S = Q_p + Q_B + Q_n , \qquad \text{II.39}$$

where Q_p is the hole charge, Q_B is the bulk charge of the space charge region, and Q_n is the electron charge. Equation II.38 then becomes to

$$C = \frac{1}{\dfrac{1}{C_{OX}} + \dfrac{1}{C_p + C_B + C_n + C_{IT}}} = \frac{C_{OX}(C_p + C_B + C_n + C_{IT})}{C_{OX} + C_p + C_B + C_n + C_{IT}} , \qquad \text{II.40}$$

whereat we utilized the general capacitance definition of equation II.35. Equation II.40 is represented by the equivalent circuit shown in figure II.33(a). If a negative gate voltage is applied, the silicon surface is heavily accumulated and Q_p dominates. Thus, C_p is very high and the four capacitances are shortened as shown in figure II.33(b). For positive gate voltages, the surface beneath the gate is depleted, and the total capacitance is a combination of the oxide capacitance C_{OX} in series with the capacitance of the space charge region of the bulk C_B in parallel with the capacitance due

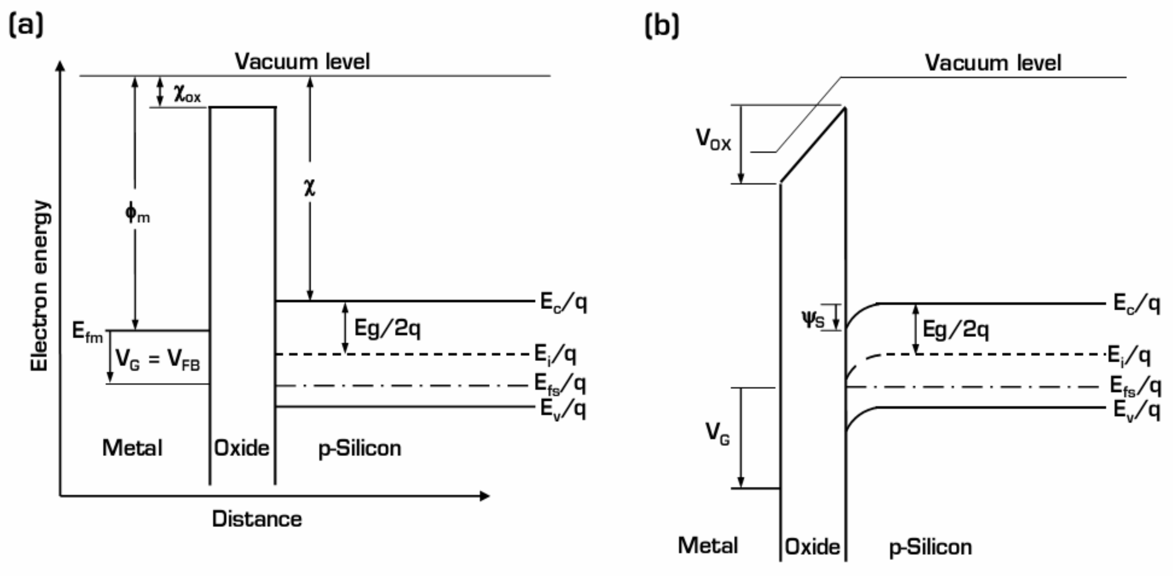

Figure II.32: Schematic band diagram of a p-MOS capacitor in (a) flatband conditions, and (b) depletion.

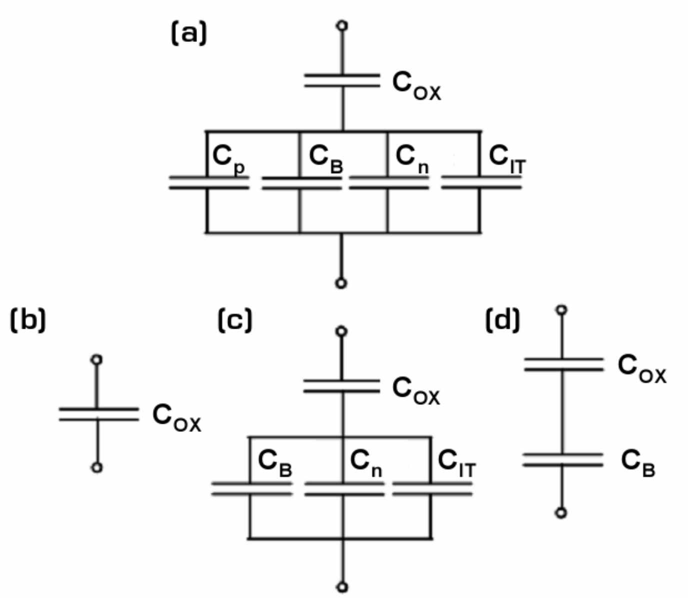

Figure II.33: Equivalent circuit of p-MOS capacitor as discussed in the text. (a) Full equivalent circuit, (b) accumulation, and inversion for the "low-frequency" measurement, (c) depletion and weak inversion, and (d) strong inversion for the "high-frequency" measurement.

to interface charges C_{IT}. For weak inversion, C_n begins to appear and the equivalent circuit can be drawn as shown in figure II.33(c). For strong inversion, C_n dominates like C_p in the case of accumulation, and therefore the equivalent circuit looks equal to that in figure II.33(b). But this is only the case for “low-frequency” measurements, where the minority carriers are able to follow the ac voltage signal; otherwise C_B dominates the parallel circuit, and the equivalent circuit can be simplified to figure II.33(d). The corresponding shape of the C-V characteristic is shown in figure II.34.

The transition from low-frequency (LF)- to high-frequency (HF)-behaviour depends on whether the generation of carriers is able to supply the current, which follows the ac-voltage signal applied at the gate, and that charges the capacitance C. This can be estimated from the equation:

$$\left|\frac{dV_G}{dt}\right| \leq \frac{q \cdot n_i \cdot w \cdot A}{\tau_G C}, \qquad \text{II.41}$$

where q is the electron charge, n_i is the intrinsic carrier density, w is the width of the space charge region, A is the area of the capacitor, and τ_G is the generation lifetime. At room temperature, this value lies far beneath 1 V/s, so that for common measurement frequencies between 100 Hz and 1 MHz and signal amplitudes of about 20 mV, one will usually obtain HF-behaviour. By measuring at elevated temperatures this constraint can be relaxed, because n_i increases.

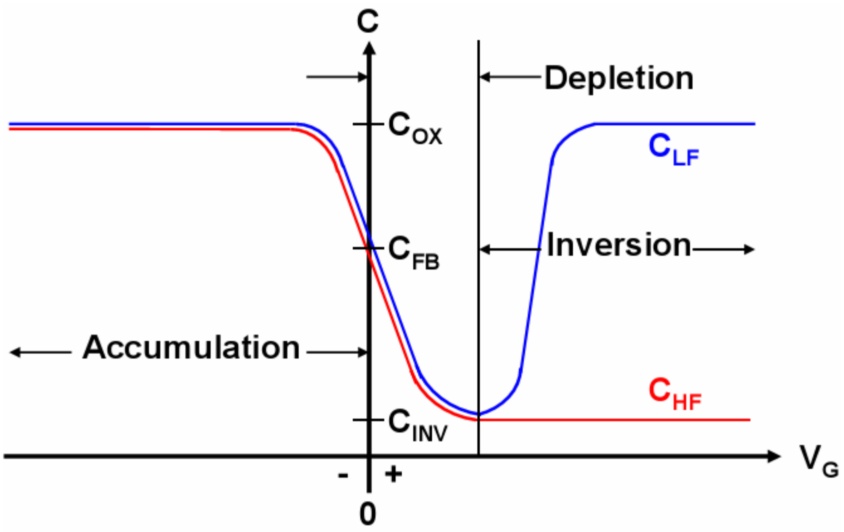

Figure II.34: C-V characteristics of a p-MOS capacitor for low-frequency (C_{LF}) and high-frequency behaviour (C_{HF}), corresponding to the equivalent circuits in figures II.33.

By investigating the C-V characteristics of an MOSCAP, one can observe several characteristics. If the device is working properly, the accumulation capacitance C_{Acc} saturates at a fixed value. For the ideal case, the C-V graph sharply and homogeneously merges from C_{Acc} to the inversion capacitance C_{Inv}. But in practice, the graph is shifted or stretched along the voltage-axis. All these possible effects are shown in figure II.35 by means of the C-V characteristics of an MOSCAP incorporating SiO_2 as the gate dielectric.

As we already discussed in the previous paragraph, in accumulation, the equivalent circuit for the C-V characteristics is shortened as depicted in figure II.33(b). Thus, the C_{Acc} we derive from the C-V measurement can be directly related to C_{OX}, and from the area-independent C_{Acc} we can estimate the insulator thickness t by the formula:

$$t = \frac{\kappa \cdot \varepsilon_0}{C_{Acc}} . \qquad \text{II.42}$$

By using κ of SiO_2, one can directly obtain EOT. On the other hand, if t is known, one can obtain an unknown κ of the investigated gate insulator material.

A shift of the C-V graph along the voltage-axis can be quantified by comparing the measured graph with the ideal (simulated) one. Even though this shift can be magnified by different values of the work function of the gate material, it is usually attributed to the presence of fixed charge within the oxide Q_{OX} [10,90]. The density of Q_{OX} can be calculated from:

$$Q_{OX} = (V_{FB,ideal} - V_{FB,real})C_{OX} \qquad \text{II.43}$$

(see also equation II.47). If the C-V curve is stretched along the voltage axis, this is generally attributed to an increase in the interface trap level density D_{IT} [8]. Furthermore, it has been shown that a lateral non-uniform oxide charge distribution in MOS-devices can indicate such a stretch-out of the C-V graphs [93].

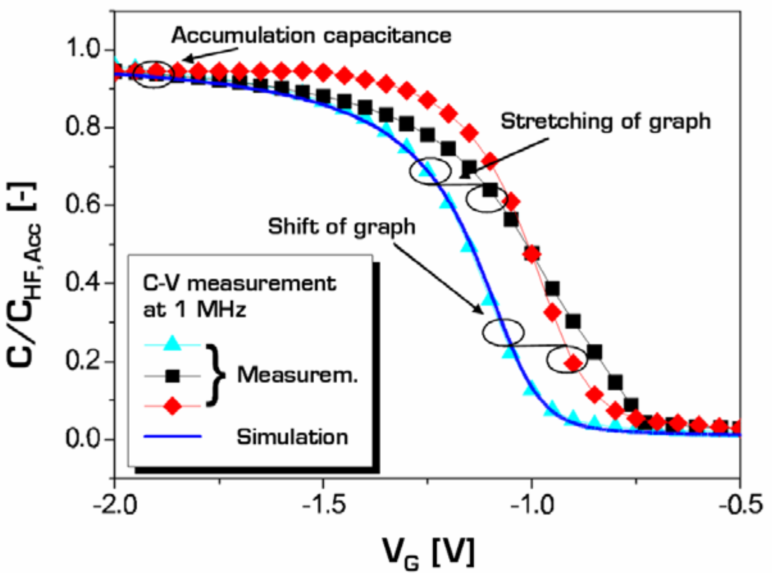

Figure II.35: Possible high-frequency C-V characteristics of an Al/SiO2/p-Si capacitor, depending on the density of interface traps and/or oxide charges.

Several methods exist to determine D_{IT} by C-V measurements. For HF-measurements, the "Terman method" [94] was one of the first being developed. The method relies on its high measurement frequency. The interface traps do not respond to the high ac-frequency applied at the gate, but they do respond on the slowly varying dc-gate-voltage. The interface trap density is then determined from:

$$D_{IT} = \frac{C_{OX}}{q}\frac{d(\Delta V_G)}{d\psi_S}, \tag{II.44}$$

where $\left(d(\Delta V_G)/d\psi_S\right)$ can be calculated from the measured C-V characteristics.

The "conductance method", proposed by Nicollian and Goetzberger [95] is in general considered to be the most sensitive and most complete method to determine D_{IT}. It is based on the measurement of the equivalent parallel conductance G_p of an MOSCAP as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density, and can be approximately expressed in terms of the measured maximum conductance:

$$D_{IT} \approx \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{\max} . \qquad \text{II.45}$$

All measurement and extraction methods – especially containing the gate dielectric capacitance [96] – described in the previous paragraphs, have been proposed and developed to investigate the SiO_2/Si system. This should not decrease their importance, but in this work we address ultrathin high-κ gate dielectrics, which demands additional considerations. Quantum-mechanical effects [97,98], high gate leakage currents, as well as series and shunt parasitic resistances [99] have to be taken into account. These issues will be discussed in detail directly at the example of the fabricated metal-gate/high-κ/Si capacitors in part IV of this work

II.3.2.3 Current-Voltage (I-V) measurements

It has been addressed several times that the raising leakage current is the main reason to substitute SiO_2/SiON as the gate dielectric. In chapter II.2.1, we already discussed the gate tunnelling current and its mechanisms. Additionally, ionic conduction can ad to such leakage currents. Current-voltage characterization should give information on the amount of this current, as well as on the present dominating mechanism.

In principle, the I-V characteristics can be measured by two different principles, the "quasi-static", and the "dynamic measurement technique". The difference between the two methods is shown in figure II.36. In both cases, the gate voltage V_G is varied stepwise and thereby, a time-dependent change of the gate current I_G can be observed. In the case of a dynamic characterization, the gate current is measured during its decay at specific time intervals t_D. The measurement of several points during a single decay allows obtaining the decay-characteristics. All causes for transient leakage-behaviour result from capacitive charging currents and the response of traps. Thus, dynamic I-V characterization can give information on the energetic position and the decay time of traps in the insulator [100]. In quasi-static measurements, t_D is so long that I_G has decreased to a quasi time-independent value. All discussions addressing the leakage current made within this work concern quasi-static behaviour.

The characterization of ultra-thin dielectric films (EOT < 2 nm) is likely affected by the tunnelling current due to direct tunnelling, Fowler-Nordheim tunnelling, or trap-induced leakage mechanisms (This topic has already been addressed in chapter II.2.1).

Concerning the reliability of a gate insulator, the *dielectric breakdown* is an important parameter (We already addressed this topic in chapter II.2.1). By I-V characterization the breakdown field E_{BD} of the insulator can be obtained from the breakdown voltage V_{BD}. Since the I-V characteristics, and especially the breakdown field E_{BD}, are strongly dependent on the morphology of the insulator, including extrinsic effects as shown in figure II.37, it is difficult to obtain intrinsic values.

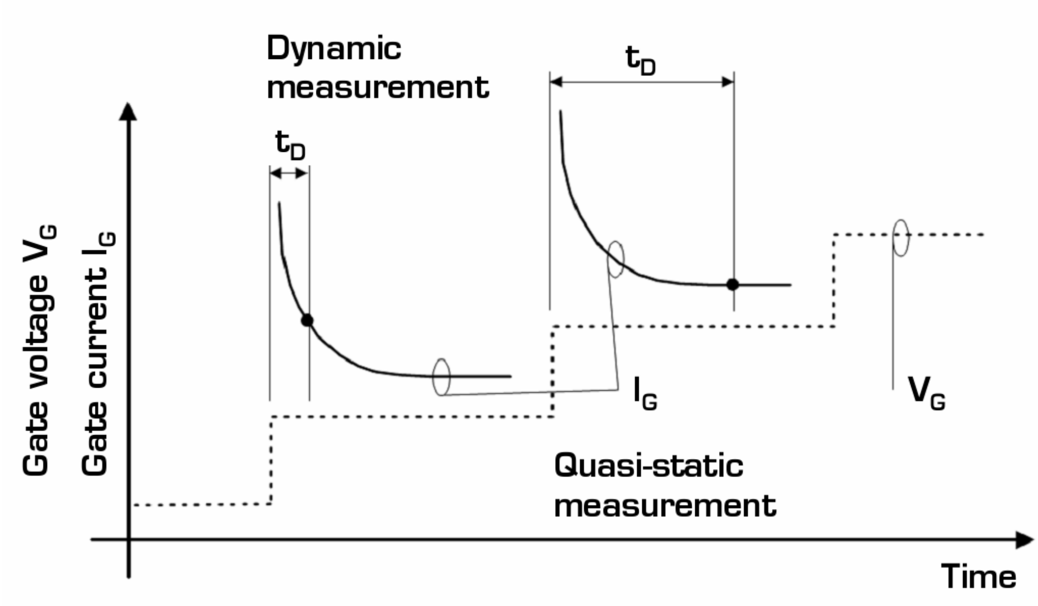

Figure II.36: Principle of the dynamic (left) and quasi-static (right) I-V characterization.

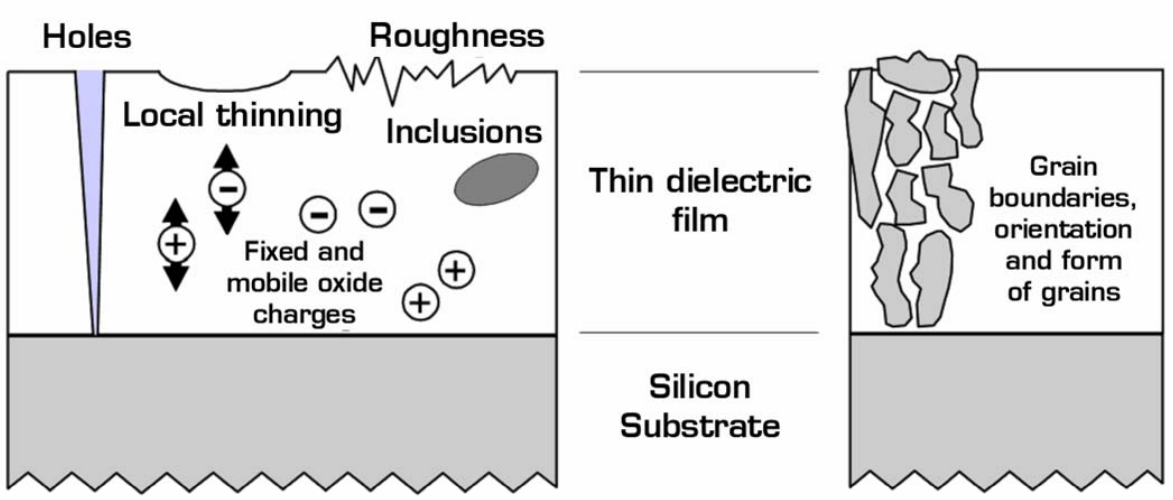

Figure II.37: Possible extrinsic effects on the I-V characteristics of a thin insulator due to film morphology. Grain boundaries, as well as orientation and form of single grains (right schematic), are only of interest for poly-crystalline films.

II.3.2.4 Electrical work function extraction

The work function of a metal or a metal compound is defined as the minimum energy required to extract an electron from the crystal lattice of the metal to vacuum. As outlined in chapter II.2.2, finding a metal with the correct work function is of fundamental importance, since this value directly yields the flatband voltage of the (ideal) MOSCAP, and thereby the threshold voltage of the corresponding MOSFET.

Reconsidering figure II.6(b), for ideal MOS structures at zero applied voltage (V = 0), the work function difference between the work function of the metal and the semiconductor ϕ_{MS} is zero [8,10]:

$$\begin{aligned} \phi_{MS} &= \phi_M - \left(\chi + \frac{E_g}{2q} - \psi_B \right) = 0 \text{; n-MOS} \\ \phi_{MS} &= \phi_M - \left(\chi + \frac{E_g}{2q} + \psi_B \right) = 0 \text{. p-MOS} \end{aligned} \qquad \text{II.46}$$

In practice, the fermi levels of the gate electrode and the substrate are misaligned by an energy difference, and a voltage (V ≠ 0) has to be applied to bring the fermi levels into alignment. Additionally, high-κ dielectrics usually exhibit fixed charge Q_{OX} that can be related to the measured V_{FB} by the expression [10]

$$V_{FB} = \phi_{MS} \pm \frac{Q_{OX}}{C_{Acc}} = \phi_{MS} \pm \frac{Q_{OX}}{\varepsilon_0 \kappa} t . \qquad \text{II.47}$$

By extracting the work function of the metal from C-V measurements, the V_{FB}-EOT method is probably the most widespread one. In order to extract the difference in work function between the metal and the silicon surface, a set of several oxide thicknesses is required to extrapolate its value, which is defined as the y-axis intercept [101]. This measurement is very straightforward to use, but it offers some several drawbacks, such as varying charge density, or the difficulty of a precise oxide thickness measurement. Additionally, a possibly interfacial SiO_2-layer has to be taken into account.

V_{FB} can also be determined by a method proposed by *Ricco* et al. [102], what in a next step allows to obtain ϕ_M by equations II.46 and II.47. Nevertheless, such methods have to be applied advisedly, because they have been originally developed for SiO_2 gate dielectrics [96].

More details on the above mentioned methods will be given in part IV of this thesis, when they are to be applied. For further information, reference [96] obtains a valuable and more extended overlook about this topic.

PART III: EXPERIMENTAL WORK

III.1 Substrate pre-treatment

The substrates we used for device fabrication are slices from commercially available p-doped (100)-silicon wafers. The (100)-surface is not a cleavage surface and is typically obtained by cutting single crystals along planes as close as possible to (100). The resulting rough surface is then chemo-mechanically polished (CMP) with colloidal SiO_2 dispersed in KOH aqueous solution [103]. Even though commercially available wafers can be described as “clean”, they have to be cleaned prior to gate oxide deposition, since metallic and organic contamination can never be totally excluded.

The high-κ gate stack commonly represents a multilayer structure including a deposited high-κ film and – in most cases – a SiO_2 layer at the interface with the Si-substrate. This interfacial layer is created during surface preparation or by the oxidant during high-κ film deposition and post deposition annealing [104]. Its composition and quality are highly dependent on the surface treatments before the high-κ deposition [105]. Investigations demonstrate that the interface layer is critical for inversion layer mobility and EOT-scaling [106].

The “RCA-clean” [107], developed in 1965, still forms the basis for most actual cleaning procedures, and is in modified forms still widely used in industry. A typical sequence is as follows:

1) Sulphuric acid/hydrogen peroxide/deionized (DI) water mixture (SPM; $H_2SO_4/H_2O_2/H_2O$ at 70 °C – 130 °C; often called as "piranha clean”). This step is used for removal of heavy organics and is often followed by a dip in diluted hydrofluoric acid (DHF).

2) “Standard Clean 1 (SC1)” uses an ammonium hydroxide/hydrogen peroxide/DI water mixture (APM; $NH_4OH/H_2O_2/H_2O$ at 60 °C – 80

°C). APM oxidizes and slightly etches to undercut and remove particles from the surface; it removes organic-, and additionally some metallic contaminants. The simultaneous oxidation and etching of the silicon surface may generate surface roughness.

3) "Standard Clean 2 (SC2)" uses a hydrochloric acid/hydrogen peroxide/DI water mixture (HPM; $HCl/H_2O_2/H_2O$ at 60 °C – 80 °C). HPM removes metallic contaminants from the silicon substrate and acts as an oxidizing agent.

DI water (also referred as "Ultra-pure water (UPW)") is used to dilute chemicals and to rinse solutions from wafers after chemical cleans. Ultrasonic (US) vibrations can enhance the particle removal efficiency. The compositions (1:1:5 to 1:2:7 for APM; 1:1:6 to 1:2:8 for HPM) and the order of the steps can vary, but all the wafers are rinsed in UPW after every chemical immersion. In many forms, the last step is a DHF-dip ("HF-last") to remove any residual chemical- or native oxide. Table III.A summarizes the cleaning sequence performed within this work prior to gate oxide deposition.

After this cleaning procedure, the samples are to be transferred into the MOCVD-system as fast as possible, to keep the actual surface characteristics of the wafer-slices as stable as possible. Details on the high-κ oxide deposition by MOCVD will be given in the next chapter.

Wet cleaning is continuously improved. This has two reasons: on one hand, it is of high economic interest, since it accounts for an important share of the total chemical consumption of a semiconductor fab, and any small improvement in chemical usage has a large overall effect. On the other hand, as already issued in the first paragraph of this chapter, is the resulting device performance improved by an improved gate oxide/Si-substrate interface.

Interuniversitair Micro-Elektronica Centrum (IMEC) introduced a simplified cleaning process called “IMEC-clean” [108]. The first step uses a sulphuric acid/ozone mixture to remove organic contamination and grow a thin chemical oxide. This step replaces the standard SPM step. The second step uses an optimized diluted HF/HCl mixture to remove particles, metal contamination, and chemical oxide, and to avoid HF-baths [107]. In case hydrophilic surfaces are preferred, a third step (an ozonated mixture, such as $DHCl/O_3$) can be added to regrow a thin passivating oxide layer. Such a surface avoids the reintroduction of metal contamination. The last rinsing step strongly determines the final surface contamination level, particularly for Calcium (Ca), which is especially important, since Ca degrades the gate oxide integrity [109].

Table III.A: Sequence of substrate cleaning prior to gate oxide deposition.

Step	Solution/Medium	Composition	Temp. [°C]	Time [min]
SPM[a]	H_2SO_4/H_2O_2	4:1	70 in US[e]	10
Rinse	DI water	-	RT[f]	-
APM[b]	$NH_4OH/H_2O_2/H_2O$	1:1:6	70 in US	10
Rinse	DI water	-	RT	-
HPM[c]	$HCl/H_2O_2/H_2O$	1:1:6	70 in US	10
Rinse	DI water	-	RT	-
Dry	N_2-blow	-	RT	-
DHF[d]	HF/H_2O	1:50	RT	0.5
Rinse	DI water	-	RT	-
Dry	N_2-blow	-	RT	-

[a] Sulphuric acid/hydrogen peroxide/DI water mixture

[b] Ammonium hydroxide/hydrogen peroxide/DI water mixture

[c] Hydrochloric acid/hydrogen peroxide/DI water mixture

[d] Diluted hydrofluoric acid

[e] Ultrasonic bath

[f] Room temperature

III.2.1 Experimental setup of the MOCVD process

MOCVD system:

The core of the MOCVD system is a commercially available, programmable hot-wall reactor from the company *ATV Technologie GmbH*. Hereon, a system for MOCVD working at atmospheric pressure (AP) has been developed. The setup has been carried out mainly by S. Harasek [86]. The working principle is schematically drawn in figure III.1. The process chamber (see figure III.2(a)) has a cylindrical shape; process gas inlet as well as process gas outlet are situated at the same side of the system. It can be heated to any chosen temperature up to 1100 °C, and is supplied by three individual gas lines that are shortly merged before they are introduced into the reaction chamber: One for the transport of the reaction gas oxygen (O_2) and two for the transport of the carrier gas argon (Ar). The carrier gas lines are piped over an electrically actuated 4-port valve, which allows switching between two modes within a sub-second range. During the "off-mode" the carrier gas flows directly into the chamber, during the "injection mode" the carrier gas flows through the heated bubbler (see figure III.2(b)), where it is saturated with the evaporated precursor. By this method, the precursor inflow can be controlled exactly.

Within this work, the deposition system has been graded up by an additional bubbler line that can be controlled separately (figure III.1). This opens the way to grow ternary oxides or stacked interlayer structures by simultaneously or alternatively injecting the individual precursors. Additionally, the various mass flows had to be optimized issuing film homogeneity improvements. In order to support the optimization, modeling and simulation carried out by a cooperative partner institution was applied.

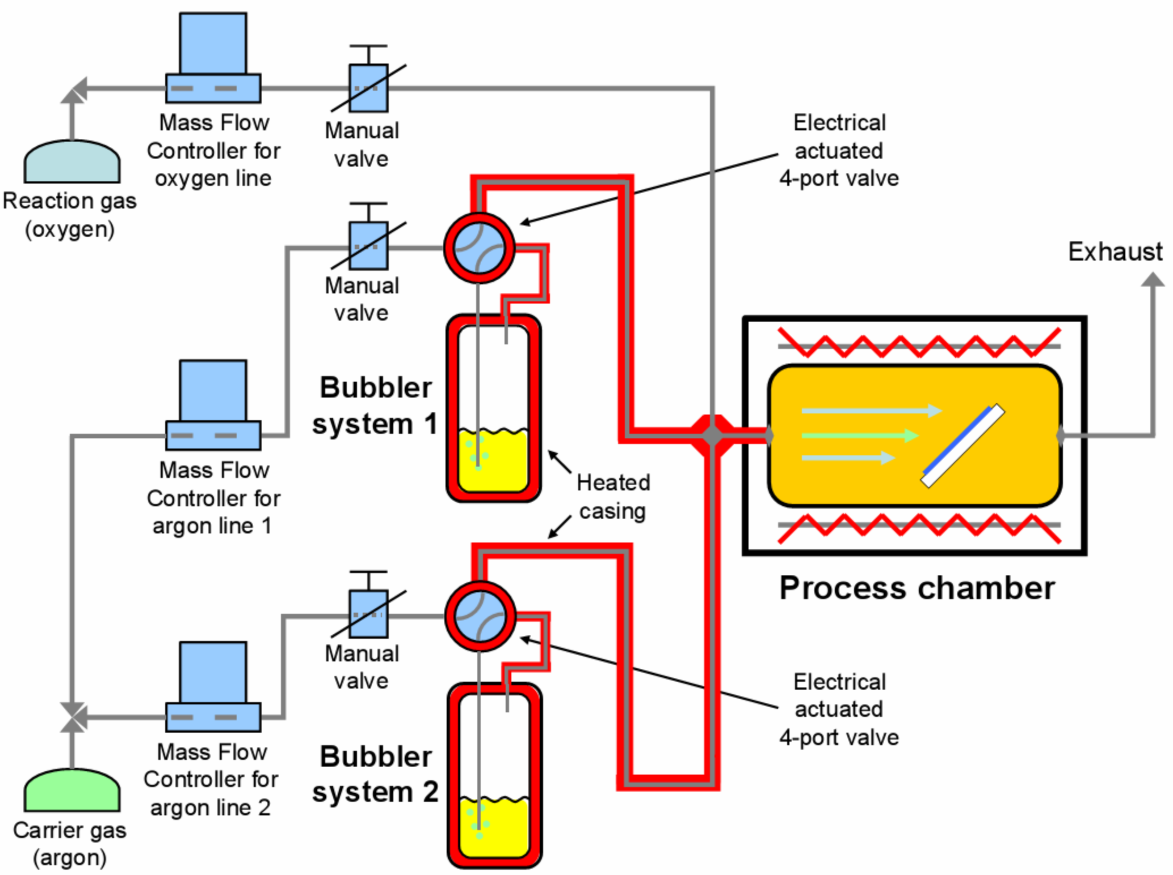

Figure III.1: Working principle of the AP-MOCVD system. Details ofthe process chamber and one of the bubbler-systems are shown in figures III.2(a) and (b).

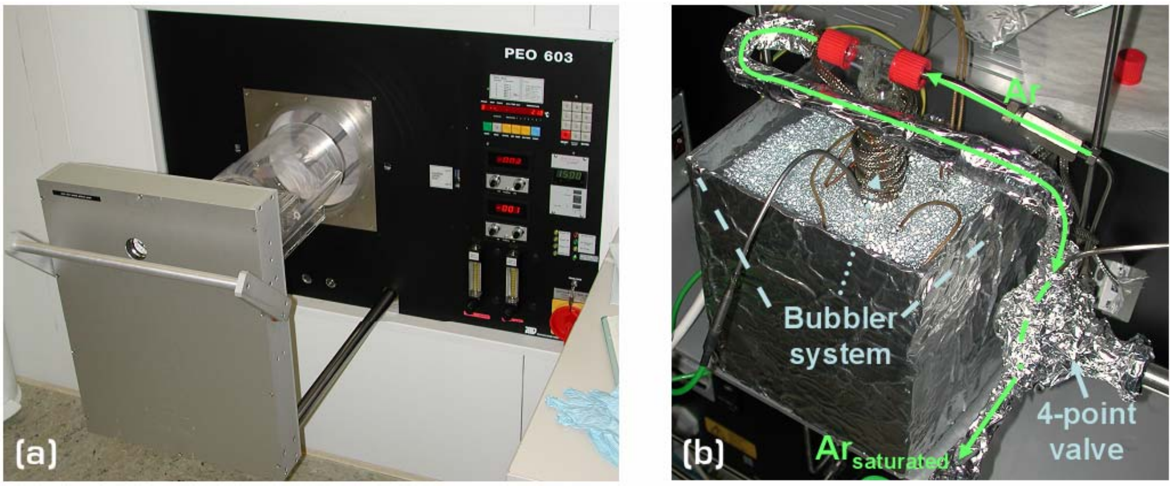

Figure III.2: (a) Programmable hot-wall reactor. The quartz-glass tube, where the CVD reactions take place, can be seen. Gas-supply is set up at the back. A single bubbler-system is shown in (b): Ar is introduced from the right and pipelined to the left, through the 4-port valve, into the reaction chamber.

Precursor substances:

As precursor we used Zirconium-trifluoroacetylacetonate [$Zr(C_5H_4O_2F_3)_4$, further denoted as “Zr(tfacac)”] and Hafnium-trifluoroacetylacetonate [$Hf(C_5H_4O_2F_3)_4$; “Hf(tfacac)”], respectively. The chemical formulas are respectively shown in figure III.3(a) and figure III.3(b). These substances show advanced stability towards unintentional hydrolysis and have sufficient volatility for a delivery at moderate bubbler temperatures (140 °C in our experiments). The already present Zr-O (Hf-O) bonds in the precursor molecule promote the formation of high quality thin films.

Deposition process:

As already mentioned, a pulsed inflow process has been developed. By this, the amount of precursor within the reaction chamber can be better controlled, thus leading to superior film stoichiometry and homogeneity. Additionally, precursor is saved, improving economic and environmental behavior. Temperature- and pulsing-time characteristics of a typical deposition process are shown in figure III.4. The optimum deposition conditions are summarized in table III.B.

The deposition temperature in all experiments has been set to 450 °C (with an accuracy of +/- 1.5 °C), which results in a maximum growth rate and a superior film characteristic, compared to deposition temperatures in the range from 350 °C to 550 °C [86]. The O_2/Ar-mass-

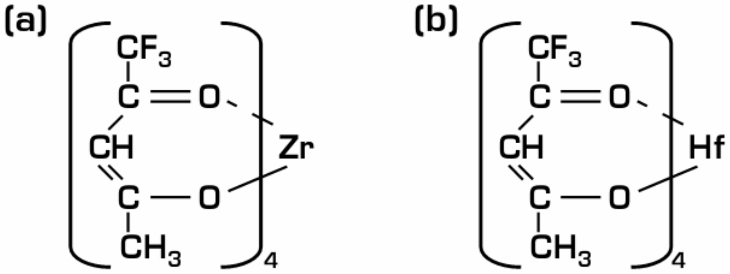

Figure III.3: Chemical structure of (a) Zirconium-trifluoroacetylacetonate [$Zr(C_5H_4O_2F_3)_4$] and (b) Hafnium-trifluoroacetylacetonate [$Hf(C_5H_4O_2F_3)_4$]. The dashed line symbolizes a weak bonding.

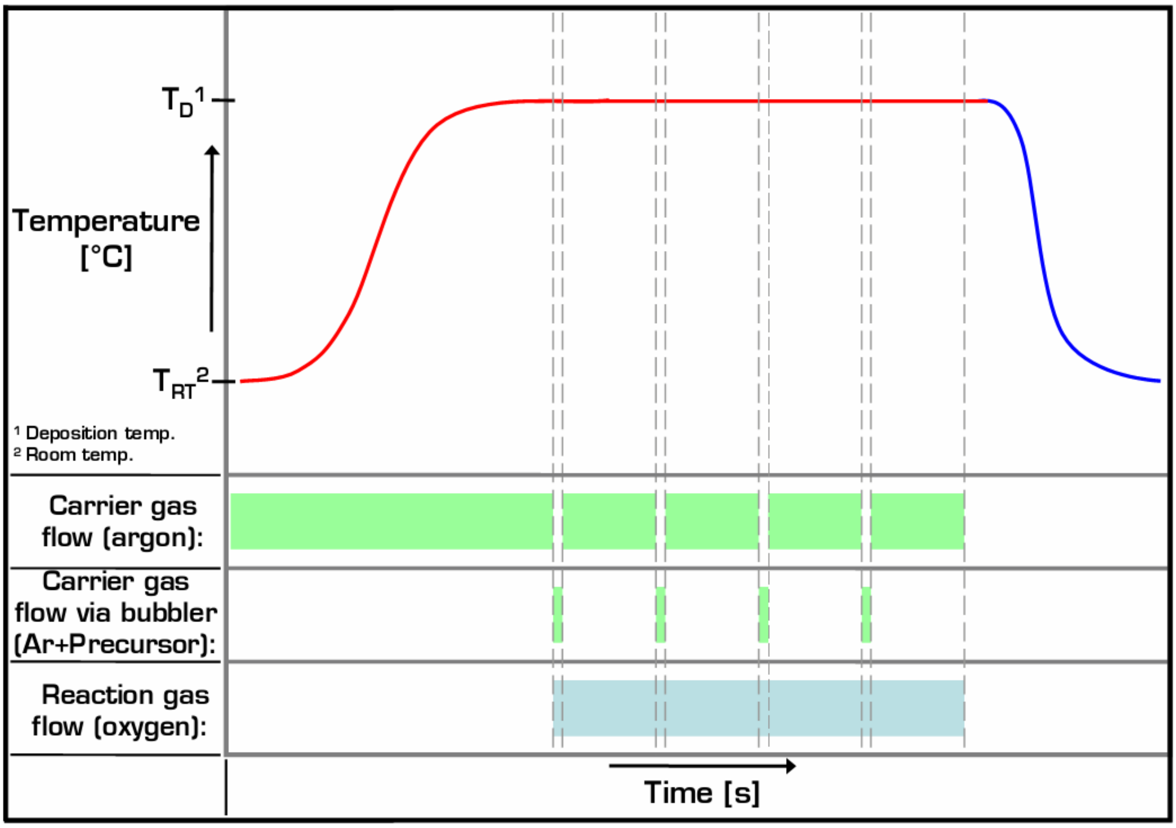

Figure III.4: Temperature profile and pulsing sequences of a typical MOCVD process. The duration of each single precursor-saturated argon pulse is 7 seconds.

flow ratio has been adjusted to 6/1. The samples are introduced on a specially constructed sample-holder positioned in the center of the quartz-glass tube, in line with the incoming gas flow. The sample holder allows exposing the substrate surface at an angle of about 45° to the gas-flow direction, which improves deposition homogeneity (see also chapter II.2.3.2).

Table III.B: Optimum process parameter for MOCVD deposition of ZrO_2, or HfO_2, from $Zr(C_5H_4O_2F_3)_4$, or $Hf(C_5H_4O_2F_3)_4$, respectively.

Bubbler temperature	140 °C
Deposition (Reactor) temperature	450 °C
Argon-flow (Carrier gas)	100 sccm[a]
Oxygen-flow (Reaction gas)	600 sccm[a]
Duration of single precursor-pulse	7 s

[a] denotes "standard cubic centimetre per minute"; 1 sccm = 0.018 mbar·l/s

We assumed our MOCVD process to take place within the *surface reaction limited regime* (see also chapter II.2.3.2): On one hand, we deposit at relatively low temperatures of 450 °C, and on the other hand, the growth rate exhibits temperature dependence [85]. Nevertheless, the resulting film thicknesses show differences up to about +/- 10 % from the average value, which is due to inhomogeneities of the reactant concentration in the reaction chamber (for further details, the reader is referred to [68] and [86]).

The resulting film thickness dependent on the precursor flow time at a deposition temperature of 450 °C is shown in figure III.5, including results for HfO_2, ZrO_2, and a mixture of both precursor substances leading to $Hf_xZr_{1-x}O_2$. It can be seen that the absolute scatter bar is decreasing with decreasing film thickness. Since we were interested in the deposition of very thin films (4 nm - 22 nm) and areas of interest of (1 x 1) cm², the resulting film homogeneity over this area is within our tolerance-limit.

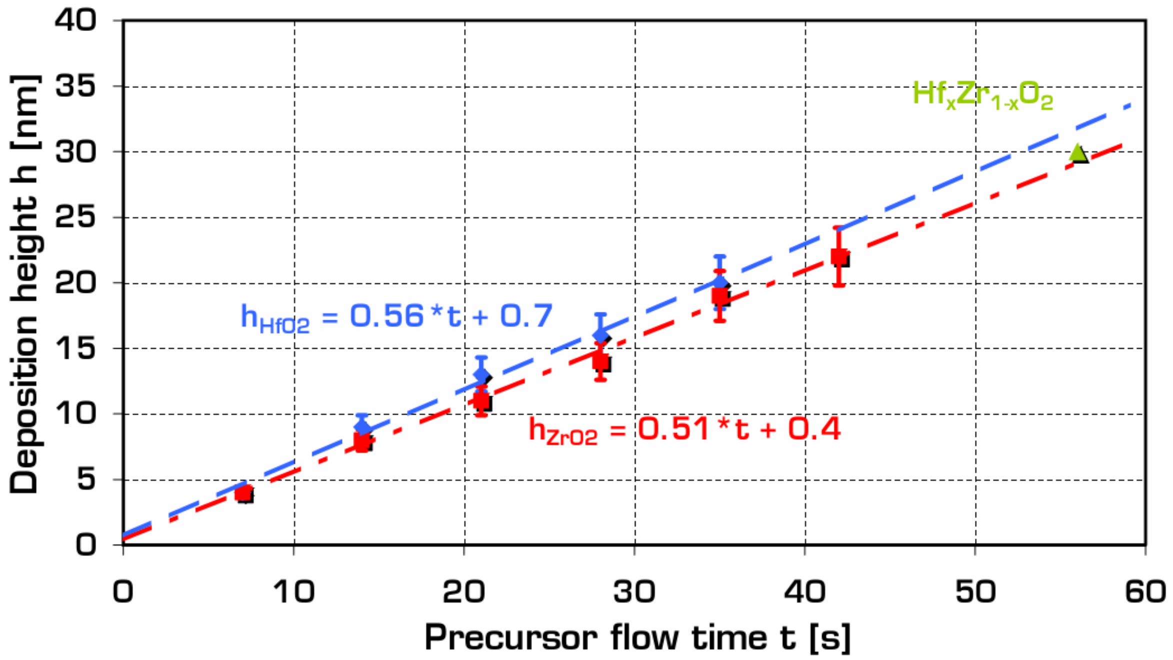

Figure III.5: Growth rate of MOCVD HfO_2, ZrO_2, and $Hf_xZr_{1-x}O_2$ deposited at 450 °C deposition temperature. The shown equations correspond to the respective trend lines and are of the form: h_{Oxide} [nm] = A [nm/s] · t [s] + B [nm], whereas A is the slope of the trend line and B is the y-axis intercept.

Table III.C: Comparison of various ZrO_2 thicknesses, measured by (**A**) SE in Vienna, by (**B**) SE in Aachen, and (**C**) by TEM.

Sample #	**Thickness A[a] [nm]**	**Thickness B[b] [nm]**	**Thickness C[c] [nm]**	
55	20 +/- 0.3	N.m.a.[d]	17.5 - 18	2 – 2.5
58	20 +/- 0.1	21	N.m.a.	N.m.a.
61	19 +/- 0.2	19	N.m.a.	N.m.a.
62	16 +/- 0.2	17	N.m.a.	N.m.a.
66	6 +/- 0.7	6	N.m.a.	N.m.a.
67	12 +/- 0.8	12	N.m.a.	N.m.a.
68	10 +/- 0.8	10	7.5 - 8	2 – 2.5
70	3 +/- 0.5	5	N.m.a.	N.m.a.
71	11 +/- 0.3	12	N.m.a.	N.m.a.
72	9 +/- 0.5	11	N.m.a.	N.m.a.
73	5 +/- 0.5	6	3.5	1.5

[a] Measured by *SOPRA GES5 Ellipsometer,* measurement inaccuracy is denoted
[b] Measured by *Philips PQ Ruby Ellipsometer*, values as obtained
[c] The first column gives the thickness of ZrO_2, the second on of the interfacial SiO_x
[d] Denotes: “No measurement available”

The thicknesses have been determined by spectroscopic ellipsometry (SE), applying a *SOPRA GES5 Ellipsometer*, and the maximum film inhomogeneity of about +/- 10 % is denoted by the scatter bars. For the reason that ellipsometry is an indirect measurement method that gains its results by comparing the measured data with a model (see also chapter II.3.1.1), we verified our data by three different methods: First, we referenced the data to the results obtained by S. Harasek in [85], second, we re-measured a series of films on a completely different ellipsometer (*Philips PQ Ruby Ellipsometer)* at *AMO GmbH* in Aachen, and third, we made

TEM-measurements[i] of various samples. Results for a series of ZrO_2 films are summarized and compared in table III.C. It can be seen that the data fits well, validating our SE measurements. Nevertheless, TEM measurements (details will be shown and discussed in chapters IV.1.3 and IV.2) reveal an interfacial layer of SiO_x - which is most likely SiO_2 - that can not be distinguished by our SE measurements. On this account, the SE measurements deliver the thickness of the total oxide stack, including both, the high-κ oxide as well as any possible interfacial layer.

III.2.2 Numerical simulation and modelling of the MOCVD process

To address the observed transport inhomogeneity within the reaction chamber, numerical simulation and modeling of the MOCVD process has been performed. This work has been performed in cooperation with C. Jordan, M. Harasek and the I*nstitute of Chemical Engineering* at the *Vienna University of Technology*[ii]. All simulations have been performed, using *Fluent* CFD software, that combines physically accurate transport models with proposed gas-phase and surface chemistry mechanisms, and predicts uniformity of film thickness and composition variation during selective growth [110].

Figure III.6 shows the reactor geometry as it has been implemented into the simulation software: The sample holder is indicated red, the inflow-gas tube blue, and the sample-carrier, measuring (4 x 4) cm² in

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[i] TEM measurements have been performed by Dr. Johannes Bernardi, at the *University Service Center for Transmission Electron Microscopy* (USTEM) of the *Vienna University of Technology*. http://www.ustem.tuwien.ac.at

[ii] Inst. f. Verfahrenstechnik, Umwelttechnik und Technische Biowissenschaften, TU Wien
Getreidemarkt 9 / 166, A-1060 Wien, http://www.vt.tuwien.ac.at

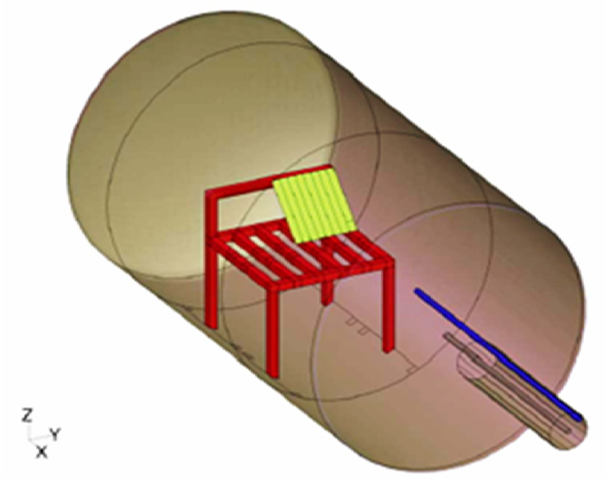

Figure III.6: Reactor geometry as implemented into simulation software, including sample holder (red), inflow-gas tube (blue) and sample-carrier (yellow).

dimension, yellow. As key-data for the simulation process, the experimentally obtained parameters summarized in table III.B have been used, the data on chemical media had to be estimated from mole mass or rather ideal gas theory as well as from kinetic gas theory. The CVD-process has been modeled using a laminar flow of an ideal gas, and the reactor walls have been set on deposition temperature on their outer side. Stationary as well as non-stationary simulations have been performed.

A stationary simulation result of the gas flow velocity during an inflowing gas pulse is shown in figure III.7(a). The velocity distribution shows a clear circularly focused geometry that keeps its narrow distribution until the gas flow hits the sample. Additionally, this velocity distribution of the incoming gas flow leads to a strongly flow-dependent precursor-concentration distribution in the reactor (see figure III.8(a)), resulting in inhomogeneities of the deposited film.

According to these results, we state a strong influence of the mass flow on the resulting deposition rate and have to consider – although we deposit at comparatively low temperatures – *mass transport limiting regime*. A reason therefore might be the relatively high reactor pressure. Figure III.7(b) draws the average precursor concentration during several cycles, summarizing non-stationary simulations. The pulsed inflow improves precursor-budget and –distribution, but does not have significant influence on the flow characteristics.

In a next step, we applied different showerhead-like flow barriers into the simulation model. Figure III.8(b) shows a snapshot of non-stationary simulation results after adapting a porous plate on the inflow-tube. It can be seen that velocity distribution is clearly more uniform than in the case without a flow barrier, and that we are able to homogeneously cover the whole sample by an inflowing gas pulse.

The use of a simulator to optimize MOCVD of high-κ materials enabled us to gain a better understanding of the experimental set up and the furnace design, and additionally gave us a toll to optimize film quality. The results of this work have been published in [111].

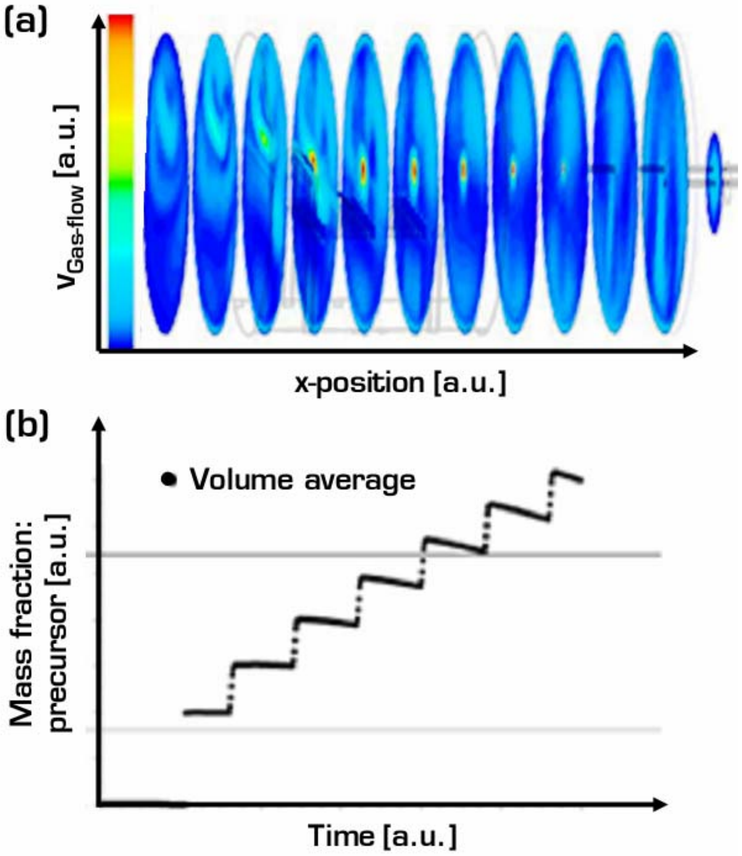

Figure III.7: (a) Contours of velocity magnitude in the MOCVD reactor (stationary simulation). (b) Average mass fraction of precursor during several cycles (non-stationary simulations).

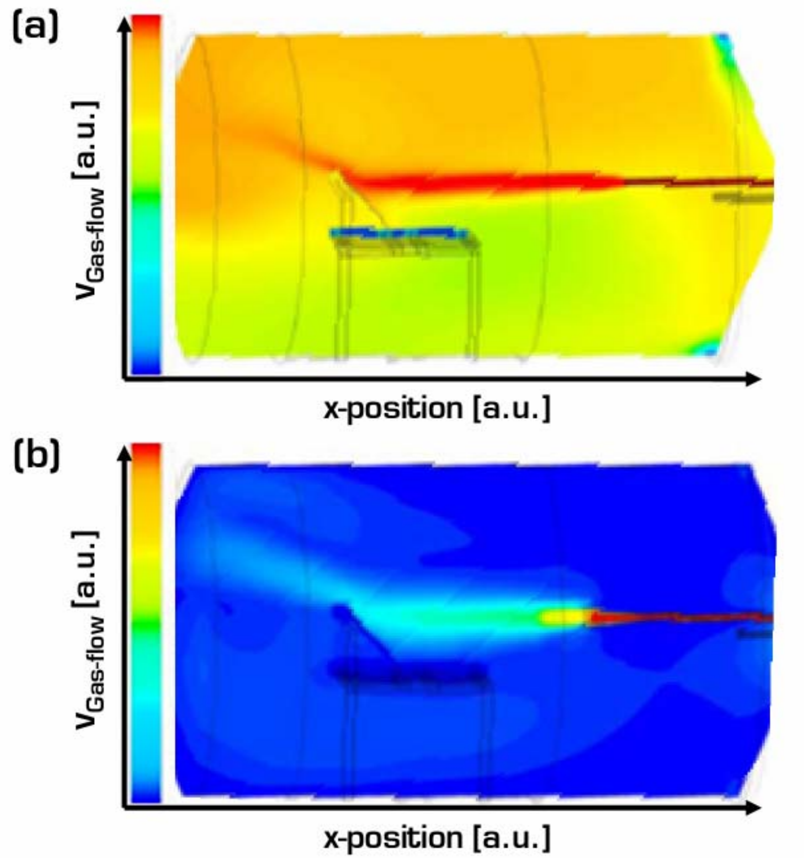

Figure III.8: Contours of velocity magnitude before (a) and after (b) applying a showerhead-like flow-barrier in the MOCVD reactor (non-stationary simulations).

III.3 Fabrication and electrical characterization of MOS capacitors

III.3.1 Gate electrode deposition and patterning

As already mentioned in chapter II.2.3.3, a metal gate electrode has to be deposited onto the gate dielectric and patterned, to complete MOS capacitors. Main tasks of the *Network of Excellence (NoE) Sinano* are based on "Joint Processing Activities (JPA)" and "Joint Characterization Activities (JCA)", whereat different parts of processing or characterization are accomplished by different project partners. Hence, deposition and patterning of the metal gate electrode was done at our institution as well as at the *Advanced Microelectronic Center Aachen (AMICA)*[i], and at the *Institute of Solid State Electronics* at *Uppsala University*[ii]. The work in Aachen has been performed by the author of this thesis during a one month enduring exchange.

Metal gate deposition and patterning of samples in Vienna and Aachen has been accomplished by a lift-off process (see figure II.24(c)). Aluminium (Al) has been either evaporated or sputter deposited, nickel (Ni) has been sputter deposited, and titanium-nitride (TiN) has been sputter deposited by a reactive sputter process, using nitrogen as the reaction gas. Processed film thickness has been consistently set to around 100 nm and at least two different gate areas have been deposited, to verify the resulting capacitance/area of the MOSCAPs. In all processes, deposition systems that have been used are commercially available, and include:

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[i] Advanced Microelectronic Center Aachen (AMICA), AMO GmbH, Otto-Blumenthal-Str. 25, 52074 Aachen, Germany

[ii] Solid State Electronics, Ångström Laboratory, Uppsala University, Box 534, SE-751 21 Uppsala, Sweden

- *Von Ardenne CS730 Cluster system (Aachen)*
- *Pfeiffer Vacuum Classic 580 (Aachen)*
- *Balzers-Pfeiffer evaporation system PLS 500 (Vienna)*
- *Pfeiffer sputter system LS 320 (Vienna)*

The performed lift-off process is summarized in table III.D, whereat “Metallization” refers to one of the processes described above.

In Uppsala, metal gate deposition and patterning of samples has been done by Dr. G. Sjöblom, using selective etching of the pre-deposited metals (see figure II.24(b)). The used deposition system was a *Von Ardenne CS730 Cluster system*, similar to that one applied in Aachen. The investigated metals contain titanium-nitride (TiN), TiN_x (Ti-rich), and molybdenum (Mo). The back-etching of the various metals was done by inductive coupled plasma (ICP) dry etching, whereat a mixture of boron-chloride/chlorine (BCl_3/Cl_2) has been used to etch TiN and TiN_x, and a sulphur-hexafluoride/argon (SF_6/Ar)-mixture has been applied to etch Mo. Further information on the processing can be found in [101].

Additionally, to enable electrical characterization, an ohmic backside contact has to be fabricated. This has been done, by either evaporating or sputtering a metal film – in our case Al – onto the backside of the sample, or by simply roughening the backside of the sample and sticking it with conductive silver paste onto a copper plate. The resulting MOSCAP is schematically shown in figure III.9, whereat the measurement principle by a thin conductive tip, as we performed it throughout our electrical characterizations, is indicated. The results of the various high-k/metal- gate stacks are presented and discussed in part IV of this work.

Table III.D: Sequence of lift-off process for deposition and patterning of metal gate electrodes.

Step	Object/Medium	Rotation [rpm][a]	Temp. [°C]	Time [s]
Pre-Bake	Sample	-	150	240
Spin-coat primer	LOR 3A lift-off resist	2500	RT[b]	30
Post-Bake primer	Sample/resist	-	150	120
Spin-coat resist	AZ 5214E resist	1500	RT	30
Post-Bake resist	Sample/resist	-	95	90
UV[c]-Exposure	Resist	-	RT	4 – 10[d]
Reverse resist	Sample/resist	-	115	120
UV-Flood-Exposure	Resist	-	RT	~ 25[d]
Develop resist	MF86MX	-	RT	60 - 70
Metallization[e]	-	-	-	-
Lift-off resist	Acetone	-	RT/US[f]	-
Develop primer	MF86MX	-	RT	~ 10
Dry	N_2-blow	-	RT	-

[a] Rotations per minute
[b] Room temperature
[c] "Ultra Violet"
[d] Depending on mask aligner and settings
[e] See metal gate deposition processes
[f] Ultrasonic bath

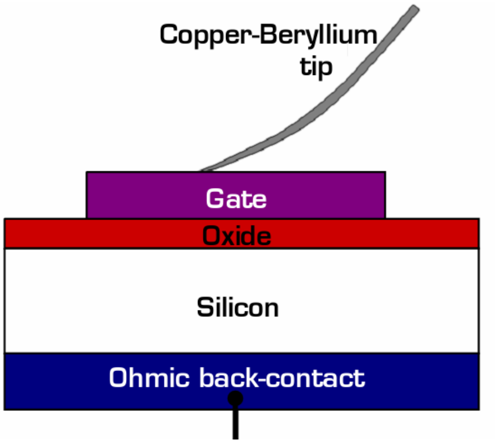

Figure III.9: Schematic of a MOS capacitor under test. The device is contacted at the gate electrode by a fine copper-beryllium tip and at the backside by a conductive silver paste/copper plate contact.

III.3.2 Electrical characterization

The fundamentals of electrical characterization methodology, as well as of the discussion of the obtainable results are already addressed in chapter II.3.2.

Capacitance-voltage (C-V) and current-voltage (I-V) measurements in Vienna have been performed at a wafer probing station from *Karl Suess*, in Aachen at a *Cascade Microtech* semiautomatic probe station. In both cases, the systems are equipped with:

- *Agilent Semiconductor parameter analyzer (4156B)*
- *Agilent pA-meter (4140B)*
- *Agilent Precision LCR-meter (4284A)*

that can be controlled by personal computer-supported measurement software. In Uppsala additional electrical characterization has been made, and the reader is referred to [101].

The obtained results will be addressed and directly discussed in part IV of this thesis.

III.4) Thermal treatment (Annealing)

The fundamental change concerning the high-κ oxides is that they are deposited oxides and not native ones. This integration of a heterogeneous material causes immense technological challenges, especially concerning the deposition process. The fundamentals of thin film technology are described in chapter II.2.3.

Thin film deposition by CVD or ALD on crystalline silicon may suffer from a series of defects (see also figure II.30), which can be summarized as follows:

1. **Interface defects/states**, due to:
    a. insufficient interface matching (e.g. dangling bonds, broken bonds, stacking faults)
    b. thermodynamical instability/phase transition at the interface (e.g. dangling bonds, broken bonds, stacking faults)
    c. substrate or reactor contamination (e.g. inclusions/ precipitates, voids)

2. **Oxide defects/traps**, due to:
    a. non stoichiometry of the oxide, mainly by imperfect growth processes (e.g. vacancies, interstitials)
    b. insufficient chemical reactions of the precursors during the growth process (e.g. precipitates, voids)
    c. substrate or reactor contamination (e.g. inclusions/ precipitates, voids)

The above mentioned defects are likely solely thermally activated and may thereby be reduced or – in the ideal case – eliminated by a thermal treatment. By applying such a temperature treatment under a specific atmosphere, one may enhance the annealing process. An oxidizing atmosphere for example, may reduce contaminants, especially carbon. On the other hand, a reducing atmosphere containing hydrogen (e.g. forming gas atmosphere (FGA)) can anneal charges like interface trapped charge or oxide trapped charge (see also chapter II.3.2.1).

Additionally, such thermal treatments shall give information on the thermal and thermodynamical stability of the investigated material systems. This is in so far important, as by implementing such materials into actual CMOS processing, the materials have to withstand temperatures up to about 900 °C.

Fortunately, most of the above described defects represent charges within the oxide, and hence are in electrical communication with the underlying silicon. Therefore, they can be qualitatively and possibly also quantitatively characterized by electrical characterization (for details, see chapter II.3.2). Chemical stoichiometry or contaminants can be characterized by physico-chemical methods described in chapter II.3.1.

Thermal annealing at different process-stages can be applied after the oxide deposition (Post-deposition annealing (PDA)), or after the metallization process (Post-metallization annealing (PMA), and rapid thermal annealing (RTA)).

Preparatory work containing the impact of different annealing processes has been made by S. Harasek and can be found in [86]. Figure III.10 shows the effect of various annealing treatments on Al/ZrO_2/p-Si capacitors, whereat the gate oxide has been deposited at 450 °C. The not annealed C-V characteristics show distinctive frequency dispersion and no increase of the low-frequency (LF) curve in inversion. After annealing in inert and oxidizing atmosphere at 650 °C, the characteristic is clearly improved, showing decreased frequency dispersion, as well as an increase of the capacitance in inversion for the LF-measurements.

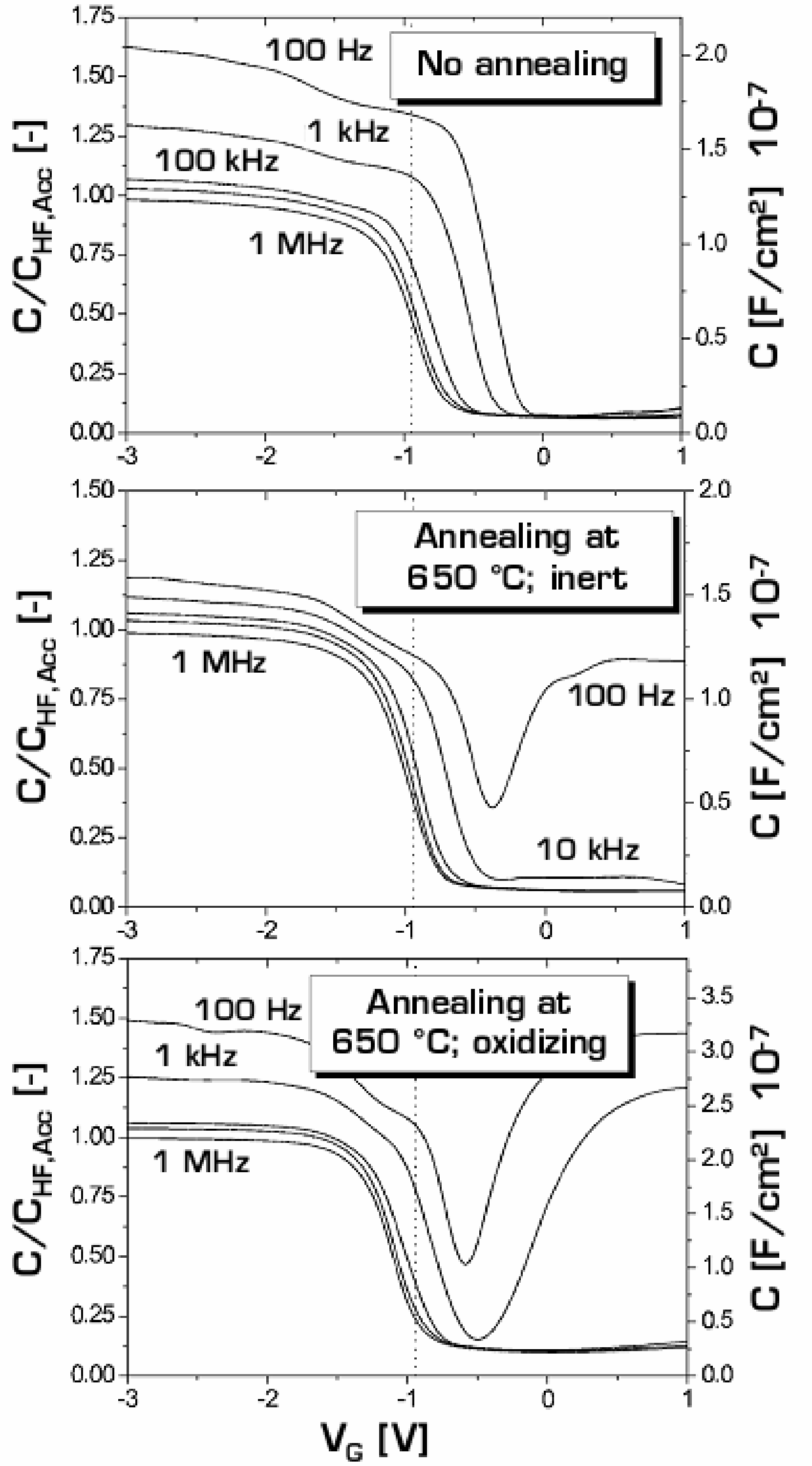

Figure III.10: C-V characteristics of Al/ZrO$_2$/p-Si capacitors after different thermal treatments. The punctuated line indicates the 'ideal' value of V$_{FB}$ (-0.95V) (adapted from [85]).

Based on these results and on literature, we exposed our samples to three temperature treatments:

- PDA at 650 °C in FGA (10% H_2 in N_2) for 5 minutes
- PMA at 400 °C in FGA for 30 minutes, or
  PMA at 450 °C in FGA for 30 minutes
- RTA at 800 °C in Ar-atmosphere for 10 seconds, or
  RTA at 950 °C in N_2-atmosphere for 5 minutes

Hereby, we compared the oxide- or device characteristics by physico-chemical-, and electrical characterization before and after the single annealing steps. Not all samples have been exposed to all, or the same thermal treatments. Table III.E summarizes the thermal processing schemes that have been applied to the investigated material systems. The impact on the resulting physico-chemical and electrical characteristics will be shown in the following chapters of this thesis.

Table III.E: Summary of applied thermal processing schemes for various gate stacks. Applied steps are shaded with annealing temperature quoted.

Gate stack	PDA[a] in FGA[d] 5 min[f]	PMA[b] in FGA 30 min	RTA[c] in Ar/N_2[e] 5 min/10 s[f]
Al/ZrO_2/p-Si	650 °C	400 °C	not applied
Ni/ZrO_2/p-Si	650 °C	400 °C	not applied
Mo/ZrO_2/p-Si	650 °C	450 °C	950 °C; 10 s
TiN/ZrO_2/p-Si	650 °C	450 °C	800 °C; 5 min
TiN/ZrO_2/p-Si	650 °C	450 °C	950 °C; 10 s
Mo/HfO_2/p-Si	650 °C	450 °C	950 °C; 10 s
TiN/HfO_2/p-Si	650 °C	450 °C	950 °C; 10 s

[a] Post Deposition Anneal
[b] Post Metallization Anneal
[c] Rapid Thermal Anneal
[d] Forming Gas Atmosphere
[e] Argon-/Nitrogen-Atmosphere
[f] Minutes/Seconds (Duration of Anneal)

PART IV: RESULTS AND DISCUSSION

IV.1 Physico-chemical properties of the gate oxides

In this chapter, we will discuss the physical and chemical characteristics of the deposited gate oxides. The obtained results give information on the fundamental properties of the processed thin films, and therefore evaluate them regarding their potential to optimize these properties by improving the experimental methodology. As a first milestone, it has been planned to successfully reproduce the superior results achieved in [86]. Constitutive on these results, the process flow has punctually been adapted. Details on the final deposition and annealing processes as well as on growth rate and resulting thickness of the films are given in chapter III.2.1 and chapter III.4.

IV.1.1 Chemical composition

The first fundamental parameter is the chemical composition of the deposited films. It is of essential necessity that one is able to grow stoichiometric reliable and reproducible films that exhibit the desired chemical composition. The chemical composition of the deposited films has been analyzed by Auger-electron spectroscopy (AES; for details see chapter II.3.1.2)

In the case of **ZrO_2 deposition from Zr(tfacac)**, we were able to fall back on the data obtained by S. Harasek. In his work [86], the deposition at 450 °C has been identified as the superior deposition temperature for the MOCVD-process. Figure IV.1(a) shows the chemical composition, obtained by AES measurements, of as-deposited ZrO_2 thin films, grown at

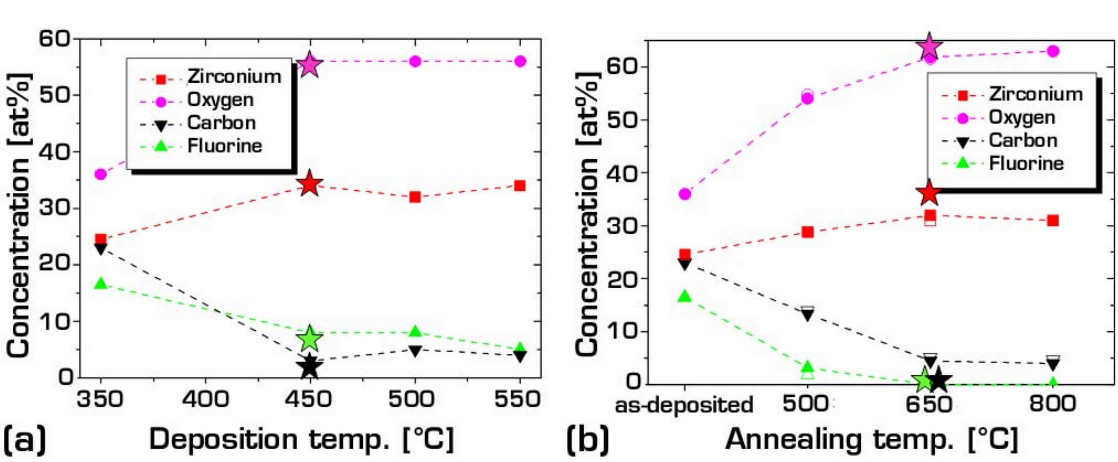

Figure IV.1: Chemical composition obtained by Auger electron spectroscopy of ZrO_2 thin films as a function of (a) deposition temperature, and (b) of post-deposition annealing temperature. The as-deposited samples in (b) have been grown at 350°C. The "common" measurement values are taken and adapted from [85]; the "stars" indicate the values obtained in this work. Symbol size exceeds measurement inaccuracy (1 - 2 at%).

various deposition temperatures, while applying the process scheme given in chapter III.2.1. The measurement points give the atomic concentration (at%) of the predominant elements in the characterized thin films obtained in [86]. The stars indicate the chemical composition obtained during this work. It can be seen that we successfully achieved to reproduce the chemical composition of the films, deposited at 450 °C. Still, one can see that the as-deposited films incorporate about 3 at% carbon (C)-, and about 7 at% fluorine (F) impurities, most likely originating from not decomposed precursor substance, and that the Zr/O-ratio (34 at%/56 at%) is not perfectly stoichiometric ZrO_2.

Based on the results in [86], we applied post deposition annealing to the samples in forming gas atmosphere (10% hydrogen in nitrogen) at 650 °C for 5 minutes. The chemical composition obtained by AES are shown in figure IV.1(b). No remaining C-, or F-content has been detected within the measurement inaccuracy of 1 at% - 2 at%, and the films exhibit almost ideal stoichiometry (Zr/O-ratio = 36 at%/64 at%). From these results we can state that after deposition at 450 °C, applying the process parameters given in table III.B and the annealing procedure described above, we obtain reproducible and almost stoichiometric ZrO_2 films.

In the case of **HfO_2 deposition from Hf(tfacac)**, we have not been able to quantitatively characterize the chemical composition of the films, since the cooperative institution that performed the Auger measurements was confronted with technical problems. Nevertheless, we qualitatively detected the elements Hf, O, as well as C, and F in the case of the as-deposited samples. Comparing these results with the ones obtained from the ZrO_2 samples and taking the similarity of the used precursor substance into account, we are able to assume that we obtain reproducible and almost stoichiometric HfO_2 films.

IV.1.2 Topography

The topography of the grown films has been investigated by atomic force microscopy (AFM; for details see chapter II.3.1.3). The MOCVD growth at different temperatures leads to different and distinctive surface characteristics. The pictures show accidentally arranged grains that are homogeneous in size and shape, whereas these parameters are dependent on the growth temperature (Further details can be found in [86]). Figure IV.2 gives an example for a 3-dimensional view of an AFM image by the means of an 8 nm thick ZrO_2 film, deposited at 450 °C. Lateral and vertical scales are similar, to give an impression of the present surface roughness, which is an important characteristic for thin films, since it influences the electronic behaviour of the dielectrics. The average roughness R_a of the given example is about 0.9 nm. R_a is given by the expression

$$R_a = \frac{1}{N} \cdot \sum_{i=1}^{N} \left| h_i - \overline{h} \right| , \qquad \text{IV.1}$$

whereat h_i are the single measured height-values, whose overall number is N, and $\overline{h}$ is the arithmetic mean value given by the expression:

$$\overline{h} = \frac{1}{N} \cdot \sum_{i=1}^{N} h_i \ . \qquad \text{IV.2}$$

This value is by all means significant for the thickness range (4 nm to 22 nm) of the films investigated during this work. Table IV.A summarizes the obtained roughness values for ZrO_2, HfO_2, and $Hf_xZr_{1-x}O_2$ thin films deposited at 450 °C.

Beside on the deposition temperature dependence, the obtained roughness values also depend on the grown film thickness, which is shown in figure IV.3. The data is taken from [86], whereat the range of values obtained within the present work and given in table IV.A is marked by the red star. One can see that the roughness increases almost linearly with increasing film thickness and that the films deposited at 450 °C tend to be smoother than films deposited at different temperatures. As shown in [86], post deposition annealed samples are expected to exhibit reduced average roughness values as low as 0.3 nm to 0.4 nm.

Table IV.A: Summary of roughness values for different MOCVD thin films deposited at 450 °C, obtained from AFM-measurements.

Oxide material:	**ZrO_2**	**$Hf_xZr_{1-x}O_2$***	**HfO_2**
Physical oxide thickness range [nm]	4 - 22	30	8 - 27
Average roughness R_a range [nm]**	0.5 – 1.0	0.64	0.5 – 1.0

* Only one thickness characterized

** Values do not linearly coincidence with rising film thickness and additionally depend on AFM-image quality as well as on the scan-size of the image!

Comparing these values to literature, they can even compete with ZrO_2 thin films deposited by atomic layer deposition (ALD) [112,113][i].

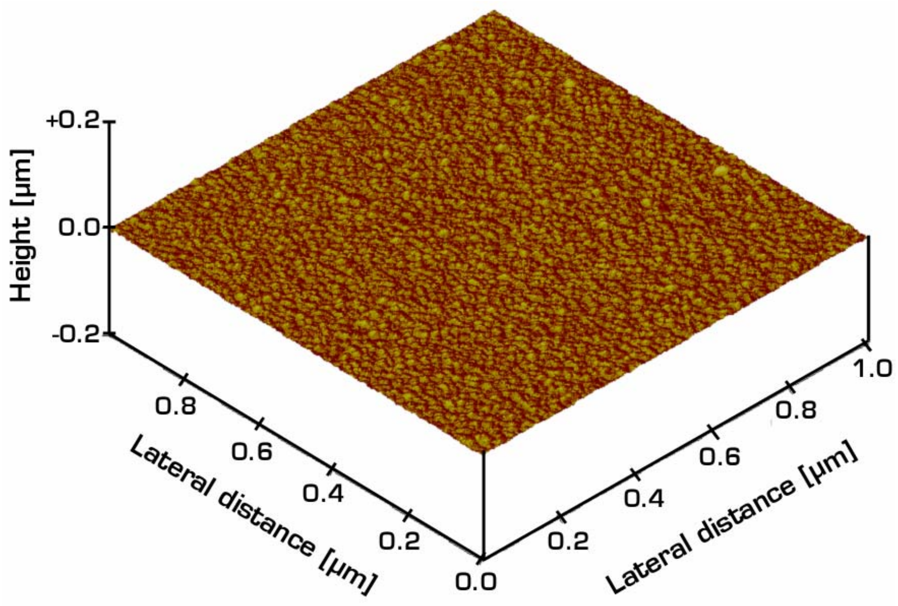

Figure IV.2: AFM-image of an 8 nm thick ZrO_2 film, deposited at 450 °C. The average roughness R_a is about 0.9 nm.

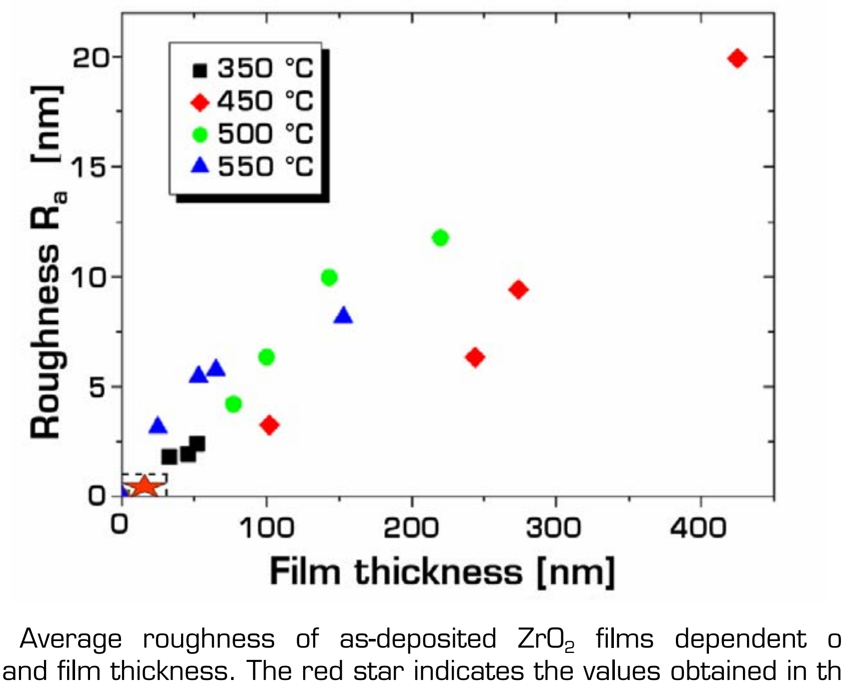

Figure IV.3: Average roughness of as-deposited ZrO_2 films dependent on deposition temperature and film thickness. The red star indicates the values obtained in this work.

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[i] Though, these references have been published in the very beginning of ALD and growth processes might still have been incorporating a CVD-component.

IV.1.3 Morphology

To get a clear impression about the morphology of the finalized gate stacks, high-resolution transmission electron microscopy (HR-TEM) measurements have been performed. Figure IV.4 shows a HR-TEM image of a Mo/ZrO_2/p-Si gate stack after PDA, PMA and RTA. The metal gate electrode, which is about 150 nm thick, and has been deposited by sputter deposition, shows a columnar polycrystalline structure. The gate oxide consists of two different layers, the intended ZrO_2 high-κ layer and an unintended interfacial SiO_x layer, which is most likely SiO_2. The high-κ layer exhibits fine-grained polycrystalline characteristics, whereas the SiO_2 is clearly amorphous. Former investigations from Balog et al. [114] as well revealed that by the deposition of thicker films, using the same precursor substance, fine-grained, nearly stoichiometric monoclinic ZrO_2 films are obtained. In the cited work [114], the authors do not state any influence of annealing up to temperatures of 1100 °C.

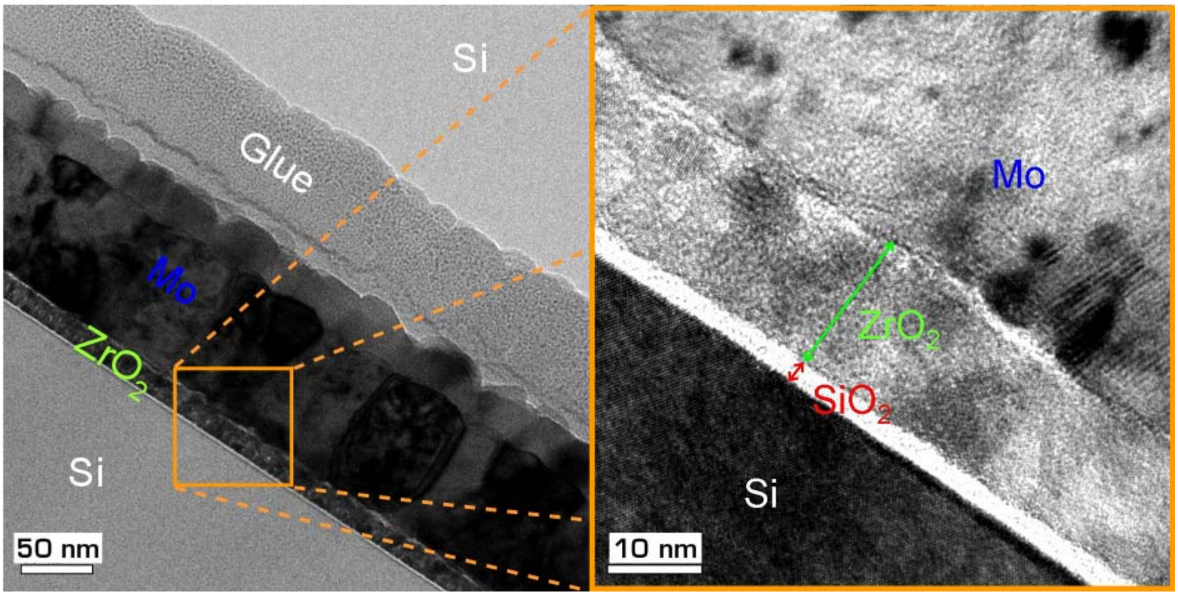

Figure IV.4: Cross section HR-TEM image of a Mo/ZrO_2/p-Si gate stack. The overall thickness of the gate oxide is ~ 20 nm incorporating a ~ 1.5 nm – 2 nm thick interfacial SiO_2 layer. The right image is the magnified section of the left image.

Since we deposited and investigated very thin films, we assumed to obtain amorphous films, or such ones that do not exhibit a pronounced polycrystalline structure. For the reason that we only had the possibility to investigate samples by HR-TEM that have already been annealed (see also chapter III.4), we have to make the following assumptions/conclusions:

- We processed on “HF-last” prepared samples, what means that we suppose to be free of any native SiO_2 when introducing the Si-samples into the MOCVD system. The fact that we reveal interfacial SiO_2 in HR–TEM images suggests that either SiO_2 already grows during the deposition process, or - which is believed in literature [104] – that it arises from the diffusion of oxygen (O) through the high-k oxide to oxidize the Si underneath.

- The RTA additionally seems to change the structure of the high-κ oxide. This cannot be proven by HR-TEM images, but results obtained by electrical characterization suggest this (This topic will be addressed in detail in the chapter IV.2).

- HfO_2 thin films have not been physico-chemically characterized as thoroughly as ZrO_2 films. This has two main reasons: First, Balog et al. in [115] showed that the grown HfO_2 and ZrO_2 show the expected similarity, while using the same precursor substances, and second, also our own results - including physico-chemical and electrical characterization (see chapter IV.2) - of these two materials are similar and comparable.

In the following chapter, we will discuss in detail all different material combinations that have been processed and investigated in design of MOS capacitors during this thesis, regarding to their electrical properties. Hereby, we will try to explain the obtained characteristics with reference to their physical and chemical characteristics.

IV.2 Evaluation of the MOS-capacitors

The following chapters discuss all investigated high-κ/metal-gate stacks regarding their most significant results. Devices containing TiN_x (Ti-rich)-gates are not shown, since they did not provide satisfying outcomes. The presented data contains mainly ZrO_2 as gate dielectric, since we have not been able to investigate the HfO_2-incorporating stacks as comprehensive as the ZrO_2-incorporating ones. Nevertheless, the investigated gate stacks incorporating either HfO_2 or ZrO_2 as gate dielectric are in general similar and comparable to each other.

IV.2.1 Gate Material: Aluminium (Al)

Aluminum is chosen, because it is the standard gate electrode for the evaluation of SiO_2 gate dielectrics. MOSCAPs incorporating a 17 nm thick (physical thickness) ZrO_2 dielectric and an about 300 nm thick evaporated Al-electrode have been investigated.

Figure IV.5(a) shows capacitance-voltage (C-V) measurements at various frequencies. It should immediately attract attention that the measured capacitance shows a strongly frequency-dependent behavior, especially in the accumulation regime: The C–V- and conductance-voltage (G–V) characteristics, may be severely degraded by the presence of a high density of interface traps or the presence of a non-stoichiometric oxide layer at the oxide/semiconductor interface, and in turn lead to improper parameter extraction [116]. An undesired thin lossy dielectric layer for example, might form between oxide and semiconductor during processing. It makes the measured capacitance strongly frequency-dependent, especially in accumulation [117]. Due to this strong frequency dispersion, proper characterization and parameter extraction from the measured capacitance and conductance are not possible. Therefore, we applied the reconstruction technique/model suggested by Kwa et al. [116] to extract the intrinsic gate capacitance and conductance from the measured non-ideal C–V- and G–V data. The results for the corrected C-V measurements of an Al/ZrO_2/p-Si MOSCAP are shown in figure IV.5(c). The applied model, containing equivalent circuit and formulas, can be found in [116]. In the following chapters that address the other investigated materials systems, for sake of convenience we will only show the corrected curves.

After the above mentioned correction, the C-V characteristic depicted in figure IV.5(c) still exhibits a frequency dependent hump around $V_G \sim 0$ V. This indicates the presence of acceptor interface traps located in the Si-bandgap [118]. The position of this hump on the voltage-axis can be energetically attributed to the position of the traps in the Si-band gap; the amount of this hump in turn to the trap density, whereas this amount strongly depends on the measurement frequency. Due to this frequency dispersion, these interface traps can be addressed as so-called “slow-traps”, since the amount of the hump shrinks with increasing measurement frequency, because these *slow traps* are not able to follow the high-frequency signal. Such traps are charged by states in the gap that are raised by imperfect interfaces. Additionally, these defects will affect reliability [119][i].

The flatband voltage V_{FB} of the device has been determined to -0.24[ii] V after a method proposed by Riccó et al. [102], a value that nicely agrees with the value (~ -0.3 V) found by Houssa [118]. Using the

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[i] J. Robertson in [119] reviews *interfaces and defects of high-k oxides on silicon*. He explains in detail the bonding principles of the Si:ZrO_2 system, which is also representative of HfO_2 and their silicates.

[ii] Concerns given in [121] can be neglected, since this is the only value that lies within the relevant voltage range. Nevertheless, we must not neglect mentioned concerns.

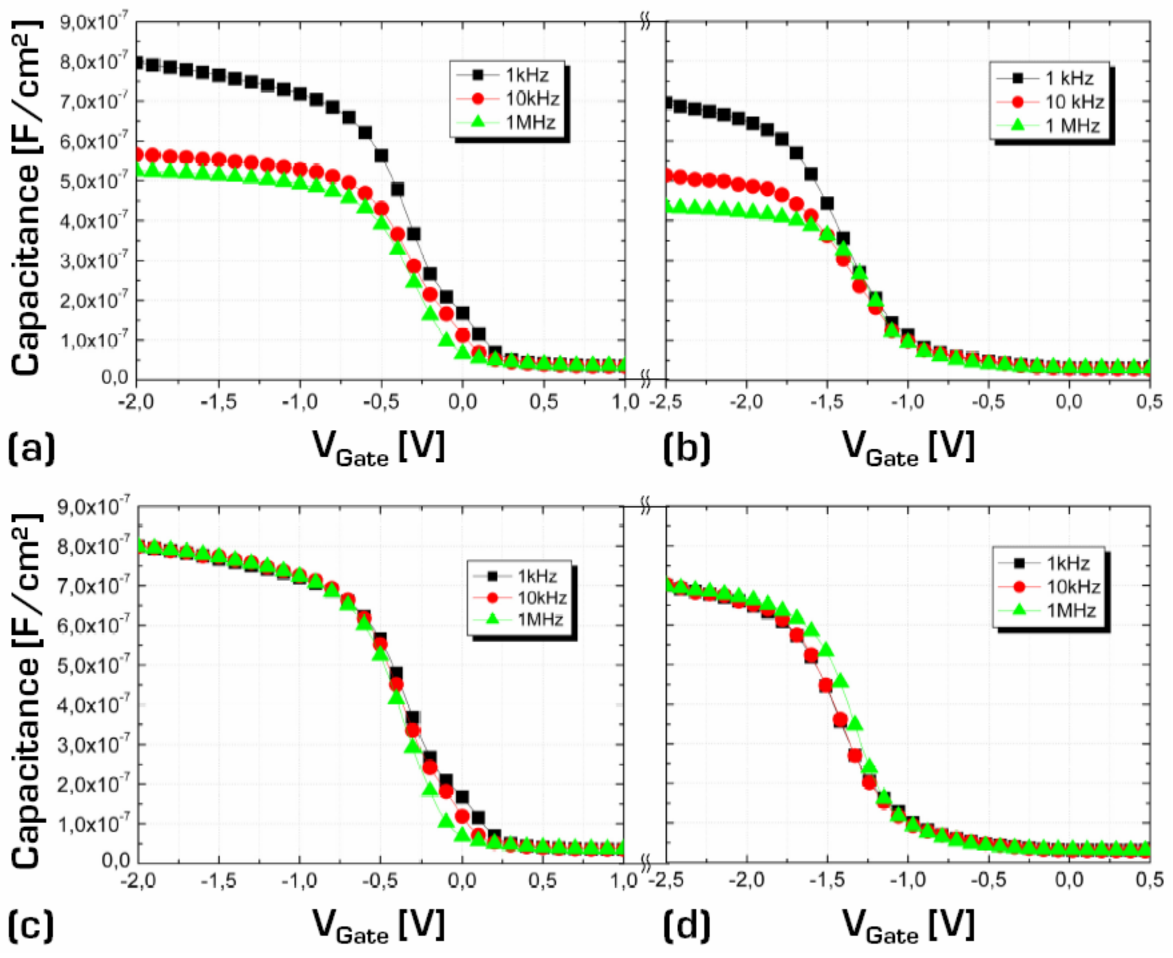

Figure IV.5: C-V measurements of Al/ZrO$_2$/p-Si capacitors at various ac-frequencies: (a) Uncorrected and (c) corrected results before PMA in FGA, and (b) Uncorrected and (d) corrected results after PMA, are shown.

workfunction of Al, determined to 4.1 eV for Al/SiO$_2$/Si capacitors by Deal et al. [120], equation II.46 leads a theoretical value of V_{FB} = -1.01 V. Since we know that the workfunction of the gate material – and hence the resulting V_{FB} – is dependent on the underlying dielectric, processing conditions, and applied thermal budget, we have to compare experimentally obtained values and these found in literature with care. Kar in [96,121] critically evaluated various capacitance techniques, such as [102], and proposed a technique that fully takes into account the interface trap capacitance and the interface trap charge. From this technique we obtained the oxide capacitance per area $C_{OX} = 0.76\cdot10^{-6}$ F/cm², which results in an overall relative permittivity of the dielectric stack ε_r = 14.6 and a corresponding EOT of 4.5 nm (More details can on the applied methodology be found in [121]). This value might – on a first glance – appear a bit low, since literature (for an overview, see [35,118]) reports values up to 25 for stoichiometric ZrO_2. But if we reconsider figure IV.4 and additionally anticipate on the HR-TEM results that will be shown in the following chapters, we assume that we have to deal with a dielectric stack composed of about 1.5 nm – 2 nm of SiO_x[i] and 15 nm – 15.5 nm of ZrO_2. By assuming a relative dielectric constant for SiO_2 of ε_r = 3.9 [8], we obtain after equation II.33 a relative dielectric constant of ε_r = 20 - 24 for ZrO_2, which corresponds with the higher values given in literature [118].

After PMA for 30 minutes at 400 °C in FGA, C-V characteristics act as shown in figure IV.5(b) and figure IV.5(d) (corrected). The frequency dependent hump around $V_G \sim 0$ V disappears (see figure IV.5(d)). Thereby, we can conclude that the PMA process has been effective in annealing out interface traps located in the Si-bandgap.

Additionally, V_{FB} is clearly shifted to a more negative value, more specific -1.48 V. This value departs from the value we obtained before the PMA. By evaluating hysteresis measurements, which are made by a forward ($-V_G \rightarrow +V_G$)–, and a subsequent back ($+V_G \rightarrow -V_G$)–sweep of the gate voltage, we observe a shift to more negative voltages for the back-sweep. Concerning the Al-gate, we assume an interfacial formation of Al_2O_3 at the gate/dielectric interface, since Al_2O_3 has a higher negative free energy of formation than any metal oxide and would hence reduce most dielectrics underneath it at elevated temperatures [122]. Since Al_2O_3 is believed to be the only high-κ oxide that has negative fixed charge [104], negative charge that have been apparent within the oxide, might have been annealed during the PMA, causing a V_{FB} shift to more negative values, if we assume the V_{FB} of the 'ideal', charge-free curve to be around -1.01 V to -1.48 V.

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[i] This is most likely SiO_2. Therefore, from now on we will use the expression "SiO_2".

Another noticeable difference between the curves in figure IV.5(b) and figure IV.5(d) is the reduction of C_{OX}, which reduces to $0.70 \cdot 10^{-6}$ F/cm². This results in an overall relative permittivity $\varepsilon_r = 13.4$ and a corresponding EOT of 4.9 nm. The present reduction is most likely caused by interfacial layer reactions during the PMA. Since we observe similar behavior when using Ni, or Mo as the gate material (see the following chapters), we assume the interfacial SiO_2-layer to grow during the temperature treatment.

Nevertheless, all assumptions made above can only be proved consistent by performing HR-TEM cross-sections and corresponding EDX-scans of the gate stacks at all stages of applied thermal budget, which unfortunately has not been possible.

Figures IV.6(a) and IV.6(b) show gate current measurements for this device. Figure IV.6(a) compares I-V measurements dependent on the measurement direction. The difference of the leakage current in accumulation ($-V_G$ applied) compared to that in depletion/inversion ($+V_G$ applied) is believed to be due to the difference in barrier heights at the Al/ZrO_2 and ZrO_2/p-Si interfaces. In the case of the forward ($-V_G \rightarrow +V_G$)-sweep of the gate voltage, the leakage current is much higher (more than 3 orders of magnitude at the future device-relevant $V_G = -1$ V) as in the case, if the voltage is swept from $+V_G \rightarrow -V_G$. The difference in the two characteristics and the "uncommon" shape of the back-sweep are believed to arise from the response of oxide trapped charges, as well as from the previously mentioned difference in barrier heights.

The physical thickness of the oxide excludes the conduction processes within the insulator to be caused by tunneling phenomena (see also chapter II.2.1). Rather shows the semi-logarithmic plot of $|I_G/V_G|$ over $|V_G|^{1/2}$ in figure IV.7(a) that two distinct regions are apparent. The linear relation at higher V_G suggests the Frenkel-Poole emission to be the dominant conduction mechanism.

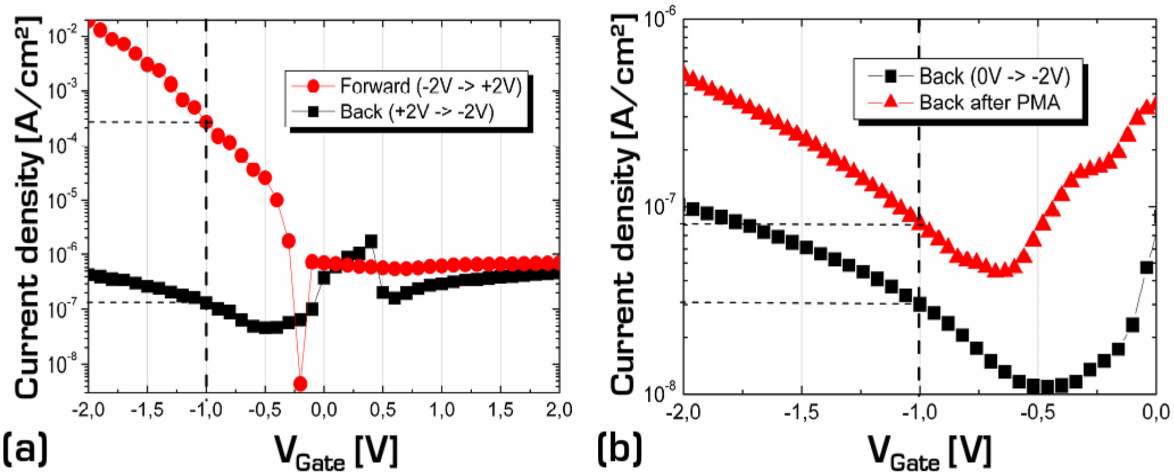

Figure IV.6: I-V measurements of Al/ZrO_2/p-Si capacitors: (a) Forward-, and back measurements, and (b) comparison of back measurements before and after PMA. The technological relevant values at V_G = -1 V are indicated.

The Frenkel-Poole model that explains the tunneling of carriers over traps within the insulator is illustrated in figure IV.7(b). The expected interface layer (SiO_2) might on one hand suppress leakage currents by its elevated energy band gap (up to 8.9 eV), but on the other hand increase the Frenkel-Poole emission by introducing additional traps at the interface within the insulator.

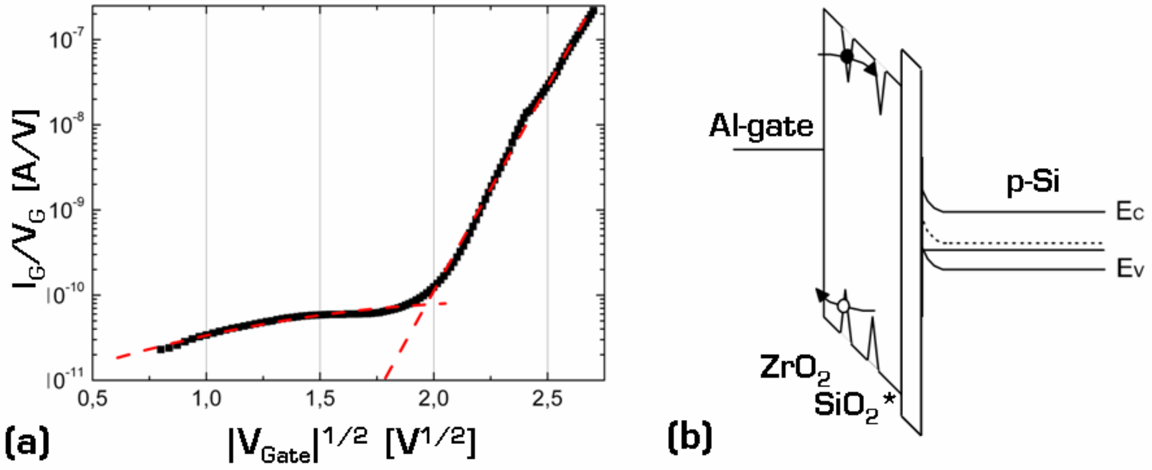

Figure IV.7: (a) Semi-logarithmic plot of $|I_G/V_G|$ over $|V_G|^{1/2}$ to examine conduction mechanisms during I-V measurements. (b) Frenkel-Poole model suggesting the tunneling of carriers over traps within the insulator.

Raised leakage current after PMA (see figure IV.6(b)) is observed compared to the device performance before annealing. Reasons therefore are already given above: Interfacial layer reactions during the PMA as well as the interfacial formation of Al_2O_3 between at the gate/dielectric interface are most likely to be the causes.

Table IV.A summarizes the obtained key data for the investigated Al/ZrO_2/p-Si MOSCAPs:

Table IV.A: Summary of key data of Al/ZrO_2/p-Si capacitors.

Thermal treatment:	**PDA***	**PMA**
Oxide capacitance per area [$\cdot 10^{-6}$ F/cm²]	0.76	0.70
Rel. permittivity of dielectric stack ε_r [-]	14.6	13.4
Equivalent oxide thickness (EOT) [nm]	4.5	4.9
Flatband voltage V_{FB} [V]	-0.24	-1.48

* PDA performed before metallization

IV.2.2 Gate Material: Nickel (Ni)

Nickel turned out to be an interesting material to be applied as Nickel-Silicide (NiSi) in "FUSI (full silicidation) gate technology", where the work function is modulated by obtaining different silicide phases [62]. MOSCAPs incorporating a 10 nm thick (physical thickness) ZrO_2 dielectric and an about 100 nm thick sputter-deposited Ni electrode have been investigated.

Figure IV.8(a) shows the corrected C-V characteristics at different measurement frequencies before PMA. One can see that the C-V curve is (i) stretched in depletion and (ii) shows a clear frequency-dependent hump; (iii) in (strong) inversion the capacitance rises again (up to C_{OX} for f = 1 kHz) even at measurement frequencies up to 10 kHz. Observations (i) and (ii) are classically attributed to a high interface charge density [118] or (additionally) a non-uniform oxide charge distribution [93], and that the signal due to interface traps is frequency-dependent. The flatband voltage V_{FB} of the device has been determined to -0.58 V. The oxide capacitance per area C_{OX} = $1.10 \cdot 10^{-6}$ F/cm², which results in an overall relative permittivity ε_r = 12.4 and a corresponding EOT of 3.2 nm.

We applied a PMA in FGA at 400 °C for 30 minutes. The resulting C-V characteristics are depicted in figure IV.8(b). Interface trap density (note the reduced humps) is clearly lowered, and additionally, the flatband voltage V_{FB} (-0.01 V) is shifted to more positive values, which can be attributed to the annealing of fixed positive charges in the oxide. The overall reduction of C_{OX} ($0.72 \cdot 10^{-6}$ F/cm²) indicates thermodynamical and/or chemical reactions within the gate stack. This results in an overall relative permittivity ε_r = 8.1 and a corresponding EOT of 4.8 nm.

So far, we have not discussed the rise of the overall capacitance C at high measurement frequencies within the inversion regime (iii), which can be observed in both figures (IV.8(a) and IV.8(b)). In an "ideal" C-V curve the

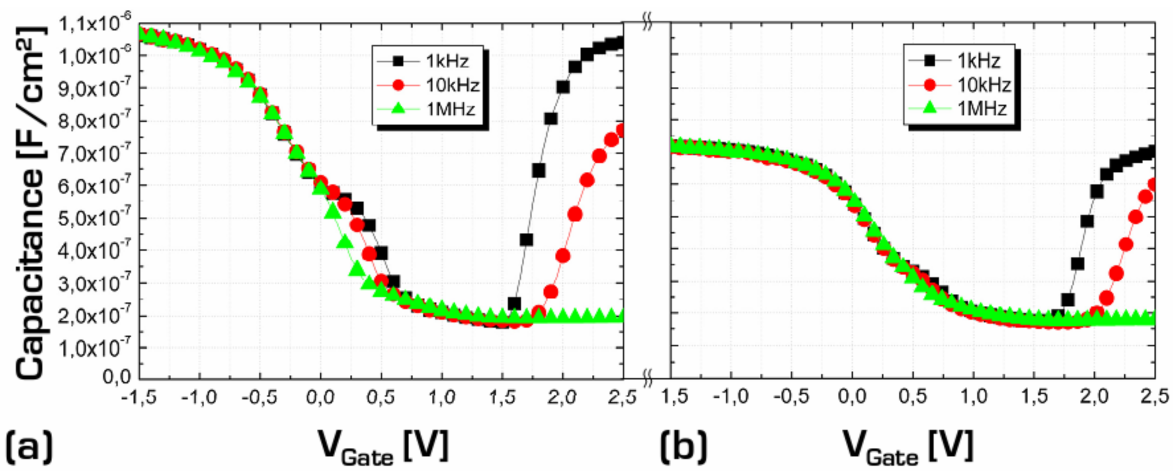

Figure IV.8: C-V measurements of Ni/ZrO_2/p-Si capacitors at various ac-frequencies: (a) Corrected results before PMA in FGA, and (b) after PMA are shown.

inversion charge, which is borne by the minority carriers, is not able to follow the HF-signal and therefore, the overall capacitance saturates at a minimum value. We cannot observe this behaviour in our measurements, so we assume - while referring to [123] - that the silicon surface beyond the gate is inverted by charge within the ZrO_2 layer. This inversion layer beyond the gate area affects the minority carrier response time and the C-V characteristics in inversion for an MOSCAP made on p-type silicon [10,123,124]. The model for the flow of the ac-current as proposed by [124] is shown in figure IV.9(a), implying that the applied frequency is high enough to neglect the differential capacitance by minority carriers, and that the dc-bias between gate electrode and silicon is zero. The current flows through the oxide, spreads laterally into the channel, and leaves the stack through the back contact. Therefore, the current flows over an area which may be many times the area of the gate electrode. The channel beyond the gate can be modelled by a distributed resistance-capacitance network (figure IV.9(b)) and further represented by a lumped capacitance C_C in series with a lumped conductance as shown by the equivalent circuit in figure IV.9(c). The conductance is divided into the conductance of the channel under the gate electrode g_G, which changes with bias, and the equivalent conductance of the channel beyond the gate electrode g_C, which stays constant (provided that the potential along the oxide surface does not change). When the conductance of the channel under the gate electrode g_G is zero, the channel under the gate electrode is pinched of and the overall capacitance measured is the oxide capacitance C_{OX} in series with the depletion layer capacitance C_D (see figure IV.8(b), gate voltage around 1.5 V). As the MOCAP is driven from depletion to strong inversion, g_G increases, allowing ac-current to flow into the distributed channel network and thereby causing the overall capacitance to increase and approach C_{OX} (see figure IV.8(b), f = 1 kHz). The distributed channel resistance-capacitance network behaves like a low pass filter and as

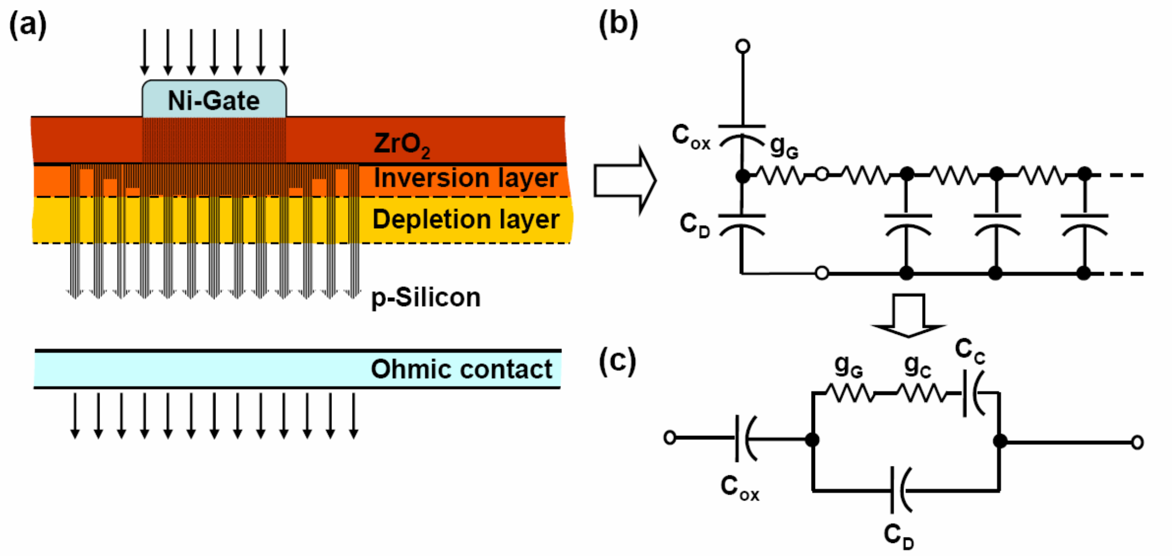

Figure IV.9: (a) Schematic of the ac-current flow through the Ni/ZrO_2/p-Si gate stack at zero dc-bias. The equivalent circuit in (b) shows the distributed channel resistance-capacitance network beyond the gate. The distributed channel network can be replaced as shown in (c). All figures are adapted from [124].

the frequency increases, the ac-current spreads within a shorter distance, and the measured capacitance saturates at values less than C_{OX} (see figure IV.8(b), f = 10 khz and 1 MHz).

Whereas the authors in [124] investigated Al/SiO_2/p-Si capacitors, and attributed the charges to be typically sodium ions or oxide fixed charge of thermal oxidation, in our devices we believe nickel ions to be present within the oxide. On one hand, we did not observe this behaviour on similar MOSCAPs incorporating different metal gate materials (see corresponding chapters). On the other hand, it is well known that oxygen ions or metals possessing a low oxidation state (valency) are usually considered to be the most mobile charge and mass carriers [125], and it has been shown that Ni is a highly soluble and fast-diffusing metal impurity in crystalline [126] and amorphous [127] silicon. By taking these facts into account, we assume diffusion of Ni-atoms into the ZrO_2 during the sputter deposition process. This stack morphology might further change during PMA due to ongoing interdiffusion or changing interface characteristics.

To get a deeper view into the stack morphology, we performed high-resolution transmission electron microscopy (HR-TEM). An example is depicted in figure IV.10, showing an about 1.5 nm - 2 nm thick amorphous SiO_2 in contact with an about 8 nm thick polycrystalline ZrO_2 (Note the oxide thickness directly after PDA determined to 10 nm by ellipsometry). This interfacial SiO_2 might already form during the MOCVD process or by reducing the ZrO_2 during PDA and/or PMA. The interface between the dielectric and the gate material is not well defined and appears somehow 'blurry'.

Figure IV.11(a) shows a scanning-TEM picture providing a larger overview of the MOSCAP. The marked area has been magnified into figure IV.11(b): As can be seen, a Ni-crystallite has been preferentially sputtered away by ion milling during the TEM preparation, resulting in a "black hole".

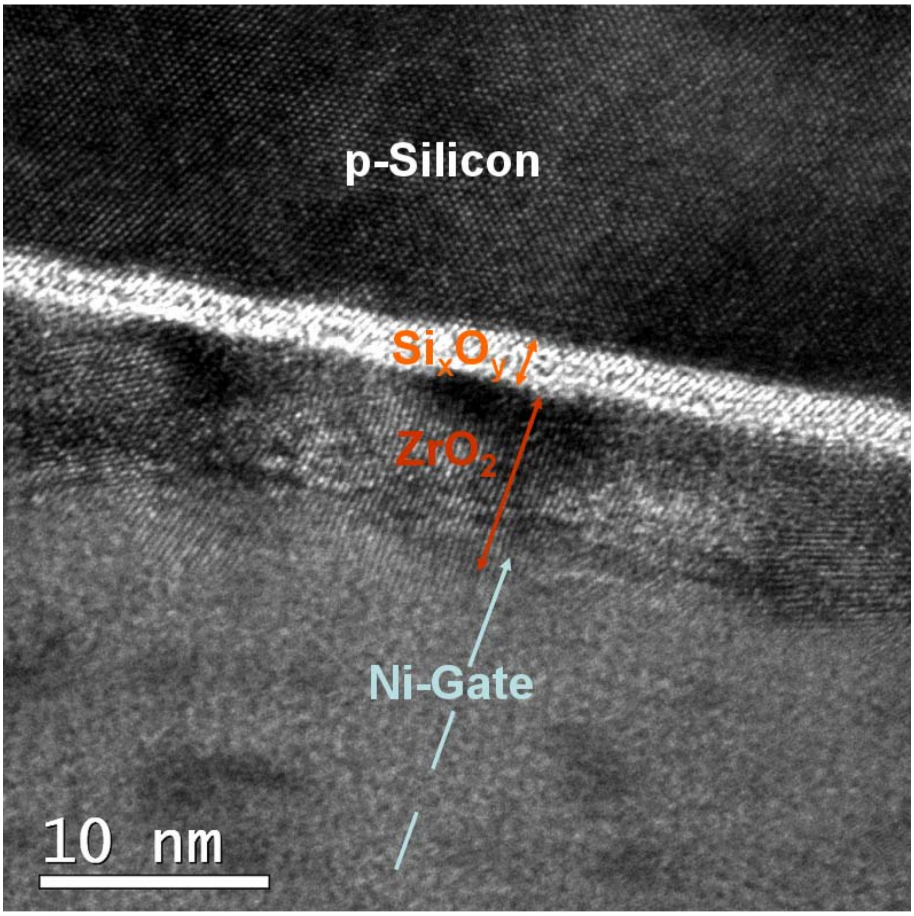

Figure IV.10: HR-TEM image of a Ni/ZrO_2/p-Si gate stack after PMA in FGA at 400°C.

Energy dispersive X-ray analysis (EDX) along the line from *0 - 1* is shown in figure IV.11(c). Even though, we cannot totally neglect any residual Ni at the gate electrode/oxide interface, the well defined peak of the Ni-signal supports our assumption of Ni-interdiffusion between the gate electrode and the gate dielectric, resulting in Ni ions that become manifested as charges within the high-κ oxide. This leads to an inversion of the silicon surface beyond the gate, if the device is driven into inversion.

Figure IV.12(a), showing hysteresis measurements at 1 MHz measurement frequency, indicates that after the PMA the number of oxide trapped charge is very low. We assume this HF-measurement not to be influenced by the above discussed Ni-contamination.

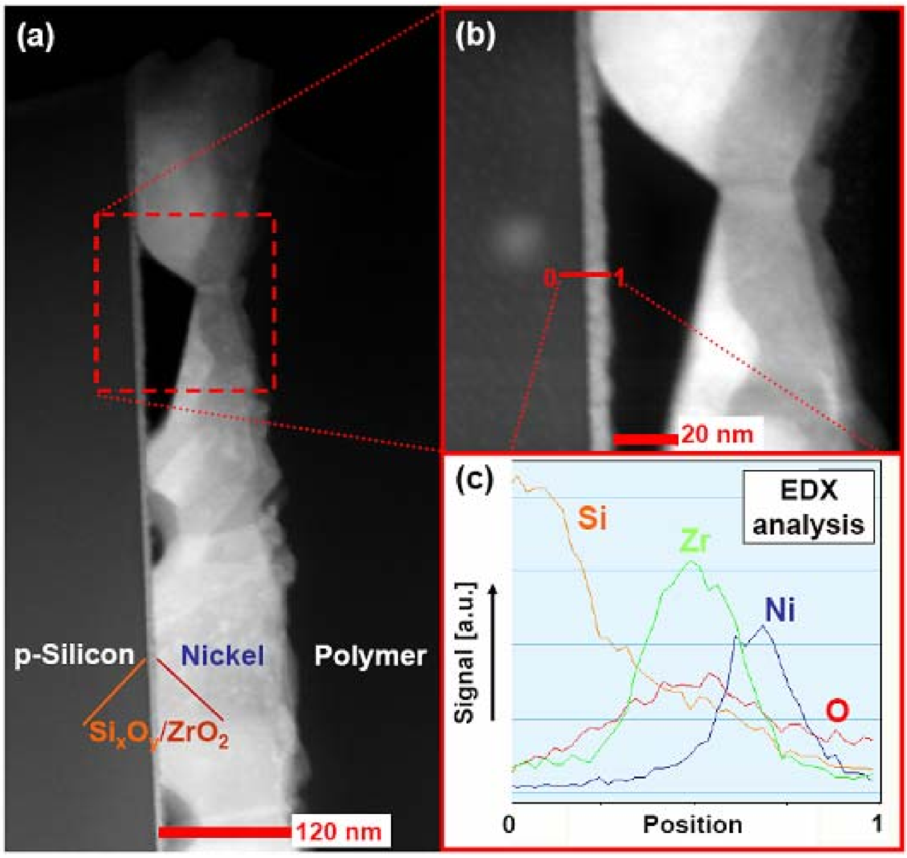

Figure IV.11: (a) Scanning-TEM (STEM) picture of Ni/ZrO$_2$/p-Si gate stack after PMA in FGA. The red-marked area is magnified in (b). Energy Dispersive X-ray (EDX) analysis along line 0 - 1 is shown in (c).

The leakage current measurements show similar characteristics as shown in the previous chapter for the Al-gate stack. In detail (see figure IV.12(b)) we observe a small decrease during PMA. This is most likely to the previously discussed thermodynamical and/or chemical reactions within the gate stack during the annealing.

Table IV.B summarizes the obtained key data for the investigated Ni/ZrO$_2$/p-Si MOS capacitors.

Table IV.B: Summary of key data of Ni/ZrO$_2$/p-Si capacitors.

Thermal treatment:	**PDA***	**PMA**
Oxide capacitance per area [$\cdot 10^{-6}$ F/cm²]	1.10	0.72
Rel. permittivity of dielectric stack ε_r [-]	12.4	8.1
Equivalent oxide thickness (EOT) [nm]	3.2	4.8
Flatband voltage V_{FB} [V]	-0.58	-0.01

* PDA performed before metallization

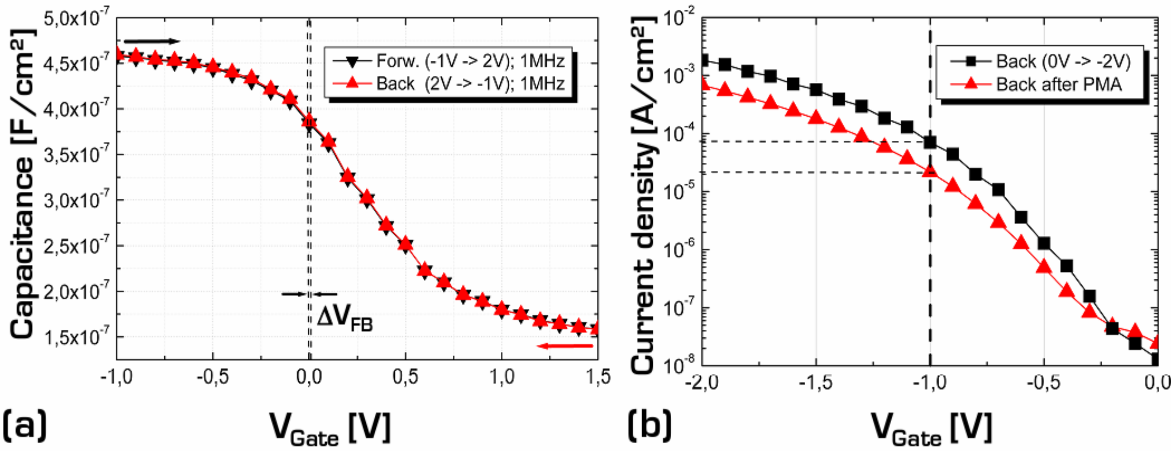

Figure IV.12: (a) C-V hysteresis measurements of Ni/ZrO$_2$/p-Si capacitor at f = 1 MHz. The shift Δ of the V$_{FB}$ is indicated. (b) I-V measurements before and after PMA. The technological relevant values at V$_G$ = -1 V are indicated.

IV.2.3 Gate Material: Titanium-Nitride (TiN)

TiN is a very promising candidate to be applied as mid-gap metal gate material in future CMOS technology. To address this issue, we investigated a number of different MOSCAPs incorporating both, ZrO_2 and HfO_2 as the gate dielectric. Results for ZrO_2 and HfO_2 are similar and comparable, but the ZrO_2-insorporating gate stacks show slightly superior behaviour. We believe this to be most likely due to our advantageous larger experience at the MOCVD process of the ZrO_2 compared to that one of the HfO_2. Hence, in the following we will summarize the results of the TiN stacks by means of MOSCAPs with 6 nm thick ZrO_2 gate dielectric and ~ 110 nm thick TiN metal-gates.

Figure IV.13(a) shows the obtained C-V measurements for various measurement frequencies after TiN-deposition. The results for lower frequencies show a frequency-dependent hump corresponding to interface traps, located at a discrete energy level. The flatband voltage V_{FB} of the device has been determined to -0.85 V. The oxide capacitance per area $C_{OX} = 1.30 \cdot 10^{-6}$ F/cm^2, which results in an overall relative dielectric permittivity of $\varepsilon_r = 8.8$ and a corresponding EOT of 2.7 nm.

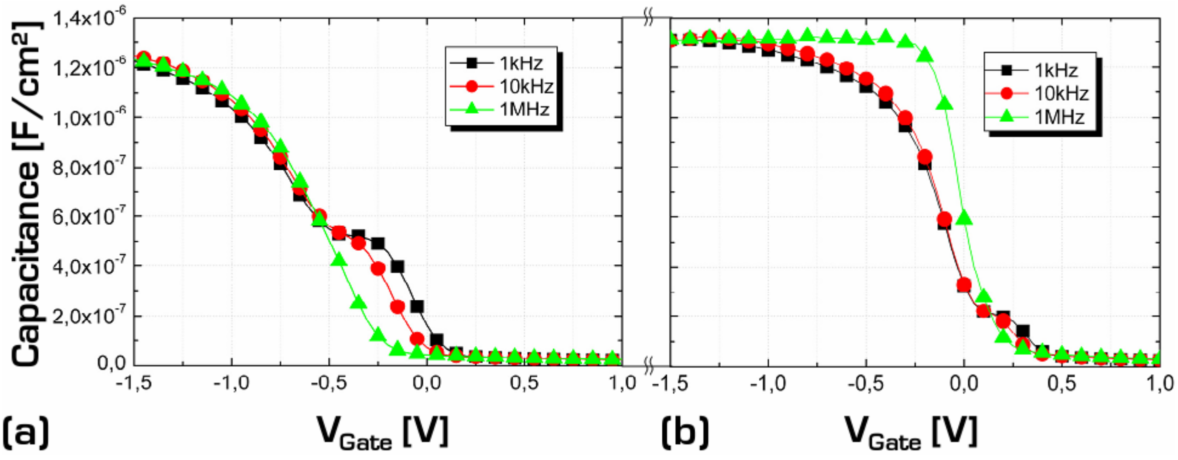

Figure IV.13: C-V measurements of $TiN/ZrO_2/p\text{-}Si$ capacitors at various ac-frequencies: (a) Corrected results before PMA in FGA, and (b) after PMA are shown.

To investigate thermal stability, PMA at 400 °C for 30 minutes in FGA has been applied. The resulting C-V characteristics are shown in figure IV.13(b). We can see that C_{OX} ($1.31\cdot10^{-6}$ F/cm^2) for these measurements stays almost constant; out of this we obtain an overall relative dielectric permittivity of $\varepsilon_r = 8.9$ and corresponding EOT = 2.6 nm. Similar experiments using temperatures up to 450 °C also delivered constant C_{OX}. This shows that TiN exhibits thermal stability at 450°C.

Interface trap density (note the reduced humps) is clearly lowered, and additionally the flatband voltage V_{FB} (-0.05 V) is shifted to more positive values, which can be attributed to the annealing of fixed positive charges in the oxide. The HF-measurement (f = 1 MHz) of this stack shows excellent C-V characteristics. The hysteresis measurements at this frequency, depicted in figure IV.14(a) confirms this behaviour and denotes a relatively low density of oxide trapped charge.

A HR-TEM measurement of the cross section of a TiN/ZrO_2/p-Si gate stack after PMA at 450 °C for 30 minutes in FGA (Note that in this case the overall oxide thickness is about 5 nm) is depicted in figure IV.15. Similar to the results for the Ni-gates, an ~ 1.5 nm - 2 nm thick amorphous SiO_2 at the Si-interface can be observed. As already mentioned

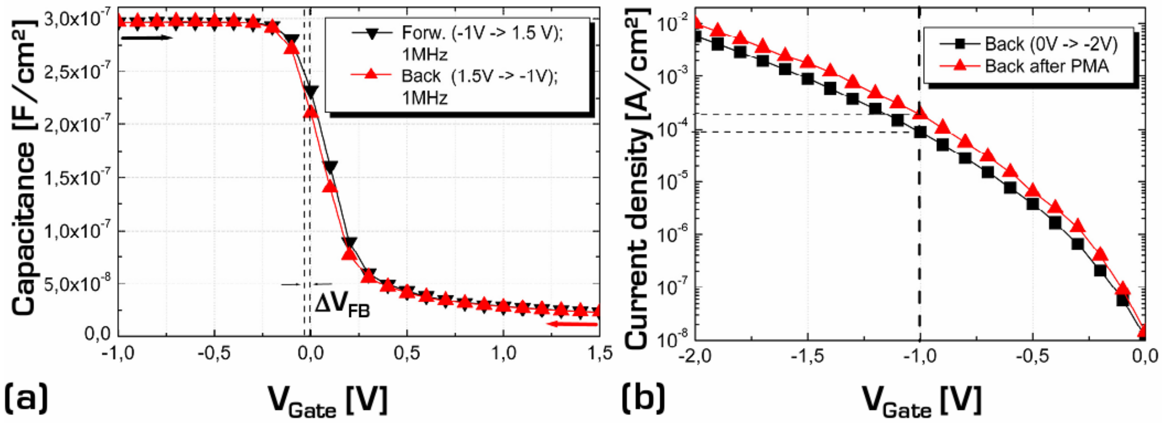

Figure IV.14: (a) C-V hysteresis measurements of TiN/ZrO_2/p-Si capacitor at f = 1 MHz. The shift Δ of the V_{FB} is indicated. (b) I-V measurements before and after PMA. The technological relevant values at V_G = -1 V are indicated.

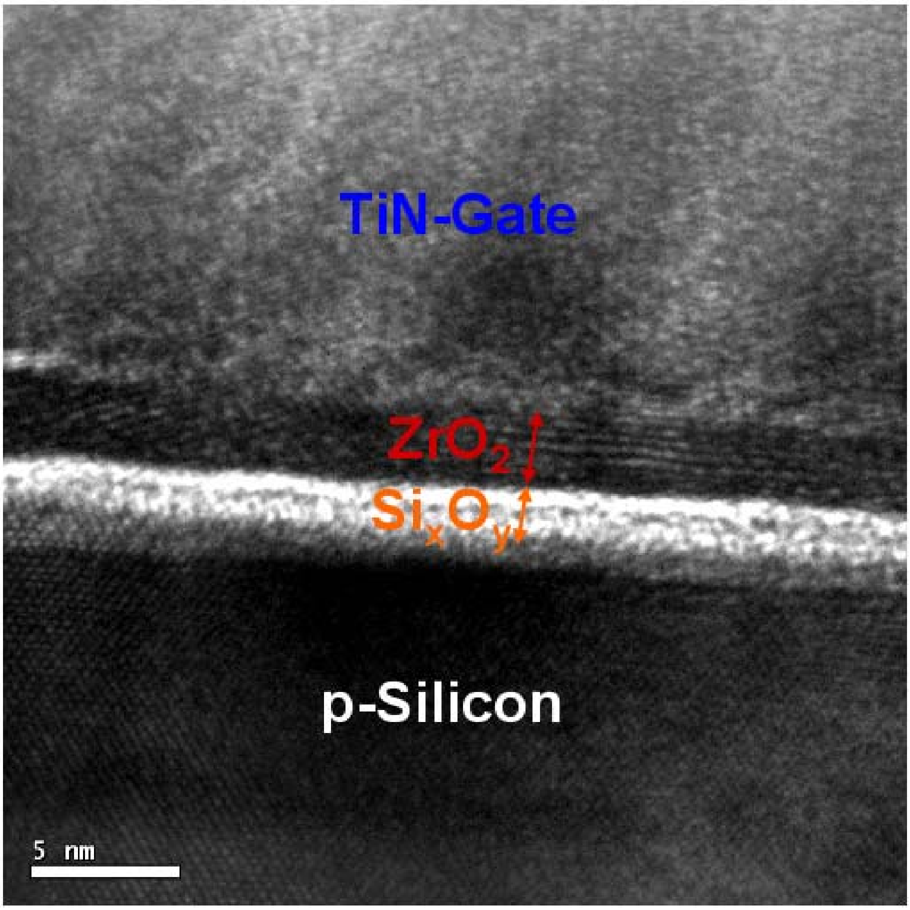

Figure IV.15: HR-TEM image of a TiN/ZrO_2/p-Si gate stack after PMA in FGA at 450°C.

in the previous chapter, this interfacial oxide might already form during the MOCVD process or by reducing the ZrO_2 during PDA and/or PMA. At this result we can exceptionally well observe the influence of the SiO_2, since the two different oxides exhibit almost the same thickness and therefore the overall achievable EOT is strongly reduced.

Again, only the relevant I-V characteristics for the accumulation regime are depicted (see figure IV.14(b)), since the conduction characteristics are similar to that explained in detail in chapter IV.2.1. In detail, the I-V measurements show more or less equal (Differences due to local phenomena may always appear) leakage currents for the samples before and after PMA. This result supports the conclusion of the thermal stability of the present gate stack.

Table IV.C summarizes the obtained key data for the investigated TiN/ZrO_2/p-Si MOSCAPs.

Table IV.C: Summary of key data of TiN/ZrO_2/p-Si capacitors.

Thermal treatment:	**PDA***	**PMA**
Oxide capacitance per area [$\cdot 10^{-6}$ F/cm²]	1.30	1.31
Rel. permittivity of dielectric stack ε_r [-]	8.8	8.9
Equivalent oxide thickness (EOT) [nm]	2.7	2.6
Flatband voltage V_{FB} [V]	-0.85	-0.05

* PDA performed before metallization

IV.2.4 Gate Material: Molybdenum (Mo)

Molybdenum (Mo), whose work function can be tailored by doping with nitrogen (N), is a suitable candidate for "single-metal tunable dual work function technology". Different MOSCAPs incorporating both, ZrO_2 and HfO_2 as the gate dielectric, have been investigated. Results for ZrO_2 and HfO_2 are similar and comparable. In the following paragraphs, we show results for MOSCAPs with 18 nm thick ZrO_2 and 14 nm thick HfO_2 as gate dielectric, respectively, and about 100 nm thick Mo metal-gates.

Zirconium dioxide:

Figure IV.16(a) shows C-V measurements for the ZrO_2-capacitors after Mo-deposition. These results have been measured at our cooperative partner at Uppsala University and therefore, we have not been able to access the full data set. Still, it can be assumed that the flatband voltage V_{FB} lies somehow within the range of 0.6 V - 0.8 V. It is not possible to determine the oxide capacitance per area C_{OX} - and consequently corresponding ε_r and EOT - since the present data has not been corrected due to parasitic series resistance, and does not include LF-measurements.

To investigate thermal stability in more detail, we applied a PMA at 400 °C in FGA for 30 minutes, and additionally an RTA at 950 °C for 10 seconds. The resulting C-V characteristics are shown in figure IV.16(b). The oxide capacitance of the devices results in $C_{OX} = 0.95 \cdot 10^{-6}$ F/cm². Hence, the overall relative dielectric permittivity $\varepsilon_r = 19.3$ and the corresponding EOT = 3.6 nm. Since we do not have equally performed electrical measurements before and after the single temperature steps, it is difficult to make any statements on their influence on oxide trap, and interface trap density. From our results of the other gate materials, we may assume annealing of interface-, and oxide trapped charge. Though, even after PMA and RTA treatment, we still observe a frequency dependent hump corresponding to interface traps that is energetically located at or near the Si-surface. The flatband voltage V_{FB} (-0.16 V) is clearly shifted to a more negative value during the RTA. This may be attributed to the annealing of fixed negative charges in the oxide, or due to physico-chemical changes within the oxide. The latter assumption is supported by I-V measurements that are depicted

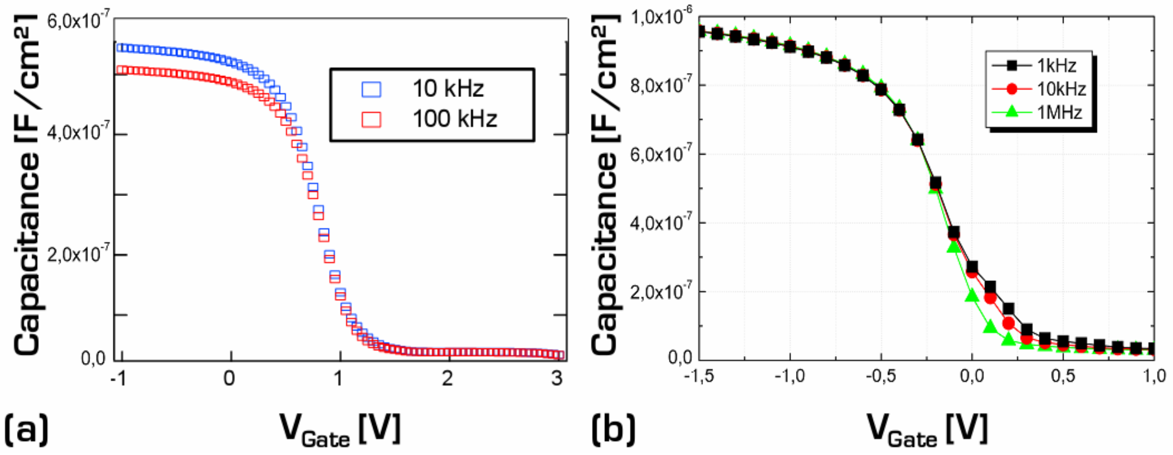

Figure IV.16: C-V measurements of Mo/ZrO$_2$/p-Si capacitors at various ac-frequencies: (a) Results before PMA, and RTA, and (b) after PMA, and RTA are shown.

in figure IV.17(b), and exhibit clearly increased values compared to the results obtained before annealing. Oxide trapped charge is most likely annealed, which can be seen by the results of the hysteresis measurement shown in figure IV.17(a).

A HR-TEM measurement of the cross section of a Mo/ZrO_2/p-Si gate stack after PMA and RTA is depicted in figure IV.18. The overall dielectric stack is about 20 nm thick, and an about 2 nm thick amorphous SiO_2 at the Si-interface is clearly visible. Optically, the ZrO_2 does not exhibit distinctive changes compared to that one after PMA (compare figure IV.10 and figure IV.15). Still, there might be some changes in the crystallinity of the ZrO_2, and also the metal/oxide interface looks somehow "problematic", but more accurate statements cannot be made in the basis of the present experimental results.

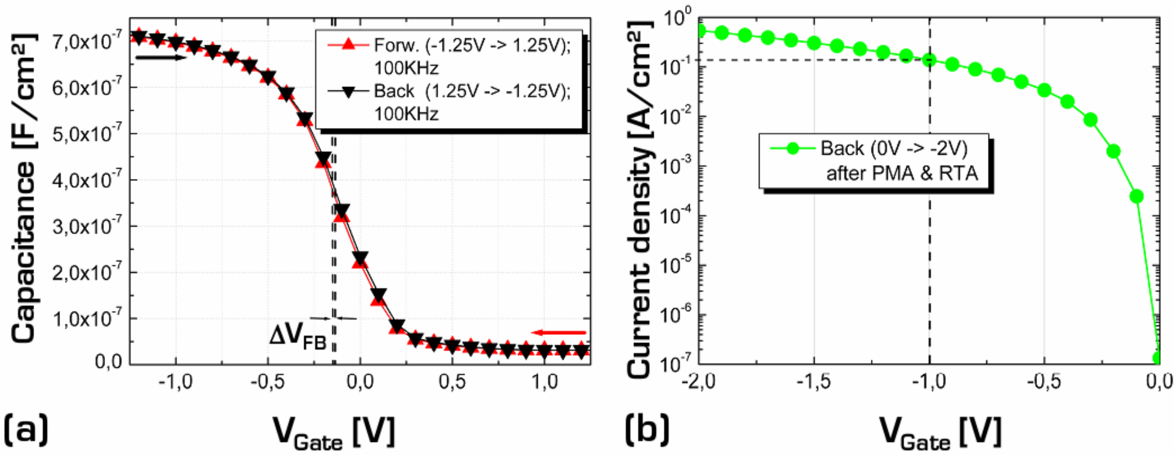

Figure IV.17: (a) C-V hysteresis measurements of Mo/ZrO_2/p-Si capacitor at f = 1 MHz. The shift Δ of the V_{FB} is indicated. (b) I-V measurements after PMA, and RTA. The technological relevant value at V_G = -1 V is indicated.

Hafnium dioxide:

Figures IV.19 show C-V measurements for the HfO_2-capacitors (a) after Mo-deposition, and (b) after PMA in FGA, and an additional RTA in Ar-atmosphere. The C-V curves in both figures appear a bit more stretched,

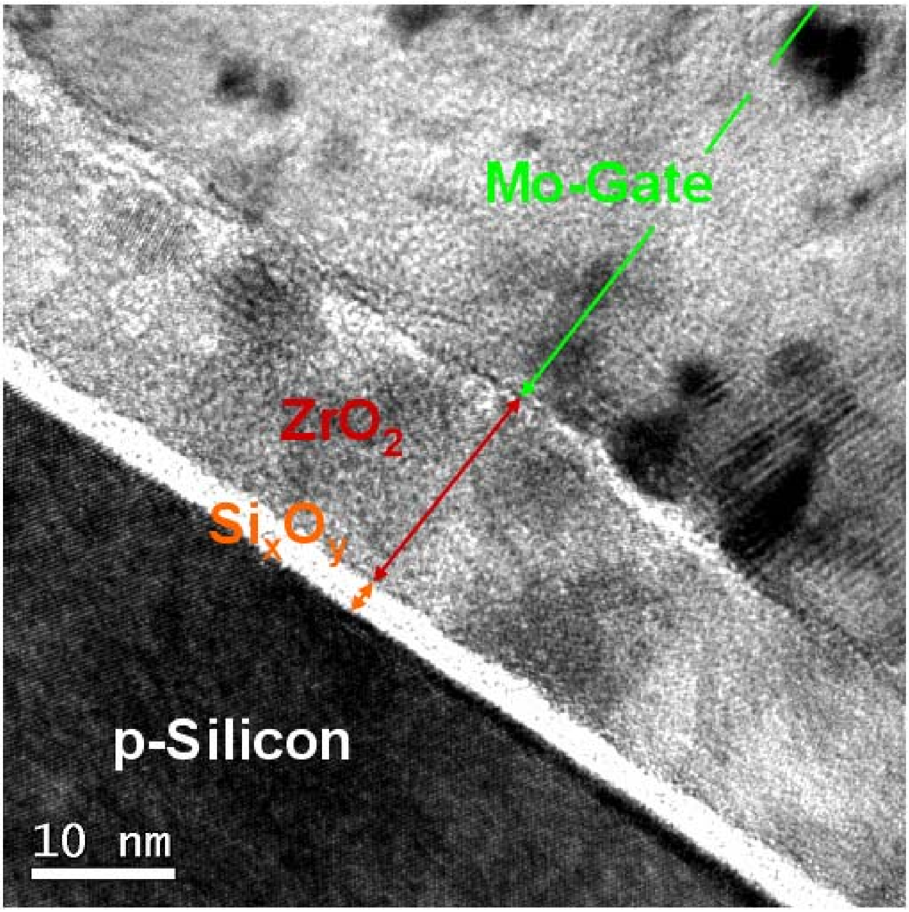

Figure IV.18: HR-TEM image of a Mo/ZrO_2/p-Si gate stack after PMA, and RTA.

indicating an increased amount of oxide traps. The flatband voltage V_{FB} prior to the RTA lies somehow within the range of 0.8 V - 1.1 V, and is clearly shifted to a more negative value (-0.23 V) during the RTA (figure IV19(b). Again, it is not possible to determine the oxide capacitance per area C_{OX} – and consequently corresponding ε_r and EOT - since the present data has not been corrected due to parasitic series resistance and does not include LF-measurements.

Compared to the ZrO_2-stacks, the present ones exhibit slightly increased humps due to interface traps after RTA at 950 °C for 10 seconds (figure IV.19(b)). But this can not be attributed only to the oxide, since the oxides differ in thickness and the present HfO_2 might in general incorporate increased oxide charge density due to unintended variations in processing. The oxide capacitance of the devices results in $C_{OX} = 0.67 \cdot 10^{-6}$ F/cm², and

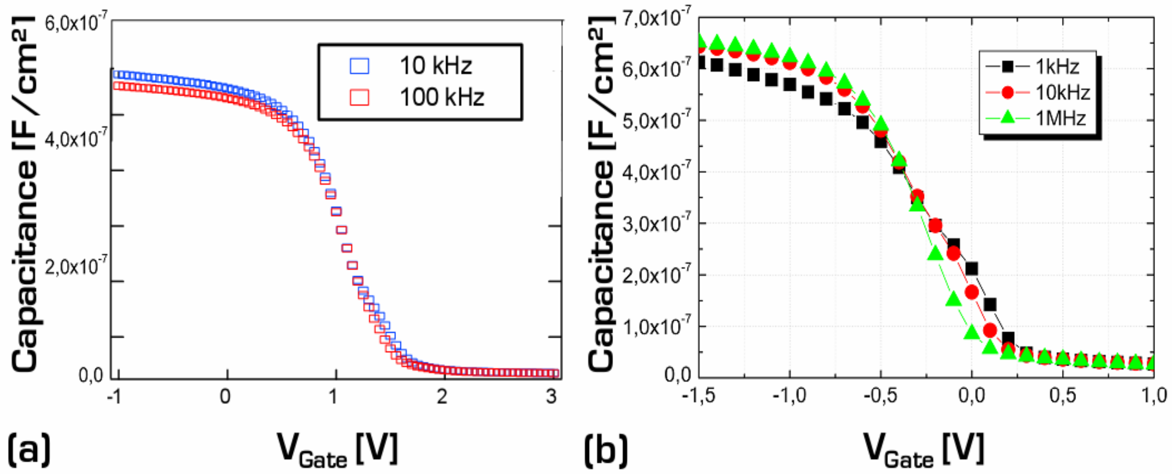

Figure IV.19: C-V measurements of Mo/HfO_2/p-Si capacitors at various ac-frequencies: (a) Results before PMA, and RTA, and (b) after PMA, and RTA are shown.

hence the overall relative permittivity of the dielectric stack ε_r = 10.6 and the corresponding EOT = 5.2 nm. Similar annealing effects as in the case of ZrO_2 may be assumed: Oxide trapped charge is most likely annealed, which can be seen by the results of the hysteresis measurement shown in figure IV.20(a). I-V measurements that are depicted in figure IV.20 (b) exhibit clearly increased values, indicating physico-chemical changes within the oxide.

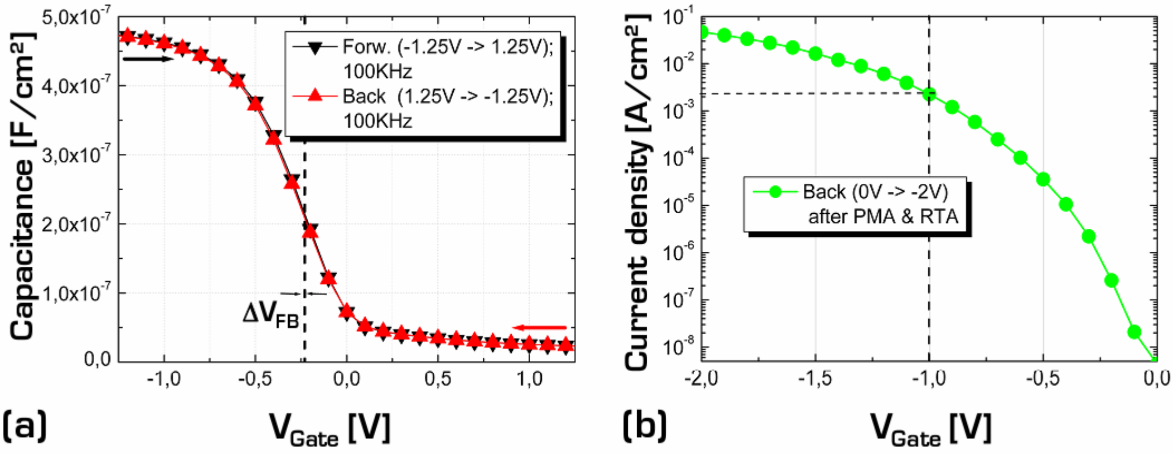

Figure IV.20: (a) C-V hysteresis measurements of Mo/HfO_2/p-Si capacitor at f = 1 MHz. The shift Δ of the V_{FB} is indicated. (b) I-V measurements after PMA, and RTA. The technological relevant value at V_G = -1 V is indicated.

Table IV.D summarizes the obtained key data for the investigated Mo/ZrO_2/p-Si and Mo/HfO_2/p-Si MOSCAPs.

Table IV.D: Summary of key data of Mo/ZrO_2/p-Si and Mo/HfO_2/p-Si capacitors after PDA, PMA and RTA*.

Gate Dielectric:	**ZrO_2**	**HfO_2**
Oxide capacitance per area [$\cdot 10^{-6}$ F/cm²]	0.95	0.67
Rel. permittivity of dielectric stack ε_r [-]	19.3	10.6
Equivalent oxide thickness (EOT) [nm]	3.6	5.2
Flatband voltage V_{FB} [V]	-0.16	-0.23

* Only data obtained at our institution is shown

IV.2.5 Comparison of the different gate stacks

Table IV.E summarizes obtained EOT, ε_r, and V_{FB} for the different metal-gates on ZrO_2/p-Si stacks. The thermal budget applied to all gate stacks was PDA at 650 °C, and PMA at 400 °C in FGA, respectively. In the case of Mo only data after an additional RTA-step at 950 °C in Ar is applicable. Corresponding HF-characteristics at 1 MHz measurement frequency are compared in figure IV.21. As shown, the TiN-, and the Mo-gate stacks show superior C-V behaviour (note the sharp transition from accumulation to inversion range) using the shape of the HF C-V-curve as a reference. Ni, TiN and Mo hint a mid-gap workfunction, whereas our presented results show that pure Ni-gates - combined with ZrO_2 as the gate insulator - don't show promising potential as a gate stack.

The resulting EOT of the ZrO_2 gate stacks dependent on the physical thickness of the overall gate dielectric is depicted in figure IV.22. Values prior to any temperature processing steps are taken, since these should be independent on the gate material. The fit of the data delivers the

Table IV.E: Summary of different metal gate/ZrO_2/p-Si(100) capacitors.

Gate:	**Al**	**Ni**	**TiN**	**Mo**
EOT [nm]	4.5[a]/4.9[b]	3.2/4.8	2.7/2.6	3.6[c]
ε_r **[-]**	14.6/13.4	12.4/8.1	8.8/8.9	19.3
V_{FB} **[V]**	-0.24/-1.48	-0.58/-0.01	-0.85/-0.05	-0.16

[a] Values obtained after PDA
[b] Values obtained after PMA
[c] Values obtained after PMA and RTA

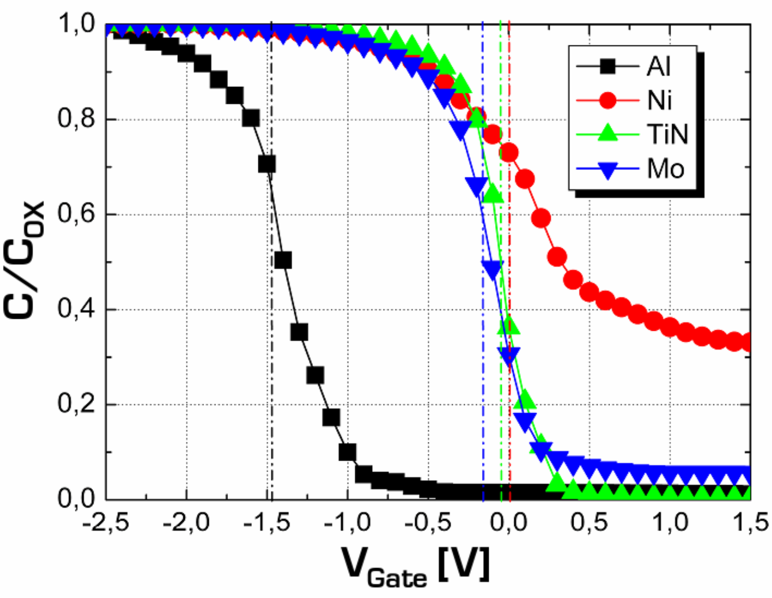

Figure IV.21: C-V curves at 1 MHz measurement frequency of different metal gate/ZrO_2/p-Si stacks. Respective corresponding V_{FB} are indicated.

expected linear correlation after equation II.30. Hence, the intercept of the fit with the EOT-axis yields the mean value of the interfacial SiO_2, which is about 1.7 nm and correlates with the HR-TEM measurements. By this, it can be significantly seen that by the applied processing scheme any achievable EOT is limited by this value.

From the slope of the linear fit in figure IV.22, which is equal to $\kappa_{SiO2}/\kappa_{ZrO2}$, one can obtain the mean value of the relative dielectric constant of the present ZrO_2, delivering $\kappa = 22.7$. This value agrees with literature (e.g.: [118]). Nevertheless, from table IV.E one can see that the value of the overall permittivity of the dielectric stack does not correlate with the

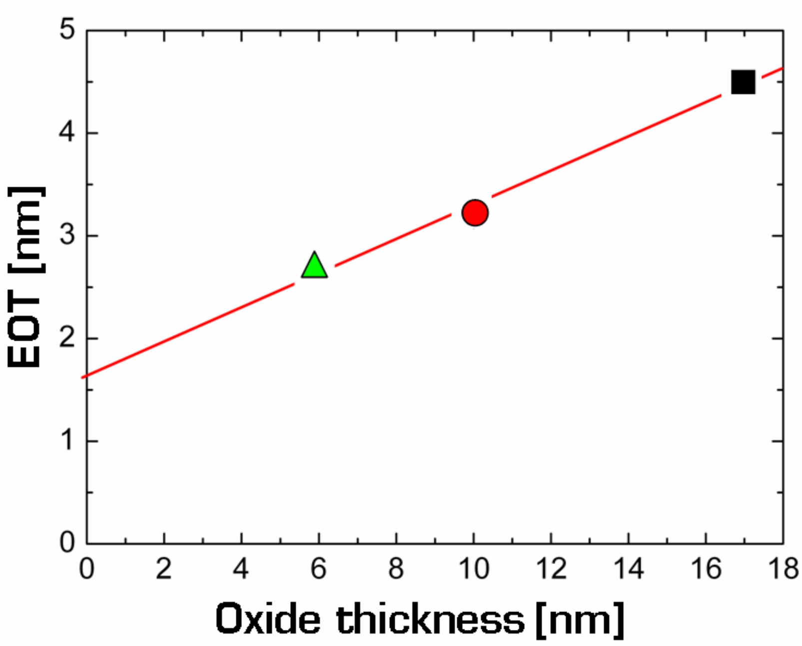

Figure IV.22: Plot of EOT over physical oxide thickness for different metal gate/ZrO_2/p-Si devices. The shown trend line is of the form: EOT [nm] = A [-] · t_{Oxide} [nm] + B[nm], whereas A is the slope of the trend line and B is the y-axis intercept.

corresponding EOT, since the ratio of the interfacial oxide grows with shrinking physical oxide thickness. After temperature processing this divergence increases, because thermal instability of gate stacks – especially in the case of Ni-gates – further influences the electrical behaviour of the stack, and correspondingly the resulting EOT and overall relative permittivity.

Finally, the impact of the single thermal processing steps on the permittivity, EOT, oxide trap density, interface trap density, and leakage current density of the gate stacks we investigated, is shown in table IV.F. It is important to add that this table only shows general trends that can be forecasted from our results. This concluding summary on the influence of thermal processing on important figures of merit of the investigated metal–gate/high-κ oxide/silicon devices closes the gap to the finalizing chapter of this thesis. At this, we draw the main conclusions that we gained by performing this exploratory work and try to give an outlook whereto this highly up-to-date and dynamic research topic might lead.

Table IV.F: Impact of single thermal processing steps on various figures of merit. Positive effects are shaded.

Figure of merit	PDA[a] in FGA[d] 650 °C 5 min	PMA[b] in FGA 400/450 °C 30 min	RTA[c] in Ar[e] 800/950°C 5 min/10 s
Rel. permittivity ε_r	↑	-	-
Equ. Oxide Thickness, EOT	↓	-	-
Oxide trap density	↓	↓	↓
Interface trap density	↓	↓	-
Leakage current density	↓	-	↑

[a] Post Deposition Anneal
[b] Post Metallization Anneal
[c] Rapid Thermal Anneal
[d] Forming Gas Atmosphere
[e] Argon Atmosphere
↑ Tends to increase
↓ Tends to decrease
\- No conclusion possible

IV.3 Conclusions and Outlook

Concluding, the content of this work can be divided into two main parts: First, the deposition of ultra thin dielectric films – namely HfO_2 and ZrO_2 – by metalorganic chemical vapor deposition from Hafnium-, and Zirconium-trifluoroacetylacetonate precursors. This part includes pre- and post-processing of the samples, namely sample pre-treatment and post-deposition annealing. The second part comprehends the deposition of suitable metal gate electrodes and the evaluation of the thermal stability of the processed devices.

Concerning the high-κ oxides, the results of this work showed that, though sufficiently high relative permittivity values have been obtained, the demanded EOT of 1 nm and less can not be achieved by these single oxides that exhibit an interfacial silicon dioxide, since any interfacial oxide layer thicker than 0.5 nm prevents this. This conclusion is agreed widespread within the international research community.

In general, temperature processing of the stacks revealed that oxide charge and interface charge densities can strongly be reduced. More precisely, it has been demonstrated that post metallization annealing is suitable to clearly improve interface behavior. Nevertheless, the processed oxides do not exhibit the necessary thermodynamical stability within their bulks and in contact with silicon.

Concerning the metal gate materials, we showed that Ni, Mo, and TiN behave as mid-gap metals on the processed high-κ/p-silicon stacks. Still, except TiN that exhibited thermal stability up to at least 450 °C, these metals will not be applied as gate electrodes in their pure forms, in addition, we showed that Ni in its pure form is not suitable to act as a gate electrode on the investigated devices. Furthermore, mid-gap metals will not be applied in future CMOS-devices, since these would lead to too big threshold voltages. But our results attribute these metals high potential to be applied in future silicon CMOS-technology, if doped with the proper nitrogen content, or implemented as silicides, even though the achieved electrical device characteristics within this work are not yet able to fulfill the strict requirements for upcoming CMOS-technology.

Addressing the points mentioned above, only the implementation of ternary and quaterneary oxides that incorporate silicate or nitrogen - and thereby prevent the formation of interfacial silicon dioxide - will help to overcome the mentioned problems. Hereby, the primary function is attributed to the deposition process, since perfectly arranged thin films of only a few nanometer thickness have to be synthesized. On the other hand, the author is convinced that a diversification of the key materials to address all different applications - like logic, low power, or storage - will take place in future device manufacturing.

Already in 2006 *Samsung* [128] presented a DRAM chip that has been processed in 50 nm node technology and incorporates an ALD-deposited multi-layered dielectric layer ($ZrO_2/Al_2O_3/ZrO_2$). *Intel* [129] recently announced to introduce high-κ/metal-gate technology at its 45 nm node, implementing an ALD-deposited Hf-based dielectric and dual metal gate technology. Since the relative permittivity of such a dielectric stack will most likely not be larger than 14 to 16, the author believes that in future, other dielectric materials, based on the lanthanides that offer a higher permittivity, might be applied. Table IV.G has been published by the *Taiwan Semiconductor Manufacturing Company* [130] and shows the route for possible future implementation of high-κ materials, agreeing with the author's belief.

Table IV.F: Potential alternative high-k dielectrics to replace SiO_2-based gate dielectrics (after *TSMC* [132]).

Gate dielectric	**Rel. diel. constant κ**	**High performance EOT limit [Å]/V_{max} [V]**	**Low-power EOT limit [Å]/V_{max} [V]**
SiO_xN_y	~5	~12/1.2	~20/1.2
SiN	~7	~9/1.0	~16/1.2
Hf-, Zr-, Al-based	~10 - 20	~7/0.9	~12/1.2
Lanthanide (e.g. La_2O_3)	~ 30	~3/0.6	~6/0.9

PART V: REFERENCES AND APPENDIX

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V.2 Appendix

V.2.1 List of symbols

Symbol	Description	Unit
A	Area	m^2
C	Capacitance	F
D	Diffusion coefficient	cm^2/s
E	Energy	eV
E_c	Bottom of conductance band	eV
E_f	Fermi energy level	eV
E_{fm}	Metal work function	eV
E_g	Energy band gap	eV
E_v	Top of valence band	eV
E	Electric field	V/m
f	Frequency	Hz
$\hbar$	Reduced Planck constant (= 1.055x10^{-34} J·s)	J·s
I	Current	A
I_D	Drain current	A
J	Current density	A/m^2
k	Boltzmann constant (= 1.381x10^{-23} J/K)	J/K
L	Length	m
m^*	Electron effective mass	kg
n	Density of free electrons	cm^{-3}
N_A	Ionized acceptor dopant density	cm^{-3}
N_D	Ionized donator dopant density	cm^{-3}
p	Density of free holes	cm^{-3}
Q	Net effective charge	C/cm^2
q	Elementary charge (= 1.602x10^{-19} C)	C
R_a	Average roughness	m
T	Absolute temperature	K
t_{ox}	Physical oxide thickness	m
V	Voltage	V
V_{FB}	Flatband voltage	V
V_T	Threshold voltage	V
W	Width	m
w	Depletion layer width	m
x/y	x,y direction	-
κ	Relative dielectric constant	-
ε_r	Relative dielectric permittivity	-
ε_0	Permittivity in vacuum (= 8.854x10^{-14} F/cm)	F/cm
ε	Dielectric permittivity (= $\varepsilon_0 \cdot \kappa$)	F/cm
τ	Lifetime or switching time	s
λ	Wavelength	m
μ_n	Electron mobility	cm^2/(V·s)
μ_p	Hole mobility	cm^2/(V·s)
ϕ	Local potential	-
ϕ_S	Potential at the silicon surface	-

Symbol	Description	Unit
ϕ_B	Potential in the silicon bulk	-
ϕ_F	Fermi potential	-
ϕ_M	Metal work function	-
χ	Semiconductor electron affinity	-
ρ	Electric charge density	C/cm²
ψ	Local band bending	-
ψ_S	Surface potential/Total bend bending	-

V.2.2 Index of equations

Equation	#
$J_n(x,y) = q\mu_n nE + qD_n \frac{dn}{dy}$	II.1
$n = n_{pB} e^{q(\phi - V - V_{SB})/kT}$	II.2
$\frac{dn}{dy} = \frac{q}{kT} n\left(\frac{d\phi}{dy} - \frac{dV}{dy}\right)$	II.3
$J_n(x,y) = -q\mu_n n \frac{dV}{dy}$	II.4
$I_D = -\left(\frac{W}{L}\right)\int_0^{V_{DS}} dV(y)\mu_n(y)Q_n(y)$,	II.5
$Q_n(y) = -q\int_0^{x_W} n(x,y)dx$	II.6
$\nabla^2\phi(x,y,z) = \frac{-\rho(x,y,z)}{\varepsilon_S}$	II.7
(electric charge density $\rho(x,y,z) = q(N_D - N_A + p_p - n_p)$)	II.8
$Q_n = -\frac{1}{2}\lambda C_{ox}\sqrt{\frac{q}{kT}}G(\phi, V, V_{SB}, \phi_F)$	II.9
$V_G - V_B - V_{FB} = V_{OX}(y) + \psi_S(y)$ $V_{GB} = V_{FB} + V_{OX}(y) + \psi_S(y)$	II.10
$Q_s(y) = Q_n(y) + Q_d(y) = -V_{OX}(y)C_{OX}$	II.11
$I_D = \mu_n\left(\frac{W}{L}\right)C_{OX}(V_G - V_T)V_D$	II.12
$I_D = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)(V_G - V_T)^2$	II.13
$n(x) = N_D \exp\left(\frac{q\psi(x)}{kT}\right)$	II.14
$p(x) = N_A \exp\left(-\frac{q\psi(x)}{kT}\right)$	II.15
$q\phi(x) \equiv E_F - E_i(x)$	II.16
$\psi(x) \equiv \phi(x) - \phi_B$	II.17

Equation	#
$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_S}$	II.18
$Q_S = \varepsilon_S F_S = \mathrm{sgn}(u_B - u_S) C_o \left(\frac{kT}{q}\right) F(u_S, u_B)$	II.19
$\lambda_i = \left(\frac{\varepsilon_s kT}{2q^2 n_i}\right)^{1/2} \left[cm\right]$ [14]	II.20
$\rho(x) = q\left[N_D(x) - N_A(x)\right]$	II.21
$F(x) = \frac{q}{\varepsilon_S}\int_w^x \left[N_A(x') - N_D(x')\right] \cdot dx'$	II.22
$\psi(x) = \frac{q}{\varepsilon_S}\int_w^x dx'(x - x')\left[N_A(x') - N_D(x')\right]$	II.23
$F(x) = \frac{q}{\varepsilon_S}(N_A - N_D)(x - w)$	II.24
$\psi(x) = \frac{1}{2}\frac{q}{\varepsilon_S}(N_A - N_D)(x - w)^2$	II.25
$\psi(x) = \psi_S\left(1 - \frac{x}{w}\right)^2$	II.26
$\tau = \frac{C_{Load} V_D}{I_D}$	II.27
$\tau_{scaled} = \frac{C_G V_D}{I_D} \cdot \frac{1}{\alpha}$	II.28
$\frac{C}{A} = \frac{\kappa\varepsilon_0}{t}$	II.29
$EOT = t_{eq} = \frac{\kappa_{SiO_2}}{\kappa_{High-\kappa}} \cdot t_{High-\kappa}$	II.30
$I_{DT} = \frac{A}{t_{OX}^2}\exp\left[-2t_{OX}\sqrt{\frac{2m^* q}{\hbar^2}\left(\phi_B - \frac{V_{OX}}{2}\right)}\right]$	II.31
$I_{FP} \cong E\exp\left[-\frac{q}{kT}\left(\phi_B - \sqrt{\frac{qE}{\pi\varepsilon_i}}\right)\right]$	II.32

Equation	#
$EOT = \frac{\kappa_{SiO_2}}{\kappa_{IL}} \cdot t_{IL} + \frac{\kappa_{SiO_2}}{\kappa_{High-\kappa}} \cdot t_{High-\kappa}$	II.33
$ZrCl_4 + 2\ CO_2 + 2\ H_2 \rightarrow ZrO_2 + 2\ CO + 4\ HCl$	II.34
$C = \frac{dQ_G}{dV_G}$	II.35
$Q_G = -(Q_S + Q_{IT})$	II.36
$V_G = V_{FB} + V_{OX} + \psi_S$	II.37
$C = -\frac{dQ_S + dQ_{IT}}{dV_{OX} + d\psi_S}$	II.38
$Q_S = Q_p + Q_B + Q_n$	II.39
$C = \frac{1}{\frac{1}{C_{OX}} + \frac{1}{C_p + C_B + C_n + C_{IT}}} = \frac{C_{OX}(C_p + C_B + C_n + C_{IT})}{C_{OX} + C_p + C_B + C_n + C_{IT}}$	II.40
$\left\lvert \frac{dV_G}{dt} \right\rvert \leq \frac{q \cdot n_i \cdot W \cdot A}{\tau_G C}$	II.41
$t = \frac{\kappa \cdot \varepsilon_0}{C_{Acc}}$	II.42
$Q_{OX} = (V_{FB,ideal} - V_{FB,real})C_{OX}$	II.43
$D_{IT} = \frac{C_{OX}}{q} \frac{d(\Delta V_G)}{d\psi_S}$	II.44
$D_{IT} \approx \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{\max}$	II.45
$\phi_{MS} = \phi_M - \left(\chi + \frac{E_g}{2q} - \psi_B \right) = 0$; n-MOS $\phi_{MS} = \phi_M - \left(\chi + \frac{E_g}{2q} + \psi_B \right) = 0$. p-MOS	II.46
$V_{FB} = \phi_{MS} \pm \frac{Q_{OX}}{C_{Acc}} = \phi_{MS} \pm \frac{Q_{OX}}{\varepsilon_0 \kappa} t$	II.47
$R_a = \frac{1}{N} \cdot \sum_{i=1}^{N} \left\lvert h_i - \bar{h} \right\rvert$	IV.1
$\bar{h} = \frac{1}{N} \cdot \sum_{i=1}^{N} h_i$	IV.2

V.2.3 Index of figures

Index	Description
IV.1	Chemical composition obtained by Augere electron spectroscopy of ZrO_2 thin films as a function of (a) deposition temperature, and (b) of post-deposition annealing temperature. The as-deposited samples in (b) have been grown at 350°C. The “common” measurement values are taken and adapted from [85]; the “stars” indicate the values obtained in this work. Symbol size exceeds measurement inaccuracy (1 - 2 at%).
IV.2	AFM-image of an 8 nm thick ZrO_2 film, deposited at 450 °C. The average roughness R_a is about 0.9 nm.
IV.3	Average roughness of as-deposited ZrO_2 films dependent on deposition temperature and film thickness. The red star indicates the values obtained in this work.
IV.4	Cross section HR-TEM image of a Mo/ZrO_2/p-Si gate stack. The overall thickness of the gate oxide is ~ 20 nm incorporating a ~ 1.5 nm – 2 nm thick interfacial SiO_2 layer. The right image is the magnified section of the left image.
IV.5	C-V measurements of Al/ZrO_2/p-Si capacitors at various ac-frequencies: (a) Uncorrected and (c) corrected results before PMA in FGA, and (b) Uncorrected and (d) corrected results after PMA, are shown.
IV.6	I-V measurements of Al/ZrO_2/p-Si capacitors: (a) Forward-, and back measurements, and (b) comparison of back measurements before and after PMA. The technological relevant values at V_G = -1 V are indicated.
IV.7	(a) Semi-logarithmic plot of $\lvert I_G/V_G \rvert$ over $\lvert V_G \rvert^{1/2}$ to examine conduction mechanisms during I-V measurements. (b) Frenkel-Poole model suggesting the tunneling of carriers over traps within the insulator.
IV.8	C-V measurements of Ni/ZrO_2/p-Si capacitors at various ac-frequencies: (a) Corrected results before PMA in FGA, and (b) after PMA are shown.
IV.9	(a) Schematic of the ac-current flow through the Ni/ZrO_2/p-Si gate stack at zero dc-bias. The equivalent circuit in (b) shows the distributed channel resistance-capacitance network beyond the gate. The distributed channel network can be replaced as shown in (c). All figures are adapted from [124].
IV.10	HR-TEM image of a Ni/ZrO_2/p-Si gate stack after PMA in FGA at 400°C.
IV.11	(a) Scanning-TEM (STEM) picture of Ni/ZrO_2/p-Si gate stack after PMA in FGA. The red-marked area is magnified in (b). Energy Dispersive X-ray (EDX) analysis along line 0 - 1 is shown in (c).
IV.12	(a) C-V hysteresis measurements of Ni/ZrO_2/p-Si capacitor at f = 1 MHz. The shift Δ of the V_{FB} is indicated. (b) I-V measurements before and after PMA. The technological relevant values at V_G = -1 V are indicated.
IV.13	C-V measurements of TiN/ZrO_2/p-Si capacitors at various ac-frequencies: (a) Corrected results before PMA in FGA, and (b) after PMA are shown.
IV.14	(a) C-V hysteresis measurements of TiN/ZrO_2/p-Si capacitor at f = 1 MHz. The shift Δ of the V_{FB} is indicated. (b) I-V measurements before and after PMA. The technological relevant values at V_G = -1 V are indicated.
IV.15	HR-TEM image of a TiN/ZrO_2/p-Si gate stack after PMA in FGA at 450°C.
IV.16	C-V measurements of Mo/ZrO_2/p-Si capacitors at various ac-frequencies: (a) Results before PMA, and RTA, and (b) after PMA, and RTA are shown.
IV.17	(a) C-V hysteresis measurements of Mo/ZrO_2/p-Si capacitor at f = 1 MHz. The shift Δ of the V_{FB} is indicated. (b) I-V measurements after PMA, and RTA. The technological relevant value at V_G = -1 V is indicated.

V.2.4 Index of tables

V.2.5 list of publications

#	**Publication**
1	S. Harasek, S. Abermann, W. Brezna, J. Smoliner, E.Bertagnolli: "MOCVD of zirconium-oxide thin films for High-K dielectrics", *SINANO-NANOCMOS* Meeting, 26.-28. January 2005, Grenoble, France, (Poster presentation)
2	S. Abermann, W. Brezna, J. Smoliner, E. Bertagnolli, E. Gornik: „SINANO-12 month progress report", January 2005 (Report)
3	S. Abermann, W. Brezna, J. Smoliner, and E. Bertagnolli: "Nanoscopic versus macroscopic C-V characterization of high-k - MOCVD ZrO_2 thin films", 31st International Conference on Micro- and Nano-Engineering, 19.-22. September 2005, Vienna, Austria, (Poster presentation)
4	S. Abermann, W. Brezna, J. Smoliner, and E. Bertagnolli: "Nanoscopic versus macroscopic C-V characterization of high-k-MOCVD ZrO_2 thin films", *Microelectronic Engineering* 83 (4-9), p. 1055-1057, (2006)
5	S. Abermann, C. Jordan, M. Harasek, and E. Bertagnolli: "Processing and simulation of few nm thick high-k dielectric films", 31st International Conference on Micro- and Nano-Engineering, 19.-22. September 2005, Vienna, Austria, (Poster presentation)
6	Abermann S., Efavi J., Lugstein A., Auer E., Gottlob H., Schmidt M., Lemme M., and Bertagnolli E.: "Impact of Al, Ni And TiN gates on ZrO_2-MOS Capacitors", ECS Fall Meeting 16.-21. October, Los Angeles, (2005), (Talk)
7	Abermann S., Efavi J., Lugstein A., Auer E., Gottlob H., Schmidt M., Lemme M., and Bertagnolli E.: "Impact of Al, Ni And TiN gates on ZrO_2-MOS Capacitors", "ECS Transactions 1, LA-G3" *ECS Trans. 1 (5)*, 507, (2006)
8	C. Jordan, S. Abermann, M. Harasek, and E. Bertagnolli: "Optimierung eines CVD-Reaktors", ZID-Projektbericht 2005, TU Wien
9	Abermann S., Efavi J., Sjoblom G., Lemme M., Olsson J., and Bertagnolli E.: "Impact of Al-, Ni-, TiN-, and Mo metal gates on MOCVD-grown HfO_2 and ZrO_2 high-k dielectrics", 14th Workshop on Dielectrics in Microelectronics, Santa Tecla, Italy, 26. -28. June 2006, (Talk)

#	Publication
10	S. Abermann, J. Efavi, G. Sjoblom, M. Lemme, J. Olsson, and E. Bertagnolli.: “Impact of Al-, Ni-, TiN-, and Mo metal gates on MOCVD-grown HfO_2 and ZrO_2 high-k dielectrics”, *Microelectronics Reliability* 47. p. 536–539, (2007)
11	S. Abermann, G. Sjoblom, J. Efavi, M. Lemme, A. Lugstein, E. Auer, H. Gottlob, M. Schmidt, J. Olsson, and E. Bertagnolli: “Comparative study on the impact of TiN and Mo metal gates on MOCVD-grown HfO_2 and ZrO_2 high-k dielectrics for CMOS technology”, 28th International Conference on the Physics of Semiconductors, Vienna, Austria, 24. – 28. July 2006, (Poster presentation)
12	S. Abermann, G. Sjoblom, J. Efavi, M. Lemme, A. Lugstein, E. Auer, H. Gottlob, M. Schmidt, J. Olsson, and E. Bertagnolli: “Comparative study on the impact of TiN and Mo metal gates on MOCVD-grown HfO_2 and ZrO_2 high- dielectrics for CMOS technology”, 28th International Conference on the Physics of Semiconductors, Vienna, Austria, July 2006, AIP Publishing, accepted
13	S. Abermann, J. Efavi, G. Sjoblom, M. Lemme, J. Olsson, and E. Bertagnolli: “Processing and evaluation of metal gate/high-k/Si capacitors”, 32st International Conference on Micro- and Nano-Engineering, Barcelona, 17.-20. September 2006, (Poster presentation)
14	S. Abermann, J. Efavi, G. Sjoblom, M. Lemme, J. Olsson, and E. Bertagnolli: “Processing and evaluation of metal gate/high-k/Si capacitors”, *Microelectronic Engineering* 84, p. 1635–1638, (2007)
15	S. Abermann, G. Sjoblom, J. Efavi, M. Lemme, A. Lugstein, E. Auer, H. Gottlob, M. Schmidt, J. Olsson, and E. Bertagnolli: “Comparative study on the impact of TiN and Mo metal gates on MOCVD-grown HfO2 and ZrO2 high- dielectrics for CMOS technology”, GMe-Workshop 2006, Oct. 13, 2006, Vienna, Austria (Poster presentation)
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V.2.6 Curriculum Vitae

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