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Synthesis, Doping and Characterization of Silicon Nanowires

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Abstract

The current master thesis describes the synthesis of silicon nanowires via the Vapor-Liquid-Solid (VLS) growth mechanism. The goal of this work is the achievement of an efficient postgrowth doping method for silicon nanowires.

The first chapter explains the needs for further miniaturization of electronic devices. An introduction into structural methods, and the properties and advantages of nanowires is given. The second chapter describes theoretical principles of the VLS growth mechanism, the important role of gold as catalyst, and epitaxial nanowire growth, followed by a section about the characterization of electrical properties of silicon nanowires. Finally, in-situ, diffusion, and ion implantation doping are described in detail.

After these theoretical considerations with regard to the experimental work, the test assemblies are presented in the third chapter. This part covers the setup of the low pressure chemical vapor deposition (LPCVD) system, the sample preparation, and the influence of the surface pretreatment for epitaxial nanowire growth. The following section describes the contact formation to silicon nanowires via electron beam lithography, metal deposition and lift-off techniques. Next, the doping processes of VLS grown silicon nanowires are shown. This chapter is concluded by the description of the used setup for the electrical characterization of silicon nanowires. The results of the experimental work are illustrated in the fourth chapter. The synthesized silicon nanowires were observed via SEM and TEM, and finally characterized by electrical measurements. The last section deals with the

electrical characterization of doped silicon nanowires. Used doping methods are diffusion doping via Spin-On-Dopant (SOD), thermal evaporation doping via phosphoric acid, and ion implantation.

The last chapter concludes with a summary and gives an outlook to future developments of nanowire integration and devices.

Contents

Chapter 1

Survey

Electronic and optoelectronic devices affect our life in many areas: mobile communication changed our behavior for appointments in business and spare time, new medical equipment improved our quality of life, and made the household chore easier through better and simpler appliances. The demand for more compact and powerful devices is given. The downsizing of integrated circuits advances steadily which means Moore's law[1] is still valid [1]. Structure sizes in micron dimensions were state-of-the-art till the eighties, as structures of sub-micron length dominated the nineties. In todays research technologies structure sizes down to ten nanometers are possible. In spite of the development of ever smaller devices has each technology limits. The continuous downsizing of structures could not always be solved in traditional ways.

The so called top-down structural method (a combination of optical lithography, thin film techniques and etching) for the shaping of integrated circuits

[1] In 1965 G.E. Moore published the paper "Cramming more components onto integrated circuits" in which he described his empirical observations about the development of the complexity of integrated circuits. He specified an exponential growth of the number of components per integrated function at minimum costs. Today in a nanoelectronic perspective we generally understand under Moore's Law that the minimum component size tends to decrease by a factor of $1/\sqrt{2}$ every three years.

has technological limits. An alternative concept for nanoscale structure formation is the bottom-up method, which makes it possible to create complex patterns from atomic or molecular elements, like nanowires.

Nanowires offer many variation possibilities for the development of novel electronic and optoelectronic devices. In 2003 Cui et al. examined high performance nanowire field-effect transistors and showed substantial advantages for nanowires in comparison with state-of-the-art planar silicon devices [2]. Some application examples are nanoscale field-effect transistors, crossed nanowire arrays, and axial or radial nanowire heterostructures [3]. In addition nanowires are also foreseen for solar cells [4] and ultrasensitive detectors for biological and chemical species [5]. But the most important component in the semiconductor industry are field-effect transistors.

The most commonly used process for nanowire synthesis is the vapor-liquid-solid (VLS) mechanism described by Wagner and Ellis in 1964 [6]. This enables the growth of nanowires using miscellaneous semiconductor materials such as: silicon [7], germanium [8] III-V semiconductor compounds (e.g. GaAs [9]), and II-VI semiconductor compounds (e.g. CdS, ZnS [10]).

The control of size, location, orientation, and growth density is essential for a successful implementation of nanowires in electrical circuits [11]. The knowledge of the physical and electrical properties of nanowires are most important to build integrated nanowire devices.

The physical and chemical properties of silicon nanowires differ in various manners from bulk silicon. Li et al. observed that the thermal conductivity of intrinsic single crystalline silicon nanowires is more than two orders of magnitude lower than in bulk silicon due to the increased phonon-boundary scattering and possible phonon spectrum modification [12]. Ma et al. showed that with a decreasing nanowire diameter beneath 7 nm the energy gap increases [13]. Dovrat et al. investigated the optical properties of nanowires and discovered a homogeneous spectrum broadening of the red and blue emission bands from silicon nanowires [14].

Investigations of the electrical properties of silicon nanowires showed that the resistivity of undoped nanowires is lower than that of intrinsic silicon [15]. Measurements of the field effect properties of an intrinsic silicon nanowire in a backgate configuration showed p-type behavior [15]. This implies that silicon nanowires grown via VLS are unintentionally p-doped. Field effect measurements of boron-doped and phosphorus-doped nanowires showed the expected behavior as p-type and n-type materials [15]. Doping of nanowires open many prospects for the future of nanoscale technology. Self-assembly techniques could be used to integrate structures of nanowire field effect transistors for nanoelectronic applications.

This first chapter described the importance of further miniaturizations of integrated circuits and gave an overview to the nanowires properties and its application possibilities. The second chapter of this master thesis covers theoretical aspects of silicon nanowire growth, their electrical properties, and methods of doping silicon nanowires. The third chapter explains the different experimental assemblies for the synthesis of silicon nanowires, doping, electron beam lithography, and electrical measurements. In the fourth chapter the results of my experiments are presented. The work closes with a summary of the obtained results and an outlook for the future developments of possible nanowire applications.

Chapter 2

Introduction

2.1 Overview

The first section of this chapter describes the nanowire synthesis using the Vapor-Liquid-Solid (VLS) mechanism. A further aspect is the important role of gold as catalyst for the nanowire growth via VLS. The next section illustrates the requirements for ordered growth and the different growth directions of silicon nanowires. The following section gives an overview of the measurement methods for the determination of the resistivity and the occurrence of the field effect. The last section gives a comprehensive overview of in-situ doping, diffusion doping (with Spin-On-Dopant and phosphoric acid), and ion implantation.

2.2 Synthesis of silicon nanowires

2.2.1 Silicon nanowire growth via the VLS mechanism

Various methods were reported for the synthesis of nanowires such as the Solid-Liquid-Solid (SLS) [16], the Solution-Solid-Solid [17], the Vapor-Solid-Solid (VSS) [18], and the Oxide-Assisted-Growth (OAG) mechanism [19]. Regardless the most common technique for creating nanowires is the Vapor-Liquid-Solid (VLS) mechanism [6, 20]. Many of the silicon investigations have employed the Vapor-Liquid-Solid (VLS) growth mechanism first introduced by Wagner et. al. [6]. A metal droplet catalyzes the decomposition of a Si-containing source gas, to function as a Si reservoir by eutectic liquid formation, and finally to precipitate silicon nanowires due to supersaturation. Gold has been the metal catalyst of choice and is mostly used due to its favorable physical and chemical properties.

Recently, epitaxially grown silicon nanowires were synthesized by the VLS growth mechanism using silicon tetrachloride ($SiCl_4$) as precursor gas, requiring however relatively high temperatures beyond 800 ℃ [11, 21]. In this case the gaseous hydrochloric acid (HCl), a byproduct of $SiCl_4$ decomposition in the reaction tube, etches the oxide layer on the Si surface, presenting a clean Si crystal surface for epitaxial nanowire growth. Epitaxial silicon has also been grown selectively by intentionally introducing HCl into the SiH_4/H_2 system [22, 23].

Many deposition techniques based on the VLS mechanism exist like laser ablation [24], molecular beam epitaxy (MBE) [25], or chemical vapor deposition (CVD) [6, 7]. The CVD process is the most commonly used technique, using a gaseous precursor which decomposes to provide the semiconductor reactant to the catalyst.

The growth of silicon nanowires via the CVD-VLS process [26] has several stages. Gold is first placed on a silicon wafer to serve as a catalyst. A

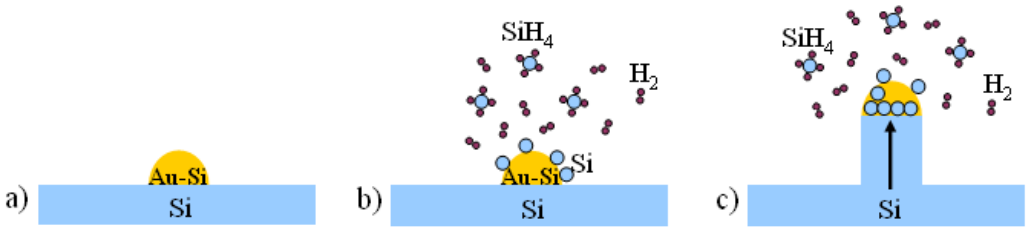


Figure 2.1: *VLS growth mechanism: a) formation of a liquid Au-Si alloy droplet (temperature > 363 ℃), b) precursor decomposition at the droplet surface, c) nucleation and nanowire growth due to supersaturation of the liquid alloy.*

liquid Au-Si alloy droplet is formed after heating above the eutectic temperature of 363 ℃ via interdiffusion (see figure 2.1a). A vapor-phase source (e.g. SiH_4) feeds the alloy droplet. The gaseous precursor decomposes ($SiH_4 -> Si + 2H_2$) at the surface of the catalytic alloy (see figure 2.1b). The continuous gas supply supersaturates the droplet and leads to a nucleation of solid silicon. The silicon diffuses into the metal/semiconductor alloy (Au-Si) and bonds to to the silicon at the liquid-solid interface. The continuous gas flow allows the nanowire growth, always with the alloy droplet on the top (see figure 2.1c).

The binary system of Au-Si has three stable states (see figure 2.2) [27]:

- A **solid gold phase** with a solubility of silicon lower than 2 atomic percent.
- A **consolute Au-Si melt** (liquid area L).
- A **solid silicon phase** with a solubility of gold lower than $2 \cdot 10^{-4}$ atomic percent.

Normally pure gold melts at 1064 ℃. The interdiffusion of silicon with gold distinctly reduces the melting point of the now gold-silicon alloy droplets formed on the surface. The eutectic temperature of 363 ℃ is reached at a concentration of 18.6 atomic percent silicon, which indicates the lowest

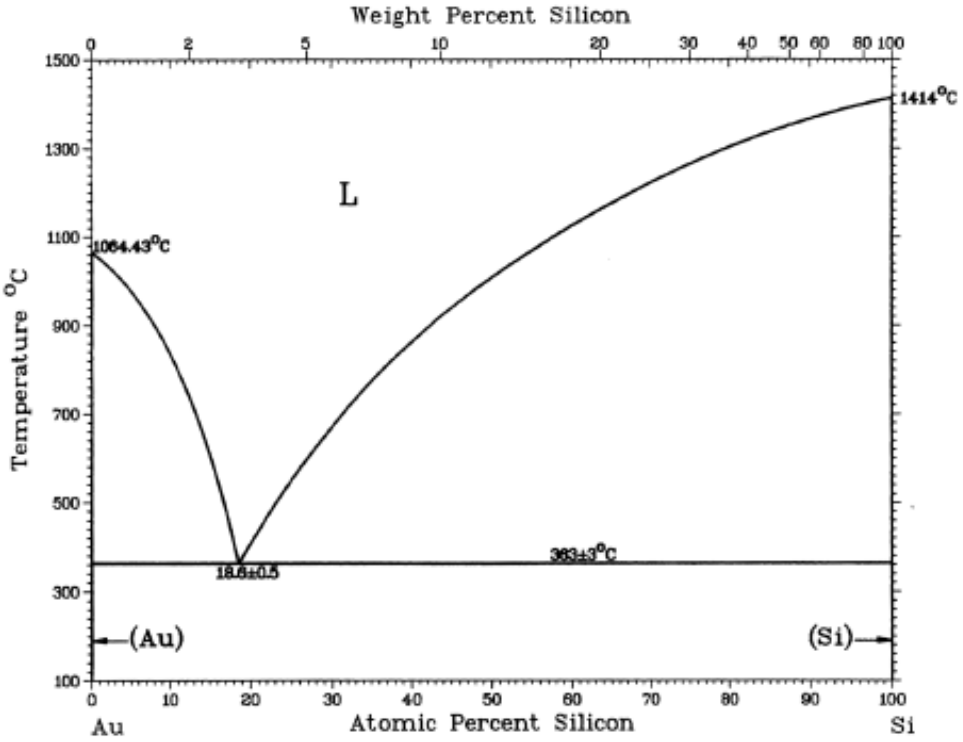


Figure 2.2: *(after Massalski et al., [27]) Binary phase diagram for the Au-Si system with the eutectic temperature at 363 ℃.*

melting point of the system. Continuous supply of the gaseous precursor increases the silicon concentration in the liquid alloy until it reaches the solidus line (see figure 2.2). Now silicon crystals deposit on the surface as a result of supersaturation, and the nanowire starts growing. The gold droplet is placed on top of the grown nanowire.

During the nanowire synthesis via the VLS mechanism two significant interfaces can be observed for nanowire growth [26]:

- The liquid-solid interface (axial growth direction),
- and the vapor-solid interface (radial growth direction).

The actual growth conditions such as temperature, pressure, flow rate, reactant species, and background gases influence the axial and radial growth of the nanowire. For example, nanowire growth at low temperatures favors the axial growth since the rate of thermal dissociation of silane is reduced. A high silane partial pressure affords an increased silicon supply which enhances also the axial growth rate of the nanowire. The use of hydrogen (H_2) as carrier gas reduces the radial growth [26].

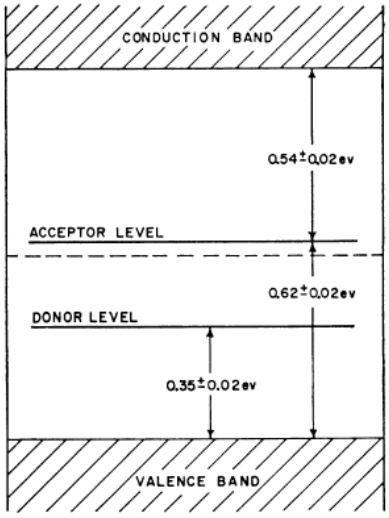


Figure 2.3: *(after Collins et al., [28]) Ionization energies for gold in silicon.*

Gold (Au) is mostly used as catalyst for the growth of silicon nanowires via VLS. It is important to note that gold is generally an unwanted material in standard microelectronic procedures as it induces deep level defects in the silicon (see figure 2.3). These recombination centers (acceptor and donor level) alter the electrical properties of silicon and decrease the minority-carrier lifetime [29]. For this reason other catalysts such as Ti [30], Al [31], or PtSi [32] were successfully integrated. Nevertheless gold has the best properties for the VLS synthesis of silicon nanowires, because it barely reacts with other chemical compounds. Besides, the precursor gas decomposition needs a good catalytic activity which is also offered by gold [33]. Another advantage for the usage of gold is the low solubility of gold in silicon [34]. Compared to

other catalyst materials gold forms an eutectic[1] alloy with silicon at low temperatures.

The lowest melting temperature of the Au-Si alloy at 363 ℃ is called the eutectic point. For an efficient growth of nanowires the temperature has to be slightly above this point. The typical process temperature of the CVD-process for silicon nanowire growth lies between 450 ℃ and 600 ℃. Plasma enhanced chemical vapor deposition (PECVD) [35] allows the growth of nanowires at temperatures below 400 ℃. A low temperature growth ability of nanowires is important for device integration and compatibility with other processes.

2.2.2 Minimum nanowire radius

The minimum diameter of a nanowire grown via VLS is given by the size of the catalytic nanocluster. Due to the supersaturation of the semiconductor in the catalyst droplet during the liquid alloy formation the diameter of the nanowires are slightly thicker [36]. In 1975 Givargizov theoretically examined the thermodynamic aspects of the VLS process, based on the Gibbs-Thomson effect[2]. Givargizov has shown that a minimum radius for nanowires exists [20]. Furthermore Givargizov stated that thin nanowires grow slower than thicker ones due to the increasing vapor pressure and the higher solubility of silicon with decreasing size of the nanocluster diameter. The growth rate decreases due to the fact that the supersaturation declines in conformity with the Gibbs-Thomson effect. In 2007 Dhalluin et al. [38] confirmed experimentally what Givargizov stated theoretically. They were able to show that a silane pressure dependent minimum nanowire radius exits. (see figure 2.4).

[1] From Greek: "eutektos", easily melted

[2] The particle surface is related to vapor pressure and chemical potential by the Gibbs-Thomson effect. This induces a larger effective vapor pressure for small liquid droplets [37].

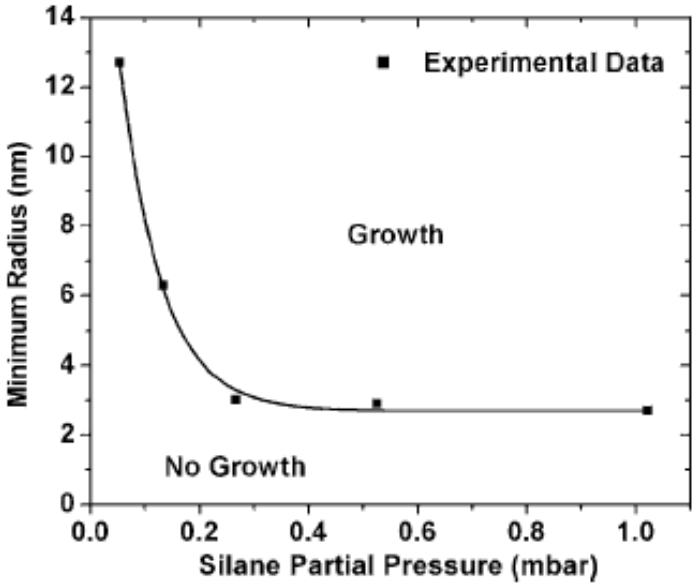


Figure 2.4: *(after Dhalluin et al., [38]) Minimum nanowire radius as a function of the silane partial pressure.*

2.2.3 Epitaxial growth of nanowires

The implementation of nanowires into integrated devices requires good control of the nanowire growth with respect to crystallinity, geometry and orientation. The growth on crystalline substrates has the benefit, that the direction of the nanowires can be influenced by the underlying crystal structure and therefore an ordered synthesis of nanowires becomes possible. The adopting of the crystal orientation by the nanowires is referred to as epitaxial[3] growth. To control the orientation during the nanowire growth it is possible to combine conventional epitaxial growth techniques with the VLS process. This technique is called Vapor-Liquid-Solid-Epitaxy (VLSE) [39].

Figure 2.5 shows the four preferred $\langle 111 \rangle$ directions of silicon nanowires on a **silicon (100) substrate**. Almost every silicon nanowire is naturally perpendicular to one set of $\{111\}$ planes of the substrate [21]. The angle

[3]From Greek: "epi", above; "taxis", in ordered manner

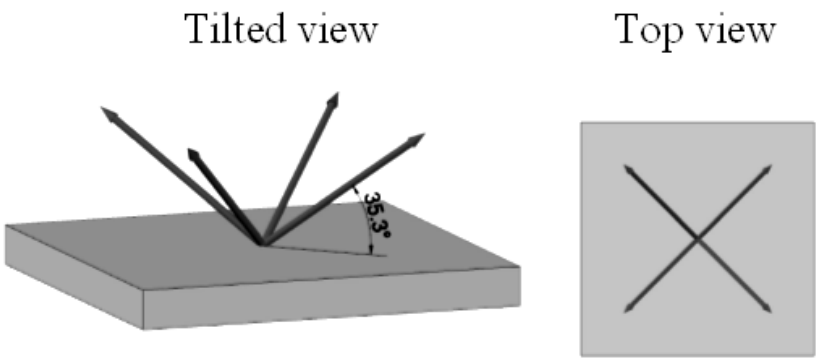


Figure 2.5: *Schematic illustration of the growth directions of epitaxial silicon nanowires on a* ***silicon (100) substrate****.*

between the ⟨111⟩ directions and the surface of the substrate is 35.3°. In the top view the grown nanowires build a network of orthogonal patterns, each projection of a direction is perpendicular to the others.

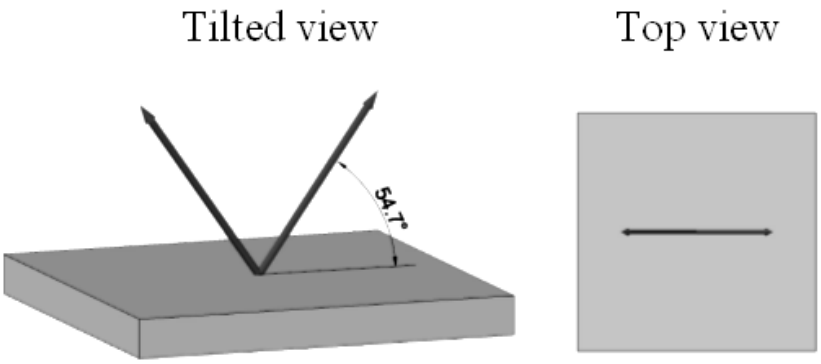


Figure 2.6: *Schematic illustration of the growth directions of epitaxial silicon nanowires on a* ***silicon (110) substrate****.*

Figure 2.6 shows the two equivalent ⟨111⟩ growth directions on a **silicon (110) substrate**. Here the angle between the ⟨111⟩ directions and the surface of the substrate is 54.7°. In the top view the grown nanowires build a network of parallel patterns.

Silicon nanowires grown in a [111] direction on a **silicon (111) sub-**

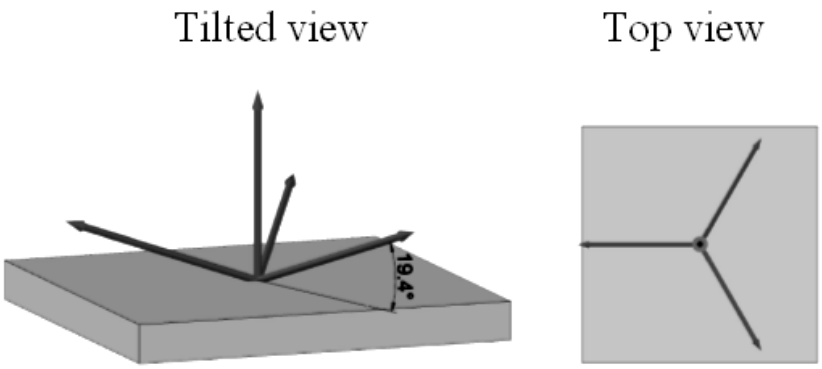


Figure 2.7: *Schematic illustration of the growth directions of epitaxial grown silicon nanowires on a* ***silicon (111) substrate****.*

strate show four epitaxial ⟨111⟩ directions (see figure 2.7). It is noteworthy that at low supersaturation the nanowires grow preferentially along the [111] direction, standing perpendicular to the substrate. At high supersaturation the three other equivalent ⟨111⟩ growth directions are favored, forming an angle of 19.4° with the substrate. In the top view these nanowires build a network of triangular patterns. Intermediate saturation results in a preferential growth in all four ⟨111⟩ directions.

Silicon nanowires grown via the VLS process are highly perfect crystals of macroscopic size [40]. Nanowires with small diameters prefer growth along the ⟨110⟩ directions and larger diameters prefer the ⟨111⟩ directions [41]. The reason for this lies in the fact that a silicon atom precipitating upon the (111) surface during growth produces the largest decrease in Gibbs free energy, because (111) planes of silicon have the largest density of surface atoms when acting as interface [42]. When the diameter is very small, the free energy of the side faces must be taken into consideration and ⟨110⟩ growth directions became more favorable.

The total free energy includes [26]:

- the interfacial energy (Au/Si),

- the surface energy (Si/vacuum),
- and the bulk energy of the nanowire.

The growth axis of silicon nanowires with a diameter above 20 nm is primarily along the ⟨111⟩ directions, whereas nanowires with a smaller diameter grow along the ⟨112⟩ directions, and the smallest nanowires are situated along the ⟨110⟩ directions (see figure 2.8) [41].

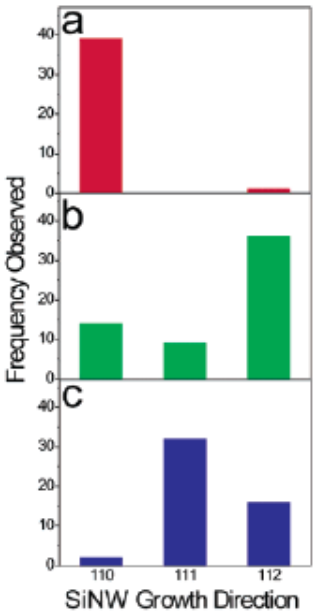


Figure 2.8: *(after Wu et al., [41]) Histograms of the growth directions for silicon nanowires with diameters from (a) 3-10 nm, (b) 10-20 nm, and (c) 20-30 nm.*

2.3 Electrical characterization

2.3.1 Resistivity measurement

A simple method for the electrical characterization of nanowires is the **two-point probe method**. Two metal probe needles are set on each end of the nanowire, a voltage source V is applied between the needles and the current I through the nanowire is measured. The resulting total resistance R_T between the two probes is given by:

$$R_T = \frac{V}{I} = R_{NW} + R_C. \tag{2.1}$$

The problem that arises is that the calculated resistance includes both the nanowire resistance R_{NW} and the unintended contact resistance R_C. In order to eliminate R_C the **four-point probe measurement technique** is used (see figure 2.9) [43].

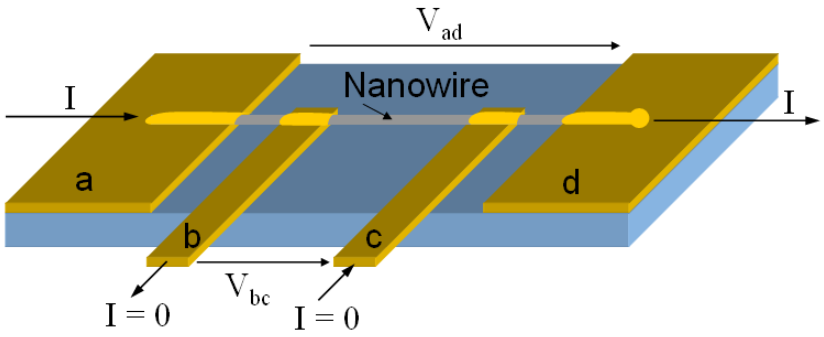


Figure 2.9: *Four-point probe measurement setup to determine the nanowire resistance.*

Two probe needles are connected to the voltage source and carry the current like before (contacts a, d), the other two probe needles are used for the sensing of the voltage drop between contact b and c. As shown in figure 2.9 the inner probe needles (b, c) have ideally no current flow, therefore

the contact resistance R_C is negligible. The measured voltage V_{bc} is consistent with the voltage at the inner segment of the nanowire. The resulting inner resistance is given by: $R_{bc} = V_{bc}/I$. Now it is possible to calculate the specific resistance ρ, also called resistivity. Based on the dimensions of the inner nanowire segment (length l, diameter d) the resistivity ρ is given by:

$$\rho = \frac{R_{bc} \cdot A}{l} \tag{2.2}$$

with the cross-sectional area of the nanowire A given by:

$$A = \pi \cdot \frac{d^2}{4} \tag{2.3}$$

2.3.2 Field effect measurements on nanowire devices

Field effect transistors are significant building blocks in the semiconductor industry, with silicon as the dominating basic material. As a consequence silicon nanowires could be a perfect addition to conventionally fabricated integrated circuits in the future.

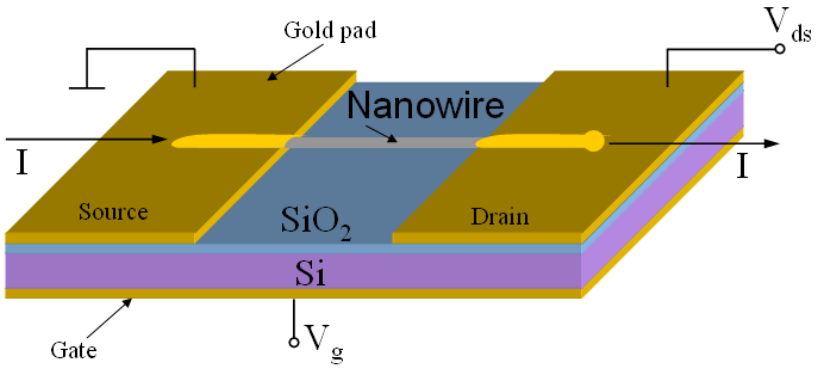
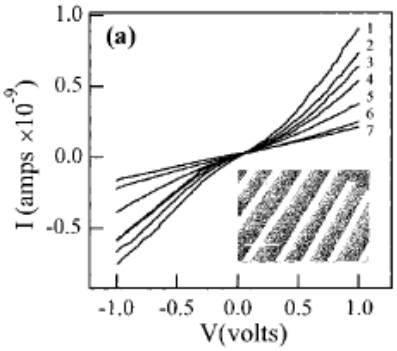


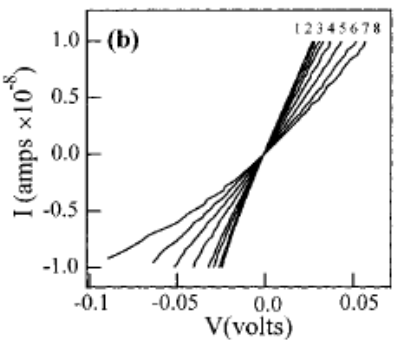
Figure 2.10: *Silicon nanowire field effect measurement in back-gated configuration.*

The measurement of the field effect occurs in a so called back-gated configuration (see figure 2.10). The nanowire is placed on a degenerately (very

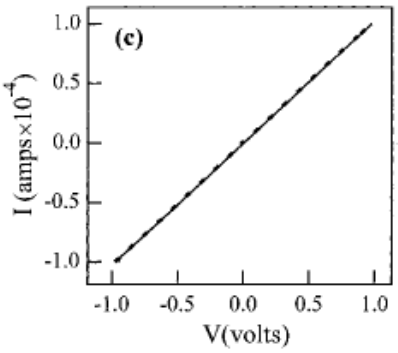
high) doped silicon substrate with a thin oxide layer (SiO_2) as gate dielectric. The nanowire is contacted with gold pads at both ends (source/drain). The substrate acts as a global backgate.



(a) intrinsic Si NW



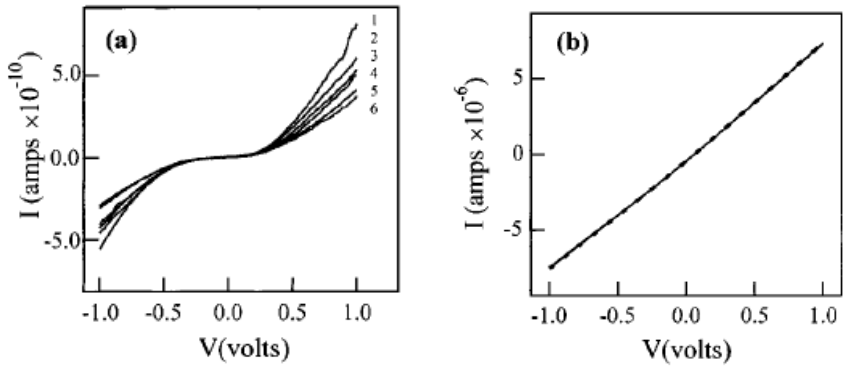
(b) lightly p-doped Si NW



(c) heavily p-doped Si NW

Figure 2.11: *(after Cui et al., [15]) Gate-dependent I-V characteristics of (a) an intrinsic silicon nanowire. Curves 1-7 correspond to V_g = -30, -20, -10, 0, 10, 20, 30 V. (b) a lightly boron doped silicon nanowire. Curves 1-8 correspond to V_g = -20, -10, -5, 0, 5, 10, 15, 20 V. (c) a heavily boron doped silicon nanowire. V_g = 20 V (solid line) and 0 V (dashed line).*

The gate characteristic is used in order to identify the carrier type and the channel mobility [29]. For n-type nanowires an increasing positive gate voltage V_g has to be applied to increase the conductance and therefore the source-drain current I_{ds}. If a negative voltage V_g is applied the channel carriers deplete and reduce the channel conductance. The behavior of p-type channels is inverted. In order to obtain the same behavior the sign of the gate



(a) lightly n-doped Si NW (b) heavily n-doped Si NW

Figure 2.12: *(after Cui et al., [15]) Gate-dependent I-V characteristics of (a) a lightly phosphorus doped silicon nanowire. Curves 1-6 correspond to V_g = 20, 5, 1, 0, -20, -30 V. (b) a heavily phosphorus doped silicon nanowire. V_g = 0 V (solid line) and -20 V (dashed line).*

voltage V_g has to be changed. Field effect measurements of intrinsic silicon nanowires show mostly a p-type behavior (see figure 2.11a) [15]. This result indicates that VLS grown silicon nanowires are unintentionally p-doped. As expected boron doped nanowires show p-type behavior (see figure 2.11b,c) and phosphorus doped nanowires show n-type behavior (see figure 2.12) [15].

2.3.3 Influence of the metal contacts

In conventional MOSFET devices the source/drain contacts are formed by degenerately doped silicon. By contrast metal contacts are used for silicon nanowires. At the metal/semiconductor interface Schottky barriers appear due to the metal work function and the Fermi level pinning of surface states [29]. Accordingly the contact properties affect to a large degree the device performance [44]. Cui et al. showed that thermal contact annealing and surface passivation increase the carrier mobility significantly [2]. The average transconductance increases from 45 to 800 nS and the mobility changes from 30 to 560 cm^2/Vs.

The carrier transport is described by the drift velocity v_d. At low electric fields v_d is proportional to the electric field strength E [29]:

$$v_d = \mu E. \tag{2.4}$$

The proportionality constant is defined as the (drift) mobility μ $[cm^2/Vs]$. The mobility μ of the nanowires can be calculated with the knowledge of the transconductance $g_m = dI/dV_g$ [26]. Transport in an ideal FET-device at low biases is characterized by the following relationship [29]:

$$g_m = \frac{\mu C}{L^2} V_{sd} \tag{2.5}$$

with the total gate capacitance C and the channel length L of the device. Unfortunately the measured extrinsic transconductance $g_{m,}$ is reduced from its intrinsic value g_{in} due to the source/drain contact resistances [45]:

$$g_{ex} = \frac{g_{in}}{1 + g_{in}R_s + (R_s + R_d)/R_{in}} \cdot V_{sd} \tag{2.6}$$

with the source and drain contact resistance R_s, R_d and the intrinsic nanowire resistance R_{in}. Equation 2.6 shows that the performance of the nanowire transistor is influenced by the contact resistance. So the calculated mobility μ using equation 2.5 may greatly differ from the intrinsic mobility of the device.

Zheng et al. compared the transconductance of heavily and lightly n-doped silicon nanowires [45]. Two-probe and four-probe measurements were made to obtain the difference between the extrinsic and intrinsic transconductance values. The result they obtained establish that the contact resistance is negligible for highly doped samples. On the other hand measurements on lightly doped samples showed a big influence of the contact resistance. The calculated intrinsic transconductance value using equation 2.6 is about four times larger than the actually measured one. Figure 2.13(d) shows the mobility values from the measured transconductance in comparison to the corrected intrinsic transconductance. The corrected mobility increases with

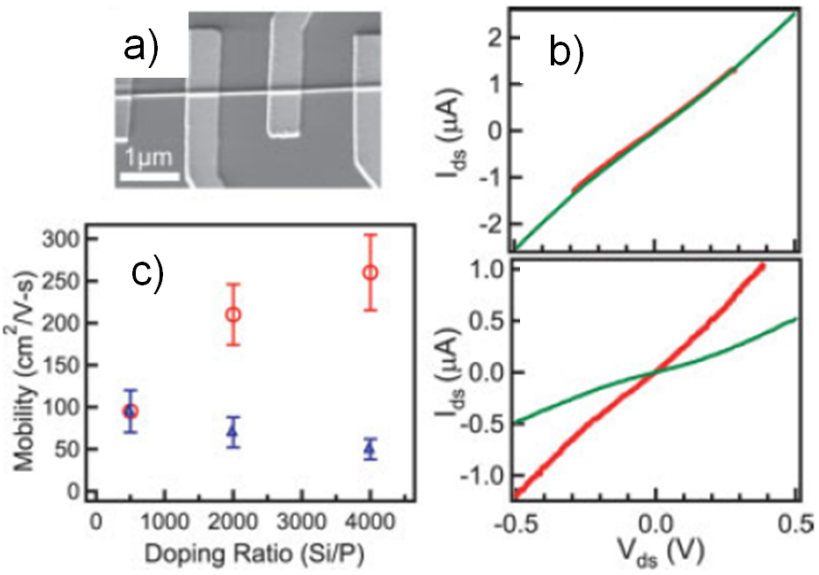


Figure 2.13: *(after Zheng et al., [45]) a) SEM image of a silicon nanowire with four contact pads. b) top figure: $I_{ds} - V_{ds}$ characteristics of a silicon nanowire using two-probe (green) and four-probe (red) contact geometries at a [Si:P] ratio of 500:1 (heavily n-doped). bottom figure: $I_{ds} - V_{ds}$ characteristics of a silicon nanowire using two-probe (green) and four-probe (red) contact geometries at a [Si:P] ratio of 4000:1 (lightly n-doped). (c) Measured (blue) and intrinsic (red) mobility values.*

decreasing doping levels, this is similar to values from bulk silicon.

2.4 Doping of silicon

Doping is used to alter the electrical properties of semiconductor materials. In order to realize electronic components it is necessary to control the desired doping profile and the carrier concentration. To put it simply two methods can be distinguished: in-situ and ex-situ doping. **In-situ doping** is carried out during the growth process of the semiconductor. If the doping takes place afterwards, for example through diffusion or ion implantation, the process is called **ex-situ doping**.

2.4.1 In-situ doping of silicon nanowires

An obvious in-situ doping method is the introduction of an additional gas, which acts as doping source, during the VLS growth of the nanowire. For n-type doping of silicon nanowires phosphine (PH_3) is mostly used as doping source gas [45]. Favored gas sources of p-type dopants during VLS growth of silicon nanowires are diborane (B_2H_6) [46], or trimethylboron ($B(CH_3)_3$, TMB) [47]. Pan et al. observed in-situ doping of silicon nanowires with diborane [46]. In-situ doping also influences the growth process of nanowires. "Higher" doped nanowires were unlike the "lower" doped case curved and kinked [46]. The TEM observations revealed in the majority of cases core-shell structures with a rippled interface between the core and the shell. The core is crystalline (typical diamond-cubic silicon structure) surrounded by an amorphous shell. A remarkable anomaly is the absence of the gold droplet on top of the nanowire. This means that the addition of diborane leads to constant loss of gold from the gold-silicon alloy. A possible explanation for the loss of gold are instabilities at the liquid/solid interface caused by the increased deposition rate of silicon due to the addition of diborane. The solubility of interstitial gold which diffuses rapidly in heavily doped p-Si becomes significant. Segmentally doped nanowires are possible by switching on and off the dopant source during growth. These nanowires show that the diameter of the doped sector is slightly larger than the undoped sector

(see figure 2.14). Some of the segmentally doped nanowires changed the growth direction after the addition of diborane (see figure 2.15). Although the specific growth direction changes the nanowire remains a single crystal.

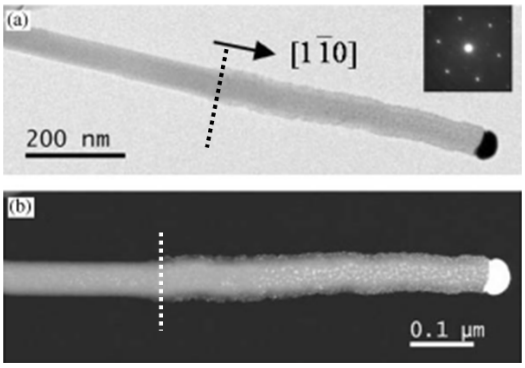


Figure 2.14: *(after Pan et al., [46]) a) Bright-field TEM image with the corresponding diffraction pattern in the inset and b) ADF-STEM image of a segmentally doped silicon nanowire grown in the same direction after the addition of diborane.*

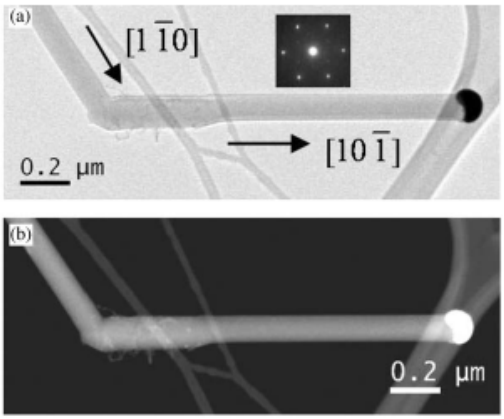


Figure 2.15: *(after Pan et al., [46]) a) Bright-field TEM image with the corresponding diffraction pattern in the inset and b) ADF-STEM image of a segmentally doped silicon nanowire that changed growth direction after the addition of diborane.*

An investigation by Kawashima et al. had concluded that the doping is based primarily upon conformal deposition of high boron concentration layers

on the sidewalls of the nanowire during the VLS growth [48]. Such boron doped nanowires have a gradient of boron concentration along the growth direction, with the lowest concentration at the top region. The sidewalls of high boron concentration are defective. Most of the boron atoms are not activated, therefore an annealing step is required. Annealing of the silicon nanowires at 1000 ℃ for one minute increased the boron concentration significantly in the top region [49]. High boron doped nanowires now had an averaged concentration along the whole length.

In addition Imamura et al. examined controlled growth of silicon nanowires with controlled impurity profiles [49]. The results showed that it is possible to grow nanowires with a diborane gas source at the beginning and a stopped boron source in the middle of the growth. The p-doped and the intrinsic region (p-i nanowires) showed differences at the TEM observation. On the contrary growth of intrinsic/p-doped nanowires (i-p nanowires) was impracticable, because both regions were heavily boron doped. The intrinsic region is doped subsequently due to the conformal deposition of the high boron concentration on the side walls of the nanowire.

The most preferred gaseous n-type doping source during the VLS growth of silicon nanowires is phosphine (PH_3) [45]. A structural analysis and a electrical characterization of phosphine doped silicon nanowires was made by Wang et al. [50]. The TEM analysis revealed that phosphine doped nanowires are mainly single crystal with a thin native oxide layer at the nanowire surface even at high phosphor concentration. The electrical characterization was made by four-point resistance and gate depended conductance measurements. The resistivity of nanowires grown at the lowest gas flow ratio ([P:Si] = $2 \cdot 10^{-5}$) is almost equal to that of nominally undoped nanowires. An increase of the gas flow ratio ([P:Si] = $7 \cdot 10^{-5}$) results in a steep decline of the resistivity. A further increase of the [P:Si] ratio ([P:Si] = $2 \cdot 10^{-4}$) leads to a much slower decrease of the resistivity. The gate dependent conductivity measurements show that the silicon nanowires have a p-type background up to a [P:Si] ratio of $2 \cdot 10^{-5}$ (see figure 2.16). With a

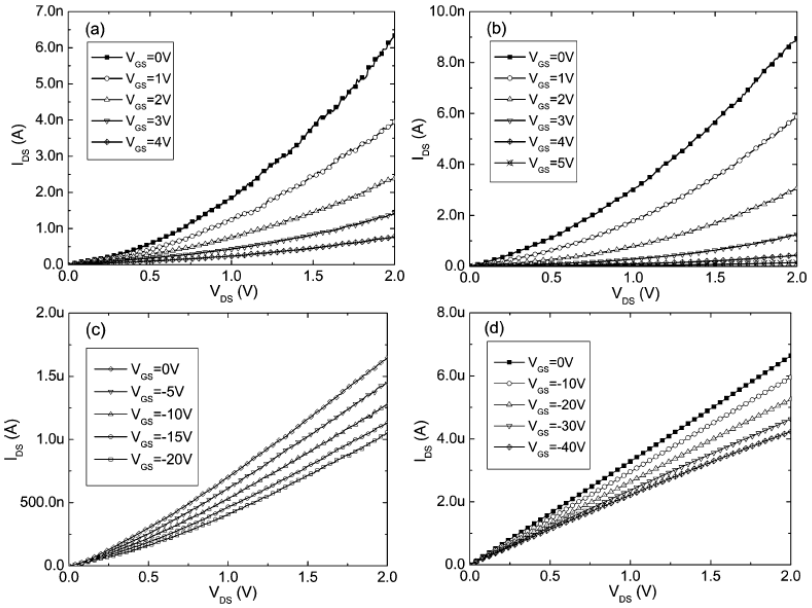


Figure 2.16: *(after Wang et al., [50]) Gate-dependent I-V characteristics of silicon nanowires grown with a [P:Si] ratio of (a) 0, (b)* $2 \cdot 10^{-5}$*, (c)* $7 \cdot 10^{-5}$*, (d)* $2 \cdot 10^{-4}$*. The topmost curves are measured under* $V_{GS} = 0V$*.*

sufficient high amount of phosphine ($7 \cdot 10^{-5}$) the nanowires convert form p- to n-type, which explains the large decrease of the resistivity of this sample.

Unfortunately it is impossible to exactly determine the electrically active p- and n-carrier concentration from the resistivity values because the carrier mobility of silicon nanowires is lower than that of bulk silicon [51]. The low mobility of silicon nanowires is expected due to electrically active defects and excess scattering at the nanowire/oxide interface [52, 53]. Only very high doped nanowires ($10^{20} cm^{-3}$) have a mobility comparable to bulk silicon [15].

2.4.2 Diffusion doping

Doping of silicon through p- or n-type impurities is easy to apply via a diffusion process. The dopant source is placed on a silicon wafer and then heated

up, doing this the dopant-atoms diffuse into the silicon. The doping concentration and the diffusion length depend on process parameters particularly temperature and duration. With low impurity concentrations and limited temperature range, the diffusion coefficient D(T) (unity: cm^2/s) is described by [29]:

$$D(T) = D_0 \cdot e^{-\Delta E/kT} \tag{2.7}$$

with the diffusion constant D_0 (extrapolated to infinite temperature) and the activation energy of the diffusion ΔE. The maximum concentration of an impurity that can be accommodated in a solid as function of the temperature is described by the solid solubility. The diffusion length L_D depends on the diffusion coefficient D(T) and the process duration τ [29]:

$$L_D = \sqrt{D(T) \cdot \tau} \quad . \tag{2.8}$$

The Diffusion of foreign atoms can be classified into three groups (see figure 2.17) [54]:

- Diffusion on mainly interstitial dissolved elements (H, Cu, Ni, Fe) has the highest diffusivites.
- Hybrid elements (Pt, Au, Zn, S) diffuse via an interstitial-substitutional exchange, named as the kick-out and dissociative mechanisms. The elements move by a interstitial mechanism, as far as they finally displace a lattice atom.
- Elements which are mainly dissolved on substitutional sites are the p-dopants boron (B), aluminum (Al) and the n-dopants phosphorus (P) and arsenic (As).

The last diffusion type occurs via native point defects approaching the substitutional dopant-atoms and subsequent formation of mobile dopant-defect pairs or mobile interstitial foreign-atoms. The dopant diffusion coefficient

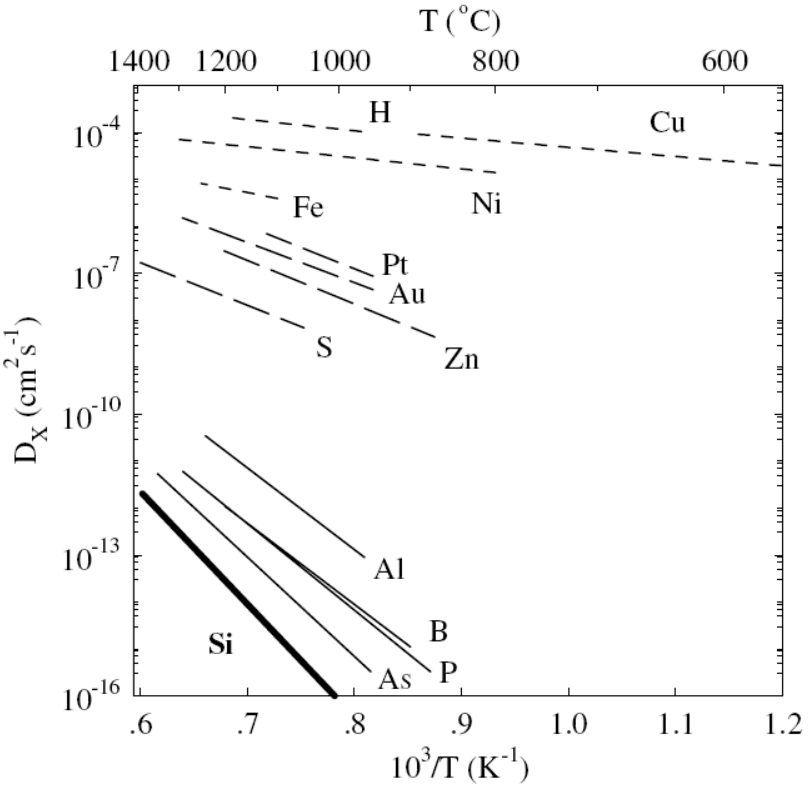


Figure 2.17: *(after Bracht, [54]) Temperature dependence of the diffusion coefficient of foreign atoms in silicon compared with self diffusion (thick solid line). The solid lines illustrate elements that are mainly dissolved on substitutional lattice sites. The long-dashed lines show hybrid elements which are mainly dissolved on substitutional sites but diffuse in an interstitial configuration via the kick-out and dissociative mechanisms. The short-dashed lines indicate diffusion on mainly interstitial dissolved elements. The data curves are representative for diffusion under electronically intrinsic conditions and thermal equilibrium of native point defects.*

under intrinsic conditions reflects the sum of different contributions which arise from the various mechanisms contributing to dopant diffusion. The relative significance of each contribution to the total diffusion coefficient can change with the doping level. Because of this doping level dependency of D(T) the knowledge of the initial and boundary conditions is important for a well directed diffusion process. Doping via diffusion is well explored in the conventional silicon process technology and therefore many concentration

profiles and simulation models for various dopants in silicon exist.

2.4.2.1 Spin-On-Dopant

One ex-situ doping method mainly used for silicon wafers is based on the usage of Spin-On-Dopant (SOD). SOD consists of a Spin-On-Glass (SOG) material [55] that is added with a dopant impurity (phosphorus, boron). Generally the sample is coated with the SOD liquid using a spinning technique and after a baking step a doped oxide-layer is formed. At high temperatures ($> 700\,℃$) the dopant in the oxide-layer diffuses into the substrate. Ingole et al. examined the doping of silicon nanowires using SOD in a proximity diffusion technique [56]. Instead of coating the silicon nanowires with SOD, a thin layer of SOD was deposited on a separate substrate to act as the dopant source. The nanowire sample was kept in a short distance to the dopant source during the doping process. An advantage of the proximity method is that the step of removing the SOD-layer can be omitted. Closer attention to the doping condition is necessary because the high temperature diffusion process with oxygen ambient was originally designed for the doping of silicon wafers. The problem with using this technique for nanowires is that overtiming the doping process leads to a total oxidation of thin nanowires [52].

Byon et al. performed post-growth doping of silicon nanowires using bismuth vapor in evacuated quartz tubes [57]. Bismuth powder was placed near the closed end of a quartz tube, while the substrate with the intrinsic nanowires was positioned a few inches away. The annealing was performed at $1000\,℃$ for 1 hour in a vacuum of $10^{-6} - 10^{-7}$ mbar. The bismuth source vaporized and achieved dopant diffusion into the silicon nanowires. The electrical characterization showed that the doped nanowires had the expected n-type behavior.

2.4.2.2 Doping via phosphoric acid diffusion

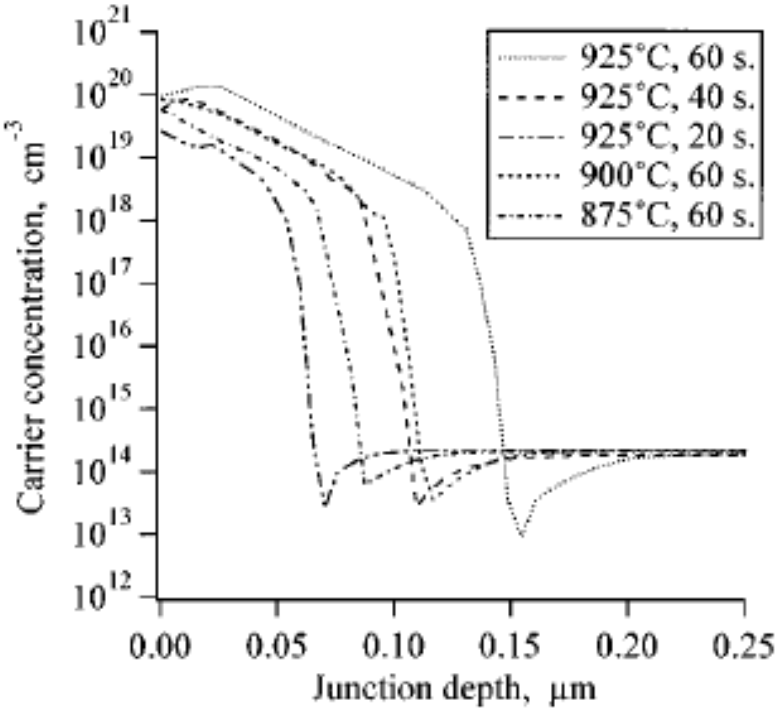


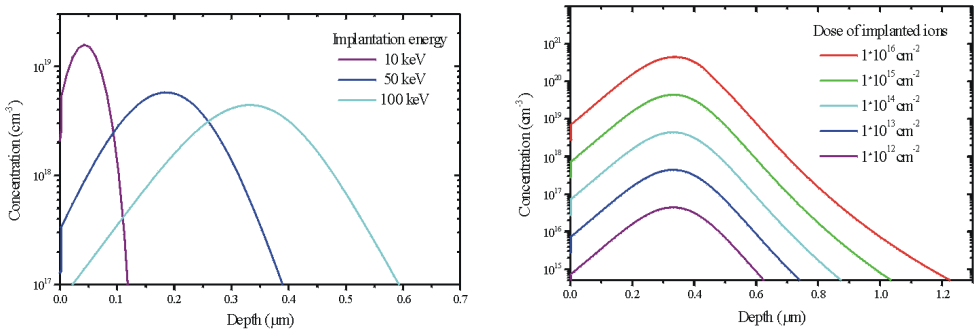
Figure 2.18: *(after Sivoththaman et al., [58]) Active carrier concentrations as a function of junction depth diffused by RTP from spin-coated H_3PO_4 films.*

Another promising doping method was performed with phosphoric acid (H_3PO_4) by Sivoththaman et al. [58]. Spin-coated phosphoric acid films were used as dopant source to form superficial junctions on a silicon wafer. The annealing was varied in temperature and time (see figure 2.18). Deeper phosphorus diffusion into the silicon was achieved by an increased temperature and/or a prolongation of time.

The utilization of phosphoric acid is promising since it is simple to handle and cost-effective. Phosphoric acid can be obtained in an adequate pure form and can be stored at room temperature. Bouhafs et al. used H_3PO_4 as a doping source in a spray process for silicon solar cells as a possible method to reduce the production costs [59].

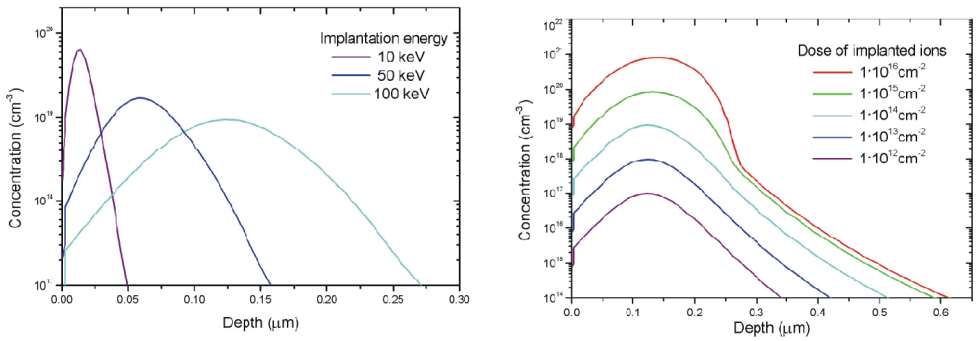
2.4.3 Ion implantation

The ion implantation gives the most precise control of an impurity profile [29]. During the ion implantation energetic charged atomic particles are accelerated and then impact the silicon substrate, the ionic particles will be slowed down through hitting the atoms of the crystal lattice. Ion implantation is a low temperature process. As the crystal lattice is destroyed after the ion bombardment an annealing step is required for recrystallization and dopant activation.



(a) Boron, ion dose = 10^{14} cm^{-2} (b) Boron, ion energy = 100 keV

Figure 2.19: *(after Ryssel, [60]) (a) Energy and (b) dose dependence of depths profiles for boron implantation in silicon.*



(a) Phosphorus, ion dose = 10^{14} cm^{-2} (b) Phosphorus, ion energy = 100 keV

Figure 2.20: *(after Ryssel, [60]) (a) Energy and (b) dose dependence of depths profiles for phosphorus implantation in silicon.*

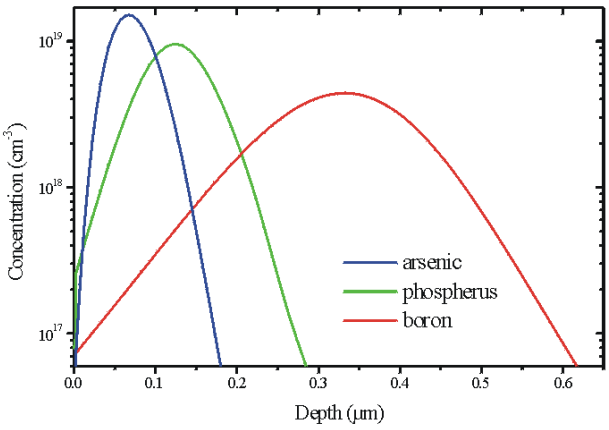


Figure 2.21: *(after Ryssel, [60]) Projected range of As, P, B at the same implantation energy of 100 keV.*

Ion implantation allows a precise control of the desired penetration depth (ion energy) and the doping concentration (ion dose). Typical ion energies are between $10-400\ keV$ with typical ion doses from $10^{11}-10^{16}\ ions/cm^2$. The larger the energy of the ions the deeper is the penetration into the target (see figure 2.19(a) for boron and figure 2.20(a) for phosphorus). A higher ion dose results in a higher doping concentration around the chosen penetration depth (see figure 2.19(b) for boron and figure 2.20(b) for phosphorus). Important for the calculation of the required ion energy is the fact that heavier ions have a shorter penetration range at the same ion energy than lighter ones (see figure 2.21).

Doping of silicon nanowires via ion implantation was successfully achieved several times by now. Hayden et al. reported partially doping of silicon nanowires via ion implantation to form the source/drain contacts [61]. Cohen et al. doped a silicon overlayer deposited over a silicon nanowire via ion implantation to shape heavily doped source and drain contacts [62]. Colli et al. showed ion implantation of thin silicon nanowires with diameters from 10 - 20 nm [63]. Their investigations reveal that the crystalline structure of the bombarded silicon nanowires can be fully recovered by thermal annealing at 800 °C for 30 minutes.

Chapter 3

Experimental setup

3.1 Overview

This chapter describes the synthesis process of silicon nanowires, their post-growth doping and the measurements of the electrical properties of such nanowires. The first section deals with the synthesis process of silicon nanowires in a hot wall low pressure chemical vapor deposition (LPCVD) setup. Special attention was paid to the sample preparation and the influence of the surface pretreatment for the VLS growth of epitaxial silicon nanowires. The second section explains the contact formation via electron beam lithography, metal deposition and lift-off techniques. The three performed doping methods for silicon nanowires, which are the SOD diffusion process, vapor phase doping, and ion implantation were described in the third section. The two different setups of the electrical nanowire measurements conclude this chapter.

3.2 Synthesis of silicon nanowires

3.2.1 LPCVD-VLS growth process

The synthesis of silicon nanowires was performed in a hot wall LPCVD setup (see figure 3.1). The temperature controlled oven has a temperature maximum of 1000℃. The CVD process uses silane (SiH_4) as precursor which decomposes to provide the semiconductor reactant to the gold (Au) catalyst. Each process the gas flow was controlled by a mass flow controller (MFC). The sample was placed into the quartz tube, therefore the lock gate can be opened and closed via a screw cap. The lock gate acts as seal and gas inlet. Further the lock gate allows the venting of the quartz tube with air. The system pressure was controlled manually by a throttle valve and an oil free piston pump. Finally the gas passes through an absorber in order to get rid of harmful precursor gases. Before the gas leaves through the exhaust it is cleaned by an absorber.

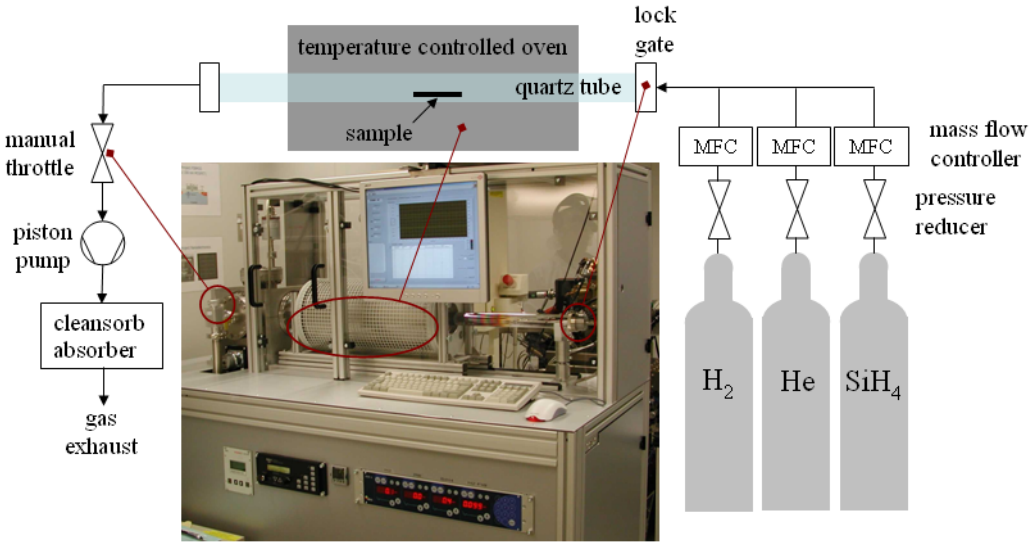


Figure 3.1: *Schematic and image of the LPCVD setup.*

The VLS growth of silicon nanowires was performed with a precursor gas flow of 100 sccm diluted silane (2% SiH_4 and 98% He) and an additional gas flow of 10 sccm hydrogen (H_2) as carrier gas. The use of hydrogen (H_2) as carrier gas lessens the radial growth of the nanowire by terminating the silicon surface [26]. The nanowires were grown at temperatures of 500 °C. Silicon nanowires were grown at a total pressure of 3, 15, or 60 mbar.

3.2.2 Sample preparation

3.2.2.1 Sample cleaning and native oxide removal

The epitaxial silicon nanowires were mainly grown on silicon substrates with a ⟨111⟩ orientation. First the wafer was cleaved into pieces of 1x1 cm^2. The samples were cleaned with acetone and isopropanol to remove the organic contaminations. Afterwards they were blown dry with ultrahigh purity nitrogen. As the silicon has a native oxide layer it is important for epitaxial growth to completely remove the oxide before growth. Since the native oxide layer is thin (2-3 nm) a short dip into buffered hydrofluoric acid (BHF; 7:1)[1] for about 5 seconds was performed. After the BHF dip the sample was rinsed with deionized water to achieve a hydrogen-terminated hydrophobic surface.

3.2.2.2 Catalyst deposition

The next step was the deposition of a thin gold layer which served as the catalyst during the nanowire growth. The gold layer was sputter-deposited with a thickness of 1-2 nm. The sample was heated up to 500 °C to get seed droplets for nanowire growth. This method leaded to a formation of droplets with a broad size distribution.

An alternative catalyst deposition method is the usage of gold colloids.

[1] The etch rate of BHF for silicon oxide is about 1 nm/s [64].

Therefore the colloids were put in a solution (distilled water, isopropanol) and dripped on the sample. The nominal size of the colloids is given (e.g. 10, 20, or 80 nm), which makes it easier to control the size of the starting nanocluster.

3.2.3 Sample treatment for epitaxial growth

Silicon diffuses through the gold film and causes the formation of a thin oxide coating over the gold layer even at room temperature [65]. The oxide layer influences the nucleation and growth of the nanowires. For this reason the influence of the surface pretreatment for vapor-liquid-solid growth of epitaxial silicon nanowires with gold catalyst and silane precursor on Si(111) substrates was examined [66].

A piece of Si(111) was cleaned and degreased with acetone and isopropanol, and blown dry with ultrahigh purity nitrogen. Next, one half of the sample was dipped into buffered hydrofluoric acid (BHF; 7:1) to resolve any native oxide followed by a water rinse to guarantee a hydrogen-terminated surface. Subsequently a 2 nm thick Au film was sputter-deposited onto the whole sample as a catalyst for VLS nanowire growth. Immediately before the sample was introduced into the low pressure chemical vapor deposition (LPCVD) system for nanowire growth the Au-coated substrate was dipped again in BHF in a manner that finally ended up with a sample divided into four parts. One-quarter of the sample was treated with BHF prior and after Au deposition, another one only previous to the Au deposition, the third partition was treated with BHF only after the Au deposition and the last partition remained untreated at all and simply covered with the 2 nm thick Au layer. Thus four different sample pretreatment procedures could be studied within a single nanowire synthesis process running through identical growth conditions. The Si(111) sample treated this way was then instantly introduced into the LPCVD system. Growth was performed for 60 min at 773 K using a precursor gas flow of 100 sccm (2% SiH_4 diluted in He) and 10 sccm

H_2 at a total pressure of 3 mbar.

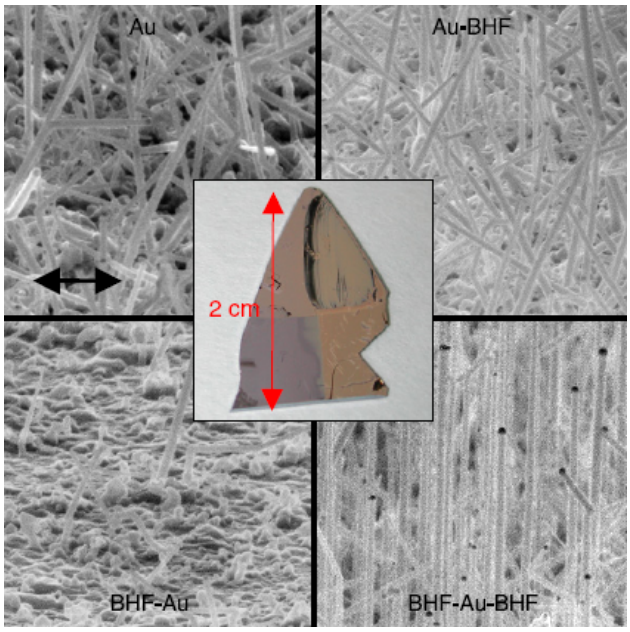


Figure 3.2: *(after Lugstein et al., [66]) SEM images (scale bar: 1μm, incidence angle: 75°) of the four sample regions with different surface pretreatments for the VLS growth of silicon nanowires on a Si(111) substrate; upper left image: region was never dipped into BHF, upper right image: region was dipped into BHF after gold deposition, lower left image: region was dipped into BHF before gold deposition, lower right image: region was dipped into BHF before and after gold deposition (the only region with epitaxially grown nanowires along the* ⟨111⟩ *directions); inset: photography of the sample.*

The optical image of an Si sample thus treated after nanowire growth, shown in the central inset of figure 3.2, reveal four apparently different nanowire growth regimes. Obviously the proper surface preparation is crucial for well-controlled nanowire growth, as can be seen in the respective scanning electron microscopy (SEM) images in figure 3.2.

The upper left SEM image in figure 3.2 confirms that this division of the sample, never treated with BHF, is sparsely covered by randomly oriented nanowires. The diameter and length of the nanowires varies over a wide range from 40 to 200 nm and 700 nm to 3 μm, respectively. The rusty color

in the optical image is mainly due to the roughening of the surface as a result of Si deposition induced by the thin Au film covering the whole surface. This proves that under the given experimental conditions even the very thin native oxide layer is detrimental to epitaxial nanowire growth.

Surprisingly the lower left SEM image, representing the part of the sample which was dipped into BHF immediately before sputtering the catalytic Au layer, shows even less nanowires. As re-oxidation of H-terminated Si surfaces is moderately slow [67] and the time between the BHF dip and the subsequent Au deposition was less than 5 min no new native oxide layer should be formed. Therefore it is supposed that Si from the substrate diffuses through the thin Au layer and undergoes oxidation even at room temperature, thereby forming an SiO_2 layer atop of the catalytic gold layer [65, 68]. Experimental verification of the migration of silicon through noble metal films, resulting in the formation of an oxide layer, was first reported in the early 1970's in the context of Schottky contacts between gold and silicon [69, 70]. It is supposed that such a thin oxide "overlayer" blocks the diffusion path of the precursor gas to the catalytic particle and thereby nanowire growth. The appearance of some isolated nanowires can be justified by cracks and discontinuities in the poor quality oxide overlayer. For separately accomplished nanowire growth experiments on substrates with a thick thermal oxide layer, or even on glass substrates, far better nanowire growth yields than on Si samples with a native oxide layer were observed. It is supposed that, due to the poor quality of the native oxide layer, there is also some diffusion of Si via cracks and discontinuities into the gold layer. Further this Si will again lead to the formation of a thin oxide layer atop of the Au catalyst, hindering effective nanowire nucleation and growth.

The removal of this oxide layer favors nanowire growth as shown in the upper right SEM image in figure 3.2. This part of the sample was treated with BHF after Au film deposition. Thus, it is supposed that the oxide layer formed atop of the Au film may be removed by the post-gold deposition BHF treatment. Remarkably the nanowires densely cover the whole substrate and

the morphology can be regarded as equivalent to the one achieved on the sample never treated with BHF.

Finally the lower right SEM image shows the part of the sample that was dipped into BHF both prior to and after Au deposition. This part of the sample can be regarded as oxide-free, and epitaxial growth of single-crystalline silicon nanowires along the $\langle 111 \rangle$ directions was obtained. It was also noticed that for samples treated in this manner and stored for a few days prior to the nanowire growth, the yield of epitaxial NW synthesis remained quite good. This indicates that exposure of the two times BHF-etched surface to air does not restore the oxide layer. The wires on this part of the sample that appear ocher in the optical image are longer, show less kinks and the dispersion of the diameters becomes significantly narrower with an average diameter of about 90 nm.

These results demonstrate that epitaxial growth of silicon nanowires with high densities is only possible if the native oxide layer on the silicon substrate and the oxide coating of the gold layer is removed before the VLS growth process is started.

3.3 Contact formation to silicon nanowires

Electron beam lithography allows a direct transfer of computer designed structures to a resist. In doing so the radiation-sensitive resist film is exposed by an electron beam. The pattern transfer occurs only via control of the electron beam without use of an additional mask layer. This technique is called maskless pattern transfer.

The formation of the contacts for silicon nanowire samples was done via the electron beam lithography system from Raith Inc. called e-Line. Contacting the nanowires is a necessary step to enable the characterization of their electrical properties. The silicon nanowires were placed on a Si wafer with a 200 nm SiO_2 layer. The isolating sample had pre-defined gold patterns (generated using a standard optical lithography process) serving as orientation points during the electron beam lithography process (see figure 3.3, a).

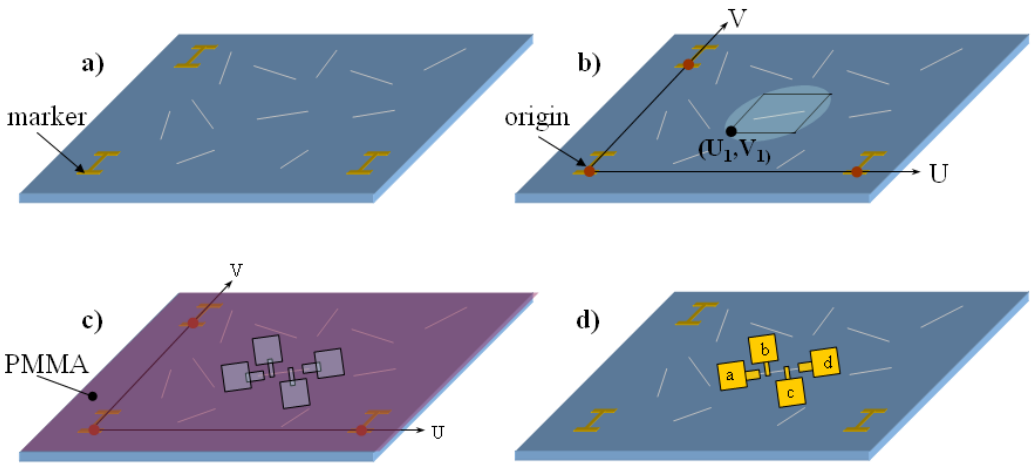


Figure 3.3: *Schematic illustration of the contacting of a single nanowire using electron beam lithography. a) Dispersion of nanowires on a isolating sample with pre-defined alignment markers. b) Adjusting of the eline U,V-coordinate system and marking of a nanowire via SEM image [U_1, V_1]. c) PMMA exposure. d) Nanowire sample after metalization and lift-off.*

After putting the sample into the e-Line system, the local coordinate system on the sample had to be adjusted. Therefore three distinctive points had to be set up to define fixed coordinates on the sample. Next, a set of desired nanowires was marked. The local coordinates were assigned to each SEM image (see figure 3.3, b). Using these SEM images the contact areas were drafted with the according e-Line software. The sample was then locked out of the e-Line system. The electron beam resist was deposited via a spinning technique on the nanowire sample. The used resist was Polymethylmethacrylate (PMMA, AR-P 679.04 from Allresist Inc.). At a spinning speed of 4000 rpm for duration of 40 seconds an approximately 400 nm thick PMMA layer was formed. Finally the sample was backed at 170 ℃ for 30 minutes to get rid of the dissolver.

After the sample had been reloaded into the e-Line system the coordinate system had to be realigned using the pre-designed markers. By the time the U,V-coordinates had been well arranged the electron beam exposure process was started (see figure 3.3, c). When the process had been completed the exposed sample was locked out and emerged in a developer (AR-P 600-56 from Allresist Inc.) for a duration of 30 seconds and subsequently put into a stopper liquid (AR-P 600-60 from Allresist Inc.) for 30 seconds. A metal film was sputter-deposited onto the sample ($\sim$ 3 nm Ti, $\sim$ 60 nm Au). Afterwards the sample was immersed into a remover liquid (AR-P 600-70 from Allresist Inc.). Now the PMMA layer had been eliminated and the metal film remained only on the exposed regions of the sample surface (see figure 3.3, d). The nanowires could then be measured using probe needles for electrical characterization.

3.4 Doping of VLS grown silicon nanowires

3.4.1 Silicon nanowire doping with SOD

Spin-On-Dopant (SOD) is used as dopant source for n-type doping (phosphorus) or p-type doping (boron). All nanowire doping was performed with a boron SOD source (Honeywell B-150). Since for electrical characterization all the nanowires were contacted via electron beam lithography, the nanowires had to be placed on an oxide layer in a horizontal position. Thus the grown nanowire sample was placed into a tubule with isopropanol, and was then treated via ultrasonic to separate the nanowires from the substrate. Subsequently a drop of the solution was applied on a silicon substrate with a 200 nm thick oxide overlayer.

First the SOD was applied with a spinning technique on the nanowire sample (5000 rpm, 40 seconds). Afterwards the sample was placed into a tube furnace and heated to a temperature of 950 °C for different durations (3, 5, and 10 minutes). The second experimental series was carried out at different temperatures (850 °C, 900 °C, and 950 °C) and all for the same duration of 10 minutes. After the SOD diffusion process the top coating of the SOD-layer was etched with buffered hydrofluoric acid (BHF; 7:1) to uncover the nanowires. Unfortunately it was impossible to etch the whole

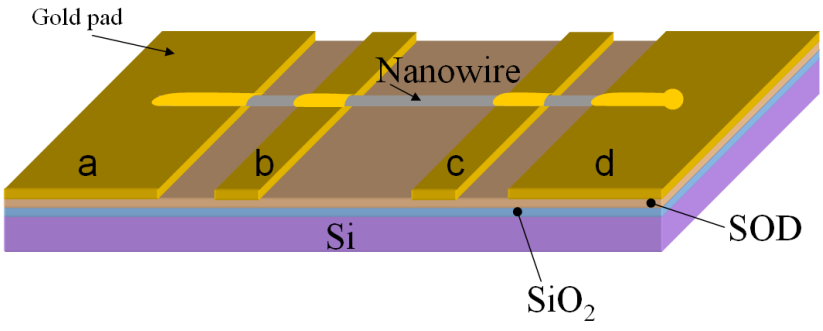


Figure 3.4: *Schematic illustration of the contact formation of a SOD-doped nanowire using electron beam lithography, metal deposition and lift-off technique.*

SOD-layer, as all the nanowires would have been removed together with the SOD coating. The remaining SOD-layer acted as a stabilizer for the nanowires. Electrical measurements on a baked SOD-layer were done, which showed insulating behavior. Consequently no influence was noticed due to the remaining SOD-layer during the electrical measurements. Finally the boron-doped nanowires could be contacted via electron beam lithography, metal deposition and lift-off technique (see figure 3.4).

3.4.2 Silicon nanowire doping via thermal evaporation

The use of phosphoric acid (H_3PO_4) as a dopant source is a simple and effective method for n-type doping of silicon nanowires. At first the dopant source had to be prepared in order to set up the diffusion process. Therefore a drop of phosphoric acid was deposited on a silicon substrate. Then the H_3PO_4 drop was uniformly dispersed across the surface. That was followed by the pre-baking of the substrate on a hotplate at 250 °C for 90 minutes. Next the surface was rinsed with deionized water to eliminate the not yet hardened H_3PO_4. The liquid parts of H_3PO_4 were thereby directly removed since liquid phosphoric acid is water-soluble.

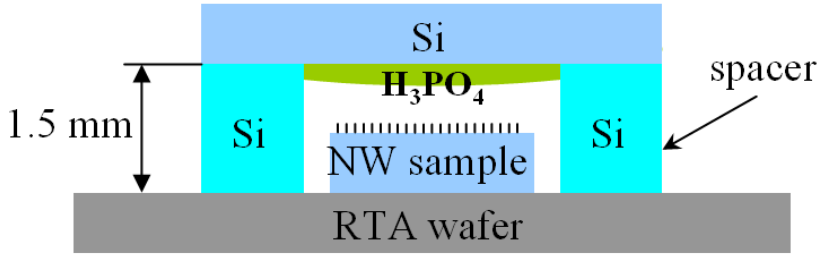


Figure 3.5: *Experimental setup for doping of silicon nanowires with a phosphorus source (H_3PO_4).*

The setup of the phosphorus doping process for silicon nanowires is shown in figure 3.5. A spacer separates the phosphorus dopant source from the

silicon nanowire sample. The nanowire sample was placed on the wafer of the RTA oven. The doping process was performed at a temperature of 900 ℃ for a duration of 4 minutes in an argon (Ar) atmosphere. After this working cycle had been finished the n-doped nanowires were separated from the substrate via ultrasonic treatment. Then the silicon nanowires were deposited on a silicone substrate with a 200 nm thick silicon oxide overlayer. The contacting of the nanowire for the electrical characterization was done again via electron beam lithography, metal deposition and lift-off technique.

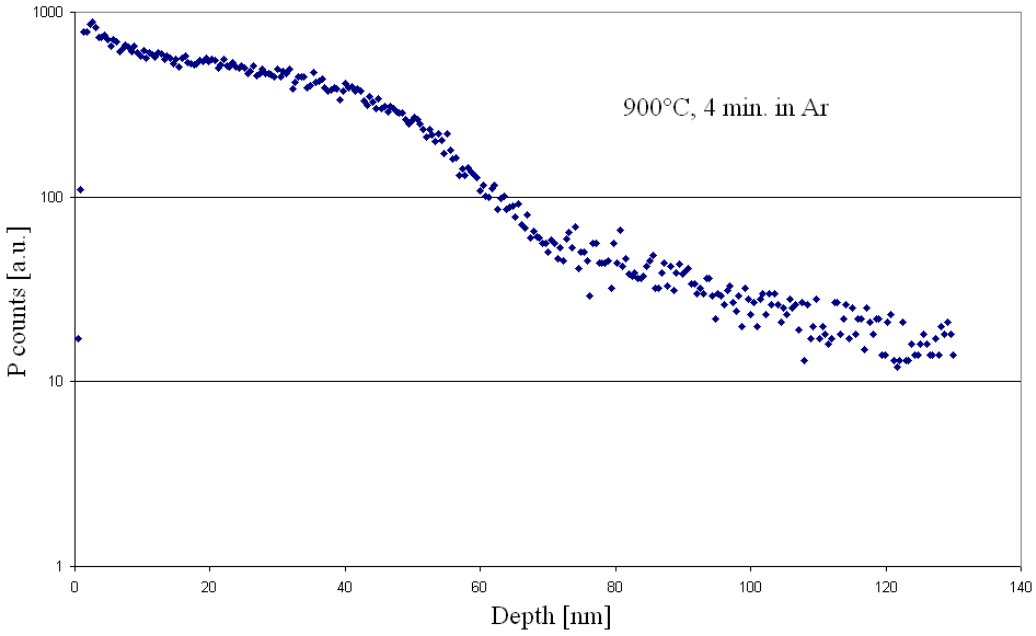


Figure 3.6: *SIMS profile of a phosphorus doped silicon substrate (diffusion parameters: T = 900 ℃, 4 minutes in Ar gas, doping source: H_3PO_4.*

An examination of the phosphorus doping profile in silicon was done using secondary ion mass spectroscopy (SIMS). Therefore the doping setup was repeated with an intrinsic silicon sample, using the same process parameters (900 ℃, 4 min. in Ar). SIMS was used for analyzing the composition of solid surfaces. The SIMS measurements of the doped substrate (see figure 3.6) reveal a high concentration of counted phosphorus clusters in a layer of about 60 nm. Below 100 nm the phosphorus concentration is very low approach-

ing the detection limit of the SIMS. Based on this results we propose that phosphoric acid doping is an adequate method for silicon nanowires up to diameters of 120 nm.

3.4.3 Ion implantation

For doping via ion implantation the grown nanowires were placed again in a horizontal position on an isolating layer (200 nm SiO_2). With regards to the required annealing step at high temperatures a sample without predefined gold patterns was chosen. To achieve markers for the lithography step, marker lines were scratched with a cleaver.

The ion implantation of the silicon nanowires was done at an ion energy of 30 keV and an ion dose of $4 \cdot 10^{13}\, cm^{-2}$. After the implantation the nanowires were annealed at 850 ℃ for 15 minutes in helium atmosphere (70 sccm He). Finally the contact structuring of the nanowires was made again via electron beam lithography, metal deposition and lift-off technique.

3.5 Electrical characterization of nanowires

The electrical characterization of the nanowires was done with a needle prober (Analytical Probe System PSM6, Karl Süss MicroTec AG), where both the four point probe and the field effect measurements were done. The probe needles are movable by set screws, allowing an exact positioning to the metal contact pads of the nanowires. The electrical signals were evaluated via a precision semiconductor parameter analyzer (Agilent/HP 4156B).

3.5.1 Four-point probe measurement

To eliminate the influence of the metal semiconductor junction the determination of the nanowire resistance was done via four point probe measurement. The setup of the analyzer was adjusted to keep the current flow at the inner probes (b,c) at zero. A voltage sweep was set up at the outer probes (a,d). With this setup the contact resistance is negligible. The resistance of the nanowire segment between the inner electrodes is consistent with the ratio of voltage drop between the inner electrodes and the current flow through the nanowire (see figure 3.7, a).

3.5.2 Nanowire based FET with back-gated configuration

To perform a field effect measurement it was necessary to contact the back side of the nanowire sample with a copper plate via a silver conductive paste. The copper plate was connected to the high doped substrate of the sample and then the gate voltage was applied to this copper plate. Due to the high doping of the substrate the whole back side of the sample acted as the gate electrode. The substrate had an oxide overgrowth layer of 200 nm, which formed the gate dielectric and the metal electrodes on the nanowire were the

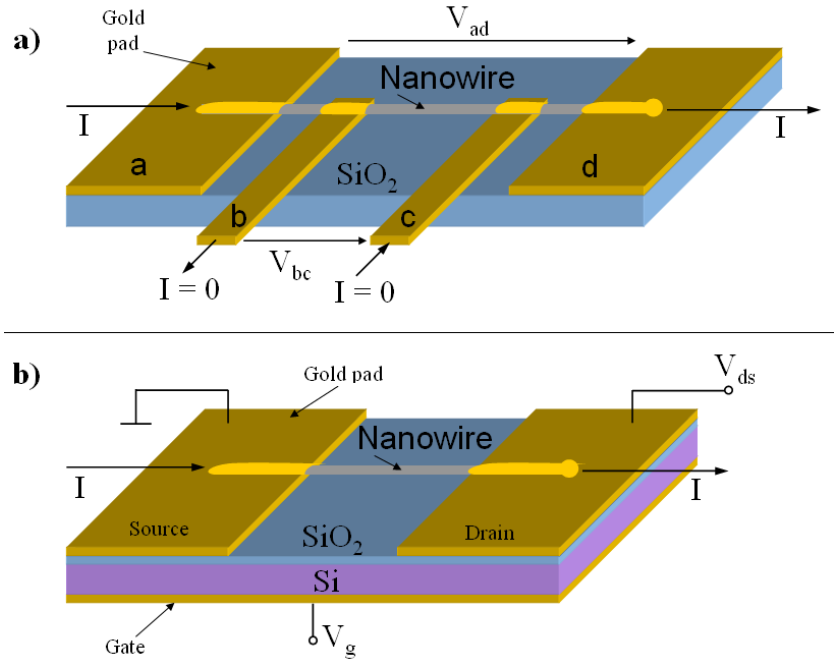


Figure 3.7: *a) Four-point probe measurement setup. b) Nanowire field effect measurement in back-gated configuration.*

source/drain contacts. The active channel was shaped by the nanowire itself (see figure 3.7, b).

Two different measurements were performed. First a constant voltage was applied at the source/drain contacts and the gate voltage was sweeped. As result a gate-dependent change of the current flow with a specific turn-off voltage could be observed (**transfer characteristic**). Second the source/drain voltage was sweeped at a constant gate voltage to obtain the **output characteristic** of the nanowire FET.

Chapter 4

Results and discussion

4.1 Overview

This chapter treats the results of the observations and measurements about intrinsic and doped silicon nanowires grown via VLS mechanism. At the beginning the influence of the total growth pressure to the nanowire growth direction and orientation is examined using SEM images and TEM analysis. Afterwards the results of the electrical measurements of these nanowires are demonstrated. The last section discusses the results of three different forms of silicon nanowire doping: ion implantation, phosphoric acid, and ion implantation.

4.2 Pressure influence of VLS grown silicon nanowires

4.2.1 Growth orientation analysis

Silicon nanowire samples were grown via LPCVD at three different settings of total growth pressure (3, 15, 60 mbar). Analysis of the growth orientation was performed with SEM and TEM.

4.2.1.1 Nanowire growth at a total pressure of 3 mbar

Silicon nanowires were synthesized at a total pressure of 3 mbar and a temperature of 500 °C for 100 minutes on a silicon (111) substrate. The SEM image in figure 4.1 reveals an orientation mostly along the ⟨111⟩ direction. The nanowires build a network of triangular patterns and many nanowires stand perpendicular to the substrate (bright spots). The length of the nanowires ranges from 1 μm to 3 μm, with diameters from 50 nm to 200 nm.

Figure 4.2 shows the high resolution TEM observations of such silicon nanowires. The nanowire is single crystalline and no crystal defects can be detected. The junction between the nanowire and the catalyst is atomically sharp (see figure 4.2, d). The Fast Fourier Transformation (FFT) of the silicon nanowire crystal reveals two spots around the midpoint (see figure 4.2, e). These spots are parallel to the nanowire axis with a reciprocal spacing of 1/(0.314 nm), according to the separation distance of the atomic layers (0.314 nm) and identifies (111) crystal planes. A thin oxide layer covers the nanowire and the gold catalyst (see figure 4.2, b). The nanowire is coated with tiny gold particles, this is caused by the low pressure growth which provokes the surface diffusion of the gold from the catalyst (see figure 4.2, a, c).

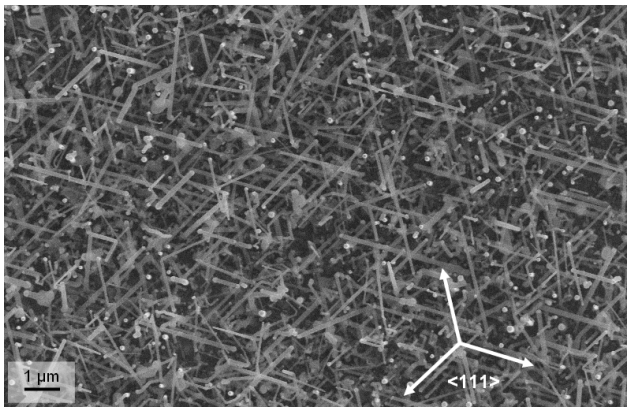


Figure 4.1: *SEM image of epitaxially silicon nanowires grown on a silicon (111) substrate at a total pressure of 3 mbar and a temperature of 500 °C for 100 minutes (top view).*

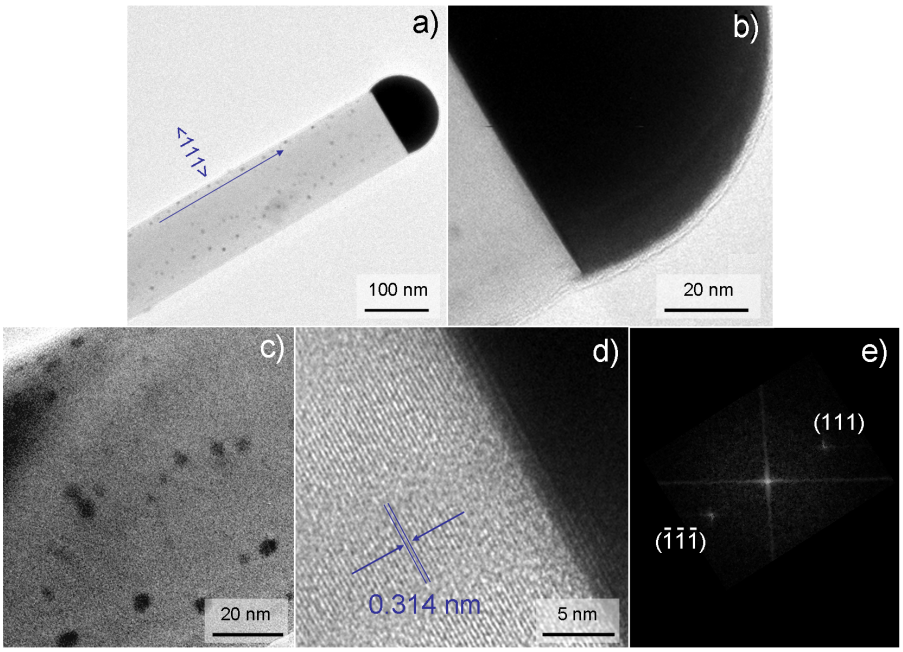


Figure 4.2: *TEM images of a silicon nanowire grown at a total pressure of 3 mbar and a temperature of 500 °C. a) Large-scale image of the Si NW. b) Coverage of the nanowire and the gold catalyst by a thin oxide layer. c) Detailed view of the nanowire sidewall showing gold particles. d) HRTEM image of he silicon/catalyst interface. e) FFT diffraction pattern of the Si NW crystal.*

4.2.1.2 Nanowire growth at a total pressure of 15 mbar

Figure 4.3 shows the top view SEM image of a sample processed at 15 mbar for 40 minutes under otherwise identical processing conditions. In contrast to the 3 mbar grown nanowires, for nanowires grown at 15 mbar no nanowire is orientated to the Si (111) substrate. The length of the nanowires varies from $2\,\mu m$ to $6\,\mu m$, which is much longer than the ones grown at 3 mbar if you take in consideration the much shorter growth duration. The higher total pressure and thereby increased SiH_4 pressure results in a larger supply of the Si source. Since the growth rate is limited by the supply of the Si source, the larger supply of Si results in a higher growth rate of roughly 250 nm/min, more than 7 times greater than that at 3 mbar (33 nm/min) [42]. The nanowire diameters range between 40 nm and 200 nm, which is more or less the same as with 3 mbar grown nanowires.

Figure 4.4 shows such silicon nanowires observed via TEM. The nanowire is crystalline without identifiable crystal defects. The separation distance of the (224) lattice plane is 0.111 nm, while the $(\bar{2}20)$ plane is separated by 0.192 nm. The [112] direction of the nanowire is parallel to the Fast Fourier Transformation (FFT) of the (224) spot. The examination of the lattice image and the FFT diffraction pattern reveals that silicon nanowires synthesized at a total pressure of 15 mbar grow along the $\langle 112 \rangle$ direction. Contrary to the silicon nanowires grown at 3 mbar, there seem to be less gold particles on the sidewalls of the examined nanowire.

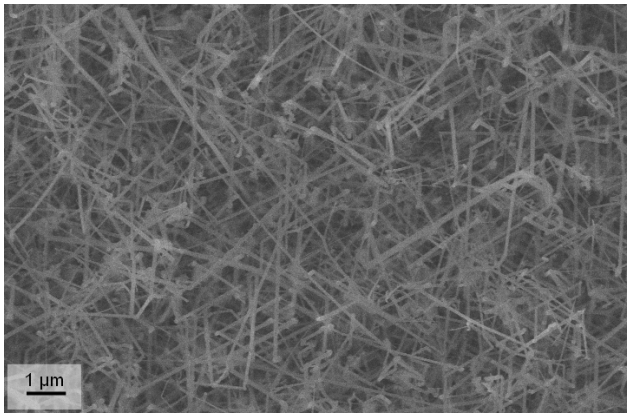


Figure 4.3: *SEM image of silicon nanowires on a silicon (111) substrate grown at a total pressure of 15 mbar and a temperature of 500 °C for 40 minutes (top view).*

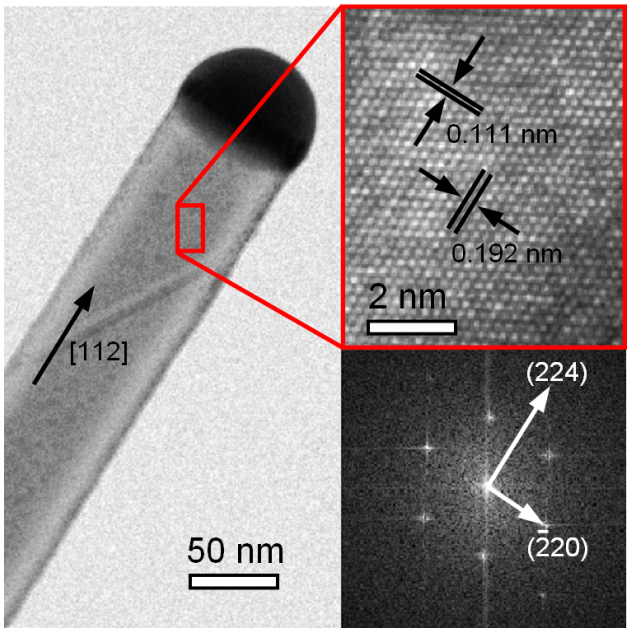


Figure 4.4: *TEM images of a silicon nanowire grown at a total pressure of 15 mbar and a temperature of 500 °C. HRTEM image of the marked area (top right image), and FFT diffraction pattern of the silicon nanowire crystal (bottom left image).*

4.2.1.3 Nanowire growth at a total pressure of 60 mbar

Finally, silicon nanowires were synthesized at a total growth pressure of 60 mbar and a temperature of 500 ℃ for 30 minutes again on a silicon (111) substrate (see figure 4.5). The nanowires seem to be grown in an unstructured manner and none of the nanowires are standing perpendicular to the substrate. Due to the high growth pressure the nanowires are very long and have smaller-sized diameters compared to the earlier examined samples. The nanowires are between 10 μm and 30 μm long, with diameters from 30 nm to 100 nm.

Figure 4.6 illustrates the TEM observations of silicon nanowires grown at a total pressure of 60 mbar and a temperature of 500 ℃. The nanowires are again crystalline without defects and only very few gold particles are on the nanowire sidewalls. The separation distance of the $(11\bar{1})$ plane is 0.314 nm, while the (224) plane is separated by 0.111 nm. The (224) lattice plane is parallel to the growth direction and attests a [112] growth direction. Silicon nanowires synthesized at a total pressure of 60 mbar grow along the $\langle 112 \rangle$ direction just like the 15 mbar nanowire sample.

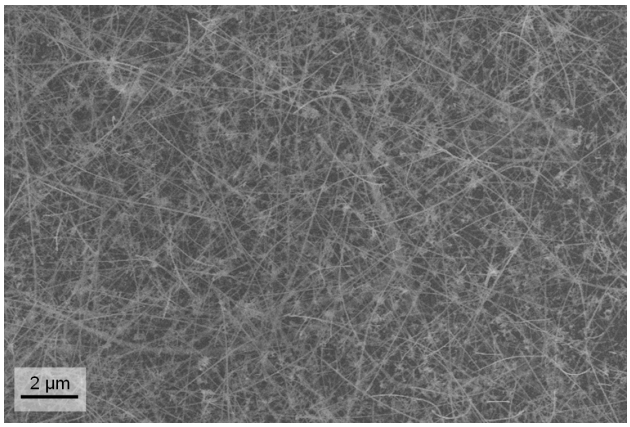


Figure 4.5: *SEM image of silicon nanowires on a silicon (111) substrate synthesized at a total pressure of 60 mbar and a temperature of 500 °C for 30 minutes (top view).*

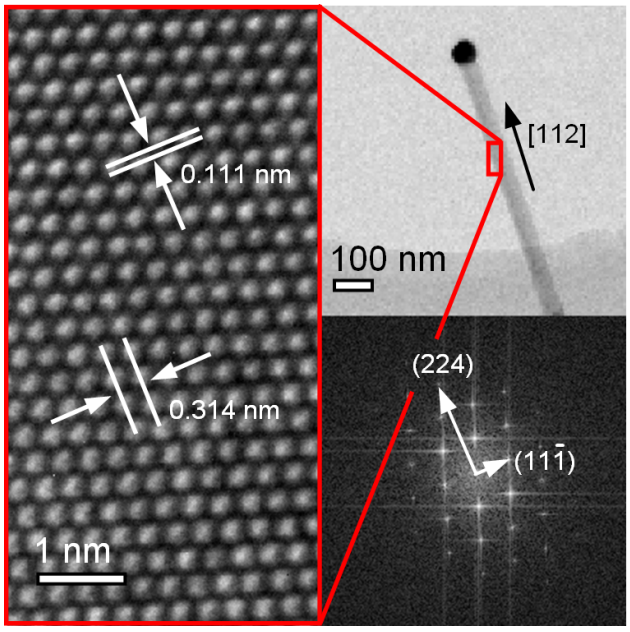


Figure 4.6: *TEM images of a silicon nanowire grown at a total pressure of 60 mbar and a temperature of 500 °C. Large-scale image of the silicon nanowire (top right image), HRTEM image of the marked area (left image), and FFT diffraction pattern of the silicon nanowire crystal (bottom left image).*

4.2.1.4 Summary

In summary a higher total pressure and the hence resulting increased silane (SiH_4) pressure cause a higher silicon supply to the catalyst and an overall faster growth of the silicon nanowire. All observed nanowires are single crystalline and show no visible defects. The gold particles on the nanowire sidewalls decrease with increasing growth pressure. The junction between the nanowire and the gold catalyst is atomically sharp at 3 mbar and becomes less distinct with increasing growth pressure. The transition from the $\langle 111 \rangle$ growth direction to the $\langle 112 \rangle$ occurs between a growth pressure of 3 mbar and 15 mbar.

4.2.2 Electrical measurements

The electrical properties of the above analyzed silicon nanowires grown at 3 mbar, 15 mbar, and 60 mbar were measured with four point configuration. The formation of the electrical contacts was performed via electron beam lithography, metal deposition and lift-off techniques. Four-point probe and field effect measurements were done using the measuring station.

4.2.2.1 Electrical characterization of nanowires grown at 3 mbar

Figure 4.7 shows the I-V curve of the four-point probe (4PP) measurement of a 3 mbar grown nanowire, the two-point probe (2PP) I-V curve measured at the outer contacts is included. The 2PP and the 4PP measurement reveal a linear behavior, which proves good contact properties. Because the inner contacts are currentless during the 4PP measurement, the contact resistance could be neglected. Hence the 4PP measurement represents only the resistance of the inner nanowire segment, whereas the contact resistance is included by the 2PP measurement. The resistance of the inner nanowire segment is defined as the reciprocal value of the 4PP linearization gradi-

ent $(2 \cdot 10^{-9})$. In this case the inner nanowire resistance is $500\,M\Omega$ with a resulting resistivity of $297.5\,\Omega cm$.

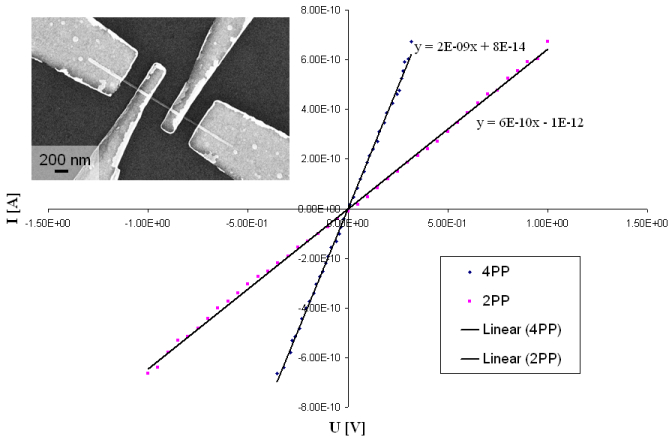


Figure 4.7: *I-V curves of a silicon nanowire grown at 3 mbar. The 4PP data points represent the resistance of the inner nanowire segment (without contact resistance). The 2PP data points represent the whole resistance between the outer contacts (including the contact resistance).*

Figure 4.8 shows the gate-dependent I-V curve of a nanowire grown at 3 mbar (transfer characteristic), with the drain/source voltage V_{ds} kept constant. The decrease of the gate voltage V_g causes an increase of the drain/source current I_{ds}, which indicates p-type behavior as expected. The drain/source current I_{ds} is not symmetrically, because the current for negative voltages of V_{ds} differs compared to positive voltages of V_{ds} at the same value. This indicates a preferred current direction, most probably caused by the metal/semiconductor interface of the contacts.

Figure 4.9 shows the I-V curve of the output characteristic of the silicon nanowire with constant gate voltages V_g. The drain/source current I_{ds} is much larger for high negative voltages of V_g than for positive voltages, which indicates the expected narrowing of the nanowire channel for higher positive voltages. The slightly unsymmetrical output voltages may occur due to different contact resistances of the source/drain connections.

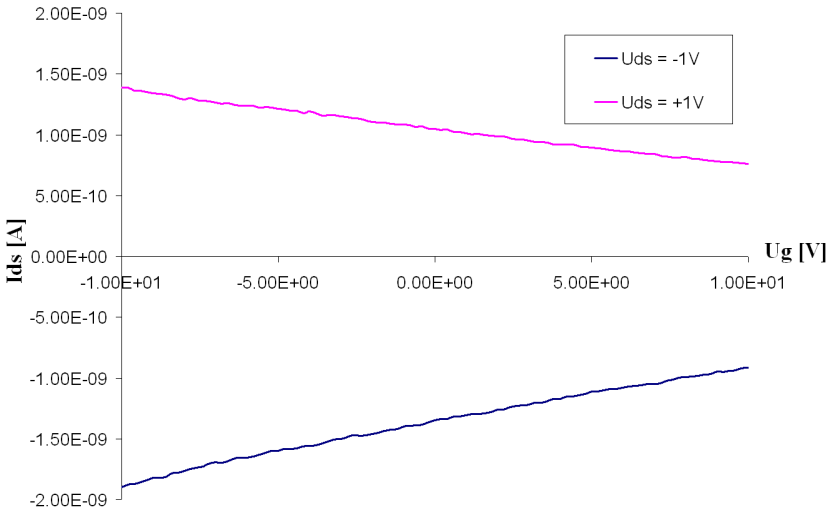


Figure 4.8: *Transfer characteristic of a silicon nanowire grown at 3 mbar in backgated FET configuration.*

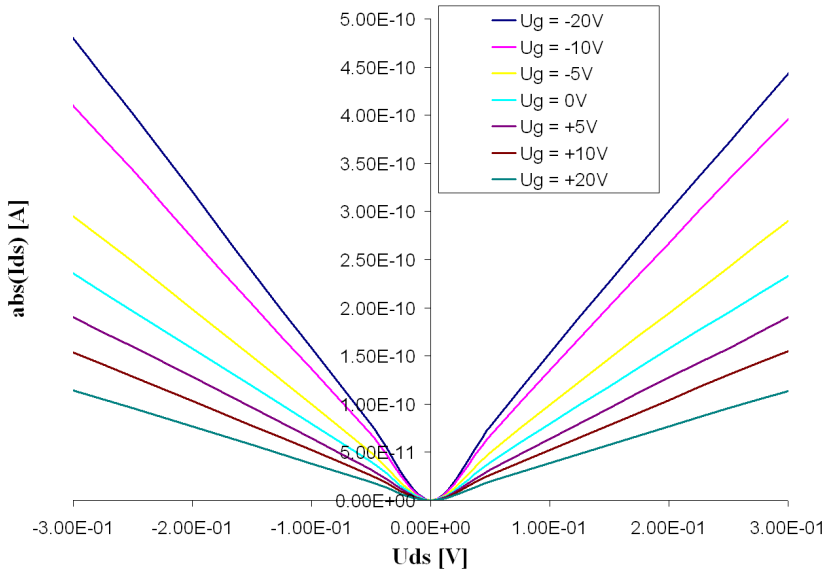


Figure 4.9: *Output characteristic of a silicon nanowire grown at 3 mbar in backgated FET configuration.*

4.2.2.2 Electrical characterization of nanowires grown at 15 mbar

Figure 4.10 illustrates the I-V curve of the four point probe (4PP) measurement of a 15 mbar grown nanowire and the two point probe (2PP) I-V curve measured at the outer contacts. Both I-V curves show a linear behavior. The resistance of the inner nanowire segment is 16.67 $G\Omega$ and the resistivity equals 4189.6 Ωcm.

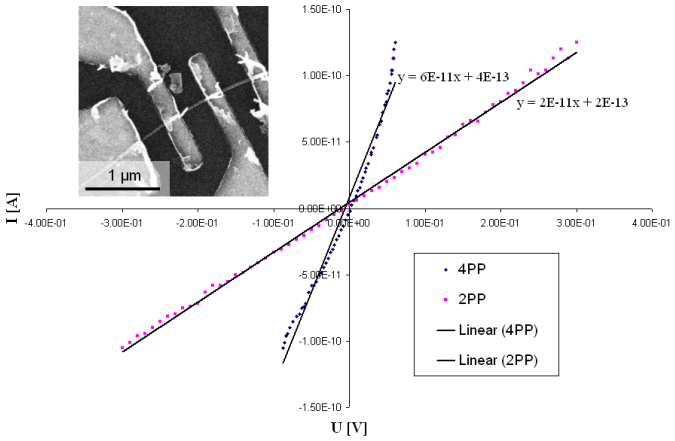


Figure 4.10: *I-V curves of a silicon nanowire grown at 15 mbar. The 4PP data points represent the resistance of the inner nanowire segment (without contact resistance). The 2PP data points represent the whole resistance between the outer contacts (including the contact resistance).*

Figure 4.11 illustrates the transfer characteristic of a nanowire grown at a total pressure of 15 mbar. Like the 3 mbar sample the drain/source current I_{ds} rises with increasing negative gate voltage V_g and decreases with positive gate voltage. The drain/source current I_{ds} here seems to be independent of the sign of the applied drain/source voltage V_{ds}.

Figure 4.12 shows the I-V curve of the output characteristic of the silicon nanowire. A dependence of the applied gate voltage V_g is given, comparable to the 3 mbar sample.

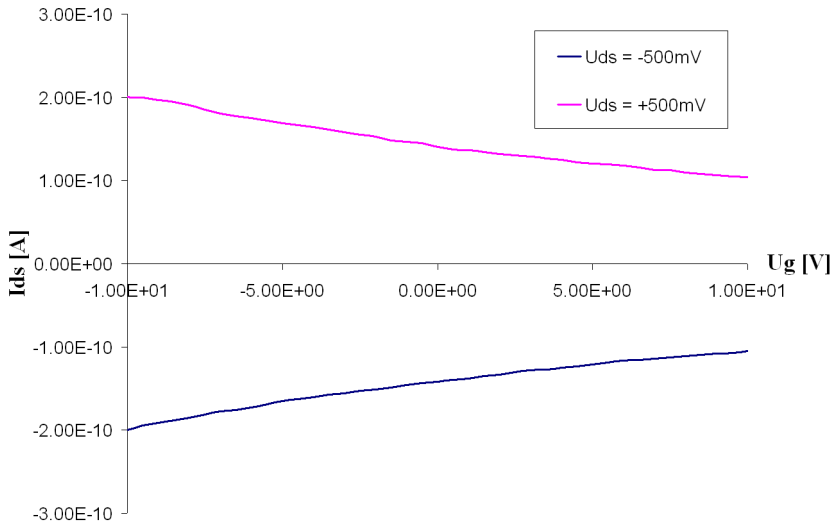


Figure 4.11: *Transfer characteristic of a silicon nanowire grown at 15 mbar in backgated FET configuration.*

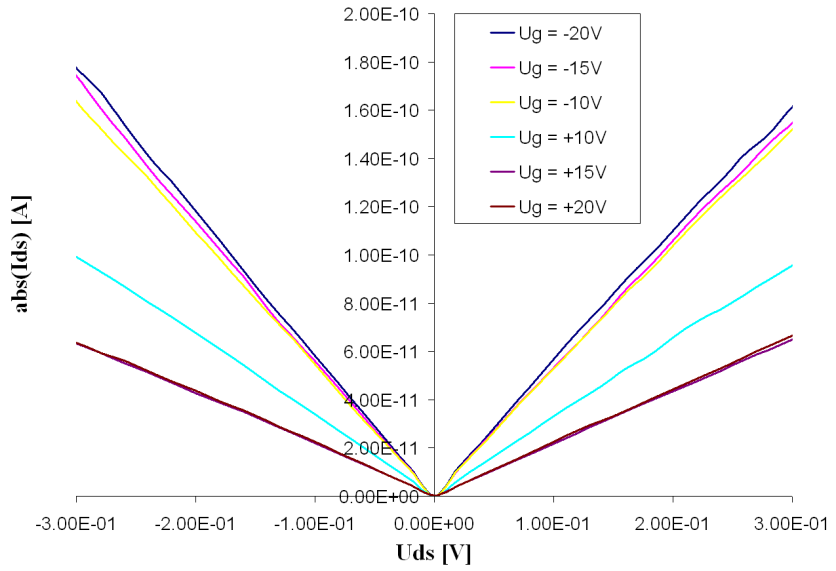


Figure 4.12: *Output characteristic of a silicon nanowire grown at 15 mbar in backgated FET configuration.*

4.2.2.3 Electrical characterization of nanowires grown at 60 mbar

Figure 4.13 represents the I-V curve of the four point probe (4PP) measurement of a 60 mbar grown nanowire and the two point probe (2PP) I-V curve measured at the outer contacts. Like the two samples before the I-V curves show a linear behavior. The inner nanowire resistance is 250 $M\Omega$, leading to a resistivity of 359.2 Ωcm.

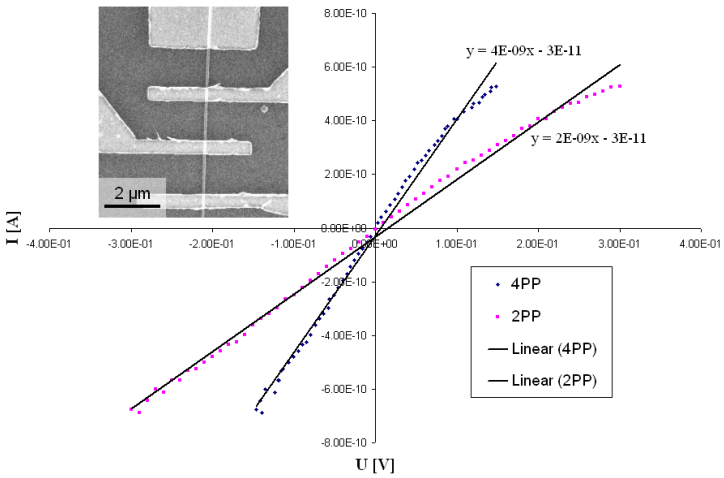


Figure 4.13: *I-V curves of a silicon nanowire grown at 60 mbar. The 4PP data points represent the resistance of the inner nanowire segment (without contact resistance). The 2PP data points represent the whole resistance between the outer contacts (including the contact resistance).*

Figure 4.14 shows the transfer characteristic of a nanowire grown at a total pressure of 60 mbar. The gate-dependency is very strong in this sample and the drain/source current I_{ds} decreases significantly at high positive gate voltages V_g. The current flow differs for the negative/positive voltages of V_{ds} indicating a preferred direction of the electric current as it was with the 3 mbar sample.

Figure 4.15 illustrates the output characteristic of the silicon nanowire. A turn-off voltage is apparent at a gate voltage of $V_g = +20$ V. In contrast to the other two samples a high turn on/off current ratio was achieved in this

sample.

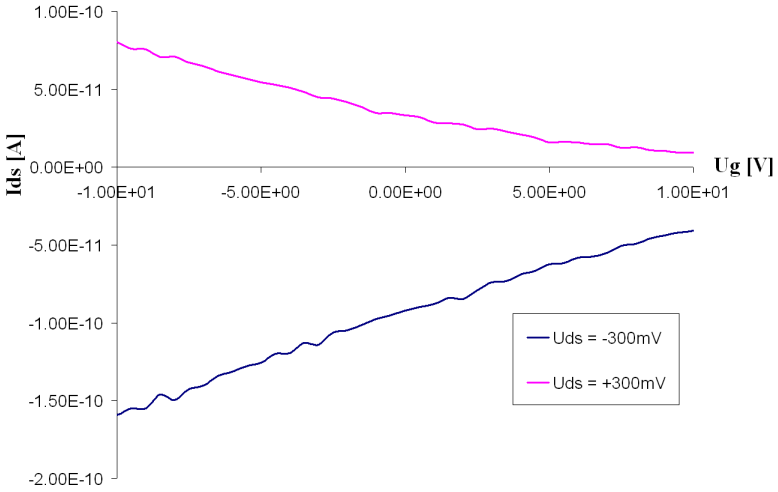


Figure 4.14: *Transfer characteristic of a silicon nanowire grown at 60 mbar in backgated FET configuration.*

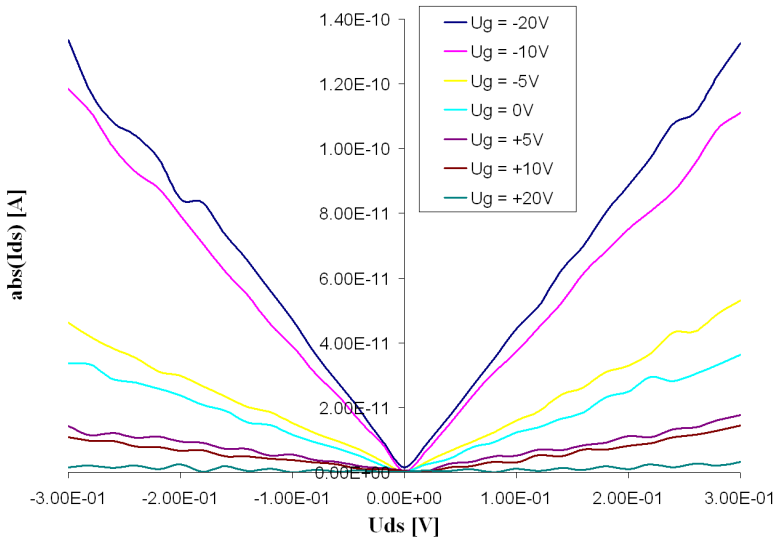


Figure 4.15: *Output characteristic of a silicon nanowire grown at 60 mbar in backgated FET configuration.*

4.2.2.4 Summary

The comparison of the resistivity values of these three different silicon nanowire types was rather astonishing. At 15 mbar the nanowires have a considerably higher resistivity value than those grown at 3 mbar and 60 mbar. Furthermore it was surprising that the nanowires grown at 3 and 60 mbar have almost the same resistivity values, although the growth pressure differs largely. The high resistivity at 15 mbar was confirmed in several other measurements.

The gate dependence of the 3 mbar and the 15 mbar samples is weak, the 60 mbar sample offers a strong gate-dependent change of the current flow. But also the geometrical properties of the silicon nanowires have to be taken into consideration. In doing so the diameters of the at 60 mbar grown nanowires are smaller than the diameters of the nanowires grown at 3 mbar and 15 mbar. The smaller nanowire diameter leads to a smaller effective channel, which increases the characteristic of the field effect. Nevertheless it is shown that nanowires can act as FET-devices in nanoelectronic applications in the future.

4.3 Electrical characterization of doped NWs

4.3.1 Silicon nanowire doping via SOD

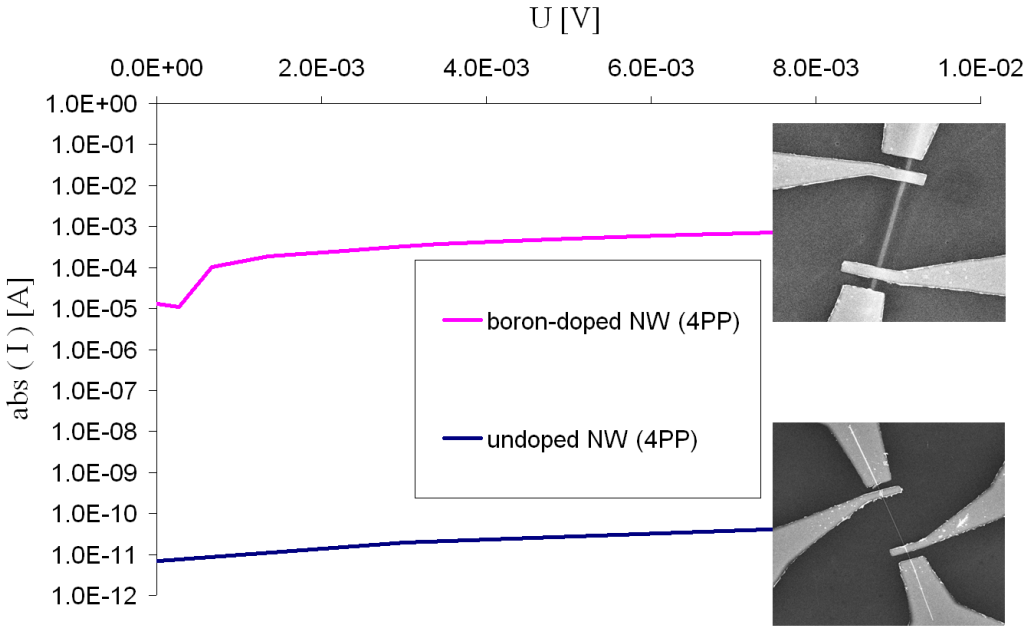


Figure 4.16: *I-V curves of an undoped silicon nanowire and a highly boron-doped silicon nanowire via Spin-On-Dopant-Boron diffusion. The 4PP data points represent the resistance at the inner contacts. (top right inset: SEM image of the boron-doped nanowire, bottom right inset: SEM image of the undoped nanowire)*

Figure 4.16 illustrates the I-V characteristic of an intrinsic nanowire in comparison to a highly p-doped silicon nanowire via Spin-On-Dopant-Boron (SOD-B) diffusion. Both nanowires are from the same sample and were grown at a total pressure of 60 mbar. The electric current of the doped nanowire is considerably larger than the intrinsic one, thus one can assume a successful doping via the SOD-B compound.

Figure 4.17 shows the result of my performed experimental series to obtain the time dependence of the SOD-B diffusion process. The resistivity of

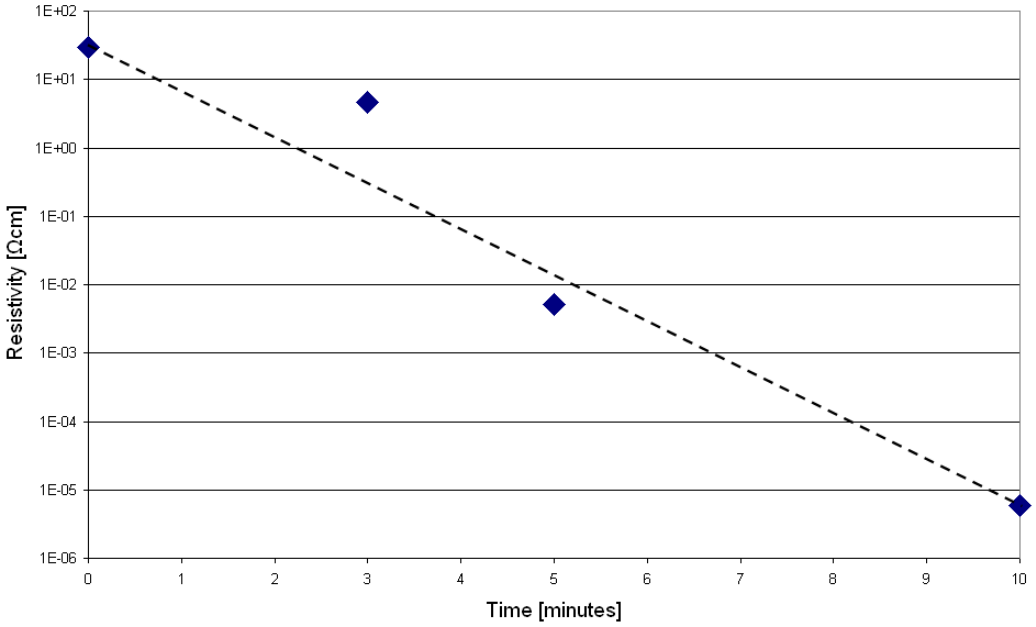


Figure 4.17: *Influence of the SOD-B doping processing time on the resistivity (T = constant = 950 °C).*

the nanowires was calculated using the data of the electrical measurements of boron-doped silicon nanowires at three different baking durations (3, 5, and 10 minutes). Beside these three resistivity values a fourth resistivity factor of an intrinsic nanowire was acquired and placed as data point at zero. The resulting curve progression shows a nearly logarithmic decrease of the resistivity the longer the diffusion process lasts.

Figure 4.18 shows the temperature dependence of the diffusion process via SOD-B. Now the calculated nanowire resistivity values at three different baking temperatures (850 °C, 900 °C, and 950 °C) were put into a diagram, included with the resistivity value of an intrinsic nanowire again placed at zero. The resulting curve shows a sharp decline of the resistivity value between 900 °C and 950 °C. The resistivity values for 850 °C and 900 °C are close together.

In summary it can be said that a sufficiently high temperature is required

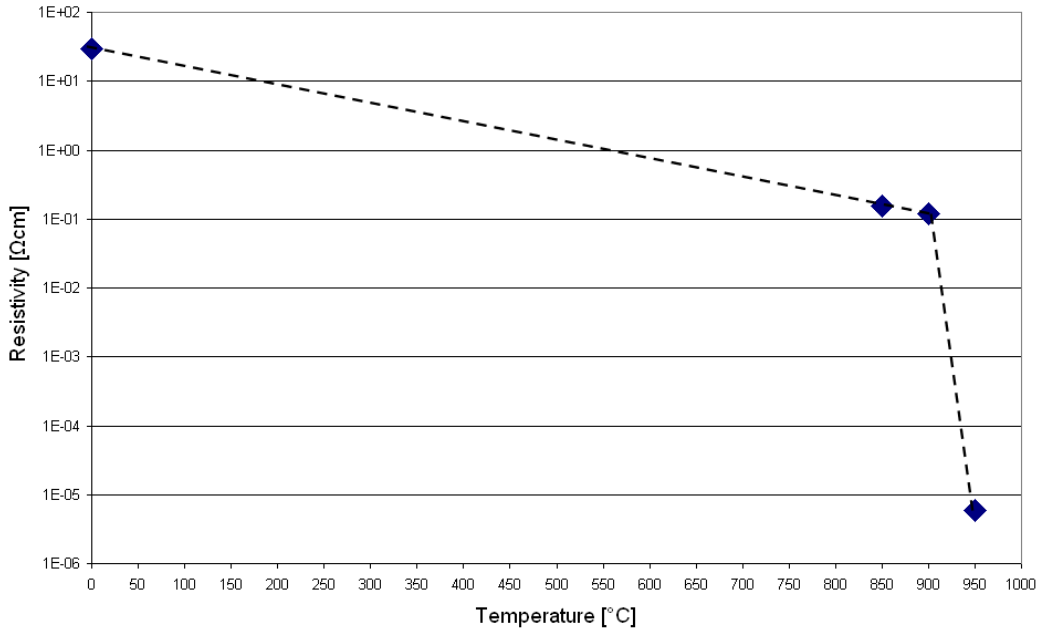


Figure 4.18: *Influence of the SOD-B doping processing temperature on the resistivity (t = constant = 10 minutes).*

for high doping levels using SOD-B. At a diffusion duration of 10 minutes the nanowires were highly doped at a temperature of 950 ℃. Using temperatures of 850 ℃ and 900 ℃ resulted in moderate doping levels. The desired doping concentration of the nanowire can be controlled to a fairly high degree by variation of the diffusion time. The curve progression of the time dependence is nearly logarithmic and therefore easily reproducible.

4.3.2 Silicon nanowire doping by vapor phase diffusion

Phosphoric acid was used for n-type doping of silicon nanowires and then contacted via electron beam lithography. Next, the electrical properties of the nanowires were investigated doing four point probe and two point probe measurements. Finally the resistivity of phosphoric acid doped silicon nanowires with three different diameters was determined and compared.

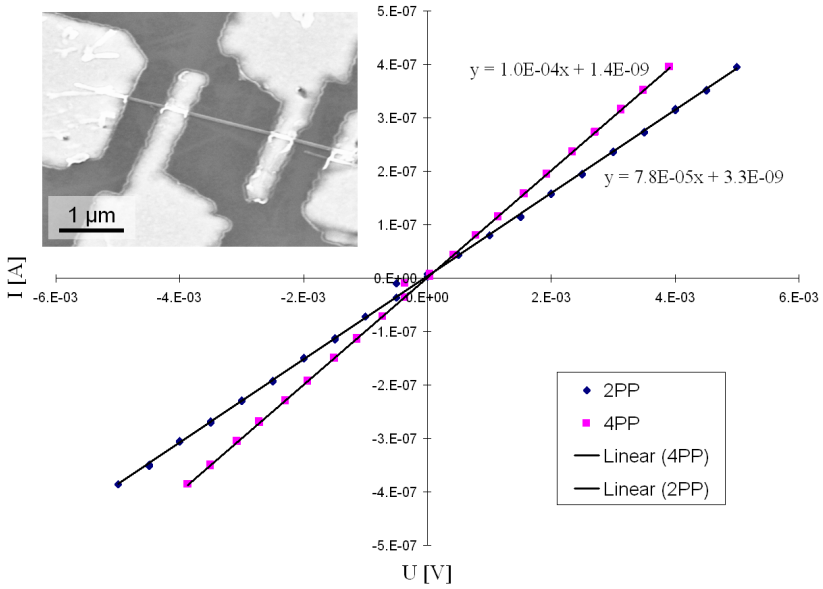


Figure 4.19: *I-V curves of a phosphorus-doped silicon nanowire doped via phosphoric acid diffusion. The 4PP data points represent the resistance at the inner contacts. The 2PP data points represent the resistance at the outer contacts. The inset shows the SEM image of the contacted nanowire.*

Figure 4.19 shows the I-V curves of a phosphorus-doped silicon nanowire. Both, the four point probe (4PP) and the two point probe (2PP) data points are strictly linear. Due to the high doping of the nanowires the contact resistance is nearly negligible, as there does not exist big differences between the two curve gradients.

Figure 4.20 shows the I-V stress test curve of a phosphorus-doped silicon

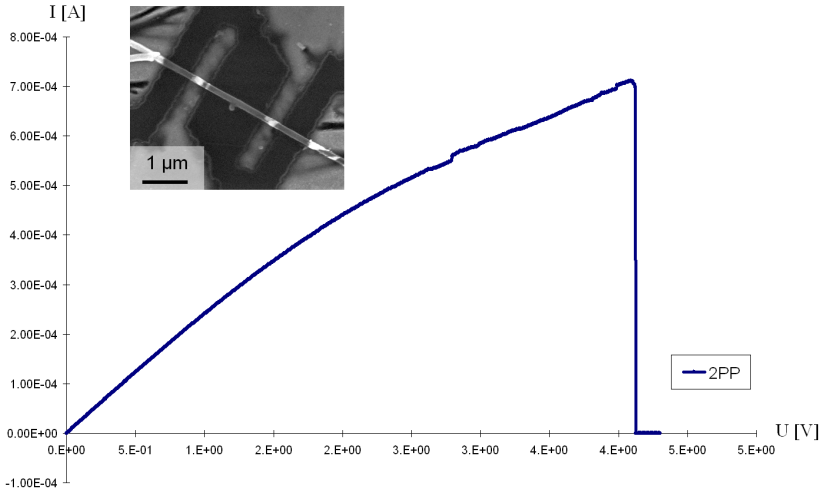


Figure 4.20: *I-V stress test curve of a phosphorus-doped silicon nanowire via phosphoric acid diffusion. The 2PP data represent the resistance at the outer contacts. The breakdown of the current flow through the nanowire at a peak current of 700 μA corresponds to a current density of $6.2 \cdot 10^6\, A/cm^2$. The inset shows the SEM image of the contacted nanowire.*

diameter [nm]	resistance [kΩ]	resistivity [mΩcm]
56	19.65	4.84
78	10.00	4.78
114	0.909	0.93

Table 4.1: *Resistance and resistivity of three phosphorus doped silicon nanowires with different diameters.*

nanowire. The current of the two point probe (2PP) data rises with increasing voltage till a peak current of 700 μA. This current corresponds to a current density of $6.2 \cdot 10^6\, A/cm^2$. In comparison the maximum recommended current density for copper wires is around $6 \cdot 10^4\, A/cm^2$. The high current density withstood by the silicon nanowire is rather remarkable. After reaching the peak point the nanowire shows a total breakdown of the current flow, with no visible change of the nanowire and the contacts seen via SEM. Nevertheless after the stress test the nanowire seemed to be defective because no further electrical measurements were accomplishable.

The resistivity of three phosphorus-doped silicon nanowires with ascending diameters was determined (see table 4.1). While the resistivity of the nanowires with a diameter of 56 nm and 78 nm is nearly equal, the resistivity of the nanowire with a diameter of 114 nm is marginally lower. It seems to me that this lower resistivity may occur because of a better integration of the dopant atoms in nanowires with larger volumes.

4.3.3 Silicon nanowire doping via ion implantation

After the silicon nanowires were boron-doped via ion implantation (ion energy: 30 keV, ion dose: $4 \cdot 10^{13}\, cm^{-2}$) and then annealed, contacting was done using electron beam lithography. Next, the electrical properties of these implanted silicon nanowires were determined, using four point probe and field effect measurements.

Figure 4.21 shows the I-V curves of a boron-doped silicon nanowire via ion implantation. The annealing step was done at a temperature of 850 ℃ for 15 minutes in a helium atmosphere. The linear 2PP curve indicates good metal/semiconductor contacts. The calculated resistivity of the nanowire is $17.44\,\Omega cm$.

Figure 4.22 shows the I-V curves of the same boron-implanted silicon nanowire type as above. This time the annealing step was done at a temperature of 950 ℃ for 15 minutes again in a helium atmosphere. Because the 2PP curve is linear one can assume that this nanowire sample shows again a low contact resistance. The calculated resistivity of the nanowire is $19.64\,\Omega cm$, which is nearly equal to the resistivity of the nanowire annealed at 850 ℃.

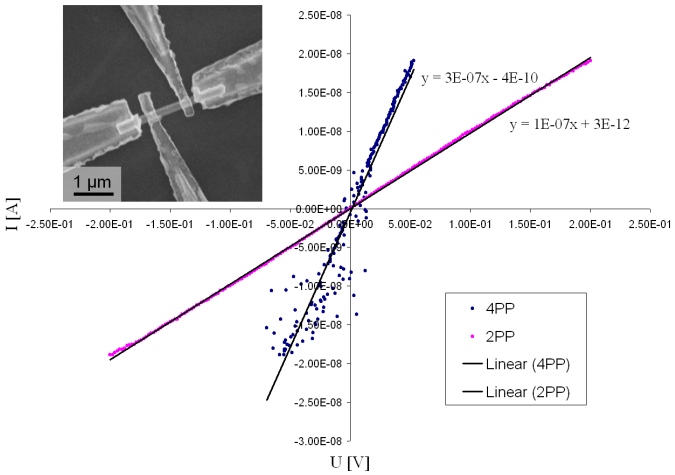


Figure 4.21: *I-V curves of a boron-implanted silicon nanowire with an annealing temperature of 850 ℃ for a duration of 15 minutes. The 4PP data points represent the resistance of the inner nanowire segment. The 2PP data points represent the resistance between the outer contacts. The inset shows the SEM image of the contacted nanowire.*

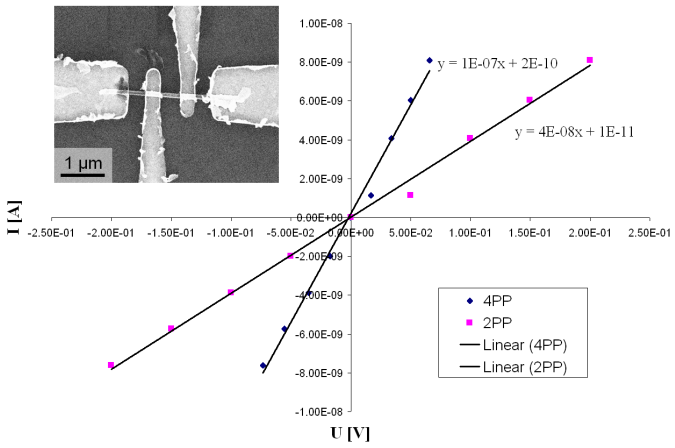


Figure 4.22: *I-V curves of a boron-implanted silicon nanowire with an annealing temperature of 950 ℃ for a duration of 15 minutes. The 4PP data points represent the resistance of the inner nanowire segment. The 2PP data points represent the resistance between the outer contacts. The inset shows the SEM image of the contacted nanowire.*

In summary an annealing step at a temperature of 850 ℃ is sufficient for the electrical activation of boron dopant atoms in the silicon crystal. Unfortunately the "high" resistivity values identify a low doping level in comparison to doped bulk silicon resistivity values. If you take into consideration the resistivity values of the phosphoric acid doped silicon nanowires described above, the resistivity of these boron-implanted nanowires is almost 4000 times higher. Ion implantation is an adequate method to dope silicon nanowires, but to achieve higher doping levels it is essential to increase the ion dose to a sufficient amount.

Chapter 5

Summary and Outlook

The ambition of this master thesis was to develop an easier to handle method for controlled nanowire doping. Process parameters and electrical measurements were examined and protocoled to make future nanowire doping procedures available.

The requirement for further miniaturization of integrated circuits to gain more powerful electric devices is given. Nanowires have big potential as they could be an alternative or an addition to traditional components in the nanoelectronic technology. The usage of nanowires may give ample variation possibilities to the development of prospective devices and applications. To unfold all possibilities of the nanowire technology it will be necessary to continue the research on process parameters and nanowire properties.

The second chapter deals with the theoretical aspects of silicon nanowires and acts as the general basis for the following experimental chapters. The chapter starts with describing the VLS mechanism, as it was later used for the growth of my nanowires. Nanowire growth is possible with various semiconductor materials, this work however focuses on the growth of silicon nanowires. Of particular importance is the role of gold as catalyst agent during the growth of silicon nanowires via VLS mechanism. Explained in more

detail is the diameter dependency of nanowires, which plays a crucial role for the growth direction. In addition, the terms of epitaxial nanowire growth are illustrated. A section on electrical characterization of silicon nanowires follows. Considered more deeply are resistivity (two-point probe and four-point probe measurement) and field effect (gate dependency), as well as the results of various researchers are presented. The electrical characteristics of nanowires can be changed through doping. The last section treats three different doping methods, namely in-situ, diffusion, and ion implantation doping.

In third chapter the experimental assemblies of my tests are explained. I begin by describing the used setup of the LPCVD system. Special attention was paid to the preparation of the samples for nanowire growth. Next, the different methods for nanowire doping are presented. First of all doping via Spin-On-Doping was performed, which was followed by doping via phosphoric acid. These two doping methods are based on a diffusion process of the dopants into the silicon nanowire. Another doping method is the ion implantation, where the nanowire is bombarded with dopant atoms. Finally, all doped silicon nanowires were contacted via electron beam lithography to enable electrical measurements.

In the fourth chapter the results of the experimental work is presented. At the beginning images of silicon nanowires grown at different pressure settings were made using SEM and then analyzed further via TEM. Besides electrical measurements were performed with those intrinsic nanowires, these included four-point probe and field effect measurements. The resistivity was calculated using the measurement data and were then compared with each other. Thereafter the electrical characterization of doped silicon nanowires was conducted via four-point probe measurements. The calculated resistivity data provide good reference values for the evaluation of the achieved doping levels. In all the examined cases the used silicon nanowires had lower resistivity values than intrinsic nanowires, this indicates successful doping.

The research on nanowires makes a lot of progress. A steady rise in techni-

cal expertise leads to a continuously growing interest in this field of research. The sound properties of nanowires and the possibility to easily alter the electrical characteristics via doping makes the implementation of nanowires imaginable. Likewise the fact that the field effect occurs to nanowires makes them a good option for transistor components. The adoption of nanowires for devices is just at its beginnings and nanowire integration can push the future development of nanoelectronic devices.

Appendix A

List of process parameters

- **Wet chemical etching:**
  - SiO_2: BHF 7:1 [NH_4F : HF (38%) = 7 : 1],
    etch rate: ∼60 nm/min
- **Sputter deposition:**
  - System: LS 320S from "von Ardenne"
  - Pressures:
    work pressure: $8 \cdot 10^{-3}$ mbar,
    base pressure: $2 \cdot 10^{-5}$ mbar
  - Sputter yield:
    Au: 1.6 nm/s at 50 W,
    Ti: 10 nm/min at 50 W

Appendix B

List of Abbreviations

ADF	Annular Dark-Field imaging
BHF	Buffered Hydrofluoric Acid
CVD	Chemical Vapor Deposition
EBL	Electron Beam Lithography
FET	Field Effect Transistor
HRTEM	High Resolution Transmission Electron Microscopy
LPCVD	Low Pressure Chemical Vapor Deposition
MBE	Molecular Beam Epitaxy
MFC	Mass Flow Controller
MOS	Metal Oxide Semiconductor
PMMA	Polymethylmethacrylate
rpm	Rotations Per Minute
RTA	Rapid Thermal Annealing
RTP	Rapid Thermal Processing

sccm	Standard Cubic Centimeters per Minute (1 sccm is defined as the particle count per minute which flows through 1 cm^3 at a pressure of 1.01325 bar and a temperature of 0°C.)
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectroscopy
SOD	Spin-On-Dopant
SOG	Spin-On-Glass
STEM	Scanning Transmission Electron Microscopy
TEM	Transmission Electron Microscopy
VLS	Vapor Liquid Solid
VLSE	Vapor Liquid Solid Epitaxy

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List of Own Publications

1. A. Lugstein, Y. J. Hyun, M. Steinmair, B. Dielacher, G. Hauer, E. Bertagnolli: *"Some aspects of substrate pretreatment for epitaxial Si nanowire growth"*. Nanotechnology, Vol. 19, pp. 485606 (2008).

2. A. Lugstein, M. Steinmair, Y. J. Hyun, G. Hauer, P. Pongratz, E. Bertagnolli: *"Pressure-Induced Orientation Control of the Growth of Epitaxial Silicon Nanowires"*. Nano Letters, Vol. 8, No. 8, pp. 2310 (2008).

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