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Large-diameter-APD receiver for optical wireless communication

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Abstract

This thesis covers the design of an opto electronic integrated circuit (OEIC) applicable as receiver in an optical wireless communication (OWC) system. With the intended application for digital audio communication, the chip produces an output level of 3.3 V, to ensure compatibility to standard decoding systems. The designed chip is optimized for processing data rates (DRs) appearing with state-of-the-art encoded audio qualities of up to 4.605 Mbit/s. For photo-detection, a fully integrated large area avalanche photo diode (APD) ($\varnothing = 800\,\mu m$) was used, offering higher sensitivity compared to other optical-detector devices. A major challenge, arising with OWC, is sensitivity to background light irradiation. Therefore the receiver contains a dummy-path working as a direct current (DC) reference for the signal-path, together forming a pseudo differential structure. Implemented feedback circuitry is able to sense and cancel an offset between these two paths. Additionally, problems arising with flicker noise when operating at low DR are addressed. Post layout simulations resulted in a sensitivity of −62.34 dBm and a dynamic range of 25.47 dB. The OEIC was designed in a 0.35 µm BiCMOS process.

Kurzfassung

Diese Arbeit umfasst den Entwurf eines optoelektronischen integrierten Schaltkreises (OEIC), einsetzbar als Empfänger für optische Freiraumübertragung (OWC). Der, für den Chip vorgesehene, Anwendungsbereich ist digitale Audiokommunikation. Um Kompatibilität zu etablierten digitalen Dekodiersystemen zu gewährleisten, ist der Chip in der Lage 3.3 V digitalen Ausgangsspannungspegel zu liefern. Die Bandbreite des Empfängers ist auf Datenraten von 4.605 Mbit/s optimiert, die bei modernen Audiosystemen mit hoher Soundqualität auftreten. Die optische Signaldetektion wird durch eine vollintegrierte Lawinenfotodiode mit einem großen Durchmesser von 800 µm realisiert. Diese Photodiodentechnologie bringt eine erhöhte Empfindlichkeit verglichen mit anderen optischen Detektoren. Eine Herausforderung, die OWC mit sich bringt, ist eine gewisse Empfindlichkeit auf Hintergrundlicht, was Arbeitspunkte der Verstärker verschieben kann. Um dem entgegen zu wirken, wurde durch Hinzufügen eines Referenzpfades zum Signalpfad eine pseudo-differenzielle Signalverarbeitung erreicht. Eine zusätzlich implementierte Rückkoppelschaltung ist in der Lage einen Offset zwischen diesen beiden Pfaden zu detektieren und auszulöschen. Weiters wird in der Arbeit das Problem mit starkem Funkelrauschen bei niedrigen Datenraten bearbeitet. Die post-layout simulierten Ergebnisse des Empfängers belaufen sich auf eine Empfindlichkeit von −62.34 dBm und einem Dynamikbereich von 25.47 dB. Der OEIC wurde in einem 0.35 µm BiCMOS Prozess entworfen.

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Glossary

AC alternating current. 34

AGC automated gain control. 31, 32, 54, 60, 61

APD avalanche photo diode. 1–3, 11, 13–15, 17, 18, 21–24, 26, 31–35, 38, 51–54, 58–60, 68

BER bit error rate. 14–17, 26, 39, 47–49, 53, 59, 60

BiCMOS bipolar complementary metal oxide semiconductor. 1, 23, 33

BJT bipolar junction transistor. ii, 7, 10, 11, 26, 29, 55, 67

BLC background light cancellation. 21, 22, 40

CCL common centroid layout. 56

CMFB common-mode feedback. 25, 40, 44–46

CS common source stage. 45, 46, 48

DAC digital to analog converter. 2, 60

DAI digital audio interface. 1, 24, 36, 59, 60

DC direct current. 3, 20, 22, 24, 34, 36–39, 44, 47, 48, 52, 54

DR data rate. 1, 3, 6, 11, 26, 30, 36, 37, 50–52, 59

DTIA dummy transimpedance amplifier. 25, 34

eh pair electron-hole pair. iv, 12, 13

EMI electro-magnetical interference. 1

FDA fully differential operational amplifier. 25, 39, 40, 45–48

FET field effect transistor. 7, 9

GBW gain bandwith product. 4, 26, 28

OCL offset cancellation loop. 24, 25, 34, 36–40, 42, 51, 54, 59

OEIC opto electronic integrated circuit. 1–3

OTA operational transconductance amplifier. 24, 25, 38, 39, 45, 47, 48

OWC optical wireless communication. 1–3, 17, 24, 36, 59

p-epi expitaxial grown and low doped p-type layer. 12

p-sub p-type bulk substrate. 12

p-well p-type well implantation. 34

PCM pulse code modulation. 20

penetration depth the depth were incoming photons generate eh pairs. 12

PINpd pin photo diode. 12, 14, 15, 17

PNd pn diode. 11

PWD pulse width distortion. ix, 17, 25, 36, 39, 47, 49

RAPD reference-APD. 24, 31, 32, 58, 60

RCLED resonant cavity light emitting diode. 2, 17, 18, 55

RMS root mean square. 5, 14, 15, 30, 51

S/PDIF Sony/Phillips-Digital-Interface. 19

SF source follower. 47

SiAPD signal-APD. 24, 31, 32, 55, 60

SNR signal to noise ratio. 14–16

SPAD single photon avalanche diode. 11, 13

SPECTRE simulator. 30

TIA transimpedance amplifier. 3, 4, 7, 9–11, 15, 17, 21–23, 25–31, 34, 35, 37–39, 47, 51, 52

TOSLINK Toshiba-link. 2, 19, 22, 36, 37, 39, 51, 59

traps contamination and defects in the crystal lattice. 6

List of Symbols

A_{APD} area of the active APD window. 18

α aperture angle of the transmitting RCLED. 18

A_r area of a spherical cone segment. 18

β_{FB} feedback factor. 4

C_{APD} APD capacity. 34

C_{dummy} dummy capacity. 24, 35

C_{EXT} external capacitance, to increase the OCL time constant. 39

C_{INT} internal capacitance, to define the lower limit of the OCL time constant. 37

C_{ox} gate oxide capacitance per unit area. 40

E_R extinction ratio. 18, 39, 55

$F(f)$ noise figure. 7

F_{EX} excess noise factor. 14

f_l lower $-3\,\mathrm{dB}$ cut-off frequency. 5, 37, 40

$f_{l,max}$ maximum lower $-3\,\mathrm{dB}$ cut-off frequency. 37

f_u upper $-3\,\mathrm{dB}$ cut-off frequency. 5

$f_c(1/f)$ flicker noise cut-off frequency. 6, 7, 9

I_{APD} light intensity at the receiver. 17

i_{APD} APD current. 31

$i_{APD,0}$ APD photo-current when receiving a '0'. 38, 39

$i_{APD,1}$ APD photo-current when receiving a '1'. 38

$i_{APD,DC}$ DC photo-current of the APD. 39, 40

i_{BL} APD photo-current induced by backgroundlight irradiation. 38, 39

i_{dark} photo-current for APD in *dark-mode*. 32

$i^2_{n,APD0}$ input referred APD mean square noise when receiving a '0'. 52

$i^2_{n,APD1}$ input referred APD mean square noise when receiving a '1'. 52

$i^2_{n,el}$ input referred mean square noise of the electonic circuit. 52

$i^2_{n,MOS}$ input referred mean square noise of M_{OCL}. 52

i^{rms}_{n} total input referred RMS noise of the receiver. 30, 40

$i^{rms}_{n,0}$ total input referred RMS noise when reveiving a '0'. 51

$i^{rms}_{n,1}$ total input referred RMS noise when reveiving a '1'. 51

$i^{rms}_{n,TIA}$ input referred RMS noise of the TIA. 37

i^{pp}_{ovl} overload current of the receiver. 17, 48

$i^{pp}_{ovl,lin}$ linear overload current of the receiver. 47

i^{pp}_{sens} electrical sensitivity of the receiver. 16

k_B Boltzmann constant. 6

k_D drain noise factor. 9

k_{eff} impact ionization coefficient ratio. 14, 59

k_f flicker noise factor. 6, 28

M APD multiplication. 14, 31

M_{OCL} p-MOS transistor for the OCL. 24, 38–40

M_{opt} optimal multiplication, where the maximum sensitivity can be achieved. 53

μ_p charge carrier mobility in pMOS transistors. 40

$\overline{P}_{APD}$ power received by the APD. 14

P_{APD0} received optical power when a '0' was sent. 38

P_{APD1} received optical power when a '1' was sent. 38

$\overline{P}_{ovl}$ optical overload power. 17

$\overline{P}_{sens}$ optical sensitivity. 17

$\overline{P}_{tr}$ transmitted optical power by the RCLED. 17

r distance between RCLED and APD at the optical transmission path. 18

R responsivity. 14, 59

R_{FB} TIA feedback resistor. 3, 4, 26, 30

R_{INT} internal resistance, to define the lower limit of the OCL time constant. 37

r_{max} maximum operating distance for the transmission system. 55

r_{min} minimum operating distance for the transmission system. 55

R_S p-substrate series resistance. 34, 35

R_T transimpedance. 3, 30

R_{T0} DC transimpedance. 30

$R_{T,(TIA+SF+FDA)}$ transimpedance from TIA input to the output of the FDA. 47

τ_{min} minimum time constant of the OCL. 37

V_{bias} APD reverse bias voltage. 13

V_{break} breakdown voltage of APD. 13, 23

V_{CM} voltage to adjust the common mode voltage of the FDA output. 25, 39, 47, 48

V_{com} common mode voltage at FDA output, after the offset was canceled. 25, 45, 47

V_{com1} common mode voltage at out1, before the offset was canceled. 25, 38, 39, 45

V_{com2} common mode voltage at out2, before the offset was canceled. 25, 45

V_G gate potential of M_{OCL}. 38, 39

w radius of the light cone. 19

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Chapter 1

Introduction

1.1 Motivation

State of the art hifi-systems use optical transmission to transfer digital audio signals from sound-cards to receivers at high DRs. The often preferred medium for this information transport is glass fiber. Compared to copper wires it comes with many advantages, like for example higher bandwidth and insensitivity to electro-magnetical interference (EMI). But it also comes with some detriments when considering destructibility through tight bending radii, or the rather high costs of the technology. Another approach, utilizing the benefits of optical signal transmission, but without drawbacks of glass fiber, is OWC. This concept facilitates a very versatile communication system, since for example the transmission distance is easily alterable and not dependent on a fiber's length. However, methods to deal with sensitivity to background light volatility, need to be considered.

This thesis focuses on developing an OEIC for the receiver side in an OWC-system, especially optimized for digital audio DRs. The chip should be capable of receiving state-of-the-art audio quality, while generating digital output levels, to provide compatibility to standard digital audio interface (DAI) ICs. The available 0.35 µm bipolar complementary metal oxide semiconductor (BiCMOS) process, enables to realize a fully integrated design, containing a large diameter APD (800 µm) as photo-detector, and the electronic receiver together on the same chip.

1.2 System concept

In modern digital audio transmission systems, several different components are involved in transporting the information from the sound-processor to the speakers. Usually the first stage is a sound-card, it processes and encodes the audio information according to a standard DAI. State-of-the-art processors are capable of handling audio data from 16

bit, sampled at 32 kHz, to 24 bit @ 192 kHz (covered in subsection 2.5.1). The signal gets modulated for transmission over a certain transport medium (e.g. copper wire, glass fiber, or air). The information then needs to be received and conditioned to be fed into a decoding component and a digital to analog converter (DAC), which outputs a multi-channel analog audio signal. Some additional amplification can be performed before feeding into the speakers. Figure 1.1 a) depicts the system setup, when using a glass fiber based transmission channel, often implemented with the Toshiba-link (TOSLINK) standard. Most of the available sound-cards have a transmission amplifier and resonant cavity light emitting diode (RCLED) modulator already included in a glass fiber connector on the PCB (often referred to as TOSLINK-TX jack). The data, transported by the fiber, is then received by a TOSLINK-RX jack, with integrated photo-detector and receiver. When approaching audio transmission with OWC, these components need to be modified. The RCLED modulator may need more transmitting power, but that depends mainly on the specified operating distance. For the receiver, additional requirements, such as higher signal sensitivity and possibly more background light immunity, emerge. This suits well to the usage of a large diameter APD for photo-detection, since it has improved signal sensitivity compared other devices (covered in section 1.5). For desensitizing the receiver against background light irradiation, already some concepts were presented in literature (covered in section 1.10). Figure 1.1 b) shows, how the developed chip is embedded in an audio transmission system, it is intended, to replace the TOSLINK-RX jack when changing from fiber based communication to OWC.

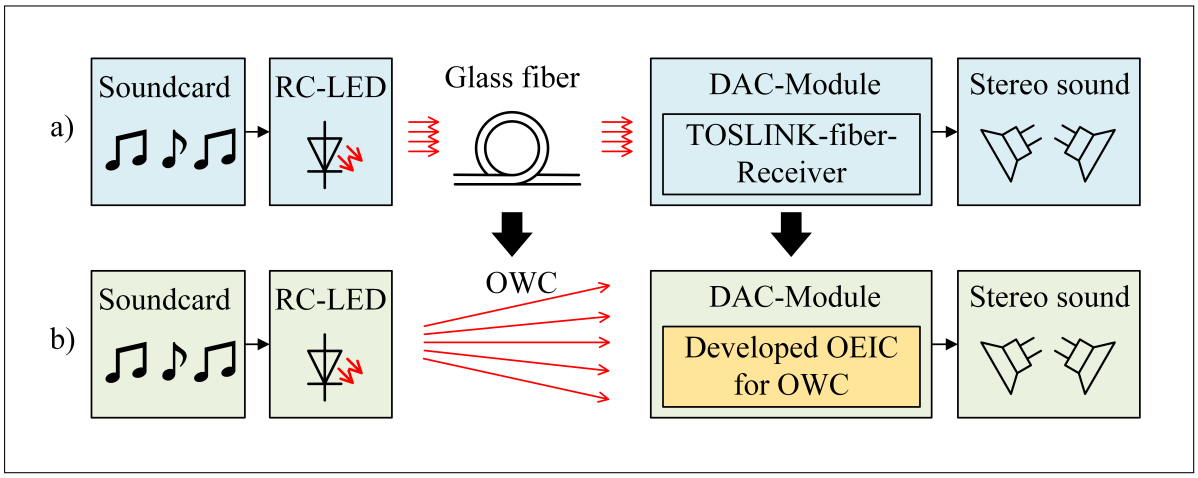


Fig. 1.1: Transformation from a wired to a wireless optical communication path. a) State of the art configuration with transmission via glass fiber. b) New configuration with transmission over the air and the developed OEIC receiver.

1.3 Basics of TIAs

This section aims to give a short introduction to one of the most important components in an optical-receiver-system, the transimpedance amplifier (TIA). Different structures with their advantages as well as the basic circuit parameters will be addressed.

Any circuit that converts current into voltage, possibly with an amplification, is basically referred to as TIA [22]. An important parameter for these amplifiers is the transimpedance R_T, it gives the proportional relationship between change in output voltage over change in input current as

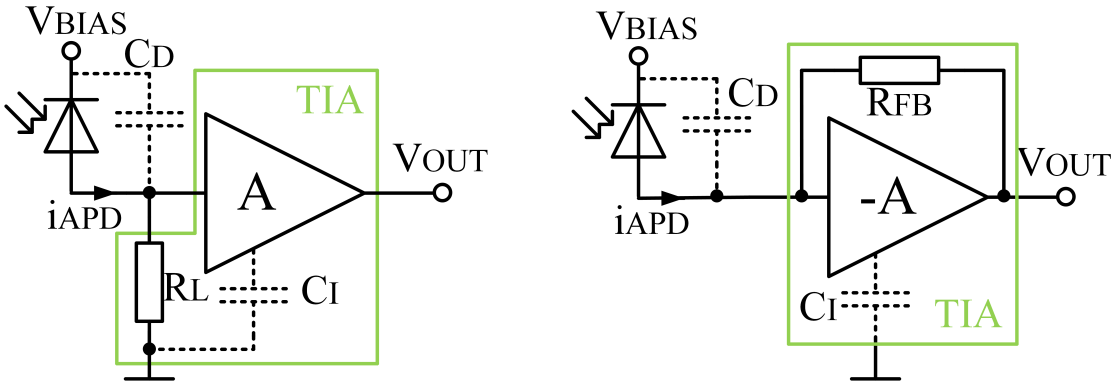
$$R_T = \frac{\mathrm{d}v_{out}}{\mathrm{d}i_{in}} \tag{1.1}$$

and is generally frequency dependent.

Basically, there can be distinguished between three different types of TIA structures (depicted in Figure 1.2), each one comes with some benefits and disadvantages.

- **Low impedance front-end:** Over a small value load resistor, the photo-current is converted into voltage which is then amplified. This circuit is very simple while achieving high bandwidths but on the other hand it has a low R_T and poor noise performance due to thermal noise, generated in the resistor ($1/\sqrt{R}$ dependency).
- **High impedance front-end:** Keeping simplicity of the circuit but choosing a high value load resistor leads to improvements considering noise performance and R_T, but comes with heavy penalty in terms of bandwidth.
- **Shunt feedback:** The photo-current is converted into voltage by a feedback resistor over an inverting voltage amplifier. This works by having virtual ground (for high gains) at the amplifier's input and therefore most of the photo current flowing through R_{FB} leading to a voltage at the output. Benefits of the shunt feedback TIA are high transimpedance and proper noise performance while sustaining reasonable bandwidth, but on the other hand, it comes with more circuit complexity.

In this thesis the TIA will be carried out with a shunt feedback structure. Considering finite values for the open loop gain A in non-ideal circuits, implies a non perfect virtual ground. This leads to variability of the photo-detector's reverse bias voltage, which in best case, should be kept constant. Also the DC-transimpedance decreases, which can be calculated by



(a) TIA with impedance front-end **(b)** TIA with shunt feedback.

Fig. 1.2: Basic types of TIA principles, A describes the gain of the amplifier stage, the shunt feedback TIA uses negative feedback.

$$R_{T0} = \frac{A}{A+1} R_{FB}. \tag{1.2}$$

For bandwidth approximation, the total capacitance at the input node C_T needs to be determined. It consists of the photon detector capacitance C_D and the amplifier's input capacitance C_I ($C_T = C_D + C_I$). This leads to the frequency dependent transimpedance

$$R_T(j\omega) = -R_{T0} \frac{1}{1 + j\frac{\omega}{\omega_c}} \tag{1.3}$$

with the cut-off frequency

$$\omega_c = \frac{A+1}{R_{FB} C_T}. \tag{1.4}$$

By implementing negative feedback, certain performance improvements can be achieved. Though, an increase in bandwidth by a factor of $(1 + A\beta_{FB})$, also implies a reduction of the gain by the same factor [8]. This constant gain bandwith product (GBW), allows to trade gain against bandwidth and vice versa. In practice this can be used to create broadband receivers, whereat reduction of the gain has to be compensated by additional amplifier stages. In section 2.3 the gain-bandwidth scaling will be exercised by varying the TIA's feedback factor β_{FB}, which is determined by R_{FB}. The intention is to optimize the design in terms of noise performance.

1.4 Noise considerations

1.4.1 Equivalent input noise

Noise is a stochastic phenomenon, therefore noise currents and voltages are described by spectral densities ($|u_n(f)|^2, |i_n(f)|^2$), which represent the spectral distribution of the corresponding root mean square (RMS) values. These can be calculated by

$$u_n^{rms} = \sqrt{\int_{f_l}^{f_u} |u_n(f)|^2 \, \mathrm{d}f} \tag{1.5}$$

$$i_n^{rms} = \sqrt{\int_{f_l}^{f_u} |i_n(f)|^2 \, \mathrm{d}f} \tag{1.6}$$

when considering the lower (f_l) and upper (f_u) cut-off frequencies of an universal amplifier's frequency response. To ease calculations regarding noise performance in complex electronic circuits, noise sources of individual components can be combined to get equivalent input noise generators (Figure 1.3). They represent the amount of noise, needed to be generated at the input, for modeling the exact behavior of all noise sources in the circuit.

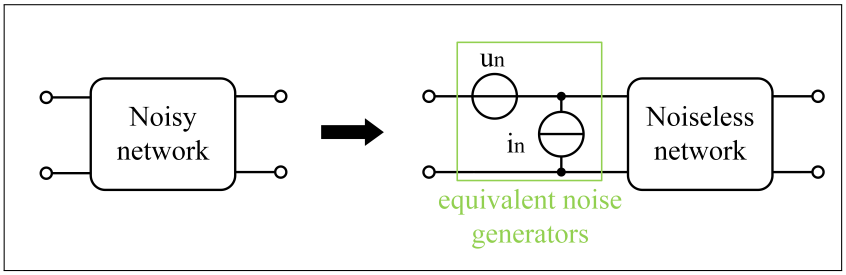


Fig. 1.3: Modeling the noise in an electronic network by equivalent noise generators at the input.

1.4.2 Major noise sources

Noise models for common electronic components are a superposition of fundamental physical noise phenomena. The major three will be briefly described in the following part ([8], [26]). They will be presented by their mean-square values, which already takes the bandwidth of the electronic circuit into account. Mean-square noise can be expressed by spectral noise densities as

$$i_n^2 = \int_{f_l}^{f_u} |i_n(f)|^2 \, \mathrm{d}f = |i_n(f)|^2 \Big|_{f_l}^{f_u} = |i_n(f)|^2 \underbrace{(f_u - f_l)}_{\Delta f}. \tag{1.7}$$

- **Thermal noise** appears in resistors and originates from thermal movements of charge carriers. It is proportional to the absolute temperature T and can be expressed as an equivalent current by

$$i_n^2 = 4k_B T \frac{1}{R} \Delta f \tag{1.8}$$

with k_B as Boltzmann-constant and Δf as the noise bandwidth of the electronic circuit in which the resistor is embedded.

- **Shot noise** occurs at pn-junctions and describes a small random fluctuation in the current caused by a large number of charge carriers overcoming the potential barrier in the junction. The passage of this barrier depends on having sufficient energy and a velocity directed towards the junction, and is therefore a statistical process. Shot noise has a resulting mean square value which can be described via

$$i_n^2 = 2qI_D \Delta f \tag{1.9}$$

with the electron charge q and the current over junction I_D. Thermal noise as well as shot noise are frequency independent, leading to a constant spectral distribution. This is often referred to as white noise.

- **Flicker noise** is also called $1/f$-noise, because of it's inverse proportionality to the frequency. It is caused by so called "traps", which is a denotation for contamination and defects in the crystal lattice [21]. Charge carriers were affiliated and released randomly by these traps. The time constants involved with this phenomena cause a decline of noise contribution at higher frequencies. The mean square value can be modeled by

$$i_n^2 = k_f \frac{I^\gamma}{f} \Delta f \tag{1.10}$$

with k_f respectively γ as device and process specific constants. As flicker noise appears with moving charge carriers it also depends on a certain direct current I.

Flicker noise is decisive at low frequencies, though in some devices it can dominate the noise contribution into the MHz range. That makes it a very important factor to keep an eye on in this thesis, were DRs of about 5 Mbit/s are pursued. A crucial parameter to be considered during design is the flicker noise cut-off frequency $f_c(1/f)$. It characterizes the point in the noise spectrum, were flicker noise falls below white noise

(containing shot and thermal noise). In practice, values from 100 Hz to 10 kHz should be achieved, but there are also devices with values up to 10 MHz. Analytic expressions of $f_c(1/f)$ for field effect transistors (FETs) and BJTs are derived in subsection 1.4.5.

1.4.3 Noise figure

For comparison of the noise performance for different amplifiers, also the signal source needs to be considered. It can be modeled by a voltage source u_0 with an internal resistance R_0 and generates noise, represented by a spectral density $|u_{n,0}(f)|^2$. Depicted in Figure 1.4, this signal generator noise density, together with the equivalent input noise density of an amplifier, can be combined to an equivalent signal generator noise density $|u_{n,e}(f)|^2$, calculated by

$$|u_{n,e}(f)|^2 = |u_{n,0}(f)|^2 + |u_{n,i}(f)|^2 + R_0^2\,|i_{n,i}(f)|^2\,. \tag{1.11}$$

This leads to the introduction of a standardized parameter that facilitates comparison of electronic systems in terms of noise performance, the noise figure $F(f)$. The idea is to relate $|u_{n,e}(f)|^2$ to a reference signal generator noise density $|u_{n,0}(f)|^2$ with a reference temperature T_0 =290 K, leading to

$$F(f) = \frac{|u_{n,e}(f)|^2}{|u_{n,0}(f)|^2} = 1 + \frac{|u_{n,i}(f)|^2 + R_0^2\,|i_{n,i}(f)|^2}{4k_B T_0 R_0} \tag{1.12}$$

So $F(f)$ gives a measure of how much the noise of the reference signal generator is increased by the amplifier. It is important to notice, that this parameter depends on the internal resistance of the signal generator.

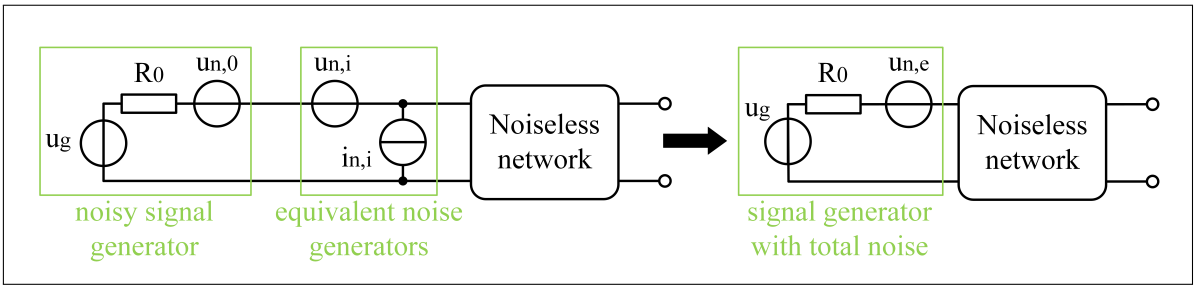


Fig. 1.4: Combining equivalent circuit noise generators with noise of a signal generator.

1.4.4 Noise contribution of single stages in amplifier chains

In practice, electronic receivers often contain amplifier chains, also TIAs for example can be understood as an apposition of single transistor amplifiers. An interesting question is:

how does the noise figure of a single amplifier stage contribute to the total noise figure? It turns out, that especially for the first amplifier stage, efforts for noise minimization pay off.

The setup for a two element amplifier chain with a signal generator is depicted in Figure 1.5. Every stage has it's small signal parameters, input (r_e) and output (r_o) resistance and the noise operation gain $A_{O,n}$, which gives the amplifiers gain while operating with a signal generator at the input and load at the output. It is expressed by

$$A_{O,ni} = \frac{r_{ei}}{r_{o(i-1)} r_{ei}} A_i \tag{1.13}$$

with A as the amplifier's open-loop gain and i meaning the index. r_{o0} would be the internal resistance of the signal generator, coming into play for the first amplifier stage. In [26] the total noise figure is then presented as

$$F = F_1 + \frac{F_2 - 1}{A_{O,n1}^2} \frac{r_{o1}}{r_{o0}} + \frac{F_3 - 1}{A_{O,n1}^2 A_{O,r2}^2} \frac{r_{o2}}{r_{o0}} + \cdots \tag{1.14}$$

This shows that the noise figure of the first amplifier stage goes directly into the noise figure of the whole chain. So efforts in optimizing F_1, immediately turn into account. Noise contribution of later elements can be reduced by increasing $A_{O,n1}$ via A_1 and r_{e1} (shown in Equation 1.13). Another fact that should be considered, especially for signal sources with low internal resistance, is to minimize r_{o1}. When r_{o1}/r_{o0} overrules $1/A_{O,n1}^2$, F_2 can also play a dominant role in the total noise figure. However in applications with optical detectors, this part is most likely negligible due to very high r_{o0}.

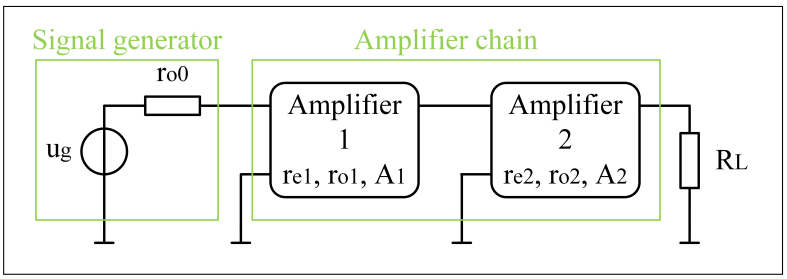


Fig. 1.5: Setup for a two element amplifier chain with a signal generator.

1.4.5 Noise in transistors

In the following section, common noise models for two transistor types are presented. Furthermore the flicker cut-off frequency, which is of interest for the TIA, designed in this thesis, will be expressed for each device.

1.4.5.1 MOSFET

Though FETs have little thermal noise induced by a parasitic gate resistance R_D, it is rather negligible in this application. The major noise source is the channel, were thermal and flicker noise is generated. Both contributers depend on the operating point, the thermal part via the transconductance g_m (see Equation 2.6) and the flicker part via the drain current $I_{D,op}$. Additionally there is a capacitive coupling from channel to gate via the gate capacitance C_{GD}, which adds induced gate noise. Since it has a $\sim f^2$ dependency, it comes into play at high frequencies and therefore will be neglected for calculation of the flicker cut-off frequency. Though for calculating the equivalent input noise it will be considered. So neglecting induced gate noise, the mean-square noise value for MOSFETs is expressed as

$$i_{n,D}^2 = \left(4k_BTk_Dg_m + k_f\frac{I_{D,op}^{\gamma}}{f}\right)\Delta f \tag{1.15}$$

with the drain noise factor k_D, which is approximately $k_D \approx 2/3$ for $L > 1\,\mu\text{m}$ and $k_D \approx 1$ for $L \approx 100\,\text{nm}$. The flicker cut-off frequency is determined by equating thermal with flicker noise in Equation 1.15, which is leads to

$$f_c(1/f) = \frac{k_f I_{D,op}^{\gamma}}{4k_BTk_Dg_m}. \tag{1.16}$$

For MOSFETs the flicker noise factor scales by $k_f \sim 1/L^2$, therefore $f_c(1/f)$ and with it the flicker noise decreases for larger transistors. This information is crucial for the TIA design covered in section 2.3. The equivalent input noise densities for MOSFETs are derived in [26], as

$$|u_{n,i}(f)|^2 = \frac{4k_BTk_D}{g_m}\left(1 + \frac{f_c(1/f)}{f}\right) \tag{1.17}$$

and

$$|i_{n,i}(f)|^2 = 4k_BTg_mk_I\left(\frac{f}{f_T}\right)^2 \tag{1.18}$$

while neglecting R_D but considering induced gate noise. k_I is a constant depending on k_D, c_{GD} and the gate noise factor k_G.

1.4.5.2 BJT

In bipolar transistors, thermal noise is generated by the parasitic base series resistance R_B. In addition to that, the base and collector currents cause shot and flicker noise in dependence of their operating points ($I_{B,op}, I_{C,op}$). Like in subsubsection 1.4.5.1 all noise contributers proportional to f^2 are neglected for calculation of the flicker cut-off frequency, this leads to the mean-square noise values

$$i_{n,B}^2 = \Big(4k_BT\frac{1}{R_B} + 2qI_{B,op} + k_f\frac{I_{B,op}^{\gamma}}{f}\Big)\Delta f \tag{1.19}$$

and

$$i_{n,C}^2 = \Big(2qI_{C,op} + k_f\frac{I_{C,op}^{\gamma}}{f}\Big)\Delta f. \tag{1.20}$$

The flicker cut-off frequency is again defined as the point were $1/f$ falls below white noise. So for the collector side this means to equalize both parts from Equation 1.20, which gives

$$f_c(1/f) = k_f\frac{I_{C,op}^{(\gamma-1)}}{2q}. \tag{1.21}$$

This
and the BJTs operating point, which dependency can be canceled by choosing $\gamma = 1$. The equivalent input noise densities for BJT are presented in the Appendix A.1.

1.4.6 $1/f$-noise in MOSFET-front-end TIAs for opto-receivers

As subsection 1.4.4 shows, the most dominant noise contributer in an amplifier system is the first stage. This means the front-end transistor in a TIA plays a very important role for minimizing the total noise figure. In opto-receivers, MOSFETs perform much better than BJTs as TIA front-ends, because of the high internal resistances of photo-diodes. The reason for this superiority can be shown by the expression of the noise figure. It is reached by applying (1.17) and (1.18) into (1.12), which gives

$$F_{MOS}(f) = 1 + \frac{k_D}{g_mR_0}\Big(1 + \frac{f_c(1/f)}{f}\Big) + g_mR_0k_I\Big(\frac{f}{f_T}\Big)^2. \tag{1.22}$$

The noise figure spectrum can be divided into three parts, always assuming application with a photo-detector implying very high internal resistance R_0.

- **For low frequencies** the flicker noise dominates, which gives a noise figure proportional to $1/f$:

$$F_{MOS} \approx \frac{k_D}{g_m R_0} \frac{f_c(1/f)}{f} \tag{1.23}$$

- **For medium frequencies** the noise figure is constant and for high R_0 it converges against 1:

$$F_{MOS} \approx 1 + \frac{k_D}{g_m R_0} \tag{1.24}$$

- **For high frequencies** noise increases drastically with a squared dependency:

$$F_{MOS} \approx g_m R_0 k_I \left(\frac{f}{f_T}\right)^2 \tag{1.25}$$

Figure 1.6 shows a typical graph of a MOSFET noise figure. f_1 denotes the frequency at which white noise becomes dominant over flicker noise. Therefore it is calculated by equating F_{MOS} from (1.23) with (1.24), which gives

$$f_1 = \frac{k_D}{g_m R_0} \frac{f_c(1/f)}{1 + \frac{k_D}{g_m R_0}} = \frac{k_D f_c(1/f)}{g_m R_0 + k_D}.$$

High values for R_0 decrease flicker and white noise, and therefore pushing f_1 to lower values. In best case, it should be as low as possible. On the contrary, large values for R_0 imply an increase of noise at high frequencies. As mentioned before, low DRs are used for signal transmission in this thesis. Which means that the designed receiver will have a rather small upper cut-off frequency. That makes noise effects, dominant at high frequencies, irrelevant.

To summarize briefly, MOSFETs perform excellent when operating in conditions of low DRs and with photo-diodes as signal generators. Based on this facts the TIA in this thesis will be carried out with a MOSFET front-end. BJTs perform much better at higher DRs due to their larger transit frequencies. For further information, the noise figure for BJTs is presented in the Appendix A.1.

1.5 Basics of APDs

This section will demonstrate the operation principle of photon detection, illustrating the evolution from basic devices like pn diode (PNd) to more sophisticated ones like APDs and single photon avalanche diodes (SPADs). Therefore the physical device structures as well as the basic mathematical models and noise performance for APDs

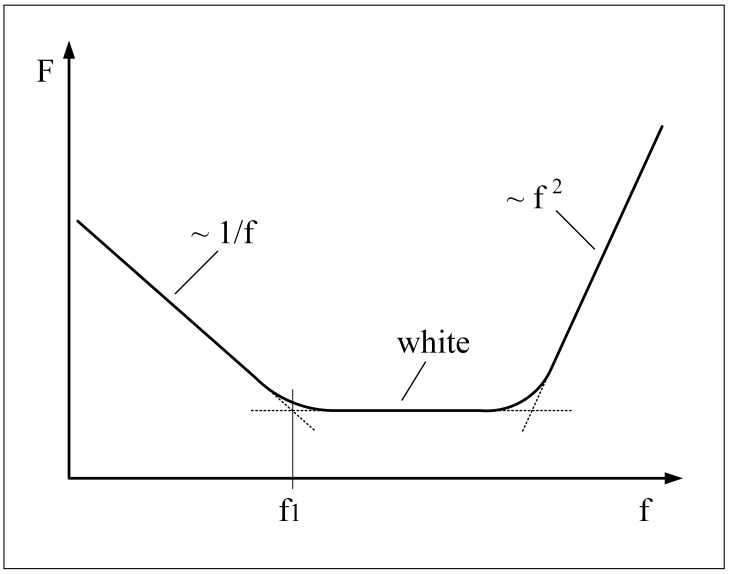
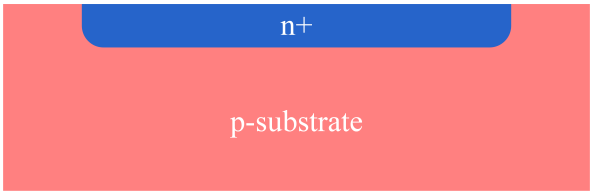


Fig. 1.6: Spectral noise figure, contains three different sections. For low frequencies, flicker noise dominates the spectral noise distribution, until the point f_1, when it gets overruled by white noise at medium frequencies. For high frequencies f^2-noise causes a steep increase of noise.

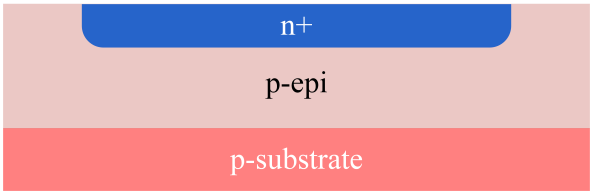
are addressed ([22]).

Probably the simplest way to detect optical power is a basic pn-junction (Figure 1.7a), in which incoming photons can generate electron-hole-pairs (eh pair) in a statistically distributed depth from the semiconductor surface. This so called penetration depth has an exponentially declining characteristic and depends on the wavelength of the incoming light. There are two major phenomena for charge carriers contributing to current flow, drift and diffusion. Drift occurs if the eh pair is generated in the depletion region of the pn-junction. Depending on the charge carrier polarity, a Coulomb-force implies the separation from each other, leading to current flow. If the eh pair is generated outside the depletion region, the charge carrier needs to diffuse into the zone where an electric field can cause a drift. Diffusion apparently is a quite slow process, so for high data rates as well as low recombination probability, it is intended for the majority of the eh pairs, to be generated in the drift zone. A further development, that takes this into account, is the pin photo diode (PINpd) (Figure 1.7b). These devices have an expansion of the drift region, achieved by a low doped p-epi layer, therefore it is more likely for an eh pair to be generated in the drift region. This leads to faster detectors and higher sensitivity because of less time for charge carriers to recombine. But the PINpd also has some disadvantages over its predecessor like e.g. higher resistivity to p-sub. In PINpd, a photon can generate one eh pair which can contribute to the macroscopic current flow,

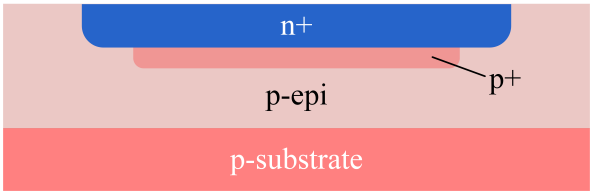
in APDs, however, these charge carriers are accelerated so they can generate new eh pairs through impact ionization. This so called avalanche effect leads to an amplification depending on how much electric field is applied (adjustable over the reverse bias voltage V_{bias}). Figure 1.7c shows a thin p doped layer beneath the n+ layer which leads to an acceleration of charge carriers by an increase of the local electric field. With this internal gain, higher sensitivities can be reached with the same incoming optical power, or gain of the following amplifiers can be traded against bandwidth. In general an APD can operate in two different modes (*linear-mode* and *Geiger-mode*) which is determined by the applied V_{bias}. In the *linear-mode*, where the reverse bias voltage is slightly below the APD's breakdown voltage V_{break}, the relation between optical power and current remains approximately linear. The *Geiger-mode*, where the reverse bias voltage is far above the breakdown voltage, is used for single photon detection and requires additional electronic effort (quenching) for proper operation. APDs that are optimized for *Geiger-mode* are called SPADs. In this thesis an APD, operating in *linear-mode*, is used for optical signal detection.



(a) pn diode



(b) pin diode



(c) avalanche photo diode

Fig. 1.7: Types of diodes for optical detection

Conversion of optical power into an electric current is mathematically expressed [17] by the responsivity R ($[R] = \mathrm{A/W}$), which is a measure for how much current is generated with an amount of optical power. Compared to related devices (e.g. PINpds) APDs have an additional acceleration zone where an applied electric field can cause an avalanche breakdown trough impact ionization. This region is called multiplication zone and its effect on the output current is represented by the multiplication factor M (often also called *gain*). If the device operates in *linear-mode* the gain can be adjusted by how much reverse bias voltage is applied to the diode. The APD current is then calculated by

$$i_{APD} = \underbrace{\overline{P}_{APD} R}_{i_{PIN}} M \tag{1.26}$$

with $\overline{P}_{APD}$ as the received optical power presented in Equation 1.42. The fact that APDs have this additional gain compared to PINpds, make them suit very well to work in conditions were high optical sensitivity is desired. When talking about system performance parameters like e.g. bit error rate (BER), sensitivity or signal to noise ratio (SNR) (all covered in section 1.6), not only circuit noise but also APD noise should be considered. For APDs shot noise and excess noise are the major contributers involved in it's total noise. Shot noise was already covered in Equation 1.9, hence in APDs the current over the junction and therefore noise is amplified by M. Excess noise basically arises with the statistical process of an avalanche breakdown [1] it is described by the excess noise factor F_{EX} and can be expressed as

$$F_{EX} = k_{eff} M + (1 - k_{eff})\Big(2 - \frac{1}{M}\Big). \tag{1.27}$$

It depends on the multiplication and the impact-ionization-coefficient-ratio k_{eff}, which gives the ratio of hole to electron ionization probabilities. Since it is more likely for an electron to be ionized, this factor is < 1. Combining shot and excess noise, the equivalent RMS noise current, generated by an APD, can be determined as

$$i_{n,APD}^{rms} = \sqrt{M 2 q i_{APD} F_{EX} \Delta f}. \tag{1.28}$$

An increase in the multiplication elevates the APD noise, a decrease weakens the photocurrent, so there has to be an optimal multiplication where the maximum sensitivity can be reached. The calculation of the APD noise is presented in subsection 3.2.1.

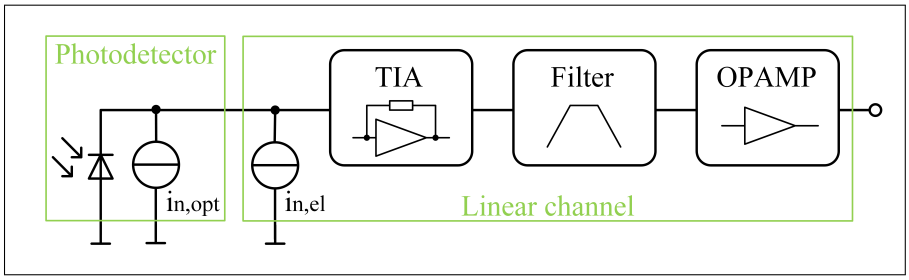


Fig. 1.8: Major components of an opto-electronical receiver.

1.6 Sensitivity of opto-electronical receivers

Like Figure 1.8 shows, a basic opto-electronical receiver system contains two major elements. The photo-detector (e.g. PINpd or APD) is followed by a channel, which includes a TIA and possibly some additional filter and amplifier components. All noise generators in the system are represented by $i_{n,opt}$, containing noise contribution of the photo-detector as well as the optical path, and $i_{n,el}$, describing noise generation caused by the electronic receiver. With the spectral densities of this noise generators at the input ($|i_{n,opt}(f)|^2$, $|i_{n,el}(f)|^2$) and the channel frequency response $H(f)$, the RMS output noise voltage can be calculated by

$$u_n^{rms} = \sqrt{\int_0^\infty \left|H(f)\right|^2 \left[\,|i_{n,opt}(f)|^2 \,|{+}i_{n,el}(f)|^2\,\right] \mathrm{d}f}. \tag{1.29}$$

For digital modulation formats, the RMS output noise voltage can differ for receiving either a '1' or a '0', represented by the notation $u_{n,1}^{rms}$ and $u_{n,0}^{rms}$.

1.6.1 Bit error rate (BER) and signal to noise ratio (SNR)

The BER describes how likely a misinterpretation of the received bit appears in a decision circuit. For example at low SNR, the probability for a '1' to be interpreted as a '0', due to noise causing the signal to overshoot the decision threshold, rises. In [22] the BER is presented as

$$BER = \frac{1}{2} erfc\left(\frac{Q}{\sqrt{2}}\right). \tag{1.30}$$

Q appears as some kind of measure for the ratio between signal and noise, but it is not equal to the basic definition of SNR. It is common to have tables, were important results of this equation are already solved. Introducing the peak-to-peak output voltage v_{out}^{pp}, Q can be expressed by

$$Q = \frac{v_{out}^{pp}}{u_{n,1}^{rms} + u_{n,0}^{rms}}. \tag{1.31}$$

In [22], SNR is defined as the "mean-free average signal power divided by the average noise power", which gives

$$SNR = \frac{(\frac{v_{out}^{pp}}{2})^2}{\frac{1}{2}\left(\overline{u_{n,1}^2} + \overline{u_{n,0}^2}\right)} = \frac{(v_{out}^{pp})^2}{2\left(\overline{u_{n,1}^2} + \overline{u_{n,0}^2}\right)}. \tag{1.32}$$

Comparing Equation 1.31 and Equation 1.32, the relation between SNR and Q for $u_{n,1}^{rms} = u_{n,0}^{rms}$, can be expressed via

$$SNR = Q^2 \tag{1.33}$$

1.6.2 Electrical and optical sensitivity

A key parameter for optical receivers is the sensitivity, it is defined as the minimum signal strength needed to achieve a certain BER. It can either be expressed in an electrical or optical domain. For the electrical sensitivity, the minimum peak-to-peak signal current i_{sens}^{pp} at the receiver input, is of interest. By knowing the midband amplification of the receiver H_0, the output voltages v_{out}^{pp} and v_{out}^{rms} can be converted into corresponding input currents via

$$i_{in}^{pp} = \frac{v_{out}^{pp}}{H_0} \tag{1.34}$$

and

$$i_{in}^{rms} = \frac{v_{out}^{rms}}{H_0}. \tag{1.35}$$

The electrical sensitivity at a certain BER (which can be represented by Q), is achieved by dissolving Equation 1.31, which gives

$$i_{sens}^{pp} = \frac{Q\left(v_{n,0}^{rms} + v_{n,1}^{rms}\right)}{H_0} = Q\left(i_{n,0}^{rms} + i_{n,1}^{rms}\right) \tag{1.36}$$

So by knowing the input referred noise current, the electrical sensitivity for the system can be calculated for specified BERs. Another way to approach sensitivity, especially advantageous for opto-electronical receivers, is to define an optical sensitivity. It also considers the photo-detector via it's responsivity R (introduced in section 1.5), and expresses how much optical power, received by the detector over time, is needed to achieve a certain BER. The optical sensitivity is expressed as

$$\overline{P}_{sens} = \frac{Q\left(i_{n,0}^{rms} + i_{n,1}^{rms}\right)}{2RM}. \tag{1.37}$$

Notice that the responsivity was multiplied by M, to calculate the optical sensitivity for usage of an APD as photo-detector. When using a PINpd for example, the multiplication factor would be omitted.

1.7 Pulse width distortion

The sensitivity specifies the lower border of the input signal so that the receiver reaches a certain BER. But there is also an upper limit for the input signal, from which the BER starts decreasing again [22]. This effect is caused by PWD. It occurs when the operating point of an amplifier is positioned, so that a deflection of the signal reaches into the non-linear range. Figure 1.9 shows how the crossing point of an eye diagram gets distorted by an operating point near the upper limit of the voltage amplifier's linear range. Additionally, the further the input signal reaches into the non-linearity, the higher random jitter gets amplified. When looking at TIAs, a maximum input current, where BER-specifications are still satisfied, can be specified. It is called input overload current i_{ovl}^{pp}, and when operating with an APD as photo-detector, it can be expressed as optical overload power by

$$\overline{P}_{ovl} = \frac{i_{ovl}^{pp}}{2RM}. \tag{1.38}$$

The ratio between sensitivity and overload $\overline{P}_{ovl}/\overline{P}_{sens}$ is called dynamic range. To maximize this parameter, the receiver needs to have a "high" sensitivity and operating points at the center of the linear range, especially for stages were the deflection of the input signal has the same magnitude as the linear range of all amplifiers.

1.8 Transmission setup

For proper application, it is crucial to define a geometrical operating range for the system to work in. Figure 1.10 shows the setup of the OWC path and it's geometrical parameters. Due to safety reasons in terms of eye damage, the transmitting power $\overline{P}_{tr}$ of the RCLED is limited to 1 mW. The light intensity at the receiver (I_{APD}) is calculated by

$$I_{APD} = \frac{\overline{P}_{tr}}{A_r} \tag{1.39}$$

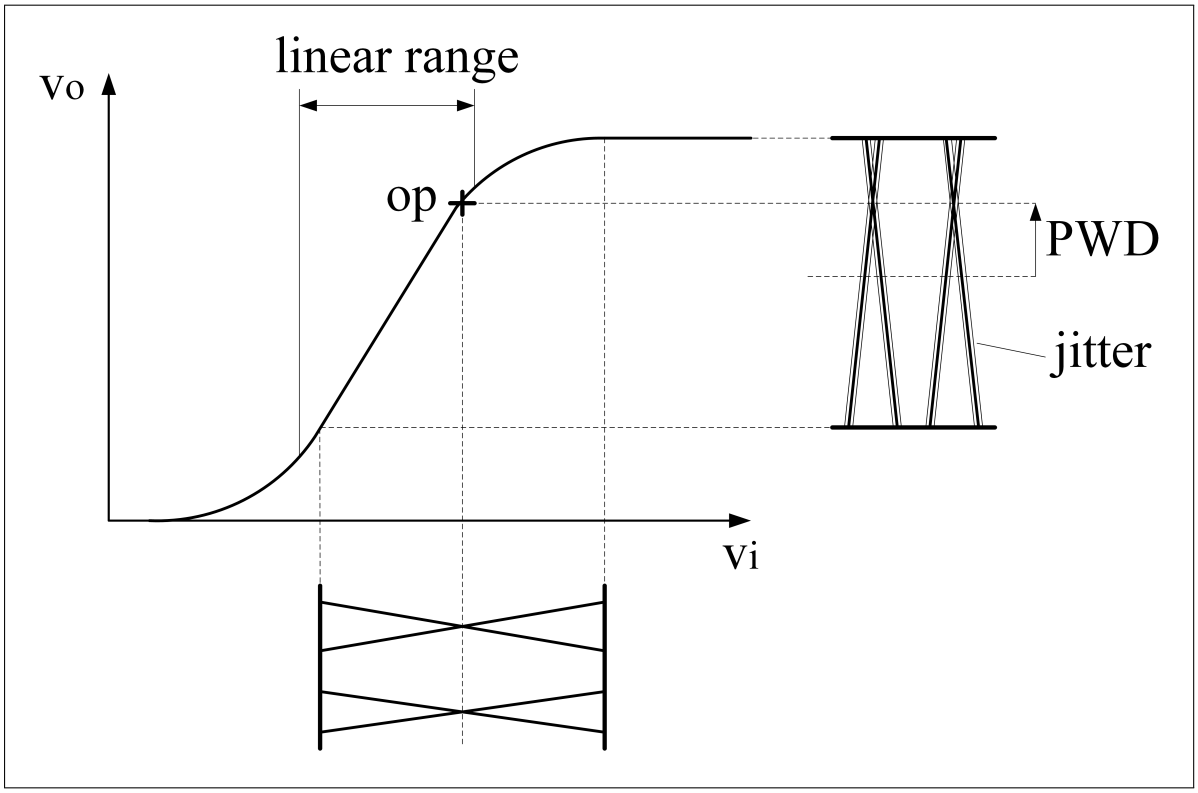


Fig. 1.9: Appearance of pulse width distortion and amplification of random jitter, when the input signal deflection reaches into the non-linear range of an amplifier.

using

$$A_r = \Omega r^2 \tag{1.40}$$

and

$$\Omega = 4\pi \sin^2\left(\frac{\alpha}{4}\right) \tag{1.41}$$

with the area of a spherical cone segment A_r and its aperture angle α which depends on the used RCLED but could also be varied via some additional optical setup. The power, received from the APD, is calculated by its area A_{APD} and the light intensity at the distance to the RCLED, which is expressed by

$$\overline{P}_{APD} = I_{APD} A_{APD}. \tag{1.42}$$

In operating circumstances the received power of the APD will have two different values for receiving either a '0' or a '1'. The relation between them is called extinction ratio $E_R = \frac{P_{APD1}}{P_{APD0}}$. $\overline{P}_{APD}$ describes the mean value of these symbol-related power values. The distance r to reach the desired mean APD power is given by

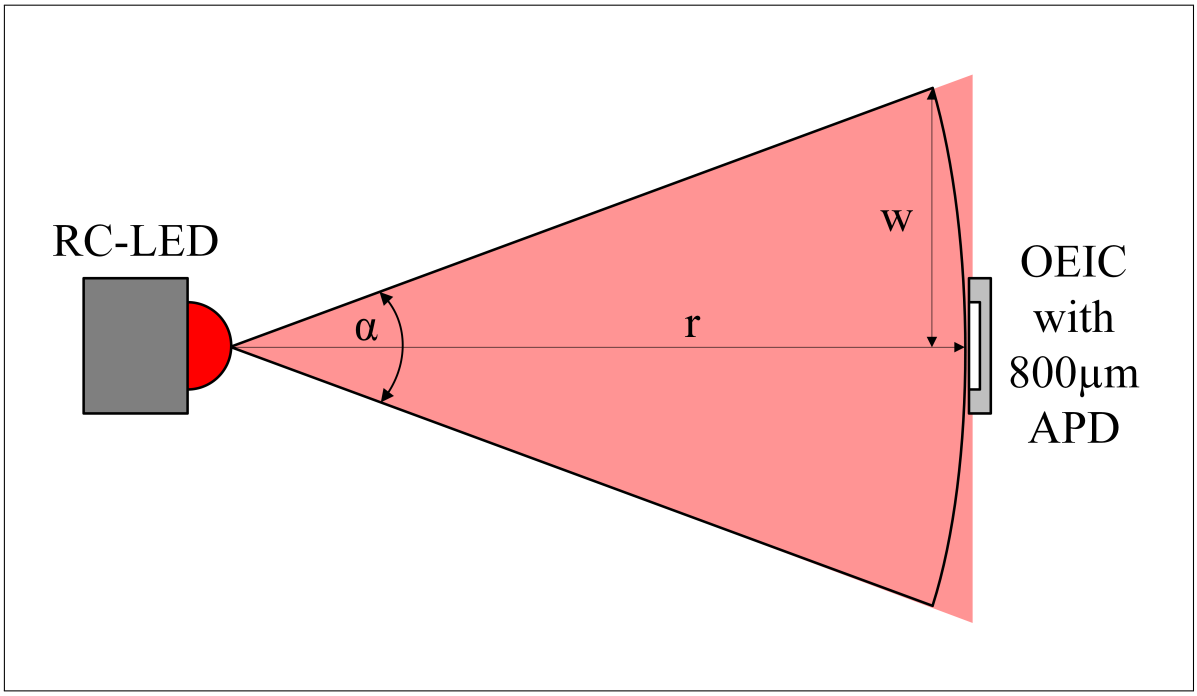


Fig. 1.10: Important parameters for calculating the operating distance.

$$r = \sqrt{\frac{\overline{P}_{tr} A_{APD}}{\overline{P}_{APD} 4\pi \sin^2(\frac{\alpha}{4})}}. \tag{1.43}$$

The target is to have high enough light-cone radius w at the maximum operating distance, so that aligning of the transmission path gets facilitated easily. This value can be calculated by

$$w = \tan(\alpha) r_{max}. \tag{1.44}$$

Concrete values for the operating distance of the proposed receiver system will be calculated in chapter 3.

1.9 TOSLINK standard

TOSLINK is a standardized optical connection system based on the IEC-60958 specification. It brings along the advantages of optical fiber communication like the electrical potential isolation between the transmitting and receiving circuit and the insensitivity against electromagnetic disturbances. The electrical pendant to TOSLINK is called Sony/Phillips-Digital-Interface (S/PDIF).

1.9.1 IEC-60958 digital audio interface (DAI)

To make interconnection of different digital audio equipment possible, it is crucial for developers to agree on a communication interface. The IEC-60958 interface is specified in a bundle of four documents ([10], [11], [12] and [13]), it works serial, unidirectional as well as self-clocking, and is intended to contain monophonic or stereophonic audio information, encoded using linear pulse code modulation (PCM) with a resolution of up to 24 bits per sample. It is divided into blocks containing 192 frames of which each one of them contains two sub-frames. In the following section these elements will be described in more detail.

Figure 1.11 shows the structure of a sub-frame. The first four bits are the preamble which provides for synchronization and identification of the frames and blocks. Figure 1.12 shows, amongst the frame format, three different characters of preamble code. 'B' indicates the start of a new block, 'M' the start of channel 1 and 'W' the start of channel 2.

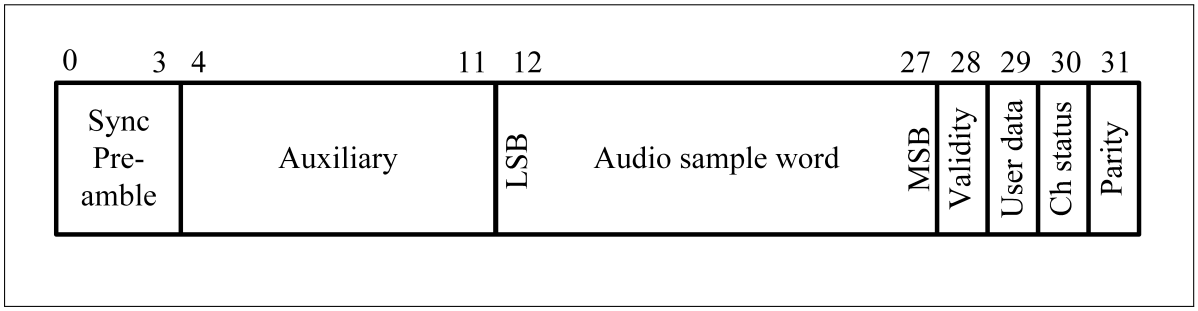


Fig. 1.11: Sub-frame format of the IEC-60958 standard, especially for a 16 bit coded audio signal.

The length of the auxiliary section depends on how much bits are required for the audio sample word, and is calculated by the difference of the used word-length to the maximum word-length. In Figure 1.11 the used sample word-length is 16 bit, so the size of the auxiliary section is 8 bits. The following bit is called validity bit and it is logical '0' if the information in the main data field is reliable, usually it is used in nonlinear PCM application to prevent accidental decoding of data before a complete channel status block is received. The user data bit can be used in any way required by the user. The channel status bit adds some additional information associated with the channel transmitted in the sub-frame. For DC minimization over the transmission line, as well as to facilitate clock recovery and make the interface insensitive to the polarity of connections, the bits 4 to 31 are encoded in biphase-mark.

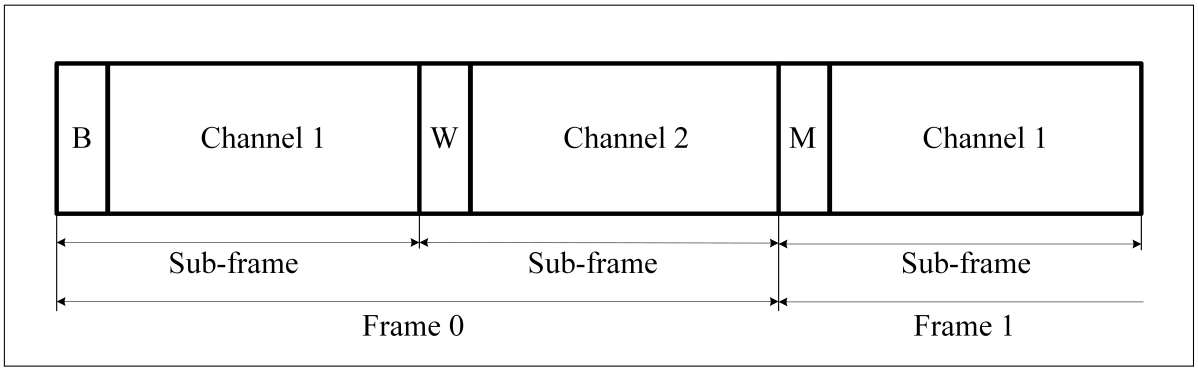


Fig. 1.12: Frame format of the IEC-60958 standard

1.10 State of the art fully integrated APD receivers

There has already been a high number of research and publications done on the topic of fully integrated APD receivers with APDs of different sizes. Optical receivers often work with a TIA for conversion from photo-current into a voltage signal and with additional amplification stages to achieve the right output level. In [3], P. Brandl and colleagues used a 100 µm CMOS compatible APD together with a receiver chip, connected via bond wires, to build an opto-electronical receiver system. This design achieved optical sensitivities of −31.8 dBm and −32.2 dBm for 2 Gbit/s and 1 Gbit/s, specified at BER = 10^{-9}. They approached the problem of sensitivity to ambient light with a differential ("dummy") path and a feedback loop. The path contains a "dummy-TIA", only working as a reference for the differential voltage level. The principle of the ambient light cancellation is to alter the input current of the "dummy-TIA" in dependence of the offset voltage between the differential paths. Some other approaches to reach a high background light immunity are presented in [22]. A big step towards cheap and robust opto-receiver solutions is reached by integrated APD receivers. In [15] and [2] a full integration of a 200 µm APD, together with the receiver circuitry on the same chip, was achieved. [15] used the same background light cancellation (BLC) method as [3] but achieved slightly better sensitivity (−32.2 dBm @ 2 Gbit/s for BER = 10^{-9}). [2] implemented a BLC method, where the offset was sensed directly after the TIAs, instead of after the limiting amplifiers. This design resulted in slightly less sensitivity (−31.8 dBm @ 1 Gbit/s for BER = 10^{-9}). In [16] and [20] larger APDs (400 µm) were implemented. By doubling the APD diameter, they estimated a drop in the receiver sensitivity by 1.25 dB, but this means also a four times larger light collecting area. So the irradiance needed, drops by 4.75 dB, which leads to an increase of transmission distance. In [20], they achieved −30.6 dBm @ 2 Gbit/s for BER = 10^{-9}. In his dissertation [14], T. Jukic tried a different BLC feedback principle than mentioned

up above, one were not the current flowing into the “dummy-TIA” but the “signal-TIA” is controlled. In [19], they implemented a 600 µm APD and achieved a versatile system that operates with high dynamic range of up to 25.88 dBm by the possibility to vary the transimpedance. The receiver circuit, designed in this thesis, will be based on a method presented in [14]. BLC will be accomplished by controlling the DC current at the TIA input. The advantages and disadvantages, arising with this feedback structure, are addressed in section 2.5. As photo-detector, a 800 µm APD will be used. The initial plan for this thesis was to optimize existing components to the bandwidth necessary for TOSLINK applications (~ 5 Mbit/s) and for usage of the large diameter APD, as well as designing a sufficient output circuitry to reach digital output levels. But the early simulations revealed that many redesigns of major components (TIA, Differential Amplifiers) needed to be done, more details for the reasons and the solutions can be found in the corresponding sections in chapter 2.

Chapter 2

Circuit design

2.1 Process technology

The semiconductor fabrication process, chosen for this thesis, is the "XO035" from XFAB [6]. It's a 0.35 µm BiCMOS p-substrate process, especially applicable for optical applications. The main supply voltage domains for the provided devices are 3.3 V and 5 V, the proposed chip is designed for $V_{DD} = 3.3\,\mathrm{V}$. An important feature of this process, is the possibility to realize opto-windows over the n+ cathode implants of the used APDs, which prevent Bragg-reflections of incoming light. Besides, a major capability is to embed circuit parts into a *deep-nwell*, enabling to apply very high negative voltages at the p-substrate (by forming a pn-junction in reverse direction). This allows the operation of APDs in linear mode, which demands to bias the device slightly below it's breakdown voltage. Typical values for the used devices in this thesis are about $V_{break} \approx -30\,\mathrm{V}$.

2.2 Circuit structure

Opto-electronic receivers, for digital communication, can basically be divided into three elementary blocks [22].

- **A photo-detector** acts as a signal source for the circuit and converts a received optical signal into electrical current.
- **A linear channel**, were the first component is a TIA, that converts the photo-current into voltage. It can be followed by numerous voltage-amplifier stages, setting the specified output level. Furthermore, through additional filter components, the frequency response of the receiver can be adjusted.

- **A decision circuit** compares the output voltage to a certain reference voltage and decides whether a '1' or a '0' was received.

The chip, designed in this thesis, contains a fully integrated APD with circuitry to produce digital output levels. The decision circuit needs to be done off-chip, but there are already excellent systems, optimized for DAIs, available on the market. The following part will give a brief introduction into the theory of the receiver's operation.

The field of application intended for this receiver is OWC. Hence environmental influences like sensitivity to background light adding up to the signal, as well as temperature effects, affecting the operation point of the APD or other receiver components, need to be considered. In [22] many different techniques to implement background light cancellation are presented. The principle is, to add an additional "*dummy*-path", that works just as a reference for the signal path. By applying feedback with high-pass characteristic and adding a method to influence one of the two paths, an offset cancellation loop (OCL) is achieved. It is capable of canceling DC-offsets, appearing for example within process variations or at temperature fluctuations during operation. Also slow changes on the signal, appearing with slow changes on environmental light, can be compensated. A design that was proposed by [14], is also used for this receiver. The function block corresponding to the OCL is marked green in Figure 2.1. The principle is, to control the gate voltage of a p-MOS transistor (M_{OCL}) in dependence of the offset between the inputs of an operational transconductance amplifier (OTA). If background light causes an increase in the photo-current, it will be recognized by an offset voltage at the OTA input. This reduces the gate potential of M_{OCL}, which results in lower channel resistance and a discharge of photo-current. If the lower cut-off frequency of this feedback filter is chosen properly, it has no effect on the fast signal changes. It can be manipulated off-chip by external capacitors (C_{EXT1}, C_{EXT2}). Detailed information about the OCL design is covered in section 2.5. The yellow marked part in Figure 2.1, represents the function block of the signal generator. It contains three devices, the signal-APD (SiAPD), the reference-APD (RAPD) and a dummy capacitor (C_{dummy}). The SiAPD is used as photo-detector, delivering photo-current for the receiver. The RAPD, however, is just used to implement an off-chip gain control circuit for the SiAPD, both are intended to have the same breakdown characteristics. C_{dummy} is used to model the capacitance of the SiAPD, making the *dummy*-path experience the same impedance-coupling to substrate. In conjunction with the ability of differential paths, to suppress common mode noise, a symmetrical coupling makes the receiver insensitive to substrate noise. The design and considerations regarding the signal generator function block is covered in section 2.4. Moving on to the amplifiers contained in the receiver, the first

stage is the TIA, marked blue in Figure 2.1. It is optimized in terms of noise behavior and has an exact replica working in the dummy path, the dummy transimpedance amplifier (DTIA). Design and simulation of this stage is covered in section 2.3. The next component in the amplifier chain is a source follower in both paths. It is used to reduce load effects on the TIA caused by following stages, like the fully differential operational amplifier (FDA). Marked red, in Figure 2.1, this function block adds additional gain to the differential signal. The output voltages of the FDA determine the upper limit of the linear dynamic range, which means the maximum photo-current, that can be amplified, before getting distorted by nonlinearities of an amplifier stage in the receiver. High sensitivity of the output common mode voltage V_{com} (describes the merged common mode voltage of V_{com1} and V_{com2} after the offset was canceled) to process variations, led to an implementation of common-mode feedback (CMFB). This enables to trim V_{com} during operation, via an external voltage V_{CM}. This was implemented to address the problem with PWD, presented in section 1.7, so that the maximum dynamic range can be achieved even when slight process variations appear. The FDA is covered in section 2.6. Marked violet, in Figure 2.1, represents the output circuitry of the receiver. It is realized with an OTA, converting the differential to a single ended signal, which is then fed into an output driver, capable of driving loads applied to the receiver's output.

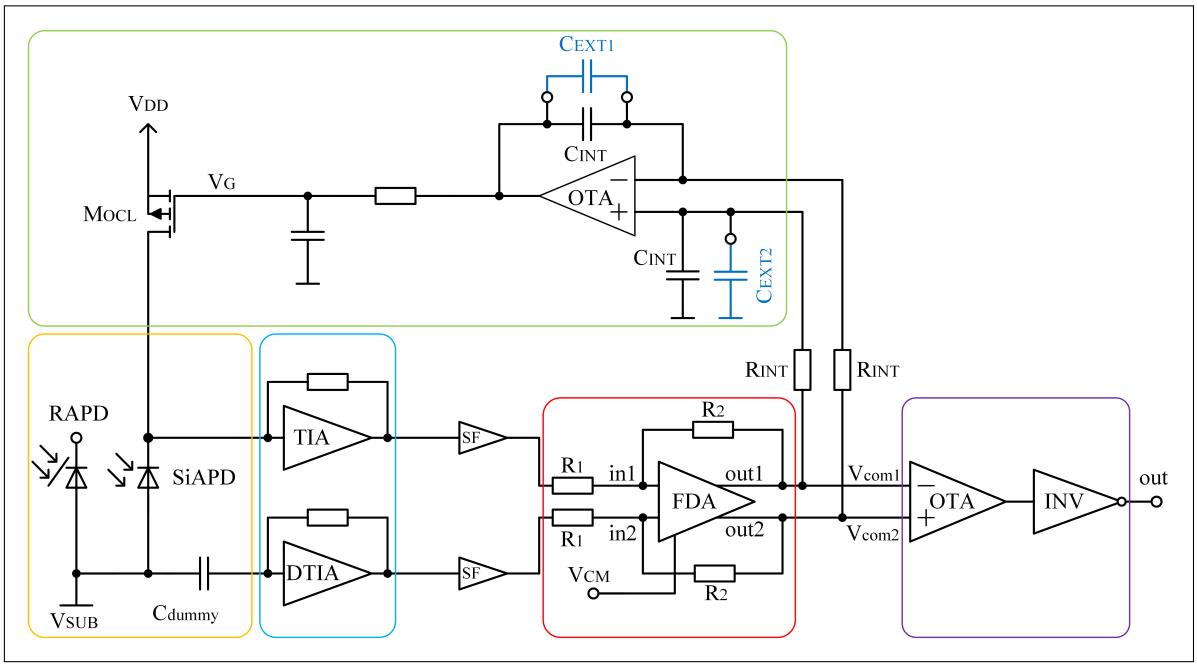


Fig. 2.1: Circuit structure of the proposed opto-electronic receiver, divided into function blocks, marked by colors. Yellow ... signal generator, blue ... TIA, red ... FDA, violet ... output circuitry, green ... OCL.

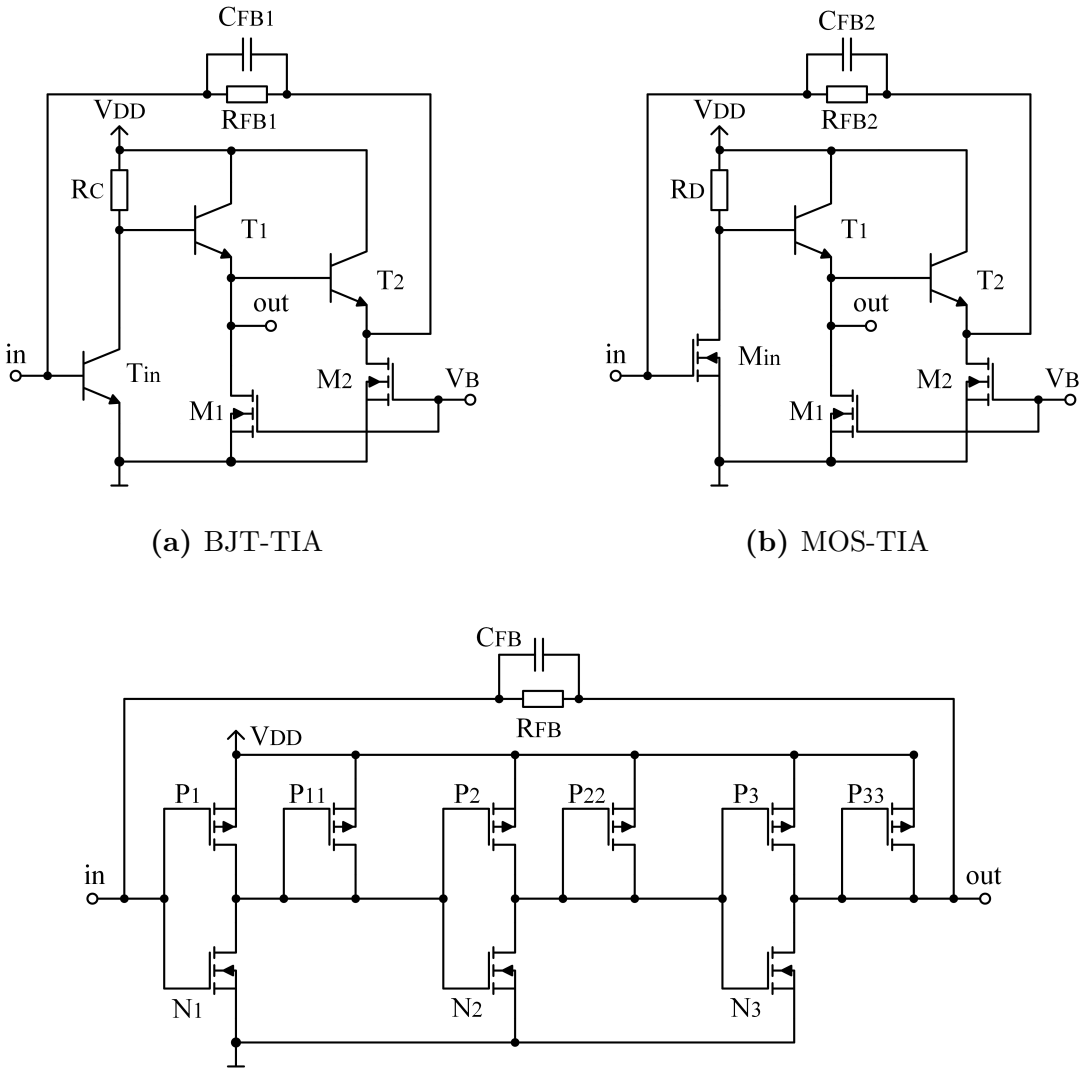
2.3 Transimpedance amplifier (TIA)

The TIA is probably the most important receiver component in terms of achieving the specified sensitivity and BER. As it is the first stage in an amplifier chain, it's noise performance has a dominant impact on the total noise (shown in subsection 1.4.4), which means that efforts in optimizing this component pay off. Especially the front-end transistor of a TIA needs to be carefully selected, matched to the application circumstances like DR and signal source. The sensitivity of an opto-electronical receiver is determined by the input referred noise, which needs to be as low as possible. Mentioned in section 1.10, the optimization of a high speed TIA ([19]) for a lower DR and larger APD should be investigated in the first place. There, a BJT front-end TIA was used, for application of up to 2 Gbit/s. At high DRs, BJTs perform much better in terms of noise than MOSFETs, due to their large transit frequency. However for lower frequencies, flicker noise becomes more important, were MOSFET front-ends perform the best (shown in subsection 1.4.6). Especially for high internal resistances of the signal generator, as it is the case for APDs, the flicker noise cut-off frequency is pushed further downwards. By knowing that, it is fair to say that just scaling the 2 Gbit/s BJT TIA down, will not be the best achievable solution, at least in terms of input referred noise. To estimate what value of input referred noise can approximately be expected, by scaling a TIA, [22] evaluates the scaling factor to somewhere between BW^1 and $BW^{1.5}$. That means if the referenced receiver has $i_n^{rms} = 270\,\text{nA}$ @ 1 GHz, an input referred noise of between 270 pA and 2.7 nA @ 10 MHz can be expected for the scaled one. However this is only a rough estimation, but it shows in which order of magnitude the values should appear. The scaling of a TIA's bandwidth can basically be done by varying the feedback resistor R_{FB} (see Equation 1.4). Since the GBW is constant, this also goes with scaling the transimpedance into the opposite direction (see Equation 1.2). If an increase in GBW is intended, also the circuit needs to be redesigned rather than just varying R_{FB}.

2.3.1 Comparison of three TIA circuits

In the following part, three different TIA circuits will be presented. Further on, the design of the TIA, used for this thesis's receiver, will be discussed in detail. All three circuit variants will be compared due to simulations on their noise spectrum as well as transimpedance.

In Figure 2.2, the three different TIA circuits are depicted. 2.2a shows the structure used in [20] and [19] with a BJT front-end, followed by a common collector stage



(a) BJT-TIA **(b)** MOS-TIA

(c) INV-TIA

Fig. 2.2: Investigated TIA circuits, a) and b) differ mainly by their front-end transistors. c) is carried out with three inverter stages, this structure was chosen for the implemented TIA in this thesis.

(emitter follower). In 2.2b the front-end transistor was replaced with a MOSFET, having the intention to achieve a lower flicker cut-off frequency at low bandwidths. For both circuits, the feedback network is realized by another common collector stage followed by a resistor and a capacitor in parallel. The feedback capacitance is primarily used to reduce gain peaking in the frequency response [20]. 2.2c shows a circuit based on an inverter chain (presented in [28]), aiming to achieve even lower flicker cut-off at very high transimpedance. For negative amplification, which is necessary at shunt feedback TIAs, there need to be an odd number of consecutive inverters. Every stage in this chain acts as a push-pull transconductor (P_i, N_i), while being loaded with a

	INV-TIA
W_{P1}	240 μm
W_{P2}	27 μm
W_{P3}	27 μm
W_{N1}	60 μm
W_{N2}	10 μm
W_{N3}	10 μm
W_{P11}	15 μm
W_{P22}	15 μm
W_{P33}	15 μm
L	1 μm
R_{FB}	120 kΩ
C_{FB}	10 fF

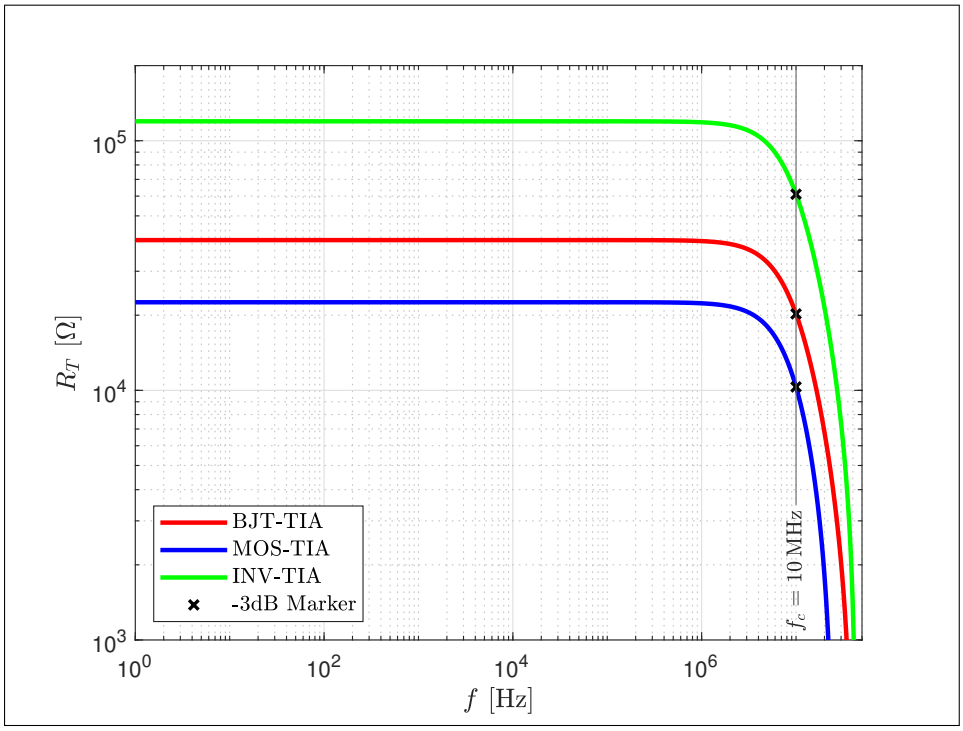
(a)

	BJT-TIA	**MOS-TIA**	**INV-TIA**
$R_{T,DC}$ [kΩ]	39.81	22.45	119.1
$i^{rms}_{n,TIA}$ [nA]	9.557	3.74	2.276

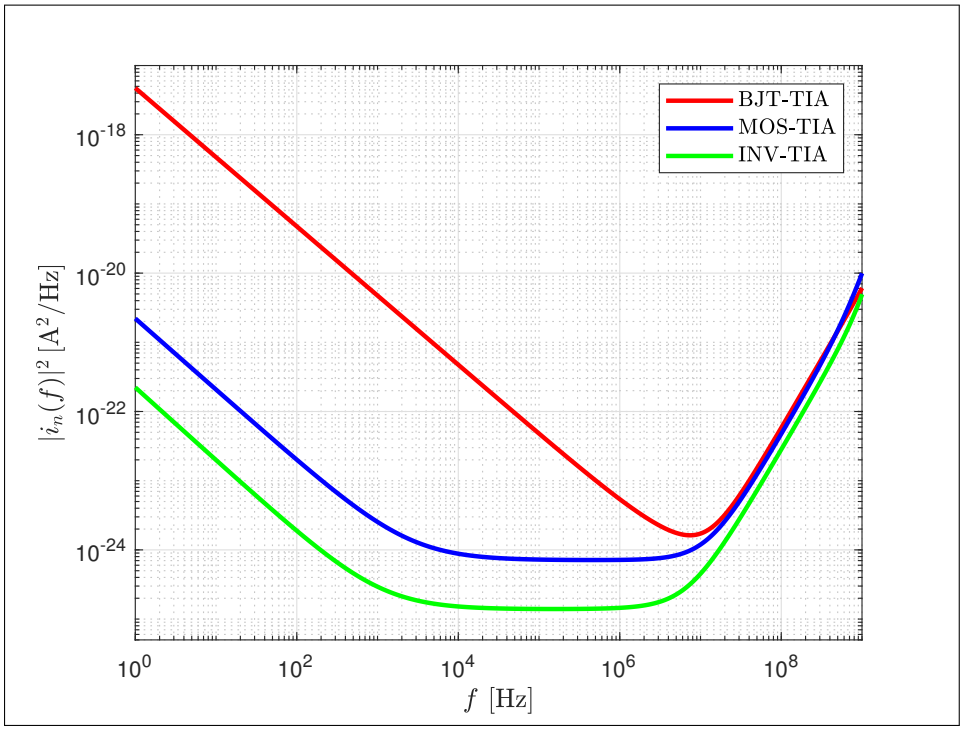
(b)

Tab. 2.1: a)Design parameters for the implemented inverter TIA, W stands for the transistor width, L for the gate length. b)Simulated circuit parameters for three different TIA designs.

diode formed by a p-MOS transistor (P_{ii}). Each stage adds additional DC gain of about $(g_{m,Ni} + g_{m,Pi})/g_{m,Pii}$ [22], parameters that can be controlled very well by the transistors geometries. In [23], the major noise contributers in this three stage inverter TIA were analyzed. While neglecting flicker noise, they showed that the input referred noise depends mainly on the noise of the first inverters and the feedback resistor. Equation 1.8 shows, that noise of the feedback resistor can be decreased by high values for R_{FB}. This suits perfectly to the high GBW of this inverter based TIA, when scaling it to low frequencies. Additionally, as it was shown in subsubsection 1.4.5.1, the flicker noise factor k_f for MOSFETs scales by $\sim 1/L^2$. Meaning for large Transistors at the first inverter stage (P_1, N_1) the flicker cut-off frequency decreases. Despite that, the inverter front-end shows even better noise performance compared to a single MOSFET front-end with resistive load. The reason for this is, that the noise, generated in the channel, is divided by the transconductance, when referring it to the input. For a single transistor amplifier the noise consists of a part generated by the load resistor and the channel noise, while being divided by the transconductance of one transistor. But for an inverter amplifier both input transistors contribute to the total transconductance, which is much



(a) Transimpedance for BJT front-end, MOSFET front-end and inverter TIA.



(b) Input referred noise for BJT front-end, MOSFET front-end and inverter TIA.

Fig. 2.3: Comparison of different TIA circuits in terms of transimpedance and noise spectrum.

larger compared to a single transistor amplifier. To make comparison of the proposed TIA circuits possible, each one of them was globally optimized with SPECTRE to a bandwidth of 10 MHz. The component values and transistor sizes for the *INV-TIA* are listed in Table 2.1(a). Since the other TIA circuits were not implemented in the final receiver, their design parameters are presented in the Appendix A.2.

Figure 2.3a shows the frequency dependent transimpedance R_T for all TIA types. The TIA is the first amplifier stage in the designed receiver, therefore it is beneficial in terms of the total noise figure, if it has a high amplification (see subsection 1.4.4). High transimpedance implies also high values for R_{FB} which decreases thermal noise contributed by the feedback resistor. So in terms of noise minimization, TIA designs with high transimpedance should be striven. That leads to superiority of the *INV-TIA* (with $R_{T,DC} = 119.1\,\text{k}\Omega$) over the *BJT-TIA* ($R_{T0} = 39.81\,\text{k}\Omega$) and *MOS-TIA* ($R_{T,DC} = 22.45\,\text{k}\Omega$). However, what affects the total receivers sensitivity the most will be the input referred RMS noise current i_n^{rms}. As subsection 1.4.6 shows, TIAs with MOSFET front-end are expected to have drastically lower flicker cut-off frequency, when operating with photo-detectors as sources and at low DRs. Looking at the spectral input referred noise densities, depicted in Figure 2.3b, one can see a difference of about three decades. While for the MOSFET front-end circuits, the white noise starts dominating the noise contribution at about 5 kHz, for the *BJT-TIA* this happens at approximately 10 MHz, were already the $\sim f^2$ noise kicks in. Further comparison of the two MOSFET front-end TIAs shows less white noise for the *INV-TIA* than for the *MOS-TIA*. This can be explained by several phenomena. First the transconductance of a complimentary inverter stage, which is much higher than that of a single transistor amplifier, leading to fewer channel noise when referring it to gate. Second the transimpedance can be pushed higher, which enables usage of high feedback resistance and therefore reduces thermal noise, produced by R_{FB}. Integrating the spectral input referred noise density over f, leads to an input referred RMS noise current of $i_n^{rms} = 9.557\,\text{nA}$ for the *BJT-TIA*, $i_n^{rms} = 3.74\,\text{nA}$ for the *MOS-TIA* and $i_n^{rms} = 2.276\,\text{nA}$ for the *INV-TIA*. Reminding the estimations for bandwidth scaling, taken at the beginning of the chapter, the input referred noise should be between 270 pA and 2.7 nA when scaling to a bandwidth of 10 MHz. This estimation is exclusively met by the *INV-TIA*, which will be used as the implemented design for the receiver in this thesis. All simulated circuit parameters for the compared circuits are summarized in Table 2.1(b).

When adding the offset cancellation loop, presented in section 2.5, the receiver will have bandpass characteristic, which adds a lower cut-off frequency to the receiver's response.

So i_n^{rms} will be further reduced by embedding the TIA into the receiver circuit. To implement the pseudo differential path, a replica of the signal TIA will be used as front end for the *dummy-path*, more on that will be discussed in subsection 2.4.1.

2.4 Signal-APD and reference-APD

In the design, two different sized APDs, sensitive for optical wavelengths of 675 nm were used. The main device is carried out with a 800 µm diameter and is used for signal detection (SiAPD), the second one (RAPD) works just as a breakdown voltage reference. It's purpose is to implement an off-chip automated gain control (AGC) circuit for biasing the SiAPD. Since the breakdown voltage has a temperature dependency (strongly decreases with decreasing temperature [9]), the reverse bias voltage needs to be controlled to keep the APD gain constant. Therefore it is crucial, for both devices, to experience an identical temperature environment, which leads to the decision to integrate them on the same chip, placed close together. For this application, no signal is required at the RAPD and it is kept in *dark-mode* by covering it with a metal layer. Another benefit that would arise with implementing an AGC is an increase of the receiver's dynamic range. This could be explained when looking at Equation 1.38, the optical overload power is inverse proportional to the APD gain M. So by reducing the gain, more optical power can be sustained before the receiver is overloaded and therefore the dynamic range increases. Besides identical temperature environment, the different sized APDs also need at least similar breakdown voltages. The easiest way to achieve this would be to use a second 800 µm device, but that would occupy large chip area. Hence to save space, the RAPD needs to be as small as possible while having sufficient similarity in breakdown voltage to the implemented SiAPD. Figure 2.4 shows simulations of APD characteristics, performed for different device diameters. Since i_{APD} scales with the active APD area, a comparison of the breakdown voltages becomes possible by considering a scaling factor. V_{break} for APDs with more than 80 µm seem to change only slightly when increasing the device diameter. The definition for the breakdown voltage, chosen in this thesis, is the point where 10 µA in dark mode are exceeded for a 100 µm APD. When applying this definition to the simulated data in Figure 2.4, $V_{break,100} = -29.55\,\mathrm{V}$ The scaled dark current for different device diameters, is determined by

$$i_{dark} = i_{ref}\left(\frac{d_1}{d_{ref}}\right)^2. \tag{2.1}$$

Calculated for a diameter value of 80 µm, this leads to $i_{dark,80} = -6.4\,\mu$A and $V_{break,80} = -29.81$ V. For the 800 µm SiAPD, this scaling law would result in $i_{dark,800} = -640\,\mu$A and $V_{break,800} = -29$ V. However when looking at the simulations in Figure 2.4, the breakdown voltages of the 800 µm and 100 µm devices are much closer to each other than what was calculated by the scaling estimation. For the 80 µm APD the scaling fits quite well, it has a slightly higher breakdown voltage than the 100 µm device. This led to the decision, to choose the 100 µm diameter for the RAPD, instead of the smaller 80 µm device. However this simulation results in quite high i_{dark} at low bias voltages of about 50 nA @ $V_{bias} \approx -1$ V. Measurements performed on APDs in this process, found in the literature ([7], [5], [27]), showed uniformly much fewer dark currents in the range of 1 pA to 100 pA. This implies that measuring the dark current of the RAPD, in terms of achieving AGC, will be challenging, due to the range of discrete component's leakage currents. Although the absolute current values of this simulation can't be taken directly, it should give a good measure for comparison of the breakdown voltages for APDs with different diameters.

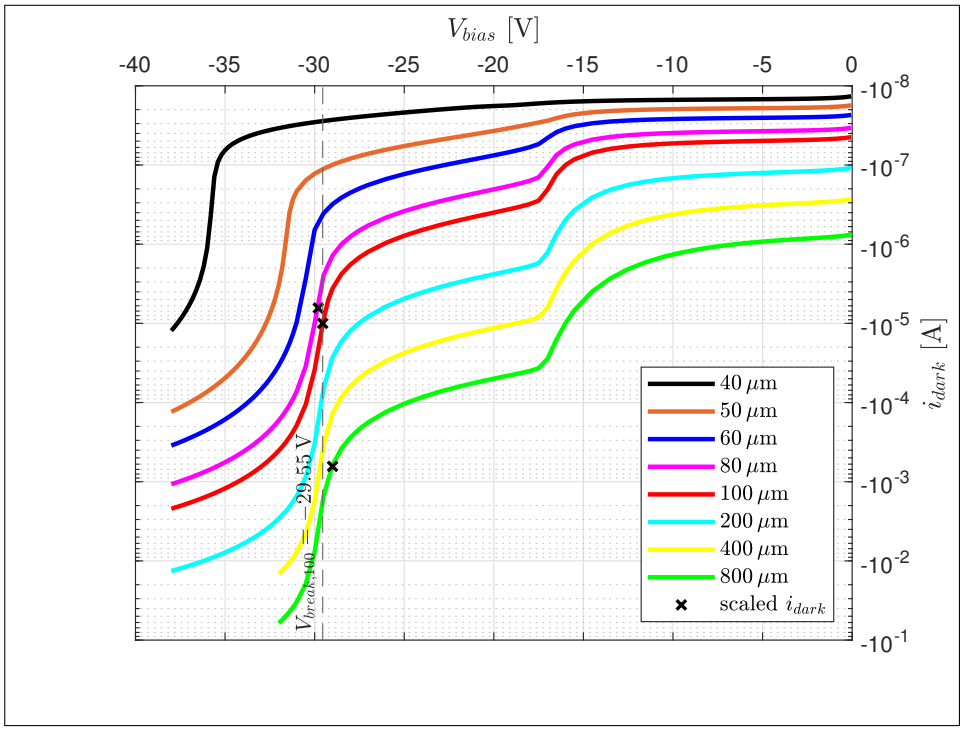


Fig. 2.4: Simulation of the breakdown voltage for different APD diameters. The black markers indicate the scaled values for i_{dark} and the resulting V_{break}, this scaling model seems to fit only for small APD diameters.

Figure 2.5 shows the crosssection of the implemented APDs, with slight improvements compared to the device in Figure 1.7c. Also metal contacts are shown, which are arranged concentric and serve as interface for connecting anode (A) and cathode (C)

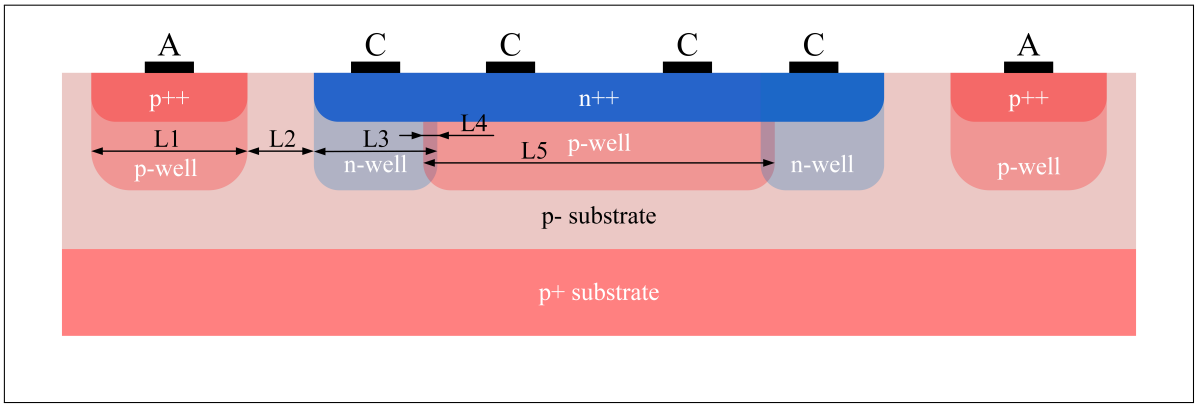


Fig. 2.5: Cross-section of an APD in the used 0.35 µm BiCMOS process.

to the electronic receiver circuit. The most important physical dimensions of the used devices are summarized in the Appendix. Depending on the APD diameter, it becomes necessary to apply more than one coaxial metal rings for the cathode contact in order to reduce series resistance in the large n++ region.

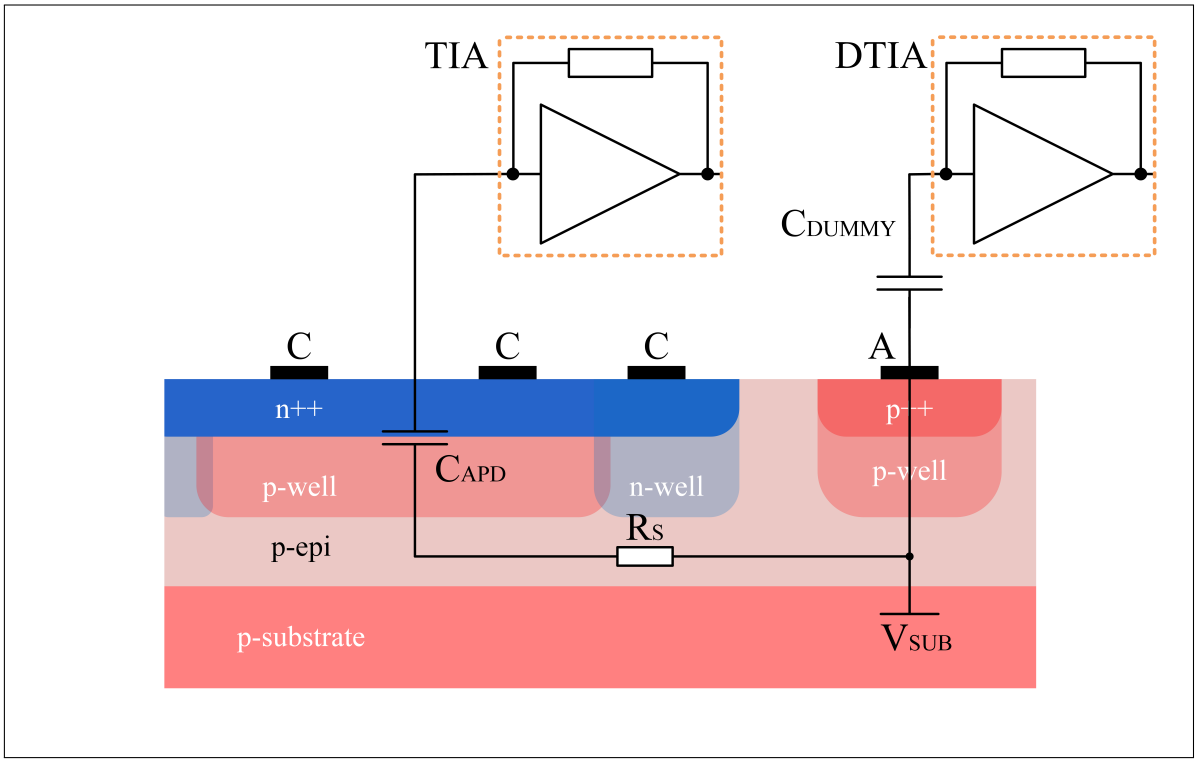


Fig. 2.6: Parasitic capacitance C_{APD} and resistance R_S appearing with APDs.

2.4.1 Parasitics within physical APD layout

As discussed in section 1.10, it is well known what system performance can be achieved with fully integrated 100 µm to 400 µm diameter APDs. But what can be expected when using a 800 µm device? As mentioned before, i_{APD} is intended to scale with area, or $\sim (d/2)^2$, but so do parasitics. Meaning that there is a certain increase in APD capacitance. Figure 2.6 shows schematically how this can be modeled in the APD cross section. C_{APD} describes the parasitic capacitance between cathode and the p-substrate. The value for an 800 µm device is estimated to about 7 pF ([18]). As shown in [22], high photo-detector capacitances increase f^2-noise when operating as signal sources for TIAs, so that it starts dominating the noise spectrum at lower frequencies. The simulations, performed in Figure 2.3b, were carried out with $C_{APD} = 7\,\text{pF}$ and showed an increase of f^2-noise at about 10 MHz. Since the bandwidth of the receiver is going to be less than that, the high value for C_{APD} should not affect the input referred noise notably. But there is another factor that needs to be considered with high photo-detector capacitance. Large C_{APD} leads to a noteworthy coupling from chip substrate to the TIA input, so noise or disturbances could be added to the received signal. This effect can be compensated by the circuit's pseudo differential path, carried out with the DTIA. In principle it should deliver a DC voltage reference for the OCL to cancel offset voltages between signal- and reference-path. In addition to that, benefits of differential ended communication like common-mode noise suppression, can be utilized. The idea is to have the same dimension of coupling to substrate like the TIA has it via C_{APD}. In that case, substrate noise or ringing would have no effect on signal quality because they get canceled by the differential path. This identical coupling is achieved by placing a capacitor (C_{dummy}) with the same value as the estimated parasitic APD capacitance, at the input of the DTIA. The amount of coupling can be described by the reactance, it is calculated by

$$X_{APD} = X_{dummy} = \frac{1}{\omega C_{APD}} \tag{2.2}$$

with ω as the frequency at which noise or ringing appears. DC reference paths often have low-pass filters at their outputs to minimize their noise generation. In this case it is crucial for the DTIA to have exactly the same alternating current (AC) characteristics as the TIA, because for example lower bandwidths would also filter the coupled disturbances and the benefit of using the differential path would fail to appear. Another parasitic effect expresses in a series resistance R_S between the substrate contact and the p-well beneath the cathode. This slightly increases the impedance seen by the

substrate against the cathode by a frequency independent part, so the real impedance is expressed by

$$Z_{APD} = X_{APD} + R_S \tag{2.3}$$

This means for designing the dummy capacitance, an additional resistor, with similar value to the parasitic resistance, could be placed for better performance. The problem is, that R_S is unknown and could only be estimated to a few Ohm [25], furthermore the value of C_{dummy} has a certain variation due to the production process. In the APD layout, additional metal rings over the cathode were applied to decrease R_S as much as possible. This led to the decision to omit a serial resistor in the design. The best way to guarantee identical coupling into both paths would be, to use a second 800 µm APD in dark-mode, which has the same parasitic capacitance and resistance as well as the same breakdown voltage. But the disadvantage and reason why it was not used in this application is the gigantic chip area it would occupy.

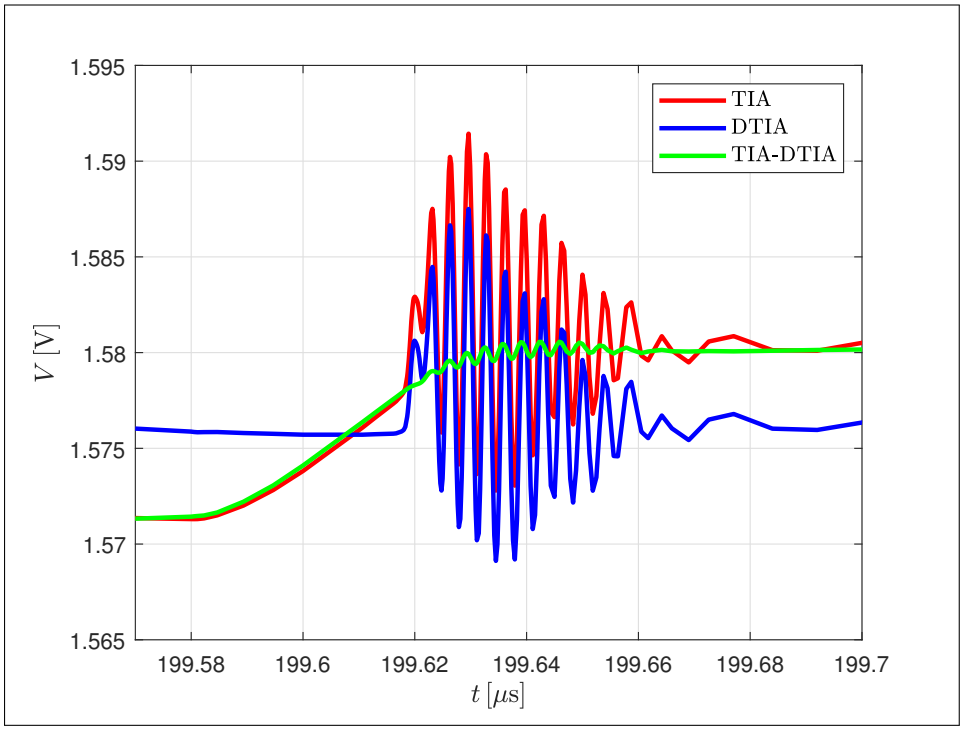


Fig. 2.7: Cancellation of coupled substrate ringing, green shows the sum of the differential signal.

Figure 2.7 shows how substrate ringing can be canceled. Red and blue represent the signals at the TIA outputs, that are processed pseudo differential. When subtract them from each other, common mode disturbances get suppressed massively, which makes the receiver insensitive to substrate noise or ringing.

2.5 Offset cancellation loop

When using optical receivers in fiber-based communication, the input signal assumably isn't influenced by background light, due to an enclosed optical transmission path. Hence for OWC, background light sensitivity is a factor that needs to be considered. The problem is, that it adds a DC component onto the fast transmitted signal, which may cause shifts in operating points of amplifiers, contained in the receiver circuit. In the worst case, this leads to non-linear distortions implying jitter amplification and PWD (see section 1.7). An approach to raise immunity to background light, is to add a highpass filter to the receiver's frequency response. By now having bandpass characteristic, slow changes on the signal (background light fluctuations are very slow compared to the transmitting DR) get canceled. Additionally, when designing a receiver for DRs were flicker noise plays a dominant role in the noise figure, a lower cut-off frequency may improve the total input referred noise. Presupposed that the filter circuit adds less noise than it saves. Nevertheless, the lower cut-off frequency has to be chosen with care, because it also comes with a trade-off. For example, imagine a coded signal were a sequence of the same binary symbol appears. The spectrum of this signal would also contain energy at lower frequencies that need to be amplified, to keep the right spectral distribution. The following part covers the requirements on the designed receiver's frequency response. Starting with a discussion on the lower cut-off frequency which is mainly determined by OCL (marked green in Figure 2.1) followed by a description of how the OCL is implemented and simulations showing the offset cancellation process.

2.5.1 Lower cut-off frequency of the receiver

As mentioned in section 1.9, the DAI for TOSLINK is coded in bi-phase mark. That means over the data bits in one sub-frame, the signal is DC-free. For estimation of the highest possible lower cut-off frequency, the duration of the longest consecutive sequence of the same symbol, appearing locally in one sub-frame, needs to be determined. Therefore a TOSLINK signal was measured, the longest sequence of consecutive symbols was three. Standard digital audio formats are sampled with rates at 32 kHz, 48 kHz, 96 kHz at either 16 or 24 bit. The most sophisticated sound-cards are capable of processing 24 bit @ 192 kHz, this will be the benchmark when specifying the bandwidth of the receiver. Table 2.2 shows the DR requirements, when transmitting the encoded information for different audio quality. The longest pulse appearing within this transmission is 5.859 µs when data is sampled with 16 bit resolution @ 32 kHz. Since the receiver, designed in

sample-rate	192 kHz		96 kHz		48 kHz		32 kHz	
bit	16	24	16	24	16	24	16	24
DR [MHz]	3.072	4.608	1.536	2.304	0.768	1.152	0.512	0.768
shortest pulse [µs]	0.326	0.217	0.651	0.434	1.302	0.868	1.953	1.302
longest pulse [µs]	0.976	0.651	1.953	1.302	3.906	2.604	5.859	3.906

Tab. 2.2: DRs arising with the state-of-the-art coding qualities, longest pulses contain a three element sequence of the same symbol

this thesis, is optimized for TOSLINK application, the minimum time constant τ_{min} for the receiver's lower cut-off frequency needs to be at least higher than this value.

The time constant, corresponding to the lower cut-off frequency is, determined by $\tau = R_{INT}(C_{INT} + C_{EXT})$ in Figure 2.1. The index "EXT" indicates an off chip implementation, while "INT" means integrated on chip. To ensure, that the minimum time constant is never undershot, the necessary values for R_{INT} and C_{INT} are integrated with some amount of buffer, leading to

$$\tau_{min} = R_{INT}C_{INT} = 750\,\text{k}\Omega \cdot 8.1\,\text{pF} = 6.075\,\mu\text{s} \tag{2.4}$$

which corresponds to the maximum lower cut-off frequency of $f_{l,max}$= 26.2 kHz, when applying external capacitance is desisted. Figure 2.8 shows, how the frequency response can be varied by increasing the OCL time constant via C_{EXT}. So in case of using the receiver for different coded formats, that are encoded with certain DC values, f_l can be decreased, to ensure proper transmission. When applying f_l to the noise spectrum of the TIA in Figure 2.3b, low frequency noise gets damped, which leads to less $i_{n,TIA}^{rms}$. Considering the noise distribution for the implemented *INV-TIA*, the critical frequency value that should be exceeded by f_l is 5 kHz. Beneath this point flicker noise dominates the noise contribution of the TIA, which is a good approximation for the total receiver's noise contribution. When planning the simulations on receiver performance, it is not always the best approach to just simulate the best case scenario, therefore the standard configuration for simulations, performed on the proposed receiver, includes an external capacitance of $C_{EXT} = 26\,\text{pF}$. This setup results in a lower cut-off frequency of $f_l = 6\,\text{kHz}$, so it is expected to produce more $i_{n,TIA}^{rms}$ than with $C_{EXT} = 0\,\text{pF}$, while still being above the 5 kHz limit. Also the time constants for this setup are acceptable in terms of simulation duration (all important information can be simulated within a 250 µs transient analysis).

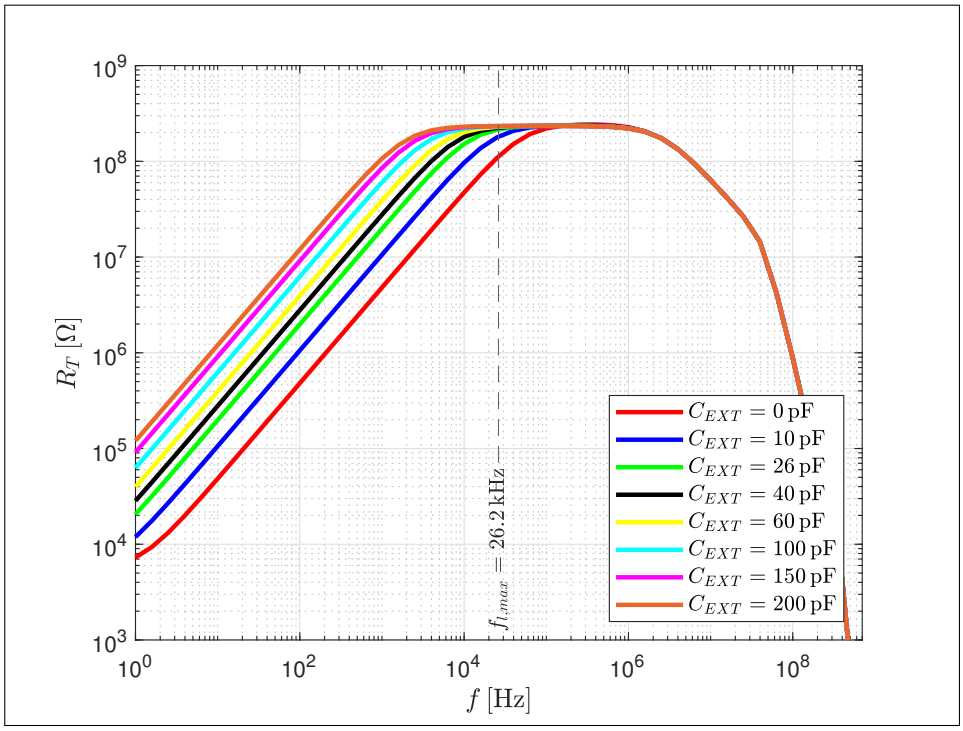


Fig. 2.8: Frequency response of the receiver for different C_{EXT}, the maximum upper cut-off frequency $f_{l,max}$ is determined by the time constant of C_{INT} and R_{INT}.

2.5.2 Working principle of the OCL

Depicted in Figure 2.1, the working principle of the OCL is based on a p-MOS transistor (M_{OCL}), which channel resistance is controlled by it's gate-potential V_G. This voltage is generated by the output of the implemented OTA, which compares the voltage of the signal-path to the reference-path (dummy-path). If there is an offset between those two voltages it produces a proportional drop of V_G, leading to a decrease of M_{OCL}'s channel resistance. The current, at the TIA input, gets drained off over the p-MOS transistor, leading to a cancellation of the offset. When talking about offset, two different types have to be distinguished. First, offset caused by a slow increase of photo-current, which elevates the voltage level of V_{com1} by a value of $\Delta V_{com1} = R_{T,(TIA+SF+FDA)}\Delta i_{APD}$. This can be achieved by background light, but also by the signal itself. When considering the transmission system, presented in section 1.8, that generates two different power levels for either a '1' (P_{APD1}) or a '0' (P_{APD0}), this means there are two corresponding photo-currents $i_{APD,1}$ and $i_{APD,0}$, which correspond via $i_{APD,1} = i_{APD,0}E_R$. Together with a photo-current induced by background light (i_{BL}), the resulting DC APD current can be expressed as

$$i_{APD,DC} = \frac{i_{APD,1}(1 + \frac{1}{E_R})}{2} + i_{BL} \tag{2.5}$$

This value needs to be drained off by M_{OCL} in order to cancel the offset, that is induced by the photo-current. For high E_R and no background light, $i_{APD,0}$ as well as i_{BL} are approximately zero, leading to a photo-current DC component of $i_{APD,DC} = i_{APD,1}/2$. Considering this, the term DC-free encoding format (used in section 1.9) is a little bit misleading, as it is referred to differential signals. However, in this context, it means just that the DC component results in exactly $i_{APD,1}/2$. For lower E_R and still no background light, it gives $i_{APD,DC}= (i_{APD,1} + i_{APD,0})/2$. The effect of offset, caused by the photo-current, is depicted in Figure 2.9a, it was simulated with ideal E_R. High $i_{APD,1}$, causes more elevation of V_{com1}, which makes a further decrease of V_G necessary, to cancel the offset. In Figure 2.9b, the influence of different values for C_{EXT} on the time constant of the OCL, is shown. It demonstrates, that when transient simulations are performed for receiver setups with more than 60 pF the simulation duration needs to be increased. What can be realized in both figures, is an increasing ripple of V_G for fast time constants, it is caused by not using a DC-free PRBS-waveform-file for simulation. At the receiver output this results in kind of tremble in the eye diagram (see subsection 2.6.3). However this should not appear when sourcing the receiver with a TOSLINK-coded waveform, besides it can be reduced by increasing C_{EXT}. The second type of offset that can be canceled by the OCL, besides by the one induced by photo-current, is offset caused by process variations in differential amplifier stages. In the proposed receiver, this can be helpful to reduce offset caused by the FDA (red in Figure 2.1) but also with differences in the signal- and reference-path. Additionally, there are matching techniques to reduce sensitivity to process variations, the designer can use during the layout procedure (see subsection 3.4.1). However the total precision of the offset-cancellation is limited to the offset of the OTA, used for the OCL. Special matching efforts need to be performed to reduce it as much as possible. In Figure 2.10, the offset cancellation is shown for two different receiver setups in terms of C_{EXT}. For using an external capacitor of 26 pF, the offset is canceled after about 100 µs, while when applying 60 pF, this happens after approximately twice the time. In Figure 2.11, the signal after the FDA is depicted with and without offset for $C_{EXT} = 26$ pF. The dimension of the offset, shown in Figure 2.11a, would cause far to much PWD to achieve the specified BER. After it is canceled (Figure 2.11b), only the operating point of the following OTA (violet in Figure 2.1) needs to be adjusted correctly to prevent PWD. It can be varied by V_{CM}, which will be explained in detail in section 2.6.

Comparing the proposed method, of implementing the OCL, to other variants mentioned in section 1.10, shows an additional noise contributer at the TIA input. In subsubsection 1.4.5.1 was shown, that the channel noise of a MOSFET mainly consists

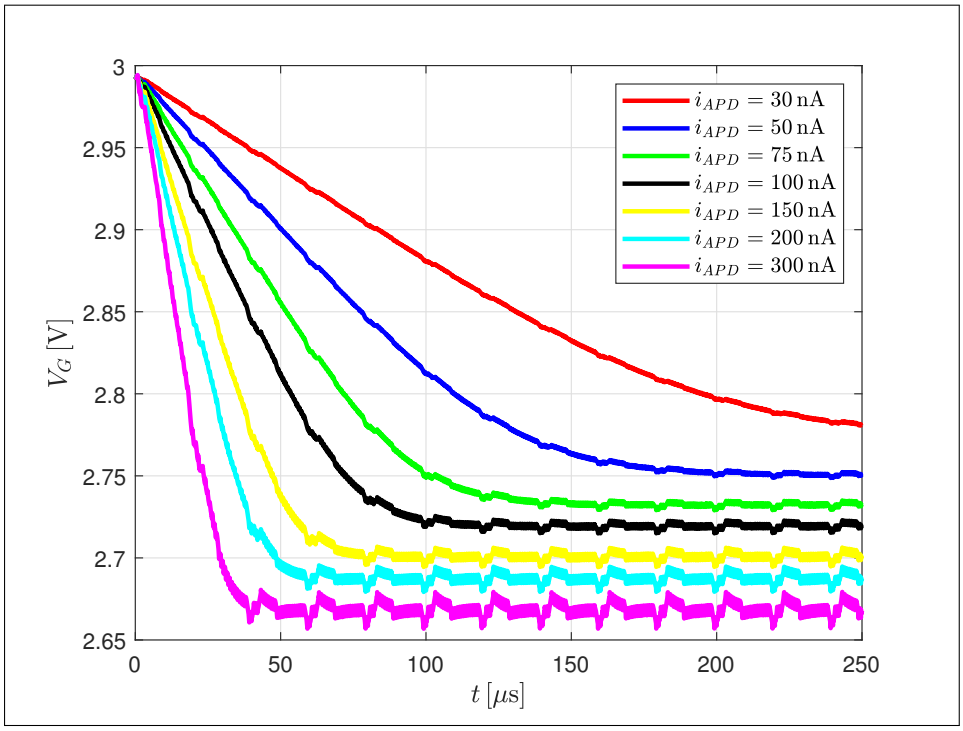
of thermal and flicker noise. Since f_l is usually set above the flicker cut-off, only thermal noise, will directly elevate the total i_n^{rms}. The amount of generated thermal noise depends on, the current the transistor needs to drain off for offset cancellation ($i_{APD,DC}$), it's transconductance at the operating point and the local temperature (see Equation 1.15). Higher i_n^{rms} will therefore decrease the receiver's sensitivity. Since the transistor operates in saturation region ($V_{DS} > V_G - V_{th}$), the transconductance at the operating point can be determined by

$$g_m = \sqrt{2\mu_p C_{ox} \frac{W}{L} i_{APD,DC}}. \tag{2.6}$$

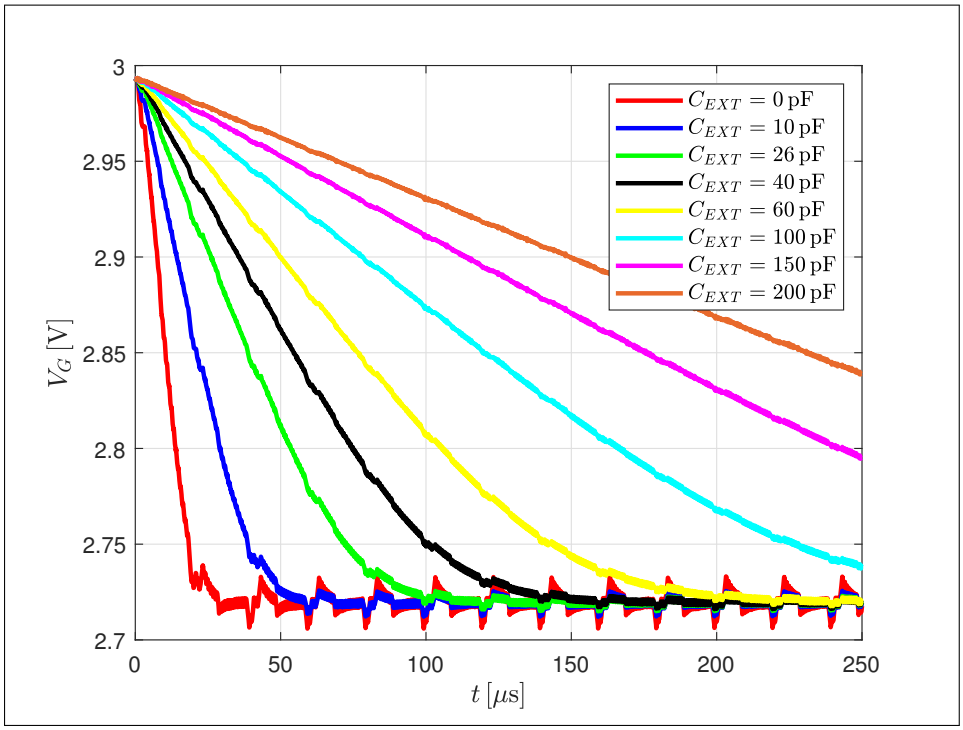
The required process parameters are given in [6] as μ_p= 503.6 cm^2/Vs and C_{ox}= 4.485 mF/m^2. It was designed with $W = 5\,\mu m$ and $L = 0.35\,\mu m$. In subsection 3.2.1, when calculating the receiver's sensitivity, the channel noise of M_{OCL} will be considered. OCL methods, where the offset cancellation is achieved by manipulating the dummy-path, rather than the signal-path, add less noise to the signal. Though, because of enabling symmetrical substrate coupling (discussed in subsection 2.4.1), the design choice was to implement the OCL with the p-MOS transistor at the signal-path front-end. Additionally, a RC-low-pass was placed at the gate of M_{OCL} to reduce induced gate noise.

2.6 Fully differential operational amplifier

FDAs provide a lot of advantages against their single ended counterparts, like a larger output swing at the same supply voltage or insensitivity to common mode noise. The major reasons why for the presented application a FDA was used, are the possibility to realize an offset cancellation loop for BLC (covered in section 2.5) and to compensate substrate noise on the signal (covered in section 2.4). But there are also some challenges to overcome while using them. The following part, starts with addressing the occurrence of common mode voltage instability and continues with explaining the principle of CMFB as a measure to deal with it. After that, the designed FDA it presented and discussed.

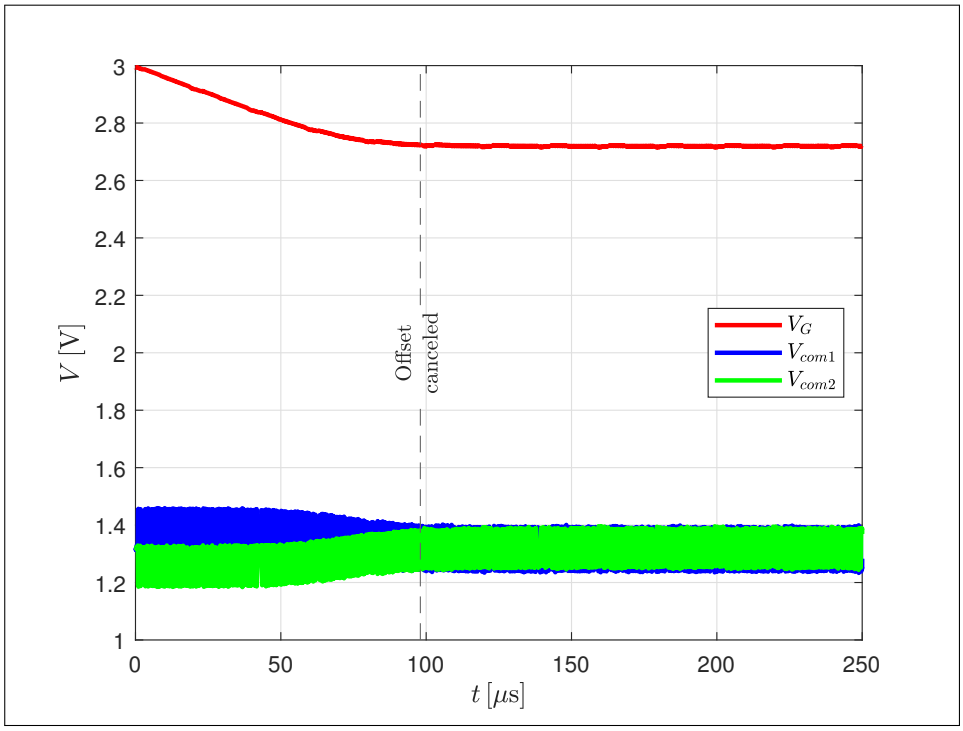


(a) Different values of photo-current @ $C_{EXT} = 26\,\mathrm{pF}$

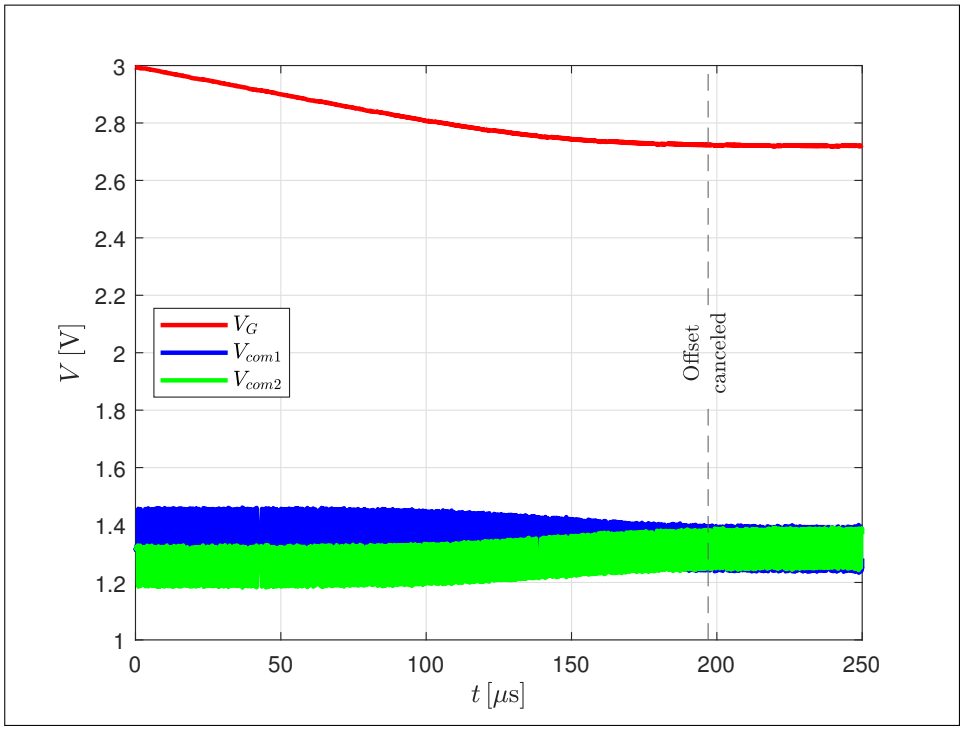


(b) Different values of C_{EXT} @ $i_{APD} = 100\,\mathrm{nA}$

Fig. 2.9: Influence on the gate potential of M_{OCL}, for different extents of offset caused by photo-current (a), and different time constants adjusted by C_{EXT}.

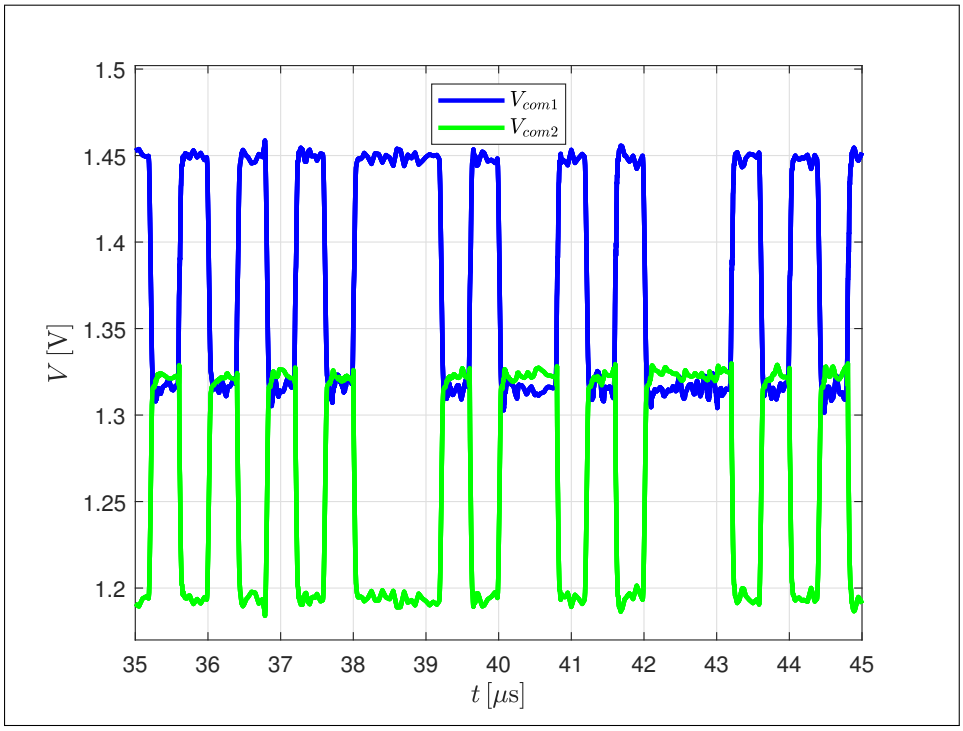


(a) Offset cancellation at $C_{EXT} = 26\,\mathrm{pF}$ and $i_{APD} = 100\,\mathrm{nA}$.

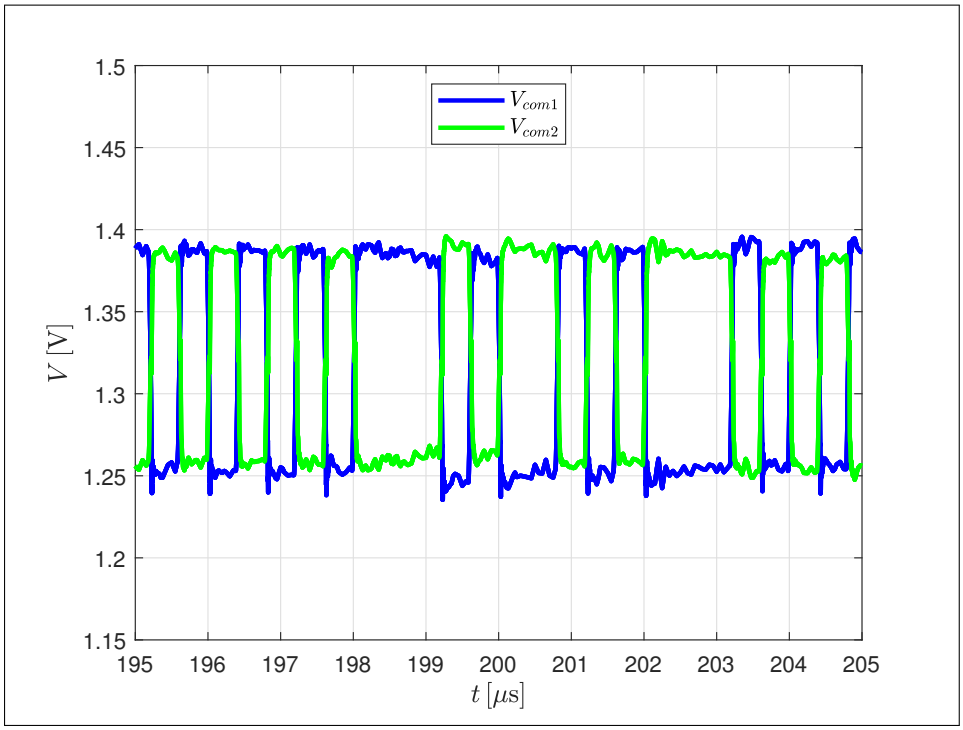


(b) Offset cancellation at $C_{EXT} = 60\,\mathrm{pF}$ and $i_{APD} = 100\,\mathrm{nA}$.

Fig. 2.10: Offset cancellation process for two different time constants of the OCL.



(a) Differential output of the FDA with offset



(b) Differential output of the FDA without offset

Fig. 2.11: Differential output of the FDA at different points in time, simulated for $C_{EXT} = 26\,\text{pF}$.

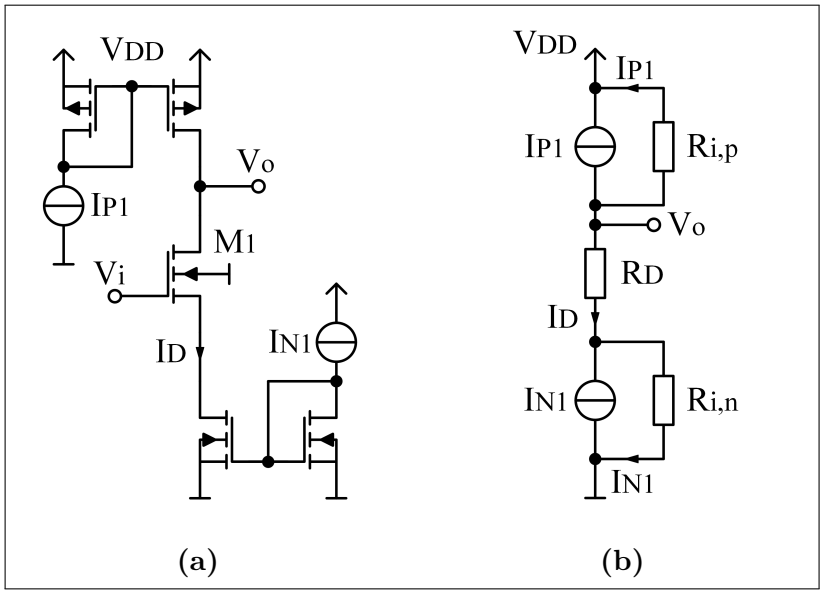


Fig. 2.12: Problem with shifts in the output common mode voltage, arising with active loaded differential stages. a) shows one half of an active loaded differential pair, b) it's equivalent circuit with current sources instead of the current mirrors.

2.6.1 Common mode feedback

A problem occurring with active loads in differential stages is a rather high common mode voltage uncertainty at the outputs, depending on process variations. This difference in common mode voltage, is even increased when using additional amplifier stages, in combination with the differential front-end. The following example presented in [8], tries to illustrate this problem. To understand this, Figure 2.12a shows one half of a fully differential pair with active load. M_1 represents the input transistor, which is sourced by a p-MOS current mirror, representing the active load, as well as a n-MOS tail current mirror. If the DC common-mode is considered, this configuration equals to a cascoded n-MOS current source, connected to a p-MOS current source. Figure 2.12b gives an equivalent circuit for this constellation. In ideal conditions, when I_{N1} is identical to I_{N2}, the common mode output voltage V_o is well defined by the output resistances of M_1 and the current sources. Though in practice I_{N1} and I_{N2} won't be exactly the same e.g. due to mismatch in the current mirror pairs. To compensate this, a change in the common mode voltage V_o at the source of M1 will appear. Since the output resistance of the current mirrors is high, even a small mismatch will lead to a significant change in the common mode voltage and can easily push one transistor towards the triode region. To prevent this, CMFB can be implemented. The principle is, to compare the

common mode output voltage to a reference voltage, and adjust one of the current sources according to their difference.

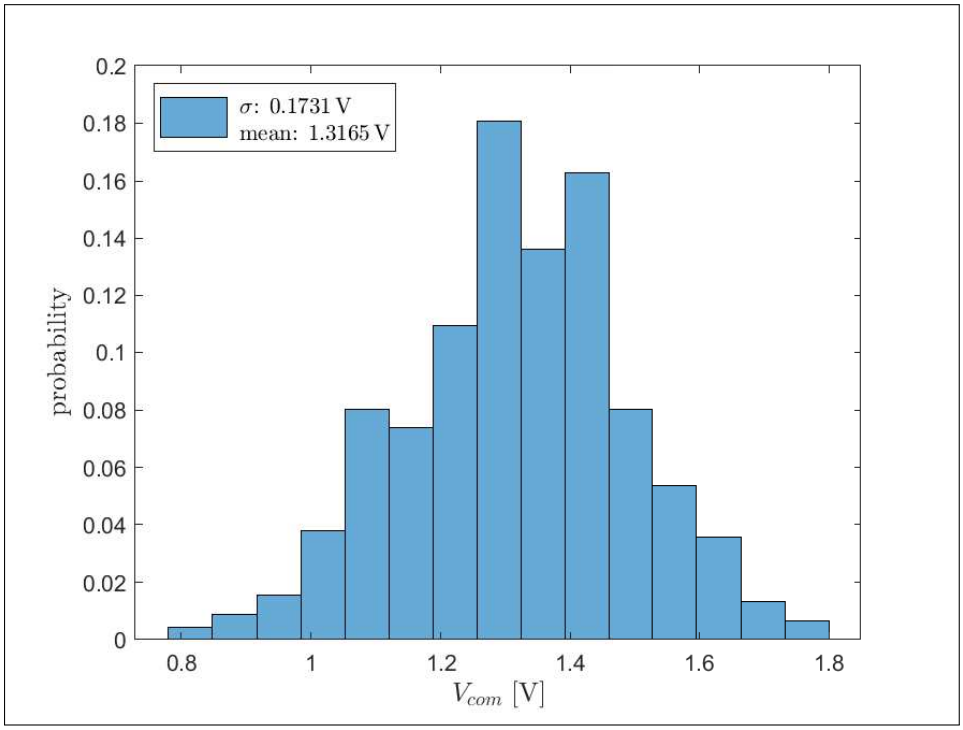


Fig. 2.13: Histogram of V_{com}, simulated with Monte Carlo analysis for 448 samples, and with $V_{CM} = 1.78\,\mathrm{V}$.

2.6.2 Design of the FDA

In the first place, the FDA was designed with an active loaded differential stage, followed by a common source stage (CS) on both outputs (see Figure 2.14). This amplifier was investigated, in terms of common mode voltage at it's outputs, by Monte-Carlo analysis. It is a simulation method, that models process variations, specified by the technology provider, to estimate yield of the designed integrated circuits. The results, for an amount of 448 samples, are depicted in Figure 2.13. With a standard deviation of almost 180 mV it showed, that V_{com} is highly sensitive to process variations, which would make the dynamic range of the receiver dependent on random conditions. In that sense, V_{com} means the common mode voltage for a canceled offset between V_{com1} and V_{com2}. In order to maximize the dynamic range, V_{com} needs to be optimized to the characteristic of the following amplifiers (see section 1.7), which in this case is the output circuitry OTA (violet in Figure 2.1). By implementing CMFB, V_{com} can be trimmed during operation by V_{CM}. The implemented method is based on [8], carried out with two additional differential pairs, depicted in Figure 2.14. A major benefit with

this method, is that it uses only transistors, which parameters are in general easier to control during production process, than that of passive components. In principle, the common mode voltage at the drains of M_{in1} and M_{in2} is sensed by the gates of M_1 and M_4. This generates a current, over the channel of M_{FB1}, proportional to the difference between the common mode voltage and the reference voltage V_{CM}. To show this, the drain currents for M_2 and M_3, which sum up to equate I_{cm}, can be expressed by

$$I_{d2} = -\frac{I_{P4}}{2} - g_{m2}\left(\frac{V_{o1} - V_{CM}}{2}\right) \tag{2.7}$$

and

$$I_{d3} = -\frac{I_{P5}}{2} - g_{m3}\left(\frac{V_{o2} - V_{CM}}{2}\right). \tag{2.8}$$

When designing M_2 and M_3 as well as M_{P4} and M_{P5} with equal sizes, this leads to $g_{m2} = g_{m3}$ and $I_{P4} = I_{P5}$. I_{cm} can now be expressed by

$$I_{cm} = \underbrace{I_{P4}}_{const.} + \underbrace{g_{m2}\left(\frac{V_{o1} + V_{o2}}{2} - V_{CM}\right)}_{proportional\,to\,(V_{oc} - V_{CM})}. \tag{2.9}$$

I_{cm} gets mirrored onto the tail of the differential stage, so the constant term in Equation 2.9 was set to $I_{P4} = I_{P2} + I_{P3}$ by designing $(W/L)_{P4} = (W/L)_{P5} = 2(W/L)_{P2} = 2(W/L)_{P3}$ and the mirror ratio between M_{FB1} and M_{FB2} was chosen to be 1:1.

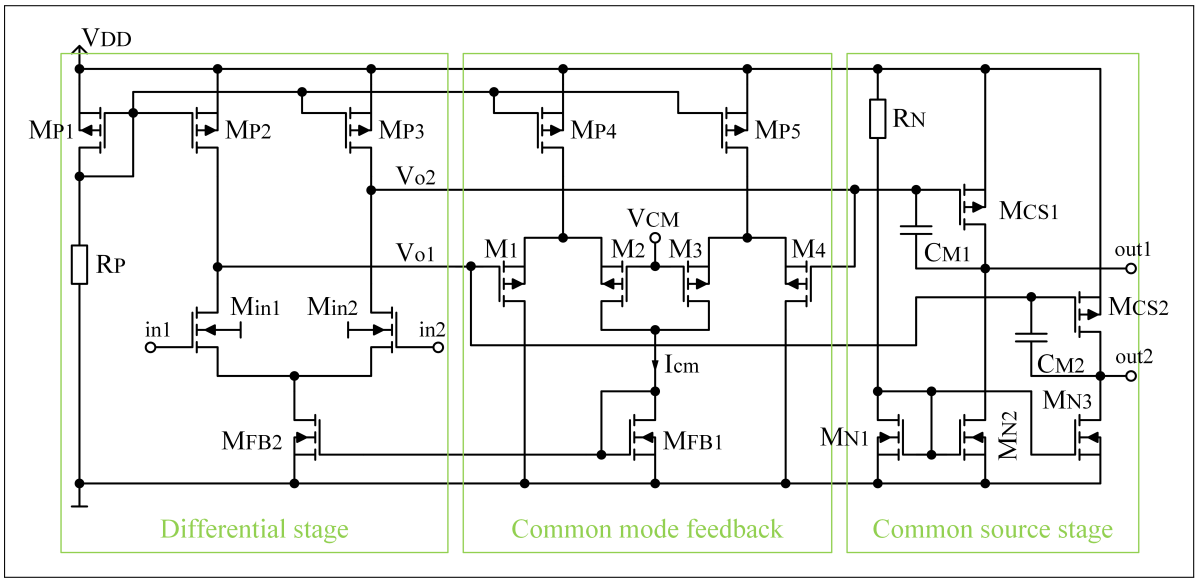


Fig. 2.14: Implemented FDA circuit, containing a differential front-end, CMFB carried out with two additional differential pairs and a CS output stage.

2.6.3 Maximizing the dynamic range

As explained before, the common mode voltage of the FDA (V_{com}) is highly sensitive to process variations. So for some chip samples this could lead to a unknown decrease of their dynamic range. For specifying the maximum photo-current for proper operation of a opto-electronical receiver there can be distinguished between two major definitions. Fist, the linear range is defined as the maximum photo-current were the signal never reaches into the non-linear area of an amplifier's characteristic. Whereas the definition of the dynamic range focuses on the maximum photo-current where BER specifications are still met, so non linear distortions are acceptable to a certain extent. The idea to maximize the dynamic range, in this thesis, was to design a very high gain output circuitry that pushes the signal onto the 3.3 V digital level. With this approach, the operating point of the output circuitry OTA, needs to be set, so a symmetrical signal swing is reached. Independent of process variations, this can be achieved by trimming V_{CM}, which therefore shifts V_{com}. This effect can be represented by a linear function as

$$V_{com}(V_{CM}) = -9.26 V_{CM} + 17.74\,\mathrm{V}. \tag{2.10}$$

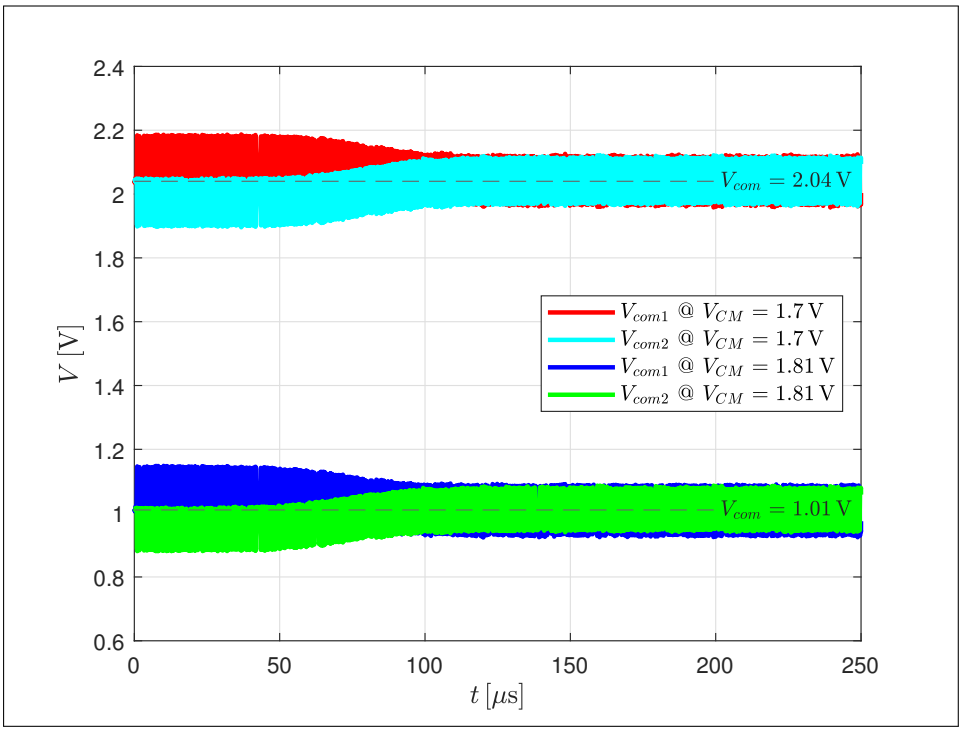
As long as V_{CM} stays within 1.6 V to 1.85 V, it is a good approximation for the shift of V_{com}. In Figure 2.15a, the common mode voltage levels for two different values for V_{CM} are depicted. It is possible to move V_{com} over a broad range of the 3.3 V span. This manipulation of the DC operating point for the output circuitry OTA, becomes specially important when sourcing the receiver with high photo-currents, to keep a high dynamic range. Though also for low signal currents PWD can appear, if V_{com} is located near the non-linear range of the output circuitry OTA. This actuality is shown in Figure 2.15b, which depicts an eye diagram of the receiver's output signal for $i_{APD} = 100\,\mathrm{nA}$ and $V_{com} = 2.46\,\mathrm{V}$, caused by $V_{CM} = 1.65\,\mathrm{V}$. The crossing point of this eye diagram is distorted upwards from center, which will lead to an increase of Bit-errors in a decision unit. As shown in Figure 2.16a, by trimming V_{CM} to 1.8 V, PWD vanishes and the eye's crossing point moves to center, to about 1.65 V, which is the optimum decision threshold at this supply voltage. The receiver's linear range can be defined by considering the transimpedance of the TIA, source follower (SF) and FDA chain, which amounts to $R_{T,(TIA+SF+FDA)} = 1.33\,\mathrm{M\Omega}$. The linear region of the output circuitry OTA lies in between approximately 0.5 V and 2.5 V (the upper limit of this entity is 3 V), so with an optimal set operating point, the receiver's linear overload current $i^{pp}_{ovl,lin}$ can be specified by

$$i^{pp}_{ovl,lin} = \frac{(V_{op,max} - V_{op,min})}{R_{T,(TIA+SF+FDA)}} = \frac{2\,\mathrm{V}}{1.33\,\mathrm{M\Omega}} \approx 1.5\,\mu\mathrm{A}. \tag{2.11}$$

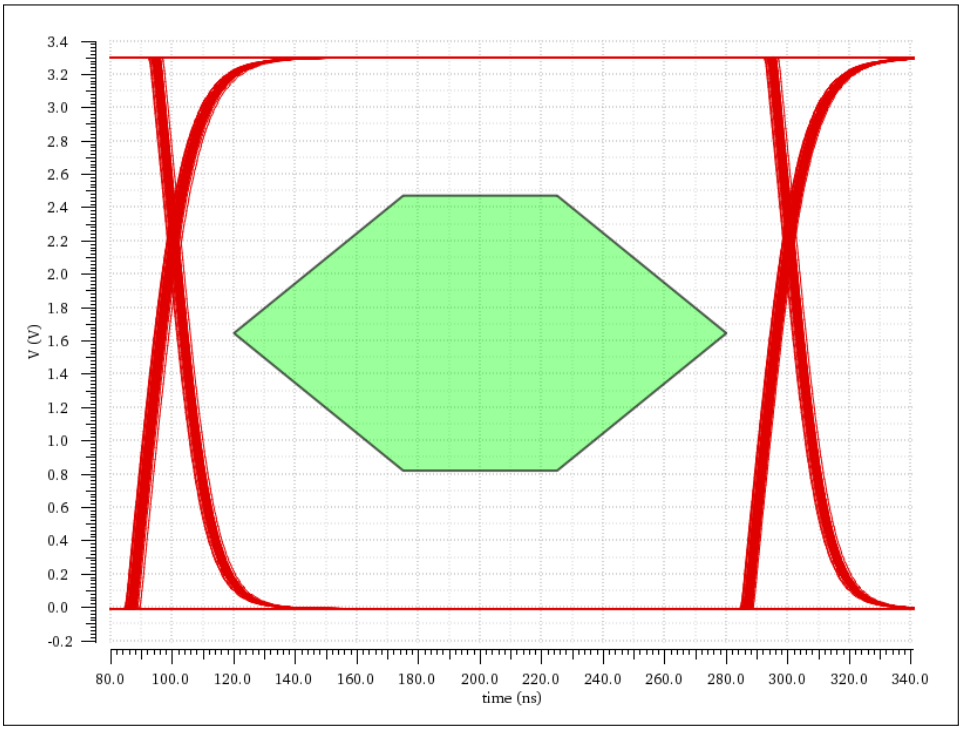
However, the receiver is capable of satisfying BER specifications with even higher input currents. Figure 2.16b shows the eye diagram at the receiver's output for an input current of 10 µA, V_{CM} needed to be adjusted to 1.745 V leading to $V_{com} = 1.58$ V. With this operating point, the signal deflects symmetrically into the non-linear regions of the output circuitry OTA. What can be noticed, is a little tremble appearing at the eye diagram, this is caused by simulating with a non-DC-free PRBS-waveform file (see also subsection 2.5.2). It can be reduced by either using DC-free coded signals or decreasing f_l by increasing C_{EXT} (covered in detail in subsection 2.5.1). So the input overload current can be specified by at least $i_{ovl}^{pp} = 10\,\mu A$. In practice, maybe even higher values can be achieved.

2.7 Output circuitry

The output circuitry consists of two major components. The pseudo differential signal, at the output of the FDA, needs to be transformed into a single-ended domain, this is achieved by a two stage Miller CMOS OTA. Since it has a signal swing that is limited to the saturation voltages of the CS transistors, another component needs to be designed, to reach full 3.3 V digital output levels. Additionally, receiver outputs in general need to have low output resistance, so that it's voltage gain is preferably unaffected by any load impedance applied at the output. This is achieved by the three-inverter output driver. By using three instead of one inverter stages, it is possible to reduce load on the OTA while containing driving capability at the receiver output. The principle is, to design the first inverter stage with small transistor sizes to keep their gate capacitance (and therefore the load on the OTA) small. Now by doubling the transistor sizes for each following stage, arbitrary driving capability can be realized in dependence of the system requirements. In the presented application, the applied load impedance will most likely be predominantly capacitive, due to MOS inputs of the following digital ICs. The simulations were carried out with a 200 pF load capacitance, which corresponds approximately to the input capacitance of an oscilloscope.

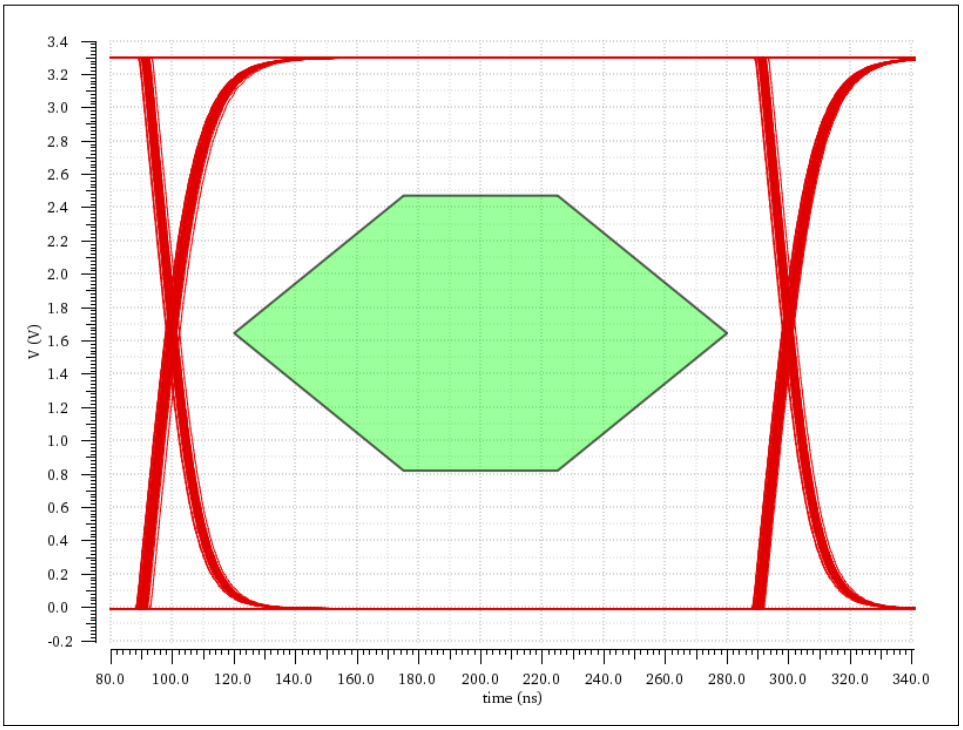


(a) Shift of V_{com} in dependence of two different V_{CM} values.

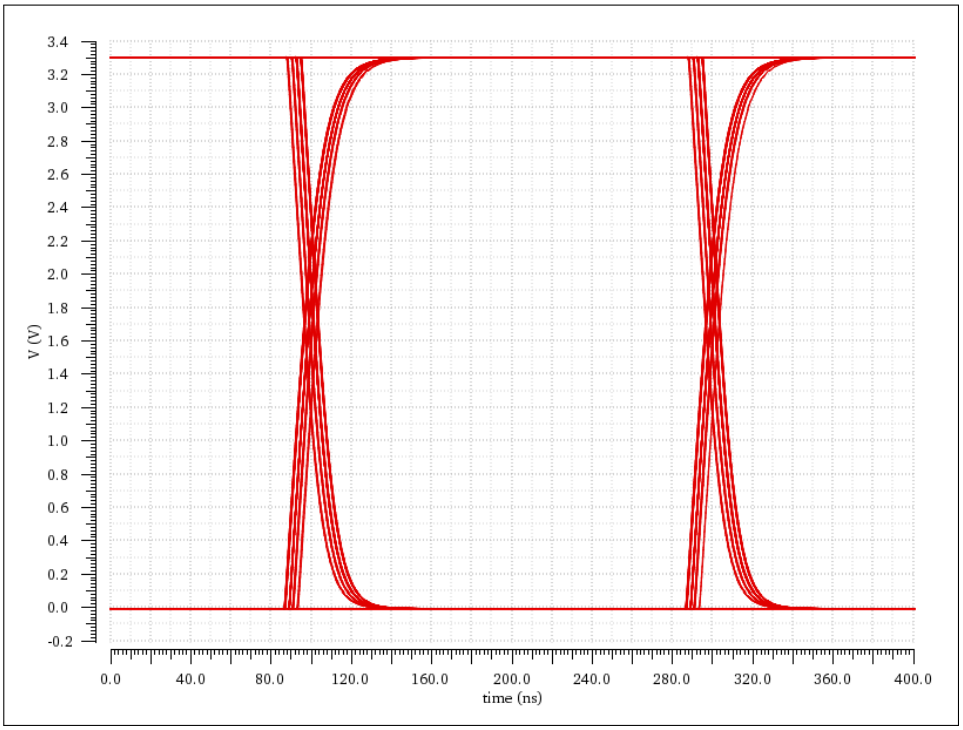


(b) PWD in the eye diagram of the output when operating the receiver with $V_{CM} = 1.65\,\mathrm{V}$ and $i_{APD} = 100\,\mathrm{nA}$, the crossing point has moved upwards from the middle, causing an increase in BER.

Fig. 2.15: Influence of V_{CM} on PWD.



(a) Eye diagram at $i_{APD} = 100\,\text{nA}$ and $V_{CM} = 1.78\,\text{V}$.



(b) Eye diagram at $i_{APD} = i_{ovl}^{pp} = 10\,\mu\text{A}$ and $V_{CM} = 1.745\,\text{V}$.

Fig. 2.16: Eye diagrams with well set V_{CM}. Simulated with a DR of 5 Mbit/s.

Chapter 3

Results

3.1 Bandwidth

The lower cut-off frequency of the receiver is determined by the OCL, covered in subsection 2.5.1. By applying two external capacitors (C_{EXT}) to the receiver, it can be varied from about 26 kHz to values of a few Hertz. The upper cut-off frequency is determined by the bandwidths of the components in the amplifier chain. In this design it was optimized to the maximum DR appearing within the range of standard audio qualities for TOSLINK application. Table 2.2 lists the formats, that state-of-the-art transmission components are capable of processing. The highest DR occurs when sampling 24 bits with 192 kHz, it results in a bit-rate of 4.608 MB/s. The optimum bandwidth, in terms of noise minimization, needs to be set to about $^2/_3 \cdot DR$ [22], which would demand an upper cut-off frequency of about 3.072 MHz. However during chip fabrication, process variations might appear, leading to the decision to choose a little bit higher value for f_u. After the post-layout simulations the receiver's upper cut-off resulted in $f_u = 4$ MHz. The frequency response is depicted in Figure 2.8.

3.2 Dynamic range

3.2.1 Sensitivity

For estimation of the receiver's sensitivity the total input referred RMS noise current needs to be identified. The noise contributers, appearing within this design are the TIA, the APD and M_{OCL}. Considering their mean square noise, the total input referred RMS noise values ($i_{n,1}^{rms}$ and $i_{n,0}^{rms}$), for either receiving a '1' or a '0', can be expressed as

$$i_{n,0}^{rms} = \sqrt{i_{n,el}^2 + i_{n,APD0}^2 + i_{n,MOS}^2} \tag{3.1}$$

and

$$i_{n,1}^{rms} = \sqrt{i_{n,el}^2 + i_{n,APD1}^2 + i_{n,MOS}^2}. \tag{3.2}$$

As mentioned in section 2.3, the noise performance of the TIA gives a good approximation for the noise of the whole amplifier chain. The implemented TIA circuit, for the designed receiver, is the *INV-TIA*, which noise density spectrum is depicted in Figure 2.3b. The circuit's mean square noise $i_{n,el}^2$ can be expressed as

$$i_{n,el}^2 = \int_{f_l}^{f_u} |i_{n,TIA}(f)|^2 \, \mathrm{d}f = |i_{n,TIA}|^2 \Big|_{f_l}^{f_u} = |i_n(f)|^2 \, (f_u - f_l). \tag{3.3}$$

When considering the receiver bandwidth, with $f_u = 4\,\mathrm{MHz}$ and $f_l = 6\,\mathrm{kHz}$ (@ $C_{EXT} = 26\,\mathrm{pF}$), the noise density is approximately constant $|i_{n,TIA}|^2 = 1.5 \cdot 10^{-25}\,\mathrm{A^2/Hz}$. Applying these parameters into Equation 3.3, results in $i_{n,el}^2 = 6.6 \cdot 10^{-19}\,\mathrm{A^2}$.

As shown in subsection 2.5.2, the current over the channel of M_{OCL}, and therefore the amount of thermal noise generated, depends on the DC photo-current $I_{APD,DC}$. By applying (1.26) onto (2.5), the mean square value contributed by this component ($i_{n,MOS}^2$) can be expressed in dependence of the received optical power at a '1' as

$$i_{n,MOS}^2 = 4k_B T_r k_D \underbrace{\sqrt{2\mu_p C_{ox} \frac{W}{L} \left(\frac{P_{APD,1}(1 + \frac{1}{E_R})RM}{2} + i_{BL} \right)}}_{g_m} (f_u - f_l) \tag{3.4}$$

Since the time constant of the offset cancellation is slow compared to the signal DR the thermal noise generated in the channel of M_{OCL} is independent of the received symbol. On the other hand when calculating the APD noise, there arise two different input referred mean-square noise currents $i_{n,APD0}^2$ and $i_{n,APD1}^2$, that need to be treated separately, because 3.1 and 3.2 are non linear functions. The APD noise can be described by

$$i_{n,APD0}^2 = M 2q \left(\frac{P_{APD,1}}{E_R} RM + \frac{i_{BL}}{M} \right) F_{EX} (f_u - f_l) \tag{3.5}$$

and

$$i_{n,APD1}^2 = M 2q \left(P_{APD,1} RM + \frac{i_{BL}}{M} \right) F_{EX} (f_u - f_l). \tag{3.6}$$

While the TIA adds a constant part, the noise, generated by the APD and M_{OCL}, depends on the signal and background light current (i_{BL}). In [20], i_{BL} was measured for a 400 µm APD. When applying their results to usual indoor light levels (300 - 500 lux [4]), and scale them up to an area of 800 µm, the irradiation causes a photo-current of approximately $i_{BL} \approx 1\,\mu\mathrm{A}$. The resulting sensitivity can now be calculated by

applying (3.1) and (3.2) into (1.37). Figure 3.1 shows how the sensitivity depends on the irradiated optical signal power, the background light and the multiplication factor. High optical signal powers as well as current induced by background light, raise shot noise in the APD and thermal noise in M_{OCL}'s channel, which therefore lowers the sensitivity. Note that for each curve there is a local minimum at a certain multiplication value. It arises from a trade-off in APDs, between shot noise amplification and photo-current increase, both caused by the multiplication M(see (1.28) and (1.27)). This sensitivity minimum is reached when operating at the optimum multiplication M_{opt}. So in order to maximize the receiver performance in volatile environment conditions, a method to control the APD gain becomes advisable. How the sensitivity is influenced by different operating scenarios, can be seen in Figure 3.1. The calculations were performed for a BER of 10^{-9} which corresponds to $Q = 5.997$, with $k_{eff} = 0.1$ (slightly higher than what was measured for the 400 µm devices in [18], to be on the safe side), $R = 0.45$ and $E_R = 1000$. Comparing the red plot ($\overline{P}_{sens} = -54.77\,\text{dBm}$ @ $P_{APD1} = 100\,\text{nW}$) with the blue one ($\overline{P}_{sens} = -62.34\,\text{dBm}$ @ $P_{APD1} = 1\,\text{nW}$), shows how drastically M_{opt} and the achievable sensitivity changes. Under the compared conditions, operating with the lower signal power and keeping the APD gain constant, lead to an increase in sensitivity of about 6 dB. However, with gain control, an increase of 8 dB would be achievable. In addition, also the influence of background light current i_{BL} is depicted in Figure 3.1. When operating with a signal power of $P_{APD1} = 1\,\text{nW}$, while being in a dark room, the sensitivity bisects from $-62.34\,\text{dBm}$ to about $-59.25\,\text{dBm}$. By adjusting M to M_{opt}, it declines only to $-60.35\,\text{dBm}$.

3.2.2 Overload power

In order to characterize the receiver's dynamic range, the minimum and maximum permissible input power levels need to be determined. While the sensitivity describes the lower limit, the overload power defines the upper boundary, so that BER specifications are still met. According to the results presented in subsection 2.6.3, the maximum linear overload current was calculated to $i^{pp}_{ovl,lin} \approx 1.5\,\mu\text{A}$. Considering the receiver set-up for $P_{APD1} = 1\,\text{nW}$ (with $R = 0.45$ and $M = 54$), the linear overload power can be determined by using 1.38. With a sensitivity of $\overline{P}_{sens} = -62.34\,\text{dBm}$ and a linear overload power of $\overline{P}_{ovl,lin} = -45.11\,\text{dBm}$ the linear dynamic range equates 17.23 dB. However it was also shown, that by adjusting V_{CM} accordingly much higher overload currents are acceptable. Successful simulations were performed for an input current of 10 µA (see Figure 2.16b). This would correspond to an overload power of $\overline{P}_{ovl} = -36.87\,\text{dBm}$ and therefore to a dynamic range of 25.47 dB, presupposed V_{CM}

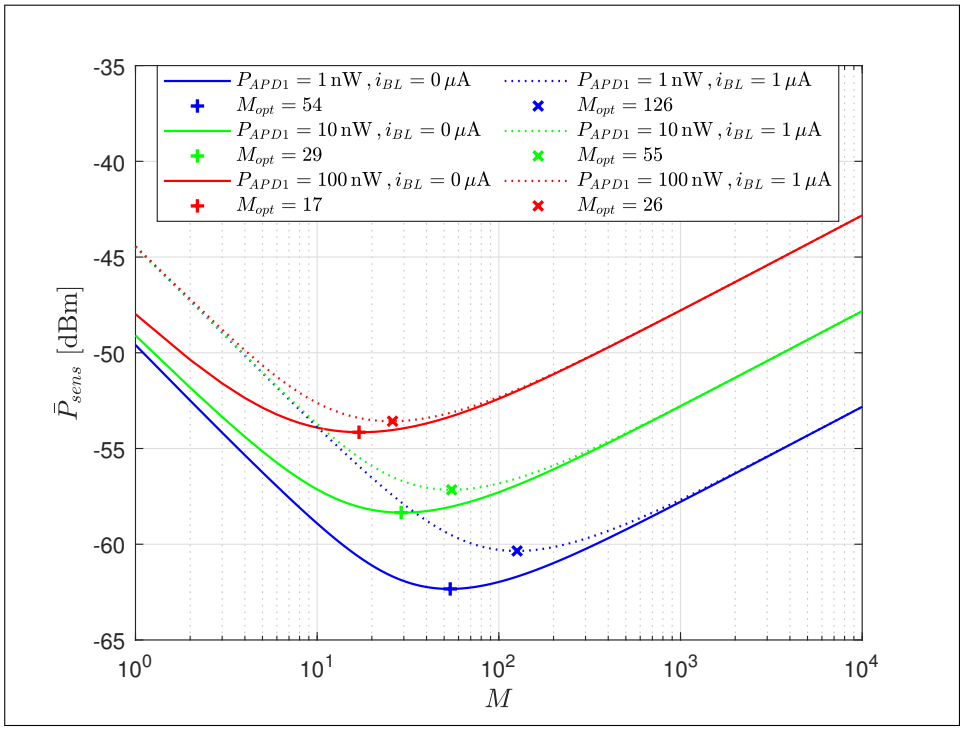


Fig. 3.1: Sensitivity of the receiver for different input signal power levels, the continuous lines are simulated without background light irradiation, the dotted lines are with a background light induced photo-current of 1 µA. Markers indicate the the optimum multiplication, where the maximum sensitivity for each operating state can be achieved.

gets adjusted accordingly (see subsection 2.6.3). Note, that background light irradiation has no effect on the receiver's overload power. It affects the DC-component of the photo-current, which causes an offset between *signal-* and *dummy-path* that gets canceled by the OCL. Without this measure, even average indoor light levels would lead to an extreme decrease of the receiver's dynamic range. However, further circuit improvements are possible, to increase the dynamic range. For example to implement AGC for the APD bias voltage. By measuring the photo-current, the multiplication could potentially be decreased when i_{APD} approaches i_{ovl}. If the AGC circuitry would be capable of reducing the APD gain to $M = 1$, a theoretical overload power of $-19.54\,\mathrm{dBm}$ can be achieved, leading to a hypothetical dynamic range of 42.8 dB.

3.3 Specification of the operating range

In this part, an example of dimensioning the transmission system for standard indoor operation is exercised. The geometrical parameters appearing with the channel setup, as well as the mathematical modeling are presented in section 1.8. With the following

specification, the system works indoors and the receiver should operate with an average optical power $\overline{P}_{APD} = 0.5\,\text{nW}$ (which means $P_{APD1} = 1\,\text{nW}$ for high E_R). The upper limit for transmitting power of the RCLED is $\overline{P}_{tr} = 1\,\text{mW}$, a device with a radiation angle of $\alpha = 5\,^\circ$ was chosen. The photo-detector of the receiver, is the integrated 800 µm SiAPD. Applying these parameters to (1.43) gives a maximum operating distance for optical paths of about r_{max}= 11.79 m, leading to a cone radius of $w = 1.14\,\text{m}$, which should be enough to prevent from aiming issues. When reducing the transmission distance, the received optical power increases, it can be calculated by

$$\overline{P}_{APD} = \frac{\overline{P}_{tr} A_{APD}}{r^2 4\pi \sin^2(\frac{\alpha}{4})}. \tag{3.7}$$

So when considering the receiver's overload power, calculated in subsection 3.2.2, this gives the minimum operating distance of r_{min}= 0.41 m @ $\overline{P}_{APD} = \overline{P}_{ovl}$.

The presented dimensioning example aims for indoor operation and a relatively low transmission distance. If other applications are desired, probably the easiest way to alter the distance specifications, is to change either the transmission power or the radiation angle of the RCLED.

3.4 Layout

3.4.1 Matching

When layouting analog integrated circuits, there are some methods to desensitize the designed components from either variations occurring at the fabrication process or changes in environmental conditions during operation. These techniques aim to assimilate the device parameters of circuit components, where mismatch would lead to a certain performance decrease. Device parameters are mainly dependent on the fabrication process, where procedures like ion-implantation and thermal-diffusion are performed, just to name a few. So for example measures to deal with anisotropic ion-implantation angles would be to have matched devices oriented the same direction and placed together closely. Thinking about diffusion process steps, where differences in concentration lead to a movement of atoms, it may be beneficial to add dummy structures to diffusion areas located at the boundaries of a device, so that they experience the same conditions like areas in the middle of the device. Matching can also be improved by choosing design parameters wisely, these are for example the emitter area for BJTs as well as W and L for MOSFETs. Large dimensions favor matching, since local variations are balanced by

averaging over a wide area. An important method to desensitize matched components against linear gradients, distributed over the chip area, is the common centroid layout (CCL) [24]. These distributions can only be referred to as "linear", at a local point of view, and within a small contemplated area. Their origin are for example local temperature sources, like a transistor dissipating electrical power, or stress gradients caused during the fabrication process. The idea of CCL is, to arrange the components in a manner, so that they have a common axis of symmetry, which therefore leads to a compensation of linear gradients. If necessary, devices can be split into multiple parts. For example, when placing two transistors (A and B), with the same design parameters (W,L), side by side $\mathrm{A}-\mathrm{B}$, their individual axes are located separately in the middle of each device. Though for CCL, it is required to divide each device into two sub devices ($\mathrm{A}_1, \mathrm{A}_2$ and $\mathrm{B}_1, \mathrm{B}_2$) with $W_{sub} = W/2$. Their electrical properties stay the same, but placed physically in the order $\mathrm{A}_1 - \mathrm{B}_1 - \mathrm{B}_2 - \mathrm{A}_2$, they now share a common axis of symmetry, located between B_1 and B_2.

When considering the layout in this thesis, particular matching efforts were performed on circuit components like inverter stages and differential input pairs. Besides maintaining uniform orientation, they were placed close together and carried out with a CCL. For typical inverter stages, the p-MOS transistor needs to be about 2.7 times larger than the n-MOS, due to it's smaller charge carrier mobility. The used CCL method, was to split the p-MOS transistor into two equal sized devices and arrange them in an order like $\mathrm{P}_1 - \mathrm{N} - \mathrm{P}_2$, leading to a common axis in the middle of the n-MOS transistor. For differential input pairs a "cross-coupled" arrangement was implemented. Therefore the two input transistors (A, B) were split into two preferably quadratic shapes ($\mathrm{A}_1, \mathrm{A}_2$ and $\mathrm{B}_1, \mathrm{B}_2$), by distributing large W values onto additional gates. If these sub units are placed in a manner of $\frac{\mathrm{A}_1-\mathrm{B}_1}{\mathrm{B}_2-\mathrm{A}_2}$, the devices symmetry axes cross in the middle of the whole quadratic arrangement.

3.4.2 Chip floorplan

The boundaries of the chip are 1.4 mm x 1.45 mm. Figure 3.2 shows the partitions of the functional blocks. Due to substrate might being biased with negative voltages down to -30 V, transistor circuitry needs to be comprised by a *deep-nwell* (see section 2.1). The major receiver circuit was combined into one large *deep-nwell*, only the output driver (meaning the three stage inverter) was sourced out to a separate one. The intention is to protect the analog amplifier circuitry from any disruptions caused by switching actions of the output inverters. Therefore the chip, additionally, contains

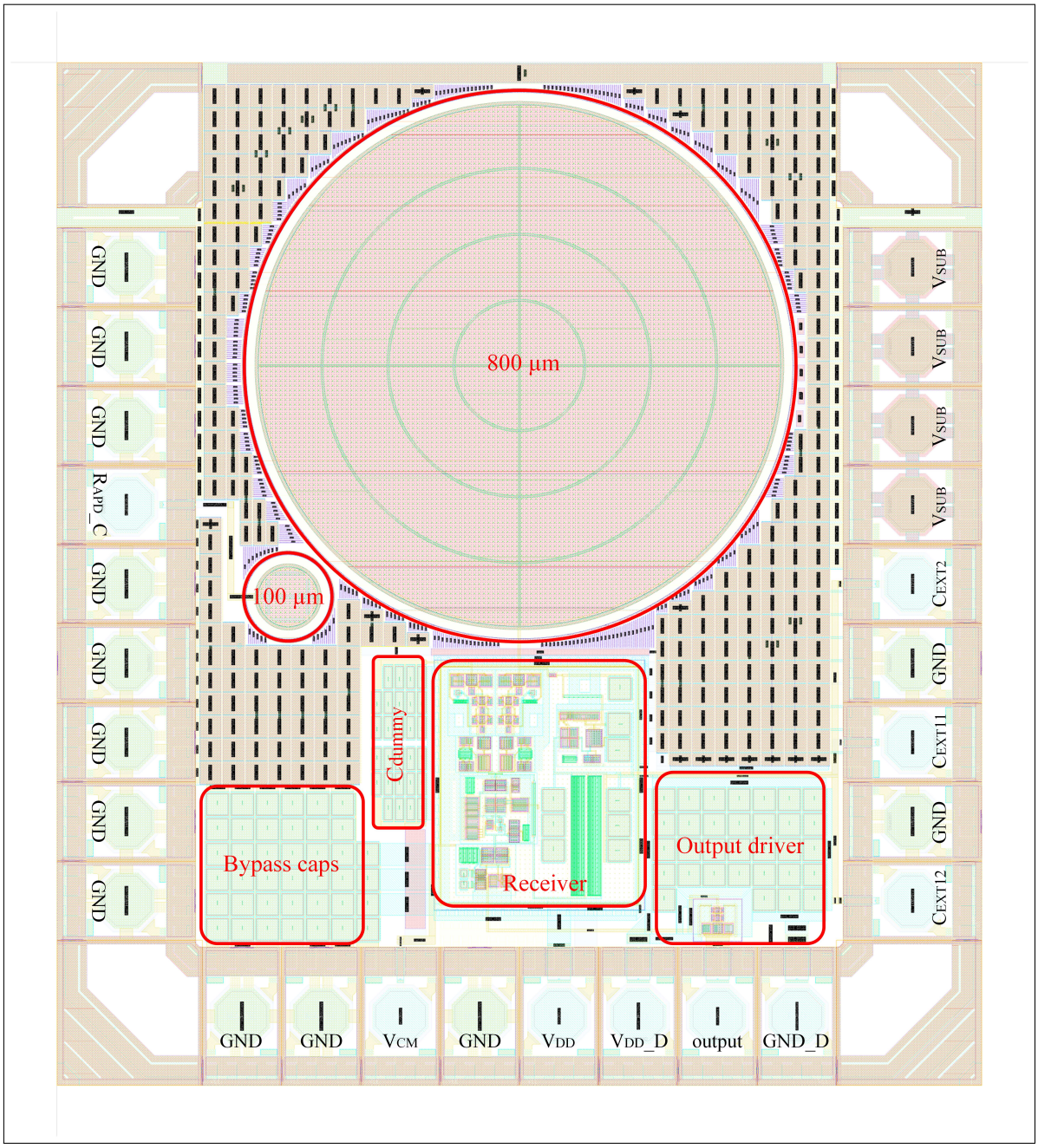


Fig. 3.2: Floorplan of the designed OEIC.

two different supply domains, one for all the analog receiver circuitry (V_{DD}, GND), and the other one for the output driver (V_{DD}_D, GND_D). Both supply domains got bypass capacitors (each one 100 pf) to reduce voltage ripple, caused by current changes over the bond-wires. These bypass capacitors were implemented using the DMIM [6] devices, offered by the process technology, due to having the highest capacitance per area. However for bypassing V_{SUB} the DMIM were not applicable, cause their punch through threshold is specified with 18 V, which would be exceeded when biasing the

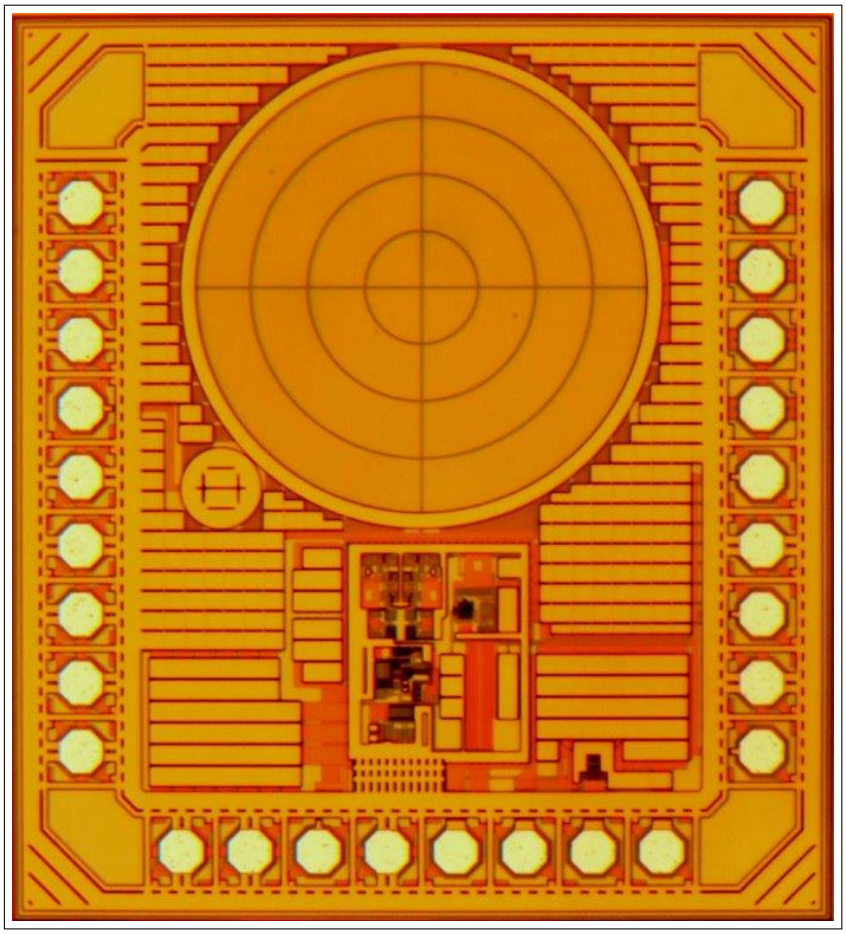


Fig. 3.3: Chip photo of the designed OEIC.

integrated APD near it's breakdown voltage. Therefore these capacitors were custom designed just by stacking the four available metal layers and connecting MET1 and MET3 as well as MET2 and MET4. Coming with the detriment of less capacitance per area, the custom capacitors are capable of sustaining larger voltages. All the residual chip area was filled with these custom capacitors between V_{SUB} and GND, resulting in a value of approximately 300 pF. Interfaces, to operate the receiver, are the output, pads for the external capacitors, V_{CM} and the cathode of the RAPD.

Chapter 4

Conclusion and Outlook

A receiver for OWC with a 800 µm fully integrated APD was designed. The chip offers a versatile method for digital audio transmission compatible to standard DAI hardware using TOSLINK specification. It is capable of processing state-of-the-art encoded sound qualities sampled with 24 bit at a rate of 192 kHz, leading to DRs of up to 4.608 Mbit/s. However as the bandwidth was designed to 4 MHz even higher DRs of up to 6 Mbit/s are receivable. The sensitivity was simulated to −62.34 dBm @ BER=10^{-9} and the overload power to −36.87 dBm leading to a dynamic range of 25.47 dB. With careful tuning of the chip's externals (via V_{CM} and C_{EXT}) even higher overload power may be achievable. A major difficulty occurring with OWC, the receiver's sensitivity to background light irradiation, was tackled by implementing an OCL. An example of dimensioning the operating range was exercised, achieving a range from 0.41 m up to 11.79 m, which should be a suitable specification for indoor application. In order to make comparison to other APD receivers possible, a figure of merit was defined in [15] as

$$FoM = 10log\frac{DR\,[\text{Gbit/s}] \cdot A_{APD}\,[\mu\text{m}^2]}{R\,[\text{A/W}] \cdot \overline{P}_{sens}\,[\text{mW}]}, \tag{4.1}$$

taking factors like the data rate, APD area, responsivity and the sensitivity into account. Table 4.1 gives an overview of performance reached by other fully integrated APD receivers. With the proposed design a very high figure of merit was achieved, but the applications differ a lot in terms of achievable DR.

Note that the results, presented for the designed receiver, are post layout simulated but not confirmed by measurements jet. Since there is no reference data regarding the 800 µm APD, some assumptions needed to be performed on key parameters like R and k_{eff}. Also the parasitics of the APD are estimated by scaling values, that were measured for smaller devices, up to the area of the implemented APD. To approve the simulated results, measurements need to be performed in the next step.

Ref.	Technology	APD-⌀ [µm]	DR [Gbit/s]	$\overline{P}_{sens}$ [dBm]	R [A/W]	FoM [dB]
[18]	0.35 µm HVCMOS	200	1	-35.5	0.41	84.34
[15]	0.35 µm BiCMOS	200	2	-32.2	0.435	83.8
[18]	0.35 µm HVCMOS	400	1	-34.7	0.41	89.56
[20]	0.35 µm BiCMOS	400	2	-30.6	0.445	88.12
[19]	0.35 µm BiCMOS	600	0.5	-33.43	0.5	90.23
This work	0.35 µm BiCMOS	800	0.006	-62.34	0.45	100.6

Tab. 4.1: Comparison of state-of-the-art large area fully integrated APD receivers.

When thinking about embedding the designed receiver into a state-of-the-art demodulation system, a possible solution would be to use the *CS8416* as decoder. It is an IEC-60958 DAI compatible IC, capable of processing sample rates from 32 kHz to 192 kHz at up to 24 Bits, with features like low-jitter clock recovery and multiple input channels. The decoded output can be converted in an analog signal by for example the *CS4344*, a 24 Bit and 192 kHz stereo Delta-Sigma DAC.

As was referred to, many times in this thesis, additional performance improvements, of the designed receiver, are conceivable when implementing an AGC for the APD biasing. The integrated RAPD serves no special purpose jet, but was added to work as a breakdown voltage reference for the SiAPD, that might be used in the future for in-situ measurements regarding the gain. In general there are three different circuit parameters that AGC possibly could improve:

- **Increase of the sensitivity:** As shown in subsection 3.2.1, for increasing background light levels, the optimal multiplication M_{opt} increases as well. By adjusting the APD bias voltage accordingly, the sensitivity for this irradiation circumstances can be maximized.
- **Increase of the overload power:** Shown in subsection 3.2.2, when the received optical power exceeds the overload power, the receiver is overloaded and therefore the BER starts to decrease. Since it is proportional to the inverse of M, a reduction of the APD multiplication implies an increase of the overload power. With this method, the dynamic range of the receiver could be elevated by several dB.
- **Temperature independency:** Shown in section 2.4, the breakdown voltage of an APD varies strongly with changes in temperature, which implies also an

altering multiplication. To ensure the receiver operates as specified in volatile environmental conditions, an automated method to stabilize the gain is advisable.

However to implement an AGC several challenges, like measure currents on the pA scale, will have to be seized.

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Appendices

Appendix A

Additional circuit information

A.1 Noise figure of a BJT (subsection 1.4.6)

The equivalent input noise densities for BJT, including $\sim f^2$ phenomena, are derived in [26], as

$$|u_{n,i}(f)|^2 = 2qI_{C,op}\left[\left(\frac{1}{g_m^2}+\frac{R_B^2}{\beta}\right)\left(1+\frac{f_c(1/f)}{f}\right)+R_B^2\left(\frac{f}{f_T}\right)^2\right]+4k_BT_0R_B \tag{A.1}$$

and

$$|i_{n,i}(f)|^2 = 2qI_{C,op}\left[\frac{1}{\beta}\left(1+\frac{f_c(1/f)}{f}\right)+\left(\frac{f}{f_T}\right)^2\right]. \tag{A.2}$$

The expression for the noise figure is achieved by applying (A.1) and (A.2) onto (1.12), which gives

$$\begin{aligned} F_{BJT}(f) = 1+\frac{R_B}{R_0}+&\left[\frac{2qI_{C,op}}{4k_BT_0}\left(\frac{1}{R_0}\left(\frac{1}{g_m^2}+\frac{R_B^2}{\beta}\right)+\frac{R_0}{\beta}\right)\right]\left(1+\frac{f_c(1/f)}{f}\right)\\ &+\left[\frac{2qI_{C,op}}{4k_BT_0}\left(\frac{R_B^2}{R_0}+R_0\right)\right]\left(\frac{f}{f_T}\right)^2 \end{aligned} \tag{A.3}$$

A.2 Additional circuit parameters

	BJT-TIA	MOS-TIA
LTin/mTin	2 µm/1	-
Win/Lin	-	92 µm/1 µm
Rfb	44 kΩ	23.5 kΩ
Cfb	10 fF	
RC	4.9 kΩ	-
RD	-	3.1 kΩ
LT1, LT2	2 µm	
mT1, mT2	1	
W1, W2	10 µm	
L1, L2	1 µm	

Tab. A.1: Circuit parameters of the investigated BJT-TIA and MOS-TIA (section 2.3).

	SiAPD	DAPD
L1	5.2	
L2	13.75	
L3	8.3	
L4	3	
L5	790	90

Tab. A.2: Dimensions of the used APDs in µm (section 2.4).

Appendix B

MATLAB code

Code for calculation of the receiver sensitivity:

```
clear all
close all
slCharacterEncoding('UTF8')
%%

keff=0.1;                       %ionization coefficient ratio
M=1;                            %declaring M as variable
PAPD1 = 1e-9;                   %irradiated optical power
Q=5.997;                        %BER=1e-9
ER=1000;                        %extinction ratio
R=0.45;                         %responsivity
iBL=1e-6;                       %Background light current
BW=3.994e6;                     %receiver bandwidth
nWhite=1.5e-25;                 %white noise TIA
q=1.602e-19;                    %electron charge
Tr=300;                         %temperature of MOCL's channel

muCox = 225.84e-6;              %Process constant
kB=1.38064852e-23;              %Boltzmann constant
kD=1;                           %Drain noise factor
W=5e-6;                         %MOCL width
L=0.35e-6;                      %MOCL gate length

PAPD=PAPD1*(1+1/ER)/2;          %average power
ipp=PAPD1*R*M;
PAPD0=PAPD1/ER;

for M = 1:1:10000

iAPD_DC_signal=(PAPD1/2)*(1+1/ER)*R*M;
```

```
iAPD_DC=iAPD_DC_signal+iBL;

F_EX=keff*M+(1-keff).*(2-1/M);

gm=sqrt(2*muCox*W/L*iAPD_DC);

in_el=nWhite*BW;
in_mos= 4*kB*Tr*kD*gm*BW;

in_APD1=M.*2*q*(PAPD1*R.*M+iBL/M)*F_EX*BW;
in_APD0=M.*2*q*(PAPD0*R.*M+iBL/M)*F_EX*BW;

in_el_rms=sqrt(in_el);
in_mos_rms=sqrt(in_mos);
in_APD1_rms=sqrt(in_APD1);
in_APD0_rms=sqrt(in_APD0);


in_rms1=sqrt(in_el+in_mos+in_APD1);
in_rms0=sqrt(in_el+in_mos+in_APD0);

i_sens(M)=Q*(in_rms1+in_rms0);
P_sens=(Q*(in_rms1+in_rms0))/(2*R*M);

A=i_sens(M)-PAPD1*R*28;
P_sens_dBm(M)=10*log10(P_sens/1e-3);

end

%Plotting:
A=i_sens-PAPD1*R*28;
figure(3)
plot(P_sens_dBm(:),'Linewidth',1)
hold on
plot(find(P_sens_dBm==min(P_sens_dBm)),min(P_sens_dBm),'kx','
    Linewidth',1.5)
hold on
grid on
set(gca, 'XScale', 'log')
xlabel('M','Interpreter','Latex','FontName','Times','FontSize'
    ,12)
ylabel('$\bar{P}_{sens}$ [dBm]','Interpreter','Latex','FontName',
    'Times','FontSize',12)
find(P_sens_dBm==min(P_sens_dBm))
```

```
min(P_sens_dBm)
```

Code for calculation of the operation range:

```
clear all;
close all;
slCharacterEncoding('UTF8')

Papd=0.5e-9;     %incident optical Power of the APD that should be
    achieved
Prc=1e-3;        %optical Power of the RCLED
a=1:0.5:10;      %angle of radiation
Aapd=5.0265e-7; %for 800um diameter
M=54;            %Multiplication factor of the APD
R=0.45;          %Responsivity of the APD

arad=(2.*pi.*a)/360; %angle in radiant
SR=4.*pi.*sin(arad/4).*sin(arad/4); %Steradiant in dependence of
    alpha
r=sqrt((Prc*Aapd)./(Papd*SR)) %distance between the RCLED and the
    APD to meet the specifications
w=r.*tan(arad) %Radius of the light cone in distance r


rvar=0.41;
p=(Prc*Aapd)./(rvar.^2*SR);
p(10)
iapd=R*p(10)*M
```

Code of Conduct

Hiermit erkläre ich, dass die vorliegende Arbeit gemäß dem Code of Conduct – Regeln zur Sicherung guter wissenschaftlicher Praxis (in der aktuellen Fassung des jeweiligen Mitteilungsblattes der TU Wien), insbesondere ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel, angefertigt wurde. Die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet. Die Arbeit wurde bisher weder im In– noch im Ausland in gleicher oder in ähnlicher Form in anderen Prüfungsverfahren vorgelegt.

Christoph Gasser
Wien, 1. Oktober 2020