

#### DISSERTATION

### Radiation Hardness Characterization of CMOS sensors for the ATLAS ITK Pixel at HL-LHC and Future Trackers

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## Kurzfassung

Das ATLAS Experiment ist eine von vier großen Detektoranlagen, die am LHC installiert wurden. Es wurde als Allzweck-Detektorsystem entworfen um Proton-Proton Kollisionen bei Schwerpunktsenergien von bis zu 14 TeV und einer Ereignisrate von 40 MHz zu Parallel zur Installation der 'High Luminosity' Erweiterung des LHC untersuchen. (HL-LHC) werden auch die Detektorsysteme in ATLAS ab 2025 umfassend erneuert. Im Zuge dieser Erweiterung wird unter Anderem der bisherige 'Inner Detektor' (ID) durch den neuen 'Inner Tracker' (ITk) ausgetauscht. Dabei vervielfacht sich die Fläche, die mit Pixel-Detektoren ausgekleidet werden muss, um beinahe das 7-fache von 1.8 auf  $12 \,\mathrm{m}^2$ . Monolithische aktive Pixelsensoren (MAPS), die mit industriellen Standardprozessen hergestellt werden können, bieten dabei eine vielversprechende Alternative zur etablierten Hybrid-Pixel-Technologie und versprechen eine signifikante Reduktion der Produktionskosten bei einer gleichzeitigen Erhöhung der Produktionsrate. Zudem kann durch die monolithische Bauweise das Detektormaterial reduziert und die Streuung von Kollisionsprodukten am Detektor verringert werden.

Basierend auf dem ALPIDE Design für das 'Inner Tracking System' (ITS) des ALICE Experiments wurde ein monolithischer Pixelsensor entwickelt, dessen Dopingprofile eine zusätzliche planare n-dotierte Schicht enthalten. Diese Schicht erzeugt eine Grenzschicht von n-dotiertem auf p-dotiertes Silizium, die sich über die gesamte Pixelmatrix erstreckt und die die vollständige Verarmung des Sensorvolumens bereits bei niedrigen Sperrspannungen ermöglicht. Die Ladungssammlung erfolgt daher vollständig durch Drift. Dadurch wird die Signalverarbeitung beschleunigt, der Ladungsverlust durch Rekombination im Sensor reduziert und die Strahlungsresistenz des Detektors erhöht. In Kooperation mit dem Halbleiterhersteller TowerJazz wurden mehrere Generationen von Pixeldetektoren mit dem neuen Sensordesign mit deren 180 nm CMOS Prozess hergestellt. Ziel dieser Arbeit war es, die Leistungsfähigkeit dieser Pixeldetektoren in Strahltests zu studieren, deren Weiterentwicklung voranzutreiben und zu zeigen, dass diese die Anforderungen, die sich für die äußeren Lagen des ATLAS ITk durch die Installation des HL-LHC ergeben, erfüllen können.

Zu Beginn wurden Tests am TowerJazz Investigator, einem analogen Testdetektor mit

vielen verschiedenen Pixeldesigns, durchgeführt um eine optimale Dimensionierung des Pixelsensors zu finden. Unter den getesteten Pixel-Designs erzielte das Layout mit einer Pixelgröße von  $30 \times 30 \,\mu\text{m}^2$  gemeinsam mit einer  $3 \,\mu\text{m}$  Sammelelektrode, die von einer kleinen Aussparung des 'deep p-wells' von ebenfalls  $3 \,\mu\text{m}$  umgeben ist, die besten Ergebnisse. Es zeigt sich jedoch auch, dass dieses Layout nach Bestrahlung sehr stark an Leistung verliert. Das Signal-Rausch-Verhältnis sinkt um etwa 75% und die durchschnittliche Zahl der Pixel, die bei einem Teilchentreffer ein Signal registrieren, auch genannt 'cluster size', verringert sich um etwa 25%. Bei noch höherer Bestrahlung werden Anzeichen erkennbar, dass die Detektionseffizienz am Pixelrand, also bei großen Abständen zur Sammelelektrode, zunehmend abnimmt. Zum Zeitpunkt der Messungen wurde dies durch eine erhöhte Streuung der Ladung zu mehreren benachbarten Pixeln, genannt 'charge sharing', erklärt wodurch der wahrscheinlichste Wert der Signalamplitude im Sensor verringert wird.

Aus den Ergebnissen mit dem TowerJazz Investigator wurde das Pixel-Layout für den ersten großformatigen monolithischen Pixeldetektor 'MALTA' (Monolithic from ALICE to ATLAS) abgeleitet. Dieser Detektor beherbergt eine  $512 \times 512$  Pixel-Matrix mit einer Gesamtfläche von etwa  $2 \times 2 \text{ cm}^2$ . Die Pixel haben eine Größe von  $36.4 \times 36.4 \,\mu\text{m}^2$  und eine 2-3 µm große Sammelelektrode die von einer 3-4 µm breiten Aussparung des 'deep p-wells' umgeben ist. Sie beherbergen eine analoge CMOS-Schaltung (auch analoges 'front-end') zur Verstärkung und Diskriminierung von Sensorsignalen und eine digitale CMOS-Schaltung (digitales 'front-end') für die Datenauslese an die Chip-Peripherie. Die MALTA-Matrix wird asynchron ausgelesen wodurch kein Taktsignal (Englisch: 'Clock') im Pixel benötigt und der Stromverbrauch der Elektronik verringert wird. Durch Strahltests mit MALTA konnte die Verringerung der Detektionseffizienz am Pixelrand bestätigt und die Ursache dafür festgestellt werden. Aufgrund der schwachen lateralen Komponente des elektrischen Felds im Sensor werden Ladungen am Pixelrand nur langsam zur Sammelelektrode transportiert. Dies führt nach Bestrahlung zu erheblichen Ladungsverlusten durch Rekombination. Die ungünstige Feldkonfiguration kommt durch den 'deep p-well' zustande, der vor Allem bei kleinen Ausparungen um die Sammelelektrode das laterale elektrische Feld stark verringert. Zusätzlich wurde eine unerwartet hohe Varianz des Detektionsgrenzwertes der einzelnen Pixel festgestellt. Diese Varianz verhindert, dass MALTA bei ausreichend niedrigen Detektionsgrenzwerten betrieben werden kann ohne gleichzeitig die Rauschtreffer-Rate stark zu erhöhen.

Um diese beiden Probleme zu lösen wurden Modifikationen der planaren n-dotierten Schicht und Neudimensionierungen einzelner Komponenten im analogen front-end in einem neuen Prototyp namens 'miniMALTA' implementiert und getestet. Die Resultate aus Strahltests zeigen, dass das miniMALTA-Design die Anforderungen für die äußerste Lage des ATLAS ITk im Bezug auf Detektionseffizienz und Strahlungsresistenz erfüllen kann.

Schließlich wurde ein neuer großformatiger Prototyp entwickelt, der im Gegensatz zu seinen Vorgängern nicht auf Wafern mit hochresistivem epitaktischem Silizium sondern aus Czochralski-Silizium hergestellt und daher als 'MALTA CZ' bezeichnet wurde. Das Substrat dieser Wafer zeichnet sich durch eine kontinuierliche, niedrige p-Dotierung aus die es erlaubt, die Verarmungszone im Sensor durch Erhöhen der Sperrspannung zu verbreitern. Dadurch vergrössert sich das sensitive Volumen und die Ladungsmenge, die bei einem Teilchentreffer gesammelt wird. Dies wiederum bewirkt eine geringere Verzögerung zwischen der Deposition von Ladungsträgern und der Detektion eines Signals im Pixel, auch genannt 'time-walk' und verbessert das zeitliche Auflösungsvermögen des Detektors. Zudem beinhaltet MALTA CZ die neuen Modifikationen der planaren n-dotierten Schicht, die die Ladungssammlung verbessern. Wieder kann mittels Strahltests gezeigt werden, dass MALTA CZ selbst ohne ein verbessertes analoges front-end die Anforderungen für die äußeren Lagen des ITk bezüglich Strahlungsresistenz und Detektionseffizienz erfüllt. Zudem weisen die Resultate in dieser Arbeit auf ein stark verbessertes zeitliches Auflösungsvermögen des Detektors gegenüber MALTA hin.

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KURZFASSUNG

### Abstract

The ATLAS experiment is one of the four large detectors installed at the LHC. It was designed as an all-purpose detector to study proton-proton collisions at center-of-mass energies of up to 14 TeV and an event rate of 40 MHz. In parallel to the installation of the High Luminosity upgrade at the LHC (HL-LHC) there will also be an extensive upgrade to ATLAS' sub-systems starting from 2025. Part of this upgrade will be the replacement of the current Inner Detector (ID) by the new Inner Tracker (ITk) which will increase the area that needs to be covered by pixel detectors by a factor of nearly 7 from 1.8 to  $12 \text{ m}^2$ . This makes monolithic active pixel sensors (MAPS), produced in industrial standard processes, an interesting alternative to established hybrid pixel detectors which promises a significant reduction in production cost and an increase in production throughput. Additionally, monolithic detectors by the detector.

Based on the ALPIDE design for the 'Inner Tracking System' (ITS) of the ALICE experiment a new monolithic pixel sensor was developed which features a modification to its doping profiles to add an additional planar n-doped layer. This layer creates a n-p-interface that spans the entire pixel matrix and and allows the full depletion of the sensor even at a low reverse bias. Thus charge can be collected entirely via drift which speeds up charge collection, reduces charge loss via trapping and thus improves radiation hardness. In cooperation with the TowerJazz foundry several generations of pixel detectors were produced in their 180 nm CMOS process. The goal of this work was to study the performance of these detectors in beam tests, enable their further development and show that they can meet the requirements of the ATLAS ITk and the HL-LHC.

First beam tests were done with the TowerJazz Investigator, an analogue test detector featuring many different pixel flavors, to find the optimal pixel dimensions. Among the tested pixel designs the best performance was achieved with a pitch of  $30 \times 30 \,\mu\text{m}^2$  and a  $3\,\mu\text{m}$  collection diode with a  $3\,\mu\text{m}$  spacing of the deep p-well around it. However, results also show that the performance of this design diminishes significantly after irradiation. The signal-noise-ratio (SNR) drops by roughly 75% and the average number of triggered pixels per particle hit, the so-called 'cluster size' reduces by roughly 25%. At even higher

irradiation levels there are signs of diminishing detection efficiency at the pixel borders at large distances from the collection diode. At the time, this was explained by the spread of deposited charge to several neighboring pixels, so-called 'charge sharing', which reduces the most probable value (MPV) of the signal amplitude in the sensor.

The results obtained with the Investigator guided the pixel design of the first full-sized pixel detector 'MALTA' (Monolithic from ALICE to ATLAS). This detector features a  $512 \times 512$  pixel matrix with a total surface area of  $2 \times 2 \text{ cm}^2$ . The pixels have a  $36.4 \times 36.4 \,\mu\text{m}^2$  pitch, a 2-3  $\mu\text{m}$  collection diode and a spacing of the deep p-well around the diode of 3-4 µm. The pixels feature an analogue front-end comprising of an amplifier and a discrimination stage and a digital front-end for the matrix readout. The pixel matrix readout is asynchronous and thus no clock in the pixel is necessary which reduces power consumption. Beam tests with MALTA confirmed the low detection efficiency at the pixel border and identified the cause. Due to a weak lateral component of the electric field in the sensor charge at the pixel border is only collected slowly. This causes significant charge loss due to trapping after irradiation. The unfavorable field configuration is caused by the deep p-well which weakens the lateral electric field especially for small spacings. Additionally, a large variance of the detection threshold was observed. Thus the detector could not be operated at its design threshold without also increasing the noise hit rate beyond manageable levels.

In order to address both these problems modifications to the planar n-doped layer and a re-dimensioning of several components of the analogue front-end were implemented in a new prototype called 'miniMALTA' and tested. Beam test results show that his detector can meet the requirements for the outermost layer of the ITk in terms of detection efficiency and radiation hardness.

Finally, a new full-sized prototype 'MALTA CZ' was produced on Czochralski silicon as opposed to previously used high-resistivity epitaxial silicon. The wafer substrate of this detector is continuously low p-doped and allows to increase the width of the depletion region in the sensor by increasing the reverse bias. This increases the sensor volume and thus the amount of collected charge. In turn this reduces the time that passes from the deposition of charge to the detection of a signal, the so-called 'time-walk', and improves the temporal resolution of the detector. Additionally, MALTA CZ features the modifications to the planar n-layer which improve charge collection. Again, the results from beam tests show that MALTA CZ reaches ITk requirements for the outer pixel layers even without an improved analogue-front end in terms of efficiency and radiation hardness. Further, results shown in this work indicate a significant improvement of the timing performance compared to MALTA.

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### Chapter 1

### Introduction

The field of High Energy Physics is concerned with furthering our understanding of the fundamental building blocks of nature. During the last century a veritable *particle zoo* has been discovered through great efforts by theoretical and experimental physicists. The theoretical framework which most consistently describes all these particles and their interaction is called the Standard Model which has successfully predicted the existence of several particles and has most recently been confirmed yet again with the discovery of the Higgs Boson[1][2].

Whereas the first elementary particle was discovered by J.J. Thompson in his laboratory at the end of the 19th century — electrons in the form of cathode rays — the Higgs Boson was only discovered in 2012 and the largest particle accelerator, the Large Hadron Collider (LHC) at CERN (incidentally the largest machine ever built), was necessary to do it. Over the course of a century the need to build bigger and bigger accelerators and detectors to discover the rarest and most short lived particles has facilitated tremendous technological progress in many fields of research besides high energy physics.

One crucial element for modern particle physics experiments are detectors which are capable of measuring incident particles with high spatial and temporal precision and accuracy. These detectors are often made from silicon, feature a pixel structure similar to that of camera sensors and are installed very close to the beam interaction point within a large particle detector system such as the big four experiments at CERN: ATLAS (A large ToroidaL ApparatuS), CMS (Compact Muon Solenoid), ALICE (A Large Ion Collision Experiment) and LHCb (LHC Beauty). Since its start of operation the LHC has already been pushed past its design performance specifications and further upgrades are to come. These upgrades will result in higher beam luminosities, radiation levels and data rates. Consequently detectors with increased precision, radiation hardness and rate capability are needed as well and this in turn drives the development of increasingly performant silicon pixel detectors. Recently, depleted monolithic active pixel sensors (DMAPS) which are entirely fabricated using complementary metal-oxide-silicon (CMOS) technology have been investigated to design a cheap and light silicon pixel detector for the upcoming High-Luminosity upgrade of the LHC and its experiments in 2025. This thesis focuses on the ongoing effort to manufacture a silicon DMAPS with a small collection electrode design which meets the requirements for the outermost layer of ATLAS Inner Tracker in collaboration with the TowerJazz foundry and their 180 nm CMOS process. The major challenge is to reach sufficient radiation hardness for the chip to stay operational during its life time.

## Chapter 2

### High Energy Physics at CERN

The Conseil Européen pour la Recherche Nucléaire is the largest particle physics research facility world wide. It was initially founded in 1954 by 12 founding member states and is located at the border between Switzerland and France close to Geneva. By now CERN has 23 member states and employs roughly 2500 staff members who are tasked with the administration and maintenance of CERN's facilities and infrastructure. About 12000 scientists work at CERN as *Users* in a multitude of scientific disciplines. The vast majority of scientific work focuses on high energy particle physics and beam physics. For this purpose, a large accelerator complex provides a multitude of particle beams and beam test environments.

#### 2.1 The Standard Model

The Standard Model is the basis for modern High Energy physics and has been developed, tested and confirmed throughout the second half of the 20th and the beginning of the 21st century. It describes 3 of the 4 fundamental physical forces, specifically the weak, strong and electromagnetic interaction, and classifies all known elementary particles.

As shown in figure 2.1 all matter consists of Fermions which have a spin of  $\frac{1}{2}$  and come in three generations of increasing mass. Fermions are again divided into quarks and leptons. The fundamental forces are transmitted via bosons which have an integer spin. The gluon transmits the strong interaction, the W<sup>±</sup> and Z bosons the weak and the photon the electromagnetic interaction. These bosons all have a spin of 1. The Higgs boson, which has a spin of 0, is responsible for the non-zero mass of all fermions and heavy gauge bosons of the weak interaction.

<sup>&</sup>lt;sup>1</sup>Wikimedia Commons, https://commons.wikimedia.org/wiki/File:Standard\_Model\_of\_Elementary\_Particles.svg, last accessed: 01.06.2020



#### **Standard Model of Elementary Particles**

Figure 2.1: Shown is a diagram of the known elementary particles described by the Standard Model<sup>1</sup>.

While the Standard Model was very successful in all its previous predictions there is physics beyond its scope. Most notably, the Standard Model does not incorporate General Relativity and furthermore does not provide an explanation for neutrino masses, the observed matter-antimatter asymmetry in our universe, Dark Energy or Dark Matter. In order to improve on the Standard Model increasingly precise measurements of its known parameters are necessary. Consequently, accelerators must be built which provide ever higher beam energies to look for new particles and higher luminosities to study exceedingly rare physics events. So far, this development has culminated in the construction of the LHC at CERN.

#### 2.2 Accelerators and beam facilities

CERN provides a large complex of accelerator facilities which are not only used for high energy physics research directly but also provide test beams for the research and development of new detector technologies and other fields of study. An overview of the accelerators operated at CERN is shown in figure 2.2.

The Super Proton Synchrotron (SPS) is the second largest accelerator at CERN and reaches proton beam energies of up to 450 GeV. It is part of the main accelerator chain which ends with the LHC but also provides a test beam for the large test beam area at the Prevessin site of CERN in France where a lot of the data for this thesis was recorded.

<sup>&</sup>lt;sup>2</sup>The CERN accelerator complex, https://cds.cern.ch/record/2225847, last accessed: 01.09.2020





Figure 2.2: Shown is a sketch of the accelerator complex at  $CERN^2$ .

Beams of various particle compositions and energies can be generated by aiming the initial proton beam at various targets and extracting the resulting secondary beam. This gives access to electron, pion, proton and muon beams with momenta ranging from a few tens to a few hundreds of GeV/c.

The LHC is by far the largest accelerator at CERN. It is a synchrotron roughly 100 m below ground and 26.7 km in length. The accelerator ring is divided clock-wise into 8 segments, also called 'Points' 1-8, where the LHC can be accessed, and at 4 of these points particle collisions take place and large experiments are installed. The heavy ion collision experiment ALICE is installed at Point 2 and the LHCb experiment which focuses on beauty quark and matter-antimatter asymmetry studies is located at Point 8. Between these two experiments the ATLAS general purpose detector is located at Point 1 and another general purpose detector, called CMS, is installed at the opposite side of the LHC at Point 5.

In the LHC two beams of either protons or lead ions revolve clock-wise and counter clock-wise, respectively, and cross each other at the four large experiment sites where the resulting high energy collisions are recorded. The beams are steered by 1232 superconducting magnets which generate a magnetic field of up to 8.33 T and allow beam energies of up to 7 TeV per proton and center-of-mass energies of up to 14 TeV in proton-proton collisions. The proton beams are segmented into 2808 bunches, each of which contains roughly  $10^{11}$  protons [3]. At the intersection points these bunches collide every 25 ns (a rate of 40 MHz) with an average 27 collisions per bunch crossing (called pile-up) which results in a peak luminosity of roughly  $10^{34}$  s<sup>-1</sup>cm<sup>-2</sup> which is calculated as [4]

$$L = \gamma \frac{n_b N^2 f_{rev}}{4\pi \beta^* \epsilon_n} R; \quad R = \frac{1}{\sqrt{1 + \frac{\theta_c \sigma_z}{2\sigma}}}$$
(2.1)

with variables as defined in the appendix, section A. On one hand, the luminosity L is dependent on the beam current ( $n_b$ , N) and on the other hand on beam optics ( $\beta^*$ ,  $\varepsilon_n$ , R). The coming upgrade of the LHC to the HL-LHC will improve both aspects in order to increase the luminosity by roughly an order of magnitude. The amount of data recorded in particle collision experiments is measured as the integrated luminosity in units of inverse femtobarn fb<sup>-1</sup>. Up to 2024 the LHC will collect a data set equivalent to 350 fb<sup>-1</sup>. During the life time of the HL-LHC it is expected that roughly 10 times this amount of data will be recorded.

<sup>&</sup>lt;sup>3</sup>High Luminosity LHC Project, https://project-hl-lhc-industry.web.cern.ch/content/project-schedule, last accessed: 01.09.2020



Figure 2.3: Shown is the time table for planned data runs and shutdowns of the LHC and its experiments<sup>3</sup>.

### 2.3 The High Luminosity upgrade of the LHC

A major bottleneck for the study of new and rare physics events are their extremely small cross sections. In order to improve the rate at which such events can be recorded the LHC will be upgraded to the HL-LHC [4] during *Long Shutdown 3* as shown in figure 2.3 and start operation in 2027. A comparison of the design parameters of the LHC and HL-LHC is shown in table 2.1.

The HL-LHC upgrade encompasses upgrades to several sub-systems of the LHC. In order to improve beam focusing new quadrupole magnets will be installed at ATLAS and CMS which reach magnetic fields of 12 T instead of the previous 8 T. The effective cross section of intersecting bunches will be increased by giving bunches an additional transverse momentum at the intersection point so that a constant luminosity can be maintained during the lifespan of the beam. Since the beams contain more particles machine protection must be improved and roughly half of the existing collimators at the LHC will be upgraded. Furthermore, several improved bending magnets are installed which can reach maximum field strengths of 11 T instead of the previous 8.3 T and are thus able to bend the beam over a shorter distance. This allows the installation of additional collimators. Finally, the entire accelerator chain leading up to the HL-LHC is improved. The first element of this chain, the LINAC2, was replaced by the LINAC4 in 2020.

The increased luminosity of the HL-LHC will have a significant impact on the performance requirements for LHC experiments. As a result, upgrades are planned for both, *Long* 

Table 2.1: Given below is a comparison of the design parameters of the LHC and HL-LHC for proton-proton collisions.

	LHC (design report)	HL-LHC (standard)
beam energy in collision [TeV]	7	7
bunches per beam	2808	2748
bunch population (protons per bunch) $[10^{11}]$	1.15	2.2
minimum $\beta^*$ (beam beta function, focal length)	0.55	0.2
$ \begin{array}{c} \epsilon_n \; ({\rm transverse \; normalized} \\ {\rm emittance}) \end{array} $	3.75	2.5
peak luminosity $[10^{34} \mathrm{s}^{-1} \mathrm{cm}^{-2}]$	1.18	12.6
events per bunch crossing (pile-up)	27	140
maximum line density [events/mm <sup>2</sup> ]	0.21	1.3



Figure 2.4: Shown is a rendering of the ATLAS experiment at CERN<sup>4</sup>. The whole detector system is centered around the interaction point in the middle of the image where particle collisions occur.

Shutdown 2 and Long Shutdown 3, which aim to improve, among other aspects, radiation hardness, primary and secondary vertex resolution and data rate capability compared to currently installed detectors.

### 2.4 The ATLAS detector

ATLAS is the largest experiment at CERN with a diameter of 25 m and a length of 44 m. The bulk of the experiment is arranged as a cylinder around the central interaction point. This cylinder is closed off on both sides by sets of several end-caps so that particles are also detected at small angles with respect to the beam. An image of the whole ATLAS experiment is shown in figure 2.4 and an image of ATLAS' cross section is shown in figure 2.5. The innermost section of ATLAS is called the Inner Detector (ID) and contains, ordered by increasing distance from the interaction point, the pixel detector, the semiconductor tracker (SCT) (silicon strip detectors) and the transition radiation tracker (TRT). The outer section of ATLAS comprises of the electromagnetic calorimeter, the hadronic calorimeter and finally the muon spectrometer.

Throughout the entire ID a solenoid magnet provides a 2 T field which is almost uniform in its strength and direction and allows for precise measurements of the momentum of

<sup>&</sup>lt;sup>4</sup>ATLAS rendering, https://cds.cern.ch/record/1095924, last accessed: 01.09.2020

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Figure 2.5: Shown is a cross section of the ATLAS detector system<sup>5</sup>. Inner detector systems include the silicon pixel and strip detectors and transition radiation detectors. Outer segments house the electromagnetic and hadronic calorimeters as well as the muon chambers.

charged particles there. A toroidal magnet system which consists of two end-caps in front of and behind the ID and a large surrounding barrel magnet which consists of eight large air-core barrel loops provides an additional magnetic field outside of the ID albeit a less homogeneous one.

#### 2.5 The ATLAS Inner Tracker upgrade (ITk)

As part of the ATLAS upgrade planned in 2025, the new Inner Tracker [5] will be installed to replace the current Inner Detector. The existing ID is nearing its end of life and cannot withstand the expected radiation levels in the HL-LHC which correspond to a total integrated luminosity of 4000 fb<sup>-1</sup>. Similarly, it can cope at most with a pile-up of roughly 50 before the buffering between the pixel front-end and the read-out driver saturates and causes a loss of data. The lower granularity of the current detector will also lead to a very high occupancy. Consequently, it would be very hard to resolve nearby tracks in the Semiconductor Tracker and the occupancy of the Transition Radiation Tracker would reach almost 100%. Finally, the implementation of a track trigger is needed to lower trigger thresholds and improve physics performance. The current Inner Detector does not support such a trigger.

<sup>&</sup>lt;sup>5</sup>ATLAS cross section, https://cds.cern.ch/record/1505342, last accessed: 01.09.2020



Figure 2.6: Shown is the cross section of the ATLAS ITk 'inclined duals' layout[5, p. 8].

The goal of the ITk is to provide an improved tracking performance while coping with the harsh conditions of the HL-LHC environment. For this reason, the TRT will be replaced by more granular silicon strip detectors. The SCT as well as the entire current pixel detector will be replaced by a new pixel tracker with a significantly reduced pixel size. The resulting improvements to the detector's resolution provide the necessary track reconstruction efficiency for an expected maximum pile-up of 200 and a line-density of up to 1.3 events/mm. In order to keep the number of fake tracks low for very high pile-ups an average 13 pixel hits per track for pseudorapidities  $\eta < 2.7$  and 9 pixel hits for  $\eta >$ 2.7 is necessary. The resulting 'inclined duals' design of the pixel detector of the Inner Tracker thus features 5 pixel and 4 strip barrel layers and several end-cap rings. The entire detector extends roughly 3.0 m in both directions from the interaction point to ensure full coverage (hermiticity) for pseudorapidity up to  $\eta = 4.0$ . A visualisation of the cross section of the inclined duals design can be seen in figure 2.6.

The surface area of the pixel detector in the ITk increases considerably from  $1.8 \text{ m}^2$  to  $12.74 \text{ m}^2$  which will be a main driver for production cost. Consequently, DMAPS chips produced in an industrialized CMOS process, like those studied in this work, may provide an interesting alternative to state-of-the-art hybrid pixel detectors. Besides the possibility to significantly lower production cost monolithic pixel chips also allow to reduce the material budget and consequently improve the performance of the tracker

Table 2.2: Given below is a comparison of the maximal 1 MeV neutron equivalent fluence for the innermost and outermost barrel layer of the ATLAS ITk in the 'inclined duals' design. A safety factor of 1.5 has been included. The innermost layer is replaced after  $2000 \text{ fb}^{-1}$  [6] (half the planned integrated luminosity for the HL-LHC).

	innermost layer	outermost layer
radius [cm]	3.9	28
integrated luminosity $[fb_{-1}]$	2000	4000
fluence $[10^{14}~1{\rm MeV}~n_{\rm eq}/{\rm cm}^2]$	50	15
dose [MGy]	500	80
hit rate $[MHz/cm^2]$	2000	100-200

due to reduced scattering of collision products. The main obstacle is to meet the ITk requirements in terms of radiation hardness and consequently the chips are designed for an implementations in the outer layers of the ITk (4th and 5th) where radiation levels are lower. A short summary of the requirements for the innermost and outermost layers in terms of radiation levels is given in table 2.2.

### Chapter 3

# Energy loss of charged particles in matter

Any measurement in a particle physics experiment such as ATLAS is based on the interaction of particles with the material of its detectors. Invariably the particles will lose some or all of their energy in whatever matter they encounter along their way. If this matter is part of the sensitive volume of a detector, a measurement can be made. If a particle is measured by several detectors along its path, it is vitally important that measurements preserve the particle's properties as much as possible until the final detector is reached (which is usually a calorimeter). These requirements dictate the physical structure of an experiment like ATLAS and its detector components. Specifically, pixel detectors must be build as light as possible so as to minimize the scattering of impinging particles and provide an accurate and precise measurement of the particles' position in time and space. It is thus important to understand how energy is deposited in a pixel detector and study the processes involved.

In the case of moderately relativistic charged heavy particles (i.e. particles heavier than electrons) the Bethe-Bloch formula

$$-\left\langle \frac{dE}{dx}\right\rangle = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} ln \frac{T_{max}}{T_{min}} - \beta^2 - \frac{\delta(\beta\gamma)}{2} - \frac{C(\beta\gamma, I)}{Z}\right]$$
(3.1)

$$T_{min} = \frac{I^2}{2m_e c^2 \beta^2 \gamma^2} \propto \frac{1}{b_{max}^2} \propto \frac{1}{\gamma^2}$$
(3.2)

$$T_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e/M + (m_e/M)^2}$$
(3.3)

with all physical symbols as given in the appendix, section A.

<sup>&</sup>lt;sup>1</sup>Review of Particle Physics, https://link.aps.org/doi/10.1103/PhysRevD.98.030001 (Figure 33.1), last accessed: 01.09.2020



Figure 3.1: Stopping power of copper for muons at various energies<sup>1</sup>. Correction terms must be applied at very low values (shell corrections) and very high values (radiative losses) of  $\beta\gamma$ .



Figure 3.2: Shown is the stopping power of silicon for several particles common in beam tests. Calculations were done using Equation 3.1. No shell corrections or radiative losses were considered. For electrons the stopping power was calculated with the formula for Møller scattering  $in^2$ .

It describes the mean rate of energy loss, the so called stopping power, in the region 0.1  $\leq \beta \gamma \leq 1000$  to within a few percent for intermediate-Z materials [7]. It is derived from the assumption, that charged particles in matter lose their energy to electrons of the target atoms via excitation and ionization. This is true until radiative processes begin to take over at values of  $\beta \gamma > 1000$ . The stopping power of copper for muons is shown in figure 3.1 and its most important features are briefly discussed here:

Minimum ionizing particle - MIP As can be seen in figure 3.1, the stopping power reaches a minimum at  $\beta \gamma \approx 3$ . This means that particles are minimally ionizing at a kinetic energy that is roughly equal to three times their rest mass.

**Delta electrons** Delta electrons ( $\delta$ -electrons) are produced when projectile particles collide head on with an electron in the medium which is the case for very small impact parameters. An amount of energy close or equal to  $T_{max}$  is transferred and thus  $\delta$ -electrons have very high energies and become ionizing particles themselves.

Stopping power at low energies At low energies the stopping power is dominated by the  $1/\beta^2$  term. In this range the interaction time between target and projectile is

 $<sup>^2 \</sup>rm Review of Particle Physics, https://link.aps.org/doi/10.1103/PhysRevD.98.030001 (Figure 33.8), last accessed: 01.09.2020$ 

comparatively long and at very low energies it is not valid anymore to assume that the electrons in the target medium are free. So-called shell corrections are necessary and these are added as the term C/Z in the square brackets of Equation 3.1. At projectile energies below MIP range the energy loss increases sharply and produces larger signals in a detector. This effect can be used to test a the stability of CMOS circuits where large charge deposits can lead to parasitic currents which are dangerous for the detector (discussed in section 4.2.4).

Stopping power at high energies At higher energies multiple effects must be taken into account. The projectile particle becomes increasingly relativistic and its electric field is flattened, i.e. stretched in the transverse and squeezed in the longitudinal direction. This increases the maximum impact parameter  $b_{max}$ , lowers  $T_{min}$  accordingly, and the logarithmic term in Equation 3.1 increases. The corresponding increase in energy loss is corrected by the density correction  $\delta$  which takes into account that the electric field of the projectile is shielded by the polarization of the target medium. This polarization is the result of a coherent oscillation of the electrons in the target medium which is called the plasma frequency

$$\omega_P = \sqrt{\frac{n_e e^2}{\epsilon_0 m_e}}.$$
(3.4)

The energy of this oscillation  $\hbar\omega_{\rm P}$  then replaces  $T_{\rm min}$ .

**Stopping power for electrons** For electrons the stopping power can be calculated with a formula that is similar to Bethe-Bloch but with some modifications due to the fact that now the projectile particle has the same mass and charge as the electrons in the medium. Additionally, while energy loss via ionization still occurs, energy loss via bremsstrahlung must be considered as well. At low energies electron shell corrections must be considered while for higher energies discrete processes such as Møller scattering ( $e^-e^- \rightarrow e^-e^-$ ) and Bhabha scattering ( $e^+e^- \rightarrow e^+e^-$ ) can be used [7]. The energy loss for an electron MIP is fairly similar to that of more massive particles, albeit at much lower momenta as shown in figure 3.2.

**Energy loss in thin layers** In the case of silicon DMAPS it is important to understand how the energy loss is affected by thin layers because the sensitive volume is likely only a few 10s of  $\mu$ m wide. Energy deposition as described by the Bethe-Bloch formula describes the mean energy loss per unit distance in a material. However, in thin layers and especially for higher energies the distribution of deposited energy per interaction has



Figure 3.3: Shown is the distribution of the total energy loss per distance for various thicknesses of the target material. While the mean energy loss based on the Bethe-Bloch formula does not depend on changes in thickness x this is not the case for the most probable value of the total energy [7].

a very significant high energy tail due to processes that are characterized by small cross sections and high energy transfers. A particle's energy loss cannot be treated as a uniform continuous process anymore because the number of interactions before the projectile leaves the material can fluctuate significantly. For example, in the case of  $\delta$ -electrons it is possible that instead of depositing their energy in the sensor they leave the detector before they interact. This causes a reduction of the energy deposit at very high energies called the Fermi plateau. For material thicknesses at the order of 100 µm the Landau distribution is sufficient to model the energy loss. However, to describe energy loss in very thin layers (at the order of ten microns) a more accurate model was developed in [8] and improved, for example, in [9]. An important feature of energy loss in thin layers is that the most probable value for the energy loss per unit distance changes for thinner layers as shown in figure 3.3.

In the specific case of detectors discussed in this work, the sensor thickness is  $25 \,\mu\text{m}$ . The corresponding energy deposition distributions were simulated with the Allpix<sup>2</sup> simulation tool [10] which utilizes the Geant4 framework [11]. Results for electrons with a momentum of 3 and 4 GeV and pions with a momentum of 180 GeV are shown in figure 3.4. These beam configurations were used to record the data on which all the results presented in this work are based. It can be seen that the most probable and mean energy deposit for all three configurations varies less than 1%. The working function of an electron-hole pair



Figure 3.4: Shown are the energy deposit distributions for electrons with a momentum of 3 GeV/c (left) and 4 GeV/c (middle) and for pions with a momentum of 180 GeV/c (right). These beams were used to record the data on which the results shown in this thesis are based. Due to the very thin silicon layer the distribution deviate from the Landau distribution. The most probable value was therefore determined by a narrow gaussian fit around the peak. It can be seen that for all three particles the deposited energy is equal to within 1%.

in silicon is 3.6 eV. With an approximate energy deposition of 5740 eV this equates to a most probable charge deposit of roughly 1600 e.

#### 3.1 Particle detection with silicon

Pure silicon is a metalloid semiconducting material. Its atomic number is 14 and it is in the same group of the periodic table as carbon (above), germanium, tin and lead (below). Similar to its group neighbors it has a face-centered diamond-cubic crystalline structure. It is generally quite unreactive but does have a high chemical affinity for oxygen. It is also the second most abundant element on Earth after oxygen. Some of its more relevant characteristics are compared to other semiconductors used in electronics applications in table 3.1.

There are several advantages of silicon that make it more popular than other semiconductors for the production of integrated circuits. Most important among them are its native insulator  $SiO^2$ , its good thermal conduction which allows to densely pack transistors and its abundance and cheap production cost. In addition silicon is by far the most established material to build CMOS circuits. Gallium arsenide is commonly used for high-frequency applications due to its high electron mobility. However, it has a high impurity concentration and no native insulator. Germanium is increasingly used in

	Si	Ge	GaAs
intrinsic charge carrier concentration (pure) [cm <sup>-3</sup> ]	$\approx 10^{10}$	$\approx 2.4 \ 10^{13}$	$\approx 2.1 \ 10^6$
band gap $[eV]$	1.12	0.66	1.42
radiation length [cm]	9.36	2.30	2.29
e/h generation [eV]	3.65	2.96	4.35
electron mobility $[\rm cm^2/Vs]$	1450	3900	8500
hole mobility $[\rm cm^2/Vs]$	500	1800	400
specific resistivity $[\Omega cm]$	$2.3 \ 10^5$	47	$10^{8}$

Table 3.1: Comparison of the semiconductor properties of silicon [12] at room temperature (300 K).

combination with silicon for high-frequency applications instead of gallium arsenide. It is however far less abundant than silicon.

The concentration of charge carriers in a semiconductor is given by

$$n = \int_{E_C}^{\infty} N(E) \times F(E) dE$$
(3.5)

where N(E) is the density of states at energy E and F(E) is the occupancy which is the probability that a state at energy E is occupied. The lower energy limit of the conduction band is denoted as  $E_{C}$ . The occupancy is given by the Fermi-Dirac distribution

$$F(E) = \frac{1}{1 + e^{(E - E_F)/k_b T}}$$
(3.6)

where  $E_F$  is the Fermi energy at which F(E) = 0.5. The Boltzmann constant is denoted as  $k_B$ .

Silicon is a non-degenerate semiconductor because its band structure has a gap between the valence and the conduction band and its Fermi energy is close to the middle of the band gap. Only very few electrons reach the conduction band via thermal excitation. Thus the intrinsic charge carrier concentration, especially at or below room temperature, is low and pure silicon can practically be treated as an insulator. However, the Fermi level can be shifted by doping silicon either with electron donors (e.g. phosphorus, arsenic) or acceptors (e.g. boron) as shown in Fig. 3.5. As long as the dopant concentration stays below roughly  $10^{19}$ /cm<sup>3</sup> silicon will remain a non-degenerate semiconductor. Silicon that is doped with donors is called n-doped and has a raised concentration of electrons in the conduction band. Silicon that is doped with acceptors is called p-doped and has a higher concentration of electron vacancies which are generally called holes. Within the crystal lattice of monolithic silicon holes behave very similar to positively charged particles and travel by switching places with electrons.

The charge carrier concentrations for electrons and holes in a non-degenerate semiconductor follow the mass-action law [13]

$$n * p = n_i^2 \tag{3.7}$$

where n and p are the concentrations of electrons and holes, respectively, and  $n_i$  is the intrinsic charge carrier concentration of pure silicon. If the concentration of one carrier species is increased via doping the concentration of the other will be reduced accordingly. However, the conductivity of the material is dependent on the concentration of both charge carriers in the conduction band and thus n-doping and p-doping will both increase the conductivity  $\sigma$  of silicon considerably because

$$\sigma = e(n\mu_n + p\mu_p). \tag{3.8}$$

Thus the conductivity of silicon is dominated by the concentration of the majority charge carrier.

#### 3.1.1 pn-Junctions

In order to turn ionized charge carriers into a measurable current an electric field inside the silicon bulk is necessary. This cannot be done by applying voltage to a piece of pure silicon because the current from the intrinsic concentration of charge carriers would produce too much noise. However, when n- and p-doped silicon come into contact a depleted region is formed around the intersection caused by the exchange of charge carriers. A qualitative sketch of the corresponding profiles for the space charge, electric field and potential and the charge carrier density is shown in figure 3.6. This exchange reaches an equilibrium once the Fermi level is constant throughout the junction. An electric field, called the built-in field, builds up until the corresponding drift current compensates for the diffusion of charge carriers. This pn-junction can be biased in reverse by applying a positive voltage to the n-doped and/or a negative voltage to the p-doped side to lower the intrinsic concentration  $n_i$  of charge carriers in the depletion region according to [13] and the charge carrier concentrations are calculated as



Figure 3.5: Band gap and Fermi level for un-doped, n-doped and p-doped silicon [13, p. 24]. N(E) is the density of states and F(E) is the Fermi distribution.

$$n = n_i e^{(\frac{E_{Fn} - E_i}{k_B T})}$$
(3.9)

$$p = n_i e^{(\frac{E_i - E_{F_p}}{k_B T})}$$
(3.10)

$$np = n_i^2 e^{(\frac{E_{Fn} - E_{Fp}}{k_B T})}$$
(3.11)

with symbols as defined in the appendix, section A. For a reverse bias the charge carrier concentration in the depletion region drops below the intrinsic value because  $E_{Fn} - E_{Fp} < 0$ . One can see that Equation 3.11 simplifies to the mass-action law if no bias is applied and  $eU_{ext} = E_{Fn} - E_{Fp} = 0$ . Increasing the reverse bias ( $U_{ext} < 0$ ) across an abrupt pn-junction (sharp interface between the p- and n-layer, constant dopant concentrations) will widen the depletion region according to

$$W_{Dp} = \sqrt{\frac{2\epsilon_s(\Psi_{bi} - U - 2k_B T/q)}{q}} \frac{N_D}{N_A(N_A + N_D)}$$
(3.12)

$$W_{Dn} = \sqrt{\frac{2\epsilon_s(\Psi_{bi} - U - 2k_B T/q)}{q}} \frac{N_A}{N_D(N_A + N_D)}$$
(3.13)

$$W_D = W_{Dp} + W_{Dn} = \sqrt{\frac{2\epsilon_s}{q}} \frac{N_A + N_D}{N_A N_D} (\Psi_{bi} - U - 2k_B T/q)$$
(3.14)

$$\Psi_{bi} = \frac{k_B T}{q} ln(\frac{n_{n0} p_{p0}}{n_i^2}) \approx \frac{k_B T}{q} ln(\frac{N_D N_A}{n_i^2})$$
(3.15)

with symbols as defined in the appendix, section A. The built-in voltage  $\Psi_{bi}$  is defined by the doping concentrations. It increases with rising temperatures and is further modified by the applied external voltage. The approximation for  $\Psi_{bi}$  assumes the full ionisation of all dopant atoms.

As an example, with doping levels of  $N_A = 10^{13}$  and  $N_D = 10^{17}$ , the built-in voltage is 0.6 V. Assuming a reverse bias voltage of -6 V for an n<sup>+</sup>-in-p diode the depletion region will almost entirely grow into the p-doped silicon. The width of this region is then



Figure 3.6: Shown are the characteristics of a pn-junction under no bias (left) and reverse bias (right). The width of the depletion region on either side of the junction depends on the concentration of acceptors and donors in the p-doped and n-doped silicon. The bias voltage is denoted as  $eU_{ext} = E_{Fn} - E_{Fp}$ .

$$W_{Dp} = \sqrt{\frac{2\epsilon_s(\Psi_{bi} - U - 2k_B T/q)}{q}} \frac{N_D}{N_A(N_A + N_D)}$$
$$\approx \sqrt{\frac{2\epsilon_s(\Psi_{bi} - U)}{q}} \frac{1}{N_A}$$
$$\approx 3.6 \times 10^3 \sqrt{\frac{\Psi_{bi} - U}{N_A}}$$
$$= 3600 \sqrt{\frac{6.6}{10^{13}}} = 29.25 \,\mu m$$

Several pixel chips discussed in this thesis were produced on wafers with a  $25\,\mu m$  layer of epitaxial silicon and would thus be fully depleted for the assumed doping level of the silicon bulk.

The voltage-current characteristic of a silicon pn-junction is qualitatively well described by the Shockley Equation [13]

$$I = I_S(e^{\frac{q_U}{k_B T}} - 1) \tag{3.16}$$

$$I_S \propto T^{3+\gamma/2} e^{-\frac{E_g}{k_B T}} \tag{3.17}$$

with all symbols as defined in the appendix, section A, and  $\gamma$  as a constant. A qualitative graph for this relation in shown in figure 3.7. I<sub>S</sub> is the saturation current which flows through a back biased diode and which has a strong dependence on temperature. The reverse bias is limited by the break down voltage beyond which charge carriers either cause a current avalanche via impact ionization or start to tunnel through the potential barrier. When a forward bias is applied the current across the junction increases exponentially.

Finally, the capacity across an abrupt one-sided junction (assuming a planar interface) where a highly doped n-well is in contact with a lower p-doped substrate can be expressed as [13]

$$C_D = \frac{\epsilon_s}{W_D} = \sqrt{\frac{q\epsilon_s}{2}} N_A \frac{1}{\sqrt{\Psi_{bi} - U - \frac{2k_BT}{q}}}$$
(3.18)

$$C_D^2 \propto U \tag{3.19}$$

with symbols as defined in the appendix, section A.



Figure 3.7: Shown is a sketch that indicates the current across a diode based on the applied external bias voltage.

 $C_D$  is dependent on the doping level  $N_A$  of the p-doped substrate into which the depletion region grows. It also depends on the applied bias voltage and the temperature. None of these parameters are easily changed without affecting the proper working of the detector. The operating temperature of the sensor raises the leakage current, the bias voltage cannot be lowered because the width of the depletion layer has a direct impact on the sensor volume and the doping levels are often dictated by foundries and by the proper functioning of the sensor and circuit components. This means that the most feasible way to improve the performance of a pn-junction silicon detector is to either make the depleted region thicker so that more deposited charge can be collected or by improving on the circuit design of the detector electronics.

#### 3.1.2 Signal generation

The principle of particle detection with a pn-junction is the measurement of a current across the depleted region caused by the electron-hole pairs which are generated by a traversing particle. These new charge carriers drift through the depletion region along the electric field and register as a current through the junction. This process is sketched out in figure 3.8. It is important to note that the charge moving through the depletion region immediately induces a current on the electrodes. This effect is described by the Ramo Theorem [14]

$$i = q\vec{v}\vec{E_w} \tag{3.20}$$

where  $\vec{E_w}$  is the weighting field which is computed for an individual electrode by removing the field of the charge carrier, setting the potential of the electrode in question to unity and that of all other electrodes to zero. The weighting field describes how strong the



Figure 3.8: A particle which moves through the depletion region will lose energy and leave a trail of electron hole pairs. Once the generated charge carriers start to drift in the electric field a voltage shift is induced across the depletion region. The new voltage level is only maintained if the charge is actually collected by the electrodes.

charge carrier's induced current is coupled to a given electrode. The charge carrier's velocity  $\vec{v}$  is

$$\vec{v} = \mu_q(\vec{E})\vec{E} \tag{3.21}$$

with  $\mu_q$  as the charge carrier's mobility and  $\vec{E}$  the electric field acting on it. Thus the induced current on an electrode is dependent on both, the electric field in the sensor which moves the ionized charge and the weighting field which dictates the induced current. The final voltage signal on a collection electrode with capacitance C is given by the total amount of charge collected:

$$\Delta V = \frac{Q_{coll}}{C_D} \,. \tag{3.22}$$

The subsequent amplification and discrimination of the signal is handled differently depending on the design of the detector circuitry.
# Chapter 4

# Silicon pixel detectors



Figure 4.1: Shown are sketches of a hybrid pixel design (left) and several monolithic pixel designs (right), including a 'large collection diode' (top), 'small collection diode' (middle) and an silicon-on-insulator (SOI) design (bottom).

Generally, a pixel detector always comprises of a sensor and a front-end. Both components are application specific integrated circuits (ASICs) segmented into pixels but fulfill a different purpose. The sensor is responsible for the generation of a measurable signal when it is hit by a charged particle of sufficient energy. The front-end is responsible for the processing of that signal.

Hybrid detectors comprise of two physically separate chips, a front-end and a sensor, which are connected to each other pixel by pixel via solder bump bonds as shown in figure 4.1 on the left. This allows the combination of various front-end and sensor chips as long a the pixel arrangement on both is compatible. This type of pixel detector tends to have good radiation hardness because front-end and sensor can be developed separately. Important drawbacks are the increased material budget which leads to more particle scattering and a higher cost of production due to non-industrialized processes during production.

Monolithic detectors are made from a single piece of silicon which combines front-end and sensor as shown in figure 4.1 on the right. This removes the need for solder bump bonds, reduces the material budget and allows production via streamlined industrial standard processes. However, there are also drawbacks. This type of detector has not yet been tested and developed as extensively as hybrids and there is not as much experience using it in particle detectors. Since sensor and front-end have to share the same space, it is more difficult to prevent cross talk between analogue and digital circuitry and to map both to the limited area in the pixel. Furthermore, the use of industrial processes which reduces production cost can also limit the implementation of custom circuitry.

# 4.1 CMOS technology

Silicon pixel detectors, sensors and front-end alike, can be fabricated using CMOS technology. The principle is to combine PMOS and NMOS transistors symmetrically to create integrated circuitry on a silicon wafer which only draws power when switching states. While the MOSFETs are located directly in the silicon bulk, other components such as oxide layers and wires (metal vias) are deposited on top of the wafer via a series of layer deposition and etching processes. The most basic building block of a CMOS circuit is a NAND-gate as shown in figure 4.2. Its logic is summarized in table 4.1.

Due to the complementary use of PMOS and NMOS, the circuit for a NAND-gate features two NMOS transistors connected in series and two PMOS transistors connected in parallel. If one or both inputs are low, then one or both PMOS transistors are active and at least one NMOS transistor is off. Consequently OUT will be pulled to VDD. On the other hand, if both A and B are high, both PMOS transistors are off and both NMOS transistors are on which pulls OUT to VSS.

	А	В	OUT
-	1	1	0
	1	0	1
-	0	1	1
	0	0	1

Table 4.1: Shown is the logic table of a NAND-gate.

It is important to note that the physical layout in figure 4.2 on the right is not the only possible implementation. In order to raise radiation hardness, circular designs with the source entirely surrounded by the gate can be used, usually at the cost of a larger foot print.

# 4.2 Pixel detector characterization

Irrespective of the design (hybrid or monolithic), pixel detectors are characterized based on a common set of parameters such as charge collection efficiency, gain, noise, threshold and detection efficiency. From the charge deposit by an incident particle to a digital data stream that is sent to a server or PC several processing steps are necessary. At the beginning charge must be collected, amplified and shaped into a detectable analogue signal. This signal is then sent to a discriminator and digitized. The digital signal is then formatted into a digital data stream that is sent off chip. A discussion of the most important parameters that influence the performance of the analogue front end are discussed in this section.

### 4.2.1 Charge collection efficiency and gain

After charge was deposited in a sensor by an incident particle, it is most important to efficiently collect this charge and produce as strong a signal as possible from it. The charge collection efficiency is the fraction of collected versus generated charge

$$\epsilon_{coll.} = \frac{Q_{coll}}{Q_{gen}} \tag{4.1}$$

and is mainly a parameter of the sensor bulk itself. It is influenced to a large extent by non-ionizing radiation damage (damage to the silicon crystal lattice) and the geometric

<sup>&</sup>lt;sup>1</sup>Wikimedia Commons, https://commons.wikimedia.org/wiki/File:CMOS\_NAND\_Layout.svg, last accessed: 01.06.2020





Figure 4.2: Shown is the CMOS version of a NAND-circuit (left) and a possible physical layout of that circuit (right)<sup>1</sup>.



Figure 4.3: Shown is a simplified circuit of a charge sensitive amplifier.

layout of the sensor and its depletion region.

Ζ

The gain is calculated differently depending on the front-end that is used. In a commonly used charge sensitive amplifier (integrator circuit), the gain is defined by the feedback capacitance  $C_f$  as shown in figure 4.3. The output voltage is inverted and determined by the charge  $Q_S$  that the current  $i_S$  transports to  $C_f$  and is calculated as

$$\Delta V_{out} = \frac{-1}{C_f} \int_0^t i_S \, dt = -\frac{Q_S}{C_f} \quad . \tag{4.2}$$

However, due to their small size, the pixels of the detectors discussed in this work can only house a limited amount of circuitry and a simpler circuit was needed. These detectors feature a small collection diode design with a capacitance of only 5 fF and thus, for a collected charge of 1600 e<sup>-</sup>, the voltage step will be roughly 50 mV. For the amplification of this signal a custom circuit was designed which can be implemented in a smaller area on the pixel. A simplified version of the open-loop amplifier as it is used in the MALTA detector (see section 5.2.1) is shown in figure 4.4. The IN node is directly connected to the collection diode and when charge is collected the voltage at IN drops. M1 then acts as a source follower which is biased by IBIAS. This means that it has a voltage gain close to unity but a large current gain and the C<sub>S</sub> capacitance discharges into C<sub>OUT</sub>. The amount of transferred charge depends on the voltage step at IN and the gain scales with the ratio of both capacitances:

$$\Delta V_{OUT} = \frac{Q_S}{C_{OUT}} = \frac{C_S}{C_{OUT}} \Delta V_{IN} = \frac{C_S}{C_{OUT}} \frac{Q_{coll}}{C_{IN}}$$
(4.3)

Consequently, the gain is high for  $C_S >> C_{OUT}$ . In the physical circuit  $C_{OUT}$  is simply the sum of parasitic capacitances connected to  $C_S$ .

Sensors can be calibrated using fluorescence sources or x-ray emitters such as  $^{55}$ Fe which cause point-like charge deposits in the sensor via the Photoelectric Effect. The amount of deposited charge is constant and the collected charge is a constant fraction of that



Figure 4.4: Shown is a simplified circuit of the amplifier used in the MALTA detector kindly provided by the author of [15].

amount when averaged over the entire sensor area. Measuring the signal amplitude at the front-end output for several Fluorescence lines therefore allows to calibrate the sensor and calculate its gain. The amount of collected charge can then be calculated from the signal amplitude and compared to the expected deposited charge based on energy loss models as discussed in section 3.

## 4.2.2 Noise

Besides the ability of a sensor and front-end to generate a large signal from deposited charge it is vitally important to do this while maintaining low noise levels and achieve a high signal-to-noise ratio (SNR). In a pixel detector noise can be generated from various sources which can generally be expressed as the sum of three different terms with different dependencies. A common unit of measurement is the equivalent noise charge which is the ratio of produced noise over the signal generated from a single collected electron [12]

$$ENC = \frac{voltage\ noise\ output}{voltage\ signal\ output\ for\ 1\ e^-} \left[\frac{V}{V/e^-}\right]$$
(4.4)

$$ENC^{2} = a_{shot} \tau + a_{1/f} C_{D}^{2} + a_{therm} \frac{C_{D}^{2}}{\tau}$$
(4.5)

(4.6)

with symbols as defined in the appendix, section A. For small collection diode designs the detector input capacitance  $C_D$  depends on the capacitance between the collection diode and the deep p-well as well as the sensor back side. The filter time  $\tau$  is a property of the in-pixel circuit.

For MOSFET transistors the shot-noise contribution is usually neglected because it dependents on the leakage current  $a_{shot} \propto I_0$  which is assumed to be low. There are however significant contributions from the thermal noise component which derives from the Brownian motion of charge carriers in the channel of the MOSFET and  $a_{therm}$  can be written as [12] [16]

$$a_{therm} = \frac{4k_B T \gamma}{g_m} \qquad for strong inversion \tag{4.7}$$

$$a_{therm} = \frac{2k_B T n}{g_m} \qquad for weak inversion \tag{4.8}$$

with symbols as defined in the appendix, section A. A transistor is in strong inversion if the gate-source voltage  $V_{GS}$  is larger than the threshold voltage, for weak inversion  $V_{GS}$ is below threshold but there is a small current present which depends exponentially on  $V_{GS}$ . The factor  $\gamma$  can be approximated by 0.67-1.0 for CMOS processes, n is the weak inversion slope.

The second important contribution to noise is 1/f-noise which also called random-telegraph-signal noise (RTS noise). Depending on the model that is used it can be derived as [12] [16]

$$a_{1/f} = \frac{K_f}{C'_{ox}WL} \frac{1}{f} \quad for \ \Delta\mu - 1/f \qquad or \tag{4.9}$$

$$a_{1/f} = \frac{K_f}{C_{ox}^{\prime 2} W L} \frac{1}{f} \quad for \ \Delta n - 1/f \tag{4.10}$$

with symbols as defined in the appendix, section A. The mobility fluctuation model  $\Delta \mu$ -1/f assumes that the mobility of charge carriers in the material fluctuates due to phonon scattering. However, in the context of a MOSFET the  $\Delta n$ -1/f model is more applicable and equation 4.10 is used. In this model the 1/f-noise originates from the generation and recombination of charge carriers in the gate oxide and its interface to the transistor bulk. In both models the 1/f-noise depends on the dimensions and capacitance of the gate oxide and the homogeneity of the transistor.

It is important to note that for pixel designs with a small collection diode the circuit input capacitance  $C'_{ox}$  cannot be neglected compared the detector input capacitance  $C_D$ . Due to its independence on frequency, the thermal noise component dominates for very fast charge deposits and the SNR can be expressed as

$$\frac{S}{N} \propto \frac{Q}{C_D} \sqrt{g_m} \tag{4.11}$$

with  $g_m$  being proportional to the transistor bias current I as either  $g_m \propto I$  for weak inversion or  $g_m \propto \sqrt{I}$  for strong inversion.

In summary, the detector performance can be optimized by keeping  $C_D$  small for a large SNR and  $C'_{ox}$  large to reduce RTS-noise. Furthermore,  $g_m$  is larger for weak inversion which raises the SNR as well.

#### 4.2.3 Efficiency and threshold

The main parameter of interest for a particle detector is its efficency which is simply calculated as

$$\epsilon = \frac{N_{det}}{N_{total}} \tag{4.12}$$

where  $N_{det}$  is the number of detected and  $N_{total}$  is the total number of impinging particles. In the context of an experiment such as ATLAS, it is also important to detect particles within a given time window. Damaged pixels which have to be turned off also reduce the efficiency as a fraction of active over total area. Consequently, more specific definitions of efficiency exist such as in-time efficiency, global efficiency and in-pixel efficiency for which different cuts to the data are applied. The most important parameter which affects a detector's efficiency is the detection threshold (or simply "threshold") at which it is able to operate. This threshold must be lowered as far as possible to improve detection efficiency, temporal and spatial resolution but must be as high as necessary to sufficiently suppress noise generated hits (noise triggered pixels).

In the case of pixel detectors the global threshold which is applied across the whole pixel matrix typically ranges from some hundred to a few thousand electrons, depending on the sensor design. Pixel designs with large collection diodes usually operate at a higher threshold than small diode designs. Irrespective of the detector design (monolithic or hybrid), per-pixel thresholds tend to vary with respect to the global threshold which is called threshold dispersion. Thus, even at high thresholds some residual noise is observed if this dispersion is large. Many front-ends support a per-pixel threshold fine tuning to minimize this effect to allow a lower overall threshold.

Besides raising efficiency, a low threshold is important for several other aspects of detector performance. The concepts of the time-walk and time over threshold (TOT) are illustrated in figure 4.5. The delay between the deposition of charge in the sensor and the detection



Figure 4.5: Shown is a sketch of how the time-walk and time over threshold are affected by small and large signals.



Figure 4.6: Shown is the measured relation between the signal size and time-walk for the MALTA detector. The plot was kindly provided by the author of [15].

of the corresponding signal by the front-end is called time-walk. In the context of the ATLAS experiment it is important to keep the timing error caused by this delay below 25 ns so that particle hits can be reliably associated with the correct bunch crossing. The TOT is the time a signal stays above the detection threshold and thus gives information about the signal size. It can be calibrated to measure the amount of deposited charge and to correct for time-walk and improve timing precision. A measurement that shows the relationship between time-walk and signal size is shown in figure 4.6. A lower threshold will not only reduce the detection delay caused by the time-walk but also improve the precision of the measured TOT.

The inherent spatial resolution of a pixel detector can be calculated from the variance of a uniform distribution which models the binary response (i.e. hit versus no hit) of a single pixel to a particle hit. The variance is then

$$m_i = \frac{1}{b-a} \int_a^b x^i dx \tag{4.13}$$

$$m_1 = \frac{b-a}{2} \tag{4.14}$$

$$m_2 = \frac{b^2 + ab + a^2}{3} \tag{4.15}$$

$$\sigma^2 = m_2 - m_1^2 = \frac{(b-a)^2}{12} = \frac{pitch^2}{12}$$
(4.16)

with (b-a) as the pixel pitch. However, a further improvement of the spatial resolution is possible if multiple pixels are triggered by an individual particle hit. The hit coordinate can then be calculated as the center of gravity of this pixel cluster

$$C\vec{O}G = \frac{\sum_{i=0}^{N} \omega_i \vec{x}_i}{\sum_{i=0}^{N} \omega_i}$$
(4.17)

where the weighting factor  $\omega_i$  is either 1 for a binary pixel response or based on the signal size, i.e. the TOT. The average number of triggered pixels per particle is mainly dependent on charge sharing, i.e. how much charge is collected by the neighbors of a pixel that was hit. However, the detection of these usually low shared signals is especially dependent on a low threshold. Thus, when lowering the threshold, the number of pixels, e.g. the cluster size, increases and the spatial resolution improves.

## 4.2.4 Radiation damage

Pixel detectors in high energy physics experiments such as ATLAS are installed as closely as possible to the interaction point in order to optimize the track resolution. For example, the innermost layer of the current ATLAS pixel tracker is only 33.25 mm away from the beam. At this distance the particle fluence is extremely high and causes considerable damage. It is therefore necessary to design a 'radiation hard' chip which maintains its performance for the entire expected life time dose.

For testing purposes, chips are irradiated in various ways to simulate radiation effects. The most common method to simulate damage to the silicon lattice (i.e. bulk damage) is to irradiate the detector with neutrons in a nuclear reactor. The neutron fluence is given in units of 1 MeV  $n_{eq}/cm^2$  and called non-ionizing energy loss or NIEL. For reference, the innermost layer of the new ATLAS ITk which is 3.9 cm from the interaction point, has a lifetime fluence of  $\sim 10^{16} n_{eq}/cm^2$  and the outermost one at 28.0 cm  $\sim 10^{15} n_{eq}/cm^2$ . For tests with ionizing radiation x-rays or a proton beam can be used which leads to charge build-up in the oxide layers present on a CMOS chip. This additional damage due to ionization, the ionizing energy loss or IEL, is commonly given as the total ionizing dose TID in units of Grey or Rad (1 Gy = 100 Rad). Finally, the robustness of a CMOS circuit against very large charge deposits is studied with heavy ion beams. A large energy deposit can cause a 'single event latch-up' in the sensor. This runaway effect is characterized by a self-enforcing current which can only be stopped by powering down the chip.



Figure 4.7: Shown is a sketch of additional energy layers in the band gap after irradiation. Levels close to the center will cause additional charge carrier generation and thus leakage current. Levels at the border will cause charge trapping.

Effects of NIEL radiation damage This type of radiation damages the crystal lattice of the monolithic silicon and creates additional energy levels in the band gap. As shown in figure 4.7 energy levels close to the center of the band gap effectively enable easier thermal excitation by providing an additional 'step' across the band gap and will act as nucleation centers for charge carriers. Energy levels close to the border of the gap are able to recombine with charge carriers for a limited duration which is called 'trapping' and reduces the amount of deposited charge available for collection in a sensor.

The induced signal at the collection diode is dependent on how far electrons and holes drift away from each other before they are collected. This distance in turn depends on the mean life time of an electron or hole in the silicon

$$d_{sep} = v_e \tau_e + v_h \tau_h = (\mu_e \tau_e + \mu_h \tau_h) E \tag{4.18}$$

$$\frac{1}{\tau_{e,h}} = \frac{1}{\tau_0} + k_{trap}\Phi \tag{4.19}$$

where  $d_{sep}$  is the separation distance and  $\tau_{e,h}$  is the mean life time of electrons and holes. The damage constant  $k_{trap}$  is a measure for the effect of the particle fluence  $\Phi$  on the mean life time. Charge trapping reduces the separation distance and thus the induced signal at the collection diode.

Another effect of NIEL radiation damage is that it causes silicon to become increasingly p-doped. This is called type-inversion because n-type silicon can turn into effective p-type silicon at high enough fluences. For high resistivity silicon (i.e. low doping concentrations) this may already be the case at fluences of  $10^{12-13}$  1 MeV  $n_{eq}/cm^2$  and is mainly caused by the creation of acceptor-like defects in the bulk. The effects of NIEL on the silicon bulk can change the doping levels and raise the leakage current so much that full depletion, even at hundreds of volts of substrate bias, is not possible anymore. This is an important phenomenon for detectors in the ATLAS environment and pixel detectors



Figure 4.8: Sketch of how the working point of a transistor can change due to radiation induced space charges. In extreme cases the oxide charge-up can prevent a PMOS from turning on or an NMOS from turning off.

must be designed with its effects in mind. A common approach is to use  $n^+$ -in-n or  $n^+$ -in-p collection diodes. After type inversion the depletion region will still grow from the collection diode into the bulk which allows to operate the detector even if it is not fully depleted.

Effects of IEL radiation damage In the case of charged particle fluence or x-rays the most important effect of the radiation damage is the charge-up of the oxides that are part of the CMOS circuitry on the chip. This charge-up occurs because hole mobility in the oxide is extremely low. While electrons eventually leave the oxide layer, holes will be trapped for a long time and cause a build up of positive space charge. If the oxide layer that isolates the gate of a MOSFET from the bulk has its own space charge, the working point of the transistor will change accordingly. A qualitative sketch of this effect is shown in figure 4.8.

Furthermore, the built up charge in the oxide can lead to parasitic currents which can bypass the gate of a MOSFET and inadvertently switch it on. An illustration of this phenomenon, and how to suppress it with a circular MOSFET design, is shown in figure 4.9.

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Figure 4.9: Left: Sketch of a MOSFET with a standard layout. Due to charge buildup in the oxide layer after irradiation a parasitic current can flow around the gate. Right: Radiation hard MOSFET design with a circular gate. Here the generation of parasitic currents is strongly suppressed.

**Single event latch-up** In an integrated circuit not all transistor structures that occur may be put there on purpose. An example is given in figure 4.10. The n-well on the left is usually kept at a high voltage (VSS) so that the parasitic p-n-p structure from the source of the PMOS, the surrounding n-well and the p-doped bulk is not activated. Similarly, the p-doped bulk is kept at a low voltage (VDD) so that the parasitic n-p-n structure from the n-well, the p-doped bulk and the drain of the neighboring NMOS is deactivated. As long as all voltages remain within design limits, neither the p-n-p nor the n-p-n structure will turn active. However, in the event of a latch-up the following might occur:

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- A sudden and very large charge deposit, for example by an impinging heavy ion, temporarily drops the voltage in the n-well.
- The parasitic p-n-p structure is activated.
- The current between the PWELL source and the p-doped bulk raises the voltage in the p-doped bulk.
- The gate (p-doped bulk) voltage of the n-p-n structure is now high.
- The parasitic n-p-n structure is activated.
- The current from the n-well to the NMOS drain keeps the n-well voltage low and the current through the circuit is self sustaining.

The overall p-n-p-n structure which causes the latch-up is called a thyristor. The resulting thermal runaway current can destroy the device if it is not stopped in time. Usually, it is necessary to power cycle the circuit. Additional n- and p- implants are added to the n- and p-wells which house NMOS and PMOS transistors to stabilize the bulk voltage and reduce the susceptibility to latch-ups.

Finally, large charge deposits may flip the sign of bits stored on the detector. This is called a single-event-upset or SEU and can corrupt the data that is stored on the chip such as DAC settings. A common method to reduce the effects of SEUs is to triplicate the flip-flop structures which are used for configuration data storage. If one part of the triplicated flip-flop is changed by an SEU, the original bit is still saved by two out of three.

## 4.2.5 Beam tests

The most important parameter for any particle detector is its particle detection efficiency. Beam telescopes consist of several particle detectors (usually also pixel detectors) to reconstruct the particle tracks of a test beam and interpolate the track intercept positions on the DUT as shown in figure 4.11.

Before any particle tracks can be projected onto a test device, all sensors must be aligned relative to each other. Several techniques and software packages exist to achieve this such as Judith [17] or proteus [18]. Once the alignment is done, tracks can be reconstructed. For high energies such as those provided by the SPS beam (ranging up to roughly 300 GeV for muons<sup>2</sup>) particle scattering is negligible and a simple linear regression fit of a straight

 $<sup>^2{\</sup>rm SPS}$ - H6 beam line manual, http://sba.web.cern.ch/sba/BeamsAndAreas/h6/H6manual.pdf, last accessed: 01.06.2020



Figure 4.10: Shown is a sketch of the parasitic p-n-p-n thyristor which comprises of the PMOS source, the n-well, the p-doped bulk and the NMOS drain. A very large charge deposit, as might be caused by an impinging heavy ion, can trigger a runaway current from the PMOS source to the NMOS drain which can only be stopped by power cycling the device.

line may suffice. At lower energies, and especially for electrons, multiple scattering must be taken into account. A commonly used track reconstruction algorithm is called 'General Broken Lines' or GBL [19]. This algorithm estimates scattering angles based on the beam particle's mass and momentum as well as other material in the beam and was used for all results which are shown in this thesis and which were obtained at the beam facilities in Bonn (ELSA) and Hamburg (DESY).

The precision with which track intersections can be projected onto a DUT is dependent on several factors. First, the inherent resolution of the telescope detectors (discussed in section 4.2). Second, the beam properties such as energy and particle species and third the number and position of telescope planes. Generally, smaller pixel pitches, more telescope planes and higher beam energies provide better resolution. For low energy electron beams the large influence of scattering often makes the use of many telescope planes irrelevant and even the pixel pitch is not as important. Instead, more attention must be paid to correctly calibrate a suitable track reconstruction algorithm and keep track of the amount and position of scattering material in the beam.

<sup>&</sup>lt;sup>3</sup>drawn with wavedrom, https://wavedrom.com/, last accessed: 01.09.2020



Figure 4.11: A sketch illustrating the basic idea of a beam telescope. A particle's track is measured by the beam telescope and reconstructed. Then the track intercept position on the DUT is interpolated and compared to its response.



Figure 4.12: Shown is the basic logic operation of a TLU (trigger logic unit) as used in beam test for this work<sup>3</sup>.

A key aspect of any beam test is the synchronization of the recorded data of the various components of the setup. For this purpose the readout of the whole test beam setup is trigger based and trigger counters are stored as part of each data stream of each detector. Triggers to read out the entire setup are generated by the 'trigger logic unit' (TLU). The basic concept of the trigger logic is illustrated in figure 4.12. The TLU has two or more trigger input channels ( $trig_{-in_{-}1}$  and  $trig_{-in_{-}2}$  in the sketch) which are scanned for coincidence events where a signal is registered on both channels within a given time window. Once the TLU registers a signal on one of the two trigger input channels, its internal coincidence flag *coinc* is raised. Only if the second trigger channel also sends a signal before the flag is lowered again a coincidence event is registered and a trigger is sent out (single bit on  $trig_{-out}$ ) to the entire setup. At the same time a *busy* bit is raised and prevents any further coincidence events until a signal on one or more  $ack_{-in}$  channels is registered which indicates that all detectors of the setup received and processed the current readout trigger. Since beam test setups often contain detectors of various types the readout times of individual components may vary considerably.

Data synchronization is done by matching up events of the same trigger from each data stream. However, de-synchronizations happen when one or more detectors miss a trigger and the method of re-synchronization is usually not a standardized process and depends specifically on the test beam environment (e.g. continuous or spill-structured beams) and the properties of the DUT (e.g. low readout speeds of a few 100 Hz of an oscilloscope versus high readout speeds of an FE-i4 front-end of 40 MHz). Consequently, the method of data synchronization is discussed specifically for each detector study presented in the following sections.

By definition, the coincidence trigger will be processed by the detectors of the test beam setup after a particle has passed. This trigger latency must be compensated for by the detectors which continuously buffer the recorded data so that it can be retrieved once a trigger arrives. If the detector is read out by an oscilloscope the trigger delay can be configured to compensate for this the trigger latency. This is possible as long as the recorded frame of the oscilloscope is large enough to still envelop the signal wave form. In the case of a digital readout as implemented for MALTA detectors, the data stream from the detector is piped through a shift register which continuously buffers the data stream from the detector for a finite amount of time before it is discarded. Once a trigger arrives, the corresponding data can be retrieved by tapping into the shift register at a position that compensates for the trigger latency.

# Chapter 5

# Studies on radiation hardness

In the context of the ITk upgrade in 2025 the ATLAS pixel group aims to develop a monolithic pixel detector which is capable of withstanding the harsh environment of the HL-LHC and can provide the necessary performance in terms of spatial and temporal resolution and efficiency. The ALPIDE chip [20][21] which was developed by the ALICE collaboration [22] for the ALICE ITS upgrade during long shutdown 2 was chosen as a promising stepping stone to produce a DMAPS prototype for the ATLAS ITk. Given the lower radiation levels and event rate at the ALICE experiment, some initial modifications to the pixel design of ALPIDE were made.

Due to the much higher event rate of 40 MHz at ATLAS charge collection had to be sped up significantly. While ALPIDE collects a large fraction of the deposited charge via diffusion and operates with only a partially depleted sensor, an additional continuous n-layer is added in the new design which stretches across the entire epitaxial silicon bulk to facilitate full depletion of the sensor at low bias voltages. A sketch of the pixel cross section of ALPIDE and the new design is shown in figure 5.1. Instead of depleting from the collection diode the depletion layer grows from the interface between the continuous



Figure 5.1: Shown is a sketch of how ALPIDE (left) and the TowerJazz Investigator (right) deplete. In ALPIDE the depletion region forms as a bubble around the collection diode. The TowerJazz Investigator features an additional continuous n-layer in the silicon bulk from which the depletion region can grow across the entire sensor volume.





Figure 5.2: Shown is an image of the TowerJazz Investigator chip (left) and a top down view of  $2\times2$  investigator pixels (right). The entire pixel matrix is divided into 134 sub-matrices. Each sub-matrix contains  $8\times8$  pixels. The various pixel flavors explore different pixel pitches (note differently sized sub-matrices), different collection diode sizes and different deep p-well spacings.

n-layer and the p-doped bulk of the epitaxial layer.

In the following sections the development of a new CMOS DMAPS design suitable for the ATLAS ITk and produced by the TowerJazz foundry is presented. These studies, which focus on the detector performance in beam tests after irradiation, encompass initial studies of a first analogue prototype, called TowerJazz Investigator, and studies of several iterations of a new fully digital chip design called MALTA.

# 5.1 TowerJazz Investigator

The TowerJazz Investigator[23] is a monolithic silicon pixel detector produced in the TowerJazz 180 nm imaging process. The pixel matrix of the chip is divided into 134 different sub-matrices which feature various pixel designs. Each sub-matrix contains  $8\times8$  pixels. An overview of the entire chip with its sub-matrices is shown on the left in figure 5.2. A close up view of  $2\times2$  pixels is shown on the right and the main design parameters, which are the spacing, pixel pitch and collection diode size, are indicated.

pixel pitch	collection n-well size	spacing	designation
30 µm	3μm	3μm	M106
$40\mu m$	3μm	30 µm	M112
$50\mu{ m m}$	3μm	40 µm	M129

Table 5.1: Overview of the design parameters of the Investigator pixel flavors chosen for beam tests. Note the large difference in spacing for the  $30\,\mu\text{m}$  pixel pitch.

As shown in figure 5.1 the CMOS circuitry is housed inside a deep p-well to shield it from the collection n-well and the charge deposited in the sensor volume. The power supply rail provides 1.8 V for the CMOS circuitry and up to -6 V for sensor biasing. The bias voltage is negative relative to the collection n-well which is kept at 0.8 V. The depletion layer grows at the interface of the new planar n-type implant. Deposited charge drifts to the small collection n-well in the pixel center and induces a voltage signal. The lower voltage on the collection n-well is dependent on the amount of charge actually collected and the new voltage is maintained until it is reset by activating the reset PMOS transistor which drains the collected charge and pulls the diode back up to its original bias voltage. The epitaxial layer has a thickness of  $25 \,\mu$ m for all samples discussed in the following sections. The substrate has a thickness of  $65 \,\mu$ m. Among all available pixel designs three have been selected for test beam studies and they are summarized in table 5.1.

Two versions of the Investigator exist which differ in terms of the doping concentration of the additional planar n-layer. The results presented here were obtained with a high doping configuration referred to as 'MP1' in [24] for further details.

The chip is read out using a circuit that is based on the 3T cell design [25] as shown in figure 5.3. Each pixel is connected to an input and reset transistor and produces a purely analogue signal which is routed to the periphery via the Mini-MatrixSelect and ColumnSelect gates. All  $8\times8$  pixel signals from that sub-matrix are then routed from the chip via the carrier board to the adapter card. The adapter card is connected to the Multi-IO (MIO) board which handles chip configuration and operation and gives direct access to a fixed set of 25 pixels within the sub-matrix via SMA connectors to read out signals. The adapter card is connected to C1HV inverting amplifiers developed by Cividec<sup>1</sup> which have a 20 dB gain and a bandwidth of 1 MHz to 2 GHz<sup>2</sup>. The signals are then recorded by DRS4 oscilloscopes [26] with a maximum sampling rate of 5 GS/s. Control of the chip by the MIO board includes the selection of a sub-matrix, power supply to the chip's CMOS circuitry and a periodic reset signal which resets the collection diode.

 $<sup>^1\</sup>mathrm{CIVIDEC}$  Instrumentation GMBH, www.cividec.at, last accessed: 01.06.2020

<sup>&</sup>lt;sup>2</sup>CIVIDEC CH1V amplifier manual, https://cividec.at/index.php?module=public.product&idProduct=32, last accessed: 01.06.2020



Figure 5.3: Overview of the readout setup for the TowerJazz Investigator.

This signal is also recorded in one channel of the oscilloscopes so that resets can be filtered out of the data in the offline analysis. This setup has been extensively characterized in [24] and first beam test results have been published in [27].

## 5.1.1 Beam test setup

All beam tests to study the TowerJazz Investigator were conducted in the SPS test beam hall at the CERN Prevessin site in France with a 180 GeV/c pion beam. An image of the test beam area is shown in figure 5.4. Irradiated samples were kept in a styrofoam box, also 'cold box', for isolation and cooled to -20°C using dry ice at first and switching to a silicon oil chiller (large metal box on the ground) later. The cold box with the test chip is placed in between the arms of a beam telescope which consists of 6 FE-i4 pixel front-ends bonded to a silicon sensor [28] and which operates on the same hardware and software for data acquisition as described in [29] even though the mechanics for mounting



Figure 5.4: Shown is a photo of the H8b section of the SPS test beam area in Prevessin, France. The beam enters the area from the left. In order from left to right, setups are operated by the University of Geneva, the ATLAS pixel group (with the author at work) and the University of Bonn.



Figure 5.5: Shown is the FE-i4 telescope in use at the H8 beam line of the SPS test beam facility.

the telescope detectors are different. An image of the telescope is shown in figure 5.5 where the upstream arm of the telescope can be seen with 3 FE-i4 detectors. Cooling pipes enter the cold box (pink styrofoam) from the right. A copper block on which the carrier board with a test sample is mounted is used for cooling.

The readout of the telescope and DUT was triggered on coincidence events from two of the three upstream telescope planes. The FE-i4 hybrid pixel detector has an asymmetric pixel pitch of  $250 \times 50 \,\mu$ m. For this reason the telescope detectors are mounted at alternating angles of 0° and 90° with respect to the beam. A sketch of the relative placement of the telescope and the DUT is shown in figure 5.6. In addition to the rotation in z (along the beam) the two outer detectors of each telescope arm were tilted by 15° with respect to the middle detector to increase the cluster size for particle hits in the direction of larger pixel pitch and thus improve resolution further in that direction. The telescope resolution is estimated by the residual distributions of interpolated track and measured DUT positions. Overall almost symmetric distributions are achieved with standard deviations of 13.1 and 13.3 µm in x- and y-direction, respectively.

Based on the constraints of the readout setup only 4 pixels of any given sub-matrix of the Investigator could be read out which were always arranged in groups of  $2\times 2$ . Additionally, the diode reset from the MIO board was recorded to filter out triggers which occurred during resets. Since a single DRS4 oscilloscope only has 4 input channels it was necessary to read out 2 oscilloscopes configured as a daisy chain where the first recorded the signals of 3 pixels and the reset signal and the second recorded the 4th pixel. The total size of the DUT ranged from  $60\times 60 \,\mu\text{m}^2$  ( $2\times 2$  pixels with  $30 \,\mu\text{m}$  pitch) to  $100\times 100 \,\mu\text{m}^2$  ( $2\times 2$  pixels with  $50 \,\mu\text{m}$  pitch) which means that the DUT itself was smaller than a single pixel of the telescope planes. Due to the extremely small dimensions of the DUT data were acquired at a very low rate. Only a very small region of interest (ROI) was enabled on the pixel matrix of the trigger planes of the FE-i4 telescope to reduce the amount of recorded data. In order to acquire sufficient statistics individual data taking runs usually lasted for 5 to 12 hours and the entire test beam campaign lasted roughly 4 months.



Figure 5.6: Shown is a sketch of the telescope geometry on top and the achieved telescope resolution in x and y direction normal to the beam on the bottom.



Figure 5.7: Shown is an illustration of how the amplitude and rise time are extracted from a waveform.

## 5.1.2 Data treatment and analysis

Due to the analogue readout of the DUT, its small dimensions and the vast difference in data acquisition rate of the telescope sensors (40 MHz clock rate) and the oscilloscopes  $\left(\frac{250}{N_{osci}}\text{Hz}\right)$  several steps of data processing were necessary.

Waveform analysis Wave forms as recorded by the oscilloscopes showed a large amount of noise, especially periodic noise, and a robust method to extract the amplitude and rise time of the signals reliably had to be used. High frequency noise on the signal is reduced by scanning the raw wave form with a 10 ns moving average. The resulting smoothed wave form is used to calculate the amplitude and rise time of the signal. The procedure is visualized in figure 5.7. The start of the signal T0 is determined by the trigger settings of the readout setup and thus fixed in time within any given recorded frame of the oscilloscope. The amplitude of the signal is determined by comparing the mean voltage levels from 70 to 20 ns before and 80 to 130 ns after the trigger time T0 (set to 0 in the figure). The section of the wave form between these intervals is then scanned and the rise time of the signal is determined as the time it takes for the signal to reach from 10% to 90% of the calculated amplitude.

**Data synchronization** Due to the small size of the DUT it was unfeasible to enable the entire pixel matrix of the telescope detectors. By triggering the telescope readout on signals from the DUT its position is projected onto the telescope planes (assuming that particle tracks are straight lines). An ROI is then placed to envelop the DUT position and



Figure 5.8: Shown are 300 seconds of recorded data on the telescope and DUT. The SPS spills can be clearly identified and line up in time.

the trigger of the test beam setup is switched to coincidence events from the telescope. This was done to reduce the amount of unneeded data recorded for tracks far away from the DUT. Since the oscilloscopes that read out signals from the investigator are much slower than the telescope, a busy logic as explained in section 4.2.5 was implemented to prevent new triggers from the telescope piling up. Due to the long data taking runs, de-synchronizations were likely to happen. The reliable re-synchronization of DUT and telescope events was achieved by exploiting the spill structure of the SPS beam as shown in figure 5.8. The SPS provides its beam in spills of roughly 5 seconds with 10 seconds or more in between. Both DUT and telescope data can be structured into spills based on the time stamps recorded with each trigger. The data sets are then compared spill by spill. Only if the same amount of triggers was registered in both data sets for a given spill the corresponding events are matched one-on-one. De-synchronized spills are cut out of the data set.

**Compensation for DUT movement** For a large part of the test beam campaign the cooling of irradiated samples was done with dry ice. The gradually reducing weight of the remaining dry ice caused the DUT to move with respect to the telescope during measurements. The effect on the data is shown in figure 5.9.

In order to correct for this movement, each data set is divided into slices which contain 100 tracks matched to a valid signal from the DUT. From this set of 100 matched track positions a median sampling distribution for the x and y position is produced. Its mean



Figure 5.9: Shown is the DUT position  $(2 \times 2 \text{ pixels})$  over time before (top) and after (bottom) correction.

and standard deviation are then used to correct the DUT position and estimate the error introduced by that shift. This approach was chosen because it is robust against outliers caused by badly reconstructed tracks and produces consistent corrections for small sample sizes. This was necessary due to the extremely low acquisition rate of tracks on the DUT. If data sets were segmented into larger slices, these slices would correspond to a longer duration of data acquisition and the DUT position within such a slice could not be assumed to be constant. The core method for this correction algorithm is shown in the appendix, section B.

The DUT position is corrected so that it is placed at the coordinate center of the telescope's reference frame, i.e. the middle point of the  $2 \times 2$  pixel DUT is at (0,0).

**Cuts** The trigger time T0 has to be reconstructed for each data set so that voltage levels before and after the signal can be calculated and an amplitude derived as shown previously in figure 5.7. Furthermore, faulty signal spikes caused by periodic noise can be cut if their trigger time is too far from the reconstructed T0. For signals with very large amplitudes the effects of noise and time-walk are negligible and T0 is calculated as the 10% amplitude cross over (green line in figure 5.7). The mean of the resulting T0 distribution is then calculated as the mean of a Gaussian fit. As shown in figure 5.10 wave



Figure 5.10: Shown is how wave forms are aligned in time based on the reconstructed trigger time T0 of the oscilloscope. On the left very large amplitude signals were used to calculate T0. The middle and right plots show T0 aligned wave forms separated into accepted and rejected signals based on an amplitude cut.

forms can then be filtered based on a cut on the calculated amplitude. Since the voltage levels before and after the step are averaged over a 50 ns time window even signals barely above the noise level can be identified reliably.

In order to improve the telescope resolution and improve the contrast of the final efficiency plots a reduced  $\chi^2$  cut of 2.0 was placed on the reconstructed track fits to remove any drastic outliers.

Finally, to allow the calculation of a signal-to-noise ratio wave forms were classified as either a valid signal or noise based on the associated geometrical information from the telescope. This method was chosen because the conventional calculation of the noise as the RMS of the signal baseline did not yield consistent results due to large amounts of periodic noise. Any wave form with a track with an intercept position on the DUT is considered to be a signal while all wave forms with associated track intercepts at least one pixel pitch away from the DUT are classified as noise. The concept is visualized in figure 5.11. The signal and noise amplitudes that are used to calculate the SNR are always the sum of all four individual pixel amplitudes, so-called cluster amplitudes.

Summaries of the track residuals and reduced  $X^2$  distributions for the entire data set that was analyzed in this work are shown in the appendix, section C.



Selection areas for signal and noise

Figure 5.11: Shown are the signal amplitude weighted track positions for the cumulative data collected for the non-irradiated M129 sample with a  $50\,\mu\text{m}$  pitch. Any wave form with an associated track on the DUT position at the center is classified as a signal. Any wave form with an associated track that misses the DUT by at least one pixel pitch is classified as noise.



Figure 5.12: Shown is the Fluorescence calibration of several Investigator sub-matrices. Depending on the calibration behavior fit function are either linear or exponential in nature. The figure was kindly provided by the author of [24].

## 5.1.3 Sensor thresholds

The sub-matrices of the Investigator show different calibration behavior depending on the pixel flavor. For sub-matrices M129 and M112 a linear model yields good fits while for M106 the behavior is much better described by an exponential model and shows saturation above a certain amount of deposited charge. In the case of M129 and M112 the capacitance on the input transistor is larger which lowers the sensor gain. For M106 the lower capacitance leads to a higher gain which pushes the output buffer into saturation for very large charge deposits. This behavior is attributed to the line that connects the collection diode to the analogue front-end input. The length of this line and thus the capacitance on it scales with the spacing. The gain of the amplifier in the analogue front-end scales inversely with this capacitance. Thus, for small spacings the gain is large.

A direct threshold calibration of the tested samples is not available. However, a fluorescence calibration for various sub-matrices was presented in [24], which the author kindly provided, and is shown in figure 5.12. While only a calibration for M106 and M129 is available, the calibration of M112 can be substituted by that of a slightly different pixel design of sub-matrix M114 which only differs in terms of collection diode size ( $3\mu m$  instead of  $5\mu m$ . Due to the altered depletion region caused by the planar n-doped layer in the sensor it is assumed that the sensor capacitance is dominated by the line routing

Table 5.2: Given are the thresholds for the tested non-irradiated sub-matrices M106 and M129 based on results given in [24]. For sub-matrix M112 no calibration was available and is substituted by a similar sub-matrix M114 which only differs in terms of collection electrode size.

amplitude cut [mV]	M106	M114*	M129
	threshold $\%$	${\rm threshold}\%$	${\rm threshold}\%$
	[e <sup>-</sup> ]	[e <sup>-</sup> ]	[e <sup>-</sup> ]
5.0	55	443	673
10.0	112	888	1348
20.0	228	1787	2701
30.0	350	2697	4058
40.0	478	3618	5421
50.0	612	4550	6789

which depends on the spacing and not the collection diode size. The threshold values for sub-matrices relevant to this work are shown in table 5.2. Since the expected deposited charge in the sensor is roughly  $1600 e^{-}$  an amplitude cut above 10 mV for M112 and M129 is not sensible since only the high energy tail of the energy deposit spectrum would be registered by the sensor.

As shown in [24] a calibration of the irradiated Investigator and its interpretation is difficult and a fluorescence calibration is not available. In the following chapters amplitudes and amplitude cuts which serve as an artificial threshold will be given in mV and no direct conversion to electrons is made. The calibration shown in this section should only be applied to values from results before irradiation and an error of 20 % should be assumed. More focus is given to the signal-to-noise ratio (SNR) which is calculated as

$$SNR = \frac{\hat{X}_{signal}}{RMS_{noise}} \tag{5.1}$$

where  $RMS_{noise}$  is the root mean square of the amplitudes of wave forms that were classified as noise based on their associated track position.  $\hat{X}_{signal}$  is the most probable value (MPV) of the amplitude for wave forms classified as signals which was calculated as the mean of a gaussian fit of a narrow window around the peak of the distribution. This was done because a direct Landau fit did not yield consistent results.

#### 5.1.4 Sensor performance before irradiation

All non-irradiated sensors were operated at room temperature and a bias voltage of -6 V. A comparison in terms of signal spectra, cluster size and rise time can be seen in figure 5.13 for all three tested sub-matrices M129, M112 and M106 (left to right). The sub-matrices M129 and M112 reach an SNR of 6 and 8 while M106 performs significatly better with an SNR of 24. All sub-matrices are present on the same chip and the epitaxial layer (and thus the sensor) has the same thickness of  $25 \,\mu\text{m}$ . It is therefore assumed that the same amount of deposited charge is present for all samples. Since the samples were not irradiated no signal loss due to charge trapping is assumed. Therefore the higher SNR on M106 confirms a higher gain due to a lower capacitance on the signal input transistor.

Compared to the pixel designs with large spacings sub-matrix M106 has a much narrower rise-time distribution which indicates a much reduced time-walk. The small peak at  $\sim 18$  ns in the M106 distribution is caused by periodic noise. The cluster size is compared in the third and fourth row of plots for amplitude cuts of 5 and 10 mV for M129 and M112 and for amplitude cuts of 5, 10 and 50 mV cuts for M106. While sub-matrices M129 and M112 show mainly a single-pixel response, the average cluster size for matrix M106 is significantly higher which is attributed to its small pixel pitch. All measured values are summarized in table 5.3.

These results show that sub-matrix M106 performs best across the board due to its lower capacitance on the collection n-well which significantly raises the gain and reduces the time-walk. Additionally, charge sharing is greatly improved by the smaller pixel pitch.

A selection of 2D resolved efficiency plots together with efficiency projections of the center regions for several amplitude thresholds is shown in figure 5.14. All three tested sub-matrices are above 97% efficient for an amplitude cut of 5 and 10 mV. This translates to a threshold of 55 and 112 e<sup>-</sup> on M106, 443 and 888 e<sup>-</sup> on M112 and 673 and 1348 e<sup>-</sup> on M129. The efficiency is uniform across the pixel corner at the center of the plot where charge sharing is most likely. However, with higher amplitude thresholds the efficiency of M129 and M112 quickly drops off as expected while M106 stays efficient even for a 50 mV cut which translates to a threshold of 612 e<sup>-</sup>. The apparent drop in efficiency at the edges of the  $2\times 2$  pixel DUT is caused by the finite telescope resolution. Tracks of particles which narrowly missed the DUT may erroneously be reconstructed to intersect the DUT and contribute to the denominator for the efficiency calculation in that area. Even at the center of the DUT the efficiency does not reach a full 100% because of the position correction that was applied to the data (see previous section on data treatment) leads to some misplaced track intercepts which can lower the efficiency by a small fraction.

sub-matrix	amplitude cut	parameter	value mean ( $\pm$ std. dev.)
M106	$5\mathrm{mV}$	SNR	24.4
M112	$5\mathrm{mV}$	SNR	8.2
M129	$5\mathrm{mV}$	SNR	6.0
M106	$5\mathrm{mV}$	cluster size	1.91 [pixels]
	$10\mathrm{mV}$		$1.70 \; [pixels]$
	$50\mathrm{mV}$		1.18 [pixels]
M112	$5\mathrm{mV}$	cluster size	1.13 [pixels]
	$10\mathrm{mV}$		1.05 [pixels]
M129	$5\mathrm{mV}$	cluster size	1.07  [pixels]
	$10\mathrm{mV}$		1.03 [pixels]
M106	$5\mathrm{mV}$	rise time mean	$20.9 \pm 1.85 [ns]$
	$10\mathrm{mV}$		$20.9 \pm 1.85 [ns]$
	$50\mathrm{mV}$		$20.9 \pm 1.76 [ns]$
M112	$5\mathrm{mV}$	rise time mean	$27.9 \pm 4.76 [ns]$
	$10\mathrm{mV}$		$27.9 \pm 4.71 [ns]$
M129	$5\mathrm{mV}$	rise time mean	$27.9 \pm 5.34 [ns]$
	$10\mathrm{mV}$		$27.9 \pm 5.14 [ns]$

Table 5.3: Given are the measured values for the signal-noise-ratio, mean cluster size and mean rise time for non-irradiated sub-matrices M106, M112 and M106.



Figure 5.13: Shown are the signal distributions (top), rise time distributions (2nd row), 1D cluster size distributions (3rd row) and 2D cluster size distributions (bottom) for the M129, M112 and M106 sub-matrices of a non-irradiated Investigator (left to right).



Figure 5.14: Shown are position resolved efficiencies for sub-matrices M129, M112 and M106 (top to bottom). On the left 2D resolved efficiencies for an amplitude cut of 5 mV are shown while the middle and right columns show efficiency projections for increasing amplitude cuts in X and Y direction, respectively. For M129 and M112 efficiencies quickly drop for higher amplitude cuts while M106 maintains efficiency.
## 5.1.5 Sensor performance after irradiation

In order to test if the Investigator can maintain its performance after the estimated life time fluence of  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL several samples were sent to the Triga reactor facility in Slovenia for neutron irradiation to that level. It was not possible to put bonded samples into the reactor because the carrier boards for the chips were too large. Consequently, measurements for non-irradiated and irradiated samples were done on physically different chips. The measurements for irradiated samples were done as presented in the previous sections using the same analysis methods and the same experimental setup but cooled to -20 °C.

A comparison of SNR, rise time and cluster size is shown in figure 5.15. Compared to non-irradiated results a clear reduction of the SNR can be observed and there is a significant overlap of the noise and signal distributions. For sub-matrix M129 a reduction of the SNR from  $\sim 6$  to  $\sim 4$  is observed. Sub-matrix M112 maintains its performance better but also shows a reduction of the SNR from  $\sim 8$  to  $\sim 6$ . The most significant reduction is observed for sub-matrix M106 where the SNR drops by 75% down to  $\sim 6$  and now shows no better performance than the larger pitch pixels.

In terms of cluster size no significant change is observed for M129 and M112 which already showed a nearly single-pixel response before irradiation. A significant reduction is observed for M106 where the cluster size for a 5 mV cut reduces from  $\sim 2$  to  $\sim 1.5$  and an almost single-pixel response for higher cuts.

The signal rise time for samples M129 and M112 shows similar results in that the mean rise time only increases slightly but the standard deviation increases significantly by  $\sim 30\%$ . For sub-matrix M106 the mean rise time is reduced by 3 to 4 ns and the rise time standard deviation for M106 more than doubles to 4.8 ns for a 5 mV cut. The corresponding distribution shows a significant tail towards higher rise times. The overall increase of noise is caused by an increased leakage current due to radiation damage.

At the time when these results became available the first fully digital prototype of the MALTA design was already in production. Laboratory characterizations showed an increase in charge sharing after irradiation and additionally an increase in gain. Furthermore, there was no indication of major charge loss due to trapping based on source scans with <sup>55</sup>Fe and <sup>90</sup>Sr. The dramatic reduction of the signal MPV for the M106 pixel was thus attributed to charge being lost to neighboring pixels which were not read out. For pixel designs with a large spacing and pitch cluster sizes were already close to unity before irradiation and stayed the same after. Consequently, it was assumed that for these pixel pitches sufficient signal amplitudes were maintained because virtually no charge sharing occurred. The lower rise time of M106 could be explained by the increase in gain.

Table 5.4: Given are the measured values for the signal-noise-ratio, mean cluster size and mean rise time for sub-matrices M106, M112 and M129 after irradiation to  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL.

sub-matrix	amplitude cut	parameter	value mean ( $\pm$ std. dev.)
M106	$5\mathrm{mV}$	SNR	5.7
M112	$5\mathrm{mV}$	SNR	5.6
M129	$5\mathrm{mV}$	SNR	3.9
M106	$5\mathrm{mV}$	cluster size	1.47 [pixels]
	$10\mathrm{mV}$		$1.19 \; [\text{pixels}]$
	$50\mathrm{mV}$		$1.01 \; [pixels]$
M112	$5\mathrm{mV}$	cluster size	1.09 [pixels]
	$10\mathrm{mV}$		1.03  [pixels]
M129	$5\mathrm{mV}$	cluster size	1.06 [pixels]
	$10\mathrm{mV}$		1.02  [pixels]
M106	$5\mathrm{mV}$	rise time mean	$16.5 \pm 4.8 [ns]$
	$10\mathrm{mV}$		$16.4 \pm 4.3 [ns]$
	$50\mathrm{mV}$		$15.0 \pm 1.4 [ns]$
M112	$5\mathrm{mV}$	rise time mean	$29.9 \pm 6.7 \text{ [ns]}$
	$10\mathrm{mV}$		$30.0 \pm 6.5 \text{ [ns]}$
M129	$5\mathrm{mV}$	rise time mean	$28.6 \pm 7.6 \text{ [ns]}$
	$10\mathrm{mV}$		$28.9 \pm 7.2 \; [ns]$

However, the cluster size distribution presented here shows a reduction in cluster size and the corresponding 2D profile does not support the hypothesis that charge is lost solely due to charge sharing. If this were the case a more uniform 2D cluster size profile would be expected. Similarly, based on how they are calculated in the analysis of this data, a much more significant increase of noise amplitudes would be expected as well since the spatial cut that is used to identify noise would be compromised. Consequently, it is plausible to assume that significant charge is lost at the pixel borders. The results of figure 5.15 in numbers are given in table 5.4.

The sensor efficiency for M129, M112 and M106 (top to bottom) after  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL is shown in figure 5.16. For the lowest amplitude of 5 mV all three samples still reach a uniform efficiency above 97%. However, this cut is only possible because



Figure 5.15: Shown are amplitude, rise time and cluster size spectra for sub-matrices M106, M112 and M129 after irradiation to  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL.



Figure 5.16: Shown are position resolved sensor efficiencies in 2D on the left and efficiency profiles for X and Y direction in the middle and right for a fluence of  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL.

the amplitude before and after a signal step is calculated as the mean voltage in a 50 ns window as shown in section 5.1.2 which strongly suppresses noise. For stronger cuts the x and y projections show that the efficiency quickly drops below 90 % and an additional loss of efficiency is observed at pixel corners (note that the 2D resolved efficiencies are shown for a 5 mV cut). This effect is especially strong for sub-matrix M106 and supports the conclusions drawn from cluster sizes concerning charge loss at the pixel borders.

Finally, one Investigator sample was irradiated to  $2.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL and the M106 matrix tested. Other samples could not be tested due to time constraints of the SPS test beam schedule. A summary of the results is shown in figure 5.17. After twice the expected life time dose the sensor shows further deterioration of the SNR which drops to  $\sim 3$ . While the efficiency drop at the border of the 2×2 pixel matrix is still caused by the



Figure 5.17: Shown is a summary of results for sub-matrix M106 after irradiation to  $2.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL.

telescope's finite resolution there is now also a drop of efficiency at the border of individual pixels and at the center of the plot in the pixel corners. The cluster size is further reduced and for an amplitude cut of 10 mV the sensor effectively shows a single-pixel response. The rise time spectrum shows a significant tail to larger rise times while the most probable value remains roughly the same which indicates a further increase in noise. The second peak to the left in this distribution is caused by periodic noise on the analogue signal from the sensor. Overall, these results are in line with the trends that were observed for non-irradiated samples and samples irradiated to  $1.0 \times 10^{15}$  1 MeV n<sub>eq</sub>/cm<sup>2</sup> NIEL.

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Figure 5.18: Images of MALTA bonded to its carrier board.

# 5.2 TowerJazz MALTA

The development of MALTA [30] [31] [32] [33] [34] [35] is based on the previous development of the monolithic pixel detector ALPIDE [20] [36] by the ALICE experiment and measurements with the TowerJazz Investigator. Accordingly, the acronym "MALTA" — Monolithic from ALice To Atlas — was chosen. Based on results with the TowerJazz Investigator [27] [24], this pixel detector features a matrix of  $512 \times 512$  pixels with a  $36.4 \mu m$  pixel pitch along both, columns and rows, a small collection diode of 2 or 3 microns diameter and a spacing around the diode of 3.5 or  $4\mu m$ . Its surface area is roughly  $2 \times 2 \text{ cm}^2$ . Images of the detector bonded to its carrier board are shown in figure 5.18.

The chip's design goal is to meet the requirements for the ATLAS ITk outer layer of the high luminosity upgrade of the LHC mainly focusing on a NIEL life time fluence of  $10^{15}$  1 MeV  $n_{eq}/cm^2$  and a life time TID of 80 MRad [5]. These requirements are much more demanding compared to the ALICE environment in terms of timing and radiation hardness and consequently place various constraints on the the chip's circuit and pixel design [15].

## 5.2.1 Pixel sensor and analogue front end design

Compared to the TowerJazz Investigator, which is read out purely analogically, the MALTA pixel features a more complex analogue front-end and digital readout circuit. An image of the in-pixel circuit layout can be seen in figure 5.19. It shows a clear spatial separation between analogue and digital front end to minimize potential cross-talk. A circuit diagram of the analogue front-end of MALTA is shown in figure 5.20.



Figure 5.19: Shown is a top-down view of the physical layout of the MALTA pixel front end.

In the DC state of the circuit the transistor M0 acts as a source for the current IBIAS which biases the source follower M1. M2 is a cascode transistor that prevents capacitive coupling between OUT\_A and M1. M5 acts as a source for the ITHR current and, together with M6, provides a low-frequency feedback to  $OUT_A$ . M3 is regulated to sink IBIAS and ITHR via the GN node. The transistors M7, M8 and M9 form a discriminator stage. While no signal is detected the current across M7 dominates compared to the current across M9 and OUT\_D is pulled high towards AVDD.

In the AC state, when charge is collected, the voltage at IN drops and CS discharges into OUT\_A as described in section 4.2.1. The voltage increase on OUT\_A will increase the current through M9 which will draw OUT\_D down to AVSS. The threshold at which this will occur is set by the current across M7 which is controlled by the DAC voltage labeled 'IDB'. The rising voltage on OUT\_A will also eventually turn off M6 so that it can't sink the current from M5 anymore. This in turn will raise the voltage on the GN node via M5. The resulting current increase through M3 will return OUT\_A to its baseline voltage. This feedback can be further tuned for large signals via M4.



Figure 5.20: Shown is the schematic of the in-pixel analogue front end of MALTA. Image kindly provided by the author of [15].

The collection diode reset is either implemented as a diode with a constant reset current or a configurable PMOS current mirror. While the diode reset is simpler to implement and has a lower input capacitance, its reset current is not configurable which might be an issue when conditions change after irradiation. The reset diode current is also dependent on the signal induced voltage change on the collection diode.

# 5.2.2 Asynchronous pixel matrix

As shown in figure 5.21 the left and the right half of the chip are different with respect to the reset mechanism (diode or PMOS). In order to operate the right side of the chip properly, additional DACS have to be configured to set the reset current. Power pads and an optional CMOS I/O for multi-chip configurations are located at the side of the matrix while the slow control, arbiter-merger structure, DACs and output pins are at the bottom.

The deep p-well, which shields n-implants of the PMOS circuitry from the depletion area and prevents their interference with charge collection, comes in two configurations. In the maximum configuration the deep p-well houses the entire in-pixel circuit while in the medium configuration it is removed in areas where only NMOS circuitry is present (in addition to the courtyard around the collection diode). Furthermore the collection n-well is either  $2\mu m$  or  $3\mu m$  in diameter and the spacing is either  $3.5\mu m$  or  $4.0\mu m$ . A full list of all pixel configurations can be seen in table 5.5.



Figure 5.21: Image of the MALTA detector and its 8 sectors of varying pixel layouts and reset mechanism.

Table 5.5: A list of pixel layout and reset modifications featured in the various sectors of MALTA.

sector	reset	diode size $[\mu m]$	spacing $[\mu m]$	deep p-well size
0	diode	2.0	4.0	medium
1	diode	2.0	4.0	maximum
2	diode	3.0	3.5	maximum
3	diode	3.0	3.5	medium
4	PMOS	3.0	3.5	medium
5	PMOS	3.0	3.5	maximum
6	PMOS	2.0	4.0	maximum
7	PMOS	2.0	4.0	medium

The whole pixel matrix is divided into 256 vertical double columns each of which contains 64 pixel groups of  $2 \times 8$  pixels. These groups are separated into odd and even groups which talk to different column buses. This is done to increase the readout bandwidth and to reduce the chance of data collisions on the buses since neighboring groups never talk to the same bus (vertical neighbors talk to even and odd buses, horizontal neighbors are in different double columns). This layout is illustrated in figure 5.22. An individual pixel in a  $2 \times 8$  pixel group is identified via the position of its bit within a 16 bit word that encodes the state of each pixel in the group ('1' for a hit, '0' for no hit). The group of the triggered pixel is identified via 5 bits which encode the group ID and 1 bit that encodes the 'group parity', i.e. if the group was even or odd. The double column is identified via an 8 bit column ID. Thus, a total of 30 bits encode the absolute position of a pixel on the matrix. Since up to 16 bits can be read out at once from a group the readout efficiency of this layout improves for larger cluster sizes where multiple pixels of a group are triggered by an incident particle.

Data from the pixel matrix is read out to the chip periphery via a novel asynchronous readout mechanic which allows to forego the propagation of a clock to the pixels and significantly reduces power consumption. Thus, registered pixel hits are not latched but instead sent to the chip output directly. A drawback of this design is that the TOT cannot be measured and the pixel response this thus binary.

When one or more pixels in a group are triggered, the 16 bit word of the corresponding group together with a reference bit and the 5 bit group ID are directly sent to the end-of-column where the parity bit is added. At this level the MALTA matrix has 512 asynchronous parallel data streams (two for each double column due to the dual-bus structure). While this maximizes the chip's data rate capabilities it also means that an arbiter-merger mechanic is necessary to serialize the output of the pixel matrix so that individual MALTA words don't collide at the chip's output pins which would cause data corruption. After the end-of-column there are 9 consecutive levels of the arbiter-merger which merge two neighboring data streams of the previous level by delaying one with respect to the other, if necessary. A 3 bit delay counter keeps track of how often a MALTA word was delayed. Also, each layer of the arbiter-merger after the first adds one bit to the column ID. Finally, a 2 bit bunch-crossing identifier (BCID) and a 4 bit chip identifier (CHIPID) are added for the full 40 bit MALTA word. The chip furthermore supports chip-to-chip powering and communication. A tenth arbiter-merger layer is present to merge possible data streams from neighboring chips.

The reference bit is necessary to indicate when data is present at the chip output. It is the only bit of the MALTA word which will always be '1'. Since the chip's output is



Figure 5.22: A sketch to indicate the composition of the MALTA word and how it translates to the matrix.

asynchronous the corresponding readout by an FPGA (field programmable gate array) must be designed accordingly and is explained in detail in the next section.

## 5.2.3 Asynchronous readout

Once a pixel hit is registered the corresponding MALTA word is asynchronously transmitted to the 40 parallel output pins at the bottom of the chip. LVDS (low voltage differential signal) drivers that can operate at up to 5 Gb/s ensure a reliable data transmission off-chip. MALTA is bonded to a high density 10 layers carrier board, as shown in figure 5.18, which interfaces to a VIRTEX VC707 evaluation board<sup>3</sup> via a high pin count FMC (FPGA mezzanine card) connector.

An image depicting the asynchronous readout scheme of the MALTA firmware is shown in figure 5.23. Each output pin is monitored by its own oversampling module which consists of a differential buffer and a delay module. One part of the differential data stream is delayed by 45° with respect to the other. Then both parts are sampled at a rate of 1.28 GHz by using four 320 GHz clocks which are phase shifted by 0°, 90°, 180° and 270°. Due to the 45° shift of one part of the differential data stream, the effective sampling

 $<sup>{}^3</sup> Xilinx \, Virtex-7 \, FPGA \, VC707 - https://www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html$ 

#### 5.2. TOWERJAZZ MALTA



Figure 5.23: Shown is a visualization of the oversampling scheme of a MALTA output  $pin^4$ .

rate of the whole signal is doubled to 2.56 GHz. This readout method provides an 8 bit sample block of a 3.125 ns frame at every rising edge of the 0° 320 MHz clock for every output pin. The resulting 390 ps resolution is necessary to ensure that MALTA words are registered by at least one sample because the pulse width of the MALTA output can be configured to be 2, 1, 0.75 or 0.5 ns.

The oversampling module of the reference bit is continuously monitored and the sampled 8-bit patterns are checked against a look-up-table to determine whether a 1 was registered in which case the sample patterns of all pins are read out. Special attention is paid to reference signals that sit between sample blocks so that an individual MALTA word is not sampled twice.

If a signal is found on the reference pin, the bits of the corresponding sample block are compared to the bits of sample blocks of all other pins. The following bit-wise operation is performed to reconstruct the full MALTA word:

$$maltaBit_i = \bigvee_{j=0}^{j<8} (sample_{0,j} \wedge sample_{i,j})$$
(5.2)

Where  $maltaBit_i$  is a bit of the MALTA word,  $sample_{0,j}$  is the j-th sample of the reference sample block and  $sample_{i,j}$  is the j-th sample of the sample block of pin *i*. A graphical explanation can be seen in figure 5.24.

Due to the reconstruction method of the MALTA word it is vitally important that the data streams of all output pins are well aligned in time. For this reason both differential

<sup>&</sup>lt;sup>4</sup>drawn with wavedrom, https://wavedrom.com/, last accessed: 01.09.2020



Figure 5.24: Reconstruction of two consecutive (red and blue) MALTA words from the asynchronous oversampling.



Figure 5.25: Shown is a cumulative plot of the relative bit-wise timing of 2000 words read out from MALTA before (left) and after (right) time alignment.

branches of each data stream from a MALTA output pin are piped through a proprietary Xilinx delay module called IDELAYE2<sup>5</sup> of the FPGA which allows to align all data streams in time to within 78 ps. The effect of this alignment can be seen in figure 5.25. The possible effects of a bad time alignment are twofold:

**Time alignment across pins** As shown in figure 5.25 the initial data from MALTA has to be aligned so that all pins are sampled at the same relative point in time. Without this alignment signals may miss the readout window which is defined by the reference bit. Due to the nature of this output stream, a 0 is sampled by default but a 1 can be missed and would corrupt the resulting MALTA word.

<sup>&</sup>lt;sup>5</sup>Xilinx 7 series FPGAs SelectIO Resources, https://www.xilinx.com/support/documentation/user\_guides/ug471\_7Seriest accessed: 01.06.2020



Figure 5.26: The first source spot recorded on MALTA. The vertical segmentation of the pixel matrix indicates the varying performance of different MALTA sectors.

Time alignment of the differential data stream A more subtle issue can arise from a bad time alignment of the differential data streams which come from the same pin, specifically the pin of the reference bit. Due to the nature of the oversampling method it is important that the phase difference of  $45^{\circ}$  between both branches of the signal is precisely maintained. If this is not the case, merging the samples from both branches will result in a wrong time-ordering and produce wrong 8 bit patterns which are in turn rejected by the look-up-table. This results in a overall loss in efficiency of the readout due to a random chance that the reference bit will not be recognized.

The reconstructed MALTA word is finally stored in a FIFO together with a 390 ps time stamp — based on where inside the 8 bit sample block the rising edge of the reference bit was detected — and a trigger ID. The total word length is then 62 bits. The trigger ID is used to reconstruct an event based data stream which is necessary for beam tests where the MALTA data has to be synchronized to that of a beam telescope. An image of the first source scan ever recorded with the working MALTA readout is shown in figure 5.26. The structure of the various pixel flavor sectors across the matrix can be seen.

## 5.2.4 Threshold and noise

It was quickly discovered, that the slow control of this first prototype of MALTA was not fully functional. Some internal voltages could not be reliably supplied by the chip's DACs and had to be supplied externally. One of these voltages configured the discriminator



Figure 5.27: Shown is a threshold scan for an individual pixel on MALTA.

stage at the output of the analogue front end which is responsible for the global threshold of the detector. This voltage is therefore the main parameter to change the threshold across the pixel matrix and very important for beam tests and efficiency studies. In the following chapter this voltage will be referred to as 'IDB' based on the label of the M7 transistor in the MALTA analogue front-end (figure 5.20).

The pixel threshold is measured by injecting test pulses of increasing voltage into the in-pixel test capacitance which is wired directly to the collection n-well. For each voltage a fixed number  $N_0$  of pulses is sent and the fraction M of pulses for which the pixel was triggered is recorded. The voltage is increased until the pixel response saturates, i.e.  $N_0=M$ , as shown in figure 5.27. The rising edge of the scan, which indicates the threshold, will move depending on the voltage that is applied to the discrimination stage of the MALTA front-end. The data points are fitted with a Gaussian error function

$$f(x|N_0,\mu,\sigma) = \frac{N_0}{2} \left( 1 + Erf\left(\frac{x-\mu}{\sqrt{2}\sigma}\right) \right)$$
(5.3)

where  $N_0$  is a scaling factor and corresponds to the number of pulses sent to the chip. The parameters  $\mu$  and  $\sigma$  are fit parameters and correspond to the threshold and noise, respectively. The conversion of the voltage amplitude of the test pulse into the equivalent injected charge in the analogue front-end is explained in detail in [15].

The results for increasingly lower threshold settings for an non-irradiated MALTA sample are shown in figure 5.28. At the time of writing, the raw data to these plots was not available anymore and cosmetic alterations to these figures were thus not possible. The labels 'Sec 1' and 'Sec 2' correspond in fact to sectors S2 and S3, respectively, as shown in figure 5.21. The top threshold scan was performed for IDB = 1.00 V and shows an average threshold of 515 e<sup>-</sup> for sector S2 and 465 e<sup>-</sup> for sector S3, respectively. The middle set of plots was recorded for IDB = 1.25 V and shows thresholds of 375 and 339 e<sup>-</sup>. The bottom set for IDB = 1.36 V shows thresholds of 249 and 226 e<sup>-</sup>. These scans only give an indication of the threshold based on the IDB voltage due to the small amount of pixels that were scanned but they show that sector S3 consistently reaches a lower threshold. The only difference in the pixel design for these two sectors is the dimension of the deep p-well which houses the in-pixel electronics and will be discussed more closely in a later section. Note that the test pulses are injected into the collection n-well through a capacitor and the shape of the deep p-well may have an influence on the voltage-to-charge translation in sectors with different deep p-wells<sup>6</sup>.

The threshold distributions show that there is significant threshold dispersion of roughly 40 e<sup>-</sup>. This was attributed mainly to the M3 transistor of the analogue front-end. Due to its small size this transistor tends to have a low impedance which is also prone to pixel-to-pixel fluctuations<sup>7</sup>. This in turn lowers and de-stabilizes the gain of the analogue front-end and increases the threshold dispersion. Furthermore, the noise distributions show a pronounced tail towards higher noise. Here it is assumed that the M1 and M3 transistors are sources of RTS noise in the circuit. The proposed solution for both these problems was to increase the length of the M3 transistor which would increase its impedance and thus stabilize the gain and also increase the area of its gate which reduces RTS noise.

A direct comparison of the threshold and noise at IDB = 1.00 V before and after irradiation to  $5.0 \times 10^{14}$  1 MeV n<sub>eq</sub>/cm<sup>2</sup> NIEL is shown in figure 5.29. While the threshold dispersion and the noise after irradiation increase significantly, the mean threshold is similar to non-irradiated results and reduces by roughly 4% for sector 2 (labeled 'Sec 1') and increases roughly 8% for sector 3 (labeled 'Sec 2'). Based on these results it can be expected that irradiated chips will have significant noise hit rates and that low operational thresholds will be difficult to achieve.

### 5.2.5 Beam test data treatment

Due to issues with the functionality of the slow control, individual noise triggered pixels could not be masked reliably on the chip and had to be filtered offline. However, this does not prevent data corruption at the chip output if noise triggered MALTA words collide there with valid data. Thus, the noise was reduced by deactivating large parts of the MALTA matrix entirely. A first step was to deactivate the right half of the detector

<sup>&</sup>lt;sup>6</sup>personal communication with the author of [15]

<sup>&</sup>lt;sup>7</sup>personal communication one of the authors of [36]



Figure 5.28: Shown are threshold distributions of sectors S2 and S3 (labeled 'Sec 1' and 'Sec 2' in the plots) of the MALTA matrix. The voltage for IDB was set to 1.0, 1.25 and 1.36 V from top to bottom. Sector S3 consistently reaches lower thresholds.



Figure 5.29: Shown are threshold distributions of sectors S2 and S3 (labeled 'Sec 1' and 'Sec 2' in the plots) of the MALTA matrix. The voltage of IDB was set to 1.0 V for a MALTA sample that was non-irradiated (top) and irradiated to  $5.0 \times 10^{14} \text{ 1 MeV } n_{eq}/\text{cm}^2$  NIEL (bottom).

by increasing the current through the PMOS reset to the point where signals were not detected anymore. Then sectors S0 and S1 were deactivated by masking their entire double columns. Luckily, some samples also allowed to mask rows in order to reduce the active area on the chip even further which kept the noise at manageable levels. As a result only sectors S2 and S3 were studied in depth in beam tests. However, this also enabled thresholds of irradiated samples that were close to the design threshold of 200 e<sup>-</sup>. The reduced active area on MALTA is referred to as the region of interest or ROI.

Any noise that was still present in the data offline was filtered by comparing the hit rate of a pixel to the mean hit rate of its neighbors. The hit rate of each individual pixel is calculated as the fraction of pixel triggers over the global number of readout triggers for the detector

$$r_{i,j} = \frac{N_{hit|i,j}}{N_{trigger}} \left[ \frac{hits}{events} \right]$$
(5.4)

where  $r_{i,j}$  is the hit rate of the pixel with coordinates (i,j),  $N_{hit|i,j}$  the number of times pixel (i,j) was triggered and  $N_{trigger}$  the number of triggers received by the detector. Then, the mean hit rate of all neighbors in the surrounding 7×7 pixel area is calculated as

$$\overline{r_{i,j}} = \frac{\left[\sum_{k,l=0}^{k,l=3} r_{i+k,j+l}\right] - r_{i,j}}{48} \left[\frac{hits}{events}\right].$$
(5.5)

Any pixel for which

$$\frac{r_{i,j}}{r_{i,j}} \ge 5 \tag{5.6}$$

was true was considered 'noisy'. Any track with a reconstructed intersection point on a noisy pixel was removed from the data. A summary plot of the fraction of offline masked pixels for all MALTA data sets studied in this work is shown in the appendix, section C. For all runs this fraction stayed below 1% of pixels of the ROI.

Cuts were applied to the reduced  $X^2$  value of track fits and the distance between the DUT cluster positions and track intersection points. The distance cut was set to  $60 \,\mu\text{m}$  and the reduced  $X^2$  cut to 3 for all runs. An overview of the  $X^2$  values and track-cluster residuals for all runs is shown in the appendix, section C.

Recorded data sets were merged and synchronized by continuously monitoring the track-cluster residuals of individual tracks. In the event of a de-synchronization the average track-cluster distance per match suddenly increases because tracks and clusters from different events are matched. An example is shown in figure 5.30 where the telescope



Figure 5.30: Shown is an example of a DUT de-synchronization. The average track-cluster residual increases suddenly as tracks and clusters of different events are matched up.

and DUT data de-synchronize after roughly 46000 events. In order to re-synchronize the telescope and DUT data streams are shifted event by event with respect to each other until the track-cluster residuals return to expected values.

### 5.2.6 Efficiency and cluster size in beam tests

The very first beam test with MALTA was performed at the ELSA facility in Bonn<sup>8</sup> where an FE-i4 telescope (described in section 5.1.1) was used for track reconstruction. Then, once a pion beam was available at the SPS at CERN further beam tests were conducted there. First beam tests at the SPS were still done with the FE-i4 telescope but eventually the KARTEL telescope which is owned and operated by the University of Ljubliana  $^9$  was used to improve spatial resolution for in-pixel efficiency studies. The MIMOSA-26 pixel detector [37], which is the main detector of the KARTEL telescope, features a  $1152 \times 576$ pixel matrix with a total sensitive area of  $2.2 \,\mathrm{cm}^2$  and a symmetric pixel pitch of  $18.4 \,\mu\mathrm{m}$ . The pixel readout of this chip is binary. The geometry and track-residual distributions achieved for this telescope are shown in figure 5.31. The KARTEL telescope consists of two telescope arms (planes 0,1,2,4,5 and 6 in the image) which each contain three MIMOSA detectors for high resolution tracking. Since MIMOSA has a comparatively slow rolling shutter readout (a few 100 µs per frame) it is necessary to include an FE-i4 detector in the telescope for better timing precision (plane 3 in the image). While in the beginning only one DUT was mounted for tests, later test beam campaigns had two DUTs mounted to increase the throughput of tested chips.

The KARTEL telescope provides a track resolution of roughly  $8\,\mu m$  in both directions

<sup>&</sup>lt;sup>8</sup>https://www-elsa.physik.uni-bonn.de/

<sup>&</sup>lt;sup>9</sup>https://www.uni-lj.si/eng/about\_university\_of\_ljubljana.aspx

based on the residual distributions shown at the bottom of figure 5.31. It should however be noted, that the average cluster size for the first MALTA prototype was very close to 1 (i.e. mainly single-pixel clusters) and that due to the asynchronous design of the MALTA matrix, the sensor response is binary, i.e. no time-over-threshold information is available. Under these circumstances the resolution of MALTA can be approximated by pitch/ $\sqrt{12} \approx 10.5 \,\mu\text{m}$  and likely contributes significantly to the width of these residual distributions.

The results of the first beam tests with non-irradiated samples are shown in figure 5.32. The plots represent in-pixel maps of  $2 \times 2$  pixels and were obtained by superimposing even and odd double columns and double rows on top of each other. Thus, for example, the bottom left quarter of a plot represents all pixels with an even column and even row whereas the top right quarter represents all pixels with an odd column and an odd row. While both sectors S2 and S3 of MALTA were tested, these plots show in-pixel maps for S2 only which has a maximum deep p-well.

The in-pixel efficiency and cluster size at a high threshold of  $470 e^-$  (left), a medium threshold of  $400 e^-$  (middle) and a low threshold of  $210 e^-$  (right) show a significant improvement of sensor performance for lower thresholds. At a high threshold a significant efficiency gradient can be seen away from the pixel center where the collection n-well is located. At pixel centers, an efficiency well above 90% is measured while in pixel corners the efficiency drops as low as 50%. This can be explained by charge sharing at pixel borders combined with a large threshold. The particle beam used for these tests was a 180 GeV pion beam with an expected most probable charge deposition of 1600 e<sup>-</sup>. If the signal is shared evenly among 4 pixels, there is a high chance that it will be missed at a threshold of 400 e<sup>-</sup> or more. Only once the threshold is lowered to 210 e<sup>-</sup> the efficiency profile flattens out.

Consistent with this hypothesis, the cluster size increases at pixel edges where charge sharing is more likely. At high and medium thresholds this increase is only small due a low efficiency in this area. However, at a low threshold the cluster size at pixel corners increases significantly. This indicates that the change to a 200 e<sup>-</sup> threshold is an important transition which enables the chip to reliably detect signals from all areas of the pixel. This is consistent with the design goal given in [15].

To test the detector performance after irradiation, a selection of samples was irradiated to a fluence of  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL. These chips were kept at temperatures of -20°C during all beam tests. The results for sector S2 are shown in figure 5.33 for efficiency (top) and cluster size (bottom). From left to right the thresholds are 310 e<sup>-</sup>, 240 e<sup>-</sup> and 210 e<sup>-</sup>. The substrate was biased to -15 V and the p-well to -6 V.



Figure 5.31: Shown is the telescope geometry (top) for the MIMOSA telescope at the SPS and its resolution based on track residuals (bottom). Telescope planes 0,1,2,4,5 and 6 are MIMOSA pixel detectors. Plane 3 is a single Fe-i4 detector to improve timing.



Figure 5.32: Shown are results for efficiency (top) and cluster size (bottom) for a threshold of  $470 e^-$  (left),  $400 e^-$  (middle) and  $210 e^-$  (right). The DUT was a non-irradiated MALTA chip with a substrate bias of -15 V and a p-well bias of -6 V. Each plot shows in-pixel distribution of  $2 \times 2$  pixels.



Figure 5.33: Shown is the evolution of efficiency (top) and cluster size (bottom) for a high threshold of  $310 e^-$  (left), a medium threshold of  $240 e^-$  (middle) and a low threshold of  $210 e^-$  (right) for a sample irradiated to  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL at a substrate bias of -15 V and a p-well bias of -6 V.

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Figure 5.34: Shown are the deep p-well shapes (top) of sectors 2 (left) and 3 (right) and the corresponding in-pixel efficiency patterns (bottom). The efficient areas of the pixel clearly follow the shape of the deep p-well or rather the pixel is efficient in areas where the deep p-well is not present.

The efficiency maps now show a drastic decline to almost 0% at pixel corners. Even for low thresholds only a minor improvement can be seen at pixel edges and at the same time a deterioration is observed at the pixel center. This phenomenon can be explained by the interplay of two factors. First, a lower threshold raises the noise output of the detector and consequently the probability that valid data collides with noise at the chip output and is corrupted because the arbiter-merger is not working. Second, shared signals have a significantly increased chance of detection at lower thresholds. At pixel borders the efficiency gain through a lower threshold is larger than the loss due to data corruption. At the pixel center, where no charge sharing occurs, it is the opposite.

The cluster size maps show a similar picture as the efficiency maps in that no strong dependency on threshold can be seen. Overall, most clusters are single pixels and only at the edges, where efficiency drops severely some increase in cluster size can be seen.

Two important conclusions can be drawn from these measurements:



Figure 5.35: Shown is the development of the efficiency and cluster size for an non-irradiated MALTA sensor operated at a threshold of  $\sim 210 \,\mathrm{e}^{-}$  for increasing substrate bias. A clear decrease of efficiency at pixel corners can be observed.

Significant signal loss occurs at pixel edges Detector efficiency is severely reduced at pixel edges after irradiation even though thresholds around 200 e<sup>-</sup> could be reached. Since the threshold is the same before and after irradiation at the lowest setting this indicates that already small signals at the pixel edges are significantly reduced further after irradiation likely due to a significant reduction in charge collection efficiency of the sensor.

An important hint to improve charge collection comes from comparing the in-pixel maps of sectors S2 and S3. As shown in figure 5.34 there is a clear difference in the shape of the efficient region around the collection n-well which follows the shape of the area in the pixel where the deep p-well is spared out. The substrate voltage can be varied from -6 to -20 V and the vertical electric field component can thus be increased significantly. However, the deep p-well is always kept at a voltage of -6 V which cannot be lowered further due to the CMOS circuitry inside. Similarly, the collection n-well is kept at a voltage of 0.8 V and thus the lateral electric field from it to the deep p-well is comparatively weak and cannot be changed. A deep p-well that extends across most of the pixel thus reduces the lateral component of the electric field. However, for signals at the pixel border the lateral field strength is critical to maintain fast and efficient charge collection. This is especially important to reduce charge trapping after irradiation. Indeed, increasing the substrate bias voltage on the detector above 12 V lowers the efficiency at pixel borders because the vertical field component dominates and reduces lateral charge collection efficiency. This effect is shown in figure 5.35. In hindsight, this also explains the previously presented results with the Investigator. Due to the small spacing the deep p-well covered almost the entire pixel and weakened the lateral electric field. After irradiation any occurring charge loss due to trapping was further exacerbated by a much slower charge collection at pixel borders.

Noise increases significantly after irradiation Threshold scans and test beam results clearly show that a threshold at or below 200 e<sup>-</sup> will be necessary for a fully efficient pixel. However, higher noise levels at lower thresholds must be avoided to prevent data corruption at the chip output. Furthermore, while noisy pixels can be masked, this also reduces the active area of the detector and thus its overall efficiency. So far, the entire detector could not be activated during a beam test due to too many noisy pixels.

To be able to lower the threshold sufficiently while keeping noisy pixels in check, the threshold dispersion must be reduced. The proposed alterations to the MALTA front-end to address these issues were already discussed in section 5.2.4. All the details of the MALTA front-end redesign can be found in [15].



Figure 5.36: Shown is a time-to-trigger distribution measured on sector S2 of a non-irradiated MALTA sample.

## 5.2.7 Timing profiles in beam tests

The MALTA firmware can compensate for trigger latencies of up to 800 ns (256 bins of 3.125 ns each) and reads out a 500 ns frame for each arriving trigger. An example for a time-to-trigger distribution of data recorded in sector S2 with a non-irradiated sample is shown in figure 5.36. It can be seen that the trigger latency of the setup was rougly 170 ns. This trigger delay is added as a time stamp to every MALTA word that is read from the chip. Thus the timing of a particle hit relative to the corresponding trigger is known. The beam test setup was however not optimized for precise timing measurements and thus the latching of asynchronous signals in the trigger logic adds a jitter to the time stamps which is assumed to be in the order of 10 to 20 ns. For large data sets this jitter is expected to average out while any constant contributions, for example a consistently higher time-walk, do not.

The in-pixel timing profiles in figure 5.37 are shown for a non-irradiated MALTA sample at a threshold of ~200 e<sup>-</sup> on the left and a MALTA sample irradiated to  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL at a threshold of 360 e<sup>-</sup> on the right. The top row corresponds to sector S2 and the bottom row to sector S3. The substrate bias was set to -12 V for both samples. The z-axis shows the time-of-arrival relative to the lowest value in each plot. This was done due to varying trigger settings and latencies across individual data taking runs. A clear increase in time of arrival further from the collection n-well can be seen and the timing profiles perfectly match the shape of the efficiency profiles from the previous chapter for both sectors. The profiles for the non-irradiated sample show a range of 30 and 40 ns for sectors S2 and S3, respectively. The range of the irradiated sample is roughly halved to

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18 and 16 ns for the same sectors. This effect may be explained by type inversion due to irradiation which affects the doping profiles in the silicon bulk. Specifically for the MALTA detector, a reduced doping of the planar n-layer that stretches across the entire pixel matrix may lead to stronger depletion in the sensor bulk for a given substrate bias. It is assumed that this lowers the capacitance on the collection diode and increases its gain. This would then also result in larger signals and a reduced time-walk. It will be shown in later chapters that the effective threshold of the MALTA sensor does indeed decrease after irradiation.



Figure 5.37: Shown are in-pixel timing profiles for a non-irradiated MALTA sample (top) at a threshold of  $\sim 200 \,\mathrm{e}^{-}$  and a MALTA sample irradiated to  $1.0 \times 10^{15} \,\mathrm{1 \, MeV} \,\mathrm{n_{eq}/cm^2}$  NIEL (bottom) at a threshold of 360 e<sup>-</sup> The plots on the left correspond to sector S2, those on the right to S3.

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Figure 5.38: Shown are simulation results of the electric field in the sensor before modifications to the planar n-layer. Figures kindly provided by the author of [38].

## 5.2.8 TCAD simulations for the MALTA sensor

In order to better understand the significant drop of efficiency at pixel borders after irradiation, a detailed study of the electric fields inside the pixel and the resulting charge collection was necessary. This was done using 3D self-consistent transient TCAD (technology computer aided design) simulations. An overview of the results is presented here. All plots in figures 5.38, 5.40 and 5.41 were kindly provided by the Author of [38] who performed these simulations and a more detailed discussion is presented there.

As already mentioned, the drift paths of deposited charge in a sensor with a small collection n-well design are longer and in combination with the weak lateral electric field this causes a longer charge collection time and exacerbates the negative effects of radiation damage. This intuitive explanation is confirmed by the TCAD simulations of the electric field shown in figure 5.38. The black arrow lines indicate the direction of the electric field while the coloring indicates the field strength. The left plot shows the lateral field strength which is zero at the border between pixels (indicated by a black star) and only increases close to the collection n-well (edges of the plot). The middle plot shows the vertical electric field (i.e. along the sensor depth) which is fairly homogeneous across the entire pixel with some increase towards the collection n-well. The electrostatic potential on the right shows a strong vertical and a weak lateral gradient.



Figure 5.39: Sketch of the two proposed process modifications to increase the lateral electric field inside the MALTA pixel.

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Figure 5.40: Shown are simulation results from [38]. Top: Field simulation for the n-gap modification. Bottom: Field simulation for the extended deep p-well modification. A clear increase in the lateral field strength is observed at the border between pixels (indicated by the black star) for both modifications.

In order to speed up charge collection at pixel edges and corners and thus improve the induced signal on the collection n-well and counteract charge-trapping two modifications to the pixel design as shown in figure 5.39 were studied. Either an extension of the deep p-well into the planar n-layer (left) or a gap in the planar n-layer (right) can be introduced so that additional positive space charge (after depletion) is placed between pixels. As a result, the lateral field strength increases as shown in figure 5.40.

Furthermore, transient simulations of the induced current and collected charge over time at pixel edges and corners show a significant improvement in charge collection as shown in figure 5.41. The top plots show the induced signal which is significantly higher for the modified pixel where charge drifts faster towards the collection n-well. The bottom plots show that the collected charge saturates faster as well and, in the case of irradiated silicon, at a higher level because charge trapping is suppressed by faster collection times.



Figure 5.41: Shown are simulation results from [38]. Transient simulations show a drastic improvement for the induced current (top) and collected charge (bottom) for both proposed modifications to the MALTA pixel layout before (left) and after (right) irradiation [38].



Figure 5.42: Shown is a top-down view of miniMALTA (top), the sector layout of the pixel matrix (bottom left) and chip bonded to its carrier board (bottom right).

# 5.3 TowerJazz miniMALTA

After extensive laboratory characterizations and beam tests with MALTA the key issues that limited MALTA's performance after irradiation had been identified. The miniMALTA prototype was designed to test the proposed solutions. Its pixel matrix contains several sectors which feature various combinations of original and improved sensor and front-end designs. Further, issues with the slow control which prevented the efficient configuration of MALTA and the reliable masking of pixels were also addressed. The results obtained with miniMALTA in laboratory measurements and beam tests have been published in [39], further publications are [40] and [41]. An overview of [39] based on the direct contributions from this thesis is given in this chapter.

Based on the proposed improvements, miniMALTA is segmented into 8 different sectors as shown in figure 5.42. The features of individual sectors are also listed in table 5.6. The pixel matrix is divided into two halves one of which implements the old and one

Sector	front-end design	process mod.	reset
0	enlarged M3/M6	standard	diode
1	enlarged $M3/M6$	extra deep	diode
		p-well	
2	enlarged $M3/M6$	standard	PMOS
3	enlarged $M3/M6$	n-gap	diode
4	standard	standard	diode
5	standard	extra deep	diode
		p-well	
6	standard	standard	PMOS
7	standard	n-gap	diode

Table 5.6: Given is a summary of the various pixel designs in the miniMALTA matrix. The front-end design refers to figure 5.20 and the process modification to figure 5.39. The only reset mechanism used in tests and characterization was the diode reset.

the new front-end design. Furthermore, within both halves of the chip, both suggested modifications to the doping implants and the original implants are present (from now on called 'extended p-well', 'n-gap' and 'standard modified', respectively). In addition both chip halves feature a sector with PMOS reset which was however not studied in beam tests.

# 5.3.1 Serial Readout

As shown for MALTA, miniMALTA data is also transported from the matrix to the chip periphery asynchronously. However, the miniMALTA word is structured differently due to the smaller pixel matrix as shown in table 5.7. While the bit formatting was mostly copied from MALTA the smaller matrix on miniMALTA means that some bits are not needed. As an example, only 2 out of 5 pixel group bits carry information because the double columns on miniMALTA contain only 4 pairs of groups. Similarly, the chip BCID is not used at all and the serial readout of the chip does not need the reference bit which is nevertheless part of the miniMALTA word. The entire miniMALTA word comprises 48 bits to which a 12 bit trigger counter is added by the FPGA.

The primary readout mode of miniMALTA is based on a single differential output line. Each 48 bit miniMALTA word is 8b/10b encoded into 6 blocks of 10 bit which are then sent out at 1.2 GHz. However, this readout mode was unstable and instead the slower

Table 5.7: Table of the miniMALTA word format. The least significant 48 bits are sent from the chip periphery. The 12 most significant bits are added by the readout FPGA and serve as a trigger counter which is necessary to synchronize DUT and reference data in a beam test environment.

bit range	bit	description	info
_	size		
[0:14]	15	BCID	40 MHz clock
[15:17]	3	Chip BCID	artefact of MALTA format,
			not used
[18]	1	Ref bit	artefact of MALTA format,
			not used
[19:22]	4	WinID	640 MHz clock
[23:24]	2	Group	pixel group along double
			column
[25:27]	3	Dummy group	artefact of MALTA format,
			not used
[28:43]	16	Pixel	pixel within $2 \times 8$ pixel
			group
[44]	1	Parity	even or uneven pixel group
[45:47]	3	Double column	double column along pixel
			matrix
[48:59]	12	L1ID	trigger counter for
			synchronization



Figure 5.43: Shown is a sketch of the slow readout protocol of miniMALTA<sup>10</sup>. The DATA and ACK line are driven by the 40 MHz clock. The ACK flag envelops the data on the DATA line that is sent out. By either shifting the miniMALTA word within the buffer or by buffering additional bits after the falling edge of ACK it is possible to compensate for shifts between the ACK flag and the data on the DATA line.

secondary readout mode at 40 MHz was used for all tests. In this mode two differential lines are used as shown in figure 5.43. The ACK flag is used to indicate data on the data line. Only while data is sent out ACK is pulled high.

Due to additional capacitances on the line, rising edges on the ACK line were not sufficiently stable to consistently read the enveloped data stream without dropping bits. Consequently, a shift register was implemented which continuously buffers bits from the data line. Once the falling edge of the ACK flag is detected, the data within the buffer is sent to a FIFO for further processing. By default (labeled as 'delay\_10' in figure 5.43) the most significant (i.e. the most recent) bits from the buffer are read out. In order to adjust to a shift of the ACK flag relative to the data output, a different delay can be chosen so that the block of bits, which is read from the buffer, can be shifted with respect to the falling edge of the ACK flag (see 'delay\_8' and 'delay\_12' in figure 5.43). For a delay < 10 the miniMALTA word within the buffer is shifted towards the LSB. For a delay < 10 the buffer keeps buffering up to 10 bits after the falling edge of the ACK before the MSB is read out. The core code in VHDL for this readout method can be found in the appendix, section B.

Due to a missing reset mechanism for the BCID counter, it could not be used to measure the time of arrival relative to a trigger as would be needed in a beam test setup. Consequently, the corresponding 15 bits of the miniMALTA word are not used and each miniMALTA output word is clipped short to 33 bits. A new 15 bit counter which can be reset is attached by the readout FPGA.

 $<sup>^{10}\</sup>mathrm{drawn}$  with wavedrom, https://wavedrom.com/, last accessed: 01.09.2020
fluence	0.0		$1 \times 10^{15}$		$2 \times 10^{15}$	
$1{ m MeV}~{ m n_{eq}/cm^2}$						
front-end	old	new	old	new	old	new
threshold [e]	569	292	363	217	290	161
thres. dispersion [e]	49	22	50	30	49	29

Table 5.8: Given below is a summary of the threshold and threshold dispersion at different irradiation levels for the miniMALTA sector with an improved front-end and the sector with the original front-end.

### 5.3.2 Threshold measurements

Besides the changes to the pixel implant layout as discussed in section 5.2.8 and the changes to the front-end the slow control of miniMALTA was improved as well. This was especially useful for threshold scans. The results for non-irradiated samples, samples irradiated to  $1 \times 10^{15}$  and  $2 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL are shown in figure 5.44. Threshold scans were performed per pixel as described in section 5.2.4 in a climate chamber at -20 °C. The plots show the threshold distributions (top) and corresponding noise distributions (bottom) for sector 0 (left plot, standard implants, enlarged transistors) and sector 4 (right plot, standard implants, standard transistors). When comparing at same radiation levels, a clear improvement of the threshold can be observed for the enlarged transistor front-end which is summarized in table 5.8. The significantly reduced threshold is attributed to an improved gain due to the enlarged (elongated) transistor M3 in the analogue front-end. Additionally, the threshold dispersion has decreased by roughly 50%.

In terms of noise the improved front-end design shows narrower distributions and fewer tails which is attributed to reduced RTS noise in the circuit. Nevertheless, the most probable value seems to be unaffected by the front-end and only increases after irradiation. When comparing the same pixel flavors at different irradiation levels the measured threshold decreases with increasing fluence. This somewhat counter intuitive development is attributed to a change in the sensor capacitance due to altered doping levels caused by type inversion.

While sector 4 on miniMALTA is closest to the original pixel design of MALTA with the standard front end and the standard modified doping implants it does have an even more reduced deep p-well than the medium deep p-well design of MALTA. Furthermore, while the voltage of IDB (i.e. the main DAC to control the threshold) was supplied externally on MALTA this was not the case for miniMALTA where the DACs were functioning as intended. Measurements of the DAC voltages of miniMALTA show that IDB = 100 corresponds to a voltage of roughly 1.1 V. This would correspond to a threshold of roughly



Figure 5.44: Shown is a comparison of the threshold (top) and noise (bottom) distribution at no irradiation and irradiation to  $1 \times 10^{15}$  and  $2 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL [39].

470 electrons on MALTA and a threshold of 570 electrons on miniMALTA which is a difference of roughly 20%.



Figure 5.45: The figure on top shows the beam telescope geometry which was used at the ELSA facility. The bottom plots show the achieved track residual distribution on the DUT.

### 5.3.3 Test beam measurements

Due to the long shutdown at CERN at the time, beam tests at the CERN SPS were not possible and instead conducted at the DESY facility in Hamburg and the ELSA facility in Bonn. Electron beam momenta ranged from 3 to 5 GeV/c at DESY and were roughly 3 GeV/c at ELSA. Thus a 'general broken lines' (GBL) tracking method which takes multiple scattering into account was used [19]. Based on the published results in [39] only data from test beam measurements at the ELSA facility is shown here.

The telescope used for these measurements was built with MALTA detectors as shown in figure 5.45. The initial telescope consisted of 7 planes in total with 3 planes per arm and an additional MALTA sensor close to the miniMALTA DUT to improve resolution. However, the offline data analysis showed, that the best track reconstruction is achieved by only using planes 2, REF and 3. Due to multiple scattering the data of more planes causes diminishing performance to the track resolution.

A comparison of the performance of the various sectors of miniMALTA is shown in figure 5.46. The plots show in-pixel efficiency maps of 2x2 pixels. The plots are arranged according to the sector layout on the miniMALTA pixel matrix as shown in figure 5.42. Comparing the bottom plots from left and right which are closest to the original MALTA pixel, an increase in efficiency by roughly 15% can be attributed to the improved front-end which has a higher gain, lower RTS noise and thus a lower effective threshold. As a result, signals from charge deposits between pixels do not fall below threshold as easily. While plots on the right show a decreasing efficiency towards pixel edges, this phenomenon is only slightly visible for the unmodified pixel sector on the bottom left. When comparing unmodified and modified pixel implants for the same front-end another increase in efficiency by roughly 5% is observed which indicates that charge collection has improved and the efficiency across the pixel is nearly flat. A selection of efficiency results with miniMALTA before and after irradiation to  $1 \times 10^{15}$  and  $2 \times 10^{15}$  NIEL is given in table 5.9.

The efficiency measurements with miniMALTA show that CMOS DMAPS with a small collection n-well can achieve the necessary radiation hardness to be used in an environment such as the ATLAS ITk. However, further timing studies will be necessary to show if a sufficient in-time efficiency can be reached as well.



Figure 5.46: Shown are the in-pixel efficiencies of a miniMALTA sample after irradiation to  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL. The figures are arranged with reference to the sector layout as shown in Fig. 5.42 with the PMOS reset sectors left out. The sample was kept at -20°C and a substrate voltage of -6 V.

Table 5.9: Given are selected efficiency results of the miniMALTA sectors at several irradiation levels.

Fluence	Process	Efficiency $[\%]$ for	Efficiency $[\%]$ for
$[1{\rm MeV}~n_{\rm eq}/{\rm cm}^2]$	modification	enlarged	standard
		transistors /	transistors $/$
		Threshold $[e^-]$	Threshold $[e^-]$
	n' gap	$99.6 \pm 0.1 \; / \; 200$	$99.1 \pm 0.1 \ / \ 380$
$0.0 \times 10^{15}$	extra deep p-well	$99.6 \pm 0.1 \; / \; 200$	$98.9 \pm 0.1 \; / \; 380$
	continuous n <sup>-</sup>	$99.6 \pm 0.1 \; / \; 200$	$97.9 \pm 0.1 \; / \; 380$
	n gap	$98.8 \pm 0.1 \ / \ 120$	$90.7 \pm 0.1 \; / \; 275$
$1.0 \times 10^{15}$	extra deep p-well	$99.2 \pm 0.1 \ / \ 120$	$92.5\pm0.1$ / 275
	continuous n <sup>-</sup>	$95.8 \pm 0.1 \ / \ 120$	$79.4\pm0.2$ / $275$
$2.0 \times 10^{15}$	n <sup>-</sup> gap	$92.1 \pm 0.2 \ / \ 120$	$73.1 \pm 0.3 \ / \ 230$
	extra deep p-well	$93.7 \pm 0.2 \ / \ 120$	76.4 $\pm$ 0.3 / 230
	continuous n <sup>-</sup>	$86.5 \pm 0.2 \ / \ 120$	$70.9 \pm 0.3 \; / \; 230$

#### 5.4. MALTA CZOCHRALSKI



Figure 5.47: Shown is a comparison of the cross section of the original MALTA pixel on epitaxial silicon (left) and the new MALTA pixel on Czochralski silicon (right). Due to the lower p-doping of the bulk in Czochralski silicon the depletion region can be significantly extended by increasing the substrate bias voltage.

### 5.4 MALTA Czochralski

This new prototype of the TowerJazz MALTA family was manufactured using Czochralski silicon which is not segmented into a substrate and epitaxial layer and thus allows for the depletion region to grow further into the silicon bulk at higher substrate biases. This increases the signal from deposited charge and is expected to improve the time resolution of the detector. The difference between the original MALTA and MALTA Czochralski (from now referred to as MALTA CZ) pixel cross sections is illustrated in figure 5.47. Several flavors of MALTA CZ exist which implement either no, an n-gap or extended p-well modification across the entire matrix.

### 5.4.1 Beam test data treatment

Similar to studies with miniMALTA, MALTA CZ studies were done with a telescope built from updated MALTA chips with improved slow control and powering. While the MALTA telescope achieves high data rates, good resolution and integrates very well with the DUTs it is possible for individual planes to de-synchronize. The effect of a telescope de-synchronization is a sharp drop of the average number of tracks per event as shown in figure 5.48. Re-synchronization is now more complicated because the telescope data stream must be broken up into the data streams of each individual telescope detector. The so-called 'seed-planes' of the telescope which are used for coincidence triggering give a coarse reference for a particle track. All remaining telescope and DUT data streams are



Figure 5.48: Shown is the effect of a de-synchronized telescope plane. After roughly 300000 events the average number of tracks per event drops to almost zero.

then shifted until their hit positions coincide best with this reference which is indicated by a sharp increase in events per track back to expected levels. An offline filter to remove noisy pixel hits from the data has been implemented in the exact same way as described in the previous section on MALTA 5.2.5. Again, any pixel with a hit rate 5 times higher than its neighbors is considered noisy and any track with an intercept on such a pixel is removed from the data set. A summary plot of the fraction of masked pixels for the entire MALTA CZ data set studied in this work is shown in the appendix, section C. For all runs this fraction stayed below 1% of pixels of the ROI.

### 5.4.2 Detector performance in beam tests

Beam tests with MALTA CZ were done at the DESY facility in Hamburg using a MALTA beam telescope as described in figure 5.49. Only three telescope planes were used to minimize beam scattering. One plane was mounted as close as possible to the DUT to improve resolution. While all telescope sensors were  $100 \,\mu\text{m}$  in thickness, the DUT was  $300 \,\mu\text{m}$  thick. The achieved resolution of this telescope is also shown in the same figure on the bottom. All irradiated samples were cooled to  $-20^{\circ}$ C. The test beam was a  $3 \,\text{GeV/c}$  electron beam. Due to multiple scattering on the detectors and DUTs themselves a general-broken-line (GBL) algorithm was used as provided by the proteus tool [18]. The cut on the reduced X<sup>2</sup> of the track fit was relaxed to 6.0 to allow for some margin of error due to unaccounted for material in the beam. For all MALTA CZ runs in this section the track-cluster distance cut was set to  $60 \,\mu\text{m}$ . A summary for the entire data set against



Figure 5.49: Shown is a sketch of the MALTA telescope used at the DESY facility for beam tests with MALTA CZ samples. The achieved track-cluster residuals are shown below and average to 14.7 µm and 14.5 µm in X and Y direction, respectively.



Figure 5.50: Shown is a photo of the DESY test beam setup for MALTA CZ. The beam enters from the back of the picture on the right.

these cuts is shown in the appendix, section C.

A photo of the setup is shown in figure 5.50. The entire setup was mounted on a large XY-stage to move the telescope and DUT into the beam. The DUT inside the cold box was again mounted on a second XY stage to move the DUT relative to the telescope.

The thresholds and efficiencies of several MALTA CZ samples have been measured extensively. However, at the time this thesis was written a full set of samples only existed for the n-gap modification and the results of this chapter focus on this sample set only.

Non-irradiated samples were operated at room temperature and the substrate voltage was not lowered below -12 V. However, for irradiated MALTA CZ samples the substrate bias voltage was gradually lowered until the breakdown of the pn-junction set in. Then, the bias voltage was ramped back by 5 V and a first set of data was taken. Afterwards, the threshold was lowered as much as possible while maintaining low noise levels and a second set of data was recorded.

A summary of the measured values of the threshold, equivalent-noise-charge (ENC) and efficiency are given in table 5.10. A clear rise in efficiency with stronger bias voltages is observed. It can also be seen that, as was already the case for miniMALTA, the threshold decreases with increasing radiation levels. Furthermore, a stronger bias voltage can be reached on the substrate for the highly irradiated sample (55 instead of 50 V).

Table 5.10: Given are measured values for the threshold, noise and efficiency for sector 2 of MALTA CZ with the n-gap modification either non-irradiated or irradiated to 1.0 and  $2.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL. Measurements at the final bias voltage with an improved threshold are marked with an asterisk.

$\label{eq:fluence} Fluence \\ [10^{15} \ 1  {\rm MeV} \ n_{\rm eq}/{\rm cm}^2]$	Substrate bias [V]	Sector S2 Threshold [e <sup>-</sup> ] / ENC [e <sup>-</sup> ]	Sector S2 Efficiency ±stat ±sys [%]
0.0	6.0	$375.0 \pm 3.4$ $9.4 \pm 0.29$	$98.63 \substack{0.02 & 0.18 \\ 0.02 & 0.11}$
1.0	12.0	$327.5 \pm 5.2$ $13.0 \pm 0.29$	$64.30_{0.22}^{0.22}_{0.22}^{0.44}_{0.46}$
	20.0	$328.6 \pm 5.3$ $13.3 \pm 0.29$	$78.93 \mathop{\scriptstyle 0.19}_{\scriptstyle 0.20} \mathop{\scriptstyle 0.60}_{\scriptstyle 0.62}$
	30.0	$330.6 \pm 5.2$ $12.9 \pm 0.29$	$88.89_{0.19}^{0.18}_{0.22}^{0.22}$
	40.0	$335.8 \pm 5.2$ $13.1 \pm 0.27$	$92.85_{0.120.40}^{0.120.34}$
	50.0	$338.9 \pm 5.5$ $13.5 \pm 0.30$	$94.88 \mathop{\scriptstyle 0.05}_{\scriptstyle 0.05} \mathop{\scriptstyle 0.45}_{\scriptstyle 0.44}$
	50.0*	$260.1 \pm 4.5 \\ 12.7 \pm 0.27$	$97.11 \substack{0.04 \\ 0.04 \\ 0.58} 0.58$
2.0	12.0	$271.1 \pm 4.3 \\ 13.3 \pm 0.51$	$49.66 \mathop{\scriptstyle 0.22}_{\scriptstyle 0.22} \mathop{\scriptstyle 0.45}_{\scriptstyle 0.45}$
	20.0	$268.3 \pm 4.3$ $13.4 \pm 0.43$	$64.68 \mathop{\scriptstyle 0.21}_{\scriptstyle 0.21} \mathop{\scriptstyle 0.48}_{\scriptstyle 0.21}$
	30.0	$270.3 \pm 4.7$ $13.4 \pm 0.51$	$79.37_{0.24}^{0.24}_{0.29}^{0.24}_{0.29}^{0.29}$
	40.0	$271.5 \pm 4.5$ $13.7 \pm 0.43$	$87.17_{0.15}^{0.15}_{0.15}^{0.35}_{0.36}$
	50.0	$269.0 \pm 4.2$ $14.1 \pm 0.48$	$91.19  {}^{0.11}_{0.11}  {}^{0.25}_{0.27}$
	55.0	$271.4 \pm 4.5 \\ 14.0 \pm 0.49$	$92.87_{0.13\ 0.62}^{0.13\ 0.97}$
	55.0*	$226.4 \pm 4.5$ $14.1 \pm 0.46$	$96.65 \mathop{\scriptstyle 0.05}\limits_{\scriptstyle 0.05} \mathop{\scriptstyle 0.32}\limits_{\scriptstyle 0.77}$



Figure 5.51: Shown is the efficiency (top) and cluster size (bottom) at increasing bias voltages for MALTA CZ irradiated to 1.0 and 2.0  $\times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL (from left to right).

The detector efficiency and cluster size against substrate voltage are shown in figure 5.51 for samples irradiated to 1.0 and 2.0  $\times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL. For both irradiation levels the efficiencies at the pixel center, edge and corner differ by up to 20% for voltages around -15 to -20 V but converge towards a common value once the maximum detector bias is reached and the threshold is lowered as much as possible. This shows that MALTA CZ has a flat efficiency profile across the entire pixel, even after a fluence of 2.0  $\times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL. The efficiency approaches roughly 90% for both samples before the threshold is lowered which then adds another  $\sim 5\%$ . Note that especially pixel efficiency at the corner and edge is raised. The cluster size increases significantly once the threshold is lowered and reaches similar levels of  $\sim 1.3$  for both samples. It is also interesting to note that sector 2 with the larger deep p-well is now slightly more efficient until the final bias voltage and threshold is reached.

#### 5.4. MALTA CZOCHRALSKI

The in-pixel efficiency and cluster size plots for sector S2 of an n-gap MALTA CZ detector irradiated to 1.0 and  $2.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL are shown in figure 5.52 and 5.53. The substrate bias at the lower irradiation level was -20 V (left) and -50 V (middle, right) and at the higher irradiation level -20 V (left) and -55 V (middle, right). For both figures the plots on the right show results for a lowered threshold.

For a low bias voltage of -20 V both samples show the familiar efficiency profiles with a lower detection efficiency at pixel borders. However, the profiles of the highly irradiated sample are much more pronounced. At the highest voltage and a low threshold both samples show flat efficiency profiles above 95%. The development of the cluster size profiles looks virtually the same.

Overall, the test beam performance of MALTA CZ shows a tremendous improvement compared to MALTA. Even without the improved front-end efficiencies close to those of miniMALTA are achieved. For sector S2 of the sample irradiated to  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL the ATLAS ITk requirement of an efficiency above 97% is met and the same sector misses this target by less than 0.5% after irradiation to twice this fluence. The cluster size, even after a high irradiation, shows values well above 1.0 across the entire pixel.



Figure 5.52: Shown are efficiency (top) and cluster size (bottom) for a MALTA CZ sample irradiated to  $1.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL at a substrate bias voltage of -20 V (left), -50 V (middle) and -50 V with lowered threshold (right).



Figure 5.53: Shown are efficiency (top) and cluster size (bottom) for a MALTA CZ sample irradiated to  $2.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL at a substrate bias voltage of -20 V (left), -50 V (middle) and -55 V with lowered threshold (right).

#### 5.4. MALTA CZOCHRALSKI



Figure 5.54: Shown are in-pixel timing profiles for MALTA CZ. The irradiation levels are 0.0, 1.0 and  $2.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL, the substrate biases are -6, -50 and -55 V and the thresholds are 375, 260 and 226 e<sup>-</sup> from left to right.

### 5.4.3 Timing profiles in beam tests

The same timing profiles that were already shown for MALTA in section 5.2.7 are presented here for MALTA CZ in figure 5.54 for sector S2. The irradiation levels are 0.0, 1.0 and  $2.0 \times 10^{15}$  1 MeV  $n_{eq}/cm^2$  NIEL, the substrate biases are -6, -50 and -55 V and the thresholds are 375, 260 and 226 e<sup>-</sup> from left to right.

While statistical fluctuations are larger and the telescope resolution is reduced due to the electron test beam the profiles still clearly show a pattern similar to that of MALTA. However, based on the range of the z-axis a clear improvement compared to MALTA can be seen. MALTA timing profiles show a range of 40 ns before irradiation and 18 ns after. MALTA CZ profiles reach ranges of roughly 4 ns at the same and higher irradiation levels which indicates a dramatically improved timing performance. This result is attributed to the increased signal sizes due to a wider depletion region in MALTA CZ and the improved charge collection at pixel borders. TU **Bibliothek**, Die approbierte gedruckte Originalversion dieser Dissertation ist an der TU Wien Bibliothek verfügbar. WEN Vourknowledge hub The approved original version of this doctoral thesis is available in print at TU Wien Bibliothek.

# Chapter 6

# Outlook

After 3 years of ongoing detector development significant progress has been made towards a CMOS DMAPS design that fulfills the requirements of the ATLAS ITk and other future trackers like it. This thesis encompasses this development from the very beginnings of a simple analogue chip, the Investigator, all the way to a full-sized digital chip, MALTA CZ, which has a working slow control, shows excellent radiation hardness and promises to show excellent performance in dedicated timing studies that are soon to follow. The resolution of several issues with the basic functioning of the MALTA detector has now paved the way for more advanced studies and several new projects are already under way.

# 6.1 Combining improvements to the MALTA front-end and sensor

Based off the initial design of the MALTA front-end significant improvements could already be achieved by re-designing several transistors and thus significantly reducing threshold dispersion and RTS noise. The n-gap and extended p-well modifications to the planar n-layer in the sensor have significantly improved charge collection at pixel borders and contributed to homogeneous efficiency profiles on miniMALTA and MALTA CZ. So far both, the improvements to the front-end and the modifications to the planar n-layer, have not been combined in a new full-sized MALTA prototype. Doing so is an obvious next step that will likely produce a chip that is capable of maintaining full efficiency even up to fluences of  $2.0 \times 10^{15}$  1 MeV n<sub>eq</sub>/cm<sup>2</sup> NIEL.

### 6.2 High precision timing studies

There is already an ongoing effort to implement precise timing for the MALTA test beam setup and laboratory measurements. The picoTDC<sup>1</sup> developed at CERN allows extremely precise measurements of the time-of-arrival of the MALTA reference bit to study the timing precision of the detector. A test beam campaign at the MedAustron facility in Vienna, which the author of this work helped to organize and conduct, has already produced first results. The coincidence time spectrum that is shown in figure 6.1 was obtained by recording the time-to-trigger of two consecutive MALTA detectors in a 142 MeV proton beam using picoTDC for timing. The large energy deposit of this comparatively low energy beam drastically reduces the time walk and allows MALTA to achieve a very high timing precision. Nevertheless, this measurement required significant data treatment where only events with single hits on either detector are accepted. Furthermore, the stability and reliability of the picoTDC readout for MALTA must be further improved.



Figure 6.1: Shown is the coincidence time spectrum of the arrival time of the MALTA reference bit from two consecutive detectors in a 142 MeV proton beam.

<sup>&</sup>lt;sup>1</sup>picoTDC: Pico-second TDC for HEP, https://indico.cern.ch/event/755407/contributions/3130541/attachments/1738' last accessed: 01.06.2020

### 6.3 Module development

There are still features of the MALTA detector which have been as yet barely studied. Among them is the infrastructure at the chip periphery which allows direct chip-to-chip powering and communication. A first module prototype has been constructed by the author of [42]. A source scan showing the successful readout of the module is shown in figure 6.2 where an <sup>55</sup>Fe source was placed between two neighboring MALTA detectors. These detectors were operated in a master-slave configuration where data from the slave is routed through the master to the readout. A new carrier board that supports a MALTA module consisting of 4 detectors has already been developed for further studies.



Figure 6.2: Shown is an  ${}^{55}$ Fe source scan recorded by a pair of MALTA detectors in a master-slave configuration. The figure was kindly provided by the author of [42].

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### Chapter 7

### Summary

With the construction of the HL-LHC a new generation of high energy physics experiments begins and brings with it unprecedented requirements for pixel detectors in terms of radiation hardness, data rate capabilities, resolution, material budget and power consumption. Furthermore, the requirements for trackers steadily increase as well. The ATLAS ID was initially installed with 3 layers of pixels and later upgraded with a 4th layer. The pixel sub-detector of the new ATLAS ITk will contain 5 layers and increase its area 7-fold. The ever increasing size of pixel trackers demands the development of a pixel detector that can be produced and paid for in large quantities. Monolithic pixel detectors, produced by using industrial CMOS processes, have been studied and developed intensively in recent years because they have the potential to meet all these requirements. The results presented in this work show the ongoing effort and success to develop such a detector.

In collaboration with the TowerJazz foundry and their 180 nm process a first analogue prototype, the Investigator, was developed to study new monolithic pixel designs. This prototype features in total 134 different sub-matrices, each with a different pixel design in terms of pixel pitch, spacing and size of the collection diode. Three sub-matrices were selected for detailed study in this work. The results showed that charge sharing is improved by small pixel pitches and the sensor gain greatly depends on the line routing of the collection diode to the input transistor of the analogue front-end which in turn is dictated by the spacing. Furthermore, there were first indications that, while a small spacing, i.e. short line routing, has beneficial effects on the sensor gain, a deep p-well that extends across most of the pixel weakens the lateral electric field in the sensor which slows down charge collection and severely reduces charge collection efficiency after irradiation. The results obtained with the Investigator informed the design of the pixel layout that was eventually chosen for a full-sized digital chip, MALTA. This pixel detector is roughly  $2\times 2 \text{ cm}^2$  large, features a  $512\times512$  pixel matrix and a symmetric  $36.4 \,\mu\text{m}$  pixel pitch. The

pixel houses a compact analogue front-end for amplification and discrimination and the digital hit signals are read out using a novel asynchronous readout architecture which reduces power consumption on the pixel matrix and increases the hit rate capability. Laboratory characterizations as presented in [15] and [42] showed elevated levels of RTS noise in the analogue front-end and an increased threshold dispersion. The beam tests presented in this work showed a diminishing detection efficiency at pixel borders and a simultaneous increase in time-walk in the same areas of the pixel. A weak lateral field in the sensor was confirmed as the cause for diminished detector performance in the following TCAD simulations.

The results obtained with MALTA led to the development of a new prototype with a small pixel matrix, called miniMALTA, which implemented a re-design of the analogue front-end to reduce threshold dispersion and RTS noise and two different modifications to the planar n-layer in the sensor bulk to increase the lateral electric field. These improvements were shown to be effective based on the test beam results published in [39] and presented in this work and proved that the MALTA design is capable of meeting ITk requirements in terms of radiation hardness and detection efficiency.

The latest iteration of the MALTA protoype family, MALTA CZ, was produced on Czochralski silicon. While MALTA was produced on epitaxial silicon which limited the depth of the depleted sensitive volume to  $25-30\,\mu\text{m}$ , the continuous low p-doped bulk of MALTA CZ allows to extend the depletion region further by increasing the substrate bias. The beam test results presented in this work show that MALTA CZ can be operated at substrate biases of up to  $-55\,\text{V}$  and can reach detection efficiencies close to those of miniMALTA even though it does not feature the already mentioned improvements to the front-end. Furthermore, timing profiles indicate a significant reduction in time-walk across the entire pixel which promises to raise the in-time efficiency of the detector to the levels required by the ITk.

The results presented in this work show that monolithic silicon pixel detectors offer a promising option for future high energy physics experiments. While significant progress towards a fully functioning detector has been made there is still a considerable amount of further research and development ahead and this field of study promises to remain just as exciting in the future as it was in the years before.

# Appendix A

# **Definitions and symbols**

Table A.1: Physical symbols for section 2.

Symbol	Definition
$\gamma$	relativistic gamma factor
$n_b$	number of bunches per beam
N	bunch population (protons per bunch)
$f_{rev}$	revolution frequency of the beam
$\beta *$	beam beta function (focal length)
$\epsilon_n$	transverse normalized emittance
R	luminosity geometrical reduction factor
$ heta_c$	full crossing angle between the colliding
	beams
σ	longitudinal RMS size
$\sigma_z$	transverse RMS size

Symbol	Definition
$\left\langle -\frac{dE}{dx}\right\rangle$	mean rate of energy loss
$m_e$	electron mass
$\epsilon_0$	vacuum permittivity
$r_e$	classical electron radius $e^2/4\pi\epsilon_0 m_e c^2$
$N_A$	Avogadro's Number
K	$4\pi N_A r_e^2 m_e c^2$
с	speed of light
z	charge number of incident particle
Z	atomic number of absorber
A	atomic mass of absorber
$\beta$	fraction of the speed of light $v/c$
$\gamma$	Lorentz factor $1/\sqrt{1-v^2/c^2}$
$W_{max}$	maximum energy transfer in a single
	collision
$I^2$	mean excitation energy
$\delta(eta\gamma)$	density effect correction for stopping
	power at high energies
$b_{max}$	maximum impact parameter
C/Z	shell correction for stopping power at
	low energies

Table A.2: Physical symbols for section 3.

Symbol	Definition
$\mu_n, \mu_p$	mobility of electrons (n) and holes (p)
$\sigma$	conductivity
$k_B$	Boltzmann Constant
T	absolute Temperature
n	density of negative charge carriers
p	density of positive charge carriers
$n_i$	intrinsic density of charge carriers (pos.
	or neg.)
$E_i$	intrinsic Fermi level
$E_{Fn}, E_{Fp}$	quasi-Fermi level in at n-doped and
	p-doped side of biased pn-junction
$\epsilon_s$	permittivity of a semiconductor s
$W_{Dn}, W_{Dp}$	width of the depletion region at
	the n-doped and p-doped side of a
	pn-junction
$\Psi_{bi}$	built-in potential of a pn-junction
$N_D, N_A$	density of donor and acceptor
	impurities
$D_p, D_n$	diffusion coefficient in p-doped and
	n-doped semiconductors
$L_p, L_n$	diffusion length in p-doped and
	n-doped semiconductors
$C_D$	detector input capacitance
au	filter time of the detector circuit
$a_{shot}$	shot-noise contribution
$a_{1/f}$	1/f-noise contribution
$a_{therm}$	thermal noise contribution
$g_m$	transistor transconductance $\frac{dV_{GS}}{I_D}$
$K_f$	technology dependent constant for
	1/f-noise
W,L	MOSFET gate width and length
$C'_{ox}$	oxide capacitance per unit area in a
	MOSFET
f	frequency

Table A.3: Physical symbols for section 3.1.

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# Appendix B

# Code

Listing B.1: Shown is the main method to correct for the changing position of the Investigator DUT with respect to the telescope. The ROOT histograms to calculate mean and standard deviation of the median distributions are hX and hY. The random number generator rGen is created locally. The sampled positions and position errors of matched tracks — xPos, yPos, xPosError, yPosError — are vectors of at least 100 double format numbers and represent the current slice of data that is being corrected. The code calculates \_nIter (default: 10000) median values from random subsets of the matched track positions of size \_sampleSize (default: 50). Track positions for samples are smeared by sampling from a Gaussian distribution with the mean and sigma given by the track position and its error (see lines 12 and 13) to take into account the finite track resolution of the telescope. The histograms hX and hY finally contain \_nIter median values and a mean correction and the corresponding error that is introduced can be accessed in lines 29-32.

```
void ShiftCompensator :: CalculateShift(
1
     TH1D *hX,
2
     TH1D *hY,
3
     std::vector<Double_t> xPos,
4
     std::vector<Double_t> yPos,
     std::vector<Double_t> xPosError,
6
     std::vector<Double_t> yPosError,
7
     Double_t &xCorr,
8
     Double_t &yCorr,
9
    Double_t &xCorrError,
    Double_t &yCorrError
11
  ){
     TRandom3* rGen = new TRandom3();
13
```

```
for(Int_t i = 0; i < _nIter; ++i){</pre>
14
       std::vector<Double_t> sampleX,sampleY;
       UInt_t len = std::min(
         std::min(xPos.size(),yPos.size()),
         std::min(yPosError.size(),yPosError.size())
18
       );
19
       for(Int_t j = 0; j < _sampleSize; ++j){</pre>
20
         Int_t rnd = rGen->Rndm()*(len-1);
         Double_t x = rGen->Gaus(xPos[rnd],xPosError[rnd]);
22
         Double_t y = rGen->Gaus(yPos[rnd],yPosError[rnd]);
23
         sampleX.push_back(x); sampleY.push_back(y);
24
       }
25
       std::sort(sampleX.begin(),sampleX.end());
26
       std::sort(sampleY.begin(),sampleY.end());
27
       Double_t medianX, medianY;
28
       if(_sampleSize%2 != 0){
29
         medianX = sampleX[_sampleSize/2];
30
         medianY = sampleY[_sampleSize/2];
       } else {
32
         medianX = (sampleX[_sampleSize/2-1]+sampleX[_sampleSize/2])/2.0;
33
         medianY = (sampleY[_sampleSize/2-1]+sampleY[_sampleSize/2])/2.0;
34
       }
35
      hX->Fill(medianX); hY->Fill(medianY);
36
     }
37
     delete rGen;
38
     xCorr = hX->GetMean();
39
     xCorrStdDev = hX->GetStdDev();
40
     yCorr = hY->GetMean();
41
     yCorrStdDev = hY->GetStdDev();
42
  }
43
```

Listing B.2: Shown is the core code for the miniMALTA readout firmware. The serial output of the chip is continuously buffered. If the ACK flag is raised the buffer is read out based on the configured delay.

```
library IEEE;
1
  use IEEE.STD_LOGIC_1164.ALL;
2
  use IEEE.NUMERIC_STD.ALL;
3
  library UNISIM;
4
```

use UNISIM.VComponents.all;

17

21

```
entity slowPackager is
7
   port(
8
       IN_SPC_CLK
                                                          := '0';
                          in std_logic
                       :
9
       IN_SPC_RESET
                          in std_logic
                                                          := '0';
                       :
       IN_SPC_ACK
                          in std_logic
                                                          := '0';
                       :
11
                          in std_logic
       IN_SPC_DATA
                                                          := '0':
                       :
       IN_SPC_SHIFT
                          in std_logic_vector(3 downto 0) := (others => '0');
                       :
       OUT_SPC_NEW_DATA : out std_logic
                                                          := '0':
14
                       : out std_logic_vector(47 downto 0) := (others => '0');
       OUT_SPC_DATA
        OUT_SPC_DATA : out std_logic_vector(33 downto 0) := (others => '0');
16
       OUT_SPC_ERROR
                       : out std_logic_vector(1 downto 0) := (others => '0')
17
   );
18
   end slowPackager;
19
20
   architecture Behavioral of slowPackager is
21
22
       -- I/O signals
23
       signal s_in_clk
                                                                 '0';
                            : std_logic
24
                                                               · =
       signal s_in_reset
                            : std_logic
                                                               :=
                                                                 '0';
25
       signal s_in_ack
                            : std_logic
                                                                 '0';
                                                               :=
26
       signal s_in_data
                            : std_logic
                                                               :=
                                                                 '0';
27
       signal s_in_shift
                            : std_logic_vector( 3 downto 0) := (others => '0');
28
       signal s_out_new_data : std_logic
                                                               :=
                                                                 '0':
29
       signal s_out_data
                            : std_logic_vector(47 downto 0) := (others => '0');
30
        signal s_out_data : std_logic_vector(33 downto 0) := (others => '0');
31
       signal s_out_error : std_logic_vector( 1 downto 0) := (others => '0');
32
33
       -- internal signals
34
       signal i_shift
                                : integer range 0 to 15
                                                               := 10;
35
       signal i_delay
                                : integer range 0 to 5
                                                               := 0;
36
       signal i_ack_timer
                                : integer range 0 to 34
                                                               := 0;
37
       signal s_readout_buffer : std_logic_vector(57 downto 0) := (others => '0');
38
        signal s_readout_buffer : std_logic_vector(43 downto 0) := (others => '0');
39
       signal s_last_ack
                                : std_logic
                                                                 '0';
                                                               :=
40
       signal s_read_word
                                : std_logic
                                                               := '0';
41
42
       constant c_nopixels
                                : std_logic_vector(15 downto 0) := "0000000000000000";
43
                                : std_logic_vector(2 downto 0) := "111";
       constant c_dummygroup
44
       constant c_refbit
                                : std_logic
                                                                 '1';
                                                               :=
45
```

```
APPENDIX B. CODE
```

```
46
   begin
47
48
       -- connect input
49
                                  <= IN_SPC_CLK;
       s_in_clk
50
       s_in_reset
                                  <= IN_SPC_RESET;
       s_in_ack
                                  <= IN_SPC_ACK;
                                  <= IN_SPC_DATA;
       s_in_data
       s_in_shift
                                  <= IN_SPC_SHIFT;
54
         i_shift
                                    <= to_integer(unsigned(s_in_shift));
56
       packageData: process(s_in_clk) is
57
           begin
58
           if rising_edge(s_in_clk) then
59
                 if s_out_reset_ack = '1' then
60
                     s_out_reset_ack
                                                    <= '0';
61
                 end if;
62
               if s_in_reset = '1' then
63
                                                  <= '0';
                  s_read_word
64
                   i_delay
                                                  <= 0;
65
               else
66
                   s_readout_buffer(57)
                                                  <= s_in_data;
67
                   s_readout_buffer(56 downto 0) <= s_readout_buffer(57 downto 1);</pre>
68
                  s_last_ack
                                                  <= s_in_ack;
69
                   if (s_last_ack = '1' and s_in_ack = '0') or s_read_word = '1' then
70
                      -- delay = [0:9] => read from buffer 1-10 bits shifted backwards (back in
71
                       -- delay = 10 => read directly from buffer
72
                      -- delay = [11:15] => wait 1-5 clock cycles, then read out directly from h
73
                      if 10-i_shift+i_delay >= 0 then
74
                                                  <= s_readout_buffer(47+i_shift-i_delay downto 0+;
                          s_out_data
75
                          s_out_new_data
                                                  <= '1';
76
                                                  <= '0';
                          s_read_word
77
                                                  <= 0;
                          i_delay
78
                      elsif i_delay < 5 then
79
                          if s_read_word = '0' then
80
                              s_read_word
                                                  <= '1';
81
                          end if;
82
                                                  <= i_delay + 1;
                          i_delay
83
                      end if;
84
                   end if;
85
```

```
end if;
86
               if s_out_new_data = '1' then
87
                                                   <= '0';
                   s_out_new_data
88
                                                   <= (others => '1');
                   s_out_data
89
               end if;
90
           end if;
91
           end process packageData;
92
93
           OUT_SPC_NEW_DATA
                                                   <= s_out_new_data;
94
           OUT_SPC_DATA
                                                   <= s_out_data;
95
           OUT_SPC_ERROR
                                                   <= s_out_error;
96
   end Behavioral;
97
```

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# Appendix C

# Summary plots



Figure C.1: Shown on top are the median and 95% quantile of all  $\chi^2$  distributions of the TowerJazz Investigator samples analyzed in the course of this work. Shown on the bottom are the track-cluster residual standard deviations in both directions.



 $\chi^2$  for analyzed MALTA samples

Figure C.2: Shown are the median and 95% quantile of all reduced  $\chi^2$  distributions of the samples analyzed in the course of this work. The top plots shows results for MALTA and the bottom plot for MALTA CZ. The calculation of the degrees of freedom for the reduced  $\chi^2$  distributions of MALTA CZ samples was not correct and the resulting values are much larger than expected. However, the plot shows that the track alignment performed consistently for nearly all samples.



Track-cluster residual standard deviations, MALTA

Figure C.3: Shown are the track-cluster residual standard deviations of the samples analyzed in the course of this work. The top plots shows results for MALTA and the bottom plot for MALTA CZ.



Fraction of masked pixels in ROI per sample, MALTA

Figure C.4: Shown is the fraction of masked pixels in the ROI for each sample studied for this work for MALTA (top) and MALTA CZ.
# Appendix D

# Abbreviations

Table D.1: Given is a list of the abbreviations used in this work.

AC	Alternating State
ALICE	A Large Ion Collider Experiment
ALPIDE	ALice PIxel DEtector
ASIC	Application Specific Integrated Circuit
ATLAS	A large ToroidaL AparatuS (deprecated)
CERN	Conseil Européen pour la Recherche Nucléaire
CMOS	Complementary Metal-Oxide-Silicon
DAC	Digital Analog Converter
DC	Direct Current
DESY	Deutsches Elektronen SYnchrotron
DUT	Device/Detector Under Test
ENC	Equivalent Noise Charge
FET	Field Effect Transistor
HL-LHC	High Luminosity LHC
ITk	(ATLAS) Inner TracKer
ITS	(ALICE) Inner Tracking System
LHC	Large Hadron Collider
LHCb	LHC beauty
LINAC	LINear ACcellerator
MALTA	Monolithic From ALice To Atlas
MALTA CZ	MALTA Czochralski
MAPS	Monolithic Active Pixel Sensor
MOSFET	Metal-Oxide-Silicon Field Effect Transistor
MPV	Most Probable Value
NMOS	N-type Metal-Oxide-Semiconductor
PMOS	P-type Metal-Oxide-Semiconductor
PSB	Proton Synchrotron Booster
PS	Proton Synchrotron
ROI	Region Of Interest
RTS	Random Telegraph Signal
SCT	SemiConductor Tracker
SEU	Single Event Upset
SNR	Signal to Noise Ratio
SOI	Silicon On Insulator
SPS	Super Proton Synchrotron
TCAD	Technology Computer Aided Design
TRT	Transition Radiation Tracker

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Along the way Lingxin, Patrick, Sascha and Florian also joined the office and have been amazing colleagues. Lingxin's puns were a horrible but at the same time a welcome distraction when I needed it. Patrick was always motivated to work on new MALTA test setups with me and always lent a helping hand. I may also have had some of the most meandering discussions with him over a great number of coffees together. Sascha, whose progress in his PhD was closest to my own, could relate best to any problems I might encounter during my thesis work. Florian has admittedly made me feel old but makes up for it many times over by his great work ethic and relentless cheerfulness.

One of the greatest enjoyments during my stay at CERN was training at the CERN powerlifting club where I met many amazing people. Among them were Joshuha and Haydn who introduced me to the world of rugby and a whole circle of new friends from all over the planet that let me make connections beyond the CERN bubble and escape my work for the occasional pint or two (or 10) in Geneva. Together with other friends from Austria — Emanuel, Jan, Lili, Sebastian and many others — and my heroic companions through many pen&paper adventures — Patrick (the most amazing Dungeon Master), Alexander, Michi and Markus — these circles of friends have made my time at CERN so enjoyable. I will also surely never forget the time I spent with many of these awesome people at the sauna in Bains de Paquis and the truly immense amounts of cheese we consumed there (I might still be digesting some of it).

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December 2016	Master of Science in TECHNICAL PHYSICS, Vienna University of Technology Monte Carlo Simulation of a new ultra-fast Gamma Detector Design Supervisors: Prof. Lembit SIHVER, Prof. Dennis SCHAART, Dr. Albert HIRTL, Dr. Stefan E.K. BRUNNER
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March 2015	Project Work at the INSTITUTE OF SOLID STATE PHYSICS Vienna University of Technology, Vienna, Austria Operating various Gauges with a Raspberry Pi Supervisor: Prof. Herbert Müller
Summer 2013	Summer Intern at SML, Lenzing, Austria Worked as an assistant in the R&D department. Tasks included calculations on transverse beams, patent research and lab work. Lab work included several tests to measure shrinkage, tensile strength and related properties of various kinds of extruded films and sheets.
Summer 2011	Summer Intern at SML, Lenzing, Austria Worked as an assistant to the storehouse management using SAP for chaotic warehousing.

## Selection of Publications

Title

DOI Lead Author Corresponding Author Published Radiation hard monolithic CMOS sensors with small electrode size for the ATLAS experiment in the HL-LHC 10.37392/RapProc.2019.22 Asensi Tortajada I. Dachs F. January, 2020

TITLE	Mini-MALTA: Radiation hard pixel designs for
	small-electrode monolithic CMOS sensors for the High
	Luminosity LHC
DOI	10.1088/1748-0221/15/02/P02005
LEAD AUTHOR	Dyndal M.
Corresponding	Pernegger H.
Author	
Published	21st April, 2019
	Transition rediction managements with a Si and a Cala
1 IILE	Transition radiation measurements with a SI and a GaAs
DOI	pixel sensor on a Timepix3 cnip
DOI	10.1016/j.nima.2019.03.092
LEAD AND CORR.	Dachs F.
Author	
Published	1st April, 2020
TITLE	Update on the TowerJazz CMOS DMAPS development for
	the ATLAS ITk
DOI	10.22323/1.340.0802
LEAD AND CORR.	Dachs F.
Author	
Published	2nd August, 2019

## Presentations and Talks

September 16th 2019	RAP Conference 2019
ACCESS	see publications section
	Oral
	Dachs F., et al.
	Radiation hard monolithic CMOS sensors with small electrode size for
	the ATLAS experiment in the HL-LHC

April 19th 2019	15th Vienna Conference on Instrumentation
ACCESS	see publications section
	Poster
	Dachs F., et al.
	Comparison of transition radiation measurements with a Si and GaAs
	pixel sensor on a TimePix3 chip
November 2nd 2018	Seminar Talk at the University of Lancaster
Access	invited talk
	Oral
	Dachs F., et al.
	Monolithic CMOS Pixel Detector Development for the ATLAS
	Upgrade
Luxue Cons 0010	Laterational Conference III de Engeneration (ICIIED)
JULY 6TH 2018	International Conference on High Energy Physics (ICHEP)
	2018
ACCESS	see publications section
	Dachs F., et al.
	Update on the TowerJazz CMOS DMAPS development for the ATLAS
	$\mid ITk$
JANUARY 17TH 2018	6th Beam Telescopes and Test Beams Workshop
Access	Workshop Homepage on Indico
1100E55	Oral
	Dachs F et al
	Test heam results with Depleted Monolithic Active Pirel
	Sensors(Tower Jazz Investigator chin) at the SPS at CERN
September 27th 2016	Austrian Physical Society, Annual Meeting
Access	APS Conference Book 2016, page 56
	Oral
	Dachs F., Sihver, L., Hirtl, A., Schaart, D.R., Brunner, S.E.K.
	Simulation of an ultra-fast Gamma Detector with GEANT4

#### Languages

GERMAN:	Mothertongue
ENGLISH:	Fluent
FRENCH:	Basic Knowledge

#### IT and Programming Skills

Basic Knowledge:	C, Python, Mathematica, LabVIEW, Linux, LATEX, GEANT4,
	VHDL
Advanced Knowledge:	C++, ROOT

#### Other Interests and Activities

MILITARY

Sports

Y	Extended 1-year training for ongoing Reserve Officers in the Austrian
	Army.
	Finished as group leader for heavy mortar units with the current
	(intermediary) rank of Sergeant.
	Promotion to Lieutenant upon conclusion of several subsequent
	courses.
	Mandatory training exercises every TWO years for 1 week.
	This activity was suspended during my PhD and will most likely stay
	suspended during any further contracts at CERN or abroad. I will
	participate in any of these activities as part of my authorized annual
	leave if necessary.
	Competitive rower on national and international level (2001 - 2005)
	Powerlifting, recreational (2005 - ongoing)