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Wafer-Scale Fabrication and Characterization of Monolithic Al-Ge Heterostructures

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durch

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Abstract

Germanium (Ge) with its high carrier mobility and CMOS compatibility offers great potential for performance improvements of integrated circuits (ICs) beyond continuous miniaturization. Strong spin-orbit coupling and quantum confinement effects make Ge particularly interesting for the exploration of quantum effects. Aluminum-Germanium (Al-Ge) heterostructures based on vapor-liquid-solid (VLS) grown nanowires (NWs) have provided excellent results in quantum ballistic, photonic and plasmonic experiments over the last years. This may lead to the development of a broad spectrum of novel devices. However, integration of VLS grown NWs in a large scale proves to be difficult.

In this thesis an approach for a wafer-scaled fabrication of monolithic Al-Ge-Al heterostructures is presented. Ge structures are patterned on Germanium-on-insulator (GeOI) substrates using lithographic techniques and reactive ion etching. Al-Ge heterostructure formation is achieved by a thermally induced exchange reaction of predefined Ge structures and Al contact pads. Ultra-short Ge channels can be formed between self-aligned Al contacts beyond lithographic limitations. This top-down fabrication technique allows the well ordered integration of large arrays of nanoscaled devices with precisely defined dimensions.

Crystallographic analyses reveal high purity and crystallinity of the Al-Ge heterostructures with almost atomically sharp interfaces. Studies of structures with different cross sections and various geometries show that the thermal Al-Ge exchange process is neither limited to geometric constraints nor to certain orientations. The conductivity of the annealed heterostructures is significantly increased due to improved contact properties of the abrupt metal semiconductor junction. Integration of such heterostructures in field effect transistors (FETs) demonstrates modulation capabilities of the drain current over several orders of magnitude. Repetitive annealing cycles enable the fabrication of ultrascaled devices with Ge channel lengths below the mean free path enabling ballistic transport in top-down fabricated Al-Ge-Al heterostructures. Further, selective chemical etching is used to further reduce the cross-section of the Ge segments as well as short Ge channels within suspended Al nanobeams are demonstrated.

Kurzfassung

Germanium (Ge) bietet mit seiner hohen Ladungsträgerbeweglichkeit und CMOS-Kompatibilität großes Potenzial für die Leistungssteigerung von integrierten Schaltungen (ICs). Starke Spin-Orbit Kopplung und Quanten-Confinement machen Ge besonders für die Erforschung von Quanteneffekten attraktiv. Aluminium-Germanium (Al-Ge) Heterostrukturen auf Basis von vapor-liquid-solid (VLS) gewachsenen Nanodrähten haben in den letzten Jahren hervorragende Ergebnisse in quantenballistischen, photonischen und plasmonischen Experimenten geliefert. Das kann zur Entwicklung eines breiten Spektrums von neuartigen Bauelementen führen. Allerdings erweist sich die Integration von gewachsenen Nanodrähten in großem Maßstab als schwierig.

In dieser Diplomarbeit wird eine Methode zur Herstellung von monolithischen Al-Ge-Al Heterostrukturen auf Waferebene vorgestellt. Ge-Strukturen werden auf Germanium-on-Insulator (GeOI) Substraten mittels lithographischer Techniken und reaktivem Ionenätzen definiert. Die Bildung von Al-Ge Heterostrukturen wird durch eine thermisch induzierte Austauschreaktion von vordefinierten Ge-Strukturen und Al-Kontaktpads erreicht. Ultrakurze Ge-Kanäle zwischen selbstauserichteten Al-Kontakten können so jenseits lithographischer Grenzen hergestellt werden. Durch den Top-Down-Fertigungsprozess wird eine geordnete Integration einer großer Anzahl von nanoskalierten Bauelementen mit präzise definierbaren Abmessungen ermöglicht.

Kristallographische Analysen zeigen die hohe Reinheit und gute kristalline Beschaffenheit der Al-Ge Heterostrukturen mit nahezu atomar scharfen Grenzflächen. Untersuchungen von Strukturen mit unterschiedlichen Querschnitten und Geometrien zeigen, dass der thermische Al-Ge Austauschprozess nicht auf bestimmte Geometrien oder Kristallorientierungen beschränkt ist. Die Leitfähigkeit der ausgetauschten Heterostrukturen ist aufgrund der verbesserten Kontakteigenschaften des abrupten Metall-Halbleiter Übergangs deutlich erhöht. Die Integration dieser Heterostrukturen in Feldeffekttransistoren (FETs) zeigt, dass der Drainstrom über mehrere Größenordnungen moduliert werden kann. Wiederholtes thermisches Annealen ermöglicht die Herstellung von Bauelementen mit ultraskalieren Ge-Kanallängen, worin ballistischen Ladungsträgertransport beobachtet werden kann. Des Weiteren wird selektives chemisches Ätzen eingesetzt, um den Querschnitt der Ge-Segmente weiter zu reduzieren, sowie kurze Ge-Segmente innerhalb freistehender Al-Nanobalken gezeigt.

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Chapter 1

Introduction

Since the introduction of the first semiconductor transistor in 1947 [1] and the first integrated circuit about ten years later [2], both based on germanium (Ge), the components of integrated circuits have been continuously scaled down to satisfy the constant quest for performance improvements and cost reductions. Following Moore's law [3] the number of components per integrated circuit has doubled every 18 to 24 months over the last decades. Silicon (Si), the second most abundant element in the earth's crust [4], has established itself as the most important material in the semiconductor industry. Its availability and good electrical and technological properties enable the cost-efficient production of electronic devices. However, miniaturization in the Si-based complementary metal-oxide-semiconductor (CMOS) process with current minimum features sizes below 10 nm is already approaching physical limits due to increasing short-channel effects [5]. Therefore, the focus of research has shifted towards new device architectures, materials and technologies [6].

Ge with its high carrier mobilities is a promising candidate for increasing switching speed and drive currents of electrical devices. However, the absence of a high-quality oxide for the use as a gate oxide in field-effect transistors (FETs) or surface passivation has long been a major technical issue. With the development of high- κ dielectrics on Ge it is again gaining more attention for the use as alternative FET channel material [7, 8]. The introduction of high quality Germanium-on-insulator (GeOI) has also been an important step towards novel high performance Ge-based devices [9, 10].

Further, Ge offers inherently strong spin-orbit coupling and the ability to host superconducting pairing correlations, revealing high potential for encoding, processing, or transmitting quantum information [11]. In a hybrid superconductor-semiconductor device, such as a Josephson field-effect transistor, it could be integrated into a gate-tunable superconducting qubit, often referred to as a gatemon [11, 12].

Moreover, with only a small difference between indirect and direct bandgap energy, Ge can be transformed into a direct bandgap semiconductor by applying e.g. high tensile strain. This enables the integration of a direct group IV semiconductor on a Si platform [13, 14]. The deployment of low-dimensional structures such as nanowires (NWs) synthesized from various semiconductor materials, which achieve remarkable electrical, optical and mechanical properties, also promises a wide application potential in nanoscaled electronics [15, 16] and photonics [17]. Si and Ge NWs thereby offer full CMOS compatibility with excellent gate electronics, especially in gate-all-around geometries.

A main issue of the integration of nanostructures is the fabrication of reliable electrical contacts. High contact resistances or strongly varying properties, depending on the doping and employed metal, often cause difficulties. Thermal diffusion processes of metals into Ge structures are often used to form intermetallic compounds in order to improve the contact quality of the metal semiconductor junction [18–20]. In the thermal diffusion of Al into Ge NW structures, no intermetallic compounds are formed. Instead, the Ge in the structure is successively exchanged, forming short channel Al-Ge heterostructures with atomically abrupt interfaces [21, 22]. Exploration of the thermal exchange reaction of Ge and Al has opened up an interesting platform for the fabrication of ultra-short Ge channels or nanodots [23–25].

With further decreasing gate lengths, the carrier transport becomes ballistic, allowing the charge carriers to move through the channel without scattering. Thereby, it is possible to exceed the velocity saturation of the carriers, with the transistor speed scalable with high mobility materials. [6, 8]. In recent years quantum ballistic transport in nanostructures has been of great interest [23, 26]. Experiments investigating this effect have long been limited to high magnetic fields (> 4 T) or ultralow temperatures [27]. Ballistic transport phenomena at room temperature were observed in low dimensional high-mobility materials like carbon nanotubes or graphene [28–30] or III-V compound semiconductor materials [26]. The formation of ultrascaled Ge segments in monolithic Al-Ge-Al NW heterostructures with thermal exchange reaction has enabled the demonstration of quantum ballistic transport in semiconductor NWs at room temperature [23].

In this thesis, the fabrication of monolithic Al-Ge-Al heterostructures embedded in the device layer of a GeOI substrate based on the thermally induced exchange reaction is investigated. So far this substitution process was only shown in Ge NWs grown by the VLS approach. The use of GeOI substrates offers the potential for a wafer-scaled fabrication of large arrays of nanoscaled devices with precisely defined geometries at predefined positions. In order to enable ballistic transport even on top-down fabricated Al-Ge structures, the production of narrow structures with ultra-short Ge segments in the nanometer range, close to the dimensions of NWs, is envisaged.

Chapter 2 provides a short theoretical introduction in the physico-chemical properties of the Al-Ge material systems, the properties and fabrication of GeOI substrates and the

solid state diffusion process enabling the controlled substitution of Ge atoms in Al-Ge heterostructures. Furthermore, theoretical aspects of the physics of metal-semiconductor interfaces and the phenomena of (quantum) ballistic transport are covered. In chapter 3 the experimental techniques required for the fabrication of the Al-Ge-Al heterostructure devices are introduced. Methods for further reduction of the structural dimensions and the production of freely suspended devices are presented. The setup for electrical measurements to characterize the properties of the Al-Ge heterostructures is described. Chapter 4 focuses on the results obtained from morphological and electrical characterizations. Thereby the thermally induced exchange reaction in structures with various dimensions, crystallographic orientations and geometries is investigated. The results of the electrical measurements, with the influence of cross section and Ge channel lengths are discussed. Finally, chapter 5 provides a summary of the key results of this thesis and gives an outlook for future investigations covering the Al-Ge-Al device structure with ultrascaled Ge segments.



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Chapter 2

Theory

This chapter discusses the theoretical aspects relevant for this work. The first part focuses on the basic physico-chemical properties of the materials Al and Ge. The basic structures and selected production methods using GeOI, the initial substrate of this work, are discussed. The second part covers the characteristics of the Al-Ge system. This includes the electrical properties of the metal-semiconductor heterostructure, interfaces and impurity states. Furthermore, the theoretical aspects of solid-state diffusion are described, with special focus on the substitution process of Ge by Al, the main process for the fabrication of Al-Ge heterostructures. Finally, the theory behind an interesting transport phenomenon for nanoscaled semiconductor structures, the ballistic transport, is described.

2.1 Materials

Ge, a semiconductor and Al, a metal, are two well-known and commonly used materials in the semiconductor industry. While the first transistor in 1948 was fabricated out of Ge, nowadays most electronic devices are realized using Si as base material. Al on the other hand is the most common metal in the earth's crust, used for a wide range of applications [31].

2.1.1 Germanium

Ge is a grey-white and brittle metalloid and an important elemental semiconductor, placed in the fourth group of the periodic table of elements with the atomic number 32. With an average occurrence of around 1.6 ppm in the earth's crust, Ge is rather scarce and not found in large deposits with high concentrations [32]. It is mainly obtained as a by-product from zinc ores and is also associated in other minerals like agryrodite (a sulfide of Ge and silver), germanite ($\sim 8\%$ Ge content) and coal. With zone-refining techniques the production of ultra-high purity crystalline Ge with an impurity of only one part in 10^{10} is possible, which is required for the use in the semiconductor industry [4].

Ge has a melting point of 938.25°C and a boiling point of 2833°C . In its solid state it crystallizes in a diamond crystal structure which can also be described as two interpenetrating fcc structures, displaced relative to each other by $1/4$ of the main diagonal. Each Ge atom is surrounded by four other atoms positioned at the corners of a tetrahedron and connected by covalent bonds [33]. The unit cell of this structure is shown in Figure 2.1a. The distance to the nearest neighbor in this lattice is $\sqrt{3}a/4$, with the lattice constant $a = 5.66 \text{ \AA}$ at 0 K [34]. Other group IV elements like C, Si and α -Sn also crystallize in a diamond structure. In the diamond crystal the atoms are in a sp^3 hybridized state and all available valence electrons can be shared with the neighbors such that only the bonding orbitals are occupied. This forms a fully occupied valence band and a conduction band which are separated by an energy gap [33]. The band structure of Ge in Figure 2.1b showing the minimum of the conduction band at L and the maximum of the valence band at Γ , resulting in an indirect band gap of $E_g = 0.66 \text{ eV}$ [35].

In an indirect band gap material, radiative interband transitions are very unlikely since they would require a three particle process with the generation of a phonon in addition to the emitted photon for conservation of momentum. Therefore, most transitions occur non-radiative without the generation of photons. However, Ge features an energy separation at the zone-center Γ valley with $E_{\Gamma 1} = 0.8 \text{ eV}$ only 140 meV larger than its indirect band gap. By applying uniaxial tensile strain in combination with high n-type doping its band structure can be altered such that it becomes a direct band gap semiconductor. This allows the implementation of LEDs and lasers made of Ge that can be monolithically integrated into a CMOS

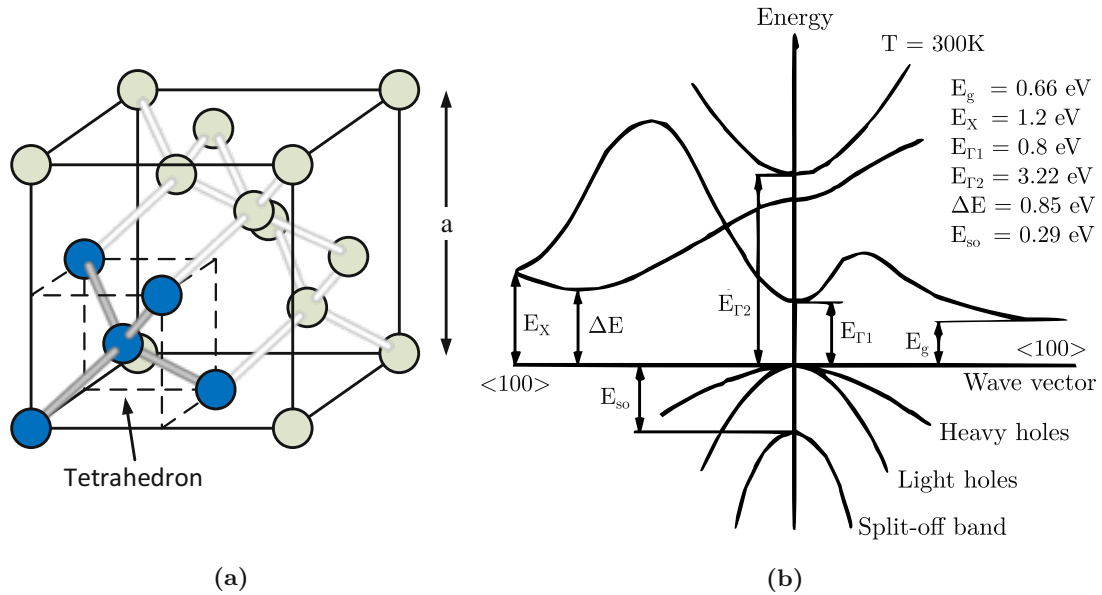


Figure 2.1: (a) Schematic representation of the diamond crystal structure of Ge with a lattice constant of $a = 5.66\text{ \AA}$. Each atom is connected to four neighbors which are distributed evenly in space to form a tetrahedron. Picture adapted from [36]. (b) The energy band structure of Ge shows an indirect band gap with $E_g = 0.66\text{ eV}$ and a direct band gap with $E_{\Gamma_1} = 0.8\text{ eV}$. Picture based on [35].

process [13, 14]. Ge also features light effective masses of electrons and holes that lead to a significantly higher carrier mobility of $\mu_e = 3800\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $\mu_h = 1820\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ compared to Si with $\mu_e = 1900\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $\mu_h = 500\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ [4]. The hole mobility is the highest of all known semiconductor materials. This makes a very promising material for high-performance CMOS technology, operable at lower supply voltages of about 0.5 V [37].

In contrast to Ge, Si forms a very stable native oxide which can be easily grown and used as high-quality gate oxide in FETs alongside numerous other applications in the semiconductor industry. The native oxide of Ge is water-soluble, thermally unstable and readily decomposes into several Ge_yO_x suboxides, which strongly affects the morphology and thus electrical quality of the interface. The quality and composition of the oxide layer which commonly consists of a mixture of GeO_2 and GeO strongly depends on oxidation condition, temperature and pressure [38]. GeO_2 would be the preferred oxidation state to reduce the density of trap states at the interface. However, at temperatures above 400°C , GeO_2 reacts with the interface and is reduced to GeO , leading to an increase in trap states [38]. In further consequence this significantly decreases the performance of a Ge-based MOSFET since this leads to an increase in leakage current. In addition, these traps reduce the intrinsically high carrier mobility of Ge due to carrier scattering and also increases the off-state leakage current and sub-threshold turn-off, limiting device scalability [37, 38].

Consequently, finding and scaling high-quality gate dielectrics on Ge that are comparable to that of state-of-the-art Si is still a challenge and focus of research. High- κ dielectric materials like HfO₂ and ZrO₂ with additional passivation layers to get rid of unstable Ge oxides [7, 8] or thin Si caps [39] have already achieved promising results.

Both Ge and its oxide are transparent to infrared and are widely used in optical applications. The absorption coefficient significantly exceeds that of Si [40], which enables highly sensitive infrared detectors. Due to its high refractive index and dispersion it is also an important material for fiber optics and other optical systems like wide-angle camera lenses and microscope lenses [4].

Finally, Ge features a large exciton Bohr radius with $a_{B,Ge}^* = 24.3$ nm, which is approximately five times larger than that of Si with $a_{B,Si}^* = 4.9$ nm. Combined with its high hole mobility, strong quantum confinement effects can thus be obtained [23].

2.1.2 Germanium on Insulator

In dedicated CMOS technology silicon on insulator (SOI) is commonly used as a source material. It benefits from lower substrate capacitance and better electrostatic control leading to leakage reduction and offers compatibility to non-planar device configurations like FIN-FETs [41]. To combine the advantages of SOI and simultaneously exploit the high carrier mobility of Ge, a GeOI substrate offers an attractive platform for future Ge-based devices. This typically consists of a Si handle wafer, stacked with a thick thermal oxide (SiO₂) and a thin Ge layer. The fabrication of a GeOI substrate can be obtained by different methods such as the Ge condensation technique [42], liquid-phase epitaxy [43] or a layer transfer technique (Smart Cut™) [9, 44, 45].

With the Ge condensation technique the GeOI structure is formed by thermal oxidation of a strained Si-Ge layer epitaxially grown on to an SOI substrate. Si is oxidized to form a SiO₂ layer while the Ge fraction in the Si-Ge layer gradually increases until eventually a pure Ge layer remains. The final thickness of the GeOI layer can be designed arbitrarily by controlling the composition and the thickness of the initial Si-Ge layer. With this method GeOI layers below 10 nm with low surface roughness of 0.4 nm rms can be achieved [42]. The high thermal budget and plastic deformations during the oxidation process may be drawbacks of this technique [9].

Another simple method to achieve high-quality single-crystal GeOI structures is liquid-phase epitaxy on Si substrates. As a first step, silicon nitride is deposited on top of the Si wafer and then patterned to open seeding windows. Ge is then non-selectively sputtered onto it, passivated by a low-temperature oxide and briefly heated just above the Ge melting point. During the slow cool down liquid-phase epitaxy occurs, with the growth front starting at the Si/Ge interface of the seeding windows. The crystal orientation of the Ge film can be controlled by the seeding Si substrate. This process is also compatible with Si-based fabrication. This Ge device structures can be reliably integrated in Si based integrated

circuits. However, the lateral expansion of the GeOI crystal is typically limited to 20 μm [43].

A layer transfer method such as the Smart Cut™ technique uses either a bulk Ge substrate or a Si substrate with epitaxial Ge as a donor wafer. The Ge substrate is implanted with hydrogen and prepared for hydrophilic bonding onto a Si wafer with thermally grown oxide on top. After subsequent annealing, the layers of the bonded wafer split due to the hydrogen induction, forming a GeOI substrate and release the remaining Ge donor substrate for reuse [46]. With this process wafer diameters up to 200 mm with a thickness range from 200 nm down to below 50 nm were demonstrated. With the selection of the starting material different crystal orientation and strains are possible [44]. Other similar layer transfer methods remove the layers above the GeOI substrate by dry and wet etching instead of the thermal cut with hydrogen implantation, resulting in a lower doping concentration but also a complete loss of the donor wafer [45].

2.1.3 Aluminum

Al is a silvery-white metal, placed in the third group of the periodic table with atomic number 13. About 8.1 % of the mass of the earth's crust consists of Al, making it the most abundant metal. However, since this element is highly reactive, it is never found in its pure form in nature [4]. The production of Al is based on the energy-intensive electrolysis of molten Al_2O_3 using the Hall-Herault process. High purity Al with $\geq 99.99\%$ purity can be reached [31]. Al crystallizes in a fcc structure with a lattice constant of $a = 4.05 \text{ \AA}$ [47]. The crystal structure is illustrated in Figure 2.2. Al has a melting point of 660.32°C and a boiling point of 2519°C [4].

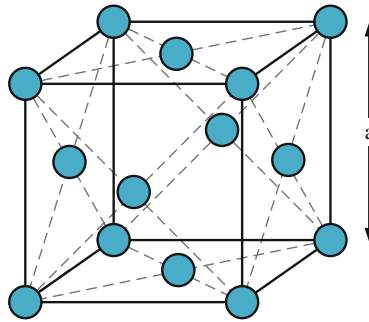


Figure 2.2: Schematic representation of the fcc crystal structure of Al with a lattice constant $a = 4.05 \text{ \AA}$. Picture adapted from [36].

The low density of 2.7 g/cm^{-3} and its good mechanical properties, combined with its good workability make Al and its alloys the second most widely used metallic material after steel [31]. Evaporated on surfaces it can form high reflective coatings both for visible light and radiant heat. Due to the relatively low electrical resistivity of $2.65 \mu\Omega \text{ cm}$ at

room temperature it is often used as an electrical conductor [4] and have been used for many years for interconnects in ICs. However, with increasing requirements in the modern semiconductor industry, especially for high-speed sub-100 nm devices, Al has now largely been replaced by copper as an interconnect material due to its higher conductivity and higher resistance to electromigration [48]. Below the critical temperature $T_c = 1.2\text{ K}$ Al reaches superconductivity [31]. In an alloy with other group 5 elements Al forms III-V compound semiconductors with direct (AlN) or indirect (AlP, AlAs, AlSb) band gap [31].

Al forms a thin but compact natural oxide passivation layer, which is strongly adherent and protects the underlying metal against further oxidation. This oxide mainly consists of amorphous Al_2O_3 , commonly called alumina, with extremely low electrical conductivity, high temperature resistance and thus exhibits high corrosion resistance to chemicals. It is applied as an insulator material in electronics, chemical industry and high temperature applications [31].

2.2 The Al-Ge System

In addition to the properties of the individual materials Ge and Al, it is also mandatory to investigate how these materials interact. Therefore, the electrical and physico-chemical properties of the Al-Ge material system are examined. In close contact these materials form a Schottky contact, which will be briefly discussed theoretically. The impurity levels of different elements with focus on Al inside the Ge band gap are also addressed. In the section about the physico-chemical properties the binary eutectic system of Al and Ge as well as the solubility of the elements in each other are discussed.

2.2.1 The Schottky Contact

At the metal-semiconductor interface between Al and Ge a potential energy barrier is formed. The properties of this junction mainly depend on the difference in work function of the two materials $\phi_m - \phi_s$, which defines the contact potential. The work function in a metal ϕ_m describes the difference between the vacuum level and the Fermi level, with $q\phi_{m,Al} = 4.2\text{ eV}$ for Al [49]. In a semiconductor it is defined as $\phi_s = \chi + \phi_n$, where χ is the electron affinity measured from the bottom of the conduction band E_C to the vacuum level E_{vac} , and ϕ_n is the energy difference between E_C and the Fermi level E_F .

If the work function of the metal ϕ_m exceeds that of the semiconductor ϕ_s ($\phi_m > \phi_s$), the energy bands of the semiconductor shift downwards. This causes electrons to migrate from the semiconductor into the metal. In an n-type semiconductor this redistribution of charges at the interface creates a depletion region near the junction, leading to a behavior similar to a p-n junction of a conventional diode. This condition is called a rectifying contact or Schottky contact and is illustrated in Figure 2.3a. In a p-type semiconductor no depletion region is formed since the extracted electrons are taken by the dopants. The majority charge carriers are accumulated near the junction and can move freely in both directions. Therefore, this junction behaves similar to an ohmic contact.

If the work function of the metal is smaller than that of the semiconductor ($\phi_m < \phi_s$) the energy bands of the semiconductor are shifted upwards to the metal, resulting in a reversed behavior, with p-type semiconductors forming a Schottky contact and n-types showing quasi ohmic behavior [36, 50].

The potential barrier height of the Schottky contact is the difference between the metal work function and the electron affinity of the semiconductor

$$q\phi_B = q(\phi_m - \chi_s). \quad (2.1)$$

For an Al-Ge junction a barrier height of about $q\phi_{B,Ge} = 0.35\text{ eV}$ is expected [49]. As a real semiconductor suffers from imperfections and dangling bonds, interface states across the

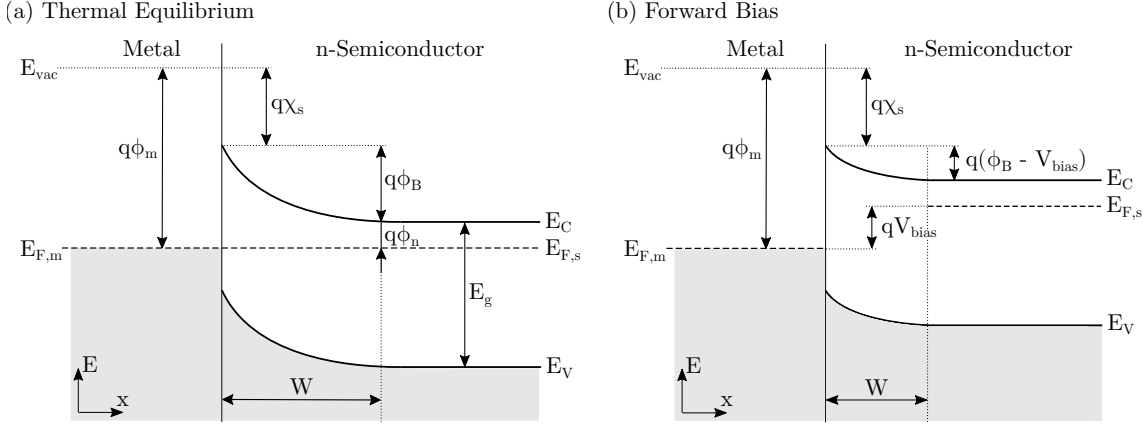


Figure 2.3: Energy-band profile of a metal-semiconductor junction for an *n*-type semiconductor with $\phi_m > \phi_s$ in (a) thermal equilibrium and (b) with an external bias V_{bias} in forward direction, reducing the Schottky barrier height $q\phi_B$ at the interface and enabling current flow by majority charge carriers.

band gap are introduced. The Fermi level at the interface can then be pinned by surface states at the value $q\phi_0$, with the new energy potential barrier height

$$q\phi_B = E_g - q\phi_0. \quad (2.2)$$

This makes the barrier almost independent of the metal work function since the surface properties of the semiconductor become dominant. In most covalent semiconductors like Si, Ge or GaAs there is a high density of surface states, leading to strong Fermi level pinning [36]. This effect can be significantly reduced by insertion of a thin dielectric at the metal semiconductor interface [51].

The potential barrier across the Schottky junction can be shifted by an external bias V_{bias} in the order of $-qV_{bias}$ (see Figure 2.3b). The depletion width W of the depleted area is also reduced with increasing bias. This then influences the current flow, which for an ideal Schottky contact is defined as

$$I = I_0 \left[\exp\left(\frac{qV_{bias}}{k_B T}\right) - 1 \right]. \quad (2.3)$$

I_0 describes the reverse saturation current and depends exponentially on the potential barrier height of the Schottky contact ϕ_B as well as the Richardson constant A^* for thermionic emission as proportionality factor, with

$$I_0 = A^* T^2 \exp\left(-\frac{\phi_B}{k_B T}\right). \quad (2.4)$$

The transport of current in a metal-semiconductor junction is mainly based on majority carriers, which is in contrast to a p-n junction, where transport is based on minority carriers [36, 50].

In a heterostructure with a Ge segment incorporated between two Al contacts, as it is the case for structures presented later in this thesis, the electrical behavior corresponds to two back-to-back Schottky diodes in series with the resistance of the Ge segment [21]. With an additional gate contact on top a so called Schottky barrier (SB) MOSFET is formed. While it behaves largely similar to a normal MOSFET, it usually shows ambipolar transfer characteristics because carriers can be injected from both drain and source through the Schottky contact. The SB-MOSFET offers advantages in fabrication and performance such as low parasitic resistance of source and drain, superior off-state leakage current control, elimination of parasitic bipolar action and atomically abrupt junctions, enabling a physical scaling of the device to sub-10 nm gate lengths [52].

2.2.2 Impurity Levels in Germanium

Al does not cause deep traps in the Ge energy band gap when incorporated into the Ge lattice. With a low ionization energy of only 10.8 meV above the valence band of Ge it is therefore considered as a shallow impurity. This is a major benefit compared to other commonly used materials such as gold or copper, as these generate deep traps in the middle of the band gap and cause a significant reduction of the minority carrier lifetime due to unwanted impurity recombination [50]. Figure 2.4 shows the energy levels for different impurities in Ge.

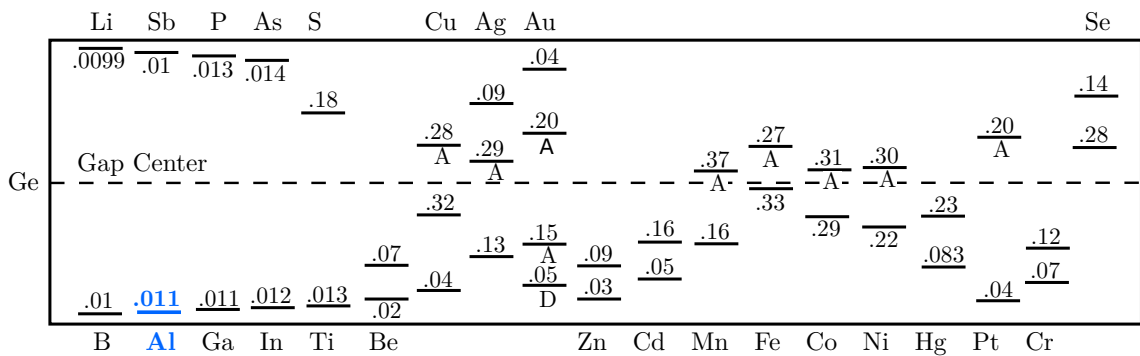


Figure 2.4: Impurity energy levels of various elements in Ge with respect to the Ge band edges (A = acceptor, D = donor). Al in Ge has a shallow ionization energy of 10.8 meV. Picture based on [53].

2.2.3 Physico-chemical Properties

Al and Ge form a simple binary eutectic system with three solid phases. The corresponding phase diagram is shown in Figure 2.5. Since Al is trivalent and Ge is tetravalent, they do not form stable stoichiometric compounds. Below the eutectic temperature of 420°C a eutectic structure with local crystallites is formed, instead of intermetallic phases, that allow very sharp metal semiconductor interfaces in NW structures [21]. In this solid eutectic

system the solubility of the two materials in each other is very low. Only about 2% of Ge atoms can be incorporated to the Al lattice at the eutectic temperature, while it is 1.1% for Al in Ge. Only under special conditions like rapid quenching of the liquid metastable compound phases beyond the limits of the solubility can be formed [47].

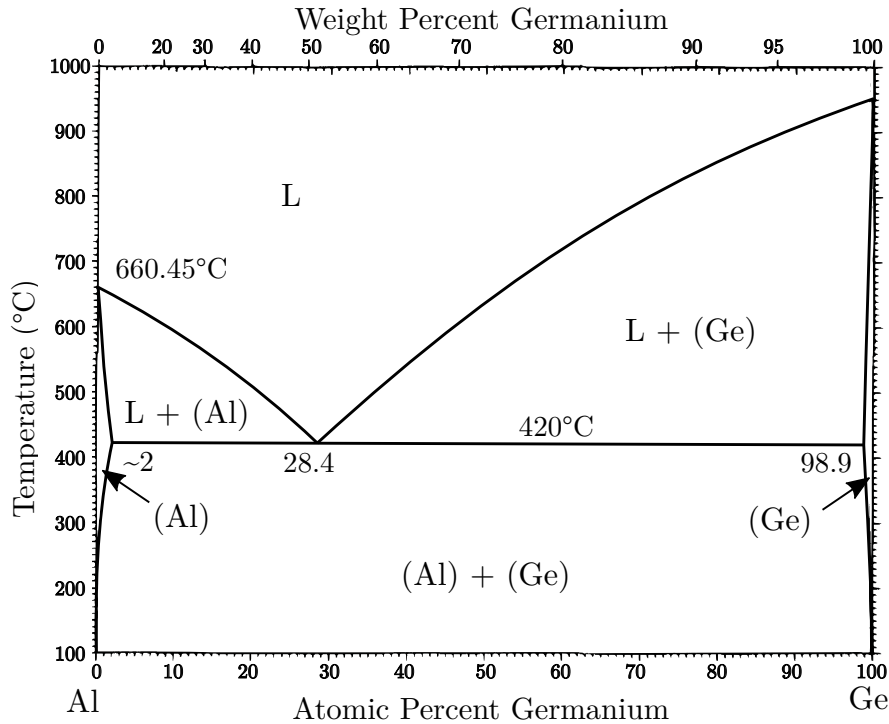


Figure 2.5: Al-Ge phase diagram with an eutectic temperature of 420°C. Picture based on [47].

2.3 Solid-State Diffusion in the Al-Ge System

Diffusion is the movement of particles such as atoms or molecules to compensate concentration gradients. It is caused by Brownian motion which is the inherent, incessant motion of small particles in a medium. While the diffusion process in gases and liquids takes place in the range of cm/s and mm/s respectively, it is rather slow in solids. In metals close to the melting point diffusion rates of about 1 $\mu\text{m/s}$ are common, but decrease strongly with decreasing temperature [54].

Thermal diffusion of metals into Si or Ge is used to form ohmic or rectified metal-semiconductor interfaces. The formation and integration of germanides like NiGe or YbGe and silicides like NiSi or TiSi₂ in advanced CMOS devices is important to reduce serial resistance and increase switching speed [55–57]. However, unwanted diffusion of light elements like O and C during processing can lead to contamination that is difficult to eliminate. Impurities can also introduce deep-level defects into the energy band gap

leading to possibly unwanted effects.

There are different mechanism of diffusion, mainly based on point defects in the crystalline solid. These defects allow the atoms to move through the crystal. Atoms which are considerably smaller than the solvent atoms and are incorporated on interstitial sites of the host lattice while containing the overall geometry of the lattice are called interstitial solid solutions. The movement of these additional atoms from one interstitial site to one of its adjacent sites is called interstitial mechanism.

The vacancy mechanism describes the diffusion of an atom to a neighboring vacancy in the lattice. Vacancies are the most common form of thermally induced atomic defects in metals and ionic crystals. The vacancy mechanism is also considered to be the dominant effect in substitutional solutes, which consist of solute atoms that are similar in size to the host atoms. Agglomerates of vacancies, such as di- or trivacancies can occur in a crystal, which diffuse similar to monovacancies, but are usually more mobile. Another diffusion mechanism is the interstitialcy mechanism, also called the indirect interstitial mechanism. An interstitial atom similar in size to the lattice atom acts as a diffusion vehicle. It replaces a neighboring atom on a lattice- or substitutional site which is then itself moved to another interstitial position. The two atoms move in unison, so it is a collective mechanism [54]. In Ge, dopant and self-diffusion in thermal equilibrium is dominated by the vacancy mechanism, mainly due to the movement of neutral and negatively charged vacancies. Therefore, diffusion of group-III elements is smaller (B) or similar (Al, Ga) to self-diffusion of Ge, while it is much larger for group-V elements like P or As. Self-diffusion in Si, especially at higher temperatures, also occurs through the interstitialcy mechanism. This makes diffusion of foreign atoms in Si always faster than self-diffusion. For Al, as well as for most other metals with a fcc crystal structure the vacancy mechanism is the determining process for self- and interdiffusion.

The flux of the diffusing particles is described by Fick's first law

$$J = -D\nabla C . \quad (2.5)$$

The vector of the diffusion flux J is directed in the opposite direction of the concentration gradient vector ∇C . The proportionality factor D is the diffusion coefficient or diffusivity and is a material property. For anisotropic media D is depicted as tensor. The diffusion coefficient strongly depends on the temperature, usually following Arrhenius law

$$D = D_0 e^{-E_a/RT} , \quad (2.6)$$

with the frequency factor D_0 , the activation energy E_a , the gas constant $R = N_A k_B \approx 8.314 \text{ JK}^{-1} \text{ mol}^{-1}$ and the temperature T . E_a and D_0 are referred as activation parameters of diffusion [54].

In a diffusion process in isolated systems without any sources or sinks the number of diffusing particles remains constant. As it obeys a law of conservation a continuity equation can be formulated:

$$-\nabla \cdot J = \frac{\partial C}{\partial t} . \quad (2.7)$$

Fick's first law (2.5) combined with the continuity equation (2.7) result in a second-order partial differential equation, which is referred as Fick's second law or diffusion equation:

$$\frac{\partial C}{\partial t} = \nabla \cdot (D\nabla C) . \quad (2.8)$$

In binary alloys the two materials can have different intrinsic diffusion coefficients. According to Fick's first law (2.5) this results in different diffusion fluxes for the particles of each material. This inequality results in a movement of the interface between the two phases due to a net mass flow accompanying the interdiffusion process, driven by the vacancy mechanism. To maintain local equilibrium during the movement of the interdiffusion zone, lattice sites are created on one side and eliminated on the other side. This is achieved by the creation and annihilation of vacancies. This process is called the Kirkendall effect and was discovered in the 1940s in a copper-brass diffusion couple [54, 58].

The movement of the interface can be expressed by the Kirkendall velocity v_K in terms of the two intrinsic fluxes, j_A and j_B , and their partial molar volumes \tilde{V}_A and \tilde{V}_B :

$$v_K = -(\tilde{V}_A j_A + \tilde{V}_B j_B) . \quad (2.9)$$

Using Fick's first law (2.5) and introducing $dC_A = -(\tilde{V}_B/\tilde{V}_A)dC_B$ the Kirkendall velocity for the one-dimensional case can be written as:

$$v_K = \tilde{V}_B(D_B - D_A)\frac{\partial C_B}{\partial x} . \quad (2.10)$$

For a simple description of isothermal diffusion in a binary substitutional alloy by a single equation (2.5) the interdiffusion coefficient can be introduced with

$$\tilde{D} = C_B\tilde{V}_B D_A + C_A\tilde{V}_A D_B . \quad (2.11)$$

Thus, it is possible to calculate the intrinsic diffusivities of both components by measuring the interdiffusion coefficient and the velocity of the Kirkendall plane. For abrupt interfaces between two material regions with different concentrations, the concentration profile can be approximated by a Heaviside step function $H(x)$. With Fick's first law (2.5) this results in a diffusion flux at the interface of

$$J_{interface}(x) = -\tilde{D}(C_B - C_A)\delta(x) , \quad (2.12)$$

with the Dirac delta function $\delta(x)$ as the derivative of this step function [59].

Usually, the diffusion rate is not constant over time due to different rate limiting processes. Based on the Deal and Grove model, which describes the diffusion of particles to the reaction surface and subsequent formation of the new phase in an oxidation process of a substrate, the solid-state reaction in NWs was kinetically studied by many research groups [18, 19, 22, 60]. The different models in these studies were used to fit the resulting data as accurately as possible and differentiate between several processes that limit the reaction speed of the diffusion. Table 2.1 shows four potential rate limiting processes that can occur during a thermal exchange reaction and their impact on the diffusion progress in the specimen. For short reaction times the diffusion and incorporation of the metal atoms into the semiconductor is limited by the reaction at the interface. The diffusion length L is proportional to the time t . If the surface area between the metal reservoir and the NW is limiting the reaction, the diffusion length additionally depends on the radius R of the NW, with $L \propto R^{-1}t$. For longer reaction times, the diffusing atoms have to travel long distances through the material, which makes diffusion the limiting factor. Therefore, the length depends on the square root of the time. If the diffusion of exchanged atoms primarily takes place over the surface, L also depends on the NW radius with $L \propto \sqrt{\frac{t}{R}}$, while it is independent of the size of the NW for volume diffusion ($L \propto \sqrt{t}$) [59].

Table 2.1: *Potential diffusion rate limiting processes of thermal exchange reaction and their influence on the diffusion length L in relation to the time t and the radius R of the NW [22]*

Al-Ge exchange regimes	Diffusion length L
Metal reservoir limited	$\sim R^{-1}t$
Interfacial exchange limited	$\sim t$ (independent of R)
Volume diffusion limited	$\sim \sqrt{t}$ (independent of R)
Surface diffusion limited	$\sim \sqrt{\frac{t}{R}}$

In most binary metal semiconductor systems where solid-state diffusion of metal into a semiconductor is studied, the metal atoms are incorporated into the semiconductors lattice, forming an intermetallic compound. The formation and propagation of different silicide and germanide phases with e.g. Ni [18, 19, 60], Cu [20, 59] or Mn [61, 62] in Si or Ge NWs was shown. These systems and their precise process control play an essential role for the integration of nanoelectronics with CMOS technology. In general, the main motivation to form intermetallic compounds is to improve the contact quality of the metal semiconductor junction. But these quasi-metallic structures still exhibit higher contact resistivity than pure metals.

However, a heat-induced solid-state replacement inside a semiconductor NW by metal atoms without the formation of intermetallic compounds was only reported in the binary Al-Ge [21] and pseudobinary Au-GaAs [63] systems. Therefore, the semiconductor NW, usually grown with the VLS method, is contacted by metal contacts that are very large in terms of volume compared to the wires. Subsequently, a thermal annealing step is performed to initiate the exchange reaction. For the Al-Ge system, the Ge atoms in the NW are gradually substituted by Al atoms, leaving behind a pure and crystalline Al segment. The emerging Al-Ge interface appears to be very sharp or even atomically abrupt, despite the big lattice mismatch of the two compounds. Furthermore, no defects are observed at the interface [21, 23].

The substitution of Ge by Al is caused by the asymmetric diffusion behavior in this binary material system. As shown in Table 2.2, the diffusion coefficient of Ge in Al as well as the self-diffusion of Al are orders of magnitude higher than the diffusivity of Al or Ge in Ge. Therefore, Ge atoms can easily diffuse into the big Al pad. In Figure 2.6 the substitution process in a Ge NW is illustrated. EDX measurements, which detected an about 2 nm thick Ge shell around the crystalline Al leads, indicate that Ge diffuses through surface channels back into the Al reservoir [22]. The lattice sites left behind are filled by Al atoms which are supplied by their rapid self-diffusion [21].

Table 2.2: Activation energy E_a and frequency factor D_0 [58, 64] for Ge and Al and the diffusion coefficient D at 400°C resulting from the Arrhenius formula (2.6).

Diffusion of:	Al	Ge	Al	Ge
in:	Al	Al	Ge	Ge
E_a (kJ/mol)	123.5	121.3	332.8	303
D_0 (cm ² /s)	0.137	0.48	1000	24.8
D (cm ² /s)	$3.57 \cdot 10^{-11}$	$1.86 \cdot 10^{-10}$	$1.5 \cdot 10^{-23}$	$7.61 \cdot 10^{-23}$

This system shows a parabolic growth behavior, approximated by

$$L = \sqrt{2Dt} \quad (2.13)$$

indicating a diffusion limited process. The exchange reaction stops when the dissolved Ge in the Al contacts surpasses its solid solubility limit [21] at about 1.69 at% at 400°C [65]. Remarkably, no contamination of the remaining Ge segment by Al atoms can be detected due to the extremely low diffusion coefficient of Al in Ge.

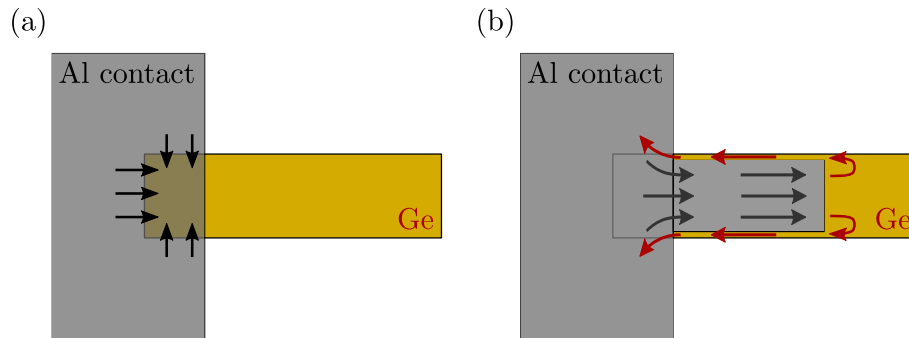


Figure 2.6: *Solid-state diffusion of Al into a Ge NW. (a) In the contact pad Al is penetrating the NW from all sides. (b) The abrupt Al diffusion front is propagating along the Ge NW while Ge diffuses along the NW surface into the Al contact [22, 66].*

For Al-Ge, an effective exchange can be observed at temperatures between 350°C and 410°C with diffusion rates of about 3 nm/s up to 20 nm/s [67]. The closer the temperature approaches the eutectic temperature, the faster the exchange reaction proceeds, which can be easily deduced from the increasing diffusion coefficients (see Equation 2.6). Furthermore, investigations of VLS grown NW with various diameters from 10 nm to 150 nm showed a slight increase in the propagation rate for smaller-diameter NWs [21, 22]. This indicates that the Al-Ge substitution is a surface-diffusion-limited process.

With this method, Al-Ge-Al heterostructures with ultra-short Ge channel lengths down to sub-10 nm length scales can be achieved [25], independent of the lithography process and its spatial resolution. This makes this process very interesting for short-channel Ge FETs [21] or the observation of quantum ballistic transport at room temperature [23].

2.4 Ballistic Transport

With continuous miniaturization of semiconductor devices into the nanometer region, short-channel effects can occur that significantly change their electronic properties. In a conventional, macroscopic conductor the propagation of charge carriers is diffuse due to frequent scattering on phonons, impurities or crystal defects. The mean free path L_m describes the mean distance between two scattering events. With every collision, energy is lost to the lattice, resulting in limited carrier velocities. The ohmic conductance

$$G_\Omega = \sigma \frac{A}{L} \quad (2.14)$$

depends on the dimension of the conductor and the conductivity σ of the material. The conductivity is temperature dependent and directly related to the mobility μ of the charge carriers. In semiconductors, both electrons and holes contribute to the current flow, with $\sigma = q(\mu_n n + \mu_p p)$ [36].

If the length of the conductor becomes comparable to or smaller than the mean free path L_m , the charge carriers are no longer transported diffusely through the material, but ballistically. The carriers follow normal phase space trajectories with very little or no scattering on the structure while gaining energy from an electric field. Since no energy is lost to the lattice, the carriers can acquire velocities much faster than the saturation velocity in diffusive transport. Within this small distance the drift velocity increases with time according to $\propto qEt/m^*$ exceeding more than twice the steady state velocity at high fields [36].

The mean free path L_m can be expressed in terms of the Fermi velocity $v_f = \hbar\sqrt{2\pi n}/m^*$ and the momentum relaxation time τ_m by $L_m = v_f\tau_m$ and depends on the material and temperature [33]. At room temperature it ranges from several nanometers in group-IV semiconductors to micrometers for high-mobility materials such as carbon nanotubes or graphite [28–30]. For Ge the mean free path is approximately 35 nm [66].

From Equation 2.14 one would consider that the conductance of a conductor between two comparatively large electrical contact pads would tend to infinity as its size is progressively reduced. But if the length of the conductor is reduced below the mean free path L_m , its conductance is no longer dependent on its dimensions. It is then limited to a contact resistance G_C^{-1} , which arises from the interface between the contact pads and the ballistic conductor. Figure 2.7b shows a schematic sketch of a one-dimensional ballistic conductor between two wide contact pads. The current in the macroscopic contacts is carried by an infinite amount of transverse modes, but inside the microscopic ballistic conductor only a few discrete modes can propagate (see Figure 2.7a). This redistribution of the continuous band structure to the discrete bands causes the contact resistance. Figure 2.7c shows the drop of the electrochemical potential at the interfaces due to the contact resistance. The potential inside the ballistic conductor is constant, implying that the charge carriers can move through it without resistance [68].

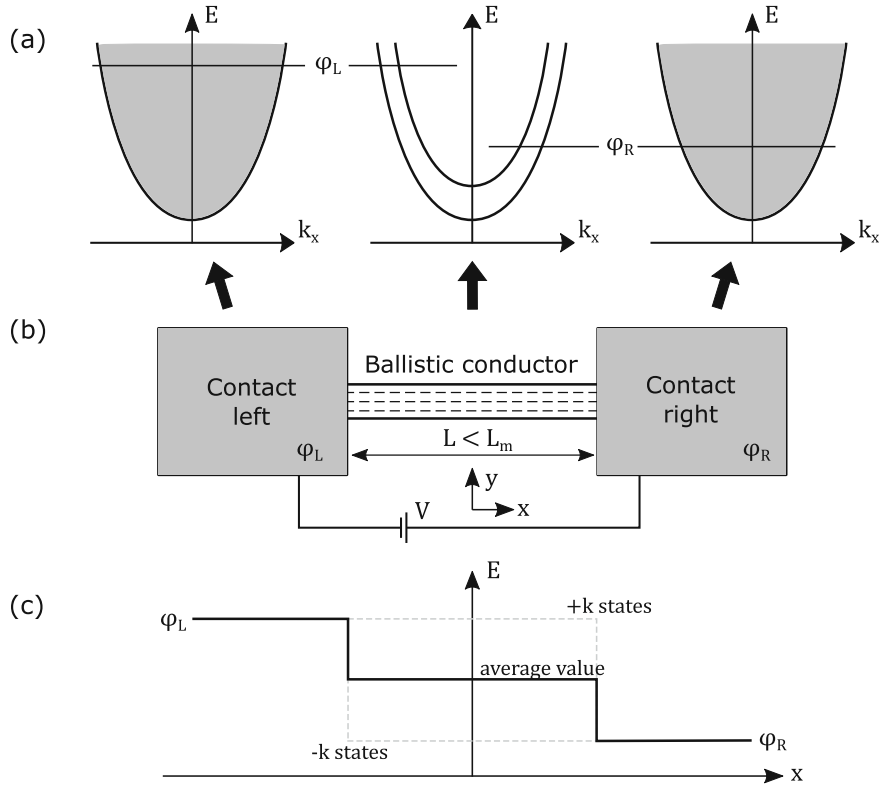


Figure 2.7: One-dimensional ballistic transport: (a) Energy bands as a function of the wave vector k_z along the direction of the one-dimensional conductor. The contacts have a high density of transverse modes (indicated by grey shading) while in the ballistic conductor only a discrete number of modes is formed. (b) Schematic sketch of a narrow ballistic conductor connected between two macroscopic contact pads at different potentials φ_L , φ_R . (c) Variation of the electrochemical potential along the structure. The potential drops equally at the two interfaces due to the contact resistance while it is flat across the conductor. Picture based on [68].

The discrete energy levels of the free electrons in the sub-bands are given by the dispersion relation

$$E_i = \varepsilon_i(k_y, k_z) + \frac{\hbar^2 k_x^2}{2m^*} \quad (2.15)$$

with the quantified energy levels ε_i of the cross section ($k_y k_z$ -plane) and the kinetic energy of the free moving carriers in the x -direction. The number of transverse modes with energies above the cut-off energy E is given by $M(E)$. Modes below this energy cannot propagate. The microscopic current through the ballistic conductor is formed by free electrons in the sub-bands that move with the group velocity v and is calculated with $I = env$. The electron density n is derived from the density of states $D(E)$ and the Fermi distribution $f(E)$

$$n = \int D(E) f(E) dE \quad (2.16)$$

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_f}{k_B T}\right)} \quad (2.17)$$

with the Fermi energy E_f . At low temperatures ($T \approx 0\text{ K}$), the Fermi distribution in the two contacts can be approximated by a simple step-function $f(E) \approx \vartheta(E_f - E)$. Therefore, the current is equal to that carried by the occupied states between the two potentials φ_L and φ_R [33, 68]. Also, reflections at the interface between the ballistic conductor and the contact pads can be neglected as long as the energy is not too close to the bottom of the band [68]. Based on these assumptions the current in one sub-band can be calculated with

$$I_i = e \int_{\varphi_R}^{\varphi_L} D_i(E) v_i(E) dE. \quad (2.18)$$

For the one-dimensional case the density of states $D_i(E)$ (with consideration of a spin degeneration of 2) and the group velocity v_i of the electrons in a sub-band are given by

$$D_i(E) = 2 \frac{1}{2\pi} \left(\frac{\partial E_i}{\partial k_x} \right)^{-1}, \quad v_i = \frac{1}{\hbar} \frac{\partial E_i}{\partial k_x}. \quad (2.19)$$

Assuming that the number of modes M is constant over the energy range $\varphi_L > E > \varphi_R$, each sub-band in the ballistic conductor carries the same current [33, 68]. Therefore, with the voltage $V = (\varphi_L - \varphi_R)/e$ between the two contacts the total current sums up to

$$I = \sum_i^M I_i = \sum_i^M \frac{e}{\pi \hbar} (\varphi_L - \varphi_R) = \frac{2e^2}{h} M \cdot V. \quad (2.20)$$

From this the conductance of the ballistic conductor as a function of modes M can be derived

$$G_C = \frac{2e^2}{h} M = G_0 M \approx \frac{M}{12.9 k\Omega}. \quad (2.21)$$

For a single-moded ballistic conductor between two conductive contacts the contact resistance is $\sim 12.9 k\Omega$, decreasing inversely with the number of conduction channels M . Usually, the contact resistance of a ballistic conductor is rather low due to a high number of modes. The number of modes can be estimated assuming periodic boundary conditions. The allowed values for the transverse modes in the k_y, k_z -plane (see the dispersion relation (2.15)) are spaced with $2\pi/W$, depending on the width W of the conductor. At the Fermi energy $E_f = \hbar^2 k_f^2 / 2m^*$ a mode can only propagate if $-k_f < k_y, k_z < k_f$. The number of modes thus results from

$$M = \text{Int} \left[\frac{k_f W}{\pi} \right] = \text{Int} \left[\frac{W}{\lambda_f / 2} \right] \quad (2.22)$$

with the integer function $\text{Int}(x)$ returning the next lower integer value [68]. A qualitative estimation of the number of modes inside a structures such as a Al-Ge-Al NW heterostructure is thereby possible. For a NW diameter of $d = 25\text{ nm}$ and a Fermi wavelength of the

short Ge channel with $\lambda_{f,Ge} = 10.67 \text{ nm}$ this results in $M = 4$ modes [66].

If the diameter/width of the nanostructure is also scaled smaller than the exciton Bohr radius a_B^* , the valence and conduction bands are composed of discrete, equally spaced sub-bands. Their occupation can be controlled by applying a gate voltage, resulting in a quantization of the conductance of the one-dimensional conduction channel with a step height of G_0 (see Figure 2.8). The exciton Bohr radius depends on temperature and material and describes the space between an electron and a hole within an exciton [66]. Ge with its large Bohr radius of $a_{B,Ge}^* = 24.3 \text{ nm}$ combined with its high hole mobility therefore is an interesting material to exploit strong quantum confinement effects which could even be observed at room temperature [23].

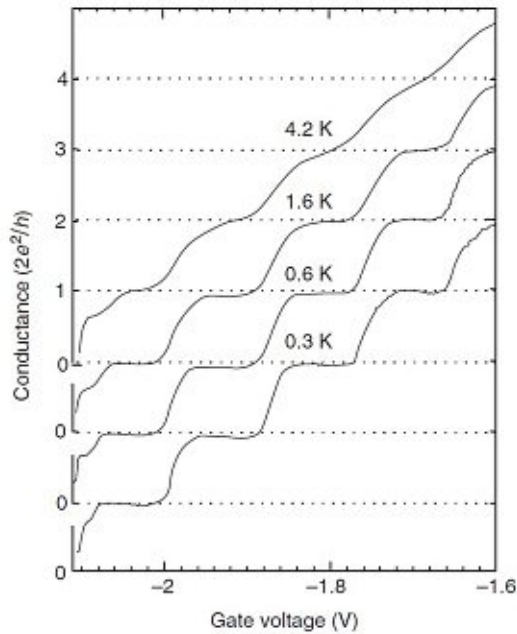


Figure 2.8: *Quantization of the conductance. With rising temperature the quantization steps become washed out [28].*

At higher temperatures, the conductance quantization becomes progressively washed out due to thermal broadening of the spacing of the one-dimensional sub-bands, making it more difficult to distinguish the individual plateaus (see Figure 2.8). The Fermi distribution $f(E)$ (defined in Equation 2.17) can no longer be approximated by a step function because of the disorder of the electron distribution in the sub-bands. Furthermore, an energy dependent transmission coefficient $T_i(E)$ describing the probability at which a carrier with a certain energy is transmitted through the contact interface has to be taken into account. Thus,

the current through the ballistic conductor at higher temperatures can be described by [28]

$$I = \frac{2e}{h} \int_{-\infty}^{\infty} dE \sum_i T_i(E) (f(E - \varphi_L) - f(E - \varphi_R)) . \quad (2.23)$$

The utilization of ballistic transport especially in nano-scaled MOSFETs is of great interest to significantly improve its performance as both the maximum current and the operating speed for the ballistic MOSFET can be increased while lowering its power dissipation [69]. Moreover, this effect enables the development of new devices like multi-valued logic gates that can handle e.g. quaternary numbers as inputs [70], or quantum logic gates in quantum computers [71].

Chapter 3

Experimental Techniques

This chapter covers the wafer-scaled fabrication of Al-Ge-Al heterostructures on GeOI substrates as well as their electrical characterization. Optical lithography and reactive ion etching (RIE) are used to pattern Ge microstructures in a variety of different shapes and orientations on the GeOI wafer. Subsequently, the structures are contacted with Al pads by lithography, sputter deposition and lift-off techniques. Using rapid thermal annealing the formation of Al-Ge-Al heterostructures with short Ge channel lengths is induced. To obtain nanoscaled devices electron beam lithography is used to further reduce the size of the pre-patterned Ge structures. A wet chemical treatment using a mixture of hydrogen peroxide and water can be used to uniformly reduce the cross section of the Ge segments. The fabrication of freestanding Al-Ge-Al devices is achieved by the Al-Ge exchange in underetched Ge nanobeams.

By using a needle probe station in combination with a semiconductor analyzer the I/V and transfer characteristics of the fabricated heterostructures are measured.

3.1 Fabrication of Microstructures on GeOI

In this work, a GeOI substrate with a 75 nm thick device layer of $\langle 100 \rangle$ oriented single crystal Ge on top of a 150 nm thick SiO_2 insulator layer and a 500 μm doped Si substrate is used as base material. On top of the substrate there is an additional, about 60 nm thin protection coating of SiO_2 to prevent oxidation or contamination of the Ge layer. Standard semiconductor processing methods can be used to precisely define both the Ge structures and the Al pads in the desired size, shape and position on the GeOI substrate.

Al-Ge-Al heterostructures commonly fabricated utilizing the thermal exchange reaction are based on VLS grown Ge NWs. In this method, the NWs are dispersed on a substrate with a thick dielectric layer. Since the orientation of the NWs after their deposition is random, the placement of the Al contacts with electron beam lithography is a complex and time consuming process [21, 66, 72]. The use of a GeOI substrate wafer is an approach to achieve wafer-scale fabrication of monolithic Al-Ge heterostructures without limiting the generality for parallel processing. It also allows to fabricate custom shaped structures since it is not limited to the rodlike structure of Ge NWs.

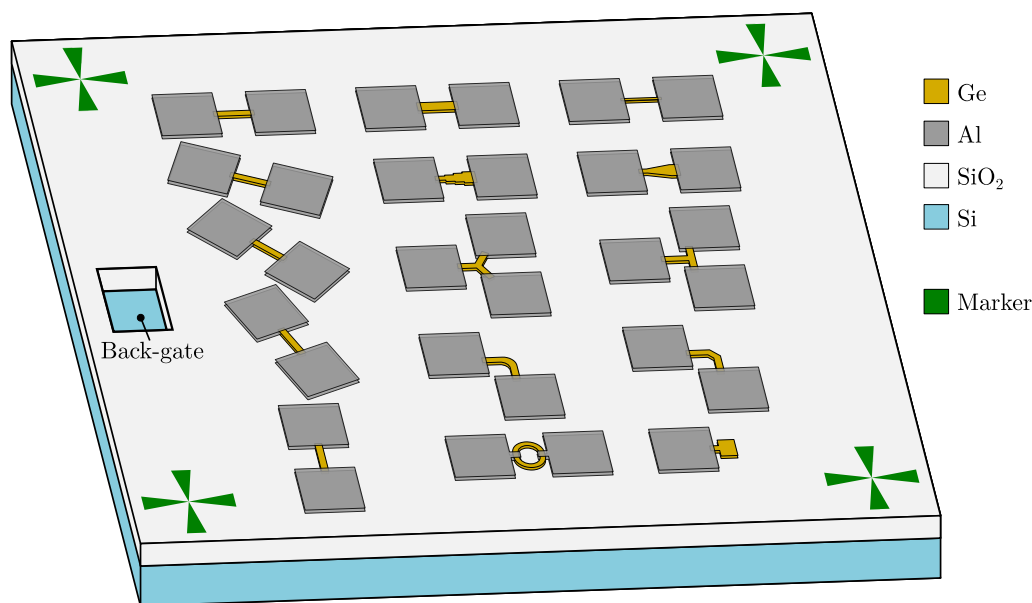


Figure 3.1: Schematic illustration of the GeOI based sample with Ge structures of different shapes and orientations, Al contact pads and alignment markers for lithography masks. A back-gate contact to the doped Si substrate for electrical measurements is also provided. Drawing is not in scale.

To study the thermally induced Al-Ge exchange reaction (see chapter 3.2) a variety of different Ge microstructures were produced. A schematic illustration of a GeOI based sample with structures in different shapes is illustrated in Figure 3.1. Straight rectangular shaped structures with a length of 10 μm and different widths and orientations on the

wafer are fabricated in order to observe the dependence of structure size and orientation of the exchange process. Further, different geometries like kinked, curved or branched wires and ring structures are created to monitor the propagation of the Al-Ge interface along complex structures.

With the available optical lithography technology in the cleanroom, a minimum feature size of approximately $2\ \mu\text{m}$ can be achieved. Each structure is contacted with Al pads, whereby each pad overlaps the ends of the Ge structure by $2.5\ \mu\text{m}$. These pads must be significantly larger in volume than the Ge structures since they serve as a reservoir for the thermal exchange reaction of Al and Ge. If the Ge concentration in Al reaches its solubility limit at about 1.69 at% [65] the exchange process would stop (see Chapter 2.3). These contacts will also be used later for electrical measurements to characterize the structures. The pad size was designed with $100\ \mu\text{m} \times 100\ \mu\text{m}$ with a thickness of 125 nm. The fabrication process is schematically illustrated in Figure 3.2. A more detailed process flow including the process parameters can be found in the appendix.

3.1.1 Fabrication of Ge Microstructures

Before the actual sample processing the protective SiO_2 capping of the GeOI wafer is removed by wet chemical etching using a buffered hydrofluoric acid (BHF). To define the structures on the Ge device layer an optical photolithography process is used for pattern transfer. First the image reversal photoresist (AZ5214) is spin coated onto the sample surface and then baked at 100°C for 1 min to harden the resist prior to exposure (3.2a). To improve the adhesion of the photoresist on the Ge surface a TI Prime adhesion promoter was used in a prior step, also spin coated and baked at 120°C for 2 min. A 1:1 Cr hard mask for the Ge device structures is then aligned and brought in contact with the coated sample using a mask aligner. The pattern is transferred to the wafer by exposing it with UV light for 3.5 s (3.2b). In this positive image process the exposed resist becomes soluble in the developer solution (AZ726MIF) while the unexposed parts are not dissolved and remain as an etching barrier.

Using RIE the Ge layer is etched according to the defined pattern (3.2c). This dry etching process allows both physical and chemical etching simultaneously. The reactive ions generated in a plasma are accelerated onto the substrate surface and create a sputtering effect while also chemically reacting with the material [73]. The RIE process with a mixture SF_6 (50 sccm) and O_2 (4 sccm) enables etching of Ge with high anisotropy, resulting in steep etching profiles. Process parameters were adjusted to achieve an etching rate of approximately $2.5\ \text{nm/s}$ and the SiO_2 layer below the Ge acts as an etch stop layer, preventing strong overetching. The photoresist is subsequently removed with acetone and isopropyl (3.2d).

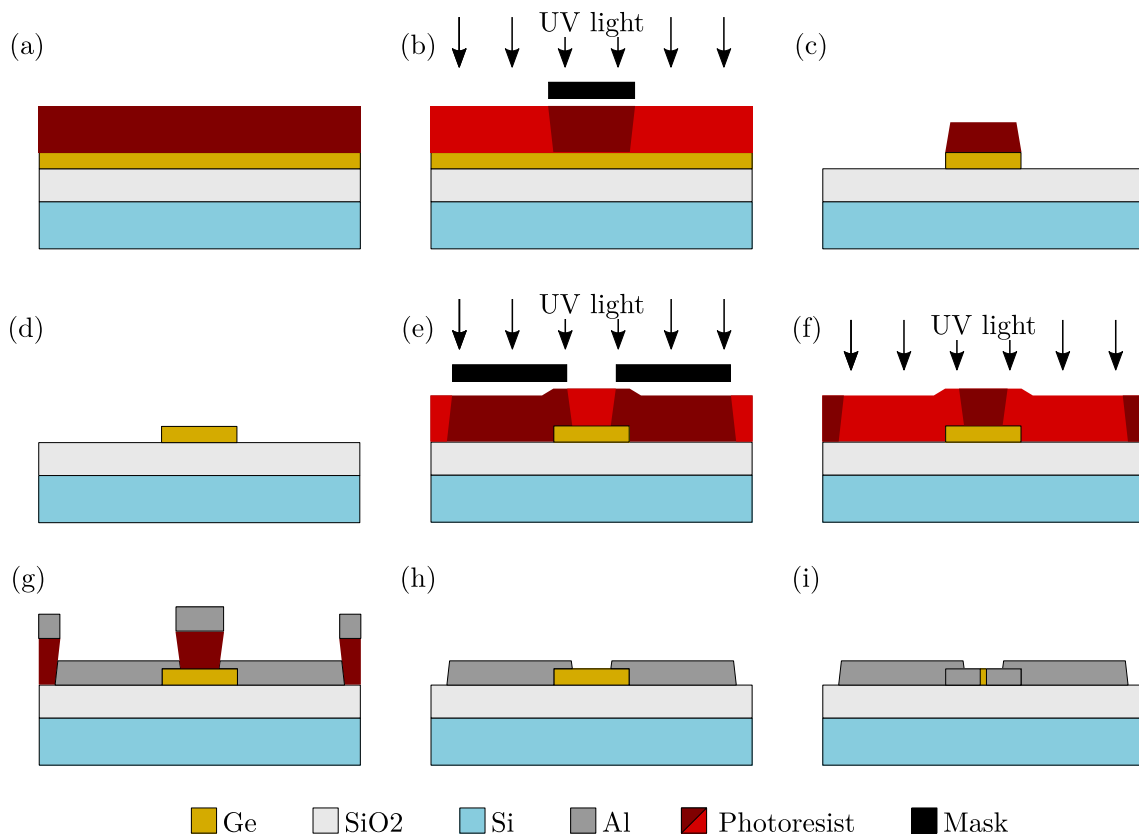


Figure 3.2: *Fabrication of monolithic Al-Ge heterostructures: (a) GeOI wafer with optical photoresist. (b) Pattern exposure with contact lithography. (c) Ge layer on the developed sample etched with RIE and (d) the resist is stripped. (e) For the fabrication of the Al contact pads the photoresist is exposed using a negative mask. (f) Reversal bake with subsequent flood exposure to invert the structure. (g) Al deposition for the contact formation. (h) The lift-off is performed in acetone. (i) Thermal Al-Ge exchange to form a short Ge channel.*

3.1.2 Al Contact Formation

In the following steps the Ge structures are contacted with macroscopic Al pads in a second photolithography process. This time an image reversal lithography process is used, which creates undercut resist sidewalls that are advantageous for a subsequent lift-off of the metal [74]. Similar to the positive process used for the Ge device structures the pattern for the Al pads is transferred with a contact mask to the spin coated and pre-baked sample by UV exposure of 4 s (3.2e). In a subsequent reversal bake of 60 s at 120°C the exposed areas of the resist lose their ability to develop while the unexposed parts remain photoactive [74]. A flood exposure (the entire sample is uniformly exposed to UV light) for 20 s is then performed to expose the yet unexposed resist areas so that they can be developed afterwards (3.2f).

To ensure intimate contact between the Ge structures and the Al pads, any GeO_x oxides naturally formed on the Ge surface are removed by dipping the sample in 14 % diluted hydroiodic acid (HI) for 5 s [75]. Using a sputtering process 125 nm Al is deposited on the sample (3.2g). For the subsequent lift-off the sample is soaked in acetone, dissolving the photoresist such that the excess Al can be removed easily (3.2h). This reveals the final Al-Ge microstructures.

3.2 Formation of Monolithic Al-Ge-Al Heterostructures with Thermal Exchange Reaction

To adjust the length of the Ge channel, the thermally induced exchange reaction is used. This technique can be used to create Ge devices with lengths in the nanometer range beyond limitations of optical lithography. The metal intrusion is induced by rapid thermal annealing in an "UniTemp UTP 1100" rapid thermal annealing (RTA) system. In the quartz chamber of this RTA oven the sample is heated to 400°C with 18 kW infrared lamps within 12 s. To avoid oxidation and other side reactions the process is carried out in a forming gas atmosphere (90 % N_2 , 10 % H_2), further improving process control. During the substitution process the abrupt metal semiconductor interface continuously moves along the structure, successively reducing the length of the Ge segment, as it is schematically shown in Figure 2.6. For exchange reactions of Al in Ge NWs under the given experimental conditions, average diffusion rates between 2.5 nm/s and 15 nm/s were experimentally observed, depending on temperature and NW diameter [66].

After each annealing step the devices are examined with a scanning electron microscope (SEM). The Ge segment lengths before and after one annealing step are compared for the calculation of the diffusion rates. The process is repeated until sufficient data points for the evaluation of the diffusion behavior with progressing diffusion are recorded and the desired Ge segment lengths are reached. To achieve short Ge devices in the region of the mean free path L_m for ballistic transport, consecutive thermal annealing steps accompanied by SEM imaging for good process control are necessary.

3.3 Fabrication of Nano-Scaled Structures on GeOI

To reduce the size of the Ge structures beyond the limits of optical lithography, electron beam lithography (EBL) and a subsequent etching process was used to reduce the lateral size of the structures. Thus, also the shape can be modified to achieve more complex structures with features in the nanometer range. Further, wet chemical etching was applied to reduce the structure size in all dimensions, both laterally and foremost the thickness of the Ge layer.

3.3.1 Electron Beam Lithography

EBL is an advanced fabrication technique to transfer patterns with nanometer feature sizes. In the direct writing system, an electron beam is focused onto a resist-covered substrate, directly writing the pattern without the need of an additional hard-mask. Its very short wavelength allows the fabrication of devices with critical dimensions as small as 10 nm. Since EBL is a sequential process it is comparatively slow, with typical operation times of several hours [76].

Similar to optical lithography EBL also suffers from proximity effects as backscattered electrons can travel a few tenths of a micron, also exposing photoresist at nearby features. This leads to modification of the desired pattern such as rounded corners or changed line widths, limiting the exposure resolution of EBL and impeding the fabrication of nano-scale features [77].

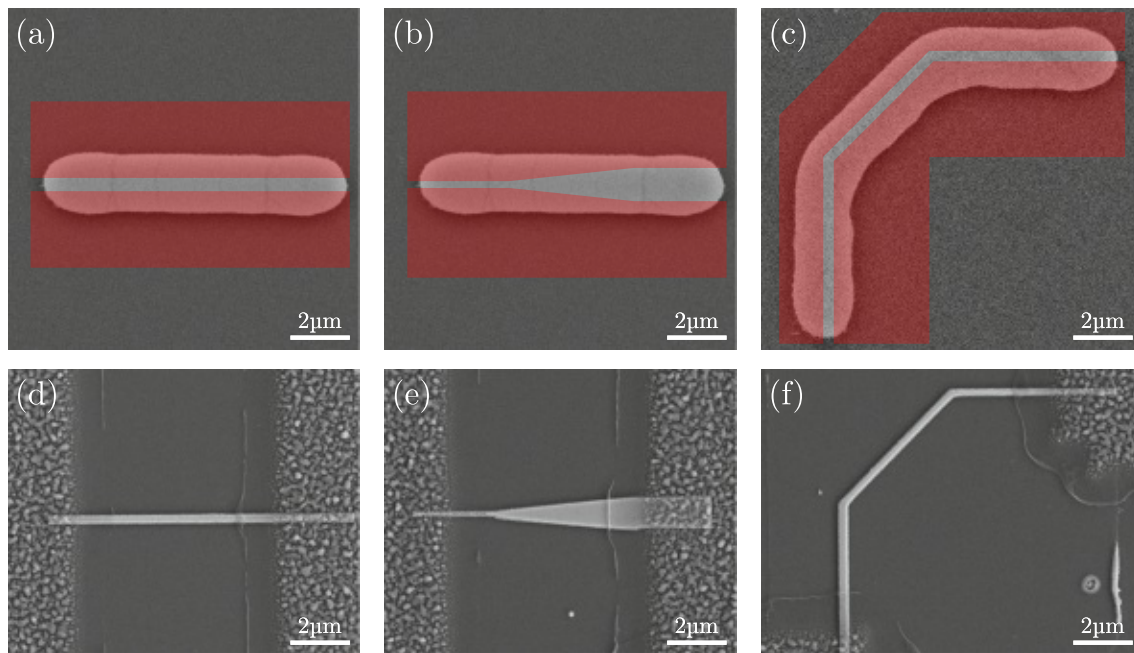


Figure 3.3: SEM images of Ge structures before and after the EBL process. (a-c) With EBL etching windows (red) are defined on the pre-defined Ge structures. Subsequent RIE removes the Ge inside these windows. The remaining narrow structures are then contacted with Al pads (d-f).

To fabricate nano-scaled Ge structures a mix and match approach is used. A sample with yet uncontacted microstructures defined by optical lithography and RIE is processed using EBL and again RIE to reduce the size of the structures to nanometer dimensions. As the Ge layer is already pre-structured, the writing process of the EBL can thus be considerably shortened, since only small etching windows need to be defined. For this purpose, a pattern

is defined and aligned with the existing structures (see Figure 3.3a-c). These windows are exposed by the focused electron beam, becoming soluble for the developer and accessible for the etchant, resulting in ultrascaled Ge nanostructures. More complex shapes and additional structural features can also be added due to the much higher resolution. Taking into account the proximity effect, the gap spacing of the EBL mask was designed slightly larger than the desired width of the final structure, especially for narrow devices. Due to the scattering of the electrons, the actual exposed windows are slightly enlarged. Thus, structure widths of 400 nm on the mask have resulted in final widths even below 100 nm.

For the EBL process the sample is spin-coated with PMMA resist (AR-P 679.04), baked at 170°C for 600 s and loaded into the vacuum chamber of the EBL system. After the patterning process the exposed resist is dissolved in a proper developer solution (AR 600-56) for 35 s and then immersed in the stopper solution (AR 600-60). Thus, obtained typical Ge nanostructures contacted with Al pads are shown in Figures 3.3d-f.

3.3.2 Ge Layer Thinning by Wet Chemical Etching

An approach to reduce the thickness of the Ge structures is selective wet chemical etching. Using a diluted solution of hydrogen peroxide and water ($\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:10$), etch rates between 12.5 nm/min and 40 nm/min are expected [75, 78]. For the actual processing a rather slow etching rate was chosen to ensure sufficient process control and to achieve uniform structures. Since Al is hardly attacked by this solution [79], the procedure can also be applied to the fully featured device i.e. after the contact formation and Al-Ge exchange. To measure the dimensions of the structure after the chemical treatment an atomic force microscope (AFM) is used. This imaging method allows high resolution measurements of the sample surface, providing detailed information about the dimensions in all three dimensions. By alternating etching and AFM measurements the thickness of the Ge structures can be reduced in a well controlled and reliable manner. The influence of the device thickness on electrical properties was determined by electrical measurements after each individual etching step.

3.4 Fabrication of Freestanding Al-G-Al Heterostructures

To further show the versatility of the heterostructure formation methodology, suspended Al-Ge-Al structures are fabricated. This is achieved by undercutting a Ge structure with a subsequent annealing process.

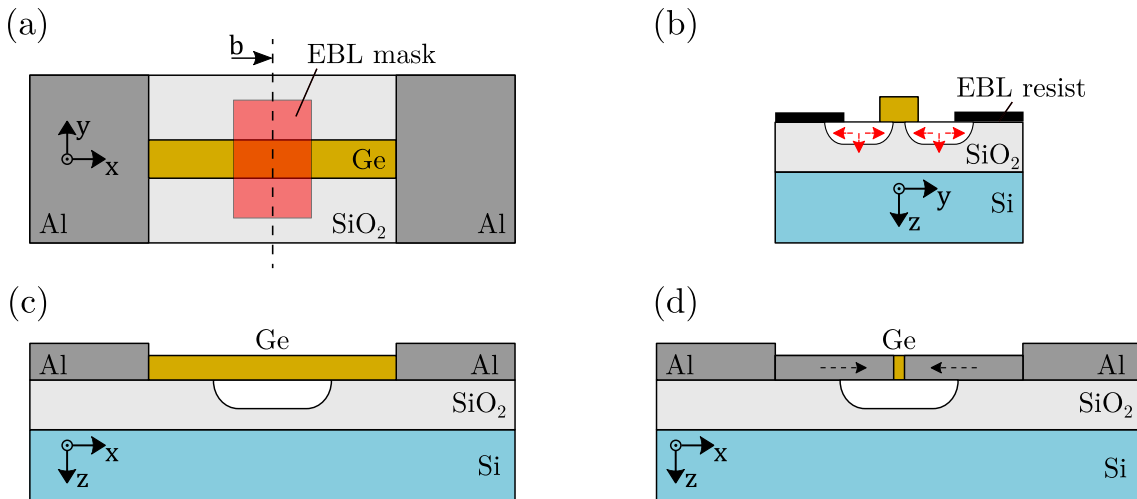


Figure 3.4: Schematic illustration of the fabrication steps to achieve a freestanding Al-Ge-Al heterostructure. (a) With EBL an etching window is defined. (b) With isotropic wet chemical etching SiO₂ is removed underneath the Ge beam, (c) finally resulting in a freestanding structure. (d) With subsequent RTA a suspended Al-Ge-Al heterostructure with a short Ge channel is formed.

The SiO₂ underneath the Ge structure is removed by wet etching with BHF. While Ge is resistant to this acid, Al is strongly attacked [79, 80]. Therefore, the etching process has to be performed before the Al-Ge exchange reaction and the Al contact pads have to be covered by a mask. Using EBL a rectangular etching window is defined in the middle of the Ge structure, with sufficient distance to the Al contact pads (see Figure 3.4a). Due to the isotropic etching behavior of BHF, the oxide is also etched in lateral direction (3.4b). With increasing progress, the resistant Ge layer is eventually completely undercut, resulting in a freestanding structure (3.4c). By subsequent thermal annealing a short Ge segment within the suspended part of the wire structure is formed (3.4d).

3.5 Electrical Characterization

For the electrical characterization of the fabricated Al-Ge-Al heterostructures a needle probe station in combination with a semiconductor analyzer (Keysight 4156B or B1500A) is used. The needle probe station is equipped with four independent low-noise source measure units (SMUs) which can be precisely placed on the Al contact pads using an optical microscope. A schematic illustration of the measurement setup for the electrical characterization is shown in Figure 3.5. The structures on the GeOI resemble FET devices with the p-doped Si substrate used as a back-gate and the two Al pads used as drain and source contacts. To achieve a back-gate contact, the SiO₂ layer is locally removed by carving or etching to make it accessible from top. The SMUs control the voltages applied to the structure while precisely measuring the current, with resolutions in the μV and fA range. The maximum currents were limited in order to avoid damaging the structures. All measurements are performed in ambient atmosphere at room temperature. To avoid influences of light and radiation the probe station is placed in a dark box.

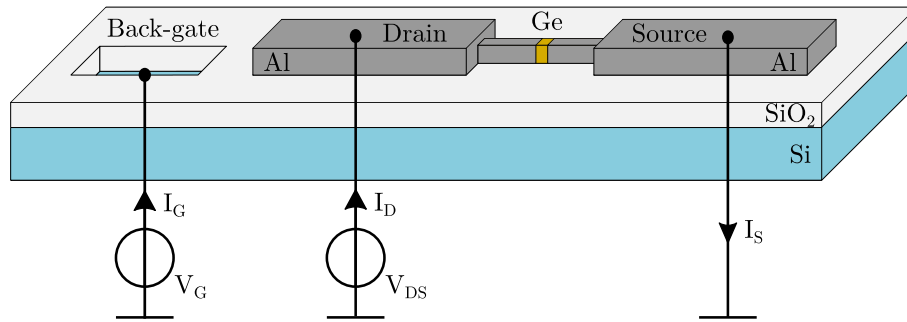


Figure 3.5: Schematic illustration of the measurement setup for the electrical characterization of Al-Ge-Al heterostructures resembling a FET device. The macroscopic contacts are accessed from the top using a needle prober. The doped Si substrate is used as a global back-gate.

3.5.1 I/V Characteristics

For the basic I/V characterization the voltage between drain and source (V_{DS}) is varied while the current is recorded with the back-gate fixed, typically at 0 V. This gives information about the resistivity and the contact properties of the fabricated structures. Nonlinear behavior of the structures is expected due to the Schottky barriers formed at the metal-semiconductor (Al-Ge) interface on each end of the Ge segment. The curve, linearly fitted around the zero point, allows an estimation of the resistance $R = \Delta V / \Delta I$. The specific resistivity of the structure is calculated with

$$\rho = R \cdot \frac{A}{L}, \quad (3.1)$$

by considering the cross-section A and the length L of the Ge channel. The resistance of the Al segments and contact pads can be neglected due to the much higher resistivity of Ge [4, 81]. Depending on the dimensions of the heterostructure, the range of the voltage sweep has to be adopted, with typical ranges from ± 20 mV for short channel devices with large cross sections up to ± 1 V for thin structures with long Ge segments. An adequate suitable step size is chosen to obtain sufficient resolution.

3.5.2 Transfer Characteristics

The fabricated Al-Ge-Al heterostructure resembles a SB-FET with the p-doped Si substrate underneath, basically acting as a global back-gate. By applying a voltage to the back-gate, the carrier concentration and therefore the carrier transport through the Ge channel can be controlled. To examine the electrostatic modulation capability the transfer characteristic is recorded. This is done by sweeping the voltage applied to the gate (V_G) and measuring the current flow I_D through the structure while V_{DS} is fixed to a certain value. The gate voltage can be varied in a wide range up to ± 80 V due to the high dielectric strength of the SiO_2 layer underneath (~ 10 MV/cm [34]). For freestanding structures the maximum gate voltage has to be lowered since the thickness of the isolating oxide was reduced, resulting in a lower breakdown strength. By linearly sweeping V_G in both directions (-30 V to 30 V and back to -30 V) hysteresis characteristics are measured to investigate the influence of surface traps.

Chapter 4

Results and Discussion

The first part of this chapter is dedicated to the morphological characterization of the fabricated devices using different analysis techniques like SEM, transmission electron microscopy (TEM), electron dispersive X-ray spectroscopy (EDX) and electron backscatter diffraction (EBSD). The influence of structure size, geometry and orientation on the thermal induced Al-Ge substitution process are investigated. Further, I/V and transfer characteristics are measured to determine the electrical properties of the formed Al-Ge-Al heterostructures. Subsequently, the influence of surface traps and ballistic transport in an ultrascaled Ge channel device are analyzed and discussed. Furthermore, the reduction of the cross-section of the Ge segments using a wet chemical treatment is presented. Finally, the fabrication of freestanding Al-Ge-Al heterostructure nanobeams is demonstrated.

4.1 Analysis of the Al-Ge Substitution Process

Until now, the Al-Ge exchange process has only been demonstrated in VLS grown NWs. To prove that the process is also feasible for a patterned GeOI substrate with a $\langle 100 \rangle$ oriented and 75 nm thick Ge device layer, basic structures with simple geometries were examined at first. Figure 4.1a shows the SEM image of a straight 320 nm broad Ge structure with a length of 10 μm , that was patterned using optical lithography and subsequent RIE. The Ge bar is contacted at both ends with two macroscopic Al pads separated by 6 μm . When the sample is heated to 400°C using RTA, the Al from the overlapping contact pads penetrates the Ge structure while the Ge atoms diffuse into the Al reservoirs. Figure 4.1b,c show that, after several annealing steps, more and more Ge is replaced by Al. This causes the metal-semiconductor interface to migrate further inwards and successively reduce the length of the Ge channel, from $L_{\text{Ge}} = 1690 \text{ nm}$ after 300 s to 850 nm after 400 s. Due to the high chemical contrast of the unreacted monocrystalline Ge (bright) and the pure Al emerging from the contacts (dark), the respective metal and semiconductor segments are clearly distinguishable in the SEM. As can be seen in Figure 4.1c, the formed Al-Ge interface is not always entirely flat. Especially for wide structures in the micrometer range oblique or curved diffusion fronts are formed frequently.

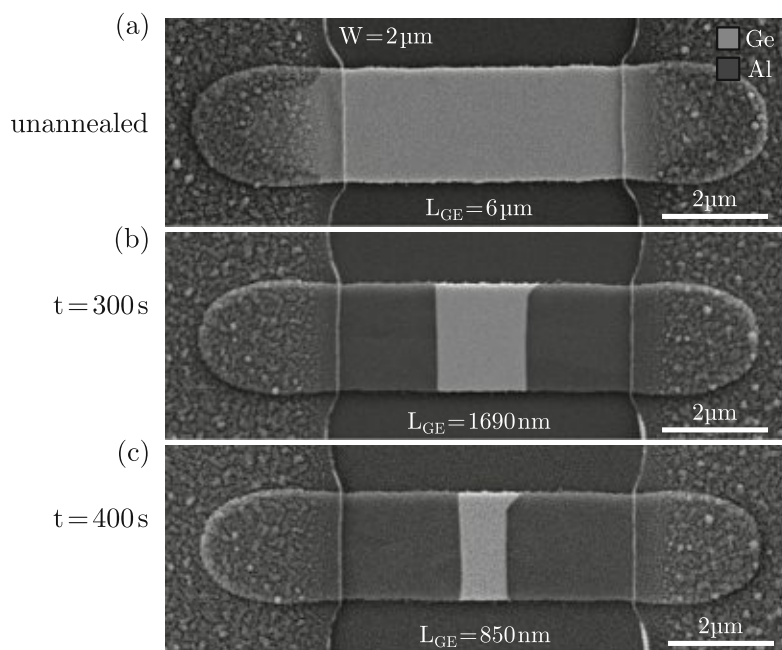


Figure 4.1: Sequence of SEM images showing the formation of an Al-Ge-Al heterostructure. Starting from a pure 2 μm wide Ge structure between two Al pads separated by 6 μm (a) the Ge channel is successively reduced to $L_{\text{Ge}} = 1690 \text{ nm}$ after 300 s (b) and a final length of $L_{\text{Ge}} = 850 \text{ nm}$ after 400 s (c).

To investigate the Al-Ge interface and the elemental composition of the structure in more detail, analyses using TEM and EDX were performed. Figure 4.2a shows a cross section along the entire Al-Ge-Al heterostructure with the 150 nm thick BOX and the Si substrate underneath. The EDX measurements in Figures 4.2b,c show the elemental composition of the structure. Besides the Ge channel (marked in yellow) between the two Al lines (green) no intermetallic phases are detected. Based on extensive TEM studies on Al-Ge exchange for VLS grown Ge NWs [25], it can be assumed that the Al propagation is caused by Ge diffusion via surface channels on the Al to the extended contact pads. The Al replacing the Ge is provided via effective Al self-diffusion [22]. Only small traces of Ge are found inside the Al leads, indicating a complete replacement of the Ge by the Al during the thermal exchange reaction. This can be addressed to the low solubility of the materials in each other. Furthermore, no Al contamination of the remaining Ge segment was detected due to the extremely low diffusion coefficient of Al in Ge [21]. A thin oxide shell is formed on top of the structure (see red indicators in Figure 4.2b), which was also found in the exchange of VLS grown Ge NWs [22].

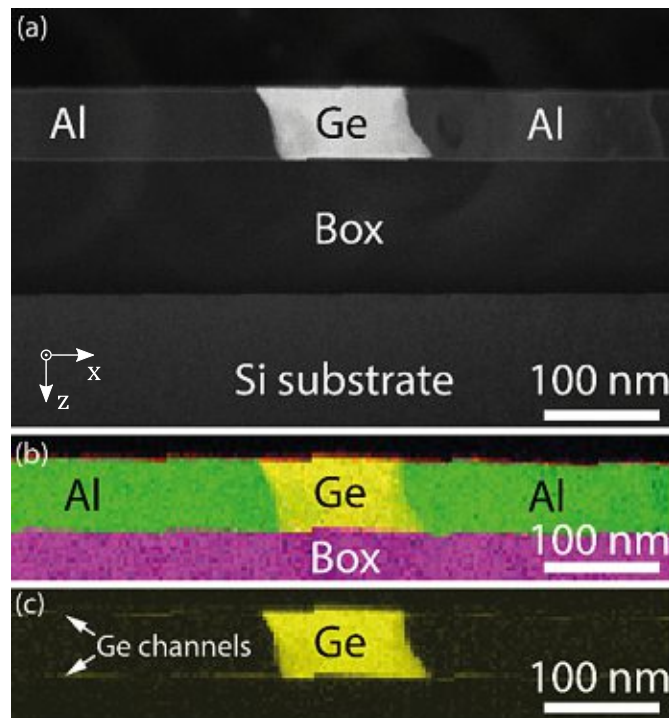


Figure 4.2: (a) TEM image of the entire Al-Ge-Al heterostructure. (b) The EDX mapping shows the elemental composition of the formed heterostructure (Ge: yellow, Al: green, O: red, Si: purple). (c) EDX image shows Ge around the Al part of the heterostructure, indicating that Ge diffuses through surface channels into the Al Pads.

A cross-sectional high-resolution TEM image of the Al-Ge interface shown in Figure 4.3a reveals the abrupt interface formed by the substitution process. The brighter segment on the right indicates the substituted Al-part and the darker region corresponds to the unreacted Ge core separated by an almost atomically sharp interface. The most prominent lattice plane of the Al-Ge interface is oriented in the (111) direction. The enlarged view in the HRTEM image in Figure 4.3b shows the sharp Al-Ge junction and the crystal structure of the two adjacent materials. Differences in the lattice constants and crystal orientations of Ge on the left side and Al on the right side can be seen.

With local Fast-Fourier-Transformation (FFT) of the two segments a more detailed information of the crystal structure can be obtained. The FFT pattern for Ge and Al are shown in Figure 4.3c and 4.3d, respectively. Both crystal structures are identified as fcc, with a lattice constant $a = 5.65675 \text{ \AA}$ and space group 227 (ICSD 43422) for the Ge part and $a = 4.04975 \text{ \AA}$ and space group 225 (ICSD 43423) for Al. The FFTs reveal that the interface is composed of a Ge {111} and an Al {200} facet. Both crystals are oriented in a [110] zone axis with a mutual in-plane rotation of 6.5° . This rotation presumably leads to strain minimization and lattice relaxation to accommodate lattice mismatch [25]. On the Ge side of the interface, a Moiré pattern can be observed (see upper left corner of Figure 4.3b), originating from overlapping Al and Ge grains due to an inclination of the interface to the electron beam direction.

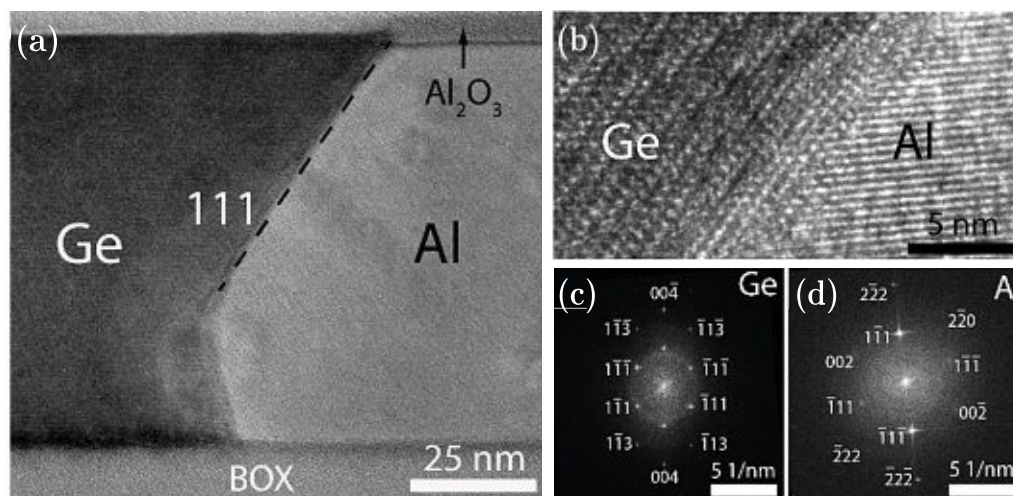


Figure 4.3: (a) TEM and (b) HRTEM image of the Al-Ge interface revealing an abrupt metal-semiconductor heterojunction. (c) and (d) show the indexed FFT pattern with [110] zone axis for Ge and Al segments, respectively.

4.1.1 Influence of Geometry on the Al-Ge Substitution Process

To determine the influence of the geometry of the Ge pattern on the exchange process, structures with different widths are fabricated using EBL. Figure 4.4 shows successive annealing cycles of such structures, with widths ranging from $4\ \mu\text{m}$ to $40\ \text{nm}$. All these illustrated structures are based on the $4\ \mu\text{m}$ wide Ge bars in Figure 4.4a and have been reduced to the respective dimensions with additional EBL and RIE processing steps.

Examining the substitution progress in the individual structures after the same annealing duration, a clear difference in the length of the remaining Ge segment can be detected. While after 60 s a considerable amount of Ge has already been exchanged in thinner structures (4.4c-f), the diffusion front in the wider structures (4.4a,b) is still largely located below the contact pad. A distinct difference in length of the Ge channel is also noticeable after 270 s, with much shorter Ge segments for thinner structures. After further 140 s of annealing, the Ge in the narrow structures (4.4c-f) is completely replaced and wires of pure, crystalline Al are thus formed. Due to the lower Al-Ge exchange rate in wider structures, short, not yet replaced Ge segments remain, with Ge channel lengths of $840\ \text{nm}$ in (4.4a) and $150\ \text{nm}$ in (4.4b). With long annealing processes it is possible to completely exchange wide structures to obtain crystalline Al pads.

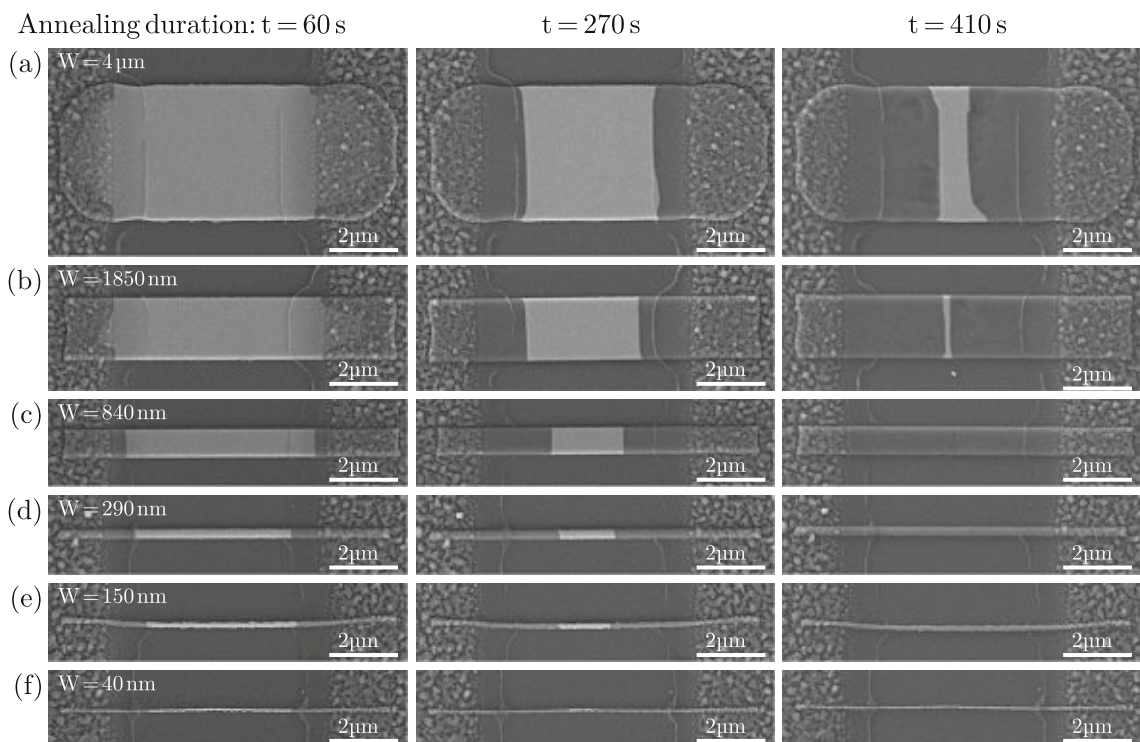


Figure 4.4: SEM images showing the annealing progress in structures of various widths of (a) $W = 4\ \mu\text{m}$, (b) $W = 1850\ \text{nm}$, (c) $W = 840\ \text{nm}$, (d) $W = 290\ \text{nm}$, (e) $W = 150\ \text{nm}$ and (f) $W = 40\ \text{nm}$.

To investigate the morphology of the formed Al-Ge heterostructures electron backscatter diffraction (EBSD) measurements were performed. Figure 4.5 shows the EBSD mapping on top of SEM images for representative structures with widths between 4 μm and 250 nm. The formed Al segments for the wider structures appear to be polycrystalline with grain sizes in the μm range. The individual grains are colored according to their crystal orientations using the scale on the lower left. The not yet reacted Ge segment retains its initial $\langle 100 \rangle$ orientation. The number of individual grains decreases for narrower structures. Structures with widths below 400 nm tend to form monocrystalline Al segments during the Al-Ge exchange reaction. Thus, long annealing processes in narrow Ge structures lead to pure Al lines consisting of two monocrystalline segments with the grain boundary at the location where the diffusion fronts from both sides merge. This is shown in Figure 4.5d, with the two monocrystalline segments marked blue and green.

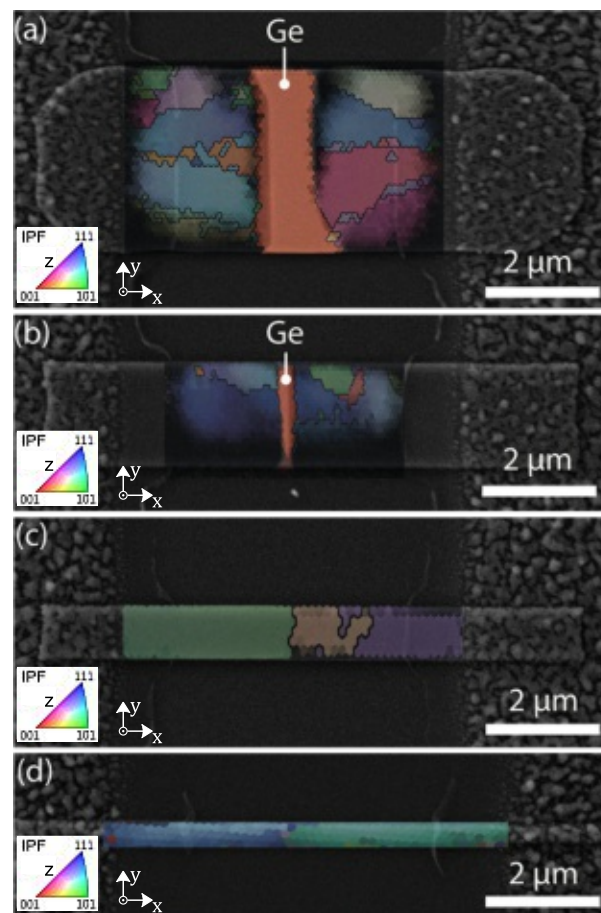


Figure 4.5: SEM images with overlaid EBSD maps of annealed structures for crystallographic analysis. The structures (a) and (b) show a short Ge segment (orange), while (c) and (d) are fully exchanged crystalline Al structures. The color scale indicates the crystal direction of the grains.

An evaluation of the Al-Ge exchange process over time by repetitive annealing steps was performed to investigate the kinetics of the thermally induced exchange reaction. Therefore, the length of the formed Al leads was determined after each annealing step using SEM imaging. The ramping up of temperature lasting about 10s was not considered in the evaluation, since the rate is significantly lower for temperatures below 400°C. Figure 4.6 shows the averaged length of the formed Al leads over time for different structures with an average width of 150 nm, 310 nm, 870 nm and 1800 nm within a range of about ± 50 nm. The variation of the formation lengths is indicated by error bars. Note that at an Al length of about 3 μm all the Ge in the structure has been replaced as the 6 μm long Ge bar between the two Al pads is substituted from both sides. The progress of the Al growth can be well fitted with a square root function (\sqrt{t}) for all widths. This is consistent with observations for VLS grown NWs, which also showed parabolic growth behavior [22]. As already indicated in Figure 4.1, narrow structures achieve a higher annealing rate, especially at the beginning of the substitution process. However, the width dependence of the rate decreases with increasing process duration.

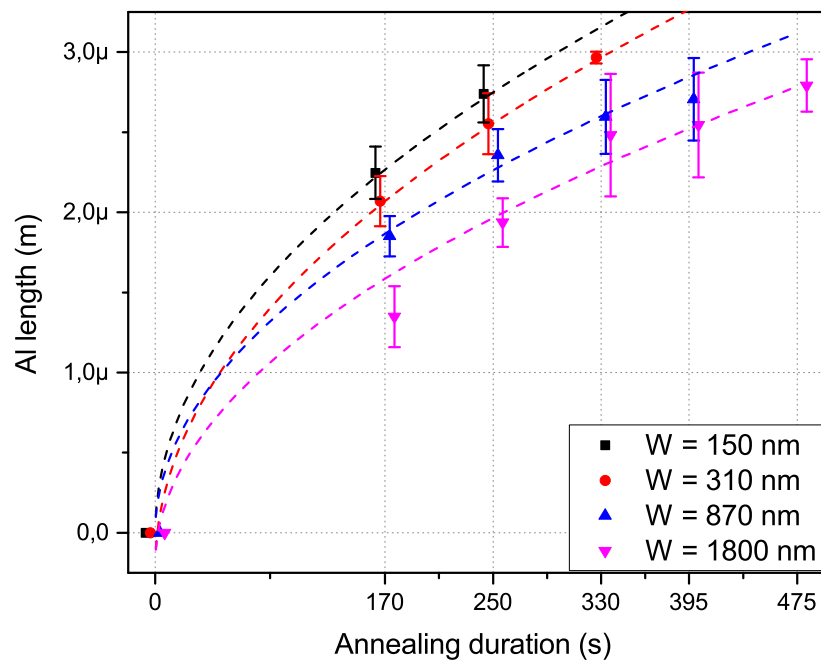


Figure 4.6: Progress of the Al formation over the annealing duration for Ge beams with different widths between $W = 150$ nm and $W = 1800$ nm, indicating a \sqrt{t} dependence of the Al length over time (dashed lines for \sqrt{t} fit). The heating process with the duration of 10 s was subtracted from the total process time.

A more detailed analysis of the Al-Ge exchange rate for the first annealing step (170 s) related to the width of the individual structures is shown in Figure 4.7, with a fitting curve indicating a $1/\sqrt{W}$ dependence. According to the observations of the EDX analysis in Figure 4.2 and an Al formation length proportional to $\sqrt{t/W}$, it can be assumed that the Al-Ge exchange reaction rate is limited by the Ge diffusion along the surface channels (see Table 2.1). It is also evident that the exchange rates are widely spread even for structures of similar widths, which makes it difficult to produce short Ge channels on many structures simultaneously. These variations may be associated with the quality of the interface between the Al reservoir and the Ge structure or to surface variations resulting from the subtractive nature of the top-down fabrication scheme using RIE [19].

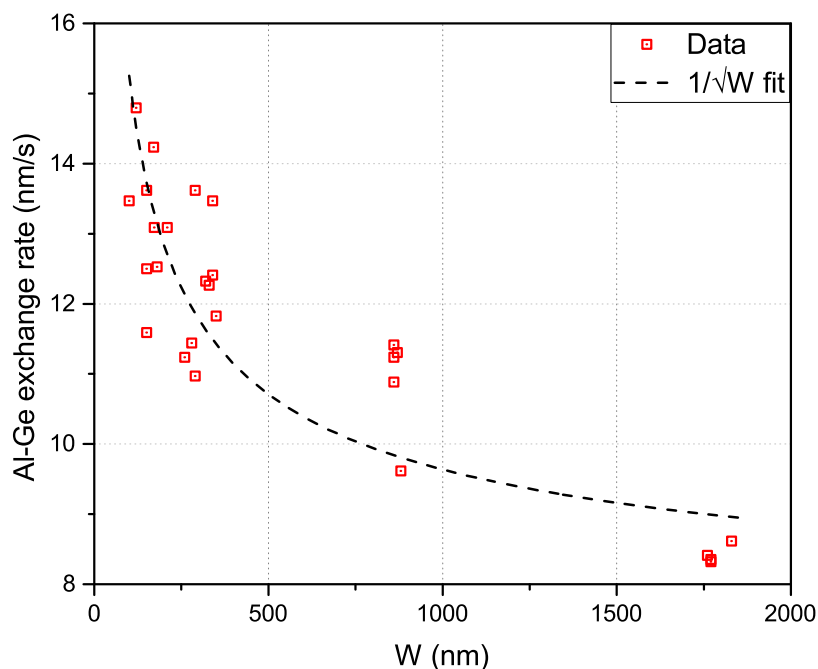


Figure 4.7: Al-Ge exchange rate for structures with different widths between $W = 150$ nm and $W = 1800$ nm for the first annealing step. It shows a significant dependence of the structure width, which can be fitted using a $1/\sqrt{W}$ function.

4.1.2 Influence of the Crystal Orientation on the Al-Ge Substitution Process

For the investigation of an influence of the Al-Ge exchange on the crystal orientation Ge structures with different orientations were fabricated and contacted with Al pads on the (100) device layer of the GeOI substrate. Starting from an original $\langle 110 \rangle$ orientation the structures are rotated in steps of 22.5° to $\langle \bar{1}10 \rangle$. Figure 4.8 shows the rotated structures after 320 s of RTA. A closer look at the Al-Ge interfaces shows that the diffusion fronts are not always oriented perpendicular to the structural direction. However, even in the rotated structures, interface planes parallel to (110) or $(\bar{1}10)$ are preferably formed.

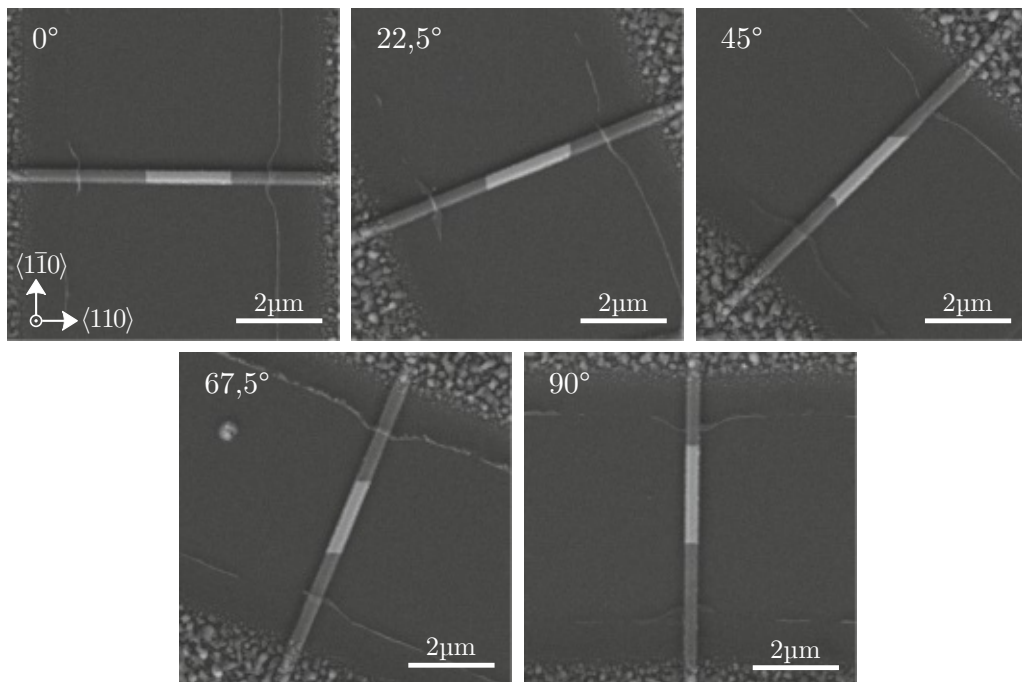


Figure 4.8: SEM images showing annealed structures with different orientations on the substrate, rotated in steps of 22.5° from the $\langle 110 \rangle$ (0°) to the $\langle \bar{1}10 \rangle$ direction (90°). $\{110\}$ interfaces are preferably formed.

In Figure 4.9 the Al-Ge exchange rates for structures in different orientations with $W = 300$ nm are analyzed for annealing durations of 90 s and 140 s. The statistical variance of the rate is indicated by error bars. In accordance to similar investigations concerning the nickel silicidation of top-down fabricated Si NWs [82], no significant dependence of the Al-Ge exchange rate on the crystallographic orientation beyond statistical variations was observed. This allows a wafer-scaled fabrication of differently oriented Al-Ge-Al heterostructures with similar Ge channel length.

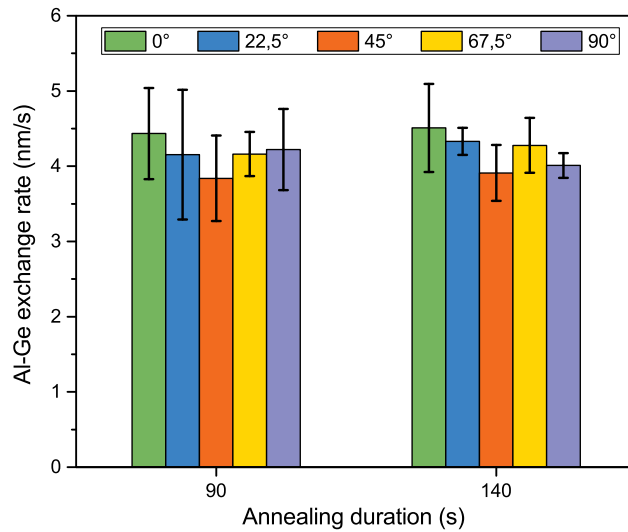


Figure 4.9: The graph shows the average Al-Ge exchange rate (rectangular bars) and its statistical variance (error bars) for different oriented structures and annealing durations of 90 s and 140 s. No significant dependence on the orientation beyond statistical variation can be observed.

4.1.3 Substitution Process in Irregular Ge Structures

In contrast to other studies where the Al-Ge heterostructure formation process was observed in intrinsically rodlike VLS grown NWs, the structures patterned on the GeOI substrate are not limited to straight lines. Figure 4.10 shows successive annealing cycles on various irregular structures with more complex geometries.

For the tapered structures shown in (4.10a) and (4.10b) the width of the Ge structure is stepwise or continuously reduced from 1100 nm down to 250 nm, respectively. Thereby the formed Al segments are adapting to the size variation of the structure. The SEM image in (4.10c) depicts a kinked structure with $W = 300$ nm connecting two Al pads displaced by 90° . The Al diffuses along these structure, preferably forming interfaces in (110) or $(\bar{1}10)$ direction, similar to the previous observations in the rotated structures. Finally, after 960 s a Ge segment in the angled part of the structure is formed. Similarly, the Al-Ge exchange proceeds in the curved structure shown in Figure 4.10d. A tripod structure connecting three Al reservoirs is shown in (4.10e). The Ge is successively replaced from all directions, forming Al-Ge-Al heterojunctions between all three contact pads. Due to variations in length of the individual leads or fluctuations in the exchange rates, a short Ge channel in one leg is formed after 710 s, leading to a connection of pure crystalline Al of the other two pads.

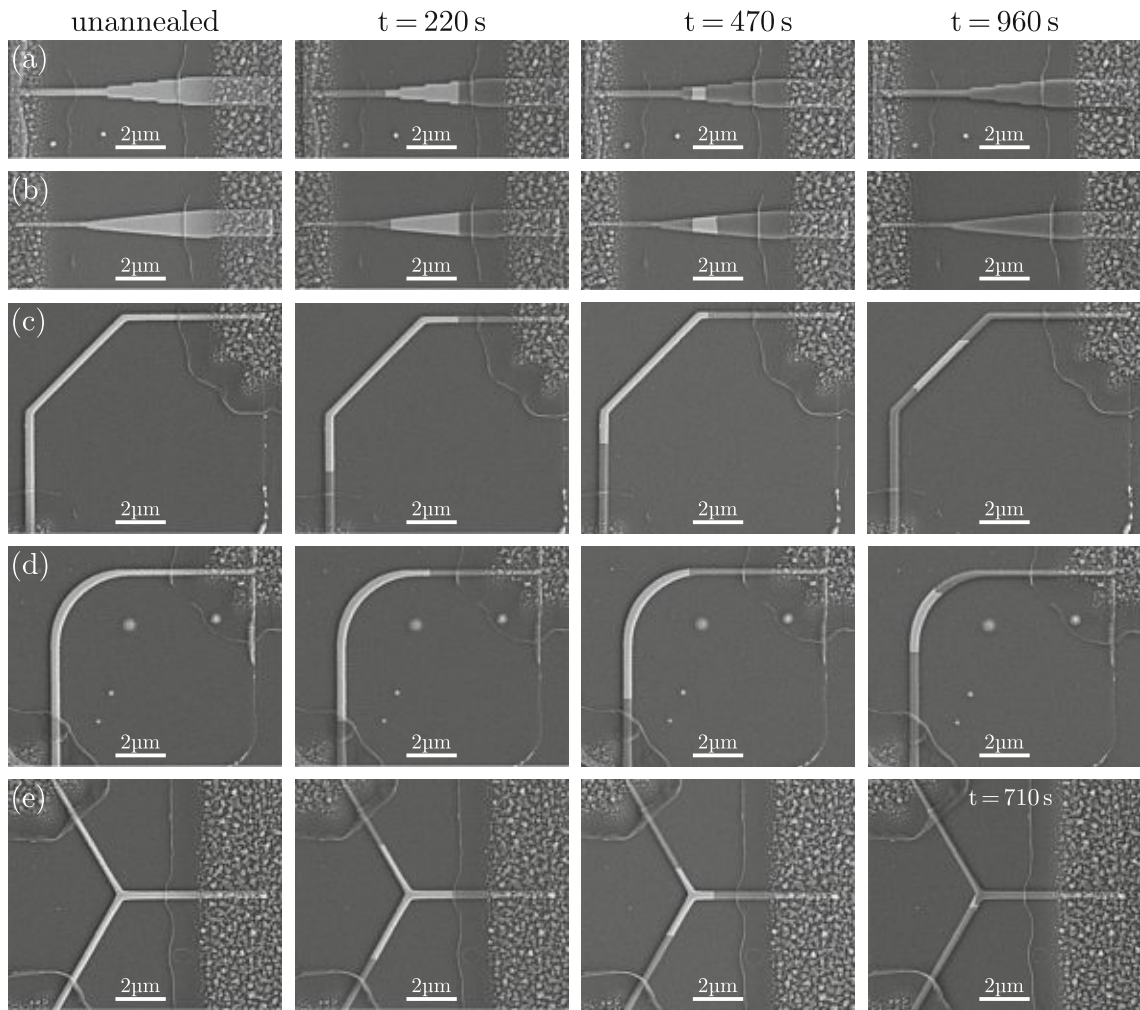


Figure 4.10: SEM images showing the Al-Ge exchange temporal progress in various irregular structures, including a stepped (a) and continuously tapered (b), kinked (c), curved (d) and tripod structure (e).

Using EBL it is also possible to create cavities or gratings in the Ge structures. The course of the thermal exchange process around this pattern can thus be observed. Figure 4.11 shows a double tapered structure with two rectangular recesses after RTA for 200 s. The substitution progresses around the recesses and a short Ge channel with abrupt interfaces is formed in the middle of the 215 nm wide strip.

Figure 4.12 shows two wide area structures with a narrow inlet that indicate the preferred directions for the Al formation process in Ge structures. Initially, the Al progresses through the 300 nm thin inlet and is then free to spread across the 4.5 μm broad Ge structure. As can be clearly seen in (4.12a) and in many other structures, the exchange is preferred in

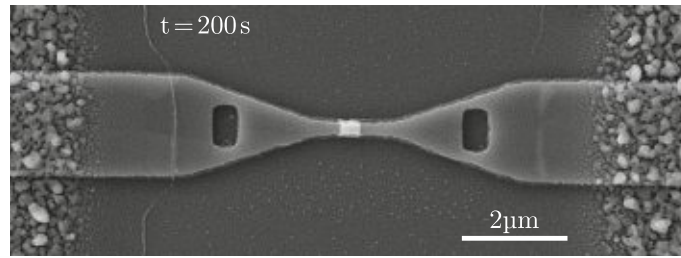


Figure 4.11: SEM image of a double tapered structure with two rectangular recesses. The Al-Ge exchange progresses around the cutouts and a short Ge channel with sharp interfaces is formed within the thin part of the structure, with $W = 215 \text{ nm}$ and $L_{Ge} = 240 \text{ nm}$.

the $\langle 110 \rangle$ directions. An exchange in $\langle 100 \rangle$ directions can also be observed regularly, as it is seen in Figure (4.12b). The different progress of the Al-Ge exchange in the broad part of the two structures with the same process duration can be explained by the different lengths of the narrow feed lines. Therefore, the directional exchange in structure (4.12a) was started with a slight delay with respect to structure (4.12b).

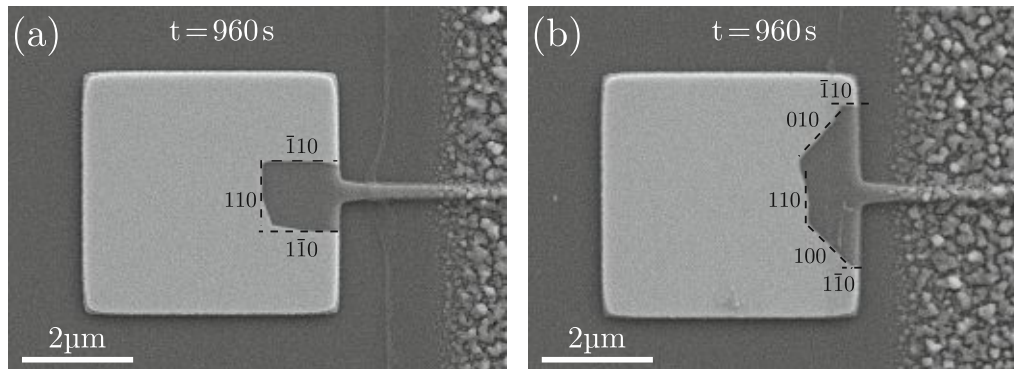


Figure 4.12: SEM image of a step structure, with a wide area structure with $W = 4.5 \mu\text{m}$ and a thin inlet of $W = 300 \text{ nm}$. It can be seen that in the wide area the Al-Ge exchange is preferred in $\langle 100 \rangle$ and $\langle 110 \rangle$ directions.

The heterostructure formation process is also possible in narrow Ge ring structures contacted by two Al reservoirs, as it is shown in Figure 4.13. After thermal annealing for a sufficiently long time, short Ge segments can be formed on both sides of the ring. Since the structure to be exchanged is significantly longer than the ones shown above, very long segments are still present even after $t = 960 \text{ s}$. Fabricating a uniform structural width of the entire ring with two similarly long Ge channels can be quite challenging and will require very elaborate process control.

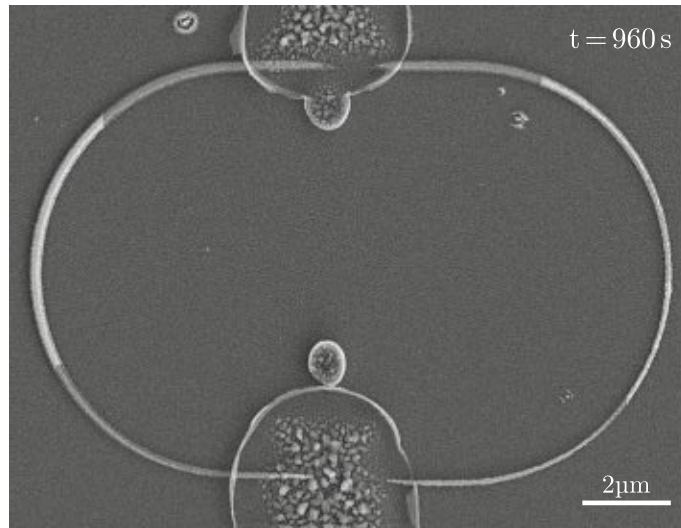


Figure 4.13: SEM image of an elliptical Ge structure, partly exchanged by Al after RTA for 960 s.

Such structures could possibly be used as tunable superconducting quantum interference devices (SQUIDS), which are the most sensitive detectors of magnetic fields [83]. When the structure is cooled below the critical temperature of $T = 1.2\text{ K}$, the Al becomes superconducting and Ge acting as a tunable semiconducting barrier. This superconductor-semiconductor transition is called a Josephson junction [66]. A superconducting loop separated by two Josephson junctions is suitable to detect changes in magnetic flux smaller than the flux quantum [83].

4.2 Electrical Characteristics of Monolithic Al-Ge Heterostructures

To investigate the electrical properties of the Al-Ge-Al heterostructures, numerous measurements were carried out. In I/V measurements and transfer characterizations, the effects of structure width and Ge channel length in different devices were compared.

4.2.1 I/V Characteristic

The I/V characteristic provides important information about the resistivity and the contact properties of the fabricated Al-Ge heterostructures. To determine how the exchange reaction affects these properties, measurements were conducted before and after thermal annealing. Figure 4.14 shows the comparison of the basic I/V characteristic before (red) and after the annealing (blue), where the Ge segment of a $2\ \mu\text{m}$ wide structure was reduced from $5.8\ \mu\text{m}$ to $1.5\ \mu\text{m}$ by RTA for five minutes at 400°C . After heterostructure formation, the resistance of the device is significantly lowered by a factor of about 15.

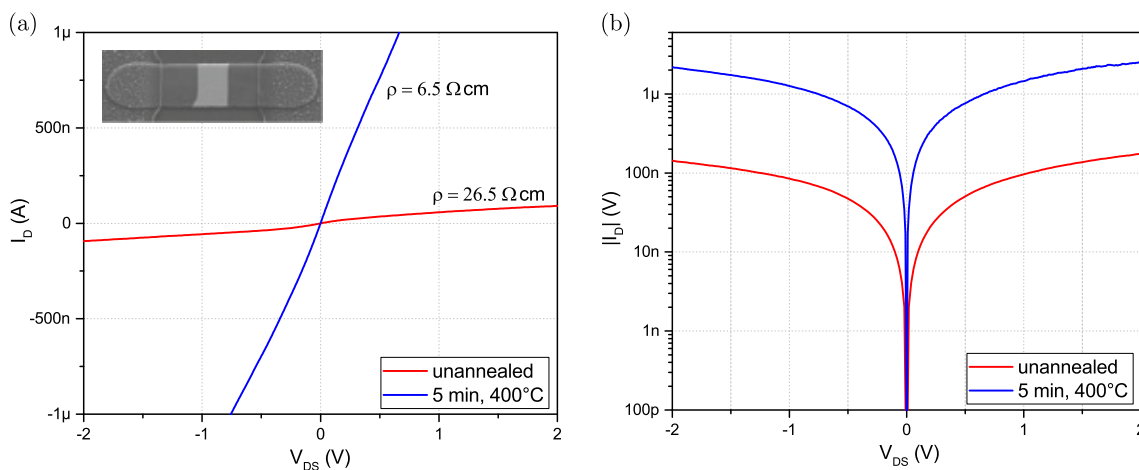


Figure 4.14: (a) I/V characteristic of a $2\ \mu\text{m}$ wide Al-Ge-Al structure before (red) and after annealing for 5 min at 400°C (blue). The SEM image of the exchanged structure is shown in the inset, with $L_{\text{Ge}} = 1.5\ \mu\text{m}$. (b) I/V measurement with absolute value of the current I_D in logarithmic scale.

The resistivity ρ of the structures is obtained by a linear fit of the measurements near the origin, taking into account their geometric dimensions. For the annealed structure the resistivity with $\rho = 6.5\ \Omega\text{cm}$ is in accordance with the values for undoped to slightly doped Ge [81]. Since the structures are very thin and not passivated by a high-quality oxide, an increase in conductivity by adsorbates and surface traps due to surface doping cannot be excluded [84]. It has been reported that this effect is particularly pronounced

in unpassivated Al-Ge-Al NW heterostructures with a high surface to volume ratio [23]. Although the resistivity is expected to be independent of the Ge channel length, it is significantly reduced after the first annealing step, which can be attributed to improved contact properties. This results from a transformation of the contact architecture, which was changed from an Al pad on top of the Ge beam to an atomically sharp contact at the Al-Ge junction within the narrow structure. Analyzing the I/V characteristics of more than ten devices, an average reduction of the contact resistance by roughly a factor of five was observed.

Several I/V characteristics for devices of different structural widths and Ge channel lengths are shown in Figure 4.15. As expected, wider structures with similar annealing progress in terms of channel length exhibit a steeper curve due to the larger cross-sectional area. Structures with similar widths and longer Ge segments show a higher resistance. It can be clearly seen that Al-Ge-Al heterostructures with ultrascaled Ge segments show exponential growth of the current I_D with increasing bias V_{DS} . Further a relatively symmetrical behavior was observed for both positive and negative voltages. This can be modeled as two back-to-back Schottky diodes.

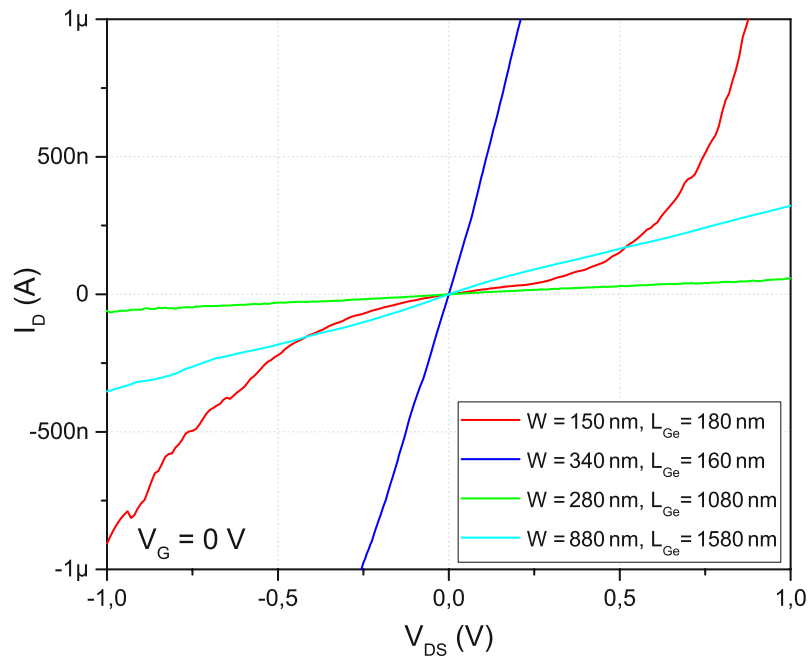


Figure 4.15: *IV characteristic of Al-Ge-Al heterostructures with different widths W and Ge channel lengths L_{Ge} .*

For a more detailed investigation of the conductivity of the formed heterostructures after different stages of annealing progress, the resistance normalized to the cross-sectional area of structures with different channel lengths was analyzed (Figure 4.16). The trend line

generated from the experimental data indicates that the resistance increases proportionally with the length of the Ge channel according to Ohm's law. A mean resistivity of $17 \Omega\text{cm}$ was determined, which is also consistent with values previously reported for intrinsic Ge [81]. The large variation in resistance of individual structures can be attributed to variations in the manufacturing process, contact properties and inaccuracies in geometric measurements. Surface traps and adsorbates may also contribute to a greater scattering of values.

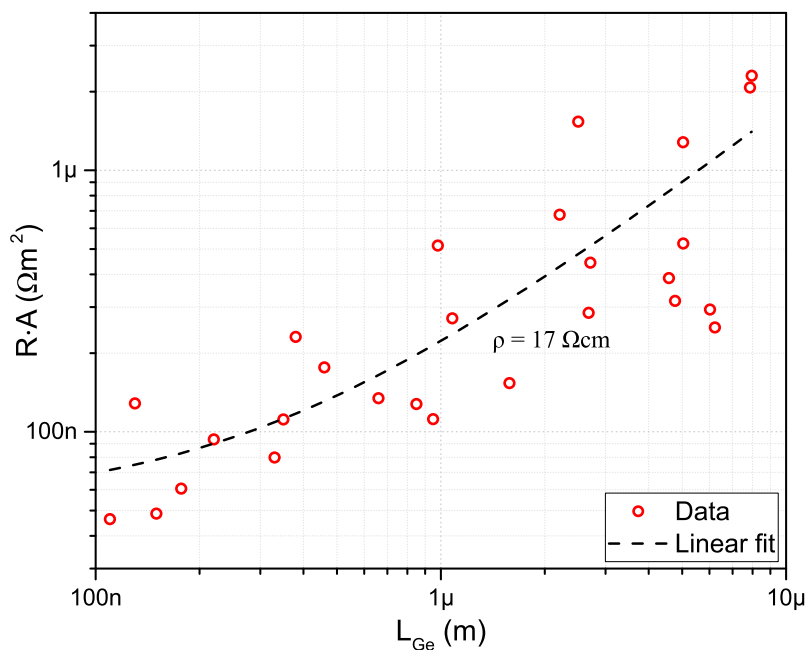


Figure 4.16: Sheet resistance $R \cdot A$ of various Al-Ge-Al heterostructure devices as a function of the Ge segment length. The data are plotted in a double logarithmic scale to cover a wide range of lengths from $L_{\text{Ge}} = 10\ \mu\text{m}$ to 100 nm .

4.2.2 Transfer Characteristic of Al-Ge FET Devices

By applying an external gate voltage (V_G) using the Si substrate as a global back-gate the Al-Ge-Al heterostructures can be operated as a SB-FET. To investigate the electrostatic modulation capability of the charge carrier in the structures transfer characterization measurements are conducted. Figure 4.17a shows the characteristic for three different Al-Ge-Al SB-FET devices. It is clearly visible that all structures exhibit a p-type behavior, although the Ge layer is not intentionally doped. Ge tends to accumulate holes at the semiconductor surface as a result of trapped negative surface charges. As a result, the energy band structure is bent upwards to maintain charge neutrality [84]. By applying a negative gate voltage, the Fermi level is shifted towards the valence band, resulting in an increased hole concentration in the Ge channel and furthermore a higher current through the channel. A positive V_G leads to a shift to the center of the energy band and thus to

a depletion of the charge carriers, until finally the intrinsic Fermi level and a minimum current flow is reached.

The fabricated heterostructures show a strong response to the applied back-gate voltage. However, due to the thick BOX layer between the structures and the back-gate a high gate voltage between ± 40 V was applied to modulate the current flow through the structure. Even with ultra-low bias voltages of only 1 mV, I_{on}/I_{off} ratios of about 10^3 can be achieved. In VLS grown NW heterostructures with similar Ge segment lengths, also formed by this thermal exchange reaction, I_{on}/I_{off} ratios of up to five orders of magnitude have been reported [85]. Due to the thick BOX layer between the structures and the back-gate a high gate voltage between ± 40 V was applied to modulate the current flow through the structure. The transfer characteristic shows a dependence of the saturation current on the geometry of the structures, as already observed in the I/V characteristics. The ohmic resistance of the devices increases for longer segments or thinner structures, reducing the current. Additionally, the off-state tends to shift towards higher gate voltages for devices with shorter Ge channels.

Especially structures with long Ge channels (>500 nm) exhibit a weak ambipolar behavior. Due to inversion in the semiconductor induced by the increasing gate voltage electron transport becomes dominant in this regime, leading to an increase of the current. This effect is characteristic for SB-MOSFETs and has already been observed in many other Al-Ge-Al NW heterostructures [66, 72].

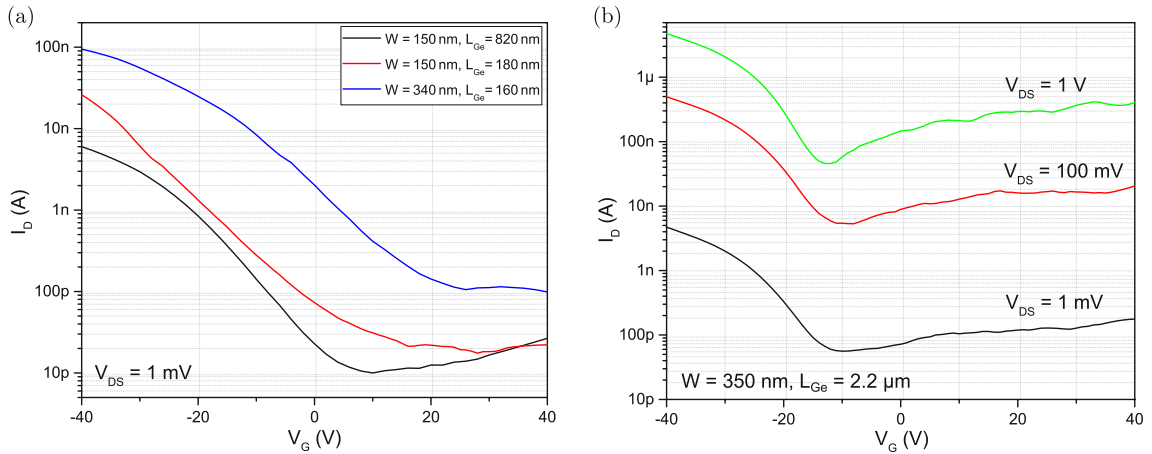


Figure 4.17: (a) Current I_D in relation to the back-gate voltage V_G at a low drain voltage $V_{DS} = 1$ mV for different devices showing a p-type behavior. The black and red curves show the transfer characteristic for devices with the same width but different L_{Ge} , while red and blue are different width devices with similar L_{Ge} . (b) Transfer characteristic for a Al-Ge-Al heterostructure with $W = 350$ nm and a long Ge channel with $L_{Ge} = 2.2$ μ m at various bias voltages V_{DS} between 1 mV and 1 V.

Figure 4.17b shows the transfer characteristic for a device with a $2.2\ \mu\text{m}$ long Ge channel for various drain voltages in the range of $1\ \text{mV}$ to $1\ \text{V}$. Due to the longer Ge channel, its modulation capability is slightly lower, with an I_{on}/I_{off} ratio of about two orders of magnitude. It is noticeable that with decreasing bias voltage the ambipolar response becomes less pronounced.

When recording the transfer characteristic, with back-gate voltage variations in both directions from $-30\ \text{V}$ to $30\ \text{V}$, a distinct hysteresis effect is apparent. This is shown in Figure 4.18 for two devices with similar Ge channels but different structure widths. The hysteresis results from a kinetic effect related to charge trapping on the surface. This effect is particularly pronounced in unpassivated NWs, which can be strongly influenced by charge trapping on the surface due to their high surface-to-volume ratio [23, 84]. Since, compared to VLS grown NWs, the structures fabricated on the GeOI substrate have a significantly higher roughness due to the etching process during production, comparatively wide structures are already susceptible to surface traps. The amount of hysteresis of the patterned Al-Ge-Al heterostructures seems to decrease with increasing structural width. This may be related to the decreasing surface-to-volume ratio, which makes the structures less susceptible to surface states. By passivating the structures with a high-quality oxide, the influence of surface traps and the associated hysteresis can be significantly reduced [23, 84].

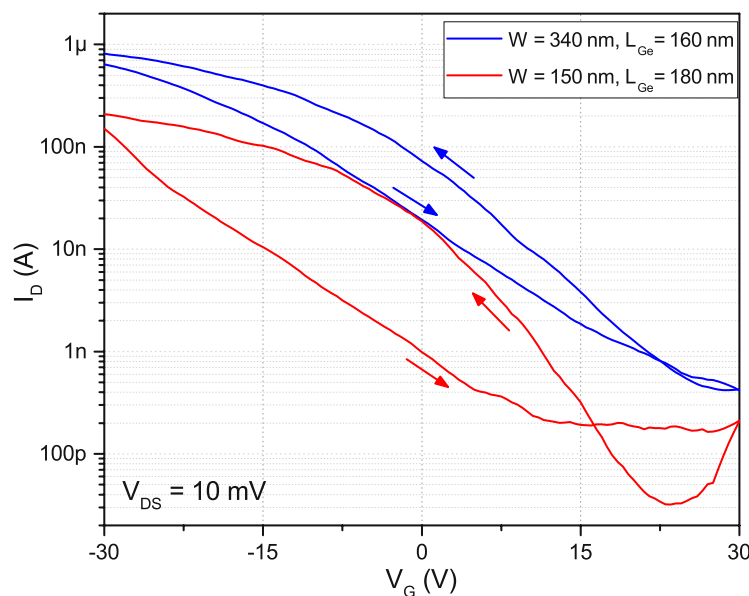


Figure 4.18: Comparison of transfer characteristics of Al-Ge-Al heterostructures with different widths and similar Ge channel length showing hysteresis effects. The arrows indicate the sweeping direction of the gate voltage. The data were recorded at a bias voltage of $V_{\text{DS}} = 10\ \text{mV}$.

4.2.3 Ballistic Transport

By further optimizing the process parameters of EBL and RIE and repetitive annealing cycles an ultrascaled NW heterostructure with a width of 40 nm and a Ge channel length of only 30 nm was fabricated. The SEM image of this structure is shown in Figure 4.19. The patterning process using RIE results in a rather rough surface of the structure compared to VLS grown NWs.

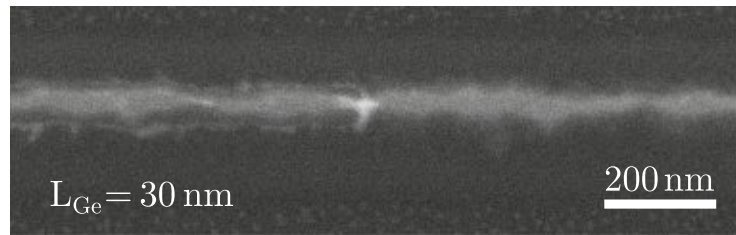


Figure 4.19: SEM image of an Al-Ge-Al NW heterostructure based on a GeOI substrate with a Ge channel length of about 30 nm, which is in the range of the mean free path for Ge with $L_{m,Ge} \approx 35$ nm [66].

With a channel length below the mean free path $L_{m,Ge} = 35$ nm ballistic transport is expected. Thereby, charge carriers can move through the Ge channel along trajectories without being scattered at the crystal lattice. This leads to an extremely high conductivity of the structure, only limited by the contact resistances.

Figure 4.20 shows the electrical characterization of the nanoscaled Al-Ge-Al structure. The I/V measurement shown in the inset reveals a linear, almost metal-like behavior, with the current proportional to the drain voltage V_{DS} . Due to the high conductivity only low drain voltages below 4 mV were applied to limit the current and furthermore prevent the structure from being destroyed. The structure exhibits an extremely high conductance of 1.17 mS. Considering the geometric dimensions, the conductivity is increased by more than 4 orders of magnitude compared to non-ballistic structures.

Measurements of the transfer characteristic revealed that even when extremely high back-gate voltages of up to ± 80 V are applied, the current can hardly be modulated. At a drain voltage of $V_{DS} = 1$ mV an I_{on}/I_{off} ratio of only 1.18 was achieved within this voltage range.

On the right side of the transfer characteristic an additional scale is shown, indicating the conductance of the structure scaled in multiples of the quantum conductance $G_0 = 2e^2/h$. It is directly proportional to the current I_D and the bias voltage V_{DS} . This scale indicates a redistribution of the ballistic current among 14 conductance channels. With increasing back-gate voltage more propagating modes are formed. This is in good agreement with the theoretical, qualitative estimation for the number of modes from Equation 2.22. With 75 nm for the thickness of the Ge layer as the maximum lateral extension of the conductor and a

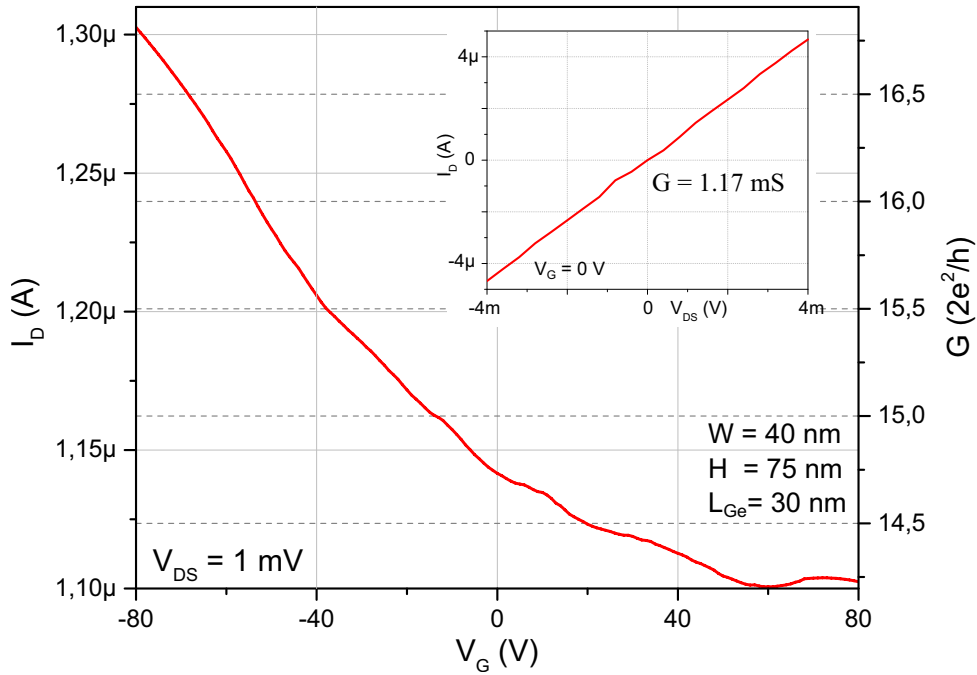


Figure 4.20: Transfer characteristic of an Al-Ge-Al heterostructure with a 30 nm long Ge channel with back-gate voltages between ± 80 V. The device shows modest modulation capabilities via the back-gate. In addition to the scale for the current I_D (left), the scale for the conductivity G in multiples of $G_0 = 2e^2/h \approx 77.5 \mu\text{S}$ is shown on the right. The inset shows the I/V characteristic of the structure. A significantly increased conductance of $G = 1.17 \text{ mS}$ is observed, also indicating ballistic transport.

Fermi wavelength of $\lambda_{f,Ge} = 10.67 \text{ nm}$, about 14 conductance channels are estimated inside this structure. The good correlation of the number of conductance channels further confirms that the current flow through the 30 nm long segment of the Al-Ge-Al heterostructure is ballistic.

A quantization of the ballistic conductance due to the control of discrete one-dimensional subbands, as demonstrated in VLS grown NWs [23], could not be observed in the examined structure. The dimensions of the cross-sectional area, especially the thickness of the Ge layer with 75 nm, clearly exceed the exciton Bohr radius of Ge with $a_{B,Ge}^* = 24.3 \text{ nm}$. Additionally, any quantization steps that might occur for measurements at room temperature would be washed out due to thermal broadening of the spacing of individual sub-bands. Thus, the observation of quantization effects requires further scaling i.e. a reduction of the Ge layer thickness or very low temperatures [28].

4.3 Al-Ge-Al Heterostructures with Reduced Channel Thickness

To reduce the dimensions of the cross-section of the Ge channel the sample was etched with a diluted $\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (1:10) etching solution. The Ge surface and any native suboxides (GeO_x , $x < 2$) present are oxidized by the H_2O_2 etchant to GeO_2 , which is water soluble and thus dissolved in the solution. The Al leads are not etched as it forms a thin and very stable native oxide layer on its surface. Therefore, even short Ge segments formed by the thermal substitution process can be selectively reduced in size without the requirement of a protective photomask. Figure 4.21 shows the SEM images of an annealed Al-Ge-Al heterostructure with a $2.2\ \mu\text{m}$ long Ge channel before and after a 45 s wet chemical treatment. The reduction of the width of the Ge segment is clearly visible in (4.22b). The edges at the Al-Ge interfaces also indicate a difference in height of the individual segments.

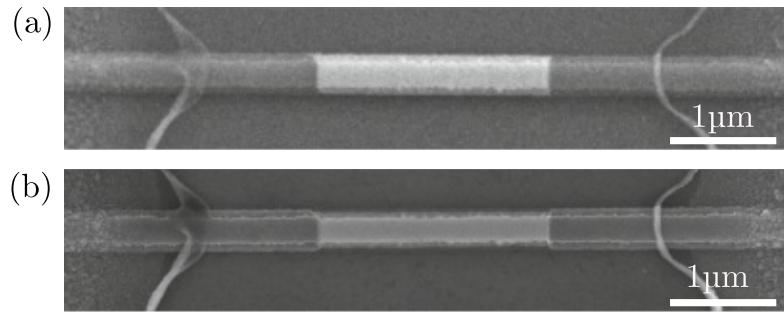


Figure 4.21: SEM image of an Al-Ge-Al heterostructure before (a) and after 45 s of etching with diluted H_2O_2 (b). After the chemical treatment the thickness and the width of the Ge segment are reduced.

With AFM topographic measurements, shown in Figure 4.22, it is possible to gain more detailed information about the structure, especially the height profile. In further consequence, the achieved etch rates can be determined. The AFM image of the complete Al-Ge-Al heterostructure in (4.22a) shows the significant difference in height between the etched Ge and the resistant Al leads. A uniform etching result was achieved without a noticeable increase in surface roughness. The cross-sectional profile in (4.22b) reveals a reduction of the Ge structure of about 20 nm in height and 60 nm in width, which was etched from both side. The overall shape of the bar remains unchanged, with a slightly increasing width towards the bottom resulting from the anisotropic RIE process. The diluted H_2O_2 etching solution thus shows a small anisotropy with an etching rate of 40 nm/min in $\langle 110 \rangle$ (y) and 27 nm/min in $\langle 100 \rangle$ -direction (z). Since the thickness of the Ge layer on the GeOI substrate is inherently very thin, a significant reduction of the width of the structure is not possible. In Figure 4.22c the topographic data of the AFM measurement are represented in three dimensions with the thinner Ge segment between the two Al leads.

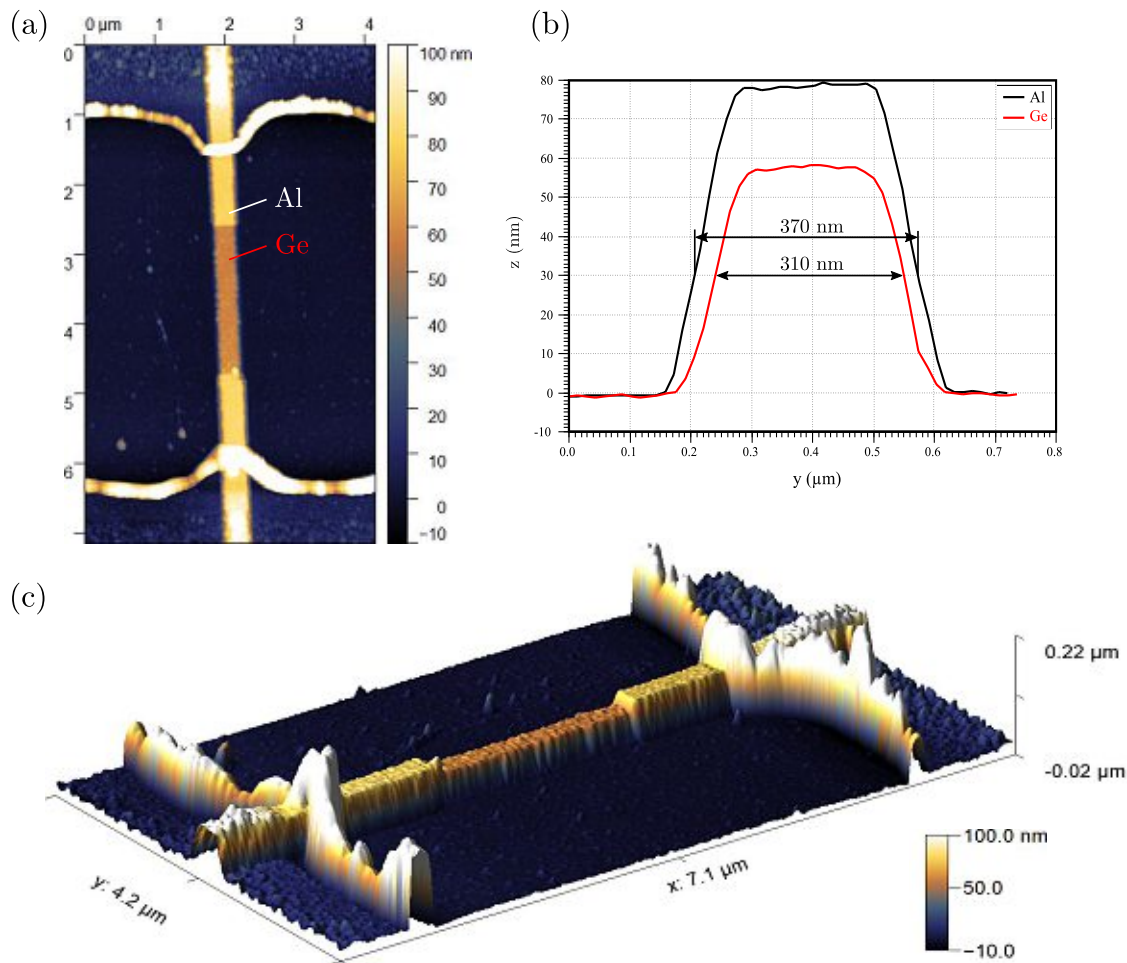


Figure 4.22: (a) AFM measurement of a heterostructure with a $2.2\ \mu\text{m}$ long Ge channel after wet etch processing. (b) Comparison of the cross-sections of the reduced Ge segment with the unaffected Al leads. Both the width and the height of the Ge channel were reduced. Note that the y and z axis are scaled differently. (c) 3D representation of the AFM, with the scale in z -direction enlarged.

To determine the effects of the reduction in the cross-sectional area through the chemical treatment on the electrical properties, I/V measurements were performed after different etching times. Figure 4.23 shows the I/V characteristic of the previously shown device in an unetched state (black) and after etching for 10 s (red) and 45 s (blue). The nonlinear behavior due to the Schottky contacts at the Al-Ge interfaces is clearly visible. A considerable increase in the resistance of the structure can be seen, which was expected due to the reduction in the lateral dimensions. While the cross-section of the structure was reduced by about 40%, its resistance has increased excessively by 80%. This may be attributed to the increased influence of surface scattering and depletion in nanostructures [28].

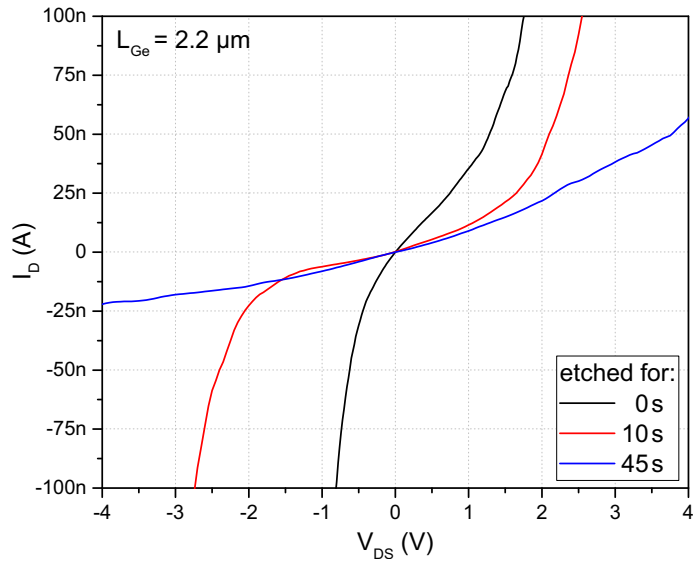


Figure 4.23: I/V characteristic of an Al-Ge-Al heterostructure device with a $2.2\ \mu\text{m}$ long Ge channel before (black) and after wet chemical etching for 10 s (red) and 45 s (blue). The cross section of the Ge layer is thereby reduced from $W \times H = 370\ \text{nm} \times 75\ \text{nm}$ (black) to $310\ \text{nm} \times 55\ \text{nm}$ (blue).

The transfer characteristic in Figure 4.24 again reveals lower currents with increasing etching duration due to the higher ohmic resistance. Its overall electrostatic modulation capability through an applied back-gate voltage remains largely unchanged. The measurement of several structures revealed that the ambipolar behavior is reduced with decreasing cross section for longer etching time.

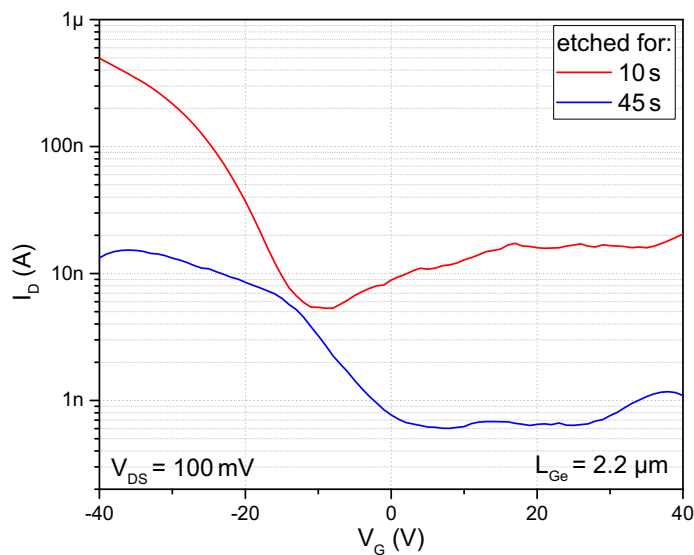


Figure 4.24: Transfer characteristic of an Al-Ge-Al heterostructure device after wet chemical etching for 10 s (red) and 45 s (blue) to reduce the cross section of the Ge layer.

The reduction of the Ge structure cross-section by wet chemical etching can also be carried out directly after the structure reduction with EBL. As the contacting and annealing is done subsequently, oxidation of the Al pads and leads by the H_2O_2 etching solution are prevented. Figure 4.25 shows an Al-Ge-Al structure which was etched in diluted H_2O_2 65 s with subsequent Al pad deposition and thermal annealing for 400 s, resulting in an 110 nm long Ge segment. The SEM image in 4.25a already indicates the reduced structure thickness due to the lower contrast, compared to previous pictures. A more precise measurement with AFM shown in 4.25b,c reveals that the conical shaped structure has been reduced to an average width of about 60 nm with a layer thickness of only 12 nm. However, the cross section along the bar is not completely uniform and shows a relatively high roughness in relation to the structure size (4.25b).

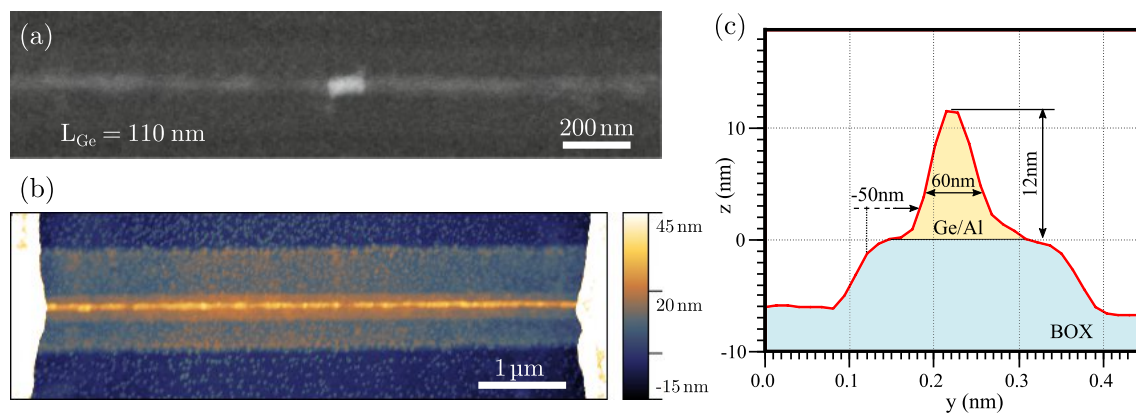


Figure 4.25: (a) SEM image of a 12 nm thick Al-Ge-Al heterostructure with $W = 60 \text{ nm}$ and $L_{\text{Ge}} = 110 \text{ nm}$. The contrast of the Al leads is already very weak due to its low thickness. (b) AFM topology of the device. (c) Cross-sectional profile (AFM) revealing a structure thickness of 12 nm. The BOX layer (blue) is also slightly etched by the diluted H_2O_2 acid.

The slightly higher part around the narrow beam in 4.25b originates from the 2 μm wide pre-patterned Ge structure using optical lithography, from which the 250 nm wide structure was formed by EBL and RIE. Outside of this Ge structure, the BOX was slightly etched during the RIE process. Similarly, H_2O_2 etching has created an about 5 nm high step along the original structure (see Figure 4.25b,c).

The electrical measurements of this narrow, short channel heterostructure device are shown in Figure 4.26. Its conductivity is well above average, as the Ge channel length already approaches the mean free path for ballistic transport. Using the back-gate with voltages between $\pm 80 \text{ V}$ the device can be very well electrostatically modulated over almost three orders of magnitude. Due to the short Ge channel the structure does not show any signs of ambipolar behavior. Furthermore, it even appears to be almost linear in the logarithmic scale within the measured range (Figure 4.26b).

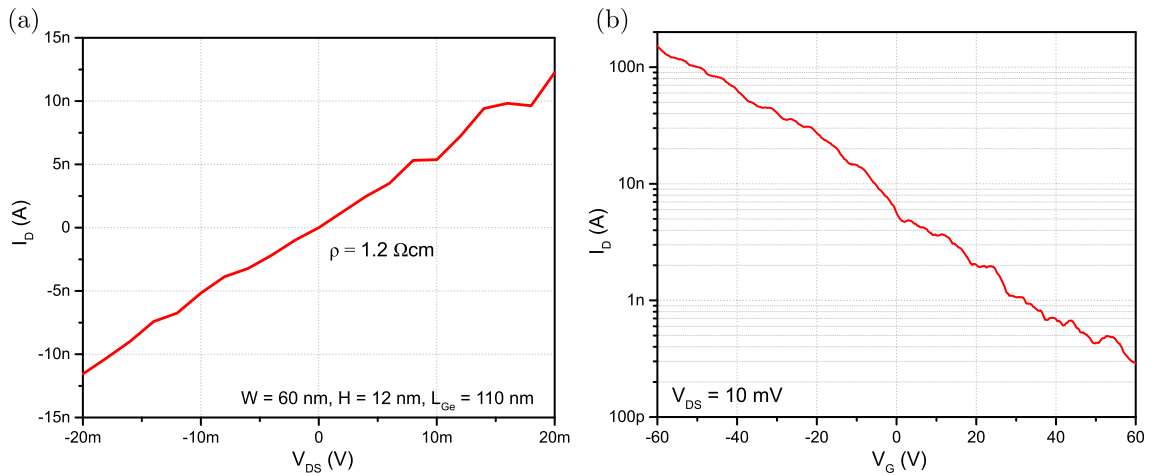


Figure 4.26: (a) I/V and (b) transfer characteristic of the 12 nm thick Al-Ge-Al heterostructure with a 110 nm short Ge channel.

4.4 Freestanding Al-Ge-Al Heterostructures

To further demonstrate the versatility of this fabrication method based on the thermal exchange reaction of Al and Ge, suspended heterostructure devices were fabricated. Figure 4.27 shows the SEM images of two underetched nanobeams. The samples were tilted in the SEM to allow a lateral view of the structures and visualize the undercut. The tilt of the sample within the SEM system results in changes of the imaging contrast as the ratio of secondary electrons to backscattered electrons is changed [86]. As a result, the image appears inverted in comparison to previous, non-tilted pictures, with Ge dark and Al light.

In Figure 4.27a, the oxide underneath a uniform structure with a width of $W = 250$ nm was removed by etching using BHF for 155 s through a $1.5 \mu\text{m}$ wide etching window defined with EBL. Within this opened window at the middle of the structure the oxide was etched deepest, with a maximum depth of 45 nm. Due to the isotropic etching behavior, the oxide has also been removed along the Ge structure, which resulted in almost the whole Ge structure between the Al contact pads being freely suspended. With subsequent annealing steps a Al-Ge-Al heterostructure within the suspended parts of the nanobeam is formed. This shows that the Al-Ge exchange process works without restrictions even in free-standing structures.

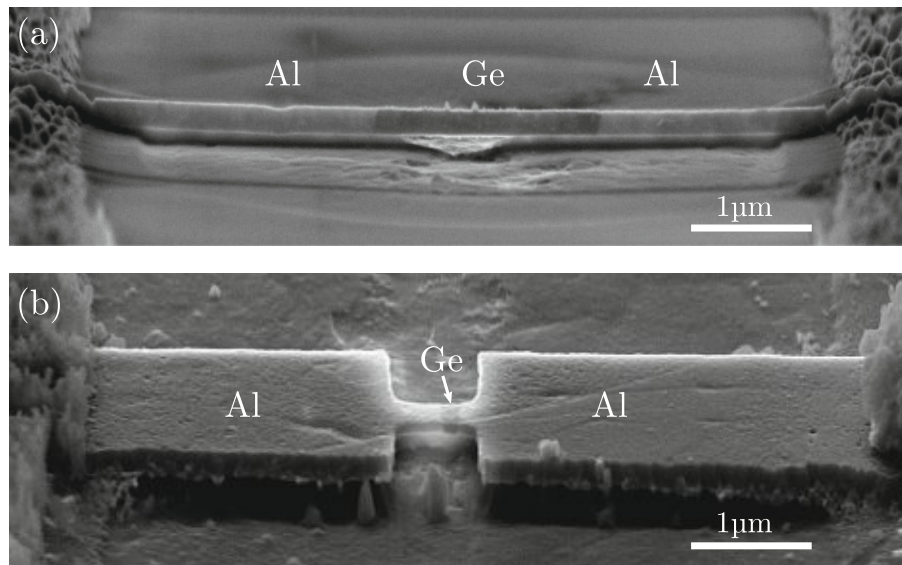


Figure 4.27: (a) Freestanding Al-Ge-Al heterostructure with uniform width of 250 nm and a 1.8 μm long Ge channel. (b) Narrow suspended nanobeam with $W = 280 \text{ nm}$ and $L_{\text{Ge}} = 148 \text{ nm}$ between two broad Al leads.

For the structure shown in (4.27b), EBL and RIE were used to partially reduce the width of the Ge structure to 280 nm. Subsequently, the BOX underneath the 680 nm long nanobeam was removed with BHF. During the thermal exchange reaction, the broad part of the structure is exchanged by Al. Finally, despite the transition to a smaller cross section, a well-defined 148 nm long Ge channel with straight abrupt Al-Ge interfaces is formed within the suspended nanobeam.

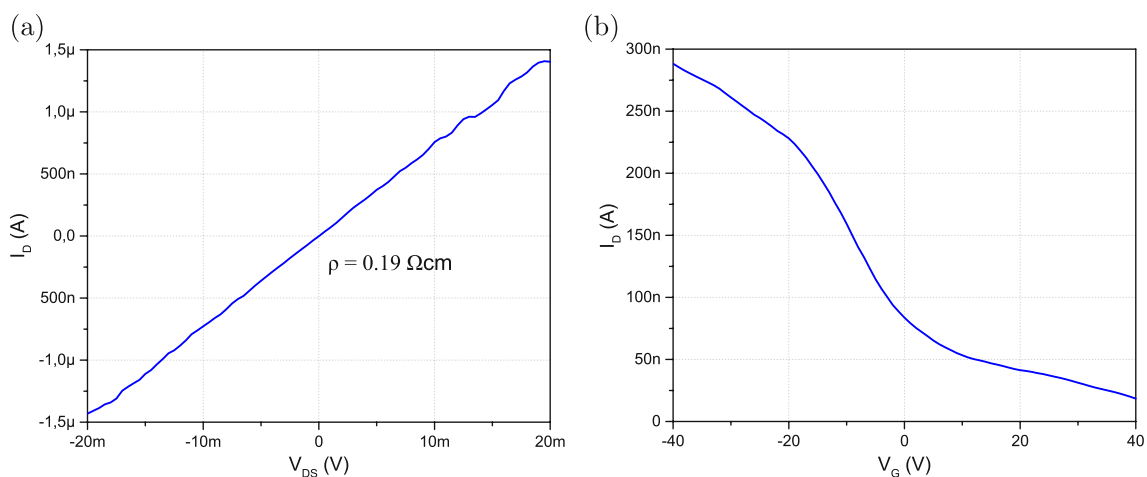


Figure 4.28: (a) I/V and (b) transfer characteristic of the freestanding Al-Ge-Al heterostructure of Figure 4.27b.

The electrical characteristic of this freestanding structure reveals an extraordinarily low resistivity of only $0.19 \Omega\text{cm}$, which is shown in Figure 4.28. Despite high back-gate voltages the suspended short channel device can only be modulated over about one order of magnitude. A further increase of the gate voltage is not possible as the dielectric strength is reduced by the thinner oxide layer and thus the structure could be destroyed.

The freestanding structure offers great potential for the fabrication of gate-all-around FETs. By depositing a gate insulator and a gate metal, the Al-Ge-Al heterostructure can be encapsulated, allowing excellent electrostatic control of the device [6, 87]. Furthermore, improved photo detector performance has been demonstrated for suspended metal-semiconductor-metal nanomembranes [88]. The freestanding structure can also be excited into mechanical vibration, making it a double-clamped resonator. In [89] a resonator using the beam as an active channel of a FET was demonstrated, that changes its properties due to the oscillation modes.



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Chapter 5

Summary and Outlook

In this thesis the thermally induced exchange reaction for the formation of monolithic Al-Ge-Al heterostructures in devices structured on a GeOI-substrate is presented. This enables the formation of ultra-short Ge segments in the nanometer range beyond lithographic limitations. HRTEM and EDX images reveal perfect crystallinity and an almost atomically sharp interface between the self-aligned Al leads and the Ge segment. The investigation of irregular structures of various geometries and orientations with widths from 4 μm to the low nanometer range show no geometrical limitations of the exchange process. EBSD measurements indicated that the formed Al segments are crystalline with grain sizes in the micrometer range. With decreasing structural size the high purity Al leads tend to be monocrystalline.

When examining the annealing process in structures with different geometries, a decrease in diffusion rates with increasing cross section has been found. The exchange rate also decreases with increasing process duration. The exchange along complex geometries, such as curved, kinked or tapered structures is also possible without restrictions, offering a variety of design possibilities. The formation of preferred diffusion fronts has been observed in $\langle 110 \rangle$ and less frequently also in $\langle 100 \rangle$ direction. Predefined recesses are also completely enclosed by the formed crystalline Al, which can be attractive for novel photonic or plasmonic devices.

Electrical characterizations reveal a significant improvement of the contact properties after the annealing process due to the atomically sharp Al-Ge interface. With a back-gate voltage applied to the p-doped Si substrate the devices can be operated as SB-FETs, where the carrier transport through the Ge channel can be modulated over several orders of magnitude. The transport characteristics clearly show a p-type behavior of the devices. An ambipolar behavior typically for SB-FETs has been observed for structures with long Ge

channels. Furthermore, the influence of adsorbates and surface traps was briefly discussed. With repetitive annealing cycles a narrow NW structure with an ultrashort Ge channel below 30 nm is achieved. For such ultrascaled devices with channel lengths below the mean free path of Ge, ballistic transport has been observed, where the absence of scattering processes during carrier transport leads to a drastic increase in conductivity.

With wet chemical etching the cross section of the Ge segment could selectively be reduced to further approach the dimensions of conventional VLS grown NWs. Finally, the fabrication of a suspended Al-Ge-Al heterostructure formed by thermal Al-Ge exchange of an underetched Ge nanobeam is demonstrated. Potential applications are possible in gate-all-around FETs, photo detectors or micro-electro-mechanical systems.

The use of a GeOI substrate as the basis for Ge structures allows the synthesis of large arrays of highly uniform (in diameter and length) nanoscaled structures. Compared to the fabrication of Al-Ge-Al heterostructures using VLS-grown Ge NWs, the usage of a slow, serial EBL process is not mandatory and can be replaced by modern, high performance lithography systems. This enables a simplified, fast and parallel integration of nanoscaled Al-Ge-Al heterostructures in the device layer of GeOI wafers. However, due to the dispersion of Al-Ge exchange rates, large-scale fabrication of specific channel lengths requires very elaborate process control.

This technology offers high potential for a broad spectrum of emerging Ge based devices embedded in monolithic metal-semiconductor-metal heterostructures such as CMOS compatible nanoelectronic and photonic devices. At low temperatures exploiting the superconductivity of Al, it can be a fundamental building block for the fabrication of superconductor-semiconductor hybrid quantum systems such as SQUIDS, oscillators or amplifiers [66, 83].

List of Abbreviations

Symbol	Description
Al	Aluminum
Al ₂ O ₃	Aluminum Oxide, Alumina
AFM	Atomic Force Microscope
Ar	Argon
As	Arsenic
Au	Gold
B	Boron
BHF	Buffered Hydrofluoric Acid
BOX	Buried oxide
C	Carbon
CMOS	Complementary Metal-Oxide-Semiconductor
Cr	Chrome
Cu	Copper
DI	Deionized Water
EBL	Electron Beam Lithography
EBSD	Electron Backscatter Diffraction
EDX	Energy Dispersive X-Ray Spectroscopy
Fcc	Face Centered Cubic
FET	Field-Effect Transistor
Ga	Gallium
GaAs	Gallium Arsenide
Ge	Germanium
GeO	Germanium Monoxide
GeO ₂	Germanium Dioxide

LIST OF ABBREVIATIONS

Symbol	Description
GeOI	Germanium on Insulator
H ₂ O	Water
HF	Hydrofluoric Acid
HfO ₂	Hafnium Oxide
HI	Hydroiodic Acid
HRTEM	High-resolution Transmission Electron Microscopy
ICSD	Inorganic Crystal Structure Database
I/V	Current/Voltage
FFT	Fast Fourier Transform
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
Mn	Manganese
N	Nitrogen
Ni	Nickel
NW	Nanowire
P	Phosphorus
PMMA	Polymethylmethacrylat
O	Oxygen
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
SB-MOSFET	Schottky Barrier MOSFET
sccm	Standard Cubic Centimeters per Minute (cm^3/min)
SEM	Scanning Electron Microscopy
SF ₆	Sulfur Hexafluoride
Si	Silicon
SiO ₂	Silicon Oxide
SMU	Source Measure Unit
Sn	Tin
SOI	Silicon on Insulator
SQUID	Superconducting Quantum Interference Devices
TEM	Transmission Electron Microscopy
Ti	Titanium
VLS	Vapor-Liquid-Solid

List of Symbols

Symbol	Description	Units
a	Lattice Constant	\AA
A	Cross-Section Area	cm^2
a_B^*	Exciton Bohr Radius	cm
C	Concentration	$1/\text{cm}^3$
D	Diffusion Coefficient	cm^2/s
\tilde{D}	Interdiffusion Coefficient	cm^2/s
$D(E)$	Density of States (1D)	$\text{eV}^{-1}\text{cm}^{-1}$
D_0	Frequency Factor	cm^2/s
e	Electronic Charge	C
E_a	Activation Energy	kJ/mol
E_C	Charging Energy	eV
E_f	Fermi Energy	eV
E_g	Energy Gap	eV
G	Conductance	S
G_0	Conductance Quantum	S
G_C	Contact Conductance	S
h	Planck Constant $\approx 6.626 \cdot 10^{-34} J s$	$J s$
\hbar	Reduced Planck Constant $\approx 1.055 \cdot 10^{-34} J s$	$J s$
I	Current	A
J	Flux of Diffusing Quantities	cm^2/s
k	Wave Number	$1/\text{cm}$
k_B	Boltzmann Constant $\approx 1.38 \cdot 10^{-23} J/K$	J/K
L	Length	cm
L_m	Scattering Mean Free Path	cm

LIST OF SYMBOLS

Symbol	Description	Units
M	Number of Modes	-
m^*	Effective Mass	kg
n	Electron Density	$1/cm^3$
N_A, N_B	Fractional Concentrations	-
p	Hole Density	$1/cm^3$
q	Unit Electronic Charge $\approx 1.602 \cdot 10^{-19} C$	C
R	Gas Constant $\approx 8.314 J K^{-1} mol^{-1}$	$J K^{-1} mol^{-1}$
R	Radius of Nanowire	cm
R	Resistance	Ω
t	Time	s
T	Temperature	K
T_i	Transmission Coefficient	-
v_f	Fermi Velocity	cm/s
v_K	Kirkendall Velocity	cm/s
V	Voltage	V
\tilde{V}	Partial Molar Volume	cm^3/mol
W	Width	cm
$\delta(x)$	Dirac Delta Function	-
$\vartheta(x)$	Step Function	-
λ	Wavelength	nm
λ_f	Fermi Wavelength	nm
μ_n, μ_p	Electron and Hole Mobility	cm^2/Vs
ρ	Resistivity	Ωcm
σ	Conductivity	S/cm
τ_m	Momentum Relaxation Time	s
φ	Electrochemical Potential	V
ϕ_B	Potential Barrier Height	V
ϕ_m	Metal Work Function	V
ϕ_s	Semiconductor Work Function	V
χ_s	Electron Affinity for Semiconductor	eV

Process Parameters

Substrate preparation

A GeOI substrate with a 75 nm thick $\langle 100 \rangle$ Ge device layer atop of a 150 nm buried SiO₂ layer and a 500 μm thick doped Si substrate is used. The substrate is coated with an about 50 nm thick protective SiO₂ layer, which is removed using BHF (etch rate approximately 1 nm/s).

- Cleaving a 5 mm \times 5 mm sample from the wafer using a diamond scribe
- BHF dip (7:1) for 80 s to remove the SiO₂ protective coating
- Dipping the sample in deionized water (DI) for 10 s and drying with N₂

Photolithography for Ge Structures

Positive photolithographic process to pattern Ge structures in the micrometer range. A Karl Süss MicroTec MJB3 mask aligner is used featuring an exposure wavelength of 450 nm.

- Spin coating of TI Prime adhesion promoter at 4000 RPM
- Baking for 120 s at 120°C
- Spin coating of image reversal resist (AZ5214) at 6000 RPM
- Baking for 60 s at 100°C
- Alignment of mask for Ge structures
- UV exposure for 3.5 s

PROCESS PARAMETERS

- Immersing the sample for 65 s in developer solution (AZ726MIF)
- Immersing the sample in DI for 30 s
- Drying the sample with N₂

Reactive Ion Etching (RIE)

The Ge structures are patterned using a RIE process in a PlasmaPro 100 Cobra system.

- Chamber cleaning: 10 min with O₂
- Preconditioning of the chamber: N₂ cooling to reach a chamber temperature of 35°C.
- Loading the sample into the load lock
- Set process parameters: SF₆: 50 sccm; O₂: 4 sccm; ICP power: 0 W; forward power: 15 W; temperature: 35°C; helium backing: 10 sccm
- RIE etching for 70 s
- Unload the sample
- Chamber cleaning: 10 min with O₂
- Resist stripping in acetone for 5 min
- Cleaning the sample with isopropanol and drying with N₂

Electron Beam Lithography (EBL)

The electron beam lithography is used to reduce the size of the predefined Ge structures, add additional structural features or define etching windows for the fabrication of freestanding wire structures.

- Scratching off the oxide layer on one side of the sample to provide a sufficient connection of the sample and the EBL system
- Placing the sample on the sample holder and inserting it into the EBL system via loadlock
- Aligning of the coordinate system and writefield

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- Taking SEM pictures of the Ge structures
 - Loading EBL mask file and aligning it to individual structures
 - Removing the sample via loadlock
 - Spin coating of PMMA resist AR-P-679.04 on the sample at 4000 RPM
 - Baking for 10 min at 170°C
 - Placing the sample on the sample holder and inserting it into the EBL system via loadlock
 - Measuring the electron beam current with Farraday cup
 - Calculate dwell times
 - Aligning of the coordinate system and writefield
 - Start exposure process
 - Removing the sample via loadlock
 - Developing for 35 s in developer solution (AR 600-56)
 - Immersing the sample in stopper solution (AR 600-60)
 - Drying the sample with N₂

After EBL, a second RIE process is performed.

Photolithography for Al Contact Pads

Image-reversal photolithographic process to pattern Al contact pads. A Karl Süss MicroTec MJB3 mask aligner is used featuring an exposure wavelength of 450 nm.

- Spin coating of image reversal resist (AZ5214) at 6000 RPM
- Baking for 60 s at 100°C
- Alignment of mask for Al contact pads
- UV exposure for 4 s

PROCESS PARAMETERS

- Reversal baking for 60 s at 120°C
- Flood exposure (UV) for 20 s
- Immersing the sample for 30 s in developer solution (AZ726MIF)
- Immersing the sample in DI for 30 s
- Drying the sample with N₂

Ge_xO_y Removal

Prior to the Al sputter deposition, the native Ge_xO_y layer on the Ge surface is removed by wet chemical etching in diluted HI (etch rate approximately 1 nm/s).

- Dipping the sample in HI for 5 s
- Dipping the sample in DI for 10 s
- Drying the sample with N₂

Al sputtering

The Al contact pads with a layer thickness of about 125 nm are deposited using a VonArdenne® sputter system.

- Loading sample and pumping sputter system to a base pressure of $2 \cdot 10^{-6}$ mbar
- Cleaning of the Al sputter target: 2 × 60 s, 100 W RF power
- 125 nm Al deposition: 4 × 60 s, 50 W RF power (working pressure: $8 \cdot 10^{-3}$ mbar)

Lift-off

Subsequent to the sputter deposition, the excess metal is removed by a lift-off procedure in acetone.

- Immerse sample in acetone at 50°C
- After 30 min, carefully rinse the sample with acetone
- Ultrasonic cleaning with 20% for 1 min in acetone
- Isopropanol dip and N₂ drying

Rapid Thermal Annealing

The Al-Ge-Al heterostructure formation process is performed in a "UniTemp UTP 1100" RTA system with the following parameters:

- Placing the sample on a carrier waver in the RTA oven
- Pumping 120 s to a pressure of about 1 mbar
- Flushing 120 s with N₂
- Pumping 120 s to a pressure of about 1 mbar
- Flushing 120 s with N₂
- Pumping 120 s to a pressure of about 1 mbar
- Flushing 120 s with N₂/H₂ forming gas
- Heating to 300°C with a 75 K/s temperature ramp
- Heating to 400°C with a slower 50 K/s temperature ramp to avoid temperature overshoot
- Annealing duration depends on desired Ge segment length
- Cooling to ambient temperature and removing the sample

H₂O₂ etching

For a selective etching of the Ge layer a diluted H₂O₂ solution is used.

- Prepare the etching solution with H₂O₂:H₂O (1:10)
- Immersing the sample in the etching solution
- Etching duration depends on the desired Ge layer thickness (etch rate approximately 40 nm/min)
- Dipping the sample in deionized water (DI) for 10s and drying with N₂

BHF Etching for Freestanding Structures

To achieve suspended wire structures, the SiO₂ layer underneath the Ge structure is removed by isotropic wet chemical etching with BHF (etch rate SiO₂: ~1 nm/s). The Al pads must be sufficiently protected by photoresist (etch rate Al: ~2 nm/s).

- BHF dip (7:1) for 155 s
- Dipping the sample in deionized water (DI) for 10s
- Drying the sample with N₂

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