DISSERTATION

# Predictive and Efficient Modeling of Hot Carrier Degradation with Drift-Diffusion Based Carrier Transport Models

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# ABSTRACT

Reliability in metal oxide semicondcutor (MOS) transistors is an important concern due to their use in crucial fields like space, military, medical, and several consumer products. As the electric fields in MOS devices increase, so does the probability of failure due to high energy carriers. Thus, simulation of these semiconductor devices before production is vital for optimizing the device designs and assessing their lifetimes. Simulation of degradation due to high energy carriers is challenging as carrier transport needs to be addressed to obtain the carrier energy distribution function (DF) via solution of the Boltzmann transport equation (BTE). This is a complicated and computationally demanding task. In laterally diffused metal-oxide semiconductor (LDMOS) transistors, for example, their large dimensions, peculiar architecture and high operating voltages make the solution of the BTE challenging. In scaled devices, on the other hand, scattering effects become dominant which makes the estimation of the DF difficult.

For this purpose, a drift-diffusion based approach is suggested which captures both the hot and cold carriers in the device. As a reference, a solution of the Boltzmann transport equation is performed using the spherical harmonics expansion method. The validity of the DD based approach is tested on LDMOS transistors by simulating the degradation characteristics like the interface state generation rates, the interface state density profiles, and changes of the linear and saturation drain currents as well as the threshold voltage shift and comparing with the spherical harmonics expansion (SHE) based approach as well as measurements. The applicability of different available analytic models for the DF has also been analyzed, namely the heated Maxwellian, the Cassi model, the Hasnat approach, as well as the Reggiani model. The DFs obtained from the different approaches are used as input for the physical HCD model and device degradation characteristics are determined. It is shown that the heated Maxwellian approach leads to an underestimation of HCD at long stress times. This trend is also typically observed for the Cassi and Hasnat models but in these models HCD is underestimated in the entire stress time window. While the Reggiani model gives good results in the channel and drift regions, it cannot properly represent the high-energy tails of the DF near the drain, and thus leads to a weaker curvature of the degradation traces. The analytical model for the carrier DF used in this work is capable of capturing DFs with very good accuracy and, as a result, the change of the device characteristics with stress time. Since the expression for the DF considers the contribution of both the hot and equilibrium carriers, it is well suited for the HCD model used which takes into account the single-carrier and multiple-carrier processes. The comparison of different realizations of the model shows that HCD captured by the DD based approach suggested in this work is very similar to the SHE based approach and matches the experiments quite well.

Particular attention is paid to study the role of the colder fraction of the carrier ensemble. The role of cold carriers is checked by neglecting their effect in HCD modeling in LDMOS devices stressed at high voltages. In the proposed model, cold carriers are represented by the corresponding term in the analytic formula for the carrier distribution function as well as by the multiple-carrier process of the Si-H bond dissociation. It is shown that even in high-voltage devices stressed at high drain voltages the thermalized carriers still have a substantial contribution to HCD. These results contradict the previous conception that cold carriers are not important for HCD in power MOSFETs.

The limits of the DD based HCD scheme is determined using devices of different dimensions. A comparison of carrier distribution functions, bond breakage rates, interface state density profiles, and changes of device characteristics such as the saturation and drain currents obtained from SHE and DD based approaches for MOSFETs with different channel lengths suggests that this DD based approach is not suited for channel lengths less than $1.5\,\mu$m. Also, in scaled devices mechanisms like electron-electron scattering start to affect the DF which cannot be captured with a simplistic approach. Thus, the simplistic DD-based HCD model is extended to the case of decananometer transistors. Special attention is paid to the effect of electron–electron scattering, which populates the high energy tail of the carrier distribution function, by using a rate balance equation. Finally, the accuracy and limits of applicability of the DD-based model are discussed concluding that the model is able to capture hot-carrier degradation in MOSFETs over a range of gate lengths with excellent accuracy.

# Acknowledgments

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I am eternally grateful to my parents who always encourage me to do better and challenge myself. They inspire me to be hardworking and persistent.

*Dedicated to my grandmother.*

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# Contents

# Chapter 1

# Introduction

One of the main concerns limiting the lifetime of semiconductor devices is hot-carrier degradation (HCD) [1, 2, 3, 4, 5, 6]. HCD is often assumed to be dominated by the interaction of carriers with the Si-H bonds which are formed at the Si-insulator interface during hydrogen annealing of the unpassivated Si bonds. The rupture of interfacial Si-H bonds leads to the creation of traps which then can capture charges and affect normal device operation. The charged traps perturb the electrostatics of the device, leading to a change in the threshold voltage ($\triangle V_{\mathrm{th}}$). The interface defects can also act as additional scattering centers and lead to changes in the mobility ($\mu$) and consequently to the degradation of linear and saturation drain currents ($I_{\mathrm{d,lin}}/I_{\mathrm{d,sat}}$), transconductance ($g_{\mathrm{m}}$), etc. Although the first observation of this detrimental phenomenon dates back over four decades, the full physical picture is complicated and not yet completely understood, making predictive modeling of HCD difficult. As a result, quite often simplified empirical/phenomenological approaches are used [7, 8]. The successful among them are based on the so-called "energy driven paradigm" proposed by Rauch and La Rosa [9, 10, 11, 12]. These approaches introduce three main modes of HCD: (i) governed by the single-carrier (SC-process) mechanism of Si-H bond dissociation, (ii) driven by the multiple-carrier (MC-process) bond breakage process, and (iii) dominated by electron-electron scattering (EES). In the SC-process, a high energy carrier ruptures the Si-H bond in a single interaction. This process is assumed to be the dominant HCD mechanism in metal oxide semiconductor field effect transistors (MOSFET) stressed at high voltages (also referred to as classical HCD). The MC-process involves interaction of the Si-H bonds with multiple low energy carriers which is more typical for scaled devices subjected to HCD at lower voltages. However, it has recently been shown that the MC degradation mode can result in a significant contribution also in high-voltage devices with channel lengths up to $2\,\mu$m [12, 13, 14], while the SC-process can be important even in decananometer MOSFETs [14, 13, 15].

Therefore, in order to properly represent the contributions of SC- and MC-processes one needs to be able to distinguish between hot and cold carriers. This information is contained in the carrier energy distribution function (DF) which can be obtained from the solution of the Boltzmann transport equation (BTE). There are two main strategies to obtain such a solution: the stochastic Monte-Carlo method [16, 17] and deterministic methods which are based on a representation of the carrier DF by a spherical harmonics expansion [18, 19, 20]. Both methods are numerically quite challenging even for ultra-scaled planar MOSFETs and especially in transistors with 3D architectures. Thereby, the computationally demanding simulations of the carrier energy distribution function are often avoided and the rates of

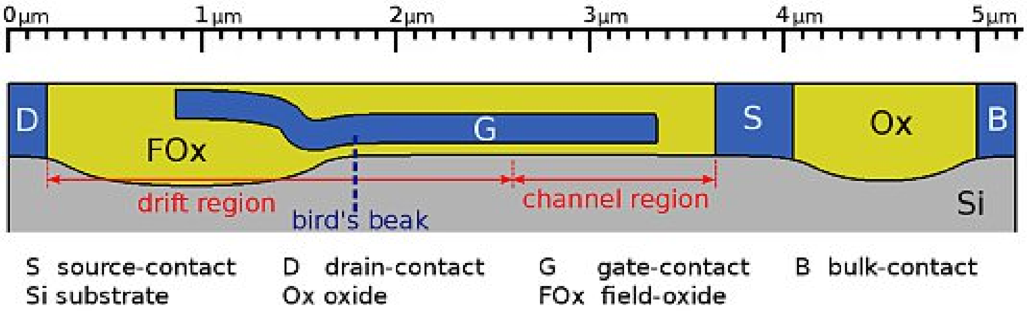

Figure 1.1: Schematic of an nLDMOS transistor showing its complex geometry which makes the transport simulations and HCD modeling challenging.

the aforementioned processes are described by empirical formulas which are related to the macroscopic transistor characteristics [21, 22, 23, 12]. Note that these models are derived and calibrated using accelerated stress conditions. Therefore, it is possible that at real operating conditions the physical picture behind HCD is different, thereby making the models based on empirical expressions not predictive.

A remedy can be a physical HCD model which covers and links the whole hierarchy of the aspects related to HCD, namely (i) thorough carrier transport treatment which provides the information about the carrier energy distribution needed to (ii) model the microscopic mechanisms of trap generation and the corresponding rates, and to (iii) simulate the characteristics of the degraded devices [15, 24]. The most computationally expensive among these sub-tasks is the carrier transport treatment which requires a solution of the Boltzmann transport equation (BTE). This becomes even more challenging for large devices like laterally diffused metal oxide semiconductor (LDMOS) transistors. First of all, this is related to the typical dimensions of these devices, as compared to nanoscale complementary metal oxide semiconductor (CMOS) transistors, and thus to a mesh which contains a large number of cells. Second, complex transistor architectures with features like a bird's beak, shallow trench isolation (STI) corners and non-planar interfaces, see Figure 1.1, as well as high doping gradients in different regions make the situation worse. Whereas in scaled devices the complexity increases due to increasingly important scattering mechanisms and complex 3D geometries such as those of finFETs. Furthermore, as we have shown [25, 26, 27], both single- and multiple-carrier mechanisms of bond dissociation provide substantial contributions to HCD in these devices.

In this context, simplified approaches to the solution of the Boltzmann transport equation such as the drift-diffusion (DD) and energy transport schemes appear to be very attractive [28, 29, 30, 31]. However, these approaches only provide some moments of the BTE rather than the full DF, which then has to be estimated using approximate analytical expressions. The most popular variant is the heated Maxwellian distribution and its modifications like a polynomial in the exponential [32], models developed by Cassi *et al.* [33], Hasnat and co-authors [34], Reggiani [35], etc. These carrier DFs are based on quantities such as the electric field or the carrier temperature obtained from a simplified moment-based BTE solution. Among them, the most successful model has been developed by Reggiani *et al.* which is suitable for the analytic description of DFs in LDMOS devices with a shallow trench isolation [35, 36]. The Reggiani model is able to represent the degradation of the device quite well when applied to HCD. Recently, the model has been demonstrated to work for LOCOS and STI-based LDMOS devices [37, 38]. However, the model has some difficulties in capturing the high-energy tail of the DF in the drain region and leads, therefore, to a less accurate description of the degradation in the drain area of the LDMOS. The inherent simplifications in all the above mentioned models limits their applicability and, thus, they cannot always substitute the solution obtained from the BTE. In this work, an analytical approach based on the physical mechanism is developed for DFs and HCD prediction.

The structure of the thesis is as follows: In order to precisely model the device degradation due to HCD, it is important to understand the difference between different reliability issues in semiconductor devices. Thus, the different degradation mechanisms and available carrier transport models in microelectronic devices are discussed in Chapter 1. The three main reliability issues discussed are: bias temperature instability (BTI), hot-carrier degradation (HCD) and time dependent dielectric breakdown (TDDB). BTI is mainly attributed to the creation of oxide defects and interface traps due to applied bias at elevated temperatures while the carriers are in equilibrium [39, 40, 41]. HCD, on the other hand, occurs due to the generation of defects at the oxide-semiconductor interface by the impinging high energy carriers [1, 7]. TDDB is a result of a percolation path in the dielectric which develops due to an applied field across the insulator [42, 43].

Chapter 2 is focused on HCD which is of most relevance for this work. This chapter also discusses the different experimental techniques used to extract interface state density profiles which are an important metric of degradation. Chapter 3 gives an overview of the existing HCD models, while Chapter 4 deals with the hot-carrier degradation model derived by our group [13, 25, 44]. Since the accurate description of HCD requires evaluating the carrier distribution function via a solution of the Boltzmann transport equation, special emphasis is given to the spherical harmonics expansion and the drift-diffusion methods. Thus, two versions of the HCD model have been used in this work, one based on carrier transport treatment by means of deterministic solution of the Boltzmann transport equation and another uses the simplified drift-diffusion scheme. In the latter implementation of our model an analytical expression is employed to approximate the carrier energy distribution function for the entire device. In Chapter 5, the results of both versions of the model are compared against experimental data for the n-and p-channel LDMOS transistors and a conclusion on the validity of the DD-based approach is drawn. The results suggest the efficiency of the DD-based method for predictive HCD simulations of LDMOS devices. The contribution of cold carriers to hot-carrier degradation is also analysed. The effect of cold carriers in our HCD model is twofold: firstly, a cold carrier term is used in the energy distribution function to account for low energy carriers, and secondly, the cold carriers determine the multiple-carrier process of Si-H bond dissociation.

Chapter 6 compares the different models for calculating the carrier DFs. The DFs obtained from the different approaches are used in our HCD simulations to predict the degradation in nLDMOS devices [45]. The simulated changes in device characteristics are compared to experimental data and conclusions on the validity of each model are drawn. Since all models use the same parameter set, the differences in the results can be directly traced back to inaccuracies in the approximation of the DF. Chapter 7 explores the limits of the DD-based method for obtaining the carrier energy DF. The analytical approach is used on planar devices with different dimensions and the HCD predicted by the SHE- and DD-based approaches are compared. The results suggest that the DD method to obtain the carrier DF looses its validity for devices scaled beyond 1.5 $\mu$m. Chapter 8 deals with an

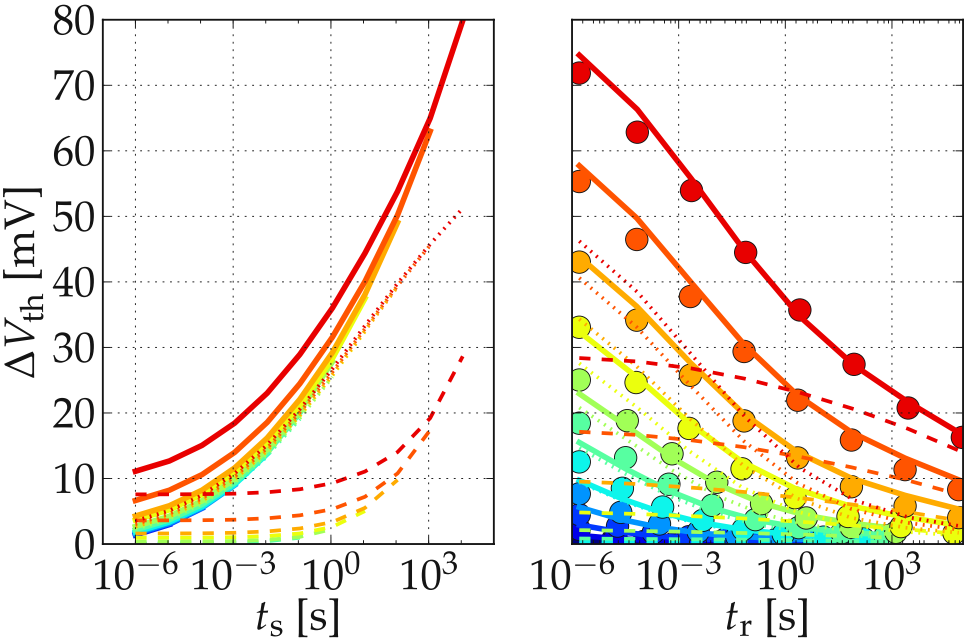

Figure 1.2: The threshold voltage shifts during NBTI stress ($t_{\mathrm{s}}$) and recovery ($t_{\mathrm{r}}$) in a pMOSFET with a 2.2 nm thick SiON oxide [46]. Dotted, dashed and solid lines represent the recoverable, permanent and the total degradation, respectively, obtained from simulations using the NMP model, while the symbols represent the experimental data. The measurements and simulations were performed with a subsequent increase in stress duration. The recovery curves suggest that the device does not fully recover within the given experimental window.

extension of our DD-based model to decananometer MOSFETs by incorporating the effects of electron-electron scattering on the carrier distribution. In Chapter 9, some conclusions are drawn, while Chapter 10 discusses future refinements and an outlook towards predictive HCD modeling.

## 1.1 Bias Temperature Instability

Bias temperature instability refers to the time-dependent instability in transistors which accelerates when bias and temperature are increased. It is particularly observed when a high voltage is applied to the gate contact of a transistor at elevated temperature, while the other contacts remain grounded. Previously BTI was considerable only in p-channel MOSFETs, especially with SiON gate dielectrics, due to hole trapping and interface state generation, but negligible electron trapping [1, 47, 48]. However, with the use of high-K dielectrics, both n- and p-channel MOSFETs can exhibit considerable BTI due to electron and hole trapping in the high-K and interfacial oxide layer [49, 50]. Another factor leading to pronounced BTI in modern devices is the aggressive down-scaling giving rise to high electric fields to maintain a reasonable subthreshold leakage. Increase in the density of integrated circuits for ultra large scale integrated systems on chips also leads to an increase in the power dissipation and self heating.

The BTI in n- and p-MOS transistors is observed when a positive or a negative voltage is applied at the gate and thus the phenomenon is referred to as positive bias temperature instability (PBTI) or negative bias temperature instability (NBTI), respectively. The consequence of BTI is a change in the threshold voltage in the inversion mode, thus, leading to a change in the drain current. BTI also affects other device parameters such as transconductance and gate-drain capacitance. In CMOS circuits this would mean performance degradation such as reduction of the switching speed. This degradation is usually attributed to chargeable defects, for instance the hydrogen bridge and the hydroxyl $E'$ centers [51, 52, 53]. The other contributors to BTI are interface traps. These defects are present directly at the interface (represented with a density $N_{\mathrm{it}}$) of the substrate and gate insulator in MOS devices [39, 40]. The capture and emission of charge carriers by these defects causes changes in the electrostatics of the device which disturb its functionality. For example, the threshold voltage in a p-MOSFET is given by [39]

$$V_{\mathrm{t}} = \Phi_{\mathrm{MS}} - \frac{Q_{\mathrm{ox}}}{C_{\mathrm{ox}}} - \frac{Q_{\mathrm{it}}(2\Phi_{\mathrm{F}})}{C_{\mathrm{ox}}} - 2\Phi_{\mathrm{F}} - \frac{Q_{\mathrm{S}}}{C_{\mathrm{ox}}}, \tag{1.1}$$

where $\Phi_{\mathrm{MS}}$ is the work function difference between the gate and the substrate, $\Phi_{\mathrm{F}}$ the Fermi potential, $Q_{\mathrm{ox}}$ $(= qN_{\mathrm{ot}})$ the oxide charge density, $Q_{\mathrm{it}}$ $(= qN_{\mathrm{it}})$ the interface charge density, $Q_{\mathrm{S}}$ the semiconductor charge density, and $C_{\mathrm{ox}}$ the oxide capacitance per unit area. The oxide and interface charges denote the charges trapped by corresponding defects and, thus, Equation 1.1 approximates the relation between the threshold voltage and the change in the oxide and interface charge densities. It should be noted that Equation 1.1 assumes that the oxide capacitance $C_{\mathrm{ox}}$ remains unchanged during stress [54]. A characteristic feature of BTI is recovery, meaning that upon the removal of stress the device parameters tend to attain their original values as shown in Figure 1.2. The difference between the original and recovered values of the parameters is often called the permanent component of BTI. In the past, the recovery of BTI was largely attributed to $N_{\mathrm{ot}}$ recovery on removal of stress, while the $N_{\mathrm{it}}$ were considered to remain unchanged during the recovery phase [55]. However, this differentiation is often debated and it was shown that $N_{\mathrm{ot}}$ also contributes to the permanent component of BTI [57], thereby making the characterization of BTI much more complex.

A majority of the modeling attempts focus on NBTI as it is a severe problem in Si/SiO$_2$ based devices. In this respect, the Reaction–Diffusion (RD) model and its extensions have been widely used [58, 59, 60, 61]. Within the framework of the RD model, the reaction phase consists of interface trap generation and release of hydrogen as a consequence. The reaction is diffusion-limited. The released hydrogen is then assumed to diffuse into the oxide during the stress. This diffusion is dependent on the stress time. During the stress phase the degradation, i.e. interface state generation, predicted by the RD model typically depends on stress time as $t^n$ [39]. However, the relaxation or recovery has not been adequately explained by any extension of the RD model.

The RD models have proven to be inaccurate and later studies have linked NBTI to reaction-limited processes like charge trapping and interface state generation [55, 62, 63, 64]. Some better descriptions were given by the double and triple well models where the diffusion of hydrogen is replaced by dispersive bond-breaking [59, 65, 66]. A more advanced model which was devised to explain the more complex experimental data was the two stage model [67]. This model suggested hole capture to occur in the gate oxide due to the presence of border traps instead of the Si/insulator interface. The introduction

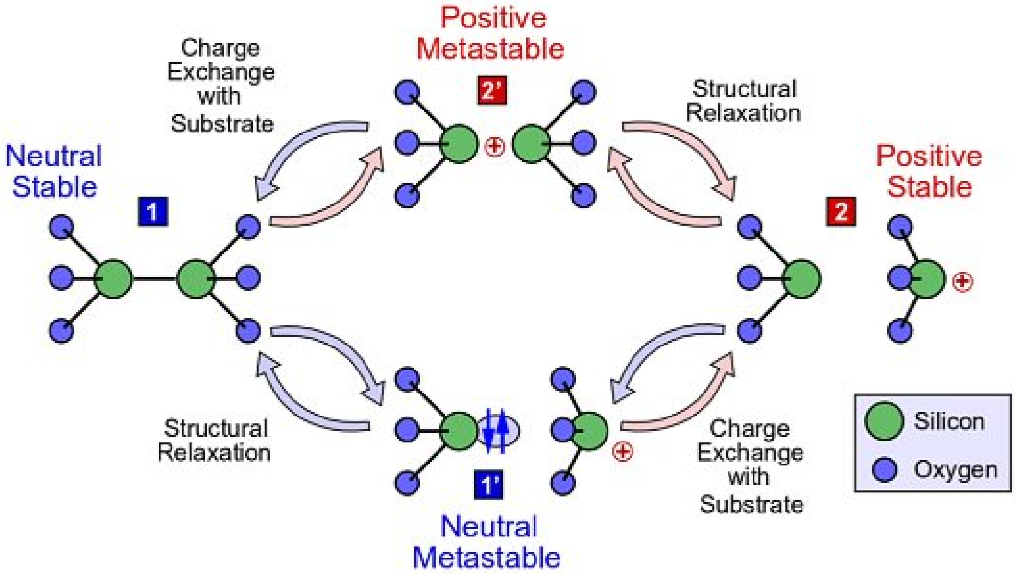

Figure 1.3: Description of the neutral and charged states of an example oxide defect within the four state model framework. A hole capture event in the equilibrium state creates the metastable state 2' which can relax to a positive stable state 2 and an $E'$ center is created. Upon electron capture, the $E'$ center is neutralized into the metastable state 1'. Now hole capture can cause a transition back to state 2 or a structural relaxation can lead to the original equilibrium state 1. From [56].

of time dependent defect spectroscopy (TDDS) has enabled detailed investigations of the charging and discharging of single defects. These investigations have led to the formulation of the four state model based on the non-radiative multiphonon (NMP) theory [68]. This model suggests the existence of two metastable states along with the conventional charged and neutral states. Within the NMP framework, the capture and emission time maps are derived using the carrier capture and emission time constants for the transitions between different states, shown in Figure 1.3. The distribution in the capture and emission time maps is mainly governed by the equilibrium occupancy difference which also describes the average contribution of a defect to the threshold voltage [69, 46]. The four state model not only explained the observations in BTI and TDDS experiments but also random telegraph noise (RTN) and flicker noise. These have been attributed to random exchange of charges between defects and the substrate during stationary conditions [70, 56]. The NMP model is highly effective in representing many more BTI characteristics when combined with a two well model for interface state generation.

## 1.2 Hot-Carrier Degradation

Similar to BTI, HCD is also related to the build-up of defects at/near the Si/$SiO_2$ interface. However, during BTI stress, the electric field component along the channel is usually constant as the source and drain contacts are grounded. Thus, only the perpendicular component of the oxide field plays a role in defect creation. Hot carrier degradation, on the other hand, occurs when a voltage between source and drain is applied, leading to

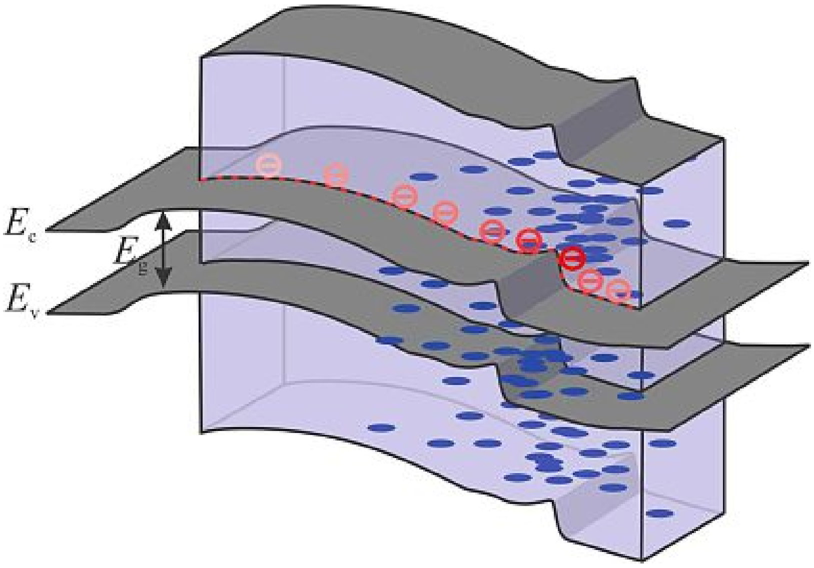

Figure 1.4: The high energy carriers in the conduction band break the Si-H bonds at the interface leading to the creation of interface defects. From [71].

the increase in the carrier flux along the channel. This makes HCD even more complex due to the simultaneous action of the two electric field components. Therefore, one can conclude that HCD has one more degree of freedom than BTI. For example, in a MOSFET, when the drain to source voltage becomes comparable or greater than the gate voltage, the inversion layer is no longer homogeneous along the channel and the carrier concentration is higher near the source. In the saturation region pinch-off occurs at the drain side. This results in a high field region near the drain leading to an increased energy of the carriers travelling from the source to the drain. These high energy carriers strike the interface breaking the Si-H bonds [72]. Additionally, the energetic carriers may lead to generation of electrons and holes by impact ionization which further facilitate Si-H bond breakage [1]. This leads to the creation of interface defects and/or charging of the already present defects, see Figure 1.4. Some of the carriers with sufficient energy to overcome the energy barrier might get injected in the oxide and create or charge oxide defects.

The high electric field near the drain region causes strong localization of the HCD near the drain or the pinch-off region as has been reported in various studies [73, 1, 5, 7]. This localization of damage is another factor that distinguishes HCD from BTI. In modern scaled devices as well as in high voltage devices, the channel hot-carrier degradation is the main regime among the many regimes of HCD identified in literature. Other HCD mechanisms are drain avalanche, secondary generated hot-carrier, substrate hot-carrier, Fowler-Nordheim and direct tunneling [1, 74]. Drain avalanche and secondary generated hot-carrier mechanisms occur due to electron-hole pair generation from impact ionization, see Figure 1.5. Substrate hot-carrier degradation originates from injection from the channel-substrate p-n junction [75]. In Fowler-Nordheim emission, the carriers overcome the triangular potential barrier and are injected into the $SiO_2$ conduction band, while in direct tunneling carriers tunnel to the channel overcoming the trapezoidal potential barrier. Both Fowler-Nordheim and direct tunneling are quantum mechanical effects and are observed in scaled devices. Note that direct tunneling is observed in very thin oxides while

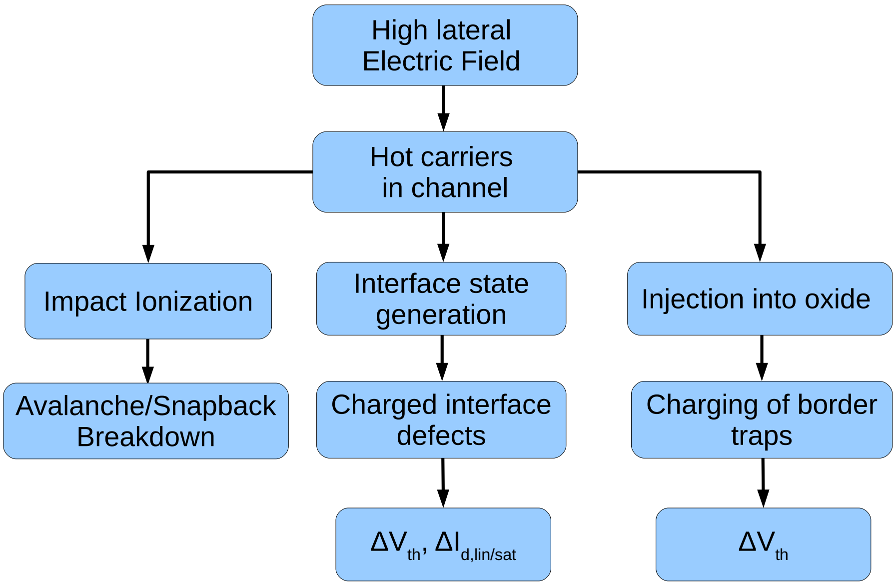

Figure 1.5: Steps involved in hot-carrier degradation

Fowler-Nordheim tunneling can occur in thicker oxides but requires a higher applied potential. Although HCD is a more general term, in this work it will be used to refer to the channel hot-carrier degradation mechanism.

The dominance of interface trap generation in hot-carrier degradation has been universally accepted for almost all technologies [76, 77, 1, 25]. Several stress and recovery measurements, see [78], show the absence of a recoverable component in HCD which leads to a controversy regarding the contribution of oxide traps as discussed in Section 1.1. The recovery in device degradation measurements is attributed to $N_{\mathrm{ot}}$ traps, whereas no recovery indicates pure $N_{\mathrm{it}}$. Moreover, many studies suggest an absence of oxide trap contribution to HCD [79, 80, 81]. NBTI and HCD also differ in their response to elevated temperatures. While NBTI is found to worsen with a rise in temperature for all devices [68], HCD becomes less pronounced in long-channel/high-voltage devices with increase in temperature [82, 83, 84]. For scaled devices, on the other hand, HCD aggravates at high temperature as electron-electron scattering populates the high energy fraction of the ensemble [85, 86]. Alternatively, the importance of electron-electron scattering in HCD has been disputed by others [87] and the cause for the increase in HCD is attributed to a mixed-mode process [87]. Recently, HCD was found to decrease at elevated temperatures in MOSFETs with SiON gate dielectric [88]. At low stress voltages, the degradation was observed to be less severe with increasing temperature, while at higher voltages no change in degradation was observed with increase in temperature. This behavior was explained as being due to different thermal responses of the two bond breakage mechanisms. The rate of the multiple-carrier process was found to decrease and the rate of the single-carrier process increased with increasing temperature [88]. In a few other investigations, HCD accelerated by self-heating has been suggested to be an important reliability concern in modern devices [89, 90]. Thus, there are a number of complex factors that collectively

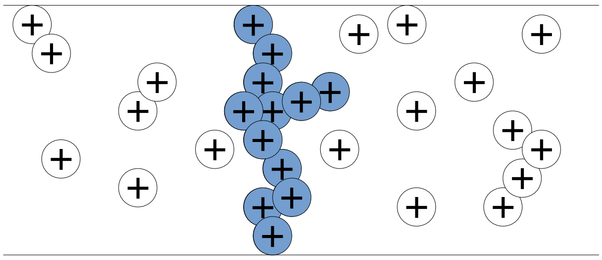

Figure 1.6: Development of a percolation path in a dielectric resulting in its breakdown.

contribute to HCD

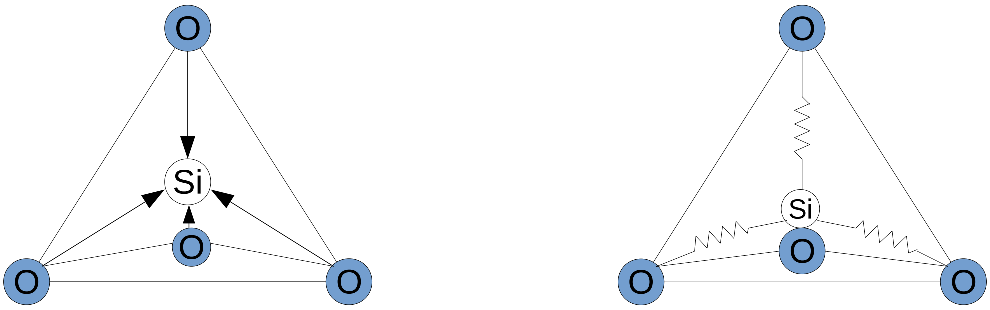

Figure 1.7: The tetrahedral $SiO_2$ structure with the arrows indicating the direction of the Si-O bond dipole moment. The strained bond is also shown where the distortions in the bond are induced by the electric field.

and need to be considered in modeling. The situation becomes even more complex when BTI mixes with HCD [91].

A comprehensive summary of widely used HCD models is presented in Chapter 3. A majority of these models are empirical while a few are physics based. However, a common feature among all modeling attempts is the interface state creation process which is controlled by the manner how the carriers are distributed over energy. Thus, the carrier energy distribution is the most important ingredient in modeling of HCD.

## 1.3 Time Dependent Dielectric Breakdown

Silicon dioxide, the native oxide of Si, has been traditionally used as dielectric in Si based devices due to its large bandgap and its high breakdown field. However, application of

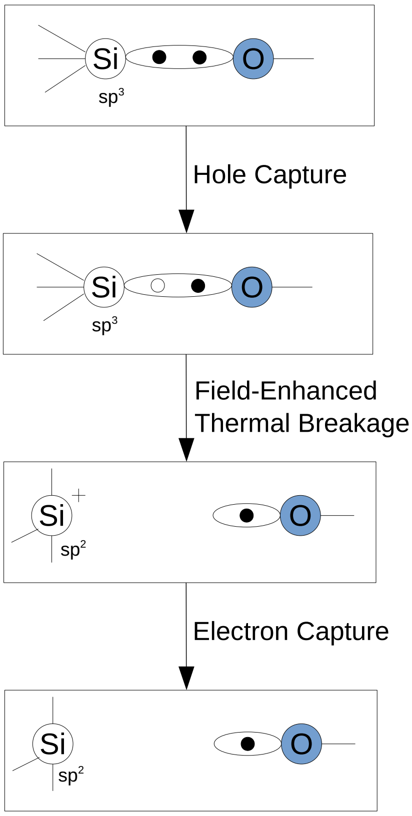

Figure 1.8: The hole-catalyzed, field-enhanced bond breakage process. A hole-capture event weakens the bond which can then be broken thermally or by a high electric field, thus, creating a defect. From [93] .

stress, such as high electric field, for long stress times can cause the dielectric to loose its insulating property. Moreover, the continuous down-scaling of transistors causes high electric fields across the dielectric which further increase the risk of failure. Dielectric breakdown can be intrinsic or extrinsic. Intrinsic breakdown occurs due to the structure of the dielectric material like crystal defects, dielectric thickness, etc. Extrinsic breakdown, on the other hand, can be caused by introduction of defects during the technological steps to manufacture the device.

Time dependent dielectric breakdown (TDDB) is observed in devices which use silicon dioxide or high-K materials. TDDB refers to the transition of the insulator from its insulating phase to a conductive phase with time when a constant electric field, smaller than the breakdown field, is applied. While the complete molecular picture is still speculative, the phenomenon is often attributed to the polar nature of the dielectric [92]. In $SiO_2$, local electric fields cause distortion in the silicon-oxygen bond leading to the possible creation of an oxygen vacancy (dangling bond) via bond breakage or coordination breakage. The coordination breakage refers to displacement of the Si ion from the fourfold coordination to a threefold coordination in the tetrahedral $SiO_2$. The coordination breakage requires much less energy than bond breakage and is considered the primary mechanism behind TDDB [93]. TDDB stress leads to generation of traps which create a percolation path, as shown in Figure 1.6, which triggers the breakdown of the insulator [94]. Time dependent dielectric breakdown can only be described statistically as nominally identical devices subjected to the same stress break down at different times. This is also the case for BTI and HCD in scaled devices. Thus, the failure probability has to be described statistically. This description allows to extract the device lifetime [95].

Breakdown in oxides thicker than 5 nm occurs abruptly after a certain electric field. Thus, a large jump in the voltage/current vs. stress time curve is observed. This effect is known as hard breakdown. In thinner oxides, on the other hand, soft breakdown occurs where the change in voltage/current with stress time is not very abrupt and the magnitude of change is many orders lower than in hard breakdown [43, 96].

Various TDDB models which consider field-induced degradation, current-induced degradation or a combination of both have been suggested [93, 97, 98, 99]. The field dependent models suggest the logarithm of time to breakdown to be proportional to the oxide electric field. One of these models is the thermochemical $E$-model. Within this model, bond breakage is triggered by the interaction of the Si-O bond, which is strained due to the local field (see Figure 1.7), with the lattice [97]. Thus, the bond breakage is considered to be a phonon driven process. The time to breakdown is given as $t_{\mathrm{BD}} = A_0 \exp\left[\gamma E_{\mathrm{ox}}\right] \exp\left[E_{\mathrm{a}}/k_{\mathrm{B}}T\right]$. However, the $E$-model was unable to explain the polarity dependence of TDDB [100].

The current driven model is the so-called $1/E$ model (the logarithm of time to breakdown is inversely proportional to the oxide electric field) where the damage is associated with the current flowing through the dielectric [93]. According to the $1/E$ model, the electrons tunneling through the dielectric from the cathode to the anode excite an electron from the valence band to the conduction, and leave a hole behind [101, 102]. On gaining energy, the holes can tunnel back into the oxide and create oxide traps. Thus, this model is also called Anode Hole Injection model (AHI). Emission of carriers through $\mathrm{SiO}_2$ is due to Fowler-Nordheim (FN) tunneling which requires high fields ($>$6 MV/cm) [103]. The $1/E$ dependence of time to breakdown is given as $t_{\mathrm{BD}} = \tau_0 \exp\left[G/E_{\mathrm{ox}}\right]$. If deep traps exist, trap assisted tunneling can lead to pre FN conduction. Since FN conduction is temperature independent, the current model was unable to explain the temperature dependence of TDDB [104]. Moreover, according to this model, breakdown occurs when a critical hole fluence is reached which has no physical explanation [105].

Other models for specific devices, such as the power-law voltage model [106, 107, 108] for thin dielectrics with transport in the ballistic regime and the exponential model [109, 110] for low-k dielectrics, have also been proposed. It has been suggested that TDDB can be better explained by a combination of field and current driven approaches [42, 111]. This combination suggests that the field strains the Si-O bonds which can then be excited by the carriers constituting the current flow. Figure 1.8 shows one of these scenarios where the bond breakage process is hole-catalyzed and enhanced by the field. Thus, the activation energy is reduced and the bond can be easily broken by phonon interactions. The combination of both field- and current-based models seems the most practical solution for modeling TDDB.

# Chapter 2

# Hot-Carrier Degradation

The semiconductor device fabrication process requires the growth of a dielectric, such as amorphous silicon gate oxide ($SiO_2$) or high-k dielectric such as $HfO_2$, on the crystalline silicon bulk/substrate (Si). The lattice mismatch at the interface of the dielectric and the substrate induces mechanical stress, leaving some of the Si atoms unsaturated. In other words, some Si atoms do not form four bonds with neighboring atoms to complete the octet. As a result, they carry up to two unpaired electrons, thereby creating two trap levels in the Si bandgap. This corresponds to electrically active Si dangling bonds which are visible in paramagnetic spin-resonance experiments [112, 113]. A large number of the unsaturated Si bonds are passivated with H gas during post-grow anneal. This creates electrically inactive Si-H bonds at the interface and shifts the corresponding energy levels out of the Si bandgap [114, 115]. However, during stress/operation of the device at high electric fields, carriers with high energies (as shown in Figure 1.4) can break the Si-H bonds, thereby creating interface traps. These defects at the interface are characterized by a density called the interface state density $N_{\mathrm{it}}$ ($\mathrm{cm}^{-2}$), which represents the number of interface traps per unit area or $D_{\mathrm{it}}$ ($\mathrm{cm}^{-2}\ \mathrm{eV}^{-1}$), the number of interface traps per unit area distributed across the energy bandgap [39]. The electrically active interface defects lead to

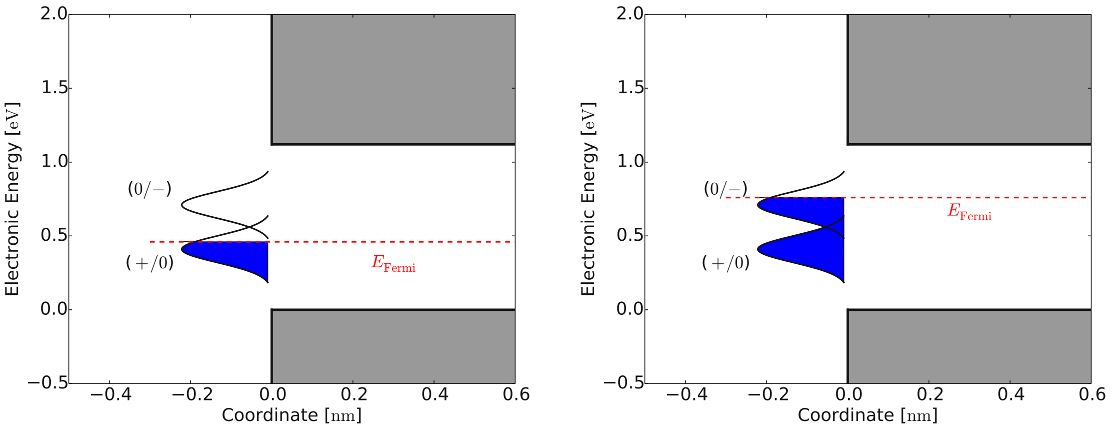

Figure 2.1: Interface trapped charge depending on the Fermi level. The traps between $E_{\mathrm{i}}$ and $E_{\mathrm{F}}$ are occupied, while others are neutral. Traps are negatively charged if the Fermi level is above $E_{\mathrm{i}}$, and positively charged if the Fermi level is below $E_{\mathrm{i}}$.

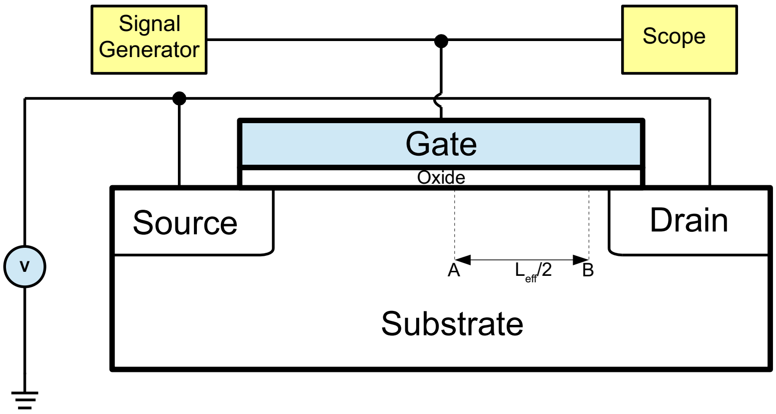

Figure 2.2: Charge pumping measurement setup. The source to substrate and drain to substrate diodes are typically slightly reverse biased while the gate is pulsed between inversion and accumulation conditions. The substrate current is typically measured as the charge pumping current.

a threshold voltage shift ($\Delta V_\mathrm{t}$) and the degradation of the drain current ($\Delta I_\mathrm{d,lin}$, $\Delta I_\mathrm{d,sat}$), thus, limiting the lifetime of the device. The traps also contribute to the leakage current and low frequency noise, thereby further disrupting the device functionality.

The charge stored in the traps depends on their position with respect to the Fermi level and thus on the bulk material, bias and temperature conditions, see Figure 2.1. The states between the intrinsic level ($E_\mathrm{i}$) and the valence band ($E_\mathrm{V}$) are filled with electrons and are donor-like as in a p-type substrate. On the other hand, the states between conduction band edge ($E_\mathrm{C}$) and $E_\mathrm{i}$ are acceptor-like as in a n-type substrate [116]. For instance, in the case of flatband conditions, if the Fermi level ($E_\mathrm{F}$) is between $\mathrm{E_C}$ and $E_\mathrm{i}$, the traps below $E_\mathrm{F}$ accept an electron to complete the octet and thus are negatively charged similar to occupied acceptors. Other states carry one unpaired electron and are neutral. On the other hand, if the Fermi level shifts below $E_\mathrm{i}$, the traps between $E_\mathrm{i}$ and $E_\mathrm{F}$ loose an electron and are positively charged (unoccupied donors) while other states stay neutral being populated by electrons [39].

To sum up, interface traps are charged when they are donor-like and donate electrons (positively charged traps) or if they are acceptors and accept electrons (negatively charged traps). Otherwise the traps are neutral and benign. The traps that are charged create fields which interfere with the electrical properties of the devices. As the trap density increases during the course of device operation, the number of charged traps also increase ultimately leading to the device breakdown.

## 2.1 Measurement Techniques

Since success of a technology node depends on the quality of the material and interface, determining the spatial distribution of the defects is vital. Modeling a degradation phe-

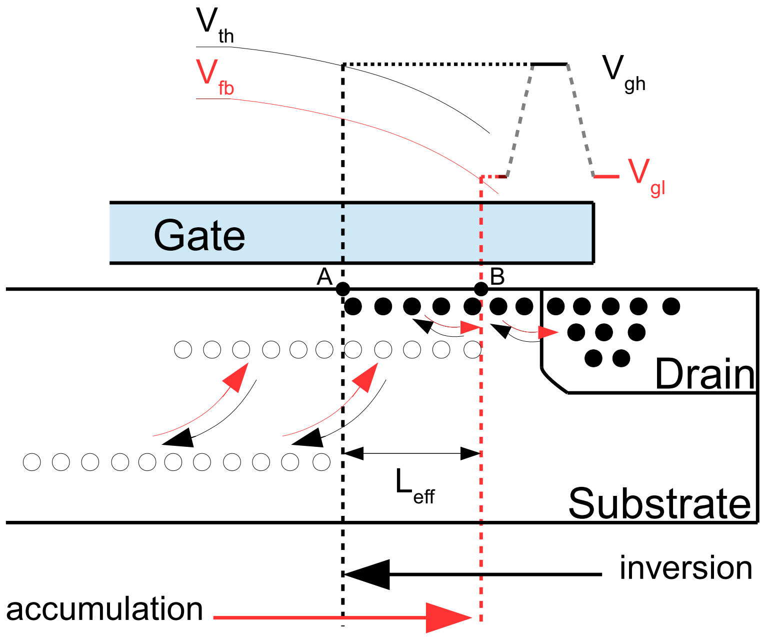

Figure 2.3: Generation of charge pumping current on application of a rectangular gate pulse. Arrows represent the carrier flow during inversion (black) and accumulation (red).

nomenon in semiconductor devices to evaluate their performance and lifetime requires the quality of the interface to be precisely characterized. Several signatures of the interfacial Si-H bond can help determine the interface state density. These include the $SiO_2/Si$ interface charges through their distortion of the electrostatics, drain-source currents originating due to interface trap states and hopping of the carriers, and the recombination current. Several techniques are used for spatially locating the interface states and tracking their evolution during stress conditions. [117, 118, 119, 120, 121]. Some widely used methods, namely the charge pumping, capacitance-voltage characteristics, and the conductance technique are explained below.

### 2.1.1 Charge Pumping

When periodic pulses are applied to the gate of a metal-oxide-semiconductor transistor, the recombination of carriers trapped by the interface states present in the channel region of the device produces the charge pumping current [118, 119]. A simple setup for the charge pumping method is shown in Figure 2.2. The gate is pulsed between accumulation and inversion conditions with the reverse biased substrate-source and substrate-drain p-n junctions. The charge pumping current produced from recombination is measured at the substrate. Alternatively, the current can be measured at the source/drain connection or at source and drain separately.

The recombination takes place in the $L_{\text{eff}}$ region, see Figure 2.2. Thus, the experimental

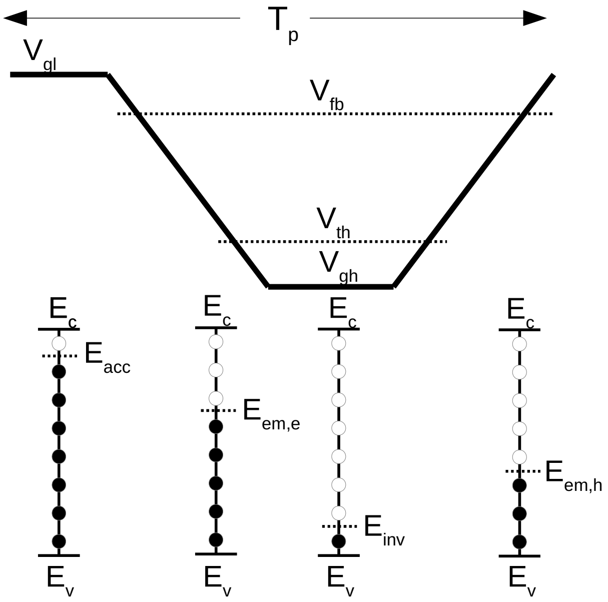

Figure 2.4: Evolution of the occupancy of interface states during one gate pulse cycle, $T_\mathrm{p}$. Traps lie in the band-gap between the valence band $E_\mathrm{v}$ and conduction band $E_\mathrm{c}$. Only the traps between the energy levels $E_\mathrm{em,e}$ and $E_\mathrm{em,h}$ contribute to the charge pumping current.

charge pumping current is the average recombination current originating from the $L_\mathrm{eff}$ region in the channel. The generation of charge pumping current is described in Figure 2.3. When the gate voltage approaches inversion, the interface is flooded, up to a certain distance, with minority carriers from the drain and source regions. Considering the drain side in Figure 2.2, the interface is flooded with minority carriers up to some distance $A$ (measured from the drain) during inversion. The majority carriers are swept into the substrate. Consequently, the interface states in this region capture minority carriers and are devoid of majority carriers. When the gate voltage approaches accumulation, the minority carriers travel back to the drain and majority carriers move from the substrate to the interface and reach point $B$ (measured from drain) with $B < A$. In the region $L_\mathrm{eff}/2$ $(A - B)$, recombination takes place, which leads to the charge pumping current. Outside this region, the supply of either electrons or holes is insufficient for recombination to take place.

It is worth mentioning that not all the electrons/holes captured by interface states in the $L_\mathrm{eff}$ region contribute to the recombination current [118, 119]. This is explained in the following example of constant high level charge pumping in a pMOSFET, Figure 2.4. During accumulation (positive $V_\mathrm{gl}$), most of the interface states are filled with electrons up to the accumulation energy level $E_\mathrm{acc}$. As the interface moves from accumulation into weak inversion (from flatband voltage $V_\mathrm{fb}$ to threshold voltage $V_\mathrm{th}$) via depletion, electrons are emitted from the traps back into the substrate due to thermal emission. When the threshold voltage is reached, all the states with energy greater than $E_\mathrm{em,e}$ are devoid of electrons. As the interface turns into inversion mode (negative $V_\mathrm{gh}$), holes flood in from

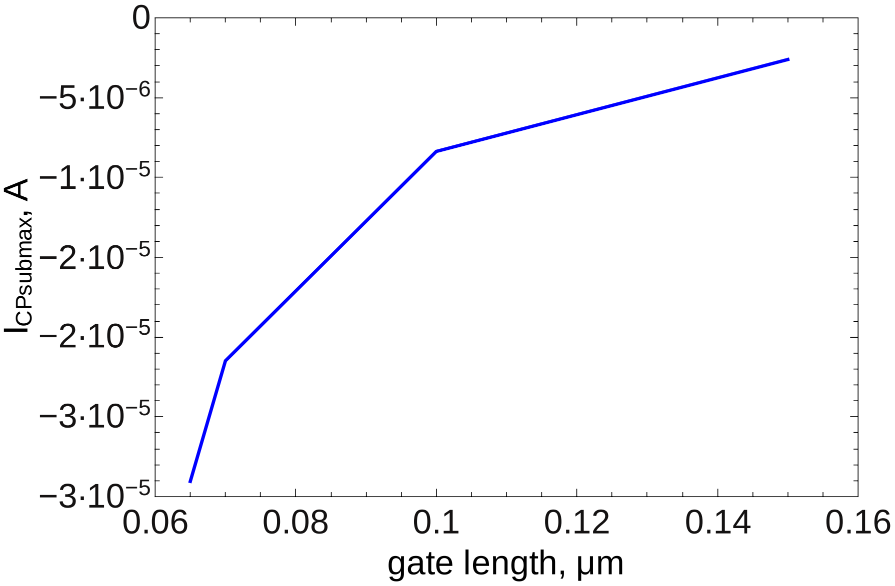

Figure 2.5: The maximum charge pumping current for nMOS devices with different channel lengths for a 65nm CMOS process.

the source and drain leading to emptying of traps via hole capture up to an energy level $E_{\mathrm{inv}}$. As the gate voltage increases back towards accumulation, holes move back to source and drain and the traps below a certain energy level, $E_{\mathrm{em,h}}$, are filled with electrons via hole emission. The interface states above this energy level are filled by electrons captured during accumulation. Thus, only the fast traps between $E_{\mathrm{em,e}}$ and $E_{\mathrm{em,h}}$ in the Si bandgap contribute to the charge pumping current. These energy levels can be calculated as [118]:

$$\begin{aligned} E_{\mathrm{em,e}} =& E_{\mathrm{i}} - k_{\mathrm{B}}T \ln\left(v_{\mathrm{th}}\sigma_{\mathrm{e}}n_{\mathrm{i}}t_{\mathrm{em,e}} + \exp\left(\frac{E_{\mathrm{i}} - E_{\mathrm{F,inv}}}{k_{\mathrm{B}}T}\right)\right) \qquad (2.1)\\ =& E_{\mathrm{i}} - k_{\mathrm{B}}T \ln\left(v_{\mathrm{th}}\sigma_{\mathrm{e}}n_{\mathrm{i}}\left|\frac{V_{\mathrm{th}} - V_{\mathrm{fb}}}{\Delta V_{\mathrm{g}}}\right| t_{\mathrm{r}}\right),\\ E_{\mathrm{em,h}} =& E_{\mathrm{i}} + k_{\mathrm{B}}T \ln\left(v_{\mathrm{th}}\sigma_{\mathrm{h}}n_{\mathrm{i}}t_{\mathrm{em,h}} + \exp\left(\frac{E_{\mathrm{F,acc}} - E_{\mathrm{i}}}{k_{\mathrm{B}}T}\right)\right) \qquad (2.2)\\ =& E_{\mathrm{i}} + k_{\mathrm{B}}T \ln\left(v_{\mathrm{th}}\sigma_{\mathrm{e}}n_{\mathrm{i}}\left|\frac{V_{\mathrm{th}} - V_{\mathrm{fb}}}{\Delta V_{\mathrm{g}}}\right| t_{\mathrm{f}}\right), \end{aligned}$$

where, $E_{\mathrm{i}}$ is the intrinsic energy level, $E_{\mathrm{F,inv}}$ and $E_{\mathrm{F,acc}}$ are Fermi energies in inversion and accumulation, $v_{\mathrm{th}}$ is the thermal velocity, $\sigma_{\mathrm{e/h}}$ the capture cross section of the traps, and $n_{\mathrm{i}}$ the intrinsic carrier concentration. Outside this band, thermal emission is the most prominent source of de-trapping.

Once the charge pumping currents are measured, $N_{\mathrm{it}}$ can be extracted using the steps described below. As an example, sample measurement data for a 65 nm nMOS transistor at temperature of 25 °C is used. For this temperature, the device was stressed for eight different times and the charge pumping current was measured using the constant base level and fixed high level techniques.

As a first step in the $N_{\mathrm{it}}$ extraction procedure, it is important to determine whether the initial interface state distribution is uniform, non-uniform or locally uniform. The charge

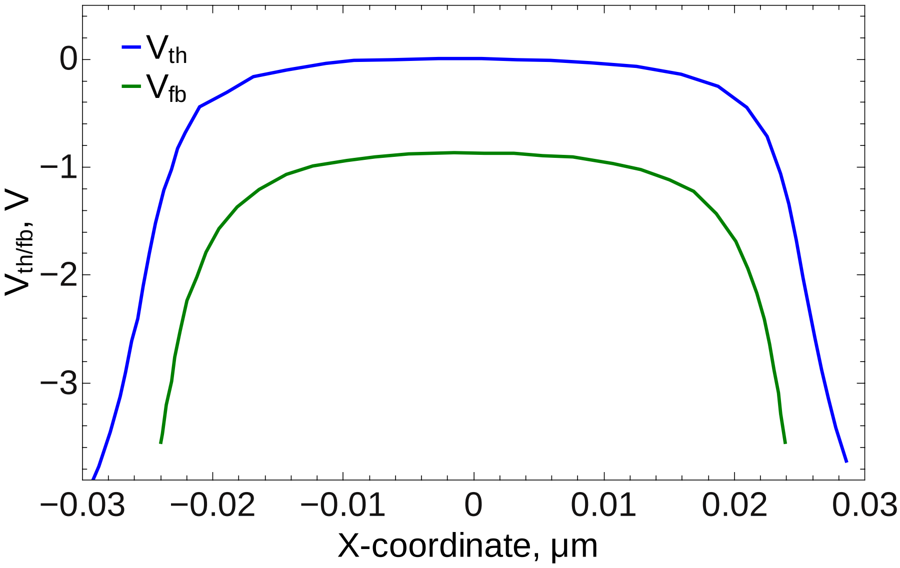

Figure 2.6: Threshold and flatband voltage profiles obtained from MINIMOS-NT using the criterion in Equation 2.3.

pumping current measurements for unstressed devices created using the same process but having different gate lengths can provide information on the nature of the $N_{\mathrm{it}}$ distribution. The maximum charge pumping current versus the gate length curve for 65 nm nMOS devices used in this example and longer gate length transistors created on the same process are shown in Figure 2.5. Figure 2.5 suggests that the interface state profile for a fresh transistor considered here is non-uniform as the increase in the interface state density is not proportional to the increase in the channel length [122]. However, the pre-stressed $N_{\mathrm{it}}(x)$ profiles are significant only when HCD is not very strong, i.e., for low stress times and biases. Due to the high interface state density after severe stresses, the contribution of the pre-stress $N_{\mathrm{it}}(x)$ profile to the total interface state density becomes negligible.

Second, the local threshold and flatband voltages are calculated for the unstressed device, see Figure 2.6. For an nMOS device, the local threshold voltage at a certain coordinate of the interface is defined as the gate voltage at which the traps can capture the minority carriers during inversion. On the other hand, the local flatband voltage at a certain coordinate of the interface is defined as the gate voltage at which the traps can capture the majority carriers during accumulation [123]. Hence, these voltages are derived using the dynamics of the capture and emission process at the interface. For the sample device, our device and circuit simulator MINIMOS-NT [124, 125] was used to obtain the threshold and flatband voltages. MINIMOS-NT employs a comprehensive set of physical models to provide steady-state, transient, and small-signal analysis of the devices. The required electron/hole concentration for the interface states to capture electrons/holes can be estimated by:

$$n_{\mathrm{e/h}} = \frac{1}{v_{\mathrm{th}}\sigma_{\mathrm{e/h}}\tau_{\mathrm{e/h}}}, \tag{2.3}$$

where $v_{\mathrm{th}}$ is the thermal carrier velocity, $\tau_{\mathrm{e/h}}$ the time constant for electron/hole trapping,

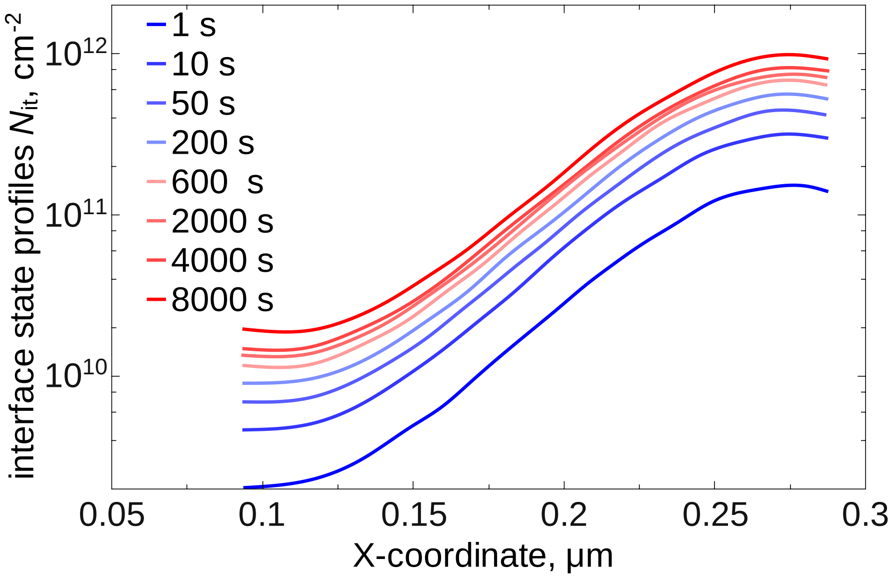

Figure 2.7: Lateral interface state profiles for eight stress times obtained using Equation 2.6 for a 65 nm nMOS stressed at $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 2.2\,\mathrm{V}$. The origin (X=0) is at the center of the channel.

and $\sigma_{\mathrm{e/h}}$ the capture cross section for electrons/holes.

Once the threshold voltage profile is obtained, the interface state profiles can be deduced using the expression:

$$I_{\mathrm{CP}} = \frac{qW}{T_{\mathrm{P}}} \int_{L_{\mathrm{eff}}} N_{\mathrm{it}}(x) \cdot \mathrm{d}x \tag{2.4}$$

where $I_{\mathrm{CP}}$ is the time averaged recombination (charge pumping) current, $W$ the width of the interface, and $T_{\mathrm{P}}$ the time period. Through this method, the $N_{\mathrm{it}}(x)$ profiles over a certain distance $L_{\mathrm{eff}}$ can be extracted as already discussed. So for Equation 2.4, the $I_{\mathrm{CP}}$ corresponding to the maximum $L_{\mathrm{eff}}$ $/V_{\mathrm{gh}}$ is used to obtain the $N_{\mathrm{it}}$ over a maximum distance along the interface. Calculating $N_{\mathrm{it}}(x)$ from equation Equation 2.4 proceeds by differentiating the equation on both sides. Thus,

$$\frac{\mathrm{d}I_{\mathrm{CP}}}{dx} = \frac{qW}{T_{\mathrm{P}}} N_{\mathrm{it}}(x), \tag{2.5}$$

rewritten as

$$\frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}V_{\mathrm{gh}}} \frac{\mathrm{d}V_{\mathrm{gh}}}{\mathrm{d}x} = \frac{qW}{T_{\mathrm{P}}} N_{\mathrm{it}}(x), \tag{2.6}$$

or

$$\frac{\mathrm{d}I_{\mathrm{CP}}}{\mathrm{d}V_{\mathrm{gh}}} \frac{\mathrm{d}V_{\mathrm{th}}}{\mathrm{d}x} = \frac{qW}{T_{\mathrm{P}}} N_{\mathrm{it}}(x). \tag{2.7}$$

Here $\mathrm{d}V_{\mathrm{th}}/\mathrm{d}x$ can be considered similar to $\mathrm{d}V_{\mathrm{gh}}/\mathrm{d}x$ as the condition for the threshold voltage. In Equation 2.3, the threshold voltage is reached at $V_{\mathrm{gh}}$.

The interface state profiles obtained using this procedure (Equation 2.6) for different stress times are shown in Figure 2.7. The extracted $N_{\mathrm{it}}(x)$ profiles were used to simulate

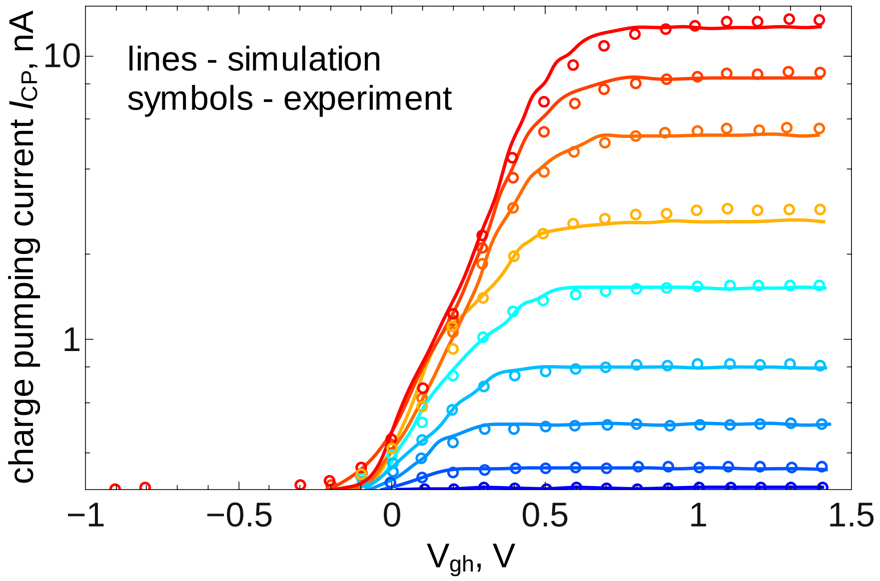

Figure 2.8: Comparison of simulated and experimental charge pumping currents after different stress conditions.

a degraded device and calculate the charge pumping currents in Minimos-NT. The comparison of charge pumping currents obtained from simulation with those from experiments are shown in Figure 2.8 for several stress conditions.

### 2.1.2 Capacitance-Voltage Characteristics

The Capacitance-Voltage (CV) method is another widely used technique to evaluate new processes, materials, and devices [126, 120]. The measurement setup is shown in Figure 2.9. In this method, the interface is swept through different regimes, i.e., accumulation, depletion and inversion, successively and the small signal capacitance is measured. In the accumulation regime, there are a large number of majority carriers at the interface. During depletion, the majority carriers move inside the bulk and only fixed charges remain at the surface which build up the depletion layer. This results in a decrease of the total capacitance. When the semiconductor-insulator interface reaches the inversion mode, the minority carriers populate the surface and balance the gate charge. The total capacitance of the device is a combination of the depletion layer and inversion layer capacitance. The total space charge density can be expressed as $Q_{\mathrm{SC}} = Q_{\mathrm{d}} + Q_{\mathrm{n}}$, where $Q_{\mathrm{d}}$ and $Q_{\mathrm{n}}$ are the deletion and inversion layer charge density, respectively [120]. An increase in the interface trap density $N_{\mathrm{it}}$ is followed by a deformation of the characteristics as the traps can dynamically be charged and discharged, while the fixed oxide charges shift the flat-band voltage. Therefore, the capacitance ($C$) is calculated as:

$$C = \frac{\mathit{\Delta} Q_{\mathrm{it}} + \mathit{\Delta} Q_{\mathrm{OX}}}{\mathit{\Delta} V_{\mathrm{th}}}. \tag{2.8}$$

where $Q_{\mathrm{it}}$ is the interface charge density and $Q_{\mathrm{OX}}$ the oxide charge density.

The frequency of the signal applied is very important to consider the contribution due to different regimes. For example, in a MOSCAP, if the signal has a high frequency, only

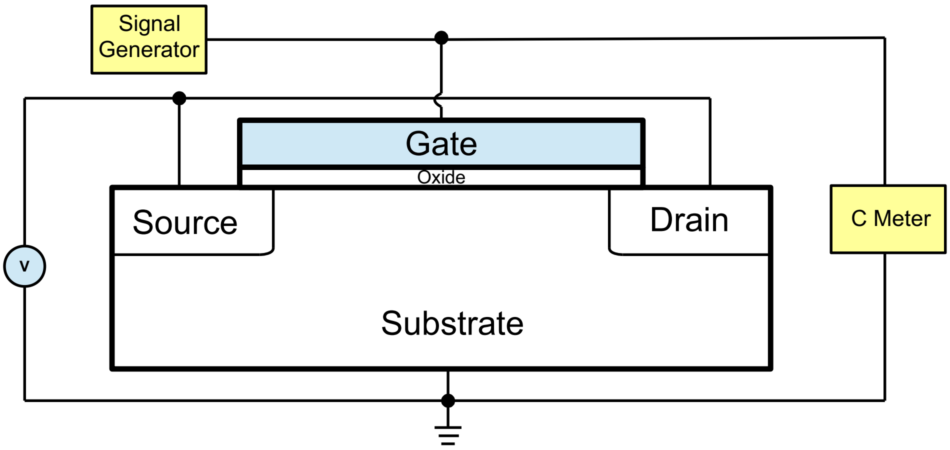

Figure 2.9: C-V measurement setup for a MOSFET.

the majority carrier response can be measured as the recombination-generation rates of the minority carriers cannot keep up with small signal variations at high frequencies. In the high frequency limit, the inversion layer charges cannot follow the AC signal. In this regime, the capacitance of the device will be determined by the depletion layer charge density alone [120]:

$$C = \frac{q\epsilon_{\mathrm{Si}}N_{\mathrm{A}}}{2\phi_{\mathrm{S}}}\frac{\mathrm{d}\phi_{\mathrm{S}}}{\mathrm{d}t}. \tag{2.9}$$

This capacitance calculated from Equation 2.9, using the doping concentration ($N_{\mathrm{A}}$), surface potential ($\phi_{\mathrm{S}}$), and permittivity of silicon ($\epsilon_{\mathrm{Si}}$), is used to evaluate the density of charges stored in interface traps. The interface charge density enters Equation 2.9 via the rate of change of the surface potential $\mathrm{d}\phi_{\mathrm{S}}/\mathrm{d}t$ calculated from $E_{\mathrm{g}}/q + \chi - \phi_{\mathrm{S}} - v_{\mathrm{n}} + V = -\frac{\delta}{\epsilon_{\mathrm{i}}}\left[Q_{\mathrm{d}} + Q_{\mathrm{n}} + Q_{\mathrm{it}} + qN_{\mathrm{f}}\right]$, where $E_{\mathrm{g}}$ is the band gap, $\chi$ the electron affinity, $v_{\mathrm{n}}$ the carrier velocity, $V$ the applied bias, $Q_{\mathrm{it}}$ the interface charge density, and $N_{\mathrm{f}}$ the fixed charge density [120].

### 2.1.3 Conductance method

The conductance method is one the most sensitive methods to determine the interface trap density. This method depends on the analysis of the change in the charge state of the traps when a small AC voltage is superimposed on the DC gate bias. The modulated signal causes the position of the Fermi level to change with respect to the position of the interface states in energy. Thus, the occupancy of the interface states changes, leading to charge release which can be measured as a parallel conductance $G$. This conductance is measured as a function of frequency $\omega$. The conductance due to interface traps $G_{\mathrm{it}}$ is calculated using the measured capacitance $C$ and conductance $G$ as:

$$\frac{G_{\mathrm{it}}}{\omega} = \frac{\omega^2 C_{\mathrm{ox}}^2 G}{G^2 + \omega^2 (C_{\mathrm{ox}} - C)^2}, \tag{2.10}$$

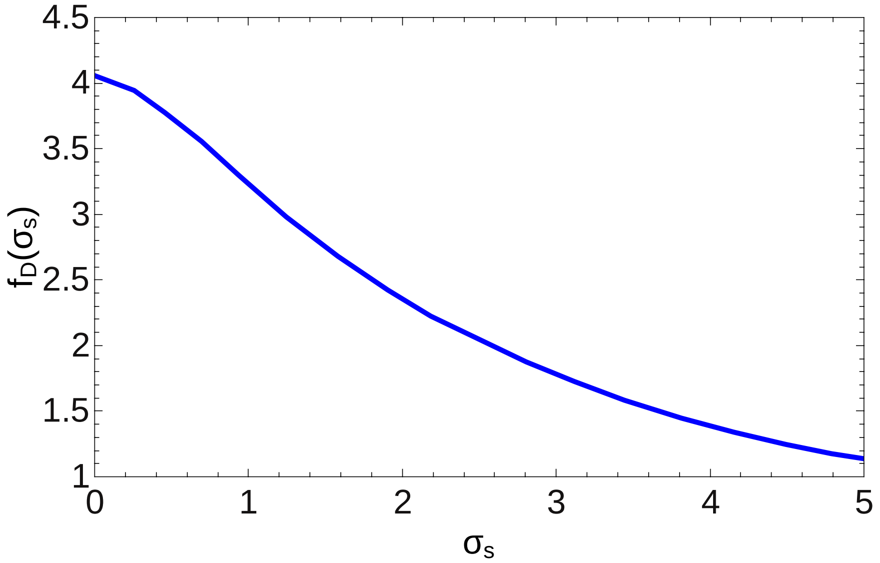

Figure 2.10: The universal function $f_\mathrm{D}(\sigma_\mathrm{s})$ used to calculate $D_\mathrm{it}$, plotted as a function of $\sigma_\mathrm{s}$ [128].

where $C_\mathrm{ox}$ is the oxide capacitance and $\omega$ is the angular frequency. The angular frequency $\omega$ is related to the characteristic trap response time $\tau = \exp\left[\Delta E/k_\mathrm{B}T\right]/\sigma v_\mathrm{th} D_\mathrm{dos} = 2\pi/\omega$ with $\sigma$, $v_\mathrm{th}$, $D_\mathrm{dos}$ being the trap capture cross section, carrier thermal energy, and density of states, respectively [127]. A plot of the normalized interface trap conductance $G_\mathrm{it}/\omega$ versus frequency has a maximum value corresponding to a peak frequency $f_\mathrm{p}$, implying maximum change in interface state occupancy which occurs when the interface traps are in resonance with the applied ac signal.

To calculate the interface trap density, the admittance is first measured at a fixed gate bias in the depletion region from any of the two regions of the curve, i.e., above or below $f_\mathrm{p}$. The value of the universal function $f_\mathrm{D}$ is then determined using the standard deviation of band-bending ($\sigma_\mathrm{s}$) obtained from the curve [128, 129]. The interface state density is then calculated as [121]:

$$D_\mathrm{it} \approx \left[f_\mathrm{D}(\sigma_\mathrm{s}) q\right]^{-1} \left(\frac{G_\mathrm{it}}{\omega}\right)_\mathrm{max}. \tag{2.11}$$

Although the interface trap density can be directly deduced from measurements, the conductance method is not applicable to interfaces with a high interface state density such as in devices with high-k dielectrics. If the interface state capacitance $qD_\mathrm{it}$ becomes larger than the oxide capacitance, the measured impedance will be dominated by the oxide capacitance and $D_\mathrm{it}$ would be underestimated [130]. Another drawback of the conductance method arises during weak inversion, when the increase in conductance due to minority carrier generation-recombination may lead to overestimation of the interface trap density.

# Chapter 3

# A Review of Existing HCD Models

As already discussed, HCD is a major reliability concern in power MOSFETs, but deeply scaled devices are also susceptible to hot-carrier effects [131]. Modeling this phenomenon is difficult as the physical effects are not completely clear and involve many mechanisms occurring simultaneously. Moreover, modeling of HCD requires solving the carrier transport problem from the full-band Boltzmann transport equation which is computationally challenging and often leads to convergence issues in large area and high voltage devices. The models also have to cope with the ever changing semiconductor industry. For example, in the eighties, the focus was on shrinking the device dimensions, while the operating voltages were not significantly reduced. This development has led to devices with high electric fields in which the carriers were energetic enough to break the Si-H bonds in a single interaction [132, 133]. Thus, the supply voltages were scaled to reduce the electric fields in the devices [134]. Due to the low source-drain voltage in extremely scaled devices, HCD was expected to be drastically suppressed as described in [135, 136, 137]. Such a trend, however, was not observed [138] and even ultra-scaled MOSFETs were found to exhibit HCD [139, 137, 140]. This peculiarity was attributed to energy exchange mechanisms, such as the multiple-carrier process and electron-electron scattering [86, 10].

Particularly for ultra scaled devices, HCD becomes complicated due to the dominance of the multiple-carrier process of Si-H bond breakage [136, 135, 139]. However, the single- and multiple-carrier mechanisms are limiting cases and commonly a superposition of the two is present [141, 25]. The interplay between the two bond breakage mechanisms causes a shift in the worst-case conditions for HCD. Typically, the worst-case HCD was observed at $V_{\mathrm{gs}} \approx 0.5V_{\mathrm{ds}}$ which corresponded to the maximum substrate current [85, 142]. This is no longer valid even for long-channel devices where the worst-case damage is observed at maximum average carrier energy, i.e. conditions corresponding to the maximum gate current [143]. In scaled devices, on the other hand, the dominance of the multiple-carrier process requires the maximum carrier flux instead of the carrier energy for most severe HCD, which is obtained at $V_{\mathrm{gs}} \approx V_{\mathrm{ds}}$ [144, 145, 146]. It should be noted that high energy carriers exist also in ultra scaled devices due to processes like electron-electron scattering, so the single-carrier process cannot be ignored [11, 137]. Similarly, in long-channel devices the multiple-carrier process is important especially at higher stress times [147]. Apart from these characteristics, the temperature behavior of HCD is another important aspect to be understood. On the one hand, in long-channel devices hot-carrier damage decreases as the temperature increases. On the other hand, scaled devices show the opposite trend, exhibiting an increase in HCD with temperature. This trend in scaled devices is observed by increased electron-electron scattering which populates the high energy tail of the carrier distribution function [148, 137, 149, 88]. Thus, a comprehensive model should capture these features of HCD and must be necessarily based on the carrier distribution function. The carrier distribution function is the key aspect as it provides the information on the interaction of carriers with the bonds. In this respect, several attempts have been made to simplify the HCD modeling problem as discussed in the following.

The first attempt for HCD modeling was the lucky electron model [150] which introduced the field-driven approach [151, 152, 77, 153]. According to this model, a defect is produced by an electron having high enough energy to overcome the potential barrier at the interface and enter the $SiO_2$ conduction band without being emitted back into the oxide. This simple model predicted that carriers with energy greater than 3.7 eV lead to interface state generation. This was deemed incorrect by measurements where the degradation was found to occur even at lower stress voltages [85]. Although the application of the lucky electron model is limited to long channel devices, it is still a popular model due to its simplicity. Takeda *et al.* proposed an extension to the lucky electron model whereby the degradation, i.e. transconductance and threshold voltage shifts with time are represented by a power law $t^n$. Using this empirical approach, the device lifetime could be easily extrapolated from accelerated hot-carrier stress measurements to real operating conditions. However, the model is of limited applicability and inaccurate to represent HCD in devices where a saturation in degradation is observed [154]. Some other extensions of the lucky electron model are: the Goo model which can capture the saturation of degradation [154], the Dreesen concept which was proposed for lightly doped drain transistors [155, 153], the Woltjer approach which incorporates a field-driven correction in the lucky electron model [76, 77]. In the Woltjer model, consideration of the electric field within the oxide allowed the description of degradation due to interface states in devices with varied dimensions and oxide thicknesses.

Mistry *et al.* introduced three different modes of degradation, i.e., generation of interface and neutral oxide traps at low gate voltages, interface state generation at mid voltage range, and oxide electron trap build-up at high voltages [156, 152]. Although this model was unable to predict the device lifetime correctly and was of limited use, it led to the idea of multiple competing mechanisms for constituting the overall degradation [152]. An important model by Moens *et al.* considers two competing mechanisms for representing degradation in LDMOS transistors and used different time exponents to characterize these mechanisms [4].

A majority of these models were empirical or at the best phenomenological and usually had time exponents to fit the experimentally obtained degradation characteristics. Another shortcoming of these models was the consideration of the electric field as the driving mechanism, which is valid only for large devices. Thus, models describing the physical picture behind HCD which were based on energy driven approaches were required [85, 86, 10].

## 3.1 The Hess Model

The first physics-based model for HCD was proposed by Hess *et al.* who suggested the existence of two mechanisms for Si-H bond breakage, i.e. the single- and multiple-carrier processes sketched in Figure 3.1 [21, 135, 157]. The single-carrier mechanism leads to breakage of a Si-H bond when a solitary hot carrier interacts with the bond, transferring its energy and leading to an excitation of one of the bonding electrons to an antibonding

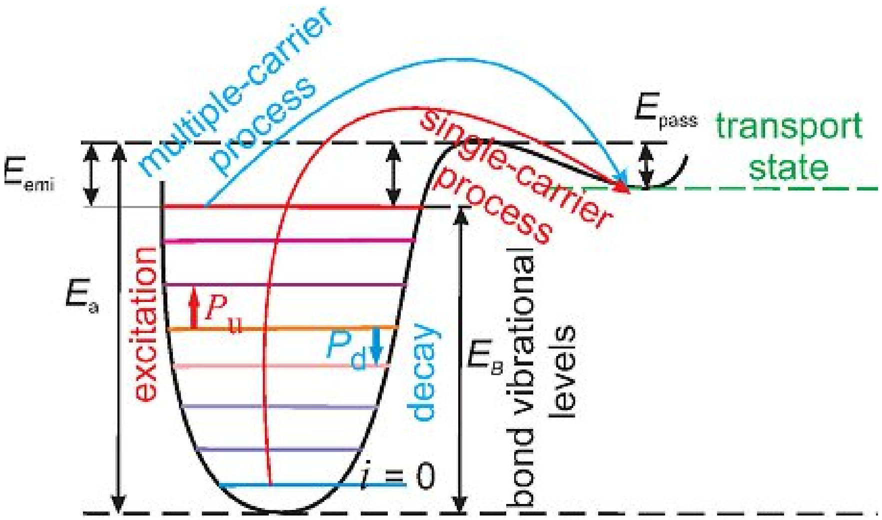

Figure 3.1: The Si-H bond as a truncated harmonic oscillator. $P_\mathrm{u}$ and $P_\mathrm{d}$ are the bond excitation and de-excitation rates, respectively, while $E_\mathrm{a}$ is the activation energy for bond dissociation. The hydrogen atom can be excited from the bonded state to the transport state via single- and multiple-carrier processes. $E_\mathrm{emi}$, and $E_\mathrm{pass}$ are the energy barriers for the transition from the highest bonded level to the transport state and for the passivation process, respectively [27].

state. Thus, a repulsive force is induced on the hydrogen atom and leads to hydrogen release. The bond breakage rate with the single-carrier process is given by [157]:

$$R_\mathrm{SP} = \int_{\varepsilon_\mathrm{th}}^{\infty} I(\varepsilon)P(\varepsilon)\sigma(\varepsilon)d\varepsilon, \tag{3.1}$$

where $I(\varepsilon)$ is the carrier flux in the energy range $[\varepsilon; \varepsilon + d\varepsilon]$, $P(\varepsilon)$ the probability of bond breakage, $\sigma(\varepsilon)$ the reaction cross section, and $\varepsilon_\mathrm{th}$ is the threshold energy the hot carrier should possess in order to initiate the bond breakage process.

The Hess formalism was successful in explaining the giant-isotope effect, i.e. different desorption rates of the hydrogen and deuterium from Si surfaces, observed experimentally [158, 159, 160]: In experiments with scanning tunneling microscopes (STM), hydrogen- and deuterium-passivated Si surfaces were bombarded by cold carriers from the tip of an STM. It was observed that much higher carrier current densities were required to break the Si-D bond as compared to Si-H. The bond breakage rates for the latter were found to be two orders of magnitude larger than the former at high voltages as shown in Figure 3.2. This effect was termed giant isotope effect and was explained by the multiple-carrier process.

Within this concept, the Si-H bond was modeled as a truncated harmonic oscillator comprising of an energy ladder, i.e. a system of eigenstates in the potential well. While interacting with colder carriers the bond can gain or loose energy, leading to its excitation or de-excitation, respectively, within the energetic states of the ladder. Such subsequent interactions with the carriers were linked to the excitation of the phonon modes. The bond is ruptured when the hydrogen leaves the highest energy level and overcomes the potential barrier $E_\mathrm{emi}$, thereby ending up in the transport mode, see Figure 3.1. The passivation process is defined as hydrogen jumping in the opposite direction over the barrier $E_\mathrm{pass}$.

The emission and passivation processes, characterized by the energies $E_{\mathrm{emi}}$ and $E_{\mathrm{pass}}$, respectively, are assumed to obey an Arrhenius law with corresponding rates $P_{\mathrm{emi}}$ and $P_{\mathrm{pass}}$. The excitation and decay rates of the bond ($P_{\mathrm{u}}$, $P_{\mathrm{d}}$, respectively) in the potential well are obtained by considering all combinations of phonon absorption (bond heating) and phonon emission (related to decay resulting from multiple-carrier process) which can be induced by the carrier flux [21, 157]

$$\begin{aligned} P_{\mathrm{u}} &= \int_{\varepsilon_{\mathrm{th}}}^{\infty} I(\varepsilon)\sigma_{\mathrm{ab}}(\varepsilon)\left[1 - f_{\mathrm{ph}}\left(\varepsilon - \hbar\omega\right)\right] \mathrm{d}\varepsilon, \\ P_{\mathrm{d}} &= \int_{\varepsilon_{\mathrm{th}}}^{\infty} I(\varepsilon)\sigma_{\mathrm{emi}}(\varepsilon)\left[1 - f_{\mathrm{ph}}\left(\varepsilon + \hbar\omega\right)\right] \mathrm{d}\varepsilon, \end{aligned} \tag{3.2}$$

with $I(\varepsilon)$ being the carrier flux, $\sigma_{\mathrm{ab/emi}}(\varepsilon)$ the reaction cross section for absorption/emission of phonons, $f_{\mathrm{ph}}$ the phonon occupation numbers, and $\hbar\omega$ the distance between energy levels. The bond breakage rate for the multiple-carrier process can then be estimated as:

$$R_{\mathrm{MC}} = \left(\frac{E_{\mathrm{B}}}{\hbar\omega} + 1\right)\left[P_{\mathrm{d}} + \exp\left(\frac{-\hbar\omega}{k_{\mathrm{B}}T_{\mathrm{L}}}\right)\right]\left[\frac{P_{\mathrm{u}} + \omega_{\mathrm{e}}}{P_{\mathrm{d}} + \exp\left(-\hbar\omega/k_{\mathrm{B}}T_{\mathrm{L}}\right)}\right]^{-E_{\mathrm{B}}/\hbar\omega}, \tag{3.3}$$

where $E_{\mathrm{B}} = E_{\mathrm{a}} - E_{\mathrm{emi}}$ is the energy of the last bonded state in the potential well, $\omega_{\mathrm{e}}$ the reciprocal phonon lifetime, $k_{\mathrm{B}}$ the Boltzmann constant, and $T_{\mathrm{L}}$ the lattice temperature.

The most important contribution of the Hess model was the consideration of the bond breakage process as a contribution of different carriers in the ensemble. Thus, the carrier distribution function was considered a major ingredient for a proper description of HCD. The DF enters the rate equations, Equations 3.1 and 3.2, via the carrier flux $I(\varepsilon)$ (see Section 4.4). The isotope effect was explained from the difference in energetics of the Si-H and Si-D bonds which led to different parameters (like phonon lifetime) of the quantum well for the two kind of bonds. The Hess model also considers the statistical distribution of the activation energy, $E_{\mathrm{a}}$, which was supported by density functional theory calculations [21, 161] and by experiments reporting a double power law of interface state generation as:

$$N_{\mathrm{it}} = \frac{p_1}{1 + (t/\tau_1)^{\alpha_1}} + \frac{p_2}{1 + (t/\tau_2)^{\alpha_2}}. \tag{3.4}$$

Here $\tau_1$, $\tau_2$ are the characteristic times, $\alpha_1$, $\alpha_2$ are the different time slopes, while $p_1$, $p_2$ are the probabilities related to the traps.

However, the microscopic Hess model was not translated to the macroscopic or device level and thus, prediction of the device lifetime and degradation characteristics such as transconductance, linear drain current, etc. was not addressed.

## 3.2 The Penzin Model

Penzin *et al.* tried to link the microscopic mechanisms suggested by the Hess model with the degradation characteristics of the device [22]. Within this model, the Si/SiO$_2$ interface is considered as a capacitor. Thus, Si-H bond dissociation leaving behind a depassivated bond and a charged hydrogen atom leads to an increased electric field in the capacitor. Due to this, the potential barrier between bonded and transport states increases. The bond-dissociation process is described by the kinetic equation:

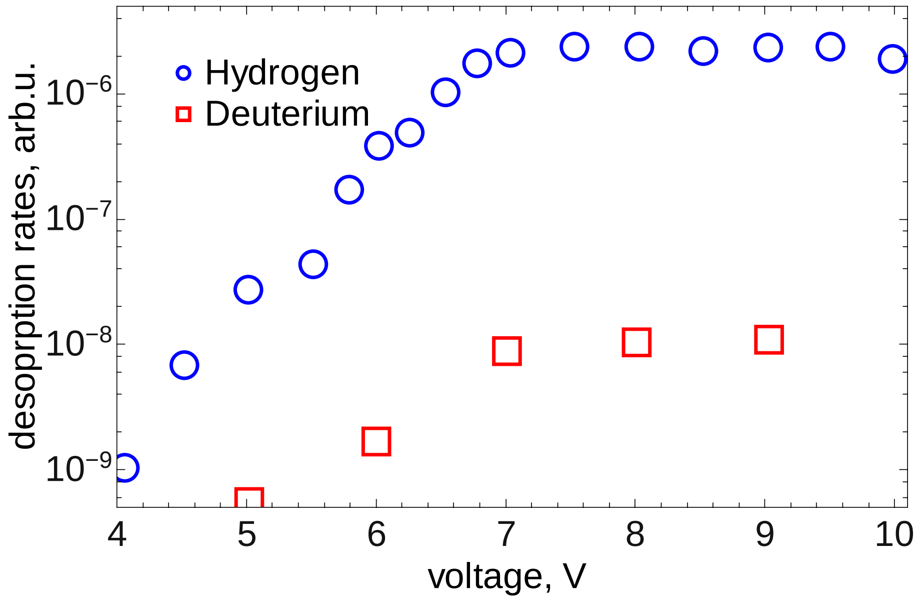

Figure 3.2: The giant-isotope effect: the desorption rates of hydrogen and deuterium atoms from passivated Si surfaces, as measured by an STM [158].

$$\frac{\mathrm{d}n}{\mathrm{d}t} = -kn + \gamma(N_0 - n), \tag{3.5}$$

with $n$ being the concentration of passivated Si-H bonds, $k$ the bond breakage rate, $\gamma$ the bond passivation rate, and $N_0$ the total concentration of Si-H bonds in the fresh device. The bond breakage rate $k$ is given by $k = k_0 \exp\left(-E_\mathrm{a}/k_\mathrm{B}T_\mathrm{L}\right) k_\mathrm{HC}$ where $k_0$ is the attempt frequency. The hot-carrier acceleration factor $k_\mathrm{HC}$ is defined as $k_\mathrm{HC} = 1 + \delta_\mathrm{HC} \left|I_\mathrm{HC}\right|^{\rho_\mathrm{HC}}$ where $\rho_\mathrm{HC}$ and $\delta_\mathrm{HC}$ are fitting parameters, and $I_\mathrm{HC}$ is the local hot-carrier current [22]. With such a formalism for the defect generation kinetics, the Penzin model could be used for TCAD device simulations.

As per the Penzin model, the activation energy increases with depassivation of the interfacial Si-H bonds and is given as:

$$\begin{aligned} E_{\mathrm{a}=}&E_\mathrm{a}^0 + \delta\left|E\right|^\rho + \beta k_\mathrm{B} T_\mathrm{L} \ln\frac{N_0 - n}{N_0 - n^0} \\ \beta =&1 + \beta_\perp E_\perp \end{aligned} \tag{3.6}$$

where $E_\mathrm{a}^0$ is the activation energy when there are no mobile hydrogen atoms, and $n^0$ the concentration of pre-existing mobile hydrogen atoms. The increase in the capacitor electric field normal to the interface, due to bond dissociation is denoted as $E_\perp$. The activation energy can also change due to stretching or squeezing the bond by an external electric field. This is represented by the term $\delta\left|E\right|^\rho$ in the expression for the activation energy, Equation 3.6.

The $N_\mathrm{it}$ concentrations simulated using the Penzin approach are shown in Figure 3.3. The simulated results compare quite well with the experimental ones. Similar to the Hess

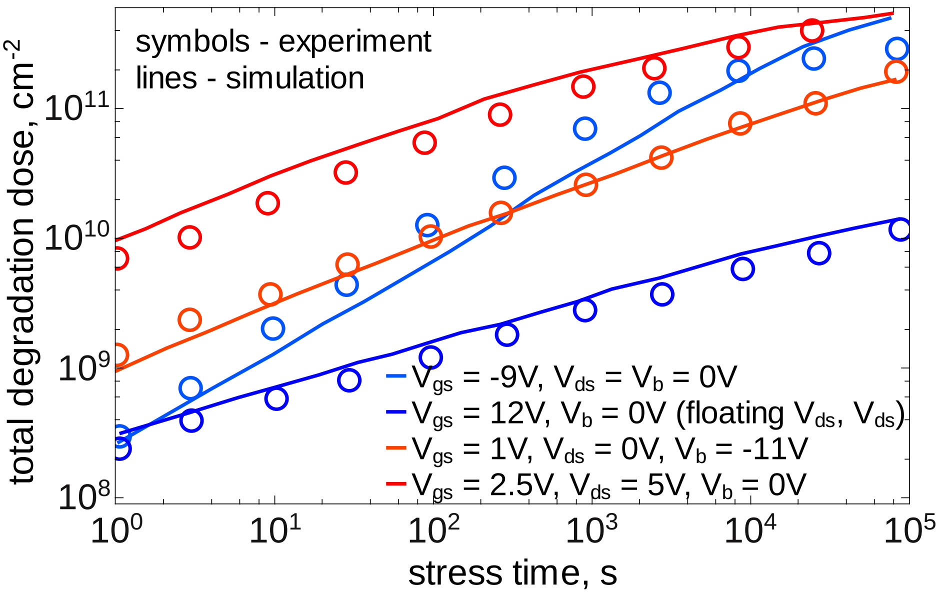

Figure 3.3: The cumulative interface state density $N_{\mathrm{it}}$ obtained with the Penzin model vs experimental ones for a hot-carrier stressed n-MOSFET. The gate length is $0.35\,\mu$m while the oxide thickness is $6.5\,$nm.

approach, the Penzin model considers the activation energy distribution which results in the sublinear slope seen in Figure 3.3. However, within this model, the carrier transport was not properly addressed and the $N_{\mathrm{it}}(x)$ profiles were not determined, except for some cumulative $N_{\mathrm{it}}$ shown in Figure 3.3. Also, the characteristics of the degraded device cannot be simulated with this approach.

## 3.3 The Reaction-Diffusion Model

Another attempt to model the physical process behind HCD was the application of the reaction-diffusion model developed for NBTI to HCD by Alam *et al.* [162, 163]. They assumed both NBTI and HCD to be involved in Si-H bond breakage with different driving forces, and tried to model the two phenomena using the same framework. However, the experimental $N_{\mathrm{it}}$ obtained from NBTI and HCD were found to have different times slopes as shown in Figure 3.4. The different stages in the reaction-diffusion model are summarized in Tab. 3.1. The degradation process starts with the reaction limited phase of Si-H bond breakage. In this phase, $N_{\mathrm{it}}$ increases linearly with time. During the second stage, no more interface states are generated and hydrogen diffusion begins. The third step comprises of a diffusion limited phase with $N_{\mathrm{it}}$ generation time slope of 1/4. In the next stage, hydrogen diffuses away with unlimited velocity and $N_{\mathrm{it}}$ depending on time as $t^{1/2}$. In the final phase, all the Si-H bonds are depassivated thus leading to saturation of interface states.

From Tab. 3.1 and Figure 3.4, it was inferred that NBTI is diffusion-limited while HCD is dominated by stage 4. The different slopes discussed above were explained by the RD model by considering the interface state density modeled as $N_{\mathrm{it}} = \int N_{\mathrm{H}}(r,t)\mathrm{d}^3r$ with $N_{\mathrm{H}}(r,t)$ being the coordinate-dependent density of H-atoms. Using the hydrogen

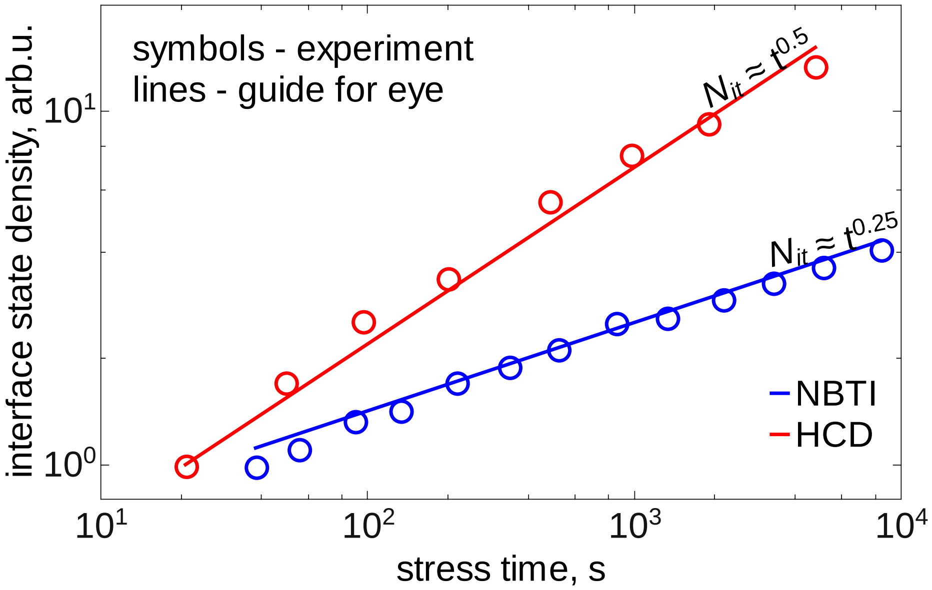

Figure 3.4: The experimentally obtained power-laws for NBTI and HCD curves plotted versus stress times from data in [162].

| Stage | Phase | time dependence of $N_{\mathrm{it}}$ | |
|---|---|---|---|
| 1 | Reaction limited (Si-H bond breakage) | $t^1$ | |
| 2 | Hydrogen diffusion (no more $N_{\mathrm{it}}$ generation) | $t^0$ | |
| 3 | Diffusion-limited | $t^{1/4}$ | |
| 4 | Hydrogen diffusion with infinite diffusion velocity | $t^{1/2}$ | |
| 5 | Saturation (all Si-H bonds depassivated) | $t^0$ | |

Table 3.1: Different stages of the reaction-diffusion model [163, 66]

diffusivity $D_{\mathrm{H}}$, $A_{\mathrm{d}}$ the degraded area of the device, and $N_{\mathrm{H}}^0$ the hydrogen density at the interface, the $N_{\mathrm{it}}$ distribution for HCD and NBTI are calculated as:

$$\begin{aligned} N_{\mathrm{it}}^{\mathrm{NBTI}} &= 1/A_{\mathrm{d}} \int_0^{(D_{\mathrm{H}}t)^{1/2}} N_{\mathrm{H}}^0 \left[1 - r/\left(D_{\mathrm{H}}t\right)^{1/2}\right] A_{\mathrm{d}} \mathrm{d}r = (1/2) N_{\mathrm{H}}^0 \left(D_{\mathrm{H}}t\right)^{1/2}, \quad (3.7) \\ N_{\mathrm{it}}^{\mathrm{HCD}} &= \pi/2A_{\mathrm{d}} \int_0^{(D_{\mathrm{H}}t)^{1/2}} N_{\mathrm{H}}^0 \left[1 - r/\left(D_{\mathrm{H}}t\right)^{1/2}\right] r\mathrm{d}r = (\pi/12A_{\mathrm{d}}) N_{\mathrm{H}}^0 \left(D_{\mathrm{H}}t\right), \end{aligned}$$

Equation 3.7 gives $N_{\mathrm{it}}^{\mathrm{NBTI}} \sim (D_{\mathrm{H}}t)^{1/4}$ and $N_{\mathrm{it}}^{\mathrm{HCD}} \sim (D_{\mathrm{H}}t)^{1/2}$.

Although the different time slopes could be explained, the reaction-diffusion model has several failings. The framework assumes that both processes are diffusion limited implying that a quick recovery should be observed on removal of the stress. This, as suggested by recent data, is not true for both NBTI and HCD [164, 165, 166]. Interface state generation has been shown to be reaction limited and HCD, in most cases, does not show any recovery. Moreover, since the model does not rely on carrier transport, the spatial $N_{\mathrm{it}}$ distribution cannot be obtained.

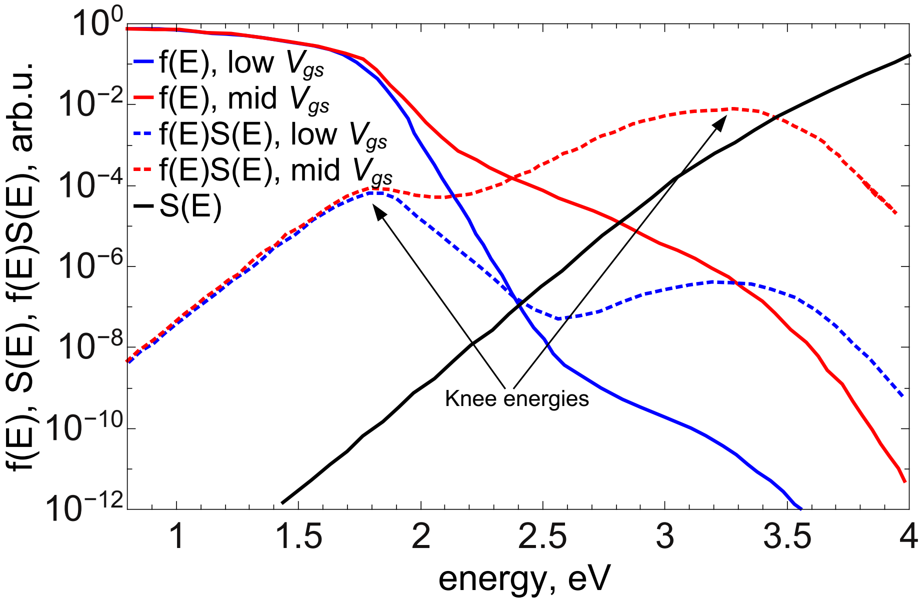

Figure 3.5: The energy driven paradigm: the knee energies shift depending on the drain voltage (data borrowed from [11]).

## 3.4 The Energy Driven Paradigm

Rauch and La Rosa suggested that in the case of scaled devices HCD is driven by the carrier energy deposited at the interface rather than by the electric field [23, 167]. They also investigated the importance of electron-electron scattering. Due to the low supply voltages in ultra-scaled MOSFETs, the single-carrier mechanism is not very prominent as the probability of finding carriers with very high energies is low. The energy exchange between carriers via carrier-carrier scattering populates the high energy tail of the carrier energy distribution function, thus increasing the probability of a single-carrier bond breakage process and of the multiple-carrier process as well [11]. The role of electron-electron scattering in scaled devices also explains the increase in HCD at elevated temperatures, which is contrary to the trend for long channel devices. At elevated temperatures, the scattering events are more intense which lead to a reduction of carrier energies in long channel devices and thus weakening of HCD. In short channel devices, however, an increase in temperature leads to more efficient scattering between the carriers causing an increase in carrier concentration in the high energy region. This suggests that the population of hot-carriers increases leading to a larger degradation [5, 148, 168, 149].

The Rauch and LaRosa approach introduce a shift of the HCD paradigm from being field driven to energy driven. The defect generation rate in the Rauch and La Rosa model has a similar form as Equation 3.1 given by: $\int f(\varepsilon) S(\varepsilon) \mathrm{d}\varepsilon$, where $f(\varepsilon)$ represents the carrier distribution function and $S(\varepsilon)$ the reaction cross section. The balance of slopes of the DF and the reaction cross section curves ($\mathrm{d}\ln f/\mathrm{d}\varepsilon = -\mathrm{d}\ln S/\mathrm{d}\varepsilon$) determines a knee energy. The Knee energy is the energy at which the defect generation rate attains a local maximum, see Figure 3.5. The knee energy was found to be weakly dependent on the drain voltage. The defect generation rate can then be calculated from the knee energy if the maximum of the product $f(\varepsilon)\,S(\varepsilon)$ is narrow enough to be approximated by a delta function. Thus, the integration over the entire energy range may be avoided.

This paradigm allows consideration of HCD without time consuming and computationally demanding transport simulations. However, there are also some shortcomings. In most cases the $f(\varepsilon)\,S(\varepsilon)$ peak is not narrow and, thus, integration over the entire energy range is required. Further, the authors used some empirical parameters based on the dominant knee energy to calculate the DF which does not capture the distribution and localization of $N_{\mathrm{it}}$, a characteristic feature of HCD. Finally, the device lifetime was estimated based on the $N_{\mathrm{it}}$ generation rate instead of using the changes observed in the device characteristics.

## 3.5 The Bravaix Model

The group of Bravaix combined the Hess model and the Rauch and La Rosa approach [10, 134, 140]. The Bravaix model uses the concept of single- and multiple-carrier processes of defect generation within the energy-driven paradigm and evaluates the DF empirically. Three main modes of bond breakage are considered in the model, i.e. a single-carrier process, a multiple-carrier process, and electron-electron scattering which are then used to calculate the corresponding lifetimes. The single-carrier process is attributed to high energy carriers, while the drain current is low [169]. In this case, the lucky electron model can be used and the device lifetime can be estimated as $1/\tau_{\mathrm{SP}} \sim (I_{\mathrm{d}}/W)\,(I_{\mathrm{s}}/I_{\mathrm{d}})^{m}$. Here $I_{\mathrm{d}}$, $I_{\mathrm{s}}$ are the drain and substrate currents, respectively, $W$ the device width, and $m$ the ratio of the powers in the impact ionization and interface state creation cross sections. The case with low carrier energies but high carrier density corresponds to the multiple-carrier process. For the MC-process, a truncated harmonic oscillator model is used to represent the breaking of the Si-H bond, as described in the Hess approach. The kinetic equation set which determines the bond passivation/depassivation rates is given by:

$$\begin{aligned}\frac{\mathrm{d}n_0}{\mathrm{d}t} &= P_{\mathrm{d}}n_1 - P_{\mathrm{u}}n_0\\ \frac{\mathrm{d}n_i}{\mathrm{d}t} &= P_{\mathrm{d}}(n_{\mathrm{i}+1} - n_{\mathrm{i}}) - P_{\mathrm{u}}(n_{\mathrm{i}} - n_{\mathrm{i}-1})\\ \frac{\mathrm{d}n_{\mathrm{N_l}}}{\mathrm{d}t} &= P_{\mathrm{u}}n_{\mathrm{N_l}-1} - \lambda_{\mathrm{emi}}N_{\mathrm{it}}\,[H^*]\,,\end{aligned} \tag{3.8}$$

with $n_{\mathrm{i}}$ being the occupancy of the $i^{\mathrm{th}}$ oscillator level, $[H^*]$ the concentration of mobile hydrogen atoms, while $N_{\mathrm{l}}$ labels the last bonded state. The rate of hydrogen release, $\lambda_{\mathrm{emi}}$, is calculated as $\lambda_{\mathrm{emi}} = \nu_{\mathrm{emi}}\exp\left[-E_{\mathrm{emi}}/k_{\mathrm{B}}T_{\mathrm{L}}\right]$, where $\nu_{\mathrm{emi}}$ is the attempt frequency, and $E_{\mathrm{emi}}$ is the energy barrier between the last bonded state and the transport mode, see Figure 3.1. The bond excitation and decay rates ($P_{\mathrm{u}}$, $P_{\mathrm{d}}$) are written as:

$$\begin{aligned}P_{\mathrm{u}} &= \int I_{\mathrm{d}}\sigma\mathrm{d}\varepsilon_{\mathrm{e}} + \omega_{\mathrm{e}}\exp\left[-\hbar\omega/k_{\mathrm{B}}T_{\mathrm{L}}\right]\\ P_{\mathrm{d}} &= \int I_{\mathrm{d}}\sigma\mathrm{d}\varepsilon_{\mathrm{e}} + \omega_{\mathrm{e}},\end{aligned} \tag{3.9}$$

where $I_{\mathrm{d}}$ is the drain current. Since, the DF is calculated empirically, the acceleration integral (first term in Equation 3.9) is substituted by the term $S_{\mathrm{MP}}\,(I_{\mathrm{e}}/e)$, where $S_{\mathrm{MP}}$ is a pre-factor [139]. This was an attempt to link the defect generation rate with the drain current. With a reasonable choice of the model parameters like $E_{\mathrm{emi}}$, and $\hbar\omega$ the bond

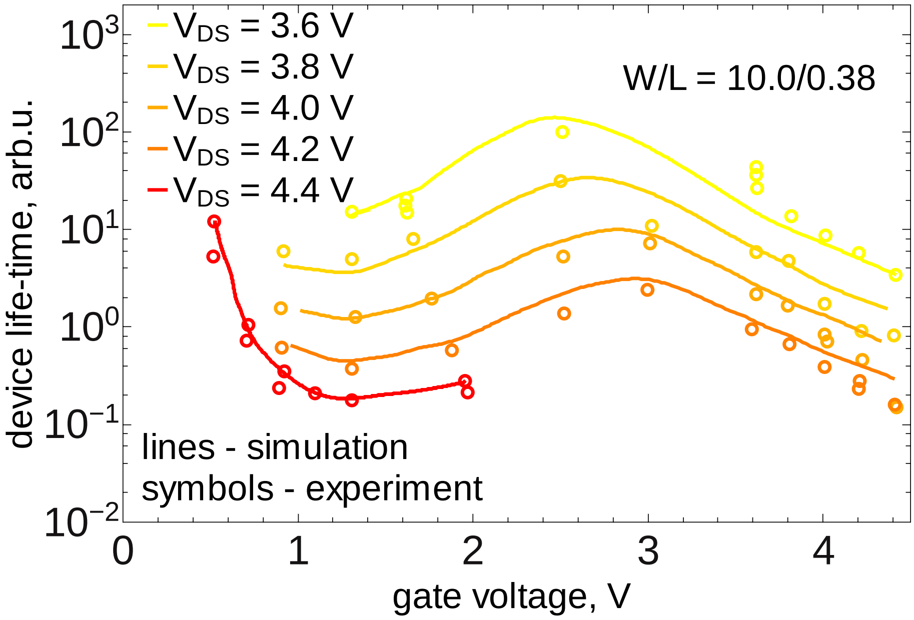

Figure 3.6: Device lifetimes obtained with the Bravaix model plotted vs. experimental data [170]

dissociation rates were accurately represented [169]. The device lifetime for the MC-process is given as $1/R_{\mathrm{MP}}$, where $R_{\mathrm{MP}}$ is interface state generation rate due to low energy carriers given as:

$$R_{\mathrm{MP}} = N_0 \left[ \frac{S_{\mathrm{MP}} \left( I_{\mathrm{d}}/e \right) + \omega_{\mathrm{e}} \exp \left[ -\hbar\omega/k_{\mathrm{B}}T_{\mathrm{L}} \right]}{S_{\mathrm{MP}} \left( I_{\mathrm{d}}/e \right) + \omega_{\mathrm{e}}} \right]^{E_{\mathrm{B}}/\hbar\omega} \exp \left[ -E_{\mathrm{emi}}/k_{\mathrm{B}}T_{\mathrm{L}} \right]. \tag{3.10}$$

The case with moderate carrier density is attributed to electron-electron scattering with lifetime $1/\tau_{\mathrm{EES}} \sim \left( I_{\mathrm{d}}/W \right)^2 \left( I_{\mathrm{s}}/I_{\mathrm{d}} \right)^m$. The quadratic relation is due to the electron-hole pairs, generated by impact ionization, not having enough energies to create interface states but are accelerated by electron-electron scattering to high energy levels where they can trigger bond dissociation. The major contribution of the Bravaix model was the prediction of the device lifetime by combining all the modes of interface state creation, see Figure 3.6.

$$1/\tau_{\mathrm{d}} = K_{\mathrm{SC}}/\tau_{\mathrm{SC}} + K_{\mathrm{EES}}/\tau_{\mathrm{EES}} + K_{\mathrm{MC}}/\tau_{\mathrm{MC}}, \tag{3.11}$$

where $K_{\mathrm{SC}}$, $K_{\mathrm{MC}}$, $K_{\mathrm{EES}}$ are fitting parameters which represent contributions of each process and $\tau_{\mathrm{SC}}$, $\tau_{\mathrm{MC}}$, $\tau_{\mathrm{EES}}$ are the device lifetimes in the SC, MC, and EES driven regimes, respectively. However, the carrier DF is calculated empirically which leaves the entire physical picture behind HCD unclear. In order to understand the physics behind the HCD mosaic, ideally accurate carrier transport needs to be addressed via the solution of the Boltzmann transport equation.

Such an approach has been developed by Tyaginov *et al.* [25, 141], which is also used in this work (Section 4.4), which tries to link the entire physical mechanism consisting of carrier transport, defect generation, and degradation of the device characteristics. The Tyaginov method has been the most accurate in modeling HCD and its effects on different devices [44, 14, 147, 88]. The authors obtain the carrier DF by solving the Boltzmann transport equation using both Monte-Carlo and spherical harmonics expansion methods [171, 141]. The carrier acceleration integral is then calculated from the carrier DF which determines the rate of interface state generation. Once the bond breakage rates are determined, the trap density can be calculated. Since this model provides information about $N_{\mathrm{it}}$ profiles and the strong localization of HCD, it can predict device lifetimes and degradation characteristics.

# Chapter 4

# The HCD Model Based on BTE Solution

As discussed in previous sections, carrier transport is the key to modeling HCD. The better the carrier transport analysis, the more precise the HCD model will be. Many approaches to solve the carier transport and obtain the carrier energy distribution function have been proposed. Some of these methods are more rigorous, while others are simplistic and less accurate. Ever since the shift of paradigm in hot-carrier degradation modeling from field driven approaches [150] to the energy driven concept [9, 11], the evaluation of the carrier distribution function has become a vital component. This has also been suggested in recent HCD modeling results where the entire Si-H bond breakage process, which is assumed to be the dominant contributor to HCD in $SiO_2$ devices, is described by the carrier energy distribution function [7, 8]. Ideally, within the semiclassical regime, the DF is obtained by solving the Boltzmann transport equation. Although both the Monte-Carlo approach and the spherical harmonics expansion method provide a solution to the BTE, the latter technique has a number of advantages: it allows to better resolve the high-energy tails of the DF (which are of crucial importance in the context of HCD), simulate long-channel devices under high operating/stress voltages in a reasonable time, and implement electron-electron scattering in a more straightforward manner and with less computational burden. Apart from these approaches, simplified techniques of carrier transport treatment such as the drift-diffusion and energy transport scheme are highly popular [33, 30]. Inspite of its limitations, the drift-diffusion method has been effective for the description of carrier transport even in modern devices [172].

In the following, a simple and efficient model for the carrier distribution function is derived. This approach to approximately calculate the DF is based on the drift-diffusion scheme where an analytical expression is used to mimic the carrier energy distribution function. To verify the obtained DF, a solution of the Boltzmann transport equation is used as a reference. The analytical method for calculating the DF is coupled with a physics-based model for hot-carrier degradation. The analytical approach for the DF is consistent with the HCD model as it contains terms for both hot and cold carriers which lead to the single- and multiple-carrier processes. We use two versions of the HCD model: one is based on more rigorous deterministic approach and is used for reference or verification, while the other one employs the DD-based concept. In the following chapters, both versions of the model are compared against experimental data for several devices and a conclusion on the validity of the DD-based version of the HCD model is drawn suggesting its efficiency for

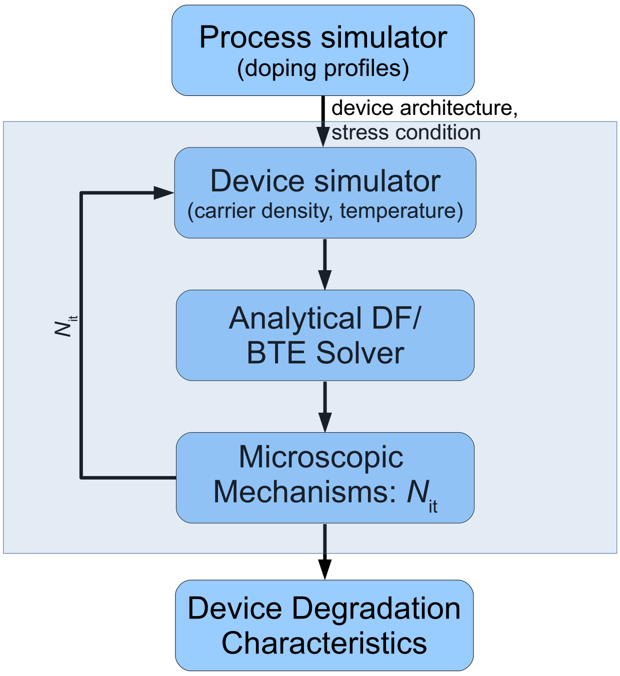

Figure 4.1: The main modules of the HCD model: carrier transport solver, modeling of the defect generation rates and interface state profiles, and simulation of the degraded device.

predictive HCD simulations under certain conditions.

## 4.1 Carrier Transport

The operation of semiconductor devices is based on the reaction of electrons and holes to the local and externally applied electrical forces. These forces are due to the potentials either existing or created inside the semiconducting material due to: (i) applied bias, (ii) depletion regions formed by immobile ionized impurities at thermal equilibrium (built-in potential), and (iii) other charge carriers or impurities (scattering potentials). Since a typical semiconductor device includes a large concentration of charge carriers and artificially introduced impurities or dopants, this many-particle system is difficult to model. Various models for carrier transport have been proposed with different levels of refinements and complexity that are applicable based on the device dimensions, usage and computational budget. Although it is attractive to choose the most fundamental concepts, they typically have high computational demands and for most engineering applications a more approximate but faster and computationally cheaper solution is acceptable.

This section provides an overview of the most important carrier transport models developed for semiconductor devices and discusses their efficiency and limitations. The carrier transport models can be categorized based on the device dimensions and characteristic lengths – de Broglie wavelength, mean free path, and phase relaxation length [173]. For an electron in silicon at room temperature, the de Broglie wavelength is approximately 8

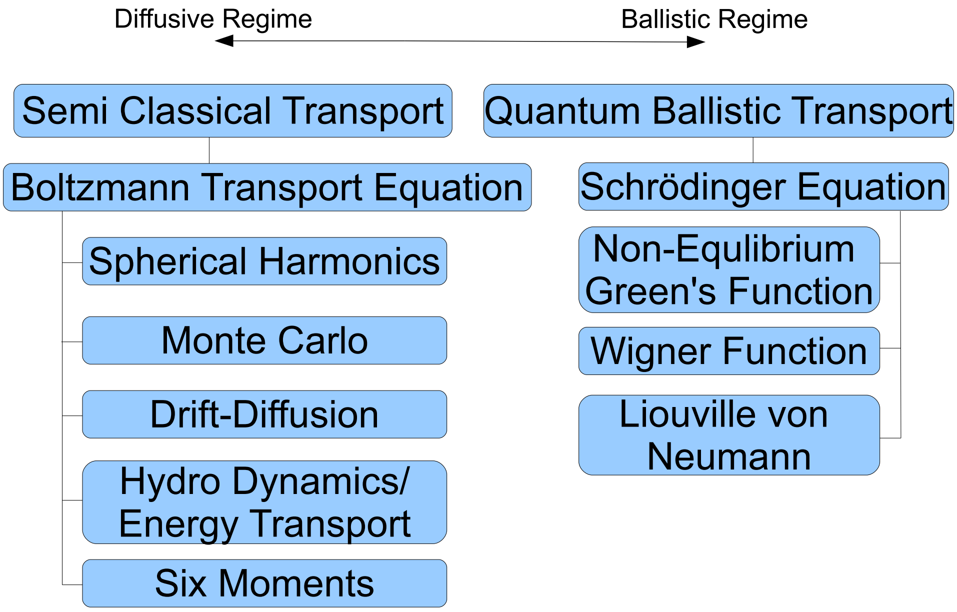

Figure 4.2: The different approaches to solve carrier transport in semiconductor devices

nm, while the mean free path and the phase relaxation length are between 5 to 10 nm. If the device dimensions are much larger than the characteristic lengths, carrier transport is governed largely by scattering and the transport is called diffusive. Semi-classical models are quite accurate in this regime to describe the motion of charge carriers. However, in nanoscale devices, smaller than the characteristic lengths, quantum effects come into play and scattering becomes less important. Thus quantum transport models are required for an accurate description of the electrostatics in the device.

In this section, the semi-classical transport models are discussed which are most relevant for HCD modeling. The Boltzmann transport equation is the backbone of semi-classical transport. The different approaches to the BTE solution starting from the Monte-Carlo method, the spherical harmonics expansion, and the techniques based on the BTE moments, i.e. the drift-diffusion and energy transport schemes, see Figure 4.2 are described in order to understand the applicability of each of these methods.

## 4.2 Semi-Classical Transport

Let us consider a semiconductor device in thermal equilibrium when no external electric field is applied and all the transient processes have relaxed. In this situation, the average energy of the carriers is equal to the thermal energy, while their average velocity is zero. This corresponds to the absence of a macroscopic current in the device. When a bias is applied, the carriers experience a force and accelerate until opposed by other forces such as scattering. Thus, the motion of particles inside a semiconductor device is a result of forces due to the applied bias, built-in potential and scattering potential. Their resultant force causes the momentum and position of the charge carriers to change. Thus, within the classical regime, to find the effect of fields on charge carriers, their momentum and position need to be evaluated.

### 4.2.1 Monte-Carlo Approach

In the Monte-Carlo method for solving the carrier transport problem, the Newton equation is evaluated for the particles. For a single ($i^{\text{th}}$) particle, the system of equations would read:

$$\frac{\partial p_i}{\partial t} = F(p,r,t) + R(p,r,t), \tag{4.1}$$

$$\frac{\partial r_i}{\partial t} = u_i(t), \tag{4.2}$$

where $F(p,r,t)$ is due to external forces and $R(p,r,t)$ is due to local forces. In the semi-classical approach, the effect of external forces is treated classically, but the local forces such as scattering are treated quantum mechanically. The above equations, 4.1 and 4.2 describe a classical carrier transport and are not fully applicable to modern devices. The above is equivalent to the BTE, band structure enters through the dispersion relation and scattering goes to R. Moreover, it is very computationally demanding to obtain a solution for all particles in a typical semiconductor device, containing $\sim 10^{20}$ particles.

### 4.2.2 Boltzmann Transport Equation

Another approach to describe carrier transport semi-classically is to consider the statistical properties of the charge carriers by defining a distribution function $f(p,r,t)$. The carrier distribution function $f(p,r,t)$ gives the probability of finding a carrier with momentum in the range of $(p, p+dp)$ and volume of $(r, r+dr)$ and satisfies the Boltzmann transport equation:

$$\partial_t f + u\nabla_{\mathrm{r}} f + F\nabla_{\mathrm{p}} f = Q(f), \tag{4.3}$$

where $Q(f)$ is the scattering operator. The semi-classical nature is incorporated in the relation of the carrier momentum $p$ with the wave number $k$ as $p = \hbar k$, $\hbar$ being the reduced Planck constant. The group velocity $u$ in Equation 4.3 is given by:

$$u(p,r) = \nabla_{\mathrm{p}} E_{\mathrm{K}}(p,r), \tag{4.4}$$

where $E_{\mathrm{K}}$ represents the kinetic energy of the carriers. The force $F(p,r)$ acting on the carriers due to the electric $E(r)$ and magnetic fields $B(r)$ and inhomogeneous material properties is [174]:

$$F(p,r) = -\nabla_{\mathrm{r}}\left(E_{\mathrm{c},0}(r) + \varepsilon(p,r)\right) + q\left(E(r) + u(p,r)\times B(r)\right), \tag{4.5}$$

where $E_{\mathrm{c},0}(r)$ is the energetic position of the bottom of the conduction band and $\varepsilon(p,r)$ represents the band structure. Scattering affects the distribution function via in-scattering and out-scattering:

$$Q(f) = \sum f(p)(1-f(p'))S(p,p') - f(p')(1-f(p))S(p',p),$$

where $S(p, p')$ represents the transition rate for a particle from a state denoted by the momentum $p$ to a state denoted by the momentum $p'$, while $1-f(p')$ represents the probability that the state at $p'$ is empty. For non-degenerate semiconductors (low carrier concentration), the Pauli principle can be neglected and thus the scattering operator becomes linear and has an easier structure:

$$Q(f) = \sum f(p)S(p, p') - f(p')S(p', p), \tag{4.6}$$

The function $S$ is assumed to account for all scattering mechanisms. The rates for the scattering mechanisms are calculated using the overlap integrals and deformation potentials followinf Fermi's Golden Rule [175].

Since the BTE is a seven dimensional integro-differential equation, it is very challenging to obtain an exact solution. The Monte-Carlo method is widely used to numerically solve the BTE, but this method requires huge computational resources especially to resolve the high-energy tail of the carrier distribution function. In this subsection more computationally efficient approaches to solve the Boltzmann transport equation are discussed. Among these are the expansion of the distribution function in momentum space into a series of spherical harmonics, the method of moments, i.e. six moments model, the hydrodynamics or energy transport scheme, and the drift-diffusion scheme which is commonly used by device engineers.

#### 4.2.2.1 Spherical Harmonics Expansion

The spherical harmonics expansion (SHE) method relies on the expansion of the carrier distribution function $f(x, k, t)$ into a series of spherical harmonics [18]:

$$f(x, k, t) = \sum_{l=0}^{\infty} \sum_{m=-l}^{l} f_{l,m}(x, \epsilon, t)\mathrm{Y}^{l,m}(\theta, \varphi), \tag{4.7}$$

where $k$ is the three-dimensional wave vector which is expressed in terms of spherical coordinates $\epsilon$, $\theta$, $\varphi$. Owing to its deterministic nature, the computational effort in the SHE method is reduced as compared to the stochastic Monte-Carlo method. However, Equation 4.7 is still five dimensional and requires a fair amount of computational resources. These high computational demands of the SHE approach are also due to the system of coupled partial differential equations which needs to be solved for each expansion coefficient ($f_{l,m}$).

#### 4.2.2.2 The Moments Method

The macroscopic models to solve the BTE are common simplifications where only a few moments of the carrier distribution function are considered, like the carrier concentration and the carrier temperature [175, 176, 177, 178]. The moments are macroscopic quantities derived by integrating the distribution function over the three dimensional $k$ space with a suitable weight function $\phi(k)$. The $i^{\text{th}}$ moment of the BTE is given as [174]:

$$\langle \phi_i \rangle = \int \phi_i(k) f(k) d^3k. \tag{4.8}$$

This reduces the complexity of the seven dimensional BTE by eliminating the three $k$ coordinates. Some information is lost in this simplification which may not be important for device engineering applications or for obtaining an approximate analysis of charge transport. The weight functions $\phi_i\left(k\right)$ are chosen as increasing powers of the vector $k$ with some scaling factor to obtain physically meaningful quantities. However, each equation for the moment $i$ contains the next higher order moment $i+1$, resulting in the variables outnumbering the equations. In order to close this system of equations, usually an a priori assumption about the shape of the distribution function is made, for example using a Maxwellian distribution. The first few moments important to this work are listed in Table 4.1.

| Order | Moment |
|---|---|
| $\phi_0$ | $n$ |
| $\phi_1$ | $\frac{3}{2}nk_{\mathrm{B}}T_{\mathrm{n}}$ |
| $\phi_2$ | $\frac{5*3}{2*2}n\left(k_{\mathrm{B}}T_{\mathrm{n}}\right)^2$ |
| $\phi_3$ | $\frac{7*5*3}{2*2*2}n\left(k_{\mathrm{B}}T_{\mathrm{n}}\right)^3$ |

Table 4.1: The first four moments of the Maxwell distribution.

The derivation of the moments of a Maxwell distribution for closure is given in Appendix B. Applying the moments in Table 4.1 to the BTE, and using the diffusion[1] and relaxation time approximations[2], the transport equations can be formulated [179]. For electrons, the first three transport equations can be written as:

$$\phi_0: \qquad \partial_t n - \frac{1}{q}\nabla J_{\mathrm{n}} = -R, \tag{4.9}$$

$$\phi_1: \qquad J_{\mathrm{n}} = \frac{q\tau_{\mathrm{m}}}{m}\left(\frac{2}{3}\nabla\left\langle\phi_2\right\rangle + qE\right), \tag{4.10}$$

$$\phi_2: \qquad \frac{3}{2}k_{\mathrm{B}}\partial_t\left(nT_{\mathrm{n}}\right) + \nabla\left\langle\phi_3\right\rangle - EJ_{\mathrm{n}} = -\frac{3}{2}k_{\mathrm{B}}n\frac{T_{\mathrm{n}}-T_{\mathrm{L}}}{\tau\varepsilon} + G\varepsilon n, \tag{4.11}$$

where $\tau_{\mathrm{m}}$ is the momentum relaxation time, $T_{\mathrm{n}}$ and $T_{\mathrm{L}}$ are the electron and lattice temperature, respectively, $R$ the net recombination rate, and $E$ the electric field.

#### 4.2.2.3 Drift-diffusion

The drift-diffusion transport model has been the workhorse of device simulation for most device engineering applications. The DD model treats the transport either phenomenologically, i.e., carriers drift in electric fields and diffuse in concentration gradients or uses the first two moments of the BTE and hence the two transport Equations 4.9 and 4.10. The equation system has to be closed at $\phi_2$ for which the relation $\phi_2 = {}^3\!/\!_2\, nk_{\mathrm{B}}T_{\mathrm{L}}$ is used. It is worth mentioning that the DD equation system does not provide any information about the average carrier energy or carrier temperature $T_{\mathrm{n}}$. Since, a thermal equilibrium

---

[1] The diffusion approximation, implying that the diffusion of carriers dominates over drift, leads to the conclusion that the antisymmetric part of the distribution function is negligible and the symmetric part is isotropic.

[2] The relaxation time approximation suggests that the perturbed distribution function will relax exponentially into the equilibrium distribution function.

condition is assumed treating $T_\mathrm{n} = T_\mathrm{L}$. The DD model is then expressed as:

$$\nabla J_n = q\left(R + \partial_t n\right), \tag{4.12}$$

$$\begin{aligned} J_n =& \mu_n k_\mathrm{B}\left(\nabla\left(nT_\mathrm{L}\right) + \frac{q}{k_\mathrm{B}} En\right), \\ =& qn\mu_n E + qD_n \nabla n, \end{aligned} \tag{4.13}$$

Similarly for holes, the DD equations read:

$$\nabla J_p = -q\left(R + \partial_t p\right), \tag{4.14}$$

$$J_p = qp\mu_p E - qD_p \nabla p, \tag{4.15}$$

where $\mu_{n/p} = q\tau_{n/p}/m_{n/p}$ is the mobility of the respective charge carriers in the device with $\tau_{n/p}$ being their momentum relaxation time and $m_{n/p}$ their mass. The electric field $E$ in Equations 4.13 and 4.15 is obtained from the Poisson equation A.3, while the diffusion coefficients ($D_{n/p}$) are determined from the Einstein relation:

$$D_{n/p} = \frac{k_\mathrm{B} T_\mathrm{L}}{q}\mu_{n/p} = V_\mathrm{T}\mu_{n/p}, \tag{4.16}$$

where $V_\mathrm{T}$ is the thermal voltage which has a value of 26 mV ($k_\mathrm{B} = 1.38 \times 10^{-23}$ J/K, $q = 1.6 \times 10^{-19}$ C) at room temperature (300 K). Equation 4.16 underestimates the diffusivity since the lattice temperature is used instead of the carrier temperature. Moreover, the numerous assumptions made during the derivation of the DD method limit its physical relevance for real device operation. However, many mobility models have been proposed to enhance the validity range of the DD approach by incorporating the electric field, doping dependencies and the role of the interface trap density to account for degradation effects [180, 181, 124]. Another major drawback of the DD method is that effects of rapidly changing electric fields, like the velocity overshoot, cannot be described [182]. In order to estimate the average carrier energy, the parameters obtained with the DD simulations are post-processed using the homogeneous energy balance equation as given in [28, 147]. However, in reality, the average energy lags behind the electric field if the latter changes rapidly. Since, to first order, the mobility depends (inversely) on the average energy, and not on the electric field, the mobility will not reduce instantly when the electric field increases. Thus, an overshoot in velocity will be observed until the carrier energy reached equilibrium with the electric field. Since the carrier energy depends directly on the electric field in the homogeneous energy balance equation, the velocity overshoot cannot be described. Nevertheless, due to its simplicity and low computational requirements, the DD model is the most widely used approach, especially for device engineering applications.

#### 4.2.2.4 Hydrodynamic/Energy Transport Model

The full Hydrodynamic (HD) transport model involves numerically challenging equations due to their hyperbolic nature. Thus, the energy transport model, which is a simplified version of the HD transport model is often used. The energy transport employs the first three or four moments of the BTE, thereby, incorporating spatial dependencies of the average carrier energy. Using Equations 4.9, 4.10, and 4.11 and the corresponding closure as in [179], the HD transport model is given as:

$$
\begin{aligned}
\nabla J_n =& q\left(R+\partial_t n\right), && (4.17)\\
J_n =& \mu_\mathrm{n} k_\mathrm{B}\left(\nabla\left(nT_\mathrm{n}\right)+\frac{q}{k_\mathrm{B}}En\right), && (4.18)\\
\nabla S_n =& -\frac{3}{2}k_\mathrm{B}\partial_t(nT_\mathrm{n})+EJ_\mathrm{n}-\frac{3}{2}k_\mathrm{B}n\frac{T_\mathrm{n}-T_\mathrm{L}}{\tau_\varepsilon}+G\varepsilon n, && (4.19)\\
S_n =& \frac{5}{2}\frac{k_\mathrm{B}}{q}T_\mathrm{n}J_n-\kappa_\mathrm{n}\nabla T_\mathrm{n}. && (4.20)
\end{aligned}
$$

The electric field $E$ is determined from the Poisson equation A.3, $\tau_\varepsilon$ is the energy relaxation time, $S_\mathrm{n}$ the heat flux density. The thermal conductivity $\kappa_\mathrm{n}$ is obtained using the Wiedemann-Franz law, $\kappa_\mathrm{n}T_\mathrm{n}=\left({}^5\!/_2-p'\right)\left({}^{k_\mathrm{B}}\!/_q\right)^2 q\mu_\mathrm{n}nT_\mathrm{n}$ where $p'$ is a correction factor. In contrast to the DD model, the energy transport model includes non-local effects. Thus, a phenomenon like the velocity overshoot can be approximately described since $\mu_\mathrm{n}$ depends on $T_\mathrm{n}$, which in turn depends on $E$ in a non-local manner (Equations 4.19 and 4.20). However, the energy transport model predicts velocity overshoot also in rapidly decreasing fields, which is not observed in Monte-Carlo simulations. This artifact was attributed to the truncation of the model after the 4th moment [183, 184].

#### 4.2.2.5 Six Moments Model

By considering two additional moments of the BTE along with those in the HD model, the six moments model can be derived [176]. An additional quantity, the kurtosis (skewness) of the distribution function is introduced as [174]:

$$\beta=\frac{3\left\langle\varepsilon^2\right\rangle}{5\left\langle\varepsilon\right\rangle^2}. \tag{4.21}$$

The quantity $\beta$ represents the deviation of the shape of the distribution function from the Maxwellian distribution. This model better represents phenomena like impact ionization, velocity overshoot, hot-carrier effects, but it is quite complex and numerically challenging. Thus, the model has not been widely used in industry and has been restricted to academic interest.

## 4.3 Carrier Energy Distribution Function

As suggested by the energy driven paradigm, the carrier distribution function is the most important ingredient of any HCD model. To calculate the DFs, we use the deterministic BTE solver ViennaSHE in this work [13, 15, 14]. The Monte-Carlo approach is not well suited for HCD modeling in power devices due its enormous computational demands related to resolving the high energy tails. Thus, it is not used in this work as we try to model devices of different dimensions and operating voltages. An alternative way, as mentioned before, is to use simplified approaches to the BTE solution such as the drift-diffusion scheme. The DFs simulated with ViennaSHE are used as a benchmark for the DD-based approach.

In the analytical approach, a simplified technique is used to obtain the carrier energy DF which uses the drift-diffusion method. However, as discussed in Section 4.2.2.3, the

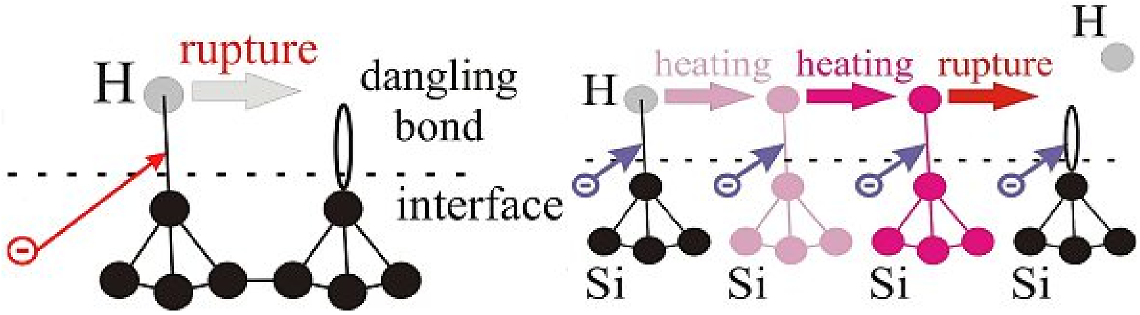

Figure 4.3: The Si-H bond dissociation due to the bombardment by a single hot-carrier (SC-process) and due to multiple interactions with colder carriers (MC-process) [8].

DD model consists of just two moments of the BTE and the full DF cannot be obtained. Thus, in order to estimate the DF, approximate analytic formulations have to be used. The parameters in the analytic DF expression can be calculated from the BTE moments obtained using DD simulations. In this context, an analytic expression for the DF has been used in this work. The analytical expression, which was suggested in [185], considers both hot and cold carriers:

$$f(\varepsilon) = A \exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\mathrm{ref}}}\right)^{b}\right] + C \exp\left[-\frac{\varepsilon}{k_{\mathrm{B}} T_{\mathrm{n}}}\right], \tag{4.22}$$

where $\varepsilon$ is the carrier energy, $T_{\mathrm{n}}$ the carrier temperature, $k_{\mathrm{B}}$ the Boltzmann constant. In Equation 4.22 the first term represents the DFs in the sections of the device where the carriers are hot, for example carriers in the channel region, the bird's beak region in LDMOS devices, as well as the high energetic carriers near the drain. The pool of cold carriers in the drain/source region is modeled by an additional cold Maxwellian term. Since the DD model assumes a thermal equilibrium condition, the carrier temperature cannot be obtained directly. Thus, the carrier temperature is evaluated from post-processing of the drift-diffusion simulation results. The electron concentration $n(x)$, the electric field profile $E(x)$, and the carrier mobility $\mu(x)$ are extracted as functions of the lateral coordinate from the DD simulations performed using the device and circuit simulator Minimos-NT [124, 125]. These quantities are then employed to estimate the carrier temperature $T_{\mathrm{n}}(x)$ using the balance equation:

$$T_{\mathrm{n/p}} = T_{\mathrm{L}} + \frac{2}{3}\frac{q}{k_{\mathrm{B}}}\tau_{\mathrm{n/p}}\mu_{\mathrm{n/p}}E^{2}, \tag{4.23}$$

where $T_{\mathrm{L}}$ is the lattice temperature, $q$ the modulus of the electron charge, and $\tau_{\mathrm{n/p}}$ the energy relaxation time with typical values of $\tau_{\mathrm{n}} = 0.35\,\mathrm{ps}$ for electrons and $\tau_{\mathrm{p}} = 0.4\,\mathrm{ps}$ for holes [28].

The DF in Equation 4.22 can represent the carriers in thermal equilibrium as well as the non-equilibrium ones. The first part of Equation 4.22 is used to determine the carrier DF in the device regions with high energy carriers, whereas the full expression is required for the regions where both hot and cold carriers lead to defect generation [147]. For the former case, two parameters $A$, and $\varepsilon_{\mathrm{ref}}$ need to be calculated which is done using the information on the available BTE moments, i.e., the estimated carrier concentration, and the carrier temperature.

$$\int_0^\infty f(\varepsilon)g(\varepsilon)d\varepsilon = n \tag{4.24}$$

$$\int_0^\infty \varepsilon f(\varepsilon)g(\varepsilon)d\varepsilon = \frac{3}{2}nk_\mathrm{B}T_\mathrm{n} \tag{4.25}$$

The Equations 4.24 and 4.25 are reduced to analytical form (for details see Appendix C) using the expression for distribution function $f(\varepsilon)$ from Equation 4.22 while for the density of states $g(\varepsilon)$ the expression proposed in [177] is used:

$$g(\varepsilon) = g_0\sqrt{\varepsilon}\left(1 + (\eta\varepsilon)^{\varsigma}\right). \tag{4.26}$$

Equation 4.26 very accurately reproduces the conventional non-parabolic Kane relation but can be integrated analytically [177]. The parameters $A$, and $\varepsilon_\mathrm{ref}$ thus obtained are substituted in Equation 4.22 to determine the energy DF.

When using the full Equation 4.22, three parameters $A$, $\varepsilon_\mathrm{ref}$, and $C$ need to be calculated, while the parameter $b$ is assigned a constant value of 1 near the drain and source regions and 2 otherwise. As before, the reduced forms of Equations 4.24 and 4.25, as shown in Appendix C, are used with $f(\varepsilon)$ from Equation 4.22 and $g(\varepsilon)$ from Equation 4.26. However, an additional Equation 4.28 derived from DF normalization, Equation 4.27, is employed so that the three required parameters can be determined.

$$\int_0^\infty f(\varepsilon)d\varepsilon = 1 \tag{4.27}$$

$$A\frac{\varepsilon_\mathrm{ref}}{b}\Gamma\left(\frac{1}{b}\right) - Ck_\mathrm{B}T_\mathrm{n}\exp\left[-\frac{\varepsilon}{k_\mathrm{B}T_\mathrm{n}}\right] = 1, \tag{4.28}$$

The Equation 4.28 is obtained from Equation 4.27 by assuming that the cold carriers are present in a small fraction of the energy region, thus the corresponding integral is not evaluated for the entire energy range. Instead, the indefinite form is used for the cold carrier term. The ternary equation system consisting of the reduced forms of Equations 4.24 and 4.25, and Equation 4.28 is thus solved to calculate the parameters $A$, $\varepsilon_\mathrm{ref}$, and $C$. This equation system is solved at each energy point $\varepsilon$ and the parameters obtained are substituted back to the Equation 4.22 to construct the DF $f(\varepsilon)$.

## 4.4 Defect Generation

Once the DFs are determined from the solution of the BTE, the defect generation rates are calculated. The HCD model considers the single- and multiple-carrier bond breakage mechanisms as two pathways of the same reaction, self-consistently, which converts electrically passive Si-H bonds to active interface traps. As already explained, the bond breakage event induced by a solitary hot carrier in a single interaction with the Si-H bond corresponds to the single-carrier process, see Figure 4.3. Since the hydrogen nucleus is much heavier than an electron, the most plausible explanation of such a mechanism is the energy exchange between the incoming high-energy electron and one of the bonding electrons. The excited binding electron is excited into an antibonding state which exerts a repulsive force acting on the H atom which leads to hydrogen release. Thus, the SC-process is often referred to as anti-bonding (AB) process. The multiple-carrier process, on

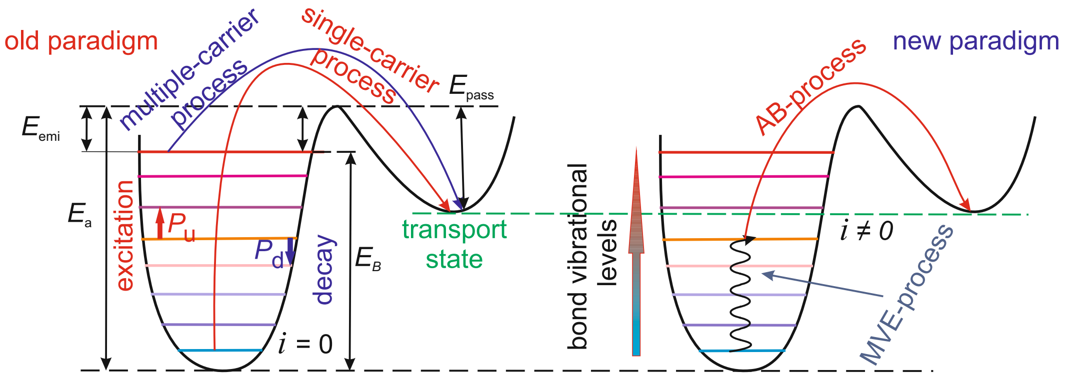

Figure 4.4: Comparison of self- and non-self-consistent consideration of SC- and MC-processes of Si-H bond breakage. The bond breakage corresponds to hydrogen release from one of these bonded states in the potential well to the transport mode [186].

the other hand, is triggered by a series of colder carriers which subsequently bombard the Si-H bond, excite and eventually break it as depicted in Figure 4.3. Previously, the single- and multiple-carrier processes of bond dissociation were assumed to be independent [25]. The interface state density was calculated as a superposition of SC- and MC-induced contributions weighted with some probability coefficients [27, 25, 10]. However, in an updated version of the model, the Si-H bond depassivation process has been modeled considering all possible superpositions of the SC- and MC-mechanisms with the corresponding rates determined by the carrier DF, see Figure 4.5.

The carrier DFs are used to compute the carrier acceleration integral which determines the rates of both single- and multiple-carrier processes [15, 13, 14]:

$$I^{\mathrm{e/h}}_{\mathrm{SC/MC}} = \int f(\varepsilon)g(\varepsilon)v(\varepsilon)\sigma_{0,\mathrm{SC/MC}}(\varepsilon-\varepsilon_{\mathrm{th}})^{p_{\mathrm{SC/MC}}}\mathrm{d}\varepsilon, \tag{4.29}$$

where $f(\varepsilon)$ is the DF, $g(\varepsilon)$ the density-of-states, $v(\varepsilon)$ the carrier group velocity, and $\sigma_0(\varepsilon - \varepsilon_{\mathrm{th}})^p$ the reaction cross section. The integrand in Equation 4.29 can be interpreted as multiplication of the carrier flux having an energy in the range $[E + dE]$ by the probability of bond-excitation by these carriers. The acceleration integrals for the SC- and MC-processes differ in the parameters $\varepsilon_{\mathrm{th}}$(threshold energy) and $p$ (11 for the SC-process and 1 for the MC-process). In the case of the single-carrier bond breakage mechanism the reaction cross section is Keldysh-like [187, 171], with the threshold energy equal to the bond breakage activation energy. For the multiple-carrier mechanism, the bond is modeled as a truncated harmonic oscillator [188, 139] comprising of an energy ladder with $N_{\mathrm{l}}$ vibrational energy levels, as shown in Figure 4.5. Due to the multi-vibrational model, the multiple-carrier pathway is also called multi-vibrational excitation process. The threshold energy for the MC-process corresponds to the distance between the bond vibrational states ($\hbar\omega$). The bond can gain/loose energy which leads to bond excitation/deexcitation. $E_{\mathrm{B}}$ is the energy required to reach the highest bonded energy level, while $E_{\mathrm{emi}}$ is the energy required for H emission from a Si-H bond that is in the highest bonded energy state. Thus, $E_{\mathrm{B}} + E_{\mathrm{emi}}$ forms the activation energy $E_{\mathrm{a}}$ for Si-H bond breakage. Conversely, the energy barrier for the passivation process, i.e. hydrogen forming the bond again, is $E_p$. .

Two vibrational modes of the Si-H bond have been identified, i.e. stretching (with $\hbar\omega = 0.25\,\mathrm{eV}$ and $E_{\mathrm{a}} = 2.56\,\mathrm{eV}$) and bending ( $\hbar\omega = 0.075\,\mathrm{eV}$ and $E_{\mathrm{a}} = 1.5\,\mathrm{eV}$) [140, 189]. In one of the most successful HCD models developed by the Bravaix group it is assumed that bond dissociation occurs via the bending mode with the corresponding values of $\hbar\omega$ and

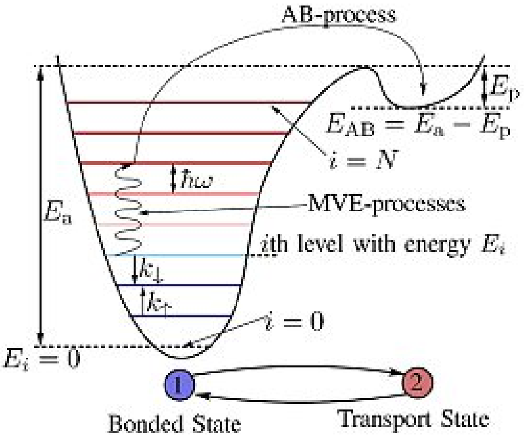

Figure 4.5: A schematic representation of the truncated harmonic oscillator model used for the derivation of the physics-based HCD model. The Si-H bond is ruptured at the transition from the bonded state 1 to the transport state 2. The required activation energy $E_\mathrm{a}$ for overcoming this barrier can be effectively lowered by the interplay between the SC- and the MC-mechanism [14].

$E_\mathrm{a}$ [140]. The vibrational lifetime ($\tau_\mathrm{e}$) chosen in that model is 10 ps while its temperature dependence is not considered [190, 140]. Experimental investigations, however, suggest that H desorption from the Si/SiO$_2$ interface occurs with $E_\mathrm{a} = 2.56\,\mathrm{eV}$ [114]. This value is close to that typical for the stretching mode with the corresponding vibrational lifetimes at $T = 25$ and $75\,^\circ\mathrm{C}$ of 1.5 and 1.3 ns, respectively, see [191]. These parameter values are used in this work.

The rates of the bond excitation/deexcitation processes triggered by the multiple-carrier mechanism are:

$$P_\mathrm{u} = I_\mathrm{MC} + \omega_\mathrm{e} \exp[-\hbar\omega/k_\mathrm{B}T_\mathrm{L}] \tag{4.30}$$

$$P_\mathrm{d} = I_\mathrm{MC} + \omega_\mathrm{e}, \tag{4.31}$$

where $\omega_\mathrm{e}$ represents the reciprocal phonon lifetime. The bond activation/passivation rates from the $i^\mathrm{th}$ level are:

$$R_{\mathrm{a/p},i} = \omega_\mathrm{th} \exp[-(E_\mathrm{a} - E_i)/k_\mathrm{B}T_\mathrm{L}] + I_{\mathrm{SC},i}, \tag{4.32}$$

with $\omega_\mathrm{th}$ being the attempt frequency. The first term in Equation 4.32 corresponds to thermal activation of the H atom, while the second one incorporates the effect of hot carriers. Each bond level, $i$, can contribute to the bond breakage mechanism as per Equation 4.32. A self-consistent consideration of the SC- and MC-processes means that first the bond can be excited by a series of cold carriers to a certain intermediate level, see Figure 4.5, and then dissociated by a solitary hot carrier which induces hydrogen release to the transport mode [136, 157, 188, 192, 13]. Note that in the case of a preheated bond the potential barrier which separates the bonded and transport states is reduced and the probability of finding a carrier which brings a bond breakage portion of energy is higher [15, 13, 14]. The system of rate equations for bond passivation/depassivation for all the energy levels in the potential well can be written as:

$$\begin{aligned}\frac{\mathrm{d}n_0}{\mathrm{d}t} &= P_\mathrm{d}n_1 - P_\mathrm{u}n_0 - R_{\mathrm{a},0}n_0 + R_{\mathrm{p},0}N_\mathrm{it}^2 \\ \frac{\mathrm{d}n_i}{\mathrm{d}t} &= P_\mathrm{d}(n_{i+1} - n_i) - P_\mathrm{u}(n_i - n_{i-1}) - R_{\mathrm{a},i}n_i + R_{\mathrm{p},i}N_\mathrm{it}^2 \\ \frac{\mathrm{d}n_{\mathrm{N_l}}}{\mathrm{d}t} &= P_\mathrm{u}n_{\mathrm{N_l}-1} - P_\mathrm{d}n_{\mathrm{N_l}} - R_{\mathrm{a},\mathrm{N_l}}n_{\mathrm{N_l}} + R_{\mathrm{p},\mathrm{N_l}}N_\mathrm{it}^2\end{aligned} \tag{4.33}$$

where $n_i$ represents the occupation number of the $i^\mathrm{th}$ energy level. Due to the large difference between phonon and Si-H bond lifetimes, the time constants for oscillator transitions are much shorter than those typical for passivation/depassivation processes. Thus, the time scale hierarchy can be used to solve the system of equations 4.33 which reduces to a single equation [13]:

$$\frac{\mathrm{d}N_\mathrm{it}}{\mathrm{d}t} = (N_0 - N_\mathrm{it}\Re_\mathrm{a} - N_\mathrm{it}^2\Re_\mathrm{p}). \tag{4.34}$$

Here $N_0$ is the density of pristine Si-H bonds present in the fresh device, while $\Re_\mathrm{a/p}$ are the cumulative bond activation/passivation rates. $\Re_\mathrm{a}$ can be obtained by summation of the bond breakage rates from each level weighed with its population number [13, 14, 15]:

$$\Re_\mathrm{a} = \frac{1}{k}\sum_{r=0} R_{a,i}\left(\frac{P_\mathrm{u}}{P_\mathrm{d}}\right)^i, \tag{4.35}$$

while $\Re_\mathrm{p}$ is attributed to thermal activation and is represented by an Arrhenius term over a single energy level as:

$$\Re_\mathrm{p} = \nu_\mathrm{p}\exp(-E_\mathrm{p}/k_\mathrm{B}T_\mathrm{L}) \tag{4.36}$$

Finally, the following analytic expression for the interface state density $N_\mathrm{it}$ is obtained:

$$\begin{aligned} N_\mathrm{it} &= \frac{1}{2\tau\Re_p}\frac{1-f(t)}{1+f(t)} - \frac{\Re_\mathrm{a}}{2\Re_\mathrm{p}}, \\ f(t) &= \frac{1-\tau\Re_\mathrm{a}}{1+\tau\Re_\mathrm{a}}\exp\left(-t/\tau\right), \\ \frac{1}{\tau} &= 2\sqrt{\Re_a^2/4 + N_0\Re_\mathrm{a}\Re_\mathrm{p}}, \end{aligned} \tag{4.37}$$

The activation energy for this reaction can be reduced by the interaction of the bond dipole moment $d$ with the oxide electric field $E_\mathrm{ox}$ [13, 15, 14]. The acceleration integral in Equation 4.29 then becomes:

$$I_\mathrm{SC/MC}^\mathrm{e/h} = \int f(\varepsilon)g(\varepsilon)v(\varepsilon)\sigma_{0,\mathrm{SC/MC}}(\varepsilon - \varepsilon_\mathrm{th} + dE_\mathrm{ox})^{p_\mathrm{SC/MC}}\mathrm{d}\varepsilon \tag{4.38}$$

The Si-H bond activation energy also varies due to the structural disorder at the Si/SiO$_2$ interface which can lead to substantial changes in the device degradation characteristics simulated with the model. The energy $E_\mathrm{a}$ is assumed to obey a normal distribution with a mean value $\langle E_\mathrm{a}\rangle$ of 2.56 eV and standard deviation $\sigma_{\mathrm{E_a}}$ of 0.15 eV [193, 194, 13].

Equation 4.37 allows evaluation of the interface state density for each position at the Si/SiO$_2$ interface and for each stress time step. $N_\mathrm{it}(x,t)$ profiles calculated from Equation 4.37 are then used as input for the device simulator to model the characteristics of the degraded device for each stress time step. The effect of charged interface traps is twofold: they perturb the local band-bending of the device and degrade the carrier mobility due to scattering of the charge carriers. The former effect is considered while solving the coupled Poisson and Boltzmann equations, while for the latter one an empirical expression for mobility degradation is used [195, 196]:

$$\mu_{\mathrm{degr}} = \frac{\mu_0}{1 + \alpha N_{\mathrm{it}} \exp(-r/r_{\mathrm{ref}})}, \tag{4.39}$$

where $\mu_0$ is the mobility in the virgin device, $r$ is the shortest distance from this local point to the interface, $r_{\mathrm{ref}} = 10\,\mathrm{nm}$ defines the maximum range within which a carrier is still influenced by the field of the trapped charge, while the parameter $\alpha = 10^{-13}\,\mathrm{cm}^2$ determines the magnitude of the effect.

| Parameter | Value | Comments |
|---|---|---|
| $\tau_{\mathrm{n/p}}$ | $\tau_{\mathrm{n}} = 0.35\,\mathrm{ps}$, $\tau_{\mathrm{p}} = 0.4\,\mathrm{ps}$ | Energy relaxation time |
| $\sigma_0$ | $\sigma_{0,\mathrm{SC}} = 5 \times 10^{-18}\,\mathrm{cm}^2$, $\sigma_{0,\mathrm{MC}} = 5 \times 10^{-19}\,\mathrm{cm}^2$ | Pre-factor in reaction cross section |
| $p$ | $p_{\mathrm{SC}} = 11$, $p_{\mathrm{MC}} = 1$ | Exponent in reaction cross section |
| $\langle E_{\mathrm{a}} \rangle$ | $2.56\,\mathrm{eV}$ | Si-H bond activation energy |
| $\sigma_{\mathrm{Ea}}$ | $0.15\,\mathrm{eV}$ | Standard deviation of activation energy |
| $\hbar\omega$ | $0.25\,\mathrm{eV}$ | Distance between bond vibrational states |
| $\omega_{\mathrm{e}}$ | $\omega_{\mathrm{e}} = 1/\tau$, $\tau = 1.5\,\mathrm{ns}$ | Reciprocal phonon lifetime |
| $\omega_{\mathrm{th}}$ | $5 \times 10^6\,\mathrm{s}^{-1}$ | Attempt frequency for thermal activation |
| $\nu_{\mathrm{p}}$ | $10^8\,\mathrm{s}^{-1}$ | Passivation attempt frequency |
| $E_{\mathrm{p}}$ | $1.5\,\mathrm{eV}$ | Passivation energy |
| $N_0$ | $1 \times 10^{11}\,\mathrm{cm}^{-2}$ | Density of precursors |

Table 4.2: The parameters used in the HCD model.

# Chapter 5

# HCD Modeling in LDMOS Devices

The LDMOS (laterally-diffused metal-oxide semiconductor) transistors are often the devices of choice in smart-power, mixed signal ICs, and high voltage automotive applications. The popularity of these transistors is also attributed to the fact that they are compatible with standard CMOS processing. This makes them easily integrable by adding a few extra process steps. Thus, radio frequency and mixed signal applications can be integrated along with the core logic transistors on a single chip. The desired breakdown voltage in LDMOS devices can be easily obtained if a suitable concentration of dopant species is chosen. However, the long drift regions cause an increase in the required chip surface while the low doping results in high power loss due to an increased ON-resistance. With the introduction of reduced surface field technology, LDMOS devices are better optimized and can provide high blocking voltages for shorter drift lengths and higher doping [197]. Thus, the ON-resistance is reduced leading to smaller power dissipation. However, lateral devices are more susceptible to hot-carrier degradation as the current flows at the Si/SiO$_2$ interface and not in the bulk as, for e.g., is the case in vertical DMOS devices.

Unfortunately, a proper treatment of carrier transport in LDMOS devices is challenging. First, due to the large dimensions of these devices as compared to nanoscale CMOS transistors, the simulation mesh contains a large number of elements $\backsim$10,000 [26]. Second, this transistor usually has a bird's beak/STI corner and curved interfaces, see Figure 5.1, and also high doping gradients in various regions. Finally, LDMOS transistors are operated/stressed at high voltages. In this section, the hot-carrier degradation model (Section 4.3-4.4), which uses the information about the carrier energy distribution is used to represent HCD data measured in n- and p-channel LDMOS transistors. The analytical (Section 4.3) and ViennaSHE based versions of the model are compared to show that both approaches can capture HCD. Particular attention is paid to study the role of the cold fraction of the carrier ensemble. The validity of the model is checked by neglecting the effect of cold carriers in HCD modeling in the case of LDMOS devices stressed at high voltages. Finally, it is shown that even in high-voltage devices stressed at high drain voltages the thermalized carriers still have a substantial contribution to HCD.

## 5.1 Experiments

To validate the model, experiments were performed using n- and p-channel LDMOS transistors. The n- and pLDMOS transistors used in this work, shown in Figure 5.1, designed on 0.35 $\mu$m and 0.18 $\mu$m standard CMOS processes, respectively, have been subjected to

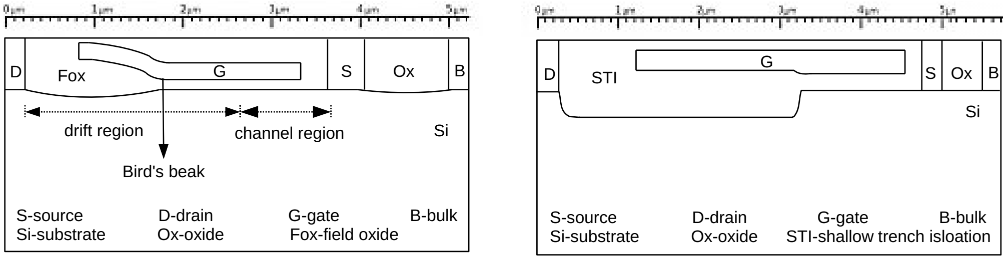

Figure 5.1: The schematic representation of the nLDMOS (left panel) and pLDMOS (right panel) transistors with all the characteristic sections labeled.

hot-carrier stress at different combinations of gate and drain voltages $V_{\mathrm{gs}}$ and $V_{\mathrm{ds}}$. The n-channel devices have a Si/SiO$_2$ interface length of $\sim$3.4 $\mu$m (length of the drift region is 2.4 $\mu$m, while the channel length is 1.0 $\mu$m), and a gate length of $\sim$2.5 $\mu$m. The p-channel transistors have an interface length of $\sim$4.4 $\mu$m, and a gate length of $\sim$3.3 $\mu$m.

The nLDMOS transistors were subjected to hot-carrier stress with six different combinations of drain and gate voltages $V_{\mathrm{ds}}$, $V_{\mathrm{gs}}$ (i.e. at $V_{\mathrm{gs}} = 2.0$ V and $V_{\mathrm{ds}} = 18, 20, 22$ V; $V_{\mathrm{ds}} = 20$ V and $V_{\mathrm{gs}} = 1.2, 1.5, 2.0$ V) at room temperature for stress times up to $\sim$1 Ms. As for the pLDMOS devices, they were stressed at $V_{\mathrm{ds}} = -50$ V and $V_{\mathrm{gs}} = -1.5, -1.7$ V for stress times up to $\sim$40 ks. To monitor HCD, the normalized changes in the linear drain current $\Delta I_{\mathrm{d,lin}}(t)$ (at $V_{\mathrm{ds}} = 0.1$ V and $V_{\mathrm{gs}} = 3.6$ V) and the saturation drain current $\Delta I_{\mathrm{d,sat}}(t)$ (at $V_{\mathrm{ds}} = 10$ V and $V_{\mathrm{gs}} = 3.6$ V) were recorded as a function of stress time for nLDMOS devices. The degradation of the threshold voltage $\Delta V_{\mathrm{t}}(t)$ was also recorded for all stress conditions using the maximum transconductance method. For the pLDMOS, $\Delta I_{\mathrm{d,sat}}(t)$ at $V_{\mathrm{ds}} = -50$ V and $V_{\mathrm{gs}} = -2.5$ V was monitored. The relative drifts in the currents at any time $t$ are defined as:

$$\Delta I_{\mathrm{d}}(t) = \frac{I_{\mathrm{d}}(t) - I_{\mathrm{d}}(0)}{I_{\mathrm{d}}(0)} \tag{5.1}$$

while the relative threshold voltage shifts are defined as:

$$\Delta V_{\mathrm{t}}(t) = \frac{V_{\mathrm{t}}(t) - V_{\mathrm{t}}(0)}{V_{\mathrm{t}}(0)} \tag{5.2}$$

## 5.2 Simulation Framework

The carrier energy distribution function is sensitive to details of the doping profiles and to the device architecture. The device structure of the n- and pLDMOS transistors was generated by the Sentaurus Process simulator [198] which was coupled to the device simulator MINIMOS-NT [124, 125] and calibrated self-consistently in order to reproduce the characteristics of the fresh transistor. An important ingredient for reliable and adequate simulations of the carrier DF with ViennaSHE is a proper mesh. It is important to emphasize that even with the DD scheme, modeling of such a large LDMOS transistor with a complicated geometry is a non-trivial task. On the one hand the required mesh is expected to be fine enough especially near the Si/SiO$_2$ interface, at the bird's beak, and close to other important device regions. On the other hand, the mesh should only contain a mod-

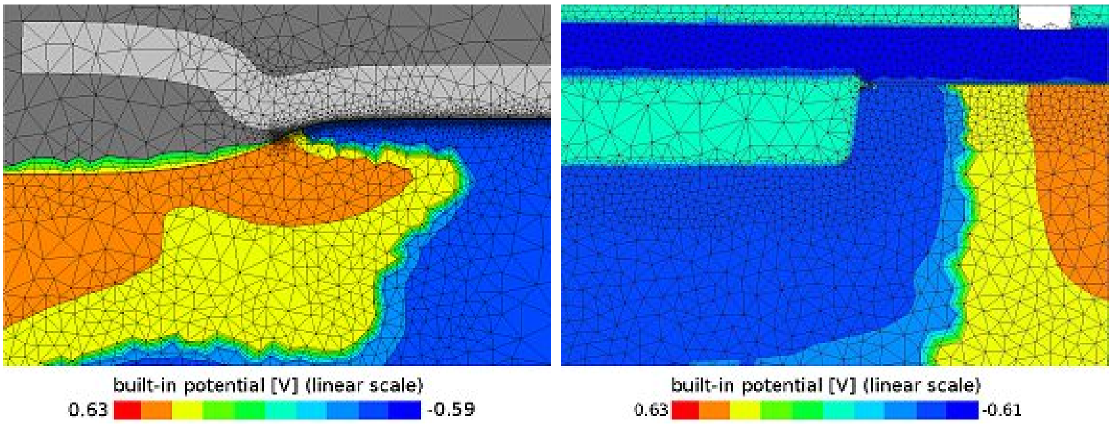

Figure 5.2: The adaptive mesh for a near interface device section of the nLDMOS (left figure) and the pLDMOS (right figure) transistors with the built-in potential represented by the color map.

erate number of elements in order to ensure a reasonable simulation time. For instance, such a mesh can be coarse in the Si bulk. To achieve these goals, the highly adaptive meshing framework ViennaMesh is used [199]. ViennaMesh generates meshes based on the built-in potential, see Figure 5.2 [26]. The resulting mesh has a fine resolution in important regions, a sufficiently low density in less important regions and contains about 11,000 elements. ViennaMesh proves to be beneficial not only for SHE simulations, but also also for the DD simulations in MINIMOS-NT.

## 5.3 Spherical Harmonics Expansion Solution

ViennaSHE is a deterministic BTE solver which considers energy exchange mechanisms such as the electric field, impact ionization, electron-electron and electron-phonon scattering, scattering at ionized impurities, surface scattering, and full-band effects [18, 20, 200]. A cell-centered discretization scheme used in ViennaSHE simplifies the treatment of material interfaces and can be used on arbitrary grids, not requiring the Delaunay property [46]. As a result, ViennaSHE provides smooth DF curves spreading over many orders of magnitude and over several electronvolts.

Figure 5.3 shows two sets of electron DFs obtained for $V_{\mathrm{gs}} = 2\,\mathrm{V}$ and $V_{\mathrm{ds}} = 20\,\mathrm{V}$ and for different positions in the nLDMOS device, i.e. one set corresponds to the bird's beak region, while the second one summarizes DFs evaluated for the drain region. One can see that the carrier DFs are severely non-equilibrium. While at the drain DFs have a cold Maxwellian tail at low energies, the DFs calculated for the bird's beak do not have this contribution and their shape is completely different. In all cases the DFs have extended high-energy tails. The DFs for the pLDMOS transistor obtained for $V_{\mathrm{ds}} = -50\,\mathrm{V}$, $V_{\mathrm{gs}} = -1.5\,\mathrm{V}$ are shown in Figure 5.4. The DFs calculated with ViennaSHE for the STI corner and the drain region have a considerable amount of high energy carriers. These DFs are used as a benchmark for the DD-based approach.

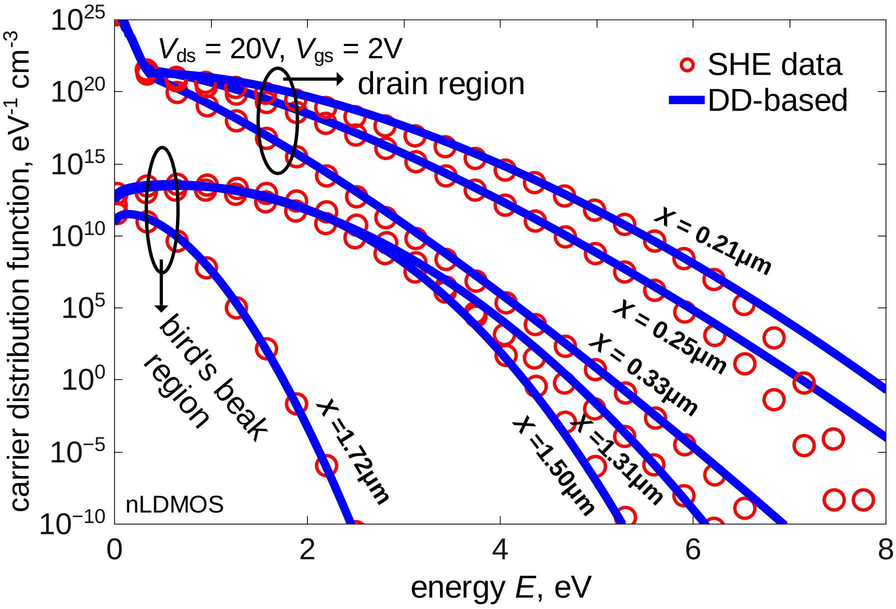

Figure 5.3: The electron DFs obtained with ViennaSHE and with the DD-based model for $V_{\mathrm{ds}} = 20\,\mathrm{V}$, $V_{\mathrm{gs}} = 2\,\mathrm{V}$, calculated for different positions near the drain and close to the bird's beak region of the nLDMOS transistor.

## 5.4 Drift-Diffusion Based Model

To avoid the cumbersome SHE simulations, the approximate DD method described in Section 4.3 is used. As can be seen in Figures 5.3 and 5.4, the DD-based model for the carrier

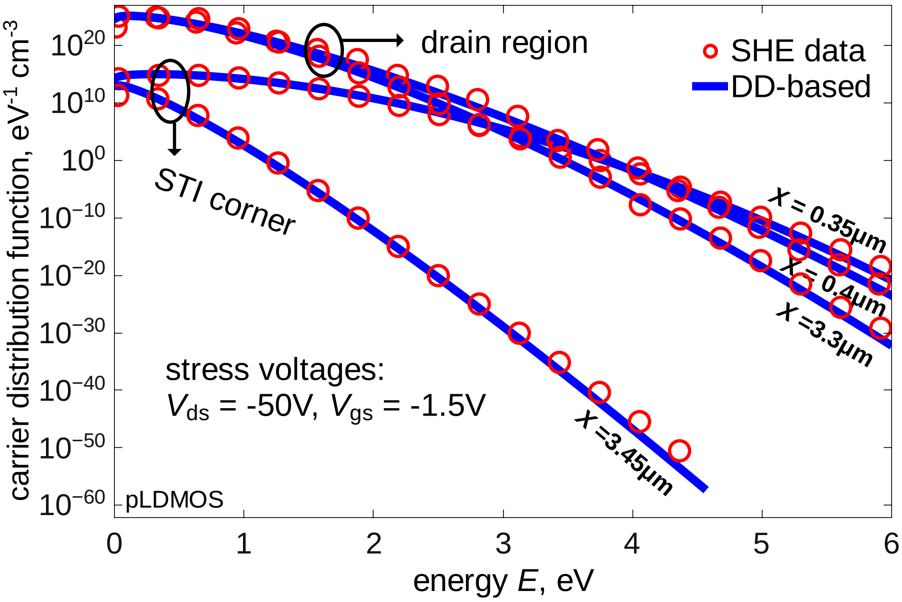

Figure 5.4: The hole DFs obtained with ViennaSHE and with the DD-based model for $V_{\mathrm{ds}} = -50\,\mathrm{V}$, $V_{\mathrm{gs}} = -1.5\,\mathrm{V}$, calculated for different positions near the drain and close to the STI region of the pLDMOS transistor.

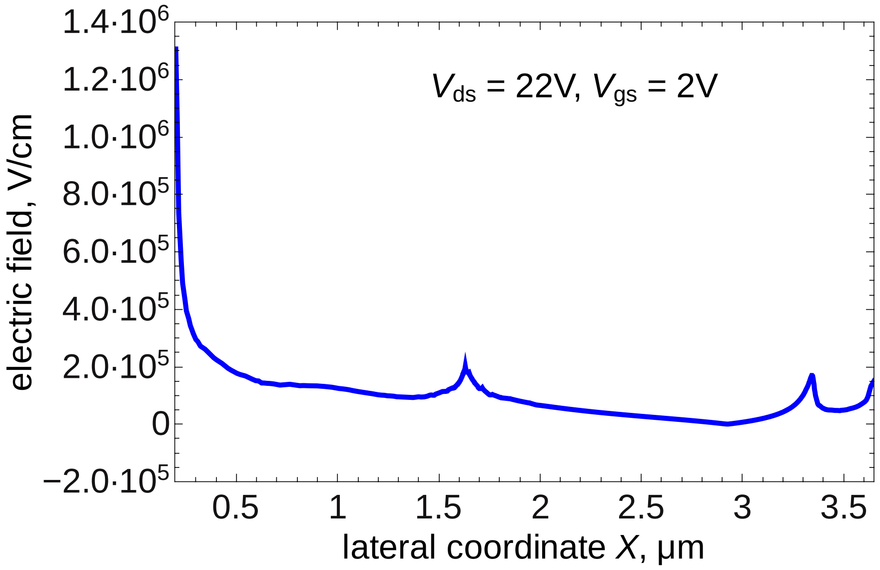

Figure 5.5: Electric field profiles simulated with MINIMOS-NT for an nLDMOS at $V_{\mathrm{ds}}$ = 22 V, $V_{\mathrm{gs}}$ = 2 V.

DF represented by Equation 4.22 can predict the DF curves as accurately as the SHE method [147]. The high concentration of traps in low energy region suggests that also in the case of long-channel and/or high-voltage devices, the multiple-carrier process has a significant contribution and cannot be ignored [26, 13, 147].

It is important to note that the contribution of oxide traps was not considered. There are two reasons for this. First, bulk oxide traps are known to be responsible for the recoverable component of degradation [56]. However, in the devices used in this work, no recovery was observed under the stress conditions used here. Second, various studies on the intimately related phenomenon of bias temperature instability suggest that trapping in the oxide bulk starts to play a prominent role at oxide fields of 6 MV/cm and higher [115]. The maximum oxide field in the nLDMOS transistors used was ∼1.3 MV/cm for $V_{\mathrm{ds}}$ = 22 V, $V_{\mathrm{gs}}$ = 2 V which is significantly smaller than 6 MV/cm, see Figure 5.5. Therefore, the contribution of bulk oxide traps can be neglected.

The effect of majority carriers is twofold: they can contribute to the interface trap generation and also be captured by existing amphoteric traps. The former mechanism was reported to be responsible for threshold voltage and drain current turn-around effects [201, 202]. In the measurements, however, no turn-around effects were observed implying that the majority carrier contribution to HCD is weak. Drift-diffusion simulations performed for the LDMOS devices, as discussed in next section, also showed that impact ionization leads to low or moderate majority carrier concentrations throughout the channel in the interface region.

## 5.5 Modeling the Degradation in nLDMOS Transistor

The DD-based scheme is able to represent the carrier distribution functions for the source and channel regions. Note that in these device sections the DFs are not severely per-

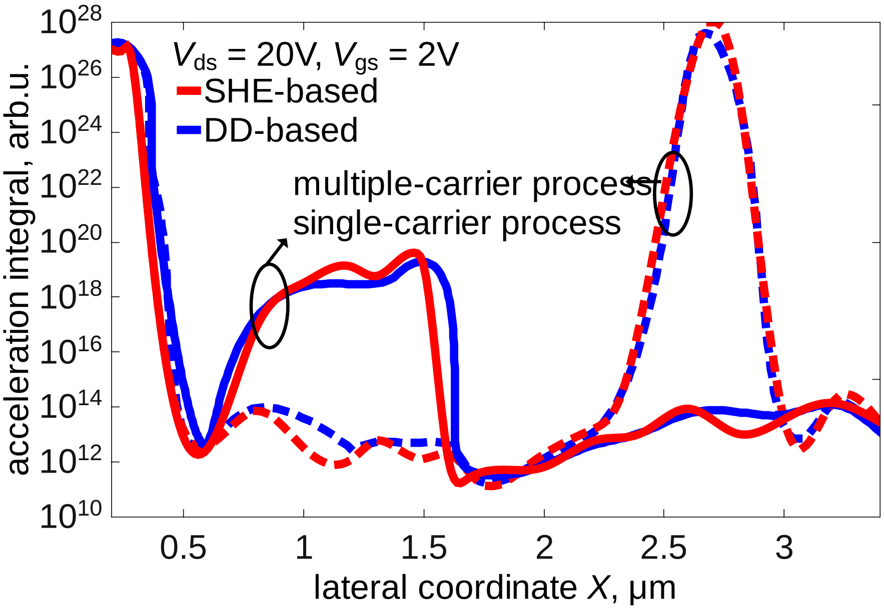

Figure 5.6: The acceleration integral in an nLDMOS calculated using the DFs obtained with the DD-based model and using ViennaSHE for $V_{\mathrm{ds}} = 20\,\mathrm{V}$, $V_{\mathrm{gs}} = 2\,\mathrm{V}$ for the single- and multiple-carrier processes.

turbed from equilibrium. As already shown in Figure 5.3, the agreement between the non-equilibrium DFs is also good, especially near the bird's beak of the nLDMOS transistor. As for the drain region, a small discrepancy is visible at high energies. At these high energies, however, the DF has dropped by more than 20 orders of magnitude and this dis-

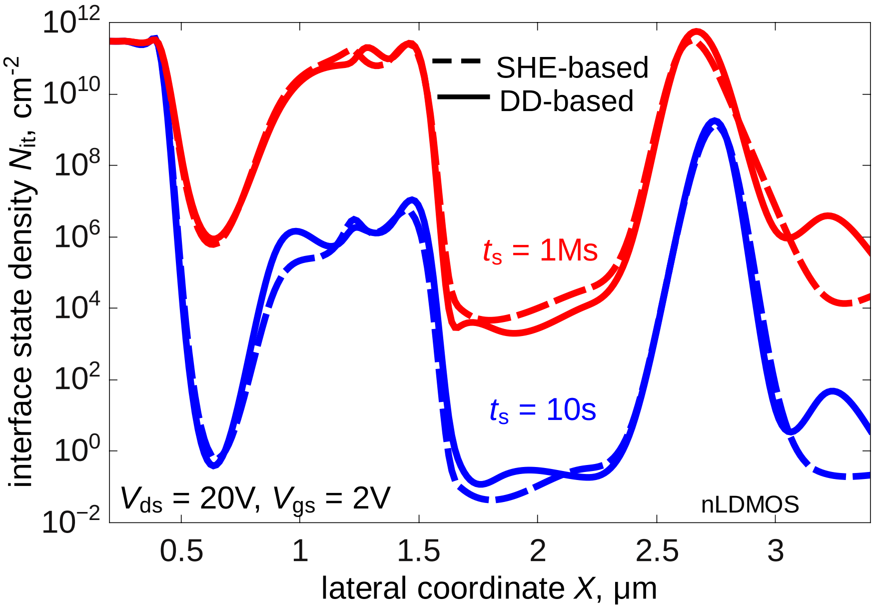

Figure 5.7: Interface state density profiles in an nLDMOS evaluated with the DD- and SHE-based models for stress voltages $V_{\mathrm{ds}} = 20\,\mathrm{V}$, $V_{\mathrm{gs}} = 2\,\mathrm{V}$ applied for 10 s and 1 Ms.

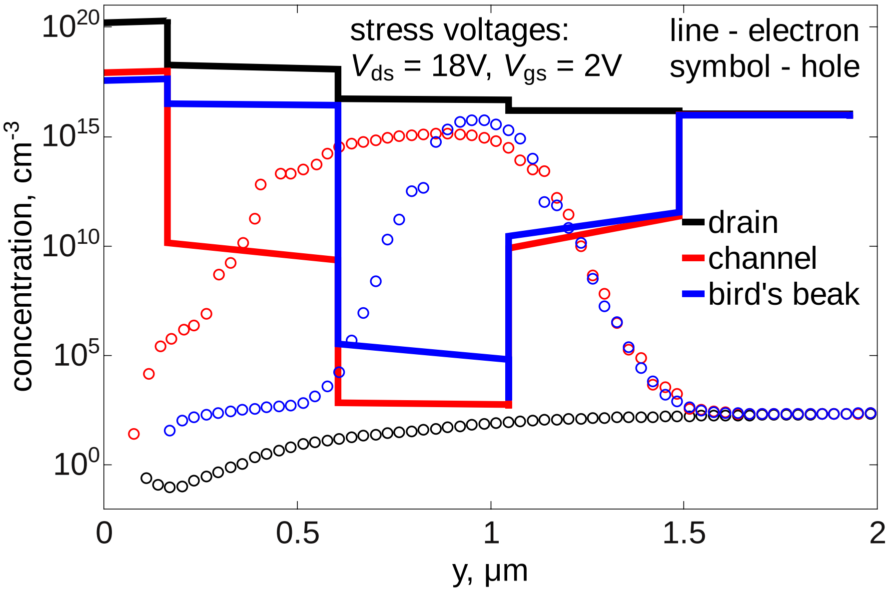

Figure 5.8: The electron and hole concentrations in an nLDMOS as a function of the coordinate $y$ perpendicular to the Si/SiO$_2$ interface evaluated near the drain region, the bird's beak, and in the channel.

crepancy does not transform into a significant error of the model. To prove this, the acceleration integrals calculated by Equation 4.29 are plotted for both the single- and multiple-carrier processes. Figure 5.6 shows that the acceleration integrals computed with the SHE- and DD-based approaches are quite similar, and thus the discrepancy in the DFs at high energies, visible for the case of the drain region, is insignificant. Figure 5.6 also demonstrates that the multiple-carrier process plays an important role in large devices such as the nLDMOS transistor and should be considered in the model. This is because the peak in the acceleration integral vs the lateral device coordinate curve at $x \sim 2.8\,\mu$m corresponds to the multiple-carrier bond breakage process indicating that the MC-mechanism is the major source of defect creation near the source region of the device.

The $N_{\mathrm{it}}(x)$ profiles simulated using the SHE- and DD-based approaches for the entire lateral coordinate range and for 10 s and 1 Ms are presented in Figure 5.7. It can be seen from Figures 5.3 and 5.6 that the carriers near the drain are rather hot and both the single- and multiple-carrier mechanisms are saturated, thus leading to an $N_{\mathrm{it}}$ peak at the drain region. Another peak is pronounced in the vicinity of the bird's beak which is due to the single-carrier process as the rate of the multiple-carrier process (Figure 5.6) is negligible in this region. The third $N_{\mathrm{it}}$ maximum located in the channel at $x \sim 2.8\,\mu$m stems from the common action of the multiple-carrier mechanism of the bond dissociation and the interaction of the dipole moment of the bond with the electric field [26]. The role of this $N_{\mathrm{it}}$ peak in the channel is also important for the representation of the overall device degradation.

It is worth discussing that only the electron induced portion of the degradation is considered because the hole concentration at the interface is very low. Figure 5.8 shows the hole concentration plotted as a function of the coordinate orthogonal to the Si/SiO$_2$ interface evaluated for three different positions in the nLDMOS devices: at the drain, in

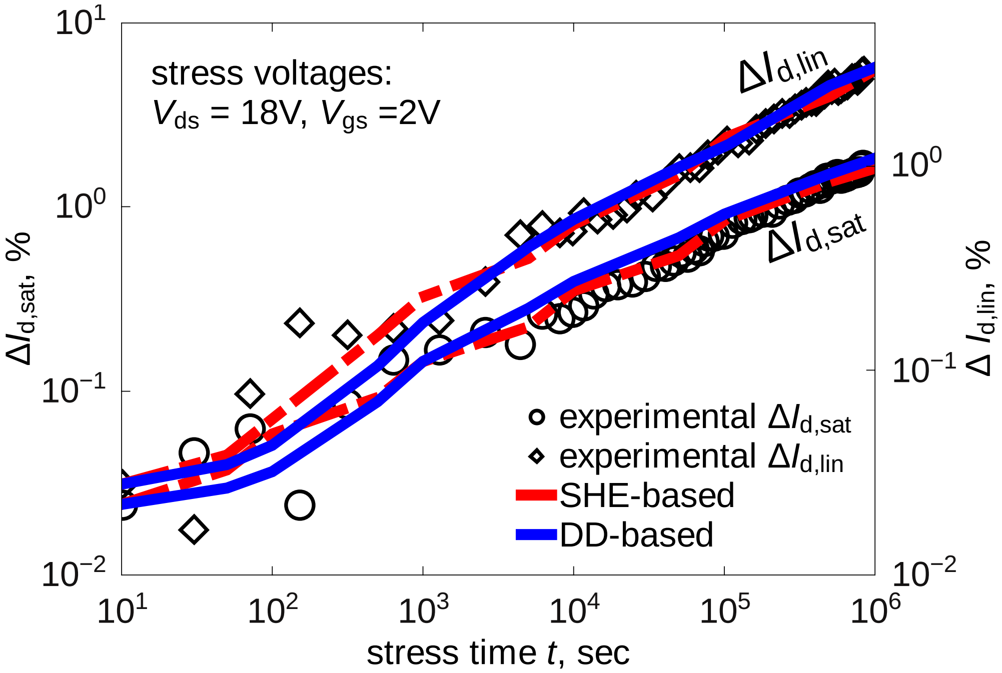

Figure 5.9: The experimental change in the saturation and the linear drain currents plotted vs. simulations obtained with the SHE- and DD-based versions of the model for a gate voltage $V_{gs} = 2\,\mathrm{V}$ and drain voltage $V_{ds} = 18\,\mathrm{V}$ in an nLDMOS transistor.

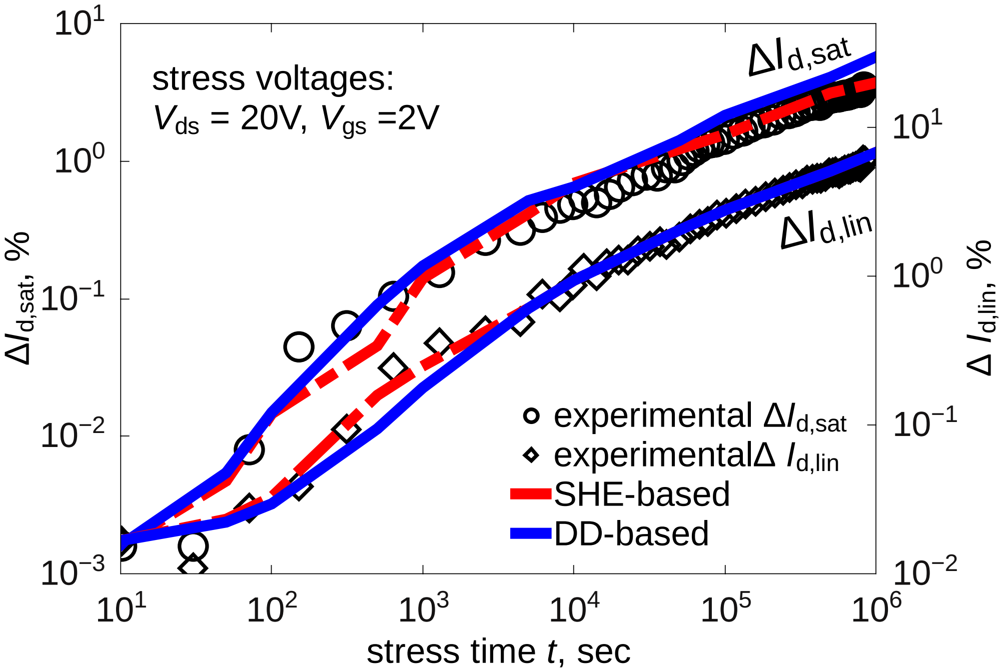

Figure 5.10: Same as Figure 5.9 but for $V_{gs} = 2\,\mathrm{V}$ and $V_{ds} = 20\,\mathrm{V}$.

the channel, and near the bird's beak. For comparison, the electron concentration profiles are also plotted in Figure 5.8. One can see that the hole concentration at the interface does

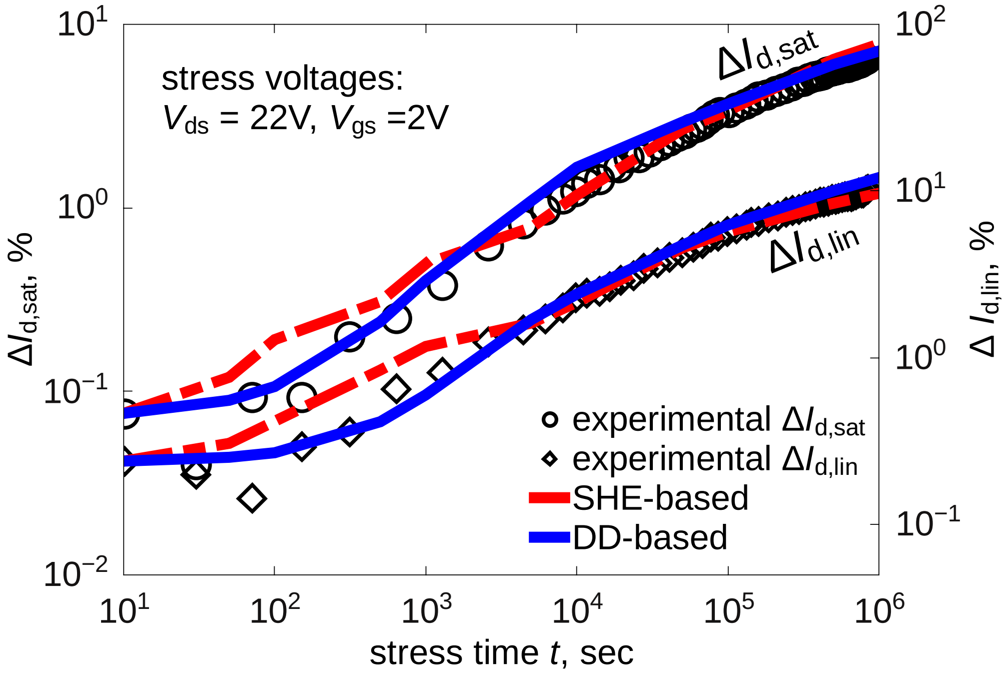

Figure 5.11: Same as Figure 5.9 but for $V_{gs} = 2\,\text{V}$ and $V_{ds} = 22\,\text{V}$.

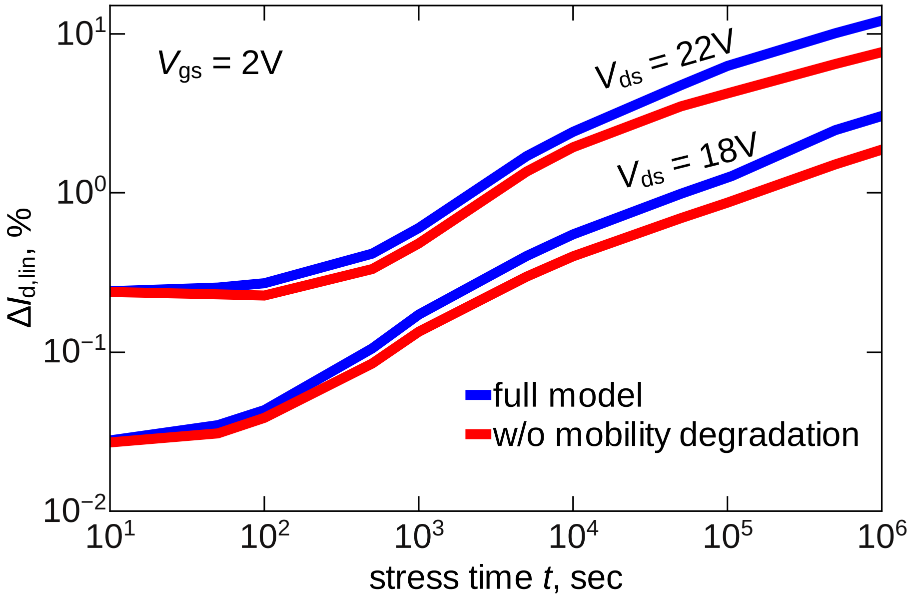

Figure 5.12: The relative change in the linear drain current simulated with the DD-based version of the model for an nLDMOS transistor. One can see that if the mobility degradation is not considered, the change in current can be severely underestimated. For instance, at a stress time of 1Ms the error in $I_{d,lin}(t)$ is 27%.

not exceed $10^5\,\text{cm}^{-3}$, i.e. around 15 orders of magnitude lower than the electron concentration. Therefore, we conclude that the contribution of holes can be neglected. The normalized experimental change of the linear and saturation drain currents simulated with

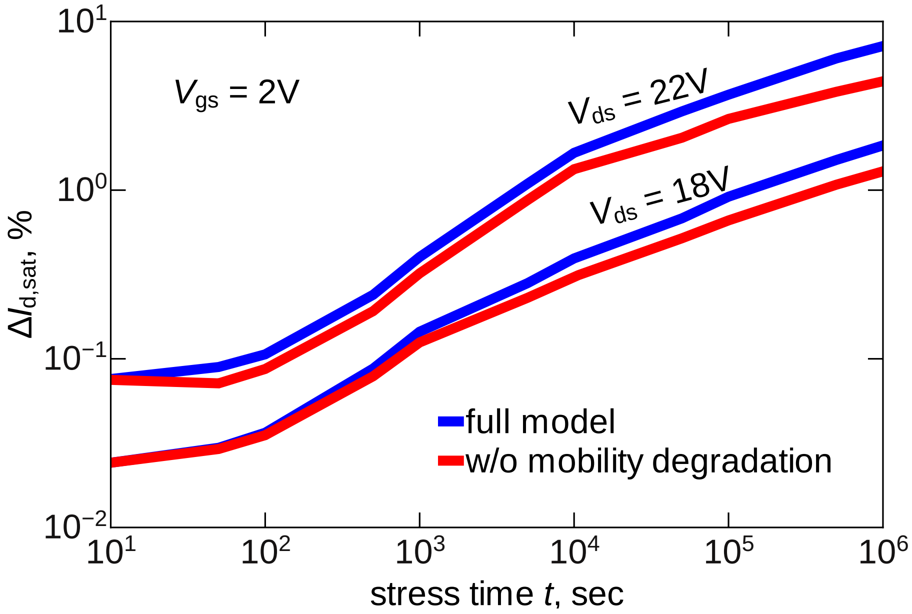

Figure 5.13: The relative change in $I_{\mathrm{d,sat}}$ simulated with the DD-based version of the model for an nLDMOS transistor. At a stress time of 1Ms the error in $I_{\mathrm{d,sat}}(t)$ is 33%.

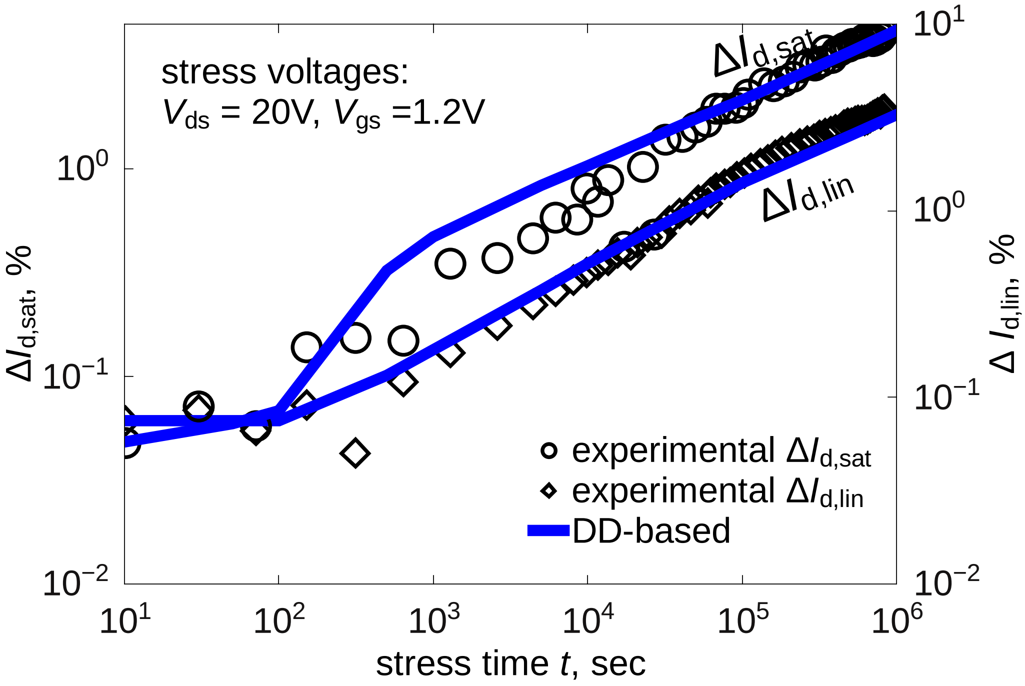

Figure 5.14: The change in the saturation and linear drain currents: experiment vs. the DD-based model in an nLDMOS. Results are obtained for a drain voltage $V_{\mathrm{ds}} = 20\,\mathrm{V}$ and gate voltage $V_{\mathrm{gs}} = 1.2\,\mathrm{V}$.

the SHE- and DD-based versions of the HCD model is plotted against the experimental data in Figures 5.9, 5.10 and 5.11 for a fixed gate voltage of $V_{\mathrm{gs}} = 2\,\mathrm{V}$ and a series of three

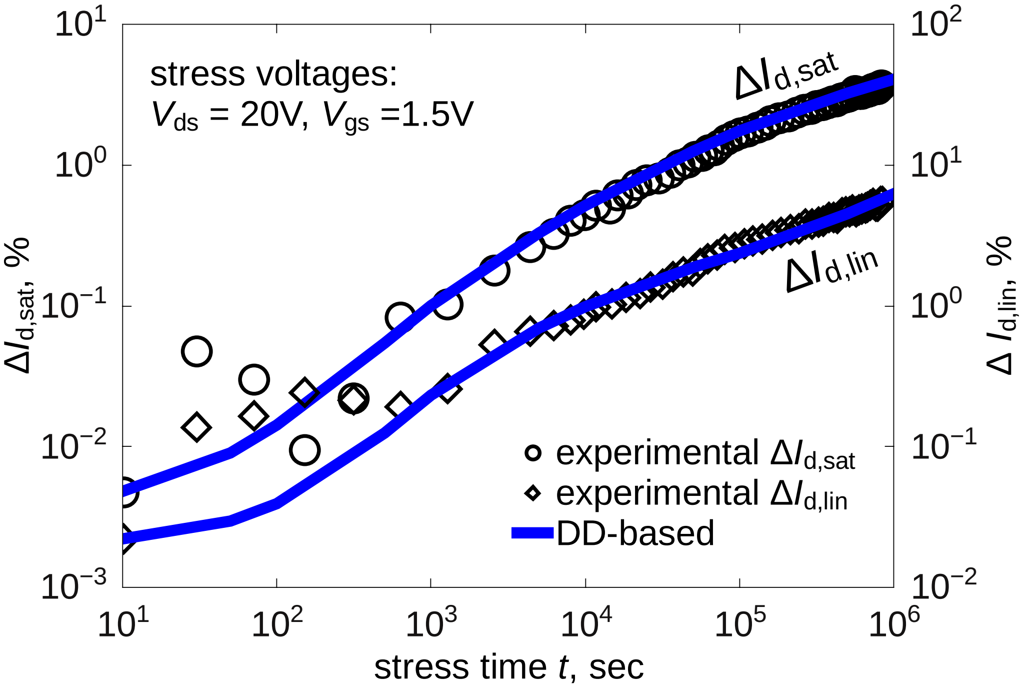

Figure 5.15: Same as Figure 5.14 but for $V_{\mathrm{ds}} = 20\,\mathrm{V}$ and $V_{\mathrm{gs}} = 1.5\,\mathrm{V}$.

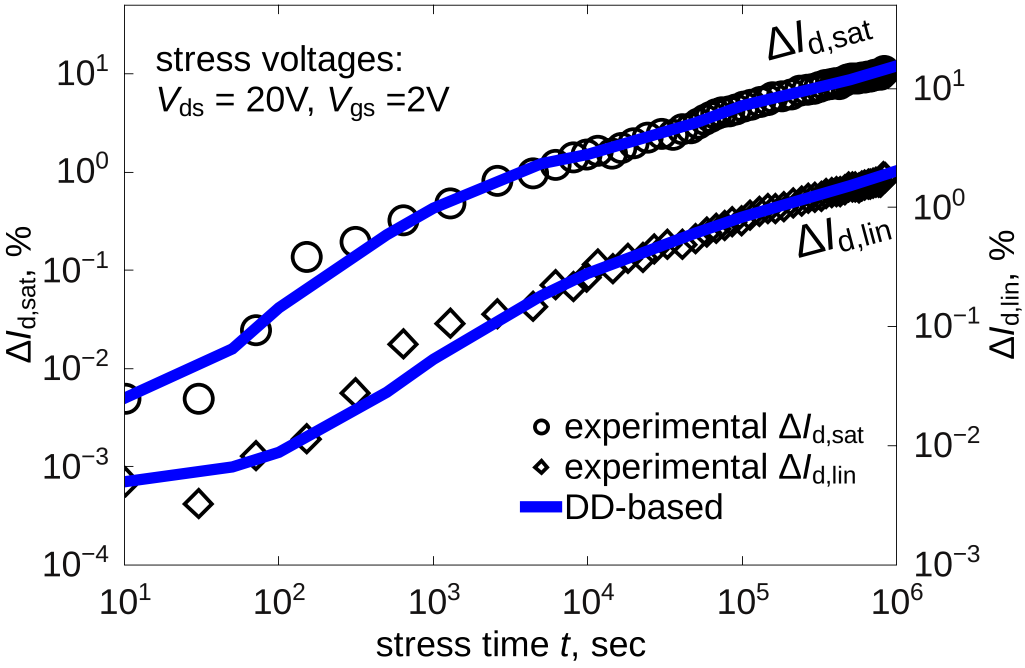

Figure 5.16: Same as Figure 5.14 but for $V_{\mathrm{ds}} = 20\,\mathrm{V}$ and $V_{\mathrm{gs}} = 2\,\mathrm{V}$.

different drain voltages: $V_{\mathrm{ds}} = 18$, 20, and 22 V. One can see that the agreement between the experimental results and the simulated data is very good. It is important to emphasize that the $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ curves obtained with the SHE- and DD-based versions of

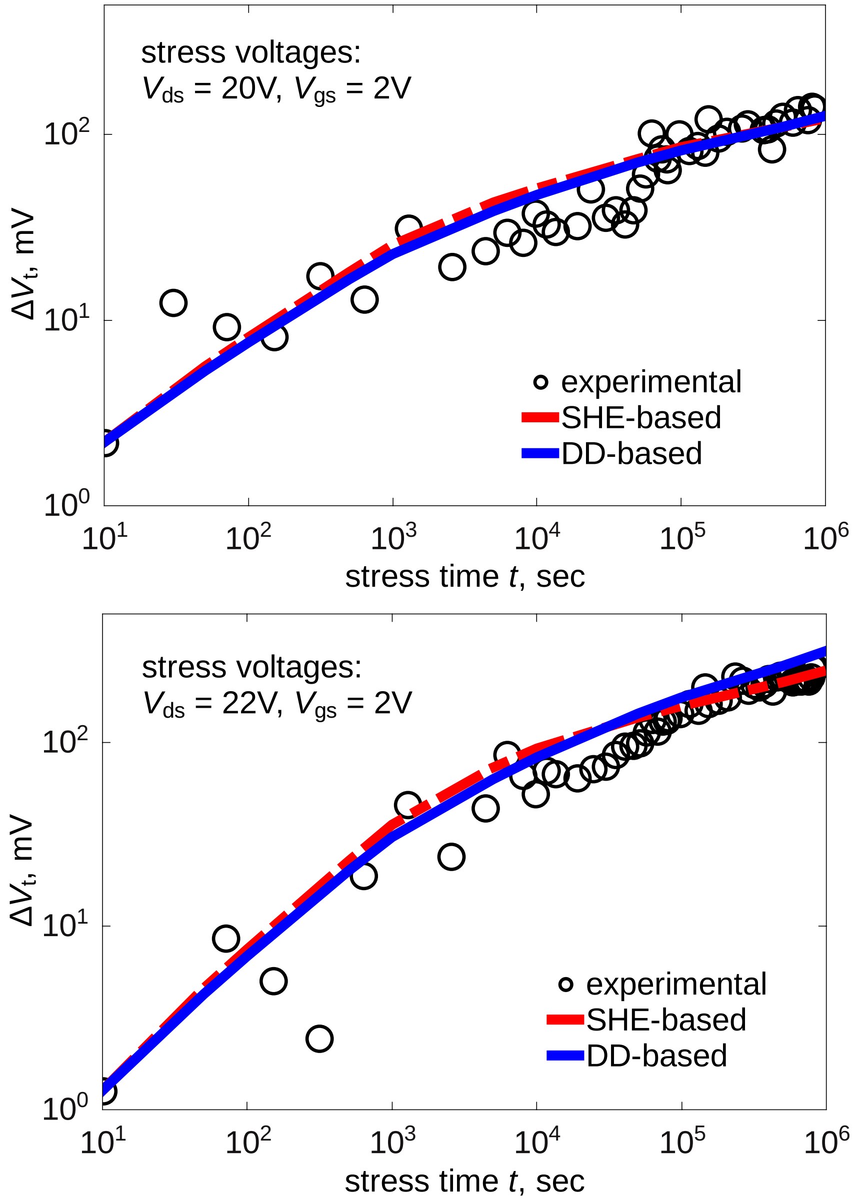

Figure 5.17: Comparison of the change in the threshold voltage obtained from experiments and simulation in an nLDMOS, using the SHE- and DD-based models, for stress voltages $V_{\rm gs} = 2\,\rm V$ and $V_{\rm ds} = 20$ and $22\,\rm V$ for stress times up to $1\,\rm Ms$.

the model are almost the same within the whole experimental time window. This makes the latter version attractive for efficient and predictive HCD simulations of nLDMOS devices. Figures 5.12 and 5.13 show the $\Delta I_{\rm d,lin}(t)$ and $\Delta I_{\rm d,sat}(t)$ traces simulated with the DD-based version of the model with and without the effect of mobility degradation (see Equation 4.39). One can see that for the entire stress time window the current degradation simulated considering only the electrostatics perturbation due to the interface state build-up is substantially underestimated.

To check the DD-based model in greater detail, the normalized changes in the linear and saturation drain currents simulated exclusively with the DD-model for a fixed $V_{\rm ds} =$

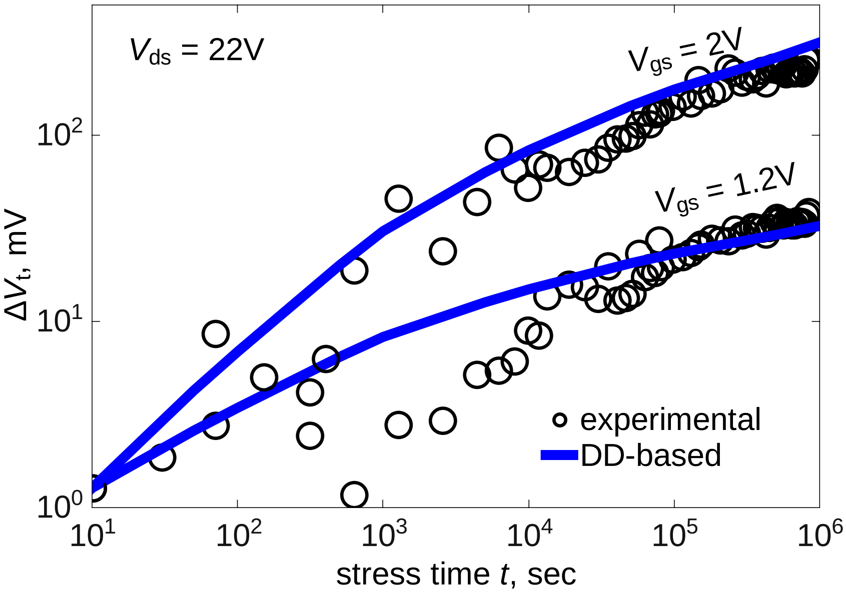

Figure 5.18: The threshold voltage shift vs. stress time: a comparison between experiment and simulation with the DD-based model for a fixed drain voltage $V_{\mathrm{ds}} = 22\,\mathrm{V}$ and two different gate voltages $V_{\mathrm{gs}} = 1.2$ and $2\,\mathrm{V}$.

20 V and three different $V_{\mathrm{gs}} = 1.2$, 1.5, and 2.0 V are plotted in Figures 5.14, 5.15 and 5.16. It can be concluded that the agreement between the experimental data and the degradation traces is very good. This is also the case for the threshold voltage shifts $\Delta V_{\mathrm{t}}(t)$ for $V_{\mathrm{gs}} = 2\,\mathrm{V}$ and $V_{\mathrm{ds}} = 20\,\mathrm{V}$ and 22 V obtained with both versions of the HCD model and plotted vs. the measured $\Delta V_{\mathrm{t}}(t)$ traces, as shown in Figure 5.17. Again, as in the case of the drain current degradation, the DD-based model is applied to represent $\Delta V_{\mathrm{t}}(t)$ traces for $V_{\mathrm{ds}} = 22$ and $V_{\mathrm{gs}} = 1.2$ and 2 V without using the ViennaSHE DFs as a reference, see Figure 5.18, and a good agreement between experiments and theory is obtained. It is important to emphasize that all above simulations were carried out with the same parameter set.

## 5.6 Modeling the Degradation in pLDMOS Transistor

The validity of the model beyond the nLDMOS transistor was tested by following a similar procedure for calculating DFs, $N_{\mathrm{it}}(x)$ profiles, and drain current degradation curves for an pLDMOS. Even in this case, the DFs obtained from the DD-based approach and SHE method are quite similar as was shown in Figure 5.4. The DF in the case of the pLDMOS transistor have a slightly different appearance in the drain region as compared to the nLDMOS, lacking the cold carrier part (Figures 5.3 and 5.4), while near the STI corner, they look similar as for the bird's beak region in the nLDMOS. This is due to differences in the architectures (and even different technology nodes) of the n- and p-channel LDMOS transistors used. Another reason which leads to the different shapes of the DFs for the pLDMOS devices is the different stress conditions for n- and p-channel transistors. Due to the high stress voltages used for the pLDMOS ($V_{\mathrm{ds}} = -50\,\mathrm{V}$) as compared to the nLDMOS ($V_{\mathrm{ds}} = 20\,\mathrm{V}$), no high concentration of cold carriers is present at the drain in the former case. As a result, the DFs for the pLDMOS lacks the Maxwellian low energy fragment which

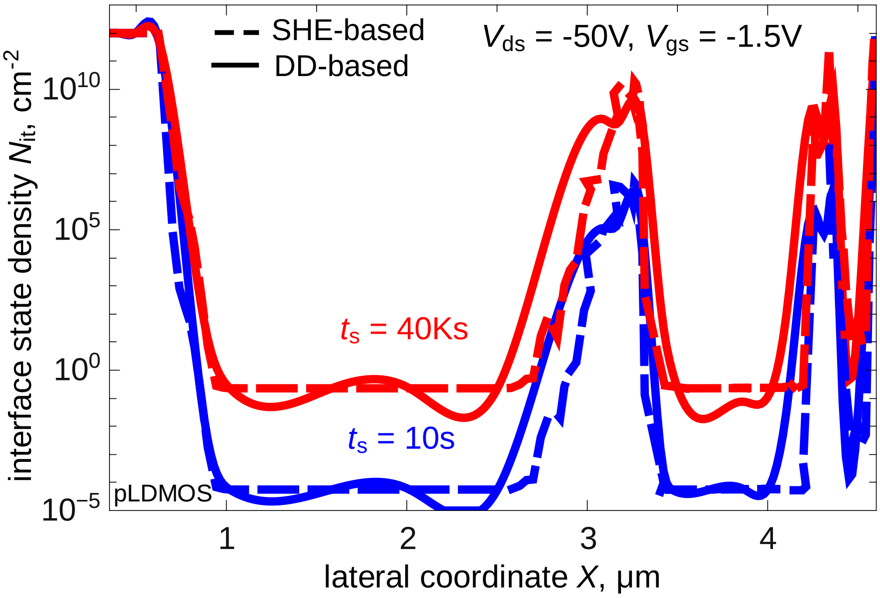

Figure 5.19: Interface state density profiles obtained with SHE- and DD-based models for the pLDMOS transistor. The stress voltages are $V_{ds} = -50\,\text{V}$ and $V_{gs} = -1.5\,\text{V}$ applied for stress times 10 s and 40 ks.

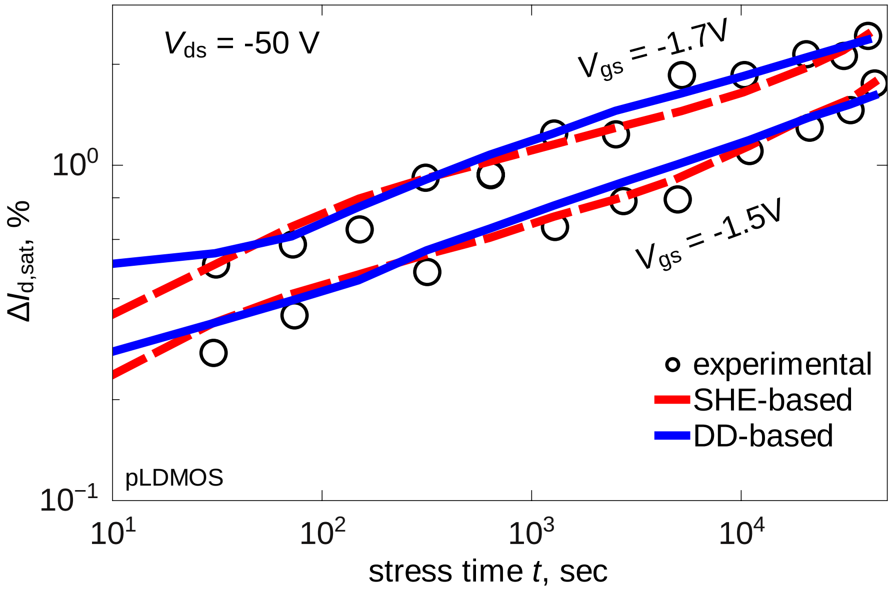

Figure 5.20: Comparison of the change in the saturation drain current in the pLDMOS transistor obtained from experiments and simulations, using the SHE- and DD-based models for stress voltages $V_{ds} = -50\,\text{V}$ and $V_{gs} = -1.5, -1.7\,\text{V}$ for stress times up to 40 ks.

was seen in the DF corresponding to the nLDMOS. The DFs are then used to calculate the $N_{it}(x)$ profiles for the entire lateral coordinate of the pLDMOS transistor. The $N_{it}(x)$ profiles are plotted in Figure 5.19. To demonstrate that the model works well for the pLDMOS device too, the $\Delta I_{d,sat}(t)$ obtained from simulations is compared against the

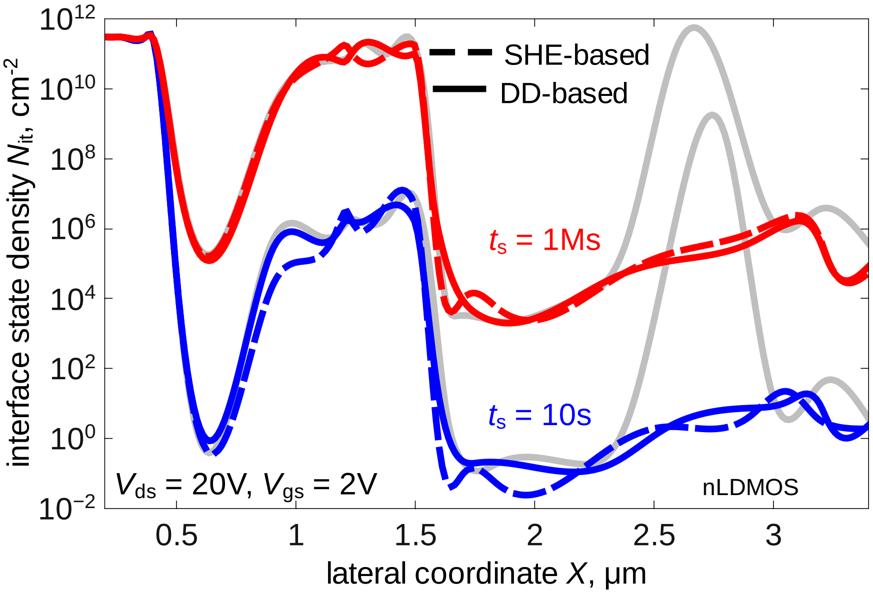

Figure 5.21: Interface state density profiles obtained with SHE- and DD-based models, for the nLDMOS transistor, without the effect of the MC-process. The stress voltages are $V_{\mathrm{ds}} = 20\,\mathrm{V}$ and $V_{\mathrm{gs}} = 2\,\mathrm{V}$ applied for stress times 10 s and 1 Ms. The case where all the superposition of SC- and MC-processes are considered in the DD-based model are also plotted for comparison (grey lines).

experimental data in Figure 5.20. As can be seen, the simulated curves agree well with the experiments.

## 5.7 Role of Cold Carriers in HCD

In order to study if the effect of cold carriers can be neglected at such high voltages as $V_{\mathrm{ds}} \geq 16\,\mathrm{V}$ the $N_{\mathrm{it}}(x)$ profiles were calculated for the nLDMOS device without the contribution of the MC-mechanism, see Figure 5.21. One can see that the channel $N_{\mathrm{it}}$ peak disappears if the MC-process is ignored. This behavior can be easily explained because carriers near the source are close to equilibrium, and therefore the carriers near the channel have moderate energies which are not enough to trigger the SC-mechanisms.

The important issue which needs to be addressed in more detail is whether the effect of cold carriers can be neglected in nLDMOS devices stressed at high voltages. This effect is twofold: the population of cold carriers is described by the second term of the energy distribution function (see Equation 4.22 ) and these low-energetic particles contribute to HCD via the MC-mechanism. To analyze the role of the first aspect, the drain DFs obtained with ViennaSHE and with the DD-based model excluding the term for cold carriers in the DF expression Equation 4.22 were calculated for two different drain voltages of 20 and 22 V, see Figure 5.22. One can see that at moderate and high energies the agreement is very good while for low energies the Maxwellian tails visible in SHE-based DFs are not reproduced by the DD-based method.

To check if this omission in the DFs at low energies translates into changes in the linear and saturation drain current degradation, $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ curves calculated

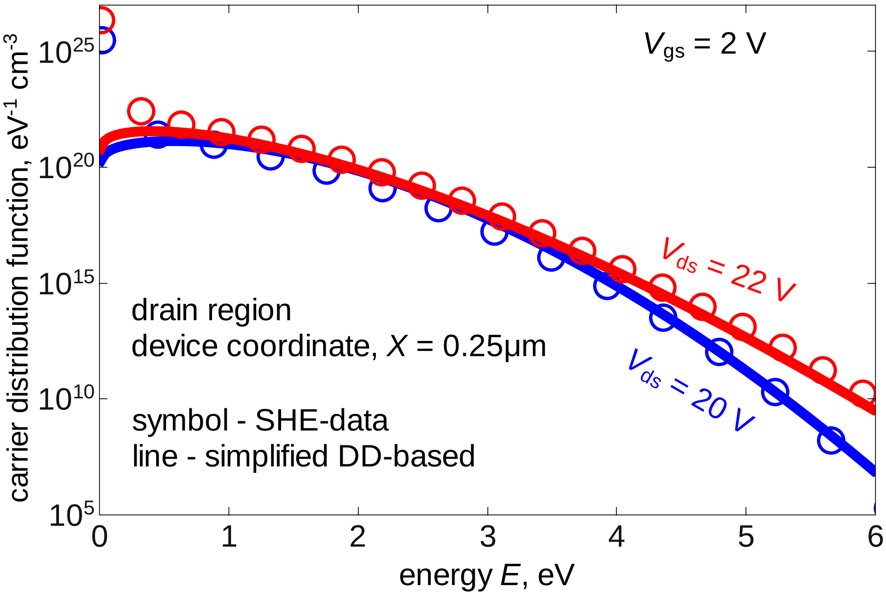

Figure 5.22: DFs for the nLDMOS transistor from ViennaSHE and the DD-based approach without the term for cold carriers in Equation 4.22, for stress voltages: $V_{\mathrm{gs}} = 2\,\mathrm{V}$, $V_{\mathrm{ds}} = 20\,\mathrm{V}$ and $22\,\mathrm{V}$.

without the effect of cold carriers for $V_{\mathrm{gs}} = 2\,\mathrm{V}$ and $V_{\mathrm{ds}} = 18$ and $22\,\mathrm{V}$ are plotted, see Figures 5.23 and 5.24. These degradation curves are evaluated using the same parameter set as those obtained with the "full" model. One can see that at short stress times neglecting the cold carrier contribution does not affect HCD, while at times longer than $\sim 5\,\mathrm{ks}$ the drain current change is substantially underestimated. This is because short term HCD is determined by the drain $N_{\mathrm{it}}$ peak which is visible already at $10\,\mathrm{s}$, see Figure 5.21. In this device area carriers are rather hot, and therefore both SC- and MC-mechanisms are coupled and have high rates. Thus, ignoring the contribution of cold carriers does not change the $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ traces.

With increasing stress time the drain $N_{\mathrm{it}}$ peak becomes broader, i.e. HCD propagates into the device. However, at these times a substantial contribution is made to the degradation by the growing $N_{\mathrm{it}}$ peaks inside the channel and the bird's beak, see Figure 5.21. The peak in the channel is determined by the MC-process (in combination with the bond breakage energy reduction due to the field-dipole interaction). Suppressing either the cold carrier fraction effect or the MC-process contribution leads to an underestimation of HCD at moderate and long stress times. This leads to the conclusion that even in the case of high-voltage devices the cold carrier contribution cannot be omitted.

The cold carriers in the drain region, having a very high occupation probability, cannot be represented if the second term corresponding to the cold carriers in Equation 4.22 is omitted, see Figure 5.22. Note that the DF in Figure 5.22 was evaluated by just setting the cold carrier coefficient $C$ to zero without further renormalization (i.e. the area under the DF curve no longer represents the local carrier concentration). This can severely affect the predictive capability of the HCD model.

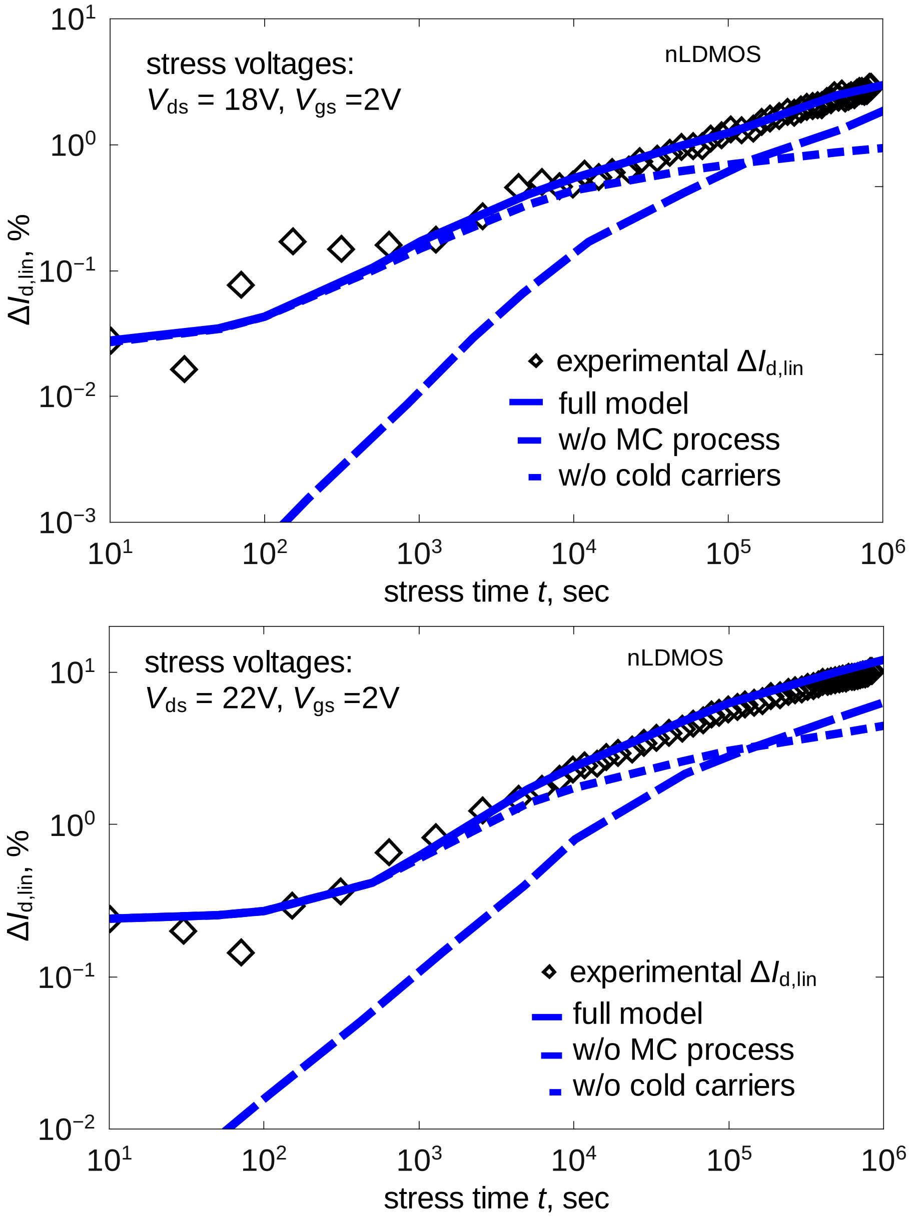

Figure 5.23: The change of the linear drain current $\Delta I_{\mathrm{d,lin}}(t)$ in an nLDMOS as a function of stress time: experimental data, the results of the full model, and the traces obtained neglecting the cold carrier term in Equation 4.22 and without the MC-process. The stress voltages were $V_{\mathrm{gs}} = 2\,\mathrm{V}$ and $V_{\mathrm{ds}} = 18$ and $20\,\mathrm{V}$.

Figures 5.23 and 5.24 show $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ obtained from the HCD model considering both SC- and MC-processes but ignoring the second term in Equation 4.22 corresponding to the cold carriers for two stress conditions, i.e. $V_{\mathrm{gs}} = 2.0\,\mathrm{V}$ and $V_{\mathrm{ds}} = 18$ and $22\,\mathrm{V}$. Interestingly, the drain current degradation is not dramatically affected at short stress times by the second term, but at high stress times, where other processes have nearly saturated, the consideration of cold carriers in the drain region results in a significant difference of $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$. Figures 5.23 and 5.24 also show the importance of the MC-process in the HCD model.

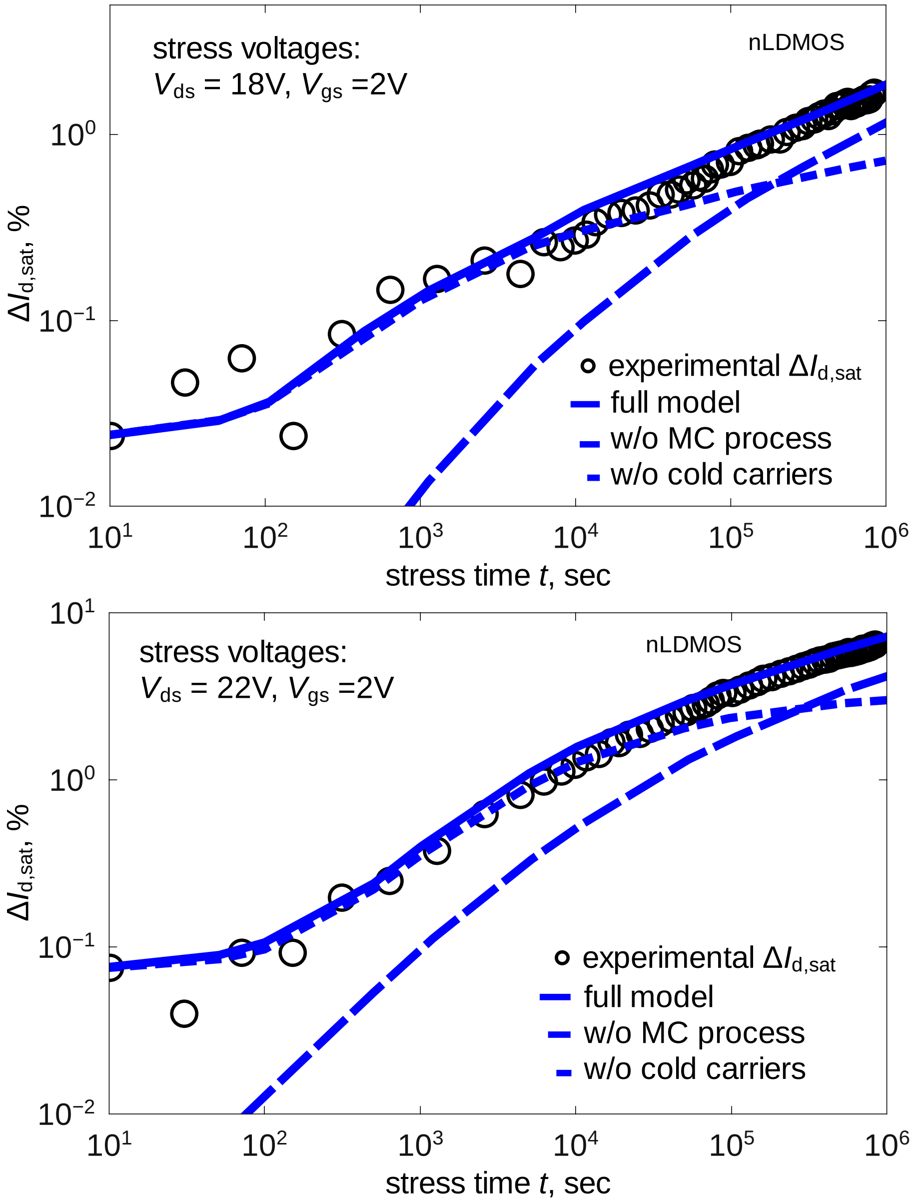

Figure 5.24: The same as in Figure 5.23 but for the saturation drain current.

The rate of the MC-process, as already discussed, is determined by Equation 4.29, where the threshold energy $\varepsilon_{\text{th}}$ is the distance between the Si-H bond vibrational levels and is ~0.25 eV [139, 140]. As for the SC-process, which has an activation energy of ~2.5 eV, the corresponding rate is not significantly affected if the DFs with the omitted cold carrier term are used, as opposed to the rate of the MC-mechanism.

As can be seen in Figure 5.23 , the HCD model considering just the SC-process fails to describe $\Delta I_{\text{d,lin}}(t)$. In the nLDMOS transistor short-term HCD is determined by the drain $N_{\text{it}}$ peak. Near the drain, the carriers are rather hot, and therefore one may expect that if the effect of cold particles is neglected, the corresponding $N_{\text{it}}$ peak and changes of the device characteristics at short stress times will not be affected. Figure 5.23 shows, however, that this is only partially true and neglecting the MC-mechanism leads to severe

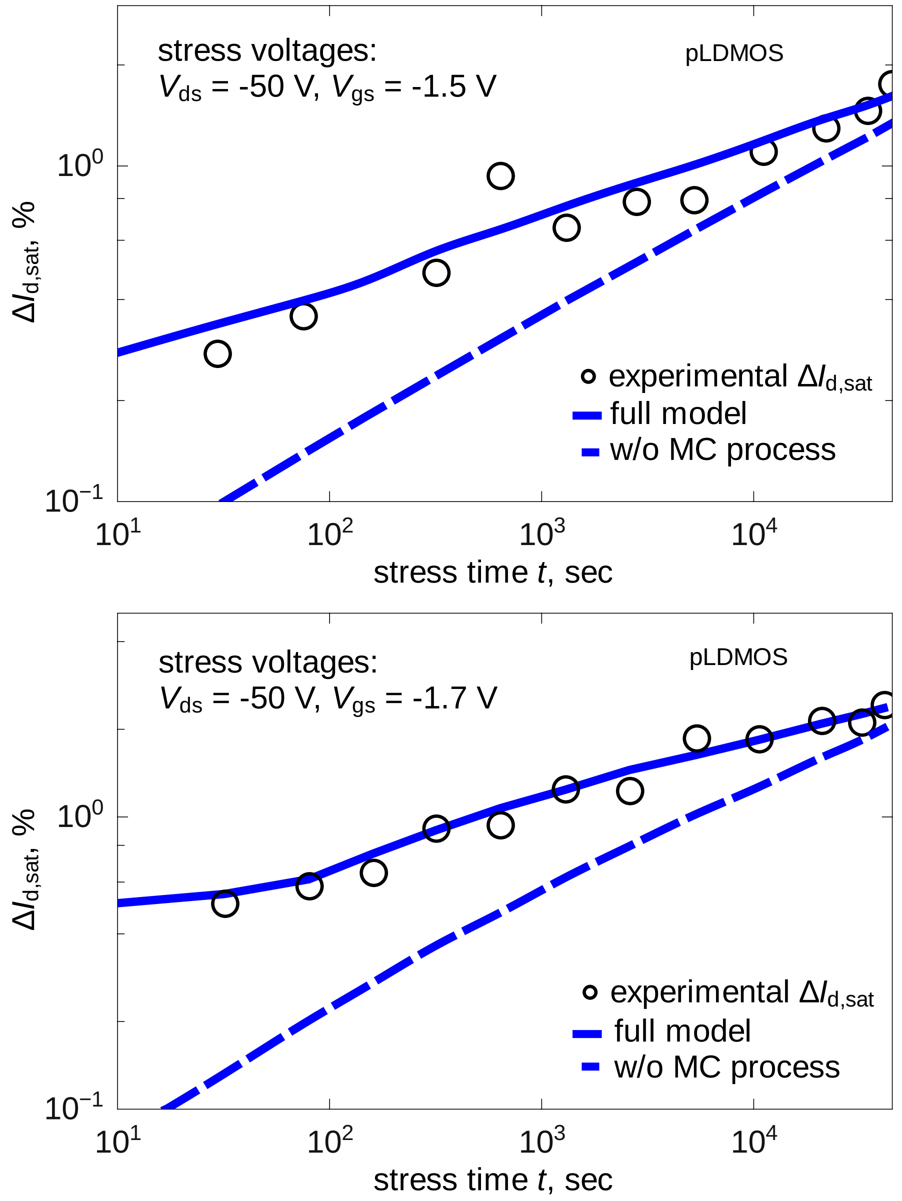

Figure 5.25: The change of the saturation drain current $\Delta I_{\mathrm{d,sat}}(t)$ in the pLDMOS as a function of stress time: experimental data, the results of the full model, and the traces obtained neglecting the MC-process. The stress voltages were $V_{\mathrm{ds}}$ = -50 V and $V_{\mathrm{gs}}$ = -1.5 and -1.7 V.

underestimation of both $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ at short stress times and for both combinations of $V_{\mathrm{ds}}$ and $V_{\mathrm{gs}}$. This originates from the fact that hot carriers contribute also to the MC bond breakage process. Let us consider an electron which has gained an energy of 1.4 eV. This electron cannot trigger the SC-process which has an activation energy of 1.5 eV [139, 140] but it can excite the bond to a higher energy level. Now the remaining bond breakage energy needed to desorb the hydrogen atom is ∼0.1 eV and the probability of finding carriers with this energy or above is very large. Therefore, it is concluded that in the drain area the MC- and SC-processes are strongly coupled and neglecting the former mechanism leads to spurious $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ results.

As for the role of the low energy fraction of the carrier ensemble in the context of the drain $N_{\mathrm{it}}$ peak, the contribution of these particles is screened by those electrons which have higher energies. Therefore, if the cold carrier term in the DF expression is omitted, the drain $N_{\mathrm{it}}$ peak is not impacted and the error in the $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ values is visible at stress times of ∼3 ks and longer. An additional factor which is also responsible for this HCD underestimation is due to the fact that the cold carriers (together with the field-dipole lowering of the activation energy) are responsible for the channel $N_{\mathrm{it}}$ peak which contributes to HCD also in the case of long stresses [26, 147].

Finally, $\Delta I_{\mathrm{d,sat}}(t)$ is shown neglecting the MC-process in the HCD model in Figure 5.25 for the pLDMOS transistor. Again, an underestimation of degradation is observed if the MC-process is not included. Since at such high stress voltages as $V_{\mathrm{ds}}$ = -50 V the concentration of hot carriers is higher than compared to the nLDMOS device, the underestimation is not as severe. As the stress time increases, the discrepancy reduces due to the increase in the number of hot carriers and the SC-process dominates at longer stress times. Neglecting the cold carrier term in Equation 4.22 does not affect the DF and the HCD in the pLDMOS as the cold carrier concentration is not very high in this device at stress voltages of $V_{\mathrm{ds}}$ = -50 V and $V_{\mathrm{gs}}$ = -1.5 and -1.7 V.

To conclude, in this section the physical model of HCD is applied to represent the degradation in nLDMOS and pLDMOS transistors. Two versions of the model have been examined, i.e. a version which employs the carrier distribution functions obtained from a deterministic Boltzmann transport equation solver and one which uses the simpler drift-diffusion approach. The electron DFs determined with the DD-based model were compared with those simulated with the SHE approach and good agreement between them was shown. Although some discrepancy between the DFs computed with these two models is visible in the drain region, this discrepancy was shown to not translate into a significant error in the degradation traces. Such a conclusion can be drawn based on the good agreement between the carrier acceleration integrals evaluated with the two versions of the model for both single- and multiple-carrier processes of Si-H bond dissociation. The corresponding interface state density profiles are also almost identical for a wide range of stress times and stress conditions. The degradation of the linear and saturation drain currents as well as the threshold voltage shift were properly represented by both versions of the model for different combinations of drain and gate voltages using a unique set of parameters. Good agreement between the results obtained with the SHE- and DD-based methods suggests that the computationally efficient drift-diffusion model is well suited for describing the hot-carrier degradation in LDMOS devices. This makes the DD-based model attractive for predictive HCD simulations of LDMOS transistors.

Using the physics-based model for hot-carrier degradation (Section 4.3 and 4.4), the role of colder carriers in HCD of n- and p-channel LDMOS transistors is also investigated. The effect of cold carriers on HCD is twofold: these carriers contribute to the low energy fraction of the carrier energy distribution function and also trigger the multiple-particle process of Si-H bond dissociation. As a result, the drift-diffusion scheme is more feasible for analysis of the role of cold carriers in HCD since the analytic formula for the distribution function contains two terms, i.e. the one which represents the hot carrier fraction of the statistical ensemble and the second one which models the thermalized cold carriers. If the multiple-carrier process rate is neglected, $\Delta I_{\mathrm{d,lin}}(t)$ and $\Delta I_{\mathrm{d,sat}}(t)$ are severely underestimated in both LDMOS transistors. Note that this trend is especially pronounced at short stress times. It has been shown that short-term HCD is determined by the drain $N_{\mathrm{it}}$ [26, 147]. In the drain the carriers are hot enough and have a high concentration. As a result, both single- and multiple-carrier processes of bond dissociation are strongly coupled. For instance, those carriers with energies slightly below the Si-H bond breakage activation energy can excite the bond, therefore contributing to the multiple-carrier process. If the bond is excited by this process, a substantially lower energy is needed to trigger the bond rupture event. Therefore, ignoring the MC-process rate can also impact the rate of the SC-mechanism. In addition, the common effect of cold carriers with the bond weakening due to the field-dipole interaction leads to a channel $N_{\mathrm{it}}$ peak which also contributes to HCD at longer stress times. Finally, it is important to emphasize that all trends are the same for both n- and p-channel devices and that for both transistors a unique set of model parameters has been used.

# Chapter 6

# Comparison of Drift-Diffusion Based Models

As already discussed in Section 4, several different approaches exist which can be employed to obtain the carrier DF in a simple manner. In this chapter, the different analytic models proposed for the carrier distribution function, namely the heated Maxwellian, the Cassi model, the Hasnat approach, the Reggiani model, and the model used in this work (Section 4.3), are compared. The applicability of these models for describing hot-carrier degradation in nLDMOS devices is verified. For reference, the carrier distribution functions are evaluated from the direct solution of the Boltzmann transport equation using the spherical harmonics expansion method. The simulation framework is the same as in Section 5.2 comprising of ViennaSHE for SHE simulations, ViennaMesh for generating the meshes, Sentaurus Process simulator for process simulations, and MINIMOS-NT for device simulations. The DFs obtained from the different models are used in the HCD model (Section 4.4) to simulate the interface state generation rates, the interface state density profiles, and changes of the linear and saturation drain currents as well as the threshold voltage shifts. These degradation curves are compared with experimental data and a conclusion on the validity of each model is drawn. Since all models use the same parameter set, the differences in the results can be directly traced back to inaccuracies in the approximation of the DF.

## 6.1 The Maxwellian Model

*The heated Maxwellian* distribution is a frequently used approach to mimic the DFs of non-equilibrium carriers [28]:

$$f(\varepsilon) = A\exp(-\varepsilon/k_{\mathrm{B}}T_n). \tag{6.1}$$

An example of the DFs obtained using the Maxwellian function for different regions of the nLDMOS device (described in Section 5.1) is shown in Figure 6.1. One can see that the DFs evaluated with the heated Maxwellian approach are close to equilibrium in the channel and drain regions of the device, while in the bird's beak region, the carriers are rather hot and the corresponding DFs are severely non-equilibrium.

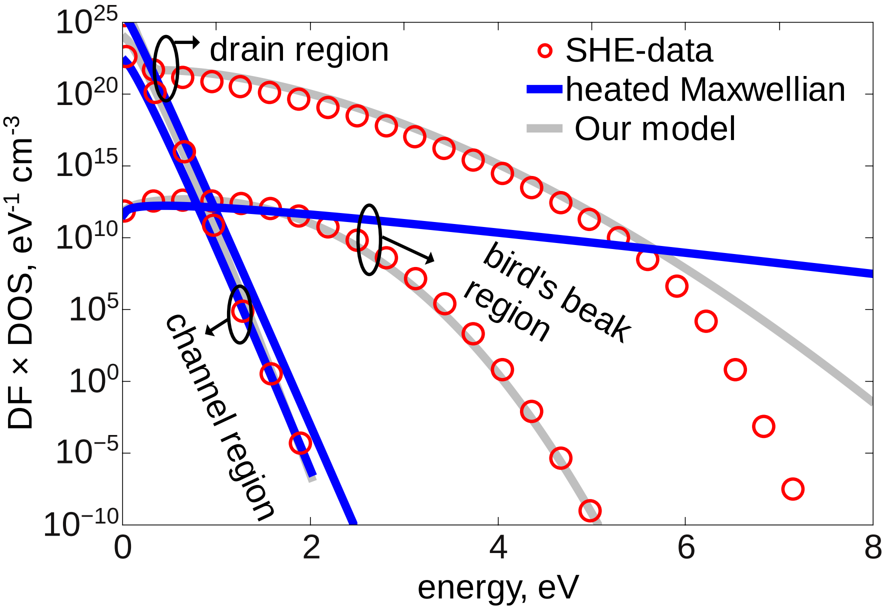

Figure 6.1: The electron DFs (coupled with the density of states to show the carrier occupancy) in nLDMOS obtained with the heated Maxwellian approach compared with those simulated with ViennaSHE for $V_{\mathrm{gs}} = 2\,\mathrm{V}$ and for $V_{\mathrm{ds}} = 18\,\mathrm{V}$ calculated at the drain, bird's beak and channel regions. For comparison, the DFs evaluated with the DD-based model in Section 4.3 (light grey lines) are also plotted.

## 6.2 Cassi Model

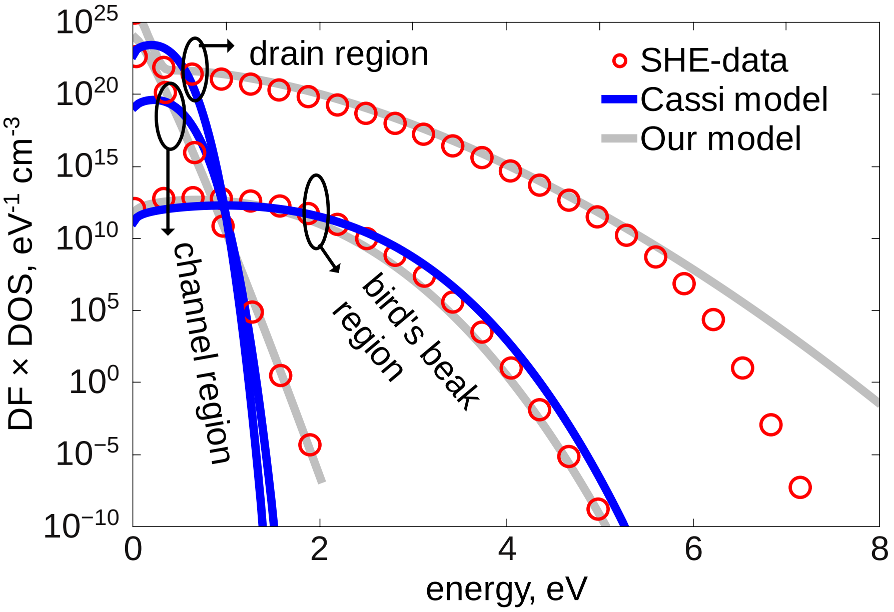

Figure 6.2: Same as Figure 6.1 but for the Cassi model.

*Cassi and Riccó* proposed an expression to account for the non-Maxwellian shape of the DFs observed in MOSFETs, especially in the drift and the drain regions. Their model for the DF is given by [33]:

$$f(\varepsilon) = A\exp\left(-\chi\varepsilon^3/E^{1.5}\right), \tag{6.2}$$

where $\varepsilon$ is the carrier energy, $\chi = 0.1$ a fitting parameter and $E$ the local electric field. The Cassi model results in DFs which are substantially non-equilibrium in the bird's beak region, as shown in Figure 6.2. Due to the fixed curvature, the shape of the DF is similar in the channel and in the drain region. Hence, the carrier energies obtained from the Cassi model for these device sections are significantly lower compared to the bird's beak region.

## 6.3 Hasnat Model

*Hasnat et al.* replaced the local electric field in Cassi's expression by a function of carrier temperature to capture the non-local behavior [34]:

$$f(\varepsilon) = A\exp\left(-\epsilon^{\xi}/(\eta(k_{\mathrm{B}}T_n)^{\nu})\right), \tag{6.3}$$

where $\xi$, $\eta$, and $\nu$ are fitting parameters. Figure 6.3 shows the DFs obtained using Equation 6.3 for different regions of the device. The DFs in the channel and the drain sections are similar to the Maxwellian, see Figure 6.1, while for the bird's beak region, the carrier energies calculated with the Hasnat model extend up to 5.5 eV and beyond.

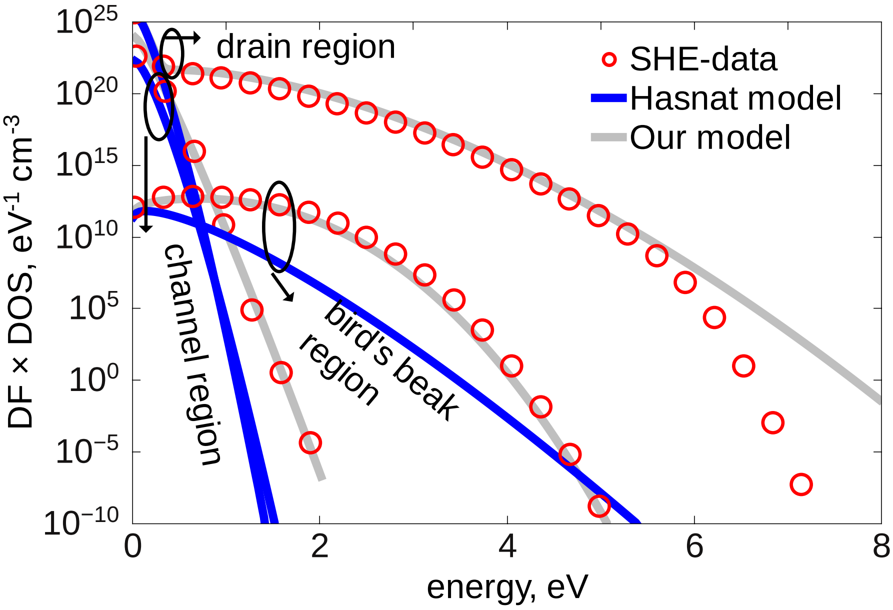

Figure 6.3: Same as Figure 6.1 but for the Hasnat model.

## 6.4 Reggiani Model

*Reggiani et al.* have recently developed an analytical model for the DFs which is focused on modeling of HCD in LDMOS devices [35, 36]. The DF is expressed as:

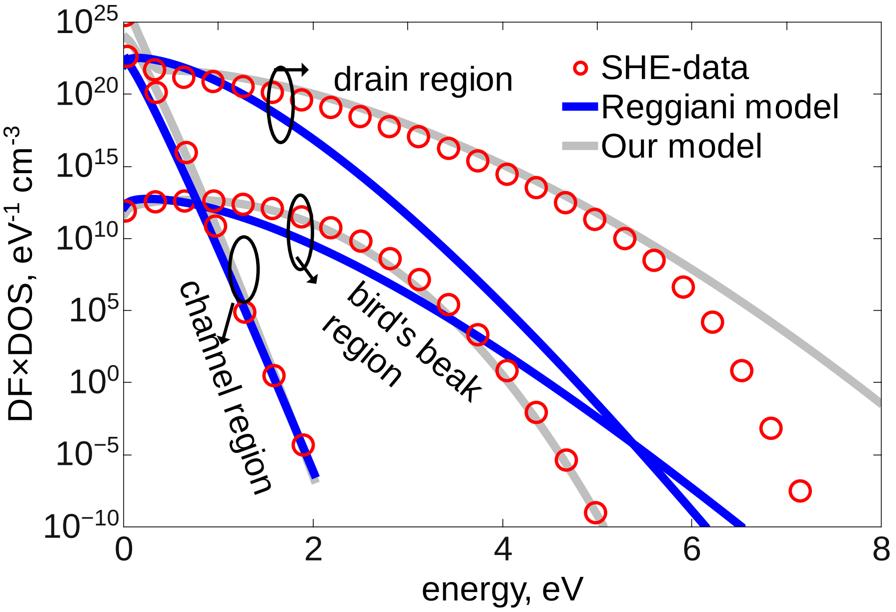

Figure 6.4: Same as Figure 6.1 but for the Reggiani model.

$$f(\varepsilon) = A \exp\left[-\alpha\varepsilon(1+\delta\varepsilon)/(k_{\mathrm{B}}T_n(1+\beta\varepsilon))\right]. \tag{6.4}$$

Here $\delta$ and $\beta$ are fitting parameters, while $A$ and $\alpha$ are evaluated using the carrier concentration $n$ and carrier temperature $T_n$ computed using the DD scheme. In long channel devices the moment $n$ can be obtained directly from DD simulations while $T_n$ is evaluated using the local energy balance equation [177]. The Reggiani model produces non-equilibrium DFs for the bird's beak and drain regions as shown in Figure 6.4. As for the channel region, the corresponding DFs are close to the equilibrium ones.

The DFs obtained by the approach proposed in this work, Section 4.3, are shown in the Figures 6.1, 6.2, 6.3, and 6.4 as gray curves. One can see that this DD-based scheme for the carrier distribution function can adequately represent the DFs.

## 6.5 Results and Discussion

To check the validity of the different HCD models, the bond breakage rates, the interface state density profiles, and the change of the linear and saturation drain currents as well as the threshold voltage shifts are calculated. The data obtained from the different versions of the model are compared against the HCD results measured in nLDMOS transistors.

### 6.5.1 Distribution Functions and Interface State Densities

*The heated Maxwellian* DFs are plotted along with the DFs calculated with ViennaSHE in Figure 6.1. As expected, the Maxwellian model is only valid in the initial part of the channel region where the carriers are almost in equilibrium. It overestimates the DFs at high energies near the bird's beak and fails completely in the drain region of the nLDMOS device. The heated Maxwellian distribution leads to reasonable $N_{\mathrm{it}}(x)$ profiles only in the

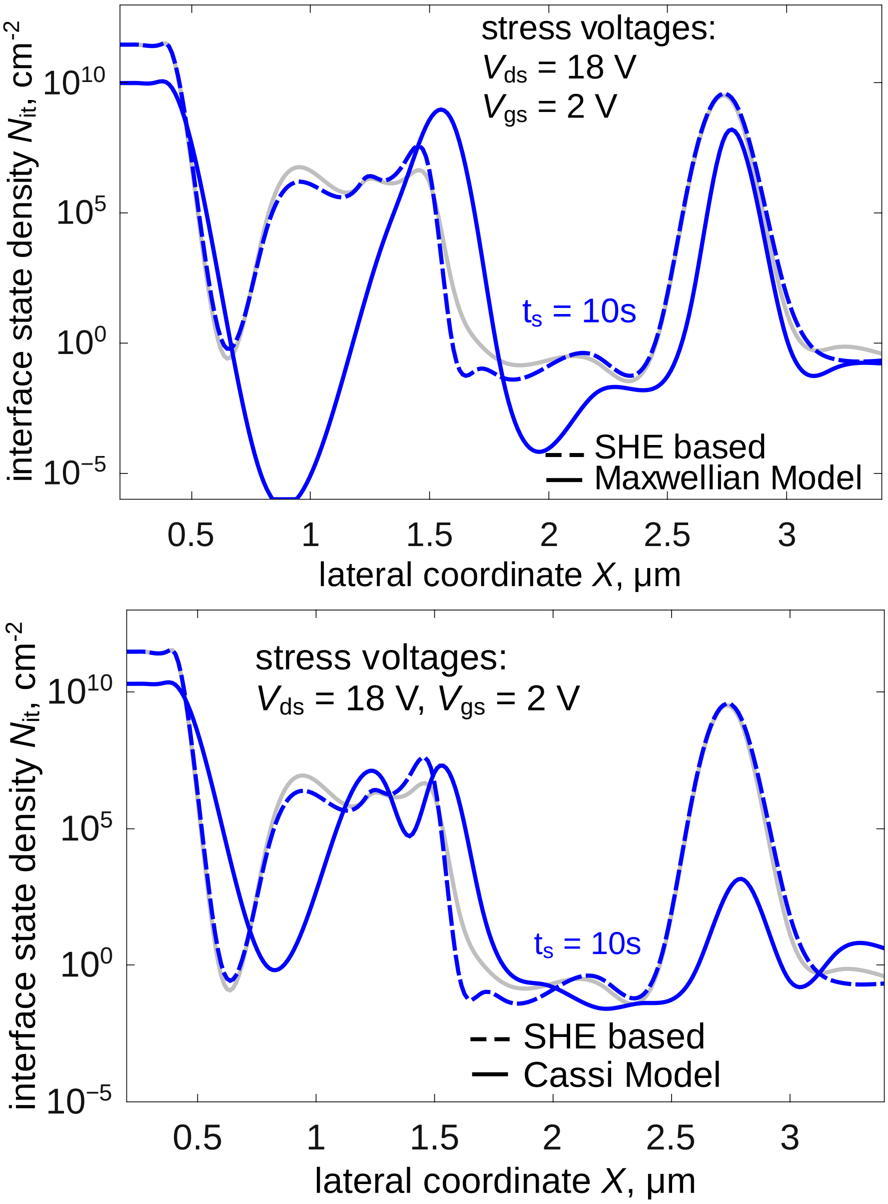

Figure 6.5: The $N_{\text{it}}$ profiles in nLDMOS transistor obtained using the heated Maxwellian (top - blue line) and the Cassi model (bottom - blue line) for $V_{\text{gs}} = 2\,\text{V}$ and for $V_{\text{ds}} = 18\,\text{V}$ and stress time of 10 s. For comparison of the $N_{\text{it}}$ profile from ViennaSHE (blue dashed line) and the DD-based approach used in this work (grey line) are also plotted.

channel and source regions when compared with the $N_{\text{it}}(x)$ profiles computed using the DF from ViennaSHE, see Figure 6.5. This approach overestimates the $N_{\text{it}}$ values in the bird's beak region and also fails in the drain region.

The *Cassi model* shows an improvement for the non-equilibrium case but cannot describe the DFs near the drain. This is because the DFs evaluated with this approach have a fixed curvature. Figure 6.5 summarizes the $N_{\text{it}}(x)$ profiles obtained using the DFs from the Cassi model and from ViennaSHE. These $N_{\text{it}}(x)$ profiles from the two approaches are only comparable in the bird's beak region. Such a behavior is also consistent with the difference

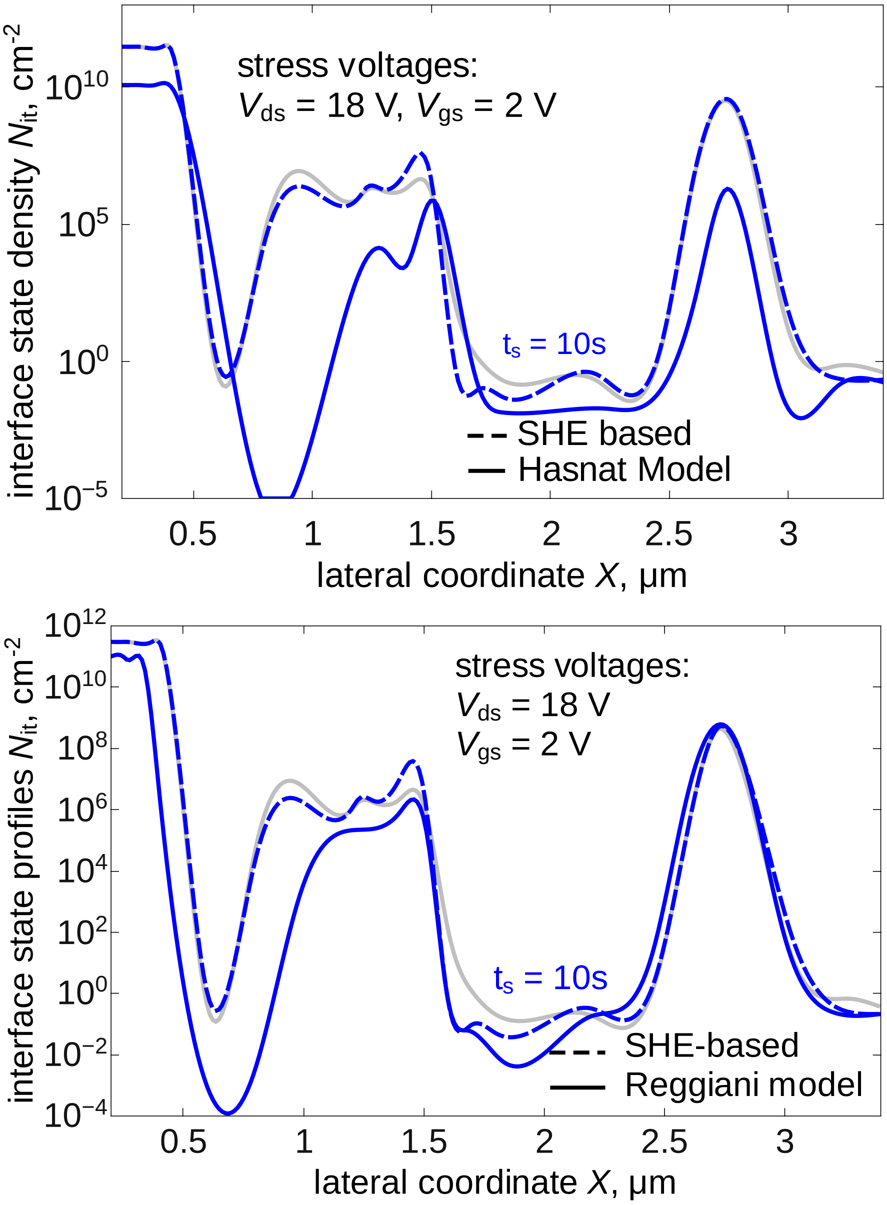

Figure 6.6: Same as Figure 6.5 but for the Hasnat model (top) and the Reggiani model (bottom).

in the DFs computed with this model and that from the BTE solution.

The *Hasnat method* cannot represent the DFs in neither the bird's beak nor the drain region, as shown in Figure 6.3. The corresponding interface trap density is plotted in Figure 6.6, which does not match those calculated with ViennaSHE in the entire $X$ coordinate range. The $N_{\text{it}}$ values are severely underestimated inside the channel and close to the drain region.

The *Reggiani approach* appears promising because it can describe the DFs in LDMOS

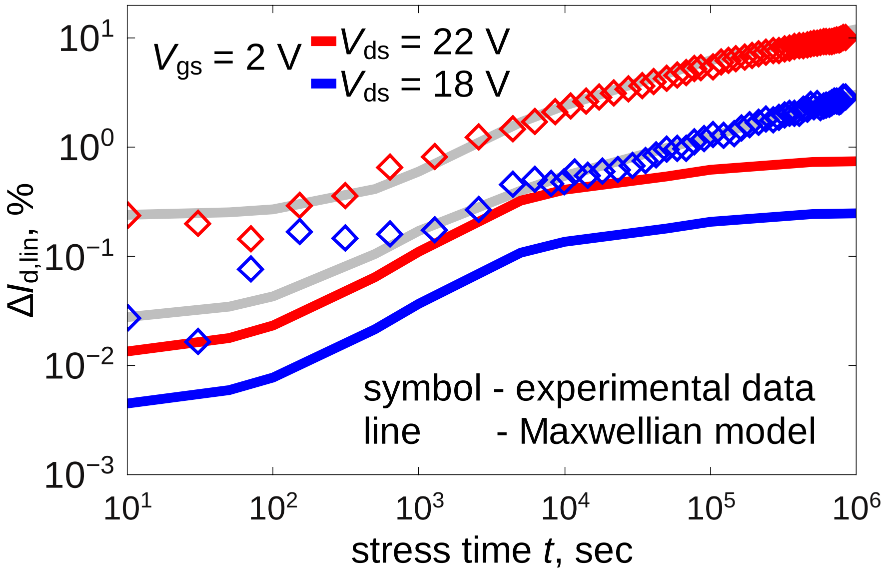

Figure 6.7: Simulated $\Delta I_{\mathrm{d,lin}}(t)$ traces obtained using the heated Maxwellian distribution plotted against experimental data for nLDMOS. Stress voltages are $V_{\mathrm{gs}} = 2\,\mathrm{V}$ and for $V_{\mathrm{ds}} = 18\,\mathrm{V}$ and $22\,\mathrm{V}$. As a reference, the degradation traces calculated with the DD-based version of the model are plotted (grey curves).

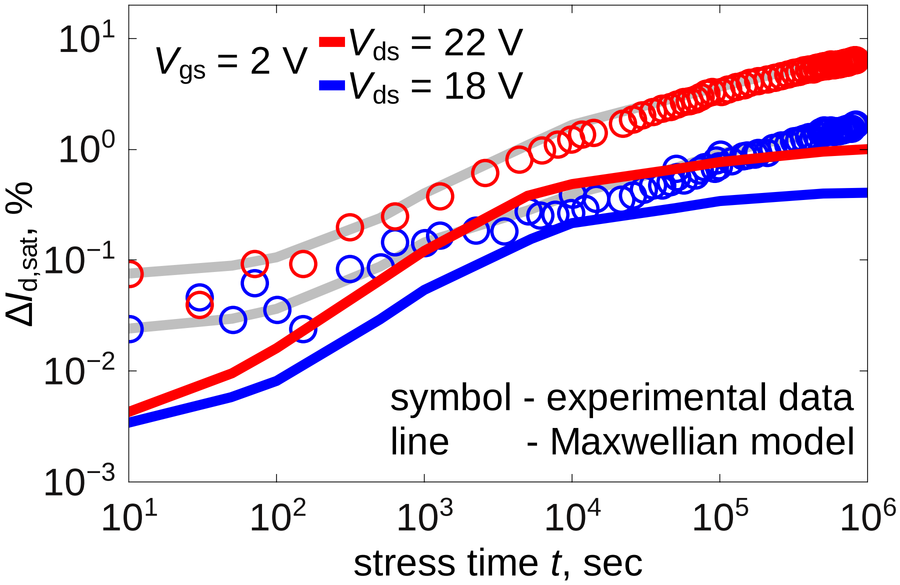

Figure 6.8: Simulated $\Delta I_{\mathrm{d,sat}}(t)$ traces obtained using the heated Maxwellian distribution plotted against experimental data for nLDMOS. Stress voltages are $V_{\mathrm{gs}} = 2\,\mathrm{V}$ and for $V_{\mathrm{ds}} = 18\,\mathrm{V}$ and $22\,\mathrm{V}$. As a reference, the degradation traces calculated with the DD-based version of the model are plotted (grey curves).

devices with good accuracy except for the drain region. The reason is that within the Reggiani model the DFs are linked to the local electric field, and thus hot carriers which form the high-energy tail of the DF are not properly described. From Figure 6.4 one can

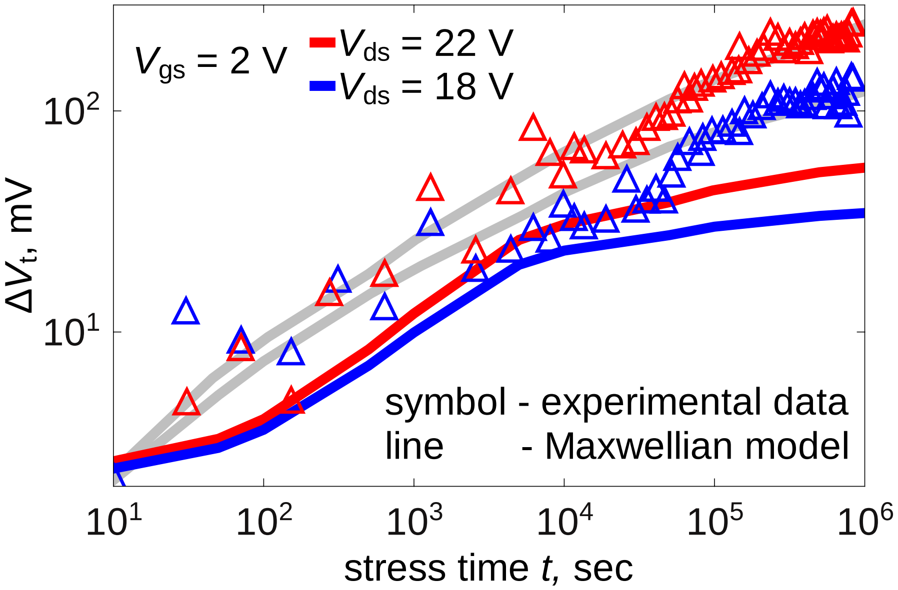

Figure 6.9: $\Delta V_\mathrm{t}$ traces simulated using the heated Maxwellian distribution vs experimental data for nLDMOS. Stress voltages are $V_\mathrm{gs} = 2\,\mathrm{V}$ and for $V_\mathrm{ds} = 18\,\mathrm{V}$ and $22\,\mathrm{V}$. As a reference, the degradation traces calculated with the DD-based version of the model are plotted (grey curves).

see that these tails are underpopulated if the Reggiani approach is used. As a result, this discrepancy translates also into an error in $N_\mathrm{it}$ which is underestimated in the drain, as is evident from Figure 6.6.

The DFs computed with the model developed in this work (Section 4.3) are also shown

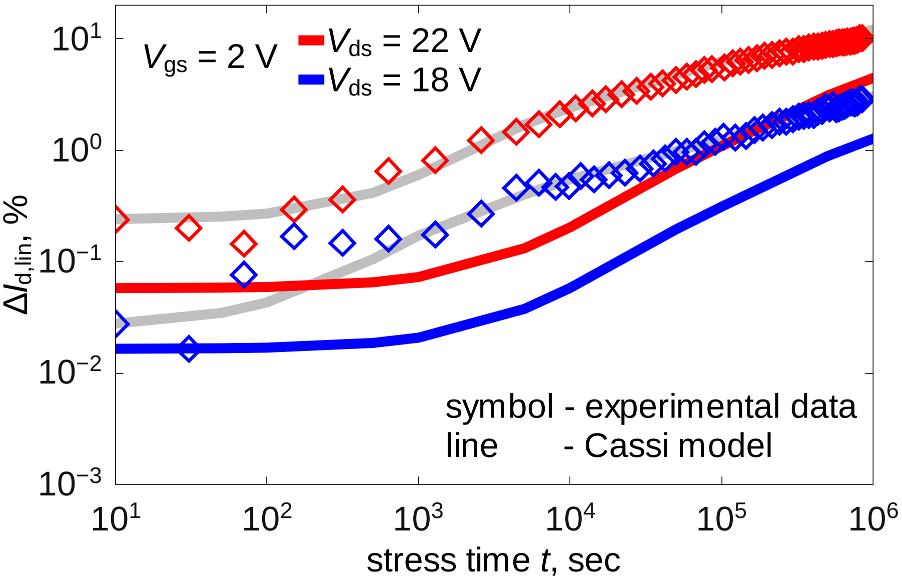

Figure 6.10: Same as Figure 6.7 but for the Cassi model.

in Figures 6.1, 6.2, 6.3, and 6.4 as light gray curves. The model was successful in representing the carrier distributions along the entire device.

### 6.5.2 Degradation Traces

The changes in $\Delta I_{\mathrm{d,lin}}(t)$, $\Delta I_{\mathrm{d,sat}}(t)$, and $\Delta V_{\mathrm{t}}(t)$ calculated with the different model versions are summarized and compared to the experimental data in Figures 6.7 – 6.18.

The *heated Maxwellian approach* leads to a saturation of $\Delta I_{\mathrm{d,lin}}(t)$, $\Delta I_{\mathrm{d,sat}}(t)$, and $\Delta V_{\mathrm{t}}(t)$

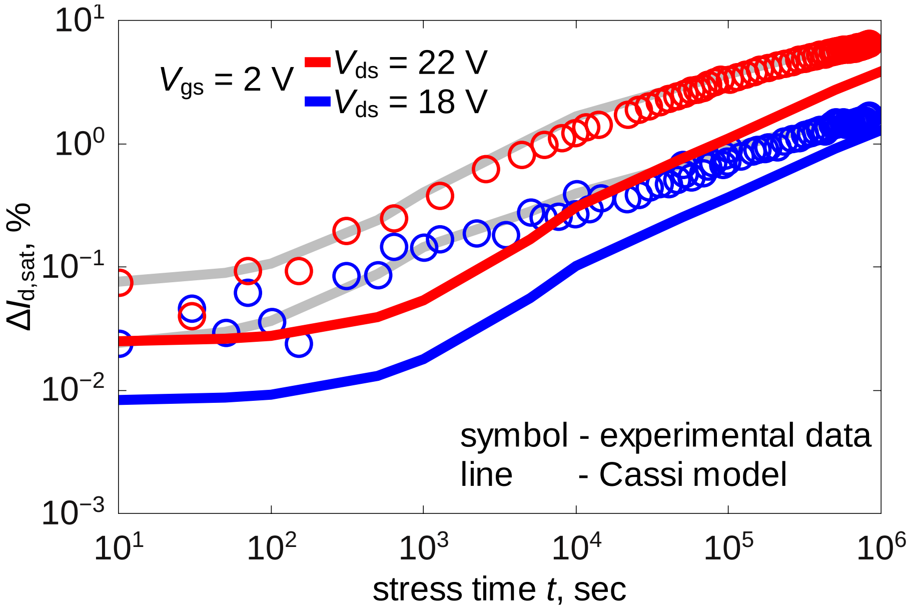

Figure 6.11: Same as Figure 6.8 but for the Cassi model.

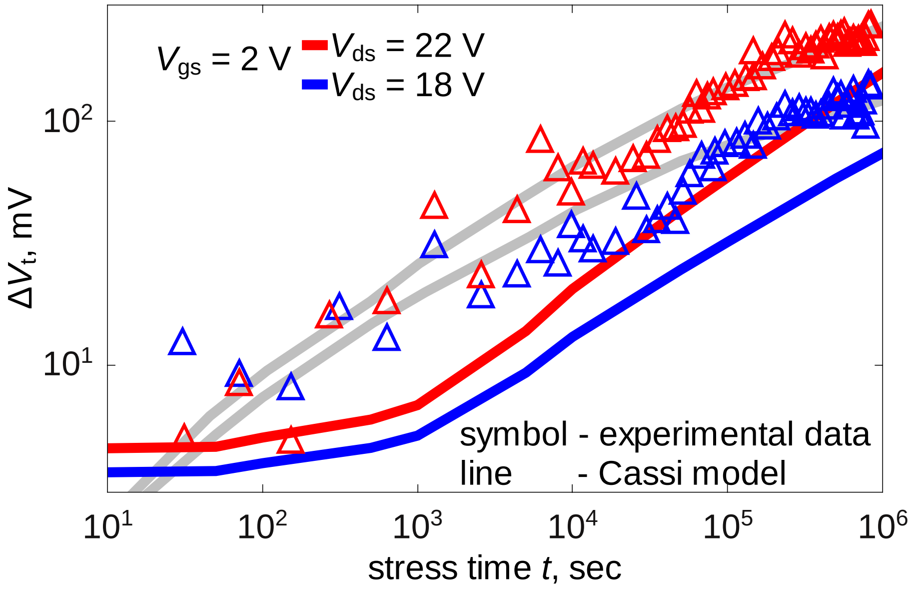

Figure 6.12: Same as Figure 6.9 but for the Cassi model.

at ∼500 s, see Figures 6.7 − 6.9. This is related to the drain $N_{\mathrm{it}}$ peak which is formed by hot carriers and which determines short term hot-carrier degradation [26, 147, 203]. One can see in Figure 6.5 that the interface state density $N_{\mathrm{it}}$ is saturated already at short stress times, and thus at long stress times, HCD is driven by colder carriers which contribute to the multiple-carrier process [26, 147, 203]. As a result, if the effect of cold carriers is underestimated, the change of the device characteristics saturates at longer stress.

Figures 6.2 and 6.5 show that the *Cassi model* highly underestimates the DFs and $N_{\mathrm{it}}$

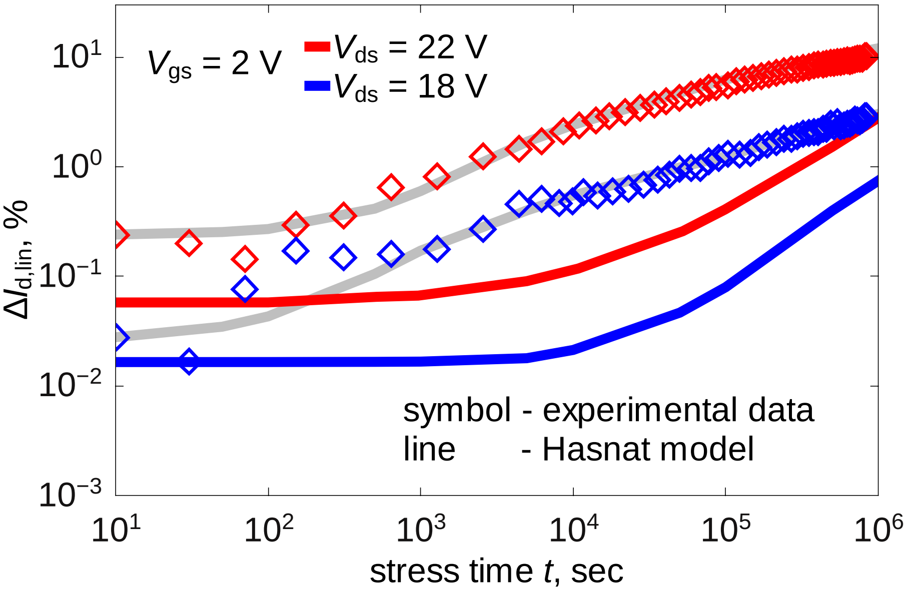

Figure 6.13: Same as Figure 6.7 but for the Hasnat model.

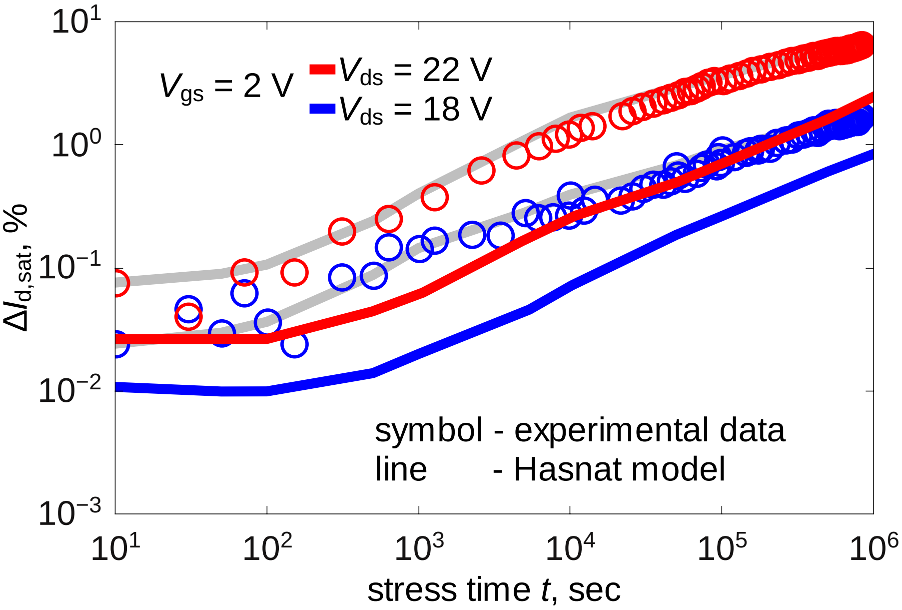

Figure 6.14: Same as Figure 6.8 but for the Hasnat model.

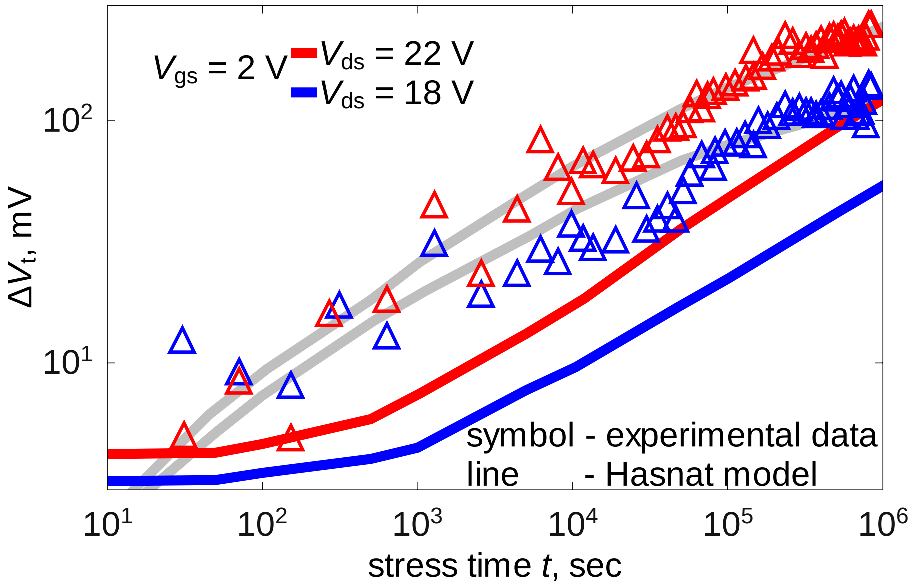

Figure 6.15: Same as Figure 6.9 but for the Hasnat model.

values near the drain region. As a consequence, the degradation of all device characteristics is underestimated as well, especially at short stress times as in Figures 6.10 – 6.12. This is because the most prominent discrepancy between the DFs obtained with ViennaSHE and the Cassi model is visible for the drain region of the device. The same behavior is typical also for the $N_{\mathrm{it}}$ drain maximum, which — as already discussed — determines short-term HCD.

The *Hasnat method* behaves similarly to the Cassi model where the DF values are un-

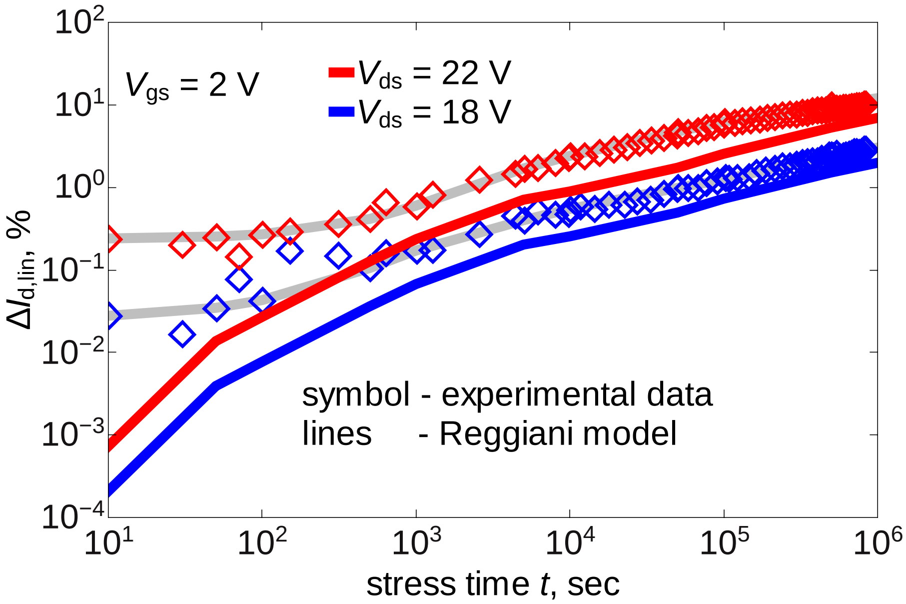

Figure 6.16: Same as Figure 6.7 but for the Reggiani model.

derestimated for most of the device regions, see Figures 6.13 – 6.15. As a result, the degradation of both linear and saturation drain currents as well as the threshold voltage shift are massively underestimated in the entire experimental stress time window.

As for the *Reggiani* model, the model underestimates the interface trap density near the drain. This peculiarity results in weaker curvatures of $\Delta I_{\mathrm{d,lin}}(t)$, $\Delta I_{\mathrm{d,sat}}(t)$, and $\Delta V_{\mathrm{t}}$ traces as shown in Figures 6.16 – 6.18. Although the degradation curves are close to the experimental ones at long stress times, they are unable to predict the correct degradation

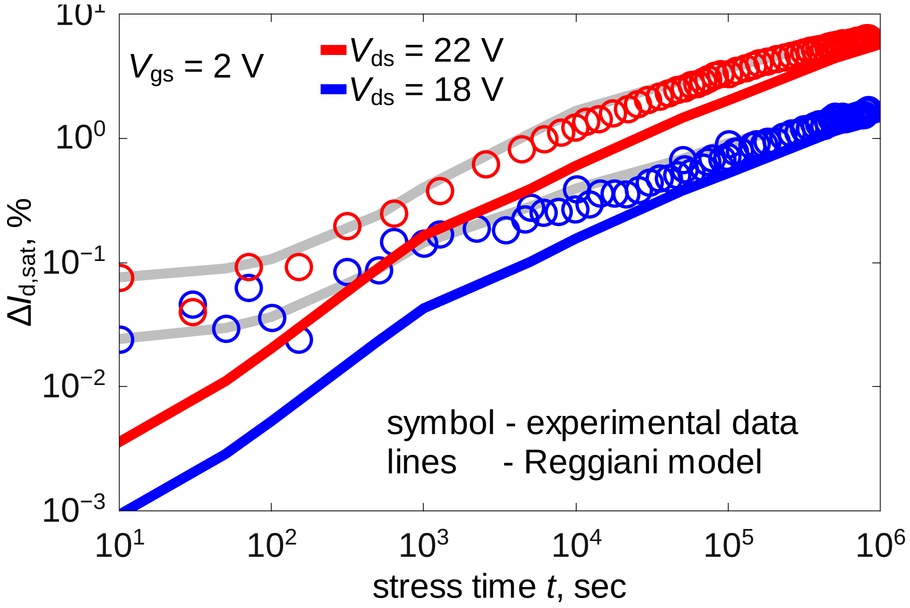

Figure 6.17: Same as Figure 6.8 but for the Reggiani model.

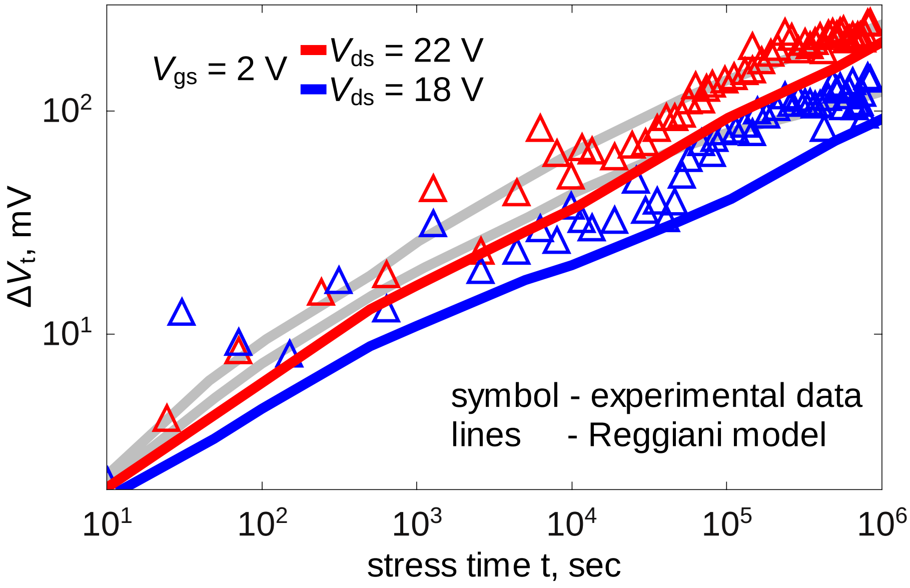

Figure 6.18: Same as Figure 6.9 but for the Reggiani model.

for the entire stress time slot.

Finally, Figures 6.7 – 6.9 show very good agreement between measured $\Delta I_{\mathrm{d,lin}}(t)$, $\Delta I_{\mathrm{d,sat}}(t)$, and $\Delta V_{\mathrm{t}}$ curves and those simulated with the DD-based method developed in this work for the whole stress time window. Both the SHE and DD variants of the HCD model use the same set of parameters for different combinations of stress voltages and for the degradation traces of different device characteristics.

To conclude, in this section a comparison between various HCD models, which employ different approaches to approximate the solution of the Boltzmann transport equation, has been performed using hot-carrier degradation data measured on nLDMOS devices. In several realizations of the HCD model, carrier energy distribution functions obtained with the heated Maxwellian, Cassi, Hasnat, Reggiani and our model are used. These different versions are compared in terms of carrier DFs, interface state density profiles, and degradation of the linear and saturation drain currents, as well as the threshold voltage. The heated Maxwellian neglects the cold carrier fraction of the carrier ensemble and thus the $N_{\mathrm{it}}(x)$ profiles are adequate to some extend only in the channel and source regions. As a result, the degradation traces ($\Delta I_{\mathrm{d,lin}}(t)$, $\Delta I_{\mathrm{d,sat}}(t)$, and $\Delta V_{\mathrm{t}}(t)$) show a spurious saturation at longer stress times. The Cassi and Hasnat models underestimate the values of the carrier DFs in most of the device regions. As for the $N_{\mathrm{it}}(x)$ profiles, the former approach leads to somewhat reasonable $N_{\mathrm{it}}$ values only near the bird's beak, while the interface state densities simulated with the latter approach have substantially lower values (as compared to those evaluated using the full BTE solution) in the entire range of the lateral coordinate. Therefore, the $\Delta I_{\mathrm{d,lin}}(t)$, $\Delta I_{\mathrm{d,sat}}(t)$, and $\Delta V_{\mathrm{t}}(t)$ degradation characteristics computed using the Cassi and Hasnat models are underestimated within the entire stress time slot. The Reggiani model can represent the DFs for most device regions except the drain where the agreement deteriorates. As a result, the curvature of the degradation traces is weaker within the Reggiani model. Finally, the proposed DD-based method can mimic the DFs in the entire device with a slight discrepancy in the drain region for the high energy tails where the magnitude of DF has already dropped by $\sim$20 orders. This discrepancy does not translate to an error in the results evaluated using this approach. This means that the agreement between the $N_{\mathrm{it}}(x)$ profiles and the $\Delta I_{\mathrm{d,lin}}(t)$, $\Delta I_{\mathrm{d,sat}}(t)$, and $\Delta V_{\mathrm{t}}$ degradation curves simulated with the SHE- and DD-based realization of the model is very good. It can, therefore, be concluded that in long-channel LDMOS transistors HCD can be modeled with very good accuracy even with a DD-based formalism provided a good approximative model for the distribution function is used.

# Chapter 7

# On the Limits of Drift-Diffusion Based HCD Modeling

In this chapter, the limits of applicability of the drift-diffusion (DD) based model for hot-carrier degradation (HCD) described in Chapter 4 are studied. In [34] it was suggested that the DD scheme is applicable for describing carrier transport in devices with gate lengths longer than $0.5\mu$m. However, as shown in [29], drift-diffusion and even hydrodynamic approaches can be inadequate for modeling HCD in nMOSFETs with gate lengths of $2.0\mu$m. Thus, in this context, the analysis of the limits of the validity of the DD-based model is a very important task. To investigate the limits of the DD-based HCD model, in this work planar nMOSFETs with identical topology but different gate lengths of 2.0, 1.5 and $1.0\mu$m are used. These devices were generated with the Sentaurus process simulator [198]. The BTE solution produced by the deterministic BTE solver ViennaSHE is employed as reference [204]. While applying the DD- and SHE-based versions of the HCD model to planar nMOSFETs, the typical stress voltages for these transistors have been used which are way lower than compared to the LDMOS devices, i.e. $V_{\mathrm{ds}} = 7.5\,\mathrm{V}$ and $V_{\mathrm{gs}} = 2.5\,\mathrm{V}$, see [141, 171, 205]. For all the devices, the electron DFs, interface state density profiles $N_{\mathrm{it}}(x)$, and degradation traces $\Delta I_{\mathrm{d,lin}}(t)$ as well as $\Delta I_{\mathrm{d,sat}}(t)$ (for up to 50 ks) are simulated.

## 7.1 Model Results for Scaled Devices

Figure 7.1 summarizes the simulated electron energy distribution functions for 2.0, 1.5 and 1.0 µm nMOS devices obtained with ViennaSHE and the DD-based approach at different lateral coordinates along the channel. At low and moderate energies the DFs computed with the analytic approach, Equation 4.22, reasonably mimic the DFs obtained from a BTE solution with ViennaSHE. However, at higher energies, the curvatures of the DFs evaluated with the two approaches are different. It can be seen that the accuracy deteriorates for shorter channel lengths. On the other hand, the occupation numbers at these energies have already dropped by several orders of magnitude, and it is not obvious whether this discrepancy in the DFs translates into a sizable error in the interface state profiles $N_{\mathrm{it}}(x)$ and the $\Delta I_{\mathrm{d,lin/sat}}$ degradation traces.

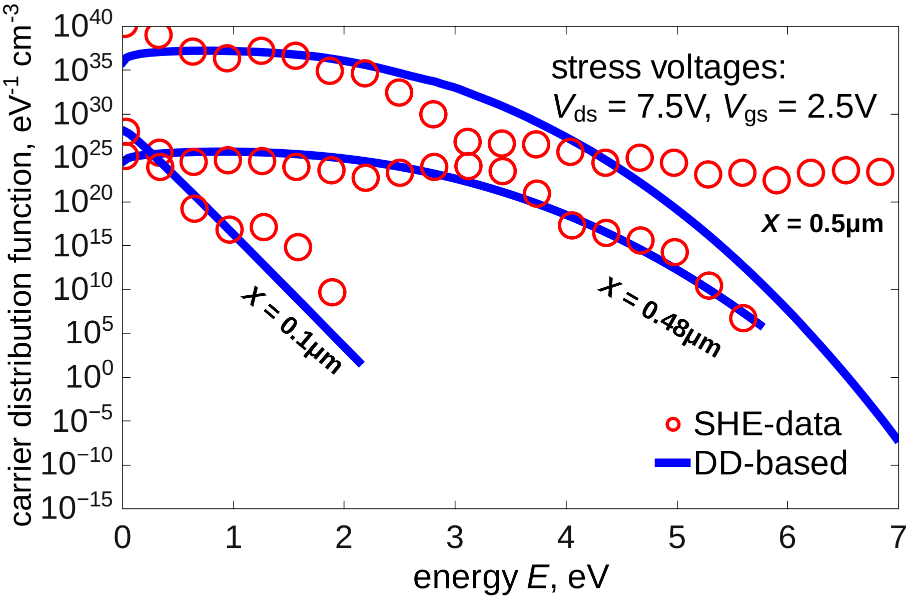

Figure 7.1: The electron distribution functions at different lateral positions along the channel for the nMOSFET with $L_G = 1.0\,\mu$m simulated with ViennaSHE and the DD-based version of the model.

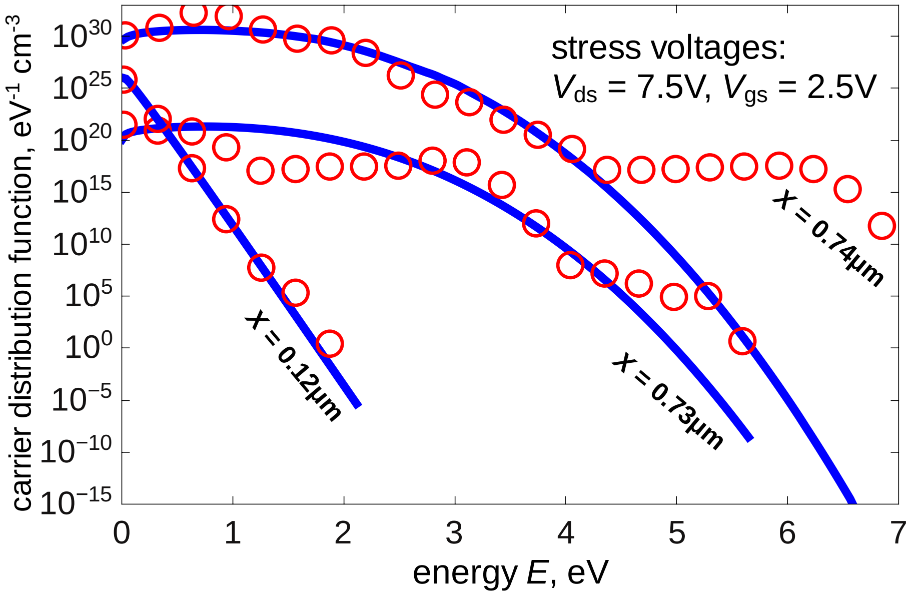

Figure 7.2: Same as Figure 7.1 but with $L_G = 1.5\,\mu$m.

To check the effect of discrepancy in the DFs on the device degradation traces in greater detail the acceleration integrals are plotted, which determine the corresponding rates, for the SC- and the MC-mechanism simulated along the Si/SiO$_2$ interface with both versions of the model, see Figure 7.6. For the $2\mu$m device the bond breakage rates for the SC- and MC-process are almost the same. This reflects the good agreement of the DFs in Figure 7.1. For the shorter structures, the acceleration integrals of both mechanisms calculated with

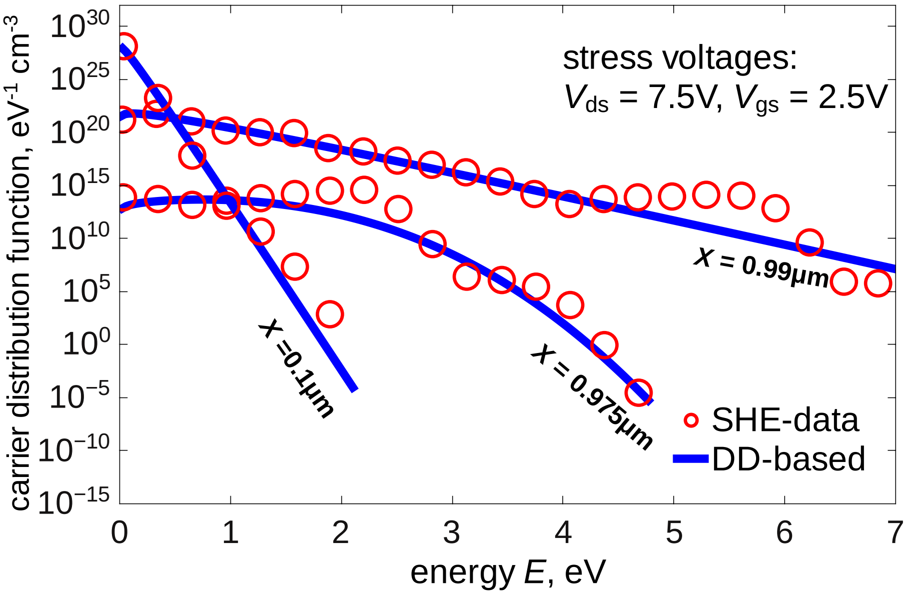

Figure 7.3: Same as Figure 7.1 but with $L_G = 2.0\,\mu$m.

the two versions of the model are significantly different. However, since in these devices the interface state profiles $N_{it}(x)$, and therefore also the degradation, are mainly determined by the SC-process, the DD-based version of the model should be able to properly capture the HCD traces for the 1.5$\mu$m structure. The situation deteriorates for the smaller nodes. Although the contribution of the MC-mechanism is properly represented by the simplified

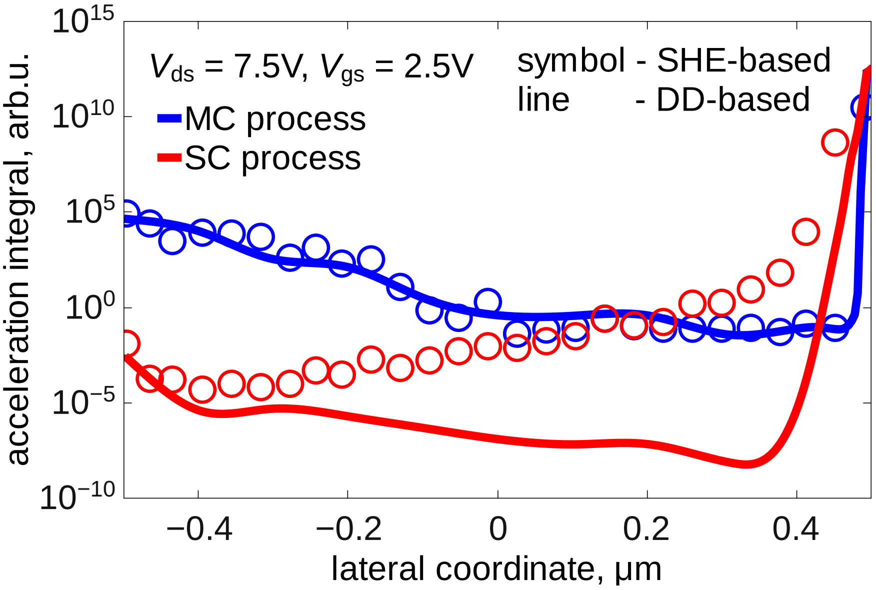

Figure 7.4: The acceleration integrals for the SC- and the MC-process calculated from the DFs obtained from the DD-based model (solid lines) and ViennaSHE (dashed lines) for $V_{ds} = 7.5\,$V and $V_{gs} = 2.5\,$V for the nMOSFET with $L_G = 1.0\,\mu$m.

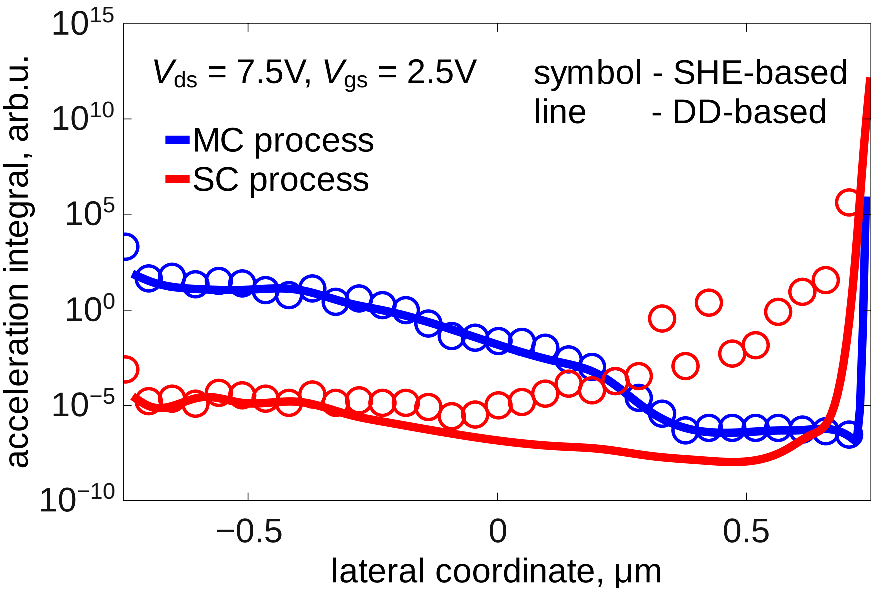

Figure 7.5: Same as Figure 7.4 but for $L_G = 1.5\,\mu$m.

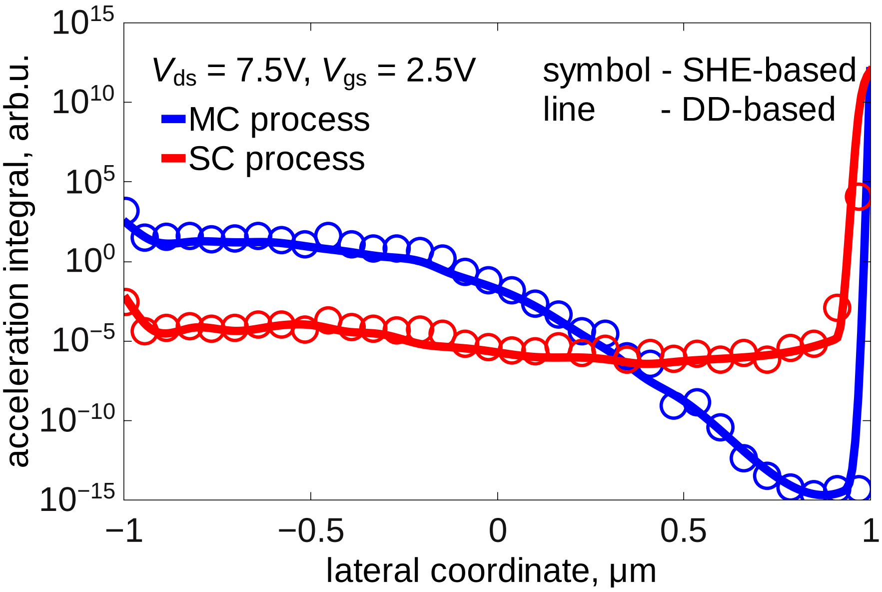

Figure 7.6: Same as Figure 7.4 but for $L_G = 2.0\,\mu$m.

approach, the bond breakage rates of the SC-process are profoundly underestimated. While the SHE-based version predicts a significant build up of interface states in the channel, triggered by the interplay between the SC- and MC-mechanism, which is not adequately described by the DD-based approach.

In order to investigate the mismatch of the DFs (Figure 7.1) and the impact of the bond breakage rates (Figure 7.6) onto the interface trap profiles, the $N_{\mathrm{it}}(x)$ values simulated with both versions of the model are plotted in Figure 7.7. One can see that in the case of the longest device, i.e. the $2\mu$m nMOSFET structure, the $N_{\mathrm{it}}(x)$ profiles are very similar. This

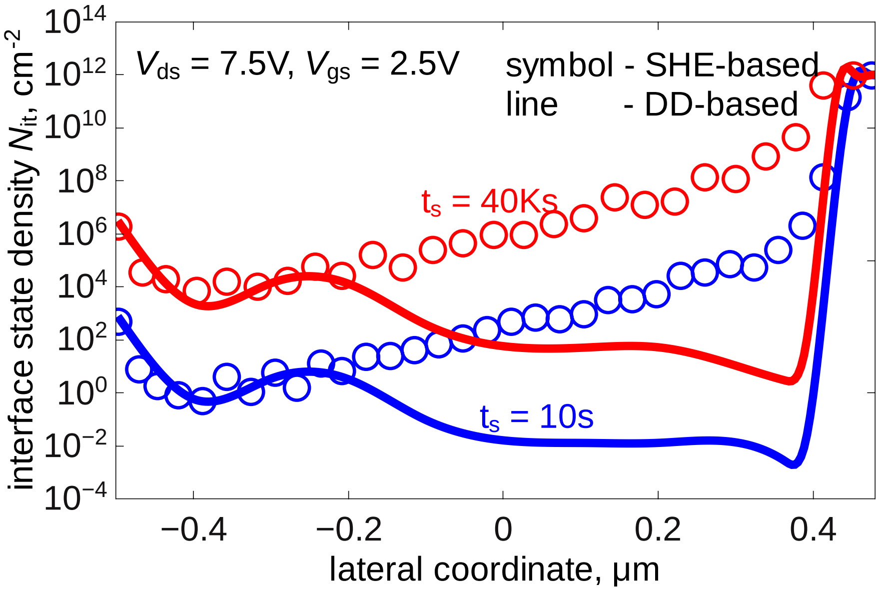

Figure 7.7: The $N_{\text{it}}(x)$ profiles evaluated for the three nMOSFETs with gate lengths $L_{\text{G}} = 1.0\,\mu$m by both versions of the model for stress times of 10 s and 40 ks.

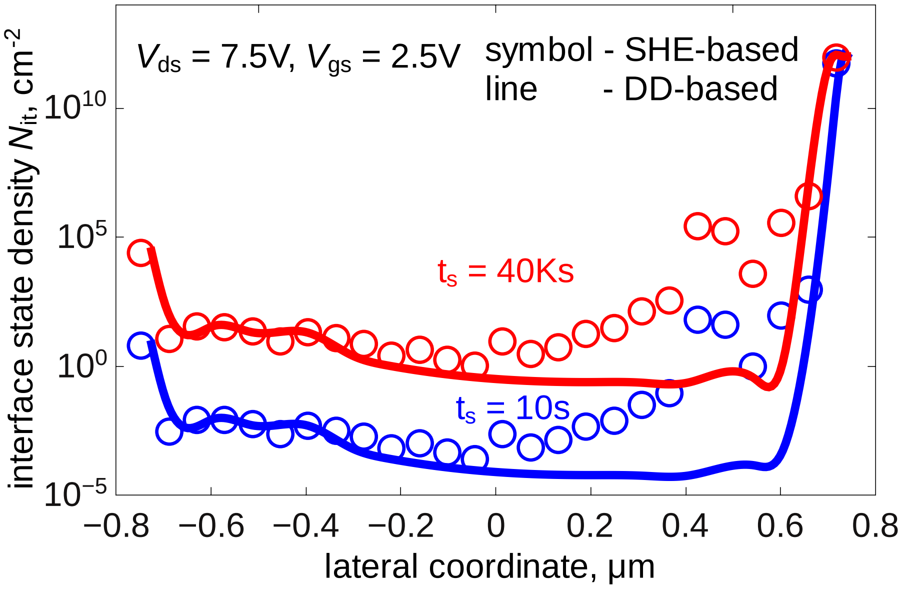

Figure 7.8: Same as Figure 7.7 but for $L_{\text{G}} = 1.5\,\mu$m.

is caused by the fact that the electron DFs are properly approximated by the DD-based model as can be seen in Figure 7.1. The situation starts to change for the shorter structure with $L_{\text{G}} = 1.5\,\mu$m, i.e. agreement between both models deteriorates. For the device with $L_{\text{G}} = 1.5\,\mu$m the discrepancy between the $N_{\text{it}}(x)$ values is visible at $N_{\text{it}} \sim 10^8\text{cm}^{-2}$. The $N_{\text{it}}$ peak at the drain side becomes broader and is shifted towards the channel as can be concluded from Figure 7.6. The DD-based approach is not able to capture this trend. Since $N_{\text{it}}$ values of $\sim 10^8\text{cm}^{-2}$ do not contribute to the total device degradation, a significant

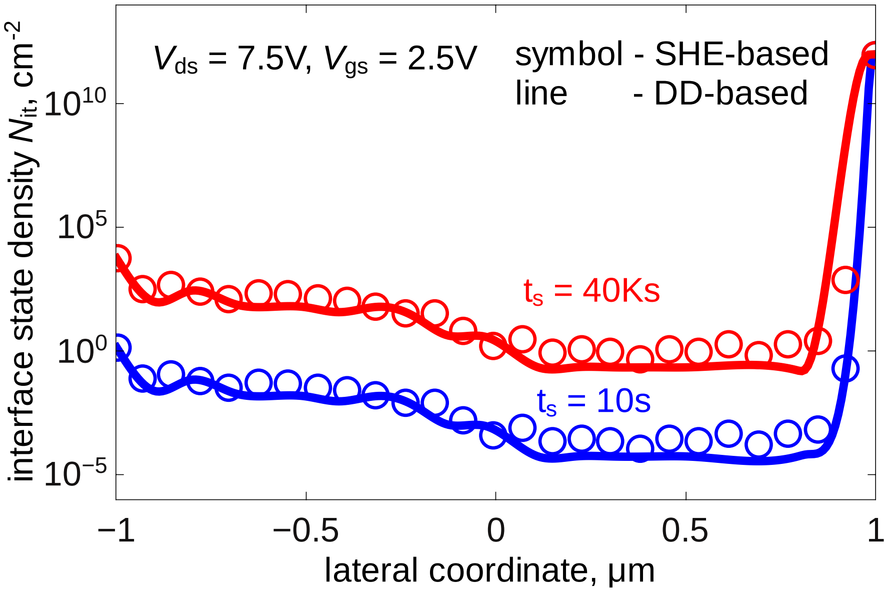

Figure 7.9: Same as Figure 7.7 but for $L_G = 2\,\mu$m.

deviation between the $\Delta I_{D,lin/sat}$ degradation curves simulated by the two model versions is not expected. For the shortest device, however, the interface trap densities already differ by about $\sim 10^{12}$cm$^{-2}$. Such large values provide a considerable contribution to HCD and lead to a visible discrepancy between the drain current degradation traces.

As a result, best correspondence between $\Delta I_{D,lin/sat}$ obtained with the SHE- and DD-based models is achieved for the 2.0$\mu$m nMOSFET, see Figure 7.11. Note, however, that

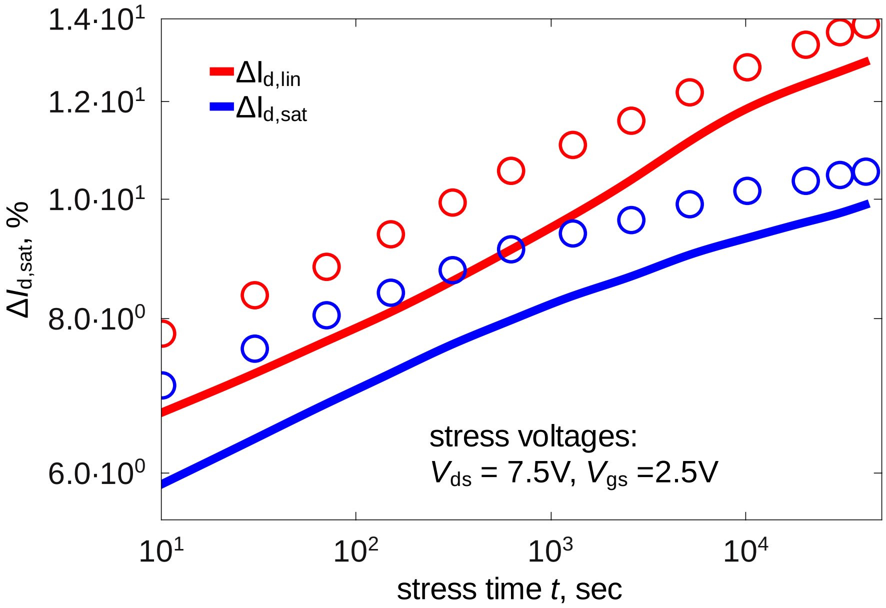

Figure 7.10: The $\Delta I_{d,lin}(t)$ and $\Delta I_{d,sat}(t)$ degradation curves obtained with SHE(symbols) - and DD-based (lines) versions model for n-MOSFET with $L_G = 1\,\mu$m.

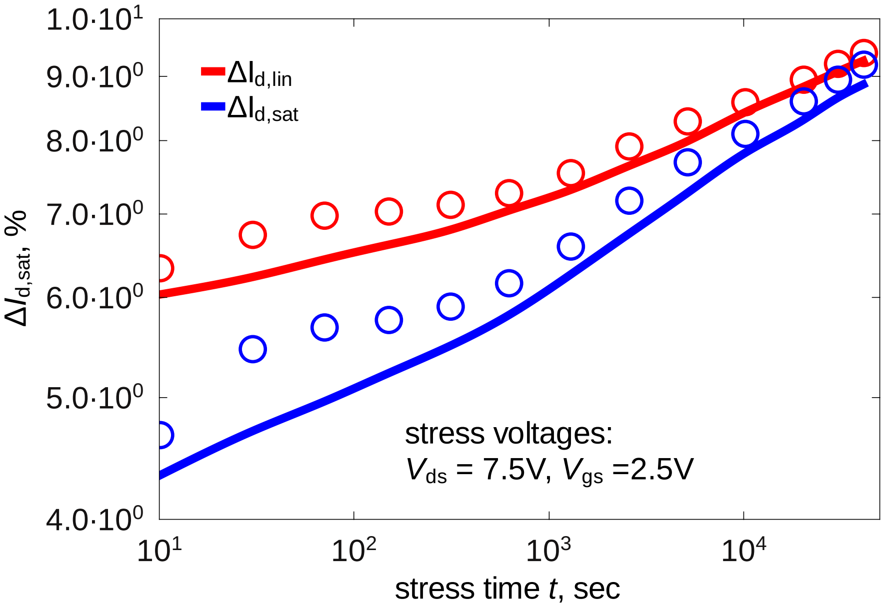

Figure 7.11: Same as Figure 7.10 but for $L_{\mathrm{G}} = 1.5\,\mu\mathrm{m}$.

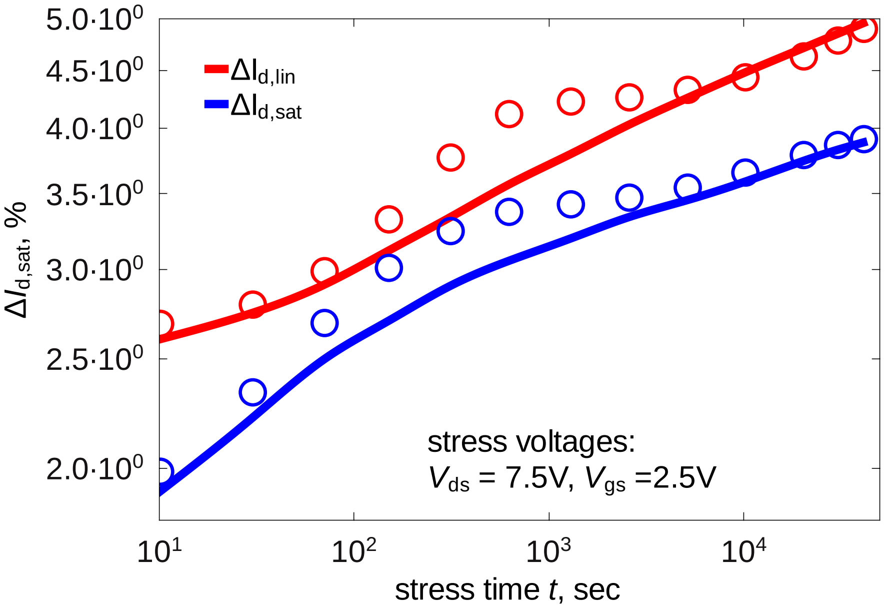

Figure 7.12: Same as Figure 7.10 but for $L_{\mathrm{G}} = 2\,\mu\mathrm{m}$.

even for this device the analytic model leads to lower $\Delta I_{\mathrm{D,lin/sat}}$ values at short stress times. This is because, as shown in [26, 147], short-term HCD is determined by the DFs at the drain, which are underestimated by the DD-based model, see Figure 7.1.

The same argument also holds for the 1.5 $\mu$m device where the agreement is still reasonable. Hot carrier degradation is slightly underestimated over the whole stress time range due to the mismatch of the interface state profiles visible in Figure 7.7. For the shortest device the DD-based model completely fails to properly reproduce the data evaluated with the full model. This already becomes evident in Figures 7.1, 7.6, and 7.7 where one can see that the DD-based model is not capable of reasonable mimicking the ViennaSHE results, respectively the big discrepancies between the shape of the interface state profiles.

To conclude, the drift-diffusion based hot-carrier degradation model, created for high voltage LDMOS devices, is found to work reasonably well for MOSFETs with channels longer than 1.5$\mu$m. In such devices, the model was able to represent the carrier distribution functions, bond breakage rates, interface state density profiles, and changes of device characteristics such as the saturation and drain currents. However, the model does not work very well for smaller nodes. The reason is that the DD-based model is not able to capture more complicated DF shapes visible in shorter devices. This is especially pronounced at high energies because the DFs simulated with ViennaSHE and by the DD-based HCD model have different curvatures. In the case of the 2$\mu$m device the curvature change occurs only when the DF values have dropped by several orders of magnitude, and therefore this discrepancy does not translate into mismatches between bond breakage rates, $N_{\mathrm{it}}(x)$ profiles and $\Delta I_{\mathrm{d,lin}}(t)$, $\Delta I_{\mathrm{d,sat}}(t)$ degradation traces.

As for shorter devices, the discrepancy in the DF curvature appears at higher population numbers, and thus is related to more pronounced errors. In the device with $L_{\mathrm{G}} = 1.5\,\mu$m this results in a mismatch in the $N_{\mathrm{it}}(x)$ profiles visible at $10^8$cm$^{-2}$, and thereby does not substantially impact the $\Delta I_{\mathrm{d,lin}}(t)$, $\Delta I_{\mathrm{d,sat}}(t)$ changes. In the shortest nMOSFET used, $L_{\mathrm{G}} = 1\,\mu$m, $N_{\mathrm{it}}$ values differ severely at values of $10^{12}$cm$^{-2}$, and hence the changes of the linear and saturation drain currents simulated with the two versions of the model are completely inconsistent.

# Chapter 8

# Role of Electron-Electron Scattering

An important aspect in modeling hot-carrier degradation for short-channel devices is electron-electron scattering (EES) [85, 86, 13, 24]. The steps for calculating the carrier DFs with EES are shown in Figure 8.1. EES populates the high-energy fraction of the carrier ensemble, thereby considerably changing the shape of the carrier DF, which is visible in a characteristic hump pronounced at high energies, see Figure 8.2 [11, 15]. Apparently EES also determines the temperature behavior of HCD in scaled devices [11, 88]. To obtain the carrier DF, the BTE should be solved taking this scattering effect into account. However, it might be possible to approximate the DFs utilizing the knowledge of the effects of EES on the DF. In this section, the drift-diffusion based model for the carrier energy distribution

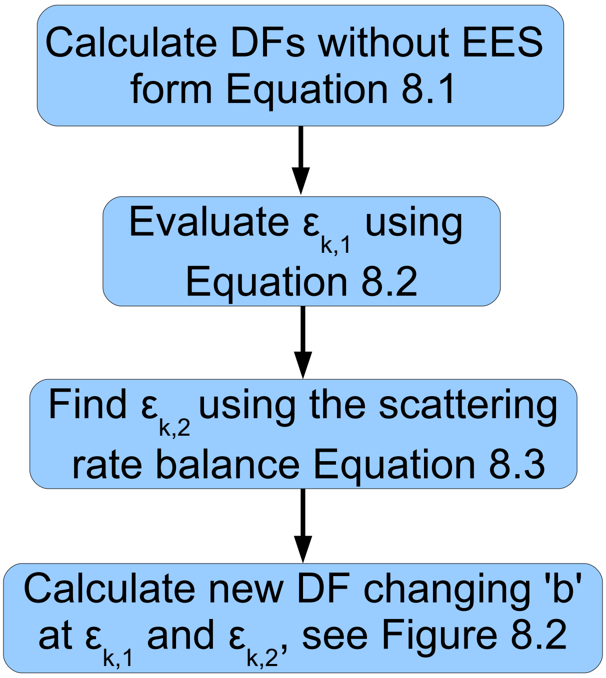

Figure 8.1: Flow chart for the calculation of the carrier DF.

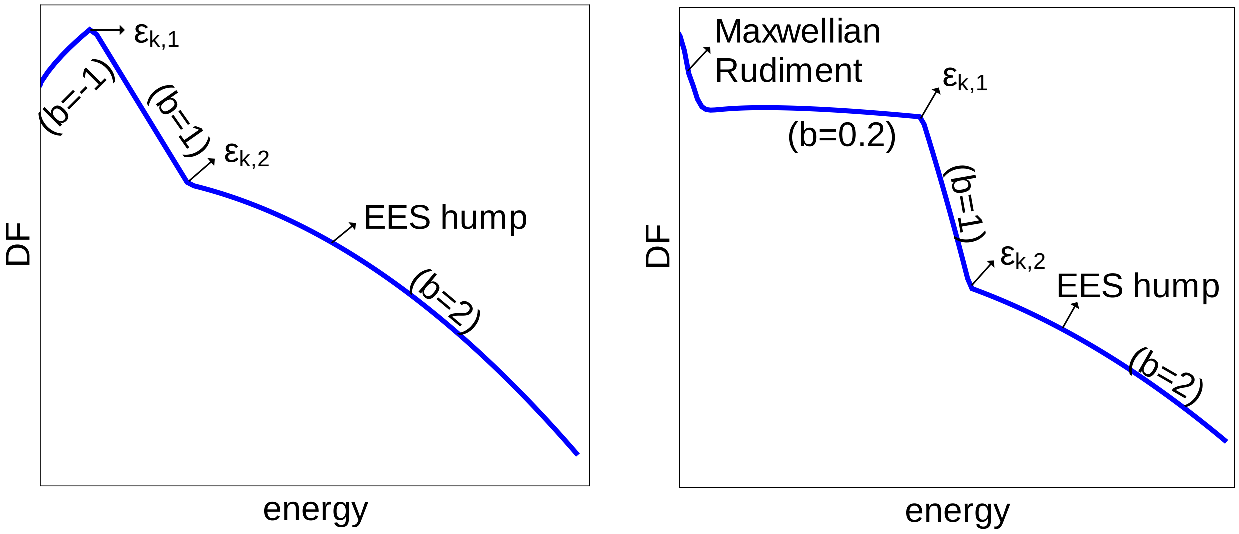

Figure 8.2: A schematic representation of the carrier DFs for the channel area (left panel) and for the drain (right panel) with all characteristic peculiarities marked.

function, Section 4.3, which was derived to describe hot-carrier degradation in LDMOS transistors, is extended for the case of decananometer devices nMOSFETs with gate lengths of 65, 150, and 300 nm. Special attention is paid to the effect of EES on the carrier DFs. To approximately consider the important effect of electron-electron scattering on the shape

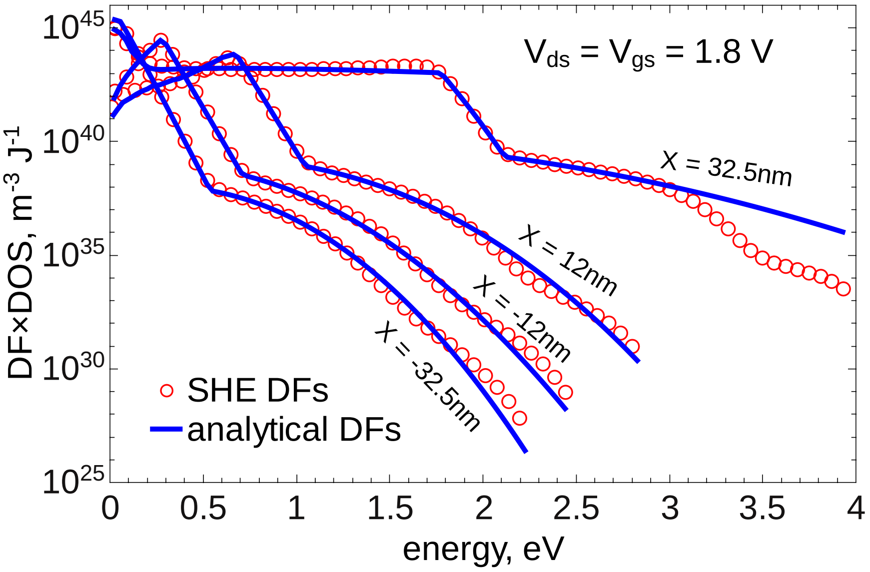

Figure 8.3: Comparison of carrier distribution functions calculated with ViennaSHE and our DD-based method in nMOSFET with $L_{\mathrm{G}} = 65\,\mathrm{nm}$ for stress condition $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$. DFs are plotted for four different positions in the device ($x =$ -32.5 nm corresponds to the source, while $x = 32.5\,\mathrm{nm}$ is related to the drain).

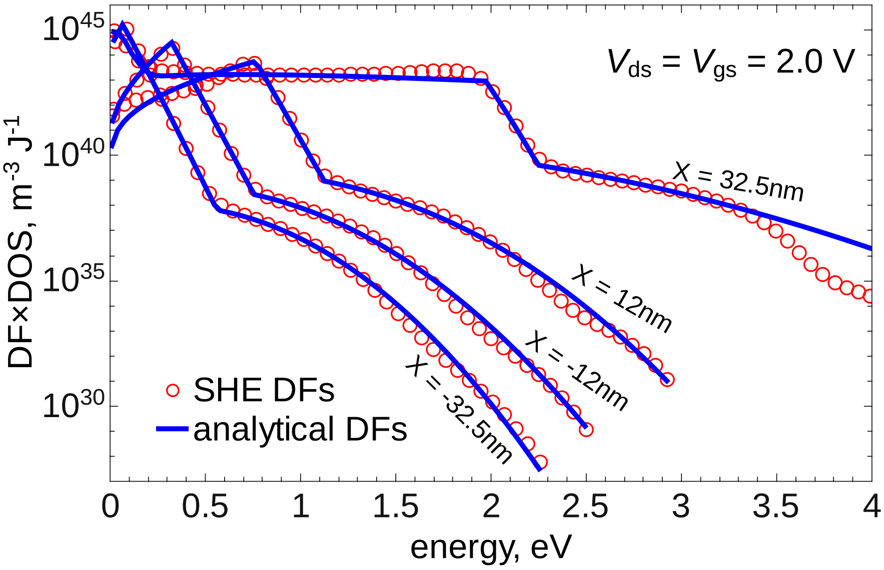

Figure 8.4: Same as Figure 8.3 but for $V_{gs} = V_{ds} = 2.0\,\mathrm{V}$.

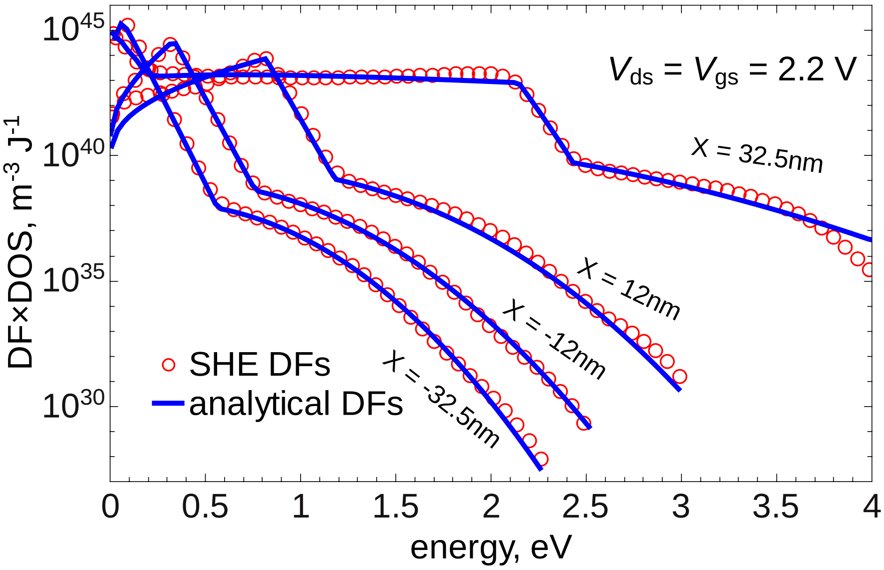

Figure 8.5: Same as Figure 8.3 but for $V_{gs} = V_{ds} = 2.2\,\mathrm{V}$.

of the distribution function, a balance equation is solved for the in- and out-scattering rates. The DFs obtained from the extended analytic approach are compared with those calculated with the deterministic Boltzmann transport equation solver ViennaSHE. Both sets of DFs are then used with the hot-carrier degradation model, Section 4.4, to calculate changes in the drain current as a function of stress time. The results of the extended DD-based model are compared with the results obtained using the full solution of the Boltzmann transport equation and with experimental data. The accuracy and limits of the applicability of the DD-based model is also studied on devices with a range of gate lengths. This model allows to avoid the computationally expensive solution of the BTE but is expected to still provide excellent accuracy.

## 8.1 Extended DD-Based Distribution Function Model

The reference electron DFs have been calculated with ViennaSHE for three different devices of the same architecture with SiON gate dielectric but with different gate lengths of 65, 150, and 300 nm and for three different stress conditions ($V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8, 2.0, 2.2\,\mathrm{V}$). The resulting DFs for the 65 nm device are shown in Figures 8.3 – 8.5. From these DF curves one

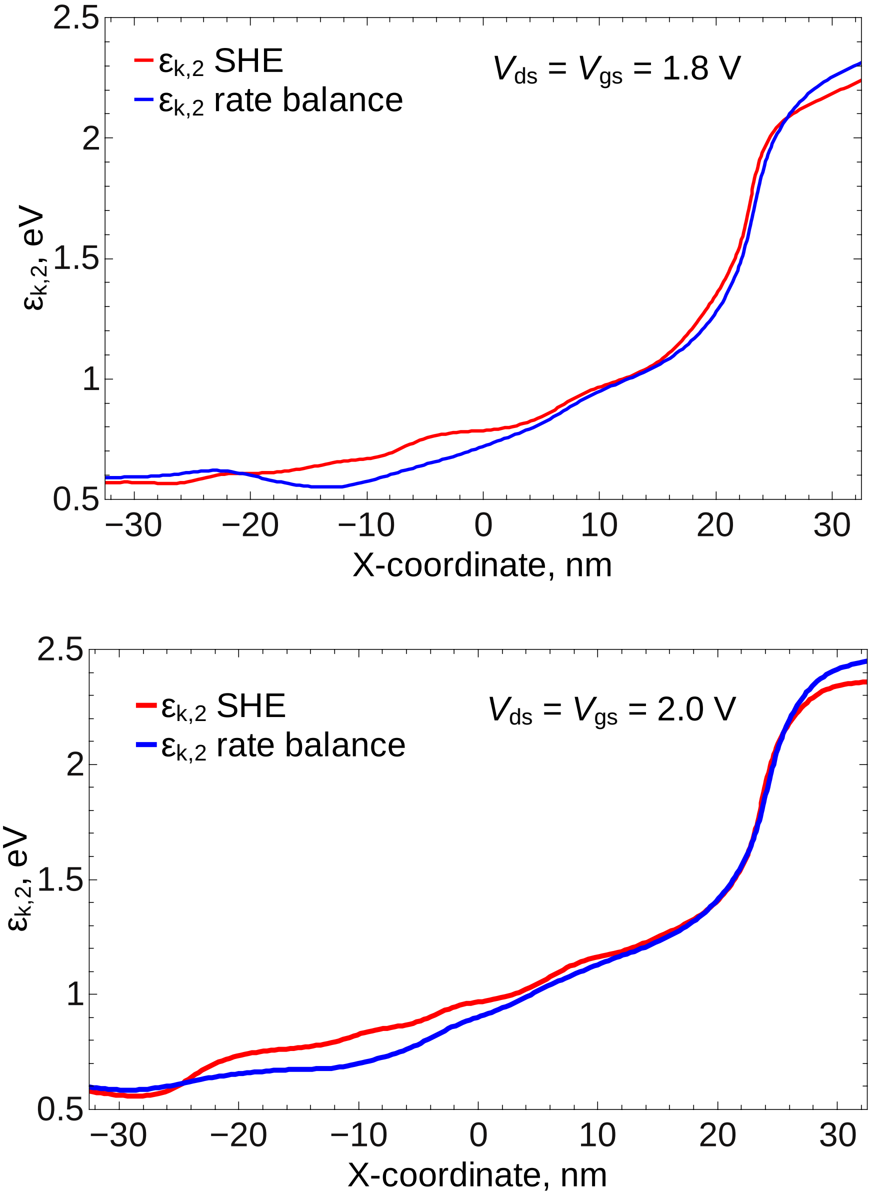

Figure 8.6: The knee energy $\varepsilon_{\mathrm{k},2}$, where EES starts to dominate the high-energy tail of the carrier DF, calculated with the analytic model plotted vs. ViennaSHE results for two different stress conditions $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$ (top) and $2.0\,\mathrm{V}$ (bottom).

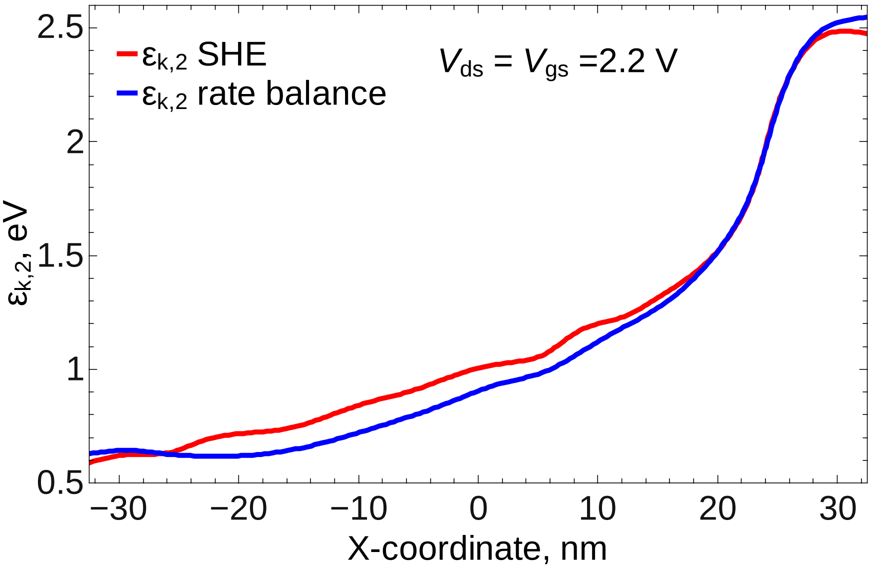

Figure 8.7: The knee energy $\varepsilon_{\mathrm{k},2}$, where EES starts to dominate the high-energy tail of the carrier DF, calculated with the analytic model plotted vs. ViennaSHE results for stress condition $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 2.2\,\mathrm{V}$.

can see that the DF shape substantially changes from the source to the drain. Indeed, DFs evaluated near the source and in the channel have a maximum visible at low and moderate energies with the corresponding energy labeled as $\varepsilon_{\mathrm{k},1}$ in Figure 8.2. As for the drain DFs, they typically feature a Maxwellian tail visible at low energies followed by a plateau. The end of this plateau also corresponds to the knee energy $\varepsilon_{\mathrm{k},1}$, see Figure 8.2. Another characteristic energy where the DF changes its curvature is related to the onset of the EES hump and is labeled as $\varepsilon_{\mathrm{k},2}$.

Such sophisticated DFs can be approximated by following the algorithm depicted in Figure 8.1. First, Equation 8.1 allows for a rough evaluation of the electron DF without the effect of electron-electron scattering using the parameters $A$, $\varepsilon_{\mathrm{ref}}$, and $C$ evaluated as earlier in Section 4.3

$$f(\varepsilon) = A \exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\mathrm{ref}}}\right)^{b}\right] + C \exp\left[-\frac{\varepsilon}{k_{\mathrm{B}} T_{\mathrm{n}}}\right]. \tag{8.1}$$

The parameter $b$ assumes a different value after every knee position, see Figure 8.2. In the channel and source regions $b$ is assigned a value of -1 before $\varepsilon_{\mathrm{k},1}$, 1 between $\varepsilon_{\mathrm{k},1}$ and $\varepsilon_{\mathrm{k},2}$, and 2 after $\varepsilon_{\mathrm{k},2}$. While for the drain region, $b$ has a value of 0.2 before $\varepsilon_{\mathrm{k},1}$, 1 between $\varepsilon_{\mathrm{k},1}$ and $\varepsilon_{\mathrm{k},2}$, and 2 after $\varepsilon_{\mathrm{k},2}$.

The first knee energy in the low energy region is evaluated analytically using the electric field from the DD simulations:

$$\varepsilon_{\mathrm{k},1} = \alpha \exp[\beta - (\gamma - \delta E)]^{\frac{1}{2}}, \tag{8.2}$$

where $E$ is the electric field, while $\alpha$, $\beta$, $\gamma$ , and $\delta$ are fitting parameters with values $0.4157\,\mathrm{eV}$, 1.3, 11.04, $1.51 \times 10^{-6}\,\mathrm{cmV}^{-1}$, respectively. The second knee energy, where EES starts to dominate the high energy tail, is obtained by considering the balance of in- and out-scattering rates. The in-scattering rate corresponds to EES, while the out-scattering includes such mechanisms as interactions of electrons with phonons and ionized impurities [206, 207].

$$r_{\mathrm{ees}} = r_{\mathrm{ii}} + r_{\mathrm{op/abs}} + r_{\mathrm{op/emi}} + r_{\mathrm{acc}} \tag{8.3}$$

The collision integral, for a nondegenerate semiconductor, is written as [175]:

$$\frac{\partial f}{\partial t} = -\sum S(p, p_2; p', p'_2) f(p) f(p_2) + \sum S(p', p'_2; p, p_2) f(p') f(p'_2). \tag{8.4}$$

suggesting that carriers with momentum $p$ out-scatter and carriers with $p'$ in-scatter due to carriers with $p_2$ and $p'_2$ respectively. Since there is an equal probability for a carrier being in/out scattered, Equation 8.4 can be written as:

$$\frac{\partial f}{\partial t} = -\sum S(p, p_2; p', p'_2) \left( f(p) f(p_2) - f(p') f(p'_2) \right). \tag{8.5}$$

Equilibrium is reached when the in- and out-scattering rates balance.

For the scattering rates in Equation 8.3 the same standard expressions [175, 208] were used in both ViennaSHE and the DD-based model. The scattering rate of carriers by accoustic phonons $r_{\mathrm{acc}}$ can be written as [175]

$$r_{\mathrm{acc}} = \frac{D_{\mathrm{A}}^2 k_{\mathrm{B}} T_{\mathrm{L}} m^* p}{\pi c_{\mathrm{l}} \hbar^4}, \tag{8.6}$$

where $D_{\mathrm{A}}$ is the accoustic deformation potential, $c_{\mathrm{l}}$ is the elastic constant ($v_{\mathrm{s}} = \sqrt{c_{\mathrm{l}}/\rho}$, $v_{\mathrm{s}}$ is the velocity of sound and $\rho$ is the mass density). For a spherical parabolic band the rate becomes

$$r_{\mathrm{acc}} = \frac{D_{\mathrm{A}}^2 k_{\mathrm{B}} T_{\mathrm{L}} m^* \sqrt{2m^* \varepsilon}}{\pi c_{\mathrm{l}} \hbar^4}. \tag{8.7}$$

Note that for a fair comparison the same physical parameters are used in both the SHE code and the analytic approximation.

Optical phonon scattering can be due to absorption or emission of the optical phonons. The corresponding rates are given by Equation 8.8 and 8.9, respectively [175]:

$$r_{\mathrm{op/abs}} = \frac{D_{\mathrm{o}}^2 N_{\mathrm{o}} m^* \sqrt{2m^* \left(\varepsilon + \hbar\omega_{\mathrm{o}}\right)}}{2\pi\rho\omega_{\mathrm{o}}\hbar^3} \tag{8.8}$$

$$r_{\mathrm{op/emi}} = \frac{D_{\mathrm{o}}^2 \left(N_{\mathrm{o}} + 1\right) m^* \sqrt{2m^* \left(\varepsilon - \hbar\omega_{\mathrm{o}}\right)}}{2\pi\rho\omega_{\mathrm{o}}\hbar^3} \tag{8.9}$$

where $D_{\mathrm{o}}$ is the accoustic deformation potential, $\hbar\omega_{\mathrm{o}}$ is the energy of optical phonon, $N_{\mathrm{o}}$ is the density of optical phonons ($N_{\mathrm{o}} = 1/\left(\exp\left[\hbar\omega_{\mathrm{o}}/k_{\mathrm{B}} T_{\mathrm{L}}\right] - 1\right)$).

The ionized impurity scattering rates are [175]:

$$r_{\mathrm{ii}} = \frac{N_{\mathrm{I}} q^4}{16\sqrt{2m^*}\pi \left(\epsilon_{\mathrm{Si}}\epsilon_0\right)^2} \left[\ln\left(1 + \gamma_{\mathrm{D}}^2\right) - \frac{\gamma_{\mathrm{D}}^2}{1 + \gamma_{\mathrm{D}}^2}\right] \frac{1}{\varepsilon^{3/2}} \tag{8.10}$$

where

$$\gamma^2 = 8m^* \varepsilon L_{\mathrm{D}}^2 / \hbar^2$$

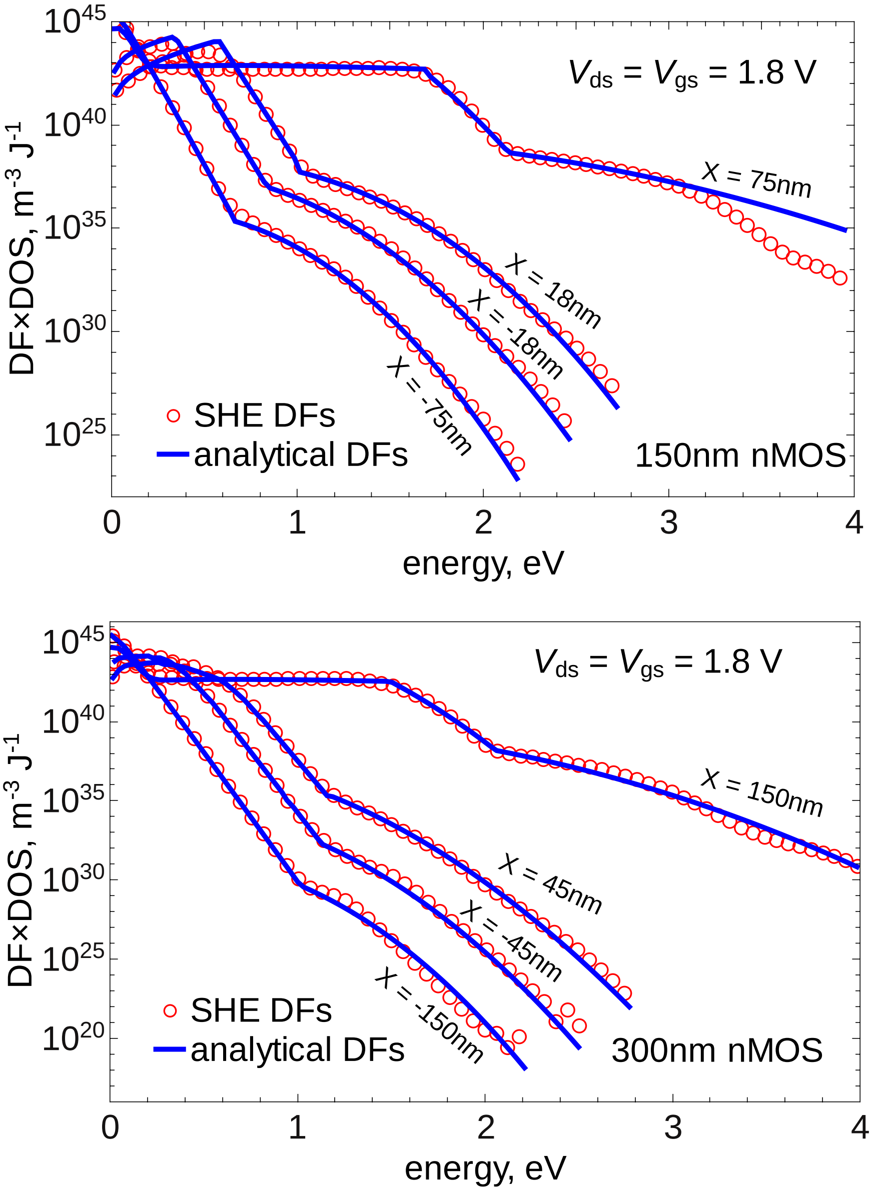

Figure 8.8: The electron DFs simulated with ViennaSHE and with the DD-based model for nMOSFETs with gate lengths of 150 and 300 nm for $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$. These DFs are plotted for different positions in the device. The source is at $x = -L_{\mathrm{G}}/2\,\mathrm{nm}$ and the drain is at $x = +L_{\mathrm{G}}/2\,\mathrm{nm}$.

with $L_{\mathrm{D}}$ being the Debye length given as:

$$L_{\mathrm{D}} = \sqrt{\frac{\epsilon_{\mathrm{Si}}\epsilon_0 k_B T}{q^2 n_0}}$$

As for electron-electron scattering, we use the following expression [208]:

$$r_{\text{ees}} = \frac{mq^4 n}{\epsilon_{\text{Si}}^2 \epsilon_0^2 \hbar^3} \sum_{\varepsilon} \frac{\sqrt{2m^*}/\hbar \left|\sqrt{\varepsilon} - \sqrt{\varepsilon_0}\right|}{\beta^2 \left(\frac{2m^*}{\hbar^2}(\varepsilon - \varepsilon_0) + \beta^2\right)} f(\varepsilon) \tag{8.11}$$

where $\beta$ is the inverse Debye length. It is important to emphasize that calculation of the rate $r_{\text{EES}}$ requires a DF. For energies $E < \varepsilon_{\text{k,2}}$ the DF calculated with Equation 4.22 can be used, while for $E \geq \varepsilon_{\text{k,2}}$ the DF is perturbed due to EES. Once the knee energies are obtained, the DFs are evaluated by changing the value of the parameter $b$ at the knees in Equation 4.22. Same approach is followed for the 150 and 300 nm devices to obtain the DFs in Figure 8.8.

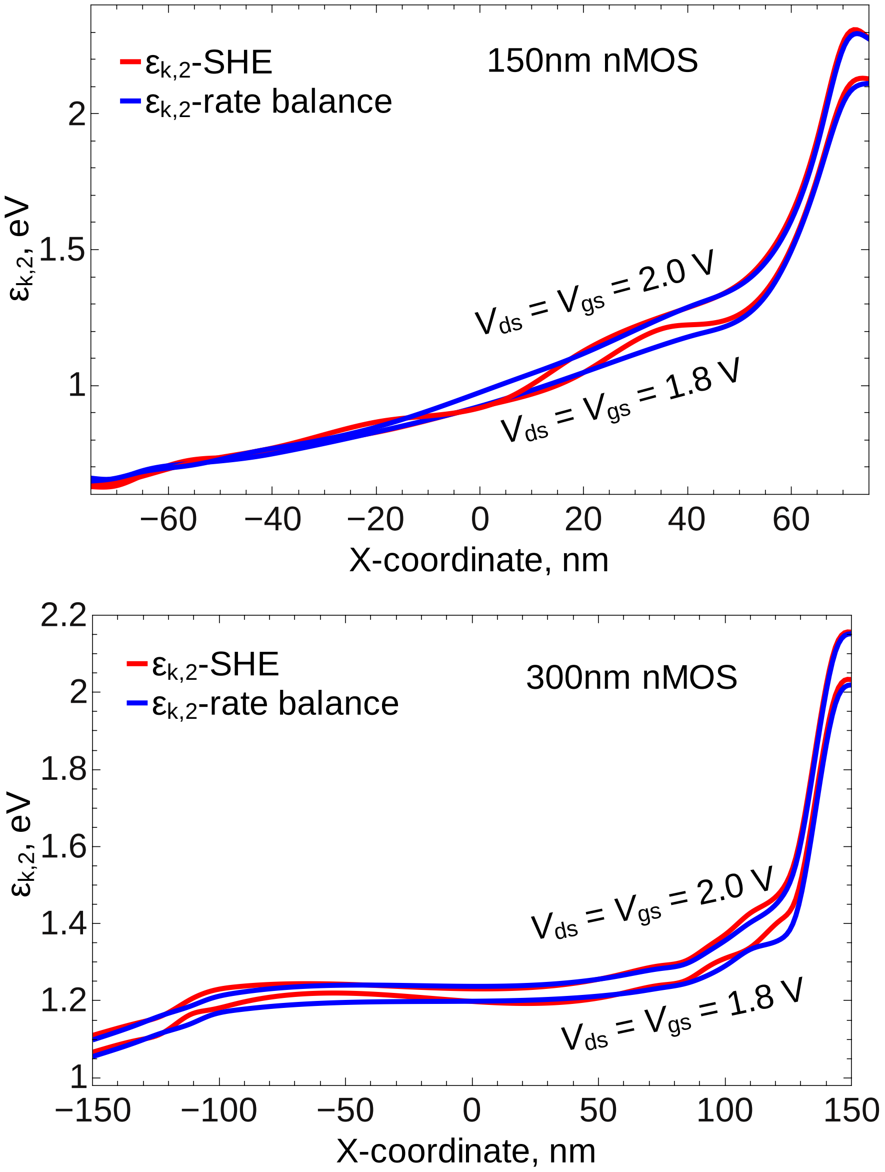

Figure 8.9: The knee energy $\varepsilon_{\text{k,2}}(x)$ for 150 and 300 nm devices calculated with the analytic model plotted vs. ViennaSHE results for stress conditions $V_{\text{gs}} = V_{\text{ds}} = 1.8\,\text{V}$ and $2.0\,\text{V}$.

## 8.2 Application of the Extended HCD Model to Scaled Devices

Figures 8.3 – 8.5 and 8.8 show very good agreement between the DFs simulated with our drift-diffusion based approach and with ViennaSHE for all combinations of $V_{\mathrm{gs}}$ and $V_{\mathrm{ds}}$ in 65 nm nMOS as well as for 150 and 300 nm nMOSFETs. Incorporation of the knee energies allow for an accurate representation of the high-energy tails and in particular the effect of EES. The values of $\varepsilon_{\mathrm{k},2}$ calculated with the analytical model are almost the same as those

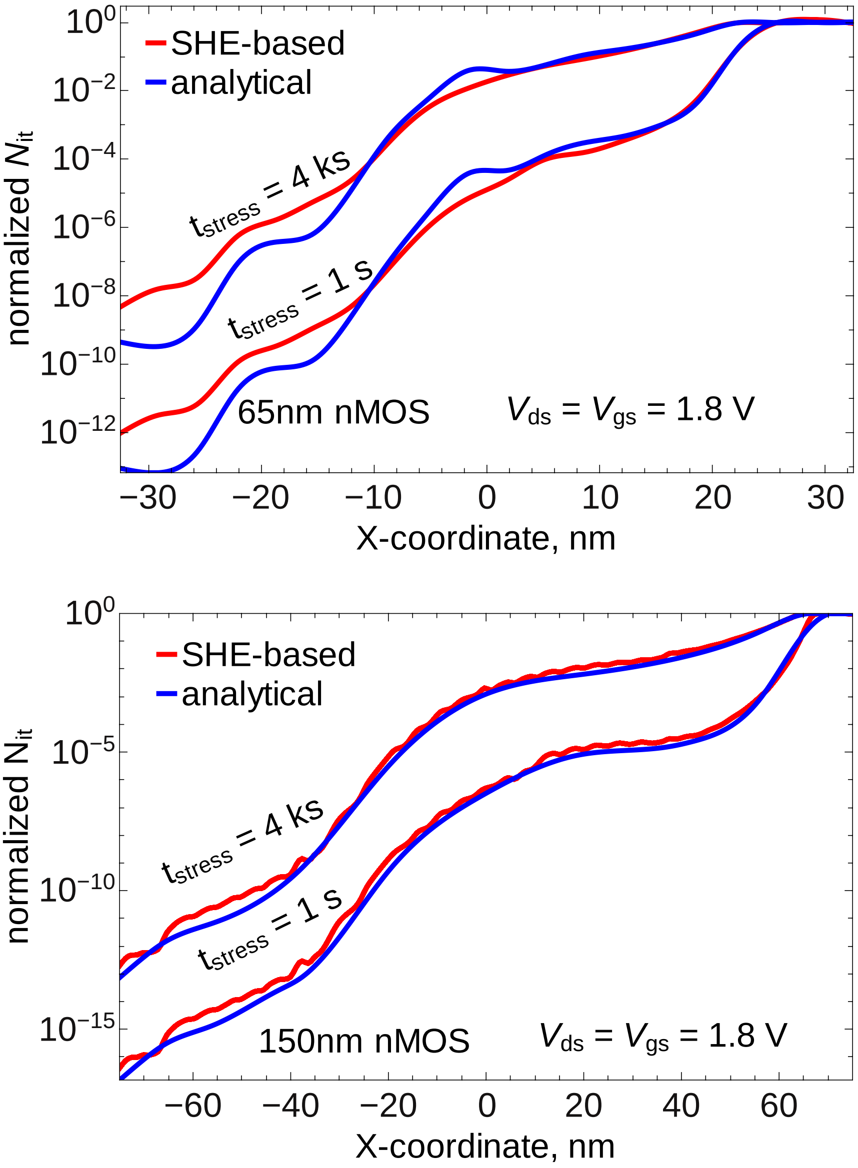

Figure 8.10: The interface state density profiles $N_{\mathrm{it}}(x)$ for 65 and 150 devices, normalized to the concentration of pristine Si-H bond , evaluated using DFs obtained with our analytic model and using ViennaSHE. Stress voltages are $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$. The profiles are shown for stress times of 1 s and 4 ks.

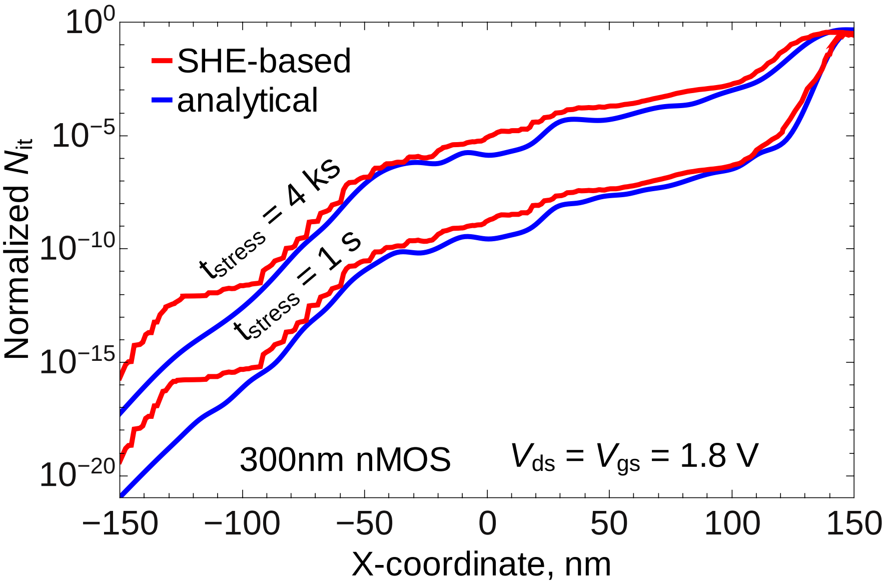

Figure 8.11: Same as Figure 8.10 but for 300 nm nMOSFET.

obtained from ViennaSHE for all the devices and stress conditions, see Figures 8.6, 8.7 and 8.9, thereby suggesting the validity of the rate balance method. After the second knee energy the analytic DFs show a visible error, especially for the 65 and 150 nm cases. However, the concentrations at these energies are quite low and do not affect hot-carrier degradation.

The carrier DFs obtained from ViennaSHE and the analytical approach are used with

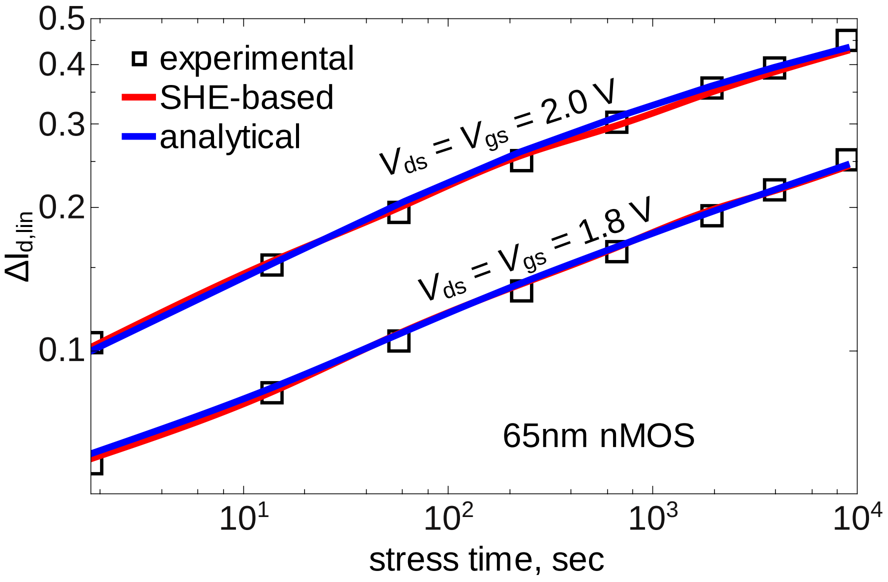

Figure 8.12: The normalized change in the linear drain current $\Delta I_{\mathrm{d,lin}}(t)$ as a function of stress time for $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$ and $2.0\,\mathrm{V}$: experiment vs. simulations for the 65 nm device.

our HCD model [13, 24] to calculate the interface state density ($N_{\mathrm{it}}(x)$) profiles. The $N_{\mathrm{it}}(x)$ profiles obtained from our physics-based HCD model for the three devices are shown in Figures 8.10 and 8.11. Figures 8.10 and 8.11 suggest that both SHE- and DD-based versions of the model for stress times of 1 s and 4 ks give similar results. These $N_{\mathrm{it}}(x)$ profiles are then used to simulate the characteristics of the degraded device.

To validate the model against experimental data, the HCD data acquired on SiON nMOSFETs with a gate length of 65 nm is used. These 65 nm devices were stressed under three different stress conditions, i.e. $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$ and 2.0 V at room temperature for ~8 ks. The relative changes in linear drain current $\Delta I_{\mathrm{d,lin}}(t)$ were recorded as a function of

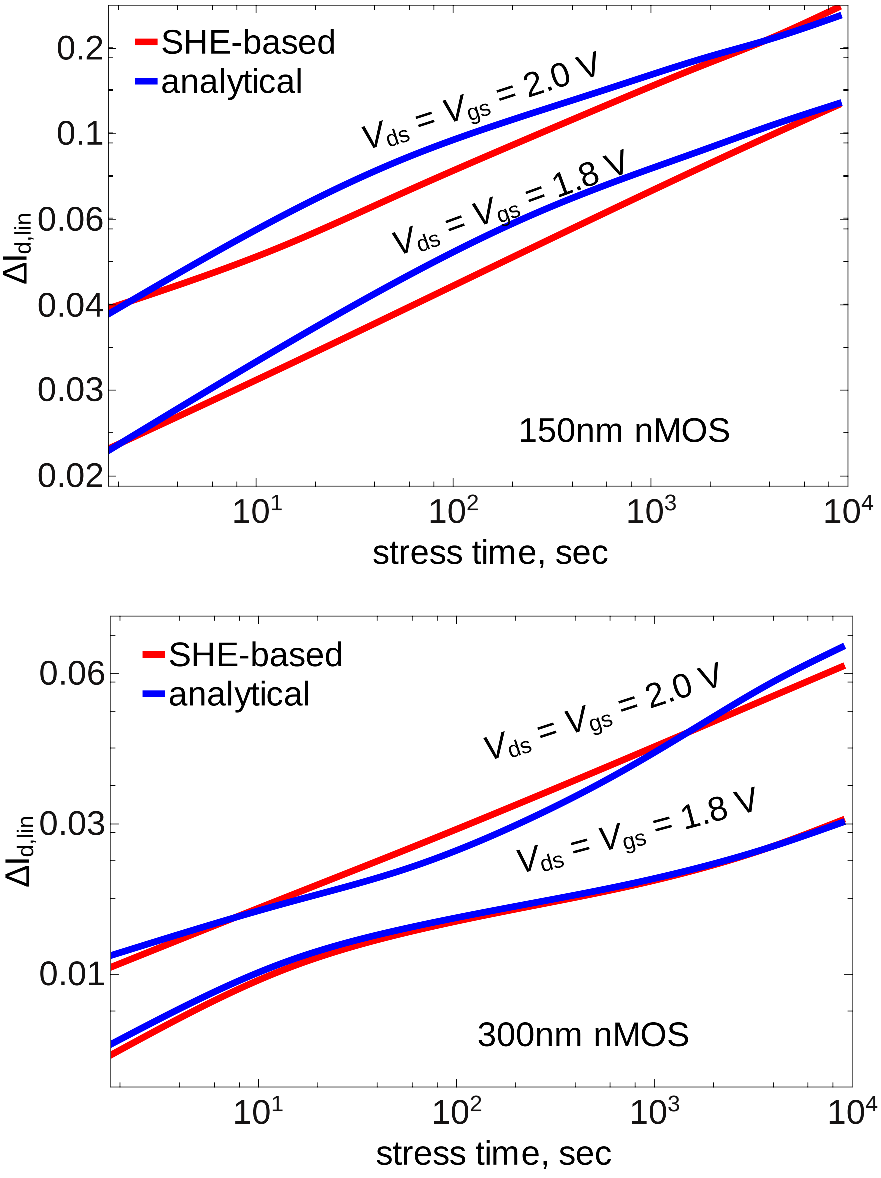

Figure 8.13: The normalized change in the linear drain current $\Delta I_{\mathrm{d,lin}}(t)$ as a function of stress time for $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$ and 2.0 V: the two simulated versions for the 150 and 300 nm devices.

stress time. A slight discrepancy in $N_{\mathrm{it}}(x)$ profiles and DFs visible at $x$ ∼-5 nm in the scattering dominated region does not translate into a model error. Figure 8.12 shows that the simulated $\Delta I_{\mathrm{d,lin}}(t)$ traces are almost identical and are in very good agreement with experimental data. As for the 150 nm transistor, Figure 8.13, there is a slight discrepancy in the results obtained with the DD-based and the full version of the model, which arises from a mismatch in the DFs observed at high energies. Finally, in the 300 nm nMOSFET, the DFs, $\Delta I_{\mathrm{d,lin}}$ acquired from the two methods match very well.

As can be understood from the schematic Figure 8.2, the DF should change its shape at a certain position in the device, say $X_{\mathrm{ch}}$. The value of $X_{\mathrm{ch}}$ is an important parameter of

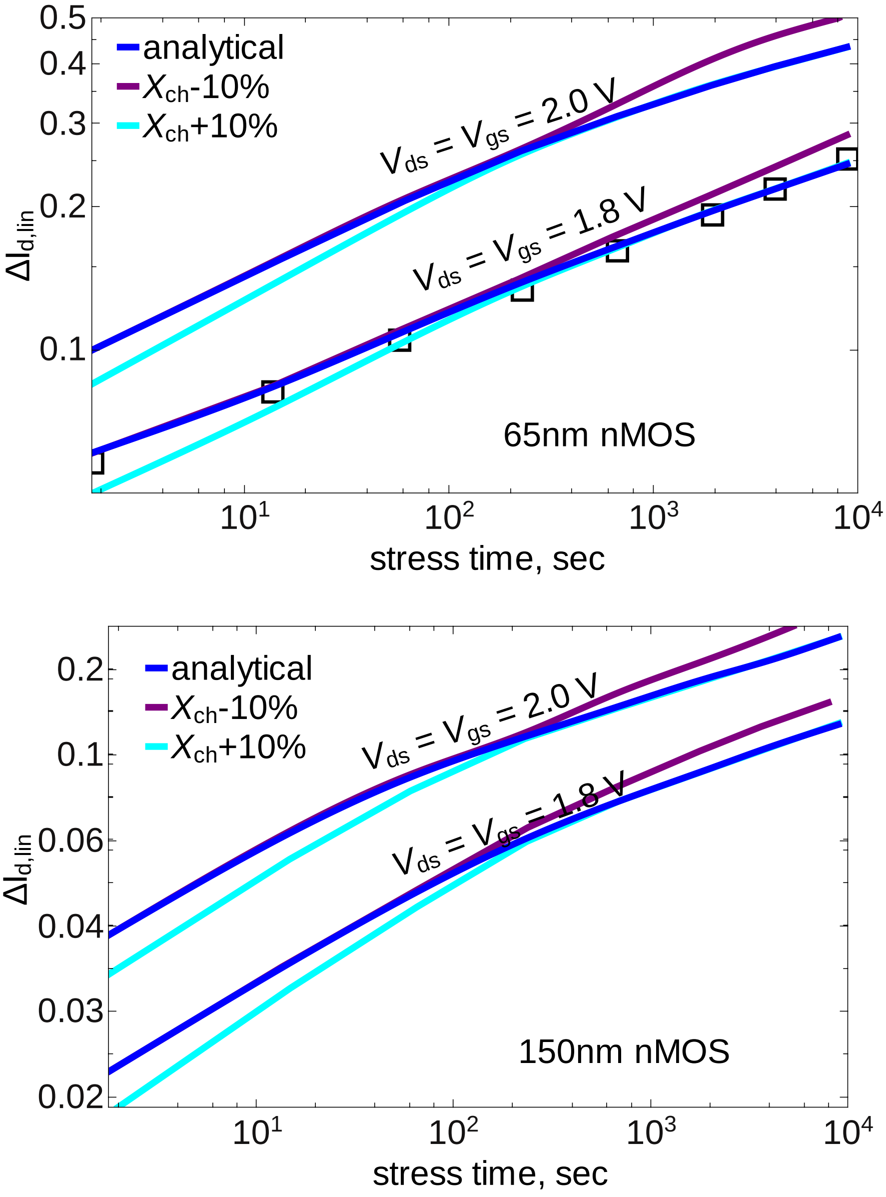

Figure 8.14: The stress voltages are $V_{\mathrm{gs}} = V_{\mathrm{ds}} = 1.8\,\mathrm{V}$ and 2.0 V. $\Delta I_{\mathrm{d,lin}}$ traces simulated with the shifted point of DF deformation with $X_{\mathrm{ch}} \pm 0.1 L_{\mathrm{G}}$ for 65 and 150 nm devices.

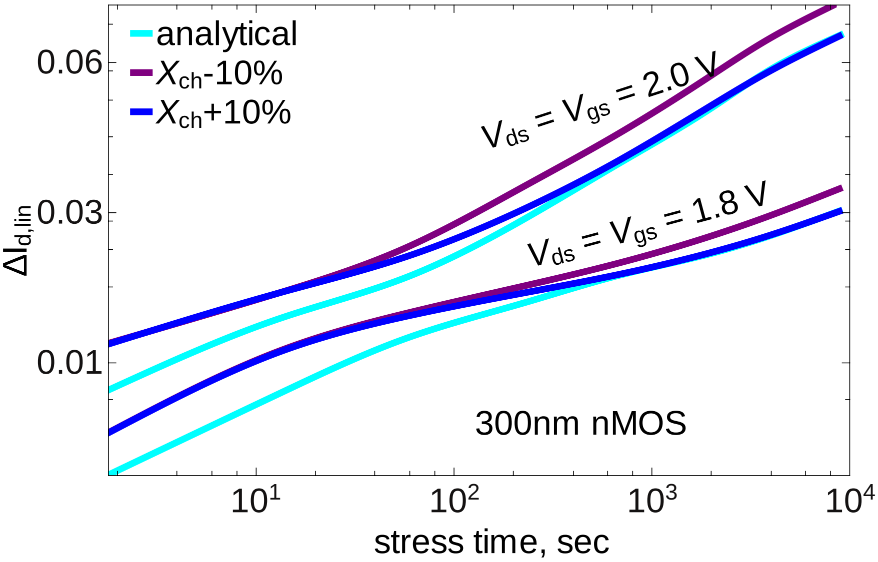

Figure 8.15: Same as Figure 8.14but for 300 nm device.

the model and therefore it is worth to study the model sensitivity to a change of $X_{\mathrm{ch}}$ to check the robustness of the model. The value of the coordinate $X_{\mathrm{ch}}$ is varied and the corresponding $\Delta I_{\mathrm{d.lin}}(t)$ traces are determined. Figures 8.14 and 8.15 summarize $\Delta I_{\mathrm{d,lin}}$ traces obtained with modified $X_{\mathrm{ch}}$ values of $X_{\mathrm{ch}}{\pm}0.1L_{\mathrm{G}}$. In all three devices the $\Delta I_{\mathrm{d,lin}}(t)$ dependencies simulated for $X_{\mathrm{ch}}{+}0.1L_{\mathrm{G}}$ show that HCD is underestimated at short times and almost by the same amount for longer stresses. HCD at short stress times is determined by the damage produced near the drain, i.e. by the drain DFs [24]. If we increase the $X_{\mathrm{ch}}$ value the change of the DF shape shown in Figure 8.2 occurs closer to the drain. Thus, DFs calculated for the segment of $[X_{\mathrm{ch}}, X_{\mathrm{ch}}+0.1L_{\mathrm{G}}]$ have lower populated high-energy tails and the damage near the drain is underestimated, thereby resulting in underestimated HCD at short stress times. The opposite trend is visible if $\Delta I_{\mathrm{d,lin}}$ dependencies are calculated for $X_{\mathrm{ch}}{-}0.1L_{\mathrm{G}}$.

## 8.3 EES Affecting the Temperature Behavior of HCD

The effect of EES also plays an important role in determining the temperature behavior of HCD in short channel devices. In [88], SiON nMOSFETs with an effective channel length of 44 nm were subjected to hot-carrier stress under Vds = Vgs = 1.8, 2.0, and 2.2 V and at two different temperatures, i.e. T = 25 and 75 °C. To asses HCD, $I_{\mathrm{d,lin}}(t)$ traces were recorded up to ∼9 ks. For $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 1.8$ and 2.0 V, $I_{\mathrm{d,lin}}$ values for T = 25 °C are higher than those for T = 75 °C. This result contradicts previous findings obtained in transistors with comparable gate lengths (e.g. [5] and [6]). Also, the distance between $I_{\mathrm{d,lin}}(t)$ curves reduces as $V_{\mathrm{ds}}$, $V_{\mathrm{gs}}$ increase, and at $V_{\mathrm{ds}} = V_{\mathrm{gs}} = 2.2$ V the $I_{\mathrm{d,lin}}$ values are almost the same for both temperatures within the whole stress time slot. This is because the rate of the MC-process was found to decrease with increase in temperature while the rate of the SC-process, augmented by EES, increases with temperature. Thus, as shown in Figure 8.16, the DFs have higher values at 25 °C in the lower energy region dominated by MC-

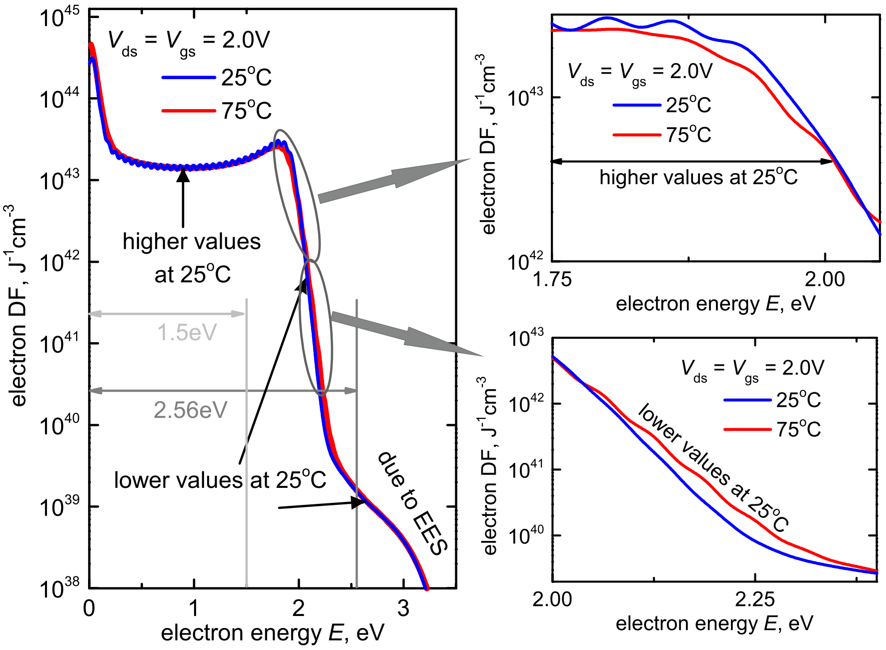

Figure 8.16: DFs near the drain region of a 44 nm SiON nMOSFET at $V_{gs} = V_{ds} = 2\,\mathrm{V}$ simulated with ViennaSHE for two temperatues, 25 °C and 75 °C. The hump in the DFs caused by EES is visible in the high energy region [88].

mechanism. While higher DF values are observed at 75 °C for the energy tails including the EES hump where the SC-mechanism of bond dissociation dominates. This trend is also evident from the distance between the $I_{\mathrm{d,lin}}(t)$ curves obtained for the two temperatures increasing when the SC-process is neglected.

# Chapter 9

# Conclusions

A comprehensive hot-carrier degradation (HCD) model should encompass all aspects of defect creation i.e. the effect of single- and multiple-carrier mechanisms and all their superpositions. Thus, an important element of the HCD model is the distribution of carriers over energy. In this work, the distribution function (DF) is first determined analytically using the moments of the Boltzmann transport equation (BTE) obtained from the drift-diffusion (DD) simulations. The expression used to approximate the carrier distribution function consists of terms for both hot and cold carriers. To compare the distribution functions, the full solution of the BTE is obtained using the spherical harmonics expansion method (SHE). The two different approaches, DD- and SHE-based, have been applied to describe carrier transport in n-channel LDMOS transistors and the calculated carrier energy distributions are used as input to a physics based hot-carrier degradation model. The degradation of the linear and saturation drain currents as well as the threshold voltage shift predicted by the two versions of the model, for different combinations of drain and gate voltages, are compared with the measurement data and it is shown that both approaches can capture HCD. This leads to the conclusion that in the case of nLDMOS devices the DD-based variant of the model provides good accuracy and at the same time is computationally less expensive. This makes the DD-based version attractive for predictive HCD simulations of nLDMOS transistors. The validity of the model is proven beyond nLDMOS transistors by following similar procedure for pLDMOS transistors. The carrier distribution functions, interface state density profiles, and changes of the drain currents vs. stress time are calculated in pLDMOS transistor. The comparison with measurements shows very good agreement.

Particular attention is paid to the study of the role of the cold fraction of the carrier ensemble. The effect of cold carriers is checked by neglecting the low energy carriers in HCD modeling in the case of nLDMOS devices stressed at high voltages. In this work, the cold carriers are represented by the corresponding term in the analytic formula for the carrier distribution function as well as by the multiple-carrier process of Si-H bond dissociation. It is shown that even in high-voltage devices stressed at high drain voltages the thermalized carriers still have a substantial contribution to HCD.

Different analytic models for the carrier distribution function, namely the heated Maxwellian, the Cassi model, the Hasnat model, the Reggiani model, and the model proposed in this work, are analyzed based on their applicability to describe hot-carrier degradation in nLDMOS devices. The DFs evaluated with these models are used to simulate the interface state generation rates, the interface state density profiles, and changes of the linear and saturation drain currents as well as the threshold voltage shift. It is shown that the heated Maxwellian model underestimates HCD at long stress times. This trend is also observed for the Cassi and Hasnat models but in these models HCD is underestimated in the entire stress time window. While the Reggiani model provides good results in the channel and drift regions, it cannot properly represent the high-energy tails of the DF near the drain, and thus leads to a weaker curvature of the degradation traces. Finally, the model used in this work is capable of capturing DFs with very good accuracy and, as a result, the change of the device characteristics with stress time.

The limits of applicability of the drift-diffusion based model for hot-carrier degradation have also been studied. Although the simplified version of the HCD model is quite successful for LDMOS devices, the analysis of linear and saturation drain current degradation predicted by the DD-based HCD model shows that it starts to fail for gate lengths shorter than 1.5$\mu$m and becomes completely inadequate for devices shorter than 1.0 $\mu$m. This limitation of the DD-based model stems from the fact that electron-electron scattering (EES) becomes significant in scaled devices and this effect is not incorporated in the simplified model.

Thus, the role of electron-electron scattering on the DF shape in short channel devices is elucidated. EES is known to dominate the high-energy tails of the DF. In this work, the energy which corresponds to the onset of such high-energy tail is called “knee energy” and is determined by the balance equation for in- and out-scattering rates. The distribution functions for scaled MOSFETs are evaluated by first finding an initial solution using the same approach as used for LDMOS devices and then refining the DF due to knee energies. The DF obtained from this extended analytic model and those obtained using the deterministic BTE solver ViennaSHE are almost identical. Furthermore, good agreement between the degradation characteristics obtained with the analytic approach and measurement data suggests that the extended model is well suited for describing hot-carrier degradation in decananometer devices. It is shown that the model can properly represent HCD in nMOSFETs with gate lengths in a range of 65-300 nm, while for longer devices a similar model but omitting EES is applicable. The main advantage of this model is that is uses the simple and fast DD scheme instead of the computationally demanding solution of the BTE.

# Appendix A

# The Basic Semiconductor Equations

The Poisson equation and continuity equations, derived from Maxwell's equations, form the basis of semiconductor device modeling describing the structure of the field problem. Since the modern semiconductor devices satisfy the criterion for quasi-electrostatic approximation[1], the displacement current ($\partial D/\partial t$) and induction ($\partial B/\partial t$) can be neglected in Maxwell's equations. Thus, the right hand side in Faraday's law $\nabla \times E = \partial B/\partial t$ becomes zero and allowing introduction of a scalar potential $\psi$.

$$E = -\nabla\psi, \tag{A.1}$$

when coupled with Gauss' law ($\nabla.D = \rho$)

$$\nabla.(\hat{\epsilon}.\nabla\psi) = -\rho. \tag{A.2}$$

Assuming the permittivity to be scalar and spatially dependent,

$$\begin{aligned} \epsilon.\nabla^2\psi &= -\rho, \\ \nabla^2\psi &= -\frac{\rho}{\epsilon} \end{aligned}$$

or

$$\nabla^2\psi = -\frac{q}{\epsilon}\left(n - p - C\right), \tag{A.3}$$

where n is the electron density, p the hole density and C the density of ionized impurities and dopants. Equation A.3 is known as Poisson's equation. The continuity equations are laid down for the electron and hole current density ($J_\mathrm{n}$, $J_\mathrm{p}$, respectively).

$$\nabla.J_\mathrm{n} - q\frac{\partial n}{\partial t} = qR, \tag{A.4}$$

$$\nabla.J_\mathrm{p} - q\frac{\partial p}{\partial t} = -qR, \tag{A.5}$$

---

[1] Quasi-electrostatic approximation is valid when the characteristic length of a system is considerably (~factor of 10) smaller than the shortest electromagnetic wavelenght present in the system.

where R denotes the net recombination rate. i.e. rate of electron-hole pair generation minus rate of recombination. Since the total number of charge particles remains constant, the Equations. A.4 and A.5 add up to zero. The unknowns in the three equations (eqns. A.3, A.4, and A.5) are $\psi$, $n$, $p$, $J_{\mathrm{n}}$, $J_{\mathrm{p}}$ (neglecting $R$, considering detailed balance for simplification). Thus two more equations are needed to evaluate the unknowns, which are endowed by the transport models.

# Appendix B

# Calculating the Moments of the Maxwell Distribution

The $i^{th}$ moment of the maxwellian distribution can be calculated from:

$$\langle \phi_i \rangle = \int k^i A \exp\left[\frac{-\varepsilon}{k_{\mathrm{B}} T_{\mathrm{n}}}\right] d^3k$$

by transforming the $k$-space into spherical polar coordinates as: $\int d^3k = \int_0^\infty 4\pi k^2 dk$.

$$\langle \phi_i \rangle = \int_0^\infty k^i A \exp\left[\frac{-\varepsilon}{k_{\mathrm{B}} T_{\mathrm{n}}}\right] 4\pi k^2 dk \tag{B.1}$$

Assuming a parabolic band dispersion relation $\varepsilon = \frac{\hbar^2 k^2}{2m}$, Equation B.1 becomes

$$\langle \phi_0 \rangle = 2\pi A \left(\frac{2m}{\hbar^2}\right)^{\frac{3}{2}} \int_0^\infty \varepsilon^{i+\frac{1}{2}} \exp\left[\frac{-\varepsilon}{k_{\mathrm{B}} T_{\mathrm{n}}}\right] d\varepsilon \tag{B.2}$$

Using the value of the gamma function ($\Gamma(x) = \int_0^\infty e^{-u} u^{x-1} du$) at1/2, $\Gamma(1/2) = \sqrt{\pi}$, and the property $\Gamma(x+1) = x\Gamma(x)$ the $i^{th}$ moment is reduced to:

$$\langle \phi_i \rangle = 2\pi A \left(\frac{2m k_{\mathrm{B}} T_{\mathrm{n}}}{\hbar^2}\right)^{\frac{3}{2}} (k_{\mathrm{B}} T_{\mathrm{n}})^i \left(i + \frac{1}{2}\right) \Gamma\left(i + \frac{1}{2}\right) \tag{B.3}$$

The parameter A in Equation B.3 can be evaluated by normalizing the distribution function.

# Appendix C

# Analytical Expression for the Moments

To calculate the moments as in Equations 4.24 and 4.25 we use the general format for a moment's equation:

$$m_i = \int_0^\infty \varepsilon^i f(\varepsilon) g(\varepsilon) d\varepsilon \tag{C.1}$$

for $f(\varepsilon)$ we use the DF expression used in this work:

$$f(\varepsilon) = A \exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\text{ref}}}\right)^b\right] + C \exp\left[-\frac{\varepsilon}{k_{\text{B}} T_n}\right],$$

and a general formulation of the the density of states $g(\varepsilon) = g_0 \sqrt{\varepsilon}\left(1 + (\eta\varepsilon)^\varsigma\right)$. The moment equation Equation C.1 then becomes:

$$m_i = \int_0^\infty \varepsilon^i \left(A \exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\text{ref}}}\right)^b\right] + C \exp\left[-\frac{\varepsilon}{k_{\text{B}} T_n}\right]\right) \left(g_0 \sqrt{\varepsilon}\left(1 + (\eta\varepsilon)^\varsigma\right)\right) d\varepsilon \tag{C.2}$$

$$\begin{aligned} = &\int_0^\infty \varepsilon^i g_0 \sqrt{\varepsilon} A \exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\text{ref}}}\right)^b\right] d\varepsilon + \int_0^\infty \varepsilon^i g_0 \sqrt{\varepsilon}\,(n\varepsilon)^\varsigma A \exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\text{ref}}}\right)^b\right] d\varepsilon \\ &+ \\ &\int_0^\infty \varepsilon^i g_0 \sqrt{\varepsilon} C \exp\left[-\frac{\varepsilon}{k_{\text{B}} T_n}\right] d\varepsilon + \int_0^\infty \varepsilon^i g_0 \sqrt{\varepsilon}\,(n\varepsilon)^\varsigma C \exp\left[-\frac{\varepsilon}{k_{\text{B}} T_n}\right] d\varepsilon \end{aligned} \tag{C.3}$$

Solving the first term in Equation C.3:

$$\begin{aligned} m_{i,1} = &\int_0^\infty \varepsilon^i g_0 \sqrt{\varepsilon} A \exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\text{ref}}}\right)^b\right] d\varepsilon \\ = &A g_0 \int_0^\infty \varepsilon^{i+\frac{1}{2}} \exp\left[-\left(\frac{\varepsilon}{\varepsilon_{\text{ref}}}\right)^b\right] d\varepsilon \end{aligned}$$

substituting $(\varepsilon/\varepsilon_{\text{ref}})^b$ as t gives:

$$\begin{aligned} m_{i,1} =& \frac{Ag_0}{b} \left(\varepsilon_{\text{ref}}\right)^{\frac{2i+3}{2}} \int_0^\infty t^{\frac{2i+3-2b}{2b}} \exp\left[-t\right] dt \\ =& \frac{Ag_0}{b} \left(\varepsilon_{\text{ref}}\right)^{\frac{2i+3}{2}} \Gamma\left(\frac{2i+3}{2b}\right) \end{aligned}$$

since $\Gamma(x) = \int_0^\infty t^{x-1} \exp\left[-t\right] dt$. Similarly, the other terms in Equation C.3 can be written as:

$$\begin{aligned} m_{i,2} =& \frac{Ag_0}{b} \left(\varepsilon_{\text{ref}}\right)^{\frac{2i+3}{2}} \left(\eta\varepsilon_{\text{ref}}\right)^{\varsigma} \Gamma\left(\frac{2i+3+2\varsigma}{2b}\right) \\ m_{i,3} =& Cg_0 \left(k_{\text{B}} T_n\right)^{\frac{2i+3}{2}} \Gamma\left(\frac{2i+3}{2}\right) \\ m_{i,4} =& Cg_0 \left(k_{\text{B}} T_n\right)^{\frac{2i+3}{2}} \left(\eta\varepsilon_{\text{ref}}\right)^{\varsigma} \Gamma\left(\frac{2i+3+2\varsigma}{2}\right) \end{aligned}$$

Thus the analytical expression for a moment can be written as:

$$\begin{aligned} m_i =& \frac{Ag_0}{b} \left(\varepsilon_{\text{ref}}\right)^{\frac{2i+3}{2}} \left(\Gamma\left(\frac{2i+3}{2b}\right) + \left(\eta\varepsilon_{\text{ref}}\right)^{\varsigma} \Gamma\left(\frac{2i+3+2\varsigma}{2b}\right)\right) + \\ & Cg_0 \left(k_{\text{B}} T_n\right)^{\frac{2i+3}{2}} \left(\Gamma\left(\frac{2i+3}{2}\right) + \left(\eta\varepsilon_{\text{ref}}\right)^{\varsigma} \Gamma\left(\frac{2i+3+2\varsigma}{2}\right)\right) \end{aligned} \tag{C.4}$$

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