

MASTER THESIS

Process Simulation and Model Development in ViennaPS

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supervised by

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Abstract

Microelectronics are present in almost all of the devices we use. Transistor and packaging miniaturization over the last several decades have resulted in highly complex fabrication. Since experiments which are required to understand the fabrication steps are becoming increasingly more expensive, computer simulations have become indispensable in the product design cycle. Simulations are used to enhance both fabrication processes (process TCAD) and analyze final device characteristics (device TCAD). In this work, ViennaPS, a process simulation library which includes Monte Carlo ray tracing and a surface description based on level sets, is improved upon and enriched with physical models, with a focus on ion-enhanced plasma etching processes.

Since SF_6/O_2 is the most frequently applied plasma etching chemistry, its physical model was implemented and validated. Due to complex fabrication processes, variations in masks used for etching are frequent. Therefore, mask properties such as etch rate, tapering angle, and thickness significantly impact the dimensions of the final structure. The implemented SF_6/O_2 model is applied to quantify this impact. The optimal mask taper angle for achieving the highest vertical etch rate and thereby the maximum depth was found to be at 0.5° and shifts to larger angles with the increase in the concentration of passivating species. At the peak depth, the bowing is minimal and vice-versa. For the faceting of thin masks, it was found that maximum depth increases with the faceting angle, and bowing is at the peak when this angle is between 15° and 20°.

In addition to the SF_6/O_2 physical model, a compact model which maps the plasma chamber parameters directly to the final geometry features was developed within the scope of this work. This geometric approach showed a firm agreement with the physical simulations, albeit with limitations in the input parameters which it is able to consider.

Kurzfassung

In fast allen Geräten, befinden sich mikroelektronische Bauteile. Der stetige Trend der Miniaturisierung von Transistoren und Gehäusen der letzten Jahrzehnte führt zu immer komplexer werdenden Herstellungsverfahren. Diese fortschreitende Erhöhung der Komplexität führt zu steigenden Kosten bei Experimenten, welche zum besseren Verständnis der Herstellungsschritte dienen. Die steigenden Kosten machen verhältnismäßig günstige Computersimulationen für den Produktentwicklungszyklus unverzichtbar. Diese Simulationen werden sowohl zur Verbesserung der Herstellungsprozesse (Process TCAD) als auch zur Analyse der resultierenden Bauteileigenschaften (Device TCAD) eingesetzt. Im Rahmen dieser Arbeit wird der Prozesssimulator ViennaPS, welcher Monte-Carlo ray tracing und eine auf Level Sets basierende Oberflächenbeschreibung verwendet, verbessert und mit physikalischen Modellen erweitert, wobei der Schwerpunkt auf ionenunterstützten Plasmaätzprozessen liegt.

Da SF₆/O₂ die am häufigsten verwendete Plasmaätzchemie ist, wurde ihr physikalisches Modell implementiert und validiert. Aufgrund der komplexen Herstellungsprozesse unterscheiden sich die Eigenschaften der für das Ätzen verwendeten Masken voneinander. Eigenschaften wie die Ätzrate, der Verjüngungswinkel und die Dicke der verwendeten Masken haben jedoch erhebliche Auswirkungen auf die Abmessungen der finalen Struktur. Um diesen Einfluss zu quantifizieren, wird das implementierte SF₆/O₂-Modell angewandt. Es wird gezeigt, dass der optimale Verjüngungswinkel der Maske zur Erzielung der höchsten vertikalen Ätzrate und damit der maximalen Tiefe 0.5 ° ist und dieser sich mit zunehmender Konzentration der passivierenden Spezies zu größeren Winkeln verschiebt. Bei der maximalen Tiefe ist die beobachtete Krümmung minimal und umgekehrt - bei minimaler Tiefe ist sie maximal. Bei der Facettierung dünner Masken wurde festgestellt, dass die maximale Tiefe mit dem Facettierungswinkel zunimmt und die Krümmung am größten ist, wenn dieser Winkel zwischen 15° und 20° liegt.

Zusätzlich zu dem physikalischen Modell wurde im Rahmen dieser Arbeit ein kompaktes Modell entwickelt, welches die Parameter für die Plasmakammer direkt auf die resultierenden Merkmale der Geometrie abbildet. Dieser geometrische Ansatz zeigte für eingeschränkte Eingabeparameter eine gute Übereinstimmung mit den physikalischen Simulationen.

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Lastly, I am deeply grateful for my family's unwavering love and support, whose encouragement and belief in me have made my academic success possible.

Affidavit

I declare in lieu of oath, that I wrote this thesis and performed the associated research myself, using only literature cited in this volume. If text passages from sources are used literally, they are marked as such.

Vienna, on March 1, 2023

Name of the Author

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1 Introduction

Microelectronics has been a fundamental technological building block of modern society for decades. Nowadays, semiconductor-based integrated circuits on microchips are present in almost all of the devices we use. Their miniaturization and enhancements made in the previous several decades have led to significant advances in various fields, including energy storage and production, the health industry, transportation, and many others. Technological developments have also enabled the emergence of entirely new fields, such as electric mobility, artificial intelligence, and the Internet of Things, reshaping many's lifestyles and ushering extreme changes to the way industry and society co-exist. Miniaturization, or scaling, has for a long time been able to follow "Moore's law" [1], which states that the number of transistors in an integrated circuit (IC) doubles after approximately every two years.

As the size of transistors continues to decrease and their density on a chip continues to increase, the fabrication complexity naturally keeps growing. Nowadays, microchips can contain billions of transistors and are made of a wide variety of materials in complex threedimensional (3D) structures, fabricated in a highly controlled environment [2]. Performing such fabrication requires a detailed understanding of the processes, and obtaining this understanding using experiments alone is extremely time consuming, expensive, and highly unfeasible. The high cost and inconvenience of running such long experiments created the need for simulating the fabrication and operation of semiconductor devices using predictive models, commonly referred to as technology computer-aided design (TCAD). To place TCAD into the industry context, the most common fabrication steps and their typical sequence is provided in the next section.

1.1 Semiconductor Fabrication

Fabrication of microelectronic devices typically begins on a silicon wafer and consists of many steps which result in highly complex structures. Each subsequent step either adds or removes a material and depends on the previous steps, making a high level of control and precision essential for the end-product performance and reliability. The fabrication steps which are used most frequently for integrated circuit (IC) fabrication are oxidation, photolithography, etching, deposition, chemical mechanical planarization (CMP), ion implantation, and diffusion [3]. This chapter provides a brief explanation of these processes.

1.1.1 Oxidation

An important reason why silicon became so significant in the semiconductor industry is the fact that it can be oxidized relatively easily to grow a dielectric layer of silicon dioxide [3, 4], which offers excellent properties including:

- Very good insulation with a resistivity higher than $1 \times 10^{20} \Omega$ cm. [5]
- High etch selectivity due to its resistance to most etching processes applied to silicon and metals. [6, 7]
- The Si SiO₂ interface is less prone to defects than other relevant materials, at least when it comes to the prototypical planar transistor architecture. [8]

The ease of forming an insulator on top of it made silicon the material of choice for the semiconductor industry, and the above-listed properties made silicon dioxide the material of choice for gate insulation for decades. It should be noted that SiO^2 has been replaced in the most advanced nodes by high-k dielectrics such as hafnium dioxide (HfO₂) due to too large leakage currents in sub-1 nm oxide layers [9]; nevertheless, it still holds an important place in the industry as it is used for back-end-of-line (BEOL) isolation, deep trench isolation, and in many applications which do not require highly-scaled advanced technology node transistor solutions. Therefore, oxidation of silicon is further described in this section.

Exposing silicon to air at room temperature produces a thin native oxide layer. The layer thickness can be controlled in the fabrication process by exposing the silicon to oxygen gas or water vapor at varying temperatures [4]. The chemical reactions occurring at the Si - SiO_2 interface are

$$Si + O_2 \to SiO_2$$
 (1.1)

$$Si + 2H_2O \to SiO_2 + 2H_2. \tag{1.2}$$

The reactions in Eq. (1.1) and (1.2) describe dry and wet oxidation, respectively. Wet oxidation consists of exposing the silicon wafer to water vapor in a controlled setting, and it is used when thicker layers are needed in a shorter amount of time. On the other hand, dry oxidation is used at smaller scales, where material quality is of higher importance. Furthermore, silicon dioxide can also be deposited, a technique which must be used when silicon dioxide is required on a non-silicon surface. This can be achieved using Plasma Enhanced Chemical Vapour Deposition (PECVD) with a tetraethylorthosilicate (TEOS) as a precursor in the following reaction [3, 10]

$$Si(OC_2H_5)_4 + 2H_2O \to SiO_2 + 4C_2H_5OH$$
 (1.3)

which is predominantly used to grow the oxide buffer layer during the local oxidation of silicon (LOCOS) [11]. It should further be noted that the deposition of alternative insulators, such as HfO^2 is typically performed using chemical vapor deposition (CVD) or atomic layer deposition (ALD) for advanced technology nodes.

1.1.2 Photolitography

The process of oxidation describes a way of growing a material on top of the wafer. To build complex structures, however, selectively removing regions and patterning the materials is essential in integrated circuit (IC) fabrication. This is achieved with the help of photolithography, the main steps of which are shown in Figure 1.1.

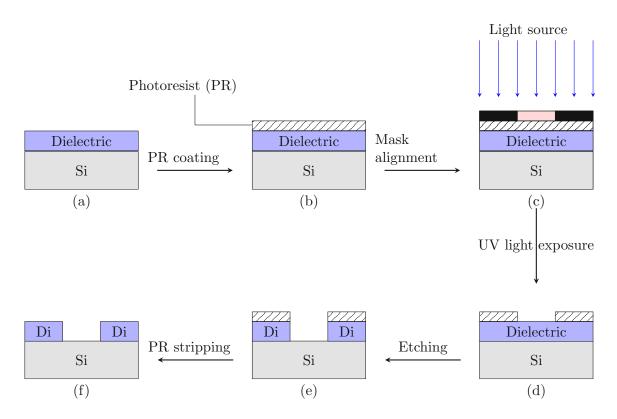


Figure 1.1: Illustration of the photolithography process sequence used to etch a dielectric layer in order to expose the silicon film. Reprinted from [12], with permission from Elsevier.

The process begins by coating the dielectric surface with a thin layer of a material which is sensitive to ultraviolet (UV) light. The film is deposited using spin coating, whereby the material is placed onto the surface in liquid form and spun to achieve uniform coating, as shown in Figure 1.1b. Following the coating, a short exposure to temperatures between 80°C and 100°C hardens the photoresist layer. In the next step, a mask selectively exposes parts of the photoresist layer to UV light. Based on the photoresist properties, parts of it are now easier to remove; essentially, the exposed part of the film either becomes soluble or is hardened depending if the photoresist is positive or negative, respectively. In Figure 1.1c, the dark part of the mask blocks the UV light while the pink segment lets the light through to the photoresist. In this case, the photoresist is "positive" meaning the exposed section becomes soluble and is subsequently removed by dipping in a solution. Once the photoresist layer is removed, as shown in Figure 1.1d, it must be hardened again to increase its resistivity to etching. To accomplish this, it is exposed to a temperature between 120°C and 180°C for around 30 minutes. In the subsequent etching step, the remaining photoresist layer protects the underlying dielectric, and only selected parts get etched away, as seen in Figure 1.1e. Finally, the remaining photoresist is taken away by exposing it to a chemical solution which targets it and does not impact the layers underneath or by oxidizing it [4, 13, 14].

The precision limit is dependent on the wavelengths of the applied UV light. Different processing techniques have been employed to improve precision. Nowadays, cutting-edge transistor nodes require extreme ultraviolet machines manipulating UV light with a 13.5 nm wavelength [15]. The precision is quantified by the value of the "pitch" which determines how close sequential features can be to each other without extensive smearing.

1.1.3 Etching

As noted in Section 1.1.2, etching is used for material removal and it is a critical step for patterning the substrate. Typically, a protective layer is deposited on top of the material to be etched to protect the sections which should remain in place. Once the wafer is patterned, it is exposed to the etchant species. One commonly used exposure method is *wet etching*, where the wafer is immersed in a liquid etchant solution resulting in a relatively cheap and easy way to etch the material, well suited when etching should be applied over the entire wafer surface of polysilicon, oxide, nitride, metals, or III–V compounds [15]. Since the etch uniformity is critical to achieving a minimum deviation in device performance, the wafer must not remain in the solution since the concentration of the chemical etchant at the surface might vary. The lack of uniformity is the reason spray etching has gradually replaced simple immersion into the solution. Spray etching ensures a consistent supply of etchant species at the surface and guarantees more uniformity across the wafer [14]. Wet etching is predominantly isotropic, i.e., the material is removed equally in all directions. Its isotropic nature becomes a problem when the thickness of the etched material is similar to the width of the material exposed to the etchant [13].

In addition to the limited precision, another downside of wet etching is the high amount of toxic chemical waste generated in the process. Another method of removing material is the process of *dry etching*, which can be highly directional (anisotropic) [13]. Dry etching is synonymous with plasma-assisted etching, which denotes several techniques which use plasma in the form of low-pressure discharges. Dry-etch methods include plasma etching, reactive-ion etching (RIE), sputter etching, magnetically enhanced RIE (MERIE), reactiveion-beam etching, and high-density plasma (HDP) etching [14]. Plasma is one of the four fundamental states of matter, describing a fully or partially ionized gas. It can be produced by applying an electric field which is strong enough to split the gas molecules into ions. These ions are then accelerated to etch away the target material. Plasma etching is widely used, especially at the advanced technology nodes, and the models developed in this work describe the underlying physics in more detail in subsequent chapters.

1.1.4 Film Deposition

Another frequently employed process is film deposition. IC fabrication requires depositing a broad range of materials on various surfaces. The deposition techniques can be divided into two main categories - physical vapor deposition (PVD) and chemical vapor deposition (CVD)[16]. The most commonly used PVD techniques are evaporation and sputter deposition, whereas CVD relies on a chemical reaction to produce a new material at the deposition site [3].

Physical evaporation can be used for easy-to-melt materials by mounting them on a filament made of a heat-resistant metal, e.g., tungsten [4]. Increasing the temperature of the filament evaporates the material and the vapor forms a film on a target wafer. Despite being easy to set up, physical evaporation has several limitations, such as film contamination with filament material, variation in the film composition in case of compounds, limitation in the thickness of the deposited film, as well as problems with forming a conformal layer [13].

During sputter deposition, the material which should be deposited is bombarded by ions, typically argon, Ar^+ . As the ions impinge the source material, they knock its particles out of the structure, and the released particles get transported to the substrate, where they adsorb onto the surface [17]. Sputter deposition can be used for the deposition of a wide variety of materials, including composites, where the deposited film has the same composition as the source and is conformal. However, topologies with sharp angles, trenches, or pillars are susceptible to shadowing during evaporation [4, 13].

Finally, during CVD, the substrate is exposed to a relatively high temperature, followed by the introduction of a gas containing the required precursor molecules. The molecules react with the substrate, depositing a thin film of the material. Depending on the precursor and substrate combination used, the reactions can occur through different mechanisms, such as thermal decomposition, pyrolysis, or reduction reactions. Although CVD is more complex and expensive to perform than PVD, it is frequently applied due to its ability to produce high-quality, uniform films with relatively precise control over its thickness and composition. Deposited material properties can be controlled by modifying the substrate temperature, the composition of the reaction gas mixture, and other experimental conditions [18]. For example, CVD can be performed at high pressures and temperatures, resulting in the deposited layer being highly conformal for various topologies [13]. On the other hand, using a precursor which strongly reacts with the surface will result in poor conformality in deep structures as most reactions will take place at the top of the structure, leaving fewer reactions at the bottom. This may result in the formation of a void or air gap in the deep feature.

1.1.5 Chemical Mechanical Planarization

As mentioned previously, since IC fabrication consists of many steps, the tiniest imperfections in a single step can lead to a chain reaction and severely impact the end-product performance and reliability. For example, light shines through the mask during photolithography, and lenses are used to manipulate the light. The focus of the light is maintained over a very small distance, and if unaccounted wafer surface deviations exceed this distance, the photoresist layer will be incorrectly exposed. The required high level of precision in the fabrication process brings about the need for a process that ensures wafer planarity. Chemical Mechanical Planarization (CMP) flattens the wafer surface by combining chemical and physical mechanisms. The mechanical part is grinding the substrate against a pad which carries a slurry with abrasive particles. The movement causes surface damage, loosens the surface material, and enhances the chemical reactions with the slurry while absorbing and carrying away the loose particles. The process is tailored to remove material from high points of the surface more effectively. Mechanical exposure could, in theory, produce the desired smoothening effect, but inevitably leads to undesired surface damage [3, 14].

1.1.6 Material Doping

Another essential step in IC fabrication is the doping of semiconductor materials, such as silicon, which can modify their properties and form a junction between p-type and n-type silicon. The doping process can be performed via diffusion of dopant particles from the surface of the wafer in either gaseous or liquid form or by using a previouslydeposited high dopant concentration [3]. Dopant particles subsequently diffuse from their initial position into the substrate under high temperatures, and typically one of the three following scenarios occurs:

- Substitutional diffusion dopant atoms move into vacant positions in the substrate's crystal lattice
- Interstitial diffusion the incoming dopant atom takes over already occupied lattice position and sends the substrate silicon atom to the interstitial position between regular lattice positions
- Interstitial diffusion the incoming dopant atom occupies an interstitial position between the regular lattice positions without displacing the substrate atom

A crucial parameter in controlling diffusion is the diffusion coefficient, which is exponentially dependent on the temperature. At increased temperatures, which typically range between 900°C and 1200°C for diffusion, the dopant atoms slowly move into the exposed silicon substrate. The diffusion takes place due to a large dopant concentration gradient at the substrate-to-doping material interface. Silicon oxide is also susceptible to diffusion, but the commonly used dopant atoms diffuse into it at significantly slower rates when compared to silicon.

An alternative to diffusion for substrate doping is *ion implantation*, a process which utilizes a particle accelerator to implant dopant atoms into the substrate. The main advantages over diffusion are [13, 14, 19]:

- Operation at reduced temperatures, which minimizes dopant movement in the substrate
- Wide variety of materials can be used as a diffusion barrier
- Any material which can be ionized can be implanted into the target
- Better control of the doping profile with a wider range of reproducible doses

Since the impinging high-energy ions inevitably damage the crystal lattice, ion implantation is typically followed by a thermal annealing step. Thermal annealing describes a heat treatment of the material with an appropriate combination of duration and temperature. Typically, rapid heating is followed by slow cooling to repair the damage and improve electrical and mechanical properties [19]. This step is also referred to as dopant activation since it ensures that the dopants are properly placed in the crystal lattice, where the charge donation or acceptance can take place. Additionally, the equipment is significantly more complex when compared to diffusion, and high dopant doses (>10¹⁶/cm³) are challenging to achieve in a reasonable time frame for production needs. However, the doping profile control and process flexibility established it as the main dopant introduction process for cutting-edge ICs [19]. It is also worthwhile to note that ion implantation is the process of choice when doping many novel semiconductor materials, like silicon carbide or gallium nitride, as diffusion would require too-high temperature to make it feasible.

1.1.7 Process Flow and System Integration

The most commonly applied processes in IC fabrication were briefly described in the preceding sections. An oversimplified typical process sequence which can be employed is provided in Figure 1.2. The processes are applied many times to generate ever-more complex structures.

As the miniaturization progressed and the complexity of fabricated structures increased, the planar design reached its physical limits. The industry started looking for solutions in the vertical dimension, which led to the introduction of the FinFET at the 22 nm technology node [20, 21]. In addition to scaling down the transistors, the focus shifted towards increasing the density of functionalities, where the term More-than-Moore came to prominence [22]. The idea here is to integrate different functionalities more closely, called heterogeneous integration. In addition to traditional memory and logic integration on the same die, radio-frequency (RF) circuits, sensors, and power electronics modules need to be connected [23]. The integration can be achieved on a chip level — System-on-a-Chip (SoC) and on the package level —System-in-a-Package (SiP). The vertical dimension can also be used for integration by stacking modules on top of each other (3D integration) [24].

Vertical integration is very promising since it reduces the total footprint, as shown in Figure 1.3 and decreases interconnect length, which improves performance without shrinking the individual transistors [25, 26]. In order to achieve vertical integration, modules need to be connected through the wafer. The connections are enabled by through-silicon vias (TSVs) — vertical interconnects consisting of a metal conductor and a thin dielectric layer at the silicon interface [27, 28, 29].

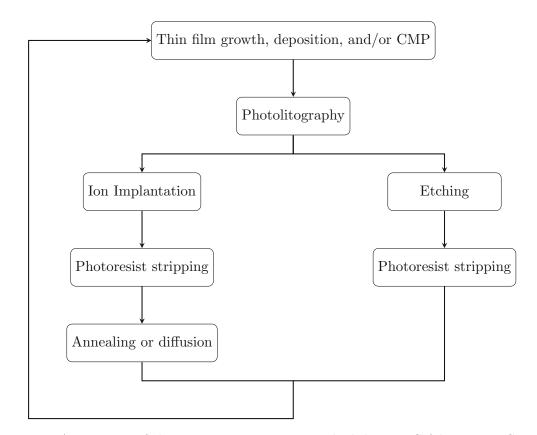


Figure 1.2: A sequence of the most common steps applied during IC fabrication. Starting with a silicon wafer, a layer of another material is deposited or grown, e.g., silicon dioxide, after which photolithography is performed to pattern the substrate. Removing the material via etching processes or doping the substrate follows, and the sequence is repeated many times to generate ever-more complex device structures.

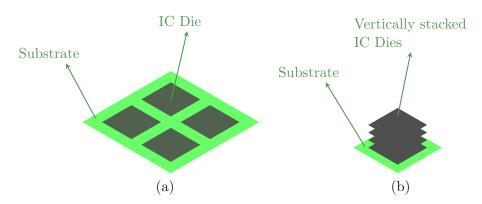


Figure 1.3: Illustration of the footprint difference associated with using a) two-dimensional (2D) over b) three-dimensional (3D) integration.

1.2 Role of TCAD

The structure of the semiconductor industry can be visualized as a pyramid [30], shown in Figure 1.4. The chain starts at the lowest level with suppliers of the wafer and electronic design automation (EDA) tools. TCAD belongs to EDA tools and is applied in a broad set of applications by semiconductor device engineers in designing process flows and devices. The device engineering is depicted on the second level of the pyramid. Engineers utilize TCAD tools to create, understand, and virtually test the design by understanding the simulated structures (process TCAD) and inspecting their mechanical, electrical, and other properties (device TCAD). This step is called virtual prototyping and requires well-calibrated models. The next level is integrated circuit design, where functional circuits are created by combining the designed processes and devices. The circuits are then manufactured, packaged, tested, and incorporated into the system with accompanying software. Finally, shown at the top of the pyramid, the product is placed on the market.

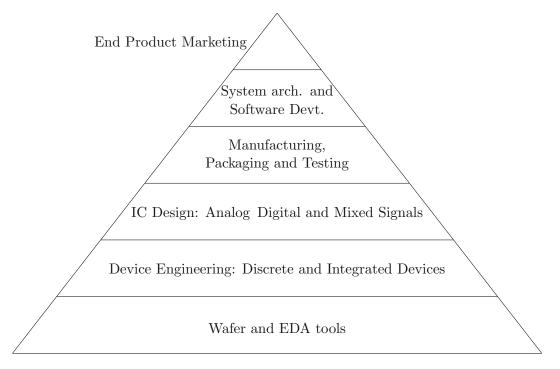


Figure 1.4: Illustration of segments of semiconductor industry in a pyramid hierarchy, adapted from [30]

As mentioned while describing the second level of the pyramid, TCAD is divided into two fields - process simulation, used to obtain the device geometry, and device simulation, which takes the geometry as an input to study and predict electrical, mechanical, and optical properties [31]. While many models used are physical and predictive, there are many challenges in the numerical simulation of processes and devices, and the results should not be blindly followed [30]. Utilizing TCAD can save significant time and resources by reducing the number of experimental runs required during the development stage [32]. The reduction is achieved by using physical models combined with numerical schemes to solve the equations describing the reactions. This way the process flows and device designs are optimized via virtual prototyping instead of running expensive and time-consuming experiments [33].

As the vertical dimension is utilized for both cutting-edge transistors advancement, e.g., FinFETs, stacked NanoWires [34], and gate-all-around FETs [35], and for integration and packaging [26, 36], the fabrication of high aspect ratio (HAR) geometries is becoming essential. As experimental testing of every required HAR structure would be incredibly expensive, process TCAD is extremely valuable in their development cycle. Plasma etching is among the most frequently applied fabrication steps in producing such structures. As with TCAD in general, capturing the underlying physics to provide a predictive model is complex, and the results must be carefully interpreted. However, physical models for plasma etching are the only viable means to avoid numerous trial-and-error procedures which inevitably come along with plasma etching due to its complexity [37].

1.3 Aim of the Thesis

As discussed in the previous section, TCAD is necessary in the product development cycle. To ensure that TCAD is optimally used, several software tools in this direction have been developed at the Institute for Microelectronics at TU Wien over the years. One of them is the currently under-development Vienna Process Simulator — ViennaPS [38], which provides a framework for physical modeling, including particle transport and their reaction with the simulated materials. The aim of this thesis is to further improve the framework and develop physical topography models which accurately replicate the physical phenomena observed during device fabrication. In this thesis, physical models for two different plasma etching chemistries are addressed: sfsix/O₂ and fluorocarbon CF_x. The final step is the application of the implemented sfsix/O₂ plasma etching model to study the impact of different mask shapes and materials on the final substrate geometry. Additionally, a compact model for process emulation is devised, which links experimental chamber parameters - pressure, feed gas composition and RF bias, directly to the final geometry, circumventing the simulation of particle transport.

1.4 Outline of the Thesis

The thesis is divided into six chapters and is organized as follows:

- Chapter 1 Introduction
- Chapter 2 gives an overview of process simulation and describes computational methods required to perform it.
- Chapter 3 provides a software implementation overview of the simulation framework used in this work.

- Chapter 4 discusses the theoretical background of the implemented physical models.
- Chapter 5 shows the results of the studies performed using the implemented models, as well as the resulting compact modeling.
- Chapter 6 summarizes the work and provides an outlook for potential next steps.

2 Process Simulation

This section begins with a brief description of the plasma reactor and the general modeling setting which enables the computational representation of semiconductor fabrication. Additionally, the computational methods required for representing physical and chemical reactions on the wafer surface are described.

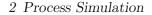
Since physical models for plasma etching are the main focus of this work, an example of an experimental setup required to physically perform this step is shown in Figure 2.1. The gas is fed into the chamber, where an RF bias through the inductive coil ionizes it and forms the plasma. At the bottom, the wafer is clamped by an electrostatic chuck (ESC) which holds it in place by inducing charge build-up at the wafer's surface, attracting electrostatic force. ESC is connected to another RF bias generator to make the ions hit the wafer. This bias creates pulses of ion bombardment and is used to control the process. At the bottom, the reactor is connected to a vacuum pump, which is also essential in sustaining and controlling plasma conditions.

Modeling physical and chemical reactions at the wafer surface means modeling material deposition and etching in the reactor. In process TCAD, to translate the experimental to simulation reactor setting, two different size scales are considered, namely reactor and feature scale, as shown in Figure 2.2. The interactions between the ions, molecules, and atoms in the chamber are considered in the reactor scale, which can often be ignored in the feature scale. The parameter considered to determine whether the inter-particle collisions can be ignored in the simulation is the mean free path of the particle in the ideal gas:

$$\bar{\lambda} = \frac{k_B T}{\sqrt{2\pi} d^2 p},\tag{2.1}$$

where k_B is the Boltzmann constant, T is the temperature, p is the pressure inside the reactor, and d is the collision diameter of the gas molecule [40].

Since the mean free path of the particles for most microelectronic fabrication processes is on the order of $\bar{\lambda} = 10$ mm, which is much smaller than the reactor region, the interactions between particles cannot be ignored when simulating the reactor scale, meaning that continuum transport equations should be applied to model the particle motion [2]. However, since the devices and wafer features simulated at the feature scale are much smaller than the mean free path, the particle-feature interactions are far more common than inter-particle collisions. The simulation of inter-particle interactions occurring in the reactor scale is a research field in its own right and is beyond the scope of this work. Nevertheless, as shown in Figure 2.3, the feature scale simulations require input from the reactor scale, primarily by defining the behavior of ions and molecules at the source plane, shown in Figure 2.2.



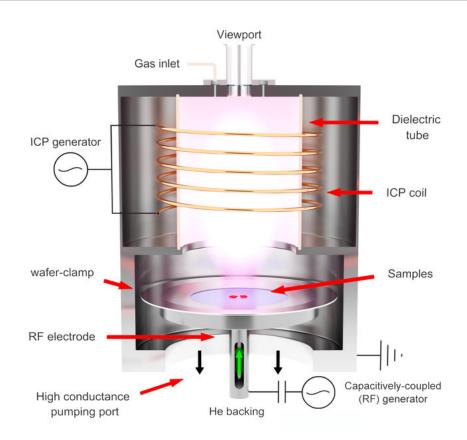


Figure 2.1: A schematic of the etching chamber of an Oxford Instruments PlasmaPro 100 inductively coupled plasma system. CC BY 3.0 [39]

The input particle fluxes that arrive at the source plane and are transported towards the feature scale must represent the reactor conditions - pressure, temperature, bias, and collisions; they are obtained either experimentally or by reactor scale simulations.

As noted earlier, since most of the etching and deposition reactions take place significantly below atmospheric pressure and the size of the patterns on the wafer are getting smaller ($<10 \mu$ m), the typical mean free path of particles defined in the Eq. (2.1) is smaller than the size of the fabricated structures [33, 41]. Therefore, it is reasonable to assume that particles in the gas phase adhere to the free molecular flow regime or ballistic transport. This assumption means that particles travel in straight-line trajectories, and the continuum transport equations, which govern the reactor scale transport, are no longer valid at this scale [41].

As shown in Figure 2.2 and Figure 2.3, the source plane is the starting point for particle simulations in the feature scale, which are then transported down to the surface under the assumption of ballistic transport. The transport is simulated using Monte Carlo ray-tracing methods. Subsequently, upon surface impact, existing knowledge from experiments or from molecular dynamics is utilized to produce a model which captures the physical and

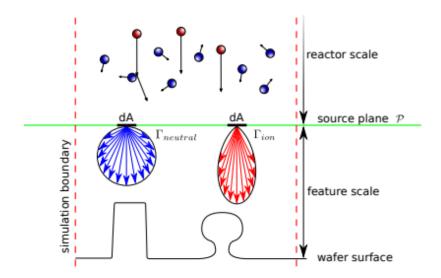


Figure 2.2: Schematic representation of the particle transport in the rector and feature scale regime. Reactor scale transport is governed by continuum transport equations which account for inter-particle collisions. The results of the reactor scale simulations serve as an input for the feature scale simulations through the source plane \mathcal{P} where ballistic transport is assumed, i.e., particles traverse in straight lines. CC BY 4.0 [42]

chemical reactions at the surface. The physical model is then calibrated and validated by fitting it to the experimental data and can ultimately be used for predictive modeling.

The simulation of a microelectronic fabrication process requires an accurate description of the topography of different materials and their interfaces. Since different fabrication steps will lead to complex topographies and surface deformations, numerically representing the surface movement to match the real-world conditions is crucial. The following subsections cover the fundamental building blocks of process simulation - surface representation and surface rate calculation.

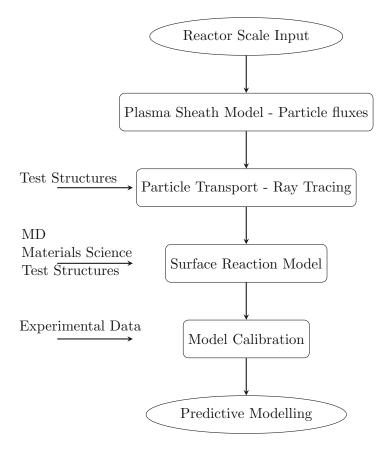


Figure 2.3: Strategy for developing and calibrating feature scale models. Adapted from [41]

2.1 Surface Representation

Based on the simulation task's requirements, choosing an appropriate surface representation is essential. The two main approaches in the context of process TCAD are an atomistic and a continuum approach, as shown in Figure 2.4 and Figure 2.5, respectively.

As the name implies, the atomistic approach considers individual particles which compose the material, making it the most rigorous physical description possible [2, 3]. Each material particle can be simulated using molecular dynamics, as noted in Figure 2.3, or statistically, using Monte Carlo methods [44]. The main issue with the atomistic approach is the simulation complexity. Accounting for each atom severely limits the time frame within which a simulation can be carried out, making it unfeasible to simulate a complete microelectronic device fabrication process [2]. However, atomistic simulations can be used to simulate reactions at the interface or at specific device regions [45]. The outputs of such simulations are valuable for models employing a continuum approach. Without a significant break-through in computing capabilities, the continuum approach is the only viable approach for longer time-frames required in the simulation of microelectronic fabrication [3], see Figure 2.6.

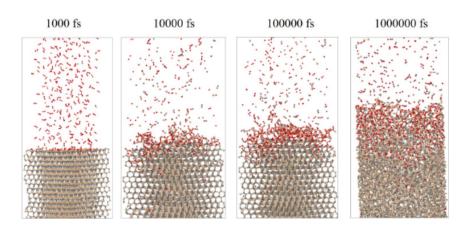


Figure 2.4: Example of a simulation using atomistic modeling. Each particle composing the material is represented. As shown above the pictures, the simulated process durations are expressed in femtoseconds and can span, in a reasonable computational run time, into the duration of microseconds. This limitation makes it impractical to simulate microelectronic fabrication processes directly. Figure from [43]

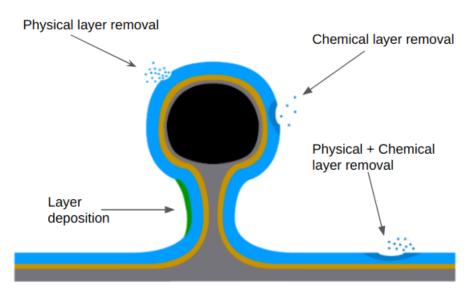


Figure 2.5: Illustration of the continuum approach in process TCAD, where materials are seen as bulk, meaning they occupy all the space between interfaces and are defined by material parameters and properties. Approximations made for the continuum approach make the process TCAD computationally feasible. Adapted from [42] CC BY 4.0.

While the atomistic approach accounts for individual particles and the region between them, the continuum approach views the material with bulk properties. The material is seen as a single entity that can be described with a single set of parameters [3, 47].

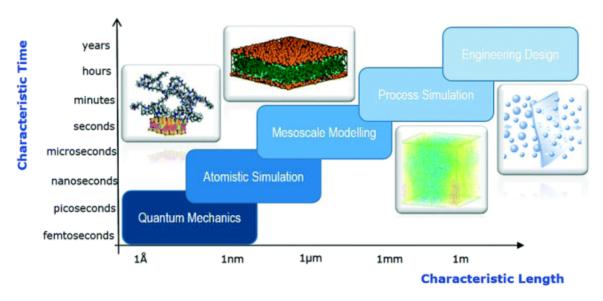


Figure 2.6: Approximate range of time and length scales covered by different modeling techniques. Process simulation spans from seconds to hours, while atomistic simulations at the longest up to microseconds. (Used with permission from Fermeglia et al., from [46]).

The approach chosen depends on the feature size and the required simulation time. If the size is significantly larger than the typical lattice, the surface should be represented as a continuum, which enables quick simulations for relatively large bodies during long simulation times. Along with the assumption that the material fills the entire space where its particles are present, two other significant issues need to be considered [3]:

- Material interfaces are abrupt and can be defined by an evolution of a single surface. This is known not to be true for some more complex processes, including oxidation.
- Material properties are homogeneous within the material region. Although this simplifies the process, it does not represent reality with rigorous accuracy.

Despite the drawbacks of the continuum representation of the material in process simulations, the speed and efficiency for determining material interfaces make it an indispensable modeling tool. Using the assumption that the material's physical properties are homogeneous and describing material interfaces as abrupt, is a sufficient assumption which allows to represent the entire material volume. In the following sections, two categories of continuum surface representation are covered - explicit and implicit.

2.1.1 Explicit Surface Representation

The most straightforward way to describe a topography is an explicit surface representation, whereby the surface elements are defined by a set of interconnected points. The name explicit stems from the fact that the stored points represent the actual location of the material surface. Figure 2.7a depicts an example of an explicit representation of a circle in two dimensions, next to the representation of a sphere in a three-dimensional space. The surface normals, essential for modeling surface movement, are facing outwards from the material. In two-dimensional (2D) representations, the surface elements are lines which connect the neighboring points, while the simplest element for three-dimensional (3D) surface representation is a triangle, as shown in Figure 2.7b.

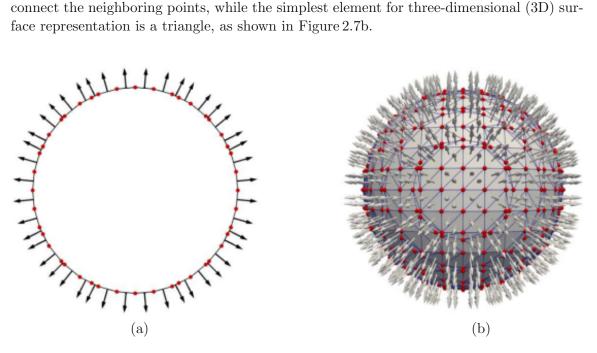


Figure 2.7: Examples of an explicit surface representation including the segments connecting the surface points and normals. a) a circle in 2D and b) a sphere in 3D. Figure from [2]

Explicit representation offers several desirable properties [48, 49, 50]:

- Theoretically, there is no limitation on the represented feature size
- Minimal memory requirements, since the number of elements is proportional to the total surface area
- Straightforward visualization, as the surface coordinates correspond to their point values in the representation
- Elements have easily determined sizes, which is useful when modeling volume phenomena, such as stress, arising from surface growth, e.g., in oxidation where the substrate grows underneath a mask
- Different materials can easily be represented by using material identifiers for surface segments

Due to these properties, explicit representation is widely used in applications such as graphics rendering and computer-aided design (CAD) [2, 51, 52]. However, two main

disadvantages bring issues to its application in process TCAD. Since the surface movement is achieved by shifting surface nodes based on their corresponding velocity, non-physical geometries can occur, as is demonstrated in Figure 2.8. The issue can be solved by creating a new mesh after each step, as seen in Figure 2.8b and Figure 2.8c, but the process is computationally inefficient and may negate the advantages of using explicit surfaces in the first place. The second issue is also related to surface movement. Namely, shifting the points will inevitably result in changes in the surface segments. The changes can lead to high aspect ratios or skewed mesh elements, shown in Figure 2.9, which do not align at the interfaces and lead to very poor mesh quality, leading to numerical errors. Poor mesh quality is problematic as it brings about the need for regular computationally expensive re-meshing.

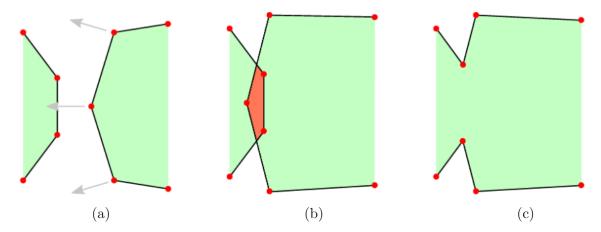


Figure 2.8: Example of a potential issue upon explicit surface movement. If two separate parts (a) move into one another, a non-physical structure may occur (b). The surfaces can be merged (c), albeit with a high computational price. CC BY 4.0 [42]

2.1.2 Implicit Surface Representation

For implicit surface representations, points on the surface are not directly stored in memory but are described by a function in a defined domain. The level set method, extensively used for numerical representation in process TCAD, is the most common implicit representation and is described in more detail in this subsection.

The level set method is a means to implicitly define a surface. The surface is determined using a signed distance function (SDF) $\phi(\vec{x})$ defined at each point in the spatial domain [53, 54]. The SDF is commonly defined on a Cartesian grid, and the distance values with their corresponding signs are defined for each point. The exact location of the surface is then found at locations where the SDF equals a specific scalar value. The value is typically zero, and in this case, the surface is said to be the zero level set. The SDF $\phi(\vec{x})$ is constructed based on the signed distance d of a domain point \vec{x} from the surface S bounding the volume V:

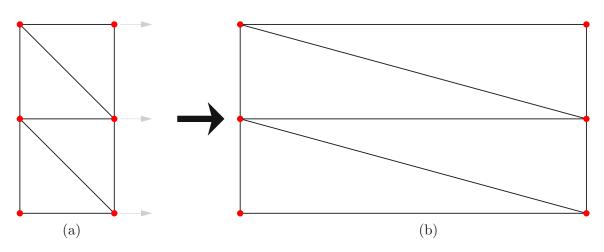


Figure 2.9: Explicit surface movement is defined by shifting the nodes. As the nodes shift, segments, e.g., triangles, are deformed and lead to a surface mesh of poor quality seen in (b).

$$\phi\left(\vec{x}\right) = \begin{cases} -d, & \vec{x} \in V \\ 0, & \vec{x} \in S \\ d, & \vec{x} \notin V \end{cases}$$
(2.2)

Using the SDF makes it straightforward to determine if a point is contained in the volume V or if it is located outside of it, based on the $\phi(\vec{x})$ function value sign. In order to determine the surface time evolution, the surface normal velocity $v(\vec{x})$ is used. Represented volumes typically have non-constant gradients of the SDF, which need to be used to normalize the velocity field $v(\vec{x})$. This normalization leads to the level set equation:

$$\frac{\partial \phi\left(\vec{x},t\right)}{\partial t} + v\left(\vec{x}\right) \left|\nabla \phi\left(\vec{x},t\right)\right| = 0.$$
(2.3)

Since Eq. (2.3) is a form of the Hamilton-Jacobi equation

$$\frac{\partial \phi}{\partial t} + H(\vec{x}, \nabla \phi, t) = 0 \quad \text{for } H(\vec{x}, \nabla \phi, t) = v(\vec{x}) \|\nabla \phi\|$$
(2.4)

and the function is defined on a regular grid, many algorithms exist which can solve it using various finite difference schemes [55, 56]. The resulting velocity is subsequently used to update the SDF $\phi(\vec{x})$. As the surface evolves, the points remain at the same position while their SDF value changes [42]. A comparison of implicit to explicit surface movement is shown in Figure 2.10. Producing non-physical geometries, a concern while using explicit representation, does not pose an obstacle with implicit surface representation as the points under consideration do not move; rather, their SDF function values are simply updated.

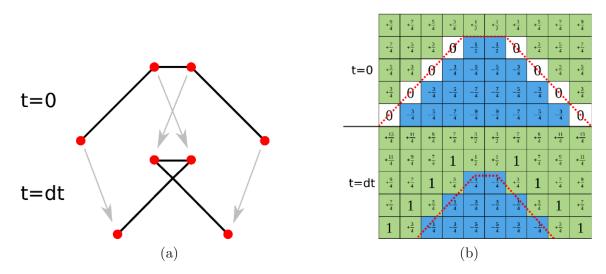


Figure 2.10: Comparison of surface movement using explicit and implicit representations. The node shifting results in a non-physical structure for explicit representation shown in (a). The same surface movement is performed using the implicit representation shown in (b). The numbers in the squares are the signeddistance-function (SDF) value for the grid points in the square centers. The dashed red line shows the real position of the surface. CC BY 4.0 [42]

2.2 Implicit Surface Evolution

As mentioned in the previous section, many methods exist to solve the level-set equation. This section covers the most frequently employed schemes in the Vienna Process Simulator ViennaPS. The level-set Eq. (2.3) is first initialized by populating the grid for time t = 0 using

$$\phi(\vec{x}, t=0) = \text{SDF}(\vec{x}). \tag{2.5}$$

Successful computation of the SDF function values at the next time step requires knowledge of the velocity at each grid point. To obtain the velocity at grid points, the velocity at the surface points v(s), where s denotes a point on the surface, must first be determined. The surface velocity is obtained by assigning the velocities in process emulation or from surface fluxes and rates in physical simulations described in the later sections. Once the velocity at the surface points is determined, the velocity field $v(\vec{x})$ can be obtained by calculating the velocity at each grid point \vec{x} . In process simulation, this velocity field does not represent a physical quantity; only the velocities at the surface have a physical meaning [57]. The main requirement for $v(\vec{(x)})$ is to be aligned with the velocity at the surface point to sustain a valid SDF throughout the surface evolution. The simplest way to extend the velocity to each grid point is to extrapolate it from the nearest point on the surface [58]. This extrapolation requires identifying the closest surface point for each grid point, which makes it very computationally expensive. Additionally, this procedure does not generally sustain the SDF. The approach used in process simulation, as described by Sethian [54], uses a fast marching method to determine the velocity field. The fast marching method is more computationally efficient and sustains the SDF analytically. Since discretization still brings errors, the SDF is re-initialized at regular intervals.

With the velocity field known, the level-set Eq. (2.3) can be solved in order to move the surface. As demonstrated in Eq. (2.4), since it is a form of the Hamilton-Jacobi equation, it can also be rewritten as

$$\frac{\partial \phi\left(\vec{x},t\right)}{\partial t} = -H(\vec{x},\nabla\phi,t). \tag{2.6}$$

Since the Hamiltonian is not time-dependent, the left-hand side is a temporal variable, and the right-hand side is spatial. To obtain an approximate solution at a grid point \vec{x} , the equation

$$\frac{\partial \phi\left(\vec{x},t\right)}{\partial t} = -H(\vec{x},\nabla\phi,t),\tag{2.7}$$

is solved by multiplying both sides by ∂t and integrating once to get

$$\int_{t}^{t+\Delta t} \partial \phi\left(\vec{x},t\right) \partial t = -\int_{t}^{t+\Delta t} H(\vec{x},\nabla\phi,t) \partial t.$$
(2.8)

Integrating the left-hand-side leads to

$$\phi^{t+\Delta t} = \phi^t - \int_t^{t+\Delta t} H(\vec{x}, \nabla \phi, t) \partial t, \qquad (2.9)$$

where the integral on the right-hand-side needs to be solved using numerical integration schemes, which simplifies the equation to

$$\phi^{t+\Delta t} = \phi^t - \Delta t \cdot \hat{H}(\vec{x}, \nabla \phi, t).$$
(2.10)

Here, the integral is calculated by computing the area under the function curve, e.g., taking an average value of the function $H(\vec{x}, \nabla \phi, t)$ in the interval $(t, t + \Delta t)$ and multiplying it by the interval duration. Many numerical schemes exist to approximate the area and compute the integral. Here, the two most frequently employed in ViennaPS: Engquist-Osher and Lax-Friedrichs schemes are briefly shown in their first-order forms.

Engquist-Osher, also known as the Upwind scheme, distinguishes between the scenarios where the surface moves towards and away from the point considered point. The integration of the Hamiltonian is performed in the following way:

$$\int_{t}^{t+\Delta t} H(\vec{x}, \nabla \phi, t) \partial t = \Delta t \cdot v(\vec{x}) \begin{cases} \partial_{i}^{+} \phi(\vec{x}), & v > 0\\ \partial_{i}^{-} \phi(\vec{x}), & v < 0 \end{cases},$$
(2.11)

where,

$$\partial_i^+ \phi(\vec{x}) := \frac{\phi\left(\vec{x} + \vec{e}_i\right) - \phi(\vec{x})}{\Delta x} \quad and \quad \partial_i^- \phi(\vec{x}) := \frac{\phi(\vec{x}) - \phi\left(\vec{x} - \vec{e}_i\right)}{\Delta x} \tag{2.12}$$

represent the *forward* and *backward* difference. This way, the computed gradient is adapted to and more relevant for the surface movement, which brings more accuracy than universally applying one of the schemes. Engquist-Osher of higher orders employs higher orders of finite differences to produce a more accurate integral evaluation, which requires more computational resources. Since the Engquist-Osher scheme is only stable for convex Hamiltonians, non-convex ones, which can appear in process TCAD, might lead to problems. In such cases, the Lax-Friedrich scheme can be employed, which is based on the central difference scheme for gradient computation, and the integration is performed via the following equation:

$$\int_{t}^{t+\Delta t} H(\vec{x}, \nabla \phi, t) \partial t = \Delta t \cdot v \nabla^{0} \phi(\vec{x}) - \Delta t \sum_{i=1}^{D} \alpha_{i} \cdot \frac{\partial_{i}^{+} \phi(\vec{x}) - \partial_{i}^{-} \phi(\vec{x})}{2}, \qquad (2.13)$$

where

$$\nabla^0 \phi(\vec{x}) := \sqrt{\sum_{i=1}^D \left(\frac{\partial_i^+ \phi(\vec{x}) + \partial_i^- \phi(\vec{x})}{2}\right)^2},\tag{2.14}$$

and

$$\alpha_i \ge \max_{\vec{x}} \left| \frac{\partial H}{\partial q_i} \right| \text{ with } q_i := \frac{\partial \phi}{\partial x_i}.$$
(2.15)

Based on the choice of the dissipation parameter α_i , the solution can be stable for nonconvex Hamiltonians. If α_i is too large, it leads to obsolete surface smoothing, while too small of a value might lead to numerical instabilities. Therefore, a proper choice must be made, which depends on the geometry and process which is being modeled.

Regardless of the integration scheme, moving a surface too far in a single step, i.e., more than a single grid spacing, might lead to a compounded approximation error and result in an unstable solution. Enforcing the upper limit to the time step is done using Courant-Friedrichs-Levy (CFL) condition. The CFL condition is used to adapt time steps using the following expression:

$$\Delta t = C_{\text{CFL}} \cdot \frac{\Delta x}{\max_{\vec{x} \in S} [v(\vec{x})]}.$$
(2.16)

Moreover, the C_{CFL} is chosen to be just under 0.5 in the ViennaLS [59] topography simulator to ensure the numerical stability of the solution while not being too restrictive on the time-step value. Too small of a value increases the number of iterations performed for a given simulation period, significantly increasing the computational run time.

This section covered the numerical methods used to move a surface. The assumption is that the surface velocity $v(\vec{s})$ is available as a base for all further calculations. The way this velocity is obtained is a distinguishing factor between process emulation and simulation and is essential for physical modeling.

2.3 Surface Velocity Calculation

Since the surface evolution is governed by the surface velocity which is calculated at every time step, the way the velocities are obtained is crucial for the simulation. A simple way is to extract geometric parameters from experimental data and change the surface accordingly. This is called process emulation. Each discrete section of the surface is assigned a velocity and moved accordingly, without modeling any physical processes. This makes emulation very computationally efficient. However, for predictive modeling and physical analysis, it is necessary to account for and describe physical and chemical reactions taking place at the surface.

As discussed at the beginning of this section, process modeling considers the feature-scale region, where ballistic transport of particles can safely be assumed. Experimental data or reactor scale simulation outputs are used as a starting point for the simulation in the form of particle fluxes. With the particle properties and the initial surface known, the next step is obtaining the particle fluxes on the surface and the kinetic energy of the incident ions. Particle fluxes on the surface are important for determining chemical reactions. At the same time, the kinetic energy of the ions can have a significant impact in the reactors operating under RF bias. The kinetic energy of neutral particles is assumed to have a negligible effect on surface evolution.

The total incoming flux at the surface point \vec{x} , labeled as $\Gamma_{in}(\vec{x})$ is composed of the particle flux arriving directly from the source and the re-emitted flux from other surface locations:

$$\Gamma_{\rm in}(\vec{x}) = \Gamma_{\rm src}(\vec{x}; q, \vec{\omega}, E) + \Gamma_{\rm re}(\vec{x}; q, \vec{\omega}, E) \tag{2.17}$$

With a few steps in between, the incoming flux is used to obtain the surface velocity. To calculate the total flux coming directly $\Gamma_{\rm src}$ from the source plane P, the entire source plane needs to be considered. The complete source plane is accounted for by adding all the individual contributions as shown in Figure 2.11.

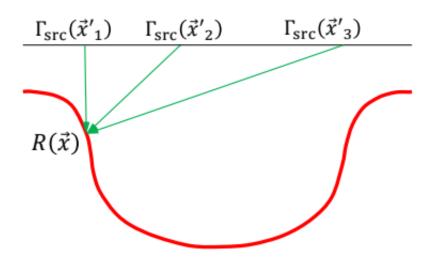


Figure 2.11: The surface rate $R(\vec{x})$ is computed by adding up contributions from all point sources at the source plane.

The resulting quantity is named a surface rate of a particle as it can represent either the total flux of the particle or, in the case of ions, the total sputter rate the particle caused. It is calculated by integrating over all the particle directions pointing toward the surface and over the entire area of the source plane. The mathematical expression follows

$$R(\vec{x}) = \int_P \int_{\vec{\omega} \cdot \vec{n}(\vec{x}) < 0} \Gamma_{\rm src}(\vec{x}; q, \vec{\omega}, E) Y(\theta, E) dP dE, \qquad (2.18)$$

where the term $Y(\theta, E)$ represents the sputter yield accounting for the impact of ions hitting the surface. This term is equal to one and it is neglected in the case of neutral particles based on the initial assumption that their kinetic energy is too low to sputter the surface material. The expression in Eq. (2.18) considers particles arriving from the source plane only. Therefore, it is necessary to extend the expression to include particles reflecting off another section of the surface and landing at \vec{x} .

$$R(\vec{x}) = \int_P \int_{\vec{\omega} \cdot \vec{n}(\vec{x}) < 0} \Gamma_{\rm src}(\vec{x}; q, \vec{\omega}, E) Y(\theta, E) dP dE + \int_S \int_{\vec{\omega} \cdot \vec{n}(\vec{x}) < 0} \Gamma_{\rm re}(\vec{x}; q, \vec{\omega}, E) Y(\theta, E) dS dE$$
(2.19)

A simplified version of this equation, and a more straightforward way of describing it is

$$R(\vec{x}) = \int_{A} \int_{\vec{\omega} \cdot \vec{n}(\vec{x}) < 0} \Gamma(\vec{x}; q, \vec{\omega}, E) Y(\theta, E) \mathrm{d}A \mathrm{d}E, \qquad (2.20)$$

where $\Gamma(\vec{x}; q, \vec{\omega}, E)Y(\theta, E)$ is either the source or the reflected flux and A stands for either the source plane P or the surface S. This expression effectively states that all incoming particles and their impacts must be accumulated to calculate the surface rate at a single surface point.

To calculate the rates $R(\vec{x})$, one needs to count the impacts of all the particles in the chamber which reach the surface S. Since this would be incredibly computationally expensive, Monte Carlo ray tracing is used for N_p particles to represent the total flux. Monte Carlo ray tracing is used to generate and simulate particle transport, as shown in Figure 2.12, by computing the intersection of the rays with the surface elements.

Since the surface is stored implicitly, representation must be adapted to compute the intersection. The conversion to a form of semi-explicit representation can be performed by spanning the lines in 2D or disks in 3D, with their normals based on the closest active grid point [60, 61], as illustrated in Figure 2.13. The point of impact for each simulated particle is the intersection of its ray and a discrete surface element from the semi-explicit representation.

Each simulated particle now represents a $\frac{1}{N_p}$ fraction of the total emitted particles. As long as the total amount of simulated particles is significantly larger than the total number of the surface elements, the resulting rates can be considered sufficiently accurate [2]:

$$N_p \gg N_{surface\, elements}$$
 . (2.21)

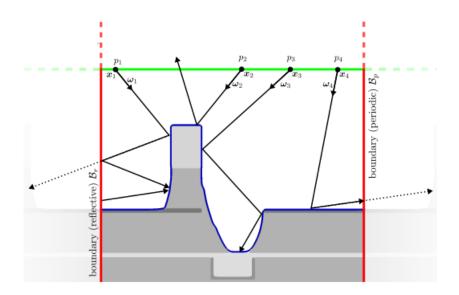


Figure 2.12: Schematic of the top-down flux calculation approach. With the particle properties and direction known, its trajectory is traced by computing the intersections with the surface elements. The particle may be reflected or terminated depending on the parameters used in the tracing process. Figure from [57].

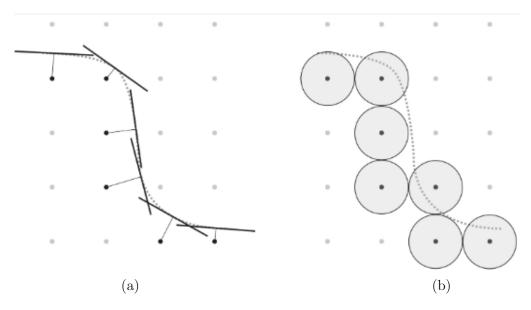


Figure 2.13: An example of a semi-explicit mesh. Since the surface is stored implicitly, there is no straightforward approach to compute the intersections of particle trajectories with the surface. Hence, from the closest active grid point, a normal is drawn to the surface where (a) a line in 2D and (b) a disk in 3D is spanned. Each of these disks is used as the area to compute surface rates at its corresponding grid point. CC BY 4.0 [42]

The change of the surface rate upon the impact is then given by

$$\Delta R(\vec{x}) = \frac{F^{tot}(\vec{x}) \cdot \Gamma(\vec{x}; q, \vec{\omega}, E)}{N_P \cdot A(\vec{x})},\tag{2.22}$$

where $F^{tot}(\vec{x})$ is the total number of particles arriving at surface location \vec{x} from the source plane:

$$F^{tot}(\vec{x}) = \int_{\mathcal{P}} \sum_{q=1}^{Q} F_q^{tot}(\vec{x}) \mathrm{d}A$$
(2.23)

As discussed previously, the flux of reflected particles also needs to be considered. Several methods exist to handle the reflected flux, such as generating new particles from the impact point or using a random number generator to determine whether the particle ray will be reflected. However, for brevity, only the method implemented in the process simulator used in this work is discussed. The reflection method used in this work is based on weight assignment. The reflected particles are addressed by assigning all particles a weight w. Upon each surface impact, the weight is decreased by a parameter called the sticking coefficient s. The sticking coefficient s is determined by the probability of the particle to stick to the surface material it impacts. Each particle is assigned a weight w = 1 upon its generation at the source plane P. Every time the ray hits the surface, it impacts it with a fraction of ws of the flux it represents. The reflected ray carries the remainder of the pre-impact weight $w_{new} = w - ws$. An example is given in the Figure 2.14 where a particle with a weight of w = 1 and a sticking probability s = 0.2 hits the surface and is reflected with the weight w = 0.8.

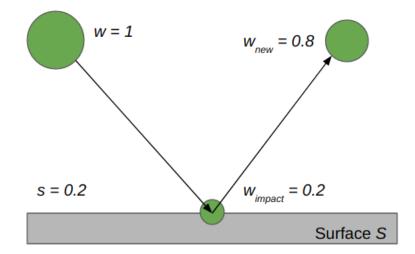


Figure 2.14: Illustration of a particle striking the surface and reflecting. Starting with a weight w = 1, the sticking coefficient s = 0.2 determines the impact weight of this particle. After the impact, the particle ray is traced further, with a reduced weight $w_{new} = 0.8$.

The change in surface rate is now given by

$$\Delta R(\vec{x}) = \frac{wF^{tot}(\vec{x}) \cdot \Gamma(\vec{x}; q, \vec{\omega}, E)}{N_P \cdot A(\vec{x})}.$$
(2.24)

Since N_p is the total number of simulated particles, the fraction

$$\frac{F^{tot}(\vec{x})}{N_p} \tag{2.25}$$

is the fraction of the physical particle flux which needs to be represented in our simulation. Therefore, multiplying it by the total physical flux $\Gamma(\vec{x}; q, \vec{\omega}, E)$ and dividing by the area $A(\vec{x})$ of the disk under consideration consideration, gives us the surface rate at the point of interest \vec{x} which is used in chemical reaction models at the surface.

It is important to note that this description of computing the surface rate addressed a top-down calculation, shown in Figure 2.12, where the particles are emitted from the source plane and traced toward the surface. Different approaches are possible, such as bottom-up [2, 57], but the description is left out since it is not applied within the scope of this work.

2.4 Surface Reflections

In the preceding section, surface reflections were discussed in the context of considering the reflected flux. The discussion focused solely on the weight of the reflected particle ray. Our attention now shifts to another crucial aspect of process modeling, namely the direction of the reflected rays. Based on the particle species and surface roughness, three types of reflections may occur - mirror, specular and diffuse, shown in Figure 2.15. Due to the directional nature of their movement, ions typically reflect specularly with a preferred direction. Neutral particles, however, more commonly reflect diffusely. Additionally, diffuse reflections are also prevalent when dealing with rough surfaces.

Having described the particle transport and surface rate calculation, all the necessary inputs for modeling the reactions at the surface are available. A typical process model involves different particle species, which requires computing surface rates for each. These rates are used in the surface chemical reaction models to obtain the surface velocity.

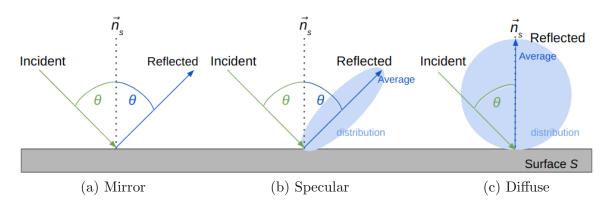


Figure 2.15: Illustration of three reflection types; (a) mirror reflection, where the incident angle is equal to the reflected one, (b) specular reflection, where particle reflections follow a distribution centered around the reflected angle equal to the incident angle, and (c) diffuse reflection, where particles are equally likely to go in any direction away from the surface, centered around the surface normal.

2.5 Chemical Modelling

In the previous section, the process of computing surface rates was described. Here, a framework for modeling the surface reactions is defined. Calculating the surface reaction rates of each particle and plugging them into the surface kinetics model produces the velocities, which are then used to move (or advect) the surface [62]. The processes on the surface are described by coefficients which are calibrated to a specific technology based on previously fabricated structures [63]. The considered processes are:

- Chemical etching
- Ion-enhanced etching
- Sputtering
- Deposition

These processes have already been described in 1.1, but a brief review of their meaning in the simulation context is given here. Chemical etching occurs when etchant particles bind to the surface particles and eliminate them from the surface. Next, ion-enhanced etching occurs when a chemical etchant has bound to the surface particles, but the resulting molecules do not have enough energy to leave the surface. Impinging ions transfer energy to these molecules, eliminating them from the surface impact point. Additionally, the incoming ions break existing bonds and enhance the creation of etch products. Similarly, ion sputtering occurs when the impinging ions hit the surface, transfer their energy and physically remove material from the top layer. Lastly, deposition, as the name implies, occurs when the impinging particles chemically react with the surface and form new layers on the top of the surface.

Each of these processes can have different properties described by the coefficients used to calibrate the model to the technology. The coefficients will be briefly discussed in the following paragraphs. To simplify modeling, the rates obtained in the simulation each represent a group of particle types, where each group might be composed of many different chemical species. The categorization is performed based on the impact on the surface. As shown in Figure 2.16, the rates usually describe neutral etchant particles, passivating particles, passivation etchant particles, and ions [42]. The rates of particle types impinging on the surface can also be used to compute surface coverages of different particle types, ϕ_x , where x is a particle type. Hence, coverages of etchant ϕ_e , polymer ϕ_p , and polymer etchant ϕ_{pe} describe the amount of material covering the surface. The coverages can be used with surface rates to obtain the expression for surface velocity. Pseudo steady-state conditions are assumed, meaning that during the time-step, any surface movement is considered to have no impact on the calculation. The assumption is sensible since the incoming particles are significantly faster than a surface movement during a single time step, which equals around several nanometers per second [37]. This allows us to assume that pseudo steadystate conditions have been reached, meaning the following system of equations describes surface processes:

$$\frac{d\phi_e}{dt} = \Gamma_e S_e (1 - \phi_e - \phi_p) - k_{ie} \Gamma_i Y_{ie} \phi_e - k_{ev} \Gamma_{ev} \phi_e \approx 0$$
(2.26)

$$\frac{d\phi_p}{dt} = \Gamma_p S_p - \Gamma_i Y_p \phi_p \phi_{pe} - \Delta_p \approx 0 \tag{2.27}$$

$$\frac{d\phi_{pe}}{dt} = \Gamma_e S_{pe} (1 - \phi_{pe}) - \Gamma_i Y_p \phi_{pe} \approx 0$$
(2.28)

Equations (2.26), (2.27), and (2.28) relate the mentioned physical processes to the change in the material coverages. The build-up or removal of the material means the surface will move. The individual terms corresponding to different processes are comprised of coefficients mentioned at the beginning of this section, which describe the process. Γ_x denotes the respective arriving fluxes on the surface element, S_x the respective sticking probabilities, Y_x the yields (e.g., etching or sputtering yield), and k_x are the stoichiometric factors, which describe how much of a material, compared to its reactant, is needed to form the reaction product. Sticking probabilities and coverages are bound to the range [0, 1], where 1 denotes a fully covered surface, or fully balanced polymer by etchant in the case of ϕ_{pe} , since this coverage is normalized to ϕ_p . Δ_p represents the material flux deposited or etched from the surface. On the very left of each equation, the change in the coverage over time is given. It is equal to the sum of the incoming and leaving particle fluxes. From the left, the first term on the right-hand side shows the incoming flux of chemical particles adsorbed to the surface, represented by Γ_e and the sticking probability. Note that the sticking probability is also influenced by the coverages in Eq. (2.26) and (2.28). The next terms to the right in all three equations represent ion-enhanced etching and sputtering, respectively, which may remove all types of particles from the surface. Next, the third term in the Eq. (2.26)

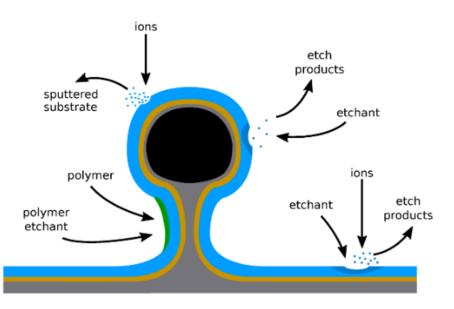


Figure 2.16: A schematic showing the processes to be simulated. Material directly exposed to ion impact gets sputtered away due to the kinetic energy the ions bring. On the sidewalls, hidden from the direct impact, a passivating layer can form, shown in green. Next, chemical etching occurs due to the formation of etch products of low binding energy upon the interaction of the incoming chemical etchant with the surface. If the chemically-modified surface is exposed to ions, ion-enhanced etching occurs, which speeds up the formation of etch products and the film removal by physically breaking the existing bonds. CC BY 4.0 [42]

represents the removal of surface material by evaporation or chemical etching. This term is only relevant for the etchant particles since they chemically react with the top surface layer to form compounds that are, in turn, easier to remove due to significantly lower surface binding energy [64]. The third term in Eq. 2.27 represents the flux of removed or deposited top-layer polymer. With all the mechanisms accounted for, adding them together should be equal to zero on the material due to the conservation of the total mass in the system.

Since plasma etching chemistries are the main topic of interest in this work, a generic velocity for that setting is of interest. This is obtained by assuming that the surface movement is governed by chemical and ion-enhanced etching, as well as physical ion sputtering, the velocity can be computed using the following expression:

$$v(\vec{x}) = \frac{1}{\rho_{sub}} \left[\underbrace{\Gamma_{ev}\phi_e}_{\text{chemical etching}} + \underbrace{\Gamma_iY_{ie}\phi_e}_{\text{ion - enhanced etching}} + \underbrace{\Gamma_iY_s\left(1 - \phi_e\right)}_{\text{ion sputtering}} \right]$$
(2.29)

With the theoretical part completed and the process of moving the surface elaborated, in the next section the software implementation of the process simulator ViennaPS is described.

3 Software Implementation

Several software tools for process TCAD have been developed at the Institute for Microelectronics at TU Wien. One of them is ViennaLS, a level-set-based topography simulator for the simulation and emulation of microelectronic fabrication processes. As discussed in previous sections, topography simulation is only one part of process simulations. A new software package, ViennaPS [38], is in development for encapsulating all required tools for a full process simulation and emulation flow. In the scope of this work, the initial software design was generated to combine the existing material simulation class with ViennaRay and ViennaLS in order to provide an easy-to-use and robust interface for the user. In addition, minor contributions were made to the initial software implementation and many bugs were identified and fixed en route to making the physical models able to replicate the experiments. Hence, this chapter is dedicated to providing an overview of the ViennaPS software, a schematic of which iis provided in Figure 3.1.

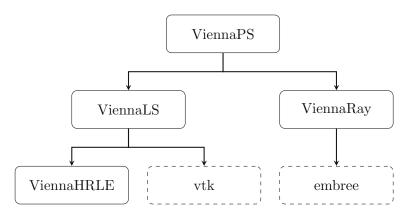


Figure 3.1: A scheme of ViennaPS dependencies - ViennaLS is used for topography simulation and ViennaRay for Monte Carlo ray tracing. ViennaRay is based on Intel®'s ray tracing kernel Embree, while ViennaLS uses the library ViennaHRLE for efficient data storage and the vtk library for visualization.

3.1 ViennaPS

The ViennaPS library is a wrapper around the topography simulator ViennaLS [59] and the ray tracing library [65] with further extensions which allow volume modeling for processes such as ion implantation. Also, the user can pass custom classes for physical models, ray tracing, and velocity fields. The idea here is to have a class which encapsulates the simulation domain and can execute different types of processes on it. As illustrated in Figure 3.2, different process models can be passed to the overarching *Process* object, which holds a handle to the simulation geometry and domain and contains parameters such as simulation time and number of rays per point. Physical or geometrical models can be used for the *Process Model*. Each *Process Model* contains surface and particle models. Surface and particle models give information which is required to perform ray tracing and move the surface. In order to enable process emulation, not specifying particles in a given process model circumvents ray tracing. This way, a pre-defined velocity field for the surface model can be directly applied to the geometry.

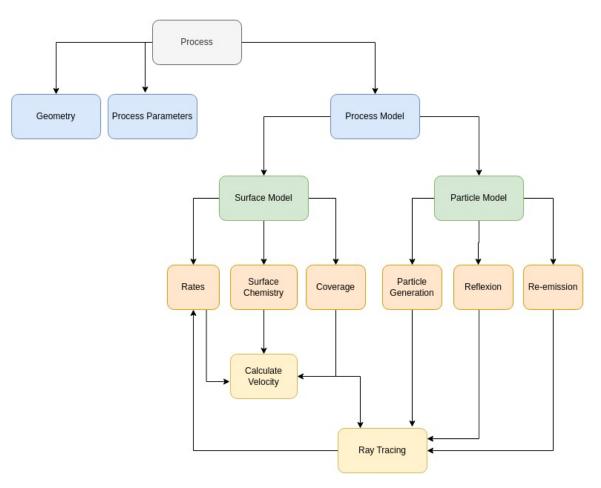


Figure 3.2: Conceptual design of ViennaPS. The main, *Process* object contains all the simulation domain data and can be used to apply different physical models.

The way this conceptual design was implemented is shown in Figure 3.3, and a brief explanation of each class is given in the following paragraphs.

psProcess serves as the main simulation interface. It encapsulates the simulation domain, the process model, the process duration, and the necessary ray-tracing parameters: It also contains the methods required to set them. Once the mentioned attributes are set, the

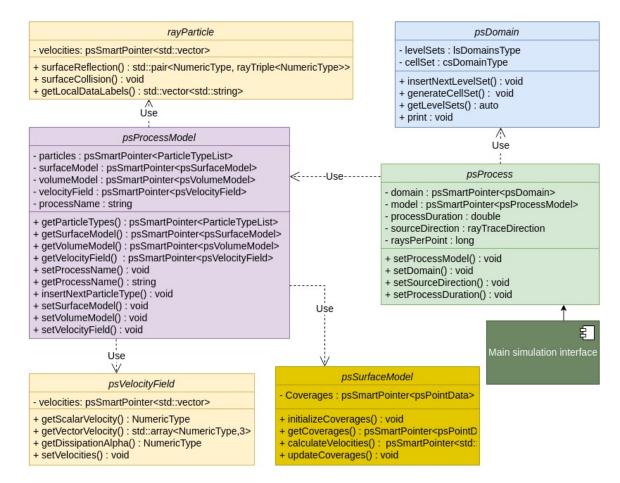


Figure 3.3: Specification diagram of ViennaPS including main classes used in process simulation and the most relevant subroutines. The *rayParticle* class serves as an interface for ray tracing. *psDomain*, which stores the simulation domain, is composed of, among other members, one or more instances of *lsDomain*, which belong to the dependency ViennaLS.

method apply() is used to perform the process and run the simulation. One of the objects it needs to use is of class *psTranslationField* which translates the velocity field from the surface to the level set points.

psDomain is a class which represents all materials in the simulation domain. The materials are stored as level sets, when describing surfaces, and cell-based structures, when describing volumes. The description of the latter is omitted here due to being out of the scope of this work. Cell-based structures are needed for processes such as diffusion and ion implantation, while level-sets suffice for plasma etching and other topography processes.

psProcessModel enables the user to describe a specific process occurring in the simulation domain. This means that the user needs to set the attributes to describe a custom process.

The attributes are pointers to a list of particles for which ray tracing is performed, the surface model, and the velocity field, all described in the following sections.

psSurfaceModel serves as a blueprint for describing surface chemistries. Effectively, the user creates a custom child class and specifies how the coverages evolve based on the rates at which particles impinge on the surface. The description of surface coverage evolution is contained in the method updateCoverages. Next, psSurfaceModel contains the method calculate Velocities, which uses the data obtained by ray tracing to return the velocities by which the surface should be advected. The method getCoverages() returns the coverage data, while the method initializeCoverages() is used to initialize the vector containing the coverage data. The underlying assumption is that they are in equilibrium. One can define the appropriate container size containing a value of 0 at each surface point and perform ray tracing until equilibrium is reached. Based on our experience having performed many simulations to date, the number of iterations it takes to reach an equilibrium is around 10, however, it is implemented to be easily customized.

psVelocityField serves as an interface for a velocity field used during advection. It holds a vector of velocities. The method getScalarVelocity() takes surface coordinates as arguments and returns the corresponding scalar velocity. Next, the method getVectorVelocity()does the same but returns the velocities along each coordinate direction. Lastly, getDissipationAlpha() is linked to the advection method used. If a Lax-Friedrichs scheme is used, the function helps to provide a stable solution.

With this implementation, the user can run the process by performing the following steps:

- Create the domain
- Create the surface model
- Define the particles (optional)
- Define the process model and set the surface model and particles in it
- Define the process and set the process model, domain, and ray tracing parameters (opt.)
- Apply the process on the domain

The option to perform process emulation is activated if no particles are passed to the *psProcessModel*, which sets a flag to circumvent ray tracing, so the surface is advected using the predefined velocity field. If one or more particles are passed, ray tracing is enabled and performed using the ViennaRay [65] library described in the following section.

3.2 ViennaRay

Flux calculations required by the ViennaPS are performed in a top-down Monte Carlo flux calculation library ViennaRay. The library is based on Intel®'s ray tracing kernel Em-

bree. It is designed to provide efficient and high-performance ray tracing while maintaining a simple and easy-to-use interface [65]. Using the concepts described in Section 2.3, ViennaRay is interfaced via instances of the class *rayParticle*, which serves as a blueprint for user-defined particles to ensure compatibility for ray tracing. Custom particles to be traced must inherit from this class and overwrite the necessary methods. The function *initNew()* initializes a new particle, and it is called every time the particle is traced from the source plane. The functions specifying particle properties are *surfaceCollision()* and *surfaceReflection()*. They describe the impact produced by a particle upon hitting the surface and how it reflects from it. Next, since a single particle type can contribute to different types of surface rates and coverages, *getRequiredLocalDataSize()* is used to determine the number of different rates affected by the particle type. To retrieve a surface rate for the subsequent velocity calculation, *getLocalDataLabels()* allows access to the rates by name.

ViennaRay can also be used as a standalone library with custom-designed geometries. However, it is developed and optimized for use with ViennaLS, described in the following section, which provides the necessary geometry representation.

3.3 ViennaLS

ViennaLS serves as a basis for process simulation. It applies the surface representation concepts described in Section 2.1 to perform topography simulations using level sets. It stores the level-set surface and provides all the necessary algorithms to initialize the geometry, manipulate the level-set values according to a velocity field, analyze surface features, and convert the LS to other material representations commonly used in device simulators [2]. Classes which serve as an interface to ViennaPS are:

- lsDomain()
- lsAdvect()

An instance of the class lsAdvect() is contained in the psProcess object described in Section 3.1. It contains the level sets, the velocity field, the integration scheme for advection, and other tools needed to manipulate the level sets which it contains as objects of the class lsDomain(). Objects of a class lsDomain() contain all the necessary data to describe the surface in a simulation space, the grid, its extents, and the boundaries of the simulation space, as well as the level set values of the surface. The level set values are stored in an optimized container provided by the ViennaHRLE library, briefly discussed in the following section. Instances of lsDomain() can be combined to provide multiple layers and represent different materials, enabling different surface reactions during process simulation.

3.4 ViennaHRLE

In Section 2.1.2, a signed-distance-function was defined at each grid point. As the CFL condition dictates that surface movement must be limited to less than a grid spacing, it is clear that not all grid points are necessary in every iteration. Therefore, considering a

narrow band of points in the vicinity of the surface is sufficient for surface movement [66]. The challenge arising from this approach is storing this irregularly spaced sparse data set in a way that utilizes the chance to improve performance over the approach of storing all grid points. Algorithms operating on the level-set typically iterate over the entire surface in a single pass, making fast sequential access a requirement for performance [2]. The ViennaHRLE library [67] is a dependency in ViennaLS to provide a container for fast access to sparse level set data. This is achieved via a hierarchical run-length encoded (HRLE) data structure [2, 68]. In a nutshell, the grid is segmented in each direction and encoded by run lengths. The segmentation and encoding allow a set of consecutive neighboring points with a similar SDF value to be described as a single entity. Now the points outside the narrow band considered for the surface movement can be grouped together and quickly skipped when iterating over the grid, which significantly reduces the iteration time[68]. A detailed library description is provided in [2, 33].

4 Physical Models

In Section 1.1, the significance of the vertical dimension in the microelectronics industry for integrating functionalities beyond memory and logic on the same die was discussed. This approach is called More-than-Moore [69] and it requires complex circuitry and interconnects throughout the entire wafer thickness, which can be several hundred micrometers deep. The large depth brought about the need for through silicon vias (TSVs) which are used to create these connections [28, 27, 70]. Due to the anisotropy that plasma etching offers, it is typically the method of choice for TSV fabrication. Additionally, plasma etching is also the process used for the fabrication of modern three-dimensional (3D) NAND-based memory. The memory capacity is limited by the number of stacked conductive and insulating layers forming the NAND gate. These gates are typically fabricated by etching through silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) stacks [71]. Using more stacks would increase the capacity, but the current limit is 128 [72]. This limitation is mainly due to not being able to fabricate a structure with a higher aspect ratio. Hence, detailed understanding of plasma chemistries is needed to create further inroads in this direction. The physical models accelerate the research by significantly reducing the number of experimental trial-and-error procedures. Two chemistries are discussed in the following subsections. The first is SF_6/O_2 , commonly used in the deep reactive ion etching (DRIE), also known as the Bosch process, to generate HAR structures. The second chemistry is a fluorocarbon plasma, which is highly suitable for etching through silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) due to its high selectivity over Si etching [73, 74] as well as SiO_2 over SiN_x [75, 76].

4.1 SF₆/O₂ Plasma Etching

To describe the feature scale simulation of SF_6/O_2 plasma etching, the surface rates of both ions and neutral particles, specifically fluorine and oxygen, and the surface coverages of neutrals, are considered. As discussed in Section 2, ray tracing is used for the calculation of the surface rates, which are used for calculating coverages during each time step. The two quantities for each particle type eventually lead to the surface velocity, addressed here as the etch rate (ER). The ER known at all surface points can be extended to all grid points needed for surface advection to solve the level set Eq. (2.3). Three physical phenomena determine the ER:

- Chemical etching
- Physical sputtering
- Ion-enhanced etching

In the process of chemical etching, the fluorine from the SF_6 species reacts with the exposed silicon surface. Many different chemical reactions take place, which are obtained using the Gibbs energy minimization, as described in [77]. However, here only the most prevalent species for silicon etching with SF_6 gas are presented [78]. Both reaction products are volatile which makes them readily desorb from the surface. The reaction between silicon and SF_6 is given by:

$$\operatorname{Si} + 2\operatorname{SF}_{6(g)} \longrightarrow \operatorname{SiF}_{4(g)} + 2\operatorname{SF}_{4(g)}$$

$$\tag{4.1}$$

Next, physical sputtering is caused by high-energy ions impacting on the surface. Due to an applied bias, ions strike the wafer surface with a high enough kinetic energy, $E_{ion} > E_{th}$ to break the existing bonds in the silicon wafer or other exposed materials.

Lastly, ion-enhanced etching, also known as reactive ion etching (RIE), combines the two previous effects. Since silicon surfaces which are saturated with fluorine are more prone to physical sputtering, the threshold energy for releasing the silicon atom E_{th} is significantly reduced compared to non-fluorinated surfaces. Therefore, ion-enhanced etching provides an etch rate which is larger than the sum of the chemical etching and sputtering.

The surface can be covered in fluorine or oxygen. The physical model keeps track of these coverages, given by θ_F and θ_O , respectively, by calculating the flux-induced rates and considering the coverages from the previous time step. They are calculated with a Langmuir–Hinshelwood-type surface site balance equations [79], given by:

$$\sigma_{Si} \frac{d\theta_F}{dt} = \gamma_F \Gamma_F \left(1 - \theta_F - \theta_O \right) - k \sigma_{Si} \theta_F - 2Y_{ie} \Gamma_i \theta_F \tag{4.2}$$

$$\sigma_{Si} \frac{d\theta_O}{dt} = \gamma_O \Gamma_O \left(1 - \theta_F - \theta_O \right) - \beta \sigma_{Si} \theta_O - Y_O \Gamma_i \theta_O \tag{4.3}$$

The term σ_{Si} represents the density of silicon at the surface point \vec{x} which is not included in the equations for legibility; Γ_F , Γ_O , and Γ_i are the emitted fluorine, oxygen, and ion fluxes, respectively; γ_F and γ_O are the sticking coefficients for fluorine and oxygen on a non-covered silicon substrate, respectively; k is the chemical etch reaction rate constant; β is the oxygen recombination rate constant; and Y_{ie} and Y_O are the total ion-enhanced and oxygen etching yields, respectively. Y_{ie} and Y_O are yield functions which are dependent on the ion energies in the reactor [33].

Since the surface movement is significantly smaller than the considered fluxes, it can be assumed that it does not impact the calculation. With this assumption of a pseudo-steady-state, Eq. (4.2) and (4.3) can be set equal to zero, resulting in the following surface coverage equations:

$$\theta_F = \left[1 + \left(\frac{k\sigma_{Si} + 2Y_{ie}\Gamma_i}{\gamma_F\Gamma_F}\right) \left(1 + \frac{\gamma_O\Gamma_O}{\beta\sigma_{Si} + Y_O\Gamma_i}\right)\right]^{-1}$$
(4.4)

$$\theta_O = \left[1 + \left(\frac{\beta \sigma_{Si} + Y_{ie} \Gamma_i}{\gamma_O \Gamma_O} \right) \left(1 + \frac{\gamma_F \Gamma_F}{k \sigma_{Si} + 2Y_{ie} \Gamma_i} \right) \right]^{-1}$$
(4.5)

The reason that pseudo steady-state can be assumed is that the incoming fluxes of all involved particles are in the order of $10^{16}-10^{19}$ cm⁻¹s⁻¹, which is significantly larger than the surface etch rate ER, which is typically in the range of several nanometers per second [37]. The oxygen particles do not take part in surface removal; instead, they occupy an area on the top surface layer and inhibit the effects of chemical etching by fluorine. Relating it to the parameters in the equation, the presence of oxygen (denoted by its flux Γ_O) tends to reduce θ_F , as can be seen in Eq. 4.4. Increasing the oxygen flux Γ_O increases the overall expression in the square brackets, which means θ_F decreases. Since oxygen has a passivating effect, the etching of silicon proceeds only due to its reaction with fluorine and physical sputtering due to the incoming ion flux. At locations where oxygen coverage is high, only ion sputtering takes place. This brings us to the expression for the etch rate (ER), which is used to move the surface

$$ER = \frac{1}{\rho_{Si}} \left(\frac{k\sigma_{Si}\theta_F}{4} + Y_p\Gamma_i + Y_{ie}\Gamma_i\theta_F \right), \qquad (4.6)$$

where ρ_{Si} is the silicon density. The first, second, and third terms in the brackets of Eq. (4.6) represent the chemical etching, physical sputtering, and ion-enhanced etching, respectively, analogous to the equation provided in Eq. (2.29).

4.1.1 Model Validation

The described model was implemented in ViennaPS and calibrated to the experimental data from Belen et al. [63] to ensure the simulations correctly replicate the changes in chamber parameters, mainly: Feed gas composition, applied bias, and chamber pressure, as well as changes in the geometry. The fluxes of the neutral species, i.e., fluorine Γ_F and oxygen Γ_O , are varied to replicate the feature changes caused by feed gas variation. The applied RF bias is modeled by assigning energy to the ions. The chamber pressure is implicitly modeled by matching the simulated profiles to the experimental ones from literature and varying the fluxes accordingly. Using these approaches, 3D simulations of SF₆/O₂ plasma etching with 0.35 µm diameter holes using a 1.2 µm thick oxide mask were performed to match the experimental setup with the parameters provided in Table 4.1. Relevant process parameters were then fitted to replicate the experiment by matching the simulated profiles to the scanning electron microscopy (SEM) profiles provided by Belen et al. [63]. The simulation parameters which resulted in the best fit to the SEM profiles resulting from the feed gas variation are given in the Table 4.2.

The outputs of 3D simulations using the parameters from Table 4.2 are shown in Figure 4.1. The resulting structures show that the model is able to capture complex phenomena. The increase in oxygen fraction in the feed gas leads to an increase in the vertical

Table 4.1: Chamber parameters for the experiments carried out by Belen et al. [63]. Fluxes were varied in the simulation to replicate the impact of the changes in gas composition and pressure.

Process Parameter	Value
Pressure	$10 - 45 \mathrm{mTorr}$
Total gas flow rate	80sccm
Inductive coil power	$800 \mathrm{W}$
RF-bias voltage	-20 V, -120 V
Wafer temperature	$5^{\circ}\mathrm{C}$
O_2 fraction in feed, y_{o_z}	0.44 - 0.62

Table 4.2: Simulation parameters used for achieving the best fit to the profile variations observed in the gas composition variation study. The simulation settings replicate a chamber with a total gas flow rate of 80 sccm at a pressure of 25 mTorr, an inductive coil power of 800 W, and an RF-bias voltage of -120 V at a wafer temperature of 5°C. The flow rates of SF₆ and O₂ gases were varied. The fraction of O₂ in the total 80 sccm is shown in the table.

Parameter	Oxygen fraction in feed gas y_{O_2}			Unit	
	0.44	0.5	0.56	0.62	
Fluorine flux Γ_F	$5.5{ imes}10^{18}$	$5{ imes}10^{18}$	$4{\times}10^{18}$	$3{\times}10^{18}$	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Oxygen flux Γ_O	$2{ imes}10^{17}$	$3{ imes}10^{17}$	$1{\times}10^{18}$	$1.5{\times}10^{18}$	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Ion flux Γ_i	1×10^{16}	$1{\times}10^{16}$	$1{\times}10^{16}$	$1{ imes}10^{16}$	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
F sticking on Si γ_F	0.7	0.7	0.7	0.7	1
O sticking on Si γ_O	1.0	1.0	1.0	1.0	1
Si density ρ_{Si}	$5{ imes}10^{22}$	$5{\times}10^{22}$	$5{\times}10^{22}$	$5{ imes}10^{22}$	$\rm atoms/cm^3$
O recombination rate $\beta \sigma_{Si}$	5×10^{13}	5×10^{13}	5×10^{13}	5×10^{13}	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Reaction rate constant	$3{ imes}10^{17}$	$3{ imes}10^{17}$	$3{ imes}10^{17}$	$3{\times}10^{17}$	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
$k\sigma_{Si}$					
Si yield proportionality	7.0	7.0	7.0	7.0	1
constant A_{Si}					
O yield proportionality	2.0	2.0	2.0	2.0	1
constant A_O					

etch rate for the change from 0.44 to 0.5, despite the fact that oxygen generally only has a passivating effect. Increasing the oxygen content further decreases both lateral and vertical etching, as intuitively expected.

Along with qualitatively capturing this phenomenon, the agreement in the etch rate is shown by overlaying the SEM cross sections from Belen et al. [63] with the cross sections of

4 Physical Models

the 3D simulated profiles from the Figure 4.1. The results are provided in Figure 4.2, where the calibrated model cross sections are shown in green. Figure 4.2a shows the capability of the model to capture more isotropic etch profiles, where no oxygen is present in the feed gas. In the experiments which involved oxygen in the feed gas, as shown in Figure 4.2b-e, the lateral etch rate is highest when the oxygen content is lowest, as depicted in Figure 4.2b. As the oxygen flux increases, sidewall passivation becomes more prominent, which leads to a decrease in lateral etching. The decrease in lateral etching is expected, leading to the previously mentioned phenomenon of a higher vertical etch rate. Since oxygen occupies the sidewall surface, more fluorine flux is reflected towards the feature bottom, as shown in Figure 4.2c. However, when the oxygen content is further increased, a negative (inward) sidewall tapering and an inhibition of vertical etching occur, as shown in Figure 4.2d and, to an even greater extent, in Figure 4.2e. Additionally, the overlaid profile in Figure 4.2a demonstrates the model's ability to capture more isotropic etching behaviour when no oxygen is fed to the reactor.

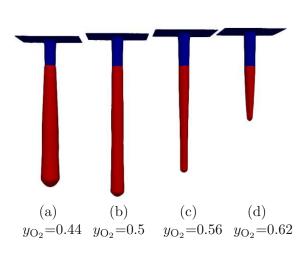


Figure 4.1: Simulated 3D profiles using the parameters from Table 4.1. Figure from [80].

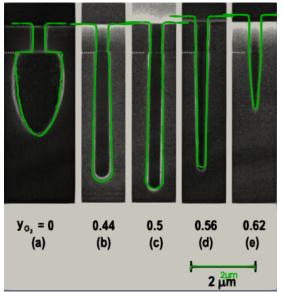


Figure 4.2: Cross sections of the obtained 3D structures, shown in green, are laid over the SEM cross sections from Belen et al. [63] in black. Reprinted with permission from [63]. Copyright 2005, American Vacuum Society.

Next, the model is calibrated to the changes in the chamber pressure. To account for the variations of chamber pressure in the model, it is essential to note that a rise in pressure leads to a direct increase in the fluxes of fluorine and oxygen (neutral species) and a decrease in the ion flux. The parameters used for producing the best fit to the profiles are given in the Table 4.3. The simulated profiles are shown in Figure 4.3, clipped where the cross sections are taken. At lower pressures, the impact of oxygen coverage on the process is less pronounced, resulting in outward sidewall tapering, as demonstrated in Figure 4.4a. As the pressure increases, despite the reduced ion flux, there is a slight increase in vertical etching due to more fluorine reflecting towards the bottom, as illustrated in Figure 4.4b. A further increase in the pressure inhibits both lateral and vertical etching and causes a change in the sidewall tapering from positive (outward) to negative (inward), as presented in Figure 4.4c.

Table 4.3: Simulation parameters used for obtaining the best fit to the profile variations observed in the pressure variation study. The simulation setting replicates a chamber with a total gas flow rate of 80 sccm at varying pressures, an inductive coil power of 800 W, and an RF-bias voltage of -20 V at a wafer temperature of 5°C.

Parameter	Char	Unit		
	10mTorr	$25 \mathrm{mTorr}$	40mTorr	
Fluorine flux Γ_F	1.8×10^{18}	$5{ imes}10^{18}$	$8.5{\times}10^{18}$	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Oxygen flux Γ_O	1×10^{17}	$3{\times}10^{17}$	$6{ imes}10^{17}$	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Ion flux Γ_i	1.2×10^{16}	$1{\times}10^{16}$	8×10^{15}	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Si yield proportionality constant A_{Si}	7.0	7.0	7.0	1
O yield proportionality constant A_O	2.5	2.0	1.0	1

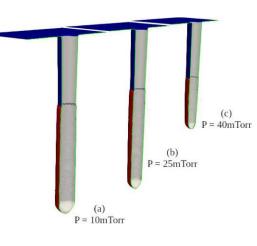


Figure 4.3: Clipped view of simulated structures using parameters from Table 4.3. The green curve denotes the cross section used for overlaying the experimental SEM profiles in Figure 4.4 Figure from [80]

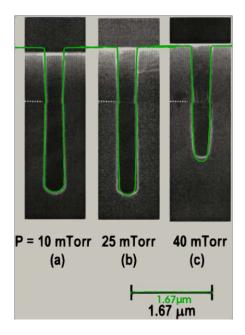


Figure 4.4: Cross section comparison for pressure variation. Reprinted with permission from [63]. Copyright 2005, American Vacuum Society. Closely capturing variations in both feed gas composition and pressure gives confidence in using the model for predictive simulations. In Chapter 5, the data is used to analyse the impact of different mask shapes on the final feature profile.

4.2 C_xF_x/Ar^+ Plasma Etching

To model SiO_2 etching in a fluorocarbon plasma, the surface model proposed in [81] is used as an approximation to the reactions shown in Table 4.4. Although the model, in principle, captures only a simple chemistry such as pure CF_2 etching of SiO₂ under Ar⁺ bombardment and polymer inhibition, it can be used for a broad set of applications if it is sensible to assume the chemical reactions at the surface are captured with SF_6/O_2 sufficient accuracy [82]. In the model, one etchant, one passivating species, and one ion species are considered. Similarly to the SF_6/O_2 model, surface coverages - chemical etchant $\theta_{\rm e}$, polymer $\theta_{\rm p}$ and polymer-etchant $\theta_{\rm e/p}$ - are used. Since an etchant can cover the SiO₂ surface or deposited polymer, SiO_2 and polymer etchant coverages are proportional to the neutrals' flux Γ_e . Analogously, polymer coverage depends on the polymer flux Γ_p . All three types of coverages are influenced by the flux of ions Γ_i , while temperature dependent evaporation flux Γ_{ev} is considered only for coverage of SiO₂ with the chemical etchant. The evaporation flux describes how much of the etchant species leaves the surface due to the impact of temperature and is proportional to Γ_e . Under the assumption of coverages reaching steady-state conditions very fast in comparison to the etching and deposition time scales, the surface site balance equations are given by:

$$\frac{d\theta_e}{dt} = \Gamma_e S_e \left(1 - \theta_e - \theta_p\right) - k_{ie}^e \Gamma_i Y_{ie}^e \theta_e - k_{ev} \Gamma_{ev} \theta_e \approx 0$$
(4.7)

for SiO_2 -etchant coverage,

$$\frac{d\theta_{\rm p}}{dt} = \Gamma_{\rm p} S_{\rm p} - \Gamma_{\rm i} Y_{\rm ie}^{\rm p} \theta_{\rm p} \theta_{e/\rm p} \approx 0 \tag{4.8}$$

for polymer coverage, and

$$\frac{d\theta_{\rm e/p}}{dt} = \Gamma_e S_{\rm e/p} \left(1 - \theta_{\rm e/p} \right) - \Gamma_{\rm i} Y_{\rm ie}^{\rm p} \theta_{\rm e/p} \approx 0 \tag{4.9}$$

for polymer-etchant coverage. The terms S_e , S_p , and $S_{e/p}$ denote the neutrals particles' sticking coefficient; Γ_e , Γ_p , Γ_i , and Γ_{ev} are etchant, polymer, and ion fluxes, respectively; Y_{ie}^e and Y_{ie}^p represent SiO₂ and polymer ion-enhanced etching yield functions, respectively.

The surface movement is dependent on the ratio of the incoming fluxes. Two surface rates are considered for polymer impact:

• Under the assumption that ion-enhanced etching is the only mechanism removing the polymer from the surface, the polymer etch rate is given by

$$ER_{\rm p} = \frac{1}{\rho_p} Y_{\rm ie}^{\rm p} \Gamma_{\rm i} \Theta_{\rm e/p}, \qquad (4.10)$$

where ρ_p is the polymer density.

Reaction		Process	
Physical sputtering			
(1) O ₂ -Si [*]	\rightarrow Si(g)+2O(g)+O ₂ -Si [*]	Physical sputtering	
Reactions with F atoms			
(2) O_2 -Si [*] +2F(p)	$\rightarrow O_2$ -Si-F ₂ (s)	Adsorption	
(3) O_2 -Si- $F_2(s)$ +2F(p)	$\rightarrow \mathrm{Si}\text{-}\mathrm{F}_4(g) + \mathrm{O}_2(g) + 2\mathrm{O}_2\text{-}\mathrm{Si}^*$	Ion-enhanced chemical etching by F	
(4) O_2 -Si- $F_2(s)$	$\rightarrow \mathrm{Si}\text{-}\mathrm{F}_2(g) + \mathrm{O}_2(g) + 2\mathrm{O}_2\text{-}\mathrm{Si}^*$	Ion-enhanced chemical sputtering	
(5) O_2 -Si- $F_2(s)$ +2F(p)+2F(g)	\rightarrow Si-F ₄ (g) + O ₂ (g)	Thermal etching by F	
Reactions with $CF_x(x=1-3)$ or ot	her fluorocarbon radicals		
(6) Si-O ₂ (s)+CF _x (g)	\rightarrow Si-O ₂ -CF _x (s)	Chemisorption	
(7) 2Si-O ₂ -CF _x (s)	$\rightarrow \rm{SiF}_x(g) + 2\rm{CO}_2(g) + \rm{Si-O_2}^*$	$\begin{array}{ll} \mbox{Ion-enhanced} & \mbox{chemical} \\ \mbox{etching by } \mbox{CF}_{\mathbf{x}} \mbox{ radicals} \end{array}$	
(8) Si-O ₂ -CF _x (s)	\rightarrow Si(s)+ 2COF_x(g)+Si-O_2*	C sputtering	
(9) Si-O ₂ -CF _x (s) + F(p) or F(g)	$\rightarrow \rm{Si-O}_2 + \rm{CF}_{x+1}(g)$	$\begin{array}{llllllllllllllllllllllllllllllllllll$	
Reactions of polymer creation or	loss		
(10) CF_x^+ at $E < E_{th}$	\rightarrow Polymer P	Direct ion deposition	
(11) Si-O ₂ -CF _x (s) at E <e<sub>th</e<sub>	\rightarrow Polymer P	Ion-enhanced deposition of sorbed radicals	
(12) $P-F(s)$	\rightarrow Etching of polymer P	Ion-enhanced etching of polymer by F atoms	
(12) $P-CF_x(s)$	\rightarrow more polymer	Ion-enhanced deposition of sorbed radicals	

Table 4.4: Reaction set for SiO_2 etching in fluorocarbon plasmas. Reprinted from [82], with the permission of AIP Publishing.

^ap stands for physisorbed atoms, s stands for chemisorbed atoms or radicals, s/P stands for chemisorbed atoms or radicals on polymer surface, the (^{*}) denotes a dangling bond or a site for chemisorption.

• At the same time, under the influence of the incoming polymer flux, polymer can deposit onto the surface with the deposition rate

$$DR_{\rm p} = \frac{1}{\rho_{\rm p}} S_{\rm p} \Gamma_{\rm p} \tag{4.11}$$

If the incoming polymer flux dominates, i.e., $DR_p > ER_p$ or effectively if $\theta_p > 1$, an etchpassivating polymer layer is deposited onto the surface. In this case, the remaining two coverages θ_e and θ_p are not relevant for surface deposition rate (DR), which is given by the difference between the two rates:

$$DR = DR_p - ER_p = \frac{1}{\rho_{\rm p}} \left(Y_{\rm ie}^{\rm p} \Gamma_i \theta_{\rm e/P} - S_{\rm p} \Gamma_{\rm p} \right).$$
(4.12)

However, if the etching mechanisms dominate, i.e., $DR_p \leq ER_p$, the SiO₂ film can be etched away at the velocity calculated considering ion-enhanced etching, physical sputtering and evaporation:

$$ER = \frac{1}{\rho_{\rm SiO_2}} \left[\Gamma_i Y_{\rm ie}^{\rm e} \theta_e + \Gamma_i Y_{\rm s} \left(1 - \theta_{\rm e} - \theta_{\rm p} \right) + \Gamma_{\rm ev} \theta_{\rm e} \right], \tag{4.13}$$

where ρ_{SiO_2} is the SiO₂ density and Y_s is the ion sputtering yield. The yield functions are dependent on the impinging ion energies and incidence angles. A generic form reads as

$$Y(E) = A(\sqrt{E} - \sqrt{E_{th}}), \qquad (4.14)$$

where the coefficient A captures angular dependence and E_{th} describes how susceptible a material is to ion impact, meaning at what threshold energy will the surface be removed upon ion impact. The exact values for the model are taken from the literature [81, 82, 83].

During SiO₂ etching in fluorocarbon plasma, either the etching or the deposition of passivating polymer layer can occur. This is demonstrated using the 3D simulation outputs from the model implemented in ViennaTS [84] library using the fluxes and sticking coefficients shown in Table 4.5. All the parameters are kept constant as the polymer flux is varied to show the flux ratio's effect on the vertical etching and the presence of the passivating polymer layer shown in Figure 4.5. As the polymer flux increases, both sidewall and vertical etching are inhibited. Additionally, the passivating sidewall polymer layer grows in thickness with the increase of polymer flux, as expected.

Parameter	Value	Unit
Etchant flux Γ_e	8×10^{16}	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Polymer flux Γ_p	$3{\times}10^{15}$ - $3{\times}10^{18}$	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Ion flux Γ_i	1×10^{16}	$\mathrm{cm}^{-2}\mathrm{s}^{-1}$
Etchant sticking coeff S_e	0.9	1
Polymer sticking coeff S_p	0.26	1
Etchant on polymer sticking coeff $S_{e/p}$	0.6	1
Simulation time t	150	s

Table 4.5: Fluxes and sticking coefficient used for the fluorocarbon plasma hole etching shown in Figure 4.5.

4 Physical Models

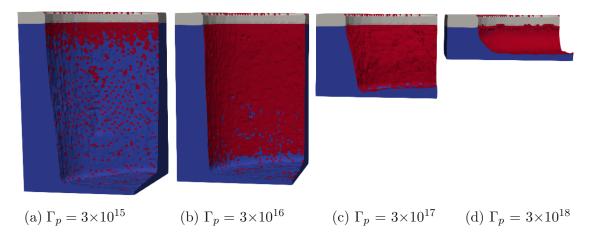


Figure 4.5: Cylindrical hole etching in fluorocarbon plasma using parameters from Table 4.5. SiO₂ is shown in blue, the mask in gray, and the polymer layer in red. With the increase in polymer flux, a more significant passivating layer forms on the sidewalls. The passivating layer is not present at the bottom since the ions sputter it away. However, vertical etching is inhibited due to more polymer species being present in the surface reactions.

5 Applications

5.1 SF₆/O₂ Mask Impact

It is often presumed in plasma etching simulations, that masks have an ideal geometry [85]. One could perform photolithography simulations in order to obtain a proper description of the mask geometry, but this might computationally inefficient and it would not help describe how the mask changes during the etching process. There are many cases where mask imperfections can have a significant impact on the final etched profile. The SF_6/O_2 plasma etching model, implemented within the scope of this thesis, is capable of qualitatively reproducing and predicting many phenomena which occur during plasma etching experiments. The effects which can occur include, but are not limited to, bowing, microtrenching, undercutting, sidewall tapering, notching, and overcutting, as shown in Figure 5.1 from Donnelly and Kornblit [79]. To quantify these effects, a calibration step is typically necessary so as to ensure that the model can accurately represent the specific experimental setup being simulated.

5.1.1 Impact of Mask Tapering

Having a predictive model for plasma etching is important in reducing the number of experimental trial-and-error runs during the design cycle. Similar studies were conducted to evaluate the impact of previously etched layers on the etch rate and sidewall tapering of the bottom of the high aspect ratio (HAR) structure. These studies were performed for fluorocarbon etching of SiO₂ and halogen gas etching of Si in 3D NAND memory stacks [3, 86]. Their results addressed the structures incorporating slight outward tapering in the mask SiO₂ layer, followed by slight inward tapering of the silicon layer. To investigate the influence of the tapering angle on the etched profile, the angle of a 1.2 μ m thick cylindrical mask with an opening diameter of 0.35 μ m is varied from 0° to 4° with other parameters fixed to the values shown in Table 4.2.

The feature cross sections for the selected gas composition of y_{O_2} are shown in Figure 5.2 to demonstrate the described effects. The initial mask taper angle increase from 0° to 0.5° amplifies the vertical etching due to more ions being reflected directly towards the bottom, similar to the microtrenching effect mentioned in Figure 5.1. In general, the taper angle increase makes the ions reflect at a more lateral angle, leading to more pronounced sidewall etching and bowing. Further increasing the mask taper angle redirects the ions toward the sidewall closer to the top of the hole, reducing the vertical etch rate and shifting the bowing effect upwards, closer to the mask.

The simulations were performed for all four mentioned gas compositions to study the

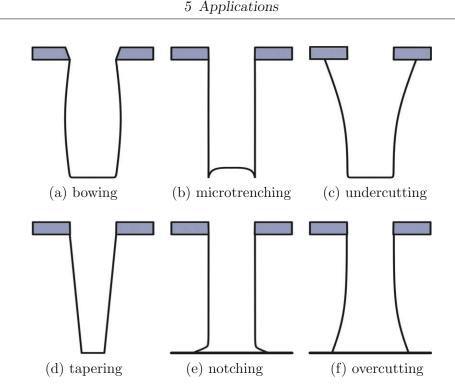


Figure 5.1: Effects of plasma etching on the final profile: (a) Bowing due to mask faceting;
(b) microtrenching due to an enhanced ion flux along the sidewall; (c) undercutting due to an isotropic component in the etch process; (d) sidewall tapering due to sidewall inhibition or deposition of polymer on the sidewall; (e) notching at the interface with an etch-stop layer due to inadequate sidewall passivation or charging effects; (f) re-entrant profile (overcutting) due to inadequate sidewall passivation and/or ion scattering. Reprinted with permission from Donnelly and Kornblit [79]

link between feed gas composition and the effects caused by taper angle changes. Two metrics describe the effects: Final depth and the width-at-half-depth (WAHD). The data is shown in Figure 5.3. The processes with a low oxygen content exhibit a weaker sidewall passivation effect, resulting in a more pronounced bowing effect, captured by the WAHD. It is noticeable that the mask geometry strongly affects these physical phenomena, and the WAHD is at its minimum for the mask taper angles at which the hole depths are at their maximum. This impact is a direct result of most ions being directly reflected to the very bottom of the hole with high energies at that taper angle. The maximum depth is achieved at a low taper angle of around 0.5° for $y_{O_2}=0.44$ and $y_{O_2}=0.5$. As the oxygen concentration in the feed gas increases, the maximum occurs at higher angles. However, for $y_{O_2}=0.62$, the highest oxygen concentration studied, a different behavior is observed due to significantly reduced vertical etching. Due to strong inward tapering, the maximum at a tapering angle of 1° as the pronounced passivation effect, combined with higher order ion reflections, favor vertical etching at higher tapering angles.

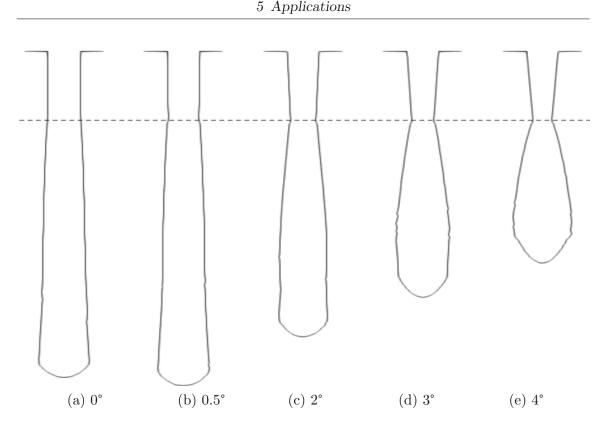


Figure 5.2: Cross sections simulated features obtained by varying the mask taper angle from 0° to 4° for $y_{O_2}=0.5$. From (a) to (e) increasing the taper angle first increases the vertical etch rate and then leads to more sidewall bowing at the expense of vertical etching. The other model parameters are given in Table 4.2.

5.1.2 Impact of Mask Faceting

In the preceding subsection, the influence of mask tapering for varying gas compositions was examined, which refers to the presence of a layer with a tapered sidewall profile on top of the layer being etched. However, ion bombardment can cause faceting at the corners during the plasma etching process even if the mask layer does not initially have any tapering [79, 87]. This is because the sputtering yield is dependent on the angle of incidence of the ions, which can cause the sharp corners to erode [88], resulting in a tapered sidewall profile on the mask forming during fabrication. To mitigate this effect, thicker masks can be used, but this approach may not always be practical since mask thickness also affects the final feature profile.

The effect of thin mask faceting on the final feature profile is investigated by varying the angle of the mask top-corner sputtering from 0° to 30° for the scenarios where the entire mask wall has the given angle, as shown in Figure 5.4. The simulation setting again replicates a chamber with a total gas flow rate of 80 sccm at a pressure of 25 mTorr, an inductive coil power of 800 W, and an RF-bias voltage of -120 V, with an oxygen fraction of $y_{O_2}=0.5$ in the feed gas. The maximum depth, maximum profile width, and the position where the maximum width occurs normalized to the interval 0 to -1 were measured and

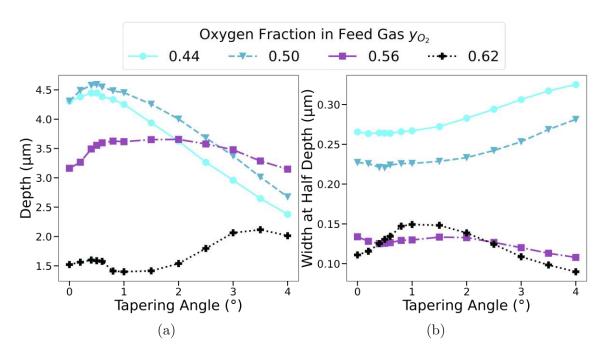


Figure 5.3: Depth and width-at-half-depth (WAHD) of a cylindrical hole as the mask tapering angle is varied from 0° to 4°. The depth is at the maximum, where the WAHD reaches its minimum for all gas compositions. When reducing the oxygen content, the depth peaks after an initial angle increase and decreases significantly as the angle increases further, while the WAHD reaches its minimum after an initial angle increase and increases significantly with further increases in the angle. Since the most significant changes were expected for small taper angles, more sample points were used in the range from 0° to 1°.

recorded. Zero represents a point just under the mask, while -1 signifies the very bottom of the feature. The results, shown in Figure 5.5a, indicate that the maximum depth increases when increasing the facet taper angle. The increase is not completely linear as it depends on the landing point of the first and second ion reflections off the sidewall. Higher faceting angles (> 30)° lead to fully directional vertical etching as no ions are reflected from the mask towards the substrate sidewall, resulting in the same profile as without faceting.

Another common feature in etched structures is the bowing effect (see Figure 5.1a), which is captured by the maximum width and shown in Figure 5.5b. The largest sidewall bowing occurs for angles between 15° and 20°, and is more pronounced for the thickest mask considered. This is a consequence of having a significant mask sidewall area to reflect the ions and direct them towards the sidewall, in comparison to the masks with thicknesses of $0.1 \,\mu\text{m}$ and $0.2 \,\mu\text{m}$. Next, Figure 5.5c shows the vertical position along the feature sidewall, where the maximum width occurs. For small angles, which indicate weak faceting, the maximum width is located just beneath the mask, suggesting the undercutting effect. In this case, the ions reflected from the mask hit directly at the bottom of the geometry, while the most significant lateral etching is due to the ions impinging on the substrate surface

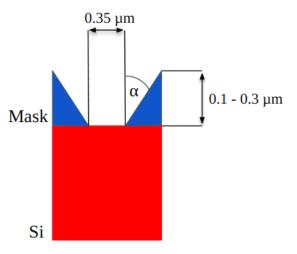


Figure 5.4: Illustration of mask faceting. Masks with a whole sidewall under angle $\alpha = 0^{\circ}$ to $\alpha = 30^{\circ}$ are considered and impact of the angle on the final feature profile is measured for 0.1 µm, 0.2 µm and 0.3 µm thick masks

just under the mask. As the tapering angle increases, the impact point of the reflected ions shifts from the feature bottom towards the bottom sidewall, causing a sharp drop in the vertical position of the maximum width. Similarly to the previous section, higher facet angles shift the bowing effect further up the profile sidewall. By employing thicker masks, a smaller fraction of the mask would be faceted, leading to a less significant impact. However, these results indicate that even a small change in the mask thickness can lead to significant changes in the final feature profile.

5.1.3 Impact of Mask Etch Rate

A SiO₂ mask sputtering yield reported in Belen et al. [63] was applied in the previous simulations. The substrate etching showed excellent agreement with the experiment. However, the slight offset between the simulated and experimental mask etch rate for settings with more oxygen in the feed gas, given in Figure 4.2d and Figure 4.2e, poses a question regarding the impact of this offset on the final profile. The experimental setup described in subsection 4.1.1 was utilized to investigate the effect of mask etching on the resulting feature profile. The oxygen fraction in the feed gas was set to $y_{O_2}=0.5$ and the mask sputtering yield was varied in the range of 0.01 to 0.5, corresponding to minimal mask etching and complete removal of the mask layer, respectively. In Figure 5.6a, the maximum depth is achieved when the entire mask is etched away (sputtering yield of 0.5), while resulting in the lowest lateral etching, as shown in Figure 5.6b. This result is consistent with the findings from the previous sections, since thinner masks cause fewer species reflections towards the sidewall. Additionally, the impact on the final profile is the most pronounced for taper angles larger than 1.5° for the WAHD and 2° for the depth. This observation implies that the perfectly fitting mask etch rate for higher oxygen contents during the model validation process would not distort the agreement of the simulation results with the experimental feature profile.

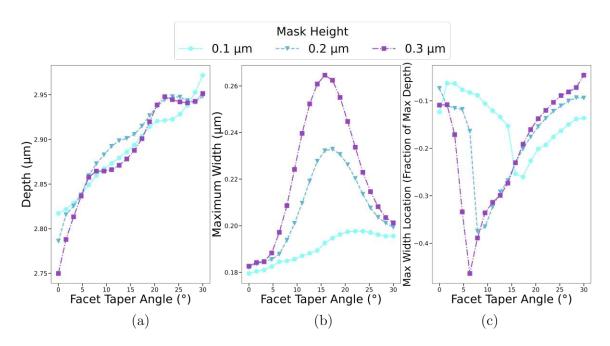


Figure 5.5: Depth, maximum width and its location down the feature sidewall plotted against high angles, relevant for thin mask faceting. In (a) the maximum depth increases with increasing the tapering angle. In (b), bowing peaks for angles between 15° and 20° with the peaks being lower for thinner masks due to a reduced ion reflection surface. (c) The maximum width location drops with initial angle increase and gradually moves up the profile with a further increase.

5.1.4 Rectangular Trench Profiles

With previous sections discussing cylindrical hole geometries, the focus now turns on trench masks. The trench masks considered here have a width of $0.4 \,\mu\text{m}$ at the top, and the parameters listed in Table 4.2 which were used for cylindrical holes, are now applied to rectangular trenches for drawing relevant comparisons.

The data presented in Figure 5.7a shows that the vertical etch rates in trenches are significantly higher than those in their corresponding cylindrical hole geometries. In addition, almost all samples, shown in Figure 5.7b, have higher lateral etch rates in trenches compared to holes. This effect is caused by a higher flux of all species reaching both the sidewalls and the bottom in a trench.

In the trench geometry, the flux is higher due to fewer reflections occurring off of the sidewalls than in a cylindrical geometry. As particles move through a trench, their movement is limited in only one direction, whereas in a cylindrical geometry, a particle's motion is hindered in all directions. The result for the trenches is that, when the particle reaches the bottom, it will have had fewer reflections, and its impact will effectively weigh more than in

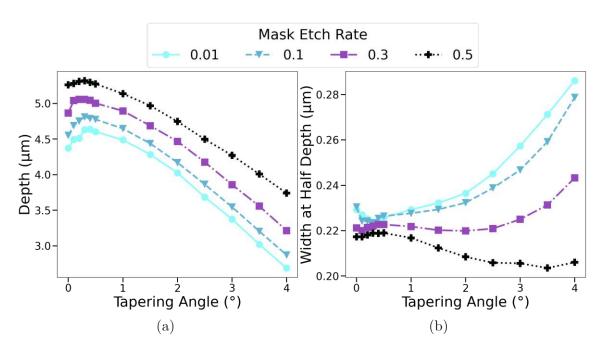


Figure 5.6: Comparison of different mask etch rates for the 1.2 µm thick mask with 0.4 µm top opening under varying taper angles with $y_{O_2} = 0.5$ and a parameter setting from Table 4.2. (a) Higher rate of mask etching causes higher vertical etch rates and (b) lower lateral rates.

the cylindrical hole geometry. The setting with the highest oxygen content, however, is an exception. For $y_{O_2} = 0.62$, the effect is less pronounced or even reversed as the increased oxygen restricts chemical reactions. With the reduced chemical etching, ion bombardment becomes the primary material removal process. As ions hit the sidewall surface, they are directed toward the bottom. For the trenches, which offer fewer opportunities for ions to be directed to the bottom, this results in a lower vertical etch rate.

The influence of the mask taper angle on the etching process is similar for both cylindrical and trench geometries. In both cases, increasing the taper angle above 1° leads to a decrease in the depth of the etched structure. Thus, the findings for the cylindrical holes presented earlier can be applied to rectangular trenches as well.

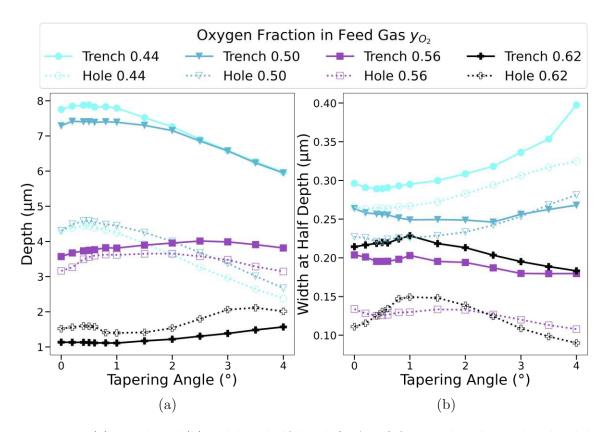


Figure 5.7: (a) Depth and (b) width-at-half-depth (WAHD) for trenches denoted with solid line and squares, and holes shown with dashed line and circles. Trench geometries exhibit higher vertical and lateral etching.

5.2 SF₆/O₂ Plasma Etching Compact Model

Since physical simulations can be very complex and still take considerable time to execute, process emulation can sometimes be used as a replacement. It is frequently the case that the process effects are sufficiently understood without a fully resolved understanding of reactions at the surface [89, 90]. In such circumstances, accurate final geometry predictions can be achieved by reproducing geometrical effects and moving the surface without physical simulations. The SF₆/O₂ physical model is used to construct a compact model which links the chamber parameters directly to the final geometry. Sample points from the studied range were used to construct a space of chamber parameters which can be linked to the final geometry. For feed gas composition, the range is from $y_{O_2} = 0.44$ to $y_{O_2} = 0.62$, and for chamber pressure, it is from P = 10 mTorr to P = 40 mTorr. These sample points represent final simulated structures and span a rectilinear grid from which any point can be taken as an input for the compact model.

Geometric features are extracted from the sample structures to generate the final geometry. In this case, final depth and profile widths are measured at specific locations down the etched hole. By using the geometric features of the sample points in the grid, geometric features at an arbitrary point on the grid are determined by identifying the corresponding grid element and performing bilinear interpolation, which is illustrated in Figure 5.8.

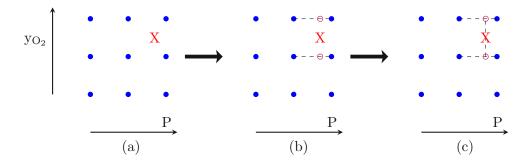


Figure 5.8: Illustration of bilinear interpolation. After locating the corresponding rectangle, an interpolation of the geometric features along one coordinate axis is performed as shown in (b). Another interpolation round in (c) is then performed between the newly generated points to obtain the values at the target point.

The final geometry can be constructed using the interpolated geometric values. The geometry widths at specific depths are known, and it is reasonable to assume rotational symmetry since there is no preferred etching direction. The points of the new surface can be generated by rotating the known widths or radii around the central rotation axis, as illustrated in Figure 5.9. This way, the bowing effect encountered in this type of etching can be replicated. With the available points, which are then connected into a mesh to construct the final geometry.

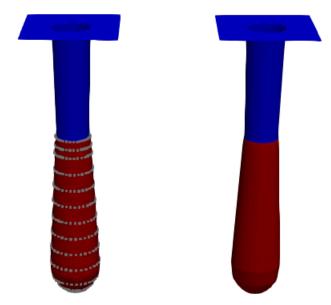
In order to verify the compact model accuracy, eighty random chamber parameter pairs are taken from the considered grid. The relative error, given by

$$E_{rel}(depth_{CM}) = \frac{depth_{simulated} - depth_{CM}}{depth_{simulated}}$$
(5.1)

is calculated for the maximum depth, as shown in the Eq. (5.1) and the WAHD. The results indicate whether the value was over- or underestimated and are provided in Figure 5.10. The average relative error for the depth $E_{rel}^{avg}(depth_{CM}) = 2.0\%$ with the maximum $E_{rel}^{max}(depth_{CM}) = 6.2\%$. The numbers are similar for the WAHD with the average $E_{rel}^{avg}(WAHD_{CM}) = 1.0\%$ and the maximum $E_{rel}^{max}(WAHD_{CM}) = 6.2\%$. Relatively low error margins indicate that this purely geometric approach can often be used as a replacement for time- and compute-intensive physical simulations. However, as mentioned earlier, typical surface movement during a process must be sufficiently understood to make the emulation reliable. Although the model can, with a reasonably low effort, be extended to input variables beyond just gas composition and pressure, there are significant limitations including:

• The model does not account for mask etching.

5 Applications



(a) Constructed points on the simulated profile (b) Constructed final geometry

- Figure 5.9: Maximum depth and radii at specific depths are measured for the simulated samples. Radii and maximum depth are interpolated as described by Figure 5.8. Further points which are used for the construction of final geometry are obtained by rotational symmetry; (a) shows a strong agreement between the points obtained and the geometry from a physical simulation, and (b) shows the final constructed geometry by connecting the calculated points.
 - Lack of geometry variation capability: The model only works for a single mask geometry.
 - Extending the input parameter space to more dimensions exponentially increases the number of required sample points which quickly number into tens of thousands. This effectively negates the initial purpose of avoiding physical simulations.

Using geometry parameters, such as mask thickness, profile width, and tapering would allow for geometry variation and scale up the input parameters. To prevent the exponential growth of the initial physical simulations required for the model to be accurate, an alternative interpolation approach, such as nearest neighbour interpolation, can be used. The description is left-out as it is outside of the scope of this work.

5 Applications

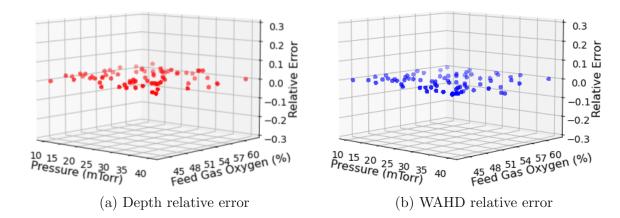


Figure 5.10: 3D plots of relative errors of 80 randomly sampled points used for compact model verification. (a) error in depth approximation and (b) error in widthat-half-depth approximation.

6 Conclusion

Process TCAD is a crucial tool in reducing the number of expensive and time-consuming experimental trial-and-error runs during design cycles. In the scope of this work, a process simulation library was improved upon and expanded to introduce physical plasma etching models.

A 3D feature-scale physical models were developed for SF_6/O_2 and C_xF_x/Ar^+ etching using ViennaPS, an in-house level set-based process simulator. The SF_6/O_2 model was calibrated using experimental data from literature in order to investigate the impact of mask geometry on the plasma-etched profiles of cylindrical holes and rectangular trenches.

The study observed that mask tapering, which is often unavoidable in lithography processing, significantly affects feature profiles. For cylindrical hole geometries, the optimal mask setup which maximizes depth is the same setup which minimizes the width-at-halfdepth (WAHD), regardless of the chamber gas composition. These observations mean perfectly vertical mask sidewalls may not produce the highest etch rates. The same trend was observed for trench geometries, but with higher vertical and lateral etching levels.

Furthermore, the effect of mask faceting on reactive-ion etching was examined by simulating the impact of fabrication parameters on various mask materials. The maximum depth increased when increasing tapering angle, and no significant difference was observed when varying mask thickness. The bowing effect peaked for taper angles between 15° and 20° and was less pronounced for the thinnest mask. Moreover, the impact of the mask etch rate was compared by examining several scenarios, from negligible etching to complete mask removal. A significant increase in vertical etching and a decrease in lateral etching were observed as the proportion of the mask being etched away increased.

Next, as a proof-of-concept, the SF_6/O_2 plasma etching model was used to design and implement a compact model. The model directly links chamber parameters used for model validation to the final geometry parameters. The final structures were predicted accurately for interpolated input data, without the need to run a physical simulation. The accuracy is significant since the final geometry generation is almost instantaneous since there is no need to perform a time-discretized simulation, which takes a considerable amount of time. However, several significant limitations exist as the number of input parameters exponentially increases the number of sample points needed.

During the research process, achieving the first model to capture the physical phenomena at play proved to be the most significant obstacle. The reasons were primarily capturing particle flux at the surface and normalizing it to represent the accurate proportion of the total flux and accurately modeling particle reflections. Overcoming this led to a more nuanced understanding of the processes in the reactor as well as the assumptions taken to model the particle transport.

This research contributes to a better understanding of the complex processes employed during semiconductor fabrication. Further work can be devoted to implement more physical models within the framework and to use different interpolation approaches to reduce the number of sample points required for a compact model with a reasonable number of input parameters. Additionally, the implemented models can be applied to analyze different phenomena, e.g., using the CF_x/Ar^+ plasma etching model to study the impact of the ion sputtering yield function on the final profile when etching materials such as HfO_2 and Si_3N_4 .

Bibliography

- G. E. Moore. Progress in digital integrated electronics [Technical literature, Technical Digest. International Electron Devices Meeting, IEEE, 1975, pp. 11-13.] *IEEE Solid-State Circuits Society Newsletter*, 11(3):36–37, 2006. DOI: 10.1109/N-SSC.2006. 4804410.
- X. Klemenschits. Emulation and Simulation of Microelectronic Fabrication Processes. PhD thesis, Technische Universität Wien (TU Wien), 2022. DOI: 10.34726/HSS. 2022.89324.
- [3] L. Filipovic. Topography Simulation of Novel Processing Techniques. PhD thesis, Technische Universität Wien (TU Wien), 2012. [Online]. Available: http://hdl.handle.net/20.500.12708/13712 (Accessed 21.01.2023).
- [4] R. F. Pierret. Semiconductor Fundamentals. Modular Series on Solid State Devices. Addison-Wesley, [Reading, Mass.], 2. ed., 21. [print.]. 2000.
- [5] J. X. J. Zhang and K. Hoshino. Chapter 2 Fundamentals of nano/microfabrication and scale effect. In *Molecular Sensors and Nanodevices (Second Edition)*, Micro and Nano Technologies, pages 43–111. Academic Press, 2019. DOI: 10.1016/B978-0-12-814862-4.00002-8.
- [6] T. Fukasawa, A. Nakamura, H. Shindo, and Y. H. Y. Horiike. High Rate and Highly Selective SiO2 Etching Employing Inductively Coupled Plasma. *Japanese Journal of Applied Physics*, 33(4S):2139, 1994. DOI: 10.1143/JJAP.33.2139.
- [7] W. J. Mitchell, B. J. Thibeault, D. D. John, and T. E. Reynolds. Highly selective and vertical etch of silicon dioxide using ruthenium films as an etch mask. *Journal of Vacuum Science & Technology A*, 39(4):043204, 2021. DOI: 10.1116/6.0001030.
- [8] T. Hori. Gate Dielectrics and MOS ULSIs: Principles, Technologies and Applications, volume 34 of Springer Series in Electronics and Photonics. Springer Berlin Heidelberg, Berlin, Heidelberg, 1997. DOI: 10.1007/978-3-642-60856-8.
- [9] M. Houssa, L. Pantisano, L.-Å. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, S. D. Gendt, G. Groeseneken, and M. M. Heyns. Electrical properties of high-κ gate dielectrics: Challenges, current issues, and possible solutions. *Materials Science and Engineering: R: Reports*, 51(4):37–85, 2006. DOI: 10.1016/j.mser.2006.04.001.
- D. A. P. Bulla and N. I. Morimoto. Deposition of thick TEOS PECVD silicon oxide layers for integrated optical waveguide applications. *Thin Solid Films*, 334(1):60–64, 1998. DOI: 10.1016/S0040-6090(98)01117-1.
- [11] M. Liu, P. Jin, Z. Xu, D. Hanaor, Y. Gan, and C. Chen. Two-dimensional modeling of the self-limiting oxidation in silicon and tungsten nanowires. *Theoretical and Applied Mechanics Letters*, 6:195–199, 2016. DOI: 10.1016/j.taml.2016.08.002.

- [12] B. S. Yilbas, A. Al-Sharafi, and H. Ali. Chapter 3 surfaces for self-cleaning. In Self-Cleaning of Surfaces and Water Droplet Mobility, pages 45–98. Elsevier, 2019. DOI: 10.1016/B978-0-12-814776-4.00003-3.
- [13] R. C. Jäger. Introduction to Microelectronic Fabrication. Modular Series on Solid State Devices. Addison-Wesley, [Reading, Mass.], 2. ed., 2002.
- [14] G. S. May and C. J. Spanos. Fundamentals of Semiconductor Manufacturing and Process Control. John Wiley & Sons, Inc., [Hoboken, New Jersey], 2006. DOI: 10. 1002/0471790281.
- R. A. Lawson and A. P. Robinson. Chapter 1 Overview of materials and processes for lithography. In *Materials and Processes for Next Generation Lithography*. Volume 11, Frontiers of Nanoscience, pages 1–90. Elsevier, 2016. DOI: 10.1016/B978-0-08-100354-1.00001-6.
- [16] W. Kern and K. K. Schuegraf. 1 Deposition Technologies and Applications: Introduction and Overview. In Handbook of Thin Film Deposition Processes and Techniques (Second Edition), pages 11–43. William Andrew Publishing, Norwich, NY, 2001. DOI: 10.1016/B978-081551442-8.50006-7.
- [17] S. Rossnagel. 8 Sputtering and Sputter Deposition. In Handbook of Thin Film Deposition Processes and Techniques (Second Edition), pages 319–348. William Andrew Publishing, [Norwich, NY], 2001. DOI: 10.1016/B978-081551442-8.50013-4.
- [18] H. U. Rashid, K. Yu, M. N. Umar, M. N. Anjum, K. Khan, N. Ahmad, and M. T. Jan. Catalyst role in chemical vapor deposition (CVD) process: A review. *Rev. Adv. Mater. Sci*, 40(3):235–248, 2015.
- [19] S. M. Sze and M. K. Lee. Semiconductor Devices : Physics and Technology. John Wiley & Sons, Inc., [New York, NY], 3rd ed., 2012.
- [20] A. Razavieh, P. Zeitzoff, and E. J. Nowak. Challenges and Limitations of CMOS Scaling for FinFET and Beyond Architectures. *IEEE Transactions on Nanotechnology*, 18:999–1004, 2019. DOI: 10.1109/TNAND.2019.2942456.
- [21] C.-H. Jan, U. Bhattacharya, R. Brain, S.-J. Choi, G. Curello, G. Gupta, W. Hafez, M. Jang, M. Kang, K. Komeyli, T. Leo, N. Nidhi, L. Pan, J. Park, K. Phoa, A. Rahman, C. Staus, H. Tashiro, C. Tsai, P. Vandervoorn, L. Yang, J.-Y. Yeh, and P. Bai. A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications. In 2012 International Electron Devices Meeting, pages 3.1.1–3.1.4, San Francisco, CA, USA. IEEE, 2012. DOI: 10.1109/IEDM.2012.6478969.
- [22] M. Graef. More Than Moore White Paper. In 2021 IEEE International Roadmap for Devices and Systems Outbriefs, pages 1–47, Santa Clara, CA, USA. IEEE, 2021. DOI: 10.1109/IRDS54852.2021.00013.
- [23] Y. Li and D. Goyal, editors. 3D Microelectronic Packaging: From Architectures to Applications, volume 64 of Springer Series in Advanced Microelectronics. Springer Singapore, [Singapore], 2021. DOI: 10.1007/978-981-15-7090-2.

- [24] C. Hu, M. Chen, W. Chiou, and D. C. Yu. 3D Multi-chip Integration with System on Integrated Chips (SoIC[™]). In 2019 Symposium on VLSI Technology, T20–T21, 2019. DOI: 10.23919/VLSIT.2019.8776486.
- [25] R. Patti. Three-Dimensional Integrated Circuits and the Future of System-on-Chip Designs. *Proceedings of the IEEE*, 94(6):1214–1224, 2006. DOI: 10.1109/JPROC.2006. 873612.
- [26] M.-F. Chen, F.-C. Chen, W.-C. Chiou, and D. C. Yu. System on Integrated Chips (SoIC(TM) for 3D Heterogeneous Integration. In 2019 IEEE 69th Electronic Components and Technology Conference (ECTC), pages 594–599, 2019. DOI: 10.1109/ ECTC.2019.00095.
- [27] J. P. Gambino, S. A. Adderly, and J. U. Knickerbocker. An overview of throughsilicon-via technology and manufacturing challenges. *Microelectronic Engineering*, 135:73–106, 2015. DOI: 10.1016/j.mee.2014.10.019.
- [28] M. Motoyoshi. Through-Silicon Via (TSV). Proceedings of the IEEE, 97(1):43–48, 2009. DOI: 10.1109/JPROC.2008.2007462.
- [29] P. A. Thadesar, X. Gu, R. Alapati, and M. S. Bakir. Through-Silicon Vias: Drivers, Performance, and Innovations. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 6(7):1007–1017, 2016. DOI: 10.1109/TCPMT.2016. 2524691.
- [30] S. Li and Y. Fu. 3D TCAD Simulation for Semiconductor Processes, Devices and Optoelectronics. Springer, New York, NY, 2012. DOI: 10.1007/978-1-4614-0481-1.
- [31] A. Toifl. Numerical Methods for Three-Dimensional Selective Epitaxy and Anisotropic Wet Etching Simulations. Thesis, Technische Universität Wien (TU Wien), 2021. DOI: 10.34726/hss.2021.91744.
- [32] C. K. Maiti. Introducing Technology Computer-Aided Design (TCAD): Fundamentals, Simulations, and Applications. Jenny Stanford Publishing, [New York], 2017. DOI: 10.1201/9781315364506.
- [33] O. Ertl. Numerical methods for topography simulation. Thesis, Technische Universität Wien (TU Wien), 2010. DOI: 10.34726/hss.2010.001.
- [34] S. Barraud, V. Lapras, M. Samson, L. Gaben, L. Grenouillet, V. Maffini-Alvaro, Y. Morand, J. Daranlot, N. Rambal, B. Previtalli, S. Reboh, C. Tabone, R. Coquand, E. Augendre, O. Rozeau, J. M. Hartmann, C. Vizioz, C. Arvet, P. Pimenta-Barros, N. Posseme, V. Loup, C. Comboroure, C. Euvrard, V. Balan, I. Tinti, G. Audoit, N. Bernier, D. Cooper, Z. Saghi, F. Allain, A. Toffoli, O. Faynot, and M. Vinet. Vertically stacked-NanoWires MOSFETs in a replacement metal gate process with inner spacer and SiGe source/drain. In 2016 IEEE International Electron Devices Meeting (IEDM), pages 17.6.1–17.6.4, 2016. DOI: 10.1109/IEDM.2016.7838441.
- [35] Y.-T. Chang, K.-P. Peng, P.-W. Li, and H.-C. Lin. Fabrication and characterization of novel gate-all-around polycrystalline silicon junctionless field-effect transistors with ultrathin horizontal tube-shape channel. *Japanese Journal of Applied Physics*, 57(4S):04FP06, 2018. DOI: 10.7567/JJAP.57.04FP06.

Bibliography

- [36] IEEE Electronics Packaging Society. Heterogeneous Integration Roadmap, 2021. [Online]. Available: https://eps.ieee.org/technology/heterogeneous-integrationroadmap.html (Accessed 28.02.2023).
- [37] F. Rodrigues, L. F. Aguinsky, A. Toifl, A. Scharinger, A. Hossinger, and J. Weinbub. Surface reaction and topography modeling of fluorocarbon plasma etching. In *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pages 229–232. IEEE, 2021. DOI: 10.1109/sispad54002.2021.9592583.
- [38] X. Klemenschits, T. Reiter, J. Bobinac, J. Piso, and L. Filipovic. ViennaPS 1.0.0, version 1.0.0, 2022. [Online]. Available: https://github.com/ViennaTools/ViennaPS (Accessed 10.02.2023).
- [39] S. Hönl, H. Hahn, Y. Baumgartner, L. Czornomaz, and P. Seidler. Highly selective dry etching of GaP in the presence of Al_xGa1-xP with a SiCl₄/SF₆ plasma. *Journal* of Physics D: Applied Physics, 51, 2018. DOI: 10.1088/1361-6463/aab8b7.
- [40] W. G. Vincenti and C. H. Kruger. Introduction to Physical Gas Dynamics. Krieger, [Malabar, Fla], 1975.
- [41] V. Singh. 5 Feature Scale Modeling. In Handbook of Thin Film Deposition Processes and Techniques (Second Edition), pages 205–240. William Andrew Publishing, Norwich, NY, 2001. DOI: 10.1016/B978-081551442-8.50010-9.
- [42] X. Klemenschits, S. Selberherr, and L. Filipovic. Modeling of Gate Stack Patterning for Advanced Technology Nodes: A Review. *Micromachines*, 9(12), 2018. DOI: 10. 3390/mi9120631.
- [43] V. Šimonka. Thermal Oxidation and Dopant Activation of Silicon Carbide. Thesis, Technische Universität Wien (TU Wien), 2018. DOI: 10.34726/hss.2018.60302.
- [44] L. Pelaz, L. Marques, M. Aboy, P. Lopez, I. Santos, and R. Duffy. Atomistic process modeling based on Kinetic Monte Carlo and Molecular Dynamics for optimization of advanced devices. In 2009 IEEE International Electron Devices Meeting (IEDM), pages 1–4, 2009. DOI: 10.1109/IEDM.2009.5424309.
- [45] M. Shayan, A. R. Merati, B. Arezoo, and M. A. Rezvankhah. Study on atomistic model for simulation of anisotropic wet etching. *Journal of Micro/Nanolithography*, *MEMS*, and *MOEMS*, 10(2):029701, 2011. DOI: 10.1117/1.3586798.
- [46] M. Fermeglia, A. Mio, S. Aulic, D. Marson, E. Laurini, and S. Pricl. Multiscale molecular modelling for the design of nanostructured polymer systems: industrial applications. *Mol. Syst. Des. Eng.*, 5(9):1447–1476, 2020. DOI: 10.1039/D0ME00109K. Publisher: The Royal Society of Chemistry.
- [47] R. Bergamaschini, M. Salvalaglio, R. Backofen, A. Voigt, and F. Montalenti. Continuum modelling of semiconductor heteroepitaxy: an applied perspective. Advances in Physics: X, 1(3):331–367, 2016. DOI: 10.1080/23746149.2016.1181986.
- [48] M. Pauly, M. Gross, and L. Kobbelt. Efficient Simplification of Point-Sampled Surfaces. In *IEEE Visualization*, 2002. VIS 2002. Pages 163–170, 2002. DOI: 10.1109/ VISUAL.2002.1183771.

- [49] M. Law. Grid adaption near moving boundaries in two dimensions for IC process simulation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 14(10):1223–1230, 1995. DOI: 10.1109/43.466338.
- [50] T. Thurgate. Segment-based etch algorithm and modeling. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 10(9):1101–1109, 1991.
 DOI: 10.1109/43.85756.
- [51] J. Bigler, A. Stephens, and S. G. Parker. Design for Parallel Interactive Ray Tracing Systems. In 2006 IEEE Symposium on Interactive Ray Tracing, pages 187–196, 2006. DOI: 10.1109/RT.2006.280230.
- [52] A. Agathos, I. Pratikakis, S. Perantonis, N. Sapidis, and P. Azariadis. 3D Mesh Segmentation Methodologies for CAD applications. *Computer-Aided Design and Applications*, 4(6):827–841, 2007. DOI: 10.1080/16864360.2007.10738515.
- [53] J. Bloomenthal, C. Bajaj, J. Blinn, M.-P. Cani, B. Wyvill, A. Rockwood, and G. Wyvill. *Introduction to Implicit Surfaces*. Morgan Kaufmann Publishers Inc. [San Francisco California], 1997.
- [54] J. A. Sethian. Level Set Methods and Fast Marching Methods, volume 3. Cambridge university press [Cambridge, UK], 1999.
- [55] S. Osher and J. A. Sethian. Fronts propagating with curvature-dependent speed: Algorithms based on Hamilton-Jacobi formulations. *Journal of Computational Physics*, 79(1):12–49, 1988. DOI: 10.1016/0021-9991(88)90002-2.
- [56] S. Osher and C.-W. Shu. High-order esentially nonoscillatory schemes for Hamilton-Jacobi equations. SIAM Journal on Numerical Analysis, 28(4):907–922, 1991. DOI: 10.1137/0728049.
- [57] P. L. Manstetten. Efficient Flux Calculations for Topography Simulation. PhD thesis, Technische Universität Wien (TU Wien), 2018. DOI: 10.34726/hss.2018.57263.
- [58] R. Malladi, J. A. Sethian, and B. C. Vemuri. Shape modeling with front propagation: A level set approach. *IEEE Transactions on Pattern Analysis and Machine Intelli*gence, 17(2):158–175, 1995. DOI: 10.1109/34.368173.
- [59] X. Klemenschits, T. Reiter, J. Bobinac, J. Piso, and L. Filipovic. ViennaLS 2.1.0, version 2.1.0, 2022. [Online]. Available: https://github.com/ViennaTools/ViennaLS (Accessed 10.02.2023).
- [60] O. Ertl and S. Selberherr. Three-dimensional topography simulation using advanced level set and ray tracing methods. In 2008 International Conference on Simulation of Semiconductor Processes and Devices, pages 325–328, 2008. DOI: 10.1109/SISPAD. 2008.4648303.
- [61] J.-C. Yu, Z.-F. Zhou, J.-L. Su, C.-F. Xia, X.-W. Zhang, Z.-Z. Wu, and Q.-A. Huang. Three-Dimensional Simulation of DRIE Process Based on the Narrow Band Level Set and Monte Carlo Method. *Micromachines*, 9(2), 2018. DOI: 10.3390/mi9020074.
- [62] D. Cooperberg, V. Vahedi, and R. Gottscho. Semiempirical profile simulation of aluminum etching in a Cl₂/BCl₃ plasma. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 20(5):1536–1556, 2002. DOI: 10.1116/1.1494818.

- [63] R. J. Belen, S. Gomez, D. Cooperberg, M. Kiehlbauch, and E. S. Aydil. Feature-scale model of Si etching in SF₆/O₂ plasma and comparison with experiments. *Journal* of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 23(5):1430–1439, 2005. DOI: 10.1116/1.2013317.
- [64] F. C. van Delft. Mechanistic framework for dry etching, beam assisted etching and tribochemical etching. *Microelectronic Engineering*, 30(1-4):361–364, 1996.
- [65] T. Reiter, X. Klemenschits, J. Bobinac, J. Piso, and L. Filipovic. ViennaRay 1.2.0, version 1.2.0, 2022. [Online]. Available: https://github.com/ViennaTools/ViennaRay (Accessed 10.02.2023).
- [66] D. L. Chopp. Computing Minimal Surfaces via Level Set Curvature Flow. Journal of Computational Physics, 106(1):77–91, 1993. DOI: 10.1006/jcph.1993.1092.
- [67] X. Klemenschits and O. Ertl and P. Manstetten and J. Weinbub and L. Filipovic. ViennaHRLE 2.1.0, version 2.1.0, 2022. [Online]. Available: https://github.com/ViennaTools/ViennaHRLE (Accessed 28.02.2023).
- [68] B. Houston, M. B. Nielsen, C. Batty, O. Nilsson, and K. Museth. Hierarchical RLE Level Set: A Compact and Versatile Deformable Surface Representation. ACM Trans. Graph., 25(1):151–175, 2006. DOI: 10.1145/1122501.1122508.
- Brillouët, Ρ. [69]W. Arden, М. Cogez, М. Β. Huizing, and R. Graef, Mahnkopf. "More-than-Moore" White Paper. International Technology Roadmap forSemiconductors (ITRS):1-31,2010.[Online]. Available: http://itrs2.net/uploads/4/9/7/7/49775221/irc-itrs-mtm-v2_3.pdf (Accessed 30.01.2023).
- H. Guo, S. Cao, L. Li, and X. Zhang. A review on the mainstream through-silicon via etching methods. *Materials Science in Semiconductor Processing*, 137:106182, 2022.
 DOI: 10.1016/j.mssp.2021.106182.
- [71] D. Bassett, W. Printz, and T. Furukawa. Etching of silicon nitride in 3D NAND structures. *ECS Transactions*, 69(8):159–167, 2015. DOI: 10.1149/06908.0159ecst.
- T. Reiter, X. Klemenschits, and L. Filipovic. Impact of plasma induced damage on the fabrication of 3D NAND flash memory. *Solid-State Electronics*, 192:108261, 2022.
 DOI: 10.1016/j.sse.2022.108261.
- [73] K. H. R. Kirmse, A. E. Wendt, S. B. Disch, J. Z. Wu, I. C. Abraham, J. A. Meyer, R. A. Breun, and R. C. Woods. SiO₂ to Si selectivity mechanisms in high density fluorocarbon plasma etching. Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena, 14(2):710– 715, 1996. DOI: 10.1116/1.588702.
- [74] H.-H. Doh, J.-H. Kim, S.-H. Lee, and K.-W. Whang. Mechanism of selective SiO₂/Si etching with fluorocarbon gases (CF₄, C₄F₈) and hydrogen mixture in electron cyclotron resonance plasma etching system. *Journal of Vacuum Science & Technology* A, 14(5):2827–2834, 1996. DOI: 10.1116/1.580231.

- [75] M. Schaepkens, T. E. F. M. Standaert, N. R. Rueger, P. G. M. Sebel, G. S. Oehrlein, and J. M. Cook. Study of the SiO₂-to-Si₃N₄ etch selectivity mechanism in inductively coupled fluorocarbon plasmas and a comparison with the SiO₂-to-Si mechanism. *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 17(1):26–37, 1999. DOI: 10.1116/1.582108.
- M. Wang, P. L. G. Ventzek, and A. Ranjan. Quasiatomic layer etching of silicon oxide selective to silicon nitride in topographic structures using fluorocarbon plasmas. *Journal of Vacuum Science & Technology A*, 35(3):031301, 2017. DOI: 10.1116/1. 4978224.
- [77] B. Wu and A. Kumar. Plasma etch method for extreme ultraviolet lithography photomask. *Applied Physics Letters*, 90(6):063105, 2007. DOI: 10.1063/1.2470470.
- [78] B. Wu, A. Kumar, and S. Pamarthy. High aspect ratio silicon etch: A review. Journal of Applied Physics, 108(5):051101, 2010. DOI: 10.1063/1.3474652.
- [79] V. M. Donnelly and A. Kornblit. Plasma etching: Yesterday, today, and tomorrow. Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, 31(5):050825, 2013. DOI: 10.1116/1.4819316.
- [80] J. Bobinac, T. Reiter, J. Piso, X. Klemenschits, O. Baumgartner, Z. Stanojevic, G. Stroff, M. Karner, and L. Filipovic. Impact of mask tapering on SF₆/O₂ plasma etching. In *Proceedings of the International Conference on Microelectronic Devices and Technologies (MicDAT)*, pages 91–94. IFSA Publishing, 2022.
- [81] A. L. Magna and G. Garozzo. Factors Affecting Profile Evolution in Plasma Etching of SiO₂ : Modeling and Experimental Verification. *Journal of The Electrochemical Society*, 150(10):F178, 2003. DOI: 10.1149/1.1602084.
- [82] E. Gogolides, P. Vauvert, G. Kokkoris, G. Turban, and A. G. Boudouvis. Etching of SiO₂ and Si in fluorocarbon plasmas: A detailed surface model accounting for etching and deposition. *Journal of Applied Physics*, 88(10):5570–5584, 2000. DOI: 10.1063/1.1311808.
- [83] M. Tuda, K. Nishikawa, and K. Ono. Numerical study of the etch anisotropy in lowpressure, high-density plasma etching. *Journal of Applied Physics*, 81(2):960–967, 1997. DOI: 10.1063/1.364189.
- [84]О. Ertl, Х. Klemenschits, L. Filipovic, and S. Selberherr. ViennaTS The Vienna Topography Simulator, 2022. [Online]. Available: https://github.com/viennats/viennats-dev (Accessed 28.02.2023).
- [85] H. Fukumoto, K. Eriguchi, and K. Ono. Effects of mask pattern geometry on plasma etching profiles. Japanese Journal of Applied Physics, 48(9):096001, 2009. DOI: 10. 1143/jjap.48.096001.
- [86] T. Ichikawa, D. Ichinose, K. Kawabata, and N. Tamaoki. Topography simulation of BiCS memory hole etching modeled by elementary experiments of SiO₂ and Si etching. In *International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, pages 45–48. IEEE, 2010. DOI: 10.1109/sispad.2010.5604576.

- [87] H. L. Bay and J. Bohdansky. Sputtering yields for light ions as a function of angle of incidence. Applied Physics, 19(4):421–426, 1979. DOI: 10.1007/bf00930106.
- [88] A. Kornblit, M. J. Grieco, D. W. Peters, and T. E. Saunders. Linewidth control in trilevel etching. In SPIE Proceedings, pages 320–326. SPIE, 1987. DOI: 10.1117/12. 940441.
- [89] X. Klemenschits, S. Selberherr, and L. Filipovic. Geometric advection and its application in the emulation of high aspect ratio structures. *Computer Methods in Applied Mechanics and Engineering*, 386:114196, 2021. DOI: 10.1016/j.cma.2021.114196.
- [90] O. Luere, E. Pargon, L. Vallier, B. Pelissier, and O. Joubert. Etch mechanisms of silicon gate structures patterned in SF₆/CH₂F₂/Ar inductively coupled plasmas. *Journal* of Vacuum Science & Technology B, 29(1):011028, 2011. DOI: 10.1116/1.3522656.