DISSERTATION

Mixed Negative Bias Temperature Instability and Hot-Carrier Stress

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Abstract

Bias temperature instability (BTI) and hot-carrier degradation (HCD) are among the most important reliability issues, which affect the performance of metal-oxide-semiconductor field-effect transistors (MOSFETs). Both are typically studied in an idealized setting. In particular, for BTI studies no voltage is applied to the drain, leading to laterally homogeneous degradation. With increasing drain bias, the degradation becomes more and more inhomogeneous and the contribution of HCD to the total degradation increases. Even though it is well understood that this mixed BTI/hot-carrier (HC) degradation corresponds to what actually happens in real circuits, there is only a limited number of studies available on the impact of the mixed stress conditions.

In this thesis, the problem of mixed negative bias temperature instability (NBTI)/hot-carrier (HC) stress conditions on SiON pMOSFET characteristics is discussed. This contains on the one hand a comparison of commonly used measurement methods for the threshold voltage shift: the single point measurement of the drain current and the gate voltage. It is shown that in the case of mixed NBTI/HC stress both methods provide different results for the shift, which has to be considered when modeling the degradation. On the other hand, the focus is on the contribution of single defects to the recoverable component of the threshold voltage degradation. Quite remarkably, mixed NBTI/HC stress affects the recoverable component considerably due to two effects.

First, the contribution of oxide defects to recovery after mixed NBTI/HC stress is suppressed independently of their lateral position. As an explanation, from an electrostatic point of view, recovery after mixed NBTI/HC stress is mainly attributed to charge carrier emissions by oxide defects near the source, which have been charged during stress. However, the experimental characterization of recovery after different stress conditions clearly suggests that even defects located in the vicinity of the source can remain uncharged after mixed NBTI/HC stress and thus do not contribute to the recovery signal although they are fully charged after homogeneous NBTI stress. As a consequence, recovery of the threshold voltage shift can be negligibly small after certain stress conditions. This leads to the conclusion that a simple electrostatic model neither describes the behavior of degradation during mixed NBTI/HC stress nor the recovery afterwards properly. Only if secondary generated carriers triggered by impact ionization and the

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carrier distribution functions are correctly considered, agreement with experimental data is obtained.

Second, the experimental data collected during this work shows that the contribution of oxide defects to the recoverable component depends strongly on the device "history". The experimental characterization shows that mixed NBTI/HC stress anneals a considerable number of oxide defects and thus dramatically reduces recovery after all kinds of stress conditions, homogeneous NBTI and mixed NBTI/HC. In this context, volatility as a possible mechanism responsible for such a reducution is discussed.

As a conclusion, both degradation mechanisms, NBTI and HCD have an impact on each other. This impact depends on both, stress conditions which trigger physical mechanisms associated with NBTI as well as HCD and previoiusly applied stress or in other words the "history".

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Kurzfassung

Die Zuverlässigkeit von einzelnen Elektronikkomponenten ist unter anderem von bias temperature instability (BTI) und hot-carrier degradation (HCD) beeinflusst. Diese Degradationsmechanismen beeinflussen die Leistungsfähigkeit von einem der wichtigsten Bauteile in elektronischen Schaltkreisen, nämlich dem metal-oxide-semiconductor field-effect transistor (MOSFET). Typischerweise werden BTI und HCD unabhängig voneinander erforscht. Zum Beispiel wird BTI unter homogenen Bedingungen charakterisiert, indem keine Spannung am Drain-Kontakt angelegt wird. Sobald die Spannung am Drain-Kontakt erhöht wird, herrschen immer inhomogenere Bedingungen vor, was zu einem wachsenden Beitrag von HCD zur Gesamtdegradation führt. Obwohl es bekannt ist, dass eine solche gemischte BTI/hot-carrier (HC) Degradation den anwendungsrelevantesten Fall darstellt, gibt es wenige Studien zu der Auswirkung auf die MOSFET-Parameter.

In dieser Dissertation wird eine fundierte experimentelle Untersuchung der Auswirkung von gemischtem negative BTI (NBTI)/HC Stress auf SiON pMOSFET Charakteristika präsentiert. Dies beinhaltet einerseits einen Vergleich zwischen zwei gängigen Messmethoden der Schwellspannungsänderung, nämlich der Messung der Gate-Spannung bei konstantem Drain-Strom und der Messung des Drain-Stromes bei konstanter Gate-Spannung. Es wird gezeigt, dass beide Messmethoden unterschiedliche Ergebnisse des zeitlichen Verlaufes der Schwellspannungsänderung nach gemischtem NBTI/HC Stress liefern. Diese Unterschiede werden ausführlich diskutiert. Andererseits liegt der Fokus auf der Untersuchung der ausheilbaren Degradationskomponente. Interessanterweise beeinflusst gemischter NBTI/HC Stress eben diese sehr stark auf Grund von zwei Effekten.

Der erste Effekt ist die Unterdrückung des Beitrags zur ausheilbaren Komponente von einzelnen Materialdefekten im Oxid unabhängig von deren lateralen Positionen. Bisher wurde angenommen, dass das Ausheilen der Schwellspannungsdegradation nur von den elektrostatischen Bedingungen während der Stressphase abhängt. Auf der Einzeldefektebene bedeutet das, dass aufgrund der inhomogenen Bedingungen im Oxid während gemischtem NBTI/HC Stress hauptsächlich Defekte nahe des Source-Kontaktes zur Ausheilung von der Degradation beitragen. Es wird gezeigt, dass diese Annahme nicht stimmt und dass auch der Beitrag von source-seitigen Defekten unterdrückt wird. Dies

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führt zu einer wesentlich höheren Reduktion der ausheilbaren Degradationskomponente als angenommen. Es wird gezeigt, dass zusätzlich zu den elektrostatischen Bedingungen, im Falle von gemischtem NBTI/HC Stress auch die Ladungsträgerverteilung im Kanal, welche sich auf Grund der inhomogenen Bedingungen und Impact Ionization ändern kann, berücksichtigt werden muss.

Der zweite Effekt betrifft das "Verschwinden" von Defekten auf Grund der Messgeschichte des MOSFETs. Die Experimente zeigen, dass Oxid-Defekte nach vielen Stresszyklen elektrisch inaktiv werden und somit weder zur Degradation, noch zur Ausheilung vom MOSFET beitragen. In diesem Zusammenhang wird der Volatility-Effekt als mögliche Ursache diskutiert.

Zusammenfassend kann gesagt werden, dass beide Mechanismen, NBTI und HCD, einander beeinflussen. Diese Beeinflussung hängt sowohl von den Stressbedingungen, die physikalische Mechanismen auslösen, welche mit NBTI und HCD assoziiert werden, als auch von vergangenem Stress ab.

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1.1. **Lateral planar metal-oxide-semiconductor field-effect transistor (MOSFET) used in complementary MOS (CMOS) technology:** The cross section of a p-channel MOSFET (pMOSFET) is shown in the left panel. Two highly p-doped source and drain regions separated by an n-doped body region (e.g. Si) and an insulating layer (e.g. silicon oxynitride SiON) separating the gate contact from the body. The right panel shows a circuit schematics of a CMOS inverter, which is a widly used application of MOSFETs in digital circuits. 2

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2.15. **Region of defects actively contributing to the degradation and recovery in an NBTI setting:** Defects whose energy levels are located in the active energy region (AER) are neutral prior stress, can be potentially charged during stress and discharged again during recovery. Furthermore, the defect energy band is chosen in such a way that the contribution of defects located in right half of the oxide dominates the degradation. Figure source: [16]. 31

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2.24. **Schematic Hydrogen release mechanism:** At the gate side a proton is trapped. During stress, the trap level can be shifted below the Fermi level, which makes it possible for the proton to be neutralized. This neutrally charged hydrogen atom can now be released by overcoming a barrier and move towards the channel side. The empty trap site can potentially be refilled by H released from the gate. This process should be strongly temperature dependent. Figure source: [74]. 40

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2.33. **Narrowing of the active energy region from source to drain:** Due to the inhomogeneous oxide electric field (E_OX) in the case of mixed NBTI/HC stress, the active energy region narrows from source to drain. Therefore, less defects contribute to degradation and recovery at the drain-side than at the source-side. 57

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Chapter 1

The Transistor

With the first analysis of electricity more than 200 years ago and the enhanced insight into the physical process of electric charge manipulation the way to revolutionary technological inventions was enabled. Although many inventions were considered fundamental research and initially ignored by industry, some of these have eventually changed our way of living and as such are of enormous economic importance. A rather prominent example is the transistor, which is one of the key inventions of modern society, arguably comparable to the domestication of fire and the invention of the wheel.

As a result of basic research on the physics of solids, transistors were able to replace vacuum tubes in the 1950s. In the following, this led to the development of the integrated circuit and the microprocessor, which are at the heart of modern electronics. Thus, transistors paved the way for a new generation of powerful and efficient electronic devices with a seemingly unlimited number of applications in everyday life. As a consequence of the continuous improvement of their performance, modern technologies have enabled numerous innovative ways of global networking by connecting things and people, optimizing work flows as well as saving valuable resources.

The economic importance of these new technologies and the pressure to keep production costs low have been the driving forces for the development and improvement of the transistor. In 1965, Moore predicted an exponential relationship between circuit complexity (number of transistors per area unit) and time, by stating that "the complexity will double annually." This prediction has in the meantime been revised to a doubling every two years [1], resulting in over 5 billion transistors being processed on a single chip today. As a consequence of the complexity increase, transistors have been downscaled to the deca-nanometer regime during the past decades, which has resulted in reliability issues, power loss and instabilities as the physical limits are approached.

As an introduction to this thesis, a short overview of the consequences that have resulted from downscaling combined with the motivation to study degradation mechanisms in transistors is given.

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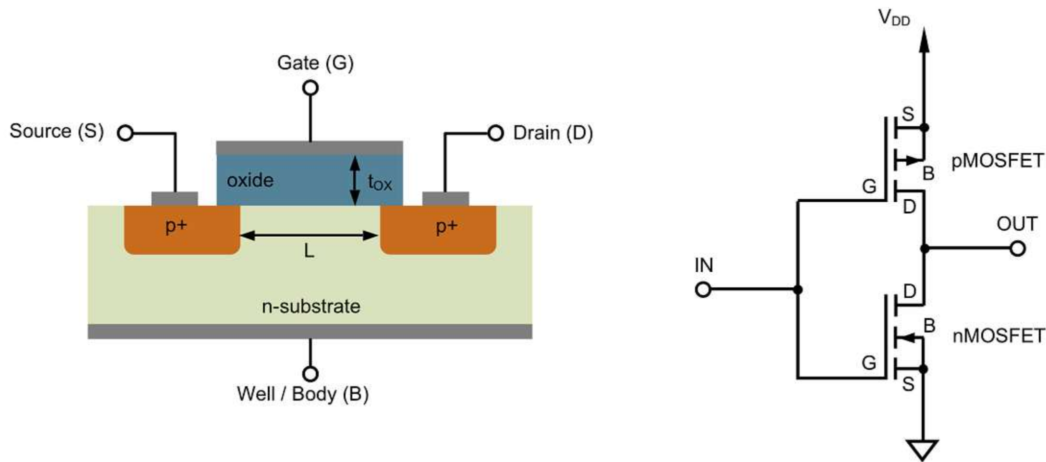

Figure 1.1.: Lateral planar MOSFET used in CMOS technology: The cross section of a pMOSFET is shown in the left panel. Two highly p-doped source and drain regions separated by an n-doped body region (e.g. Si) and an insulating layer (e.g. silicon oxynitride SiON) separating the gate contact from the body. The right panel shows a circuit schematics of a CMOS inverter, which is a widly used application of MOSFETs in digital circuits.

1.1. The Transistor in Digital Circuits

Since the transistor has been invented, an enormous diversity of transistor technologies has arisen, each of them developed for a different purpose. As examples for the numerous purposes, the basic function of a bipolar junction transistor (BJT) is to amplify current in electronic circuits, the insulated-gate bipolar transistor (IGBT) is a power semiconductor device primarily used as an electronic switch in power electronics and the field-effect transistor (FET) acts like a switch in digital circuits. Particularly the metal-oxide-semiconductor field-effect transistor (MOSFET) is one widely used transistor technology in digital circuits due to the achievable short switching times and the nearly loss-less control at low frequencies. In the present work, MOSFETs were studied exclusively.

The MOSFET in digital circuits can be compared to a switch realized by modifying the conductivity properties of semiconductors. Figure 1.1 shows the cross section of a pMOSFET containing two highly p-doped regions, source and drain, separated by an n-doped body region. An insulating layer (e.g. amorphous silicon oxynitride SiON) is sandwiched between the gate and the body, separating them from each other. Therefore, the gate electrode (metal or polysilicon), the insulating layer and the substrate form the MOSFET capacitor, which prevents a current flow and enables a loss-less control of the MOSFET. Assuming that this capacitor is ideal (no charges in the oxide, resistivity of the oxide is infinite) the MOSFET function can be explained based on the band diagrams shown in Figure 1.2.

In the case of a pMOSFET, a positive gate voltage (V_G) accumulates the majority carriers of the substrate, which are electrons, in a layer near the oxide/substrate

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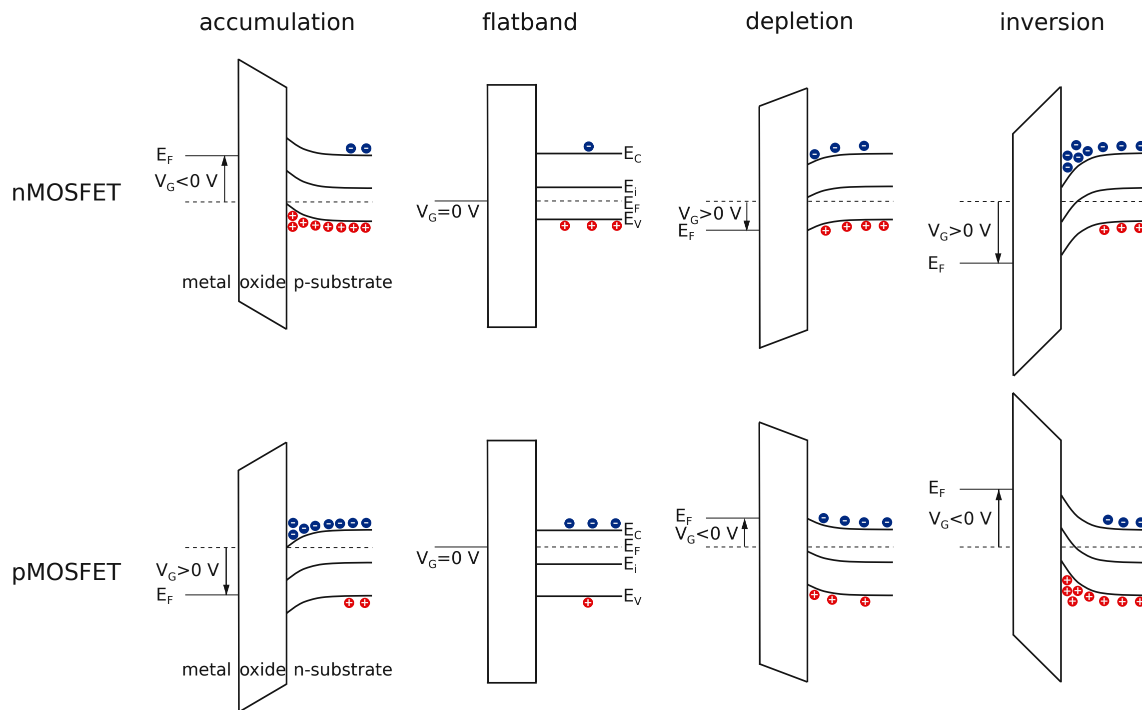

Figure 1.2.: The energy band diagrams for an ideal MOSFET capacitor: Under different bias conditions the MOSFET can be driven from accumulation (left) to inversion (right). **Top:** nMOSFET **Bottom:** pMOSFET

interface. In the band diagram shown in Figure 1.2, this means that the conduction band (E_C) bends down towards the Fermi level (E_F). When sweeping V_G towards zero, the MOSFET reaches its flatband condition for $V_\mathrm{G} = 0\,\mathrm{V}$ (ideal capacitor, otherwise the contact voltage must be considered), where the majority and minority carriers are in thermal equilibrium. By applying a low negative V_G the majority carriers are forced away from the interface and therefore a depletion layer near the interface forms, which results in a bending up of the bands and the intrinsic energy (E_i) moves closer to E_F. With further increasing negative V_G, the depletion layer is populated by minority carriers until V_G exceeds a certain threshold voltage (V_th) and the concentration of minority carriers is high enough to form a thin inversion layer near the interface. In the band diagram the inversion mode can be explained by a crossing of E_i and E_F where the minority carriers exceed the majority carriers at the interface. In this context it has to be mentioned, that V_th is defined as a microscopic parameter which indicates the transition to the inversion mode.

As a consequence, if the supply voltage (V_DD) is applied between the drain and the source, V_G controls the drain current (I_D) as seen in the transfer characteristics (I_D-V_G) shown in Figure 1.3 for an nMOSFET. If $V_\mathrm{G} = 0\,\mathrm{V}$, the MOSFET is in its off-state and current flow is inhibited because of the reverse biased p-n junction. As soon as a positive V_G is applied and increased an I_D can flow due to the inverted interface until it reaches the saturation which corresponds to the on-state of the pMOSFET. This basic function

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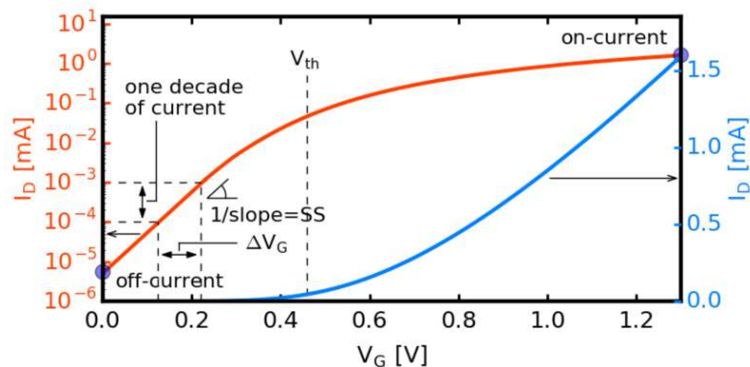

Figure 1.3.: Typical transfer characteristics of an nMOSFET: Drain current I_{D} plotted against gate voltage V_{G} on a log-lin (red, left scale) and a lin-lin (blue, right scale) scale. Off-current (current flowing when MOSFET is switched off), subthreshold slope (slope of the subthreshold region in a log-lin plot), threshold voltage (I_{D} where the inversion layer is formed) and on-current (current flowing in the on-state) are the most important parameters characterizing the I_{D}-V_{G}.

of a MOSFET makes it quite advantageous for processing of digital signals in circuits as shown in Figure 1.1 for the digital stage of a CMOS inverter. For this example, the nMOSFET is in its on-state in the case that the input is at a digital high level while the pMOSFET is in its off-state. As a result, the output voltage is at ground (digital low level). By contrast, if the input voltage is near zero, the nMOSFET is in its off-state while the pMOSFET is conductive, which results in an output voltage at V_{DD} (digital high level). This corresponds to inverting a digital signal.

Due to the imperfections of real devices, the CMOS technology allows for deviations from the perfect digital low level at ground and the digital high level at V_{DD} by defining the first as a voltage between $0\,\mathrm{V}$ and $1/3\,V_{\mathrm{DD}}$ and the second as a voltage between $2/3\,V_{\mathrm{DD}}$ and V_{DD}. Thus, a reliable and proper signal processing requires digital low and high levels within these margins at a low circuit power consumption, which implies some limitations for the MOSFET design. These limitations can be explained based on the characteristics of a real device as shown in Figure 1.3. The I_{D}-V_{G} of a MOSFET is typically characterized by four parameters determined by materials, doping and geometry: the off-current, the sub-threshold swing (SS) (reciprocal value of the sub-threshold slope (S) in a log-lin plot), V_{th} (in this case a macroscopic parameter corresponding to, e.g., the gate voltage at which a certain I_{D} flows) and the on-current. The off-current ($I_{\mathrm{D}}{\neq}0\,\mathrm{A}$ at $V_{\mathrm{G}}{=}0\,\mathrm{V}$) is caused by leakage currents between source and drain and is inevitable. Furthermore, the switching process between off- and on-state shows switching dynamics characterized by V_{th} and SS which are limited to certain minimum values. At this point it has to be mentioned that several definitions for the extraction of the macroscopic parameter V_{th} exist [2] which contradicts the definition of V_{th} as the gate voltage where inversion is satisfied. While V_{th} as a macroscopic parameter is extracted from the transfer characteristics and is based, e.g., on an I_{D} threshold or on the maximum transconductance, V_{th} as a microscopic parameter defines the transition from accumula-

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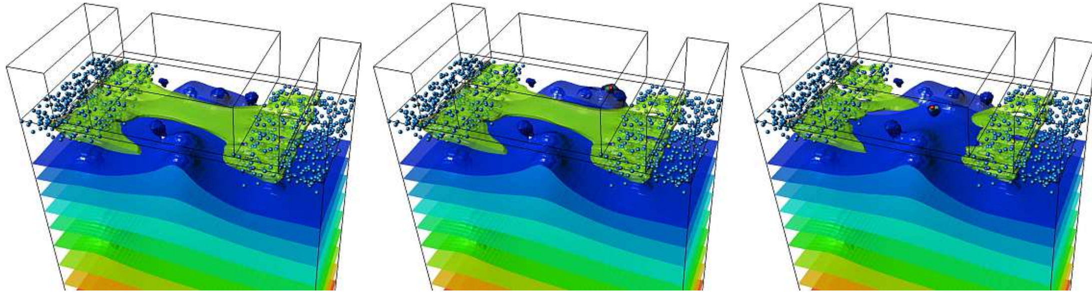

Figure 1.4.: Percolation path: A single percolation path formed by random discrete dopants (current flow shown in the uppermost layer) and contours of constant potential in a pMOSFET: **Left:** current flow without a disturbance due to charge exchange events caused by oxide defects. **Center:** reduced current flow when a defect located beside the percolation path traps a charge carrier. **Right:** disturbance of the current flow when a defect located directly in the center of the percolation path traps a charge carrier. [3]

tion to inversion. The latter depends on the lateral position due to non-uniform doping profiles along the channel.

These parameters have to meet certain requirements in order to ensure a correct interaction of the MOSFET with other circuit components. For example, clearly distinguishable digital levels require a ratio between on- and off-current which is as large as possible. This can be achieved by maximizing V_{DD} while simultaneously keeping SS and V_{th} as low as possible. Besides increasing the ratio, a high V_{DD} would also ensure an on-current which is high enough to drive subsequent digital stages, and low SS and V_{th} would enhance the switching dynamics. However, increasing V_{DD} conflicts with the requirement of low power consumption since $P \propto V_{\mathrm{DD}}^2$ and, as mentioned in the previous paragraph, SS and V_{th} are either fundamental limits or limited due to materials, doping and geometry of the MOSFET.

The consideration of these aspects in the fabrication process provides fundamental challenges for the design of MOSFETs in general. However, excessive scaling of the MOSFET geometries has led to further challenges.

1.2. Scaling Trend of MOSFETs and Challenges

While decades ago transistor structures were processed in the micrometer range, modern transistor structures have been scaled down to 22 nm in 2008 and to 14 nm or even less in the current generation of transistors [4]. In addition to the scaling of the gate width (W) and gate length (L) of the transistors, the oxide thickness (t_{OX}) has also been scaled down, reaching values of less than 2 nm, which corresponds in fact to a rather small number of atom layers.

The scaling of the geometry results in several design and fabrication challenges. For example:

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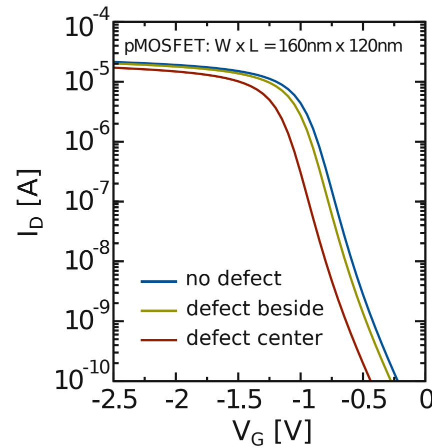

Figure 1.5.: Schematic transfer characteristics of a pMOSFET for the three cases shown in Figure 1.4. The more the current flow is disturbed by a trapped charge carrier, the more V_{th} shifts, the subthreshold slope decreases and the on-current reduces.

- A short transistor length (less than 100 nm) leads to short-channel effects, e.g., drain-induced barrier lowering, which affects the MOSFET performance. Moreover, channel leakage currents are more pronounced, therefore, the off-current increases significantly

- Considering that the oxide capacitance (C_{OX}) is proportional to the ratio between channel area (A) and t_{OX}, where $A{=}L{\times}W$, t_{OX} has to be downscaled in the same manner as A. Otherwise, C_{OX} would increase significantly which would have a considerable impact on V_{th} and the switching dynamics. However, t_{OX} is limited to a certain minimum value because of quantum effects like tunneling, leading to a dramatic increase of leakage currents if the oxide thickness is further reduced. With a t_{OX} below this value, a loss-less control cannot be ensured any longer.

- As a consequence, the oxide electric field (E_{OX}) has increased considerably due to the indirect proportionality to t_{OX}. E_{OX} could be decreased by a decrease of V_{DD}. However, due to the limited subthreshold slope, the supply voltages cannot be scaled in the same manner as the device geometry without affecting the ratio between the on- and off-currents. As a consequence, degradation effects depending on E_{OX}, e.g., the bias temperature instability (BTI), have a greater impact in downscaled devices than in devices with thicker oxides.

Another consequence of downscaling is a higher device variability due to the variance of parameters between transistors processed in the same manner. This is because nanoscale devices contain, in contrast to large devices, only a countable number of discrete dopants. Therefore, the slightest deviations of their number or position influence the non-uniform current flow over the width, the so-called percolation path as shown in Figure 1.4 left [3, 5]. Furthermore, the relative deviation of device dimensions due to

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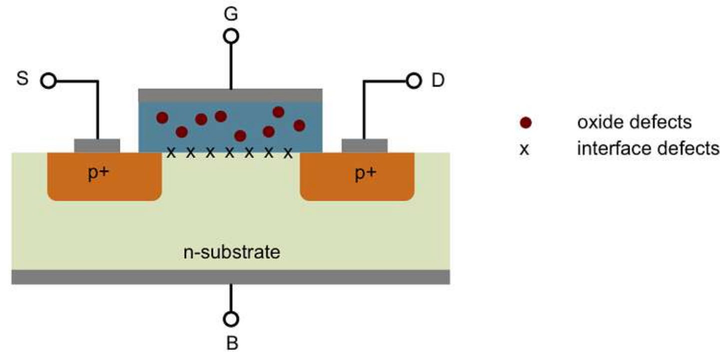

Figure 1.6.: Two defect types in MOSFETs: Defects can be defined as deviations within the short-range order of the atomic structure. Interface defects occur due to dangling bonds at the interface between the crystalline substrate and the amorphous oxide. Oxide defects can be either vacancies, e.g., the oxygen vacancy, or bridging atoms, e.g., the H bridge, hydroxyl-E′ center.

fabrication variability increases with scaling. As a result of both, the variance of discrete dopants and dimension deviations, even transistors of the same technology and processed in the same manner show a significant variance in their characteristics, like V_{th}. This variance results in an increased ratio between defective and functional devices and affects the performance of circuits detrimentally [6].

Additionally, any real device contains structural defects, for example, impurities, interstitials, vacancies and dangling bonds. Two of the most important defect types are shown in Figure 1.6, interface defects and oxide defects. While both are considered the main cause of device degradation, oxide defects are the main focus of this thesis. Both have energetic states within the band diagram shown in Figure 1.2 and are capable of exchanging charge carriers with the valance or conduction band of the substrate.

Interface defects occur when interfacing different materials, like crystalline Si and amorphous SiON. Such material transitions result in an interface region containing trivalent Si dangling bonds. Such interface states known as P_{b}-centers, which are amphoteric traps and act as donors as well as acceptors [7, 8]. Typically they act as traps for electrons and holes and distort the device characteristics detrimentally. Charge exchange between interface states and the substrate is consistent with the Shockley-Read-Hall (SRH) theory [9]. In order to ensure a proper MOSFET function, such interface defects have to be reduced considerably. This reduction is realized by a passivation of the dangling bonds by hydrogen (H) during a processing step of forming gas annealing.

Oxide defects are intrinsic defects and can be either vacancies, e.g., the oxygen vacancy, or bridging atoms, e.g., the H bridge. Phenomenologically they are classified in defects near the interface, also called border defects or defects away from the interface [10, 11]. Microscopically the border defects are often associated with E' centers, which are trivalent silicon dangling bonds in the oxide [8] or hydrogenic defects [12]. Similar to the interface defects, defects in the oxide also can distort device characteristics due to

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charge exchange events with the substrate. Such charge exchange is consistent with non-radiative multiphonon processes [13, 14, 15].

Due to the comparatively large C_{OX} in devices with large A, a single capture or emission event caused by an oxide defect has a small impact on the MOSFET parameters. In stark contrast, in nano-scale MOSFETs with dimensions around 100 nm or smaller, containing just a handful of defects such events affect device performance severely [16, 17, 18]. Depending on the position of the defect, the percolation path is disturbed as can be seen in the center and right panels of Figure 1.4. Charge exchange events of defects located near or in the percolation path cause a V_{th} shift, a degradation of the subthreshold slope and a reduction of the on-current as summarized in Figure 1.5. Even one single active defect may shift V_{th} by a detrimental value, and thus, change the transistors behavior and dynamics in digital circuits dramatically. Such a shift of transistor characteristics can endanger the correct interaction with other components, which makes the circuit less reliable and more likely to fail.

1.3. Reliability

A reliable MOSFET meets the requirement of correct interaction with other circuit components. Unfortunately, even under nominal operating conditions, this correct interaction cannot be ensured at all times. So-called degradation mechanisms, which are associated with shifts of the device characteristics, endanger the correct interaction and reduce the time-to-failure of integrated application. The physical processes responsible for these mechanisms are in the focus of the device reliability research field, including the characterization, understanding and modeling of, e.g., BTI, hot-carrier degradation (HCD), stress induced leakage current (SILC) and trap assisted tunneling. Only with a deep understanding of how degradation is caused, advanced simulations based on realistic models can ensure a robust circuit design. Moreover, such a fundamental knowledge is a great advantage for future transistor designs to prevent instabilities.

The focus of this thesis lies on the experimental characterization of degradation mechanisms. In this context, numerous methods and sequences have been introduced. Each of these methods and sequences is suitable for the characterization of a certain parameter or physical quantity. For example, charge pumping (CP) allows for the characterization of interface defects, whereas time-dependent defect spectroscopy (TDDS) is suitable for the characterization of single oxide defects. The methods and sequences are discussed in Chapter 3 in detail.

In general, degradation has been shown to consist of a recoverable and a permanent component. While, for example, the recoverable component of BTI is attributed to oxide defects, which capture and emit charge carriers, HCD is suspected to be determined by breakage of H passivated Si dangling bonds at the substrate/oxide interface, typically associated with a permanent component of degradation. Both degradation mechanisms are typically studied in an idealized setting and independently from each other [16, 19, 20, 21, 22, 23, 24] as discussed in Chapter 2. In particular, for BTI studies no voltage is applied to the drain, leading to homogeneous degradation. With increasing drain bias,

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the degradation becomes more and more inhomogeneous and the contribution of HCD to the total degradation increases. Even though it is well understood that this mixed degradation corresponds to the situation in real circuits, there is only a limited number of studies available on the impact of the mixed stress conditions [25, 26, 27]. Additionally, defect creation, annealing, activation, and deactivation as well as secondarily generated carriers and non-equilibrium effects play an important role.

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Chapter 2

Degradation Mechanisms

The term of degradation is associated with unwanted shifts of certain MOSFET characteristics which can endanger the correct interaction with other circuit components in digital circuits. For example, drifts of V_{th}, also called threshold voltage shift (ΔV_{th}), during operation seriously reduce the time-to-failure of integrated applications. Degradation phenomena like stress induced leakage current (SILC), time-dependenc dielectric breakdown (TDDB), bias temperature instability (BTI) and hot-carrier degradation (HCD) describe the origins of these uncontrolled drifts. Especially the last two are commonly listed as the most prominent challenges which have to be properly understood [4]. In order to meet these challenges, advanced simulations based on physical models are required for a robust design of circuits.

Throughout the process of understanding and modeling degradation mechanisms, different pieces of the puzzle have been put together in order to get the big picture. In this thesis, one important piece of the puzzle in the context of BTI and HCD and their interplay is contributed. Therefore, the theoretical background and state of the art modeling attempts are introduced in this chapter.

2.1. Bias Temperature Instability

The phenomenon BTI has been known for more than 50 years [16, 28, 29, 30] and describes basically the temperature and gate bias, or in other words the oxide electric field (E_{OX}), dependent shift of transistor parameters. For example, at BTI conditions the transconductance (g_{m}), the linear drain current ($I_{\mathrm{D,lin}}$), the saturation drain current ($I_{\mathrm{D,sat}}$) and the channel mobility (μ_{eff}) decrease while the sub-threshold swing (SS), the off-current and V_{th} increase as shown in Figure 2.1. Further, as devices have been downscaled, the vulnerability to BTI has increased. The oxide field at nominal operating conditions has increased due to the scaling of t_{OX}, the nominal operating temperature has increased due to the higher power dissipation, and charge exchange events of single defects have a detrimental impact on the MOSFET electrostatics. All these aspects

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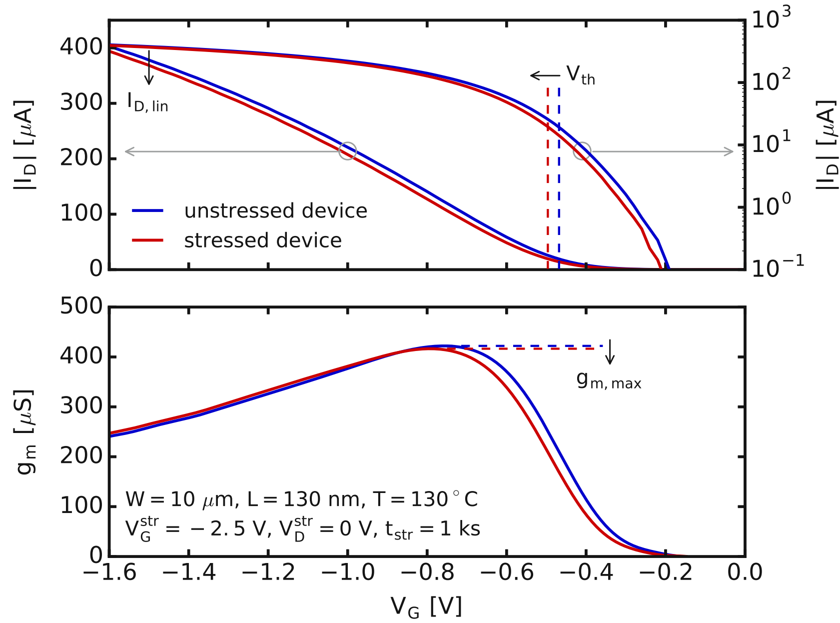

Figure 2.1.: Transfer characteristics and transconductance of a large-area pMOSFET after NBTI stress: The I_D-V_G (top) is recorded in the linear region for $V_\mathrm{D} = -0.1\,\mathrm{V}$ and the transconductance is extracted (bottom). After 1 ks of NBTI stress, the V_th is shifted and $I_\mathrm{D,lin}$ as well as $g_\mathrm{m,max}$ are reduced.

together with the challenge of keeping pace with the downscaling of device dimensions have led to several modeling attempts, which are introduced in this section.

2.1.1. Experimental BTI Characteristics

Although BTI affects all device parameters, as it is shown illustratively in Figure 2.1, it is commonly studied and expressed in terms of an equivalent ΔV_th since BTI affects the threshold voltage significantly. Typically, BTI is characterized as a gate bias is applied to the gate contact while drain, source and well contacts are at ground. In experiments BTI is classified according to the sign of the gate bias, namely NBTI if a negative V_G is applied and positive bias temperature instability (PBTI) if a positive V_G is applied, commonly studied in pMOSFETs and nMOSFETs, respectively. By contrast, the study of NBTI in nMOSFETs and PBTI in pMOSFETs receives less attention due to the difficulty of the experimental characterization. This is because most of the transistors are protected against electrostatic discharge, which is realized by a diode. This allows only for the operation in inversion mode but not in accumulation. Thus, in most real devices of a commercial technology it is not possible to study NBTI in nMOSFETs and PBTI in pMOSFETs.

Both, NBTI and PBTI, are usually characterized at accelerated stress conditions, which allow for obtaining meaningful parameter shifts within feasible experimental time slots of minutes, days or weeks instead of years. Such accelerated stress is associated

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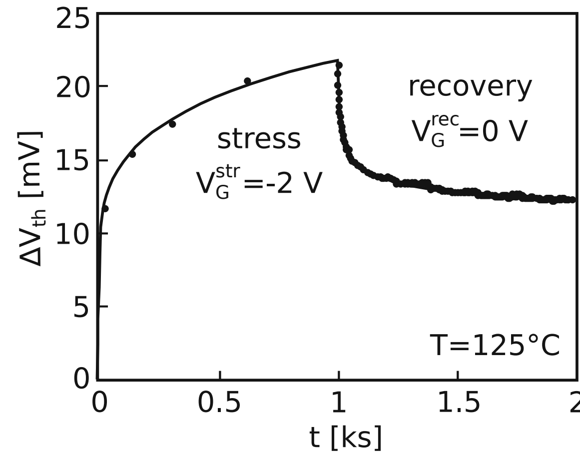

Figure 2.2.: Shift of the threshold voltage during stress and recovery: ΔV_{th} during stress and recovery of a FinFET is shown. During stress ΔV_{th} increases and decreases again as soon as the stress bias is removed. Figure source: [31].

with V_{G} above nominal operating conditions and elevated temperatures, e.g., 80–150 °C. Most of the BTI studies in this regard are realized by the on-the-fly (OTF) method, the measure-stress-measure (MSM) or the extended measure-stress-measure (eMSM) method. Although these methods are discussed in the Sections 3.1, 3.4 and 3.5 in detail, they are introduced in this subsection briefly.

- MSM measurements are realized by short interruptions of the applied gate and drain voltages in order to characterize the degradation state of the device, e.g., by taking an I_{D}-V_{G} curve. From this, the monitored parameter is extracted and the degradation and/or recovery over time is obtained.
- The OTF method obtains ΔV_{th} during operation without interruption of the applied voltages. By a periodic modulation of the gate voltage at stress conditions ($V_{\mathrm{G}}^{\mathrm{str}}$) at a certain V_{D} and simultaneous monitoring of I_{D}, ΔV_{th} can be estimated at a stress level.
- The eMSM method comprises of basically three phases. First, the unstressed device is characterized by taking an I_{D}-V_{G}. Subsequently, $V_{\mathrm{G}}^{\mathrm{str}}$ typically higher than nominal operating conditions is applied for a certain stress time (t_{str}). Finally, the recovery is obtained with the gate voltage set to recovery conditions ($V_{\mathrm{G}}^{\mathrm{rec}}$) near V_{th} or below by monitoring the evolution of ΔV_{th} over a certain recovery time (t_{rec}) without interruption of the applied voltages.

The impact of a stress and a recovery bias on V_{th} of a FinFET is illustrated in Figure 2.2. During stress, V_{th} drifts and ΔV_{th}, being the difference between the current V_{th} and the threshold voltage before stress ($V_{\mathrm{th,0}}$), increases while it decreases again as soon as the stress is removed. The decrease of ΔV_{th} is also called recovery or relaxation. The sign of ΔV_{th} illustrated on a linear scale, as in Figure 2.2, commonly corresponds to

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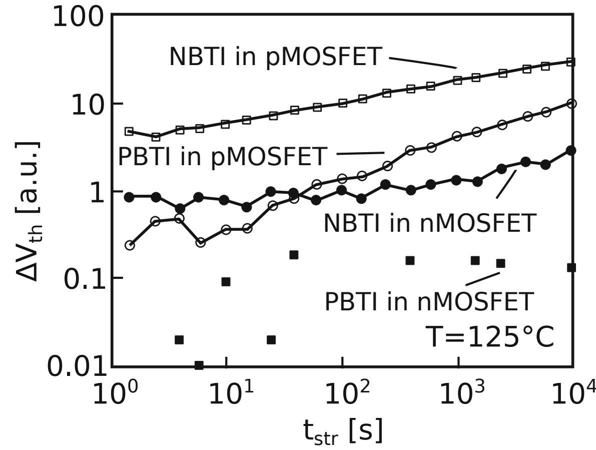

Figure 2.3.: Shift of the threshold voltage under NBTI and PBTI stress: Both BTI classifications for SiO_2 nMOSFET and pMOSFET. NBTI stress conditions with $V_G < 0\,V$ have the greatest impact on pMOSFET. Figure source: [32].

whether an n-channel or a p-channel device is probed and whether the absolute value of V_{th} increases or decreases. In the case that $|V_{th}| > |V_{th,0}|$, ΔV_{th} is negative for p-channel devices and positive for n-channel devices while it has the opposite sign for both in case that $|V_{th}| < |V_{th,0}|$. If $|V_{th}|$ drifts towards larger $|V_G|$, which is typically associated with the term of degradation, ΔV_{th} drifts to more negative values for p-channel devices and more positive values for n-channel devices. By contrast, the dynamics show the opposite trend if $|V_{th}|$ shifts towards smaller $|V_G|$, which is typically associated with a recovery of the degradation.

The particular behavior of ΔV_{th} over time during stress and recovery strongly depends on whether NBTI or PBTI is applied and on almost every device characteristics and probe condition, namely t_{OX}, E_{OX}, temperature, W and L, transistor type and many more. Useful for the further discussion, the most important dependencies are introduced briefly, starting with the fact that NBTI and PBTI have considerably different impacts on ΔV_{th} [32]. A characterization of these different impacts for an SiO_2 oxide can be seen in Figure 2.3. While NBTI ($V_G < 0\,V$ applied) has the greatest impact on pMOSFETs, PBTI ($V_G > 0\,V$ applied) nearly does not affect nMOSFETs. Based on this, it is not surprising that the most studied case is NBTI on pMOSFETs. In the following, the focus is mainly on NBTI on pMOSFETs.

Moreover, the evolution of ΔV_{th} is affected by the gate bias applied during stress as well as during recovery as illustrated in Figure 2.4. Based on the impact of V_G^{str} and the gate voltage at recovery conditions (V_G^{rec}) on ΔV_{th} measured for a large-area SiON pMOSFET it can be seen that while a higher V_G^{str} accelerates the increase of ΔV_{th} over time a higher V_G^{rec} suppresses the recovery of ΔV_{th} [33].

Similar to the acceleration of the V_{th} shift over time due to a higher gate bias at stress conditions, degradation is also accelerated because of an elevated temperature (T). In this regard, Figure 2.5 shows that the degradation of ΔV_{th} is higher and changes

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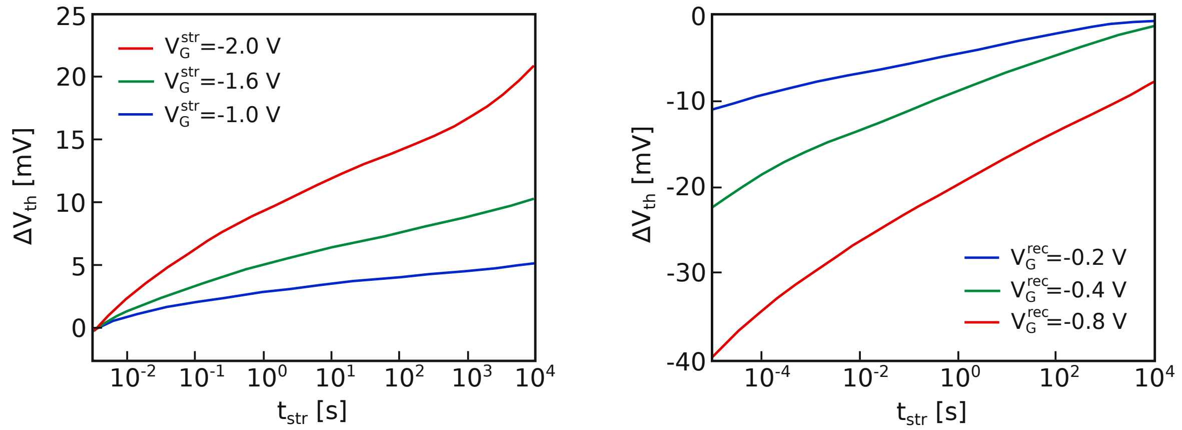

(a) The ΔV_{th} behavior depends strongly on $V_{\mathrm{G}}^{\mathrm{str}}$. With increasing $V_{\mathrm{G}}^{\mathrm{str}}$ the absolute value of ΔV_{th} increases.

(b) The ΔV_{th} behavior depends strongly on $V_{\mathrm{G}}^{\mathrm{rec}}$. With increasing $V_{\mathrm{G}}^{\mathrm{rec}}$ the device recovers less.

Figure 2.4.: Bias dependence of the threshold voltage shift over time: measured on a large-area SiON pMOSFET with L and W in the range of µm during (a) stress for different $V_{\mathrm{G}}^{\mathrm{str}}$ and (b) during recovery after the same $V_{\mathrm{G}}^{\mathrm{str}}$ at different $V_{\mathrm{G}}^{\mathrm{rec}}$. Figure source: [33], smoothed.

faster with elevated T [33]. By contrast, the ΔV_{th} recovery shows only a weak, almost negligible, temperature dependence for large-area devices, which is not shown here.

All shown dependencies on gate bias and temperature are different for different device dimensions and different architectures. While the latter are not discussed in detail here, the changes in device dimensions together with the limitations in time of the experimental window are quite important in regard of understanding the different approaches of modeling device degradation. For an explanation, one should take a look at the lower limit of the experimental window during stress ($t_{\mathrm{str,min}}$) of the measurements in Figure 2.3 and Figure 2.5. This lower limit is 1 s and 10 s, respectively, which are common lower limits in literature until approximately 2004. The reason lies in the measurement sequences for the characterization of degradation. The interruptions of the applied voltages using the MSM method, although as short as possible, can take 50 ms or more and disturb the degradation or recovery state seriously. Due to such a distortion of the degradation or recovery state the MSM method often cannot capture short-term effects because the interruption of the applied voltages might reverse their impact on device characteristics. This makes reliable short-term measurements ($t_{\mathrm{str}} < 1\,\mathrm{s}$ or $t_{\mathrm{rec}} < 1\,\mathrm{s}$) impossible.

As a result, for a long period of time models were developed based on mainly long-term ΔV_{th} measurements from 1 s to nearly 10 ks. The long-term characterization, at a first glance and in a very simplified way, shows that ΔV_{th} in stress measurements of large-area devices has power-law-like behavior. Thus, simple empiric models based on a power-law-like life-time estimation as shown in Figure 2.5 have been popular [32, 34, 35, 36].

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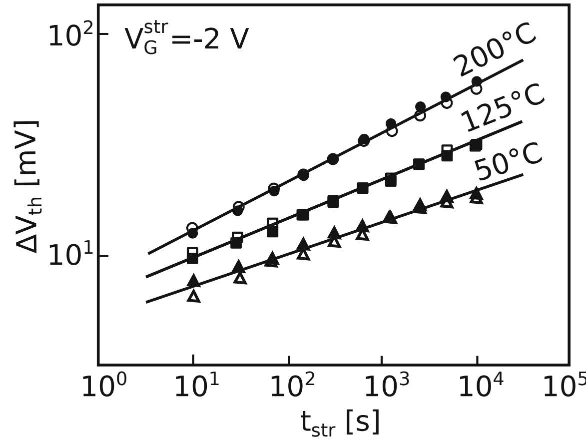

Figure 2.5.: Temperature dependence of degradation at the same stress bias: T accelerates the degradation of ΔV_{th}, which is shown here for a FinFET at three different temperatures (open and closed symbols; two similarly processed wafers). The data is described by a power-law dependence. Figure source: [31].

The power-law covers a stress bias dependent pre-factor, a temperature dependence following an Arrhenius' law and the power-law in time. Based on this, the ΔV_{th} can be extrapolated in order to estimate the parameter shift over time. However, such an empirical description is quite inaccurate and overestimates the ΔV_{th} over time because it neither describes the short-term behavior for stress times below 1 s nor the very long-term behavior for stress times larger than 10 ks nor recovery effects due to interruptions of the stress properly as discussed in the following.

2.1.2. The Reaction-Diffusion Model

Beside the empirically found power-law as an attempt to estimate the life-time of a transistor, also physics-based models have been introduced in order to describe the processes leading to device degradation. A widely accepted model in this regard is the reaction-diffusion model. This model is capable of reproducing the time evolution of device degradation of large-area MOSFETs. It was introduced in 1977 [30] and continuously adapted [32, 37, 38]. The basic assumption of the reaction-diffusion model is that Si-H bonds at the interface between the substrate and the oxide can be broken by NBTI stress, schematically shown in Figure 2.6. Consequently, the remaining Si dangling bonds (interface-states or interface-traps) are positively charged, which can be expressed by a interface-charge density (N_{it}), and the hydrogen atom diffuses into the dielectric where also other H related species can be created like for example a H_2 molecule. Further, H can also recombine with the positively charged Si dangling bond, thus the bond is again passivated.

As soon as experimental characterization methods were improved and capable of measuring short-term effects a few inconsistencies between the reaction-diffusion model and the experimental data arose. In the context of the improvement of measurement meth-

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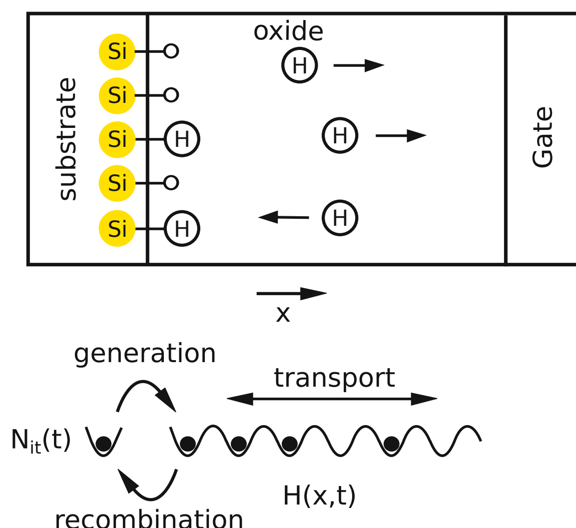

Figure 2.6.: Schematic illustration of the classical reaction-diffusion model of NBTI: Si-H bonds at the interface between the substrate and the oxide are broken during NBTI stress. Neutral H, expressed by the H density $H(x, t)$, diffuses into the oxide and leaves behind positively charged interface states. H diffusion proceeds via shallow hopping sites in the oxide shown as a regular network of potential wells. Figure source: [31].

ods, three aspects have to be mentioned: the characterization of the recoverable component of BTI, the continuous application of stress and the broadening of the experimental window. As an explanation, in Subsection 2.1.1 it is mentioned that as soon as the stress bias is removed a recovery effect of ΔV_{th} is measured. As long as the stress and recovery in MSM measurements are interrupted in order to record a transfer characteristic for the extraction of V_{th} the overall degradation and recovery state will be different than if the stress and recovery biases are applied continuously. Therefore, innovative measurement methods have been introduced, which can obtain ΔV_{th} without any interruptions of stress or recovery and additionally are capable of the characterization of short-term effects. An example in this regard is the OTF method capable of obtaining the ΔV_{th} degradation without interruptions of the stress bias. However, realized with standard equipment the OTF has an integration time of more than 20 ms in order to achieve a statistical error of ±1 mV in ΔV_{th} [39], which is quite long in the context of short-term measurement. Soon after the OTF method had been proposed, the fast-V_{th} and fast-I_{D} methods were introduced [31, 39, 40]. Such fast methods are based on single point measurements of ΔV_{th} during recovery instead of interruptions in order to record an I_{D}-V_{G}. Either I_{D} or V_{G} is measured at a point near V_{th} during the recovery phase in eMSM measurements and the corresponding ΔV_{th} is extracted. Both will be discussed in detail in Section 3.5. These new methods extended the $t_{\mathrm{str,min}}$ and the lower limit of the experimental window during recovery ($t_{\mathrm{rec,min}}$) to 100 µs or even 1 µs, which allows for a proper short-term characterization of BTI recovery.

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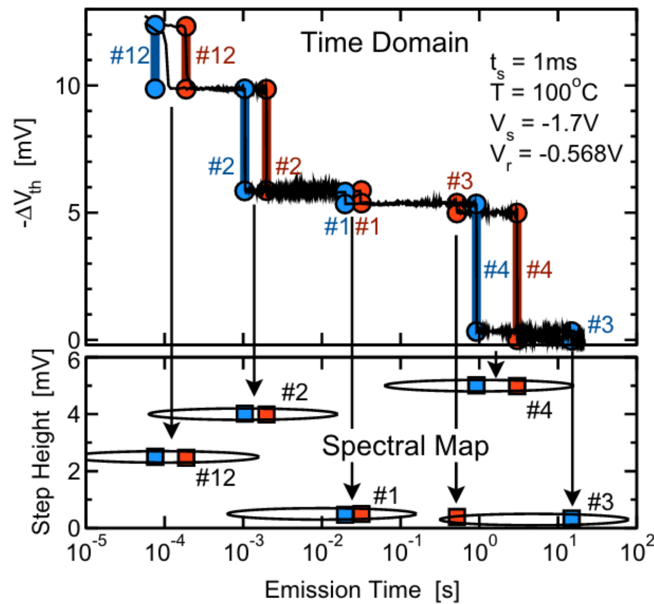

Figure 2.7.: Recovery traces of a nano-scale pMOSFET and the spectral map: Two ΔV_{th} recovery traces of a pMOSFET. **Top:** Recovery proceeds step-wise due to emission events of single defects in the oxide. The symbols mark the extracted emission times and step heights which are nearly unambiguous fingerprints of each defect. **Bottom:** The step heights and the emission time build the spectral map. Figure source: [41].

The improvement of experimental setups and the broadening of the experimental window have led to different insights into degradation mechanisms and the understanding of BTI changed. Some important inconsistencies between the reaction-diffusion model and the experimental data are:

- A $\log(t_{\mathrm{str}})$ behavior of ΔV_{th} for $t_{\mathrm{str}}<1\,\mathrm{s}$ was found. Several investigations [31, 39, 32, 42] have led to the conclusion that not only the creation of interface states contributes to ΔV_{th} during stress but also hole trapping in oxide defects near the interface between substrate and oxide. It has been found that there is evidence that these processes are highly coupled, which is not possible to be explained by the reaction-diffusion model.
- Even after long stress times ($>1\,\mathrm{ks}$) ΔV_{th} can recover more than 60 % within the first second [43]. Since the reaction-diffusion model assumes diffusion-limited degradation, which implies also a diffusion limited relaxation, 60 % of recovery means that 60 % of the hydrogen must diffuse back to the interface and passivate the positively charged dangling bonds within one second. This implies that the backward diffusion happens by orders of magnitude faster than the forward diffusion. This cannot be explained by the effect of diffusion since the diffusivity of H is a material constant.

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- The overall recovery is considerably slower than the degradation during stress as obtained from eMSM measurements [44], which can be understood as an asymmetry of stress and recovery. In this context, the reaction-diffusion theory predicts a relatively short recovery phase (50 % relative recovery as soon as t_{rec}=t_{str}). Thus, the reaction-diffusion model is not capable to model the asymmetry.

- Recovery is a bias-dependent process (shown in Subsection 2.1.1). This is not in agreement with the reaction-diffusion model because it predicts recovery due to the back-diffusion of neutral H_2 and as such is bias-independent.

- It has been shown that interface-states nearly do not recover in the context of MSM measurements [45]. Therefore, the reaction-model, where recovery is explained as passivation of interface-states is not suitable to model recovery.

In order to overcome some of the mentioned inconsistencies, the reaction-diffusion model has been improved over the last two decades including the attempt to describe the diffusion as a dispersive process instead of a classical, i.e., Gaussian-like, process [31, 32, 46, 47].

These improvements notwithstanding, the complicated behavior of ΔV_{th} during stress and recovery has led to the development of the non-radiative-multiphonon (NMP) model as a different approach to explain BTI. For the development of the NMP model two processes played a major role, the improvement of measurement setups as well as the downscaling of MOSFETs. As soon as devices were scaled to the nanometer regime it has been recognized that the recovery of MOSFETs proceeds not continuously as shown in Figure 2.2 but step-wise as shown in Figure 2.7 top.

2.1.3. Properties of Material Defects in Experiments

Back in the 80's, it was found that random fluctuations in the terminal currents are caused by structural defects, also called states or traps, in the bulk oxide. Such fluctuations are due to defects randomly exchanging charge carriers with the substrate [48, 13]. The corresponding noise was introduced as random telegraph noise (RTN). The study of nano-scale devices has shown that device degradation and recovery is determined by single hole capture and emission processes in pMOSFETs, respectively, which is consistent with a first-order reaction-rate but not with a diffusion-limited process [49, 50, 40]. Soon it has been proposed that single oxide defects near the interface between oxide and substrate communicate with the inversion layer in the channel by exchanging charge carriers.

Such charge carrier exchange events, also called capture and emission events, of oxide defects near the interface are a serious perturbance of the electrostatic conditions in nano-scale devices. Considering the average impact of one capture or emission event due to the downscaled device dimensions and the inhomogeneous channel potential due to randomly placed dopants [51], such events cause step-wise measurable shifts in ΔV_{th} experiments. Therefore, each individual defect leaves its fingerprint by the fact that it appears with a certain step height (d), a certain mean value of the capture time (τ_c)

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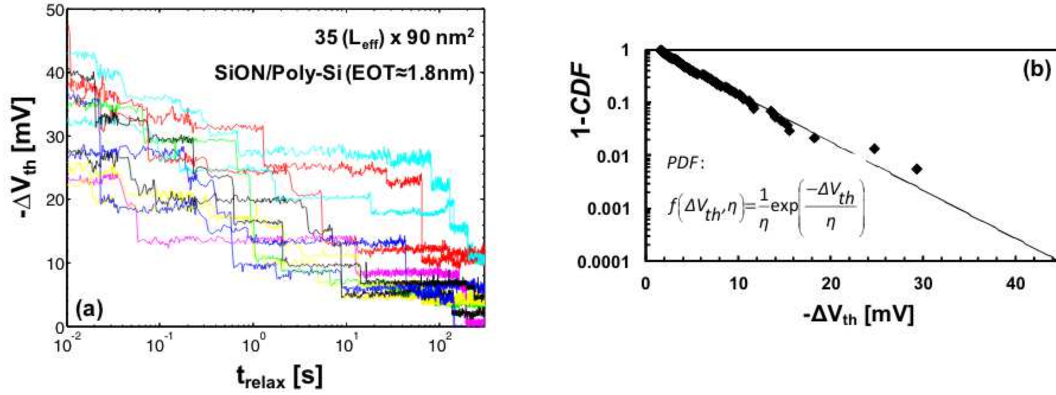

Figure 2.8.: Step height distribution of individual defects: (a) Typical NBTI recovery traces in nano-scale devices. Each step corresponds to a single gate oxide defect discharge event. (b) The ΔV_{th} step heights plotted on CCDF plot. The step heights appear exponentially distributed. Figure source: [18].

and a certain mean value of the emission time (τ_{e}) in ΔV_{th} traces, which depend on the position relative to the dopants, the depth of the defect in the oxide, the gate bias and the temperature. For example, as discussed in Chapter 1, the randomly placed dopants cause the current to flow inhomogeneously from source to drain. As soon as a defect is located right above the percolation path [52], its step height can be considerably larger than estimated from the charge-sheet approximation [53].

In this context, based on the characterization of the step heights caused by single defects, an exponential step height distribution has been found [17, 18, 54, 55, 56] as shown in Figure 2.8. Since this distribution is based on a statistical characterization, the influence of device-to-device variation of the number of oxide defects and random dopants are considered. In detail, the probability density function (PDF) can be expressed as

$$f(\Delta V_{\mathrm{th}}, \eta) = \frac{1}{\eta} \mathrm{e}^{-\frac{\Delta V_{\mathrm{th}}}{\eta}} \tag{2.1}$$

with

f	probability density function
ΔV_{th}	threshold voltage shift
η	mean value of the step height distribution.

The corresponding CCDF is

$$F(\Delta V_{\mathrm{th}}, \eta) = \mathrm{e}^{-\frac{\Delta V_{\mathrm{th}}}{\eta}}. \tag{2.2}$$

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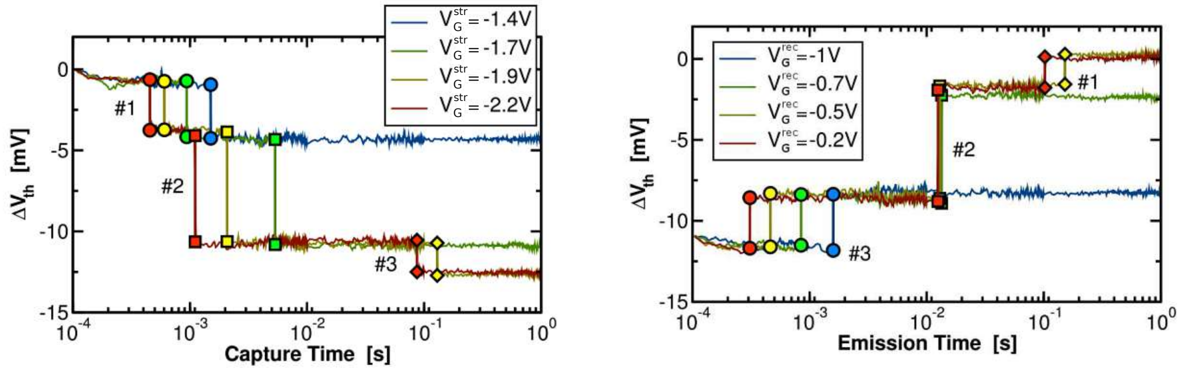

(a) Stress: single oxide defects capture holes from the inversion layer. This process is measureable as single steps at stochastically distributed τ_c around a characteristic mean value, which depends strongly on V_G^{str}. With increasing V_G^{str}, τ_c decreases.

(b) Recovery: single oxide defects emit the holes to the depletion layer. This process is measureable as single steps at stochastically distributed τ_e around a characteristic mean value, which depends strongly on V_G^{rec}. With increasing V_G^{rec}, τ_e increases.

Figure 2.9.: Bias dependence of the capture and emission time: Three defects enumerated with 1, 2 and 3 in an SiON pMOSFET with L and W in the range of 100 nm are characterized during (a) stress for different V_G^{str} and (b) during recovery after the same V_G^{str} at different V_G^{rec}. Similar to the the measurements in large-area devices (Figure 2.4) the over all ΔV_{th} of nano-scale MOSFETs depends on V_G. Figure source: [33].

The mean value of the d distribution can be written as

$$\eta = \frac{q}{C_{ox}} \cdot 2 \tag{2.3}$$

with

q	elementary charge
C_{ox}	oxide capacitance.

From experiments with the TDDS framework on nano-scale MOSFETs, it has been found that BTI degradation and recovery can be explained by capture and emission events of single oxide defects [16]. The TDDS framework, which will be introduced in Section 3.7 in detail, consists of several eMSM cycles followed by a postprocessing of the recorded data. ΔV_{th} is obtained during the recovery phase by a single point measurement of I_D or V_G near V_{th} (also known as fast-I_D or fast-V_{th} methods in literature [31, 39, 40]). Figure 2.7 top shows typical recovery measurements of a nano-scale MOSFET, containing the steps of five defects enumerated with 1, 2, 3, 4 and 12. Due to the fact that the capture and emission events are assumed to be stochastic processes, TDDS

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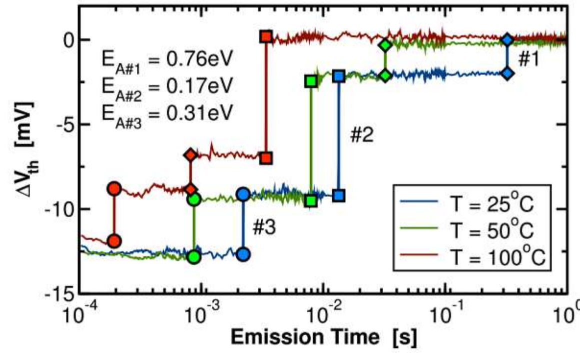

Figure 2.10.: Temperature dependence of the characteristic emission times: Temperature accelerates degradation and recovery. Figure source: [33].

requires a number, e.g., 100, of the same stress/recovery experiments in order to capture the statistics for a reliable characterization. The spectral map in Figure 2.7 bottom visualizes the individuality of each defect. It is built by entering d and τ_e of each emission event into a two-dimensional diagramm. From this, the spectral map can be obtained as the distribution of the numerical data [41].

τ_e and τ_c are strongly bias and temperature dependent. In this regard, the bias dependence is shown in Figure 2.9 where three defects characterized on nano-scale SiON pMOSFETs capture a hole during stress and emit it during recovery. The capture events (Subfigure 2.9a) cause an increase of the absolute value of ΔV_th comparable to the degradation of large-area devices shown in Subfigure 2.4a while the emission events (Subfigure 2.9b) cause a decrease of ΔV_th comparable to the recovery of large-area devices shown in Subfigure 2.4b. Both, capture and emission events happen at stochastically distributed τ_c and τ_e, respectively.

With increasing $V_\mathrm{G}^\mathrm{str}$ τ_c decreases and with increasing $V_\mathrm{G}^\mathrm{rec}$ τ_e increases. This leads to a different contribution of the three shown defects to degradation and recovery of ΔV_th. At $V_\mathrm{G}^\mathrm{str}{=}-1.4\,\mathrm{V}$ (blue trace in Subfigure 2.4a) τ_c of defect 2 and 3 are larger than the upper limit of the experimental window during stress ($t_\mathrm{str,max}$), which is 1 s. Thus, only defect 1 contributes to ΔV_th. At $V_\mathrm{G}^\mathrm{str}{=}-1.7\,\mathrm{V}$ (green trace in Subfigure 2.4a) τ_c of defect 2 is decreased and shifted to times within the experimental window. Therefore, the capture event of defect 1 and defect 2 contribute to ΔV_th. Finally at $V_\mathrm{G}^\mathrm{str}{=}-1.9\,\mathrm{V}$ and $V_\mathrm{G}^\mathrm{str}{=}-2.2\,\mathrm{V}$ also defect 3 contributes to ΔV_th.

At recovery conditions, the process is quite similar. While at $V_\mathrm{G}^\mathrm{rec}{=}-0.2\,\mathrm{V}$ all three defects contribute to recovery, at $V_\mathrm{G}^\mathrm{rec}{=}-1\,\mathrm{V}$ only defect 3 contributes to ΔV_th because τ_e of the other two defects are higher than the upper limit of the experimental window during revery ($t_\mathrm{rec,max}$). Quite comparable to the measurements in large-area devices (Figure 2.4) the evolution of ΔV_th of nano-scale MOSFETs is accelerated during stress with increasing V_G and decelerated during recovery.

The capture and emission events are also highly affected by T as shown in Figure 2.10 based on the temperature dependence of the emission events. In contrast to the discus-

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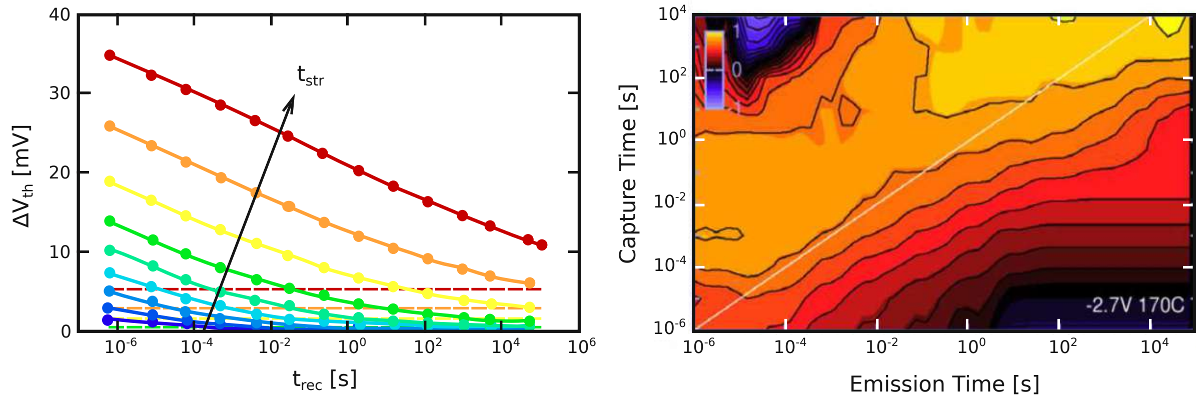

Figure 2.11.: A capture/emission time: The CET map is obtained by a variation of $V_\mathrm{G}^\mathrm{str}$ and $V_\mathrm{G}^\mathrm{rec}$ at NBTI conditions (left). The solid lines are obtained by integrating the CET map following and the dashed lines are the permanent component not visible in the CET map (right). The CET map summarizes the particular $\tau_\mathrm{e}(V_\mathrm{G})$ and $\tau_\mathrm{c}(V_\mathrm{G})$ behavior of many defects. Figure source: [16].

sion in Subsection 2.1.1 regarding the temperature dependence of recovery of large-area devices, which is negligible, in nano-scale devices the picture is a little more complicated. Basically, with increasing T, both, τ_c during stress and τ_e during recovery decrease to lower values. In Figure 2.10 it can be seen that τ_e decreases with increasing T but the overall difference beween ΔV_th at the lower limit of the experimental window and ΔV_th at the upper limit is temperature independent because only the three defects can contribute to recovery.

The bias dependence of the capture and emission times leads to a crossing point of both, where $\tau_\mathrm{e}(V_\mathrm{G})$ and $\tau_\mathrm{c}(V_\mathrm{G})$ are equal, illustrated in Figure 2.16. Around this crossing point, defects cause random exchange events as shown in Subfigure 2.12b, which is called RTN. Since the whole $\tau_\mathrm{e}(V_\mathrm{G})$ and $\tau_\mathrm{c}(V_\mathrm{G})$ behavior is different for each defect, at a certain V_G some defects might capture charge carriers (because $\tau_\mathrm{c} \gg \tau_\mathrm{e}$), some defects might emit previously captured charge carriers (because $\tau_\mathrm{c} \ll \tau_\mathrm{e}$) and some defects might cause an RTN signal (because $\tau_\mathrm{e} \approx \tau_\mathrm{c}$). Finally, summing up the contribution of the transitions of all electrically active defects to ΔV_th results in what is conventianally observed as BTI degradation and recovery.

Such a broad distribution of the characteristic times and their bias dependence can be illustrated as a CET map shown in Figure 2.11. The idea is that similar defects can be grouped together using a suitably defined density g [57]. In order to draw such a map, the capture time is obtained at different stress conditions while the emission time is taken at different recovery conditions. With increasing $V_\mathrm{G}^\mathrm{str}$ and constant $V_\mathrm{G}^\mathrm{rec}$, τ_c decreases, while τ_e is not affected. With increasing $V_\mathrm{G}^\mathrm{rec}$ and constant $V_\mathrm{G}^\mathrm{str}$, τ_e increases, while τ_c is not affected. The particular behavior of $\tau_\mathrm{e}(V_\mathrm{G})$ and $\tau_\mathrm{c}(V_\mathrm{G})$ can be plotted as a density:

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$$g(\tau_\mathrm{c},\tau_\mathrm{e}) \approx -\frac{\partial^2 \Delta V_\mathrm{th}(\tau_\mathrm{c},\tau_\mathrm{e})}{\partial \tau_\mathrm{c}\tau_\mathrm{e}}$$

or

$$\tilde{g}(\tau_\mathrm{c},\tau_\mathrm{e}) = \tau_\mathrm{c}\tau_\mathrm{e} g(\tau_\mathrm{c},\tau_\mathrm{e})$$

if it is represented on logarithmic axes.

Figure 2.11 shows how broad the distribution of the capture and emission times can be, which cannot be explained by models like SRH or the reaction-diffusion model. Thus, new perspectives were needed.

2.1.4. Two-State Model Including Non-Radiative Transitions

Due to several inconsistencies of the reaction-diffusion model with the experimental observations, single donor-like defects in the oxide have been taken into account as the main physical cause of NBTI. The random exchange of charge carriers between an oxide defect and the substrate, which occurs if the defect energy is approximately equal to the Fermi level, produces an RTN signal in ΔV_th measurements as shown in Subfigure 2.12b. One simple modeling attempt to describe charge transfer reactions in RTN signals as capture and emission events is provided by the two-state model illustrated in Subfigure 2.12a. Therefore, the charge state of the defect was described by either the neutral state 1 or the charged state 2 with the defect occupancy of the state i (X_i) being 1 when the defect is in state i and 0 otherwise [41]. The transition probabilities are obtained as a Markov process. The probability for the transition from i to j within the next infinitesimally small time interval h is given as

$$P\left\{X_j(t+h) = 1 | X_i(t) = 1\right\} = k_{ij}h + O(h) \tag{2.4}$$

with $\lim_{h\to 0} O(h)/h = 0$ and

X_j / X_i	defect occupancies of the states j / i
t	time
k_{ij} / k_{ji}	rate for the transition from state i to state j / j to state i (probability per unit time)
h	infinitesimally small time interval
$O(h)$	higher-order terms of h.

The probability that no transitions from j to i occurs is given as

$$P\left\{X_j(t+h) = 1 | X_j(t) = 1\right\} = 1 - k_{ji}h + O(h). \tag{2.5}$$

If h is assumed to be so small that all higher-order terms are negligible and that the defect is currently in state i, $p_i(t) = P\left\{X_i(t) = 1\right\}$ the probability that $X_j(t+h) = 1$ is given as

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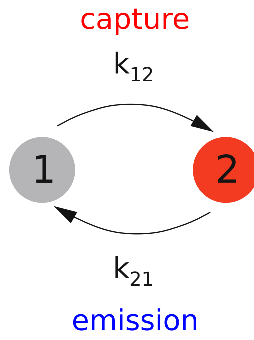
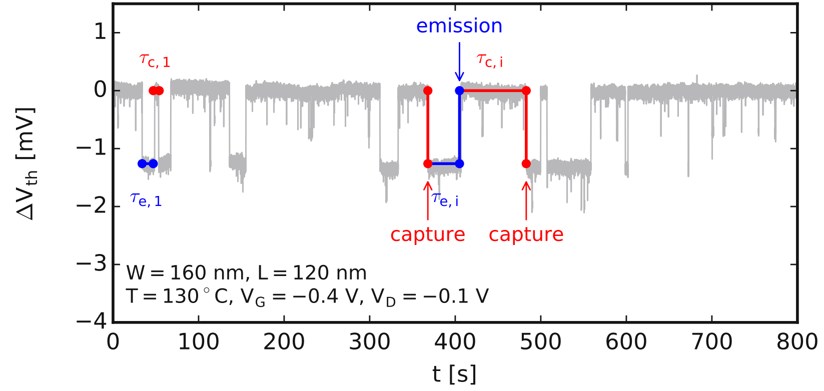


(a) State transition rate diagram for a two-state model



(b) The random charge exchange events produce capture and emission events. The mean values of the characteristic times can be calculated as $\tau_\mathrm{c} = \sum_{i=1}^{N} \tau_{\mathrm{c},i}/N$ and $\tau_\mathrm{e} = \sum_{i=1}^{N} \tau_{\mathrm{e},i}/N$

Figure 2.12.: Two-state model: an RTN signal can be modeled using a two-state Markov model.

$$p_j(t+h) = P\{X_j(t+h) = 1|X_i(t) = 1\}\, p_i(t) + P\{X_j(t+h) = 1|X_j(t) = 1\}\, p_j(t) \quad (2.6)$$

By replacing the conditional probabilities in Equation 2.6 by the rates in Equation 2.4 and Equation 2.5, rearrangement and inserting $1-p_j(t)$ for $p_i(t)$, the differential equation can be obtained:

$$\frac{dp_j(t)}{dt} = k_{ij}(1 - p_j(t)) - k_{ji}p_j(t). \quad (2.7)$$

This is an ordinary differential equation with the solution

$$p_j(t) = p_j(\infty) + (p_j(0) - p_j(\infty))\mathrm{e}^{-t/\tau} \quad (2.8)$$

with

$p_j(\infty) = k_{ij}/(k_{ij} + k_{ji})$	probability that the defect is in the state j for $t \gg \tau$
$\tau = 1/(k_{ij} + k_{ji})$	transition time constant.

This solution describes the probability of the defect being in state j as an exponential transition from its inital value $p_j(0)$ to its final stationary value $p_j(\infty)$.

The probability that the defect is in the other state i can be calculated as $1-p_j(t)$. If it is assumed that $i = 1$ is the neutral state and $j = 2$ is the charged state, the capture time τ_c and emission time τ_e would be the transition times from i to j (τ_{12}) and from j to i (τ_{21}), respectively. τ_{12} and τ_{21} are stochastic variables. For the calculation of

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the transition times, the initial defect state is assumed to be neutral, thus, in state 1 ($p_1(0) = 1$). In this case, the time until the defect transits to state 2 is independent of the backward rate k_{21}. The probability that the defect is in state 1 at a certain time (t) is given as $p_1(t) = \exp(-k_{12}t)$ and that it is in state 2 as $p_2(t) = 1 - p_1(t)$. If $\tau_{12} < t$, the probability that the defect is in state 2 can be written as $p_2(\tau_{12}) = 1 - \exp(-k_{12}\tau_{12})$ and the PDF can be expressed as $g(\tau_{12}) = dp_2(\tau_{12})/d\tau_{12} = k_{12}\exp(-k_{12}\tau_{12})$. The mean value of τ_c is the expectation value of the exponential distribution, which is given by

$$\bar{\tau_\mathrm{c}} = \int_0^\infty \tau_\mathrm{c} g(\tau_\mathrm{c}) d\tau_\mathrm{c} = \frac{1}{k_{12}}. \tag{2.9}$$

Similar arguments hold also for the emission time:

$$\bar{\tau_\mathrm{e}} = \int_0^\infty \tau_\mathrm{e} g(\tau_\mathrm{e}) d\tau_\mathrm{e} = \frac{1}{k_{21}} \tag{2.10}$$

with

$\bar{\tau_\mathrm{c}}$ / $\bar{\tau_\mathrm{e}}$	mean value of the capture time τ_c / emission time τ_e
g	probability density function.

A proper RTN analysis is only possible if $\bar{\tau_\mathrm{c}} \approx \bar{\tau_\mathrm{e}}$ (energy level of the defect is located near the Fermi level), $(\tau_\mathrm{e},\tau_\mathrm{c}) \in [t_\mathrm{rec,min},t_\mathrm{rec,max}]$ and $\tau_\mathrm{e},\tau_\mathrm{c} \ll t_\mathrm{rec,max}$ at certain V_G and T. Only RTN signals caused by defects with characteristic times, which fullfil these prerequisites, can be characterized because of a statistically meaningful number of transitions.

If $\bar{\tau_\mathrm{c}} \ll \bar{\tau_\mathrm{e}}$ or $\bar{\tau_\mathrm{c}} \gg \bar{\tau_\mathrm{e}}$, eMSM measurements are required where the gate bias is switched from $V_\mathrm{G}^\mathrm{rec}$ to $V_\mathrm{G}^\mathrm{str}$ and back to $V_\mathrm{G}^\mathrm{rec}$ in order to obtain the probability transition. For this it is assumed that the Markov process is stationary before each change of the gate voltage. Before switching from $V_\mathrm{G}^\mathrm{rec}$ to $V_\mathrm{G}^\mathrm{str}$ the probability that the defect is in its state 2 is given as $p_2(t) = p_2(V_\mathrm{G}^\mathrm{rec})$. With Equation 2.8 the probability after switching the gate voltage from $V_\mathrm{G}^\mathrm{rec}$ to $V_\mathrm{G}^\mathrm{str}$ can be calculated as

$$p_2(t) = p_2(V_\mathrm{G}^\mathrm{str}) + \left(p_2(V_\mathrm{G}^\mathrm{rec}) - p_2(V_\mathrm{G}^\mathrm{str})\right) \mathrm{e}^{-t_\mathrm{str}/\tau_\mathrm{c}} \tag{2.11}$$

and the probability after switching the gate voltage from $V_\mathrm{G}^\mathrm{str}$ to $V_\mathrm{G}^\mathrm{rec}$ as

$$p_2(t) = p_2(V_\mathrm{G}^\mathrm{rec}) + (p_2(t_\mathrm{str,max}) - p_2(V_\mathrm{G}^\mathrm{rec}))\,\mathrm{e}^{-t_\mathrm{rec}/\tau_\mathrm{e}} \tag{2.12}$$

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with

τ_c / τ_e	time constant for the transition from recovery to stress / from stress to recovery conditions
$\tau_c(V_G)$ / $\tau_e(V_G)$	defect time constant at different gate bias
V_G^{str} / V_G^{rec}	gate bias at stress/recovery conditions
t_{str} / t_{rec}	stress / recovery time
$t_{str,max}$	point in time when the bias conditions are switched from stress to recovery
f	occupancy.

The corresponding transition time constants are given as

$$\tau_c = \frac{1}{\frac{1}{\tau_c(V_G^{str})} + \frac{1}{\tau_e(V_G^{str})}} \tag{2.13}$$

and

$$\tau_e = \frac{1}{\frac{1}{\tau_c(V_G^{rec})} + \frac{1}{\tau_e(V_G^{rec})}}. \tag{2.14}$$

The corresponding occupancies are given as

$$f(V_G^{str}) = \frac{\tau_e(V_G^{str})}{\tau_e(V_G^{str}) + \tau_c(V_G^{str})} \tag{2.15}$$

and

$$f(V_G^{rec}) = \frac{\tau_e(V_G^{rec})}{\tau_e(V_G^{rec}) + \tau_c(V_G^{rec})}. \tag{2.16}$$

According to Equation 2.11, the occupancy for the transition from $f(V_G^{rec})$ to $f(V_G^{str})$ is

$$f(t_{str}) = f(V_G^{str}) + \left(f(V_G^{rec}) - f(V_G^{str})\right) \mathrm{e}^{-t_{str}/\tau_c}$$

while according to Equation 2.12, the transition from $f(V_G^{str})$ to $f(V_G^{rec})$ is

$$f(t_{str}, t_{rec}) = f(V_G^{rec}) + (f(t_{str}) - f(V_G^{rec}))\, \mathrm{e}^{-t_{str}/\tau_e}.$$

Experimentally the differences $f(t_{str}) - f(V_G^{rec})$ is seen when switching from recovery to stress conditions and $f(t_{str}, t_{rec}) - f(V_G^{rec})$ when switching from stress to recovery conditions which results in

$$\Delta f(t_{str}) = \left(f(V_G^{str}) - f(V_G^{rec})\right) \left(1 - \mathrm{e}^{-t_{str}/\tau_c}\right) \tag{2.17}$$

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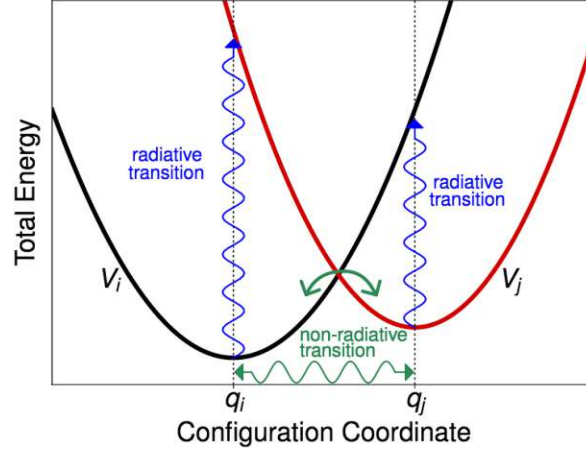

Figure 2.13.: Configuration coordinate diagram for a two-state model using a non-radiative multiphonon theory: The transition from i to j proceeds either radiatively or non-radiatively. In typical semiconductor devices, the radiative transition can be excluded as no photons are available during the regular operation. Therefore, the energy needed to overcome the difference between the minimum point and the crossing point of the parabolas hasto be supplied by phonons. Figure source: [58].

and

$$\Delta f(t_{\mathrm{str}}, t_{\mathrm{rec}}) = \left(f(V_{\mathrm{G}}^{\mathrm{str}}) - f(V_{\mathrm{G}}^{\mathrm{rec}})\right)\left(1 - \mathrm{e}^{-t_{\mathrm{str}}/\tau_{\mathrm{c}}}\right)\mathrm{e}^{-t_{\mathrm{str}}/\tau_{\mathrm{e}}}, \tag{2.18}$$

respectively.

The overall degradation can be obtained as

$$-\Delta V_{\mathrm{th}}(t_{\mathrm{str}}, t_{\mathrm{rec}}) = \sum_{k}^{N} d_{\mathrm{k}}\left(f_{\mathrm{k}}(V_{\mathrm{G}}^{\mathrm{str}}) - f_{\mathrm{k}}(V_{\mathrm{G}}^{\mathrm{rec}})\right) h_{\mathrm{k}}(t_{\mathrm{str}}, t_{\mathrm{rec}}; \tau_{\mathrm{c,k}}, \tau_{\mathrm{e,k}}) \tag{2.19}$$

with

k	defect index
N	total amount of active defects
d_k	step height of defect k, induced shift in ΔV_{th}
h_k	$h(t_{\mathrm{str}}, t_{\mathrm{rec}}; \tau_{\mathrm{c}}, \tau_{\mathrm{e}}) = \Delta f(t_{\mathrm{str}}, t_{\mathrm{rec}}; \tau_{\mathrm{c}}, \tau_{\mathrm{e}}) / \left(f(V_{\mathrm{G}}^{\mathrm{str}}) - f(V_{\mathrm{G}}^{\mathrm{rec}})\right)$.

So far, the stochastic process of capture and emission events has been formulated based on a two-state model. In order to be able to calculate the transition rates between the state i and j, it has to be considered that when electrons or holes are captured or emitted from oxide defects the whole surrounding (electrons and nuclei) is influenced. In each state, neutral and charged, the total energy consists of contributions from the ionic system, the electronic system, and a coupling term. In a simplified way, the atomic positions are reduced to one-dimensional configuration coordinates and the adiabatic energy

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surface, which would be obtained by solving the Schrödinger equation, is approximated by a harmonic oscillator. The total energy of each charge state i can be written as

$$V_i = \frac{1}{2} M \omega_i^2 (q - q_i)^2 + E_i \tag{2.20}$$

with

V_i	total energy of the charge state i
M	effective mass
q	reaction coordinate
q_i	local equilibrium position
ω_i	vibrational frequency in minimum i
E_i	potential energy.

This parabolic approximation is shown in the configuration coordinate diagram in Figure 2.13 for both states i and j. For the calculation of the transition rates of such a defect, two transition possibilities between the neutral and the charged state can be considered as shown in Figure 2.13, the radiative transition and the non-radiative transition. The radiative, or optical, transition occurs around the minima of the parabolas according to the Franck-Condon principle. During the transition from state 1 to state 2 the lattice coordinate q does not change and a photon would have to supply the energy to the system. However, no photons are available for such direct transitions during regular operation in typical semiconductor devices. Therefore, the transition between 1 and 2 has been described by non-radiative multiphonon processes [13, 14, 15], where the energy to overcome the barrier has to be supplied by phonons. This means that the system has to overcome the difference between the minimum points E_1 or E_2 and the crossing point of the parabolas $\mathcal{E}_{12}$ as illustrated in Figure 2.14.

The NMP transition describes the charge carrier transfer between the conduction or the valence band of a semiconductor and the oxide trap. The corresponding rates for continuously distributed charge carrier energies can be written as [59, 60]

$$k_{ij}^{\mathrm{C}}(E, E_{\mathrm{D}}) = \int_{E_{\mathrm{C}}}^{\infty} D_{\mathrm{n}}(E) f_{\mathrm{p}}(E) A_{ij}(E, E_{\mathrm{D}}) f_{ij}(E, E_{\mathrm{D}}) \mathrm{d}E \tag{2.21}$$

$$k_{ij}^{\mathrm{V}}(E, E_{\mathrm{D}}) = \int_{-\infty}^{E_{\mathrm{V}}} D_{\mathrm{p}}(E) f_{\mathrm{p}}(E) A_{ij}(E, E_{\mathrm{D}}) f_{\mathrm{ij}}(E, E_{\mathrm{D}}) \mathrm{d}E \tag{2.22}$$

$$k_{ji}^{\mathrm{C}}(E, E_{\mathrm{D}}) = \int_{E_{\mathrm{C}}}^{\infty} D_{\mathrm{n}}(E) f_{\mathrm{n}}(E) A_{ji}(E, E_{\mathrm{D}}) f_{ji}(E, E_{\mathrm{D}}) \mathrm{d}E \tag{2.23}$$

$$k_{ji}^{\mathrm{V}}(E, E_{\mathrm{D}}) = \int_{-\infty}^{E_{\mathrm{V}}} D_{\mathrm{p}}(E) f_{\mathrm{n}}(E) A_{ji}(E, E_{\mathrm{D}}) f_{ji}(E, E_{\mathrm{D}}) \mathrm{d}E \tag{2.24}$$

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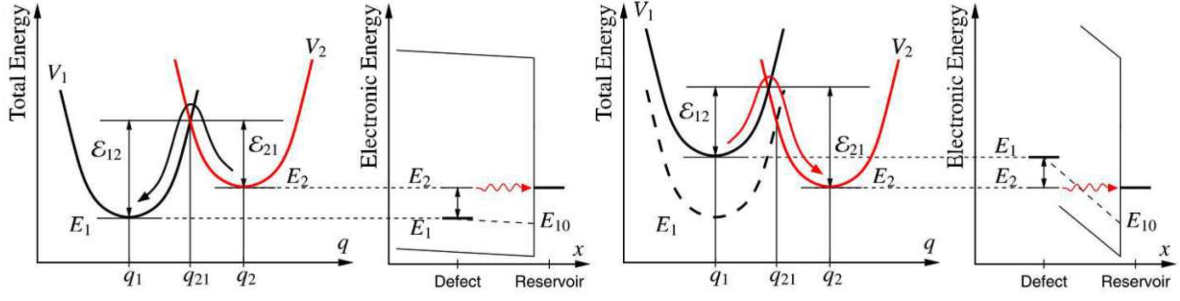

Figure 2.14.: The field-dependence of the NMP transition: As a consequence of the electrostatic shift of the defect level, the relative position of the parabolas change. Figure source: [16].

with

k_{ij}^{C} / k_{ij}^{V}	transition rate from i to j for the conduction / valence band
k_{ji}^{C} / k_{ji}^{V}	transition rate from j to i for the conduction / valence band
E	energy
E_{D}	trap level
E_{C} / E_{V}	conduction / valence band edge energy
D_{n} / D_{p}	density of states of the conduction / valence band
f_{n} / f_{p}	carrier distribution functions for electrons / holes
A_{ji} / A_{ji}	electron wave functions of both states and accounts for possible tunneling processes
f_{ji} / f_{ji}	lineshape function

Under homogeneous bias conditions the carriers in the channel are in equilibrium and thus the carrier distribution functions, f_{n} and f_{p}, are properly described by the Fermi-Dirac distribution. Substituting f_{n} and f_{p} by the Fermi-Dirac distribution and considering a linear electron-phonon coupling, the transition time constants for hole capture and emission are given by

$$\tau_{\mathrm{c}} = \frac{1}{k_{12}} = \frac{1}{k_0} \mathrm{e}^{\mathcal{E}_{12}/(k_{\mathrm{B}}T)} \tag{2.25}$$

$$\tau_{\mathrm{e}} = \frac{1}{k_{21}} = \frac{1}{k_0} \mathrm{e}^{(\mathcal{E}_{21}+E_1+E_2)/(k_{\mathrm{B}}T)} \tag{2.26}$$

with

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(a) The energy level E_1 of the defect at the depth x is located below or above the Fermi level if recovery conditions $E_{\mathrm{OX}}^{\mathrm{L}}$ or stress conditions $E_{\mathrm{OX}}^{\mathrm{H}}$ are applied, respectively.

(b) The AER defines the region where energy levels of defects may be located in order to be shifted above the Fermi level when a stress bias is applied and below the Fermi level when a recovery bias is applied.

Figure 2.15.: Region of defects actively contributing to the degradation and recovery in an NBTI setting: Defects whose energy levels are located in the AER are neutral prior stress, can be potentially charged during stress and discharged again during recovery. Furthermore, the defect energy band is chosen in such a way that the contribution of defects located in right half of the oxide dominates the degradation. Figure source: [16].

$\mathcal{E}_1$ / $\mathcal{E}_2$	minimum of the total energy of the charge state 1 / 2
$\mathcal{E}_{12}$ / $\mathcal{E}_{21}$	energy barrier height for the transitions $1 \rightarrow 2$ / $2 \rightarrow 1$: difference between E_1 / E_2 and the crossing point of the parabolas (Figure 2.14)
k_{B}	Boltzmann constant
T	temperature.

The relative position of the parabolas depends on E_{OX}, which leads to a field- and temperature-dependence of the NMP transition as shown in Figure 2.14. At recovery conditions, the minimum of the neutral state parabola E_1 is located energetically below the minimum of the charged state parabola E_2. If the defect was previously charged, it will transit from the charged state to the neutral state. At stress conditions, $E_2 > E_1$ and a previously neutral state will transit to the charged state. According to Equations 2.9 and 2.10, the field- and temperature-dependence of the transitions rates leads to a field- and temperature-dependence of τ_{e} and τ_{c}, which reflects the experimentally observed behavior of single oxide defects discussed in Subsection 2.1.3.

Figure 2.14 already illustrates that in eMSM measurements only defects in a certain energy region contribute to ΔV_{th}. This area is the AER and is shown in Figure 2.15

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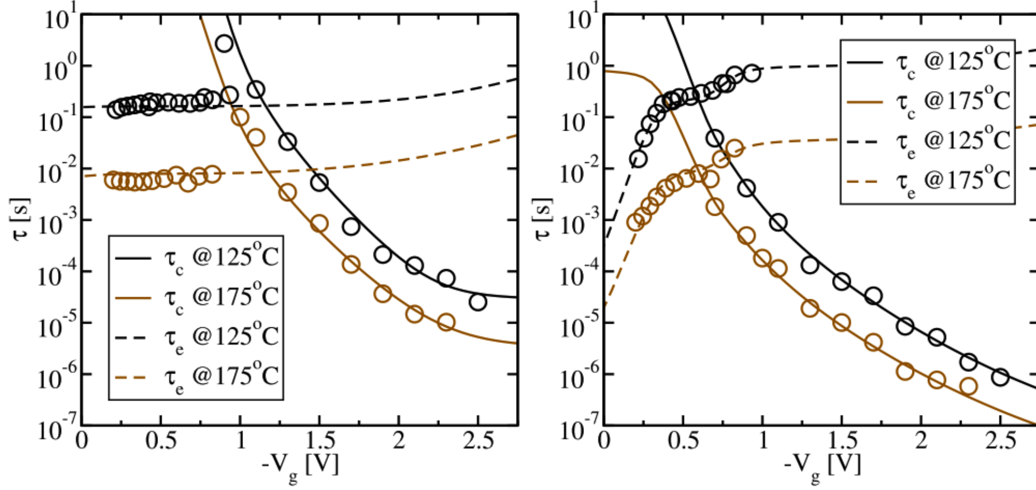

Figure 2.16.: Switching and fixed oxide defects: TDDS data of a fixed positive charge trap (left) and a switching trap (right). Figure source: [61].

[16]. As an explanation, a defect energy level E_1, which is below the Fermi level E_F at recovery conditions (low level is abbreviated with L, $V_\mathrm{G}^\mathrm{rec} \approx V_\mathrm{th}$) and above the Fermi level at stress conditions typically above nominal operating conditions (high level is abbreviated with H) is withing the AER. Following the switch from the recovery to the stress voltage, defects with energy levels within the AER are moved above the Fermi level and capture charge carriers. Therefore, as time progresses, the AER determines the maximum possible degradation. Back at recovery voltage, the defects are moved back below the Fermi level and emit the charge carriers again.

The boundaries of the AER can be defined as shown in the following. E_1 depends on the bias via the depth-dependent electrostatic potential $\varphi(x)$: $E_1(x) = E_{10} - q\varphi(x)$. At low defect concentration, it can be assumed to first-order that the charged defects inside the oxide do not significantly impact the electrostatic potential. With this assumption, the potential can be written as

$$\varphi(x) = \varphi_\mathrm{s} - xE_\mathrm{OX},$$

where φ_s is the potential at the interface. In a simple approximation, the trap level depends on the applied bias via

$$E_1 = E_{10} - q\varphi_\mathrm{s} + qxE_\mathrm{OX}.$$

With this, the lower boundary (E_L) of the AER can be written as Equation 2.27 and the upper boundary (E_U) of the AER can be written as Equation 2.28

$$E_\mathrm{L}(x) = E_\mathrm{F} + q\varphi_\mathrm{s}^\mathrm{H} - qxE_\mathrm{OX}^\mathrm{H} \tag{2.27}$$

$$E_\mathrm{U}(x) = E_\mathrm{F} + q\varphi_\mathrm{s}^\mathrm{L} - qxE_\mathrm{OX}^\mathrm{L} \tag{2.28}$$

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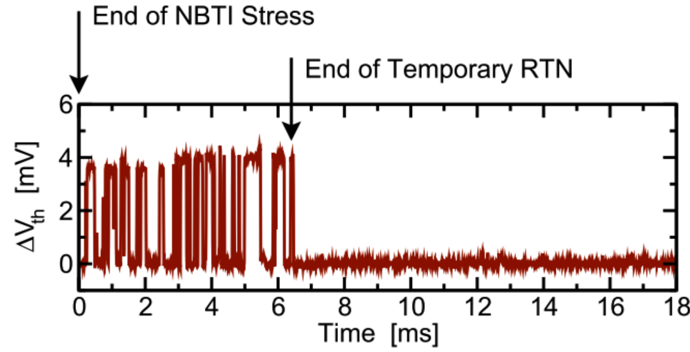

Figure 2.17.: Interrupted RTN: After NBTI stress the defect produces RTN for a limited amount of time and is then neutral. Figure source: [16].

with

E_L / E_U	lower / upper energy boundary
q	elementary charge
φ_s^H / φ_s^L	potential at the interface at stress / recovery conditions
E_{OX}^H / E_{OX}^L	electric field across the oxide at stress / recovery conditions
x	depth

Although the two-state model can explain a field- and temperature-dependence of the characteristic capture and emission times, important details seen in experiments are still missing in this model. For example:

- The predicted field-dependence of $\tau_c(V_G)$ is nearly linear, which is not the case in experiments. TDDS data shown in Figure 2.16 illustrates that $\tau_c(V_G)$ shows some curvature on a logarithmic scale.
- Defects have been observed which show an interrupted RTN signal [62, 40, 41]. Figure 2.17 illustrates a defect, which produces an RTN signal only for a limited amount of time after NBTI stress. Such observations have led to the conclusion that in addition to a neutral and a charged state also a metastable state must exist. This metastable state can either be neutral or charged.
- $\tau_e(V_G)$ cannot be explained properly by a two-state model. As shown in Figure 2.16 two types of defects occur, which have been named switching and fixed oxide defects [61]. In the first case $\tau_e(V_G)$ is nearly constant and shows only a slight bias-dependence. In the second case $\tau_e(V_G)$ is nearly bias-independent above V_{th} and drops below V_{th}. Such a behavior could be captured by two different paths for the emission process.

Especially the last two findings have led to the consideration of additional states. As a result, the four-state NMP model has been proposed [40].

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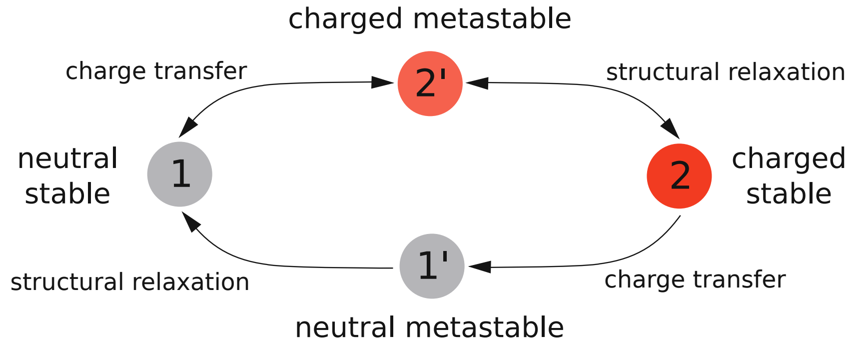

Figure 2.18.: Four-state diagram: The four-state NMP model consists of two stable (1 and 2), two metastable states ($1'$ and $2'$), two neutral (1 and $1'$) and two charged (2 and $2'$) states.

2.1.5. Four-State Non-Radiative-Multiphonon Model

In order to reflect experimental observations like different $\tau_\mathrm{e}(V_\mathrm{G})$ behavior and interrupted RTN signals, the two-state model has been extended as shown in the diagram in Figure 2.18 [16]. The potential energy surface is illustrated in Figure 2.19. The resulting four-state model consists of the two stable states 1 (neutral) and 2 (charged), which correspond to the two states in the two-state model, and additionally two meta-stable states, $1'$ (neutral) and $2'$ (charged). The transitions between 1 and $2'$ and vice versa as well as 2 and $1'$ correspond to NMP transitions as discussed in the previous subsection. The transitions from $2'$ to 2 and vice versa as well as from $1'$ to 1 proceed via a thermal barrier. This thermal barrier is associated with a structural relaxation of the defect and is described by transition state theory [63, 64] as

$$k_{2'2} = \nu \mathrm{e}^{-\mathcal{E}_{2'2}/(k_\mathrm{B}T)}, \tag{2.29}$$
$$k_{1'1} = \nu \mathrm{e}^{-\mathcal{E}_{1'1}/(k_\mathrm{B}T)}, \tag{2.30}$$
$$k_{22'} = \nu \mathrm{e}^{-\mathcal{E}_{22'}/(k_\mathrm{B}T)}, \tag{2.31}$$
$$k_{11'} = \nu \mathrm{e}^{-\mathcal{E}_{11'}/(k_\mathrm{B}T)} \tag{2.32}$$

with

k_ij	transition rate $i \rightarrow j$,
ν	attempt frequency,
$\mathcal{E}_\mathrm{ij}$	energy barrier height,
k_B	Boltzmann constant,
T	temperature.

Assuming the defect is in its neutral state 1, the capturing of a charge carrier proceeds via $1 \rightarrow 2' \rightarrow 2$. The NMP transition $1 \rightarrow 2'$ reflects the charging of the defect and

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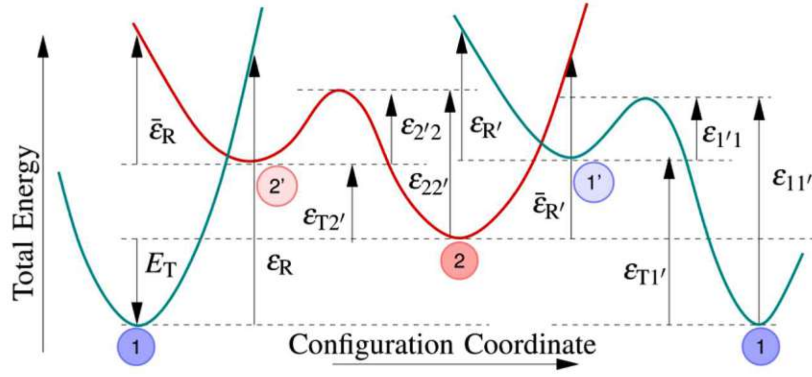

Figure 2.19.: Configuration coordinate diagram for a four-state model using a non-radiative multiphonon theory: Schematic cross-section of the potential energy surface of the four-state NMP model. The energy parameters needed for calculating all transition rates are shown. Figure source: [65].

corresponds to what is experimentally measurable. This transition is followed by a transition to the stable state $2' \rightarrow 2$ via the thermal barrier.

The emission process may proceed via two different paths, either $2 \rightarrow 2' \rightarrow 1$ (fixed oxide traps defects) or $2 \rightarrow 1' \rightarrow 1$ (switching oxide defects). Figure 2.19 shows the case of a switching defect. If the defect is in the stable and charged state 2, the transition to the metastable state $1'$ is an NMP transition, which is followed by a thermal transition to the stable state 1. The experimentally measurable ΔV_{th} step in a recovery trace corresponds to the transitions $2 \rightarrow 1'$ and $2' \rightarrow 1$.

The NMP transition rates can be calculated using the Equations 2.21 to 2.24:

$$
\begin{aligned}
k_{12'} &= k^{C}_{12'} + k^{V}_{12'} \\
k_{2'1} &= k^{C}_{2'1} + k^{V}_{2'1} \\
k_{21'} &= k^{C}_{21'} + k^{V}_{21'} \\
k_{1'2} &= k^{C}_{1'2} + k^{V}_{1'2}
\end{aligned}
$$

The four-state model can be written in a similar manner to the one of the two-state model. As a result, the overall capture and emission times (transition from one stable state to the other via a meta-stable state) can be written as

$$
\tau_{\mathrm{c}} = \frac{1}{\dfrac{k_{11'}k_{1'2}}{k_{11'} + k_{1'1} + k_{1'2}} + \dfrac{k_{12'}k_{2'2}}{k_{12'} + k_{2'1} + k_{2'2}}} \tag{2.33}
$$

and

$$
\tau_{\mathrm{e}} = \frac{1}{\dfrac{k_{1'1}k_{21'}}{k_{1'1} + k_{1'2} + k_{21'}} + \dfrac{k_{2'1}k_{22'}}{k_{2'1} + k_{2'2} + k_{22'}}}, \tag{2.34}
$$

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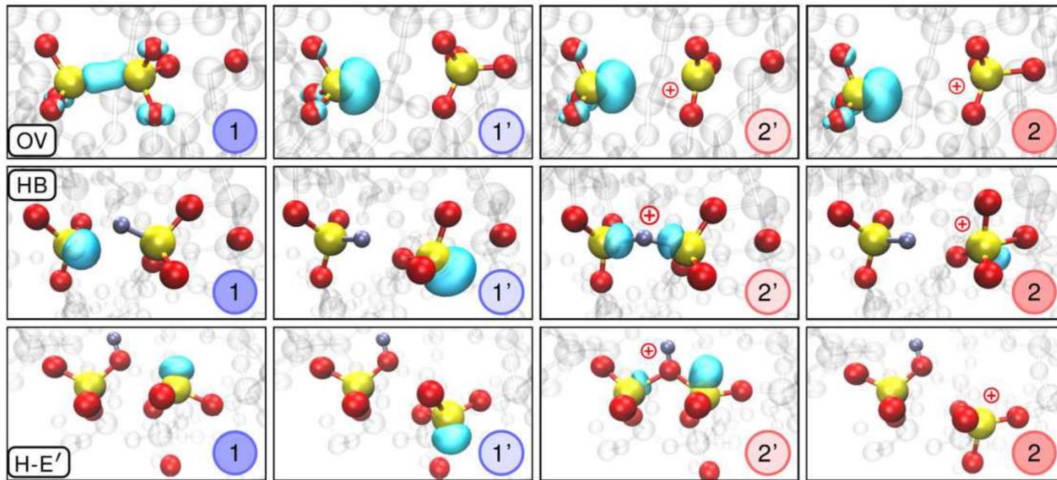

Figure 2.20.: Possible defect candidates: Atomic configurations corresponding to the states 1, 1′, 2′ and 2 for three possible oxide defects [65]. **Top:** Oxygen vacancy. **Center:** Hydrogen bridge. **Bottom:** Hydroxyl-E′ center. H atoms are shown as silver, Si atoms are yellow and O atoms are red. The blue bubbles represent the localized highest occupied orbitals for the neutral charge states and the lowest unoccupied orbital for the positive charge states. Figure source: [65].

respectively where τ_c corresponds to τ_{12} and τ_e to τ_{21}.

The four-state model captures the bias- and temperature-dependence of the capture and emission times quite well. It can also explain the interruption of RTN signals, where the RTN is, for example, the hopping between 1 and 2′ and the interruption is the transition to the stable state 2.

However, at this point the question which structural oxide defect would cause measurable steps in the ΔV_{th} traces remains open. Promising defect candidates suitable for the four-state model are the oxygen vacancy and the hydrogen bridge defects [66, 67]. Moreover, the hydroxyl-E′ center has also been proposed as a possible defect candidate [65]. The atomic configurations of all three defect candidates are shown in Figure 2.20. However, by a statistical analysis of the experimentally found NMP parameter distributions (shown in Figure 2.19) for numerous defects and comparison with the parameters extracted from density-functional-theory (DFT) calculations [68] show that the oxygen vacancy is a very unlikely defect candidate [65]. By contrast, the hydrogen bridge and the hydroxyl-E′ give a good match for the majority of the parameters of the four-state model. Therefore, both of them are promising defect candidates for the four-state model.

Although the extension of the two-state model to a four-state model reflects the experimental observations quite well, the whole picture is still not completed. As will be discussed in the following, observations like the permanent component and volatility of defects need for further extensions.

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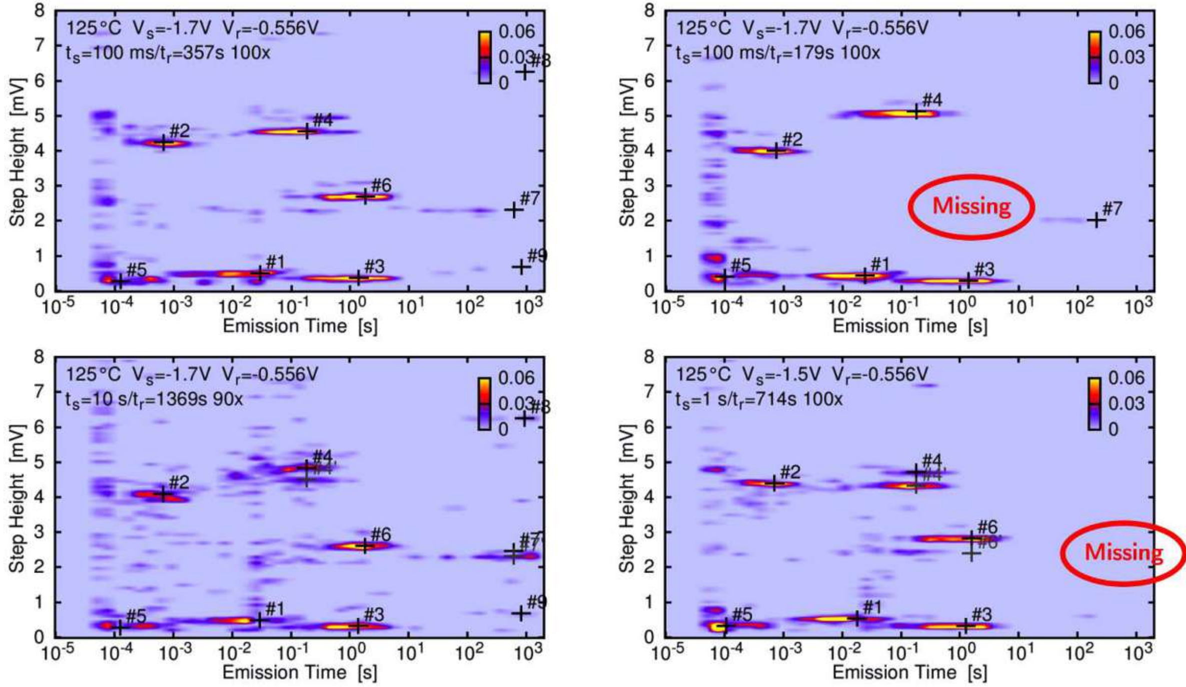

Figure 2.21.: Defect volatility in spectral maps: Defects can dis- and reappear in TDDS measurements. Here this is shown based on spectral maps of different measurements on the same nano-scale device. Figure source: [33, 69].

2.1.6. Defect Volatility

The four-state model, as discussed so far, has been developed for active defects, which basically can be characterized in TDDS measurements ($\tau_\mathrm{c}<t_\mathrm{str,max}$ and $\tau_\mathrm{e}\in[t_\mathrm{rec,min},t_\mathrm{rec,max}]$ for any $V_\mathrm{G}^\mathrm{str}$, $V_\mathrm{G}^\mathrm{rec}$ and T). However, it has been found that oxide defects can all of a sudden disappear from one to the other measurement from the measurement window ($\tau_\mathrm{c}\notin[t_\mathrm{str,min},t_\mathrm{str,max}]$ and $\tau_\mathrm{e}\notin[t_\mathrm{rec,min},t_\mathrm{rec,max}]$) as it is shown in Figure 2.21 based on spectral maps for four different TDDS measurements. Additionally, the disappeared defects can also reappear. An electrically active state can be modeled using the previously discussed four-state NMP model. The disappearing of a defect in TDDS measurements can be described as a transition from one of the four states to an inactive state. This transition from an active state to the inactive state as well as the backward transition have been formulated as volatility [67, 69, 70, 65].

As it is shown in Figure 2.22 the dis- and reappearing can occur several times during TDDS measurements. The corresponding time constant for the transition from the active into the inactive state is typically in the range of hours to weeks. It has been proposed that the transitions between active and inactive states can be described as thermally activated rearrangement of the atomic structure. The reaction barrier can be estimated as [70, 65]

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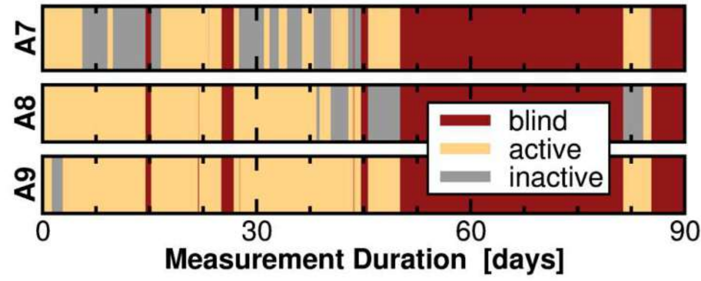

Figure 2.22.: Monitoring of volatile defects over three months: The shown defects A7, A8 and A9 can be both, active and inactive. Figure source: [65].

$$\frac{t}{\tau_{\mathrm{v}}} = \nu \mathrm{e}^{-E_{\mathrm{B}}/(k_{\mathrm{B}}T)} \tag{2.35}$$

with

τ_{v} transition time constant for volatile transitions
ν attempt frequency
E_{B} energy barrier height.

The possible potential energy surface of this thermal transition into an inactive state is shown in Figure 2.23 and the corresponding atomic structure on the right hand side of Figure 2.26. Both figures show the transition $2' \rightarrow 0^{+}$ of a hydroxyl-E′ center, where $2'$ is the charged metastable state of the four-state model. As a general explanation, for the atomic structure the transition from activity to inactivity means that a hydrogen atom is released from the hydrogen bridge or the hydroxyl-E′ center and relocated to a neighboring atom. This corresponds to either a neutral H atom moving away from the neutral defect state, which is associated with a transition to the neutral volatile state 0^{n}, or to a proton from the positive defect state, which is associated with a transition to a positive volatile state 0^{+}. This results in four possible purely thermally activated transitions starting from a four-state model: $2' \rightarrow 0^{+}$, $2 \rightarrow 0^{+}$, $1 \rightarrow 0^{\mathrm{n}}$ and $1' \rightarrow 0^{\mathrm{n}}$. From these four, it has been found that the transitions starting from 1 and $2'$ are always lower in energy [70], especially $2' \rightarrow 0^{+}$ is a quite promising transition for the explanation of volatility. Moreover, it has been found that the hydrogen bridge is not a suitable candidate to explain volatility since the transition barriers are too high to explain the experimental characterizations. By contrast, the hydroxyl-E′ center has been considered as the suitable defect candidate for the explanation of volatility.

Figure 2.23 shows the hydroxyl-E′ potential energy surface of the extension of the four-state model based the transition $2' \rightarrow 0^{+}$. As discussed in the previous paragraph, two additional states, a positive 0^{+} and a neutral 0^{n} and their respective barriers are added. Theoretically, in such a configuration, it would be possible that transitions between 0^{+}

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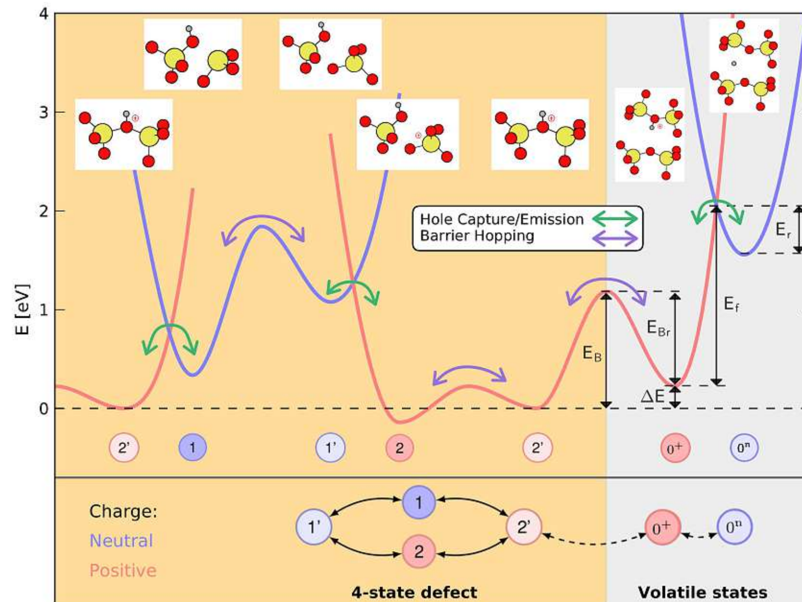

Figure 2.23.: Example of the potential energy surface of a hydroxyl-E′ center including volatile states: The defect can become volatile starting from a positive charge state, which is one of the four (active) NMP states. As soon as it overcomes the barrier E_B it is inactive and not visible in measurements. Figure source: [65].

and 0^n cause RTN since they include a hole capture or emission. However, this has been discarded because it has been shown that due to typical transition barrier heights E_B, E_{Br} and E_f charge capture or emission events in the volatile states would occur most probably with a similar or lower frequency as volatility itself [58].

Basically, transitions from other active states are also possible, for example, the transition $1' \rightarrow 0^n$ via a hydrogen hopping process. However, it has been found that this transition is associated with the permanent component of degradation as will be discussed in the next subsection.

2.1.7. Recoverable and Permanent Component

Oxide defects contribute differently to ΔV_{th} during recovery and thus can be classified into defects contributing to the recoverable component and defects contributing to the permanent component of degradation [71, 72]. Those with characteristic capture and emission times lying within the measurement window are typically associated with the recoverable component while those with $\tau_c < t_{str,max}$ but slowly-relaxing, $\tau_e > t_{rec,max}$, are associated with the permanent component. However, properties like τ_c and τ_e and thus their assignment to the recoverable or the permanent component is highly alterable due to reactions with hydrogen [69]. Defects can also be created or annealed, whereby these terms are often related to the transition from the active to inactive states or to precursor

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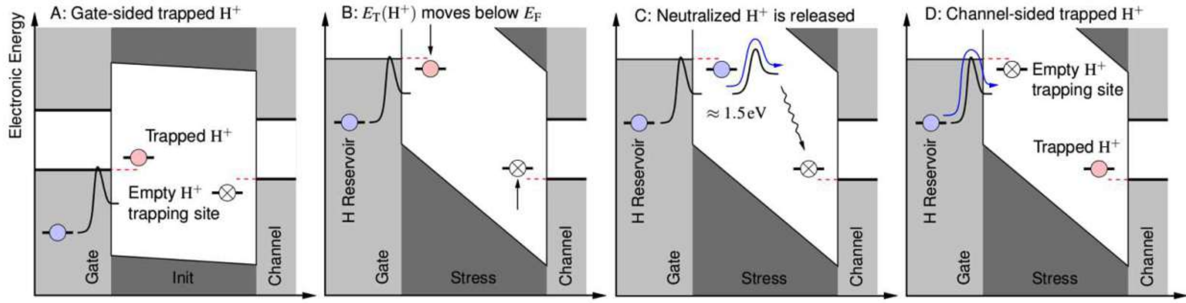

Figure 2.24.: Schematic Hydrogen release mechanism: At the gate side a proton is trapped. During stress, the trap level can be shifted below the Fermi level, which makes it possible for the proton to be neutralized. This neutrally charged hydrogen atom can now be released by overcoming a barrier and move towards the channel side. The empty trap site can potentially be refilled by H released from the gate. This process should be strongly temperature dependent. Figure source: [74].

states [62, 65, 69, 72]. The particular properties and their contribution to degradation can be spread widely.

In order to explain the permanent component of ΔV_{th} in NBTI measurements a gate-side hydrogen release model has been proposed [73, 74]. The idea is based on the fact that in amorphous SiO_2 hydrogen can bind to a bridging oxygen, as calculated in recent DFT calculations [75, 76]. Throughout the binding process, the hydrogen can release its electron and bind to the oxygen or the hydrogen breaks one of the Si-O bonds and forms a hydroxyl group, which faces the dangling bond of the other Si. Such a defect is quite similar to the E′ center and is additionally to the previously discussed defects a proper candidate for the explanation of volatility.

A schematic illustration of the hydrogen release model is shown in Figure 2.24. During stress, the energy level of a trapped H^+ near the gate can move below the Fermi level. Consequently, it is neutralized and emitted over a thermal barrier. The H^0 moves quickly towards the channel where it can become trapped in a preexisting hydrogen trapping site, again releases an electron and causes a ΔV_{th} shift. The gate side can be interpreted as a hydrogen reservoir.

Figure 2.25 shows schematically that the hydrogen release model can be formulated by assuming that the oxide consists of discrete interstitial sites i at which hydrogen can occur in a neutral position. From this interstitial sites, it can be either trapped in a neutral configuration or in a positive configuration. The rate equation for the interstitial hydrogen species can be written as

$$\frac{\partial H_i}{\partial t} = -\sum_j k_{\mathrm{h}}(H_i - H_j) + \sum_n T_{i,n} \tag{2.36}$$

with

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H_i	expectation value of hydrogen in a neutral interstitial position at site i
t	time
k_h	hopping rate from interstitial site i to j, thermal transition
i	defect site where the hydrogen can be trapped
j	neighbouring sites
$T_{i,n}$	trapping rates for interstitial site i interacting with several trapping sites n.

Thereby, one spatial interstitial site i is allowed to interact with several trapping sites n. The corresponding trapping rate is

$$T_{i,n} = k_{01} H_i \left(H_\mathrm{max}^\mathrm{T} - (H_{i,n}^0 + H_{i,n}^+) \right) - k_{10} H_{i,n}^0 \tag{2.37}$$

with

k_{01} / k_{10}	transition rate from the interstitial to the neutral trapped configuration / from the neutral to the interstitial, thermal transition
$H_\mathrm{max}^\mathrm{T} \geq H_{i,n}^0 + H_{i,n}^+$	maximum number of trapped hydrogen atoms
$H_{i,n}^0$ / $H_{i,n}^+$	expectation value of trapped neutral / positive hydrogen trapped.

The temporal change in the number of neutral and positive trapped hydrogen atoms is given by

$$\frac{\partial H_i^0}{\partial t} = -k_{12} H_i^0 + k_{21} H_i^+ + T_i \tag{2.38}$$

$$\frac{\partial H_i^+}{\partial t} = k_{12} H_i^0 - k_{21} H_i^+ \tag{2.39}$$

with

k_{01} / k_{10}	transition rate from the interstitial to the neutral trapped configuration / from the neutral to the interstitial, thermal transition.

The trapping rates $T_{i,n}$ describe the transition from the interstitial to the neutral trapped configuration. The corresponding transition rates k_{01} and backwards k_{10} are modeled as a thermal activation using an Arrhenius law for each trapping site (i, n).

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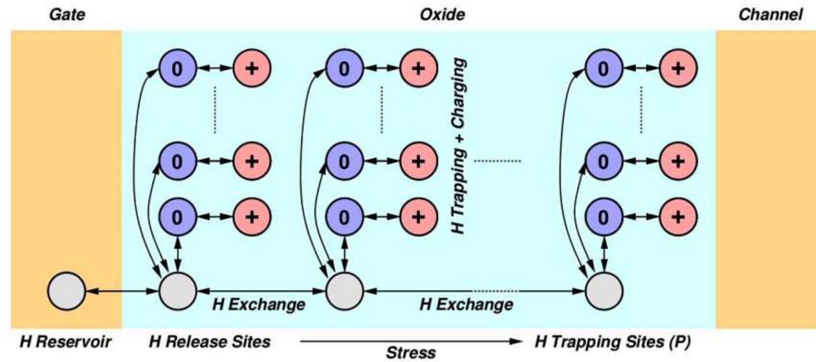

Figure 2.25.: One dimensional schematic of the H-release model: The oxide of a MOSFET consists of potential trapping sites for hydrogen. Hydrogen can either occur in a neutral interstitial position (grey) or as a trapped neutral configuration H^0 (blue) or in a trapped positive configuration H^+ (red). The gate side acts as an additional hydrogen reservoir. Due to the high diffusivity of hydrogen the exchange to a new trapping site can ocur very fast and is therefore not rate limiting. Figure source: [74].

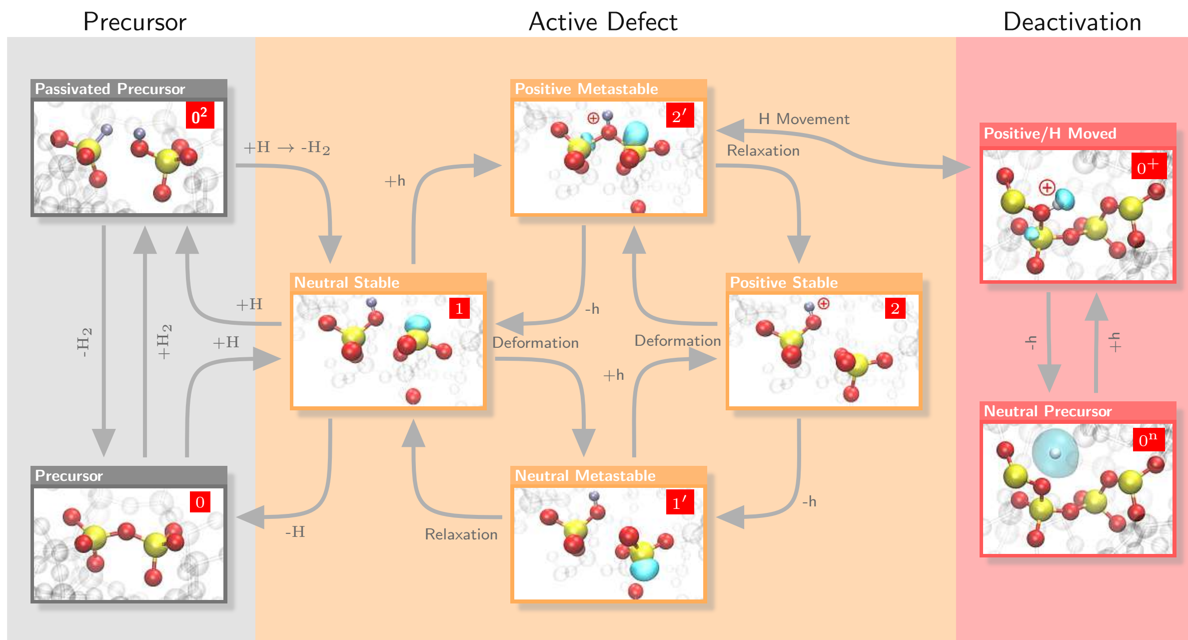

Figure 2.26.: Extended four-state NMP model: Illustrated for a promising defect candidate, the hydroxyl-E′ center. Still, the core of this model (middle) is build around the bistable defect with four states (1,1′,2,2′) and describes the active defect, which is capable of capturing and emitting charge carriers. However, the extended variant of the model also accounts for the inactive phases of the defect via transitions to the precursor states 0 and 0^2 (left) and the inactive states 0^+ and 0^n (right).

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The number of neutral and positive trapped hydrogen can be calculated using rates with standard non-radiative multiphonon theory.

Figure 2.26 shows a complete picture of all defect states being capable to describe the recoverable and the permanent component of NBTI degradation as well as the temporary inactivity of single oxide defects. This extended four-state model includes the four active states (center), the transition to the inactive states starting at state 2′ (right) and the transition to the precursor states starting at state 1 (left) of a hydroxyl-E′ center.

2.2. Hot-Carrier Degradation

In Chapter 1 it is mentioned that basically two types of defects appear in MOSFETs, the interface defects and the oxide defects. So far, it has been discussed how charge carrier exchange between oxide defects and their surrounding affect the device parameters in the context of NBTI degradation. In this chapter, the most important modeling approaches for the degradation mechanism HCD, which is associated with the creation of interface defects, are summarized. Similar to BTI, also HCD is a detrimental mechanism in MOSFETs, which affects device parameters, such as I_D, V_th and on-resistance (R_on). In this context, *hot* is associated with the kinetic energy of the carriers accelerated by high channel electric fields. Therefore, HCD is best observed at high electric fields along the channel, which is typically achieved by a high drain voltage at stress conditions ($V_\mathrm{D}^\mathrm{str}$) and a gate bias close to the operating conditions.

The process itself is known since the 60's [77] and over the time several modeling approaches have been made in order to reflect the changing impact on MOSFET parameters because of the scaling trend. In this context, several attempts have been made in order to distinguish different HCD modes [78], e.g., hot-carrier injection (HCI). HCI is associated with channel carriers, which are entering the conduction band of the oxide as they overcome the energetic barrier between the substrate and the oxide. This requires a kinetic energy higher than 3 eV. Although the electric fields in the device increased due to the scaling of device dimensions, the simultaneous reduction of the operating voltages compensated this increase and led to a lower kinetic energy of the carriers. Therefore, HCI has faded from the spotlight and new modeling attempts have been made.

One of the first successful HCD models was the so-called “lucky-electron” model [79], valid for long channels or high electric fields. This concept introduces a threshold energy level which needs to be surmounted by the carriers in order to trigger impact-ionization. As soon as a carrier travels a sufficiently long distance without collisions, this energy can be reached. However, it has been found that even for low operating voltages around 1.5 V in devices with dimensions in the deca-nanometer regime HCD is a severe degradation mechanism [80, 81]. Thus, models were required, which take into account colder carriers as a physical cause for HCD.

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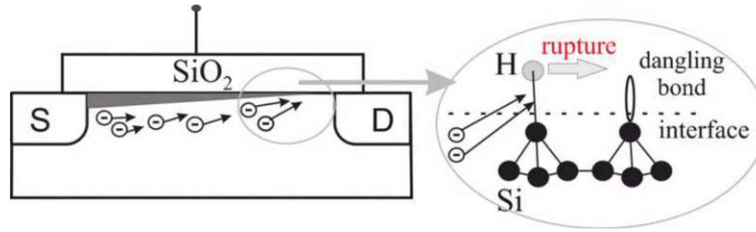

Figure 2.27.: Dissociation of the Si-H bond: A schematic presentation of hot-carrier degradation. The dissociation of the Si-H bond induced by the successive bombardment of two hot carriers is sketched in the right part. Figure source: [23].

2.2.1. Experimental Characterization of HCD

HCD in experiments is often characterized by either using the charge pumping method (Section 3.2) in order to extract the number of interface states or by measurements of the linear drain current shift ($\Delta I_{\mathrm{D,lin}}$). Since defects located at the oxide/substrate interface cause surface scattering, which lowers the carrier mobility and tilts the transfer characteristics, the impact of HCD is much more pronounced in $I_{\mathrm{D,lin}}$ than in V_{th}. $I_{\mathrm{D,lin}}$ can be measured using the method for ΔV_{th} extraction discussed in Subsection 2.1.1. The stress and recovery phases are interrupted periodically in order to record an I_{D}-V_{G} characteristics, extract $I_{\mathrm{D,lin}}$ and subtract it from the unstressed value. In contrast to BTI and as already mentioned in Subsection 2.1.2 created interface states barely recover. Therefore, the recovery of HCD is negligible, and interruptions of the stress conditions hardly affect the degradation state of $I_{\mathrm{D,lin}}$.

The temperature dependence of HCD is different than the one of BTI. For long channel devices, for example, the degradation of $I_{\mathrm{D,lin}}$ is less detrimental at increased temperatures. However, for short-channel devices HCD is accelerated at higher temperatures [82]. This channel length and temperature dependent acceleration of degradation is caused by temperature-dependent contributions of scattering effects, which may populate the high energetical fraction of the carrier ensemble [23].

In contrast to the temperature dependence of HCD, the field dependence is independent of the channel length. In general, the degradation of $I_{\mathrm{D,lin}}$ is highly channel electric field dependent [83, 23]. However, investigations have revealed that the peak of the electric field, the peak of the average carrier kinetic energy and the maximum of the created interface defect density do not correlate with each other [84, 85, 86].

2.2.2. Hess Model

The Hess model proposes that HCD is determined by the dissociation of neutral hydrogen-passivated Si dangling bonds at the substrate/oxide interface by channel carriers (see Figure 2.27) [87, 88, 89, 90]. This is based on two ideas: a hot carrier with sufficient kinetic energy scatters with a dangling bond and causes it to break (single particle process, shown in the left panel of Figure 2.28), as well as multiple colder carriers cause one bond

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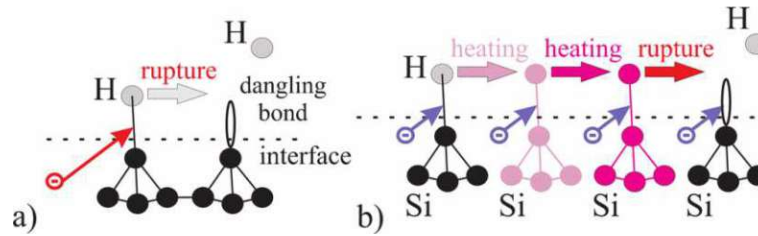

Figure 2.28.: Single-particle and multiple-particle mechanism: A schematic representation of the SP- and MP-mechanisms. According to the SP-process a solitary energetical carrier can dissociate the bond. The MP-mechanism corresponds to the subsequent bombardment of the the bond by several colder carriers followed by the bond excitation and eventually the H release. Figure source: [23].

to dissociate (multiple particle process, shown in the right panel of Figure 2.28). The bond breakage process at the interface between substrate and oxide results in P_b centers [91, 92], which can capture and emit charge carriers and distort device characteristics. For example, the trapped charges act as Coulomb scattering centers and degrade the carrier mobility. The capture and emission dynamics are described by the standard SRH theory.

For the modeling of bond dissociation, the Si-H bond is typically modeled using a truncated harmonic oscillator [23]. This oscillator is characterized by the system of eigenstates as shown in Figure 2.29. The single particle process corresponds to the excitation from one of the eigenstates to the last bonded state and the transition to the transport state. Most probably, the interaction energy excites the bonding electron of H to an antibonding state, which consequently leads to the release of the hydrogen atom. The desorption rate of this process can be written as the acceleration integral [90]

$$R_{\mathrm{SP}} \sim \int_{E_{\mathrm{th}}}^{\infty} I(E)P(E)\sigma(E)dE \tag{2.40}$$

with

R_{SP}	desorption rate for the single particle process
E_{th}	threshold energy
$I(E)$	carrier impact frequency on the surface per unit area within the range of $[E; E + dE]$,
$P(E)$	desorption probability
$\sigma(E)$	energy-dependent reaction cross section.

The multiple particle process corresponds to an excitation from one eigenstate to the next with each scattering process between a colder carrier and the Si-H bond, whereby the occupation number obeys a Bose-Einstein distribution. This multivibrational mode excitation is accompanied by the phonon mode decay with the corresponding rates

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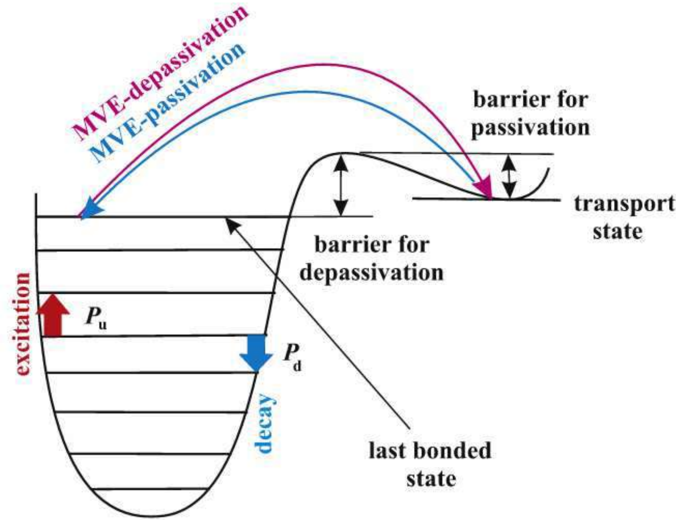

Figure 2.29.: The Si–H bond as a truncated oscillator: The depassivation and passivation processes are highlighted. Figure source: [93].

$$P_{\mathrm{d}} \sim \int_{E_{\mathrm{th}}}^{\infty} I(E)\sigma_{\mathrm{ab}}(E)[1 - f_{\mathrm{ph}}(E - \hbar\omega)]\mathrm{d}E \tag{2.41}$$

$$P_{\mathrm{u}} \sim \int_{E_{\mathrm{th}}}^{\infty} I(E)\sigma_{\mathrm{emi}}(E)[1 - f_{\mathrm{ph}}(E + \hbar\omega)]\mathrm{d}E \tag{2.42}$$

with

P_{d} / P_{u}	total phonon emission / absorption rate
E_{th}	Threshold energy
$I(E)$	carrier impact frequency on the surface (per unit energy and area),
$\sigma_{\mathrm{ab}}(E)$ / $\sigma_{\mathrm{emi}}(E)$	scattering cross-sections for bond-phonon emission / absorption
f_{ph}	phonon occupation numbers
$\hbar\omega$	phonon energy.

The bond rupture happens from the last bonded level to the transport state. Finally, the bond-breakage rate corresponding to the multiple particle process can be written as

$$R_{\mathrm{MP}} = \left(\frac{E_{\mathrm{B}}}{\hbar\omega} + 1\right)\left[P_{\mathrm{d}} + \mathrm{e}^{-\hbar\omega/(k_{\mathrm{B}}T_{\mathrm{L}})}\right]\left[\frac{P_{\mathrm{u}} + \omega_{\mathrm{e}}}{P_{\mathrm{d}} + \mathrm{e}^{-\hbar\omega/(k_{\mathrm{B}}T_{\mathrm{L}})}}\right]^{-E_{\mathrm{B}}/(\hbar\omega)} \tag{2.43}$$

with

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R_{MP}	bond-breakage rate corresponding to the multiple particle process
E_{B}	energy of the last bonded level in the quantum well, dissociation energy
$\hbar\omega$	phonon energy
k_{B}	Boltzmann constant
T_{L}	lattice temperature
P_{d} / P_{u}	total phonon emission / absorption rate
ω_{e}	phonon reciprocal life-time.

The Hess model was quite revolutionary because it expressed the idea that HCD is controlled by the distribution function, which enters the acceleration integral in Equation 2.40. It consideres the interface traps on a microscopic level. However, it remains unconnected to the device level. For example, the degradation of parameters like g_{m} and $I_{\mathrm{D,lin}}$ cannot be modeled with the Hess model only.

2.2.3. Energy Driven Paradigm

Rauch and LaRosa suggested an alternative empirical model, which reflects the importance of the carrier energy on the degradation. The so-called energy driven paradigm consideres that in the case of scaled devices with channel lengths less than 180 nm the driving force of HCD is the carrier rather than the electric field [83, 94, 95, 24] as it was in the "lucky-electron" model. One further issue associated with the approach of Rauch and LaRosa is the increasing impact of the electron-electron scattering on HCD at reduced channel lengths because it populates the high energy tail of the carrier distribution function.

The impact ionization rate as well as the rate of hot-carrier induced interface state generation is controlled by terms as the following.

$$\int f(E)\sigma(E)\mathrm{d}E$$

$f(E)$ is the carrier distribution function and $\sigma(E)$ is the reaction cross section. While the first is strongly decaying with increasing energy, the second one grows power-law-likely. The product of both results in a maximum. As long as this is sufficiently narrow, it can be approximated by a delta-function, which avoids time-consuming calculations of the carrier distribution function. The integral can be substituted by a stress condition related empirical factor.

Although the findings of Rauch and LaRosa are a substantial simplification of the HCD treatment, the energy driven paradigm suffers from some shortcomings. For example, the product $f(E)\sigma(E)$ is not necessarily narrow. Moreover, the energy driven paradigm does not consider N_{it} as a distributed quantity and, therefore, it does not capture the strong localization of HCD.

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2.2.4. Bravaix Model

The Braivaix model is based on features of both, the Hess model and the findings of Rauch and LaRosa. Important ideas of the Hess model which enter the Bravaix model are the interplay between single and multiple carrier mechanisms as well as the realization that the damage is defined by the carrier distribution function. The latter enters Equation 2.43 via the particle flux $I(E)$ in P_d and P_u. The findings of Rauch and LaRosa enter the Bravaix model via the substitution of the acceleration integral by the stress condition related empirical factor discussed in the previous subsection.

The Bravaix model describes the kinetics of the oscillator (Figure 2.29) as a system of rate equations [90, 96, 22]:

$$\frac{\mathrm{d}n_0}{\mathrm{d}t} = P_\mathrm{d} n_1 - P_\mathrm{u} n_0 \tag{2.44}$$

$$\frac{\mathrm{d}n_\mathrm{i}}{\mathrm{d}t} = P_\mathrm{d}(n_\mathrm{i+1} - n_\mathrm{i}) - P_\mathrm{u}(n_\mathrm{i} - n_\mathrm{i-1}) \tag{2.45}$$

$$\frac{\mathrm{d}n_\mathrm{N}}{\mathrm{d}t} = P_\mathrm{u} n_\mathrm{N-1} - \lambda_\mathrm{emi} N_\mathrm{it}[H^*] \tag{2.46}$$

with

n_i	occupancy of the i_th oscillator level
t	time
P_d / P_u	total phonon emission / absorption rate
N	last bonded level
λ_emi	rate of hydrogen released to the transport state, thermal barrier
N_it	interface-charge density
$[H^*]$	concentration of the mobile hydrogen

The phonon emission and absorbtion rate are calculated differently to Equations 2.41 and 2.42 [90]:

$$P_\mathrm{d} = \int j_\mathrm{D} \sigma dE_\mathrm{e} + \frac{1}{\tau} \tag{2.47}$$

$$P_\mathrm{u} = \int j_\mathrm{D} \sigma dE_\mathrm{e} + \frac{1}{\tau} \mathrm{e}^{-\hbar\omega/(k_\mathrm{B} T_\mathrm{L})} \tag{2.48}$$

with

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P_d / P_u	total phonon emission / absorption rate
j_D	drain current density
σ	cross-section of excitation of a phonon mode
τ	phonon life-time
$\hbar\omega$	phonon energy
k_B	Boltzmann constant
T_L	lattice temperature

Based on the energy-driven paradigm the integral can be substituted by the empirical factor S_MP. With this and for the case of weak bond-breakage rate the equation system 2.44 to 2.46 can be solved for N_it to yield:

$$N_\mathrm{it} = \sqrt{N_0 \lambda_\mathrm{emi} \left(\frac{P_\mathrm{u}}{P_\mathrm{d}}\right)^N} t^{1/2} \tag{2.49}$$

The multiple particle process related interface state generation rate (bond-breakage rate corresponding to the multiple particle process) can be written as

$$R_\mathrm{MP} \sim N_0 \left[\frac{S_\mathrm{MP}(I_\mathrm{D}/q) + \omega_\mathrm{e} \mathrm{e}^{[-\hbar\omega/(k_\mathrm{B}T_\mathrm{L})]}}{S_\mathrm{MP}(I_\mathrm{D}/q) + \omega_\mathrm{e}}\right]^{E_\mathrm{B}/(\hbar\omega)} \mathrm{e}^{-E_\mathrm{emi}/(k_\mathrm{B}T_\mathrm{L})} \tag{2.50}$$

with

N_0	ground state, it is assumed that the bond occurs most likely in the ground state $n_0 \approx \sum n_\mathrm{i} \approx N_0$
E_B	energy of the last bonded level in the quantum well, dissociation energy
S_MP	empirical factor substituting the acceleration factor (energy-driven paradigm)
I_D	drain current
E_emi	thermal energy barrier of hydrogen released to the transport state
$\hbar\omega$	phonon energy
k_B	Boltzmann constant
T_L	lattice temperature
ω_e	phonon reciprocal life-time.

Depending on whether the stretching or bending vibrational mode is considered, the values for E_B, $\hbar\omega$ and ω_e can be chosen [96]. With the findings of all involved persons, the dissociation rate by multiple particle processes is represented quite well. Consequently, the life-time can be estimated for the different regimes like the hot-carrier regime where the single particle mechanism plays the dominant role, the intermediate case where electron-electron scattering leads to a population of the high energetical tail of the charge carriers and the high electron flux where the multiple particle process dominates the bond dissociation.

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Nevertheless, the missing carrier transport treatment which allows one to distinguish between the single particle process, electron-electron scattering, and multiple particle process driven modes, affects the model quality. Since these mechanisms affect each other via the carrier distribution function they have to be considered. Moreover, the scheme for the single particle process rate is based on fitting parameters and not on physical mechanisms.

2.2.5. HCD Model Based on the Exact Solution of the Boltzmann Transport Equation

In order to overcome the disadvantages of the Braivaix model, a model based on the exact solution of the Boltzmann transport equation (BTE) has been proposed [93, 23, 97, 98]. This approach captures the physical picture behind HCD more accurately by covering three aspects of HCD: the carrier transport, a microscopic description of the defect creation kinetics and the degraded device simulation. The aspect of the carrier transport is solved by using either a stochastic or a deterministic solver of the BTE. While the stochastic solver employs the Monte Carlo method, the deterministic solver is based on the expansion of the carrier density function in a series of spherical harmonics. The latter appears especially for ultra-scaled devices more appropriate because electron-electron scattering, for example, can be implemented easily without leading to a long computational time.

Furthermore, for a proper HCD treatment one has to consider both types of carriers, minority and majority. Due to impact ionization (II), secondary majority carriers are generated. If the device is operated near or beyond pinch-off conditions, channel carriers with sufficient kinetic energy can trigger impact ionization, thereby, generate secondary majority carriers which are accelerated towards the source due to the channel electric field. As a consequence, additional interface states to those created by the primary channel carriers can be created and result in an additional peak of the interface state density N_{it} shifted towards the source (see Figure 2.30). This additionally created interface states significantly change the degradation characteristics [99, 100].

For a proper modeling approach, the distribution functions for both, majority and minority charge carriers, are evaluated at each point at the interface. The distribution functions enter the carrier acceleration integral, which controls single particle as well as multiple particle mechanisms.

$$I = \int_{E_{\mathrm{th}}}^{\infty} f(E)g(E)\sigma(E)v(E)dE \tag{2.51}$$

with

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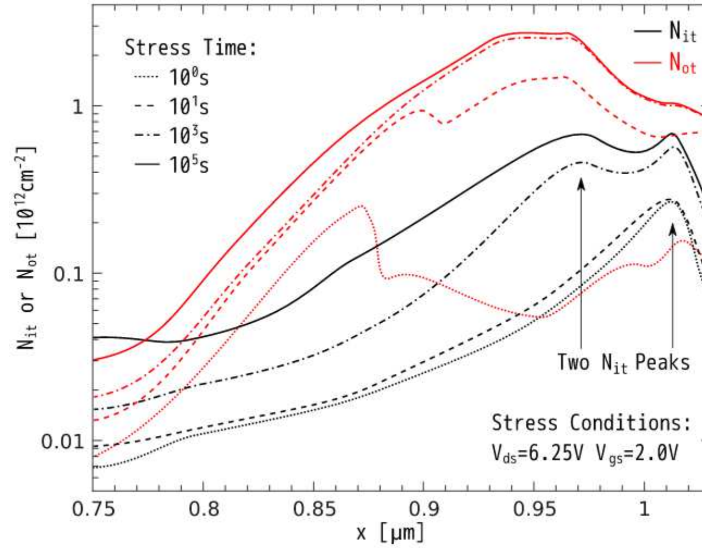

Figure 2.30.: Evolution of lateral trap density distribution with stress time: N_{it} and N_{ot} as a function of the lateral position at different stress times. It is clearly visible that a second N_{it} peak occurs due to interface states created by secondary generated majority carriers. Figure source: [101].

I	carrier acceleration integral
E_{th}	threshold energy
$f(E)$	carrier distribution function
$g(E)$	density-of-states
$\sigma(E)$	reaction cross section
$v(E)$	carrier velocity

For the single particle process, the superposition of electron and hole acceleration integrals weighted with the corresponding attempt frequencies gives the generation rate (bond-breakage rate corresponding to the single particle process)

$$R_{\mathrm{SP}} = N_0 \left[1 - \mathrm{e}^{-(\nu_{\mathrm{SC,e}} I_{\mathrm{SC,e}} + \nu_{\mathrm{SC,h}} I_{\mathrm{SC,h}})t}\right] \tag{2.52}$$

with

N_0	ground state
$\nu_{\mathrm{SC,e}}$ / $\nu_{\mathrm{SC,h}}$	attempt frequencies for electrons / holes
$I_{\mathrm{SC,e}}$ / $I_{\mathrm{SC,h}}$	acceleration integral for electrons / holes
t	time

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For the multiple particle process, the Si-H bond is treated as a truncated harmonic oscillator, which leads to the bond-breakage rate corresponding to the multiple particle process

$$R_{\mathrm{MP}} = N_0 \left[\frac{\lambda_{\mathrm{emi}}}{P_{\mathrm{pass}}} \left(\frac{P_{\mathrm{u}}}{P_{\mathrm{d}}} \right)^N \left(1 - \mathrm{e}^{\lambda_{\mathrm{emi}} t}\right) \right]^{1/2} \tag{2.53}$$

with

N_0	ground state
N	last bonded level
λ_{emi}	rate of hydrogen released to the transport state, thermal barrier
P_{pass}	rate of passivation of dangling bonds
P_{d} / P_{u}	total phonon emission / absorption rate
t	time.

The model is able to capture the degradation of MOSFET parameters like $I_{\mathrm{D,lin}}$ measured in devices with different channel lengths and at different hot-carrier (HC) stress conditions. As will be shown in Chapter 5, also effects associated with oxide defects can be explained. In particular, with a thorough carrier transport treatment and under consideration of secondary generated majority carriers in the channel also recovery after different stress conditions can be modeled properly. However, one open question remains, namely how oxide traps contribute to HCD. As already shown in Figure 2.30, not only N_{it} but also N_{ot} increases with the stress time. It has been assumed that so-called turn-around effects shown in Figure 2.31 could be the result of the interplay between different defect types [23].

2.2.6. Turn-Around Effects

Stress time-dependent turn-arounds of degradation as shown in Figure 2.31 have been discussed in literature for ΔV_{th} and $\Delta I_{\mathrm{D,lin}}$ [99, 100, 102]. A turn-around means in this regard that the degradation trend changes after a certain stress time. In Figure 2.31, ΔV_{th} initially decreases while after 10ks it starts to increase.

In the case of V_{th} degradation, it has been proposed that the turn-around can be explained by two aspects. The first aspect concerns the additionally created interface states by secondary generated carriers as already mentioned in the previous subsection. The second aspect, which is finally responsible for the turn-around itself, is the interplay between ΔV_{th} contributions of defects at the interface and the oxide [101]. In case of ΔV_{th} degradation, it has been demonstrated that during stress V_{th} decreases due to minority charge carriers trapping in the oxide while after a certain stress time it increases due to trapping of majority charge carriers by interface traps, generated during stress. This turn-around effect is caused by the partial compensation of the charge stored in the oxide traps by interface state trapping.

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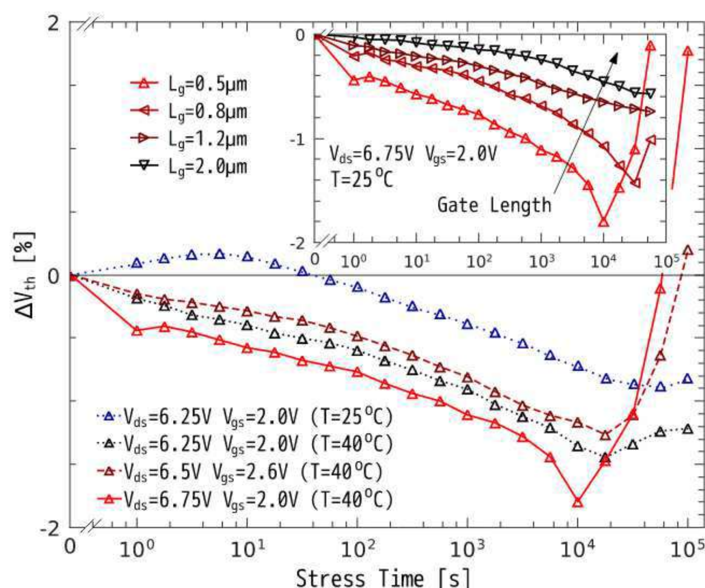

Figure 2.31.: Turn-around of the threshold voltage shift: ΔV_{th} as a function of stress time at various voltages. Initially ΔV_{th} decreases due to minority charge trapping in the oxide while after 10ks it starts to increase due to trapping of majority carriers by interface defects. Figure source: [101].

The explanation for the turn-around in $\Delta I_{\mathrm{D,lin}}$ is quite similar to the one for the turn-around of ΔV_{th}. Charges of opposite signs are trapped in different sections of the characterized transistor [102]. As a result, $\Delta I_{\mathrm{D,lin}}$ first increases followed by a decrease for longer stress times. In Section 5.1 it will be shown that a turn-around effect was measured. However, the exact interplay between oxide defects and interface defects remains still an open question.

2.3. Mixed NBTI/HC Conditions

Typically BTI and HCD are discussed and characterized independently from each other with regard to defect creation and annealing, the permanent and recoverable component, and their impact on parameter shifts. Although MOSFETs are not only subjected to either BTI or HCD conditions but also to stress conditions where both mechanisms contribute to degradation, only a limited number of studies is available on their simultaneous contribution or their interplay [21, 25, 26, 27, 103]. In this context, the term of mixed BTI/HC stress is used in order to express conditions linked to $|V_{\mathrm{G}}^{\mathrm{str}}| > 0\,\mathrm{V}$ and $|V_{\mathrm{D}}^{\mathrm{str}}| > 0\,\mathrm{V}$.

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2.3.1. Mixed NBTI/HC stress

So far, oxide defects in the context of BTI where V_{D} is zero during stress have been discussed. In such a case, E_{OX} could be approximated as laterally homogenous, which means that it has the same value for each lateral defect position (X_{T}). The behavior of oxide traps depend on the defect properties, which are reflected in the NMP rates. Their contribution to degradation and recovery is given typically by characteristic times, which fulfill the following requirements: $\tau_{\mathrm{c}}<t_{\mathrm{str,max}}$ and $\tau_{\mathrm{e}}\in[t_{\mathrm{rec,min}},t_{\mathrm{rec,max}}]$. In this subsection the impact of $|V_{\mathrm{D}}^{\mathrm{str}}|>0\,\mathrm{V}$ on the contribution of oxide defects to degradation and recovery is discussed.

In the case of a pMOSFET, as soon as both, V_{G} and V_{D}, are less than zero, the lateral dependence of the channel potential (V_{ch}) has to be considered. In the simplest case, V_{ch} can be approximated linearly [27]

$$V_{\mathrm{ch}}(X_{\mathrm{T}}) = V_{\mathrm{D}}\frac{X_T}{L} \tag{2.54}$$

for those positions where the condition of inversion is fulfilled. At the pinch-off point it can be written as

$$V_{\mathrm{ch}}(X_{\mathrm{T}}) = (V_{\mathrm{G}} - V_{\mathrm{th}})\frac{X_{\mathrm{T}}}{L - L_{\mathrm{sat}}} \tag{2.55}$$

with

V_{ch}	channel potential
V_{D}	drain voltage
V_{G}	gate voltage
X_T	absolute lateral position (0 at source and L at drain
L	channel length
V_{th}	threshold voltage.

Since the applied V_{G} is constant over all lateral positions, but the channel potential increases from source to drain, E_{OX}, which is proportional to the difference of both, will decrease from source to drain. As E_{OX} remains unaffected at the source-side compared to homogeneous NBTI conditions, but is reduced at the drain end of the channel, different lateral positions will contribute differently to degradation and recovery. In a very simplified model based on an exponential dependence of the degradation on the applied gate to channel voltage, a lateral position dependent ΔV_{th} can be expressed as

$$\Delta V_{\mathrm{th}}(X_{\mathrm{T}}) = V_0(t_{\mathrm{str}})\mathrm{e}^{C\left(V_{\mathrm{G}}^{\mathrm{str}} - V_{\mathrm{ch}}^{\mathrm{str}}(X_{\mathrm{T}})\right)} \tag{2.56}$$

with

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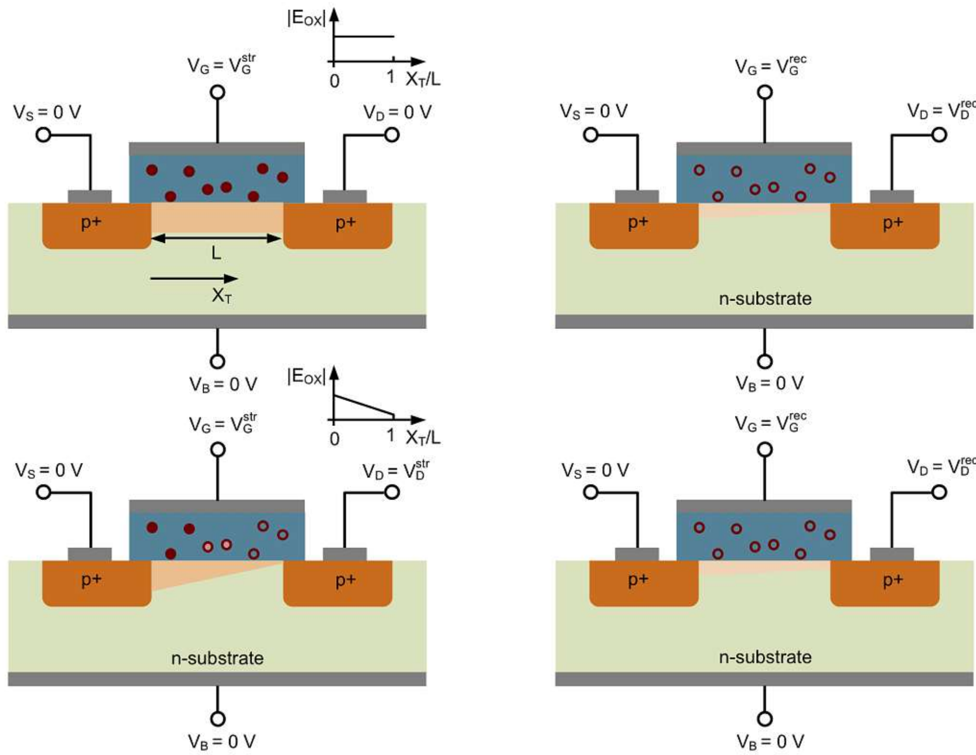

Figure 2.32.: Contribution of active oxide defects at different stress conditions shown for a pMOSFET: Schematic illustration of eight uniformly distributed oxide defects. **Top:** At homogneous NBTI stress conditions (left) all defects capture a hole, each shown as filled circles and emit at recovery conditions (right), shown as empty circles. Therefore, all defects contribute to the recoverable component. **Bottom:** At inhomoneous NBTI stress or in more general mixed stress conditions where $V_{\mathrm{G}} = V_{\mathrm{G}}^{\mathrm{str}}$ and $V_{\mathrm{D}} = V_{\mathrm{D}}^{\mathrm{str}}$ (left) three defects near the source capture a hole each, illustrated as filled circles, two defects in the center capture a hole each but with a reduced occupancy, shown as light red filled circles and three defects near the drain do not capture a hole at all, shown as empty circles. At recover conditions (right) only defects which have captured a hole during stress – something in between of three and five – emit. Therefore, only three to five defects contribute to the recoverable component instead of eight.

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ΔV_{th}	position dependent threshold voltage shift
V_0	stress time and temperature dependent constant
X_T	absolute lateral position (0 at source and L at drain)
t_{str}	stress time
C	technology dependent constant
V_{ch}	channel potential.

Equation 2.56 shows that while each lateral position contributes equally to ΔV_{th} for homogeneous NBTI, at inhomogenous NBTI conditions with $V_{\mathrm{G}}^{\mathrm{str}} < 0\,\mathrm{V}$ and $V_{\mathrm{D}}^{\mathrm{str}} < 0\,\mathrm{V}$ each position contributes differently. This means that positions within the region near the source, where V_{ch} is very low, contribute more to ΔV_{th} than positions within the region near the drain, where V_{ch} might even reduce E_{OX} to zero. From the perspective of degradation being the result of capture events of oxide defects, Figure 2.32 shows schematically what would happen from an electrostatic point of view. It is assumed that the shown eight defects, uniformly distributed over all lateral positions, contribute to degradation and recovery at NBTI conditions by capturing a hole during stress and emitting it during recovery. This means that the energy levels of the defects are below the Fermi level at recovery conditions, and at each position E_{OX} is sufficient to shift the energy levels above the Fermi level during stress. In other words all shown defects are within the active energy region and $\tau_{\mathrm{c}}<t_{\mathrm{str,max}}$ as well as $\tau_{\mathrm{e}}\in [t_{\mathrm{rec,min}},t_{\mathrm{rec,max}}]$. By contrast, in the case of inhomogenous NBTI conditions, E_{OX} remains quite unaffected in the region near the source but is seriously reduced in the region near the drain. As a result, the energy level of source-side defects can be shifted above the Fermi level during stress, thus such defects can capture a hole during stress and emit it during recovery. Quite to the contrary, the energy level of some drain-side defects can no longer be shifted above the Fermi level during stress, thus, the drain-side defects do not capture a hole. Defects in the central region most probably will show a reduced occupancy.

In Figure 2.32 it it can be seen that not only the contribution of oxide defects to the total degradation changes at inhomogneous NBTI conditions compared to homogenous NBTI conditions but also their contribution to recovery. In this context, after homogeneous NBTI stress all eight defects emit a hole during recovery but only three to five defects emit one after inhomogenous NBTI stress. Thus, recovery will be reduced with increasing $V_{\mathrm{D}}^{\mathrm{str}}$.

In such a simplified electrostatic picture, the significant change of the behavior of drain-side defects is attributed to the E_{OX} dependence of the characteristic capture and emission times (Equation 2.25 and Equation 2.26) and of the occupancy (Equation 2.17 and Equation 2.18). At the defect level a reduction of E_{OX} typically leads to an increase of τ_{c}, a decrease of τ_{e} and a decrease of the occupancy. Therefore, at inhomogeneous NBTI stress conditions, the transition constants of source-side defects remain nearly unmodified while those of drain-side defects are significantly modified. In other words, the active energy region narrows from source to drain as shown in Figure 2.33. As a consequence, independently of the total number of defects, those at the drain-side will

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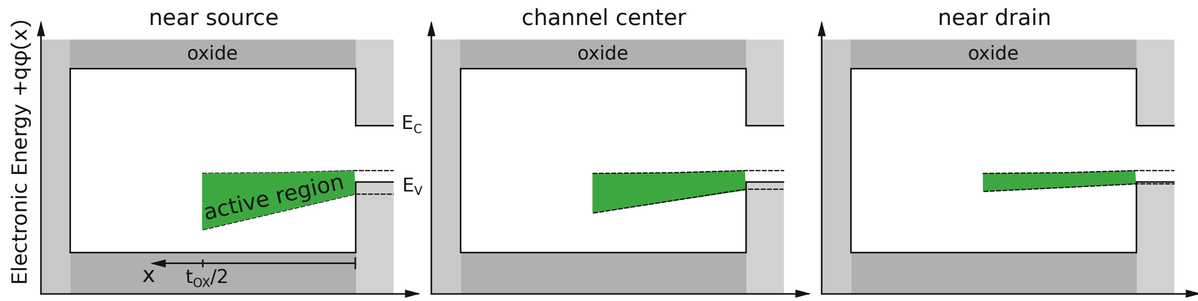

Figure 2.33.: Narrowing of the active energy region from source to drain: Due to the inhomogeneous E_{OX} in the case of mixed NBTI/HC stress, the active energy region narrows from source to drain. Therefore, less defects contribute to degradation and recovery at the drain-side than at the source-side.

contribute less to degradation and recovery than those in the central region or at the source-side.

As will be discussed in Chapter 5, the whole picture is more complicated since effects like II have to be taken into account as well. As a main result of this thesis, it will be shown that taking only the modified electrostatics during mixed NBTI/HC stress into accound does not reflect the defect behavior in experiments fully.

2.3.2. Step Height Dependence on the Drain Voltage

The drain voltage has not only a considerable impact on the defect behavior during stress as shown in the previous section but also on the behavior during recovery. It has been shown that the exponential step height distribution introduced in Equation 2.2 depends on the readout conditions [17]. A typical drain voltage at recovery conditions ($V_{\mathrm{D}}^{\mathrm{rec}}$) is $-0.1\,\mathrm{V}$ (for pMOSFETs) and the gate voltage $V_{\mathrm{G}}^{\mathrm{rec}} \approx V_{\mathrm{th}}$. Similar to what has been discussed in the previous subsection, the lateral local electrostatic conditions change when $V_{\mathrm{D}}^{\mathrm{rec}} < -0.1\,\mathrm{V}$. As a consequence, defects near the drain contribute differently to the recovery trace or an RTN signal than defects near the source and the exponential tail shown in Figure 2.8 decreases.

In the case of an RTN signal, the change of E_{OX} due to an increased readout drain voltage shifts τ_{c} of defects in the vicinity of the drain outside the measurement window. Therefore, such defects can no longer capture and emit charge carriers. Consequently, the number of active RTN defects changes, which affects the exponential step height distribution. In the case of defects which capture a charge carrier under stress conditions and emit it under recovery conditions, only τ_{e} can be affected by a changed readout drain voltage. In particular, τ_{e} of drain-side defects and defects located in the center of the channel is shifted towards smaller emission times if $V_{\mathrm{D}}^{\mathrm{rec}} < -0.1\,\mathrm{V}$. Thus, such defects still contribute to the recovery of the device.

However, for defects which capture a charge carrier during stress and emit it during recovery another consequence of an increased $|V_{\mathrm{D}}^{\mathrm{rec}}|$ has to be considered. According

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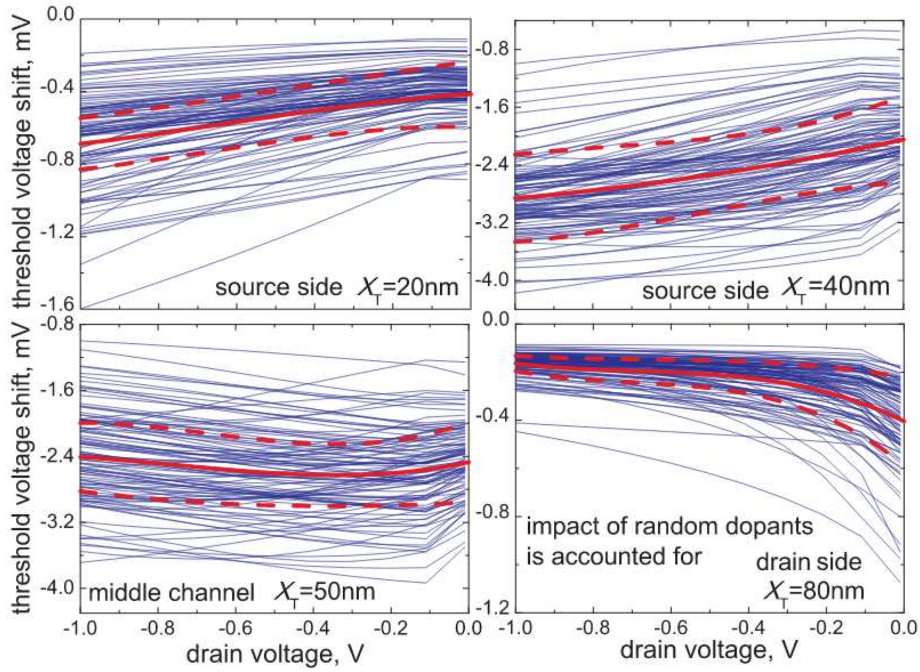

Figure 2.34.: Step height with respect to the drain voltage at different lateral positions: The $d(V_\mathrm{D})$ characteristics for 2.2 nm thick SiON oxide film pMOSFETs with $W = 150$ nm and $L = 100$ nm with 100 different random dopant configurations and four different lateral defect coordinates X_T simulated using TCAD. The red lines indicate the characteristics with average (solid) and plus/minus standard deviation cubic parameterization coefficients (dashed). Since the shape of the curves is more strongly affected by the lateral trap position than by the random dopant distribution, it can be used as a defect fingerprint and allows to evaluate the lateral defect coordinate. Figure source: [104].

to simulations considering different random dopant configurations it has been shown that the step heights of the active defects change with $V_\mathrm{D}^\mathrm{rec}$ [104]. This effect is shown in Figure 2.34 for 100 different random dopant configurations and four different lateral defect coordinates using 2.2 nm thick SiON oxide film pMOSFETs with $W = 150$ nm and $L = 100$ nm. The average behavior of the step height with respect to the drain voltage at a constant gate voltage $d(V_\mathrm{D})$ clearly shows that the shape of the curves is affected by the lateral defect position. For example, while $|d(V_\mathrm{D})|$ of defects in the vicinity of the source at $X_\mathrm{T}/L = 0.2$ (0 is at source and 1 is at drain) increases for increasing $|V_\mathrm{D}|$, $|d(V_\mathrm{D})|$ of defects in the vicinity of the drain at $X_\mathrm{T}/L = 0.8$ decreases for increasing $|V_\mathrm{D}|$. Therefore, the $d(V_\mathrm{D})$ characteristic can be used as a defect fingerprint and its lateral position can be extracted.

For the position extraction a simplified technique can be applied [104]. The ΔV_th step heights with respect to the readout drain bias can be fitted linearly using such a simplified technique. The relative lateral position can be extracted using

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$$\frac{X_T}{L} = 0.5 - \text{sign}(P_1)\sqrt{2\alpha^2 \log\left(\frac{P_{0\max}}{P_0}\right)} \tag{2.57}$$

with

X_T	lateral position in the channel
L	channel length
P_1	slope of the linear fit
α	constant, found to be approximately 0.17 [104]
$P_{0\max}$	largest step height observed in the measurements, corresponds to $P_0(X_T = L/2)$
P_0	intercept of the linear fit

This technique is based on the realization that the main information regarding the lateral trap coordinate is given by the slope (P_1) and the intercept (P_0) of the linear fit. The sign of P_1 determines whether the trap is at the source- or at the drain-side. P_0 is responsible for the proximity of the defect to one of the electrodes. The shape of P_0 with respect to the lateral defect position is symmetric (also shown in [17]) and can be approximated by a Gaussian function

$$P_0 = P_{0\max} e^{(X_T - L/2)^2/(2\sigma)}$$

with $P_{0\max} = P_0(X_T = L/2)$ and $P_0(X_T = 0) = P_0(X_T = L) = 0$.

The standard deviation has been found to be proportional to the channel length. In other words, in experimental data defects which cause small steps in the ΔV_{th} traces compared to the steps caused by other defects in the same device, are located in the vicinity of the source or the drain. Defects which cause comparably large ΔV_{th} steps are located near the center of the channel. Depending on the behavior of $d(V_{\text{D}})$ (increasing or decreasing with increasing $|V_{\text{D}}|$) the defect's position can be assigned to either the source-side or the drain-side. This technique has been applied successfully to measurement data presented in Chapter 5 in order to extract the lateral defect position [104, 105].

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Chapter 3

Experimental Characterization

The study of degradation mechanisms prevalent in transistors includes a thorough experimental characterization of time-dependent variation and time dependent drifts of MOSFET parameters. Therefore, different measurement methods and sequences have been developed. In this chapter, an overview is given and the purposes, advantages and challenges of commonly used techniques are introduced. Then, challenges which had to be faced during the measurements for this thesis, are discussed. In this context, the fact that most of the measurement techniques have been developed for the characterization of either NBTI or HCD degradation plays an important role. For the discussion of such challenges, the focus lies on the V_{th} extraction methods applied using MSM techniques as this method is most relevant for the understanding of the results presented in Chapter 5.

As an introduction to this chapter, Figure 3.1 illustrates the stress conditions for triggering both degradation mechanisms, NBTI and HCD, including the so-called mixed NBTI/HC stress conditions applied for the characterization of the unavoidable interplay of both. The region of stress conditions in this figure shows the 2-dimensional parameter space ($V_{\mathrm{D}}^{\mathrm{str}}$,$V_{\mathrm{G}}^{\mathrm{str}}$) applied in this thesis. The measurements discussed in the current and the following chapters were conducted on 2.2 nm SiON pMOSFETs of a 130 nm commercial technology ($V_{\mathrm{DD}} = -1.5\,\mathrm{V}$ and $V_{\mathrm{th}} = 465\,\mathrm{mV}$). One has to distinguish between large-area devices and nano-scale devices. The first have the dimensions $W = 10\,\mu\mathrm{m}$ and $L = 120\,\mathrm{nm}$ or $L = 130\,\mathrm{nm}$, and the second $W = 160\,\mathrm{nm}$ and $L = 120\,\mathrm{nm}$ or $L = 130\,\mathrm{nm}$.

3.1. On-The-Fly (OTF) Measurements

Using the OTF measurement method, MOSFET parameter shifts are probed directly during operation without interruption of the applied voltages. It was introduced in 2004 for the purpose of measuring the device degradation ΔV_{th} during stress conditions [106], which typically refer to much higher biases than used at nominal operating conditions. This technique aims for the direct characterization of the ΔV_{th} evolution.

The basic measurement procedure is shown in Figure 3.2 for BTI measurements. It consists of a periodic modulation of $V_{\mathrm{G}}^{\mathrm{str}}$ with the modulation amplitude ($\Delta V_{\mathrm{G}}^{\mathrm{str}}/2$) at a

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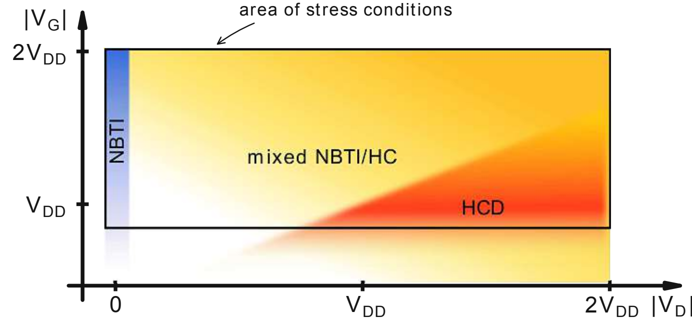

Figure 3.1.: Range of stress conditions: Schematic illustration of the different stress conditions NBTI, HCD and mixed NBTI/HC. The area of stress conditions defines the boundaries of the 2-dimensional parameter space ($V_{\mathrm{D}}^{\mathrm{str}}$,$V_{\mathrm{G}}^{\mathrm{str}}$) applied in this thesis. Different colors separate the voltage combinations which trigger different degradation mechanisms, while the color intensity indicates the increasing impact of the stress on the parameter shifts.

certain drain measurement voltage ($V_{\mathrm{D}}^{\mathrm{meas}}$) while I_{D} is determined at three measurement points for each modulation period n. The modulation of $V_{\mathrm{G}}^{\mathrm{str}}$ induces a $\Delta I_{\mathrm{D}}(n)$, which changes over the modulation periods due to the degradation-induced ΔV_{th} during stress. From the modulation amplitude and the corresponding ΔI_{D} the transconductance can be obtained according to

$$g_{\mathrm{m}}(V_{\mathrm{G}}^{\mathrm{str}}, V_{\mathrm{D}}^{\mathrm{meas}}, t_{\mathrm{str}}) = \left.\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{G}}}\right|_{t_{\mathrm{str}},V_{\mathrm{th}}} = -\left.\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{th}}}\right|_{t_{\mathrm{str}},V_{\mathrm{G}}} \approx \frac{\Delta I_{\mathrm{D}}}{\Delta V_{\mathrm{G}}^{\mathrm{str}}} \tag{3.1}$$

with

$V_{\mathrm{G}}^{\mathrm{str}}$	gate stress voltage
$V_{\mathrm{D}}^{\mathrm{meas}}$	drain voltage applied during measurement
I_{D}	drain current
t_{str}	stress time
V_{th}	threshold voltage.

A step-by-step integration of $\partial I_{\mathrm{D}}/g_{\mathrm{m}}$ gives the threshold voltage shift during stress:

$$\Delta V_{\mathrm{th}}(t_{\mathrm{str}}) = -\int_{I_{\mathrm{D}}(0)}^{I_{\mathrm{D}}(t_{\mathrm{str}})} \frac{\partial I_{\mathrm{D}}}{g_{\mathrm{m}}(t_{\mathrm{str}})} \approx -\sum_{n=1}^{N} \frac{I_{\mathrm{D}}(n) - I_{\mathrm{D}}(n-1)}{1/2(g_{\mathrm{m}}(n) + g_{\mathrm{m}}(n+1))} \tag{3.2}$$

with

n	sequential number of measurement
$N+1$	number of I_{D} measurements.

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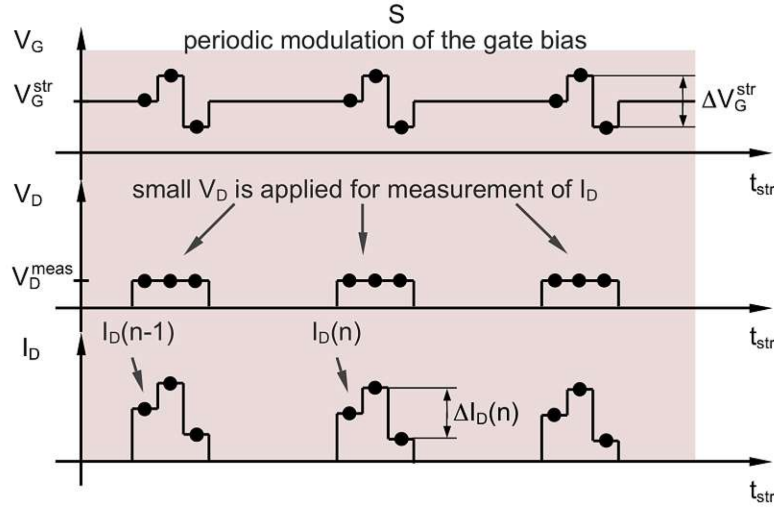

Figure 3.2.: OTF measurement procedure at NBTI conditions: $V_{\mathrm{G}}^{\mathrm{str}}$ is modulated periodically at a certain $V_{\mathrm{D}}^{\mathrm{meas}}$ while I_{D} is determined. With this, the transconductance $g_{\mathrm{m}} = \Delta I_{\mathrm{D}}/\Delta V_{\mathrm{G}}^{\mathrm{str}}$ can be calculated for each modulation step.

One challenge arises due to the fact that a parameter which is typically measured at a level near the threshold regime, namely V_{th}, is extracted from a measurement at stress level where the applied voltages are considerably higher than the threshold voltage. A proper separation of the impact of mobility fluctuations at stress level and V_{th} drifts at a level near the threshold regime on the measurement is, therefore, an issue [107]. The reason is that shifts of the transfer characteristics along the V_{G}-axis (V_{th} drifts) and "tilts" of the transfer characteristics (see Figure 3.3) are indistinguishable at the stress level. Such "tilts" are caused by defects located near or at the oxide/substrate interface which contribute to surface scattering and lower the carrier mobility. Based on a simple SPICE level 1 model, the following three parameter equation meets this challenge and separates the mobility and the V_{th} effect from each other:

$$G_{\mathrm{SD}} = \beta \frac{V_{\mathrm{G}} - V_{\mathrm{th}}}{1 + \Theta(V_{\mathrm{G}} - \mathrm{V}_{\mathrm{th}})} \tag{3.3}$$

with

G_{SD}	drain-source conductance
β	global mobility (parameter)
V_{G}	gate voltage
V_{th}	threshold voltage (parameter)
Θ	leads to an asymptotic approach to a maximum value $G_{\mathrm{SD}} = \beta/\Theta$ describing the mobility decrease due to surface roughness for high gate fields (parameter).

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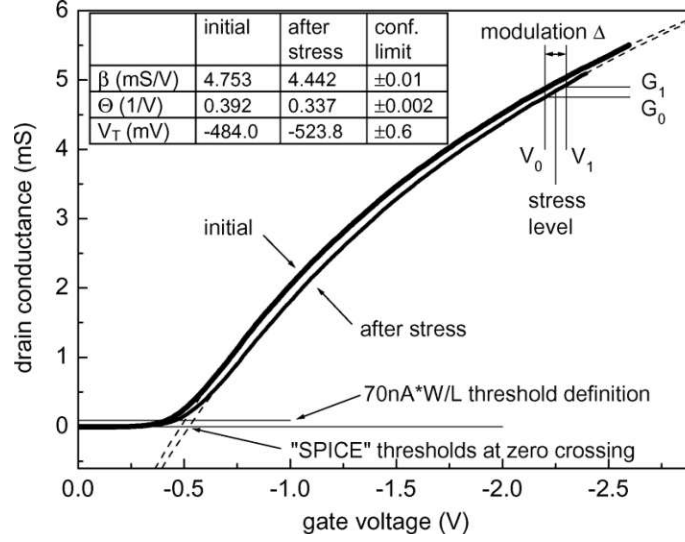

Figure 3.3.: Transfer characteristic before and after stress: Both curves are fitted using the SPICE level 1 model (dashed lines), which describes I_D above $g_\mathrm{m,max}$ very well. The difference between the zero crossing points is ΔV_th. Figure source: [107].

The SPICE model has an empirical background and describes I_D above $g_\mathrm{m,max}$ in the linear V_D regime rather well, as shown in Figure 3.3. However, it does not explain the threshold voltage shifts near the regime typically defined as the threshold regime in other measurement methods.

The extraction of ΔV_th depends on the modulation around $V_\mathrm{G}^\mathrm{str}$. Therefore, two measurement points on the transfer characteristics, namely $I_\mathrm{D}(V_0 = V_\mathrm{G}^\mathrm{str}\text{-}\Delta V_\mathrm{G}^\mathrm{str}/2)$ and $I_\mathrm{D}(V_1 = V_\mathrm{G}^\mathrm{str}+\Delta V_\mathrm{G}^\mathrm{str}/2)$ or $G_0 = G_\mathrm{SD}(V_0)$ and $G_1 = G_\mathrm{SD}(V_1)$, respectively, are inserted into Equation 3.3. Assuming that Θ is known from an initial characterization of the device the two-equation system containing only two unknowns, β and V_th, can be solved and as a result the threshold voltage can be calculated using

$$V_\mathrm{th} = V_0 - \frac{-(1+\Theta\Delta V_\mathrm{G}^\mathrm{str}) + \sqrt{(1+\Theta\Delta V_\mathrm{G}^\mathrm{str})^2 + 4\Theta G_0/g_\mathrm{m}}}{2\Theta} \tag{3.4}$$

with

V_0	corresponds to $V_\mathrm{G}^\mathrm{str} - \Delta V_\mathrm{G}^\mathrm{str}/2$
$V_\mathrm{G}^\mathrm{str}$	gate stress voltage
$\Delta V_\mathrm{G}^\mathrm{str}$	amplitude of gate stress voltage modulation
G_0	drain-source conductance at $V_\mathrm{G}^\mathrm{str} - \Delta V_\mathrm{G}^\mathrm{str}/2$
Θ	asymptotic approach to a maximum value $G_\mathrm{SD} = \beta/\Theta$ describing the mobility decrease due to surface roughness for high gate fields.

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Unfortunately, the extraction of V_{th} from a measurement at stress level and not from a measurement in the threshold regime introduces errors. In general, due to the modulation of the gate bias, the stress level changes, leading to a different degradation state than the state obtained after constant stress over the whole t_{str}. For example, it has been shown that ΔV_{th} is underestimated with the OTF method [43]. This systematic error could be minimized by a small modulation amplitude $\Delta V_{\mathrm{G}}^{\mathrm{str}}$. However, the error in g_{m} in Equation 3.1 is inversely proportional to $\Delta V_{\mathrm{G}}^{\mathrm{str}}$ and thus the smaller the amplitude is, the more error is introduced to g_{m}. Since the error in g_{m} determines the error of the V_{th} extraction in Equation 3.4, the choice of the modulation amplitude affects the statistical error in V_{th} [107].

Moreover, the modulation time plays a major role in the obtained degradation state. In order to minimize the change of the degradation state due to the modulation, the time within which the modulation is performed must be as short as possible. As a consequence, the integration time of the measurement has to be as short as possible. However, a decrease of the integration time in measurements leads to an increase of the statistical error of the measured V_{th}. Integration times in the order of µs or ms lead to a relative accuracy in the measured I_{D} of 10^{-4} or less. This corresponds to a statistical error of V_{th} of $\pm 12\,\mathrm{mV}$, which is too high. In order to achieve a statistical error of, e.g., $\pm 1\,\mathrm{mV}$ in V_{th}, I_{D} has to be measured with a relative accuracy of 8×10^{-6}. With standard equipment, the integration time required to achieve such a relative accuracy would be more than 20 ms which enlarges the measurement time enormously. Unfortunately, 20 ms is way too long if the prevention of recovery during the measurement is required. [107]

The OTF method is quite sensitive to mobility changes induced by stress [108] while it is quite insensitive to V_{th} changes because the I_{D}-V_{G} curve flattens out at the stress level [107]. Since V_{th} is the parameter of interest, an insensitivity to the changes of the threshold voltage shift is a considerable disadvantage. Together with the introduced systematic error due to the voltage modulation, this disadvantage makes the OTF method unfavorable for this thesis.

3.2. Charge Pumping (CP)

The CP effect was reported in 1969 for the first time [109]. One milestone in the development of this technique was the investigation and explanation of the method in 1984 [110]. The CP technique is a reliable and precise method for the measurement of defects at the substrate/oxide interface of a MOSFET. Thus, it is often used for the characterization of HCD, which is typically associated with an increase of such defects. The corresponding experimental setup is illustrated in Figure 3.4 and the schematic measurement procedure in Figure 3.5. The gate is pulsed by a generator between accumulation, in case of an nMOSFET defined by the low level of the gate voltage (V_{GL}) smaller than the flatband voltage (V_{FB}), and inversion, defined by the high level of the gate voltage (V_{GH}) higher than V_{th}. The source to substrate and drain to substrate diodes are slightly reverse biased. Simultaneously, the bulk current (I_{B}), which consists of leakage currents of the reverse biased diodes and the I_{CP}, is measured.

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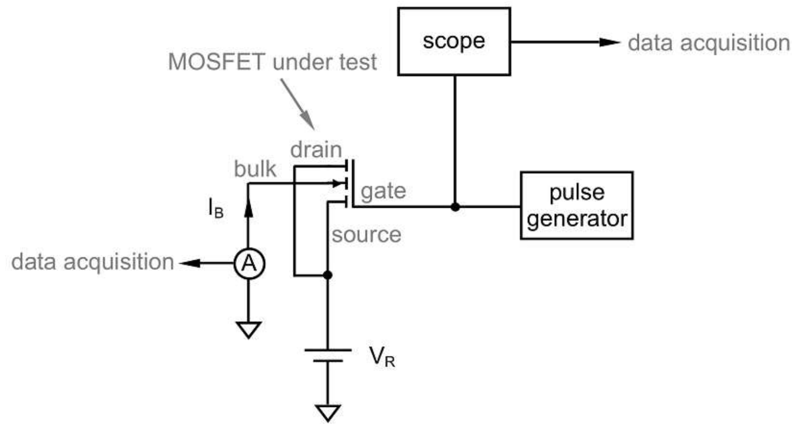

Figure 3.4.: Experimental setup for the CP technique: The gate is pulsed by a generator between accumulation and inversion while the source to substrate and drain to substrate diodes are slightly reverse biased (V_{R}). Simultaneously, the I_{CP} is measured.

The occurrence of I_{CP} can be explained by the recombination of majority carriers with minority carriers. A schematic illustration of the gate pulse and the corresponding I_{CP} is shown in Figure 3.5. When the pulse level is in the inversion phase (pulse level at V_{GH}), a thin layer in the substrate near the interface (channel) is depleted of the majority carriers and populated by minority carriers. This leads to a trapping of some of them by existing interface defects. As soon as the pulse drives the MOSFET into accumulation (pulse level at V_{GL}), the minority carriers leave the channel and the majority carriers flood it. Simultaneously, some of the interface defects with energies close to the valence band or conduction band can emit their trapped charges by thermal emission before the accumulation phase is reached due to the finite rising and falling slopes. These minority carriers are pushed into the substrate while switching to the accumulation phase without any contribution to I_{CP} because the overall amount of positive and negative charges is not changed throughout this process. By contrast, all other trapped minority carriers recombine with the majority carriers in accumulation, which gives rise to a net flow of charge into the substrate. This can be measured as I_{CP} and is directly proportional to the pulse frequency and the mean interface-state density. In the accumulation phase, some of the majority carriers are trapped by interface defects. Driving the MOSFET back into inversion results in a similar process as described for the transition from inversion to accumulation but with opposite carrier types.

As a consequence of the thermal emission of carriers during the rising and falling edge of the pulse, only interface defects within a particular energy range around midgap, which is smaller than the entire silicon bandgap, can be measured in I_{B}. The energy boundaries in the lower and upper half of the bandgap, defining the active energy interval, are given by [111]

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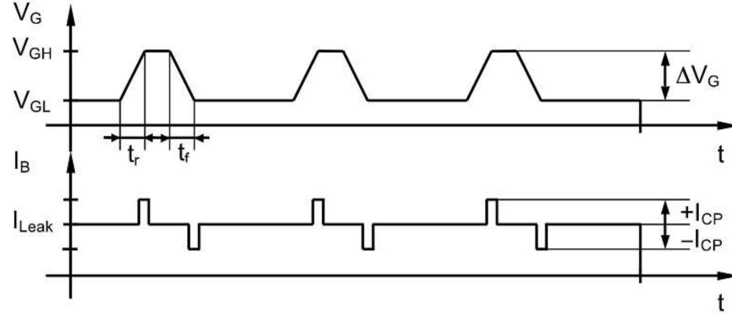

Figure 3.5.: Schematic illustration of the charge pumping effect: I_{CP} is measured as a change of I_{B} when sweeping V_{G} between inversion and accumulation back and forth. I_{CP} corresponds to the recombination current of trapped minority carriers and majority carriers and is a measure for the interface charge density.

$$E_{\mathrm{em,h}} = E_{\mathrm{i}}(T) - k_{\mathrm{B}}T\ln\left(v_{\mathrm{th}}(T)\sigma_{\mathrm{p}}n_{\mathrm{i}}(T)\frac{V_{\mathrm{th}} - V_{\mathrm{FB}}}{\Delta V_{\mathrm{G}}}t_{\mathrm{r}}\right) \tag{3.5}$$

$$E_{\mathrm{em,e}} = E_{\mathrm{i}}(T) + k_{\mathrm{B}}T\ln\left(v_{\mathrm{th}}(T)\sigma_{\mathrm{n}}n_{\mathrm{i}}(T)\frac{V_{\mathrm{th}} - V_{\mathrm{FB}}}{\Delta V_{\mathrm{G}}}t_{\mathrm{f}}\right) \tag{3.6}$$

with

$E_{\mathrm{em,h}}$ / $E_{\mathrm{em,e}}$	boundary in the lower / upper half of the bandgap
E_{i}	intrinsic Fermi level
t_{r} / t_{f}	pulse rise / fall time
ΔV_{G}	pulse amplitude
v_{th}	thermal drift velocity
σ_{p} / σ_{n}	capture cross section for holes / electrons
n_{i}	intrinsic carrier concentration.

For the calculation of I_{CP}, it has to be considered that dependent on the chosen V_{GL} and V_{GH} only a particular fraction of the channel is probed during a gate pulse as shown in Figure 3.6 with two pulses (a) and (b) [112]. Due to the lateral doping profile along the channel (regions near source and drain are typically lightly doped) the local V_{th} and V_{FB} differ along the channel. The requirement for driving one particular lateral position from accumulation to inversion is met if $V_{\mathrm{GL}} < V_{\mathrm{FB}}$ and $V_{\mathrm{GH}} > V_{\mathrm{th}}$ at this position. Pulse (a) meets this requirement only for the lightly doped regions near the source and the drain but not for the central region because $V_{\mathrm{GH}} < V_{\mathrm{th}}$. Summing up the length of the regions, which contribute to I_{CP} for pulse (a) results in the effective length $L_{\mathrm{eff,a}}$. By contrast, pulse (b) meets the requirement for a broader lateral range, including the central region of the channel, resulting in an effective length $L_{\mathrm{eff,b}}$. In this regard, the effective area,

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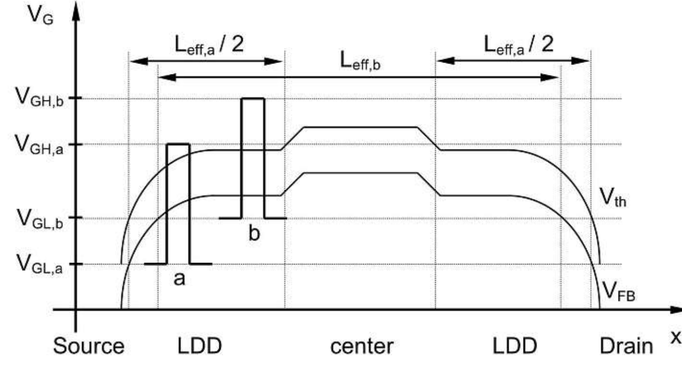

Figure 3.6.: Effective channel length: Due to lateral doping profile the local V_{th} and V_{FB} differs along the channel. Depending on V_{GL} and V_{GH} different channel areas contribute to I_{CP}. For pulse (a) only for the lightly doped regions near the source and the drain contribute to I_{CP}. Therefore the effective length is $L_{\mathrm{eff,a}}$. For pulse (b) a broader region, including the central region of the channel, contributes to I_{CP}. Therefore the effective length is $L_{\mathrm{eff,b}}$. Figure source: [112].

which corresponds to the fraction of the channel probed during the gate pulse, can be calculated according to

$$A_{\mathrm{G,eff}}(V_{\mathrm{GL}}, V_{\mathrm{GH}}) = W \cdot L_{\mathrm{eff}}(V_{\mathrm{GL}}, V_{\mathrm{GH}}) \tag{3.7}$$

with

$A_{\mathrm{G,eff}}$	active channel area
L_{eff}	effective channel length
W	gate width.

Finally, the charge pumping current can be written as [110, 112]

$$I_{\mathrm{CP}} = Wfq \int_0^{L_{\mathrm{eff}}(V_{\mathrm{GL}},V_{\mathrm{GH}})} \mathrm{d}x \int_{E_{\mathrm{em,h}}}^{E_{\mathrm{em,e}}} \mathrm{d}E D_{\mathrm{it}}(E,x) \tag{3.8}$$

with

f	pulse frequency
q	electron charge
W	gate width
$E_{\mathrm{em,h}}$ / $E_{\mathrm{em,e}}$	boundary in the lower / upper half of the bandgap
D_{it}	interface-state density.

The measurable I_{CP} depends on the active energy interval, which is affected by experimental parameters like t_{r} and t_{f} of the pulse, the ΔV_{G} as well as T. This allows

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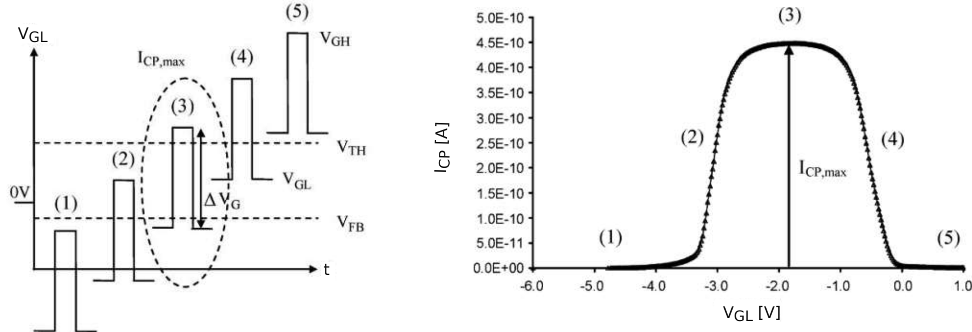

Figure 3.7.: Constant amplitude CP method: V_{GL} is swept through a broad voltage range from $V_{\mathrm{GL}} < V_{\mathrm{FB}}$ to $V_{\mathrm{GL}} > V_{\mathrm{th}}$ while t_{r}, t_{f} and ΔV_{G} are constant as shown on the left hand side. $I_{\mathrm{CP}}(V_{\mathrm{GL}})$ shown on the right hand side increases with increasing V_{GL} as long as $V_{\mathrm{GL}} < V_{\mathrm{FB}}$, is at its maximum when both $V_{\mathrm{GL}} < V_{\mathrm{FB}}$ and $V_{\mathrm{GH}} > V_{\mathrm{th}}$ are fulfilled, and finally decreases with further increase of V_{GL} when only $V_{\mathrm{GL}} > V_{\mathrm{FB}}$ is satisfied. Figure source: [112].

for an energetic profiling by modification of the experimental parameters. Moreover, due to the fact that V_{th} and V_{FB} depend on the lateral position in the MOSFET, the spatial distribution of interface defects can also be analyzed. As a result, different CP techniques have been proposed [112].

For example, the constant amplitude CP technique uses a variable V_{GL} and constant t_{r}, t_{f} and ΔV_{G} as shown in Figure 3.7. V_{GL} is swept through a broad voltage range from $V_{\mathrm{GL}} < V_{\mathrm{FB}}$ to $V_{\mathrm{GL}} > V_{\mathrm{th}}$. This leads to an $I_{\mathrm{CP}}(V_{\mathrm{GL}})$ which shows first an increasing behavior with increasing V_{GL} as long as $V_{\mathrm{GL}} < V_{\mathrm{FB}}$. Then the charge pumping current reaches its maximum when both $V_{\mathrm{GL}} < V_{\mathrm{FB}}$ and $V_{\mathrm{GH}} > V_{\mathrm{th}}$ are fulfilled. Finally I_{CP} decreases with further increase of V_{GL} when only $V_{\mathrm{GL}} > V_{\mathrm{FB}}$ is satisfied. In this technique, the active energy interval remains constant but in fact, different channel areas contribute to I_{CP}, depending on V_{GL} and ΔV_{G} as shown in Figure 3.6 schematically. Although it seems quite advantageous to distinguish between contributions of central interface defects and defects in the lightly doped regions based on the $I_{\mathrm{CP}}(V_{\mathrm{GL}})$ shape, such a characterization technique remains qualitative because the particular effective channel area ($A_{\mathrm{G,eff}}$) contributing to I_{CP} at each V_{GL} is unknown.

By contrast, V_{GL} remains at a fixed value for the whole measurement satisfying $V_{\mathrm{GL}} < V_{\mathrm{FB}}$ while V_{GH} is swept through a broad voltage range. As a consequence, $A_{\mathrm{G,eff}}$ is a function of V_{GH} only, which leads to a probing of the channel from outside to inside in a symmetrical way if V_{GH} is swept from $V_{\mathrm{GH}} < V_{\mathrm{FB}}$ to $V_{\mathrm{GH}} > V_{\mathrm{th}}$. In order to distinguish between local and energetic information, the active energy interval defined by the energy boundaries given in the Equations 3.5 and 3.6 has to be fixed. This is realized by adapting t_{r} and t_{f} after every V_{GH} step as a compensation of the increasing ΔV_{G}. Pure energetic profiling is enabled if V_{GL} and V_{GH} are fixed at $V_{\mathrm{GL}} \ll V_{\mathrm{FB}}$ and $V_{\mathrm{GH}} \gg V_{\mathrm{th}}$, respectively, and either t_{r} or t_{f} are changed. Furthermore, by variation of T the active energy interval can be broadened or narrowed.

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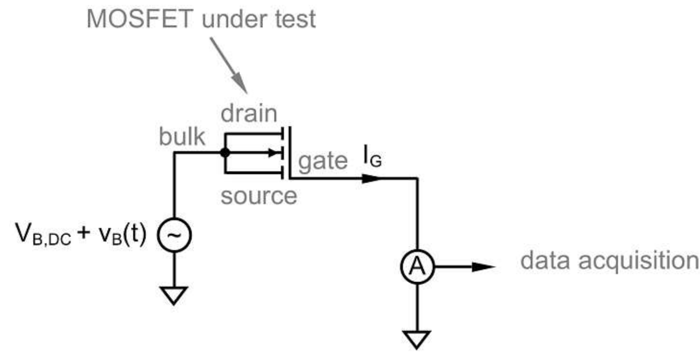

Figure 3.8.: Experimental setup for C-V profiling: At the bulk contact an AC signal with a DC offset is applied and the phase-shifted I_G is measured.

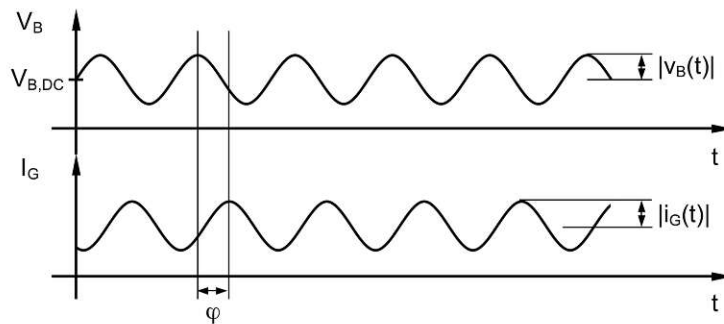

Figure 3.9.: C-V measurement procedure: The DC offset $V_{B,DC}$ drives the MOSFET from accumulation to inversion. The AC component with the amplitude $|v_B(t)|$ induces a phase-shifted gate current $i_G(t)$, which contains the information of the defects which capture and emit charge carriers at a certain energy level.

Both, energetic and position profiling of defects at the interface, typically realized with standard equipment, has made the CP method a widely used characterization technique. It gives a deep insight into degradation mechanisms associated with an increase of interface defects, typically HCD.

3.3. Capacitance-Voltage Profiling (C-V)

In addition to the CP method, the C-V method allows for an energetic profiling of defects as well. The C-V technique was introduced in 1960 in order to determine the majority carrier concentration in semiconductors [113]. Meanwhile, this method is also used for tracking the V_{th} and V_{FB} shifts in MOSFETs due to previously applied stress [114, 115]. As shown schematically in Figure 3.8, the basic experimental setup can be realized by the application of a bulk voltage (V_B) at the drain, bulk and source contacts

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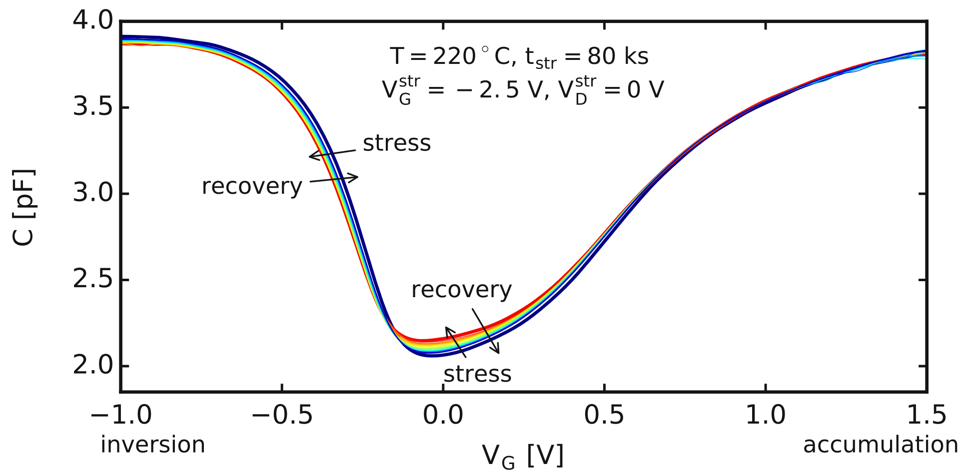

Figure 3.10.: C-V curves for a pMOSFET: The shape of the C-V curves in Figure 3.10 changes during stress and recovery. From these changes the information about the defects at different energy levels contributing to degradation and recovery as well as about V_{th} and V_{FB} can be extracted.

and a simultaneous measurement of the I_{G}. The applied V_{B} signal is a superposition of a DC offset, which drives the MOSFET from accumulation to inversion, and a small AC component with an amplitude typically around 50 mV. Due to the gate capacitance (C), the simultaneously measured I_{G} is phase-shifted as illustrated in Figure 3.9. Using an equivalent circuit diagram C can be calculated from the V_{B} and I_{G} signals.

Typical curves of C with respect to the DC offset of V_{G} are shown in Figure 3.10. When sweeping the DC component from accumulation to inversion, a depletion layer near the substrate/oxide interface forms because the majority carriers are forced away into the substrate. The remaining fixed ionized acceptors or donors build up a depletion charge and reduce the total gate capacitance. As soon as the minority carriers at the interface exceed the majority carriers and an inversion layer is created, the gate capacitance increases again. From the change of the C-V shape in Figure 3.10 during stress and recovery phases, the different energy levels contributing to degradation and recovery as well as V_{th} and V_{FB} can be extracted. This allows for a thorough characterization of degradation mechanisms like BTI and HCD.

3.4. Measure-Stress-Measure (MSM)

One widely used method for the experimental characterization of device degradation is the MSM technique. This method comprises basically of the following phases (also shown in Figure 3.11):

1. Measure: The virgin device is characterized.

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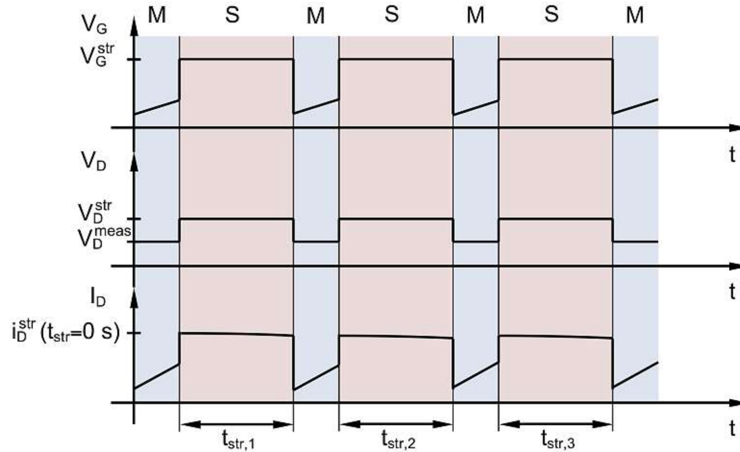

Figure 3.11.: MSM sequence: The applied gate and drain voltages (S) are interrupted periodically in order to characterize the degradation state of the device, e.g., by taking an I_D-V_G curve (M). The monitored parameter, e.g., V_th is extracted and the degradation over time is obtained. The overall stress time is obtained as $t_\mathrm{str} = \sum_i t_{\mathrm{str},i}$.

2. Stress: The device is subjected to a stress bias, which is typically much higher than the nominal operating conditions.

3. Measure: The stressed device is characterized.

4. The cycle comprising of the second and third phase can be repeated with either constant or increasing $t_{\mathrm{str},i}$.

The second phase does not necessarily have to be a stress phase, it could also be a recovery phase. The main difference between stress and recovery is the applied voltages. While stress is associated with biases typically much higher than the nominal operating conditions, recovery is associated with either no bias applied or biases around V_th. The characterization of the stressed device in the first and third phase can be realized by either taking an I_D-V_G curve (e.g., in order to obtain ΔV_th or $\Delta I_\mathrm{D,lin}$) or by applying one of the previously mentioned measurement methods, the CP method (e.g., in order to obtain the HCD induced interface state creation) or the C-V method. Consequently, the experimental setup has to be chosen according to the measurement method.

Especially for ΔV_th measurements, it has been found that MSM is quite disadvantageous. As discussed in Section 2.1, degradation comprises of a permanent and a recoverable component. Because of the recoverable component, ΔV_th recovers as soon as the stress is removed or as soon as the bias is switched to a lower voltage. Therefore, the overall device degradation state will be different when obtained by interruptions of stress than if the stress bias is applied continuously. Moreover, the MSM method cannot capture short-term effects of ΔV_th degradation and recovery (discussed in Subsection 2.1.1). The interruptions of the applied voltages, although as short as possible, can take 50 ms

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or more. Therefore, the degradation or recovery state of the device is distorted because the interruption of the applied voltages might reverse the impact especially of short-term effects on device characteristics. Therefore, the MSM method often cannot capture this impact, which makes reliable short-term measurements ($t_{str} < 1$ s or $t_{rec} < 1$ s) impossible.

In order to overcome these disadvantages, two innovative and fast measurement methods have been introduced, which can obtain ΔV_{th} without any interruptions of stress or recovery. These two methods are summarized in the following section as eMSM methods.

3.5. Extended Measure-Stress-Measure (eMSM)

The eMSM method consists of single point measurements of either I_D (corresponds to the constant voltage (cv) method in this thesis) or V_G (corresponds to the constant current (cc) method in this thesis) at a point near V_{th} during the recovery phase and a subsequent ΔV_{th} extraction. The basic measure-stress-measure sequence of this method is quite similar to the sequences discussed in the previous section. The main differences are that the measure phase refers to a recovery phase where I_D or V_G is measured and that neither stress nor recovery is interrupted. Both measurement methods are discussed and compared in the following.

The cv method and and the cc method have been introduced in the literature as the fast-I_D method and the fast-V_{th} method, respectively [31, 39, 40, 116]. The extraction of ΔV_{th} for both methods is shown in Figure 3.12.

- The cv method: ΔV_{th} is measured by recording I_D at a constant voltage, typically near V_{th} and subsequently converting I_D to ΔV_{th} using the initial I_D-V_G [31, 116].
- The cc method: ΔV_{th} is monitored by recording V_G, which is controlled by a feedback loop of an operational amplifier to achieve a constant drain current, typically near the threshold current [39].

The eMSM technique allows for a more extensive analysis of ΔV_{th} compared to other techniques. First, eMSM allows for short-term measurements ($t_{rec} < 1$ s after the recovery phase is triggered) because the recovery is measured without any distortions of the degradation or recovery state which is in contrast to the MSM method (discussed in the previous section and in Subsection 2.1.2). Furthermore, due to the fact that no bias modulation is applied during the stress phase which is the case if the OTF technique is used, no systematic error is introduced by periodic changes of the gate bias. Moreover, considering a statistical error of ± 1 mV in ΔV_{th}, the relative accuracy in the measured I_D needs to be 10^{-3} in the eMSM technique, which is achievable with reasonable integration times. Furthermore, this technique is insensitive to mobility changes induced by stress in contrast to the OTF technique [108]. Finally, the information about the recovery evolution of the MOSFET in eMSM measurements allows for the observation of both, the recoverable and the permanent component of the ΔV_{th} degradation [71]. In the context of ΔV_{th} measurements, these facts make the eMSM technique advantegeous.

Both extraction methods, the cv and the cc method, have been developed mainly for BTI measurements and provided equivalent results for NBTI stress. However, recent

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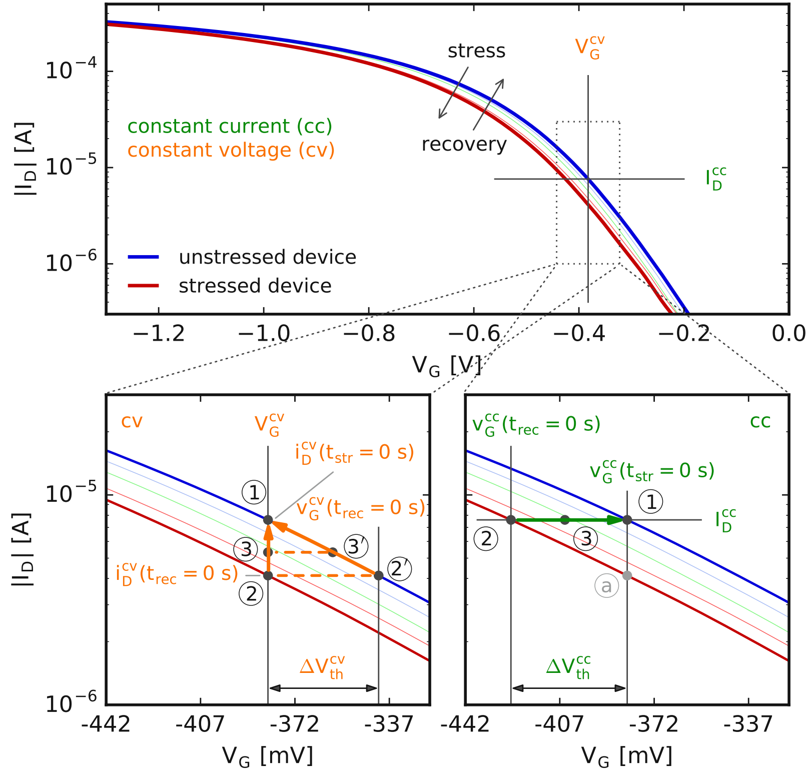

Figure 3.12.: Two different methods to extract the threshold voltage shift during recovery: The cv and cc methods. **Top:** Characteristics of an unstressed device (blue) and of a device after degradation (red). During the measure phase the parameters and thus the shape of the I_D-V_G characteristics drift towards their initial values. **Bottom:** ΔV_th is monitored using either the cv method (orange) by recording $i_\mathrm{D}^\mathrm{cv}(t)$ at a constant voltage near V_th and mapping to ΔV_th using the initial I_D-V_G or the cc method (green) by recording $v_\mathrm{G}^\mathrm{cc}(t)$ at a constant current near the threshold current.

recovery measurements recorded after mixed NBTI/HC stress have shown that ΔV_th extracted from the cv method and from the cc method can differ significantly. These deviations might lead to inconsistent model parameters and lifetime predictions. Therefore, in this section, the difference between both measurement methods is thoroughly analyzed and discussed considering the shifts of MOSFET parameters like $g_\mathrm{m,max}$, $I_\mathrm{D,lin}$, $I_\mathrm{D,sat}$ and SS.

3.5.1. Constant Voltage (cv) Method

The basic experimental setup which has been introduced for TDDS measurements in 2010 [40, 16, 33] is shown in Figure 3.13. The voltages applied to the gate and drain contacts are provided by constant voltage sources while I_D is measured simultaneously by a transimpedance amplifier. The feedback resistor of the transimpedance amplifier

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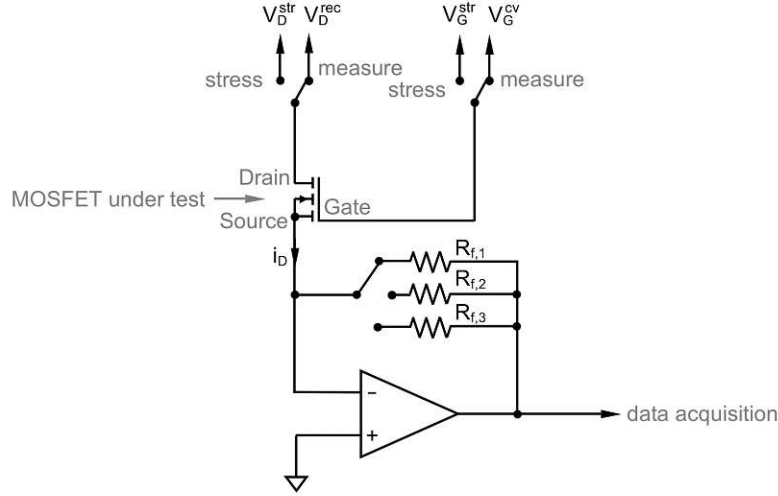

Figure 3.13.: Experimental setup for the cv method: The voltages applied to the gate and drain contacts are realized as constant voltage sources. I_D is measured using a transimpedance amplifier, where the feedback resistors $R_\mathrm{f,n}$ define the measurement range.

$R_\mathrm{f,n}$ defines the measurement range for I_D. The evolution of V_G, V_D and I_D over time for all three phases is shown in the measurement procedure in Figure 3.14.

The V_th extraction for the cv method is illustrated in the left bottom panel of Figure 3.12. During the first measure phase an initial I_D-V_G characteristics within a narrow gate bias window around the V_G^cv is measured at $V_\mathrm{D}^\mathrm{rec}$ (typically $-0.1\,\mathrm{V}$ in the measurements performed for this thesis) in order to characterize the unstressed device. The corresponding drain current is labeled with ① in the left bottom panel of Figure 3.12:

$$i_\mathrm{D}^\mathrm{cv}(V_\mathrm{G}^\mathrm{cv}, V_\mathrm{D}^\mathrm{rec}) = i_\mathrm{D}^\mathrm{cv}(t_\mathrm{str} = 0\,\mathrm{s}).$$

Thereafter, the device is subjected to a stress bias ($V_\mathrm{G}^\mathrm{str}$ and $V_\mathrm{D}^\mathrm{str}$) for the time t_str and immediately afterwards to recovery bias (V_G^cv and $V_\mathrm{D}^\mathrm{rec}$) for the time t_rec. As a result of the degradation of I_D during stress, directly after stress release the I_D-V_G characteristics are shifted and the drain current is reduced to ②:

$$i_\mathrm{D}^\mathrm{cv}(V_\mathrm{G}^\mathrm{cv}, V_\mathrm{D}^\mathrm{rec}) = i_\mathrm{D}^\mathrm{cv}(t_\mathrm{rec} = 0\,\mathrm{s}).$$

While subjecting the device to recovery conditions, I_D recovers from its reduced value towards its initial value and is monitored simultaneously. In a postprocessing step, each measured value of i_D^cv is transformed to a voltage v_G^cv, which corresponds to the gate voltage at i_D^cv on the initial I_D-V_G characteristics (② → ②', ③ → ③', ...). Finally, the threshold voltage shift can be calculated as

$$\Delta V_\mathrm{th}^\mathrm{cv}(t_\mathrm{rec}) = V_\mathrm{G}^\mathrm{cv} - v_\mathrm{G}^\mathrm{cv}(t_\mathrm{rec}).$$

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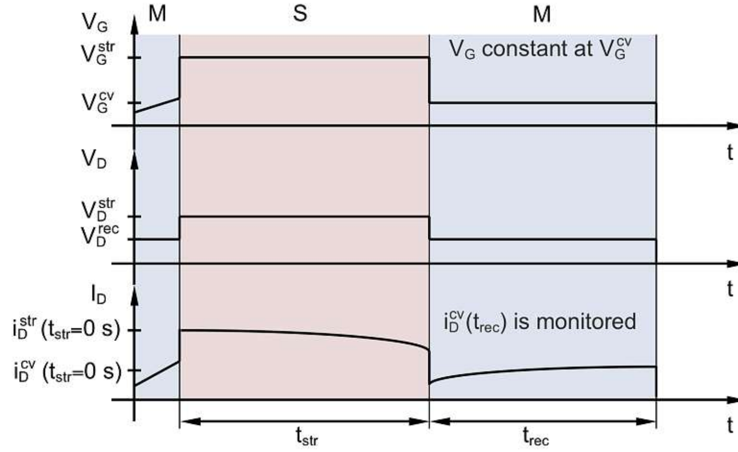

Figure 3.14.: Measurement procedure for the cv method: After the initial characterization of the unstressed device, V_G^{str} and V_D^{str} are applied. During t_{str} I_D degrades. Afterwards, the measurement voltages V_G^{cv} and V_D^{rec} are applied and I_D recovers. During the last phase, i_D^{cv} is recorded in order to extract ΔV_{th}.

3.5.2. Constant Current (cc) Method

Obtaining ΔV_{th} from the cc method requires a measurement setup as shown in Figure 3.15 [39]. Similar to the cv method, the gate and drain voltages during the stress phase as well as the drain voltage during the recovery phase are provided by constant voltage sources. In contrast to the cv method, in the cc method the drain current during the recovery phase is controlled by a feedback loop of an operational amplifier in order to achieve a constant value, typically near the threshold current. The evolution of V_G, V_D and I_D over time for this case is shown in the measurement procedure in Figure 3.16.

ΔV_{th} obtained using the cc method does not require a transformation since ΔV_{th} can be calculated directly as shown in the right bottom panel of Figure 3.12. First, the gate voltage labeled with ① which corresponds to the measurement current I_D^{cc} is obtained by recording v_G^{cc} for a short duration at recovery conditions (drain current is held at I_D^{cc} at V_D^{rec}):

$$v_G^{cc}(I_D^{cc}, V_D^{rec}) = v_G^{cc}(t_{str} = 0\,\mathrm{s}).$$

Then, the device is subjected to a stress bias (V_G^{str} and V_D^{str}) for the time t_{str} and subsequently to the recovery bias V_D^{rec} while the drain current is held at I_D^{cc} for the time t_{rec}. The consequence of the I_D-V_G characteristics shift due to the device degradation during stress is a reduced gate voltage ② directly after stress release:

$$v_G^{cc}(I_D^{cc}, V_D^{rec}) = v_G^{cc}(t_{rec} = 0\,\mathrm{s}).$$

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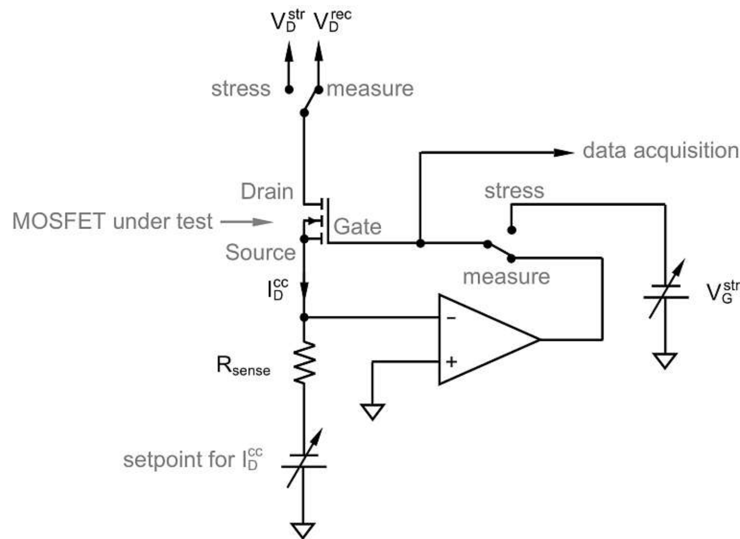

Figure 3.15.: Experimental setup for the cc method: The main difference to the cv method is that the drain current during the recovery phase is controlled by a feedback loop of an operational amplifier in order to achieve a constant value, typically near the threshold current.

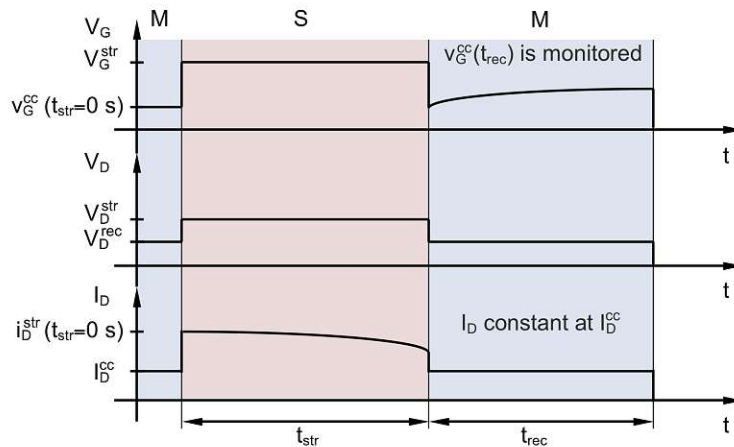

Figure 3.16.: Measurement procedure for the cc method: After the initial characterization of the unstressed device, V_G^{str} and V_D^{str} are applied. During t_{str} I_D degrades. Afterwards, the measurement voltage V_D^{rec} is applied while I_D is held at the constant value I_D^{cc}. During the last phase, v_G^{cc} recovers and is recorded in order to extract ΔV_{th}.

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During recovery, the gate voltage recovers towards its initial value and is monitored simultaneously. Finally, the threshold voltage shift can be calculated for all $v_{\mathrm{G}}^{\mathrm{cc}}$:

$$\Delta V_{\mathrm{th}}^{\mathrm{cc}}(t_{\mathrm{rec}}) = v_{\mathrm{G}}^{\mathrm{cc}}(t_{\mathrm{rec}}) - v_{\mathrm{G}}^{\mathrm{cc}}(t_{\mathrm{str}} = 0\,\mathrm{s}).$$

3.5.3. Comparison of V_{th} Extraction Methods

The cv method and the cc method can be considered equivalent only if the following requirements are met. The I_{D}-V_{G} characteristics shifts along the V_{G}-axis during stress and recovery and the shape (slope and curvature) of the curve section between ① and ②' in the left bottom panel of Figure 3.12 equals the shape of the curve section between ② and ⓐ in the right bottom panel. In other words, neither $g_{\mathrm{m,max}}$ nor SS change significantly during the experiment and the device-to-device variability is considered properly by setting each measurement point according to $v_{\mathrm{G}}^{\mathrm{cc}}(t_{\mathrm{str}} = 0\,\mathrm{s}) = V_{\mathrm{G}}^{\mathrm{cv}}$. In fact, all MOSFET parameters drift during stress and recovery differently, strongly depending on the stress conditions. As a result, the shapes of the unstressed and stressed I_{D}-V_{G} curves differ from each other, which leads to $\Delta V_{\mathrm{th}}^{\mathrm{cc}} \neq \Delta V_{\mathrm{th}}^{\mathrm{cv}}$ as it will be discussed in the next subsection.

For a comparison of the different threshold voltage extraction methods 21 large-area devices were measured. The measurements were performed at $T = 130\,°\mathrm{C}$ (controlled by a thermo chuck) using fabricated silicon wafers. Initially, I_{D}-V_{G} characteristics for the linear ($V_{\mathrm{D}} = -0.1\,\mathrm{V}$) and saturation ($V_{\mathrm{D}} = V_{\mathrm{DD}}$) regime were taken. Considering the I_{D}-V_{G} in the linear regime, $V_{\mathrm{th,0}}$ was extracted as the gate bias where the extrapolation of the I_{D}-V_{G} slope at its maximum transconductance intercepts the x-axis (extrapolation in the linear region method in [2]). This results in $V_{\mathrm{th,0}} = (-465 \pm 10)\,\mathrm{mV}$. During the subsequent stress/recovery measurements, each of the 21 devices was subjected to one combination of gate and drain stress voltage ($V_{\mathrm{G}}^{\mathrm{str}}$ is -1.5, -2 and $-2.5\,\mathrm{V}$, $V_{\mathrm{D}}^{\mathrm{str}}$ is 0, -0.5, -1, -1.5, -2, -2.5 and $-2.8\,\mathrm{V}$) for a stress time $t_{\mathrm{str}} = 1.1\,\mathrm{ks}$ and subsequently ΔV_{th} is measured for a recovery time $t_{\mathrm{rec}} = 3\,\mathrm{ks}$. Immediately afterwards, I_{D}-V_{G} characteristics for the linear region and in the saturation regime are measured in order to compare the characteristics of the tested and the virgin devices. Doing so, the maximum transconductance shift ($\Delta g_{\mathrm{m,max}}$), $\Delta I_{\mathrm{D,lin}}$, the saturation drain current shift ($\Delta I_{\mathrm{D,sat}}$) and the sub-threshold swing shift (ΔSS) are extracted for each device. Furthermore, $\Delta V_{\mathrm{th}}^{\mathrm{cv}}$ and $\Delta V_{\mathrm{th}}^{\mathrm{cc}}$ was extracted from the I_{D}-V_{G} characteristics of the degraded devices and the unstressed devices in two different regions near $V_{\mathrm{th,0}}$ of the initial curve: the subthreshold region, abbreviated with sub in the following, and a region above the threshold voltage. Two cases are distinguished, both illustrated in Figure 3.17: with and without device variability.

In the first case, the recovery conditions are chosen in equidistant intervals to $V_{\mathrm{th,0}}$ for each device (top panel in Figure 3.17). This means that $V_{\mathrm{G}}^{\mathrm{cv}}$ or $I_{\mathrm{D}}^{\mathrm{cc}}$ has to be set individually, depending on $V_{\mathrm{th,0}}$. In the shown measurements, recovery conditions were defined as $V_{\mathrm{G}}^{\mathrm{cv}} = V_{\mathrm{th0}} + 35\,\mathrm{mV}$ or $I_{\mathrm{D}}^{\mathrm{cc}} = I_{\mathrm{D}}(V_{\mathrm{th0}} + 35\,\mathrm{mV})$ for the subthreshold region and $V_{\mathrm{G}}^{\mathrm{cv}} = V_{\mathrm{th0}} - 130\,\mathrm{mV}$ or $I_{\mathrm{D}}^{\mathrm{cc}} = I_{\mathrm{D}}(V_{\mathrm{th0}} - 130\,\mathrm{mV})$ for the region above $V_{\mathrm{th,0}}$, both at $V_{\mathrm{D}}^{\mathrm{rec}}$.

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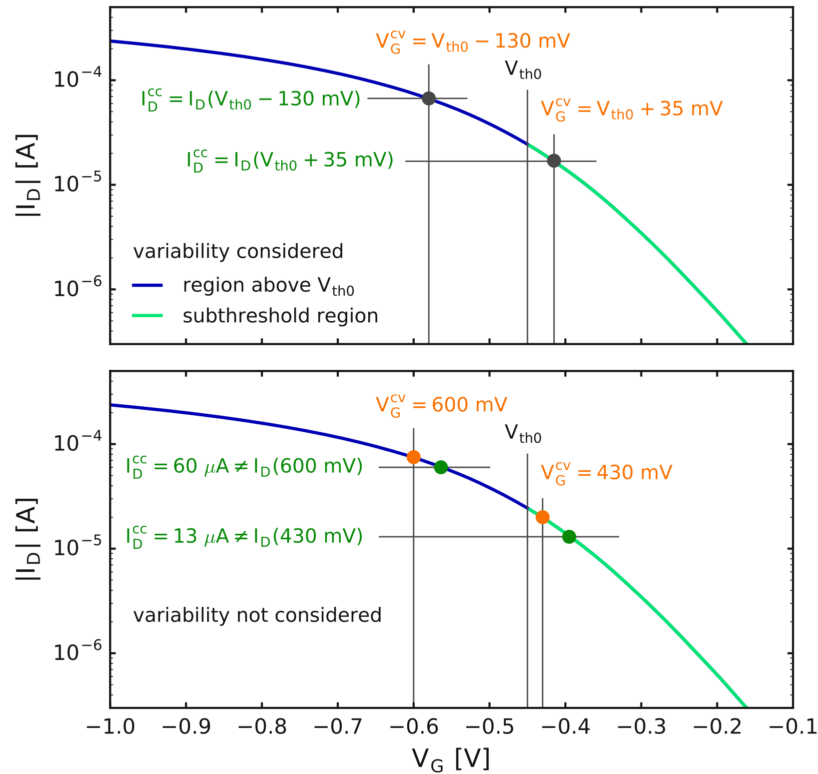

Figure 3.17.: Difference between considered device variability and not considered device variability: Top: Variability is considered as the recovery conditions are chosen in equidistant intervalls to $V_{\text{th},0}$ for each device individually. This ensures that the measurement current for the cc method corresponds always to the measurement voltage in the cv method indicated by the black markers. **Bottom:** Variability is not considered as the recovery conditions are fixed for every device so that in average $I_{\text{D}}^{\text{cc}} = I_{\text{D}}(V_{\text{G}}^{\text{cv}})$. For devices which deviate from the average characteristics the recovery conditions set in the cv method (indicated by the orange markers) differ from recovery conditions set in the cc method (indicated by the green markers), which leads to a significant difference of the extracted ΔV_{th}.

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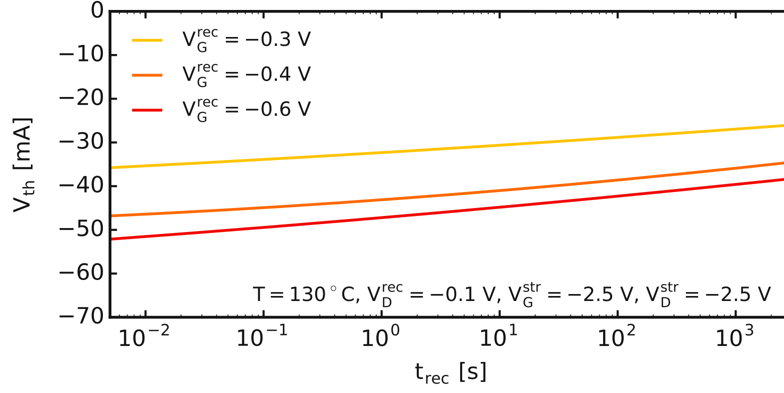

Figure 3.18.: Threshold voltage shift at different recovery conditions: The ΔV_{th} recovery trace differs for different recovery conditions.

This ensures that the measurement current in the cc method corresponds always to the measurement voltage in the cv method. In the second case, the recovery conditions are set to fixed values, independent from $V_{\text{th,0}}$, which is $V_{\text{G}}^{\text{cv}} = -0.43\,\text{V}$ or $I_{\text{D}}^{\text{cc}} = -13\,\mu\text{A}$ in the subthreshold region and $V_{\text{G}}^{\text{cv}} = -0.6\,\text{V}$ or $I_{\text{D}}^{\text{cc}} = -60\,\mu\text{A}$ in the region above $V_{\text{th,0}}$ in the measurements performed for this thesis. On average, the requirement $I_{\text{D}}^{\text{cc}} = I_{\text{D}}(V_{\text{G}}^{\text{cv}})$ is met but this does not hold true for every particular device as shown in Figure 3.17 bottom. If it holds true, strongly depends on the deviation of the individual I_{D}-V_{G} characteristics from the average.

At a first glance, it seems that the second case is easier to implement. The reason is that it requires only one analysis per device architecture and device dimensions prior to all experiments in order to determine an average I_{D}-V_{G} characteristics and define the recovery conditions. By contrast, the first case needs an I_{D}-V_{G} analysis per device prior to each experiment, which means much more effort for the experimentalist. However, the second case means that the recovery conditions differ for the cv and the cc method depending on the deviation of the individual I_{D}-V_{G} characteristics from the average. From Figure 3.18 it can be seen that different recovery conditions lead to different ΔV_{th} recovery traces. This introduces a difference between $\Delta V_{\text{th}}^{\text{cv}}$ and $\Delta V_{\text{th}}^{\text{cc}}$. The following results lead to a similar conclusion.

In Figure 3.19 the relative difference between ΔV_{th} extracted from the cv method and extrated from the cc method (δ) is calculated as

$$\delta = (\Delta V_{\text{th}}^{\text{cc}} - \Delta V_{\text{th}}^{\text{cv}})/\Delta V_{\text{th}}^{\text{cv}} \cdot 100$$

and is plotted against the relative degradation of $g_{\text{m,max}}$, $I_{\text{D,lin}}$, $I_{\text{D,sat}}$, and SS under consideration of the device variability. Each point in the scatter plot corresponds to the measurement of one particular device, which has been subjected to one particular ($V_{\text{G}}^{\text{str}}$,$V_{\text{D}}^{\text{str}}$) combination. Additionally, in order to analyze if the difference between both measurement methods correlates with the degradation of MOSFET parameters, the Pearson correlation coefficient as a measure for a linear correlation between δ and

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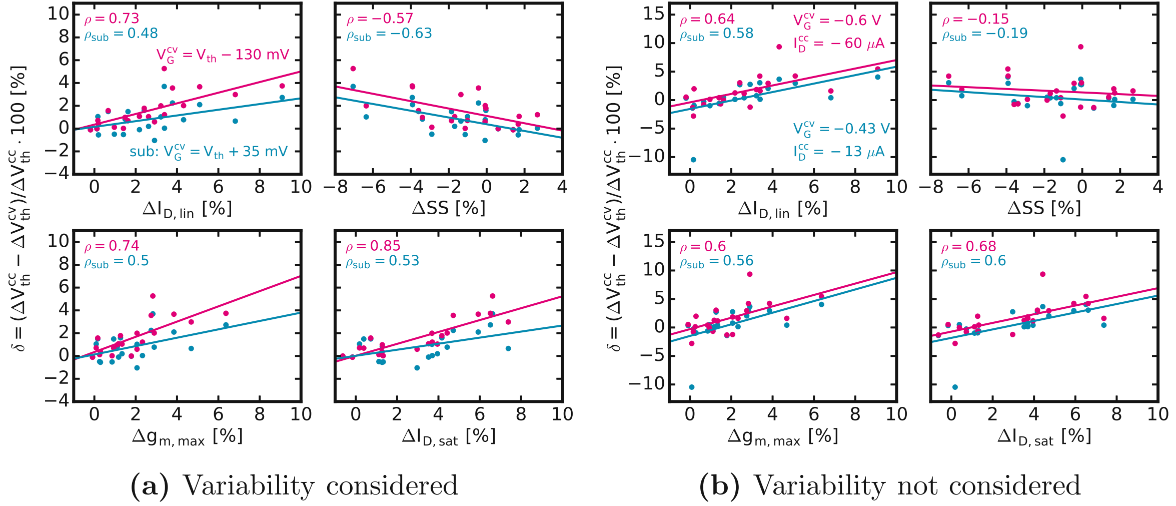

(a) Variability considered **(b)** Variability not considered

Figure 3.19.: Correlation of δ with the degradation of MOSFET parameters: Each point in the scatter plots corresponds to the degradation after subjecting the MOSFET to a particular $V_{\mathrm{G}}^{\mathrm{str}}$-$V_{\mathrm{D}}^{\mathrm{str}}$ combination. The relative difference δ increases with larger degradation and it is in average lower for the subthreshold region.

$\Delta g_{\mathrm{m,max}}$, $\Delta I_{\mathrm{D,lin}}$, $\Delta I_{\mathrm{D,sat}}$, and ΔSS is given for each region: ρ_{sub} for the subthreshold region and ρ for the region above $V_{\mathrm{th,0}}$. As can be seen, δ correlates differently with the relative change of the MOSFET parameters:

- δ increases with larger degradation of $g_{\mathrm{m,max}}$, $I_{\mathrm{D,lin}}$, $I_{\mathrm{D,sat}}$ and SS,
- on average, δ is lower for the subthreshold region,
- the maximum difference $\delta_{\mathrm{max}} < 6\,\%$,
- δ correlates strongly with ΔSS in the subthreshold region but weaker in the region above $V_{\mathrm{th,0}}$ and
- δ correlates strongly with $\Delta g_{\mathrm{m,max}}$, $\Delta I_{\mathrm{D,lin}}$, $\Delta I_{\mathrm{D,sat}}$ in the region above $V_{\mathrm{th,0}}$ but weaker in the subthreshold region.

The correlation between δ and ΔSS, $\Delta g_{\mathrm{m,max}}$, $\Delta I_{\mathrm{D,lin}}$, and $\Delta I_{\mathrm{D,sat}}$ is dominated by the impact of the MOSFET parameter shift on the change of the slope and the curvature of the I_{D}-V_{G} characteristics. While SS characterizes essentially the slope and the curvature in the subthreshold region, $\Delta g_{\mathrm{m,max}}$, $\Delta I_{\mathrm{D,lin}}$, and $\Delta I_{\mathrm{D,sat}}$ affect the slope and curvature at $V_{\mathrm{th,0}} - 130\,\mathrm{mV}$. Thus, a change of SS during stress and recovery affects mainly δ in the subthreshold region. However, the analysis shows that δ does not exceed $4\,\%$ if the measurement point is chosen in the subthreshold region.

If the variability of the MOSFETs is not considered and the measurement points are chosen at fixed values near the mean value of $V_{\mathrm{th,0}}$, the main observations change. Subfigure 3.19b shows the correlation between δ and ΔSS, $\Delta g_{\mathrm{m,max}}$, $\Delta I_{\mathrm{D,lin}}$, and $\Delta I_{\mathrm{D,sat}}$.

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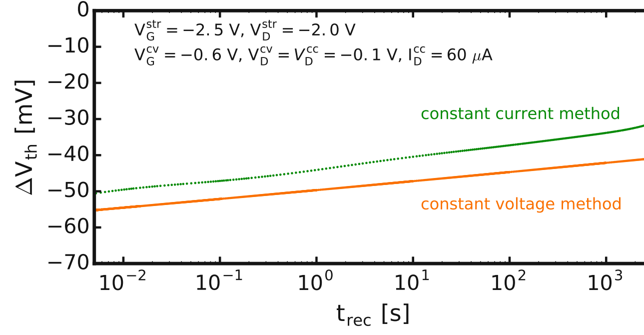

Figure 3.20.: Recovery traces of the threshold voltage shift monitored with the cv and cc method: Degradation caused by mixed NBTI/HC stress leads to different evolutions of ΔV_{th} recovery.

Some observations are comparable to the observations in Subfigure 3.19a: δ increases with larger degradation and δ is lower for the subthreshold region on average. However, the maximum difference $\delta_{max} > 10\,\%$, which interestingly occurs at low degradation, is higher, and the correlation with all parameters is weaker than if variability is considered. Due to the fact that $v_G^{cc}(t_{str} = 0\,s)$ does not necessarily equal V_G^{cv} the two sections measured with the cc method and the cv method can differ in slope and curvature even if the degradation is low.

Recorded ΔV_{th} recovery during the measure phase confirms these results. For low degradation of the parameters (ΔSS, $\Delta g_{m,max}$, $\Delta I_{D,lin}$, and $\Delta I_{D,sat}$ are less than $2\,\%$), the cc method and the cv method show quite comparable results. By stark contrast, degradation caused by mixtures of BTI and HCD or pure HCD, where the parameter degradation exceeds $4\,\%$, leads to completely different ΔV_{th} traces. Figure 3.20 shows two recovery traces where it can be seen that $\delta \approx -10\,\%$ at low t_{rec} but increases with t_{rec}, which indicates that the evolution of the slope and the curvature during the measure phase can differ significantly. For example, if $\Delta g_{m,max}$ does not recover but ΔV_{th} does recover, the shape of the I_D-V_G characteristics distorts during the measure phase. This is a realistic example since the transconductance is affected by scattering of channel carriers at charged interface states. The number of such interface states increases during stress and as a consequence, the transconductance reduces. As discussed in Chapter 2, interface state barely recover [22, 24, 93, 97, 117].

From this analysis, it cannot be concluded which of both techniques should be chosen for ΔV_{th} measurements. Nevertheless, the advantages and disadvantages of both measurement methods are discussed briefly. The constant voltage setup as used in [40, 16] measures the drain current with a transimpedance amplifier where the feedback resistor defines the measurement range for I_D during stress as well as during the measure phase. Due to the fact that I_D can vary between the stress and measure phase by a few orders of magnitude and in order to ensure a proper measurement resolution during the measurement, the feedback resistor has to be changed between stress and recovery. Thus, an additional delay on the order of ms is introduced and important information

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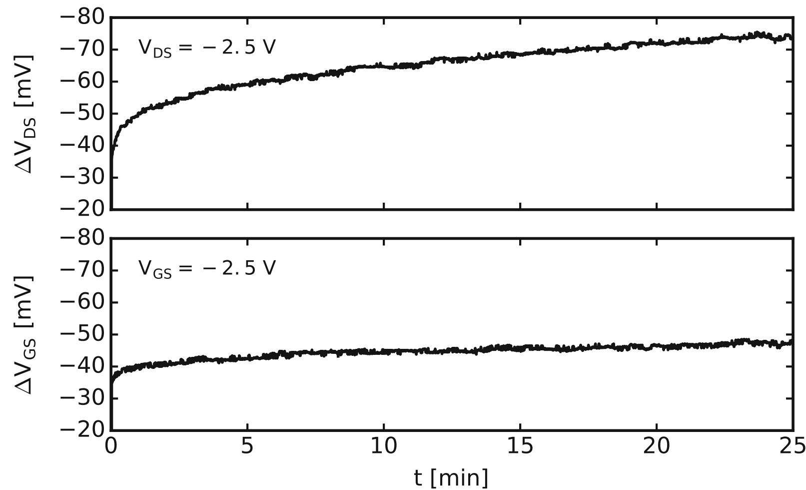

Figure 3.21.: Unstable stress voltages in the cc method: The applied voltages are not stable during stress as soon as $V_{\mathrm{D}}^{\mathrm{str}} \neq 0\,\mathrm{V}$. As soon as the device degrades its g_{m} reduces and the ratio between the drain-to-source voltage and the voltage over the serial resistance R_{sense} changes. Both, the voltage between the drain and the source contact (V_{DS}) and the voltage between the gate and the source contact (V_{GS}) drift slightly, which results in voltage differences ΔV_{DS} and ΔV_{GS} compared to the unstressed device.

regarding the evolution of ΔV_{th} during the first ms after stress is lost. By contrast, the cc setup as proposed in [39] minimizes the delay between the stress and measure phase because no feedback resistor has to be changed between both phases. As a consequence, the cc method is advantageous in the case that the degradation of the device cannot be estimated prior to the MSM measurement, which is a requirement for the proper choice of the feedback resistor in the constant voltage setup. However, the requirement that the stress voltage applied to the gate contact has to be constant in order to avoid changes of the degradation state of the device makes the cv method easier to implement (as also discussed in [107]), e.g., using standard equipment. The reason is that the MSM cycles can be realized with one voltage source. This is not the case for the cc method where a voltage source is required during stress and a current source is required during recovery.

Further measurements using both methods showed that δ can be even higher, up to 100 %. One error has not been taken into account so far. By taking a look at the measurement setup for the cc method in Figure 3.15 it becomes clear that in the case that $V_{\mathrm{D}}^{\mathrm{str}} \neq 0\,\mathrm{V}$ the stress conditions are not stable as shown in Figure 3.21. As soon as the device degrades, its g_{m} reduces and the ratio between the drain-to-source voltage and the voltage over the serial resistance R_{sense} changes. The consequence is that the stress conditions of the device drift slightly during t_{str}. It has already been discussed that changes of the stress conditions over t_{str} lead to a different degradation state compared to the state after stable stress conditions.

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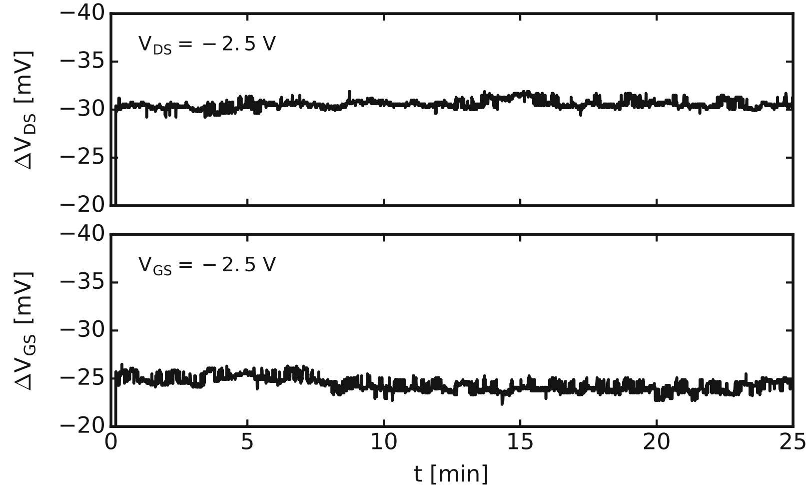

Figure 3.22.: Stable stress voltages with offset in the cv method: The constant offset in the voltage between the drain and the source contact (V_{DS}) and the voltage between the gate and the source contact (V_{GS}) means that the preset stress voltages do not correspond to the applied voltages.

As a comparison, Figure 3.22 illustrates that the setup for the cv method (see Figure 3.13) provides stable stress voltages. However, it has to be mentioned that the constant offset around 30 mV means that the set stress voltages do not correspond to the applied voltages. This offset introduces a systematic error for further modeling attempts. As shown in Figure 3.23 even slight deviations of the stress conditions, although stable, can make a difference for the ΔV_{th} recovery traces.

Both, the drift of the stress voltages using the cc method as well as the constant offset in the cv method, lead to a relative difference between $\Delta V_{\mathrm{th}}^{\mathrm{cv}}$ and $\Delta V_{\mathrm{th}}^{\mathrm{cc}}$ higher than obtained in Figure 3.19. Since a constant offset is easier to be considered for modeling attempts, the cv measurement method was applied for the results presented in the following chapters.

3.6. Random Telegraph Noise (RTN) Analysis

Due to the intensive down-scaling of MOSFETs, the gate area has reached dimensions in the nanometer regime where single capture and emission events of oxide defects are measurable. In this context, the observation of the so-called RTN became more likely. This phenomenon (shown in Subfigure 2.12b) has been known and modeled since the 1980s [16, 48, 62] and describes the discrete changes in the conductance of electronic devices generated by capture and emission of charge carriers by individual oxide defects. The capture and emission events can be measured as a change of ΔV_{th} with either the setup for the cv ΔV_{th} extraction shown in Figure 3.13 or the setup for the cc ΔV_{th} extraction shown in Figure 3.15.

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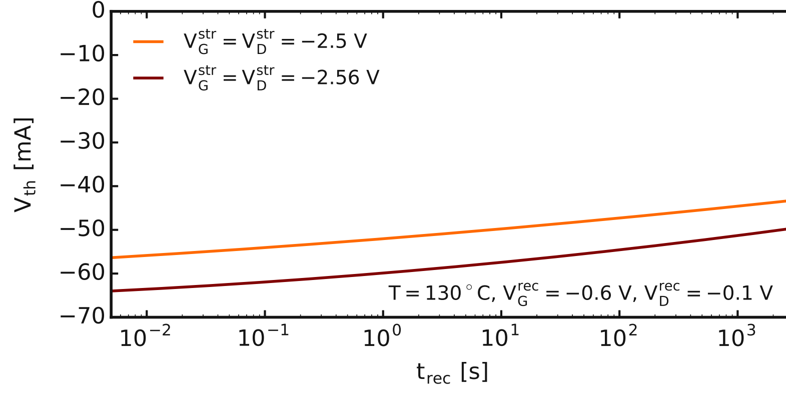

Figure 3.23.: Threshold voltage shift after different stress conditions: Even slight deviations of the stress conditions can make a difference in the ΔV_{th} recovery traces.

RTN analysis includes the characterization of the mean values of the characteristic τ_{e} and τ_{c} at different bias and temperature. Therefore, a ΔV_{th} trace is recorded using linear time steps. For a proper analysis, the trace has to contain at least ten capture and emission events to calculate a mean value of the characteristic times

$$\tau_{\mathrm{c}} = \frac{1}{N} \sum_{i=1}^{N} \tau_{\mathrm{c},i} \tag{3.9}$$

$$\tau_{\mathrm{e}} = \frac{1}{N} \sum_{i=1}^{N} \tau_{\mathrm{e},i} \tag{3.10}$$

with

$\tau_{\mathrm{c}}/\tau_{\mathrm{e}}$	mean capture/emission time
N	number of capture or emission events
$\tau_{\mathrm{c},i}/\tau_{\mathrm{e},i}$	individual capture/emission time of one event.

Using a step detection algorithm like the Canny algorithm [118] or a Hidden Markov Model, the discrete steps are located in time and $\tau_{\mathrm{e},i}$ as well as $\tau_{\mathrm{c},i}$ are extracted for each pair of emission and capture events i. As a result, the mean values $\tau_{\mathrm{e}}(V_{\mathrm{G}},T)$ and $\tau_{\mathrm{c}}(V_{\mathrm{G}},T)$ provide important information about the behavior of the defect which has caused the steps in ΔV_{th}.

The characterization of defects using the RTN analysis is only feasible for defects with rather similar capture and emission times, where $\tau_{\mathrm{e}} \approx \tau_{\mathrm{c}}$ is fulfilled. This limits the range of bias conditions drastically because of the properties of material defects in experiments as discussed in Subsection 2.1.3. Both, τ_{e} and τ_{c} change opposite to V_{G}. As a result,

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RTN analysis can be applied only within a narrow window around the gate bias of the intersection point of $\tau_e(V_G)$ and $\tau_c(V_G)$. For a full characterization using the NMP model as required for an extraction of the important parameters which describe the nature of the defect, the characteristic capture and emission times have to be measured over a broad V_G range.

As soon as V_G is not within the narrow window around the intersection point of $\tau_e(V_G)$ and $\tau_c(V_G)$, two cases can be distinguished, either $\tau_e \ll \tau_c$ or $\tau_e \gg \tau_c$. The first corresponds typically to the defect properties at recovery conditions, where V_G is near V_{th} and the second corresponds typically to the defect properties at stress conditions, both discussed in Subsection 2.1.3. This means that $\tau_c \in [t_{str,min}, t_{str,max}]$ and $\tau_e \in [t_{rec,min}, t_{rec,max}]$ can be obtained by a kind of eMSM method, which has been developed particularly for the extraction of defect characteristics in experiments, the TDDS framework.

3.7. Time-Dependent Defect Spectroscopy (TDDS)

The TDDS framework has been introduced recently with the main purpose to characterize single oxide defects in MOSFETs [40]. In general, both, the setup for the cv ΔV_{th} extraction shown in Figure 3.13 and the setup for the cc ΔV_{th} extraction shown in Figure 3.15 can be used as experimental setups. However, in the following, the focus is on the cv setup since this method is in the focus of this thesis. The measurement procedure corresponds basically to a sequencing of the stress and recovery phase of the eMSM technique after the initial characterization of the device (Figure 3.14) including several postprocessing steps:

1. Characterization of the unstressed device by taking an initial I_D-V_G.
2. Subjecting the device to a stress bias for t_{str}.
3. Monitoring I_D for t_{rec} providing its recovery behavior over many decades in time.
4. Repetition of the second and third phase, for example $N = 100$ times.
5. Mapping I_D to ΔV_{th} as explained in Figure 3.12.
6. Postprocessing of the data by extractin step heights and step times.

As already discussed in the introduction, the capture and emission events of defects affect device characteristics like V_{th}. As long as the energy level of the defect is located in a certain area in the band gap, it can be shifted above the Fermi level by applying a stress gate bias typically above nominal operating conditions and shifted below the Fermi level by applying a recovery gate bias typically around the threshold voltage. Depending on the detailed defect configuration the defect can capture and emit a charge carrier at stochastic times. Such charge exchange events between the oxide and the channel can be measured as stepwise shifts of ΔV_{th}. While the step heights cannot be resolved in large-area devices due to the small impact of one charge exchange event, they can be

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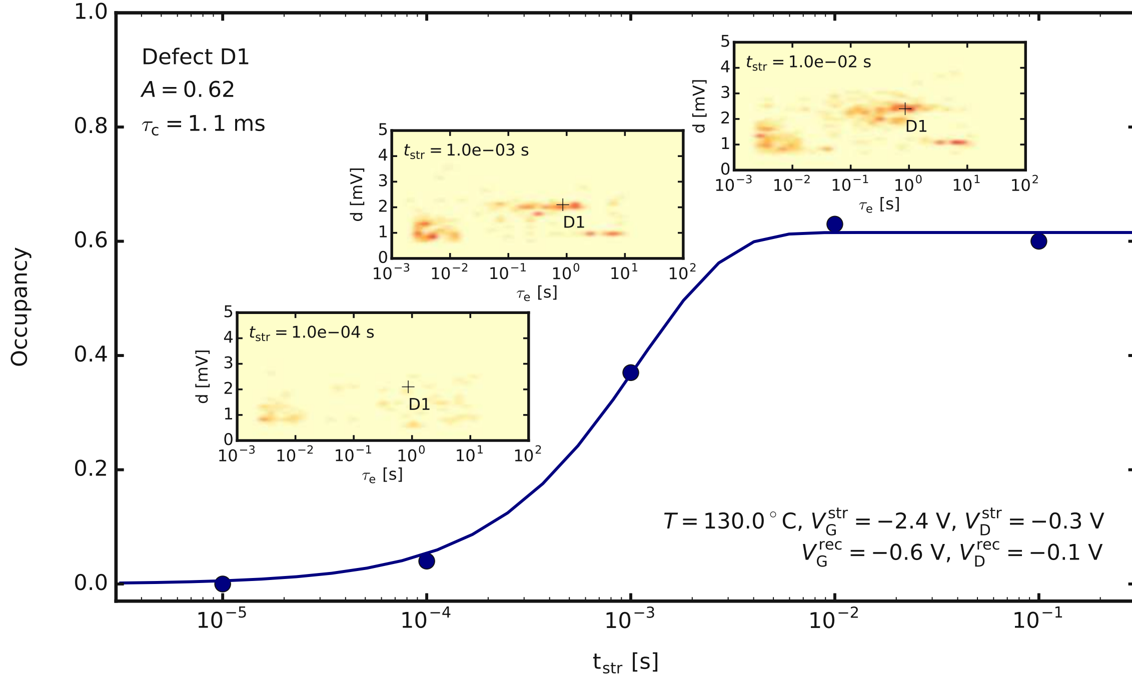

Figure 3.24.: Occupancy with respect to the stress time: With increasing stress time the occupancy of the defect D1 increases. As a consequence the number of emission events increases. The occupancy can be calculated for each stress time as the ratio between the number of emission events (N_e) and the number of recovery traces (N_t). By fitting the measurement points with an exponential function (Equation 3.11, τ_c can finally be extracted.

experimentally assessed in nano-scale devices containing only a handful of defects [17, 18].

Due to the fact that the capture and emission events are stochastic, TDDS requires a number, e.g., 100, of stress/recovery experiments to capture statistics for a reliable characterization. The top panel of Figure 2.7 shows typical recovery measurements containing the steps of five defects enumerated with 1, 2, 3, 4 and 12. These defects have each captured a charge carrier during the previous stress phase and emit this charge carrier during the recovery phase, which causes a step in the ΔV_{th} recovery trace. In a postprocessing step, d and τ_e are extracted for each step and can be binned into a two-dimensional histogram shown in the bottom panel Figure 2.7 bottom. As a result, a cluster for each defect forms in the spectral map, which is an unambiguous fingerprint of the defect. By assignment of each cluster to a certain defect, the mean values for d and τ_e can be calculated.

In contrast to τ_e, τ_c is measured indirectly. Two reasons can be mentioned in this regard. In BTI measurements no V_D^{str} is applied and thus I_D is nearly zero. Therefore, the charge exchange events cannot be measured in I_D. In mixed NBTI/HC stress measurements the charge exchange events cannot be measured, especially for high V_D^{str}. In

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addition, considering the number of charge carriers in the channel at stress conditions and the measurement range defined by the feedback resistor of the transimpedance amplifier the single steps cannot be resolved at stress. As a result, τ_c has to be extracted from the occupancy with respect to t_{str}, which is shown in Figure 3.24.

In Figure 3.24 τ_c of a defect named D1 is extracted. This is done by exploiting the stress time dependence of the occupancy. From this, the occupancy can be calculated as the ratio of the number of emission events (N_e) to the number of recovery traces (N_t). The occupancy N_e/N_t in respect to t_{str} follows an exponential function according to Equation 2.18:

$$\Delta f(V_G^{str}, V_D^{str}, t_{str}) = A(V_G^{str}, V_D^{str}) \left(1 - e^{-t_{str}/\tau_c(V_G^{str}, V_D^{str})}\right) \tag{3.11}$$

with

Δf	occupancy, experimentally characterized as the ratio between N_e and N_t
V_G^{str}	gate stress voltage
V_D^{str}	drain stress voltage
t_{str}	stress time
A	corresponds to $(f(V_G^{str}) - f(V_G^{rec}))\, e^{-t_{str}/\tau_e}$ in Equaton 2.18
τ_c	capture time.

By fitting the measurement points with this exponential function, τ_c can finally be extracted. The spectral maps illustrate that with increasing t_{str} the intensity of the cluster assigned to the defect named D1 increases as well.

One challenge of the TDDS, which has to be mentioned at this point is that defects with similar d and τ_e cannot be distinguished in the spectral map because they cause clusters at similar positions. Often, this challenges the full characterization of a defect because the defect characteristics have to be recorded for a wide range of stress and recovery bias conditions. Each change of the stress bias results in a shift of τ_e, τ_c and/or d. In devices with more than four experimentally feasible defect clusters in the spectral map it is quite likely that two defects cross their paths in the spectral map and thus cannot be distinguished. This limits the voltage range in which defects can be characterized fully. In most of the measurements, this leads to a pre-selection of defects.

However, the TDDS is one of the most reliable techniques in the context of single oxide defect characterization which has led to numerous conclusions as already discussed in Chapter 2. Although it has been developed for BTI measurements, it has been experienced that it is also reliable in mixed NBTI/HC measurements, presented in Chapter 5.

3.8. Temperature Accelerated Measurements

Typical capture and emission times of oxide defects vary by many orders of magnitude, from µs to weeks, depending on their properties, the temperature, and the bias

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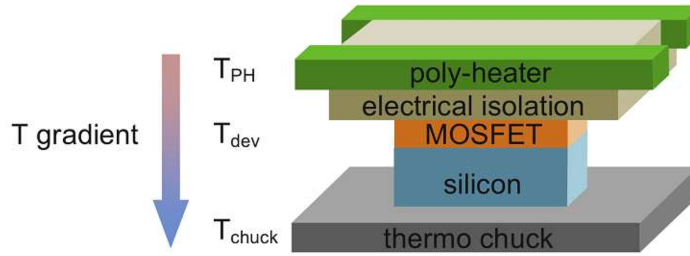

Figure 3.25.: Poly-heater-device system: Polycrystalline silicon wires (poly-heater) are processed near the MOSFET and are electrically isolated.

conditions applied to the MOSFET. However, especially in TDDS measurements the experimental window is limited due to the fact that each measurement contains, e.g., 100 stress/recovery cycles. In order to capture the characteristics of a defect with a characteristic emission time of one week, the measurement would take approximately two years for one gate and drain voltage combination. If it is taken into account that a thorough characterization of defects requires more than one measurement, such measurement durations are not feasible. However, defects with very large emission times are of special interest because they contribute among others to the permanent component of degradation, which is expected to dominate the device lifetime distribution. Therefore, their thorough characterization would be essential.

Not only defects with large emission times can be a challenge for the experimental characterization. Defects with emission times smaller than $t_{\mathrm{rec,min}}$ are a challenge as well. One possibility to overcome these challenges is to accelerate or to slow down the charge carrier exchange by changing the temperature during the stress and recovery phases in TDDS measurements independently. The impact of T on τ_{c} and τ_{e} is discussed in Subsection 2.1.3. In order to shift τ_{c} and τ_{e} lying outside experimentally feasible time slots, defined temperature ramps (one example is shown in Figure 3.27) can be applied during stress and/or recovery. For this purpose, an *in situ* heating technology for temperature accelerated measurements has been introduced recently [119, 120, 121].

Such temperature accelerated measurements can be based on local heaters realized as polycrystalline silicon wires (poly-heater). They are processed near the MOSFET and electrically isolated as shown in Figure 3.25. In contrast to the experimental setups for the ΔV_{th} extraction in eMSM measurements, the poly-heater-device system has two additional contacts for the application of a voltage to the poly-heater (see Figure 3.26). As long as no voltage V_{PH} is applied to the wires, the MOSFET and the poly-heater are held at a fixed device temperature (T_{dev}) and at a fixed poly-heater temperature (T_{PH}), respectively, both corresponding to the thermo chuck temperature (T_{chuck}): $T_{\mathrm{dev}} = T_{\mathrm{PH}} = T_{\mathrm{chuck}}$. When a voltage is applied to the wires resulting in a current flow through the poly-heater (I_{PH}), the dissociated heat corresponding to the power dissipated in the poly-heater (P_{PH}) elevates T_{PH} first. Immediately afterwards, a temperature gradient forms vertically across the device stack because $T_{\mathrm{chuck}} < T_{\mathrm{PH}}$. As a consequence, T_{dev} is elevated as well: $T_{\mathrm{chuck}} < T_{\mathrm{dev}} < T_{\mathrm{PH}}$.

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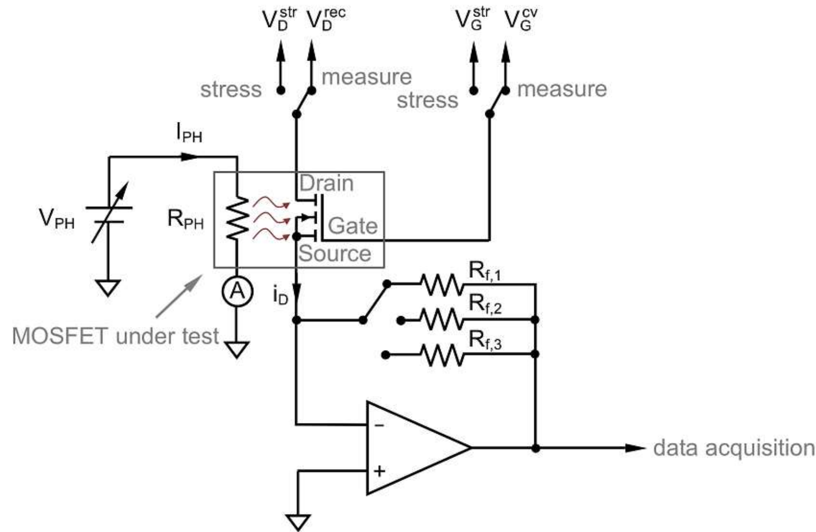

Figure 3.26.: Experimental setup for temperature accelerated measurements: The voltages applied to the gate and drain contacts are realized as constant voltage sources and I_{D} is measured using a transimpedance amplifier. The heating with the polyheater is realized with a constant voltage source V_{PH}. Simultaneously the poly-heater current I_{PH} is measured.

3.8.1. Poly-Heater Calibration

In order to assign the correct T_{dev} to P_{PH}, the system has to be calibrated prior to the measurements. The calibration procedure is shown schematically in Figure 3.28. The calibration consists of the following steps:

1. I_{D} is obtained at different $T_{\mathrm{chuck}} = T_{\mathrm{dev}}$ at $P_{\mathrm{PH}} = 0\,\mathrm{W}$ over a wide range of temperatures. It has to be considered that $I_{\mathrm{D}}(V_{\mathrm{G}},V_{\mathrm{D}})$ has to be chosen in such a way that no stress is introduced to the device, e.g., in the subthreshold region near V_{th}.

2. I_{D} is obtained at different P_{PH} at a fixed T_{chuck}, which corresponds to the temperature minimum (T_{min}) of the setup.

3. $I_{\mathrm{D}}(T_{\mathrm{chuck}})$ and $I_{\mathrm{D}}(P_{\mathrm{PH}})$ are fitted with a polynomial fit of first or second order.

4. With the coefficients of the fits, $T_{\mathrm{dev}}(P_{\mathrm{PH}})$ is interpolated for arbitrary poly-heater power at a certain T_{chuck}.

This calibration method can also be applied to obtain the temperature of the poly-heater $T_{\mathrm{PH}}(P_{\mathrm{PH}})$. In this context, the increase of the poly-heater resistance (R_{PH}) with T caused by the reduction of the carrier mobility of the polycrystalline silicon wires can be characterized. Therefore, $R_{\mathrm{PH}}(T_{\mathrm{chuck}})$ at $P_{\mathrm{PH}} = 0\,\mathrm{W}$ and $R_{\mathrm{PH}}(P_{\mathrm{PH}})$ at $T_{\mathrm{chuck}} = T_{\mathrm{min}}$ are measured and fitted with a polynomial fit of first or second order. With the fitted

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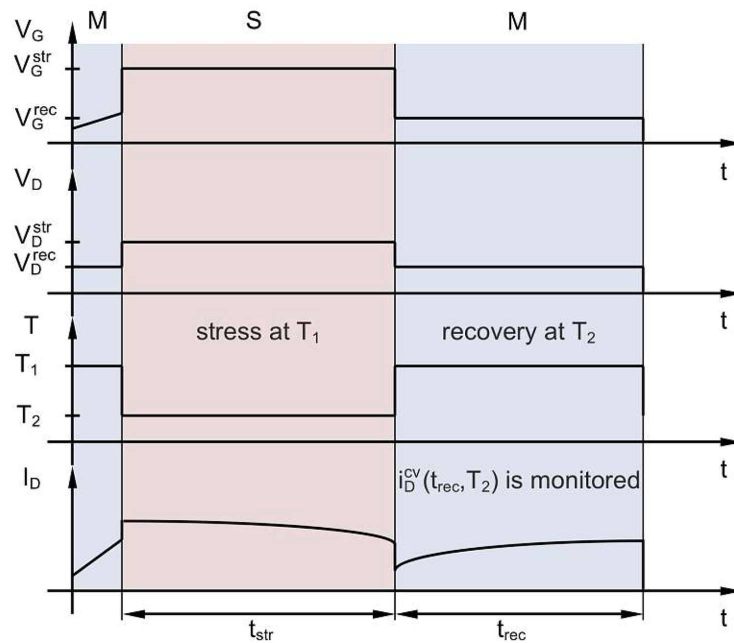

Figure 3.27.: Measurement procedure using a poly-heater: During an MSM sequence, the temperature can be elevated, e.g., during recovery. This would accelerate recovery, which allows for the characterization of effects typically lying outside the measurement window.

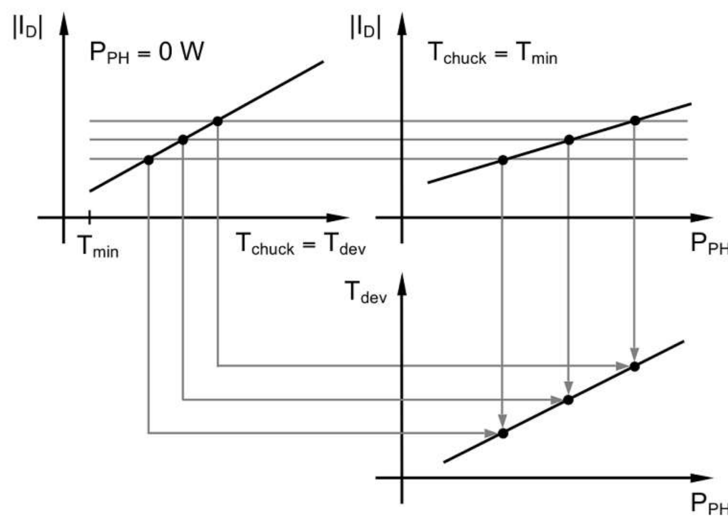

Figure 3.28.: Schematic poly-heater calibration: I_D is obtained at the required $T_{chuck} = T_{dev}$ for $P_{PH} = 0\,W$ and at different P_{PH} at a fixed T_{chuck}, which corresponds to the T_{min} of the setup. $I_D(T_{chuck})$ and $I_D(P_{PH})$ are fitted with a polynomial fit of first or second order. With the coefficients of the fits, $T_{dev}(P_{PH})$ is interpolated for arbitrary poly-heater power at a certain T_{chuck}.

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coefficients $T_{\mathrm{PH}}(P_{\mathrm{PH}})$ can be interpolated. For such calibrations it has to be considered that the coefficients of the polynomial fits are valid only for a certain T_{chuck}. If the poly-heater is used at a different T_{chuck} the calibration has to be repeated for each required T_{chuck}.

The poly-heater technique is able to reach temperatures far beyond the scope of conventional thermo chuck systems. While the latter are typically used up to 200 °C, poly-heater systems can elevate T_{dev} up to 300 °C and more. As a result, the probing temperature range of the poly-heater technique is much wider than the one used for its calibration. In order to make use of this wide range, an analytical expression for $T_{\mathrm{dev}}(P_{\mathrm{PH}})$ has been proposed [121]. Unfortunately, T_{dev} does not depend linearly on P_{PH} but exponentially. A linear dependence is associated with simple Joule heating where the thermal resistivity (R^{th}) of surrounding materials does not play a role. By contrast, in the case of the poly-heater system R^{th} increases simultaneously with the temperature increase. Thus the functional dependence of the device temperature on the power supplied to the heater is an exponential function:

$$T_{\mathrm{dev}}(P_{\mathrm{PH}}) = T_0 - \frac{1}{\alpha} + \left(\frac{1}{\alpha} + T_{\mathrm{chuck}} - T_0\right) e^{\alpha R^{\mathrm{th}}_{\mathrm{sub},0} P_{\mathrm{PH}}} \tag{3.12}$$

with

T_{dev}	device temperatre
P_{PH}	poly-heater power
T_{chuck}	chuck temperature
$R^{\mathrm{th}}_{\mathrm{sub},0}$	thermal resistance of the substrate
α	constant
T_0	constant.

As shown in Figure 3.29, this type of temperature elevation is quite fast compared to other heating setups, e.g., the furnace which was used for the temperature control of devices mounted on a ceramic package in this thesis. As soon as a certain voltage is applied to the poly-heater, it takes approximately 1 ms until the maximum P_{PH} is reached, a process mainly limited by the finite speed of the voltage source [121]. Afterwards, P_{PH} tends to decrease slightly for approximately 1 s because R_{PH} increases due to the elevated T_{PH} until the thermal equilibrium between heater, wafer and chuck is restored. Due to the delayed thermal coupling of poly-heater and MOSFET, T_{dev} increases after turning on the poly-heater and needs up to 10 s for the stabilization. Then, T_{dev} remains constant until the heater is turned off again. After turning off the heater power, P_{PH} decreases to zero within 1 ms, again mainly limited by the finite speed of the voltage source, and T_{dev} needs up to 10 s until it reaches T_{chuck} finally. As a comparison, the furnace which was used for the experimental characterizations of MOSFETs mounted on ceramic packages in this thesis needs more than 30 min until the thermal equilibrium of the system is restored after a temperature change. Due to the significant temperature

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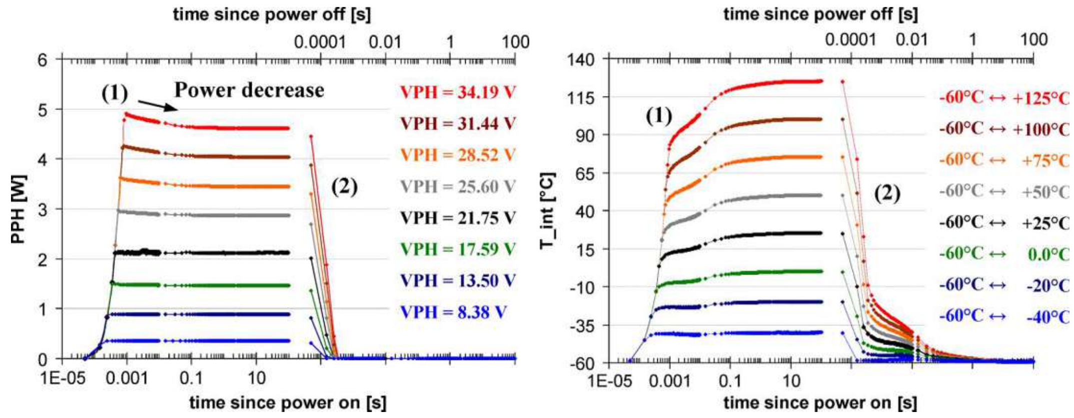

Figure 3.29.: Heating and cooling characteristics: For $T_{\text{chuck}} = -60\,°\text{C}$. **(1)** Left: The heater power is abruptly turned on. Right: Within 1 ms the maximum of P_{PH} is reached. Afterwards, P_{PH} tends to decrease slightly for approximately 1 s until the thermal equilibrium between heater, wafer and chuck is restored. Due to the delayed thermal coupling of poly-heater and MOSFET, T_{dev} needs up to 10 s until stabilization. **(2)** Left: The heater power is abruptly turned off. Right: P_{PH} decreases to zero within 1 ms and T_{dev} needs up to 10 s until it reaches T_{chuck}. Figure source: [120].

switching speed, the poly-heater system is quite promising for the realization of fast temperature ramps [119].

However, the possibility of an application of defined temperature ramps is not the only advantage of a poly-heater system. It can also overcome limitations typically associated with a thermo chuck. One limitation is that switching of the temperature in conventional setups, where T_{dev} is controlled by the thermo chuck and the MOSFET is contacted by probe-needles, the probe-needle contact can get lost. The reason for this is that heating and cooling a wafer on a thermo chuck results in a considerable thermal expansion of the probe-needles. As a consequence, a continuous manual needle adjustment is required when T_{dev} is changed. By contrast, heating with the poly-heater is local and causes no thermal expansion of needles and pads. This enables a change of temperature simultaneously with the measurement cycles without introducing additional delays due to manual needle adjustments.

3.8.2. Temperature Accelerated Measurements in Ceramic Packages

A hardware and software application for temperature control of local poly-silicon heater structures based on the setup in Figure 3.26 has been developed within the TDDS framework [122]. This allows for controlled temperature pulses or ramps during device recovery within the TDDS sequence of stress and recovery cycles. The poly-heater setup can be easily realized with standard equipment as well. Unfortunately, during

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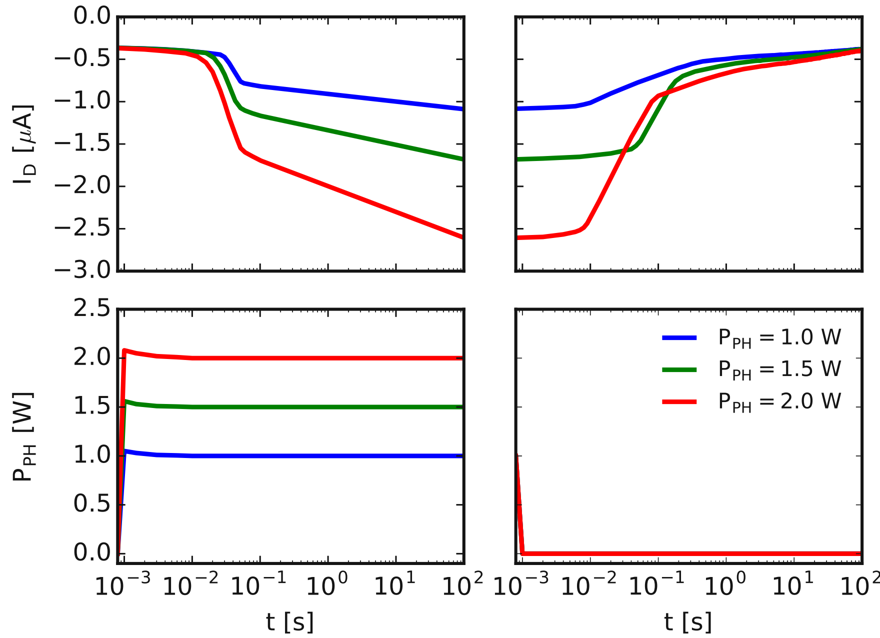

Figure 3.30.: Dependence of the drain current on the dissipated poly-heater power in packaged large-area devices: The left panels show I_D and P_{PH} after the poly-heater is turned on and the right panels show I_D and P_{PH} after the poly-heater is turned off. While the stabilitzation of P_{PH} needs approximately 10 ms, the stabilization of T_{dev} needs 30 min at least (100 s are shown in this figure).

the measurements with this application, difficulties arose, which are discussed in the following.

For the experimental characterization only poly-heater MOSFETs mounted on a ceramic package were available, which introduces a number of complications due to two facts. On the one hand, a ceramic package has no defined heat sink as the thermo chuck in the previously described setup. On the other hand the thermal resistance of the materials surrounding the heater/device system is higher in a package than in the poly-heater-device-chuck-system shown in Figure 3.25 and described in [112, 121]. These two facts lead to a completely different thermal coupling and thermal dynamics between the poly-heater and the MOSFET, which can be seen from the characterization of the heating and cooling dynamics in Figure 3.30. V_{PH} was applied abruptly while I_{PH} and I_D (proportional to T_{dev}) were measured simultaneously. P_{PH} was calculated by multiplication of V_{PH} and I_{PH}.

Although the switching of P_{PH} shows a very comparable time evolution to the measurements on the fabricated wafers (Figure 3.29), I_D does not reach a thermal equilibrium within 100 s. While the stabilization of P_{PH} needs approximately 10 ms, the stabilization of T_{dev} needs 30 min at least. This makes the calibration quite tedious and a pulse-like elevation of the temperature impossible because the whole system needs much longer

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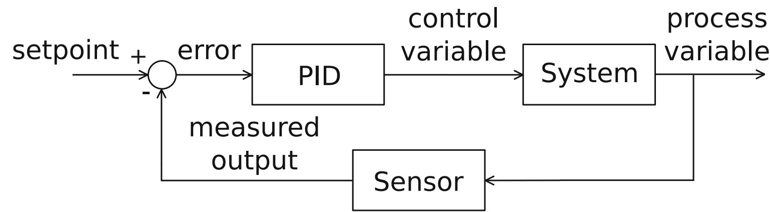

Figure 3.31.: Control loop: A controller (in this case a PID controller) calculates an error value as the difference between the setpoint and the process variable. Based on this error, a correction is applied to the system.

to reach thermal equilibrium than the previously described poly-heater-device-chuck-system.

One way to overcome the challenge of slow heating and cooling dynamics would be to implement a control loop, e.g., using a proportional-integral-derivative (PID) controller illustrated in Figure 3.31. In this context, it is quite easy to implement one in order to hold P_{PH}, which is proportional to T_{PH}, at a constant value by adjustment of the control variable V_{PH} according to the calculated difference between the setpoint for $T_{\mathrm{PH}}(P_{\mathrm{PH}})$ and the measured process variable $P_{\mathrm{PH}}{=}V_{\mathrm{PH}} \cdot I_{\mathrm{PH}}$. Unfortunately, this does not change the behavior of I_{D}, which is proportional to T_{dev}. As discussed in Figure 3.30, P_{PH} stabilizes within 10 ms and is constant afterwards while I_{D} drifts for a longer time. Thus, the implementation of a controller in order to hold I_{D} at a constant value by adjustment of P_{PH} seems to be the proper solution. In such a controller, I_{D} corresponding to the set T_{dev} would be the setpoint, V_{PH} would be the control variable and I_{D} would be the process variable, which is measured in order to calculate the error.

However, such a controller cannot be realized, since I_{D} depends not only on T_{dev}. In fact, I_{D} changes also due to device degradation. If, for example, I_{D} was held constant during the stress phase in eMSM measurements by adjustment of P_{PH}, P_{PH} would increase continuously because I_{D} degrades during stress. As a result, T_{dev} would increase, which accelerates again the degradation of the device. This could consequently overheat the device dramatically. During the recovery phase, I_{D} recovers, which would lead to a decrease of P_{PH} and thus to a cooling effect. As a result, neither during stress nor during recovery, I_{D} could be held at a constant value by adjustment of V_{PH} without changing the degradation and recovery state considerably.

Besides the difficulties associated with the thermal dynamics of the system, also difficulties related to the calibration of nano-scale devices made it nearly impossible to use the poly-heater system. Due to the fact that single oxide defects cause RTN signals with steps of several pA up to µA, I_{D} switches periodically around the calibration point in any nano-scale device. If steps in the drain current of the same magnitude were caused by temperature changes, the corresponding temperature change would be several °C. Even if a nano-scale device is suitable for calibration (no RTN signals), the elevated temperatures during the calibration often lead to the creation of new defects which change the I_{D} level. In other words, the calibration is not reproducible. In this case, a lot of devices

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have to be calibrated in order to be able to calculate mean values for the calibration parameters.

From these experiences, it can be concluded that temperature accelerated measurements using an *in situ* poly-heater are advantageous in the term of the application of fast temperature ramps only if a defined temperature gradient can form between the heating wires and the thermo chuck. In the case of devices mounted on a ceramic package, the time until thermal equilibrium is reached is quite comparable for devices heated by a poly-heater and devices heated by a furnace.

3.9. Conclusions

In this chapter, an overview of commonly used techniques for the experimental characterization of degradation mechanisms is given and challenges which had to be faced for the measurements conducted in this thesis, are discussed. In this context, two methods for the extraction of ΔV_{th} from single point measurements in eMSM sequences are compared. It can be concluded that the extraction of ΔV_{th} using a constant current method and the extraction of ΔV_{th} using a constant voltage method are equivalent methods if three requirements are fulfilled: First, the I_{D}-V_{G} characteristics shift during stress and measurement along the V_{G}-axis but do not change their slope and curvature significantly. Second, the measurement current in the constant current method and the measurement voltage in the constant voltage method are chosen in the subthreshold region near to the threshold voltage of the unstressed device. Third, the device-to-device variability is taken into account, which means that the recovery conditions are set individually for each device depending on its threshold voltage. In case that one of these requirements is not met and depending on the stress and measurement conditions, the extracted $\Delta V_{\mathrm{th}}^{\mathrm{cc}}$ and $\Delta V_{\mathrm{th}}^{\mathrm{cv}}$ can even differ more than 10%.

However, in measurements differences up to 100 % were observed at certain stress conditions. Due to the fact that the measurement setup for the constant current method has been developed for BTI measurements ($V_{\mathrm{D}} = 0\,\mathrm{V}$) only, the stress voltages drift as soon as stress conditions with $V_{\mathrm{D}} \neq 0\,\mathrm{V}$ are applied. As a consequence, the degradation state of the device using the constant voltage method and using the constant current method differ from each other significantly. This leads to completely incompatible ΔV_{th} traces extracted from both methods. The measurements presented in the following chapters were performed using the constant voltage method since the stress voltages are stable during stress.

Additionally, in order to accelerate the degradation and recovery of MOSFET parameters by the application of fast temperature ramps independently from each other, a hardware and software application for the temperature control of *in situ* poly-silicon heater structures has been developed. Measurements on the available devices, which are mounted on a ceramic package, showed that the heating dynamics differs significantly from the one introduced in previous studies because the thermal properties of the surrounding materials differ. As a conclusion, such setups for temperature accelerated measurements are advantageous in the term of the application of fast temperature

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ramps only if a defined temperature gradient can form between the heating wires and the thermo chuck. In the case of devices mounted on a ceramic package, the time until thermal equilibrium is reached is quite comparable for devices heated by a poly-heater and devices heated by a furnace, namely more than 30 min. As a consequence, the measurements presented in the following were performed at a constant temperature during stress and recovery.

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Chapter 4

Discrete Steps in Large-Area Devices

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It is widely accepted that discrete steps in the ΔV_{th} traces, which are caused by individual oxide defects, can be experimentally resolved only in nano-scale devices (this is also discussed in Subsection 2.1.3 and shown in Figure 2.7). However, during the measurements conducted in this thesis discrete steps in the ΔV_{th} traces were also measured in large-area devices. An example is shown in Figure 4.1. In this figure an RTN signal measured on a large-area device with $W = 10\,\mu\mathrm{m}$ and $L = 120\,\mathrm{nm}$ is illustrated.

During the first observations of discrete steps in large-area devices, they were misinterpreted as contact issues. Especially in measurements directly on chip, a temporary failing contact between the needles and the pads have a similar impact on ΔV_{th} traces as the discrete steps associated with charge carrier exchange events caused by oxide defects. However, such steps were observed in a significant number of large-area pMOSFETs and their characteristic capture and emission times showed a bias and a temperature dependence. In particular, 40 % of the large-area MOSFETs showed step heights of $d > 0.15\,\mathrm{mV}$, 30 % showed step heights of $d > 0.5\,\mathrm{mV}$ and 10 % showed step heights of $d > 1\,\mathrm{mV}$. Since no studies on discrete steps in ΔV_{th} traces in large-area devices have been reported in the literature up to now.

4.1. Probability to Measure Discrete Steps

The step heights of discrete steps in the ΔV_{th} traces caused by individual defects in nano-scale MOSFETs are exponentially distributed, as shown in Subsection 2.1.3. Since this empirically found distribution has been formulated based on the measurements of numerous devices and hundreds of defects, it is assumed that the influence of device-to-device variation on the number of oxide defects and random dopants are considered. From the CCDF in Equation 2.2 the probability that a step height with a value greater than a certain ΔV_{th} occurs in a device with a certain W and L can be calculated.

First the probability to measure a step in ΔV_{th} traces with $d > 0.15\,\mathrm{mV}$ (smallest observed d in the large-area devices) in nano-scale devices with $W = 160\,\mathrm{nm}$ and $L = 120\,\mathrm{nm}$ is calculated. For this purpose, SiON pMOSFETs of a 130 nm commercial technology

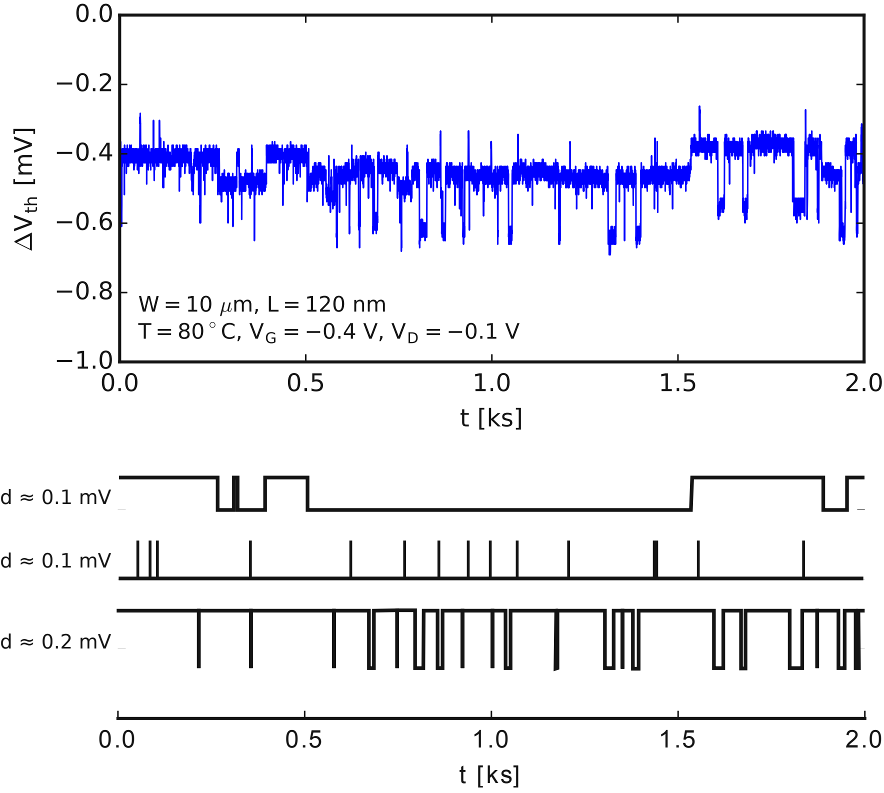

Figure 4.1.: RTN in large-area device: Top: The measured ΔV_{th} trace contains at least three RTN signals but only the one with the largest step height $d \approx 0.2\,\mathrm{mV}$ can be analyzed reliably for different temperatures and gate biases. **Bottom:** The three single RTN signals are shown schematically.

with $t_{\mathrm{OX}} \approx 2.2\,\mathrm{nm}$ were considered. With $C_{\mathrm{OX}} \approx 3.1 \times 10^{-16}\,\mathrm{F}$ and the mean value of the exponential step height distribution for nano-scale devices with the dimensions mentioned in this paragraph, $\eta_{\mathrm{ns}} \approx 1 \times 10^{-3}\,\mathrm{V}$ (Equation 2.3), the probability is

$$F(0.15\,\mathrm{mV}, \eta_{\mathrm{ns}}) \approx 0.86$$

.

By contrast, the probability to find a step with $d > 0.15\,\mathrm{mV}$ in the ΔV_{th} traces of large-area devices with $W = 10\,\mathrm{\mu m}$, $L = 120\,\mathrm{nm}$ as it was observed it is orders of magnitude smaller. With $C_{\mathrm{OX}} \approx 1.9 \times 10^{-14}\,\mathrm{F}$, the mean value of the exponential step height distribution for large-area devices with the dimensions mentioned in this paragraph, $\eta_{\mathrm{la}} \approx 1.6 \times 10^{-5}\,\mathrm{V}$, according to Equation 2.3 the probability is

$$F(0.15\,\mathrm{mV}, \eta_{\mathrm{la}}) \approx 0.00008$$

.

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These results show that it is quite likely to observe discrete steps in the ΔV_{th} traces of nano-scale devices but it should be highly unlikely to observe them in the signal of large-area devices. However, in 40 % of the large-area MOSFETs step heights with $d > 0.15\,\mathrm{mV}$ were measured which is orders of magnitude more than the calculated probability.

In the introduction of this chapter, it is mentioned that the characteristic capture and emission times of the discrete steps in the ΔV_{th} traces of large-area devices showed a bias and a temperature dependence. In this context, the experimental characterization of these dependencies is presented in the next section.

4.2. Experimental Characterization

The fact that it is assumed to be highly unlikely to measure discrete steps in the ΔV_{th} traces caused by individual defects leads to the assumption that maybe other processes are responsible for the observed discrete steps. For further conclusions, the temperature and bias dependences of the characteristic times of the RTN signal in Figure 4.1 were obtained. Therefore, pMOSFETs mounted on ceramic packages were measured since in such an experimental setup contacting issues are minimized.

The experimental characterization of the steps in large-area devices appeared to be quite complicated. Most of the observed step heights are smaller than 0.5 mV, which is very close to the resolution limit of the setup. As soon as the noise amplitude of the signal increases slightly due to, e.g., previously applied stress or elevated temperatures the steps cannot be extracted from the trace anymore. Therefore, statistics cannot be captured with such a small sample set. Nevertheless, a large-area device RTN signal could be characterized, shown in Figure 4.1.

In this figure at least three RTN signals can be seen. The signal with the largest step height, $d \approx 0.2\,\mathrm{mV}$, was characterized since the others were not accurately detectable over different temperatures and gate bias conditions. The results of this analysis is shown in Figure 4.2. The mean values of τ_{c} and τ_{e} were obtained according to Equations 3.9 and 3.10, respectively. It is quite remarkable that $\tau_{\mathrm{c}}(V_{\mathrm{G}})$ and $\tau_{\mathrm{e}}(V_{\mathrm{G}})$ behave similarly to the $\tau_{\mathrm{c}}(V_{\mathrm{G}})$ and $\tau_{\mathrm{e}}(V_{\mathrm{G}})$ of an individual defect in a nano-scale device (see Subsection 2.1.3): With increasing $|V_{\mathrm{G}}|$, τ_{c} decreases and τ_{e} increases and both decrease with increasing temperature.

Unfortunately, as mentioned previously, a thorough analysis of the “defect” parameters with the TDDS framework was not possible. As soon as a stress bias was applied the discrete steps could not be resolved anymore. This results in a too small data set in a too narrow gate bias region to check whether the four state NMP model can explain the observed behavior in order to make conclusions on the properties of such a “defect” in large-area devices. Nevertheless, a few thoughts which might be useful for a future work on this topic are summarized in the following.

- The large-area devices showing discrete steps in their ΔV_{th} traces in the shown measurements have a small ratio L/W. They are quite short but very wide. So far, the dependence of the step height distribution on the channel area or on L

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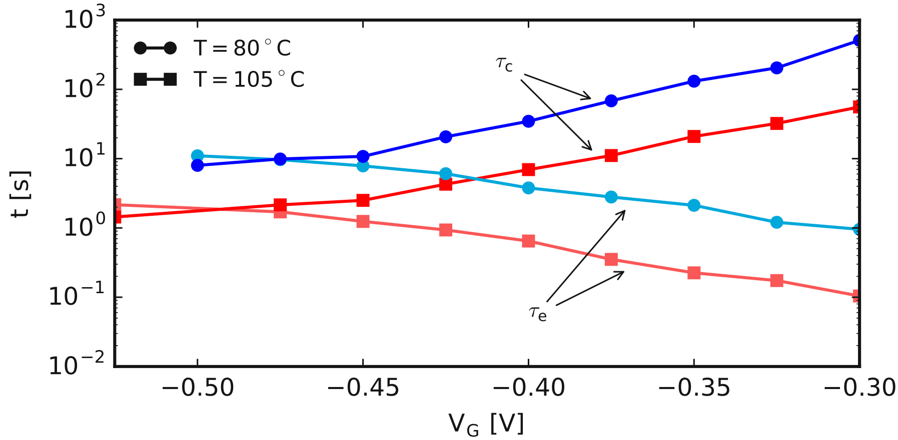

Figure 4.2.: Characteristic capture and emission times obtained from the RTN analysis: τ_c and τ_e behave similarly to an individual defect in a nano-scale device. With increasing $|V_G|$ τ_c decreases and τ_e increases. Both decrease with increasing temperature.

and W independently from each other have been made [18, 56]. However, any study on the dependence of the exponential step height distribution on the L/W ratio has been found – especially for very small ratios. Thus, the empirically found exponential step height distribution might have a different shape for different L/W ratios. In other contexts, e.g., the degradation and recovery of the device-to-device variability, it has been discussed that the edge area might play a role for experimental characterization [123]. This is because, the oxide in the outer regions (edge area) grows less homogeneously than in the middle of the active area during fabrication. Therefore, relative to the active area of the oxide, the edge area is larger in narrow long channel devices than in short wide channel devices. Although the edge area is not the reason for the discrete steps in the measurements, it shows that L/W ratio related effects might have an impact on the step height distribution.

- The discrete steps in large-area devices were always measured in the subthreshold region. In this regime, the conductive channel is not completely formed. Thus, similar to the percolation path in nano-scale devices shown in Figure 1.4, the current flow is not uniformly distributed over the width and single defects might have a similar impact on I_D as shown for nano-scale devices.

- Possible causes for the steps in large-area devices might be capture and emission events of not a single defect but of a cluster of defects. If, for example, the capture and emission events of several defects are coupled and they capture and emit charge carriers simultaneously, the step height in the ΔV_{th} trace would be of course larger than step heights caused by single defects. With this idea, several questions arise,

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like if and how such clusters can form, if and how the capture and emission events can be coupled and many more.

In order to obtain the cause of discrete steps in large-area devices, a thorough experimental analysis is required. The analysis remains an open issue for future works.

4.3. Conclusions

About 40 % of the large-area MOSFETs showed step heights of $d > 0.15\,\mathrm{mV}$ in ΔV_{th} measurements, 30 % showed step heights of $d > 0.5\,\mathrm{mV}$ and 10 % showed step heights of $d > 1\,\mathrm{mV}$. Due to the challenging experimental characterization of steps close to the resolution limit of the experimental setup, the bias dependence and the temperature dependence of only one RTN signal could be characterized. It was observed that with increasing $|V_{\mathrm{G}}|$, τ_{c} decreases and τ_{e} increases and both decrease with increasing temperature. Such a behavior of the characteristic capture and emission times is comparable to the behavior of the characteristic times of single defects. However, due to a too small data set it could not be proved if $\tau_{\mathrm{c}}(V_{\mathrm{G}})$ and $\tau_{\mathrm{e}}(V_{\mathrm{G}})$ can be modeled with a four-state NMP model. Finally, a few thoughts on possible causes for such steps in ΔV_{th} traces in large-area devices were summarized. For example, not a single defect but a cluster of coupled defects might cause such steps. However, further analysis is required on this topic in order to give a proper explanation for possible causes.

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Chapter 5

Impact of Mixed NBTI/HC Stress on MOSFET Characteristics

BTI and HCD are among the most important reliability issues in modern devices. However, as already discussed in the previous chapters, these degradation mechanisms are typically studied in idealized settings. In particular, for BTI studies no voltage is applied to the drain, leading to homogeneous conditions across the oxide and thus to a homogeneous degradation. As soon as $|V_\mathrm{D}|$ is increased, degradation becomes more and more inhomogeneous and the contribution of HCD to the total degradation increases (see Subsection 2.3.1). Even though it is well understood that MOSFETs in real circuits are rarely subjected to idealized BTI or HCD conditions, there is only a limited number of studies available on the impact of the mixed stress conditions as illustrated schematically in Figure 3.1. Therefore, a thorough experimental study of the impact of mixed stress conditions on 2.2 nm SiON pMOSFETs characteristics of a 130 nm commercial technology ($V_\mathrm{DD} = -1.5$ V and $V_\mathrm{th} = 465$ mV) is presented in this chapter, which contains the first experimental characterization at the single defect level.

As an introduction to this chapter, it should be again mentioned that the permanent component, on the one side, is attributed to the generation of interface and oxide defects, the hopping of H through the oxide, and defects with large characteristic emission times. On the other side, the recoverable component of degradation is typically attributed to the emission events of previously charged oxide defects within experimentally feasible time slots (on the order of seconds or minutes). In the following, the focus lies mainly on the recoverable component of degradation.

5.1. Large-Area pMOSFET Characteristics

The characterization of recovery in large-area devices ($W = 10$ µm, $L = 120$ nm or 130 nm) has revealed that with increasing $|V_\mathrm{D}^\mathrm{str}|$ the recovery can be negligibly small. Figure 5.1 illustrates one measurement in this regard. In this measurement, seven cycles of 5 ks stress and 10 ks recovery at a constant $V_\mathrm{G}^\mathrm{str}$ and each cycle increasing $|V_\mathrm{D}^\mathrm{str}|$ were per-

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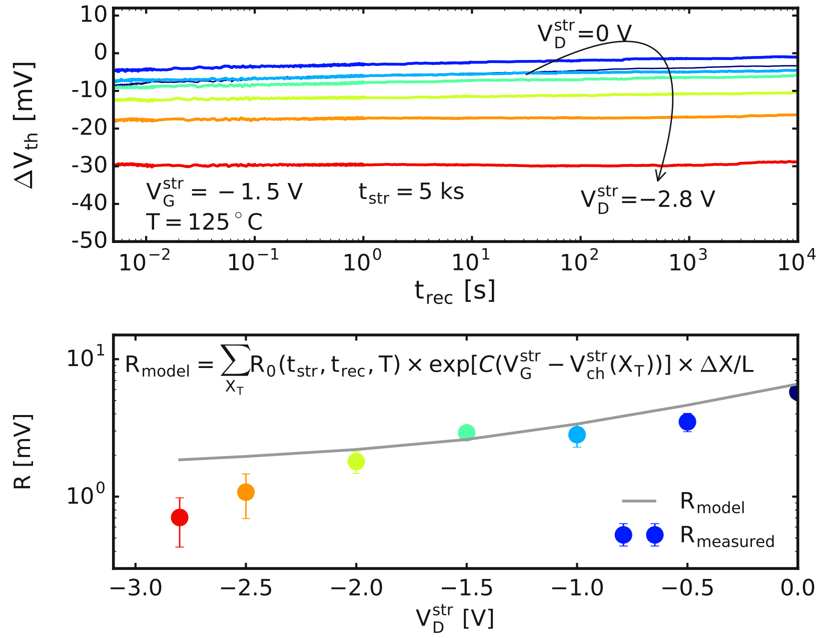

Figure 5.1.: Recovery after mixed NBTI/HC stress: Seven cycles of 5 ks stress and 10 ks recovery at a constant V_G^{str} and increasing $|V_D^{str}|$ were performed. **Top:** Recovery traces show the reduction of R with V_D^{str}. **Bottom:** Comparison of R and a simulation using an electrostatic model. A discrepancy between $R_{measured}$ and R_{model} can be seen, especially at $V_D^{str} < -2\,\text{V}$. R can be negligibly small (less than 1 mV in 10 ks of recovery) after mixed NBTI/HC stress. Figure source: [105].

formed. ΔV_{th} was extracted from a single point measurement of I_D at V_G^{rec} (constant voltage method introduced in Section 3.5). It can be seen that the threshold voltage shift during recovery (R), extracted according Equation 5.1 with $t_{rec,min} = 3\,\text{ms}$, reduces with V_D^{str}. For example, the recovery trace after $V_D^{str} = -2.8\,\text{V}$ (red trace) recovers less than 1 mV in 10 ks.

$$R = |\Delta V_{th}(t_{rec} = t_{rec,min}) - \Delta V_{th}(t_{rec} = t_{rec,max})| \tag{5.1}$$

R	ΔV_{th} shift during recovery (recoverable component)
ΔV_{th}	threshold voltage shift
t_{rec}	recovery time
$t_{rec,min}$	lower limit of the experimental window during recovery
$t_{rec,max}$	upper limit of the experimental window during recovery

The measurement data are compared to a simulation using an electrostatic model as introduced in Subsection 2.3.1. This model takes into account a lateral position dependent threshold voltage shift based on a linear approximation of the channel potential

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under stress according to Equation 2.54. This approximation is valid for lateral positions at the inversion state. At the pinch-off, the channel potential can be calculated using Equation 2.55. In this regard, it is discussed in Subsection 2.3.1 that using an electrostatic model, it is expected that recovery is reduced after stress with increasing $|V_D^{str}|$ because drain-side defects most probably will not contribute to recovery due to the reduced E_{OX}. However, source-side defects should be nearly unaffected by V_D^{str} and contribute to R independently from the drain bias.

Although an electrostatic model describes the behavior of R after NBTI rather well, Figure 5.1 bottom shows discrepancies between the experimental data and the simulation after mixed NBTI/HC stress. The measurements summarized in this figure, as well as measurements in [26], indicate that R can be negligibly small after mixed NBTI/HC stress. This would mean that almost no oxide defects contribute to the recoverable component. This contradicts the assumption that source-side defects contribute nearly unaffected to R. Since oxide defects are uniformly distributed all over the device area, such a behavior cannot be explained by an inhomogeneous E_{OX} only.

In order to analyze the origin of the discrepancies between the experimental data and the simulation, interplay between NBTI and HCD in large-area devices is studied. For this, the eMSM measurement method was used according to Section 3.5 and extracted ΔV_{th} from a single point measurement of I_D at V_G^{rec} during recovery (constant voltage method). 58 devices were measured at $T = 130\,°C$ using the following phases:

1. Measure: I_D-V_G characteristics in the linear ($V_D = -0.1\,V$) and saturation regime ($V_D = V_{DD}$).

2. Stress: application of a (V_G^{str},V_D^{str}) combination within the range of stress conditions shown in Figure 3.1 per device: V_G^{str} is -1.5, -2 and $-2.5\,V$, V_D^{str} is 0, -0.5, -1, -1.5, -2, -2.5 and $-2.8\,V$ for a certain stress time 0.02, 1.11 and 1111 s.

3. Measure: ΔV_{th} for $t_{rec} = 3\,ks$ at recovery conditions (typically $V_D^{rec} = -0.1\,V$ and $V_G^{rec} \approx V_{th}$).

4. Measure: I_D-V_G characteristics in the linear and saturation regime.

From these measurements following was extracted:

- The threshold voltage shift directly after stress (ΔV_{th}^{AS}): extracted as $|\Delta V_{th}(t_{rec,min} = 3\,ms)|$.

- $\Delta V_{th}(t_{str})$ based on the ΔV_{th}^{AS} extraction for different t_{str}.

- ΔV_{th} during recovery.

- The relative $\Delta I_{D,lin}$ and $\Delta I_{D,sat}$ extracted from the I_D-V_G characteristics.

- Recovery according Equaton 5.1.

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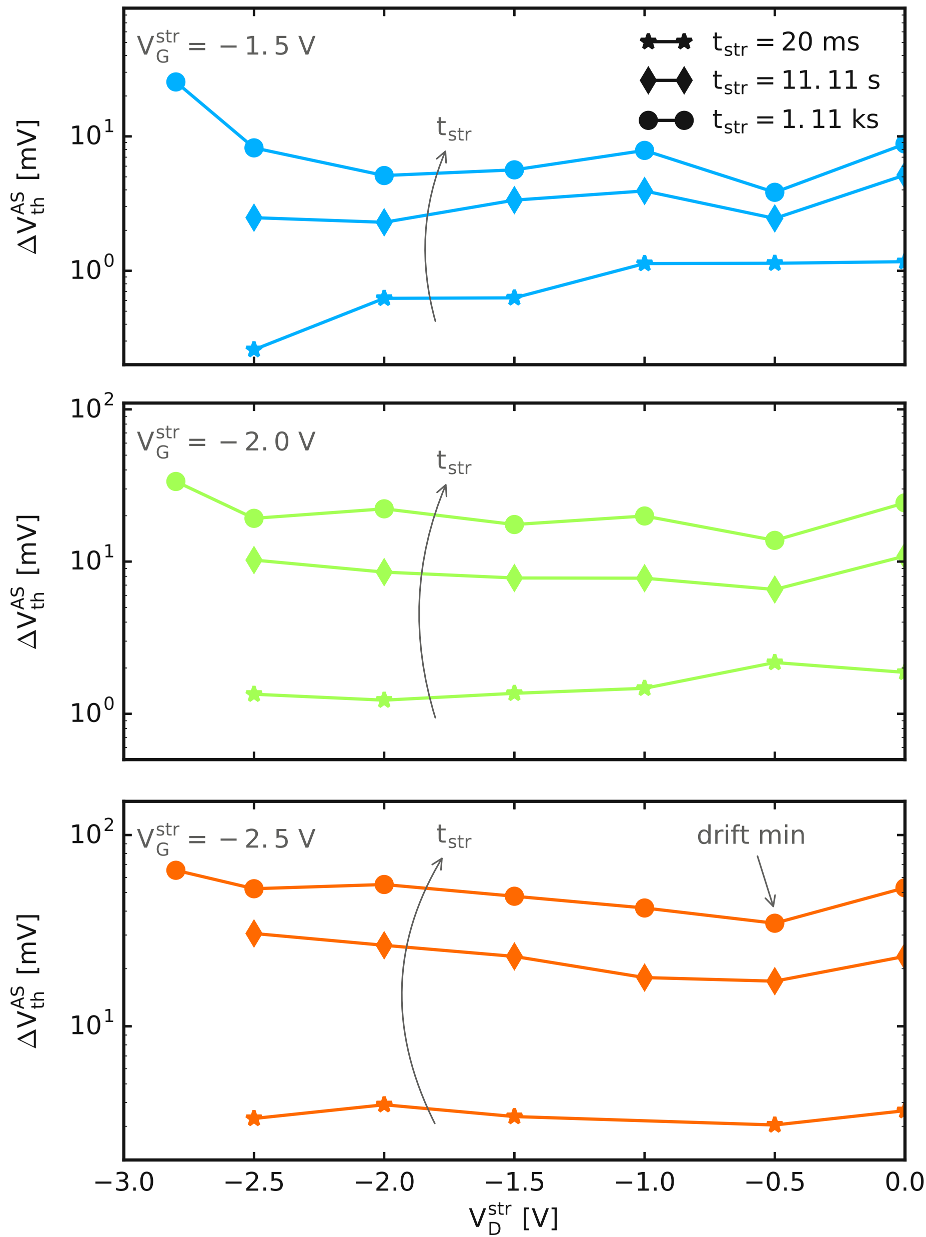

Figure 5.2.: Degradation after stress: ΔV_{th}^{AS} was extracted at $t_{rec,min} = 3$ ms. **Top:** For $t_{str} = 20$ ms the reduction of E_{OX} across the gate oxide near the drain region suppresses NBTI with increasing $|V_D^{str}|$. For larger t_{str} it can be seen that with increasing $|V_D^{str}|$, the interplay between NBTI and HCD leads to two local minima of ΔV_{th}^{AS}, at $V_D^{str} = -0.5$ V and $V_D^{str} = -2$ V. **Center:** Similar to the top panel. With increasing stress time a drift minimum starts to form at $V_D^{str} = -0.5$ V. **Bottom:** The minimum of ΔV_{th}^{AS} at $V_D^{str} = -0.5$ V forms clearly for $t_{str} = 11.1$ s and $t_{str} = 1.11$ ks as discussed in [25, 26]. Figure source: [124].

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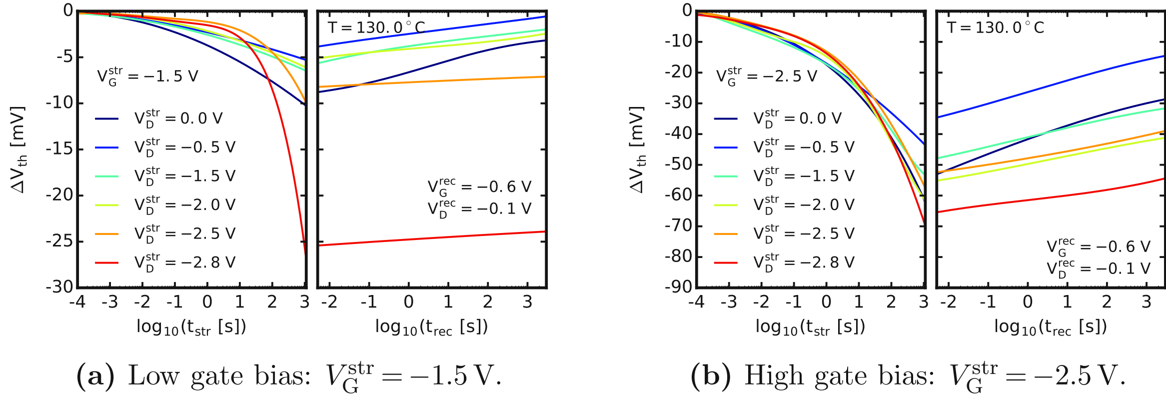

(a) Low gate bias: $V_G^{str} = -1.5$ V. **(b)** High gate bias: $V_G^{str} = -2.5$ V.

Figure 5.3.: Stress and recovery traces at two different gate stress biases: The ΔV_{th} drift during stress depends strongly on t_{str}. Below 100 s the degradation at $V_D^{str} = 0$ V (NBTI) dominates. Above this stress time degradation is more and more dominated by the HC regime. Figure source: [124].

From Figure 5.2 it can be seen that local degradation minima form after stress depending on the stress voltages and on the stress time. While after $t_{str} = 20$ ms ΔV_{th}^{AS} decreases or stays constant with increasing $|V_D^{str}|$, for longer stress times $t_{str} > 10$ s a drift minimum forms around $V_D^{str} = -0.5$ V. Quite interestingly, for $V_G^{str} = -1.5$ V a second minimum forms at $V_D^{str} = -2$ V. The dependence of the formation of such minima on t_{str} is confirmed by the data of Figure 5.3 for the two cases $V_G^{str} = -1.5$ V and $V_G^{str} = -2.5$ V. Especially for $V_G^{str} = -1.5$ V it can be seen that if $t_{str} < 100$ s and $V_D^{str} < 0$ V, $\Delta V_{th}(t_{str})$ is always lower than for homogeneous NBTI.

It has already been discussed in literature [25, 26] that drift minima such as shown in Figure 5.2 occur for long stress times. This behavior was explained by competing processes contributing to the degradation: while sweeping V_D^{str} from 0 V to, e.g., -3 V, ΔV_{th}^{AS} reduces first due to the fact that $|E_{OX}|$ decreases at the drain-side and, as a consequence fewer drain-side defects capture charge carriers. From a certain V_D^{str} on, this effect is compensated by the contribution of HCD to ΔV_{th}^{AS} which leads to an increase. However, this behavior has not been observed for all V_G^{str} and t_{str} in the measurement. For example, ΔV_{th}^{AS} reduces at $V_G^{str} = -1.5$ V and $t_{str} = 20$ ms with increasing $|V_D^{str}|$ without forming any drift minima. It can be concluded that whether and where a minimum forms in ΔV_{th}^{AS} depends strongly on the stress time and on the gate and drain bias.

The analysis of the degradation of $I_{D,lin}$ and $I_{D,sat}$ illustrated in Figure 5.4 shows a strong dependence on t_{str} as well. After $V_G^{str} = -1.5$ V and $t_{str} = 1.11$ ks, a minimum in the $\Delta I_{D,lin}$ and $\Delta I_{D,sat}$ curves can be seen around $V_D^{str} \approx -1$ V, which is comparable to the results in literature [25]. Remarkably, the measurements show that after shorter stress with $t_{str} = 11.1$ s $\Delta I_{D,lin}$ and $\Delta I_{D,sat}$ are higher at a certain V_D^{str} than after stress with $t_{str} = 1.11$ ks also at $V_G^{str} = -1.5$ V. This means that with increasing stress time both first increase, then this trend obviously turns around and they decrease again. Such a behavior has not been observed for higher gate bias $V_G^{str} = -2.5$ V in these measurements.

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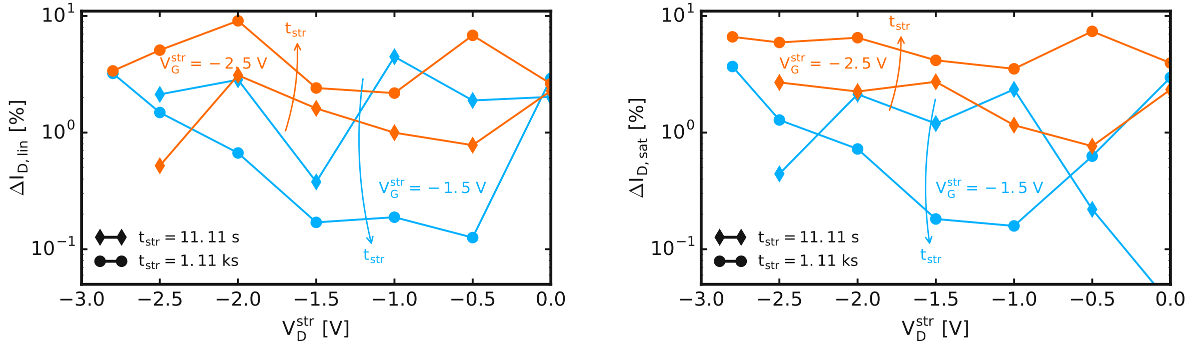

(a) Degradation of the linear drain current: $I_{\mathrm{D,lin}}$ extracted at $V_{\mathrm{D}} = -0.1\,\mathrm{V}$ and $V_{\mathrm{G}} = V_{\mathrm{DD}}$.

(b) Degradation of the saturation drain current: $I_{\mathrm{D,sat}}$ extracted at $V_{\mathrm{D}} = V_{\mathrm{G}} = V_{\mathrm{DD}}$.

Figure 5.4.: Degradation of the drain current in the linear and saturation regime: While the degradation behavior at $V_{\mathrm{G}}^{\mathrm{str}} = -1.5\,\mathrm{V}$ and $t_{\mathrm{str}} = 1.11\,\mathrm{ks}$ is comparable to the results in literature, the curves for $V_{\mathrm{G}}^{\mathrm{str}} = -1.5\,\mathrm{V}$ and $t_{\mathrm{str}} = 11.1\,\mathrm{s}$ show that $\Delta I_{\mathrm{D,lin}}$ and $\Delta I_{\mathrm{D,sat}}$ is higher for lower stress times at certain ($V_{\mathrm{G}}^{\mathrm{str}}$,$V_{\mathrm{D}}^{\mathrm{str}}$) combinations. This means that the degradation evolution of both turns around during stress. Similar behavior was also observed for the degradaton of $g_{\mathrm{m,max}}$ and SS. Figure source: [124].

For a detailed analysis of the time dependent $\Delta I_{\mathrm{D,lin}}$ and $\Delta I_{\mathrm{D,sat}}$ evolution at higher gate stress bias, ten devices were measured using the MSM method (see Section 3.4) with the following phases:

1. Measure: I_{D}-V_{G} characteristics in the linear ($V_{\mathrm{D}} = -0.1\,\mathrm{V}$) and saturation regime ($V_{\mathrm{D}} = V_{\mathrm{DD}}$).
2. Stress: application of a ($V_{\mathrm{G}}^{\mathrm{str}}$,$V_{\mathrm{D}}^{\mathrm{str}}$) combination per device: $V_{\mathrm{G}}^{\mathrm{str}}$ is -0.7, -1, -1.5, -2.0, -2.3 and $-2.8\,\mathrm{V}$ and $V_{\mathrm{D}}^{\mathrm{str}} = -2.8\,\mathrm{V}$ for a certain stress time.
3. Measure: I_{D}-V_{G} characteristics in the linear and saturation regime.
4. Repeat the second and the third phase with increasing t_{str}.
5. Relax: application of recovery conditions for t_{rec}.
6. Measure: I_{D}-V_{G} characteristics in the linear and saturation region.
7. Repeat the fifth and the sixth phase with increasing t_{rec}.

From the I_{D}-V_{G} characteristics $\Delta I_{\mathrm{D,lin}}$ and $\Delta I_{\mathrm{D,sat}}$ are extracted during stress and recovery, which can be seen in Figure 5.5. It has to be noted that a small discrepancy occurs due to the interruptions of the stress and recovery phase compared to measurements without interruptions (also mentioned in Section 3.4). This is because each interruption during stress leads to a partial recovery of the degradation and each interruption during recovery slightly stresses the device. Therefore, the results from these

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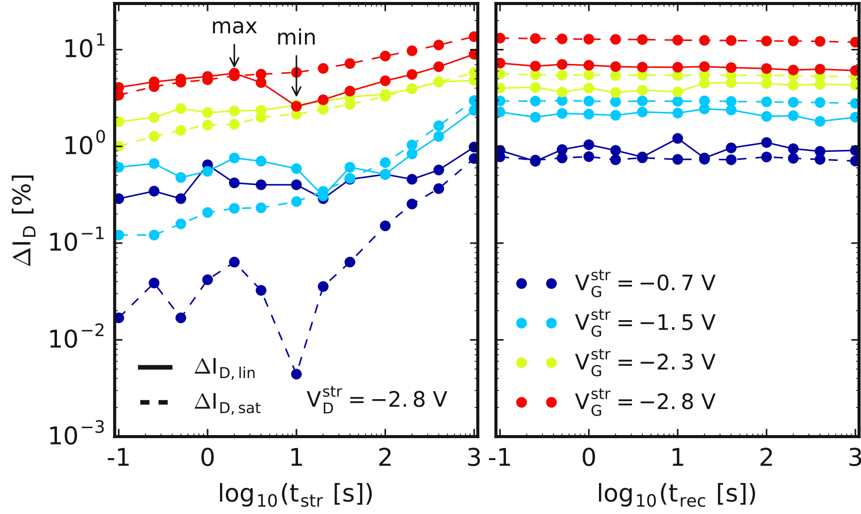

Figure 5.5.: Degradation and recovery of the drain current in the linear and in the saturation region as well as the threshold voltage shift: The degradation and recovery were measured by short interrupts of the stress and recovery phase in order to measure $I_{\mathrm{D,lin}}$ and $I_{\mathrm{D,sat}}$. Especially $\Delta I_{\mathrm{D,lin}}$ but also $\Delta I_{\mathrm{D,sat}}$ show a local maximum after one second of stress, a local minimum after approximately ten seconds of stress, and increases for larger stress times. No turn-around effect was measured for ΔV_{th}.

measurements are shown as a schematic illustration but are not suitable as a basis for a further model development. The analysis of the degradation and recovery of $\Delta I_{\mathrm{D,lin}}$ and $\Delta I_{\mathrm{D,sat}}$ shows that local minima and maxima occur at higher gate bias as well. Depending on the stress voltage combination, $\Delta I_{\mathrm{D,lin}}$ has a local maximum after one second of stress, followed by a local minimum after approximately ten seconds of stress.

Such stress-time dependent turn-arounds of degradation have already been observed recently [99, 100, 102] and discussed in Subsection 2.2.6. Although the explanation in the mentioned subsection cannot be applied to the measured $\Delta I_{\mathrm{D,lin}}$ turn-around in the same way due to the different measurement methods, it gives an idea that II and the interplay of different types of defects together with the creation of secondary generated carriers triggered by II may determine the behavior of device degradation. However, these results merely suggest an interplay between NBTI and HCD and no detailed information about the particular processes at the single defect level can be extracted from these measurements. Thus, the impact of mixed NBTI/HC stress on the behavior of single defects was analyzed and the results are presented in the next subsection.

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Transistor	Def. Nr.	Def. Name	X_T/L	Type
A	1	A1	0.40	blue
	2	A2	0.21	magenta
	3	A3	–	–
	4	A4	0.32	blue
	5	A5	0.17	magenta
B	1	B1	0.71	magenta
	2	B2	0.82	green
	3	B3	–	–
	4	B4	–	–
C	1	C1	0.81	green
	2	C2	–	–
	3	C3	0.86	magenta
D	1	D1	0.20	blue

Table 5.1.: Relative lateral defect position and classification due to capture behavior: By exploiting the recovery drain bias dependence of the step heights for constant gate recovery voltage $V_{\mathrm{G}}^{\mathrm{rec}}$, the lateral position X_{T}/L (0 at source, 1 at drain) was extracted [105]. The uncertainty of X_{T}/L is about 20 %. Defects A3, B3, B4 and C2 showed a very complex behavior (e.g., due to an overlap with other defects in the spectral map at certain bias conditions) and were not characterized fully. The defects are assigned to three types according to their capture behavior during mixed NBTI/HC stress which is explained based on Figure 5.9.

5.2. Individual Defects

In addition to the large-area devices nano-scale devices are used to study the behavior of individual defects in greater detail. The capture and emission processes of single defects which contribute to recovery after NBTI stress, were analyzed. For this, 20 single defects in ten nano-scale pMOSFETs were measured and nine of them in four devices were fully characterized. A list of the extracted defects can be seen in Table 5.1. These particular nine defects were selected in order to best represent the supposed uniform lateral distribution. They were also selected according to their distribution in the spectral map and the ability to characterize properties like τ_{e}, τ_{c}, occupancy and step height over a wide range of stress and recovery voltages.

For the characterization of the single defects, the TDDS framework described in Section 3.7 was used and following phases were applied:

1. Measure: I_{D}-V_{G} characteristics.

2. Stress: Application of a ($V_{\mathrm{G}}^{\mathrm{str}}$,$V_{\mathrm{D}}^{\mathrm{str}}$) combination within the region of stress conditions shown in Figure 3.1 for a certain t_{str}.

3. Measure: ΔV_{th} at $V_{\mathrm{G}}^{\mathrm{rec}}$ and $V_{\mathrm{D}}^{\mathrm{rec}}$ for t_{rec}.

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4. Repeat the second and third phase 100 times in order to capture the statistics.

The recovery traces contain the typical steps due to charge exchange events between the channel and the oxide caused by single oxide defects. Each defect causes exponentially distributed steps with a particular step height at a particular mean value of τ_e. By assigning the unique steps to a defect, the following parameters were extracted for each defect:

- $\tau_e(V_G^{rec},V_D^{rec})$
- $\tau_c(V_G^{rec},V_D^{rec})$
- Occupancy(V_G^{rec},V_D^{rec})
- The lateral position X_T

An analysis at the single defect level gives insight into the detailed behavior of individual defects already measured on average in large-area devices (Figure 5.1). The most surprising finding is that some of the source-side defects do not contribute to R after mixed NBTI/HC stress although they do so after homogeneous NBTI stress with the same V_G^{str}. As discussed above, this behavior cannot be explained by a simple electrostatic model only. In order to assign the behavior of a defect to its position, the relative lateral defect position X_T/L was extracted according to Equation 2.57 – the background is explained in Subsection 2.3.2 – by exploiting the readout drain bias dependence of the ΔV_{th} step heights caused by the defects (see Figure 5.6). In the present case $P_{0max} = 10\,mV$ because these were the largest step heights observed corresponding to defects in the middle of the channel. The results for the relative lateral positions are listed in Table 5.1 and shown in Figure 5.7 as a schematic sketch.

In homogeneous NBTI measurements the defects show a typical behavior as discussed in Subsection 2.1.3. The emission behavior in dependence of V_G^{str} is shown in Subfigure 5.8a for the device B. The emission times of the defects B1 and B2 at the readout conditions are within the experimental window. Therefore, as soon as B1 and B2 capture charge carriers during stress, the emission events are visible in the recovery trace as single steps. At $V_G^{str} = -1.6\,V$ only defect B1 captures a charge carrier during stress because $\tau_c < t_{str} = 10\,s$. Thus, emission events of B1 can be measured during recovery. At $V_G^{str} = -2.2\,V$, τ_c of B2 is low enough that it also captures charge carriers within $t_{str} = 10\,s$. Thus, in the recovery traces steps caused by B1 and B2 are measured. In other words, by increasing $|V_G^{str}|$, the occupancy grows while τ_c decreases. This behavior is also shown in Subfigure 5.9a for all characterized defects.

The measurements at mixed NBTI/HC stress conditions illustrate a more complicated behavior. For a better understanding, it should be recalled what is discussed in Subsection 2.3.1. For mixed NBTI/HC, it is expected that the occupancy of defects near the drain will be reduced compared to homogeneous NBTI measurements due to the reduced E_{OX} and thus increased τ_c. At the same time it is expected that source-side defects remain almost unaffected at mixed stress conditions compared to NBTI conditions. However, Subfigure 5.8b reveals that this assumption is not true. The defects A2 and

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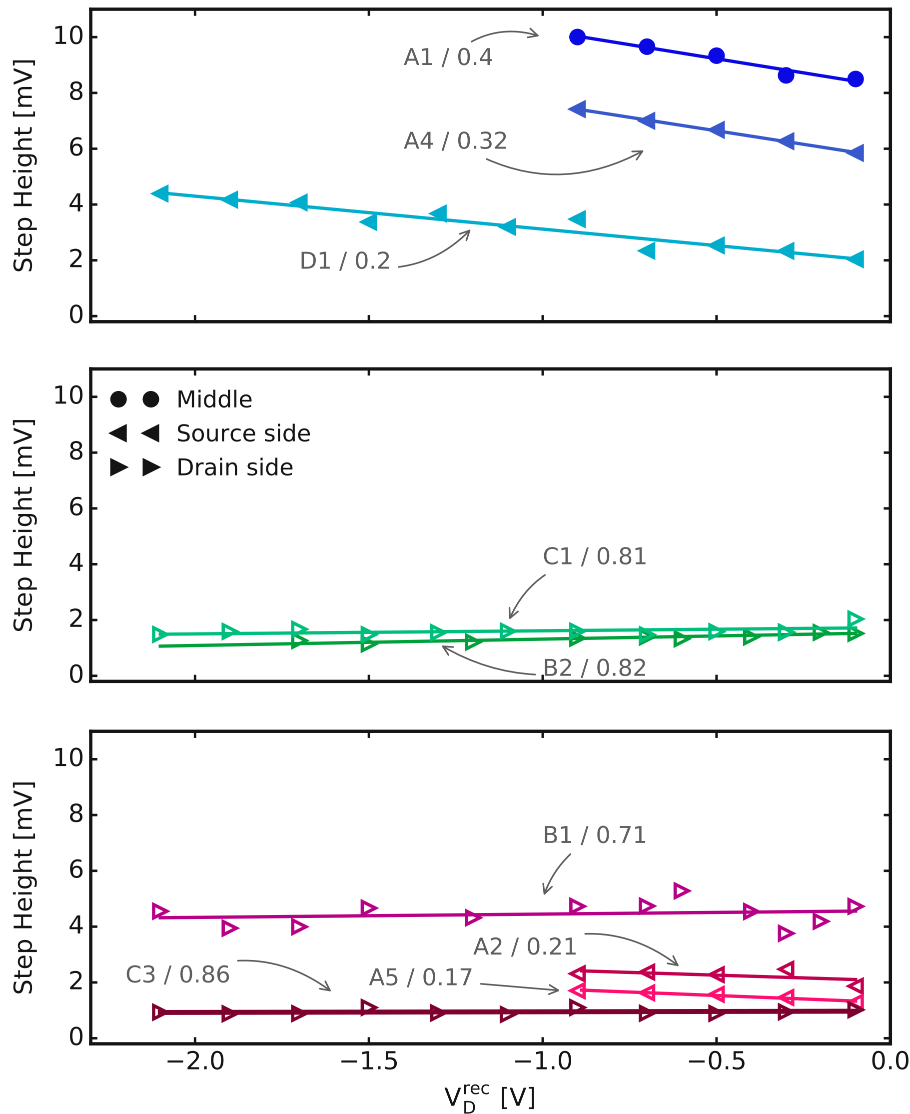

Figure 5.6.: Extraction of the lateral position: The lateral position X_T/L (0 at source, 1 at drain) was extracted by exploiting the recovery drain bias dependence of the step heights for constant V_G^{rec} [104]. The subfigures show the separation of the defects into three types according to their capture behavior during mixed NBTI/HC stress: blue group, green group and magenta group. Measurement data and linear fits are labled with the defect name and the extracted relative lateral position. Figure source: [105].

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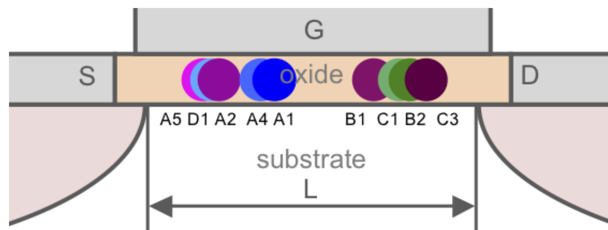

Figure 5.7.: Lateral defect distribution: Schematic sketch of the positions of the nine characterized defects within the oxide. Figure source: [105].

A5, which are in the vicinity of the source, capture charge carriers at homogenous NBTI stress with $V_G^{str} = -1.8\,V$ and emit them during recovery. Contrary to expectations, at mixed NBTI/HC stress with $V_G^{str} = -1.8\,V$ and $V_D^{str} = -2.8\,V$ they do not emit charge carriers during recovery. This means that their behavior is affected by V_D.

The behavior of all defects at mixed NBTI/HC stress conditions is shown in Subfigure 5.9b. At a fixed V_G^{str} (around $-2\,V$) and increasing $|V_D^{str}|$ the defects can be separated into three groups: Either the occupancy is constant for the whole V_D^{str} range (defects A1, D1 and A4 – blue group) or it decreases continuously for $V_D^{str} < 0\,V$ (C1 and B2 – green group) or it shows a local minimum at $V_D^{str} \approx -0.8\,V$, a local maximum at $V_D^{str} \approx -1.5\,V$ and decreases to zero for $V_D^{str} < -1.5\,V$ (C3, B1, A5 and A2 – magenta group). The extracted τ_c with respect to the drain bias shows a slightly increasing trend only for the green group. For the magenta and blue groups τ_c is either constant or decreases.

The green and blue groups behave as expected and discussed previously. Drain-side defects (green group) show a decreasing occupancy and increasing τ_c for mixed NBTI/HC stress due to the significantly reduced E_{OX}. Source-side to mid-channel defects (blue group) show a constant occupancy over the whole V_D^{str} range. However, the defects in the magenta group, where also the two interesting defects A2 and A5 are assigned to, show an unexpected behavior. This can be visualized by a parameterization in terms of V_D^{str} and V_G^{str} in Figure 5.9. This parametrization is illustrated in Figure 5.10 and shows that the traces for increasing $|E_{OX}|$ during NBTI stress and increasing $|V_D^{str}|$ at a fixed V_G^{str} during mixed NBTI/HC stress follow reverse trends for the green group. In other words, the occupancy increases and τ_c decreases for increasing $|E_{OX}|$ while the occupancy decreases and τ_c increases for increasing $|V_D^{str}|$. In stark contrast, the magenta group shows a different behavior for increasing $|V_D^{str}|$. For these defects, increasing $|V_D^{str}|$ causes a decrease in both, occupancy and τ_c.

The fact that A2 and A5 emit charge carriers after homogeneous NBTI but do not after mixed NBTI/HC stress does not mean that they are volatile as soon as mixed NBTI/HC stress is applied. The volatility of all defects was checked regularly by intermittently applying homogeneous NBTI conditions. A volatile defect would have remained neutral after stress independently from the stress conditions. To the contrary, all defects which remained neutral after mixed NBTI/HC stress with high $|V_D^{str}|$ were found to be charged after these intermittent homogeneous NBTI stress checks. None of the characterized defects showed a temporary electrical inactivity during the discussed measurements. The

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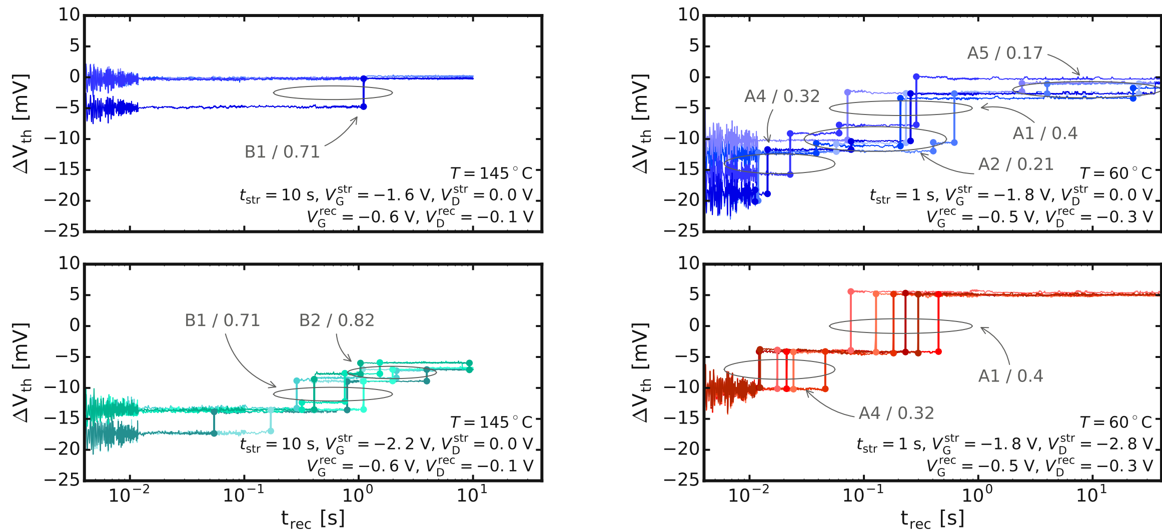

(a) NBTI stress measured on device B: The traces contain discrete steps caused by B1 and B2. **Top:** B2 does not capture a charge carrier at $V_G^{str} = -1.6\,V$ and thus does not emit during the recovery measurement. Only one emission event of B1 can be observed here. **Bottom:** At $V_G^{str} = -2.2\,V$, B1 and B2 capture a charge carrier in 60 % and 50 % of the stress phase, respectively, and emit them during the recovery measurement.

(b) Mixed NBTI/HC stress measured on device A: The traces contain discrete steps caused by A1, A2, A4 and A5. **Top:** At $V_G^{str} = -1.8\,V$ and $V_D^{str} = 0\,V$ all four defects capture a charge carrier during stress and the emission events can be observed in the recovery trace. **Bottom:** At $V_G^{str} = -1.8\,V$ and $V_D^{str} = -2.8\,V$ A2 and A5 do not capture a charge carrier and thus cannot be observed in the recovery traces.

Figure 5.8.: Recovery traces of nano-scale devices after different stress conditions: Six of 100 measured recovery traces show the behavior of the unique steps caused by single defects in the devices B and A. The percentage of emission events is not scaled directly proportional since only six of the 100 recorded traces are shown. Figure source: [105].

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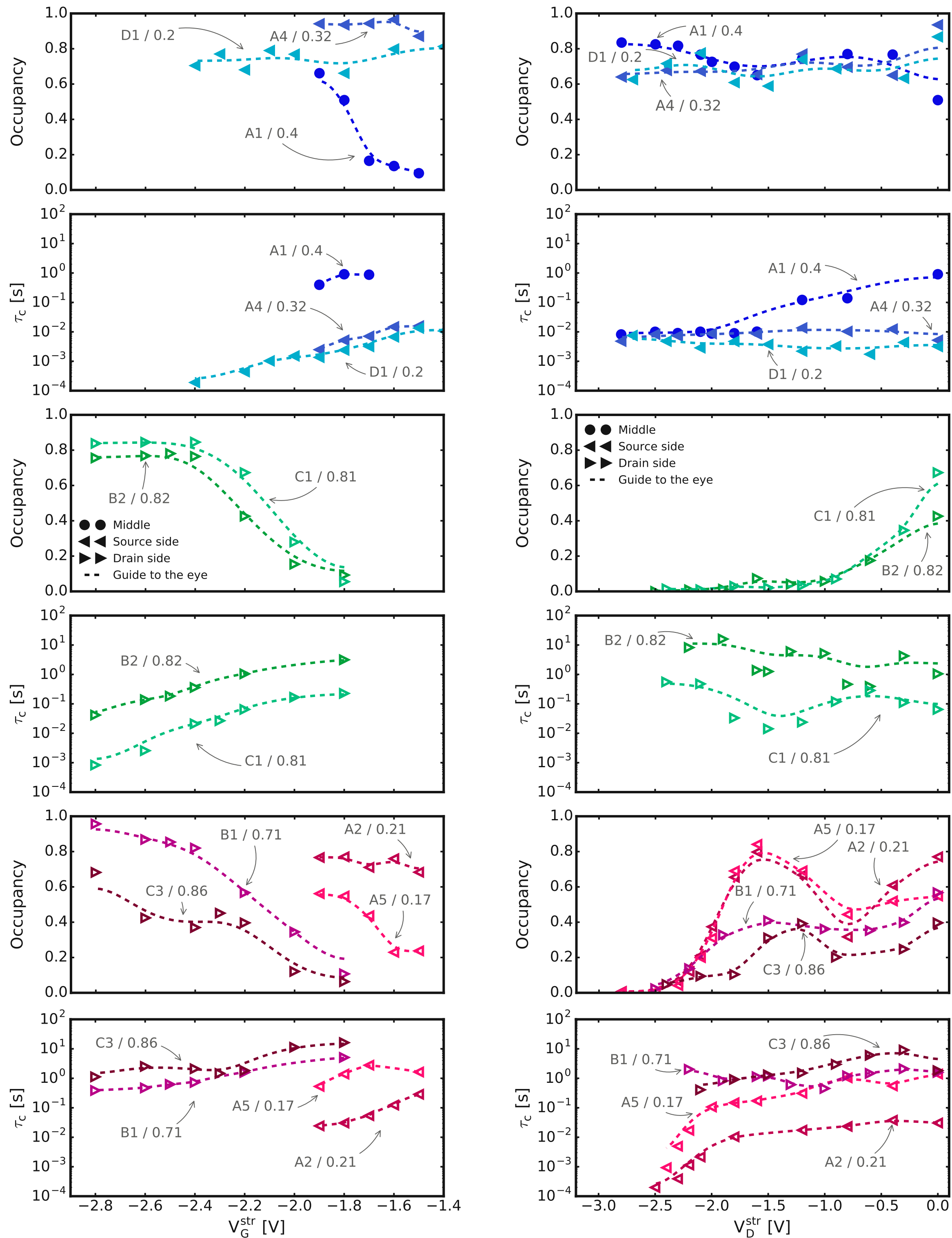

(a) NBTI stress: The defects show a typical behavior. By increasing $|V_G^{str}|$ the occupancy of the defects increases and τ_c decreases.

(b) Mixed NBTI/HC stress: Three types of defects according to their occupancy behavior: blue, green and magenta.

Figure 5.9.: Capture characteristics: For (a) NBTI stress and (b) mixed NBTI/HC stress. Figure source: [105]

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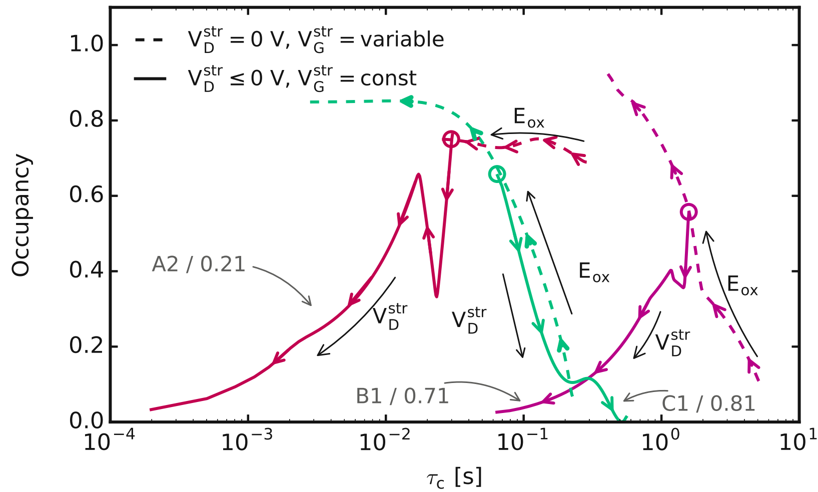

Figure 5.10.: Occupancy versus capture time: A parameterization of $V_{\mathrm{G}}^{\mathrm{str}}$ and $V_{\mathrm{D}}^{\mathrm{str}}$ demonstrates the difference between green and magenta type shown for three defects. **Dashed lines:** For NBTI stress the occupancy increases and τ_{c} decreases for increasing $|E_{\mathrm{OX}}|$ (corresponds to an increasing $|V_{\mathrm{G}}^{\mathrm{str}}|$). **Solid lines:** As soon as $V_{\mathrm{G}}^{\mathrm{str}}$ is held at a constant value and $V_{\mathrm{D}}^{\mathrm{str}} < 0\,\mathrm{V}$, the occupancy of the green defects shows a reversed trend compared to NBTI. The occupancy decreases and τ_{c} increases. This can be explained by the reduction of E_{OX} near the drain for $V_{\mathrm{D}}^{\mathrm{str}} < 0\,\mathrm{V}$. By contrast, the occupancy of the magenta defects shows a completely different trend, namely towards decreasing τ_{c} for a decreasing occupancy. This is an indication for a different process. Figure source: [105].

neutrality after mixed stress conditions must be attributed to microscopic changes in the charge transfer process with increasing $|V_{\mathrm{D}}^{\mathrm{str}}|$. In this regard, Figure 5.11 shows that not only τ_{c} can change but also τ_{e} can change for different drain biases. Consequently, the ratio $\tau_{\mathrm{e}}/\tau_{\mathrm{c}}$ changes for some defects, which affects the occupancy, illustrated in Figure 5.12. This means that as long as $\tau_{\mathrm{e}} \gg \tau_{\mathrm{c}}$ and $\tau_{\mathrm{c}} < t_{\mathrm{str}}$ at stress condition, the defect captures a charge carrier during stress and emits it during recovery (top panels of Figure 5.13). However, if the relation is reversed $\tau_{\mathrm{e}} \ll \tau_{\mathrm{c}}$, the situation is more complicated. Then, it is more likely that a defect emits a captured charge carrier immediately after the capture event while the stress bias is still applied (central panels of Figure 5.13). Although the capture and emission events can repeat several times, it is very likely that no emission event can be measured at recovery conditions, which explains the considerable reduction in occupancy. By contrast, volatile defects do not capture or emit charge carriers at all (bottom panels of Figure 5.13).

It can be concluded that depending on their detailed configuration, defects at all lateral positions can remain neutral after mixed NBTI/HC stress and thus do not contribute to R. This is the primary reason for the discrepancy between the experimental data and simulation at high $|V_{\mathrm{D}}^{\mathrm{str}}|$ as shown in Figure 5.1. So far, such a behavior has not been considered in the current models because oxide defects have been studied only

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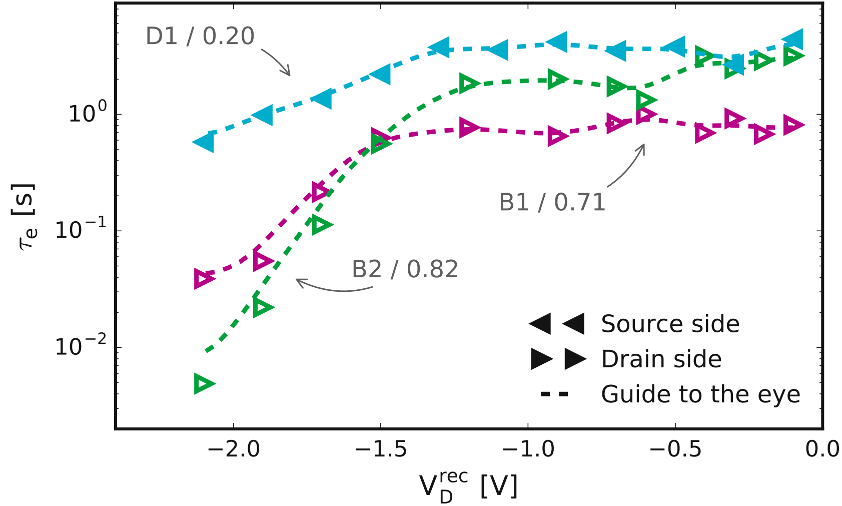

Figure 5.11.: Emission time characteristics: The emission time decreases with $|V_D|$. As a consequence, if $\tau_e \ll \tau_c$ at stress conditions, the defect captures a charge carrier but immediately emits it before switching to recovery conditions. This holds true for all defects of the green and magenta group.

under homogeneous NBTI conditions. In order to explain such a complex behavior like the distortion of the characteristics of source-side defects, also non-equilibrium carrier transport processes induced by the high $|V_D^{str}|$ have to be taken into account in addition to an inhomogeneous E_{OX}.

In this context, the considerable change of τ_e and τ_c can be explained by a change of the transition rates $k_{1,2'}$ and $k_{2,1'}$ between the states 1 and 2′ and the states 2 and 1′, respectively, in the four-state NMP model (Figure 2.18) [125]. The calculation of the transition rates includes among other factors the energy distribution function of the charge carriers (discussed in Subsection 2.1.5 and shown in Equations 2.22 and 2.24) illustrated in Figure 5.14. This figure shows clearly that under homogeneous NBTI conditions the carriers in the channel near the source are in equilibrium and thus properly described by the Fermi-Dirac distribution. As soon as a drain bias is applied this approximation is no longer valid. Carriers can gain energy by the channel field, exchange energy by various mechanisms, and can be severely out of equilibrium.

Furthermore, if the device is operated near or beyond pinch-off conditions, carriers with sufficient kinetic energy can trigger II and consequently generate secondary carriers. As a consequence, additionally to the minority charge carriers in the channel also majority charge carriers are available and may interact with the oxide defects. In Figure 5.14, this is shown as a change of the distribution function of the electrons. Thus a thorough carrier transport treatment by means of a solution of the BTE for each (V_G^{str},V_D^{str}) combination and each lateral position is needed for such situations.

For this purpose, the quasi-equilibrium model, termed $NMP_{eq.}$, which approximates the carrier energy distribution function by a Fermi-Dirac distribution independently

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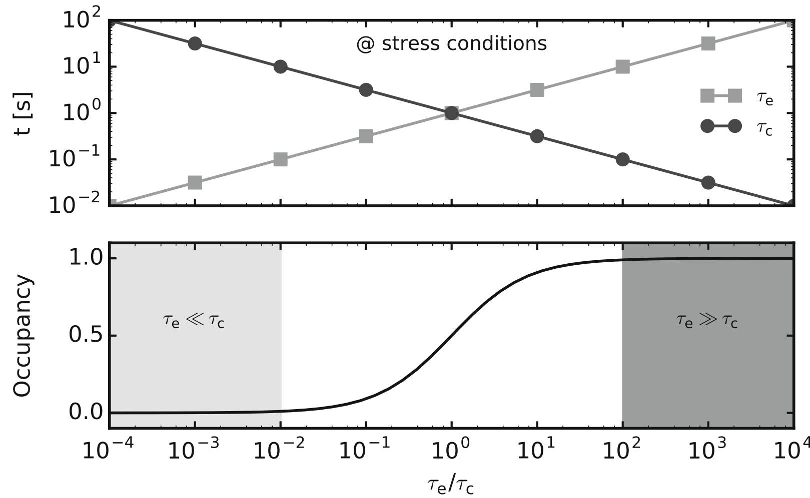

Figure 5.12.: Change of occupancy in respect of the ratio of emission to capture time: Shifts of τ_e and τ_c by a few orders of magnitude affect the occupancy. **Top:** Schematic visualization of the shift from $\tau_e \ll \tau_c$ to $\tau_e \gg \tau_c$ at stress conditions. **Bottom:** Occupancy in respect to the ratio τ_e/τ_c is zero if $\tau_e \ll \tau_c$ and at its maximum if $\tau_e \gg \tau_c$. Figure source: [124].

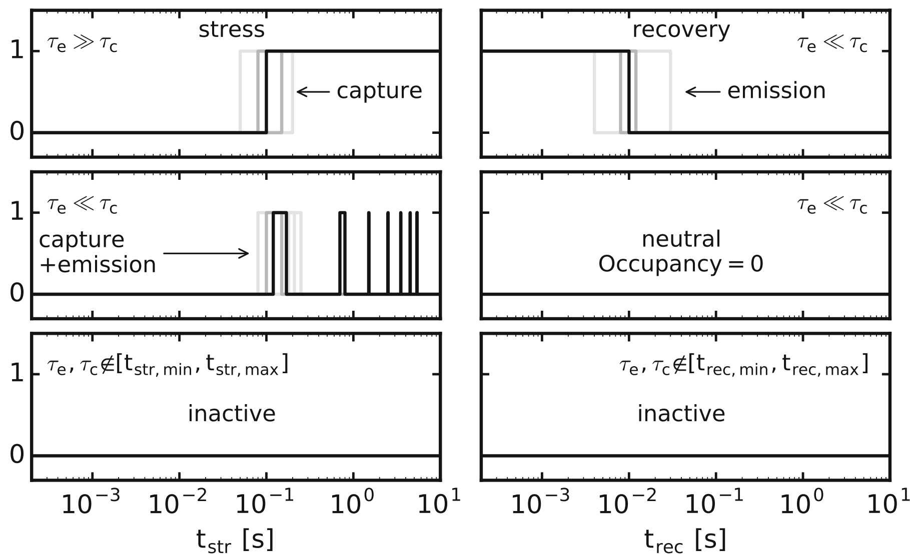

Figure 5.13.: Schematic illustration of capture and emission events: The charge state of the defect 0 if it is neutral and 1 if it is charged. **Top:** $\tau_e \gg \tau_c$ at stress condition. The defect captures a hole during stress and emits it during recovery. **Center:** $\tau_e \ll \tau_c$ at stress condition. The defect captures a charge carrier and emits it immediately afterwards at stress conditions. As a consequence, no emission event can be measured at recovery conditions. **Bottom:** Volatile defects are not electrically active.

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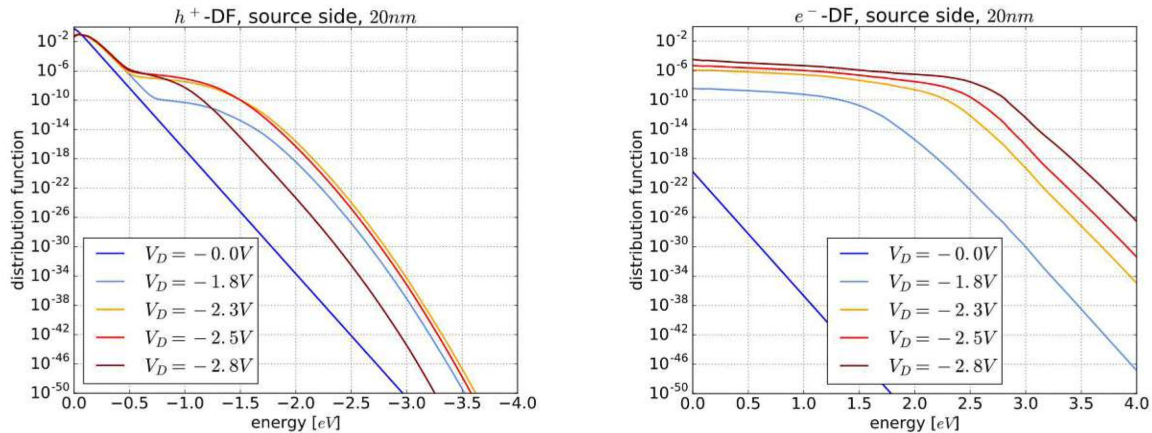

(a) Distribution function of holes: For different V_D and the same V_G.

(b) Distribution function of electrons: Same as (a) but for electrons.

Figure 5.14.: Distribution function of holes and electrons in the vicinity of the source: Under homogeneous NBTI conditions ($V_\mathrm{G} = -1.5\,\mathrm{V}$) the carriers in the channel are in equilibrium and thus properly described by the Fermi-Dirac distribution. By contrast, as soon as a drain bias is applied the carrier ensemble can be severely out of equilibrium. Furthermore, if the device is operated near or beyond pinch-off conditions carriers with sufficient kinetic energy can trigger II and consequently generate secondary carriers. With a thorough carrier transport treatment by means of a solution of the BTE for each ($V_\mathrm{G}^\mathrm{str}$,$V_\mathrm{D}^\mathrm{str}$) combination and under consideration of secondary generated carriers the distribution functions for $V_\mathrm{D} < 0\,\mathrm{V}$ can significantly differ from the equilibrium solution.

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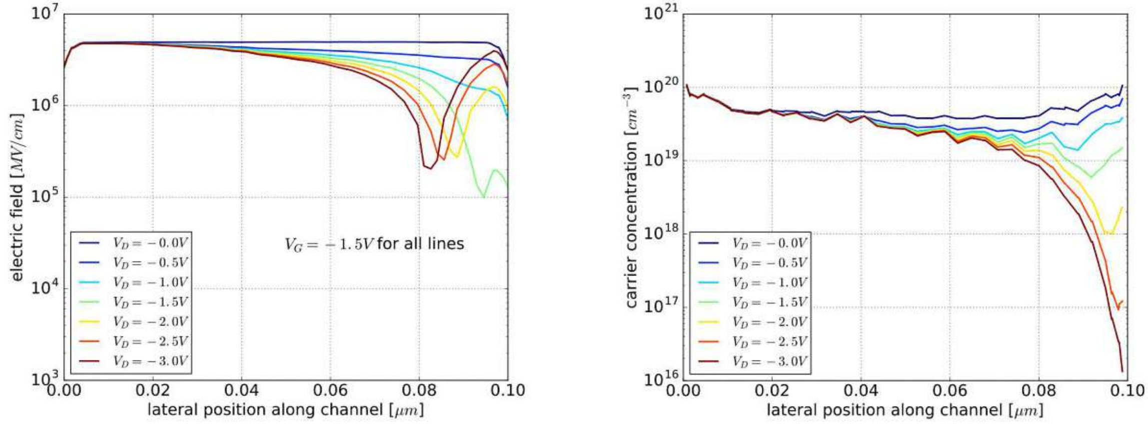

(a) Electric field: Lateral dependence of E_{OX} obtained from simulations with the device simulator MINIMOS-NT.

(b) Carrier concentration: Lateral dependence of the carrier concentration obtained from simulations with MINIMOS-NT.

Figure 5.15.: The lateral electric field and carrier concentration: For the simulation of the transition rates between the defect states 1 and 2′ and the states 2 and 1′ of the four-state NMP model at different V_{D}.

from $V_{\mathrm{D}}^{\mathrm{str}}$ is expanded to the NMP$_{\mathrm{neq.}}$ model, which includes the distribution functions for holes and electrons evaluated with the higher-order spherical harmonics expansion simulator SPRING [125]. Thereby the bipolar BTE was solved self-consistently including phonon and impurity scattering mechanisms as well as impact ionization with secondary carrier generation.

The NMP$_{\mathrm{eq.}}$ model implies that oxide defects mainly interact with carriers in the valence band. Moreover, as it is discussed in Subsection 2.3.1, defects at the source-side are unaffected by $V_{\mathrm{D}}^{\mathrm{str}}$. In contrast, the NMP$_{\mathrm{neq.}}$ model considers the interaction of high energetic carrier in the valence band as well as the interplay of defects with the secondary generated electrons in the conduction band. With this model, the observed defect behavior of $V_{\mathrm{D}}^{\mathrm{str}}$-dependent transition rates even for defects located in the vicinity of the source contact can be captured quite well.

By coupling the NMP model with the device simulator MINIMOS-NT [126] and by considering the real distribution functions of the holes and electrons, the accurate transition rates between the states 1 and 2′ and the states 2 and 1′ for different V_{D} can be calculated. Thus the behavior of τ_{e} and τ_{c} under different stress conditions can be simulated. The electric field and the carrier concentration obtained in simulations using MINIMOS-NT are shown in Figure 5.15. After obtaining the NMP parameters of a defect based on the gate bias dependence of τ_{e} and τ_{c} (Figure 5.16 for the defect B1), the NMP parameters under consideration of the correct distribution function of the charge carriers in the channel the τ_{e} and τ_{c} behavior for different V_{D} can be calculated without introducing any new parameters.

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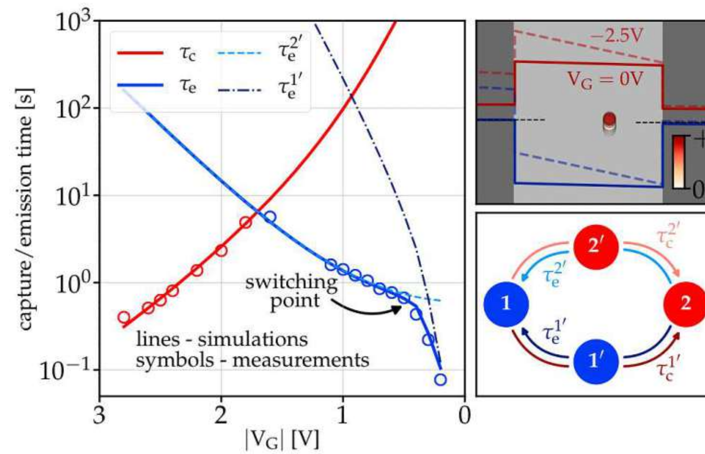

Figure 5.16.: Gate bias dependence of the characteristic times of switching defect B1 modeled with the four-state NMP model: The left panel shows the measurement data (circles) and the simulation results (solid lines). The right panels show the shift of the defect due to an increased E_{OX} (top) and the different capture and emission pathways which cause the switching behavior. The switching point describes the change from the preferred path for emission $2 \rightarrow 2' \rightarrow 1$ to $2 \rightarrow 1' \rightarrow 1$. Charging the defects always proceeds over the path $1 \rightarrow 2' \rightarrow 2$. Figure source: [125].

Figure 5.17 shows the difference between modeling the characteristic quantities of defect B1 using the $\text{NMP}_{\text{eq.}}$ model and the $\text{NMP}_{\text{neq.}}$ model. The characteristic times τ_c and τ_e modeled using the $\text{NMP}_{\text{eq.}}$ model show an increasing trend simply due to the change of E_{OX} at this lateral position and at $V_G = -1.5\,\text{V}$. This does not correspond to the experimental data, which shows a slightly decreasing trend. Furthermore, although the simulated occupancy captures the general decreasing trend for increasing $|V_D|$, it does not reflect the complex experimental behavior. Only if the non-equilibrium conditions are correctly considered an agreement with experimental data is obtained. The $\text{NMP}_{\text{neq.}}$ model is able to capture the rather complex experimental trends, like the decrease of the occupancy to zero at high drain voltages, and properly describes all characteristic quantities of B1.

The behavior shown in Figure 5.17 depends strongly on the configuration of the defect and its lateral position. The impact of the different distribution functions on the defect's behavior cannot be formulated generally. From the experimental results, one can observe that defects assigned to the magenta group are more affected by changes in the distribution functions of the holes and electrons than defects assigned to the green or blue groups. However, the lateral position of a defect is not a meaningful measure for the classification of the three color groups. For example, the defects A5, D1 and A2 are located near the source and quite close to each other but only A5 and A2 show the typical behavior of the defects in the magenta group.

Using the $\text{NMP}_{\text{neq.}}$ model, not only the behavior of individual defects can be simulated with a excellent agreement with the experimental data, also the recoverable component

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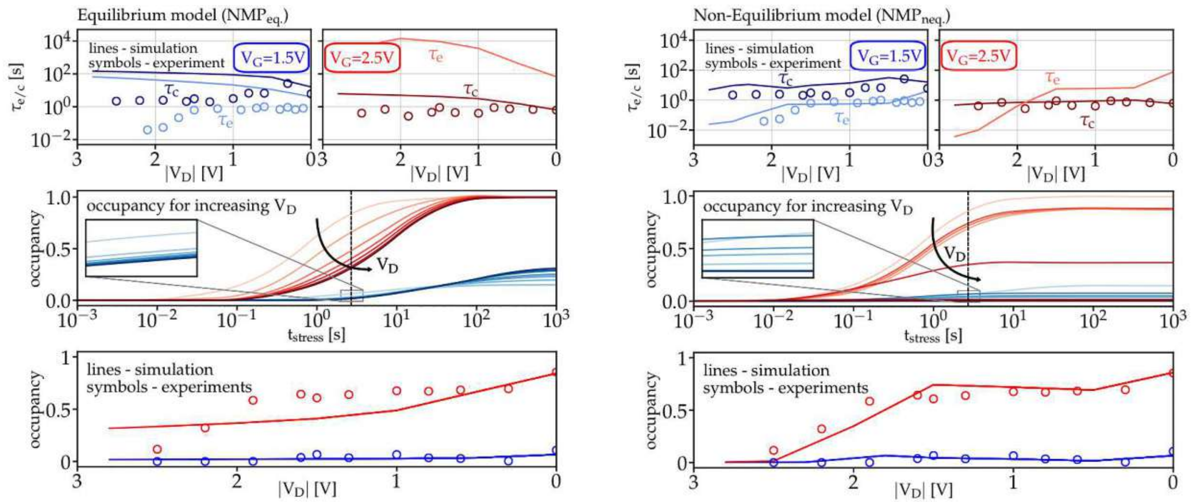

(a) NMP model assuming equilibrium channel carriers: Neither τ_c and τ_e nor the occupancy can be modeled properly. The simulation data of τ_c and τ_e show an increasing trend due to the change of E_OX, which does not correspond to the experemental trend.

(b) NMP model assuming non-equilibrium conditions: This model is able to capture the rather complex experimental trends, like the decrease of the occupancy to zero at high drain voltages, and properly describes all characteristic quantities of B1.

Figure 5.17.: Experimental characterization of the defect B1 for increased drain voltage vs. simulation results obtained with the NMP model: Top: τ_e and τ_c for $V_\mathrm{G} = -1.5\,\mathrm{V}$ and $V_\mathrm{G} = -2.5\,\mathrm{V}$. **Center:** Simulated occupancy for different t_str. **Bottom:** Occupancy at $t_\mathrm{str} = 2\,\mathrm{s}$ – simulation (dashed lines) and experimental data (open circles). Figure source: [125].

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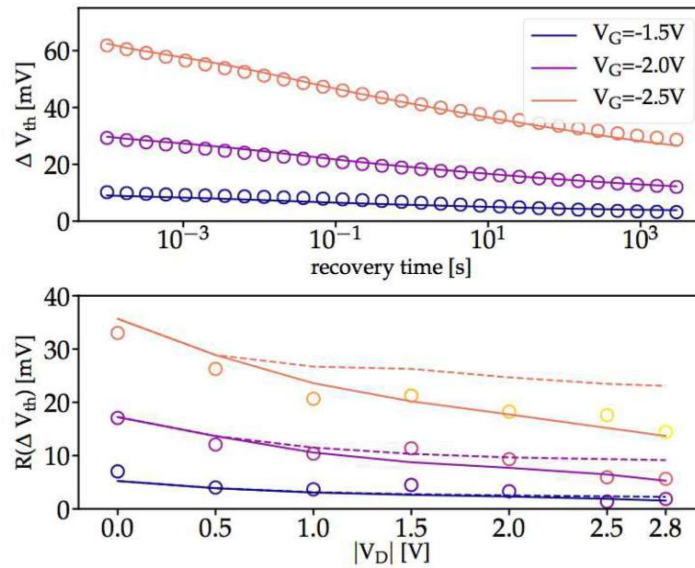

Figure 5.18.: Recovery in large-area pMOSFETs: The open circles show the experimental data and the solid and dashed lines illustrate the simulated threshold voltage shifts. **Top:** Comparison of simulation and experimental data for homogeneous BTI conditions. This data set was used to calibrate the NMP model to extract a unique parameter set for all simulations. **Bottom:** R after mixed stress conditions. The $\mathrm{NMP_{neq}}$ model (solid lines) captures the experimental trend, while the equilibrium NMP model (dashed lines) fails to predict the recovery behavior. Figure source: [125].

of ΔV_{th} of large-area devices can be modeled. This can be done by assuming a large number of defects with different NMP parameters and by considering the lateral and bias dependent distribution functions of the charge carriers in the channel. The recovery R of the measurements discussed in Section 5.1 can be modeled for different bias stress conditions. Figure 5.18 shows that as long as the carriers in the channel are assumed to be in equilibrium independently of the drain bias, R is reduced only due to the change of E_{OX} and no agreement between the experimental data and the simulation can be obtained, quite similar to the discrepancy shown in Figure 5.1 using a simplified electrostatic model. Quite to the contrary, using the non-equilibrium distribution function, the modeled R captures the experimental observations for different stress bias combinations very well.

Finally, Figure 5.19 highlights the main difference between the $\mathrm{NMP_{eq.}}$ model and the $\mathrm{NMP_{neq.}}$ model based on the lateral distribution of charged oxide defects directly after stress. Similar to the discussion in Subsection 2.3.1 and the illustration in Figure 2.32, without taking into account non-equilibrium effects defects located near the source remain unaffected. Their behavior does not depend on the drain bias. By contrast, defects located near the source or in the middle of the channel may be uncharged after mixed NBTI/HCD stress due to the reduces oxide field. The $\mathrm{NMP_{neq.}}$ model, which takes non-equilibrium effects as discussed in the current chapter into account, predicts

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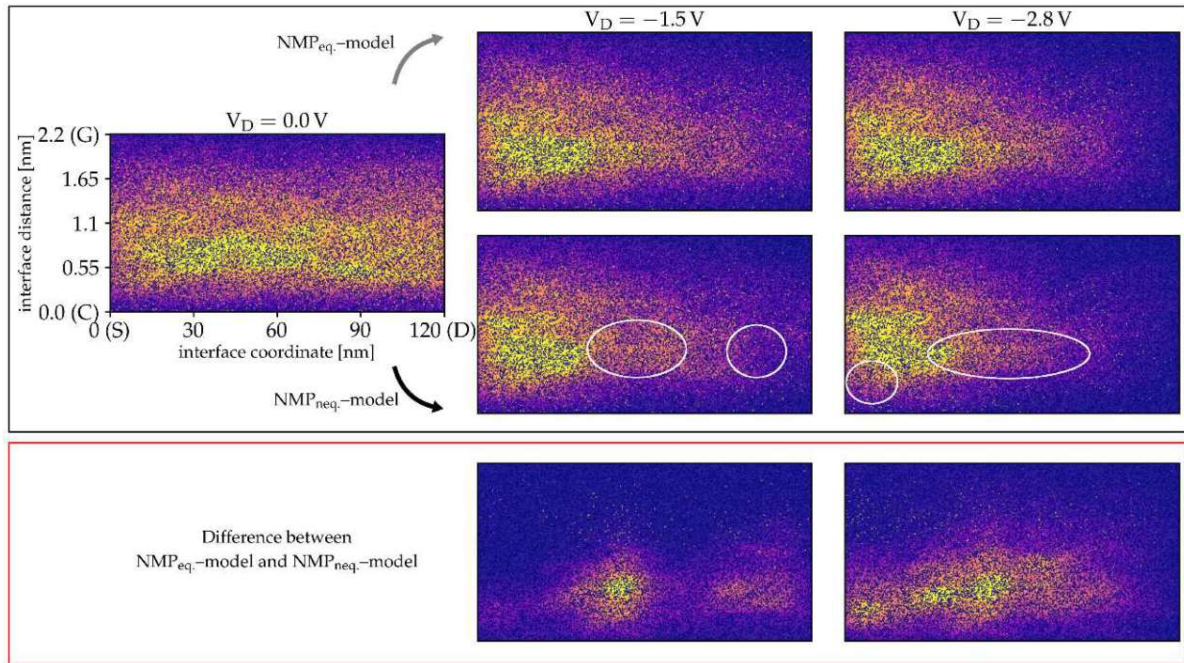

Figure 5.19.: Comparison of the distribution of charged oxide defects directly after stress in large-area pMOSFETs: Using the NMP$_{eq.}$ model defects in the source region are unaffected by an increased V_D. Defects located near the drain as well as in the middle of the channel may remain uncharged due to the reduced oxide field. The NMP$_{neq.}$ model predicts a faster reduction of charged defects (highlighted areas) with increasing drain bias. Remarkably, defects located near the source may remain uncharged as well, which corresponds to the experimental observations. Figure source: [125].

a faster reduction of charged defects with increasing drain bias. Remarkably, not only defects located near the drain but also near the source may remain uncharged, which corresponds to the experimental observations.

5.3. Volatile Oxide Defects

The term of defect volatility is introduced as transitions between active and inactive defect states in Subsection 2.1.6. Volatility describes the phenomenon that defects repeatedly disappear (become electrically inactive) and reappear (become electrically active) during measurements. In other words, a volatile defect does not capture or emit charge carriers, schematically shown in Figure 5.13 bottom. In the previous section, the results for the recovery after mixed NBTI/HC stress are presented and it is shown that recovery can be seriously reduced due to non-equilibrium processes. Even source-side defects can remain neutral after mixed NBTI/HC stress as shown schematically in the central panels of Figure 5.13. Although the neutrality of some defects after mixed NBTI/HC stress has the same consequence for recovery as volatile defects, namely no contribution

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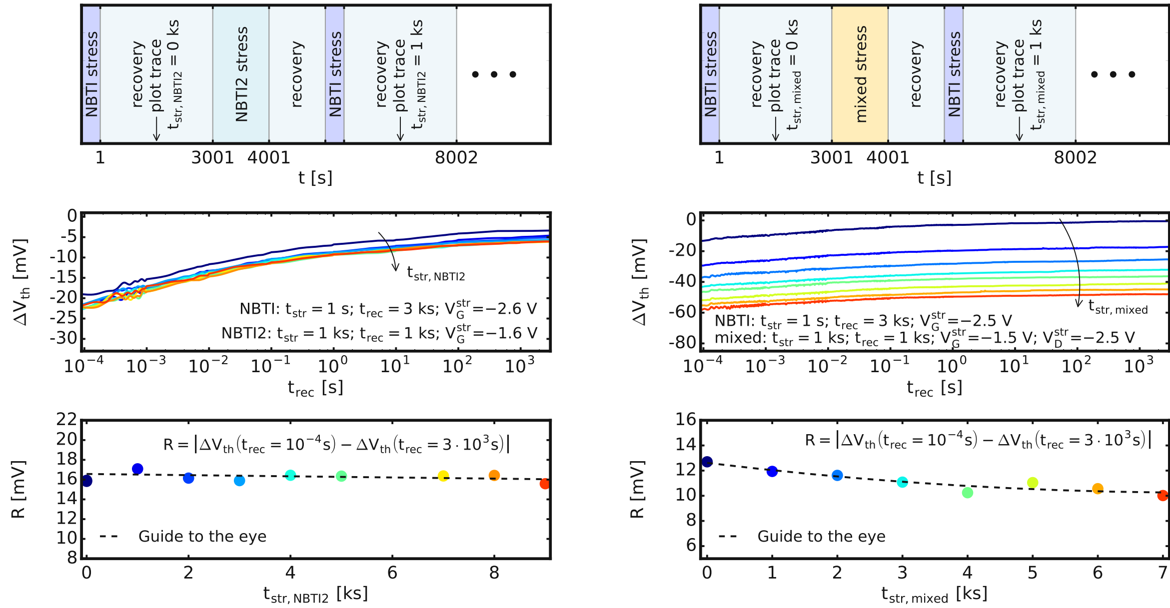

(a) Cycles with only homogeneous NBTI stress: Ten cycles of 1 s NBTI stress/3 ks recovery/1 s NBTI2 stress/3 ks recovery were performed at $T = 125\,°\text{C}$. **Top:** Schematic sketch of the measurement sequences. **Center:** recovery traces. **Bottom:** R defined according Equation 5.1 shows a reduction of 3 %.

(b) Cycles of NBTI and mixed NBTI/HC stress: Eight cycles of 1 s NBTI stress/3 ks recovery/1 ks mixed NBTI/HC stress/1 ks recovery were performed at $T = 125\,°\text{C}$. **Top:** Schematic sketch of the measurement sequences. **Center:** recovery traces. **Bottom:** R defined according Equation 5.1 shows a reduction of 22 %.

Figure 5.20.: Recoverable component of homogeneous NBTI stress: Reduction of R after NBTI due to a preceeding NBTI stress (a) and reduction of R after NBTI recovery due to former mixed NBTI/HC stress (b).

to recovery, there is a fundamental difference between the neutral defects during recovery and volatile defects. Neutral defects affect only the recovery after mixed NBTI/HC stress but not recovery after homogeneous NBTI stress while the volatile defects disappear from all measurements and affect recovery after homogeneous NBTI stress as well. It is mentioned that the volatility of the characterized defects in the previous section was checked regularly by applying homogeneous NBTI conditions and measuring if the observed defects are still electrically active. None of them were volatile during the measurements presented in the previous section. However, following the termination of this study after thousands of cycles of mixed NBTI/HC stress, some defects simply disappeared from the homogeneous NBTI checks. This could be attributed to volatility and is discussed in this section.

In the following R is extracted according to Equation 5.1, but with a different lower limit: $R = |\Delta V_{\text{th}}(t_{\text{rec}} = 10^{-4}\,\text{s}) - \Delta V_{\text{th}}(t_{\text{rec}} = 3 \times 10^{3}\,\text{s})|$. One main difference to the

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previous section is, that R in this section is the recovery after homogeneous NBTI stress and not recovery in general.

Measurements on large-area devices shown in Figure 5.20 illustrate that the behavior of R depends strongly on the "history" of the device. R is extracted from the recovery traces after homogenous NBTI stress with $V_{\mathrm{G}}^{\mathrm{str}} \approx -2.5\,\mathrm{V}$, $t_{\mathrm{str}} = 1\,\mathrm{s}$ and $t_{\mathrm{rec}} = 3\,\mathrm{ks}$. In between measurements of R, stress and recovery cycles of different stress conditions were performed. For example, the measurement shown in Subfigure 5.20a consists of the following alternating cycles applied subsequently to the same device: measurement of R, 1 s NBTI2 stress, 3 ks recovery, measurement of R, 1 s NBTI2 stress, 3 ks recovery and so on. In this context, NBTI2 stands for a homogeneous NBTI stress with a different gate bias than the one used for the measurement of R, $V_{\mathrm{G}}^{\mathrm{str}} = -1.6\,\mathrm{V}$. From the bottom subfigure it can be seen that no considerable reduction of R with respect to the cumulative NBTI2 stress time ($t_{\mathrm{str,NBTI2}}$) can be seen. The reduction is less than 0.5 mV in average at 125 °C, which corresponds to approximately 3 %. In this regard, it has been shown recently, that a considerable reduction of the recoverable component after alternating homogeneous NBTI stress is measurable at higher temperatures and longer stress times [127, 128, 129]. For example, in [127], R shows a reduction of 25 % after 30 cycles of 10 ks stress/10 ks recovery at 200 °C for a similar technology as it is used for the measurements.

By contrast, R reduces significantly even at 125 °C if a mixed NBTI/HC stress has been applied previously, as shown in Subfigure 5.20b. The mixed NBTI/HC stress and recovery cycles were performed instead of the NBTI2 cycles. $V_{\mathrm{G}}^{\mathrm{str}}$, t_{str} and t_{rec} of the mixed NBTI/HC stress and recovery were similar or the same as of the NBTI2 cycles but with a $V_{\mathrm{D}}^{\mathrm{str}} = -2.5\,\mathrm{V}$ applied. The measurement consists of the following alternating cycles applied subsequently to the same device: measurement of R, 1 s mixed stress, 3 ks recovery, measurement of R, 1 s mixed stress, 3 ks recovery and so on. With respect to the cumulative mixed NBTI/HC stress time ($t_{\mathrm{str,mixed}}$) R reduces by 2.8 mV, which corresponds to 22 % at 125 °C. A quite similar reduction of R due to previously applied mixed NBTI/HC stress at the same temperature has been already observed [72].

It has been introduced previously that R can be understood as the cumulative contribution of defects, which have been charged during stress and emit charge carriers during the recovery phase. If R is reduced considerably, some of the defects must have disappeared in terms of electrical activity and thus do no longer contribute to R. However, from the measurements on large-area devices the volatility of individual defects cannot be observed because their individual contributions to the ΔV_{th} traces cannot be resolved. Therefore, the volatility checks performed on nano-scale devices (results presented in the previous section) can provide a detailed insight into the behavior of individual defects. The characterized defects in this regard are listed in Table 5.2.

Similar to the measurement sequences shown in Subfigure 5.20b alternating homogeneous NBTI and mixed NBTI/HC stresses were performed on the nano-scale devices. The purpose of applying the homogeneous NBTI stress was comparable to the one in the measurements on the large-area devices, the extraction of R. Additionally, the activity of the observed individual defects was checked. In this context, the measurements on device B as a representative device for all measured pMOSFETs are discussed.

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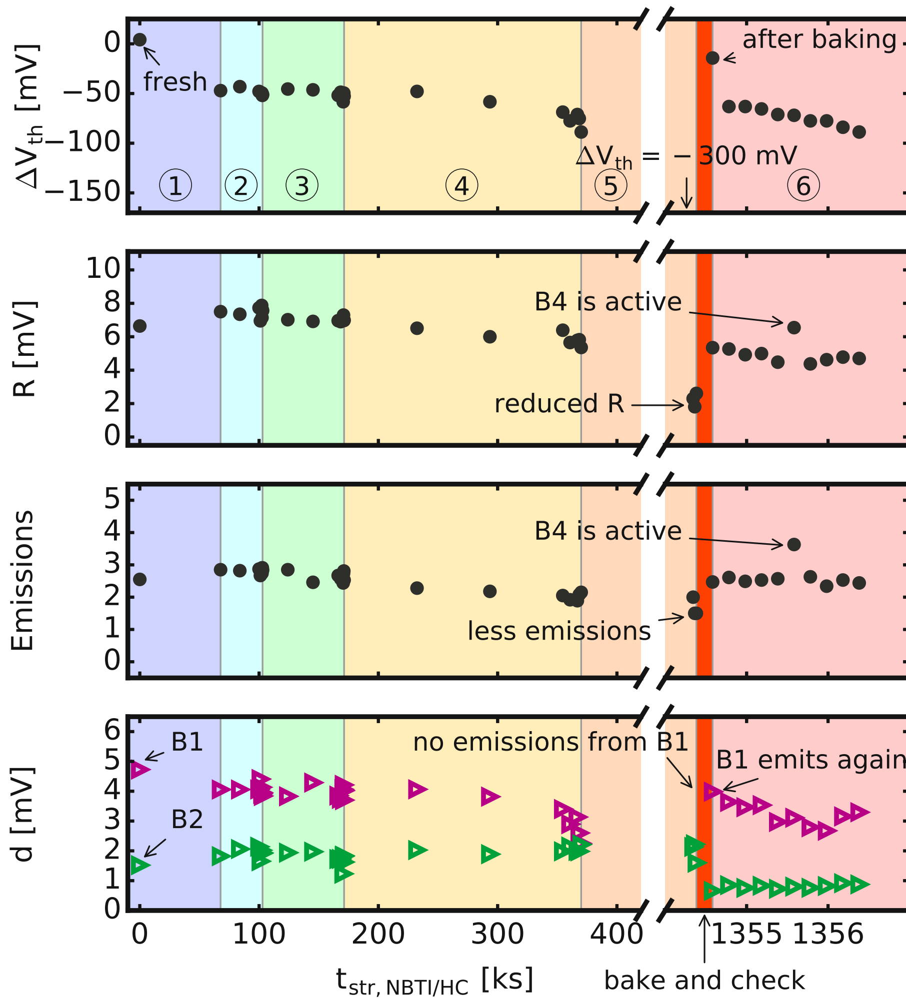

Figure 5.21.: Overall degradation and recovery after NBTI stress of device B: TDDS cycles with NBTI and mixed NBTI/HC stress were recorded at $T = 145\,°\mathrm{C}$. Except of region ① measurement cycles were performed like shown in Figure 5.20b top – NBTI stress / recovery / mixed NBTI/HC stress / recovery / ... Parameters obtained from NBTI measurements are summarized here. Regions: ① NBTI stress recovery cycles with $V_\mathrm{G}^\mathrm{str} = -2.2\,\mathrm{V}$, $t_\mathrm{str} = 1\,\mathrm{s}$ and different recovery voltages $V_\mathrm{G}^\mathrm{rec}$ and $V_\mathrm{D}^\mathrm{rec}$, ② $V_\mathrm{D}^\mathrm{str} = -1\,\mathrm{V}$ and different $V_\mathrm{G}^\mathrm{str}$, ③ $V_\mathrm{D}^\mathrm{str} = -1.5\,\mathrm{V}$ and different $V_\mathrm{G}^\mathrm{str}$, ④ $V_\mathrm{D}^\mathrm{str} = -2\,\mathrm{V}$ and different $V_\mathrm{G}^\mathrm{str}$, ⑤ different $V_\mathrm{G}^\mathrm{str}$ and $V_\mathrm{D}^\mathrm{str}$, ⑥ cycles with $V_\mathrm{G}^\mathrm{str} = -2.5\,\mathrm{V}$ and $V_\mathrm{D}^\mathrm{str} = -2.7\,\mathrm{V}$. R reduces because B1 and B2 change their step heights due to the former applied mixed NBTI/HC stress. It was found that it is more likely for defects with larger step heights, which dominate R, to reduce. Furthermore, some defects like B1 become inactive and do not contribute to R anymore.

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Transistor	Def. Nr.	Def. Name	X_T/L	Volatility
A	1	A1	0.40	no
	2	A2	0.21	no
	3	A3	–	no
	4	A4	0.32	no
	5	A5	0.17	no
B	1	B1	0.71	yes
	2	B2	0.82	no
	3	B3	–	yes
	4	B4	–	yes
C	1	C1	0.81	yes
	2	C2	–	yes
	3	C3	0.86	yes
D	1	D1	0.20	no

Table 5.2.: Defect volatility after different stress conditions: Summary of the observed defect volatility. While the defects B3 and B4 showed a regular volatile behavior by getting inactive and active again from time to time, the defects B1, C1, C2 and C3 were volatile after all stress conditions.

Figure 5.21 is a summary of all recovery measurements after homogeneous NBTI stress of device B. In this device, especially the defects B1 and B2 were monitored. As can be seen, while ΔV_{th} increases with respect to the cumulative stress time of the mixed NBTI/HC stress cycles ①–④, R reduces from 6.5 mV to 5 mV. After all mixed NBTI/HC stress cycles ①–⑤ (before baking) R has reduced to 2 mV. From the mean number of emissions (average over 100 traces of one measurement) and the step heights of the observed defect B1 and B2, the reasons for the reduction becomes clear: on the one hand, the number of emission events reduces, while on the other hand the step heights of the defects change. In this particular case mainly the change of the step height of B1, which is the largest in this device, and the inactivity of B1 before baking contribute to the reduction of R. After three days of baking at 280 °C, B1 becomes active again, as shown in cycle ⑥ in Figure 5.21, with a slightly different step height. During this last cycle, mixed NBTI/HC cycles was applied until the MOSFET failed completely.

Regarding the step height change during the cycles ①–④ in the particular case shown in Figure 5.21, it has to be mentioned that both trends were measured in all devices, increasing and decreasing. In the small sample set, it appears that the decreasing trend was more likely for defects with larger step heights, which dominate R. This concerns B1, A1 and C1 listed in Table 5.1. Interestingly, according to the extraction of the lateral position in [105, 104, 124] these are the defects located laterally near the center of the oxide. Whether a defect changes its step height during operation is predominatly due to deviations of the electrostatic surrounding of the defect as discussed in [16]. This means that as soon as other defects are generated/activated or annealed/deactivated in the vicinity of the observed defect, the step height can change. Thus, the reduction of

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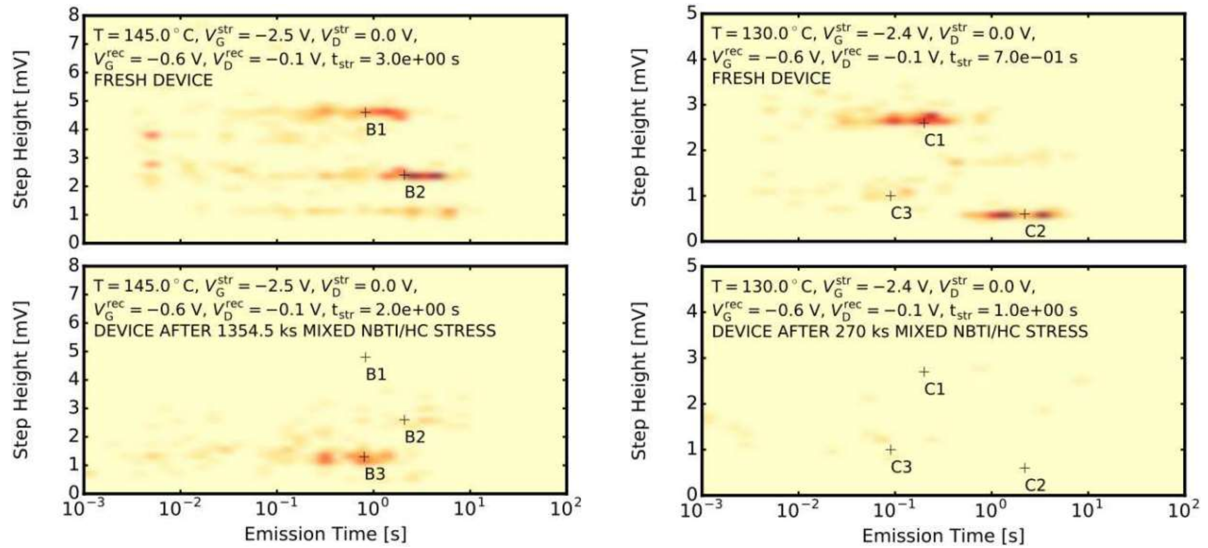

(a) Device B: The defect B1 is active in the unstressed device (top) and volatile after 1354.5 ks of different mixed NBTI/HC stress conditions (bottom).

(b) Device C: The defects C1, C2 and C3 are active in the unstressed device (top) and volatile after 270 ks of different mixed NBTI/HC stress conditions (bottom).

Figure 5.22.: Spectral maps of devices B and C after NBTI stress: The spectral maps of the unstressed devices (top) shows that B1, C1, C2 and C3 are active after NBTI stress. After several cycles of mixed NBTI/HC stress B1, C1, C2 and C3 disappear completely from the spectral map. Especially in device C almost no defect contributes to recovery.

R due to step height changes is most probably attributed to activation or deactivation of other defects near the observed defect in the oxide.

The dominant contribution to the reduction of R after NBTI stress due to previous mixed NBTI/HC stress is the deactivation of defects, as can be seen in the spectral maps (extracted according to the method described in [40]) in Figure 5.22 for the devices B and C. Especially device C is remarkable in this regard because after 270 ks of mixed NBTI/HC stress all defects observed in this device disappear completely and do not reappear until the device failed completely. With this, R reduced permanently to zero. In this context, a few observations on the volatility of defects in the introduced measurements can be summarized.

- Six out of 13 defects show volatility. Three of these six defects, B1, C1 and C3, are located laterally between the center and the drain. For the other three no extraction of their lateral position was possible due to their complicated behavior. While the statistics are small, it appears that it is more likely for defects near the drain to be deactivated with mixed NBTI/HC stress.

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- In [58] the probability to find a defect showing volatility in a measurement window of several minutes to one day is estimated with 22 %. In the presented measurements 46 % show volatility in a measurement window up to 100 s, which is considerably more than this previous estimate. If the reaction barrier of the transition between active and inactive defect states is estimated with an Arrhenius law, as proposed in [65], the temperature plays a major role for the transition time constant and thus for the probability that a defect shows volatility or not. Despite the awareness that the estimation in [58] and the percentage found in the experiments are not fully comparable due to different definitions of the experimental window, self-heating effects might be an issue in the context of defect volatility.

- Apparently, there are two types of volatility. The defects B3 and B4, for example, repeatedly dis- and reappear as expected from volatile defects. By contrast, B1, C1, C2 and C3 disappeared after a certain cumulative stress time of mixed NBTI/HC stress and C1, C2 and C3 did not appear again anymore, even after baking and further measurements.

- It has been previously suggested that volatility concerns all oxide defects [65]. However, the continuous reduction of R shown in Subfigure 5.20b as well as the permanent deactivation of defects as shown in Subfigure 5.22b is an evidence that some defects are “permanently” annealed. The corresponding transitions to a precursor state has been introduced recently in the context of the permanent component of NBTI degradation [74, 115]. Whether such transitions are truely “permanent” has to be checked in future long-term measurements.

5.4. Conclusions

In this chapter the impact of mixed NBTI/HC stress conditions on SiON pMOSFET characteristics was studied with a focus on the recoverable component of ΔV_{th} degradation. It was found that recovery of large-area devices after different stress conditions can clearly deviate from the behavior expected from a simple electrostatic model. This behavior is strong evidence that fewer defects contribute to recovery than would have been expected. Interestingly, the study of the impact of mixed NBTI/HC stress on the behavior of single oxide defects showed that source-side defects can remain neutral after mixed NBTI/HC stress and do not contribute to recovery although they are charged after homogeneous NBTI stress. Defect characteristics like τ_{e} and τ_{c} distort and, as a result, if a defect captures a charge carrier it emits it immediately afterwards still at stress conditions. Consequently, the defect remains neutral after mixed NBTI/HC stress. This effect is determined by non-equilibrium processes triggered by hot carriers with sufficient energies and depends on the detailed defect configuration. By replacing the conventional equilibrium distribution in the charge trapping model with a thorough carrier transport treatment which also considers secondary majority carriers in the channel, recovery after different stress condition can be modeled properly.

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Furthermore, recovery after homogeneous NBTI stress depends on the "history" of the device. Especially if stress and recovery cycles with mixed NBTI/HC stress are performed, recovery after homogeneous NBTI stress is considerably reduced with respect to the cumulative mixed NBTI/HC stress time. Measurements at a single defect level show that this reduction is due to changes of the defect step heights, which is most probably attributed to a distortion of the electrostatic surrounding due to the activation or deactivation of other defects in the vicinity of the observed defect. On the other hand, with a much greater impact on the reduction of recovery, some defects simply disappear from the measurements after numerous cycles of mixed NBTI/HC stress. As a result, recovery after a subsequent homogeneous NBTI stress can be reduced down to zero. Such a deactivation of oxide defects has previously been attributed to defect volatility, a repeated dis- and reappearance of oxide defects. However, a continuous reduction of recovery as well as a seemingly "permanent" deactivation of some of the defects are evidence that a permanent deactivation might play a role here.

The results in this chapter show clearly that NBTI and HCD are not completely independent degradation mechanisms. The fact that effects like II, which are typically associated with HCD, affect the recoverable component of degradation, which is typically associated with the recoverable component of NBTI, leads to the conclusion that degradation mechanisms can be coupled.

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Chapter 6

Conclusion and Outlook

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The impact of mixed NBTI/HC stress conditions on SiON pMOSFET characteristics was studied with a focus on the recoverable component of ΔV_{th} degradation. It was found that recovery of large-area devices after different stress conditions can clearly deviate from the behavior expected in a simple electrostatic model. This is a strong evidence that fewer defects contribute to recovery than would have been expected. In this context, the study of the degradation behavior in large-area devices gives a hint that impact ionization and secondary generated carriers play an important role at mixed NBTI/HC conditions. However, from measurements of large-area devices, the processes relevant for the recoverable component cannot be fully characterized. The study of the impact of mixed NBTI/HC stress on the behavior of single oxide defects showed that source-side defects can remain neutral after mixed NBTI/HC stress and do not contribute to recovery although they are charged after homogeneous NBTI stress. Such a behavior cannot be explained by an electrostatic model only since the electrostatic conditions at the source side are almost unaffected even at high $|V_{\mathrm{D}}^{\mathrm{str}}|$. The founding is that defect characteristics like τ_{e} and τ_{c} distort and, as a result, if a defect captures a charge carrier it emits it immediately afterwards still at stress conditions. Consequently, the defect remains neutral after mixed NBTI/HC stress. This effect is determined by non-equilibrium processes triggered by hot carriers with sufficient energies and depends on the detailed defect configuration. With a model extension, including a thorough carrier transport treatment and under consideration of secondary majority carriers in the channel, recovery after different stress conditions can be modeled properly.

Measurements show that recovery after homogeneous NBTI stress depends strongly on the "history" of the device. Especially if stress and recovery cycles with mixed NBTI/HC stress are performed, recovery after homogeneous NBTI stress is reduced continuously and considerably with respect to the cumulative mixed NBTI/HC stress time. Measurements at a single defect level show that this reduction is due to both, changes of the defects step height and deactivation of defects. The change of the step height is most probably attributed to a distortion of the electrostatic surrounding due to the activation or deactivation of other defects in the vicinity of the observed defect. With a much greater impact on the reduction of recovery, some defects simply disappear

from the measurements after numerous cycles of mixed NBTI/HC stress. As a result, recovery after homogeneous NBTI stress can be reduced even to zero. Such a deactivation of oxide defects has been assumed to be attributed to defect volatility, a repeated dis- and reappearance of oxide defects. However, a continuous reduction of recovery as well as a seemingly “permanent” deactivation of some of the defects are evidence that a permanent deactivation might play a role here. For a full characterization of such a reduction of recovery, further long-term measurements of a large number of individual defects and a thorough analysis of self-heating effects are requried.

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Appendix A

List of Symbols

A.1. Physical Constants

k_B	Boltzmann constant
q	elementary charge

A.2. Physical Quantities

T	temperature
T_{chuck}	thermo chuck temperature
T_{dev}	device temperature
T_{min}	temperature minimum
T_{PH}	poly-heater temperature
P_{PH}	power dissipated in the poly-heater
I_{PH}	current flow through the poly-heater
V_{PH}	voltage applied to poly-heater
R_{PH}	poly-heater resistance
R^{th}	thermal resistivity
V_{th}	threshold voltage
$V_{th,0}$	threshold voltage before stress
A	channel area
$A_{G,eff}$	effective channel area
I_D	drain current
R_{on}	on-resistance
I_B	bulk current
I_G	gate current
V_G	gate voltage
V_D	drain voltage
V_B	bulk voltage
V_D^{meas}	drain measurement voltage

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$I_{\mathrm{D,lin}}$	linear drain current
$\Delta I_{\mathrm{D,lin}}$	linear drain current shift
$I_{\mathrm{D,sat}}$	saturation drain current
$\Delta I_{\mathrm{D,sat}}$	saturation drain current shift
I_{CP}	charge pumping current
V_{GL}	low level of the gate voltage
V_{GH}	high level of the gate voltage
ΔV_{G}	pulse amplitude
$\Delta V_{\mathrm{G}}^{\mathrm{str}}/2$	modulation amplitude
t_{r}	rise time
t_{f}	fall time
t_{str}	stress time
$t_{\mathrm{str,min}}$	lower limit of the experimental window during stress
$t_{\mathrm{str,max}}$	upper limit of the experimental window during stress
t_{rec}	recovery time
$t_{\mathrm{rec,min}}$	lower limit of the experimental window during recovery
$t_{\mathrm{rec,max}}$	upper limit of the experimental window during revery
V_{FB}	flatband voltage
$D_{\mathrm{it}}(E)$	interface-state density at energy level E
N_{it}	interface-charge density
N_{ot}	bulk-oxide-charge density
g_{m}	transconductance
$g_{\mathrm{m,max}}$	maximum transconductance
$\Delta g_{\mathrm{m,max}}$	maximum transconductance shift
ΔV_{th}	threshold voltage shift
$\Delta V_{\mathrm{th}}^{\mathrm{AS}}$	threshold voltage shift directly after stress
$V_{\mathrm{G}}^{\mathrm{str}}$	gate voltage at stress conditions
$V_{\mathrm{G}}^{\mathrm{rec}}$	gate voltage at recovery conditions
$V_{\mathrm{G}}^{\mathrm{cv}}$	gate voltage at recovery conditions using the cv method
$I_{\mathrm{D}}^{\mathrm{cc}}$	drain current at recovery conditions using the cc method
V_{DD}	supply voltage
$V_{\mathrm{D}}^{\mathrm{str}}$	drain voltage at stress conditions
$I_{\mathrm{D}}^{\mathrm{str}}$	drain current during stress
$V_{\mathrm{D}}^{\mathrm{rec}}$	drain voltage at recovery conditions
τ_{e}	emission time
τ_{c}	capture time
t	time
d	step height
R	threshold voltage shift during recovery
I_{D}-V_{G}	transfer characteristics
L	gate length
W	gate width
N_{e}	number of emission events
N_{t}	number of recovery traces

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E_C	conduction band
E_F	Fermi level
E_i	intrinsic energy
E_OX	oxide electric field
t_OX	oxide thickness
C_OX	oxide capacitance
S	sub-threshold slope
SS	sub-threshold swing
ΔSS	sub-threshold swing shift
δ	relative difference between ΔV_th extracted from the cv method and extrated from the cc method
κ	relative permittivity
μ_eff	channel mobility
X_i	defect occupancy of the state i
V_ch	channel potential
X_T	lateral defect position

A.3. Acronyms

AER	active energy region
BJT	bipolar junction transistor
BTE	Boltzmann transport equation
C-V	capacitance-voltage
CCDF	complementary cumulative distribution function
CET	capture/emission time
CMOS	complementary MOS
CP	charge pumping
cv	constant voltage
cc	constant current
MOSFET	metal-oxide-semiconductor field-effect transistor
FinFET	multi-gate field-effect transistor
pMOSFET	p-channel MOSFET
nMOSFET	n-channel MOSFET
FET	field-effect transistor
IGBT	insulated-gate bipolar transistor
BTI	bias temperature instability
NBTI	negative bias temperature instability
PBTI	positive bias temperature instability
HCD	hot-carrier degradation
HC	hot-carrier
HCI	hot-carrier injection
OTF	on-the-fly
MSM	measure-stress-measure

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eMSM	extended measure-stress-measure
TDDS	time-dependent defect spectroscopy
RTN	random telegraph noise
SRH	Shockley-Read-Hall
SILC	stress induced leakage current
TDDB	time-dependenc dielectric breakdown
NMP	non-radiative-multiphonon
PDF	probability density function
DFT	density-functional-theory
II	impact ionization

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Finally, I would like to finish with a quote, which highly motivated me during my work. In *Momo* by Michael Ende Beppo Roadsweeper says to Momo:

“Sometimes, when you’ve a very long street ahead of you, you think how terribly long it is and feel sure you’ll never get it swept. And then you start to hurry. You work faster and faster and every time you look up there seems to be just as much left to sweep as before, and you try even harder, and you panic, and in the end you’re out of breath and have to stop – and still the street stretches away in front of you. That’s not the way to do it.

You must never think of the whole street at once, understand? You must only concentrate on the next step, the next breath, the next stroke of the broom, and the next, and the next. Nothing else.

That way you enjoy your work, which is important, because then you make a good job of it. And that’s how it ought to be.

And all at once, before you know it, you find you’ve swept the whole street clean, bit by bit.

What’s more, you aren’t out of breath. That’s important, too.”

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Experience

since Feb. 2018 **Junior Managers Program Trainee**, *Robert Bosch AG*.
- Business development in the field of Internet of Things
- Analytics of environmental data
- Moderation of Design Thinking workshops

Jan. 2014 – Jan. 2018 **Project Assistant**, *Institute for Microelectronics, Faculty of Electrical Engineering and Information Technology, Vienna University of Technology*.
- Development of experimental setups in microelectronics
- Hardware and software development for probing transistors
- Experimental characterization of field-effect transistors

2013 **Project Assistant**, *Institute for Production Engineering and Laser Technology, Faculty of Mechanical and Industrial Engineering, Vienna University of Technology*.
- Development of an ellipsometer for the measurement of layer thicknesses
- Characterization of thin organic photovoltaic layers

July 2011 – Sept. 2012 **Official in charge**, *Department for Financial Affairs, Austrian Students' Union*, Vienna.
- Participation in compiling of the annual budget and financial report
- Organization of the print contract for the Austrian Students' Union magazine *Progress*

July 2009 – June 2011 **Chair of the University Representation of Students**, *Union of Students at the Vienna University of Technology*.
- Strategical, personnel and economic management of a public body with approximately 25,000 members and EUR 500,000 annual budget
- Representative of the only shareholder of two limited liability companies
- Superior of 30 officials in charge and employees
- Negotiation partner and contact person for study matters

July 2001 – July 2011 **Freelancer, employee**, *various companies*, Vienna, Mödling, Villach.
- Inter alia: Web designer at Virtual Business, project manager trainee at Human Consult PlanungsgmbH Mödling, tutor at Schülerhilfe Humer GmbH, vacation worker at Infineon Techn. Austria AG, tutor at Vienna University of Technology

Education

2013 – present **Doctoral (PhD) Program in Engineering Sciences**, *Electrical Engineering, Vienna University of Technology*.
- Research of degradation mechanisms in field-effect transistors
- Characterization of material defects in field-effect transistors

Oct. 2004 – Oct. 2012 **Diploma Program Technical Physics**, *Vienna University of Technology*.
- Passed with distinction
- Master's thesis: Characterization of Doped CaF_2 Crystals Towards a Solid-State Optical Clock

Sept. 1999 – June 2004 **Engineering-Focused Secondary School**, *Computer Engineering, HTL Mödling (Federal Higher Technical Institute for Educating and Experimenting for Electronics Mödling)*.
- Passed with distinction
- Final examination project: Wireless Security System

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Additional Education

since March 2018 — **Coaching Program for Adult Eduction**, *Austrian Students' Union*.
- Ten modules covering group dynamics, moderation, communication, conversational skills, methodology, outdoor education, conflict management, supervision, etc.

2009 – 2011 — **Negotiation and Communication Training**.
- Rhetoric, training seminar organized by the Union of Students at the Graz University of Technology, November 27th to 29th, 2009 in Velden
- Negotiation, training seminar organized by the Union of Students at the Vienna University of Technology, March 13th to 15th, 2009 in Reichenau an der Rax
- Feminism, training seminar organized by the Austrian Students' Union, March 18th to 20th, 2011 in Reichenau an der Rax

2006 – 2008, 2011 — **Teambuilding**, *The Independent Tutorial Project of the Austrian Students' Union*.
- Methods for leading activities and knowledge of group dynamics
- Organization of the mentoring program for first-year university students

Summer 2004 — **Project Management**, *Human Consult PlanungsgmbH Mödling*.
- Education in project management
- Management of projects with MS Project

Volunteer Activities

since Jan. 2017 — **Member of the Board of Control**, *Austrian Students' Union*.
- Control of the financial transactions of the Austrian Students' Union as well as the unions of students at the universities and their enterprises

Sept. 2006 – Juni 2017 — **Representative of Interests**, *Union of Students at the Vienna University of Technology*.
- Member of self-governing bodies of the Vienna University of Technology. Inter alia: Habilitation Committee, Committee for Appointments, Curricular Committee, Senate
- Member of the editorial board of the program representation's magazine *Phi-6*
- Organization of the mathematics bridging course for first-year university students
- Chair of the program representation of students of Technical Physics, Union of Students at the Vienna University of Technology
- Chair of the program representation of doctoral candidates, Union of Students at the Vienna University of Technology

Languages

German — Native Speaker

Bulgarian — Native Speaker

English — C1 according to the Common European Framework of Reference for Languages

Computer Skills

OS — MS Windows, Mac OS X, Linux Ubuntu

Languages — C, C++, Fortran, Python

Office — Open Office, MS Office, LaTeX

PM Tools — MS Project

Projects

2014 – 2016 — **Member of the Vienna young Scientists Symposium Organization Committee**, *Vienna University of Technology*.
http://vss.tuwien.ac.at
- Chair of the organization committee and editor of the conference proceedings
- Speaker

2007 – 2012 — **Member of an Amateur Theater Group**.
http://www.fstph.at/theater
- Formation and organization
- Actor

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