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TECHNISCHE UNIVERSITÄT WIEN

DISSERTATION

Experimental Characterization of Bias Temperature Instabilities in Modern Transistor Technologies

ausgeführt zum Zwecke der Erlangung des akademischen Grades
eines Doktors der technischen Wissenschaften

eingereicht an der Technischen Universität Wien
Fakultät für Elektrotechnik und Informationstechnik

von

MICHAEL WALTL

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Kurzfassung

Die komplementäre Metall-Oxid-Halbleitertechnologie (CMOS) ist jene Basistechnologie, welche in den meisten elektronischen Geräte des Alltags Anwendung findet. Um die Leistungsfähigkeit der Bauelemente weiter zu erhöhen, werden die in der CMOS Technologie eingesetzten MOS Feldeffekttransistoren (MOSFET) stetig weiter verbessert. Im speziellen konnten durch die Verkleinerung der Bauteilgröße der MOSFETs bis in den Nanometerbereich die Schaltfrequenzen deutlich erhöht werden, jedoch sind mit dieser Optimierung auch ernstzunehmende Zuverlässigkeitsprobleme zu tage getreten. Das ist Motivation für viele Forscher weltweit, welche die Zuverlässigkeit solcher Bauelemente intensiv studieren.

Der bekannteste Effekt, welcher die Leistungsfähigkeit von Transistoren verringert und somit ernsthafte Auswirkungen auf die Lebensdauer hat ist bekannt unter dem Namen *Bias Temperature Instabilities* (BTI) bekannt. In diesem Zusammenhang lässt sich BTI als eine Verschiebung der Schwellspannung beobachten. Die dafür liegt in Lade- und Entladevorgängen von einzelnen Defekten, welche sich an der Halbleiter/Oxid Grenzfläche oder im Dielektrikum befinden. Während der letzten Jahre hat die Modellierung von BTI in großen Transistoren viel Aufmerksamkeit erhalten. Der große Nachteil der Analyse von großen Transistoren ist jedoch, dass aufgrund der Vielzahl von Defekten, nur deren durchschnittlicher Einfluss auf die Verschiebung der Schwellspannung gemessen werden kann. Im Gegenteil dazu können in nur wenigen Nanometer kleinen Transistoren die Lade- und Entladevorgänge der einzelnen Defekten genauer studiert werden. Somit wird ein exakter Einblick in die Physik der Lade- und Entladevorgänge einzelner Defekte gewährt. Um eben solche Lade- und Entladevorgänge von einzelnen Defekten genau zu erforschen, wurde die sogenannte *Time-Dependent Defect Spectroscopy* (TDDS) entwickelt, welche in dieser Arbeit genau diskutiert wird. Um die spannungs- und temperaturabhängigen Lade- und Entladevorgänge einzelner Defekte zu modellieren, wird in weiterer Folge das sogenannte vier-Zustands *non-radiative-multiphonon* (NMP) Modell verwendet.

Obwohl die TDDS bisher schon sehr erfolgreich angewandt wurde um Lade- und Entladevorgänge einzelner Defekte in Transistoren mit SiON als Dielektrikum zu erforschen, gab es zu Beginn dieser Arbeit kein Messgerät welches allen Anforderungen der TDDS gerecht wird. In dieser Arbeit wird eine neues Messgerät, nämlich das TDDS Messinstrument (TMI), entwickelt und präsentiert. Das TMI ist eine Kombination aus programmierbaren Spannungssignalgen-

eratoren, sowie Messeinheiten welche es ermöglichen den Drain-Sourcestrom sowie den Gatestrom der Transistoren mit Strommessauflösungen im Picoamperebereich zu erfassen. Weiteres ermöglicht das TMI hohe Abtastraten für Strommessauflösungen im Picoamperebereich. Mit dem TMI können die Lade- und Entladevorgänge von einzelnen Defekten in n-Kanal und p-Kanal MOSFETs mit SiO_2 oder SiON Dielektrika, aber auch in MOSFETs mit sogenannten *high-k* Dielektrika gemessen werden. Um die Messdaten zu analysieren wird ein komplexer Stufendetektionsalgorithmus verwendet. Dieser ermöglicht es äquidistant und nicht-äquidistant abgetastete Messdaten, wie sie bei TDDS auftreten, zu analysieren.

Unter Einsatz des TMIs wurden einzelne Defekte im Zusammenhang mit *positive* BTI (PBTI) in nMOSFETs das erste Mal analysiert. Ähnlich zu *negative* BTI (NBTI) in pMOSFETs, wurden einzelne Defekte mit spannungsabhängigen sowie spannungsunabhängigen Emissionszeiten gefunden. Diese komplexen, von der Gatespannung abhängigen, Lade- und Entladezeiten können unter Anwendung des vier-Zustand NMP Modells erklärt werden. Als nächstes wurden einzelne Defekte in SiGe Transistoren untersucht. Mit auf unsere Messdaten kalibrierten detaillierten TCAD Simulationen, welche das vier-Zustands NMP Modell anwenden, zeigen wir, dass die Lebensdauer von SiGe Transistoren jene von herkömmlichen Si pMOSFETs bei weitem übersteigt. Dies unterstreicht die außergewöhnliche Zuverlässigkeit der SiGe Transistoren in Bezug auf NBTI. Anschließend wird noch eine Methode präsentiert, um Defekte, welche eine sogenannten permanente Verschiebung der Schwellenspannung verursachen zu untersuchen. Es stellt sich heraus, dass obwohl null Volt an den vier Anschlüssen des MOSFETs angelegt sind, eine beträchtliche Anzahl von Defekten in SiON pMOSFETs geladen wird. Zu guter Letzt wird das TMI eingesetzt um ein Transistorarray zu steuern. Hierbei können mehr als 52000 MOSFETs analysiert, und somit Daten für statistische Aussagen gesammelt werden.

Zusammengefasst wurde mit der TMI ein leistungsfähiges Messsystem entwickelt, welches es ermöglicht, die Zuverlässigkeit von Transistoren in Bezug auf BTI und der sogenannten *hot carrier* Degradation in wenigen Nanometer kleinen sowie vielen Mikrometer großen Transistoren zu erforschen. In Kombination mit computergesteuerten Öfen oder Waferprobern stellt die TMI ein hochmodernes Messinstrument zur Charakterisierung von Transistoren dar.

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Abstract

The complementary metal-oxide-semiconductor (CMOS) technology is the cornerstone of most electronic devices used in everyday life. In order to improve the performance of these devices, the MOS field-effect-transistors (MOSFETs) used in CMOS technologies are continuously optimized. In particular, the scaling of the geometry of MOSFETs down to dimensions in the nanometer regime has increased the switching rates, but on the other hand led to severe reliability issues. As a consequence, transistor reliability is intensively studied by many researchers world wide.

The most prominent mechanism which degrades the device performance and thus seriously affects the time-to-failure is known as the bias temperature instabilities (BTI). BTI manifests itself as a threshold voltage shift caused by charging and discharging of interface states and structural defects located in the dielectrics. During the last decades much attention has been put into modeling of BTI in large-area MOSFETs. However, the big disadvantage of considering large-area devices is that due to the huge number of defects present, only the average contribution of these defects to the shift of the threshold voltage can be studied. Conversely, by probing nanoscale transistors single charge capture and emission events of individual traps can be assessed, which provide detailed insight into the physics of charge trapping. To study charge capture and emission events of single defects, the time-dependent defect spectroscopy (TDDS) has been proposed and is discussed in detail in this work. In order to model the charge trapping kinetics, that is the bias and temperature dependent capture and emission times of single defects, the four-state non-radiative multiphonon (NMP) model is used.

Although the TDDS was already successfully applied to investigate single charge trapping in SiON pMOSFETs, no dedicated measurement setup was available which covers the large list of features of the TDDS. In this work a new measurement equipment, namely the TDDS measurement instrument (TMI), is developed and presented in detail. The TMI combines voltage units which allow to create arbitrary and highly accurate programmable voltage signals, and data sampling units to monitor the drain-source and gate current with a measurement resolution in the sub-picoampere regime. Furthermore, the TMI supports a high sampling frequency even at a current resolution in the picoampere regime. Using the TMI, charge trapping of single defects in conventional SiO_2 n-channel and p-channel MOSFETs, MOSFETs employing high-k dielectrics or even more exotic transistors based on 2D materials can be monitored. To analyze the measure-

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ment data, a sophisticated step detection algorithm is presented which is able to detect discrete steps in uniformly and non-uniformly sampled measurement data, just as they occur in TDDS experiments.

With the TMI, positive BTI (PBTI) of nMOSFETs has been investigated at the single defect level for the first time. Similar to negative BTI (NBTI) studies on pMOSFETs, single defects with bias-dependent and bias-independent emission times have been found. The intricate charge capture and emission dependence on the gate bias can be very well explained by our four-state NMP model. Next, SiGe quantum-well devices were investigated at the single defect level as well. Using detailed TCAD simulations which employ the four-state NMP model calibrated to our measurement data, we demonstrate that the device time-to-failure easily outperforms the lifetime of conventional Si pMOSFETs, underlining the superior NBTI of SiGe transistors. Afterwards, a method which allows to study the permanent contribution to the threshold voltage is presented and it is shown that even at zero bias at all four terminals a significant amount of charge becomes trapped in SiON pMOSFETs. Finally, the TMI is used to control a transistors array where more than 52000 MOSFETs can be studied and thus highly accurate statistics can be collected.

In summary, with the TMI a new powerful measurement framework has been developed which allows to characterize the transistor reliability with respect to BTI and hot carrier degradation in nanoscale and large-area devices. In combination with computer-controlled furnaces and probe stations, the TMI serves as a state-of-the-art device characterization instrument.

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Since the last three years the lunch breaks shared with the "Team Cooking" were a daily highlight. Regular discussions about life beyond our research activities while enjoying varieties of pasta and curry made for a welcome change.

Last but not least I want to express my deepest graduate to my parents *Michaela* and *Ernst*. Without their financial and emotional support I would not have been able to study at a technical university. Special thanks go to my sister *Magdalena* and brother *Bernhard*, recently pushing ourselves to successfully participate at the 33th Vienna City Marathon. I am deeply grateful to my uncle *Manfred Schwanninger*, who besides his extraordinary commitment to research, always supported me. Much to my regret Manfred was not allowed to share the finalization of this thesis with us. Finally, I want to thank *Elisabeth* for her patience and understanding for the numerous hours spent at the Institute.

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List of Symbols

Physical Quantities

Symbol	Unit	Description
A	1	Occupancy
A_{pMOS}	m^2	Gate area of pMOSFET
A_{nMOS}	m^2	Gate area of nMOSFET
C_{DG}	F	Drain-gate capacitance of a MOSFET
C_{DS}	F	Drain-source capacitance of MOSFET
c_1	$\mathrm{eV}/[\mathrm{a.u.}]^2$	Curvature of potential energy surface of state 1
c_2	$\mathrm{eV}/[\mathrm{a.u.}]^2$	Curvature of potential energy surface of state 2
C_{ox}	F	Oxide capacitance
ΔD_{it}	cm^{-3}	Change of the interface charge density
ΔD_{ox}	cm^{-3}	Change of the oxide charge density
ΔN_{it}	cm^{-3}	Change of the interface trap density
ΔN_{ox}	cm^{-3}	Change of the oxide charge density
ΔQ_{it}	C	Change of the interface charge
ΔQ_{ox}	C	Change of the oxide charge
D_{it}	cm^{-3}	Interface charge density
$\Delta V_{\mathrm{in,max}}$	V	Input voltage range
ΔV	V	Voltage resolution
ΔV_{th}	V	Threshold voltage shift
ϵ_{r}	1	Relative permitivity
$\epsilon_{\mathrm{HfO_2}}$	1	Relative permitivity of HfO_2
ϵ_{ox}	F/m	Permitivity of the gate dielectrics

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ϵ_t^c	eV	NMP barrier for charge capture
ϵ_t^e	eV	NMP barrier for charge emission
ϵ_{Si}	1	Relative permitivity of silicon
ϵ_{SiO_2}	1	Relative permitivity of SiO_2
$eta_{\mu m}$	V	Average step height of defect in large-area transistor
eta_{nm}	V	Average step height of defect in nanoscale transistor
E_A	eV	Activation energy
E_A^c	eV	Activation energy of charge capture
E_A^e	eV	Activation energy of charge emission
E_F	eV	Fermi-level
E_{ox}	V/m	Electric oxide field
$E_{ox,s}^{eff}$	V/m	Effective electric oxide field during stress
E_T	eV	Defect trap level
f_{ox}	1	Occupancy of oxide traps
f_s	Hz	Sampling frequency
f^{max}	Hz	Maximum frequency
$f_{s,max}$	Hz	Maximum sampling frequency
g_m	S	Transconductance
H_{it}	cm^{-3}	interfacial hydrogen concentration
I_{ch}	A	Channel conduction current
I_{DS}	A	Drain current
$I_{D,lin}$	A	Drain current in the linear regime
I_G	A	Gate current
I_{in}	A	Input current
I_{max}	A	Maximum current
I_{ref}	A	Reference current
$I_{sc,max}$	A	Short-circuit current
k_{12}	1/s	Transition rate between state 1 and state 2
k_{21}	1/s	Transition rate between state 2 and state 1
k_{ij}	1/s	Transition rate between state i and state j
k_H	1/s	Hydrogen dimmerization rate
k_{H_2}	1/2	Hydrogen atomization rate
k_r	1/s	Reaction-diffusion model forward reaction rate
k_r	1/s	Reaction-diffusion model backward reaction rate
L	m	MOSFET gate length
μ_{eff}	$cm^2/(Vs)$	Effective channel mobility
ν_0	1/s	Attempt frequency
N_e	1	Number of emission events
$N_{it,0}$	cm^{-3}	Initial interface state density

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N_{it}	cm^{-3}	Interface state density
N_N	1	Number of measured recovery traces
N_{pMOS}	cm^{-3}	pMOSFET trap density
N_{nMOS}	cm^{-3}	nMOSFET trap density
N_T	1	Number of active defects
$N_{T,\mu m}$	1	Number of active defects in large-area devices
$N_{T,nm}$	1	Number of active defects in nanoscale devices
N_{tot}	cm^{-3}	Total dopand concentration
ϕ_B	V	Channel surface potential
ϕ^r	V	Position dependent potential drop across the gate stack during recovery
ϕ^s	V	Position dependent potential drop across the gate stack during stress
P	V	Permanent component of the threshold voltage shift
P_{avg}	V	Average permanent threshold voltage shift
P_{max}	V	Maximum of the permanent threshold voltage shift
P_{min}	V	Minimum of the permanent threshold voltage shift
q_1	a.u.	Reaction coordinate of state 1
q_2	a.u.	Reaction coordinate of state 2
q_{12}	a.u.	Difference between reaction coordinates of state 1 and state 2
q_{21}	a.u.	Difference between reaction coordinates of state 1 and state 2
R_{ref}	Ω	Reference resistor
σ_{th}	V^{-1}	Variance of the threshold voltage
τ_c	s	Charge capture time
τ_c^L	s	Charge capture time at low bias
τ_c^H	s	Charge capture time at high bias
τ_e	s	Charge emission time
τ_e^L	s	Charge emission time at low bias
τ_e^H	s	Charge emission time at high bias
τ_p	s	Voltage pulse duration
t_{EOT}	m	Effective oxide thickness
t_f	s	Signal fall time
t_{ox}	m	Oxide thickness
t_{HfO_2}	m	Thickness of HfO_2 layer
t_M	s	Measurement window
t_p	s	Duration of voltage pulse
t_{SiO_2}	m	Thickness of SiO_2 layer
t_r	s	Signal rise time
t_r	s	Recovery time

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$t_{r,max}$	s	Maximum recovery time
t_s	s	Stress time
$t_{s,eff}$	s	Effective stress time
t_{SiCap}	m	Thickness of the Si cap layer
t_{SiGe}	m	Thickness of the SiGe layer
t_{sw}	s	Switching time
ΔU_B	eV	Energy barrier height
U_1	eV	Energy level of state 1
U_2	eV	Energy level of state 2
U_{12}	eV	Energy difference between state 1 and state 2
U_{21}	eV	Energy difference between state 2 and state 1
V_B	V	Bulk voltage
V_{DD}	V	Nominal operation voltage
V_D	V	Drain voltage
$V_{D,off}$	V	Drain voltage of MOSFETs which are not accessed
$V_{D,r}$	V	Drain recovery voltage
$V_{D,s}$	V	Drain stress voltage
$V_{Gp,off}$	V	Gate voltage of pMOSFETs which are not accessed
$V_{Gn,off}$	V	Gate voltage of pMOSFETs which are not accessed
V_{GS}	V	Gate voltage
$V_G^{\downarrow}$	V	Down sweep of the gate voltage
$V_G^{\uparrow}$	V	Up sweep of the gate voltage
V_G^{ov}	V	Gate overdrive voltage
$V_{G,r}$	V	Gate recovery voltage
$V_{G,s}$	V	Gate stress voltage
V_i	V	Input voltage
V_{max}	V	Maximum voltage
V_{off}	V	Offset voltage
V_{out}	V	Output voltage
V_p	V	Voltage of voltage pulse
V_{ref}	V	Reference voltage
V_S	V	Source voltage
V_{th}	V	Threshold voltage
W	m	MOSFET gate width
x_T	m	Trap spatial position

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Constants

k_B	Boltzmann's constant	$1.380\,662 \times 10^{-23}\,\mathrm{J^{-1}\,K^{-1}}$
q	Elementary charge	$1.602\,189\,2 \times 10^{-19}\,\mathrm{C}$
ϵ_0	Vacuum Permitivity	$8.854\,187\,817 \times 10^{-12}\,\mathrm{F\,m^{-1}}$

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Acronyms

ADC	Analog to Digital Converter
AER	Active Energy Region
aRTN	Anomalous Random Telegraph Noise
BCSUM	Bootstrapping and Cumulative Sum
BTI	Bias Temperature Instabilities
CCDF	Complementary Cumulative Distribution Function
CCU	Current Convert Unit
CDF	Cumulative Distribution Function
CET	Capture Emission Time
CMOS	Complementary Metal-Oxide-Semiconductor
CP	Charge Pumping
CSUM	Cumulative Sum
CV	Capacitance-Voltage
DAC	Digital to Analog Converter
DAU	Data Aquisition Unit
DCIV	Direct Current Voltage
DCU	Device Connector Unit
DFT	Density Functional Theory
DLTS	Deep Level Transient Spectroscopy
DSO	Digital Storage Oscilloscope
DUT	Device Under Test
DW	Double Well
EOT	Effective Oxide Thickness
EPR	Electronic Paramagnetic Resonanz
EEPROM	Electrically Erasable Programmable Read-Only-Memories
ESR	Electronic Spin Resonanz
FET	Field-Effect Transistor
GaN	Galiumnitride
HCD	Hot Carrier Degradation
HEMT	High-Electron-Mobility Transistor
HKMG	High-k Metal Gate
HMM	Hidden Markov Model
HR	Hydrogen Release
LER	Line Edge Roughness

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MGR	Metal Grain Roughness
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOSHEMT	Metal-Oxide-Semiconductor High-Electron-Mobility Transistor
MPE	Multiphonen Emission
MPFAT	Multiphonon-Field-Assisted Tunneling
MSM	Measure-Stress-Measure
nMOSFET	N-Channel MOSFET
NBTI	Negative Bias Temperature Instabilities
NMP	Non-Radiative Multiphonon
OPAMP	Operational Amplifier
OTF	On-the-Fly
PBTI	Positive Bias Temperature Instabilities
PDF	Probability Distribution Function
PGU	Pulse GeneratorUnit
pMOSFET	P-Channel MOSFET
PSU	Power Supply Unit
QM	Quantum-Mechanical
RD	Reaction-Diffusion
RDD	Random Discrete Dopand
RTN	Random Telegraph Noise
RTS	Random Telegraph Signal
SCU	Source Converter Unit
SDR	Spin Dependent Recombination
SiGe	Silicon-Germanium
SILC	Stress Induced Leackage Current
SMU	Source Measure Unit
SRAM	Static Random Access Memory
TAT	Trap Assisted Tunneling
TCAD	Technology Computer Aided Design
TDDS	Time-Dependent Defect Spectroscopy
TMI	Time-Dependent Defect Spectroscopy Measurement Instrument
UFSP	Ultra Fast Single-Pulse
UPS	Uninteruptable Power Supply
VU	Voltage Unit
VLSI	Very Large Scale Integrated

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1 Introduction

At the begin of this thesis a brief introduction into the recent advances of the semiconductor industry is given, starting with the fast progress in device scaling. Afterwards, a short summary of the main reliability issues which have to be addressed in modern transistors is presented. To study the degradation of the device performance, sophisticated measurement methods are required. A short overview of proposed experimental methods is thus discussed next. Due to considerable limitations of conventional available measurement setups, we finally developed our own custom-made measurement instrument. Detailed information on the motivation for our own investigations is finally provided.

1.1. Scaling Trend in Microelectronics

Complementary metal-oxide-semiconductor (CMOS) technology, which combines n- and p-type metal-oxide-semiconductor (MOS) transistors as the basic building blocks for circuits, is the cornerstone of the enormous success of the semiconductor technology which is today present in a vast number of applications, thereby simplifying and enhancing our lives in a variety of ways. During the last decades the challenge for the semiconductor industry was to keep pace with Moore's Law, which predicts doubling of the density of the transistors approximately every two years [1] in order to improve performance and reduce production costs. In addition to the scaling of the width and lengths of the transistors, scaling rules require that the insulating layer is also thinned accordingly. Unfortunately, due to the limited subthreshold slope, the supply voltages cannot be scaled in the same manner as the device geometry without deteriorating the ratio between the on and off currents, see Figure 1.1. Also, the thickness of the insulating layer has to be kept above a certain critical thickness in order to avoid excessive leakage currents. As a consequence, the electric fields inside the devices have increased considerably over the last decades. To overcome this detrimental trend, alternative dielectric materials are required. Therefore, gate stacks using high-k materials together with metal-gate contacts have been introduced and are commonly used in state-of-the-art devices. A typical high-k gate stack consists of a Hafniumoxide (HfO_2) layer

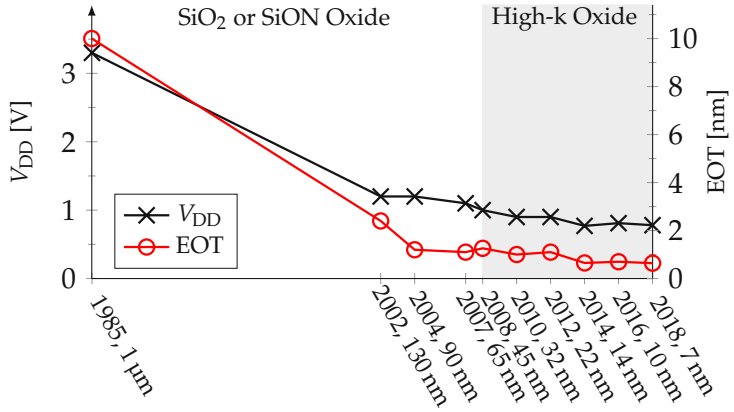

Figure 1.1: The trend of the nominal operating voltage V_{DD} and the effective oxide thickness EOT over the recent years and the associated technology nodes is shown. As can be seen, V_{DD} does not scale in the same as the EOT does. To hold the gate leakage current at nominal operating conditions under technology relevant values high-k gate stacks are commonly used in devices since 2008 (the technology dependent parameters are taken from the ITRS reports from 2001, 2007 and 2013).

on top of an SiO_2 interfacial layer [2, 3, 4, 5]. The equivalent SiO_2 oxide thickness effective oxide thickness (EOT) for such a gate stack is given by the relation

$$t_{EOT} = t_{SiO_2} + \frac{\epsilon_{SiO_2}}{\epsilon_{HfO_2}} t_{HfO_2} \tag{1.1}$$

with the layer thicknesses t_{SiO_2} and t_{HfO_2}, and the permitivities ϵ_{SiO_2} and ϵ_{HfO_2} of the SiO_2 and HfO_2, respectively. High-k gate stacks are nowadays common for planar devices integrated in high-performance complementary metal-oxide-semiconductor (CMOS) applications. To further enhance the performance of CMOS applications the use of high mobility channels is considered [6, 7]. This can be achieved for instance by introducing a SiGe channel which has a higher mobility than the conventionally used silicon, thereby resulting in larger on currents.

1.2. Variability and Yield

During the device fabrication process variations between seemingly identical devices are unavoidable. As such process variations cause a deviation of the device behavior from its ideal characteristics they can have a detrimental impact on the performance of single devices and circuits [8]. In this context, the yield, defined as [9]

$$\text{Yield} = \frac{\text{number of devices which work properly}}{\text{number of fabricated devices}} \tag{1.2}$$

is also seriously affected by these variations [9]. Inherently, the yield can be further considered in terms of failure-types, classified into [10]

(i) catastrophic yield losses, hypernym for all chips which do not work due to functional failures, and

(ii) parametric yield losses, covering all devices which are properly operating, but however, do not meet certain power or performance criteria.

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The process variations, referred to as time-zero device variability, are considered contributors to parametric yield losses, are distributed across the wafer and are unavoidably introduced because of a limited controlability of the fabrication process [11]. They can be classified into [12]

(i) local and random variations within a die or within a single structure with only a few transistors,

(ii) variations across a single wafer due to inhomogeneities during processing, and

(iii) variations between different wafers in a lot due to changing processing conditions during the manufacturing process.

Fluctuations in the surface roughness and thickness of patterned structures contribute to line edge roughness (LER) and are the cause of a stochastic variation of the device geometry [13]. The metal grain roughness (MGR) has to be considered in high-k transistors, as these devices require a metal gate contact on top of the high-k dielectrics. Because the work-function of the metal layer depends on the orientation of metal grains random variations of the threshold voltage are introduced [14]. Random discrete dopands (RDDs) play a very important role in scaled transistors as the random placement of the small number of dopand atoms available in such devices causes fluctuations of the threshold voltage of more than tens of millivolt [15, 16, 17, 18]. The impact of the random discrete dopand (RDD) fluctuations on the standard deviation of the threshold voltage σ_{th} can be approximately expressed by an analytic function [19]

$$\sigma_{\text{th}}^2 \approx \sqrt[2]{4q^3\epsilon_{\text{Si}}\phi_{\text{B}}}\left(\frac{t_{\text{ox}}}{\epsilon_{\text{ox}}}\right)^2 \frac{\sqrt[2]{N_{\text{tot}}}}{W \times L} \tag{1.3}$$

with ϕ_{B} the surface potential and N_{tot} the doping concentration. Most important, σ_{th} depends on oxide thickness t_{ox} and the total dopand concentration N_{tot}. Further examples for process variations are annealing effects and lithographic limitations [19, 11, 20].

In general, the variation of the physical parameters constraints systematic and random contributions. Assuming these to be statistically independent, the total variance is obtained as [21, 22, 23, 24]

$$\sigma_{\text{var}}^2 = \sigma_{\text{rand}}^2 + \sigma_{\text{syst}}^2 \tag{1.4}$$

with the variances of the and random and systematic components σ_{rand}^2 and σ_{syst}^2, respectively. However, to account for the constituents properly they have to be isolated and characterized independently of each other, which can be very difficult [11].

1.3. Non-Ideal Transistor Structures

A conventional n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) is shown in Figure 1.2. Such devices consist of a poly-Si gate on top of the SiO_2 insulator. However, imperfections of the ideal SiO_2 are introduced either during device fabrication or due to interfaces between different materials. These deviations from the ideal atomic structure can lead to electri-

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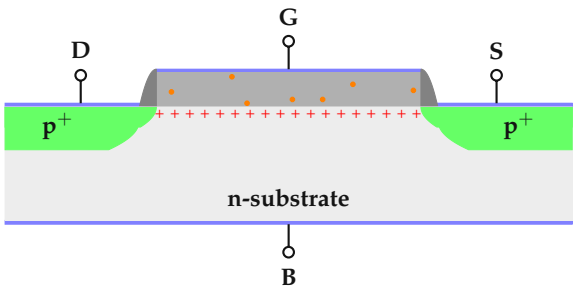

Figure 1.2: Schematic of a conventional p-channel MOSFET with a SiO_2 gate dielectric is shown. When a negative gate bias is applied a conducting channel is formed at the interface between the oxide and the substrate (red signs). Additionally, some defects due to imperfect atomic structure of the oxide are shown (orange dots).

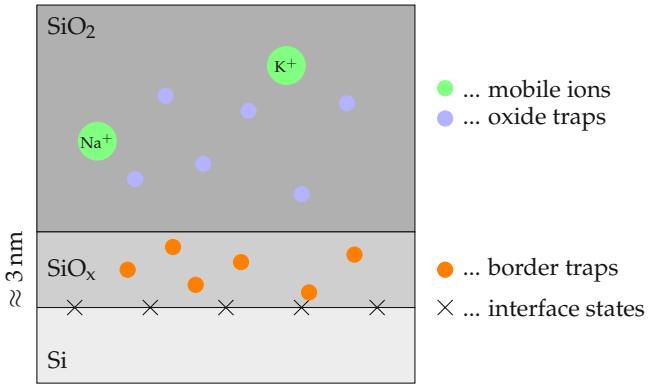

Figure 1.3: The schematic of the SiO_2/Si systems shows the different types of charges, after [25].

cally active sites considered as charge traps in MOS structures. In the commonly used terminology traps occurring in thermally grown SiO_2 are classified into [25, 26]

- fixed oxide charges, due to structural defects in the SiO_2 near the SiO_2/Si interface,
- mobile ionic charges, due to impurities,
- oxide trapped charges, due to trapped charges in the SiO_2,
- border traps, which are defined to be located within the first $\approx 3\,\text{nm}$ of the SiO_2, and
- interface states, a consequence of the lattice mismatch between crystalline Si bulk and the amorphous SiO_2 insulator.

This phenomenological classification is shown in Figure 1.3. The thickness of the gate dielectric layers of modern transistors is below 3 nm, a consequence of the scaling of device geometries into the sub-nanometer regime. Thus traps in the oxide are commonly referred to as border traps. The border traps and interface states are both the most prominent point defects responsible for aging of the MOSFETs.

In Figure 1.4 the $I_{DS}(V_{GS})$ characteristics of an ideal defect-free and a fabricated n-channel MOSFET (nMOSFET) are compared. As can be seen, both devices differ in their threshold voltage, sub-threshold slope and *on* current. The shift of the threshold voltage is caused by border traps, whereas the interface states are responsible for the reduction of the sub-threshold slope, as they de-

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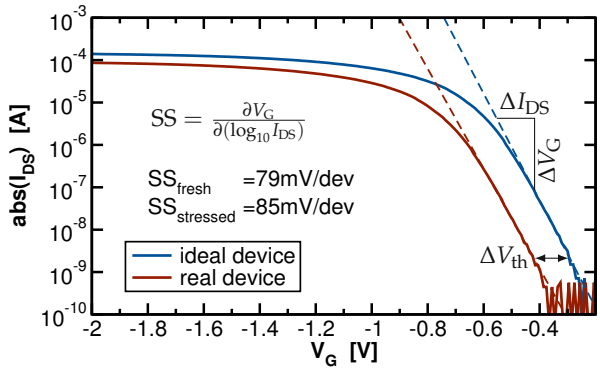

Figure 1.4: The $I_{DS}(V_{GS})$ characteristics of an ideal pMOSFET is compared to the $I_{DS}(V_{GS})$ characteristics of a real nMOSFET. The various charges and traps shift of the threshold voltage. Furthermore, a reduced subthreshold-slope (SS) and a reduced *on* current is a consequence of interface states and border traps.

grade the channel mobility. These charges $\rho(x)$, are distributed through the oxide and determine the total threshold voltage shift [27, 28]

$$\Delta V_{\text{th}} = -\frac{1}{C_{\text{ox}}}\frac{1}{t_{\text{ox}}}\int_{t_{\text{ox}}} x\rho(x)dx. \tag{1.5}$$

C_{ox} the oxide capacitance per unit area and $t_{\text{ox}}$the oxide thickness. The average ΔV_{th} produced by N negatively charged traps approximated using the charge sheet approximation is

$$\Delta V_{\text{th}} = \frac{qN}{C_{\text{ox}}}. \tag{1.6}$$

Furthermore the ΔV_{th} accumulated during bias temperature instabilities (BTI) stress can be expressed in terms of a change of the oxide and interface charges ΔQ_{ox} and ΔQ_{it}. For the interface charges the charge capture and emission is assumed to be very fast. Thus the charge associated with these states follows the Fermi-level directly and can be expressed by [29]

$$\Delta Q_{\text{it}}(t) = q_0 \int \Delta D_{\text{it}}(E_{\text{T}}, t) f(E_{\text{F}}, E_{\text{T}}, t) \text{d}E_{\text{T}} \tag{1.7}$$

with $\Delta D_{\text{it}}(E_{\text{T}}, t)$ the time-dependent density of interface states and $f(E_{\text{F}}, E_{\text{T}}, t)$ their occupancy. When a large negative bias temperature instabilities (NBTI) stress bias is applied the Fermi-level is close to the valence band edge which corresponds to $f(E_{\text{F}}, E_{\text{T}}, t) \sim 1$. As a consequence all interface states which are generated during stress become charged. In contrast to the fast charge transitions associated with interface states, the charging and discharging of oxide traps has considerable larger transition times. As in that case the occupancy cannot directly follow the Fermi-level the oxide charge is given by [29]

$$\Delta Q_{\text{ox}}(t) = q_0 \iint \Delta D_{\text{ox}}(x, E_{\text{T}}, t) f_{\text{ox}}(x, E_{\text{T}}, t)(1 - x/t_{\text{ox}}) \text{d}x\text{d}E_{\text{T}} \tag{1.8}$$

with $\Delta D_{\text{ox}}(x, E_{\text{T}}, t)$ the spatially dependent density of oxide traps and $f_{\text{ox}}(x, E_{\text{T}}, t)$ the corresponding occupancy. Note that the impact of a single charge on $\Delta Q_{\text{ox}}(t)$ strongly depends on the position of the oxide trap. The closer the trap is located to the channel, the larger the impact of the trap on the $\Delta Q_{\text{ox}}(t)$, and implicitly on the threshold voltage, is.

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Finally, the contributions of the interface states and oxide charges to the total threshold voltage shift can be summarized to

$$\begin{aligned}\Delta V_{\text{th}} &= -\frac{\Delta Q_{\text{ox}} + \Delta Q_{\text{it}}}{C_{\text{ox}}} \\ &= -\frac{q(\Delta N_{\text{ox}} + \Delta N_{\text{it}})}{\epsilon_{\text{r}}\epsilon_0} t_{\text{ox}}\end{aligned} \tag{1.9}$$

with the corresponding trap densities. The time-dependent $\Delta V_{\text{th}}(t)$ directly follows from changes of the interface trap density and oxide charge density. Such charging and discharging interactions are dynamic processes and can be describe statistically, see Section 4.

1.4. Defect Candidates

Although a lot of effort has been put into studying point defects in SiO_2/Si material systems, their exact microscopic picture is still controversial. To provide chemical information about the defect, electronic spin resonanz (ESR) measurements appeal to be the most promising method. The ESR, also frequently referred to as electronic paramagnetic resonanz (EPR), is a well-established method to study materials showing unpaired electrons. When an atomic structure is exposed to a magnetic field, the energy levels of the paired electrons are splitted proportional to the magnetic field. An unsaturated electron, however, can move between the two discrete energy levels by absorbing a photon, provided by microwaves typically in the range of $9-10\,\text{GHz}$. The absorbed energy can be measured and further analyzed [30, 31, 32, 33]. Theoretical information on the atomic structure of possible defect configurations in the insulator is obtained from ab initio atomistic simulations using density functional theory (DFT).

The most prominent candidate for defects in SiO_2 is the so-called oxygen vacancy, referred to as E' centers. By using ESR, E' centers have been identified as hole traps in pMOSFETs [31, 34, 35]. Of particular interest in our context is the suggestion that there are possibly two stable atomic configurations of the E' center, namely the dimer and the so-called puckered configuration [36]. In a defect-free crystalline SiO_2 structure each silicon atom is bonded to four neighboring oxygen atoms. A missing oxygen atom is compensated by a covalent bond between two silicon atoms. This configuration is referred to as the dimer configuration and shown in Figure 1.5 (state 1). In the neutral dimer configuration the covalent bond can be weakened by capturing a hole. Furthermore, the positions of the two silicon atoms are slightly displaced relative to each other from their equilibrium positions, see Figure 1.5 (state 2'), and can further transit to the puckered configuration. The so called puckered configuration has the silicon atom bonded with an oxygen atom located at the back of the defect, see Figure 1.5 (state 2). The broken bond of the other silicon atom is neutralized by the remaining electron and both structures are dislocated from their equilibrium positions, thus leading to a charged puckered configuration. The detailed electronic structure behind the defects is calculated using DFT and shown in Figure 1.6 for the oxygen vacancy [37].

Some recent studies have suggested defects involving hydrogen bonds as defect candidates [40, 41]. In thermally grown SiO_2 insulators a considerable amount of process-related interstitial hydrogen is available, supporting the presence of such defects for instance in the hydrogen bridge

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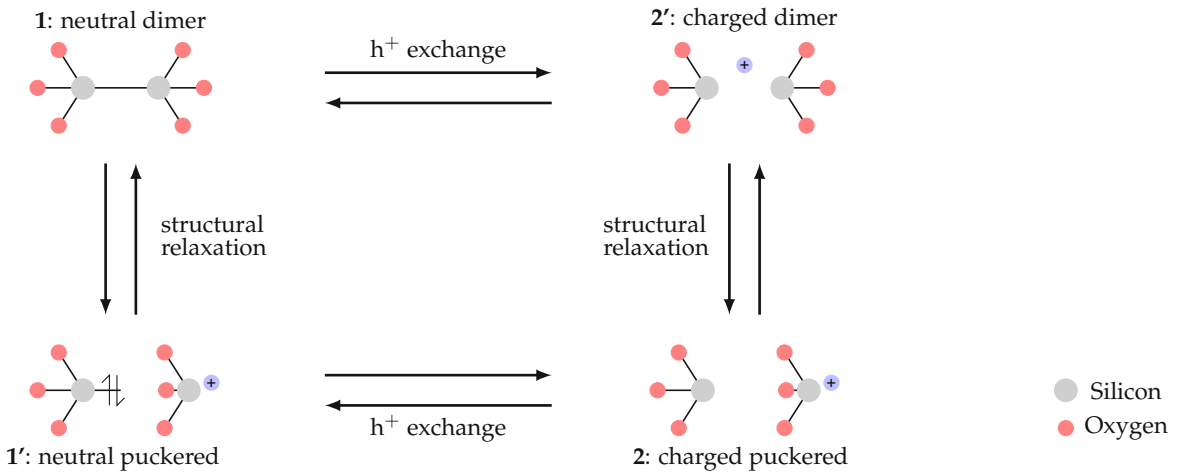

Figure 1.5.: In the neutral dimer configuration a covalent bond exists between two silicon atoms. After hole capture the dimer configuration becomes positively charged and the atoms are slightly displaced from their neutral equilibrium position. The charged dimer configuration can now be neutralized by hole emission, i.e. electron capture, or can relax into the puckered configuration. Additionally, the different states of the shown E′ center are numbered according to the four-state NMP model, see Section 4.3.3.

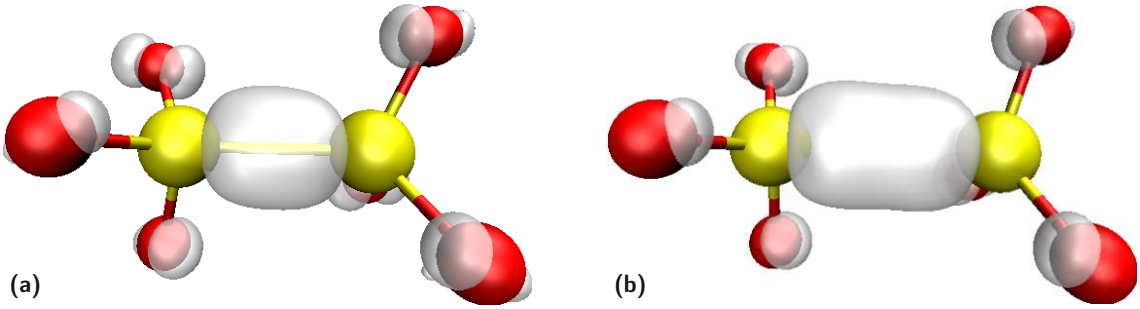

Figure 1.6.: The DFT calculations for the oxygen vacancy in the **(a)** neutral dimer configuration and the **(b)** positively charged dimer configuration, after [38, 39, 37].

configuration. The configuration of the hydrogen bridge is obtained by introducing a hydrogen atom as the connecting link between the two silicon atoms of the E' center configuration, see DFT calculations in Figure 1.7.

Another promising candidate for border traps is the hydroxyl E' center. Recent investigations have shown a good agreement between experimental data and DFT calculations of this particular defect structure [MWC16]. The four states of the hydroxyl E' configuration are shown in Figure 1.8.

In addition to border traps, interface states, commonly associated with P_b centers, play a considerable role in MOSFET devices [42, 31, 34]. There are several types of P_b centers available at SiO_2/Si interfaces depending on the crystal orientation of the interface. In (111) orientated SiO_2/Si interfaces only one type P_b centers is available whereas in (100) orientated SiO_2/Si interfaces two configurations, know as P_{b0} and P_{b1} centers, are present [43]. All types of P_b centers are of an amphoteric nature. Their density of states distributions comprise two disjunct peaks, one in the

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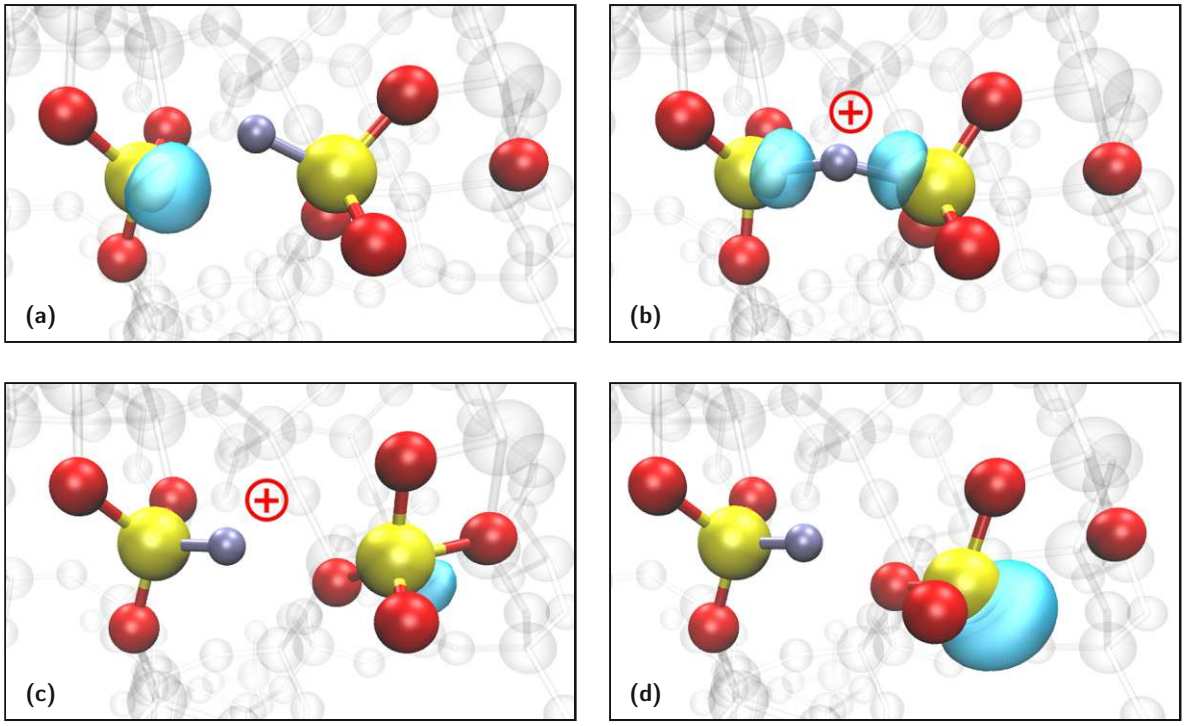

Figure 1.7.: The four states of the hydrogen bridge: **(a)** In the initial configuration, H (silver) sits between two Si atoms (yellow) which themselves are surrounded by three O atoms (red). The electron density of the localized Kohn-Sham-eigenstate is shown as turquoise 'bubbles'. **(b)** *Upon hole capture* the defect can go into the positively charged configuration, where the Si atoms move closer together. **(c)** The stable positive state is shown where the right Si has moved through the plane of its three O neighbors, forming a puckered configuration by bonding to the O in the far right. **(d)** The defect is neutralized but remains in the puckered configuration [MWC16].

lower half and one in the upper half of the band gap [44]. Depending on their trap level an interface state can be considered a donor-like trap in case of $E_T < E_F$, or an acceptor-like trap when $E_T > E_F$. The possible charge states are given by

$$P_b + h^+ = P_b^+$$
$$P_b^+ + e^- = P_b$$

and

$$P_b^- + h^+ = P_b$$
$$P_b + e^- = P_b^-$$

for donor-like and acceptor-like traps, respectively.

1.5. Reliability

With the aggressive scaling of the device dimensions, reliability challenges such as bias temperature instabilities (BTI), hot carrier degradation (HCD) or stress induced leakage current (SILC)

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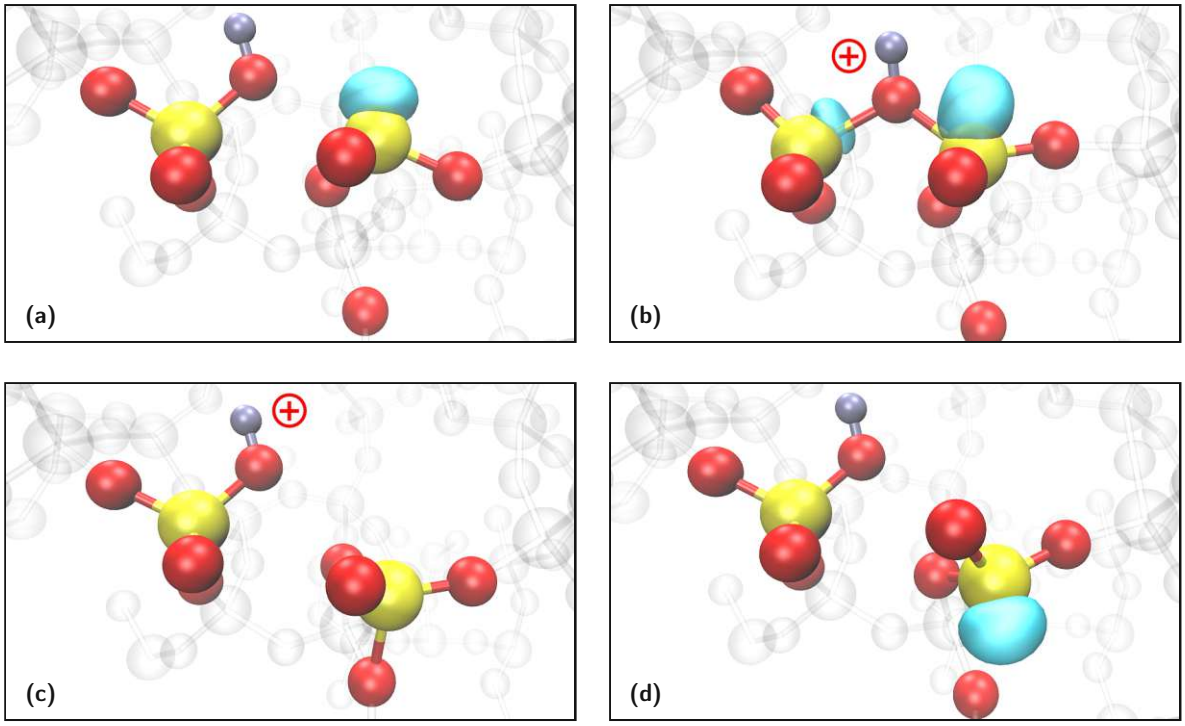

Figure 1.8.: The four states of the hydroxyl E' center: **(a)** In the neutral configuration, a hydroxyl group sits at the left Si while the other carries a dangling bond. **(b)** After hole capture the dangling bond has lost its electron and reforms the Si-O-Si bridge, resulting in the typical proton sitting on a bridging O. **(c)** The right Si moves through the plane of its O neighbors, forming a bond with the O in its back. **(d)** The dangling bond is restored but points into the other direction [MWC16].

have become more severe. The two former are due to charging and discharging of oxide defects and interface states as well as the creation of new defects. Newly created defects inside the oxide can act as trap assisted tunneling (TAT) centers, thereby increasing the tunneling current through the oxide after device stress. This phenomenon is known as SILC and can cause some difficulties in thin oxides in the context of static random access memory (SRAM) devices [45, 46]. In the worst case only one defect is required to form a tunneling path for electrons from the gate to the channel. This implies that SRAM cells will become unintentionally discharged if the oxides are too thin.

1.5.1. Bias Temperature Instabilities

Back in the 1960s Miura et al. observed an increase of the electron concentration at flat band bias conditions after a MOS structure had been subjected to a positive bias stress. They linked their observation to the presence of vacancies located in the oxide [47]. After this first observation little attention had been paid to this phenomenon for more than 30 years until the introduction of nitrogen into the gate stack to suppress boron outdiffusion, which in turn led to a dramatic increase of this instability. Today this phenomena is well known as the bias temperature instabilities (BTI), and has attracted the interest of the semiconductor industry and researchers alike. As a conse-

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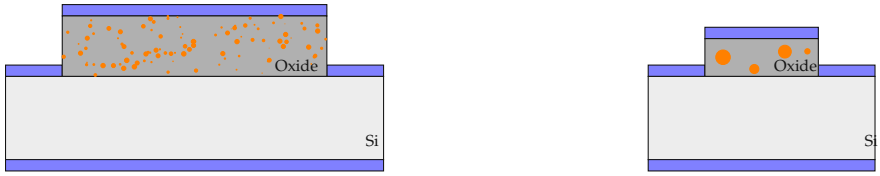

Figure 1.9.: When large-area devices (**left**) are scaled into the nanoscale regime (**right**), the number of defects (symbols) is reduced. However, at the same time the impact of a single defect on the device behavior becomes more pronounced (indicated by the size of the symbols).

quence, a vast amount of literature is available on this topic, which, however, contains numerous contradictory claims, thereby making BTI a highly controversial issue.

The detrimental impact of BTI on the device performance is typically expressed by a shift in the threshold voltage and a degradation of the channel mobility. To a certain extent the performance of both, nMOSFETs and pMOSFETs, is seriously affected by BTI. In this context, the terms positive bias temperature instabilities (PBTI) and NBTI are commonly used and thereby refer to the positive or negative gate bias used in enhancement-mode devices during stress. Regardless of whether the MOSFET is subjected to PBTI or NBTI stress, the defects charged during stress can become uncharged during recovery and thus the device partially recovers on very large time scales. The contribution of each single defect to the total threshold voltage shift therein strongly depends on the device geometry. In large-area devices numerous defects are present, however, their average contribution to the threshold voltage shift is very small, see Figure 1.9 (left), and can not resolved by measurements. Thus a continuous recovery behavior is observed. In nanoscale devices the situation is completely different. Due to the reduction of the device width and length below a few hundred nanometers and the thinning of the gate insulator to approximately 2 nm only a handful of defects exist in these devices, see Figure 1.9 (right). In contrast to their large area counterparts, the contribution of each particular defect, i.e. the charge capture and charge emission processes, can now be resolved by measurements and are visible as discrete steps in the drain-source current. Thus the charge trapping kinetics of single defects can be studied in detail, as it is done within the framework of the time-dependent defect spectroscopy (TDDS), see Section 5.

Furthermore, the impact of BTI strongly depends on the device technology. In the case of conventional SiO_2 oxides, NBTI in p-channel MOSFETs is much more pronounced compared to PBTI on nMOSFETs. Since nitrogen was introduced to fabricate SiON oxides, BTI has became a more severe reliability issue and is observed in both nMOSFETs and pMOSFETs. In high-k gate stacks both phenomena, PBTI and NBTI, play an important role and are currently investigated intensively.

1.5.2. Hot Carrier Degradation

Another important device reliability issue is the degradation of the devices due to hot carriers, known as hot carrier degradation (HCD). In this context the term *hot* refers to the high energy of carriers which are accelerated by the electric field. Such hot carriers can damage the SiO_2/Si

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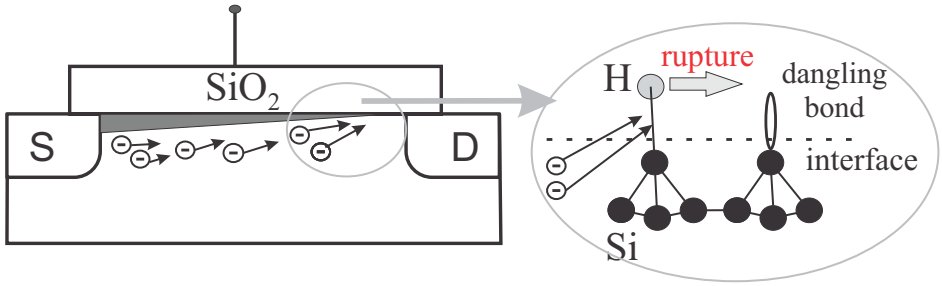

Figure 1.10.: Due to an applied drain-source bias a non-uniform distribution of the electric field along the interface is present in the MOSFET. The carriers are accelerated towards the drain contact and collide with the SiO_2/Si interface. Thereby Si-H bonds can be dissociated and electrical active dangling bonds are created. These bonds can be charged and discharged by carriers captured from the conducting channel and perturb the device electrostatics. As a consequence, the channel mobility is reduced [48].

interface by dissociating neutral Si-H bonds and leaving electrically active dangling Si-H bond behind, see Figure 1.10. There are four main modes of hot carrier stress [49]:

(i) Channel Hot Electron (CHE) Stress: Electrons with energies above a certain threshold are able to trigger a bond dissociation mechanism, which is referred to as single particle (SP) mechanism. This SP mechanism is dominant in large-area devices. However, in nanoscale transistors these carriers do not have sufficient energy to directly create a dangling bond. In such devices the carriers induce a dissociation of the bond by a series of collisions of lower energetical carriers, which is associated with the so called multiple particle process [48]. CHE stress is the most important regime in modern scaled MOSFETs.

(ii) Substrate Hot Electron (SHE) Stress: High bulk voltages cause a large electric field in the substrate which can accelerate carriers from the p-n junction located below the conducting channel towards the insulator interface. Again, if the energy of the carriers is high enough they are injected into the oxide.

(iii) Drain Avalanche Hot Carrier (DAHC) Stress: The channel pinch-off near the drain leads to a high vertical field in this area. The electrons and holes generated by impact ionization can be either injected into the oxide or contribute to a substrate current.

(iv) Secondarily Generated Hot Electron (SGHC) Stress: The SGHC injection originates from impact ionization of carriers generated due to DAHC and are accelerated towards the bulk.

Considering the experimental conditions, the difference between BTI stress and HCD stress is that the former uses $V_{D,s} = 0\,V$ whereas during HCD stress $V_{D,s} \approx V_{G,s}$ or $V_{G,s} \approx V_{D,s}/2$ depending on the channel length is typically used [50, 48]. Furthermore, the impact of HCD is twofold. The interface states generated during stress can capture carriers, become charged and perturb the device electrostatics which leads to a threshold voltage change. Charged defects can also degrade the carrier mobility and hence the drain current.

The initial investigations on HCD where carried out on long channel devices [51] operating at high drain-source voltages. However, in modern nanoscale transistors lower operating voltages

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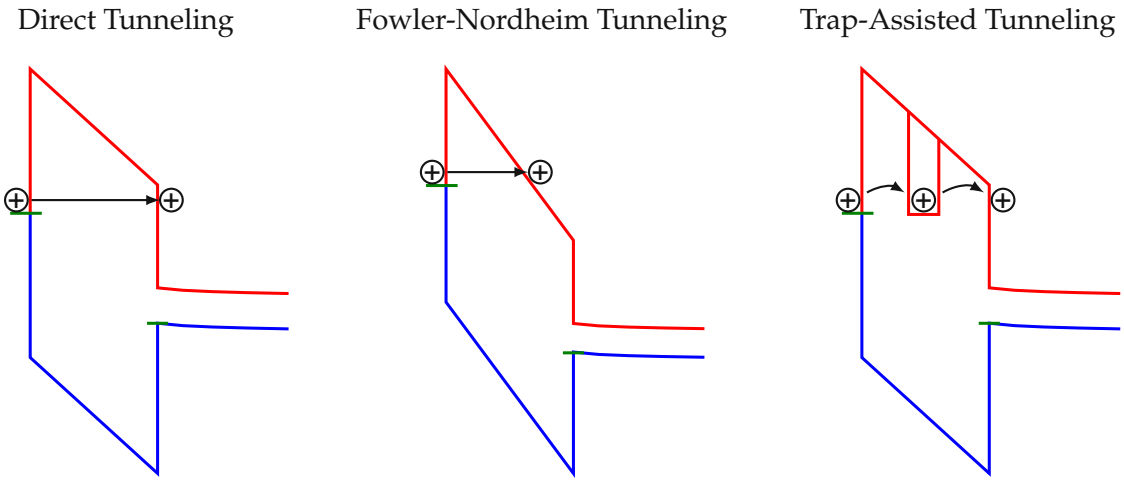

Figure 1.11.: The three main tunneling mechanism which have to be considered in pMOSFETs. (**left**) Direct tunneling and (**middle**) Fowler-Nordheim tunneling [58] describe direct tunneling of a charge carrier through the oxide. (**right**) In contrast, trap assisted tunneling involves two or more steps and is considered to be the main contributor to stress induced leackage current (SILC).

are typically used. Nonetheless, even if hot electrons are unlikely in such nanoscale devices a degradation of device performance due to HCD is observed [52, 53]. As a consequence, the picture of HCD has to be extended to consider the contribution of *cold* carriers [54, 55, 56]. In contrast to hot carriers which can directly create an interface state, the dissociation of the Si-H bond involving cold carriers is stimulated by a series of particles, based on the principle of multiple vibrational excitation [54].

Recent reliability studies in ultra-scaled FinFETs [53] have shown that in these devices BTI still remains a challenge. Furthermore, it has been demonstrated that hot-carrier degradation becomes more pronounced in most recent ultra-scaled MOSFETs. Finally, the situation is made even more complicated due to HCD acceleration by self-heating typical for these 3D transistors [57].

1.5.3. Stress Induced Leakage Current

The faster scaling of the oxide thickness compared to the operating voltage leads to an increase of the oxide fields during normal device operation, resulting in an increased tunneling current. In this context, direct tunneling (DT) which is independent of the electric field for low oxide fields and Fowler-Nordheim tunneling where only a reduced energy barrier has to be passed have to be addressed, see Figure 1.11. In both tunneling mechanisms an electron is able to tunnel directly through the oxide. Note that for Fowler-Nordheim tunneling a reduced tunnel barrier has to be overcome, a consequence of a high gate voltage. Another tunneling mechanism is called trap assisted tunneling (TAT) wherein two or more defects located in the oxide are involved. Such defects are either preexisting or can be created when high electric fields are applied at the gate. The creation of the defects gives rise to stress induced leackage current (SILC), where an increased gate leakage current is measured at low electric fields [59, 60]. This mechanism is particularly im-

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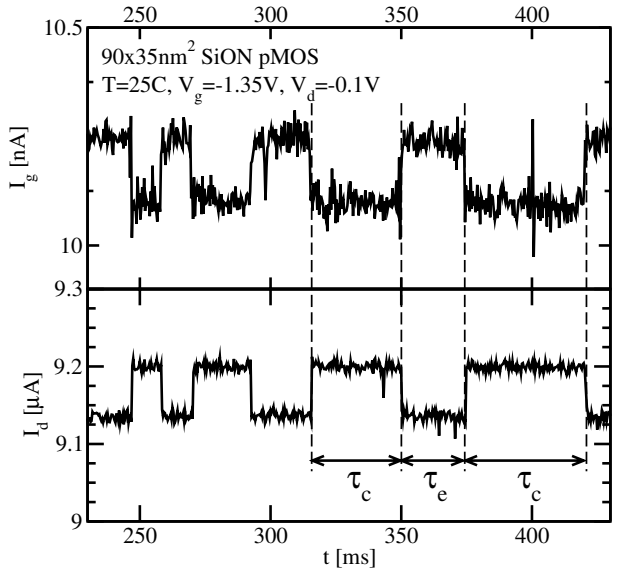

Figure 1.12: The drain and gate currents are simultaneously measured on a nanoscale SiON pMOSFET ($W = 90\,\text{nm}$ and $L = 35\,\text{nm}$). Each discrete step in the measurement data corresponds to either a charge capture or charge emission event of an oxide defect. By comparing the gate and drain currents a clear correlation between the charge transitions is visible, after [64, MWC17].

portant in electrically erasable programmable read-only-memoriess (EEPROMs) where the gate dielectric is repeatedly subjected to high electric fields during writing and erasing cycles. An increase of the gate leakage current at low gate bias conditions triggers self-discharging of memory cells and is therefore mainly responsible for the degradation of the data retention time [61]. As SILC increases with decreasing oxide thickness, it has been identified as one of the main showstopper for further scaling of non-volatile memories [45, 62].

As mentioned previously, charge capture and emission in oxide traps becomes visible as discrete steps in the drain-source current when a device is sufficiently small. Quite remarkably, in such nanoscale transistors discrete charge capture and emission events are also visible in the gate current provided that the oxide is thin enough [63, 64], see Figure 1.12. A decrease in the gate current is sometimes correlated with an increase of the drain current, while sometimes the opposite behavior is seen. The anti-correlation between discrete transitions which can be seen in the gate and drain current is typically observed in SiON pMOSFETs, where a high-level of the drain current can correspond to a low-level of the gate leakage current and vice versa [64], see Figure 1.12. To result in a low-level leakage current, the oxide trap has to be neutral. In this state, the defect does not perturb the surface potential along the conducting channel and hence does not degrade the drain current, leading to the observed high-level of the drain-source current. In contrast, a discrete increase of the gate current causes a discrete step in the drain current towards a smaller value. This observation is related to a hole capture event of the single trap, which then becomes positively charged. Furthermore, the charged trap perturbs the surface potential along the channel and causes the drain current to decrease. When single trap SILC is studied in SiON nMOSFETs, correlated low and high current levels of the gate leakage current and drain current are typically observed [64]. Conversely, in high-k metal gate nMOSFETs anti-correlated charge capture and emission events are visible in the drain-source and gate current [63]. This contradiction requires closer inspection to fully understand the origins of charge trapping causing the correlated and anti-correlated fluctuations of the drain-source and gate current.

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Nonetheless, the repeated charging and discharging of the defect and the correlated changes in the gate current give arise to single defect SILC which is visible in nanoscale devices only. Analogously to classical BTI investigations, in large area devices the vast number of defects and their ultra-small step heights do not allow to identify them individually.

To explain SILC and BTI separately, several models have been proposed recently [65, 66, MWC17, 67]. However, by studying single defect SILC, it has been demonstrated that the same defects are responsible for BTI and SILC [64]. Therefore, to reliably describe the interplay between SILC and BTI, a unified description of charge trapping is required. This can be achieved by using the four-state NMP, which is discussed on Section 4.3.3. As discussed later, this model appears promising to explain SILC and BTI. However, to settle this claim, further investigations are required.

1.6. Defect Centric Perspective

Although modern devices have been dramatically scaled, gate dielectrics with a thickness around 2 nm still contain thousands of atoms. Even with modern computer hardware, the computational effort involved in a direct computation of the electrical properties of the oxide using ab initio methods would be too large. As a consequence, a hierarchical simulation workflow is required for the simulation of BTI and related degradation mechanism affecting devices and circuits. The individual simulation levels are summarized in the defect centric picture [MWJ6], see Figure 1.13. The lowest level uses atomistic simulations such as DFT calculations to study the atomic structure of defects. The first abstraction level focuses on the modeling of the trapping kinetics, i.e. the capture and emission times of single traps, which can be directly measured on each single transistor. With a model explaining the trapping kinetics at hand, device transport models allow to simulate the transistor characteristics considering charge trapping. Based on these simulations, compact models can be derived which can be employed in circuit simulations. The results from the circuit simulations can be further used to study the interplay of complex components, for instance gates, flip-flops and registers, and can be extend to whole applications.

1.7. Measurement Methods and Motivation

As apparently BTI is still not fully understood, the definition of a generalized experimental setup to quantify the BTI induced deviation of the device characteristics from its nominal behavior remains difficult. To measure the impact of charge trapping on the device performance, shifts of the threshold voltage and changes in the subthreshold-slope of the transistors $I_{DS}(V_{GS})$ or changes of the $C(V)$ characteristics are typically investigated. For this, several techniques have been proposed. The developed setups are mostly based on programmable general purpose instruments extended with partly custom-made circuits and configurations to compensate for missing features and circumvent various limitations. In the following sections the methods which have been used to study BTI in various technology nodes are briefly summarized

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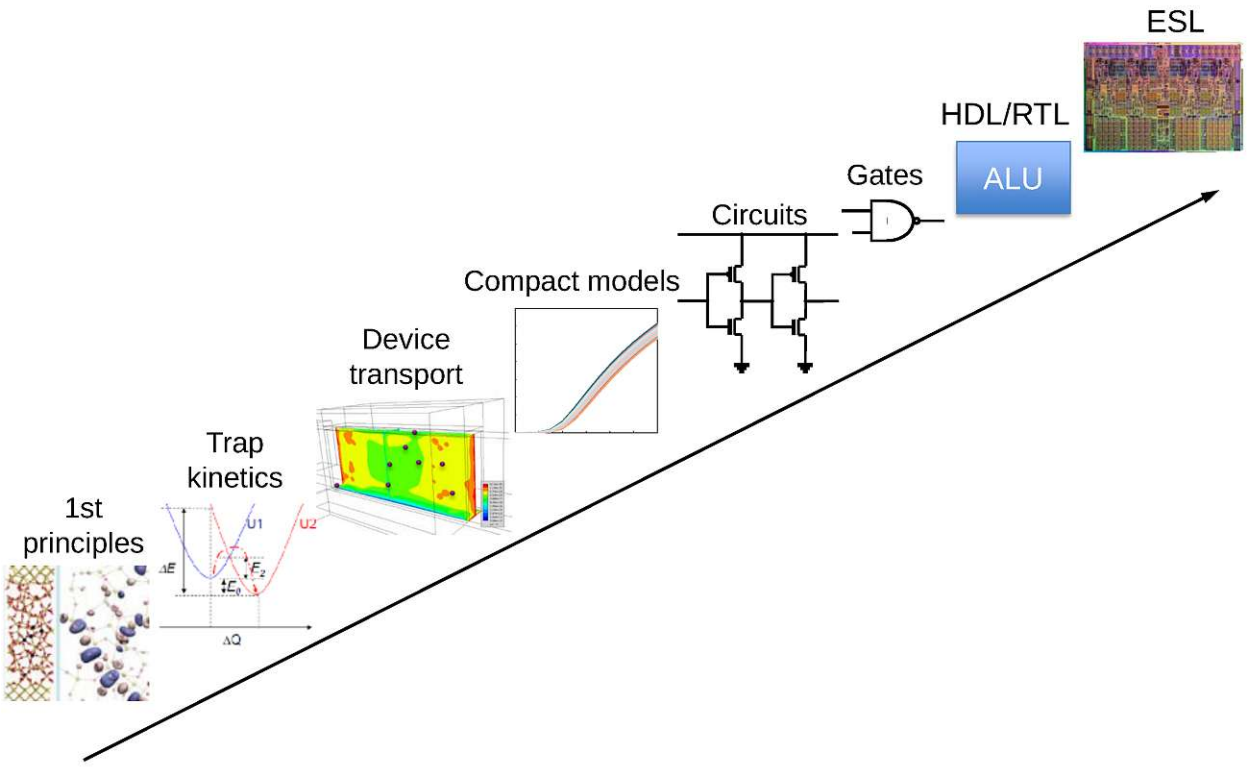

Figure 1.13.: The hierarchy of the defect centric perspective shows how the understanding of BTI at the defect and transistor level can be propagated up to higher levels [MWJ6].

1.7.1. IDVG based Method

One method to study the threshold voltage shift relies on measuring the $I_{DS}(V_{GS})$ characteristics prior and after the device has been stressed. The threshold voltage shift is then calculated as the difference between the gate voltages necessary to achieve the same drain-source current for both $I_{DS}(V_{GS})$ characteristics. For instance, the voltage level corresponding to the maximum of the device transconductance, that is $V_{GS} = V(@\max g_m)$, can be used as gate voltage at which the threshold voltage shift is determined [68, 69]. The advantage of this method is that it can be easily implemented using general purpose instruments. However, the recovery of the device during slow $I_{DS}(V_{GS})$ sweeps leads to an underestimation of the threshold voltage shift. Furthermore, the choice $I_{DS}(V_{GS})$ sweep range is crucial as during such slow voltage sweeps the device may see some stress, particularly for the initial $I_{DS}(V_{GS})$ measured on a fresh device. Conversely, a $I_{DS}(V_{GS})$ ramps starting from accumulation accelerates de-trapping of the trapped charge, and will thereby lead to an underestimation of threshold voltage shift too.

To measure fast $I_{DS}(V_{GS})$ sweeps, the pulse $I_{DS}(V_{GS})$ method was proposed in [70] and further optimized in [71, 72]. It allows to measure complete $I_{DS}(V_{GS})$ characteristics within $\sim 1\,\mu s$, see Figure 1.14. Using the fast pulse $I_{DS}(V_{GS})$ technique threshold voltage shift is reported to be about 10 times and about 4 times larger for pMOSFETs and nMOSFETs, respectively, compared to data extracted from conventionally slow measured DC $I_{DS}(V_{GS})$ sweeps [72].

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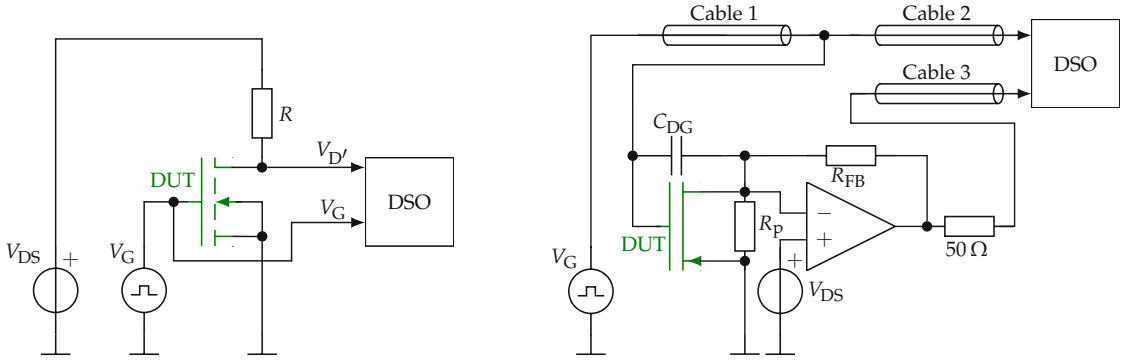

Figure 1.14.: (**left**) The fast $I_{DS}(V_{GS})$ method relies on simultaneous measurement of the voltage at the drain and gate terminal of the transistor using an oscilloscope, after [70]. A change of the drain-source current through the device causes a change of the drain potential which is a consequence of the drain-source current dependent voltage drop at the series resistor. In this configuration BTI affects the drain bias and thus additional delays are introduced as the parasitic capacitances C_{DG} and C_{DS} have to be recharged. (**right**) To further enhance the $I_{DS}(V_{GS})$ sweep time an OPAMP is introduced, after [72]. In this configuration the drain bias is controlled to be constant by the feedback loop of the current-to-voltage converter. The enhanced setup allows to record a full $I_{DS}(V_{GS})$ curve within 1 µs.

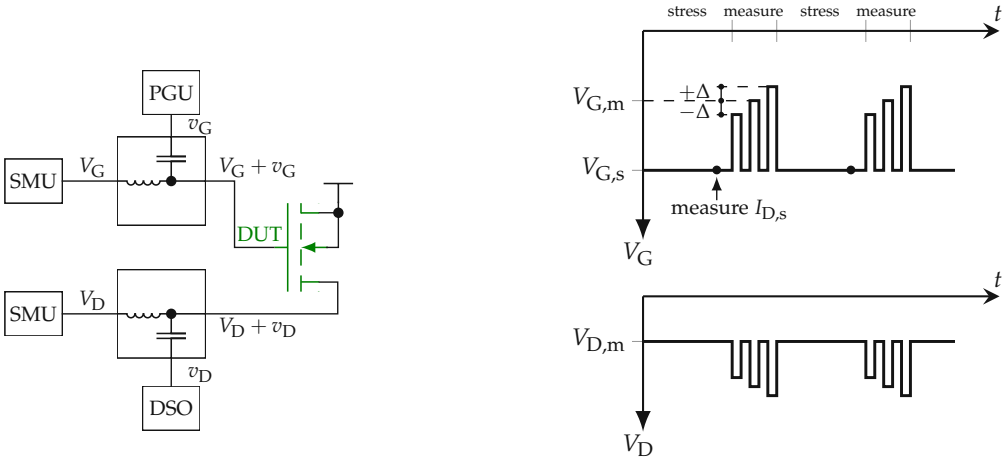

Figure 1.15.: (**left**) The drain and gate biases are generated as the sum of a DC signal, provided by SMUs, and an AC signal, provided from a pulse generator, using a bias-tee. At the drain terminal, the AC current is monitored using a high-speed oscilloscope whereas conventional SMUs are used to measure the DC currents. (**right**) To illustrate the measurement scheme, the corresponding drain and gate biases are shown. The $I_{DS}(V_{GS})$ is recorded by applying a sequence of short measurement pulses with increasing gate bias. Between the measurement pulses the stress biases are applied at both terminals which prevent the device from recovering during the $I_{DS}(V_{GS})$ sweep, after [73].

Based on the pulse $I_{DS}(V_{GS})$ technique an ultra-fast $I_{DS}(V_{GS})$ method has been presented [73, 74], see Figure 1.15. The setup has been realized using Keithley 4200 semiconductor characterization instruments providing the required SMUs and pulse generators. With this technique measure-

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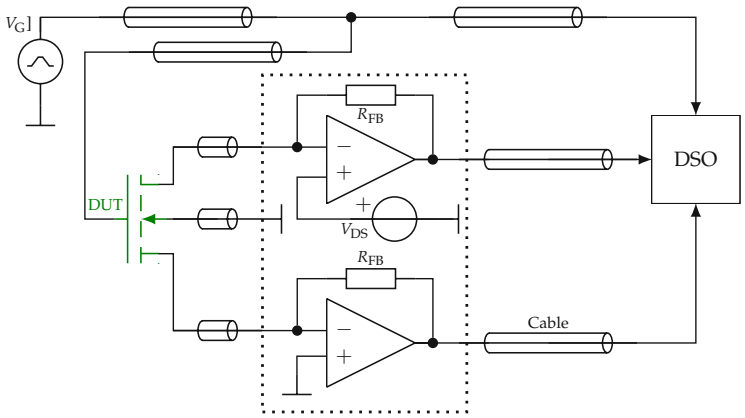

Figure 1.16: A pulse generator provides the trapezoidal voltage pulses required for the UFSP method. The rise and fall time are thereby set to $\sim 3\,\mu s$. Furthermore, the source and drain currents are converted to voltages using custom-designed current-to-voltage converters. To monitor the resulting output and DSO is used, after [75].

ment pulses in the sub 100 ns regime are achieved resulting in a minimized recovery of the device during these pulses.

Although the presented methods allow to characterize BTI, their applicability is limited to large-area devices. This limitation is a consequence of the large current measurement resolution around 2 µA. To properly resolve currents typical in nanoscale transistors a current resolution at least in the sub-nanoampere regime is required.

1.7.2. Ultra Fast Single-Pulse Method

Quite recently, the ultra fast single-pulse method, which employs the split $C(V)$ technique to determine the channel mobility, was presented [75]. Usually, the mobility degradation measurement technique relies on measuring the channel conduction current I_{ch} and a subsequent $C(V)$ characteristics. The effective channel mobility μ_{eff} can then be calculated using the relation [76, 77, 78, 79, 80]

$$\mu_{eff} = \frac{L}{W}\frac{I_{ch}}{V_D Q} \tag{1.10}$$

with Q extracted from the $C(V)$ measurement. Note that the split $C(V)$ technique sets the drain bias to 0 V during $C(V)$ measurements and $V_D \neq 0\,V$ during the $I_{DS}(V_{GS})$ sweep which is necessary to determine I_{ch}. To account for any impact of V_D on the channel mobility and to avoid any rearrangement of the connectors and cables when the $C(V)$ measurement configuration is changed to the $I_{DS}(V_{GS})$ configuration, the ultra fast single-pulse (UFSP) method has been proposed [75], see Figure 1.16.

1.7.3. On-The-Fly Method

To monitor the transient characteristics of the threshold voltage shift $\Delta V_{th}(t)$ the so called on-the-fly (OTF) method was introduced in [81]. To eliminate any recovery-related effects, the stress signal is not interrupted during measurement. In the OTF technique the drain current is typically

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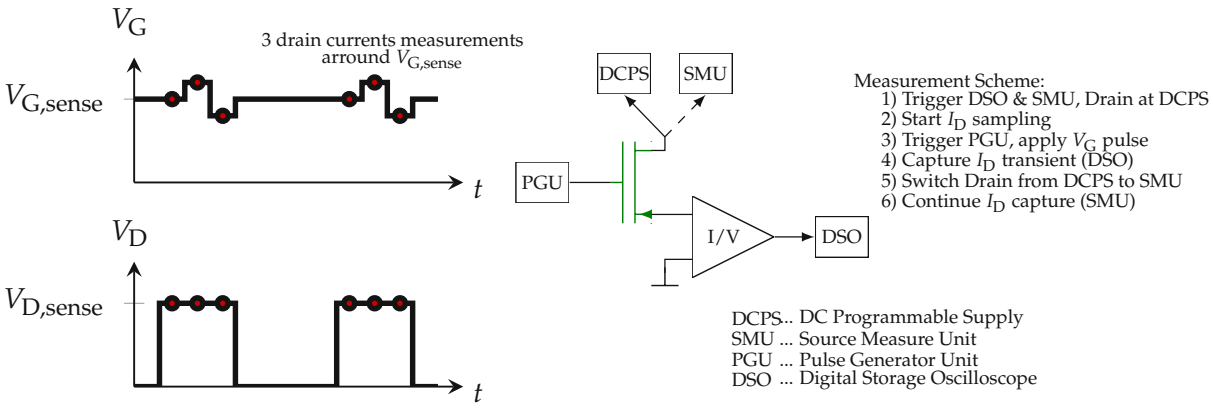

Figure 1.17.: (**left**) The gate voltages used to monitor ΔV_{th} on-the-fly, after [81]. Periodic voltage pulses are applied around the stress bias and the current is measured at each voltage level. During the measurements a small V_D is applied to the device. During stress the drain bias is set to $V_D = 0\,V$. (**right**) As general purpose SMUs are very slow, an additional current-to-voltage converter is added and a digital oscilloscope is used to monitor the drain-source current in the range of $t_r = 1\,\mu s \ldots 30\,ms$, after [82].

recorded in the linear regime, that is $I_{D,lin}$, and measured using periodic pulses around the gate bias, see Figure 1.17 (left). Using the measured $I_{D,lin}$ the threshold voltage shift can be calculated to [83]

$$\Delta V_{th} \approx -\sum_{n=1}^{N-1} \frac{I_{D,lin}[n] - I_{D,lin}[n-1]}{(g_m[n] - g_m[n-1])/2} \tag{1.11}$$

with the estimated transconductance

$$g_m[n] = \frac{I_{DS}[n](V_{GS} + dV) - I_{DS}[n](V_{GS} - dV)}{2dV}. \tag{1.12}$$

Nevertheless, as the measurement delay of general purpose SMUs is pretty large, in [82] an additional current-to-voltage converter connected to a DSO is used to monitor the fast ΔV_{th} recovery by measuring the current through the device at the source terminal of the transistor, see Figure 1.17. Both the SMU and the DSO are synchronized with the pulse generatorunit (PGU) providing the gate bias. By using this configuration a fast measurement delay of around 1 µs is achieved.

1.7.4. Computer Controlled Measure-Stress-Measure Measurements

To perform measure-stress-measure (MSM) experiments the combination of a PCI interface card providing several analog to digital converters (ADCs) and digital to analog converters (DACs), and custom-made current-to-voltage converters were used in [84, 85], see Figure 1.18.

As the setup is designed to investigate several devices simultaneously, the PCI interface requires synchronized DACs to provide the stress and recovery biases and synchronized ADCs to record the output voltage of the current-to-voltage converters. Using this setup controlled stress and recovery cycles with a minimum delay of $\sim 30\,\mu s$ can be achieved.

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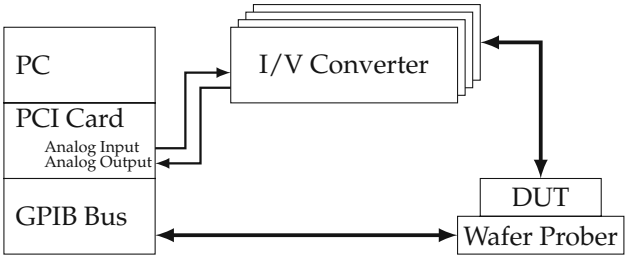

Figure 1.18: To measure several devices simultaneously, a PCI interface providing the biases and ADC to record the output signal of a custom-made current-to-voltage converter can be used, after [84].

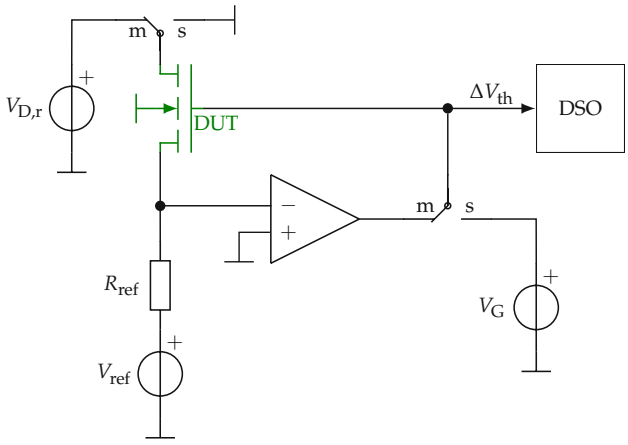

Figure 1.19: The fast V_T method allows to directly measure the threshold voltage shift ΔV_{th}. During stress the switches are put into position 's' and thus the drain bias is held at zero volt whereas the stress bias $V_{G,s}$ is applied at the gate contact. For recovery the switches are in position 'm', providing $V_D = V_{D,r}$ and $V_{GS} = V_{GS}(I_{DS} = I_{ref})$. The latter is achieved using feedback loop and the OPAMP which controls the recovery gate bias, after [87].

1.7.5. Fast-VT Method

The so called *fastVT* method proposed by [86, 87] is a very elaborate technique which allows to directly monitor the threshold voltage shift. The operating principle is shown in Figure 1.19. During the stress cycle the switches are put into position 's', thereby disabling the OPAMP circuit and setting the terminals of the device under test (DUT) to $V_S = V_D = V_B = 0\,V$ whereas $V_{GS} = V_{G,s}$. The recovery conditions are provided by setting the switches to position 'm'. In that case the drain voltage changes to $V_D = V_{D,r}$ and the feedback loop built around the OPAMP is closed. The recovery gate bias $V_{G,r}$ is now controlled by the OPAMP to minimize the current difference between the drain-source current through the device I_{DS} and the reference current given by $I_{ref} = V_{ref}/R_{ref}$. To monitor the threshold voltage shift a combination of a slow sampling unit to record the data for $t_r > 30\,ms$ and a high speed DSO to record the data within $t_r = 1\,\mu s \ldots 30\,ms$ is used. The advantage of this method is that ΔV_{th} data can be directly monitored after the feedback loop setup time, which is typically about $0.5\,\mu s$.

So far the *fastVT* method was successfully used to monitor single charge trapping in nanoscale transistors [88, 89, 90].

1.7.6. Motivation for Custom-Made Measurement Setup

Common to all these different measurement methods is the observation that high speed measurements with sampling times around $1\,\mu s$ can not be achieved with general purpose instru-

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ments. Most of the setups are configured using synchronized combinations of conventional SMUs and pulse generators to provide output voltages and DSOs and SMUs to record the currents. To achieve high measurement accuracy, additional custom-made hardware is typically required. However, the handling of such setups is inconvenient and error-prone but necessary as there is no suitable general-purpose measurement setup available commercially.

In our initial efforts to study charge trapping in nanoscale devices we performed stress and measure experiments using general purpose SMUs. However, it turned out that the measurement delay was too large ($\sim 1\,\text{ms}$) and the threshold voltage shift resolution too low to resolve threshold voltage shifts below $\Delta V_{\text{th}} \sim 3\,\text{mV}$. To overcome both limitations we developed our own measurement setup, called time-dependent defect spectroscopy measurement instrument (TMI). In this context the time-dependent defect spectroscopy (TDDS) refers to the measurement technique proposed to study charge trapping in nanoscale devices, and will be discussed in great detail in Section 5.

Although the main focus during development of the TMI was the study of charge trapping in nanoscale devices, the TMI was also successfully used for the characterization of large-area transistors, and was quite recently used to investigate alternative structures such as Galiumnitride (GaN) high-electron-mobility transistors (HEMTs). A practical side effect of the TMI are the low production costs compared to general purpose instruments and the possibility to modify the configuration individually. For instance, the TMI has been recently configured to control and measure transistor array structures, see Section 11. In this application the TMI replaces three Keithleys and thereby reduces the setup costs by a factor of around 15–20. Furthermore, on the one hand BTI often requires very time-consuming measurements and on the other hand the achieved results have to be confirmed by investigating several identical devices. To achieve this within a reasonable time span, parallization of measurements is required. Due to the manageable costs of the TMI and the flexible adjustment to any setup, the TMI has proven invaluable for the rigorous study of BTI.

In the first part of this thesis, the most important features of BTI are summarized, followed by an introduction of defect modeling. A particular focus will be put onto the four-state NMP model which has by now been successfully used to explain charge trapping on a wide range of technologies. Next, the TDDS is introduced and the design concept and features of the TMI are discussed in greater detail. Then another important aspect, namely the analysis of the collected measurement data is presented. The latter requires elaborate algorithms to analyze equidistant and non-equidistant sampled measurement data. Furthermore, as the contributions of single traps to the total threshold voltage shift can be very small, the separation of capture/emission events from measurement noise requires careful attention. Also the observation of volatile defects, defects producing multiple emission events, and random telegraph noise (RTN) signals have to be studied individually. Finally, recent findings concerning NBTI and PBTI in SiON MOSFETs and PBTI in strained SiGe devices are presented.

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Part I.

Theory

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2

Bias Temperature Instabilities

Bias temperature instabilities (BTI) are one of the most prominent degradation mechanism in modern semiconductor devices and are a serious threat to the performance of n-channel an p-channel MOSFETs. The detrimental impact of BTI on the device behavior can be observed when a large bias is applied at the gate contact of the device. This bias is typically referred to as the stress bias. Furthermore, the device temperature plays an important role in context of BTI. Thus elevated temperatures are used during investigations concerning BTI.

An almost inexhaustible amount of literature is available on this puzzling phenomenon, wherein the controversial origins of the detrimental impact on the device performance are discussed. This chapter provides an overview of BTI, starting with a qualitative description of BTI in various technologies, followed by an introduction of the impact of BTI on the device behavior. Afterwards the consequences of device degradation on circuits are presented, and finally the time-dependent variability is introduced.

2.1. Phenomenological Classification

In general, BTI is classified into positive BTI (PBTI) and negative BTI (NBTI), where the terms *positive* and *negative* refer to the sign of the gate bias. Most commonly NBTI is typically studied in pMOSFETs while PBTI has received more attention in nMOSFETs while NBTI/nMOSFETs and PBTI/pMOSFETs investigations are rather rare because their impact on the device performance is less pronounced. Furthermore, carrying out NBTI/nMOSFETs and PBTI/pMOSFETs experiments is rather difficult, because most test structures contain ESD protection diodes. These diodes are implemented to protect the gate oxide from any unwanted electrostatic discharges. A disadvantage of such ESD diodes is the suppression of large positive/negative gate voltages on pMOSFETs/nMOSFETs thereby making NBTI/nMOSFETs and PBTI/pMOSFETs investigations difficult. However, for the development of a detailed picture of charge trapping, i.e. defect energy

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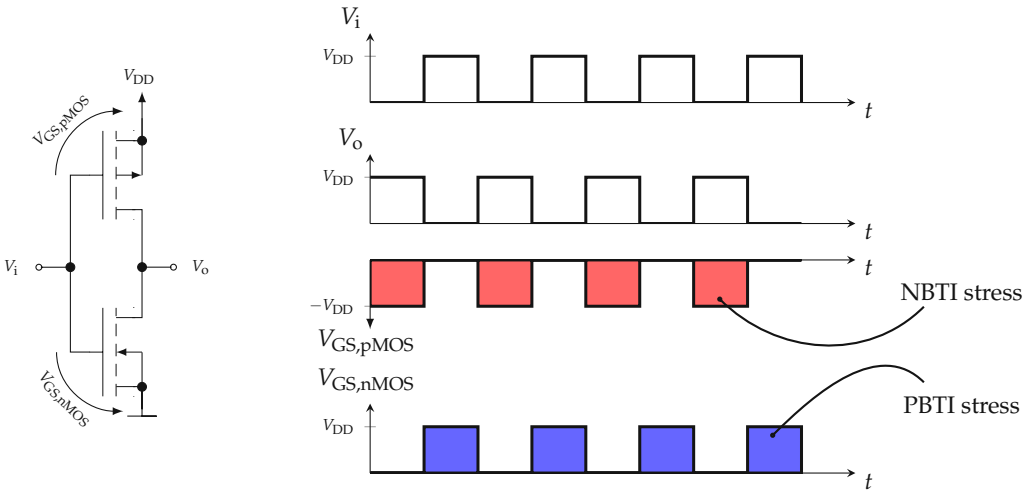

Figure 2.1.: A simple CMOS inverter can be made by connecting one nMOSFET and one nMOSFET in series sharing the gate contact. The input and output voltages are shown as well as the corresponding gate biases. During $V_i = V_{DD}$ the nMOSFET is subjected to PBTI stress whereas the phases with $V_i = 0\,V$ are responsible for NBTI stress of the pMOSFET.

levels and distributions inside gate dielectrics, ideally both NBTI and PBTI have to be carefully analyzed on nMOSFETs and pMOSFETs at the same time.

To illustrate the importance of BTI in modern CMOS applications a simple inverter circuit is shown in Figure 2.1. The inverter uses one pMOSFET and one nMOSFET which are connected in series. At any time one MOSFETs is subjected to BTI stress as both devices are controlled by a common gate terminal. While the input voltage of the inverter is a logical *one*, i.e. $V_{GS} = V_{DD}$, the nMOSFET is subjected to positive bias stress. In contrast, a logical *zero* signal applied at the input, i.e. $V_{GS} = 0\,V$, results in $V_{GS} = -V_{DD}$ at the pMOSFET and is equivalent to negative bias stress of this transistor. As a consequence, NBTI and PBTI are both important phenomena in CMOS applications.

2.2. Impact on Devices

As a consequence of the stress, the following is typically observed, see Figure 2.2:

(i) Shift in the threshold voltage

(ii) Reduction of the transconductance g_m, i.e. the slope of the $I_{DS}(V_{GS})$ characteristics

(iii) Reduction of the on current

The shift in the threshold voltage is typically attributed to oxide defects whereas interface states are often considered the reason for a reduction of the sub-threshold slope.

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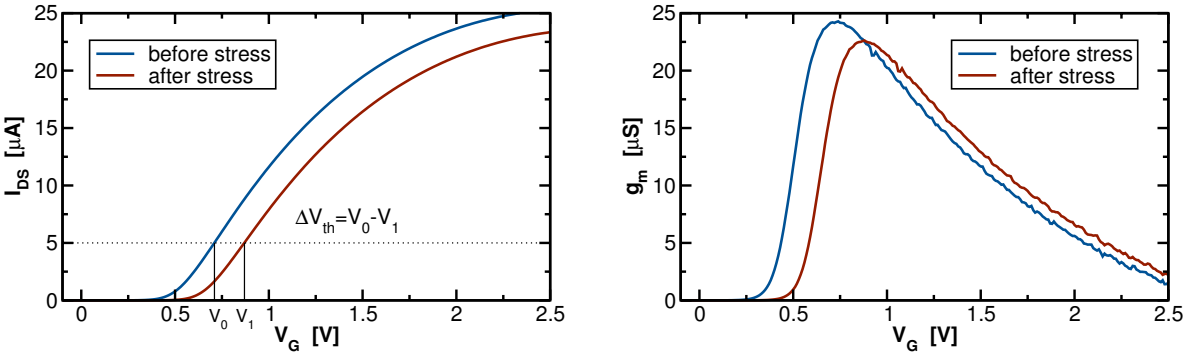

Figure 2.2.: (**left**) When an nMOSFET is subjected to PBTI stress the device threshold voltage changes and the $I_{DS}(V_{GS})$ characteristic is shifted towards larger gate voltages. (**right**) At the same time the transconductance g_m and also the sub-threshold slope becomes smaller.

In the simplest case, the impact of BTI on the device characteristics for different technologies is typically expressed as a threshold voltage shift. While many definitions of the threshold voltage exists, the threshold voltage shift ΔV_{th} is often simply defined as the voltage difference between the gate bias of the unstressed and stressed device required to drive the same drain-source current, as indicated in Figure 2.2. As circuit designs rely on defined thresholds for the device *on* and *off* state, this definition also provides a good indication of the device deviation from its ideal behavior for circuit designers.

The most fundamental problem in experimentally assessing BTI is the fact that the degradation recovers as soon as the stress voltage is reduced. In fact, this recovery can be so strong, that even with a fast measurement using a delay of 1 ms, 50% or more of the degradation is lost. This has dramatic consequences on reliability statements made at nominal operating conditions, which are typically extrapolated from experimental data recorded at higher temperatures and stress biases. An underestimation of BTI at such accelerated test conditions will lead to overly optimistic lifetimes of the devices. Furthermore, to develop models which can be used in device simulators to provide an accurate explanation of BTI a detailed knowledge of the entire stress and recovery characteristics is of utmost importance.

The most common experimental method to measure the threshold voltage shift is to apply a stress gate bias for a certain time and monitor the recovery of ΔV_{th} starting immediately after stress release. In Figure 2.3 typical stress and recovery traces are shown for NBTI/pMOSFET investigations. As can be seen, for nMOSFETs a positive ΔV_{th} is obtained, while the pMOSFETs show a negative ΔV_{th}. In both cases ΔV_{th} often recovers towards $\Delta V_{th} = 0\,\mathrm{V}$. Note that the ΔV_{th} remaining at end of the measurements is often considered a permanent contribution to BTI whereas the other part builds the recoverable component of the threshold voltage shift. Obviously, these two components are ill-defined as they depend strongly on the duration of the recovery period.

As a consequence of the changes in the transistor characteristics, the dynamic response of the transistor will also change. As an example consider a voltage step function applied at the gate contact of a single device, see Figure 2.4. For this simple estimation a realistic switching transient

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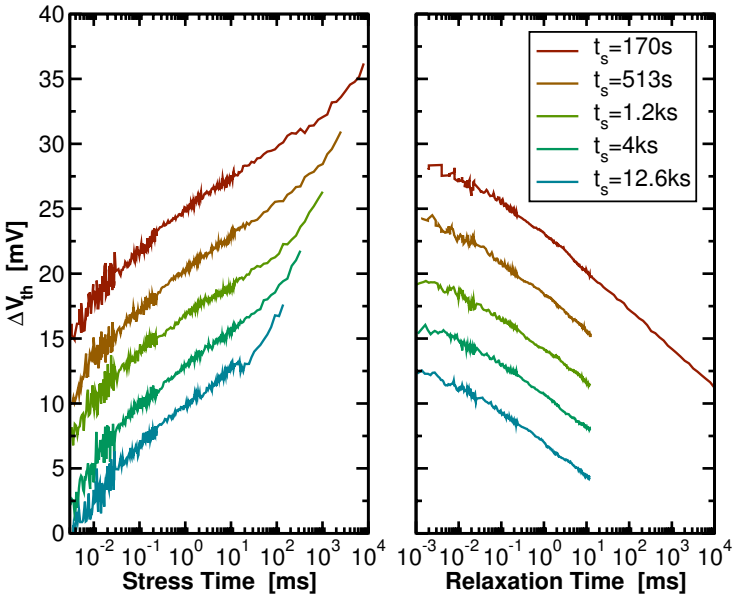

Figure 2.3: Stress and recovery traces recorded on a large-area pMOSFET. As can be seen, the threshold voltage shifts recover towards $\Delta V_{th} = 0\,V$. It has to be noted that a small $V_{D,s}$ has to be applied if BTI needs to be measured during stress in order to measure any drain-source current. However, $V_{D,s}$ has to be kept low in order to avoid HCD related effects. Note that the measurements have been performed using a general purpose instrument. Thus considerable large measurement delays are achieved, after [29, 91, 92, 93, 94].

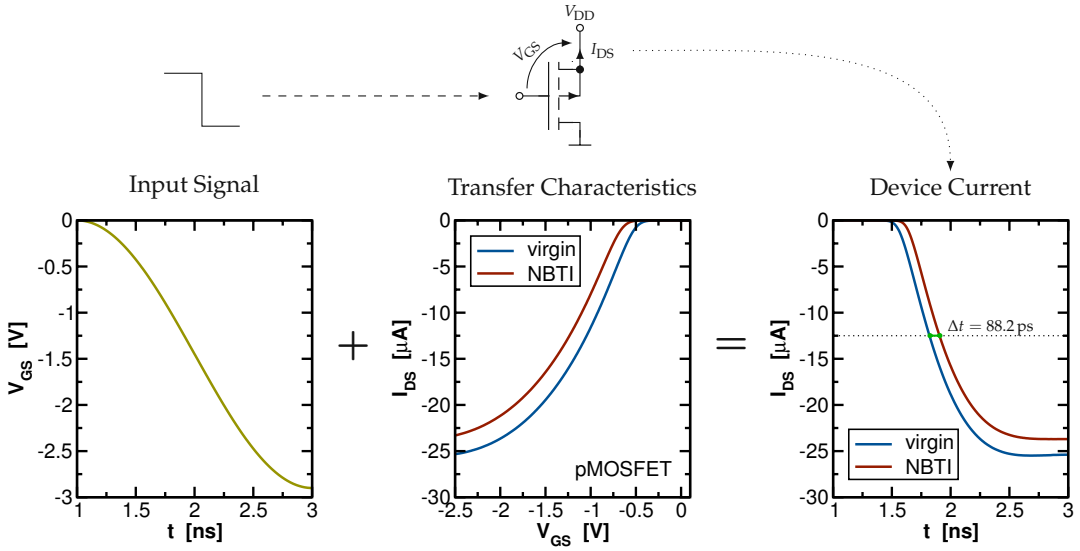

Figure 2.4.: A change in the threshold voltage causes an additional delay in the output signal. In addition, the decreased slope of the $I_{DS}(V_{GS})$ decreases the output signal rise time and thus reduces the operation speed of the transistor. Also a reduced maximum output current is obtained from the pMOSFET affected by NBTI. All measurements have been performed using the TMI.

for the gate voltage step of 3 ns is assumed. As expected, the drain-source current directly follows the abrupt change of the input gate bias. However, considering the changes in the device threshold voltage and sub-threshold slope, a delayed response of the pMOSFET on the gate bias, compared to the virgin device is observed. Furthermore, a decreased on current is visible as a consequence of NBTI, which will increase the charging time of the subsequent inverter stage. Although the aging of this exemplary pMOSFET only leads to an apparently small delay of $\Delta t \approx 88\,ps$, the timing of a large number of devices in high-speed applications can be negatively affected.

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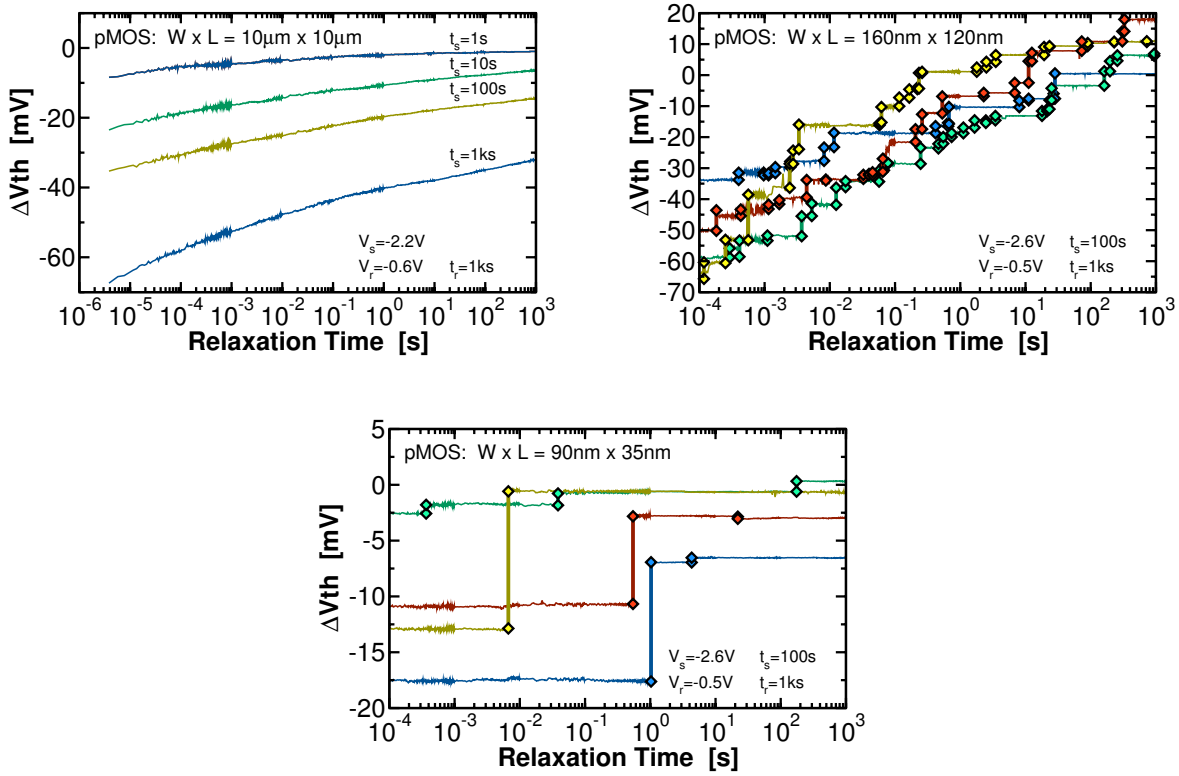

Figure 2.5.: The shown recovery traces are recorded from three different pMOSFETs with **(top left)** $W \times L = 1\,\mu\text{m} \times 1\,\mu\text{m}$, **(top right)** $W \times L = 160\,\text{nm} \times 120\,\text{nm}$ and **(bottom)** $W \times L = 9\,\text{nm} \times 70\,\text{nm}$. In contrast to the large-area device, the recovery of the nanoscale transistors proceeds in a discrete manner with numerable amount of steps, a consequence of the device scaling.

2.3. Consequences of Device Scaling on Bias Temperature Instabilities

To study BTI devices are repeatedly stressed and the transient recovery behavior is subsequently recorded an analyzed. While the recovery traces obtained from large-area devices show a continuous characteristics, see Figure 2.5 (left), the nanoscale MOSFETs show discrete steps in the recovery traces, see Figure 2.5 (middle) and Figure 2.5 (right). It has to be noted, that the smaller the gate area gets the larger the observed ΔV_{th} shift of the single charge emission events gets. The latter observation can not be approximated with a simple power law. The transient behavior can be deduced to a strong geometry depended active number of traps N_{T} and a geometry dependent average step height of single defects η. It has been found that the number of traps decrease with the device area $N = N_{\text{T}} \times A$, whereas the impact of each single trap gets more pronounced $\eta = \eta_0 / A$. As a consequence, the same traps are responsible for BTI in large-area and nanoscale devices and thus the total threshold voltage shift can be modeled as the sum of N independent transitions, i.e. defects, with different impact on the ΔV_{th}. Each single defect can be clearly identified by its capture time τ_{c}, emission time τ_{e} and its step height. The defect can either be neutral or

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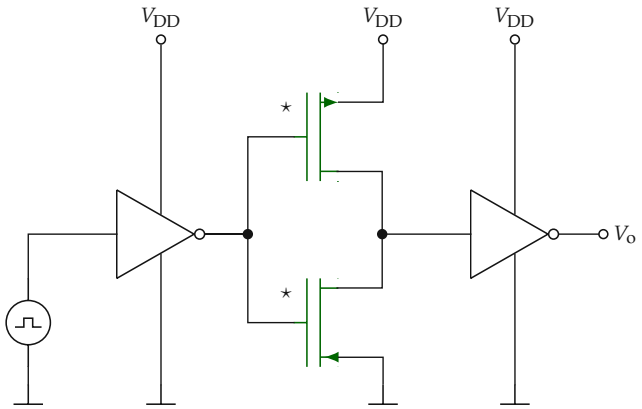

Figure 2.6: The inverter consist of a three stage chain where only the inverter stage in the middle is considered to degrade, after [95].

charged depending on whether a low or high gate bias is applied. Thus each charge state can be described by its characteristic capture and emission times τ_c^L and τ_e^L or τ_c^H and τ_e^H, respectively.

2.4. Impact of Bias Temperature Instabilities on Circuits

In the following the consequences of BTI on a three stage inverter circuit is discussed. The corresponding circuit is shown in Figure 2.6 where the two MOSFETs of the middle inverter stage are considered to be small enough so that the impact of single defects becomes important. To simulate the transient behavior of the three stage inverter chain, SPICE simulations using compact models for each device are performed [95]. The compact model for the inverter stage in the middle of the schematic in Figure 2.6 is thereby extended to consider time dependent threshold voltage shifts induced by single defects. For simplicity the compact model introducing the complex capture and emission time dependence of single defects on the gate bias $\tau_c(V_{GS})$ and $\tau_e(V_{GS})$ is reduced to four time constants at low and high gate bias, τ_c^L, τ_e^L, τ_c^H and τ_e^H, which is a good approximation for digital circuits. In this model the probability of a defect to capture or emit a charge is described by [95]

$$P_{c,e}^{L,H} = \frac{\tau^{L,H}}{\tau_{c,e}^{L,H}} \left(1 - e^{-\frac{\Delta t}{\tau^{L,H}}}\right) \tag{2.1}$$

using the relation

$$\frac{1}{\tau^{L,H}} = \frac{1}{\tau_c^{L,H}} + \frac{1}{\tau_e^{L,H}} \tag{2.2}$$

where the indices 'c' and 'e' express the capture and emission process and the superscripts 'L' and 'H' denote either low or high gate bias. The presented formalism also allows to consider RTN signals and also slow defects which are typically assigned to BTI.

The transient simulation evaluated at two different times for an input signal with frequency $f = 250\,\text{MHz}$ is shown in Figure 2.7. As can be seen in the transient device threshold analysis after $t = 10^{-8}\,\text{s}$, two fast RTN defects capture a charge at low gate bias and emit their charge at high gate

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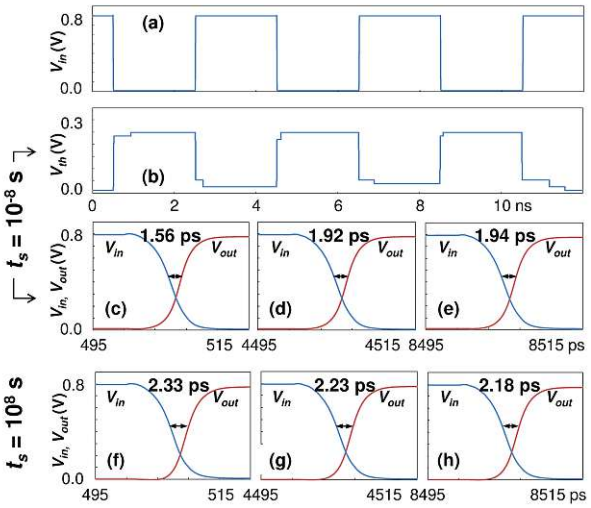

Figure 2.7: A rectangular voltage signal is applied at the inverter chain with a frequency of $f = 250\,\text{MHz}$ **(a)**. After $t = 10^{-8}\,\text{s}$ two defects producing RTN are visible during the high an low cycles of the signal **(b)** leading to variations of the inverting delay **(c-e)**. After $t = 10^{8}\,\text{s}$ several traps affect the ideal device behavior and are responsible for the so-called jitter **(g-i)**, after [MWJ6].

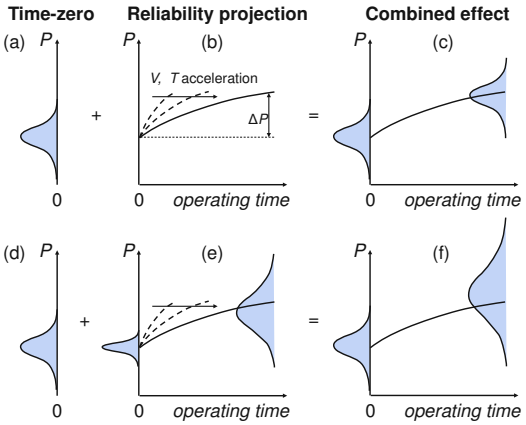

Figure 2.8: Two approaches to consider time-zero variability together with time-dependent effects are shown. **(a)** The time-zero variability is described by a mean value and variance of the underlying distribution. **(b)** A projection of the mean value is considered to **(c)** account for time-dependent effects. Alternatively, **(d)** the time-zero variability **(e)** is considered to have time-dependent mean values and time-dependent variances. **(e)** shows the propagation of the variability considering time-dependent effects, after [MWJ6].

bias. At $t = 10^{8}\,\text{s}$ additional "slow" defects increase the threshold voltage of the device. Overall, a variation in the inverter switching delay is visible, the so-called jitter, and a deceleration of the inverter stage is apparent, emphasizing the importance and role of BTI in modern circuits.

2.5. Time-Dependent Variability

A very important aspect in scaled devices is the device variability, i.e. the deviation between nominally identical devices. In this context the time-zero variability, see Section 1.2, and time-dependent variability have to be addressed, see Figure 2.8. The former is a consequence due to the limited controlability of the production process whereas the latter is primarily defined by charge trapping and defect creation. Most importantly, the time-dependent variability is inversely proportional to the device area, thereby making this time-dependence more pronounced in nanoscale MOSFETs. In large-area devices, a vast number of defects results in an on average similar time-dependent device behavior. In nanoscale devices on the other hand the situation is completely different as only a handful of defects with widely distributed time constants and distributed ΔV_{th}

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are present. As a consequence, a large time-dependent variation between different devices is visible.

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3

Main Features of Bias Temperature Instabilities

Most commonly BTI is studied in terms of an equivalent threshold voltage shift which occurs when a device is subjected to stress. As the device performance changes particularly slowly at use conditions, the experiments are usually performed at significantly larger biases and temperatures which are called *accelerated stress conditions*. With the results obtained from voltage and temperature accelerated tests, analytical or empirical models can be derived, calibrated and then used to predict the impact of BTI on the device performance at nominal operating conditions. Therefore, sophisticated models are required which have to provide an accurate description for temperature and field dependent effects.

3.1. Temperature Dependence

To illustrate the temperature dependence of the threshold voltage shift after the transistor has been subjected to NBTI stress, several recovery traces on a large-area pMOSFET are measured after the transistor has been stressed. The measured recovery of the threshold voltage is plotted after normalization to $\Delta V_{\mathrm{th}}(t_{\mathrm{r}} = 1\,\mu\mathrm{s})$ in Figure 3.1. Most notably, a similar recovery behavior is obtained for ΔV_{th} recovery traces measured at different temperatures. As demonstrated in the following, this observation is important because by studying large-area devices the recovery seems to have only a weak temperature dependence. In contrast, a strong temperature dependence is obtained when the average emission time of single defects is studied in detail on nanoscale devices, see Figure 3.2. Using such scaled transistors, the temperature activation of the charge trapping kinetics is directly visible, emphasizing the need for experiments on small devices.

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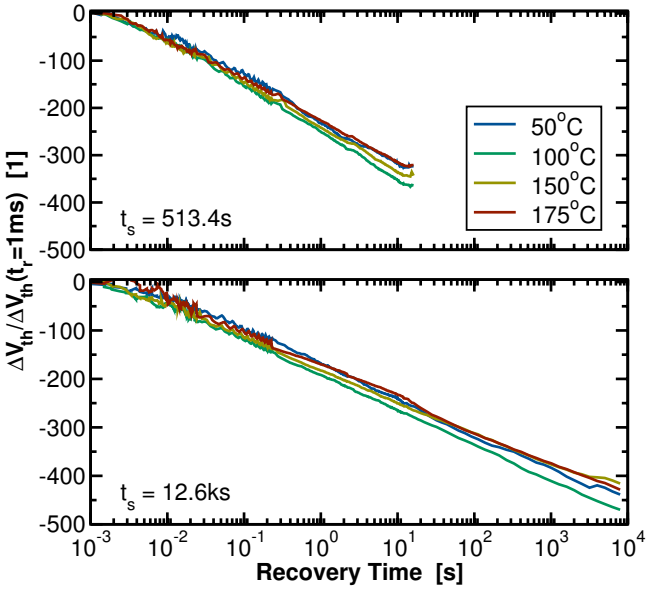

Figure 3.1: The recovery traces of a large-area device ($W \times L = 10\,\mu\text{m} \times 10\,\mu\text{m}$) are shown recorded at four different temperatures after the device has been stressed for (**top**) $t_s = 513.4\,\text{s}$ and (**bottom**) $t_s = 12.6\,\text{ks}$. Furthermore the recovery ΔV_{th} characteristics is normalized to $\Delta V_{th}(t_r = 1\,\text{ms})$. As can be seen, a similar recovery behavior is obtained at different temperatures, which reveals that at a first glance the device recovery only shows a weak or negligible temperature dependence.

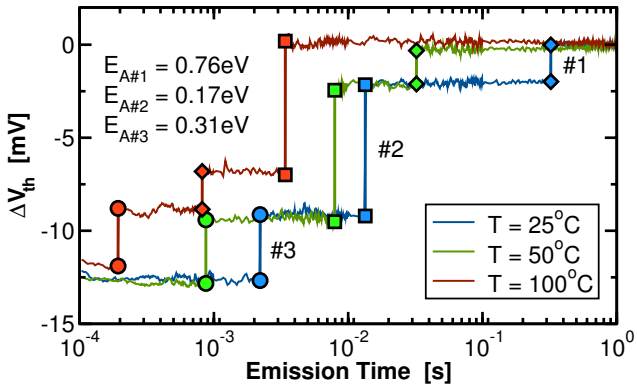

Figure 3.2: In nanoscale devices (schematic for pMOSFET with $W \times L = 150\,\text{nm} \times 100\,\text{nm}$) the recovery proceeds in discrete steps. As single defects produce exponentially distributed emission times around their average emission time, the traces for each temperature are calculated by averaging 100 single traces. Clearly visible, at higher temperatures the emission events move towards shorter emission times. The given activation energies E_A are calculated using an Arrhenious' law.

3.2. Field Dependence

Next, the phenomenological impact of the stress and recovery field on the threshold voltage shift is shown. Again, the results of large-area devices and the results obtained from their nanoscale counterparts are compared.

3.2.1. Bias Dependence of the Capture Time

Considering the threshold voltage shift of large-area transistors recorded during stress, as visible in Figure 3.3 (left), it can be clearly seen that the absolute threshold voltage shift increases at larger stress biases. This observation is intuitively clear, because a higher stress bias leads to higher oxide field and as a consequence more defects can become charged. Also visible is the continuous characteristics of the threshold voltage shift which can be attributed to the contribution of many defects with very small step heights to the total threshold voltage shift. In contrast, for nanoscale

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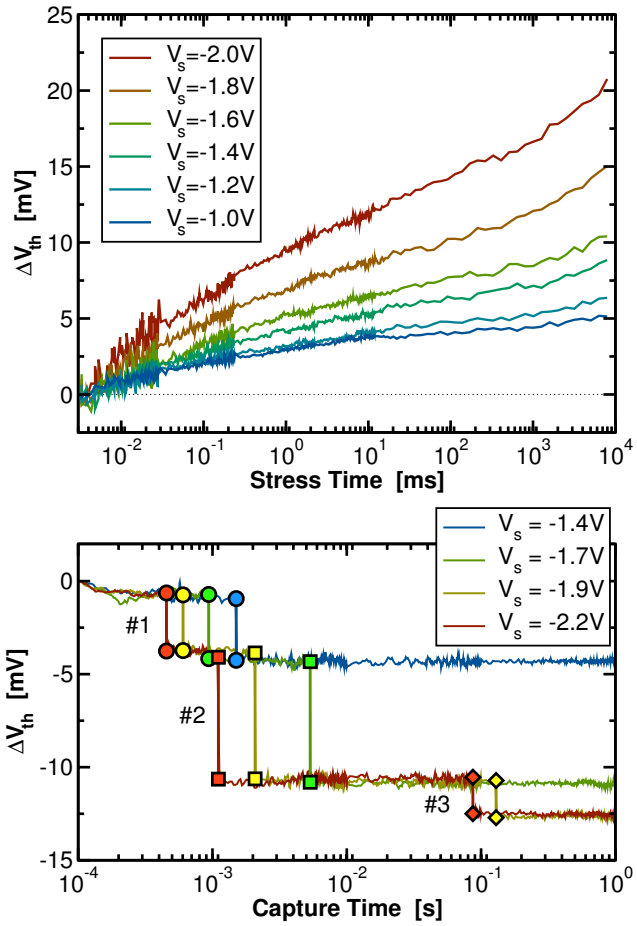

Figure 3.3: A strong dependence of the ΔV_{th} on the stress bias $V_{\text{G,s}}$ can be observed for (**top**) large-area devices and (**bottom**) nanoscale transistors. Whereas the former shows a continuous increase in the threshold voltage shift, the ΔV_{th} from the latter is dominated by discrete ΔV_{th} steps at characteristics capture times of the single defects contributing to it. As can be seen, at larger $V_{\text{G,s}}$ the capture times of the defects become smaller, and additional defects can become charged.

devices the impact of the stress bias can be illustrated best in terms of single defects which become charged during the stress cycle, see Figure 3.3 (right). Thereby each defect has its individual charge capture time which is strongly bias and temperature dependent. As a consequence of the decreasing capture time at higher stress biases, the probability of a single defect to become charged increases when the stress bias is increased.

3.2.2. Bias Dependence of the Emission Time

Analogously to the stress bias dependence of the threshold voltage shift, the threshold voltage shift does also depend on the gate bias during recovery. As can be seen in Figure 3.4 (left), the larger the recovery bias gets, the slower the device recovery proceeds. In line with the accumulated threshold voltage shift during stress from Figure 3.3 (right), the recovery of nanoscale devices proceeds in a discrete manner too, see Figure 3.4 (right). The emission time of such charge emission events can be very sensitive to the recovery bias. However, in contrast to the charge capture events, charge emission of single defects can also be bias-independent. Thus the emission time of a defect does not change with the gate bias. This behavior can be seen for defect #2 which remains unaffected by an change of the gate bias, whereas the two other defects emit their charge at shorter emission times for lower recovery bias. In general, the bias independent emission time

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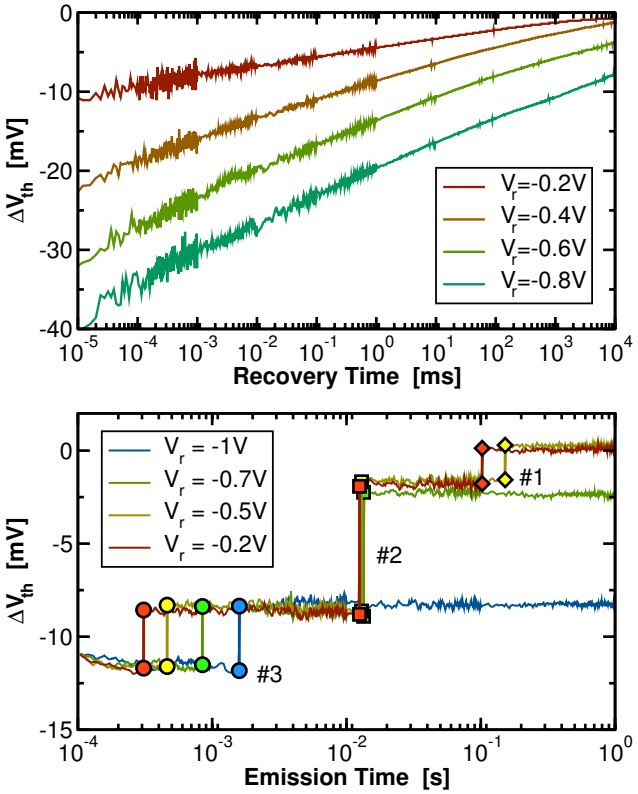

Figure 3.4: The recovery of the threshold voltage shift is affected by the recovery bias $V_{G,r}$, shown for (**top**) a large-area transistor and (**bottom**) a nanoscale transistor. In the case of the large-area transistor, the smaller $V_{G,r}$ is the slower the ΔV_{th} recovery proceeds. The recovery behavior of the nanoscale transistor is dominated by discrete ΔV_{th} shifts produced by the charge emission of single traps. Most notably, defect #1 and defect #3 show bias dependent emission times whereas the emission time of defect #2 appears unaffected by $V_{G,r}$.

is associated with *fixed oxide traps* whereas the bias dependent emission times are due to *switching traps*. As one can easily see, providing an accurate model of the bias dependence of BTI is pretty challenging as for instance the field dependence of individual defects is observed to be on one hand negligible and on the other hand very strong.

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4 Modeling of Bias Temperature Instabilities

As discussed in previous chapters, BTI has a detrimental impact on the transistor characteristics by *(i)* shifting the threshold voltage V_{th}, and reducing *(ii)* the device transconductance, *(iii)* the device saturation current and *(iv)* the channel mobility. As a consequence, increasingly large delays are introduced in high performance CMOS circuits which affect the timing of the transistors. Furthermore, defects can act as TAT centers and thus endanger the reliable operation of SRAM devices. In order to correctly understand the experimental data and to be able to provide meaningful lifetime predictions, a thorough and systematic theoretical analysis of the experimental data is required. Therefore, a variety of theoretical models for BTI have been suggested, starting from empirical fit expressions over more or less accurate compact models up to detailed TCAD models.

Because the impact of BTI on a transistor is typically expressed in terms of an equivalent threshold voltage shift, models developed around these instabilities rely on reproduction of the ΔV_{th} measured for different stress and recovery biases and at different temperatures. Furthermore, the threshold voltage shift caused by BTI is observed to be the superposition of a recoverable and permanent component. Thus a suitable model necessarily has to capture both contributions to the measured threshold voltage shift.

In the following, empirical models which are due to their simplicity regularly used to describe BTI are presented. As empirical descriptions can not reflect the physics behind BTI, namely the trapping kinetics of single defects, modeling of single defects is introduced next. Finally, recent advances on how to properly explain the permanent threshold voltage shift via the hydrogen release (HR) model are discussed.

4.1. Empirical Models

Empirical models provide the simplest description for experimental data and are often used if the detailed mechanism behind an observation is not known. In the context of device physics

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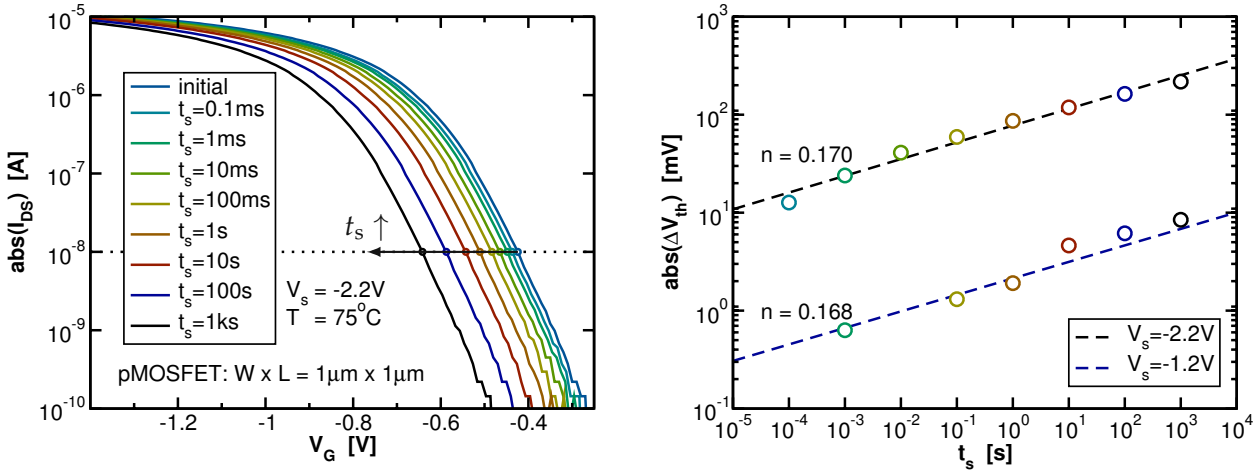

Figure 4.1.: (**left**) For pMOSFETs subjected to NBTI stress the $I_{DS}(V_{GS})$ characteristics are shifted towards larger absolute threshold voltages with increasing stress times. To determine the threshold voltage shift, the gate voltage leading to a defined drain-source current is calculated for all stress times. (**right**) The stress bias dependence of the threshold voltage shift can be modeled using a power law.

experimental data can often be modeled using a power law or exponential-like functions [96, 97]. The advantage of such empirical formulations is that they provide a fast and simple method to quantify the results with a reduced parameter set. Although such models are used to compare different technologies they have to be treated with care as they do not provide a physics-founded description of the underlying mechanism and thus extrapolations may be inaccurate.

Next, the BTI modeling using a power law is briefly discussed, followed by the reaction-diffusion (RD) model and its extensions.

4.1.1. Power Law based modeling of Bias Temperature Instabilities

At its simplest, the impact of BTI on the device threshold voltage of large-area devices can be expressed by comparing the $I_{DS}(V_{GS})$ characteristics before and after the transistors have been subjected to BTI stress, see Figure 4.1. As can be seen, the larger the stress time gets, the larger the observed threshold voltage shift will be. The observed threshold voltage shift can be described by a power law in time

$$\Delta V_{th} = A t_s^n \tag{4.1}$$

with A being a stress voltage dependent prefactor and n the power law exponent in the range of 0.1 and 0.25 [98]. The prefactor itself is stress bias dependent and given by

$$A \propto E_{ox}^{\gamma} \approx \left(\frac{V_{ov}}{t_{ox}}\right)^{\gamma} \tag{4.2}$$

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with the overdrive voltage $V_{ov} = |V_{G,s} - V_{th}|$ and the exponent γ typically in the range of 2.5 to 3 for NBTI in Si devices [98]. Furthermore, the temperature dependence follows an Arrhenius' Law

$$\Delta V_{th} \propto e^{-\beta E_A} \tag{4.3}$$

with the activation energy E_A reported to be in the range $60 - 80\,\text{meV}$ [99]. The combination of all three equations leads to the simple analytic expression

$$\Delta V_{th} = A \left(\frac{V_{G,s} - V_{th}}{t_{ox}} \right)^{\gamma} e^{-\beta E_A} t_s^n \tag{4.4}$$

for the threshold voltage shift. Based on the above equation for instance the device lifetime can now be estimated. However, an extrapolation based on such an empirical description is usually very inaccurate. To provide a more accurate explanation for BTI a physically correct BTI model is needed. The most promising approach appears to be based on the study of single defects, which much more clearly reveals the underlying physics. For this, nanoscale devices have to be used as they allow to study single defects individually.

4.1.2. Reaction-Diffusion Model

For a long time the reaction-diffusion (RD) model was the most successful model to explain NBTI observed in large-area devices [100]. The RD model assumes that interface states, which are dangling bonds present at the Si/SiO_2 interface, are the culprit for threshold voltage shifts introduced during normal device operation. During the fabrication process interface states can be passivated by hydrogen (H) thereby forming a Si-H bond. However, in the RD model it is assumed that this formation can capture a hole which weakens the Si-H bond. As a consequence the H can be released from the Si atom leaving an unsaturated, electrically active bond behind. The hydrogen itself is then assumed to diffuse into the gate dielectric. Conversely, hydrogen atoms can turn around to passivate the dangling Si bond and neutralize the interface state.

By analyzing $C(V)$ characteristics under different stress conditions [100] observed that the creation of interface states follows a power law of the form $N_{it} \propto t^{1/4}$. This behavior was then described by considering passivation and depassivation of the Si dangling bonds according to [100]

$$\frac{\partial N_{it}}{\partial t} = k_f (N_{it,0} - N_{it}) - k_r N_{it} H_{it} \tag{4.5}$$

with k_f and k_r the forward and backward rate, respectively, N_{it} the interface state density and H_{it} the interfacial hydrogen concentration. Note that in this one-dimensional mathematical framework the hydrogen concentration is a function of $H(x,t)$ and $H_{it} = H(0,t)$. The diffusion of released hydrogen is described by

$$\frac{\partial H}{\partial t} = -D \frac{\partial^2 H}{\partial x^2} \tag{4.6}$$

with D the diffusion coefficient.

Nearly forty years little attention was paid to BTI until the continued scaling of the transistor geometries reached the sub-micrometer regime. During that time the RD model was used to describe BTI.

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As the impact of BTI on ΔV_{th} was revisited using more detailed stress/measure sequences, the threshold voltage shift was found to relax immediately after stress release and the relaxation was observed to continue for very long recovery times. To describe both observations, a modified RD model was proposed [101, 102, 103, 104, 105]. In this modified model the one-dimensional motion of hydrogen was replaced by three-dimensional hydrogen distribution and diffusion. Furthermore, the diffusion H and H_2 molecules and their inter-conversion is considered. Based on (4.5) and (4.6) the modified RD model is described by

$$\frac{\partial N_{\text{it}}}{\partial t} = k_{\text{f}}(N_{\text{it},0} - N_{\text{it}}) - k_{\text{r}} N_{\text{it}} H_{\text{it}} \tag{4.7}$$

$$\frac{\partial H}{\partial t} = -D\frac{\partial^2 H}{\partial x^2} - k_{\text{H}} H^2 + k_{\text{H}_2} H_2 \tag{4.8}$$

$$\frac{\partial H_2}{\partial t} = -D_2\frac{\partial^2 H_2}{\partial x^2} + \frac{k_{\text{H}}}{2} H^2 - \frac{k_{\text{H}_2}}{2} H_2 \tag{4.9}$$

$$\tag{4.10}$$

with k_{H} and k_{H_2} the reaction rates for dimmarization and atomization of hydrogen, respectively. However, closer inspection revealed that not even this extended RD model can describe the dynamics of BTI [106, 92, 107, MWJ8, 108].

4.2. Single Charge Trapping Models

In contrast to large-area devices the recovery of the threshold voltage shift recorded from nanoscale devices proceeds in discrete steps, see Section 2.3 and Figure 2.5. To describe such a recovery behavior a stochastic charge trapping model is required rather than an approximation by a simple power law, because the latter can not capture the discrete recovery of nanoscale transistors, see Section 3. In such datasets each single defect can be clearly identified by its capture time τ_{c}, emission time τ_{e} and its step height, and can either be neutral or charged depending on whether a low or high gate bias is applied. In previous studies, single charge trapping has been studied from RTN signals recorded on small-area devices [109]. During these investigations the charge capture and emission times have been found to be very sensitive to the applied bias. This bias dependence of the charge capture and charge emission is also observed when stress/recovery experiments are performed and analyzed. In contrast to traditional RTN analysis, stress/recovery experiments rely on charging and discharging a single defect during the stress and recovery phases, respectively. In such experiments a high gate bias is initially applied to charge the defect. Next, the gate voltage is switched to the recovery bias and the drain-source current is recorded. From the experimental data the capture and emission time of single defects can now be extracted, see Section 5. Hence the charge capture and emission time is very sensitive to the applied bias and different biases are used during stress and recovery, each charge state can be described by its characteristic capture and emission times $\tau_{\text{c}}^{\text{L}}$ and $\tau_{\text{e}}^{\text{L}}$ or $\tau_{\text{c}}^{\text{H}}$ and $\tau_{\text{e}}^{\text{H}}$, respectively. Considering a two stage model [90] the transition times between the neutral and charged state can then be expressed as

$$\frac{1}{\tau_{\text{c}}} = \frac{1}{\tau_{\text{c}}^{\text{H}}} + \frac{1}{\tau_{\text{e}}^{\text{H}}} \tag{4.11}$$

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and

$$\frac{1}{\tau_e} = \frac{1}{\tau_c^L} + \frac{1}{\tau_e^L} \tag{4.12}$$

for charge capture and charge emission, respectively. The occupancies, i.e. the probability that the defects is either charged after the stress bias has been applied or the defect is neutral after the recovery bias has been applied for and indefinitely long time, are given by

$$f^H = \frac{\tau_e^H}{\tau_e^H + \tau_c^H} \quad \text{and} \tag{4.13}$$

$$f^L = \frac{\tau_e^L}{\tau_e^L + \tau_c^L}. \tag{4.14}$$

The stress time dependent transition for the capture process reads

$$f(t_s) = f^H + (f^L - f^H)e^{-t_s/\tau_c} \tag{4.15}$$

and the time dependent occupancy, i.e. the probability of a defect to be charged after the stress time t_s and recovery time t_r has elapsed, becomes

$$f(t_s, t_r) = f^L + (f(t_s) - f^L)e^{-t_r/\tau_e}, \tag{4.16}$$

considering that the defect can switch back to its neutral state after t_s elapsed and the low bias is applied at the gate. To simplify the equations stated above we can assume that each defect emits his charge after indefinitely long recovery time which means that the low level occupancy can be considered zero. This yields

$$f(t_s, t_r) = A(1 - e^{-t_s/\tau_c})e^{-t_r/\tau_e} \tag{4.17}$$

with A a prefactor which represents the capture probability for $t_s \to \infty$. At a first glance, one might expect this prefactor to be close to 1 but this is only the case for very large gate biases. As soon as the stress voltage is reduced, the capture time increases while the emission time decreases, thereby resulting in $A < 1$. This means that although a nominal stress bias is applied the defect can emit its charge during stress and thus is never occupied with a probability of 100 %. Nonetheless, using the occupancy functions the normalized transition function can be defined

$$\begin{aligned} h(t_s, t_r, \tau_c, \tau_e) &= \frac{A(1 - e^{-t_s/\tau_c})e^{-t_r/\tau_e}}{A} \\ &= (1 - e^{-t_s/\tau_c})e^{-t_r/\tau_e} \end{aligned} \tag{4.18}$$

and is shown in Figure 4.2 for different capture and emission times. The total threshold voltage shift can finally be expressed by

$$\Delta V_{th}(t_s, t_r) = \sum_k^{N_T} \eta_k A_k h_k(t_s, t_r, \tau_{c,k}, \tau_{e,k}) \tag{4.19}$$

with η_k the contribution of defect k to the ΔV_{th} and A_k the occupancy [90]. Using (4.19) the threshold voltage shift due to charge trapping is expressed in terms of charge transitions caused by

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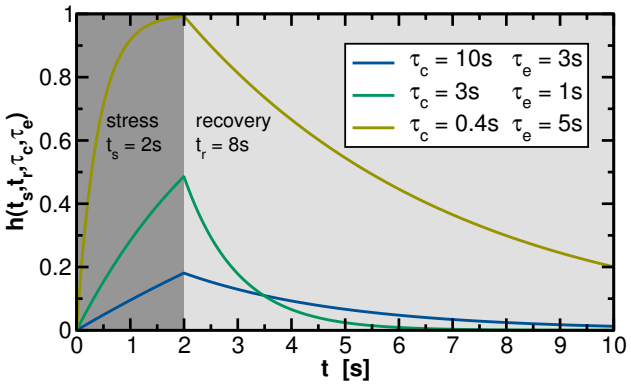

Figure 4.2: The transition function gives the probability of a defect to be either it the charged or neutral state. When a constant stress an recovery time is considered, the maximum of the normalized transition function is defined by the capture and emission time of a single defect. In case of $\tau_c < t_s$ the occupancy gets close to one whereas for $\tau_c > t_s$ the defects transition to the charged state is very unlikely. The situation is the same for charge emission.

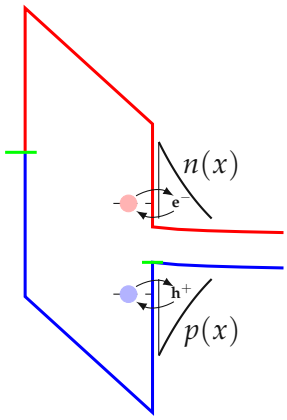

Figure 4.3: An electron trap which is located above the fermi-level and a hole trap which is energetically located below the fermi-level are shown in the dielectric of a MOSFET. The arrows indicate the charge capture and emission process, after [113].

single defects. As already mentioned, in nanoscale devices only a handful of defects are present. Furthermore, the impact of these defects on the total ΔV_{th} is can be resolved by our measurement equipment and the single charge transitions manifest as discrete steps in the drain-source current. By studying the dependence of the ΔV_{th} on the gate area it has been found that the trap density and the average step height follow $N_{\text{T},\mu\text{m}} \approx A N_{\text{T,nm}}$ and $eta_{\mu\text{m}} \approx eta_{\text{nm}}/A$, respectively. As a consequence, ΔV_{th} in large-area devices can also be expressed in terms of single charge trapping using (4.19), however, larger trap densities $N_{\text{T},\mu\text{m}}$ with smaller contributions $eta_{\mu\text{m}}$ to the total ΔV_{th} have to be considered. Note that, because $eta_{\mu\text{m}}$ is typically below the measurement resolution single charge trapping can only be investigated in modern nanoscale transistors.

4.2.1. Elastic Tunneling

The first modeling attempts trying to describe charge trapping were based on the assumption that charge capture and charge emission can be described by elastic tunneling processes [110, 111, 112], see Figure 4.3. During an elastic tunneling process the carrier does not change its energy which is illustrated by the same energy level of the defect in the dielectrics and the carrier located in the valence/conduction band. The charge transfer transitions considered as elastic tunneling processes lead to charge transition times which are proportional to the trap depth x_0 [93]

$$\tau \propto \mathrm{e}^{-x/x_0}. \tag{4.20}$$

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This dependency introduces some difficulties when describing charge trapping. In order to correctly reproduce the recovery behavior of large-area transistors, widely distributed charge emission times are required. However, such a broad distribution can only be achieved by devices having thick oxides, which is not the case in modern ultra-scaled devices [114]. Furthermore, elastic tunneling is inherently temperature independent and can not explain the strong temperature acceleration of charge capture and emission, which becomes visible when single defects are studied, see Section 3.1. As a consequence, models based on elastic tunneling can not provide an accurate description of charge trapping in the context of BTI.

4.2.2. Charge Trapping involving Multiple Phonons

The most promising model to describe BTI was initially proposed in [93] and refined in [115, 88, 116]. It employs the concept of charge trapping which was introduced to describe RTN signals and $1/f$ noise [117, 118] and relies on hole trapping in defect sites located in the oxide supported by a multiphonen emission (MPE) process [119, 120]. Compared to elastic tunneling considerably larger capture and emission times are achieved for MPE processes [121].

Initially, to explain charge trapping of single defects the HDL model for a switching oxide trap was used [122]. The HDL model is two stage model, and has been proven to explain the ΔV_{th} characteristics during stress and recovery [93], see Figure 4.4. In this model a neutral defect (state

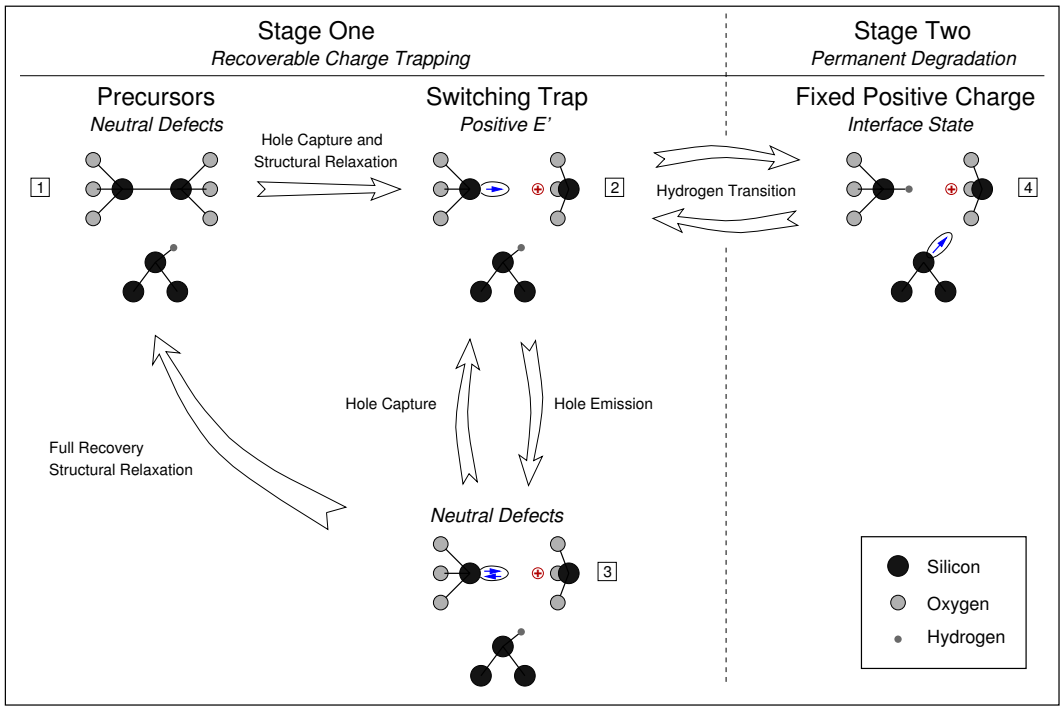

Figure 4.4.: The switching trap model for the creation of an E′ center (stage 1) is coupled with the creation of an interface state (stage 2). The former is considered to contribute to the recoverable component of BTI whereas the latter was assumed to be the culprit for the permanent ΔV_{th}, after [93].

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1) can capture a hole and afterwards relax into the positively charge E' center configuration (state 2). From its charged state, the defect can either be repeatedly uncharged and charged (state 3), or the defect can be uncharged and subsequently recover into its neutral state. Both pathways describe defects which contribute to the recoverable ΔV_{th}. Alternatively, starting from state 2 the defect can be passivated by a hydrogen released from an interface state (state 4) and contribute to the permanent ΔV_{th}. In this model, the transition between state 1 and state 2 is modeled using the multiphonon-field-assisted tunneling (MPFAT) mechanism [123, 124] and the transition between state 2 and state 4 is described by field dependent thermal barriers, also know as double-well model [125], see Section 4.4.1. By using this switching trap model the strong bias dependence of the charge capture and emission time of single defects as well as their temperature dependence can be explained [126].

To study the complex bias and temperature dependence of charge capture and charge emission transitions of single defects, the TDDS has been proposed, see Section 5. Detailed TDDS studies have revealed defects with strongly bias-dependent emission times, an observation which can be partly described by the two-stage switching trap model. Additionally, a notable number of single defects show bias-independent emission times. To model this particular bias-independency the HDL model is extended by an additional metastable state [126, 127, 116] leading to the four-state NMP model.

4.3. Recoverable Component of Bias Temperature Instabilities

4.3.1. Modeling of Single Trap Characteristics

The most basic formulation for charge transfer reactions is provided by the two-state model which will be introduced first. As will be pointed out the two-state model can not describe all features observed in the experiments and is therefore extended by two metastable states leading to the well-established four-state NMP model [113, 90]. It has to be noted that the description of the trapping kinetics of single defects using the four-state NMP model is fully consistent with DFT results of likely defect structures.

4.3.2. Two State Modeling

The simplest formulation for charge transfer reactions, i.e. charge capture and emission, is provided by a two state model, see Figure 4.5. Initially, RTN signals have been studied to understand the bias and temperature dependent characteristics of the discrete charge capture and emission events [128]. As can be seen, the voltage signal switches between two discrete voltage levels.

The straightforward stochastic description for the two stage process relies on the Markov model which assumes that

1. each state is stable,

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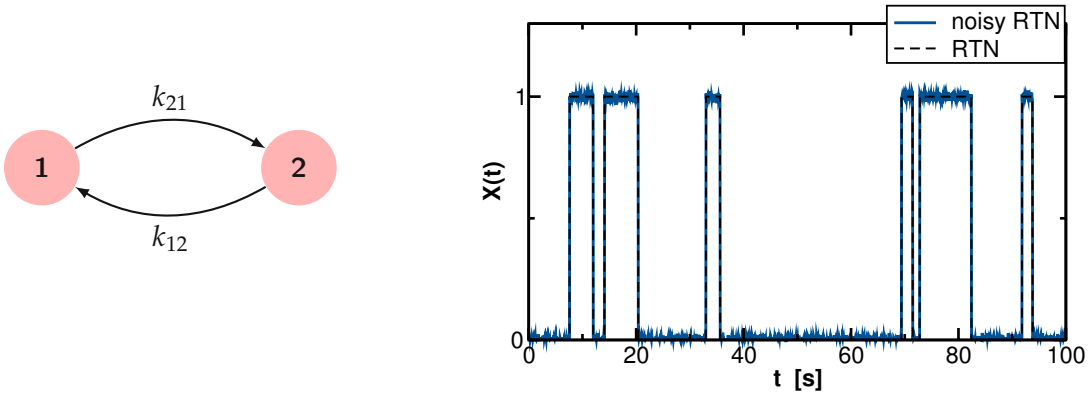

Figure 4.5.: A simple two state Markov process (left) is used to describe RTN signals (right). The transition rates are the reciprocal values of the mean capture and emission time and define the transition probability. It has to be noted that the transition times are exponentially distributed around their mean values, thus in case of equal forward and backward transition rates the RTN is not equal a rectangular signal with a duty cycle of 50 %.

2. the transitions are memoryless and
3. only determined by its time independent transition rates.

The charge capture and emission time τ_c and τ_e for a two state defect can be calculated from the transition rates k_{12} and k_{21} using the relations [90]

$$\tau_c = 1/k_{12} \quad \text{and} \tag{4.21}$$
$$\tau_e = 1/k_{21}. \tag{4.22}$$

Therein the transition rates k_{ij} give the probability for the transition from state i to state j to occur within a unit time interval.

To provide a solid physical based explanation for charge trapping in oxides, the NMP theory is used [129, 121]. The NMP theory relies on solving the Schrödinger equation for a certain atomic configuration leading to the so called adiabatic energy surfaces. In the case of BTI the change of the charge state of a single defect considerably impacts the position of the surrounding atoms and the atoms. Thus, a system involving N atoms spans a $3N$-dimensional space as each position of a single atom is given by its three-dimensional coordinates leading to adiabatic energy surfaces which are impossible to implement in device simulators. To simplify the complex adiabatic energy surfaces the atomic positions are reduced to one-dimensional configuration coordinates and the adiabatic energy surface is approximated by a harmonic oscillator. The potential energy surfaces for a two state defect are shown in Figure 4.6 and can be expressed as

$$U_1(q) = U_1 + c_1(q - q_1)^2 \tag{4.23}$$
$$U_2(q) = U_2 + c_2(q - q_2)^2 \tag{4.24}$$

thereby considering the states 1 and 2 as the neutral and the charged state, respectively. In the case of donor-like traps, i.e. hole traps, state 2 represents a positively charged state and in the case of acceptor-like traps, i.e. electron traps, state 2 is ascribed to a negatively charge state. The barrier

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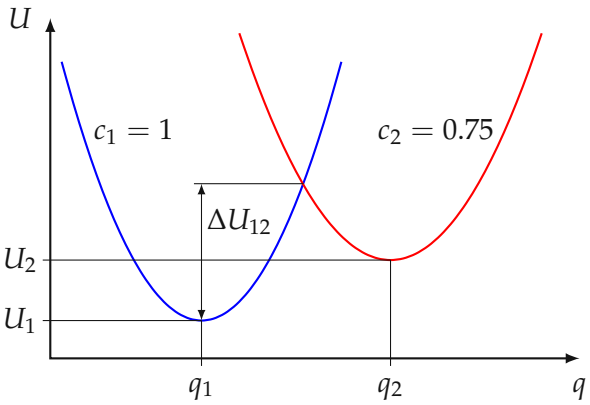

Figure 4.6: The potential energy surfaces are shown for the two state process. The energy barriers for the forward and backward transitions are determined by U_1 and U_2.

ΔU_B between state i and j can get calculated in the classical limit by considering the intersection point of the parabolas and the difference in the energy levels $U_{12} = U_2 - U_1$ together with $q_{12} = q_2 - q_1$, which yields

$$U_1(q) = U_1 + c_1 \Delta q^2 \tag{4.25}$$

$$U_2(q) = U_1 + U_{12} + c_2(\Delta q - q_{12})^2 \tag{4.26}$$

for the adiabatic potentials. Solving the set of equations for Δq for the case of linear electron-phonon coupling ($c_1 = c_2 = c$) leads to the analytic solution

$$\Delta q = \frac{\frac{U_{12}}{c} + q_{12}^2}{2q_{12}} \tag{4.27}$$

for the position of the intersection point and the NMP barrier

$$\Delta U_B(q_{12}) = \left(\frac{U_{12} + c q_{12}^2}{2\sqrt{c} q_{12}} \right)^2 . \tag{4.28}$$

The forward and backward rate, and thus the capture and emission times of the two state process can be calculated by

$$\tau_c = \frac{1}{k_{12}} = \frac{1}{k_0} e^{\beta \Delta U_B(q_{12})} \tag{4.29}$$

$$\tau_e = \frac{1}{k_{21}} = \frac{1}{k_0} e^{\beta(\Delta U_B(q_{21}) + U_1 - U_2)} \tag{4.30}$$

with $\beta = 1/(k_B T)$ and the prefactor k_0. The dependence of the capture and emission times on the difference of the energy levels between state 1 and state 2 is shown in Figure 4.7 with corresponding RTN signals. For $U_{12} < 0$ the forward rate exceeds the backward rate $\tau_c > \tau_e$ and thus the system is preferably in state 2. In contrast, $U_{12} > 0$ leads to $\tau_c < \tau_e$ and then state 1 is the preferred state. For $U_{12} = 0$ an equal forward and backward rate, $\tau_c = \tau_e$, is obtained.

So far, the two state charge transfer process has been considered in general terms. To describe the trapping kinetics of oxide defects, state 1 is assumed to be the neutral state and state 2 the charged state. Relying on the hole picture the physical process behind the transition $1 \rightarrow 2$ is ascribed to hole capture, i.e. electron emission process, and the transition $2 \rightarrow 1$ to the hole emission, i.e. electron capture process. In the case of an electron trap, the roles of electrons and holes are exchanged.

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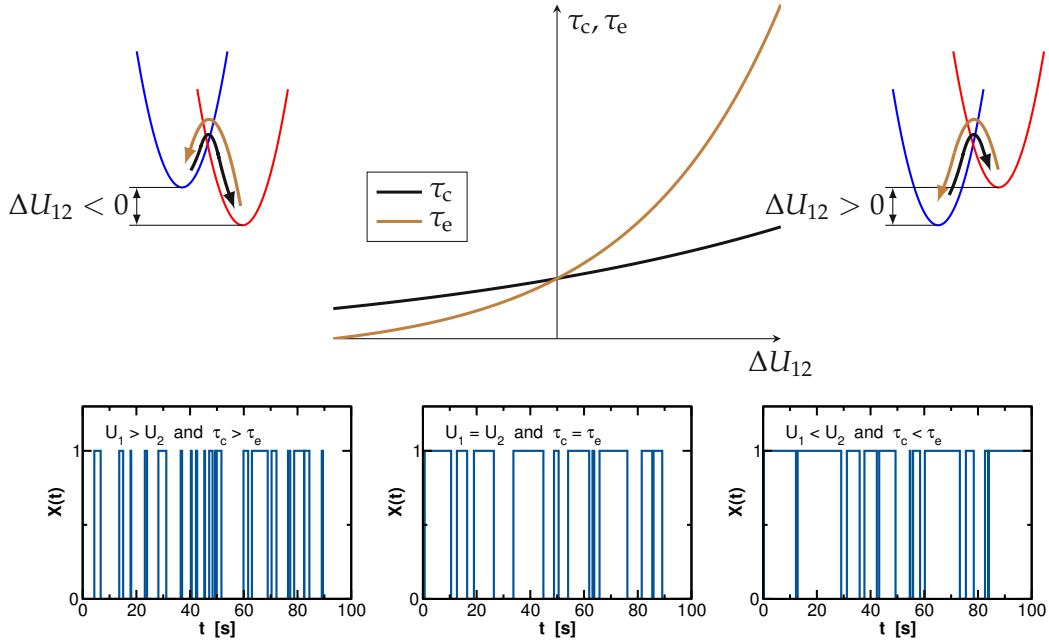

Figure 4.7.: The capture and emission times strongly depend on the energy levels U_1 and U_2. For $\Delta V_{12} = U_1 - U_2 < 0$, the backward rate is larger than the forward rate, i.e $\tau_c < \tau_e$, whereas $U_1 > U_2$ leads to $\tau_c > \tau_e$. The RTN signals are calculated for the respective regimes.

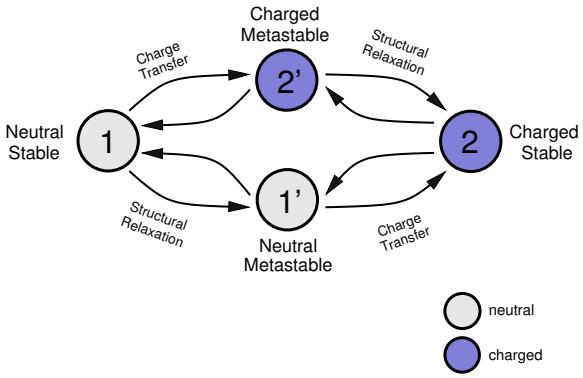

Figure 4.8: The four-state NMP model is used to describe the response of the capture and emission times of single defects to varying biases and temperatures. In general, the model considers two stable states 1 (neutral) and 2 (charged) and two metastable states 1′ and 2′. These states are required for an accurate description of the bias dependence of the emission times as well as other features [88].

4.3.3. Four-State Non-Radiative Multiphonon model

During extensive single-trap studies employing TDDS on pMOSFETs, volatile defects which spontaneously disappeared and reappeared were found. Furthermore, it has been observed that single-trap emission times can be either *(i) switching trap* or *(ii) fixed oxide trap* like. For switching traps a strong bias dependent emission time is observed, whereas bias independent emission times are linked to fixed oxide traps.

In order to explain all features observed from single defects the four-state NMP is used, see Figure 4.8. In principle, the four-state NMP model consists of two stable states 1 and 2 and two meta-stable states 1′ and 2′. The states 1/1′ are considered to be neutral while the states 2/2′ represents a charged defect. The charge capture events are described as a transition from state 1 to

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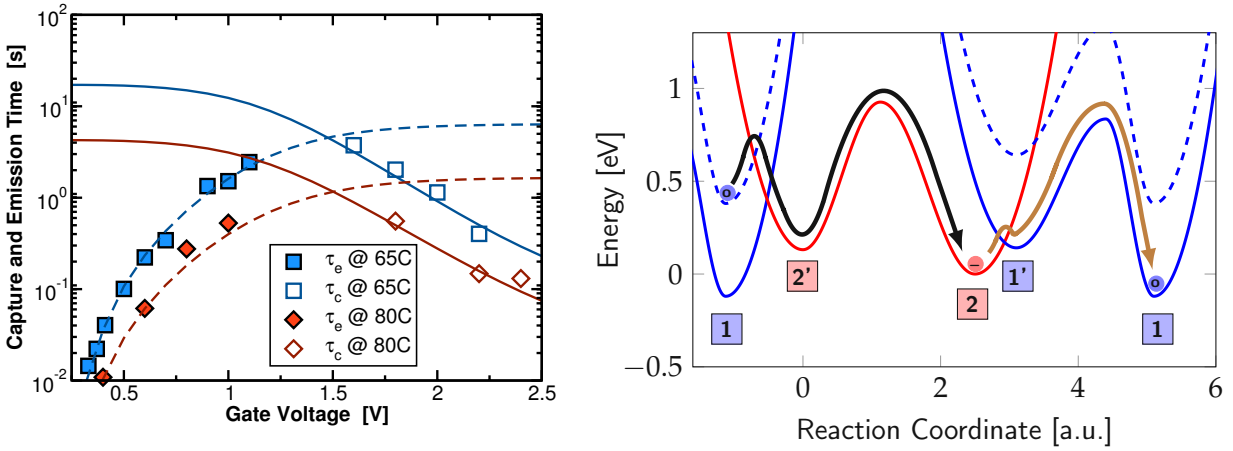

Figure 4.9.: The switching trap behavior is characterized by bias-dependent emission times (left). The four-state NMP model explains the capture and emission time characteristics well. The corresponding potential energy surfaces are shown (right). In order to achieve bias-dependent capture and emission times the transition rates must be dominated by the NMP barriers, thus require $\epsilon_b^c > \epsilon_t^c$ and $\epsilon_b^e > \epsilon_t^e$ [MWC20].

state 2 via the meta stable state 2′ and hole emission proceeds from state 2 to state 1 via either state 1′ or state 2′. The model implicitly distinguishes between

(i) *switching traps* with bias dependent emission times, following the pathway $2 \rightarrow 1 \rightarrow 1$ and

(ii) *fixed oxide traps* with bias independent emission times, choosing the pathway via $2 \rightarrow 2' \rightarrow 1$.

The switching trap characteristics and its corresponding configuration coordinate diagram is visible in Figure 4.9. As can be seen a strong bias and temperature dependence is visible for the capture and the emission time. By using the four-state NMP model, the capture and emission time characteristics and its temperature dependence can be explained. As visible in the configuration coordinate diagram the charge capture event is described by a charge transfer reaction followed by a thermal transition via the pathway $1 \rightarrow 2' \rightarrow 2$. It has to be noted that a small thermal transition barrier ϵ_t^c with respect to a larger bias dependent transition barrier ϵ_b^c is present, leading to a smaller transition rate $k_{2'2}$ compared to $k_{12'}$. Thus the transition from state 1 to state 2 is primarily dominated by the latter. The bias dependent charge emission process follows the pathway $2 \rightarrow 1' \rightarrow 1$. Again a negligible thermal transition barrier ϵ_t^e compared to the bias-dependent transition barrier ϵ_b^e results in a bias-dependent emission time.

The charge capture transition for fixed traps follows the same pathway as obtained for switching traps, i.e. $1 \rightarrow 2' \rightarrow 2$, see Figure 4.10. In contrast to switching traps, the bias independent charge emission proceeds via the pathway $2 \rightarrow 2' \rightarrow 1$. This requires a smaller thermal transition barrier ϵ_t^e compared to the charge transfer barrier ϵ_b^e.

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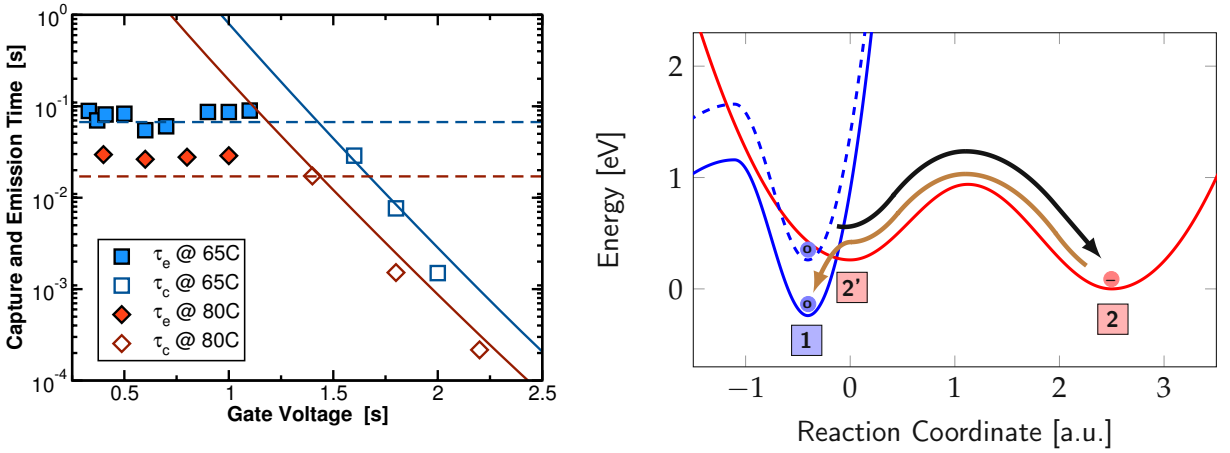

Figure 4.10.: The bias-independent emission times are characteristic for fixed oxide traps (left). Using the four-state NMP model the capture and emission times and their temperature dependence can be nicely reproduced. The corresponding potential energy surfaces (right) show the capture pathway defined by the NMP barrier, i.e. $\epsilon_b^c > \epsilon_t^c$, however, the emission pathway is primarily determined by the thermal barrier, thus $\epsilon_b^e > \epsilon_t^e$ leads to the bias-independent emission time behavior.

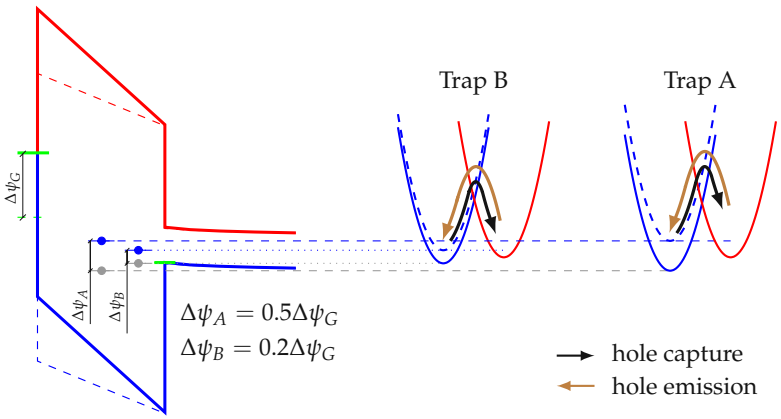

Figure 4.11: The two traps A and B have different trap levels and different positions inside the gate dielectric. Depending on their depth the trap levels are shifted by a different amount when the gate bias changes. As a consequence, a different impact on the forward transition barriers is obtained (right). In summary, the closer the trap is to the gate the larger the shift of the trap level is and thus the smaller the NMP transition barrier gets [MWC20].

4.3.3.1. Trap Position and Bias Dependence

Another important aspect is the determination of the location of the traps in the oxide. For this consider two traps, A and B, placed at a different depths in the SiO_2 gate dielectric of a pMOSFET, see Figure 4.11. Without any loss of generality both traps are considered to be modeled via a simple two state process. At recovery bias conditions both traps are neutral and their trap levels are below the Fermi-level of the channel. When a stress bias is applied at the gate, the trap level shifts with respect to the Fermi-level of the channel depending on their trap depth due to the electric field in the oxide. As can be seen, A is located closer to the gate and thus its trap level is shifted further compared to the trap level of B which is located closer to the channel. The different changes in their trap levels cause different barrier heights ϵ_b^A and ϵ_b^B and thus different transition

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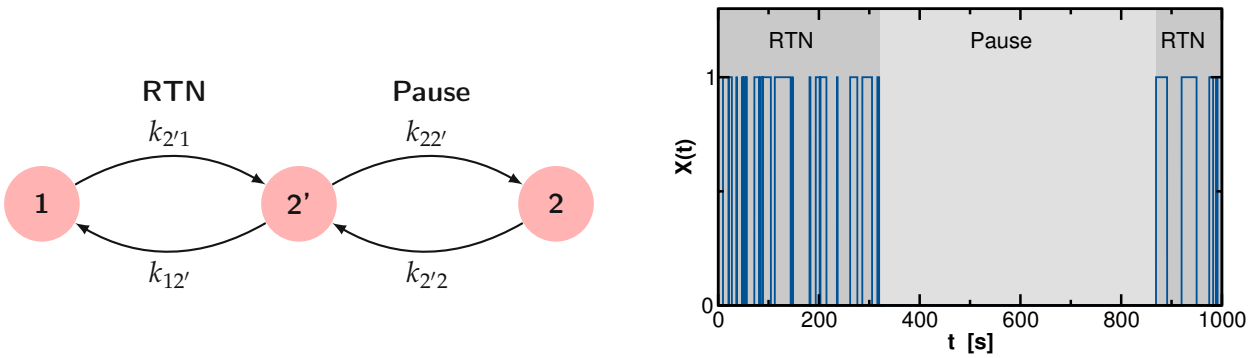

Figure 4.12.: Several defects have been found which produce RTN. A small number of defects incidentally stop to produce RTN. Such signals are termed aRTN and can be described by a three state Markov chain.

rates from neutral the state 1 to the charged state 2. Overall, the closer the trap is located to the gate, the larger is the observed dependence of the capture time on the stress bias.

4.3.3.2. Random Telegraph Noise Signals

While performing single trap measurements, defects producing RTN signals have been observed to be rather the rule than the exception. As the capture and emission time of single traps depend on the applied gate bias, the presence of RTN is also strongly gate bias dependent. As previously discussed, typical RTN signals can be described by a two state model. For experimentally detectable RTN signals, the forward and backward transition rates have to be of the same order, otherwise the single charge capture and emission events are not clearly visible in the measured traces.

Quite remarkably, twenty-eight years ago RTN signals have been observed which occasionally disappear and reappear, a phenomenon termed anomalous random telegraph noise (aRTN) [130], see Figure 4.12 (left). Such defects produce an RTN signal for a limited amount of time until the signal disappears. After a random amount of time, the signal reappears. In those days this behavior was observed for approximately 4 % of the defects. However, it has been recently found that a significant number of defects show the observed volatility. Considering nanoscale devices, NBTI stress can both decrease and increase the number of traps producing RTN [MWC19]. The occurrence of this phenomena is considerably enhanced when stress pulses with positive gate bias which drive the pMOSFET into accumulation are applied . This corresponds to the observation that in large-area devices NBTI stress increases the noise level in the measurement data, [131, 132].

To explain aRTN signals, at least a three state Markov model has to be considered, see Figure 4.12 (left) [90].

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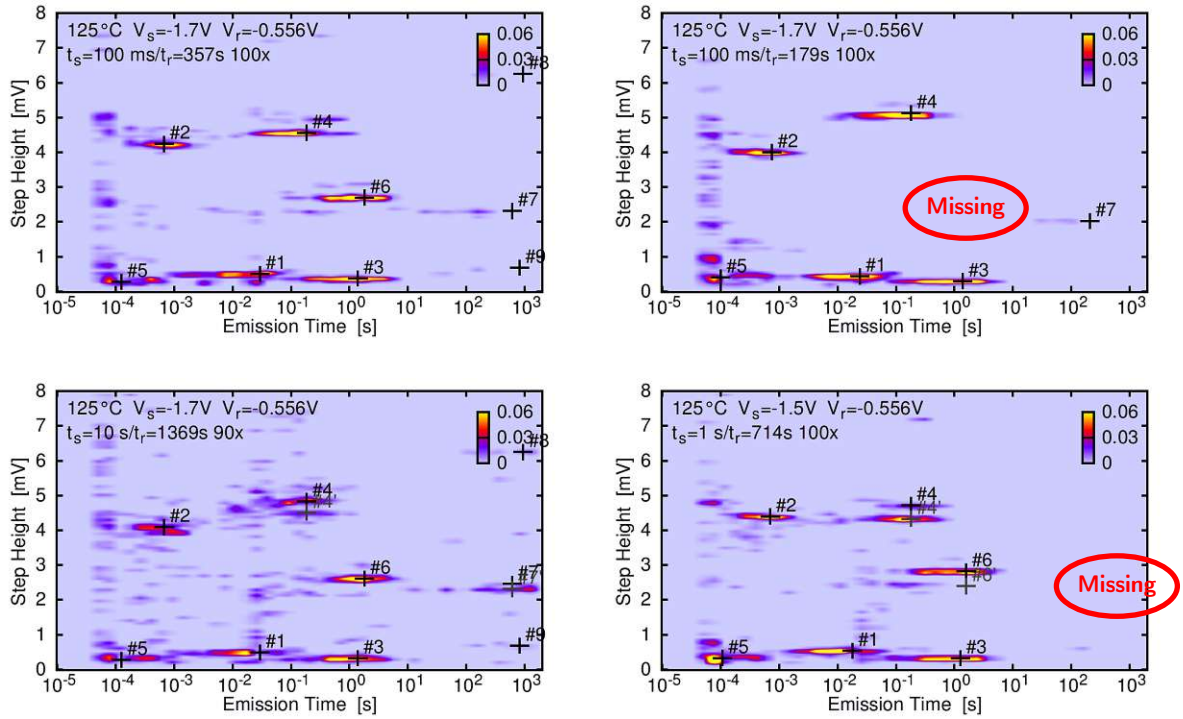

Figure 4.13.: By analyzing the discrete threshold voltage shifts caused by charge emission events of individual traps in nanoscale devices the so-called spectral maps can be created. Every cluster can be attributed to a single trap. As can be seen, numerable defects have been found in the investigated pMOSFET. Quite noteworthy, defect #6 (**top row**) and defect #7 (**bottom row**) suddenly disappear independently from each other. In all subsequent experiments both defects remained invisible [MWC12].

4.3.3.3. Volatility of Defects

As discussed later in Chapter 5, nanoscale devices allow for individual trap identification by their emission time τ_e and their step height d, that is their contribution to the threshold voltage shift. To identify single traps, the emission events of a series of measured traces at certain bias conditions are collected within the so-called spectral map. As shown in Figure 4.13 clusters are visible each representing a single trap.

After probing a single transistor for several weeks or month, defects have been found to disappear and reappear. For instance, defect #6 which shows an emission time $\tau_e \approx 1\,\mathrm{s}$ and a step height of $d \approx 3\,\mathrm{mV}$ suddenly disappeared and remained in his new configuration, see Figure 4.13 (top). The same observation was made for defect #7, see Figure 4.13 (bottom). Initially, both observations were considered rare events. However, recent investigations showed that there is a remarkable number of traps showing such a volatile behavior. Quite interestingly, volatile defects have been observed in n-channel and p-channel MOSFETs using SiON and HK gate stacks and are thus not limited to any particular technology. As the phenomenon is stochastic, it is very difficult study it systematically. However, these defects will an essential clue on the chemical nature of oxide traps.

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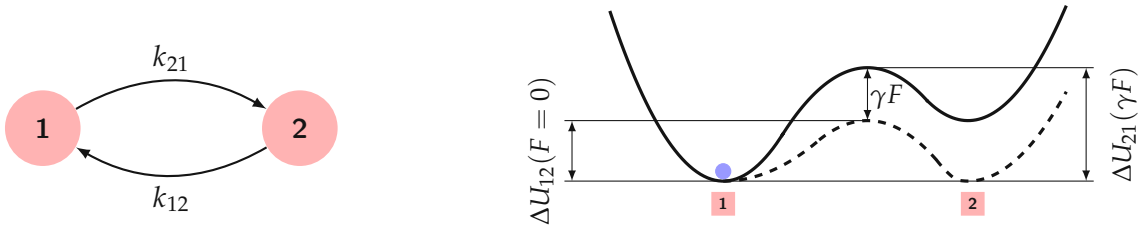

Figure 4.14.: The double well model is based on a two state process. To account for bias dependent transition rates, a field dependent energy barrier is introduced. The strength of the field dependence is given by the prefactor γ, after [125].

4.4. Permanent Component of Bias Temperature Instabilities

As previously mentioned, the recovery of a device subjected to BTI stress is the sum of a recoverable and permanent component. The recoverable component is assigned to oxide traps and can be explained by the four-state NMP model. In contrast, the permanent component is caused by defects with even larger time constants, and is mostly interpreted as the creation of interface states. Although the creation dynamics of the latter are still unclear, their presence is universally acknowledged [133, 134].

In several studies an increased number of interface states has been shown using several experimental techniques, such as ESR [135, 136], spin dependent recombination (SDR) [136], direct current voltage (DCIV) [137], charge pumping (CP) [138, 139, 140] and $C(V)$ measurements [141]. To describe the permanent component, a purely empirical double well (DW) model was proposed and used in several studies [125, 113, 142]. However, the DW model only provides a rather phenomenological explanation of the experimental data. Recently, a new model relying on a hydrogen release mechanism has been proposed providing a physical based explanation for the accumulation of the permanent component of BTI [143, MWC7, MWC6]. Both models are discussed in the following.

4.4.1. Double Well Model

The P_bH configuration is a possible candidate for an interface trap contributing to the permanent threshold voltage shift. In its neutral state a Si atom located at the interface is saturated by a hydrogen atom. During stress, the hydrogen atom can be released from the Si atom and moves away, leading to a dangling bond at the interface, which is known as P_b center. The neutral and the charged state of the P_b center can be assigned to state 1 and state 2 shown in Figure 4.14 (left). The transition $1 \rightarrow 2$ describes defect creation and the opposite pathway the neutralization of

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the defect. The relations between the capture and emission time and the corresponding transition rates are given by

$$\tau_c = \frac{1}{k_{12}} \quad \text{and} \tag{4.31}$$

$$\tau_e = \frac{1}{k_{21}}. \tag{4.32}$$

Without considering a specified atomic configuration, the forward transition rate k_{12} and the backward transition rate k_{21} are modeled to be bias dependent by introducing a bias dependent energy barrier, see the configuration coordinate diagram shown in Figure 4.14 (right). The resulting barriers read [93]

$$\epsilon_{12} = U_{12} - \gamma F, \tag{4.33}$$

$$\epsilon_{21} = U_{12} - U_2 + \gamma F \tag{4.34}$$

with the F electric field and γ a prefactor describing the bias dependence. The corresponding capture and emission times are then given by

$$\tau_c = \nu_0 e^{\beta \epsilon_{12}}, \tag{4.35}$$

$$\tau_e = \nu_0 e^{\beta \epsilon_{21}} \tag{4.36}$$

with ν_0 the attempt frequency. Using the stated relations various energy barriers can now be used to obtain a distribution of charge capture and emission times. Note that considering the energy levels U_{12} and U_2 as random independent numbers, no correlation between τ_c and τ_e would be obtained. However, the potential energy surfaces calculated from DFT simulations are a result of various forces acting on the atomic structure. As such a strong correlated between U_{12} and U_2 is present. Nonetheless, to simplify the model, the energy barriers ϵ_{12} and ϵ_{21} are assumed to be independently distributed. Although the double-well model provides not a very physics based explanation for interface states, its applicability is currently justified as it reproduces the experimental data well and allows easy implementation into device simulators.

4.4.2. Hydrogen Release Model

During the long puzzling history of BTI different mechanisms have been assumed to be responsible for the recoverable and permanent contributions [144, 145, 99, 146]. Recently a new model based on the interaction of point defects with interstitial hydrogen has been suggested to explain the permanent component of BTI. The model thereby allows to reproduce experimental data collected from ultra-long time experiments of more than eight month on a single device.

Conventionally, defects responsible for the permanent component have been associated with interface states which typically show very large time constants [99, 147]. Furthermore it has been suggested that, in addition interface states, hydrogen related donor traps can be created which could dominate the permanent degradation at longer times [143, 148, 149]. Thus instead of considering different contributors to the recoverable and permanent component it is rather more tempting to assume the same kind of atomic configuration of the traps responsible for both. The vital

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difference between traps contributing to the recoverable and permanent threshold voltage shift is due to their capture and emission time constants. In general, traps which have an emission time τ_e smaller that the experimental window t_r, i.e. $\tau_e < t_r$, obviously contribute to the recoverable ΔV_{th}, and traps with $\tau_e > t_r$ are seen as the permanent ΔV_{th}. In the HR model a hydrogen atom can be released by a trap with $\tau_e < t_r$, move through the oxide as interstitial hydrogen, and can subsequently be trapped by a defect with $\tau_e > t_r$, thereby contributing to the permanent component.

The cornerstone of the HR model are recent DFT studies which have demonstrated that hydrogen can bind to Si – O – Si bridges in amorphous and defect free SiO_2 [150, 151], as has been observed in previous experiments [149]. For this to happen, stretched Si – O – Si precursors have to be available, which is particularly likely close to the interface. It has to be noted that this stretched precursor is not available in crystalline SiO_2, where only a proton can bind in a stable manner to the bridging oxygen [152]. Considering the stretched Si – O – Si bond, the interstitial hydrogen can release its electron and bind to the oxygen. Alternatively, the hydrogen can break one of the Si – O bonds and form a hydroxyl group (– OH), which then faces the dangling bond of the other Si, leading to a configuration very similar to the E' center [153]. Recently, it has been demonstrated that the energy barrier of this defect to become charged and discharged is in agreement with defects found to be responsible for the recoverable component in pMOSFETs [MWC16]. Furthermore, since the H can be removed over a thermal barrier, leaving an electrical inactive defect precursor behind, this defect appears to be consistent with the observed volatility of oxide traps [MWC12] as well, see Section 4.3.3.3.

The HR model is built around the hydrogen which can be released at the gate side during stress and in the following moves through the oxide towards the channel interface. As shown in the model in Figure 4.15, a defect available in a suitable precursor state provides a trapped hydrogen atom located at the gate site. When a stress bias is applied, the trap level of the trapped H^+ moves below the Fermi-level of the gate and thus the hydrogen is neutralized. After passing a thermal barrier, the neutralized hydrogen moves very fast towards the channel. Close to the channel, the neutralized hydrogen can get trapped by an empty H^+ trapping site, energetically aligned above the channel Fermi-level. As a consequence, an additional charge at the interface with very slow time constants is created, and thus contributes to the permanent component.

Nonetheless, it has to be mentioned that the microscopic trapping mechanism is very complex as it strongly depends on the atomic configuration of the involved defects. In such SiO_2/Si system defects can exhibit various atomic configurations which are mostly based on disorders of the perfect crystal structure due to nested hydrogen [154, 155, 156]. These anomalies differ in the displacement ant the bond angles between the single atoms thereby leading to different energy barriers for charge trapping. However, these energy barriers are an essential clue for the HR model as they primary define the time constants responsible for charge capture and emission. Hence defects responsible for the permanent threshold voltage shift require a large emission time, only structures exhibiting a large energy barrier for charge emission are of particular interest in context of the HR model. Finally, to provide validate the accurate description of the permanent contribution by the HR model, the energy barriers used within the HR model are in agreement with the energy barriers obtained from DFT simulations.

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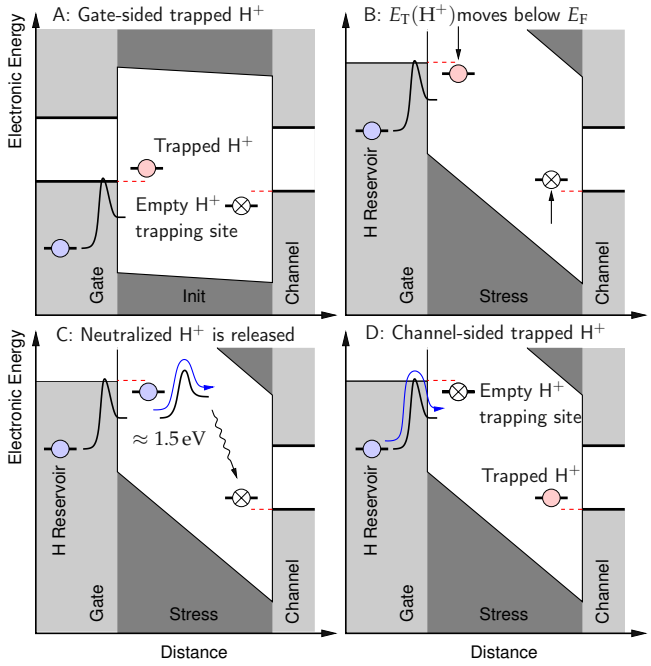

Figure 4.15: The schematic representation of the HR model shows the trapped H^+ at the gate side in the initial configuration (A). During stress the H^+ trap level is below the Fermi-level (B). Next, the H^+ is neutralized and can detrap via a thermal barrier and afterwards migrate very quickly towards the channel (C). There the neutralized H^+ becomes trapped by a precursor with its energy level above the Fermi-level of the channel (D). In particular at high temperatures, additional H^+ can be released from a reservoir at the gate side, [MWC6].

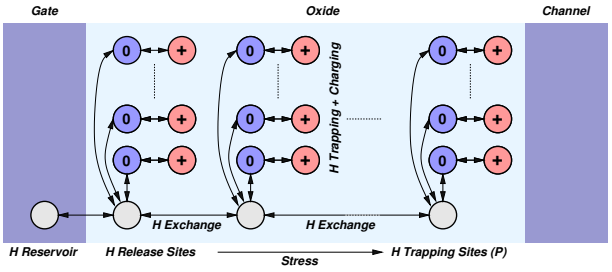

Figure 4.16: The simplified one-dimensional model shows the hydrogen which migrates through the oxide towards the channel. Thereby the hydrogen can get trapped, for instance bonded to an bridging oxygen atom, or detrapped, leading to interstitial hydrogen. Additional hydrogen can get released from a reservoir over a thermal barrier, [MWC6].

For the sake of completeness, it is worth mentioning that various configurations of the SiO_2/Si system involving hydrogen are available [154, 155, 156]. This makes the understanding of the detailed chemical trapping mechanism very complex.

The model discussed in the following relies on the HR mechanism, see Figure 4.15. A simplified one-dimensional schematic for the HR model is shown in Figure 4.16. Since only a small number of hydrogen atoms are present in the gate stack, the model deals with absolute numbers and not with concentrations. The equation describing the temporal change of interstitial hydrogen at site i given reads

$$\frac{\partial H_\mathrm{i}}{\partial t} = -\sum_j k_\mathrm{H}\left(H_\mathrm{i} - H_\mathrm{j}\right) - \sum_n T_{i,n} \tag{4.37}$$

where the first sum runs over all neighboring sites j, thereby describing the diffusion of the interstitial hydrogen which is considered a thermally activated hopping process with the rate

$$k_\mathrm{H} = k_{ij} = k_0 \mathrm{e}^{\frac{-qE_\mathrm{H}}{k_\mathrm{B}T}} \tag{4.38}$$

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and the prefactor $k_0 = D_\mathrm{H}/a^2 = 4 \times 10^{10}\,\mathrm{s}^{-1}$ using the diffusion constant $D_\mathrm{H} = 10^{-4}\,\mathrm{cm}^2/\mathrm{s}$ and the hopping distance of $a = 5\,\text{Å}$ according to literature [157, 158]. At each site i the interstitial hydrogen can get can trapped in its neutral configuration described by the trapping rates

$$T_{i,n} = k_{01} H_\mathrm{i} \left(H^\mathrm{T}_\mathrm{max} - (H^0_{i,n} + H^+_{i,n})\right) - k_{10} H^0_{i,n} \tag{4.39}$$

via the rate k_{01} and the transition back k_{10}. These rates are modeling using the Arrhenius law and read

$$k_{01} = \frac{1}{\nu} \mathrm{e}^{-\beta E_{01}} \tag{4.40}$$

$$k_{10} = \frac{1}{\nu} \mathrm{e}^{-\beta E_{10}} \tag{4.41}$$

with ν the attempt frequency and the distributed energy barriers E_{01} and E_{10}. At each site only a certain number of traps is allowed, which is considered by the term $H^\mathrm{T}_\mathrm{max} - (H^0_{i,n} + H^+_{i,n})$ in the model. Next, the transition of the hydrogen from its neutral configuration either to the positively charged state or the transition back to interstitial hydrogen has to be considered. Both cases are described by the corresponding rate equations

$$\frac{\partial H^0_i}{\partial t} = -k_{12} H^0_i + k_{21} H^+_i + T_i \tag{4.42}$$

$$\frac{\partial H^+_i}{\partial t} = k_{12} H^0_i - k_{21} H^+_i \tag{4.43}$$

while NMP theory is used to model the transition rates k_{12} and k_{21} from the neutral to the positively trapped state and vice versa.

Finally, close to the gate (either poly-silicon and/or metallization) a hydrogen reservoir is assumed to exists, consisted with NRA data [159, 160]. The interaction between the bonded hydrogen and the gate stack is described by

$$\frac{\partial H_\mathrm{R}}{\partial t} = -k_{\mathrm{R}0} H_\mathrm{R} + k_{0\mathrm{R}} H_\mathrm{i} \tag{4.44}$$

for sites i at the gate/oxide interface, with $k_{\mathrm{R}0}$ and $k_{0\mathrm{R}}$ the forward and backward rates, respectively. An evaluation of the model against the recent experimental data is discussed in part three of this thesis.

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Part II.

Experimental

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5

Time-Dependent Defect Spectroscopy

MOSFETs have a large number of traps with detrimental impact on their device performance. In order to explore the mechanism responsible for altering of the device characteristics, $1/f$ noise and random telegraph signal (RTS) [128] have been studied in large-area and nanoscale transistors. RTS, also known as random telegraph noise, have been recorded and analyzed to study the capture and emission time of single defects. Therefore charge capture and charge emission processes have to appear within the experimental window with measurable time resolution. As the charge transfer transition times are very sensitive to the gate bias, RTS analysis only provides information on the charge trapping kinetics within a very narrow gate bias range.

A standardized method to detect a broad variety of traps in semiconductors is the deep level transient spectroscopy (DLTS) [161]. The DLTS relies on the measurement of the capacitance of p-n junctions and works as follows: Initially, a reversed bias is applied to a p/n junction, thus a depletion region is formed at the interface. By applying a short voltage pulse ($\approx$ 1 ms) at the forward biased p/n junction, the depletion layer shrinks and traps which are energetically aligned below the shifted Fermi-level become charged. When the applied bias is switched back the newly charged trap does not immediately become neutralized, resulting in a wider depletion layer. The increase of the depletion layer width leads to a measurable decrease of the junction capacitance.

The TDDS applies DLTS to small devices and augments it by a statistical analysis. The only prerequisite is that the devices have to be small enough to exhibit measurable discrete capture and emission events. An overview of the estimated mean step heights for different technologies based can be seen in Figure 5.1. Quite remarkable, in most recent technology nodes less than one trap per device on average is present. However, as the number of traps dramatically decreases with the device geometry, their impact gets worse. For instance, the average ΔV_{th} of a single defect the present in a transistor produced within the 10 nm exceeds 100 mV. Note that $\Delta V_{\text{th}} = 30$ mV is the typically criteria used for lifetime projections. Thus the proper operation of a single device can be solely determined by only one defect.

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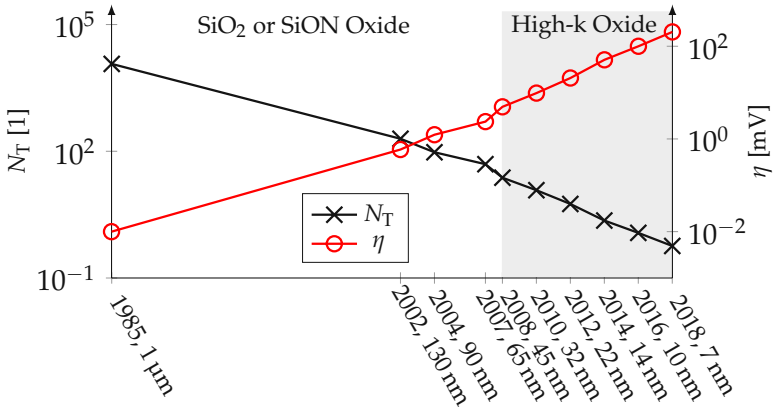

Figure 5.1: The number of active traps N_T significantly decrease in most recent technology nodes, while the average threshold voltage η produced by such defects dramatically increase. N_T and η are calculated from according to the values from Figure 1.1 using the number of traps and average step heights obtained form our single defect studies [MWC26, MWC20, MWC4].

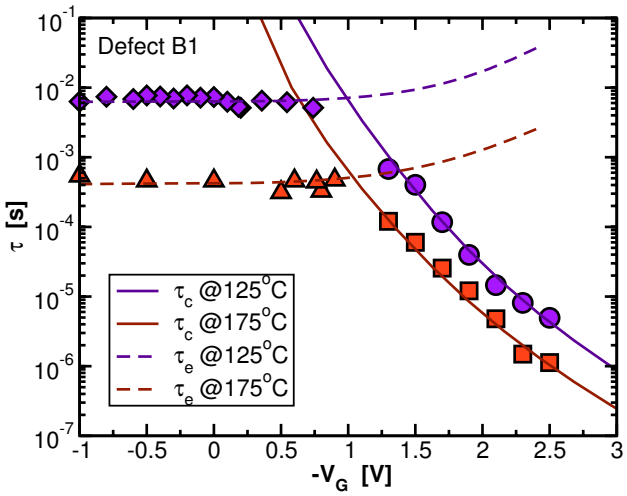

Figure 5.2: The capture and emission time characteristics for defect B1 identified in a SiON pMOSFET is shown at two different temperatures. Defect B1 has a bias independent emission time, a behavior referred to as *fixed charge trap*. The lines are calculated by the four-state NMP model which nicely reproduces both characteristics [MWC25].

In all our single defect investigations the step heights are widely distributed from several hundred millivolt up to 50 mV and even higher depending on the device geometry. Furthermore, in many cases the distribution can be well approximated by an exponential distribution. The smallest detectable step heights are a consequence of the limited current measurement resolution and the device geometry. As the average step height becomes smaller with increasing channel area the number of defects producing experimentally resolvable ΔV_{th} shifts decreases and are visible as measurement noise thereby obscuring the recovery traces. The detectable step heights using the TMI at the best current resolution are around 0.1 V and 0.5 V for SiON nMOSFETs and high-k MOSFETs, respectively, see Chapter 8 and Chapter 9.

In most cases single defects can be unambiguously identified by their capture and emission time as well as their step heights. The capture times themselves depend on the gate bias and on the device temperature. Although the emission times are temperature dependent too, they have been observed to be either bias independent, so called *fixed traps* or bias dependent, so called *switching* traps, shown in Figure 5.2 and Figure 5.3, respectively. The previously introduced four-state NMP model has been developed to explain the bias and temperature dependence of these defects. From the simulations the location of the trap inside the oxide and its energy level can be estimated. As the four-state NMP requires several parameters which describe complex dependencies of the

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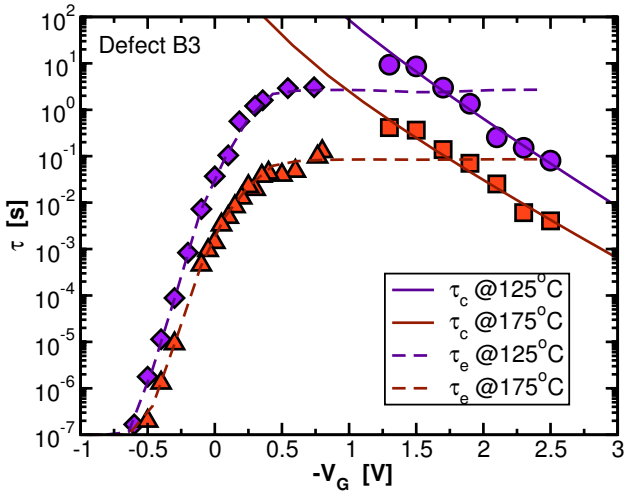

Figure 5.3: The emission time of defect B3 strongly depends on the recovery bias, a behavior referred to as *switching trap*. Above a certain voltage the emission time saturates and becomes bias independent. Again, the four-state NMP model nicely explains the observed characteristics [MWC25].

model itself, detailed knowledge of the charge transition times over a wide gate voltage range are required. Therefore DC stress, pulse stress and AC stress signals are used within the framework of TDDS to achieve meaningful trapping time characteristics for single defects.

5.1. Defect Analysis for the Time-Dependent Defect Spectroscopy

When a nanoscale device is subjected to BTI stress, a defect can become charged if its *(i)* a capture time is smaller than the stress time $\tau_c < t_s$ and *(ii)* if it is energetically realigned below or above the Fermi-level for the applied stress bias in case of a pMOSFET or nMOSFET, respectively. When a recovery bias is applied at the gate contact, the trap level is shifted above/below the Fermi-level and the defect can become uncharged. The charge emission event of several defects is visible in the recovery traces in Figure 5.4. Also visible is a defect producing RTN which is characterized by subsequent charge capture and emission events.

5.1.1. Charge Emission Time Extraction

Next, the measured recovery traces have to be analyzed for discrete shifts in ΔV_{th}. For this a sophisticated step detection algorithm is used, which is described in detail in Chapter 7. The extracted emission events occurring at τ_e with step height d are then collected in the emission time versus step height (τ_e, d) plane, called spectral map. Therein each single charge emission event is marked, see Figure 5.5. By collecting all charge emission events from repeatedly measured recovery traces recorded at the same bias conditions, stress/recovery time, and device temperature the emission events form clusters in the spectral map. Each cluster delivers information about the defect step height and emission time. The latter can be calculated as the average of all single emission events contributing to a certain cluster by

$$\tau_e = \frac{1}{N_e} \sum_{i=0}^{N_e-1} \tau_{e,i} \tag{5.1}$$

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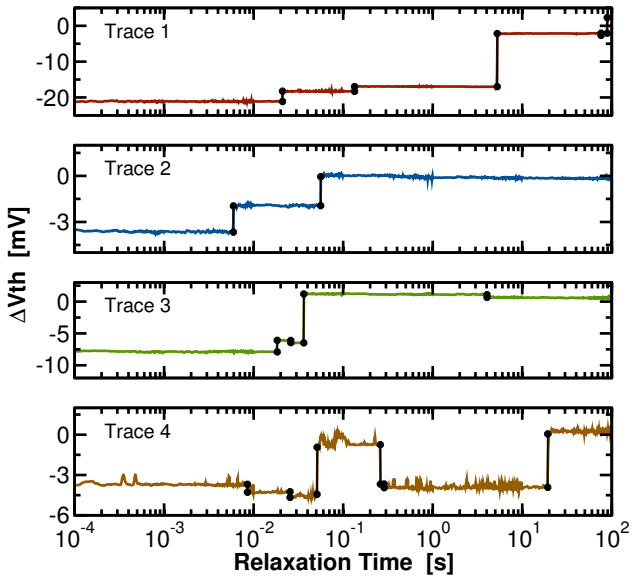

Figure 5.4: Four selected recovery traces recorded on an SiON pMOSFET are shown. As can be seen, the device recovery proceeds in discrete steps with various typical step heights. In particular, trace four shows a defect which produces RTN as it captures the charge immediately after the trap has been neutralized.

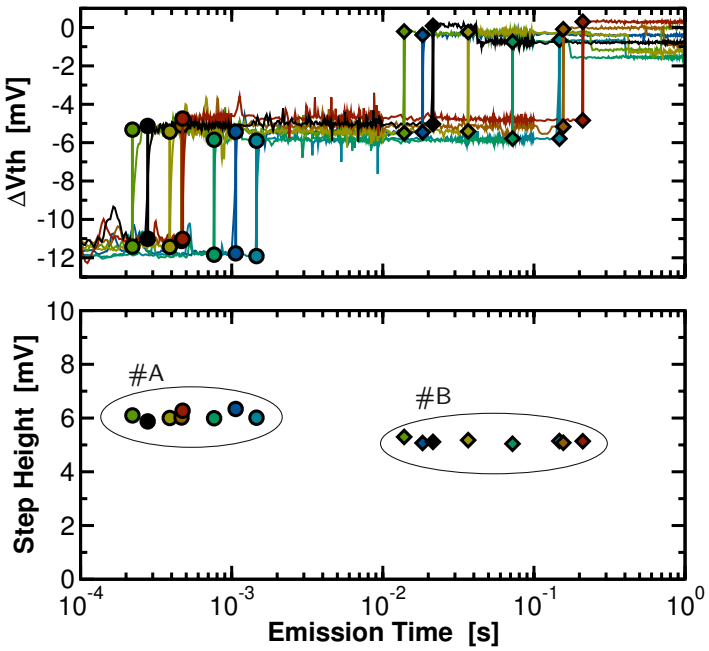

Figure 5.5: (top) The recovery traces are analyzed for discrete ΔV_{th} steps. **(bottom)** Afterwards, the steps are collected in the (τ_e, d) plane, which we call spectral map. As can be seen, the single emission events form clusters which are considered as the fingerprint of a single defect.

with N_e the number of emission events. In the spectral map shown in Figure 5.6 based on the measurement data recorded using a SiON pMOSFETs with a geometry of $W = 160\,\text{nm}$ and $L = 120\,\text{nm}$. As can be seen, six defects with various step heights and widely distributed emission times are are visible.

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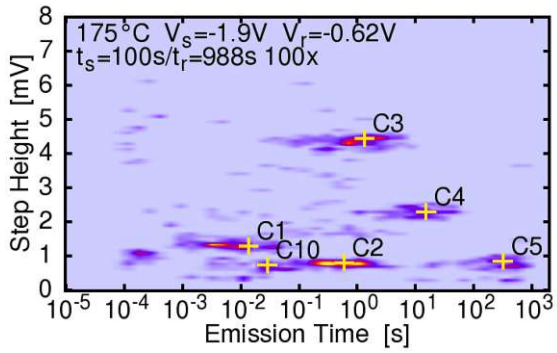

Figure 5.6: A spectral map showing six defects with different emission times and step heights. The cluster have been extracted from 100 recovery traces recorded at the stress and recovery conditions and at a constant device temperature [MWC22].

5.1.2. Charge Capture Time Extraction

As previously shown, the average emission time is calculated from typically 100 recovery traces, each measured under the same experimental conditions. In contrast, the charge capture time can not be determined directly. To extract the capture time DC stress/measurement sequences with increasing stress times are used. During the stress phases a constant stress bias $V_{G,s}$ is applied at the gate for a certain stress time t_s. Under these circumstances, the expectation value of the occupancy, which is the probability of a defect to become charged during stress, follows

$$O(t_s) = A(1 - e^{-\frac{t_s}{\tau_c}}) \tag{5.2}$$

with A the equilibrium occupancy observed after indefinitely long stress. When switching to recovery bias conditions the defect become discharged and the occupancy functions then reads

$$O(t_s, t_r) = A(1 - e^{-\frac{t_s}{\tau_c}})e^{-\frac{t_r}{\tau_e}}. \tag{5.3}$$

The correlation between different stress times and the occupancy function is shown in Figure 5.7. Obviously, the longer the device is stressed the more likely the defect becomes charged. Given that the used recovery gate bias and recovery time guarantee $O(t_{r,max}) = 0$, the defect will very likely emit its charge during recovery, presuming the defect has been charged during stress. Thus by repeatedly stressing the device and recording the device recovery, the number of charge capture transitions during stress equals the number of emission events during recovery. Using (5.2), the capture time can be extracted by analyzing typically 100 traces at different stress times, see Figure 5.8.

5.1.2.1. Advanced Extraction of Charge Emission Time

By applying the DC measurement method the bias dependence of the emission time can only be studied in a very narrow gate voltage range. For pMOSFETs, for $V_{G,r} \gg V_{th}$ leads to a large drain-source current during device recovery. As the measurement resolution decreases towards higher current ranges of the measurement unit, the value for the smallest measurable step heights increase. Towards $V_{G,r} < V_{th}$ the drain-source current becomes very small close to the measurement resolution, see Figure 5.9. To circumvent this limitation the DC stress signal is extended by

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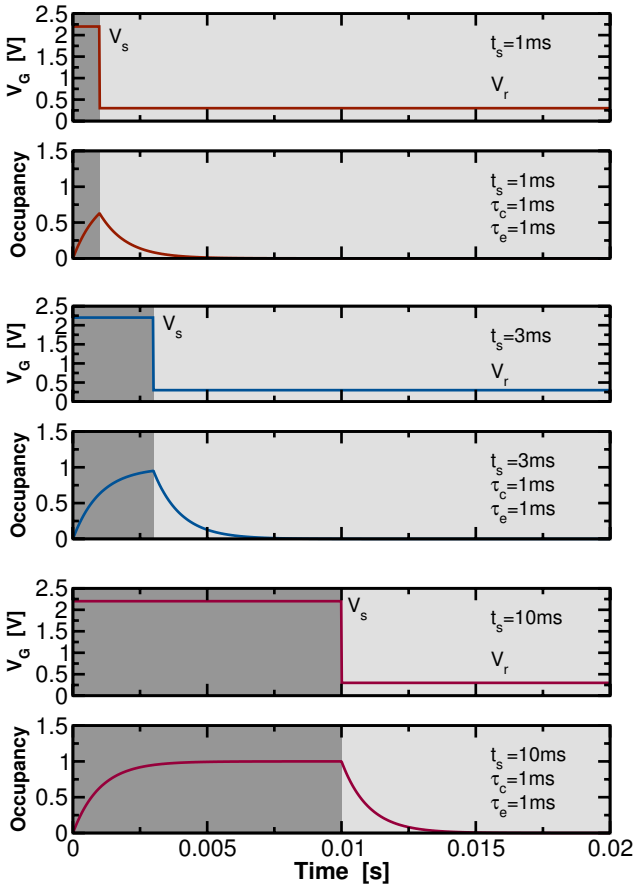

Figure 5.7: The defect occupancy during the DC stress/recovery cycle is plotted for different stress times ((**top**) $t_s = 1\,\text{ms}$, (**middle**) $t_s = 3\,\text{ms}$ and (**bottom**) $t_s = 10\,\text{ms}$). For larger stress times the probability of the defect to charge during stress, which is also called the occupancy, increases. Note, the recovery time has to be large enough to guarantee $O(t_{r,max}) \approx 0$. If t_r is to short the defect can not emit within the measurement window, leading to large errors in the capture times.

an additional accumulation voltage pulse V_p, see Figure 5.10. The modified occupancy function then becomes

$$O(t_s, t_p, t_r) = A(1 - e^{-\frac{t_s}{\tau_c}})e^{-\frac{t_p}{\tau_p}}e^{-\frac{t_r}{\tau_e}}. \tag{5.4}$$

with τ_p the voltage pulse width.

The idea behind the additional voltage pulse is very simple. Under the assumption that, the stress time and the stress voltage of the conventional DC stress cycle lead to $O(t_s) = A = 1$, implying the defect has been charged, the accumulation voltage pulse can discharge the defect. If this is the case, this defect will not contribute to the subsequent recovery trace. Conversely, if the defect is not discharged during the accumulation pulse, the charge emission will occur during relaxation and the corresponding ΔV_{th} step will be visible in the recovery trace. As charge emission is a stochastic process, the probability of the defect to emit during recovery strongly depends on the choice of V_p and t_p. By repeatedly performing the experiment using the same biases and times, the probability of the defect to emit its charge during t_p can be extracted by counting the number of emission events during subsequent device recovery. Analogously to the charge capture events, the dependence of the number of emission events on the voltage pulse width can be described by an exponential function

$$O(t_p) = Ae^{-t_p/\tau_p}. \tag{5.5}$$

An example for the extraction of the emission time using an additional accumulation voltage pulse during stress is shown in Figure 5.11.

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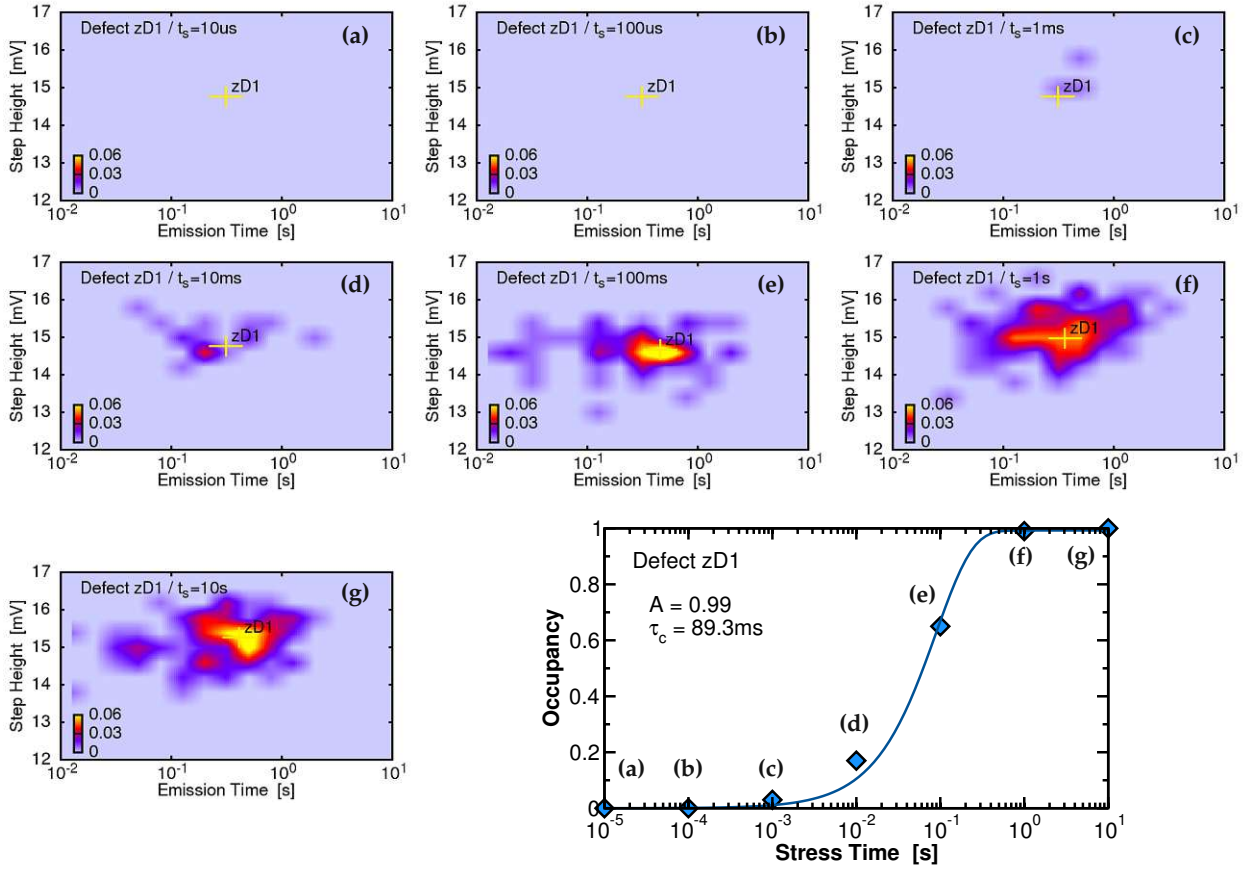

Figure 5.8.: The spectral maps show that with an increasing stress time the occupancy of the defects increase, thus the number of emission events increases. The occupancy can be directly calculated for each stress time as the ratio between the number of emission events N_e and the number of traces N_N, i.e $O(t_s) = N_e/N_N$. As can be seen, the latter shows an exponential dependence on the stress time, from which the capture time can be estimated by applying (5.2).

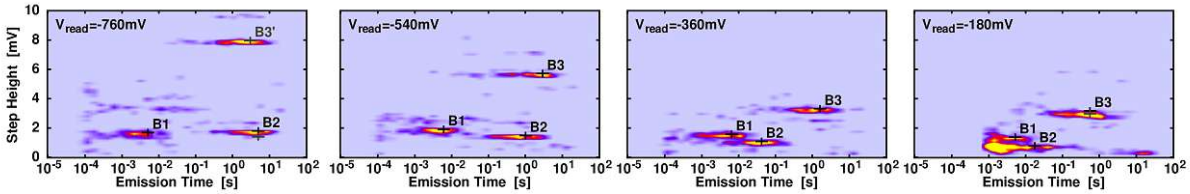

Figure 5.9.: The spectral maps show defects B1, B2 and B3 measured on a pMOSFET with $V_{th} \approx -400\,mV$. Towards larger recovery bias, the step heights of the clusters decrease. For $V_{G,r} = -180\,mV$ the defects B1 and B2 begin to overlap. A further increase of the recovery bias would fuse the two clusters to a single one and hamper the extraction of the capture and emission time [MWC25].

The impact of the voltage pulse on the defect occupancy for the defects B1 and B3 is shown in Figure 5.12 and Figure 5.13, respectively. For the fixed trap B1 the occupancy is not affected by V_p, thus a bias independent emission time characteristic is obtained. For defect B3, the exponential occupancy characteristic is shifted towards shorter times for an increased voltage pulse.

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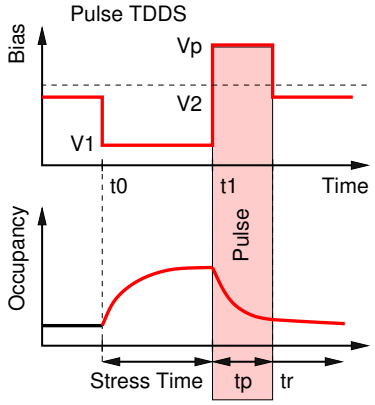

Figure 5.10: The concept of the *dynamic* TDDS extends the DC stress scheme by introducing a voltage pulse, with width t_p and bias V_p, immediately before the recovery bias is applied. For an accumulation voltage pulse, the emission process is accelerated, visible by a considerable change of the occupancy during t_p [MWC25].

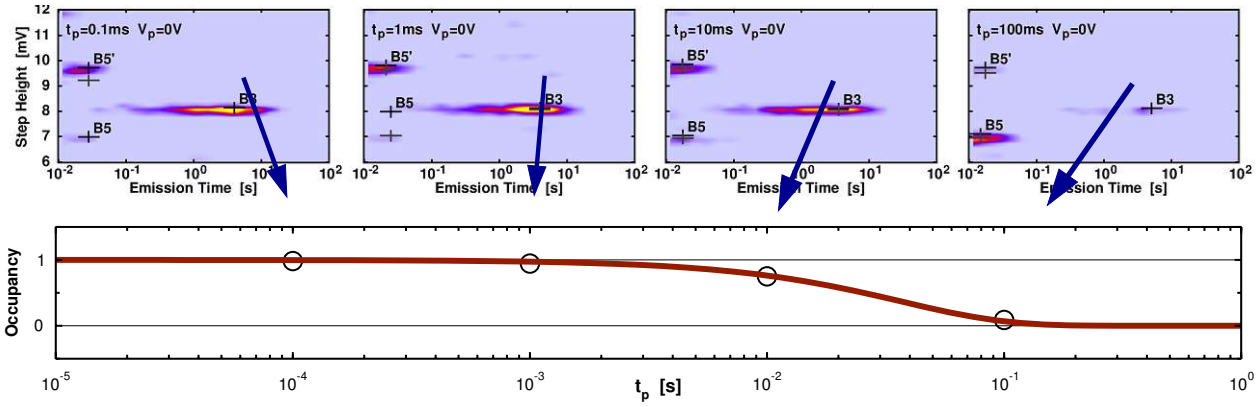

Figure 5.11.: The spectral maps recorded using pulse stress signal at different pulse width t_p show a cluster assigned to defect B3. As can be seen, with increasing t_p the cluster occupancy decreases, a consequence of the reduced number of emission events contributing to it. Analogously, the defect occupancy decreases and follows an exponential behavior. By using (5.5) the dynamic TDDS allows to determine the emission for accumulation biases [MWC25].

5.1.2.2. Combination of Conventional and Dynamic Time-Dependent Defect Spectroscopy

To considerably extend the gate bias range for the extraction of the charge capture emission time a voltage pulse, that is the dynamic TDDS, between the DC stress and recovery period is introduced, see Figure 5.14. As previously mentioned, the capture time can not be extracted directly from the recovery traces. Therefore, a similar measurement scheme has to be applied as for the extraction of the emission time using pulse measurements.

5.1.3. Application of Capture and Emission Time Extraction

As long as the recovery traces only show emission events which have significantly different step heights and disjunct emission times, the identification of the single defects is straightforward. However, this case is not always guaranteed, and thus fully automatic device characterization is very challenging. The evaluation of TDDS data requires considerable care. In order to demonstrate some difficulties during cluster detection and further analysis, assume two defects with their

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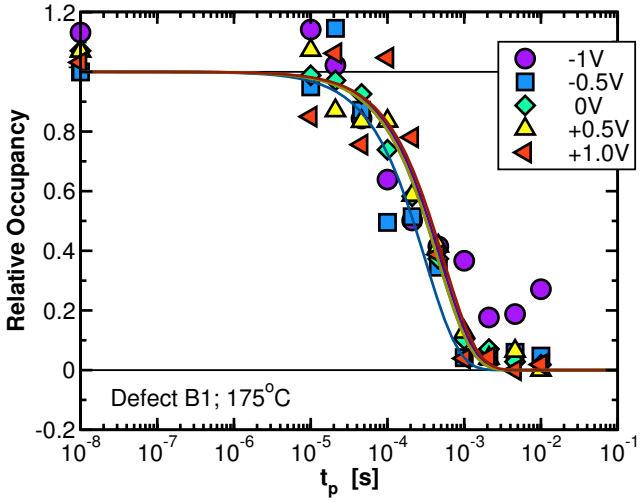

Figure 5.12: The occupancy of defect B1 remains unaffected by varying V_p. As a consequence B1 has a bias independent emission time which we link to fixed oxide traps [MWC25].

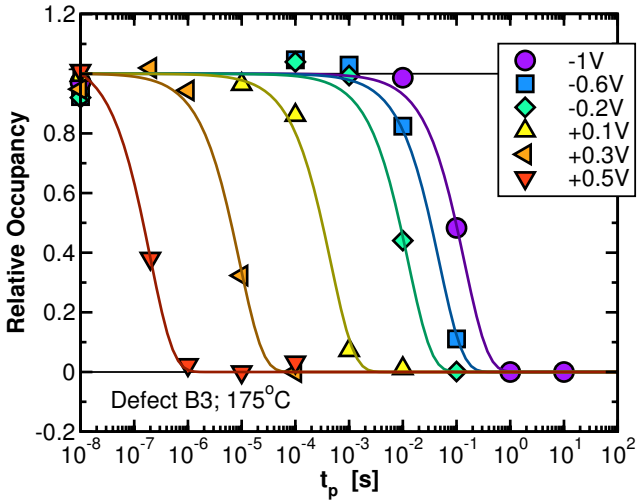

Figure 5.13: For the switching trap B3 the emission time changes with bias. As a consequence, the mean occupancy is shifted towards shorter times when V_p is increased [MWC25].

emission times very close to each other, but with different step heights, see Figure 5.15. Again, the (τ_c, d) tuple extracted from the recovery traces form two clusters around the corresponding mean step heights and emission times. Nevertheless, when these two traps emit within the same data sampling interval, a large cumulative ΔV_{th} shift occurs. As a consequence, a third cluster in the spectral map is visible. The step height of this cluster equals the sum of the two initial traps, and is arranged around the overlap of the initial clusters. Thus this coincidence that both defects emit at the same time leads to a reduced occupancy. This can lead to slightly shifted emission times. This concern has also be addressed when calculating the charge capture time. The extraction of τ_c relies on counting the emission events at different stress times. Following from that, the calculated capture time is distorted which in turn leads to an error of the parameterset extracted by the four-state NMP model.

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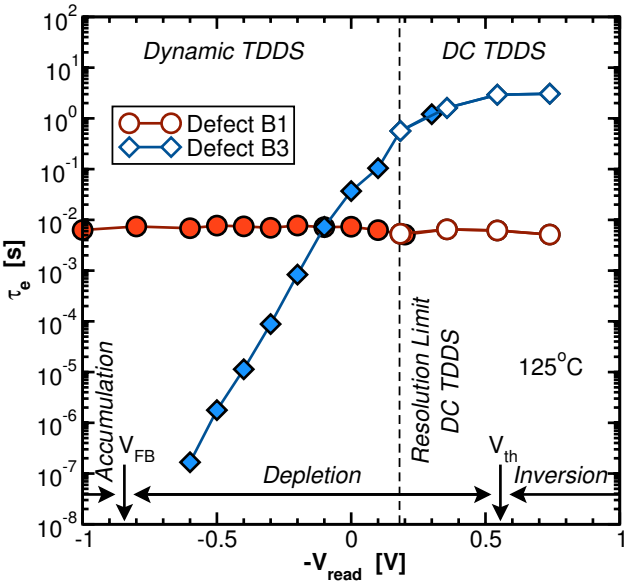

Figure 5.14: The conventional DC TDDS allows for direct extraction of the emission time. Once the measurement resolution limit of the conventional DC TDDS is reached, the dynamic TDDS allows further extraction of τ_e towards accumulation voltages. With the combination of both methods the trapping kinetics can be studied over a wide gate voltage range. From that, trap parameters with reduced uncertainties can be calculated using the four-state NMP model [MWC25].

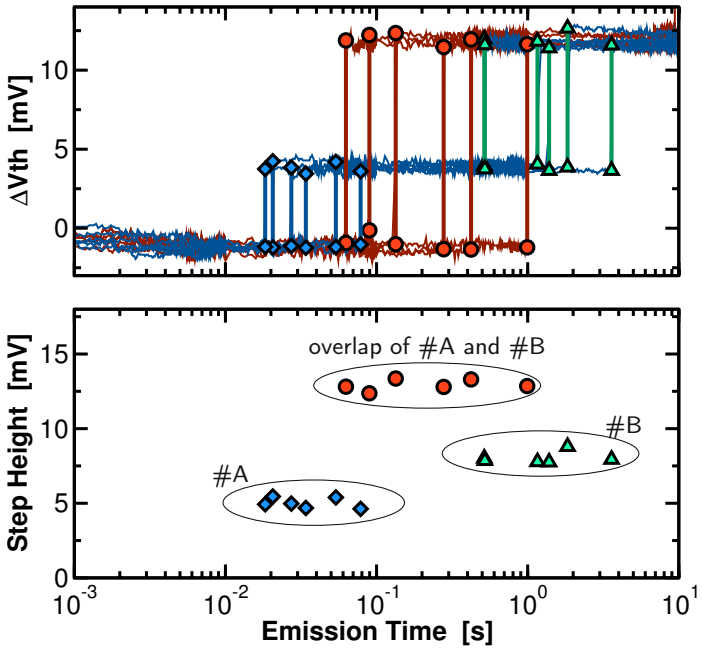

Figure 5.15: The analysis of two defects with emission time within the same decade requires special care. In this case typically a third cluster appears in the spectral map representing simultaneously occurring emission events. As a consequence, the occupancies in the initial clusters is reduced as the number of emission events contributing to it is decreased. This leads to distorted capture and emission times.

5.2. Frequency Dependence of the Transition Times

To study the frequency dependence of the transition time, the DC stress signal of the conventional TDDS is replaced by an AC stress signal, see Figure 5.16. The capture probability of the defect, that is the defects occupancy during the stress cycle, increases during the high cycles and decreases during the low cycles of the AC signal. From the two-state perspective, the capture probability only depends on the effective stress time $t_{s,eff} = \alpha t_s$, which is primarily determined by the duty cycle α of the AC stress signal and the overall stress time t_s. Thus the two-state model does

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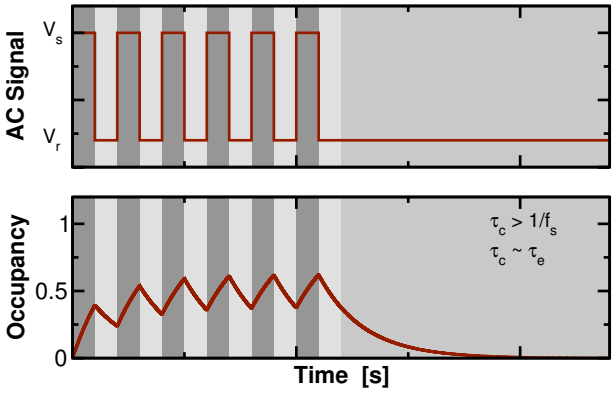

Figure 5.16: (top) During AC BTI stress the gate bias switches between $V_{G,s}$ and $V_{G,r}$ with the signal frequency f. **(bottom)** From the two-state perspective, the occupancy of the defect on depends effective stress time $t_{s,eff}$ which is the product between the duty cycle and total stress time. In the underlying case, the defect has a similar capture and emission time which are larger than $1/f_s$. Otherwise the defect will be either be permanently charged or discharged during the AC stress cycle.

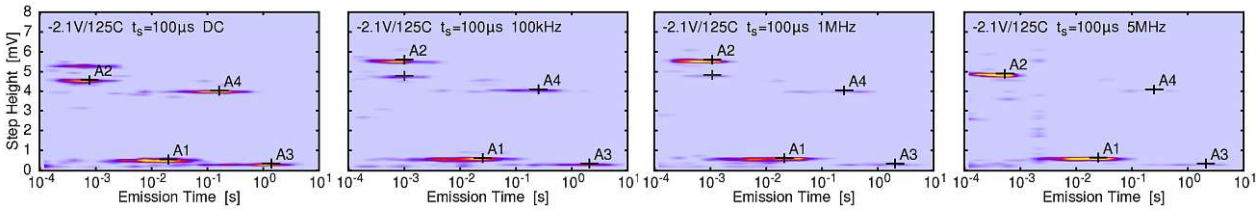

Figure 5.17.: (a) The conventional DC TDDS is used to identify four defects, namely A1 to A4. **(b-d)** By increasing the frequency of the AC stress signal it is observed that the clusters of defects A3 and A4 become fainter. Thus these defects show a visible dependence on the frequency of the AC stress signal which can be explained by an increase of the capture time at higher frequencies. Such a behavior cannot be explained using a two-state model [MWC25].

not implicate any frequency dependency of the charge capture and emission times. However, by performing AC stress experiments defects have been found which show frequency dependent capture times, see Figure 5.17. The defects A1 and A2 visible in the spectral maps do not show any frequency dependence because they have a capture time below $\tau_c < 10\,\mu s$, which is shorter than the AC stress pulse width. In contrast, the clusters for the defects A3 and A4 become fainter with increasing frequency. This can be explained with increased capture times at higher frequencies which leads to a reduced capture probability at the end of the AC stress cycle. Quite remarkably, the frequency dependence of the capture times can be nicely reproduced by the four-state NMP model, shown for defect A3 in Figure 5.18.

In general, experiments using high frequency AC signals exceeding 1 MHz have to be thoroughly designed as capacitive and inductive couplings may affect the measurements. Reference measurements have to be performed to guarantee the signal integrity of the configuration. Nonetheless, AC measurements using frequencies from several MHz up to GHz require special test structures. Recently, an on-chip oscilloscope has been proposed to study the frequency dependence of NBTI and PBTI of high-k transistors [162]. Although PBTI was found to be frequency independent for $f > 75\,kHz$, NBTI appears to be frequency dependent up to at least $f = 30\,MHz$. The former is in agreement with the frequency dependent capture time of defect A3, see Figure 5.18, as this investigations were performed on a pMOSFET as well.

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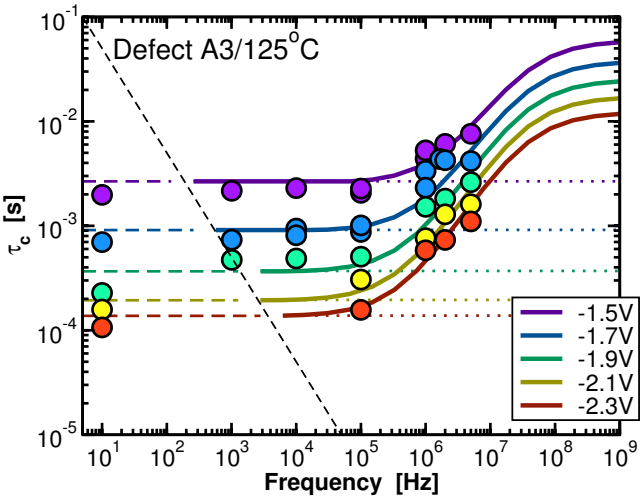

Figure 5.18: With an increase of the AC stress frequency, the charge capture time of defect A3 increases. The lines are calculated with the four-state NMP model which very well reproduces the frequency dependent capture times [MWC25].

5.3. Temperature Dependence

During extensive single trap investigations, the capture and emission times of single traps have been observed to change with device temperature. Their temperature dependence can be described using an Arrhenius' Law and follow the relation

$$\tau_{c,e}(T) = \nu e^{\frac{q_0 E_A^{c,e}}{k_B T}} \tag{5.6}$$

with k_B the Boltzmann constant, q_0 the elementary charge, T the absolute temperature, the attempt frequency ν, and the activation energy $E_A^{c,e}$ for charge capture and charge emission, respectively. Typical activation energies E_A are in the range of 0.5 eV up to 2 eV limited by the measurement resolution for both charge capture and emission of defects in SiON and high-k transistors [MWC25, MWC20, MWC4].

5.4. Step Height Distribution Function

In order to study the average contribution of single traps to the ΔV_{th} shift, the complementary cumulative distribution function (CCDF) the of step heights can be calculated from a large number of devices. The CCDF plot shown in Figure 5.19 demonstrates that the step heights are exponential distributed and can be described by the probability distribution function (PDF)

$$f(\Delta V_{th}) = \frac{1}{\eta} e^{-\frac{\Delta V_{th}}{\eta}} \tag{5.7}$$

with η the mean threshold voltage shift induced by a single charge. Furthermore, the cumulative distribution function (CDF) of the step heights is given by

$$F(\Delta V_{th}) = 1 - e^{-\frac{\Delta V_{th}}{\eta}}. \tag{5.8}$$

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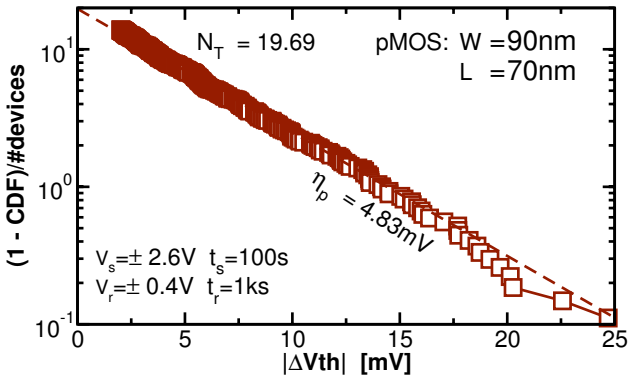

Figure 5.19: The step height distribution function for SiON pMOSFETs can be described with a unimodal CCDF. From the CCDF normalized to the number of devices the active trap density can be directly obtained as the intersection between the extension of the CCDF and the ordinate.

To study the step height distribution, the complementary cumulative distribution function can be used and normalized to the number of devices

$$\mathrm{CCDF}(\Delta V_{\mathrm{th}}) = \frac{1 - F(\Delta V_{\mathrm{th}})}{N_{\mathrm{devices}}} = N_{\mathrm{T}} \mathrm{e}^{-\frac{\Delta V_{\mathrm{th}}}{\eta}}. \tag{5.9}$$

The advantage of this formulation is that the number of traps per device N_{T} is directly accessible from the plots. In recent investigations exponentially distributed amplitudes have been found for RTN signals [163, 164, 165]. These findings strengthen the link between RTN and BTI [166, 126]. Furthermore, the average contribution of a single trap to the threshold voltage shift η plays an important role in the context of device variability in deeply scaled devices [165, 167, 168].

In pMOSFETs employing a high-k gate stack the step height distribution functions are found to be bimodal, see Chapter 9 [169, MWJ1]. Such a behavior can be described by the sum of two unimodal CCDFs given by

$$1 - \mathrm{CDF} = A_1 \mathrm{e}^{-\frac{\Delta V_{\mathrm{th}}}{\eta_1}} + A_2 \mathrm{e}^{-\frac{\Delta V_{\mathrm{th}}}{\eta_1}}. \tag{5.10}$$

5.5. Capture/Emission Time Approach in Large-Area Devices

So far the trapping kinetics of single defects in nanoscale devices have been described by their capture/emission time characteristics. Now this approach will be extended to large-area devices. Therefore, the capture/emission time distribution function $g(\tau_{\mathrm{c}}, \tau_{\mathrm{e}})$, which gives the number of defects contributing to ΔV_{th} within the interval $[\tau_{\mathrm{e}}, \tau_{\mathrm{e}} + \mathrm{d}\tau_{\mathrm{e}}]$ and $[\tau_{\mathrm{c}}, \tau_{\mathrm{c}} + \mathrm{d}\tau_{\mathrm{c}}]$, is introduced. Therefrom the threshold voltage shift can be calculated via [90]

$$\Delta V_{\mathrm{th}} \approx \int_0^{t_{\mathrm{s}}} \mathrm{d}\tau_{\mathrm{c}} \int_{t_{\mathrm{r}}}^{\infty} \mathrm{d}\tau_{\mathrm{e}} g(\tau_{\mathrm{c}}, \tau_{\mathrm{e}}). \tag{5.11}$$

Hence defects contributing to ΔV_{th} have been charged until t_{s} and are not discharged after t_{r}. Furthermore, by reformulating (5.11) to

$$g(\tau_{\mathrm{c}}, \tau_{\mathrm{e}}) \approx \frac{\partial^2 \Delta V_{\mathrm{th}}(\tau_{\mathrm{c}}, \tau_{\mathrm{e}})}{\partial \tau_{\mathrm{c}} \partial \tau_{\mathrm{e}}} \tag{5.12}$$

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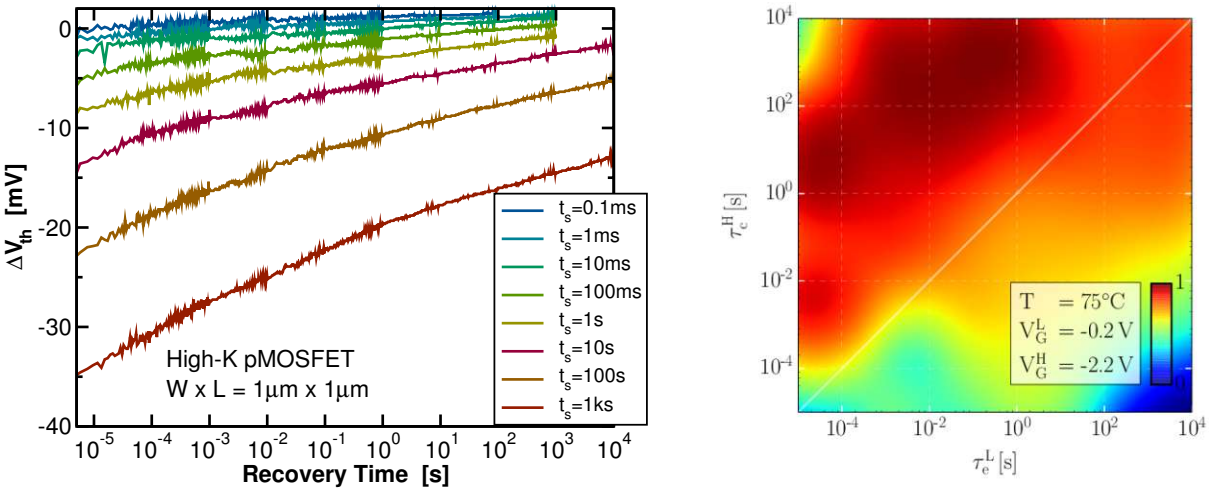

Figure 5.20.: (left) The recovery traces are recorded for different stress and recovery times using a high-k pMOSFET. **(right)** Using (5.12) the CET map is directly calculated from the measurement data. Note that the capture time refers to stress bias and the emission time refers to recovery bias. The recovery traces have been recorded with our developed measurement instrument.

the capture emission time (CET) map can be directly calculated from a set of experimental recovery traces recorded for different stress times, see Figure 5.20. Equation (5.12) is used in Chapter 9 to compare simulated CET maps with CET maps directly calculated from measurements. As will be shown, the simulations reproduce the characteristics of the experimental CET map, confirming the accuracy of this approach.

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6 Experimental Setup

To experimentally characterize BTI and the single traps responsible for the degradation of the device performance, sophisticated measurement tools are necessary. In recent investigations BTI has been studied in a large variety of devices, like *(i)* conventional SiON or SiO_2 MOSFETs, *(ii)* high-k MOSFETs, *(iii)* GaN metal-oxide-semiconductor high-electron-mobility transistors (MOSHEMTs) or *(iv)* more exotic transistors using 2D materials. Apparently, numerous general purpose instruments are available, but most of them are either very costly or do not cover the large list of requirements. Furthermore, since these measurements typically drive the equipment toward their limits, unexpected behavior is often observed, like undocumented settling periods at zero volts for transitions from positive to negative voltages. This undocumented behavior was observed regularly in our previous attempts and is also regularly reported by our partners. Furthermore, for these setups a range of different tools are required which have to communicate seamlessly. Particularly for long-term experiments it was regularly observed that setups using off-the-shell equipment occasionally produced communication errors or crashed for other reasons. These failures were virtually impossible to track down due to the lacking documentation of the equipment internals. In order to maintain complete control over the delicate measurements setup, an elaborate measurement setup to study single defects in nanoscale MOSFETs has been developed during the previous years. In the following, the requirements for BTI characterization and the basic measurement concepts are discussed, followed by a detailed presentation of the developed equipment.

6.1. Requirements for Time-Dependent Defect Spectroscopy Measurements

To collect experimental data for BTI analysis, very fast measurement methods are necessary because recovery starts immediately after stress, is very fast, and continues for very long times. Furthermore, the threshold voltage shift has to be monitored with a high resolution in time and voltage. While the high time resolution is required to properly resolve RTN signals, the high

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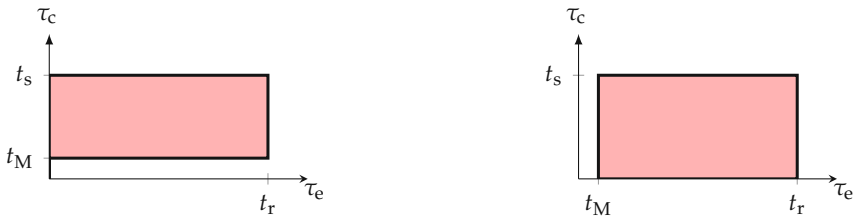

Figure 6.1.: The accessible capture and emission time ranges are limited by the stress time t_s, the measurement delay t_M and the measurement window t_r. For the (**left**) MSM method all defects with $\tau_c < t_s$ and $t_M < \tau_e < t_r$ are accessible whereas for (**right**) OTF methods defects with $t_M < \tau_c < t_s$ and $\tau_e < t_r$ can be accessed.

ΔV_{th} resolution is required to study very small threshold voltage shifts below 1 mV. Such ΔV_{th} shifts typically correspond to shifts in the drain-source current of less than 0.1 nA. The high ΔV_{th} resolution is particularly important because only a few defects are beneficially aligned (from an experimental perspective) to the conducting channel to produce large ΔV_{th} shifts. Most ΔV_{th} shifts are close to the measurement limit of conventional setups.

Common ways to measure a ΔV_{th} drift are the *(i)* OTF method, the *(ii) fast* V_T method or the *(iii) fast* I_{DS} method [87], see Section 1.7. The OTF method allows to monitor the threshold voltage shift during device stress without any interruption. Thus defects with a capture time smaller than the measurement delay, that is $\tau_c < t_M$, are not accessible by OTF methods, because they require to measure the first-data point, see Figure 6.1 (left).

In contrast to OTF methods, the capture time window is limited by the stress time t_s, that means $\tau_c < t_s$, and the emission time window is limited by the measurement delay and the recovery time leading to $t_M < \tau_e < t_r$, see Figure 6.1 (right). The measurement delay is thereby defined by the measurement equipment and should be held as short as possible. This can be particularly difficult when studying single charge trapping in nanoscale transistors as this requires a current resolution of several tens of pico-amperes. Furthermore, as will be demonstrated later, the measurement delay is related to the noise level of the recovery traces because the larger the sampling frequency is, the larger the noise level of the sampled signal gets. As a consequence, the minimum detectable step height for single trap BTI investigations increases. In contrast to the measurement delay, there is no theoretical limit for the maximum recovery time.

The *fast* V_T and the *fast* I_{DS} method are based on the MSM principle where the device is repeatedly stressed and monitoring of the device recovery is started immediately after stress release, see Figure 6.2. A feedback loop of an OPAMP is used to control the gate voltage at the *fast* V_T method, see Figure 1.19. In contrast, the *fast* I_{DS} method relies on the direct measurement of the drain-source current I_{DS} and the gate current I_G. Afterwards, the drain-source current is converted into a threshold voltage shift ΔV_{th} using the $I_{DS}(V_{GS})$ characteristics of the device recorded prior to the stress/recovery measurements. It has to be noted that the selection of the correct $I_{DS}(V_{GS})$ characteristics for the extraction of ΔV_{th} is of utmost importance, since each transistor accumulates a long term degradation through all measurement cycles and the sub-threshold slope may change during BTI stress. If I_{DS} is converted to ΔV_{th} using an $I_{DS}(V_{GS})$ recorded immediately before each MSM sequence, the remaining degradation from the previous recovery cycle of the total ΔV_{th} is

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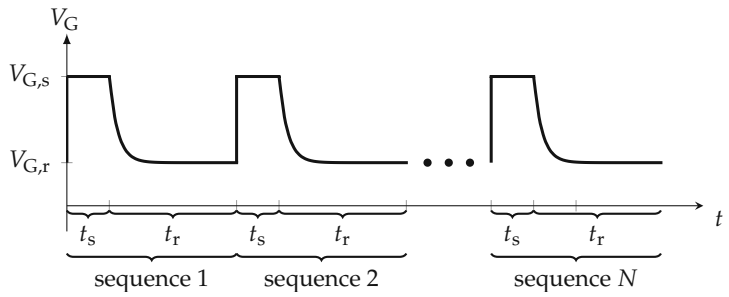

Figure 6.2: Using the MSM method the device is stressed repeatedly and the recovery behavior is monitored between the stress cycles. Note that the switching transient between stress and recovery bias has to be held as short as possible. This is necessary to minimize recovery during the time the voltage level changes.

lost. Conversely, if the conversion of the I_{DS} to ΔV_{th} is based on an initial $I_{DS}(V_{GS})$ changes of the subthreshold slope and the threshold voltage will not be transferred to the ΔV_{th}. In summary, there are several ways to calculate the ΔV_{th} whereas the choice of the reference $I_{DS}(V_{GS})$ depends on the experimental questions.

In both MSM concepts the measurement delay is primarily defined by the switching transient between stress and recovery phases and has to be held as short as possible. Furthermore, a detailed knowledge of the transient behavior is required to perform accurate device simulations. As previously mentioned, using a general purpose instrument we noticed that some additional delay at the output voltage of 0 V was introduced when directly switching from a positive output voltage to a negative output voltage and vice versa. Such additional delays have to be avoided during all measurement routines.

6.2. Time-Dependent Defect Spectroscopy Measurement Instrument

In order to provide an experimental setup which allows full control of the experimental parameters, that are the output voltages and the corresponding switching behavior between different voltage levels as well as different data acquisition scheme and control output, the TMI has been invented. Although, the TMI has been initially designed to perform TDDS experiments it turned out that due to the modular design the TMI can be easily adjusted characterize large-area transistors and much more. The following section gives an overview of the design of the TMI and summarizes the main features.

6.2.1. Design of the Time-Dependent Defect Spectroscopy Measurement Instrument

The overall application of the TMI can be separated into three main tasks: *(i)* providing defined output voltage characteristics (static or transient), *(ii)* record input voltages or currents, and *(iii)* provide an interface between the TMI and the device under test. In addition, an external digital I/O interface for synchronization between different instruments or external devices is available. The TMI can be controlled via an USB interface.

The schematic shown in Figure 6.3 provides an overview of the modular design of the TMI. The

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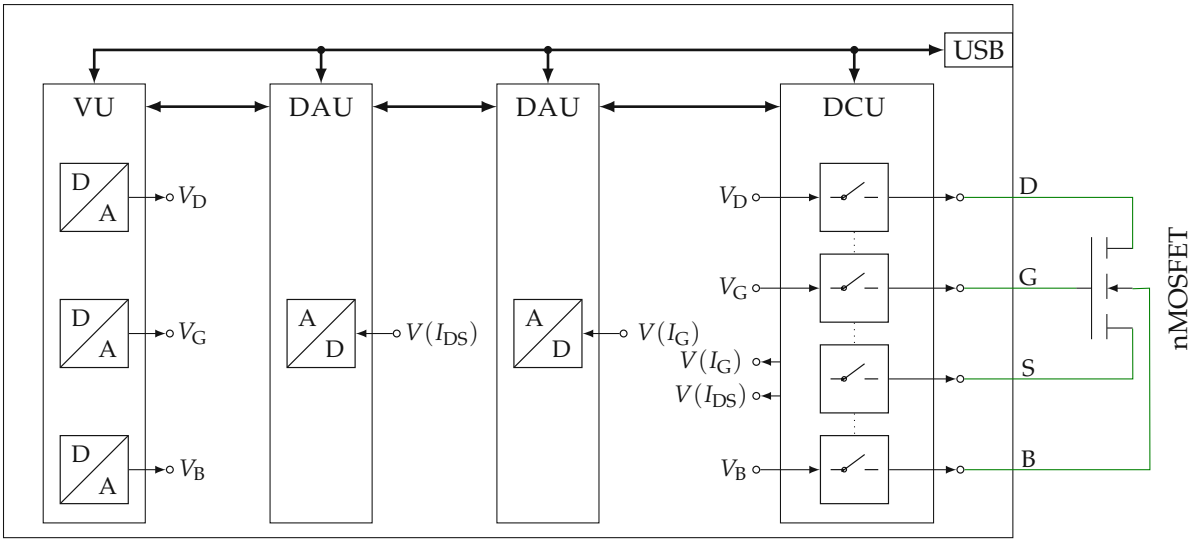

Figure 6.3.: In the standard configuration the TMI is equipped with one voltage unit (VU) providing three synchronized output voltages, two data aquisition units (DAUs) to monitor I_{DS} and I_G and the device connector unit (DCU), which is the link to the device under test.

standard configuration contains one VU providing programmable output signals, up to two DCUs used to monitor input voltage signals and providing external control lines, and one DCU as the link between the TMI and the device under test. The external control lines can be used to synchronize the DCUs with external general purpose instruments or voltage sources. Furthermore, additional hardware, such as polyheater controller units, can be connected to the TMI using the external I/O port. The voltage and data acquisition units are directly controlled via a USB interface. A backbone bus system is used to synchronize the individual units, to exchange control information and to connect the digital and shielded analog power supply.

In addition, the schematic in Figure 6.3 shows the configuration used to measure the drain-source and gate current of an nMOSFET. As can be seen, all terminals of the device under test are connected to the DCU, which provides output buffers and current to voltage converter units. The biases forwarded by the DCU are provided by the VU which is itself connected to the former. Furthermore, the single DAUs are connected to the appropriate outputs of the DCU providing measurable voltages proportional to the drain-source and gate current. Note that all outputs of the DCU are initially floating and are connected only immediately before the measurement. This is important as it has been found that even at zero gate bias MOSFETs accumulate a ΔV_{th} shift, see Chapter 10.

6.2.1.1. Voltage Unit

The concept of the VU is shown in Figure 6.4. In the entire design the digital and analog components are electrically isolated from each other in order to guarantee low noise in the analog output signals.

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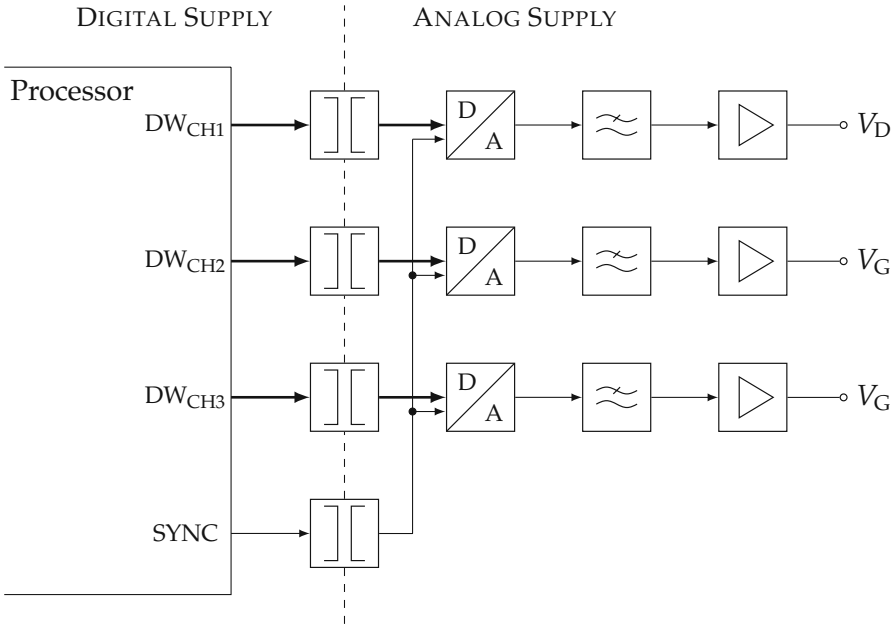

Figure 6.4.: The schematic of the VU shows the three output DACs together with the corresponding output amplifiers. The digital control lines of the processor are decoupled from the analog area. The processor itself is connected to the backbone bus system for data exchange and synchronization purposes. The bus connections between the processor and the DAC are emphasized by thicker lines.

The main unit of the digital part is an ARM processor, which also provides the USB interface for external communication. Furthermore, the processor is connected to an internal bus system to exchange control information with other modules and to provide a synchronized timing behavior. Furthermore, the digital and shielded analog power-supply are distributed by the backbone bus system.

The analog part consists of three DACs controlled by 16 bit data-words followed by a low pass filter stage and an additional output amplifier. The latter is necessary to drive coaxial cables and to act as short circuit protection for the preceding DAC stage. To calculate the digital data word for a given output voltage the relation

$$d_{\mathrm{w}} = V_{\mathrm{out}} \frac{V_{\mathrm{out,max}}}{2^N - 1} \tag{6.1}$$

with N the number of bits provided by the DAC can be used. The data-words and the synchronization lines for each of the three DAC are decoupled from the digital area by integrated high-speed opto-couplers.

When switching between to defined voltage levels the output voltage characteristics are of particular interest. On the one hand the switching transient has to be as short as possible, while on the other hand the voltage overshoot also has to be taken into account. In general it can be said that the steeper the switching transient becomes, the larger the corresponding voltage overshoot is. To compensate for the detrimental voltage overshoot, several techniques such as pole compensation, gain compensation, lead and lead-lag compensation are used is OPAMP circuits [170]. The

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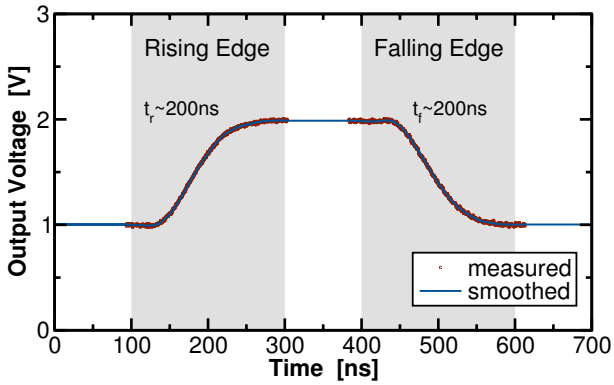

Figure 6.5: Exact switching transients when the output voltages changes are essential for reliability experiments. The rising and falling edge of the output signal of the voltage unit (VU) are measured with an oscilloscope (red symbols). As can be seen, the output amplifier is adjusted to a switching time of approximately 200 ns without any overswing.

compensated switching transient of the developed voltage unit is shown in Figure 6.5. As can be seen, the voltage unit provides a rise time and fall time of $t_r = t_f \sim 200\,\text{ns}$ without any voltage overshoot. Following from that the maximum available output frequency is $f^{max} = 1\,\text{MHz}$.

The output current limits, output voltages ranges and the corresponding voltage resolutions are summarized in Table 6.1 and Table 6.2.

Table 6.1: The maximum ratings for output currents defined by the corresponding output buffer.

Short Circuit Output Current	$I_{sc,max}$	90 mA
Maximum Output Current	I_{max}	35 mA

Table 6.2: The two output voltage ranges which are currently available together with their corresponding voltage resolutions.

Output Voltage Range	Voltage Resolutions
$\pm 5\,\text{V}$	$\Delta V = 152.5\,\mu\text{V}$
$\pm 8\,\text{V}$	$\Delta V = 244.1\,\mu\text{V}$

6.2.1.2. Data Acquisition Unit

The DAU has been developed to record an analog input voltage in the range of $V_{max} = \pm 2.5\,\text{V}$ using a high sampling rate up to $f_{s,max} = 1\,\text{MHz}$. The DAU thereby provides two operation modes with different accuracies, as summarized in Table 6.3. The block-diagram of the DAU is shown in Figure 6.6. At the analog input connector the signal can either be directly forwarded to the input filter stage or an additional voltage offset can be added followed by a subsequent amplifier. The latter pathway allows to shift the allowed input voltage range by a maximum of 2.5 V in each direction. The span of the input voltage is $\Delta V_{in,max} = 5\,\text{V}$ and the input voltage range

$$-\frac{\Delta V_{in,max}}{2} \leq V_i \leq \frac{\Delta V_{in,max}}{2}. \tag{6.2}$$

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DAU mode	$f_{s,max}$	ΔV
fast mode	1 MHz	305.2 µV
normal mode	250 kHz	76.3 µV

Table 6.3: The available DAU input modes and the corresponding sampling frequencies are summarized together with the measurement resolution.

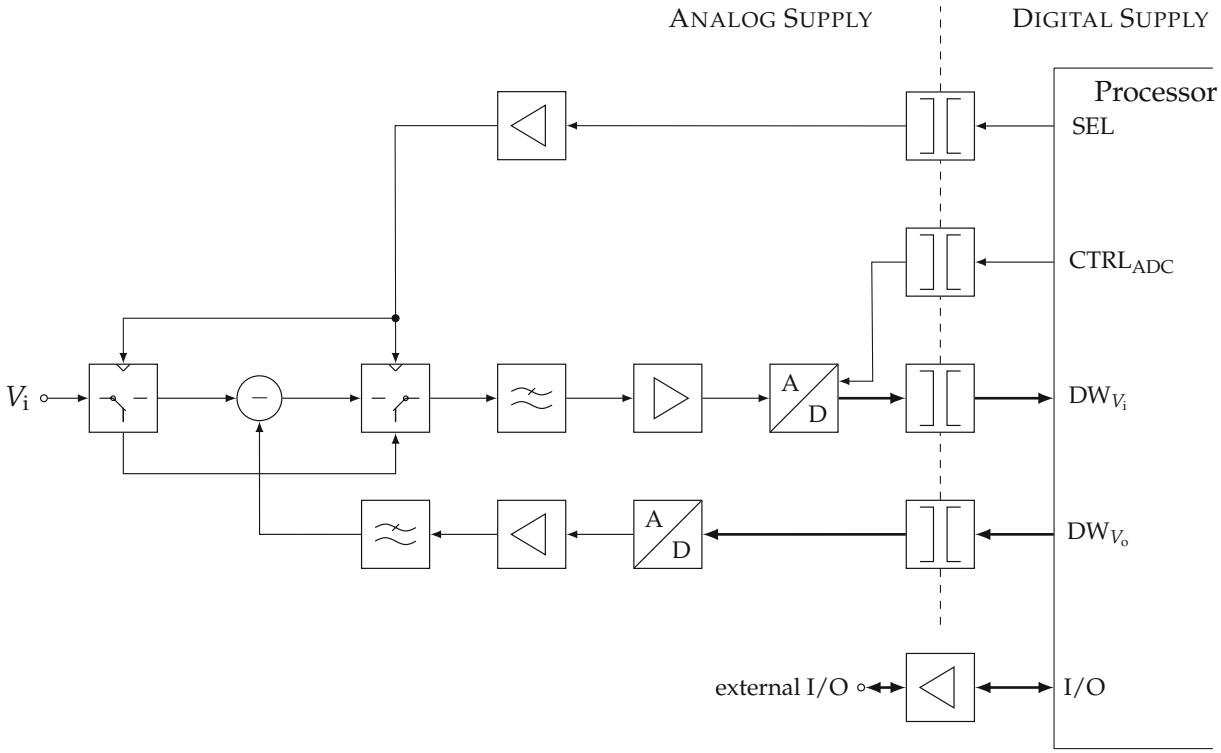

Figure 6.6.: The analog input signal is passed to the input filter with or without subtraction of a programmable offset voltage. A high precision ADC converts the analog signal to a digital-word and is controlled by a decoupled processor unit. Furthermore, the processor unit provides programmable external digital control lines. For the communication with the PC a USB interface is available.

By adding an additional voltage offset in the range of $V_{off} \in [-2.5\,V : 2.5\,V]$, the provided input voltage range can be adjusted to

$$V_{off} - \frac{\Delta V_{in,max}}{2} \leq V_i \leq V_{off} + \frac{\Delta V_{in,max}}{2}. \tag{6.3}$$

The offset voltage V_{off} can be programmed with a resolution of 12 bit leading to an accuracy of $\Delta V_{off} = 1.22\,mV$. A subsequent amplifier and filter stage is used to suppress the DAC and amplifier noise. It has to be noted that the measurement accuracy of the ADC is independent of the alignment of the input voltage range. Especially when the focus is put on single traps, the recovery traces need to have a very high measurement resolution. The programmable input offset allows to shift the mean value of the input voltage range without any losses of the accuracy. Both switches used to select the signal path between the input connector and the filter stage are synchronized and controlled by a driver stage electrically isolated from the main processors.

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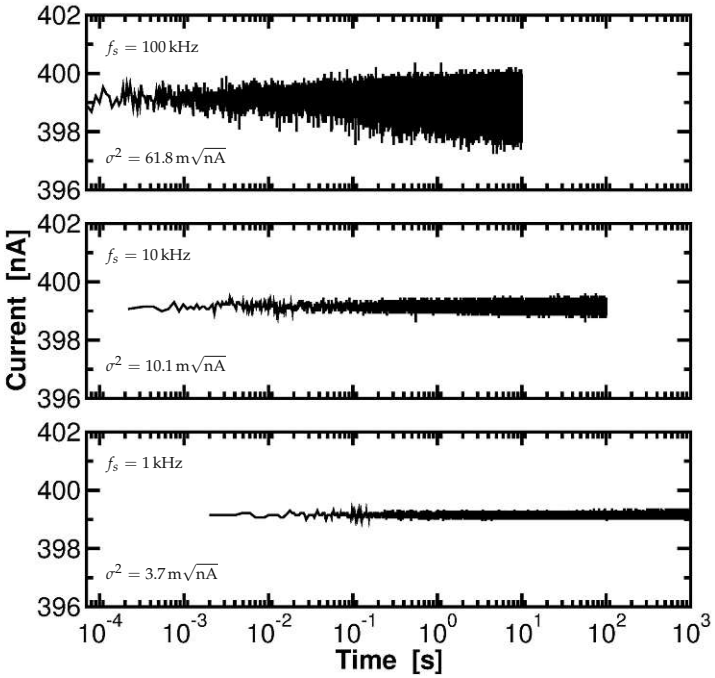

Figure 6.7: Schematic traces uniformly sampled with different sampling frequencies using the current range of 2.5 µA which is most suitable for characterization of single charge trapping in nanoscale transistors. The variance of the uniformly sampled traces does not change during a single trace. At a smaller sampling frequency, which corresponds to a higher integration time, the variance of the signal, that is the signals noise power, decreases. To record long traces at highest speed a large data memory is necessary. Note that the buffer of the TMI available for a single trace is limited to 10^6 samples.

The input filter and a high precision amplifier unit implemented prior to the ADC are designed to match the bandwidth of the input signal to the sampling frequency. It is of utmost importance to carefully calibrate both units in order to hold the noise level of the measured signal as low as possible and at the same time take advantage of the high sampling frequency.

As discussed in Chapter 5, for monitoring the device reliability the input signal has to be recorded for very long time ranges up to 100 ks. In order to achieve a manageable number of data-points per trace but at the same time having a high sampling time resolution, a non-uniform sampling scheme is used preferentially. In Figure 6.7 the input signal for uniformly sampled data at different sampling frequencies is shown. As expected, with a smaller sampling frequency, which is equivalent to a larger integration time, the variance of the sampled signal decreases. Thus, using a non-uniform sampling scheme the variance of the signal decreases automatically during the measurement, because the integration time is increased after each decade, see Figure 6.8. With the possibility of using either a uniform or a non-uniform sampling scheme, a new challenge for the subsequent data analysis algorithms arises which is discussed in Chapter 7.

6.2.1.3. Device Connector Unit

The DCU acts as the interface between the DUTs and the TMI. It provides floating output terminals which are connected to the appropriate signal lines only during the measurement. As the data aquisition unit is designed to record voltage signals, the main purpose of the DCU is to convert the currents flowing through the MOSFET terminals into voltages measurable by the corresponding DAU. To achieve a high current resolution from the milli-ampere regime down to the

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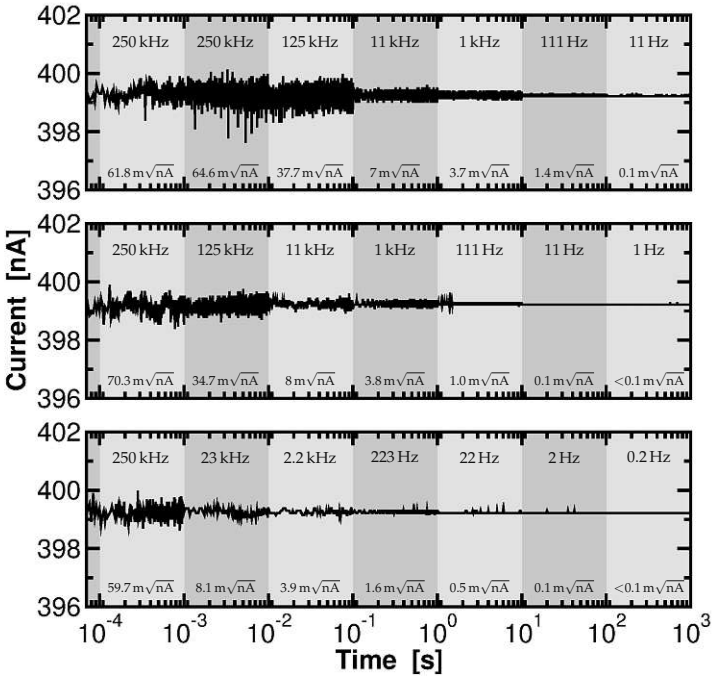

Figure 6.8: The non-uniformly sampled data recorded with (**top**) 200 samples per decade (this is the most common case used in our experiments), (**middle**) 1000 samples per decade and (**bottom**) 10000 samples per decade shows a reduced signal noise power (see variances given at the bottom of each sub-figure) with increasing sampling time because the sampling frequency (given at the top of each sub-figure) is decreased. As a consequence of the adjusted sampling frequency, the measurement resolution increases automatically. Another benefit of the non-uniformly sample scheme is the reduced number of datapoints with allows to record ultra-long traces.

sub-picoampere regime and at the same time hold the noise level as low as possible, a thorough design of the analog part of the circuit layout is required.

A schematic illustration of the entire concept of the device connector unit is shown in Figure 6.9. As can be seen, the drain and bulk terminals of the DUT are connected to the VU using intermediate amplifier stages. Furthermore, the output amplifiers provide the necessary currents and a subsequent low pass filter stage is implemented to block HF noise. At the source terminal a high-precision current convert unit (CCU) is available. The detailed configuration of the CCU is illustrated in Figure 6.10. It is important to note that the potential at the input terminal is held at $V_{\mathrm{i}} = 0\,\mathrm{V}$. At the output terminal a voltage signal proportional to the input current I_{in} is obtained given by

$$V_{\mathrm{out}}(t) = A \times I_{\mathrm{in}}(t). \tag{6.4}$$

In order to provide a wide input current range, different input gains $A = [10^2, 10^3 \ldots 10^8, 10^9]$ can be selected. The maximum input current for the selected gain A is

$$I_{\mathrm{max}} = \frac{2.5}{A} \tag{6.5}$$

and the corresponding accuracy

$$\Delta I = \frac{1}{A} \cdot \frac{2.5}{2^{15}}. \tag{6.6}$$

The maximum available input voltage $V_{\mathrm{in,max}} = 2.5\,\mathrm{V}$ and the number of quantized values $N_{\mathrm{D}} = 2^{15}$ are given by the ADC providing a 16 bit resolution and a input voltage range of $\pm 2.5\,\mathrm{V}$. Note that for the best current accuracy provided by $A = 10^9$ an alternative OPAMP with ultra-low input bias current has to be used and the use TRIAX components is recommended. Furthermore, the current ranges can be adjusted on demand by modifying the gain of the amplifier stage. All switches

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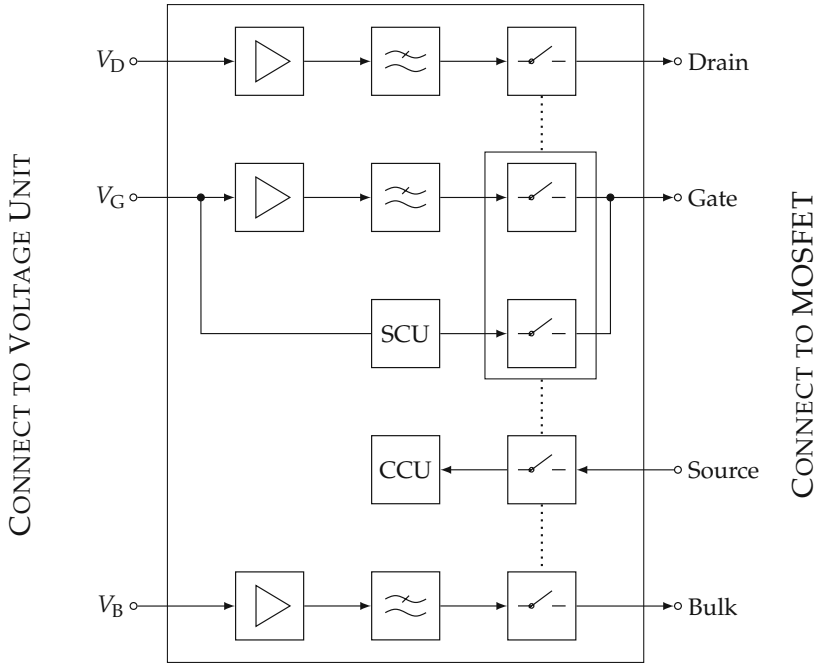

Figure 6.9.: The output terminals of the DCU are initially floating to avoid any distortion of the devices. At the source terminal, the CCU holds the source voltage at $V_S = 0\,V$. By contrast, the SCU allows to output a voltage and measure the current simultaneously, which is necessary for monitoring the gate current.

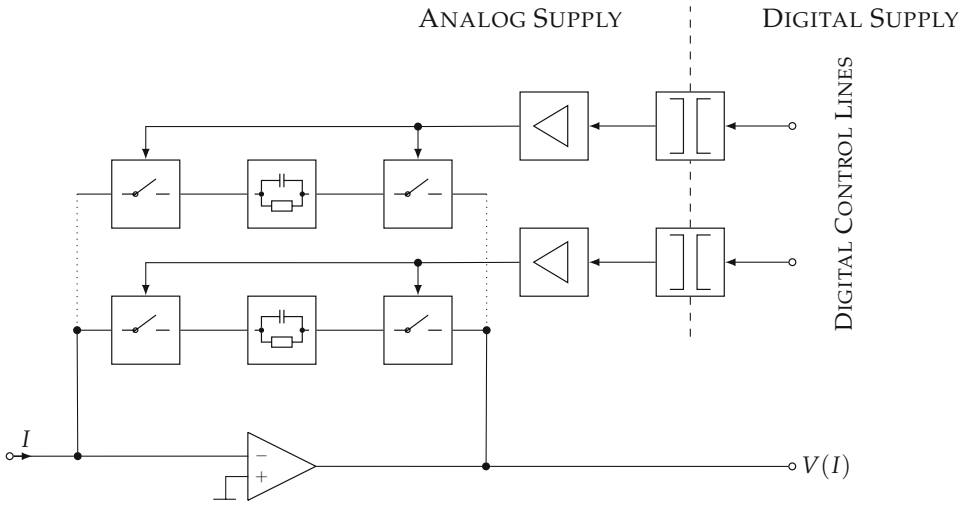

Figure 6.10.: The CCU provides eight input current ranges selectable using synchronized switches. By using the OPAMP, the potential of the input pin is held at 0 V. Again, the analog and digital components are electrically isolated.

used to select the appropriate current range are synchronized and connected via the backbone bus system to the DAU. Again, the digital and analog sub-circuits are electrically decoupled.

To measure the gate current, a source converter unit (SCU) has been designed, see Figure 6.11. In contrast to the CCU, the SCU provides a defined output voltage while the input current can be

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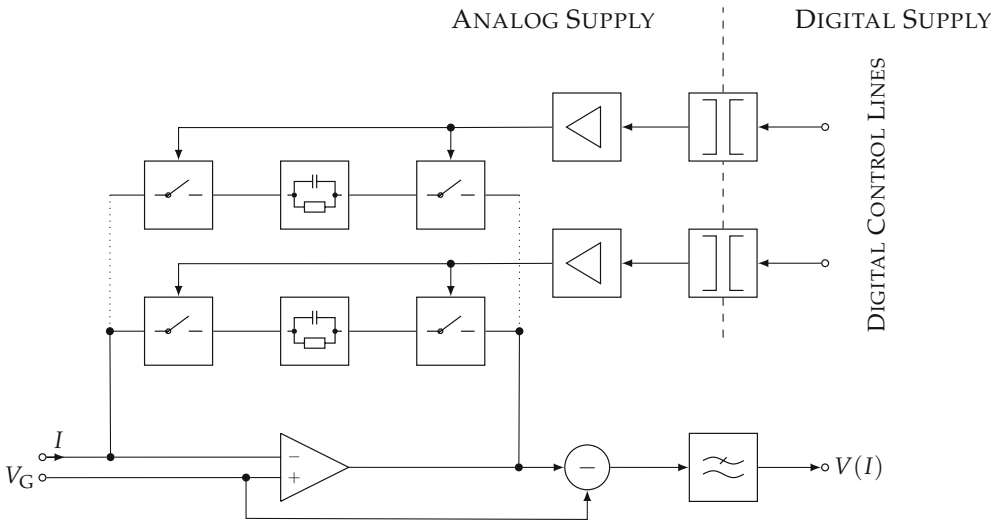

Figure 6.11.: The SCU operates like a general purpose SMU. A defined output voltage is provided and the current is converted to a proportional voltage at the same time. Similar to the CCU, synchronized switches allow to select the appropriate input voltage range.

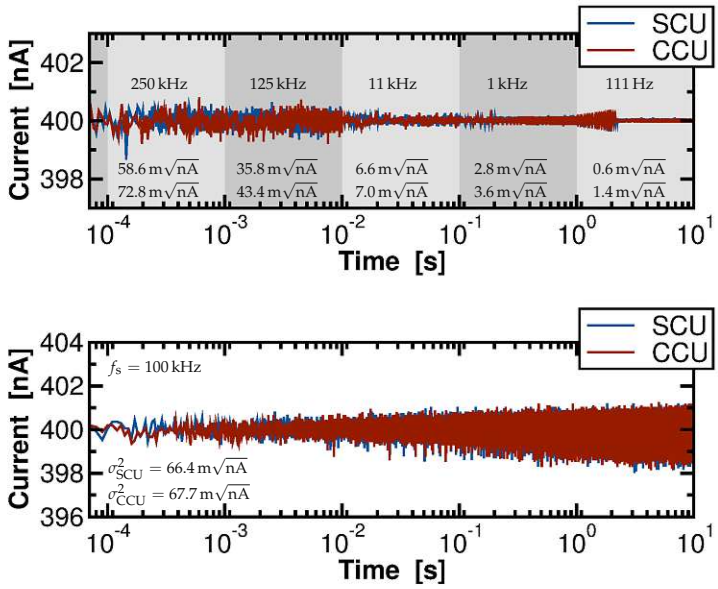

Figure 6.12: A comparison of (**top**) a non-uniformly sampled signal and (**top**) a uniformly sampled signal measured with the CCU and SCU shows similar signal noise level. An additional low pass filter suppresses the noise level of the SCU below the noise level of the CCU although the SCU requires an additional OPAMPs.

measured. For that the CCU has to be extended by an additional subtraction unit followed by a filter stage. In general, each additional amplifier stage introduces noise to the measurement signal and an additional offset voltage which has to be compensated. However, due to the final low pass unit of the SCU its noise level is similar to the noise level from the voltage signals from the CCU, see Figure 6.12.

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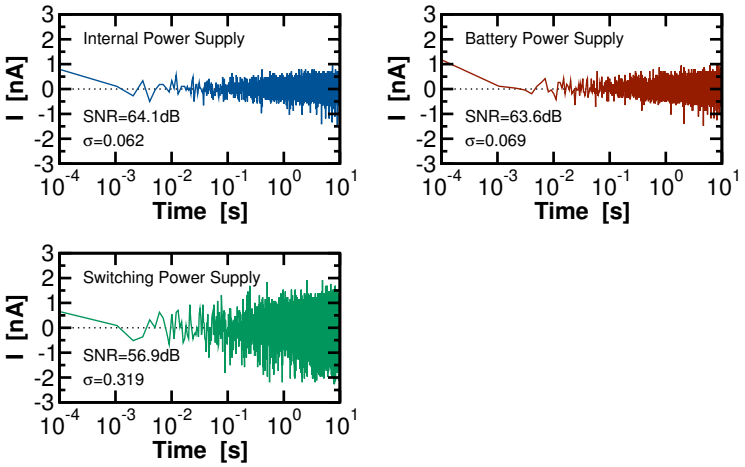

Figure 6.13: The noise of the signal measured by the TMI is compared for power supplied by **(top left)** the integrated PSU **(top right)** a switching power supply and **(bottom)** a battery. As can be seen, equal signal to noise ratios (SNRs) are obtained for the signal recorded using the internal and the battery power supply. Using a switching power supply leads to a significant increase of the noise level in the signal and thus reduces the maximum achievable measurement resolution.

6.2.1.4. Power Supply

In analog circuits and especially in instruments used to precisely record signals with a very high accuracy the power supply plays a crucial role. Therefore, the power supply of the TMI is thoroughly separated into a digital supply, providing the power for the processors, the USB interface and the external control lines and an analog supply which drives the very sensitive input/output terminals of the VU, the DAU, and the DCU. To emphasize the important role of a low noise analog power supply a test voltage signal is recorded, while the supply voltage of the analog part of the TMI is provided by

1. the integrated power supply unit (PSU),
2. a battery, and
3. a switching power supply

as the main power supply of the TMI. As can be seen in Figure 6.13, the distortion caused by the switching power supply is not acceptable . The best solution is to use battery powered systems or the integrated PSU which provides a reasonably low noise level.

6.2.2. Properties of the Time-Dependent Defect Spectroscopy Measurement Instrument

The figures of merit for our measurement instrument are the sampling bandwidth, which defines the smallest measurable switching transient between the stress and recovery cycle, and the minimum measurable input current, which strongly depends on the gain of the input amplifier, see Figure 6.14. While the input bandwidth is limited by the maximum sampling frequency of $f_{\mathrm{s,max}} = 1\,\mathrm{MHz}$ due to the integrated ADC, different gains of the input signals are available providing different measurement resolutions. The minimum current resolution $\min(I) \sim 1\,\mathrm{pA}$, which underlines the thoroughly worked out design.

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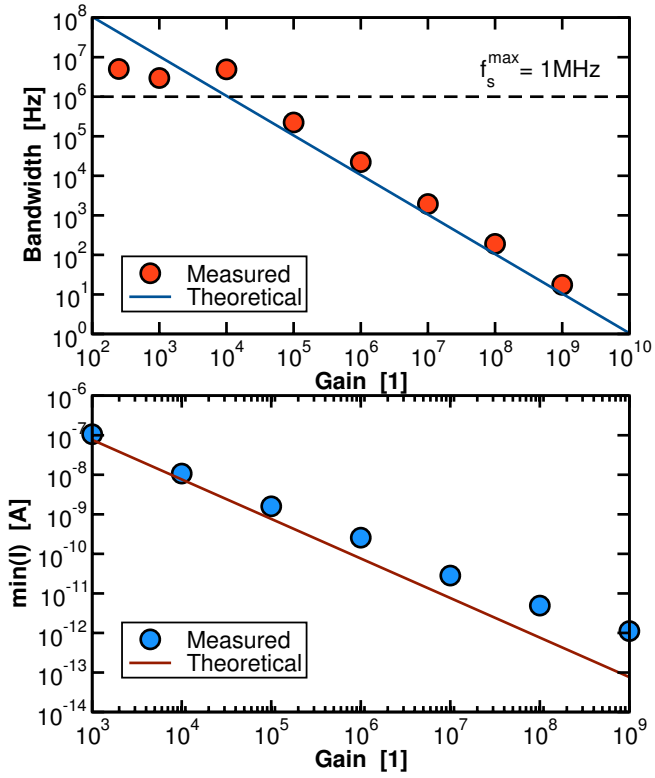

Figure 6.14: (**top**) For small gains the signal bandwidth is limited by the maximum sampling frequency. Towards higher input gains the bandwidth is limited by the OPAMP and the input circuit. (**bottom**) The higher the signal gain gets, the smaller the current resolution gets. The theoretical limit is a consequence of the current resolution provided by the least significant bit of the ADC. However, the experimentally measured resolution is higher because the signal is overshadowed by measurement noise.

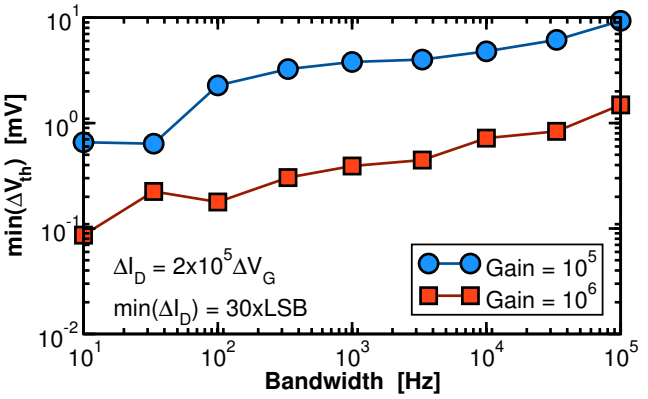

Figure 6.15: For a smaller input bandwidth, that means a larger integration time, of the I/V converter stage the measurement resolution of the ΔV_{th} is significantly increased, leading to smaller measurable ΔV_{th} shifts. The minimum detectable ΔV_{th} is calculated for the two most common gains of the I/V converter which are used to study single charge trapping in nanoscale devices. This is done using the given relation between the I_{DS} and V_{GS}, extracted from a measured $I_{DS}(V_{GS})$ characteristics of a nanoscale pMOSFET.

The correlation between the bandwidth and the minimum detectable ΔV_{th} is shown in Figure 6.15. According to (4.19) the smaller the measurable current shift gets the more defects can be studied properly using the TMI. Quite remarkably, at a sampling frequency of $f_s \approx 30\,\text{kHz}$ the current resolution is already below $\Delta V_{th} < 1\,\text{mV}$. Furthermore, on the one hand BTI recovers very quickly and on the other hand the device recovery behavior has to be monitored for very long times, for instance $t_r = 10\,\text{ks}$ and even longer. Due to the limited high speed data buffer of the available instruments, linear sampling at a high frequency is not feasible. For instance, data sampled with $f_s = 1\,\text{MHz}$ for just $t_r = 1\,\text{ks}$ using an ADC with 16 bit resolution would need a disk space of 1.86 GB. Since typically 100 traces are recorded at a number of biases and temperatures, a linear sampling scheme is not suitable to study single defects in nanoscale devices. Thus a logarithmic sampling scheme, with typically 200 samples per decade, is preferred. Note, by using the latter,

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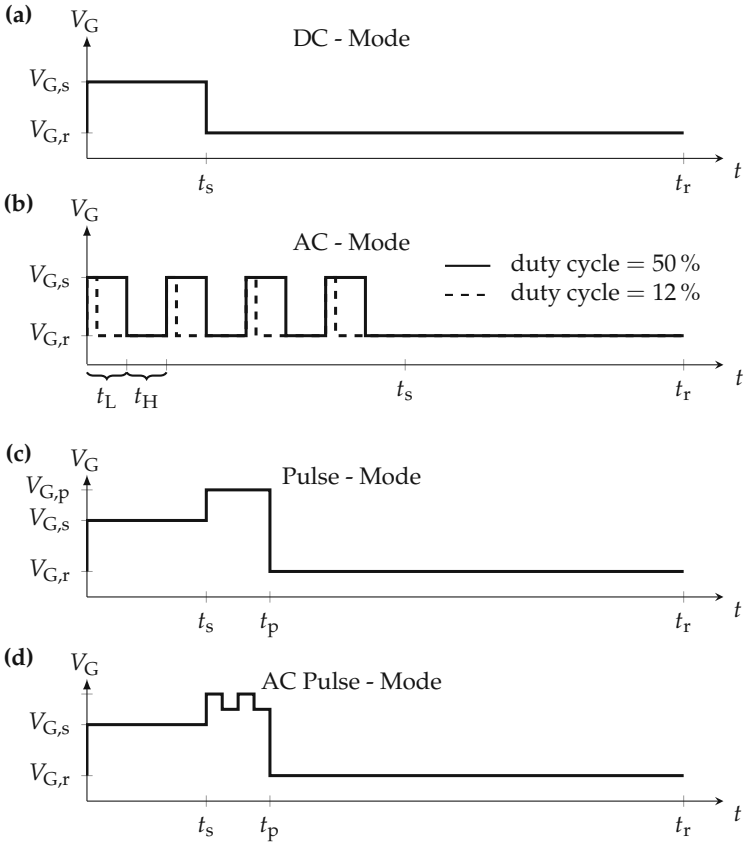

Figure 6.16: The core output signals implemented in the TMI and the corresponding configuration are shown. The signals involve **(a)** DC stress signals, **(b)** AC stress signals, **(c)** DC pulse stress signals and **(d)** DC stress with subsequent AC stress signals.

the sampling frequency is increased every decade and as a consequence the current resolution implicitly is improved.

6.2.3. Output Signals

The TMI provides all output voltage signals which have been used so far in context of the TDDS, see Figure 6.16. These output modes involve

- DC stress signals,
- AC stress signals,
- DC stress signals with a subsequent voltage pulse and
- DC stress signals with a subsequent AC voltage signal.

After each stress cycle the output voltages switch to recovery bias conditions and I_{DS} and I_G are monitored. In addition to the listed output signals, individual time-dependent voltage characteristics can be programmed. The listed core signals provide a time resolution of 500 ns whereas the time resolution of individuals signals is limited to 1 µs.

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	$f_{s,max}$	uniform sampling	non-uniform sampling	switch gain
14 bit fast mode	1 MHz	Yes	Yes	No
14 bit normal mode	250 kHz	Yes	Yes	Yes
16 bit fast mode	750 kHz	Yes	Yes	No
16 bit normal mode	250 kHz	Yes	Yes	Yes

Table 6.4.: The available configurations of the DAU are summarized in the table above. It has to be noted, that the same measurement resolution is achieved for the 14 bit and 16 bit mode. However, the input current ranges of the 16 bit mode are two times the input current ranges of the 14 bit mode.

Furthermore, custom voltage ramps can be independently configured for each output with a resolution of 10 µs in time, see Figure 6.17. From this, simple voltage sweeps as used for $I_{DS}(V_{GS})$ measurements can be derived.

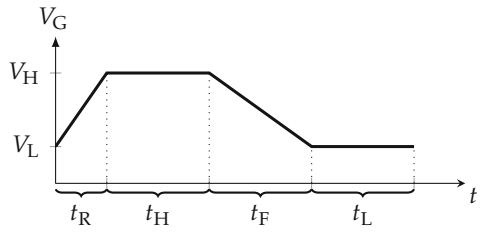

Figure 6.17: Schematic of the ramp signal and its corresponding parameters: rise time t_R, high time t_H, fall time t_F and low time t_L as well as low voltage level V_L and high voltage level V_H.

6.2.4. Data Acquisition

The main feature of the DAU is to record the drain-source and gate current during the stress and recovery cycle. For this, the appropriate biases are provided by the VU. If the input current during stress and recovery lies inside the same current range, switching between them is very fast and the measurement delay is only determined by the bandwidth of the input amplifier, see Figure 6.18. However, different current ranges during stress and recovery require switching of the input stages of the TMI between different input gains. This adds an additional delay of at least $t_{sw} = 1$ ms, which is quite short compared to general purpose instruments.

Furthermore, the DAU provides two measurement and two sampling modes, leading to four possible sampling configurations, summarized in Table 6.4.

6.3. Control of the Experiments

The devices probed in our experiments are either packaged into custom ceramic packages or directly measured at the wafer level. For the packaged devices, special furnaces are available which allow to contact the chips and to apply a defined temperature profile. For the wafer-level exper-

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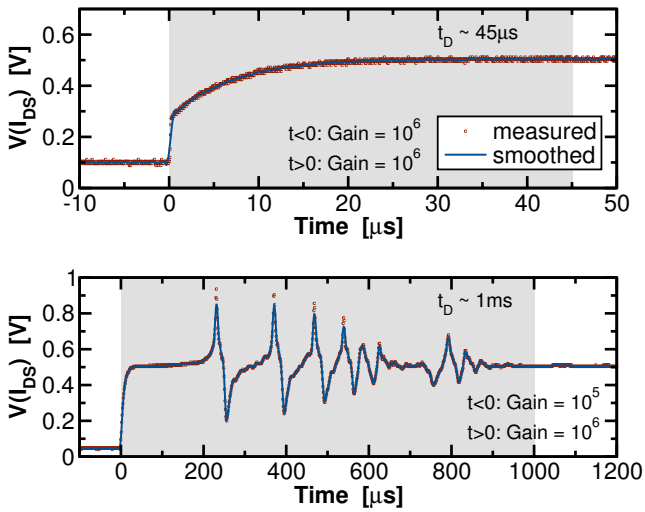

Figure 6.18: (**top**) The switching transient between the stress and recovery is primarily defined by the bandwidth of the input buffer at different gains, see Figure 6.16. (**bottom**) If the input current ranges have to be switched, an additional delay of at least $t_{sw} = 1\,\text{ms}$ is introduced because mechanical relays are used to select the gain of the I/V converter unit. The typical bouncing characteristics occurring when the switch position of a relay is changed is visible during the switching cycle (colored light gray).

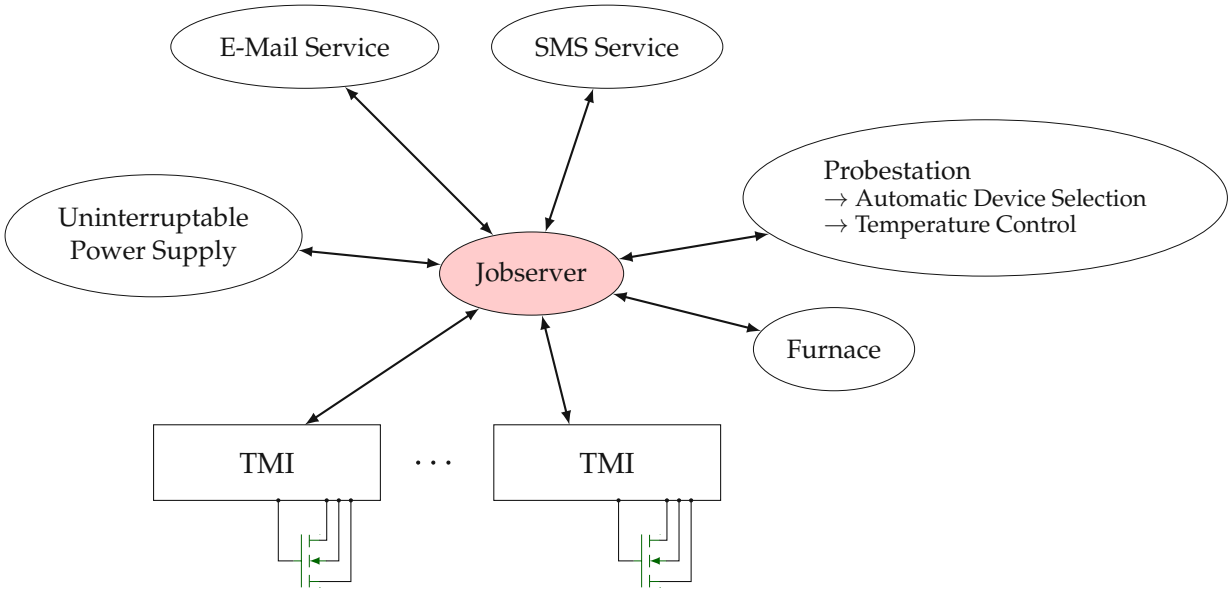

Figure 6.19.: The jobserver control device selection for the semi-automatic probestations or transistor arrays, the device temperature, the UPS and several TMIs in parallel. Furthermore, status E-Mails and SMS can be sent to inform the user about the measurement progress and other events.

iments a semi-automatic probestation, which allows to automatically move the contact probes between different transistors, is used. To control the interaction between all the individual components, a jobserver has been designed, see Figure 6.19. The jobserver is responsible for device selection in case of a semi-automatic probestation, and also controls the device temperature via the power-supply of the furnace or the thermo-chuck of the probestation. Furthermore, a queue control has been implemented which allows to submit jobs any time which will be sequentially processed. As BTI measurements can last several months, the setup is protected against power supply interruptions using UPSs, which are monitored by the central jobserver. A very convenient

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feature of the jobserver is the E-Mail notification feature which provides the user with information regarding successful or failed measurements.

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7 Advanced Step Detection Algorithm

In the previous sections the TDDS and the measurement setup based on the TMI has been discussed in detail. Furthermore, it has been mentioned that in nanoscale transistors the recovery after the device has been subjected to NBTI or PBTI stress typically proceeds in discrete steps. To further analyze the individual constituents contributing to the recovery behavior, an elaborate step detection algorithm is required. For that the advanced bootstrapping and cumulative sum (BCSUM) algorithm is presented in this section. After the requirements are briefly introduced, the cumulative sum charts [171, 172] and the bootstrapping mechanism which are the key components of the algorithm are discussed. Finally, the functional interplay is presented.

7.1. Requirements

To study the trapping kinetics of single traps, the recovery traces have to be analyzed for discrete steps. Thus the algorithm has to be able to detect abrupt changes in various signals which

1. are uniformly or non-uniformly sampled, and thus
2. need not to exhibit a constant variance over time, i.e. a constant signal noise level, and which
3. contain positive and negative discrete steps.

Furthermore, the algorithm should be configurable with just a few parameters and has to be executable with reasonable computational effort.

In general, the measurement window of the TDDS can be very large. The emission times of the single traps contributing to BTI have widely distributed time constants, from microseconds over days up to weeks or even years. A measurement window spreading over several decades in time goes hand in hand with the necessity of finding a trade off between the sample intervals and the amount of measurement data recorded. An adjustment of the sampling time intervals to higher

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values for larger recovery times is therefore necessary. Thus, for recording the recovery traces a non-uniform sampling scheme with usually 200 datapoints per decade is preferred to uniformly sampled data. The non-uniform sampling provides a high sampling rate immediately after switching from stress to recovery bias conditions to avoid the loss of any important information. For very long recovery traces a feasible number of data samples is achieved. In order to link the sampling intervals with the signal bandwidth the scaling property of the Fourier transform [173]

$$r(at) \overset{\mathcal{F}}{\Longleftrightarrow} \frac{1}{a} R\left(\frac{\omega}{a}\right) \tag{7.1}$$

has to be considered. Using this relation a compression in the time is transferred domain into a dilatation in the frequency domain and vice versa, $\mathcal{F}$ denotes the Fourier transform operator and $R(\omega) = \mathcal{F}\{r(t)\}$ is the Fourier transform of the time signal $r(t)$. An decade-wise adjustment of the sampling rate directly decreases or increases the noise power of the measurement signal when the sampling rate is decreased or increased, respectively. It is therefore necessary that the step detection of the advanced algorithm can operate on non-uniformly sampled measurement data as well.

The experimental investigation over the last years performed on different technologies showed that a large number of single traps tend to produce fast RTN signals with $\tau_c \approx \tau_e$. Such RTN signals are typically observed over many decades showing the same capture and emission time. By using a non-uniform sampling scheme, the sampling time intervals get increased and as a consequence the RTN signal is visible as very short pulses in the traces at high recovery times. Furthermore, in most cases peaks in the measurement data caused due to RTN consists of just a few datapoints, which makes the detection of RTN very difficult. Nonetheless, the introduced BCSUM algorithm is able to detect such short pulses present in our measurement data.

7.2. The Bootstrapping and Cumulative Sum Algorithm

In general, the step detection algorithm has to extract unknown steps of height d given an unknown mean value of the signal, $\mu(t_r)$. Based on the mean shift model given by

$$r = \mu + d\sigma(t_r - \tau_e) \tag{7.2}$$

with the step function σ and the emission time τ_e, a statistical treatment of this problem is possible using the bootstrapping and cumulative sum (BCSUM) algorithm [174].

The BCSUM detection algorithm has the ability of detecting either positive or negative steps in a data set. From the BCSUM procedure the decision that either a discrete step in the underlying data samples exists or not is obtained by selection of a detection sensitivity parameter ϵ. In the following the cumulative sum charts [171, 172] are discussed, the bootstrapping mechanism is introduced and finally the advanced detection method is presented.

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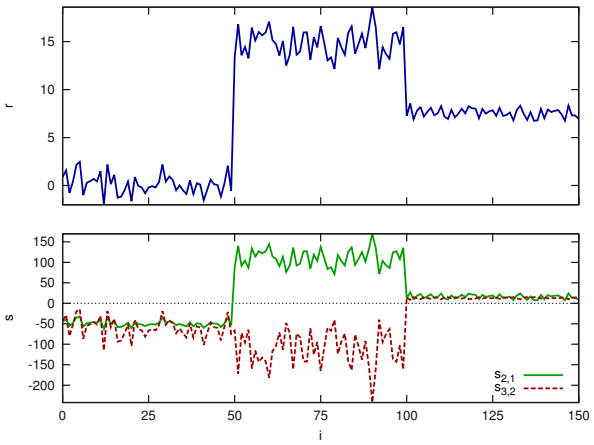

Figure 7.1: The log-likelihood ratio **(bottom)** is calculated for normally distributed data for $N_1(0,1)$, $N_2(15,1.5)$ and $N_2(7.5,0.5)$ **(top)**. When the test signal r changes its underlying distribution function from N_1 to N_2 the resulting log-likelihood ratio $s_{2,1} = \ln p_2(r)/p_1(r)$, whereas p_1 is the Gaussian distribution function for N_1 and p_2 the Gaussian distribution function for N_2, shows a change in the sign at the transition time instance, called change point. When the underlying data distribution of r goes from N_2 to N_3 a sign change is observed in the log-likelihood ration $s_{3,2} = \ln p_3(r)/p_2(r)$ [MWC26].

7.2.1. Cumulative Sum Charts

First consider a series of independent measurement points $\mathbf{r} = [r_0, r_1, \ldots, r_{N-1}]$ with N the number of samples. The signal distributions before and after a change in the signal mean are given by $p_0(r)$ and $p_1(r)$, respectively, with their corresponding means μ_0 and $\mu_1 = \mu_0 + d$, where d is the step height. Introducing the log-likelihood ratio given by

$$s_i = \ln \frac{p_1(r_i)}{p_0(r_i)} \tag{7.3}$$

a change in the signal mean is reflected by a change of the sign of the mean value of the log-likelihood ratio S_m^n [172] of the data set $[r_m, \ldots, r_n]$ given by

$$S_m^n = \sum_{i=m}^{n} s_i \tag{7.4}$$

and is illustrated in Figure 7.1.

Together with the assumption of normally distributed samples with the probability density function

$$p_{\mu,\sigma}(r_i) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{(r_i-\mu)^2}{2\sigma^2}\right), \tag{7.5}$$

the log-likelihood ratio for $d = \mu_1 - \mu_0 > 0$ and $\sigma = \sigma_0 = \sigma_1$ is

$$s_i^{\uparrow} = A\left(r_i - \mu - \frac{d}{2}\right) \quad \text{with} \quad A = \frac{\mu_1 - \mu_0}{\sigma^2}, \tag{7.6}$$

and the change point position is at the sample with index

$$i_{\tau_e}^{\uparrow} = \{k : \min_{0<k<N-1} S_0^k\}. \tag{7.7}$$

In the case of trapping events, a negative mean shift is obtained and the log-likelihood ratio for $d < 0$ reads

$$s_i^{\downarrow} = A\left(r_i + \mu - \frac{d}{2}\right) \quad \text{with} \quad A = \frac{\mu_1 - \mu_0}{\sigma^2}. \tag{7.8}$$

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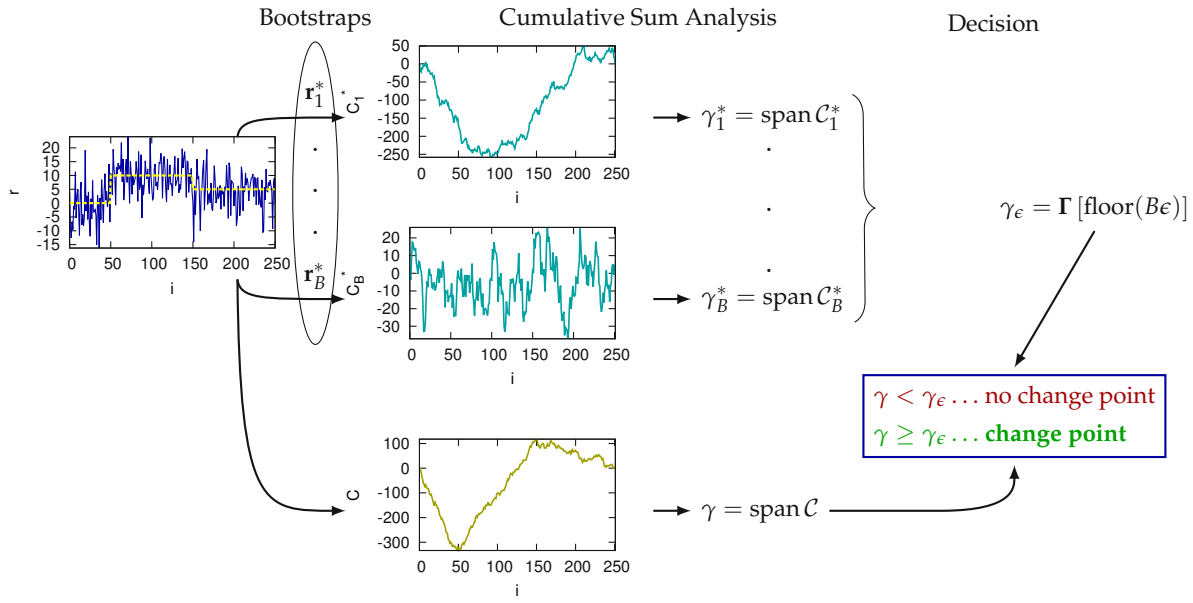

Figure 7.2.: Illustration of the bootstrap and cumulative sum algorithm to detect one step in a very noisy data set. Even though the data set contains two steps, the algorithm has to be applied recursively because at most one, that is, the biggest change point is detected. Using the initial data set $\mathbf{r}$ a number of B bootstraps $\mathbf{r}_b^*$ are created. These bootstraps $\mathbf{r}_b^*$ are resampled data sets of the initial data set $\mathbf{r}$ by applying resampling with replacement scheme. Afterwards, the cumulative sum charts of the bootstrapped and the original data are created. The spans of the single CSUM charts of the bootstrapped data are collected by a sorted list, from the minimum to the maximum, $\mathbf{\Gamma}$. The decision threshold γ_ϵ equals the element of $\mathbf{\Gamma}$ with index $i = B\epsilon$, with $\epsilon \in [0,1]$ called the detection sensitivity. Finally, the decision threshold γ_ϵ is compared to the span of the CSUM chart obtained from the initial data set γ. For $\gamma > \gamma_\epsilon$ the initial data set contains a change point. In that case the initial data set has to be split at the change point and the algorithm is applied recursively to both sequences. This divide and conquer procedure is continued until no further change points larger than a threshold are detected in the subsequences [MWC26].

with the change point at the sample index position

$$i_{\tau_e}^{\downarrow} = \{k\colon \max_{0<k<N-1} S_0^k\} \tag{7.9}$$

Since the change of the mean is unknown the detection of either positive or negative changes has to be provided by the algorithm. Combining both cases, $d > 0$ and $d < 0$, the log-likelihood ratio for normally distributed samples can be formulated as

$$s_i = r_i - \nu \tag{7.10}$$

where the threshold value ν already considers the prefactor A. With the choice of $A = 1$ the CSUM chart function is

$$\mathcal{C} = \sum_N r_i - \nu \quad \text{with} \quad \nu = \frac{1}{N}\sum_N r_i. \tag{7.11}$$

The sample index of the change point is given by

$$i_{\tau_e} = \left\{k\colon \max\left(|i_{\tau_e}^{\downarrow}|, |i_{\tau_e}^{\uparrow}|\right)\right\} = \{k\colon \max\left(|\mathcal{C}|\right)\}. \tag{7.12}$$

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7.2.2. Bootstrapping

A frequently used method for parameter estimation of a set of data samples for unknown underlying distributions is bootstrapping. Its big advantage is that it is fully automatic and it does not matter how complicated the mathematical model for the probability distribution is.

For a given set of samples $\mathbf{r}$ of length N a bootstrap sample $\mathbf{r}^*$ is obtained by randomly choosing N samples from $\mathbf{r}$ with replacement. Since bootstrapping is a resample technique with replacement, the samples out of $\mathbf{r}$ can occur never, once or more often in the bootstrap estimate $\mathbf{r}^*$ [175].

The statistical nature of bootstrapping includes the necessity of a huge number B of bootstrap samples $\mathbf{r}_b^*$. This circumstance inevitably leads to computationally expensive procedures.

7.2.3. The Algorithm

The BCSUM algorithm is a Monte Carlo based combination of bootstraps and cumulative sum charts to detect changes in the signal mean. The divide and conquer procedure to detect one change point in the measurement data set $\mathbf{r}$ is:

1. Calculate the B bootstrap samples $\mathbf{r}_1^*, \mathbf{r}_2^*, \ldots \mathbf{r}_B^*$ from $\mathbf{r}$.
2. Create the cumulative sum charts $\mathcal{C}_b^*$ for each bootstrap sample $\mathbf{r}_b^*$ with $b \in [1, B]$.
3. Estimate the spans of each chart $\mathcal{C}_b^*$ and collect them into a sorted list from the minimum to the maximum $\mathbf{\Gamma}$.
4. With the detection sensitivity ϵ the decision threshold is obtained as $\gamma_\epsilon = \mathbf{\Gamma}[\text{floor}(B\epsilon)]$, where $[\cdot]$ denotes the list index operator. For a data set $\mathbf{r} = [r_0, r_1, \ldots, r_{N-1}]$ the list index operator is
$$\mathbf{r}[i] = r_i. \tag{7.13}$$
5. Create the CSUM chart $\mathcal{C}$ from the initial data set and evaluate $\gamma = \text{span}\,\mathcal{C}$
6. A change point in the underlying sequence occurs if $\gamma_\epsilon < \gamma$. Split the data set at the change point position and recursively continue with 1) for each subsequence until all change points are detected.

Critical parameters for the detection outcome of the BCSUM algorithm is the number of bootstraps B and the detection sensitivity ϵ. For statistical relevance, the bootstrapping and the calculation of $\mathcal{C}_b^*$ has to be performed many times, $B = 10^5$ is recommended.

A choice of $\epsilon \approx 1$ means that just the most dominant changes in mean are detected. For very fast events, which often just span two or three measurement data samples, the detection sensitivity is a crucial parameter. To extract small and very fast changes $\epsilon \approx 0.6$ is recommended. Moreover, the position of the change point in the measurement data is directly accessible via the CSUM chart obtained from the initial data series.

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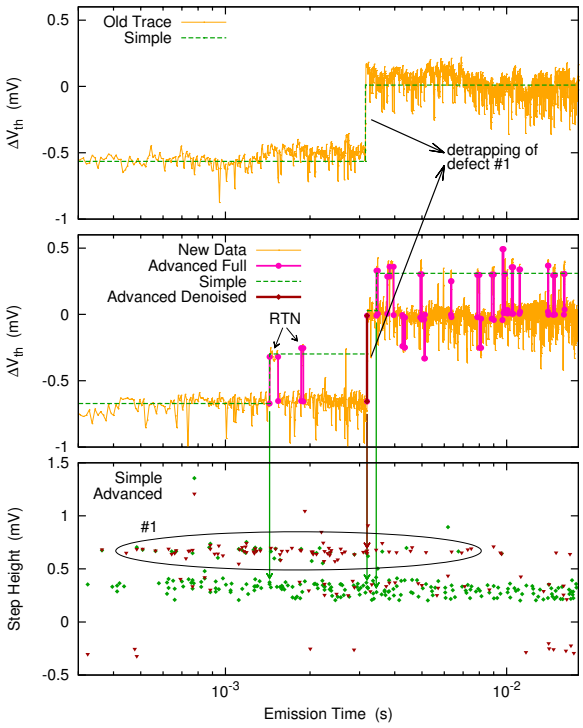

Figure 7.3: An example recovery trace (**top**) showing a single detrapping event, in this case for a defect named #1, which is clearly visible and not contaminated by RTN. However, new measurements recorded several weeks after the first dataset are strongly influenced by a new defect producing RTN (**middle**). The initially used naive algorithm just detects three positive changes because only positive steps are considered (**middle**, *Simple*). The BCSUM method additionally detects negative steps stemming from RTN (**middle**, *New Full*). In the spectral map (**bottom**), here depicted for 100 traces, the steps detected with the simple method (green) show step heights below the step level for the defect #1 which equals the step heights produced by an RTN defect. Furthermore, the large step is extracted with a wrong amplitude and so it does not contribute to the defect #1 in the spectral map. The BCSUM algorithm extracts the amplitudes corresponding to the defect #1 correctly [MWC26].

Last, but not least it has to be noted that the algorithm can be applied to uniformly and non-uniformly sampled data as well. This property is very important in the context of the TDDS. To cover several decades in time a compromise between the sampling rate and the accumulated recovery time is necessary in order to achieve a feasible amount of measurement data.

7.3. Evaluation of the Algorithm

An example of common recovery traces recorded on a $W \times L = 160\,\text{nm} \times 120\,\text{nm}$ pMOSFET is shown in Figure 7.3. As long as the DUT contains only single emission events, which is the case for defects with $\tau_e \gg \tau_c$, the TDDS data can be analyzed in a straight-forward manner. However, this is not the case for signals containing single defects producing RTN. As can be seen from Figure 7.3 (middle) the initially used step detection algorithm considers steps in one direction leading to a falsely extracted step height. The BCSUM algorithm detects all steps correctly by using just two parameters.

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Part III.

Results

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8

Positive Bias Temperature Instabilities in SiON n-channel MOSFETs

The main focus of the research on charge trapping in SiON transistors was primarily put on NBTI in pMOSFETs. By probing nanoscale pMOSFETs employing the TDDS single defects have been studied with the following properties:

i) Nanoscale devices show discrete recovery behavior

ii) Single traps show *fixed trap* and *switching trap* charge capture and emission time characteristics when the stress and recovery gate bias is varied

iii) Temperature dependence of the charge transition times with activation energies in the range of 0.5 eV up to 1.4 eV for charge capture and emission were found, mostly limited by the experimental resolution as the time constants depend exponentially an the activation energy

iv) Charge capture shows a notable frequency dependence when AC stress biases are applied

v) Widely distributed step heights and transition times are visible

vi) Defects in pMOSFETs are considered to be hole traps

All these observations have been consistently explained by our four-state NMP model. These findings, however, raise the question whether the defects causing PBTI in nMOSFETs show a similar response to the variation of the bias conditions and temperature or not. To settle this question the TDDS technique has been applied to characterize PBTI in pMOSFETs where electron traps are typically considered to contribute to the threshold voltage shift ΔV_{th}.

Again, to separate individual emission events belonging to different defects, the devices used for TDDS must only show a handful of defects. However, recent reports have revealed that pMOSFETs show an approximately ten times higher trap density than their nMOSFET counterparts ($N_{\mathrm{pMOS}} \approx 10 \times N_{\mathrm{nMOS}}$) [99, 176]. As a consequence, just a few carefully selected nanoscale nMOSFETs would show a noticeable number of defects visible in the recovery traces. Thus to

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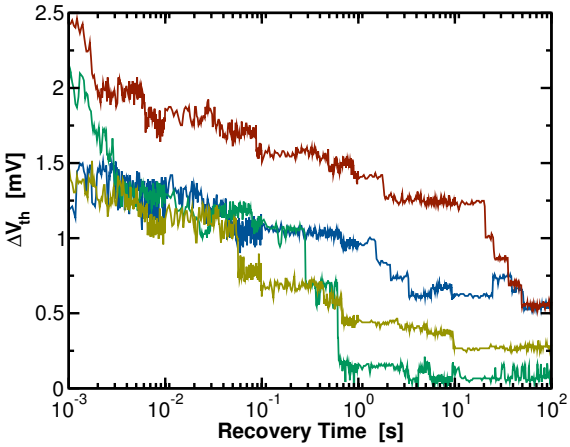

Figure 8.1: Five selected recovery traces with each discrete step corresponding to the emission of a single electron. The traces have been recorded on an nMOSFET ($W = 0.16\,\mu m$, $L = 2\,\mu m$) after BTI stress with $t_s = 100\,s$ and $V_{G,s} = 2.2\,V$. As clearly visible, the step heights of the discrete charge transitions are in the range of $\Delta V_{th} \approx 0.15\,mV$ and lower, a consequence of the relatively large device area. Such small step heights are equivalent to drain-source current fluctuations below 1 nA and increase the experimental effort. As in the NBTI/pMOSFET case, the emission times are distributed over a large time scale [MWC20].

efficiently apply the TDDS for PBTI/nMOSFET measurements a device with a scaled gate area of $A_{pMOS} \approx 10 \times A_{nMOS}$ has been deliberately chosen, compared to our previous studies [127, 146, 177]. As the average step height inversely scales with the gate area, considerably smaller threshold voltage shifts are obtained due to single electron emission events, visible in the recovery traces depicted in Figure 8.1 In the following the behavior of electron traps is studied in a nanoscale nMOSFET with $W = 0.16\,\mu m$ and $L = 2\,\mu m$ when the transistor is subjected to PBTI stress, for various bias conditions and temperatures. The stress voltages have been varied in the range of $1.4\,V \leq V_{G,s} \leq 2.2\,V$, the stress times between $100\,\mu s \leq t_s \leq 100\,s$, and the device temperature from 50 °C up to 80 °C. In order to collect a statistically relevant amount of data, the device has been repeatedly stressed and the recovery behavior recorded and analyzed [MWC26], see Figure 8.1.

To check the statistical relevance of the different observed step heights, the CCDF of nMOSFETs and pMOSFETs ($W = 150\,nm$, $L = 120\,nm$) of the same technology but different geometries are compared in Figure 8.2. To account for the dependence of the step heights on the geometry, the CCDF of the step heights is multiplied by the gate area. Furthermore, the CCDF in Figure 8.2 demonstrates that the step heights in SiO_2 nMOSFETs also roughly follow an exponential distribution, similar to defects causing NBTI in pMOSFETs. As a consequence, the defects in nMOSFETs and pMOSFETs are expected to have a similar distribution inside the device.

In the investigated pMOSFETs, three defects, namely n_1 with $\tau_e \approx 100\,ms$ and $d \approx 0.15\,mV$, n_4 with $\tau_e \approx 100\,ms$ and $d \approx 0.48\,mV$, and n_5 with $\tau_e \approx 1\,s$ and $d \approx 0.26\,mV$ could be identified, visible in the spectral map of Figure 8.3 at 50 °C, at a recovery voltage of $V_{G,r} = 0.41\,V$ after stressing the device at $V_{G,s} = 2.2\,V$. Both the capture and emission processes have been found to be temperature dependent. This behavior is reflected by the spectral maps in Figure 8.3 (left) and Figure 8.3 (middle) as the single clusters move towards lower emission times for increasing device temperature. Additionally, new defects are shifted into the measurement window at higher temperatures. This is in agreement with previous observations from NBTI/pMOS experiments confirming a strongly thermally activated electron emission similar to that of hole traps [MWC25]. As can be seen from the spectral maps in Figure 8.3 the necessity of a very high measurement

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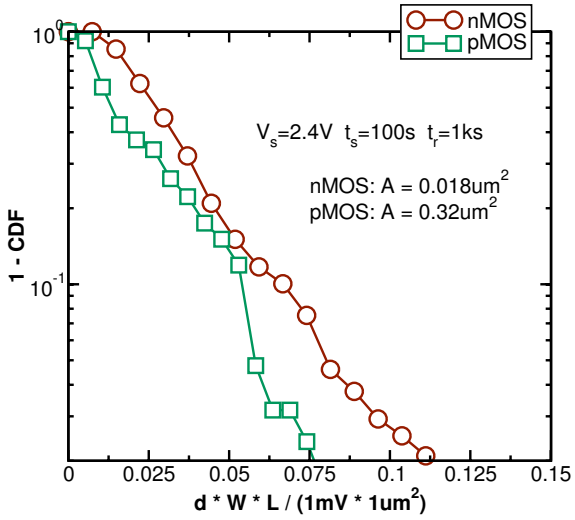

Figure 8.2: The CCDF of the step heights multiplied by the gate area $A = W \times L$ is depicted for nMOSFETs and pMOSFETs of the same technology (SiO_2 oxide with an EOT of $t_{EOT} = 2.2\,nm$). The CCDFs of the normalized step heights have a similar shape so that the defects in both devices are expected to have the same spatial depth distribution within the oxide. As a further consequence, traps causing PBTI in nMOSFETs have a similar electrostatic impact on the conducting channel as observed in pMOSFETs when NBTI is studied. The above statistics are extracted from recovery traces with $t_r = 1\,ks$ of several devices after oxide stress conditions of $V_{G,s} = 2.4\,V$ for $t_s = 100\,s$ [MWC20].

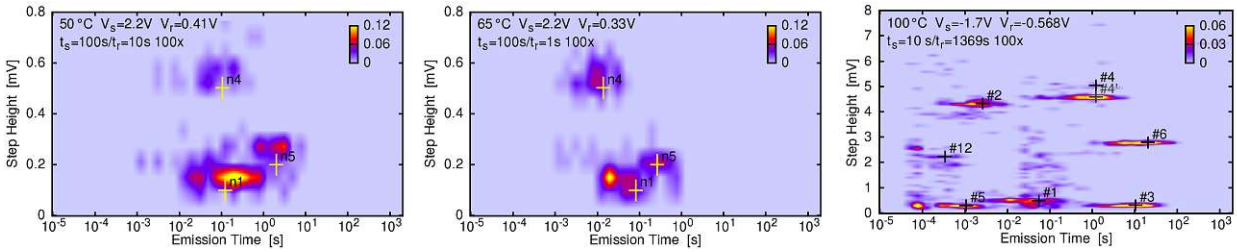

Figure 8.3.: The nMOSFET used for this study shows a handful of defects. The individual defects identified by clusters in the above spectral maps move towards lower emission times when the device temperature is increased (50 °C **left**, 65 °C **middle**). Compared to previous studies on NBTI/pMOSFETs (W=150 nm, L=120 nm) [127] (**right**), defects observed in PBTI/nMOSFET experiments show a similar response to the device temperature. Note that the single defects show very small step heights due to the investigated device area posing a challenge to the experimental design. From the three defects identified (n_1, n_4, n_5), defects n_1 and n_4 are studied in more detail [MWC20].

resolution is obvious. This is especially the case for defect n_1 which shows a step height of $d \approx 0.15\,mV$.

In Figure 8.4 the Arrhenius' plot of the defects n_1 and n_4 is shown when the device temperature T is varied between 50 °C and 85 °C. The thermally induced change of the capture and emission times of the defects n_1 and n_4 are approximated by an Arrhenius' law with activation energies E_A in the range of $0.37\,eV \leq E_A \leq 0.9\,eV$ for both electron capture and emission. In previous studies activation energies E_A for pMOSFETs have been found to be within the same range [MWC25]. This indicates, that defects causing PBTI on nMOSFETs follow the same temperature activated mechanism as the defects causing NBTI on pMOSFETs.

Two out of the three identified defects, namely n_1 and n_4, are studied in detail. The emission time of n_1 is independent of the applied recovery bias and remains constant over a wide recovery voltage range, see Figure 8.5. Quite to the contrary, the observed emission times of defect n_4 shows a strong recovery voltage dependence. Towards higher gate voltages the emission times τ_e

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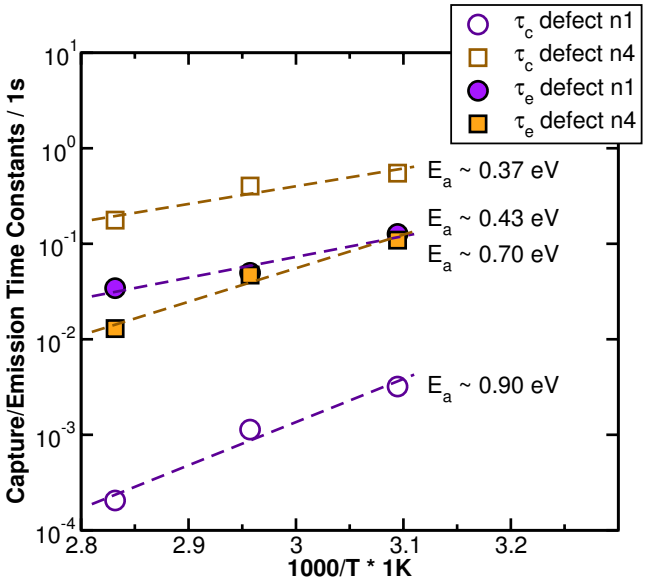

Figure 8.4: The temperature dependent capture and emission time constants recorded after BTI stress with $V_{G,s} = 2.2\,V$ and $t_s = 10\,V$ are visualized in an Arrhenius plot. The particular activation energies E_A assume similar values as those observed for pMOSFETs [127, 177, MWC20].

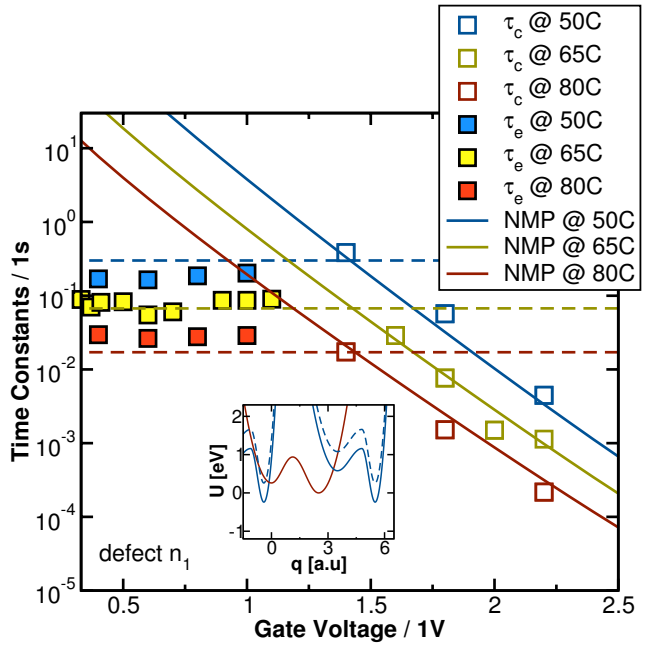

Figure 8.5: The gate voltage dependence of the capture time τ_c and the emission time τ_e is shown for defect n_1. The emission time appears to be independent of the applied bias (*fixed charge trap*) whereas the capture time shows a significant dependence. Good agreement between data (symbols) and model (lines) is obtained. The inset shows the configuration coordinate diagram of the NMP model required to fit the data [MWC20].

saturate and become bias-independent, see Figure 8.6. The capture time τ_c of the defects n_1 and n_4 depends exponentially on the stress recovery gate voltage $V_{G,r}$ and shows a strong temperature dependence. Both defects show a similar temperature activation for charge capture and emission, see Figure 8.4. Additionally, an evaluation of the model against the experimental TDDS data is given in Figure 8.5 and Figure 8.6. As can be seen, the trapping kinetics can be nicely explained by the four-state NMP model.

As recoverable BTI and RTN are apparently caused by the same defects [131, 178], the bias conditions under which RTN from particular defects can be measured, becomes predictable [MWC25].

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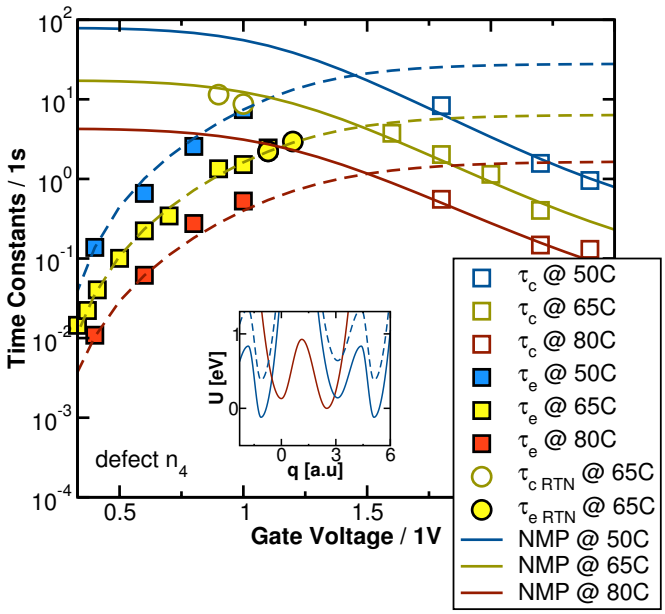

Figure 8.6: Contrary to defect n_1, the emission time of defect n_4 shows a very strong dependence on the gate voltage, a behavior attributed to *switching traps*. Just like the fixed charge trap behavior, the switching trap behavior can be well explained by the four-state NMP model (lines). The inset shows the configuration coordinate diagram of the NMP model [MWC20].

Therefore two conditions have to be fulfilled: *(i)* The carrier capture and emission times τ_c and τ_e have to be about the same order of magnitude and *(ii)* the sum of the capture and emission time has to be smaller than the TDDS measurement window $\tau_c + \tau_e \ll t_r$ and *(iii)* the sampling frequency has to be selected that $f_s << 1/\tau_c$ and $f_s << 1/\tau_e$. The first condition is necessary in order to ensure that the charge capture and charge emission events occur within a certain time window. Conversely, for $\tau_c < \tau_e$ the defect will more favorable remain in its charge state and it will take very long for the charge emission to occur. For $\tau_c > \tau_e$ the defect will be mainly neutral and it will take very to for the defect to become charged. Considering defect n_4, the first prerequisite is fulfilled near the intersection point of the capture and emission times estimated by the NMP model. The second prerequisite is necessary to ensure that both charge transitions occur withing the TDDS measurement window $\tau_c + \tau_e \ll t_r$. To account for the third condition the choice of the sampling frequency and the recovery time plays an important role. The sampling frequency has to be selected that $f_s << 1/\tau_c$ and $f_s << 1/\tau_e$ because otherwise the charge transitions are to fast and will not be visible in the measurement traces.

By considering the previously mentioned requirements capture and emission times can be extracted from RTN. As can be seen in Figure 8.6 (yellow circles) several charge transition time data points for defect n_4 in the gate voltage range of $1.0\,\mathrm{V} \leq V_{GS} \leq 1.2\,\mathrm{V}$ at $T = 65\,^{\circ}\mathrm{C}$ are extracted from such RTN signal.

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9

Negative Bias Temperature Instabilities in High-k SiGe Transistors

To sustain Moores' Law, conventional MOSFETs have been scaled down to the nanometer regime. However, due to the limited subthreshold slope, the device supply voltages cannot be scaled in the same manner as the device geometry without any losses of the device performance. As a consequence, the oxide fields occurring in the scaled devices increase, thereby leading to an increase of the gate leakage current. In order to avoid the detrimental increase of the gate leakage currents, high-k (HK) gate stacks together with metal gate (MG) contacts are used in state-of-the-art MOSFETs. The fabricated high-k gate stack employed in such devices typically consists of a Hafniumoxide (HfO_2) layer on top of a SiO_2 interfacial layer [2, 3, 4, 5]. Just like with transistors using SiO_2 or SiON gate dielectrics, BTI is one of the most critical reliability issues in HK transistors as well.

To further enhance the performance of transistors, SiGe quantum-well pMOSFETs have been proposed [179, 180, 181, 182], see Figure 9.1 (left). These transistors employ HK gate stacks on top of a SiGe quantum-well layer, and have been initially developed to take advantage of the higher carrier mobility of the strained SiGe layer. Quite surprisingly, it was found that NBTI is considerably smaller in these quantum-well devices. Furthermore, a strong dependence of the absolute threshold voltage shift on the Si cap layer thickness together with a stronger oxide field acceleration with respect to Si devices was reported. It has been speculated that these observations are a consequence of the energetical realignment of the SiGe channel with respect to the gate stack [179, MWC24]. As the previous observations were made on large-area devices, a more precise justification was difficult to give. As previously mentioned, using large-area devices only the average response of a large number of defects can be studied. However, to provide a more detailed understanding of this phenomenon, the impact of the individual constituents has to be studied.

To study the impact of the Si cap layer thickness on the device performance devices with two different geometries are compared, namely nanoscale SiGe pMOSFETs with a gate width of $W = 90\,\text{nm}$ and a gate length of $L = 35\,\text{nm}$, and large-area SiGe pMOSFETs with $W = L = 1\,\mu\text{m}$. For

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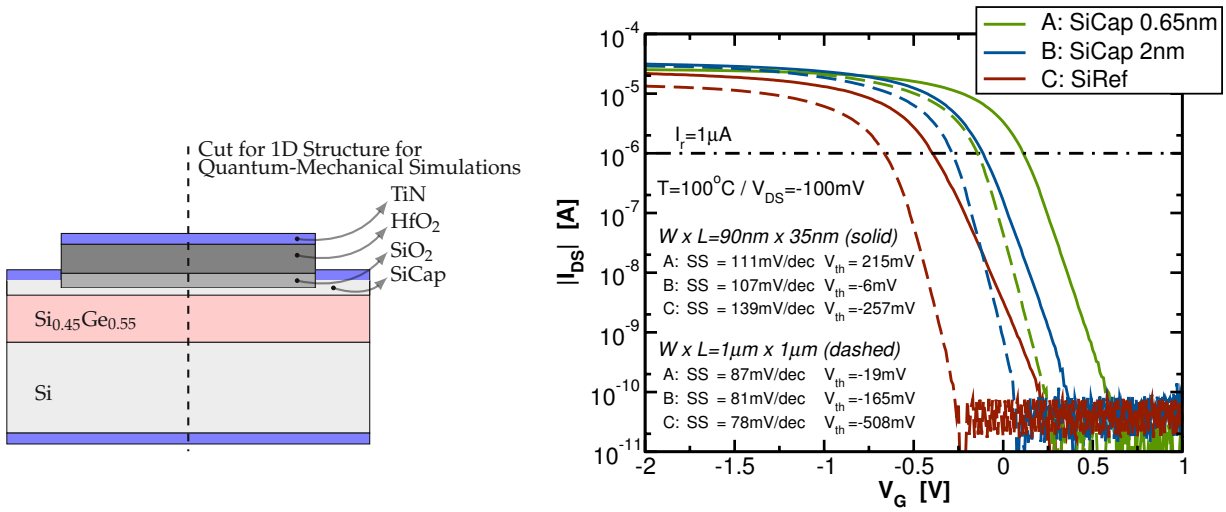

Figure 9.1.: (**left**) Schematic view of the studied high-k metal gate (HKMG) devices show a thin Si cap layer on top of a strained $Si_{0.45}Ge_{0.55}$ layer. In this work, nanoscale and large-area devices with two different Si cap layer thicknesses of $t_{SiCap} = 0.65\,nm$ and $t_{SiCap} = 2\,nm$ and a reference Si transistor have been studied in detail. Therefore quantum-mechanical simulations and classical devices simulations have been carried out. While the quantum-mechanical simulations have been performed using a simplified 1D model given by a cut perpendicular to the channel through the middle of gate contact, the latter uses 2D devices structures. (**right**) The $I_{DS}(V_{GS})$ characteristics of all studied large-area and nanoscale devices show that the threshold voltage and the sub-threshold slope (SS) vary with the thickness of the Si cap layer. The threshold voltage is extracted as the gate voltage at which $I_{DS} = -70\,nA \cdot W/L$. As can be seen, the devices with the thin Si cap layer have the largest threshold voltage V_{th} whereas the reference devices show the smallest V_{th} [MWJ2, MWJ1].

each geometry three different device variants, namely devices with a Si cap layer thickness of $t_{SiCap} = 0.65\,nm$ and $t_{SiCap} = 2\,nm$, as well as a conventional Si transistor which is the reference device, are studied. The $I_{DS}(V_{GS})$ characteristics of the corresponding devices is shown in Figure 9.1 (left). A strong correlation between the threshold voltage, extracted as the voltage at which $I_{DS} = -70\,nA \cdot W/L$, and the Si cap layer thickness is visible. The devices with the thin Si cap layer show the highest threshold voltage whereas the lowest values are observed for the reference devices. These different threshold voltages have to be considered during NBTI characterization when stress and recovery experiments are performed. In general, the oxide stress field $E_{ox,s}^{eff}$ can be estimated by

$$E_{ox,s}^{eff} \approx \frac{V_G^{ov}}{t_{EOT}} = \frac{V_{G,s} - V_{th}}{t_{EOT}} \tag{9.1}$$

with V_G^{ov} the gate overdrive voltage, t_{EOT} the effective oxide thickness, $V_{G,s}$ the stress voltage and V_{th} the threshold voltage of the device. In order to apply similar stress and recovery oxide fields different gate voltages have to be used for the stress/measure experiments carried out at the different device variants. This is particularly important as the degradation and recovery of the threshold voltage strongly depends on the stress and recovery oxide field.

In the following section, the impact of NBTI on nanoscale and large-area SiGe HKMG pMOSFETs is investigated. Starting with the description of the device electrostatics using quantum-mech-

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anical and classical device simulations, the device structure and doping profiles are reproduced. Next, the TDDS is used to study single defects in nanoscale pMOSFETs. By employing the four-state NMP model, see Section 4.3.3, the charge transition times of single defects are explained. Afterwards, charge trapping in large-area SiGe devices is discussed and modeled using the four-state NMP model in combination with our classical device simulator Minimos-NT. Finally, the lifetime projections which are based on our simulations are presented.

9.1. Device Simulation

At the begin of our investigations the device structure has to be created. Therefore quantum-mechanical (QM) and classical device simulations are carried out. The QM simulations are necessary to consider quantum-effects in nanoscale devices and are performed on a simplified 1D device structure. Afterwards, classical devices simulations are performed using Minimos-NT and a 2D device structure. The latter simulations are required to apply our four-state NMP model to explain charge trapping in these devices.

9.1.1. Quantum Mechanical Simulations

As the thin SiGe channel underneath the Si cap layer requires careful consideration, detailed QM simulations are carried out. These are performed by using our QM Schrödinger Poisson solver VSP to calibrate the device structures to the experimental $C(V)$ characteristics of large-area devices with $W = L = 10\,\mu m$ [183, 184]. This is achieved by thoroughly adjusting the individual layer thicknesses using a simplified one-dimensional structure of our transistor, see Figure 9.1. From the QM simulations the band structure and the corresponding sub-bands are obtained and shown in Figure 9.2. The peaks of the first two wavefunctions in the subbands are located in the SiGe near the SiGe/Sicap interface. As the subbands give the probability of finding the carriers, the peaks in the SiGe suggest that the conducting channel is more likely located in the SiGe layer than in the Si cap layer. Furthermore, the charge separately calculated for the SiGe and Si cap layer at different gate biases for the different device variants is notably larger inside the SiGe layer than in the Si cap layer, see Figure 9.3. This result confirms the previous claim that the channel is primarily in the SiGe layer and is particularly important when charge trapping is considered in these devices. The prevalent channel inside the SiGe layer will be demonstrated to be the cause for the reduced susceptibility of the SiGe device to NBTI.

9.1.2. Classical Device Simulations

Based on the layer thicknesses and bulk doping density obtained from the one-dimensional QM simulations, the two-dimensional device structures of the pMOSFETs are created. For this purpose, the classical device simulator Minimos-NT [185] is used and a quantum-corrected drift-diffusion model is solved [186].

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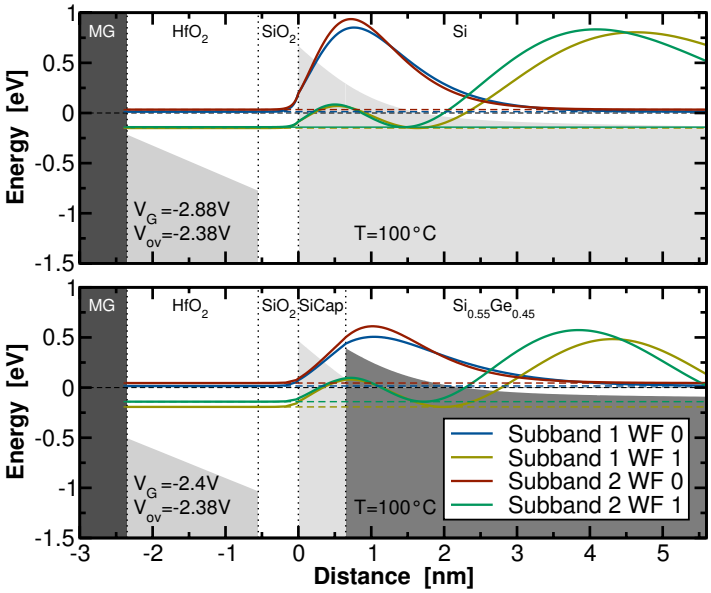

Figure 9.2: The band diagrams of (**top**) the reference device and (**bottom**) the device with $t_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$ are shown at stress bias conditions. The wavefunctions (WF) of the corresponding subbands highlighted are calculated with our Schrödinger-Poisson solver. Note that for the SiGe device the peaks of the wavefunctions are located in the SiGe and near the SiGe/Si cap interface. Consequently, the current is dominantly located inside the SiGe layer. In contrast, for the reference device the peaks of the wavefunctions, and as a consequence the conducting channel, are closer to the SiO_2/Si interface. This observation is very important, because the closer the traps are located to the channel the larger the step heights are, compare CCDF presented in part one [MWJ1]. As the device variants have different threshold voltages, the band diagrams are calculated at the same overdrive voltage in order to obtain comparable carrier concentrations in the inversion layer.The band-diagram of the device with $t_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$ at stress bias conditions [MWJ2].

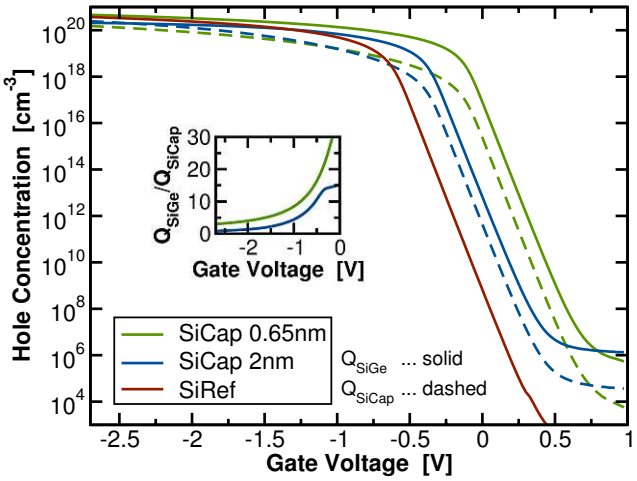

Figure 9.3: The hole concentration for the Si cap layer and the SiGe layer is calculated at different gate biases from our QM simulations. As can be seen, the charge present in the SiGe layer exceeds the charge of the Si cap layer, confirming the channel to be more likely located in the SiGe layer. The inset gives the ratio between the charge in the SiGe and Si cap layers. With increasing Si cap layer thickness, the channel in the SiGe is less pronounced, a behavior that weakens the superior NBTI behavior of the SiGe devices [MWJ2].

As can be seen from Figure 9.4, the simulations which have been performed using the calibrated 2D devices nicely reproduce the experimental $I_{\mathrm{DS}}(V_{\mathrm{GS}})$ characteristics. From our 2D device simulation the surface potential and the carrier concentration at the interface can be calculated. Both quantities are used in combination with the four-state NMP model to explain the intricate capture and emission times of the single defects measured on our nanoscale devices and the continuous recovery observed on large-area transistors. Note that all $I_{\mathrm{DS}}(V_{\mathrm{GS}})$ characteristics have been reproduced using the same devices structure with an appropriate gate area and the corresponding Si cap layer thickness.

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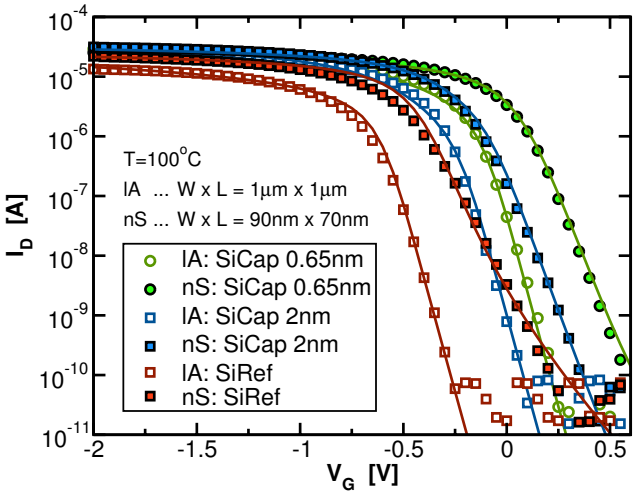

Figure 9.4: The $I_{DS}(V_{GS})$ characteristics of the large-area (open symbols) and the nanoscale pMOSFETs (closed symbols) have been measured using the TMI. Using the classical device simulator Minimos-NT the characteristics can be nicely reproduced. This has been achieved using the same device structure with the corresponding Si cap layer thicknesses and an appropriate gate area [MWJ2].

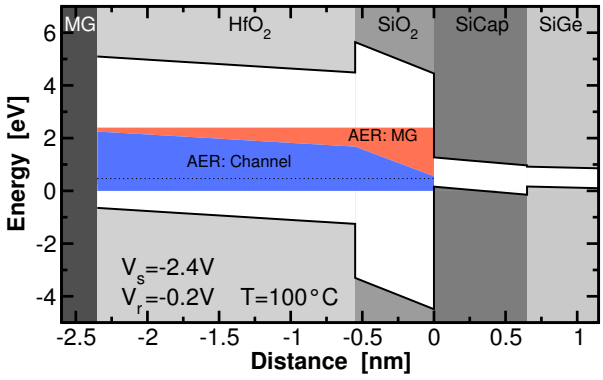

Figure 9.5: The band-diagram of the SiGe transistor with $t_{SiCap} = 0.65\,nm$ is shown with the corresponding active energy region (AER) calculated for a stress bias of $V_{G,s} = -2.4\,V$ and a recovery bias of $V_{G,r} = -0.2\,V$. As can be seen, the AERs are separated into an area which can exchange their charge with the MG (red) and in an AER (blue) for charge exchange with the conducting channel. Additionally, the conducting channel at the SiCap/SiGe interface is shown in the AER (dotted line) [MWJ2].

Based on our classical device simulations the band-diagram of our SiGe devices can be calculated. In Figure 9.5 the valance and conduction band edges are shown at stress bias conditions. In addition, the so called active energy region (AER) for charge trapping is highlighted in the band-diagram. This area is very important as it is a necessary condition for a single defect contributing to NBTI that at defined stress and recovery bias conditions the defect is energetically located inside such an AER. Only those defects which are energetically arranged inside the AER can change their charge state during stress and thus contribute to a change in the threshold voltage. The borders of the AER are defined by the considered stress and recovery gate bias. Thus at stress bias conditions the energetic level E_T of a defect located at x_T inside the gate stack has to lie above the corresponding Fermi level E_F

$$E_T + qV_{G,s} - q\phi^s(x_T) > E_F \tag{9.2}$$

and below the Fermi-level at recovery bias conditions

$$E_T + qV_{G,r} - q\phi^r(x_T) < E_F \tag{9.3}$$

with $\phi^s(x)$ and $\phi^r(x)$ the position dependent potential drop across the gate stack for stress and recovery bias conditions, respectively. Furthermore, the AER region can be separated into an AER for charge trapping with the MG and into an AER for charge trapping with the conduction channel. Both AERs can be described using (9.2) and (9.3) with its corresponding Fermi levels. Additionally,

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the energy level of the conducting channel located in the SiGe, which is by itself determined by the t_{SiCap} dependent band offset between the Si cap and SiGe, is visible in the AER in Figure 9.5. As this certain energy level is higher than the Fermi level of the Si cap only a reduced number of defects can capture a hole from the SiGe.

9.2. Single Charge Trapping

To get a detail insight into the charge trapping kinetics, single defects have to be studied. This can be achieved using nanoscale devices by employing the TDDS. In the following, the results of single defect characterization using the scaled SiGe devices with different Si cap layer thicknesses and the reference devices are discussed. First, the recovery traces and the complementary cumulative distribution functions (CCDFs) of the step heights of the three device variants are compared. Next, the charge transition times of various single defects are extracted and finally modeled using our four-state NMP model.

9.2.1. Characterization of Single Defects

To experimentally characterize a single defect, its intricate bias and temperature dependent capture and emission times have to be determined. In combination with the step height, that is the threshold voltage shift caused by this single defect, the transition times are more or less unique fingerprints of each single defect. To measure the single defect characteristics the TDDS is used in combination with our developed TMI, see Section 5 and Section 6. Using our equipment, the nanoscale SiGe devices with different Si cap layer thicknesses and the reference devices are repeatedly stressed at constant gate voltages varied between $V_{\mathrm{G,s}} \in [-0.7\,\mathrm{V}, -2.6\,\mathrm{V}]$ during which the drain-source voltage is $V_{\mathrm{D,s}} = 0\,\mathrm{V}$ to prevent HCD related effects. After each stress cycle a recovery gate voltage in the range of $V_{\mathrm{G,r}} \in [0.1\,\mathrm{V}, -0.5\,\mathrm{V}]$ is applied and the drain-source current is recorded at a drain bias of $V_{\mathrm{D,r}} = -100\,\mathrm{mV}$.

The initial recovery traces are shown in Figure 9.6 for all three device variants and reveal that a large number of discrete ΔV_{th} steps are present. Each ΔV_{th} step corresponds to a single defect which has been charged during the stress cycle and uncharges during the recovery cycle. Although all three DUTs nominally have the same gate stack, the number of steps in the recovery traces differs significantly in all three devices. In particular, for the same stress voltage the devices with the thickest Si cap have the largest number of active defects, followed by the Si reference device. The smallest number of active defects is observed in the SiGe device with the thinnest Si cap. As can be seen, at the end of the measured recovery traces a significant threshold voltage shift ΔV_{th} remains. This is due to defects which have been charged during the stress cycle but have not emitted their charge during the recovery cycle. A further increase of the measurement window, that is the recovery time, would lead to a lower remaining ΔV_{th}. It has to be noted that single defects can have emission times up to weeks, month or even years [MWC19]. Following from that, a negligible remaining ΔV_{th} would require ultra long recovery times.

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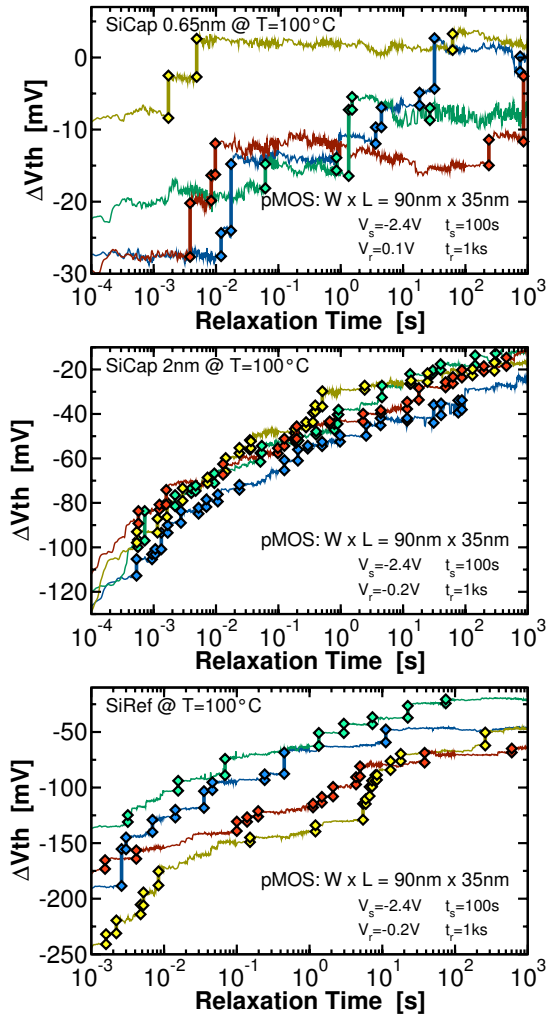

Figure 9.6: The recovery traces of the studied nanoscale SiGe pMOSFETs are recorded after NBTI stress and clearly show a discrete recovery which reveals the individual defects. Each discrete step corresponds to the emission of a single hole from a defect in the gate stack, while the step-height shows its contribution to the threshold voltage shift ΔV_{th}. As can be seen from the recovery traces, the number of active defects increase with larger Si cap layer thickness (**top**: $t_{\text{SiCap}} = 0.65\,\text{nm}$ and **middle**: $t_{\text{SiCap}} = 2\,\text{nm}$). The traces from the reference pMOSFETs without a SiGe layer (**bottom**) show the largest threshold voltage shift among the studied devices. Note that relatively high stress voltages had to be used to cause a measurable degradation of the device with the thinnest Si cap layer [MWJ1].

Considering the $I_{\text{DS}}(V_{\text{GS}})$ characteristics, in Figure 9.1 (right), all three technologies have different threshold voltages. Using (9.1), apparently the device with the thinnest Si cap is subjected to the largest overdrive, however, it still degraded less than all the others. Thus, the difference in the threshold voltages does not explain the observed difference in the device threshold voltage shift.

To study the distribution of the step heights, the complementary cumulative distribution functions (CCDFs) of the step heights d of the hole traps present in more than 680 nanoscale transistors of all device variants is shown in Figure 9.7 (left). The mentioned active trap density N_{T} and average step height of a single defect η is extracted using ((5.9)) and ((5.10)) for both the unimodal and the bimodal CCDF, respectively. As can be seen from the CCDFs, the step heights of the transistors with $t_{\text{SiCap}} = 0.65\,\text{nm}$ and the reference transistors appear to be unimodally distributed. However, the devices with $t_{\text{SiCap}} = 0.65\,\text{nm}$ have a significantly lower mean number of defects, $N_{\text{T}} = 6.24$, compared to the reference transistor with $N_{\text{T}} = 36.85$. A particularly noteworthy observation is that the step heights for the devices with the thick Si cap layer follow a bimodal distribution. Furthermore, the unimodally distributed CCDF of the $t_{\text{SiCap}} = 0.65\,\text{nm}$ devices and the first part of the bimodal CCDF of the transistors with $t_{\text{SiCap}} = 2\,\text{nm}$ can both be fitted with $\eta = 2.14$. The

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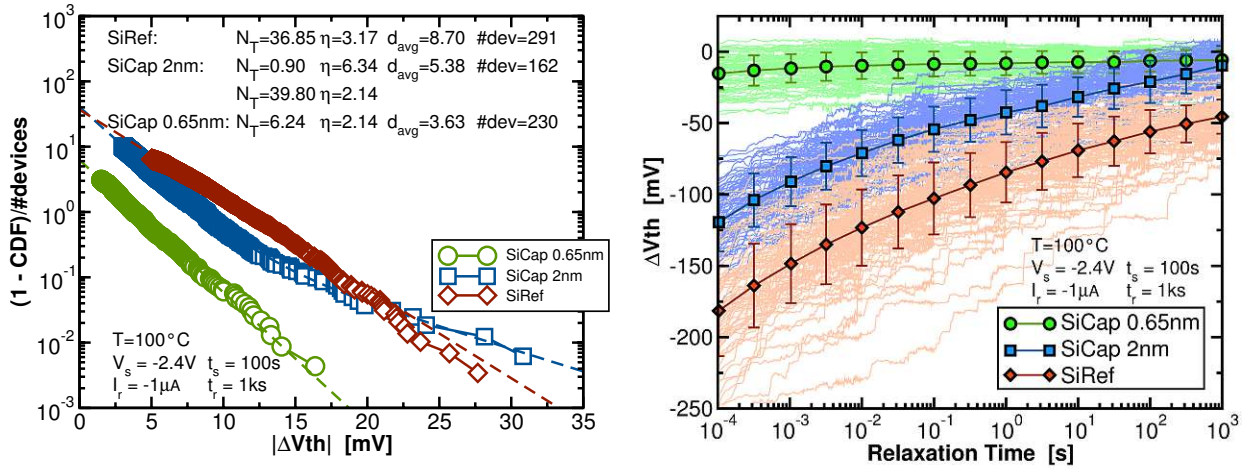

Figure 9.7.: (**left**) The step heights d typically follow a unimodal distribution for the reference devices and the SiGe pMOSFETs with the thinnest Si cap layer of $t_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$. Conversely, the devices with $t_{\mathrm{SiCap}} = 2\,\mathrm{nm}$ show a bimodal CCDF with a similar value of η for steps smaller than 12 mV as observed for the CCDF for the $t_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$ devices. Quite interestingly, the number of accessible defects N_{T} and the averaged step heights d_{avg} increase with the Si cap layer thickness. The increasing d_{avg} is an indicator that the channel gets closer to the interface near the gate stack. As a consequence of the increased d_{avg} the number of defects N_{T} which can be monitored using TDDS also increase. Thus, both the larger d_{avg} and the larger N_{T} indicate that the channel is located more closely to the IL/SiCap interface for the devices with the thick Si cap layer and the reference transistors compared to the devices with the thin Si cap layer. (**right**) The averages of the single traces used to calculate the CCDF for the three studied device structures are shown. In accordance with the CCDF, the reference MOSFETs show the largest threshold voltage shift ΔV_{th} whereas for the SiGe transistors with $t_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$ a very small ΔV_{th} shift is observed. Nonetheless, a remarkable reduction of NBTI is achieved for devices with a thin Si cap layer. Note that all experiments are performed at the same overdrive voltage to ensure comparable stress and recovery oxide fields [MWJ1].

second part of the bimodal CCDF shows a significantly larger value for η, indicating that the defects are closer to the channel than is the case for smaller η.

The unimodal CCDFs appear to be a consequence of the dominant conduction channel present at the SiCap/SiGe interface and the channel at the SiO_2/SiCap interface for the device with the thinnest Si cap layer and the reference Si devices, respectively. For a bimodal CCDF the defects appear to interact with two conducting channels. Furthermore, in nanoscale devices the position of random discrete dopands within the channel influences the percolation path of the drain-source current. It is conceivable that the dopands within the Si cap are unfavorably located in a way that only a single current path either in the SiGe layer or at the SiO_2/SiCap interface is present whereas the other channel is turned off. Moreover, it is possible that defects located near the SiO_2/SiCap interface can influence the potential of both channels, leading to very large step heights. From that it follows that there is no unique relation between the step height of a single defect and the corresponding channel the single defect is interacting with. However, the CCDF is created from a large number of defects (more than 4000 for the devices with the thick Si cap layer) and devices. Based on the η values observed from our experimental data for the devices with the thick Si cap layer we link the first part of the bimodal CCDF to charge trapping interaction with a channel

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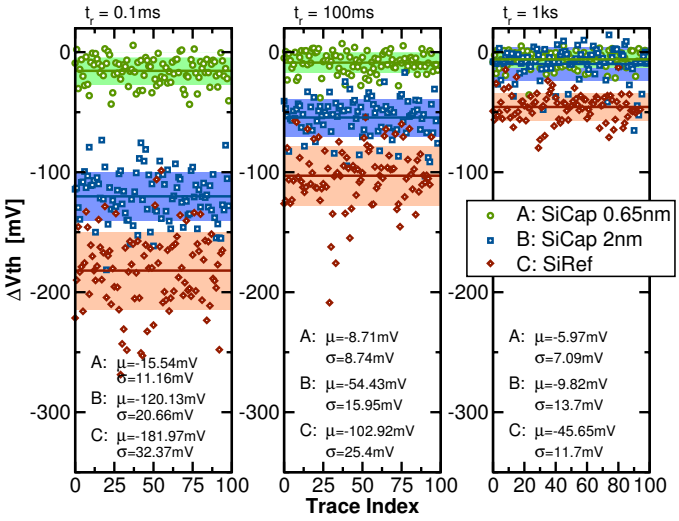

Figure 9.8: The threshold voltage shift ΔV_{th} (symbols) measured after certain recovery times (**left** $t_{\mathrm{r}} = 0.1\,\mathrm{ms}$, **middle** $t_{\mathrm{r}} = 100\,\mathrm{ms}$ and **right** $t_{\mathrm{r}} = 1\,\mathrm{ks}$) is plotted for the different device variants versus the trace index. Note that the standard deviation (marked by colored area) of the ΔV_{th} distribution also decreases for larger recovery times. Also note that the standard deviation is related to the maximum observed step height of the device variants. The largest observed step height of a single defect for the devices with the thin Si cap layer is about half of the maximum step height of the two other technologies, see Figure 9.7 (left) [MWJ1].

present in the SiGe layer and the tail of the distribution to a superposition of charge trapping interactions between the gate stack and the SiGe and/or SiO_2/SiCap channel.

The average ΔV_{th} of the single traces used to calculate the CCDF is shown in Figure 9.7 (right). In accordance with the CCDF, the devices with the thinnest Si cap layer show the smallest threshold voltage shift whereas an approximately ten times higher average threshold voltage shift is observed for the reference devices. This trend reflects the decreased NBTI present in the SiGe devices with respect to the reference devices.

At that point it has to be noted that the recovery is very sensitive to the readout/recovery bias conditions. To ensure that the recovery traces are recorded at comparable bias conditions, a current criterion is used to determine the recovery voltage. As shown in the $I_{\mathrm{DS}}(V_{\mathrm{GS}})$ characteristics in Figure 9.1, the recovery voltage is set to $V_{\mathrm{G,r}} = V_{\mathrm{GS}}(I_{\mathrm{DS}} = -1\,\mu\mathrm{A})$. According to (9.1) a comparable oxide field is then applied to all DUTs during recovery. Using the current criterion the recovery traces used for the computation of the CCDF are recorded.

Using the experimental recovery traces from Figure 9.7 (right) the evaluation of the threshold voltage shift of 100 devices for the three device variants at certain recovery times is shown in Figure 9.8. The standard deviation of the ΔV_{th} distribution is found to decreases for larger recovery times. Quite remarkably, a correlation between the standard deviation σ and the maximum observed step height for a device variant is visible. The larger the largest observed step is, see Figure 9.7 (left), the larger σ is. This is also the case for the standard deviations from the ΔV_{th} distributions analyzed at certain recovery times.

Next, the discrete ΔV_{th} steps from the recovery traces of various SiGe transistors are extracted and binned into spectral maps, see Section 5.1. In such spectral maps the single defects are represented by clusters. From our SiGe MOSFETs, eight defects have been identified in the device variant with $t_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$ and the reference transistors and seven defects are studied in more detail in the devices with $t_{\mathrm{SiCap}} = 2\,\mathrm{nm}$. Considering the spectral maps, the temperature dependence of charge emission of all defects can be seen very well. When the device temperature is increased, the clusters move towards shorter emission times confirming the temperature activation of charge

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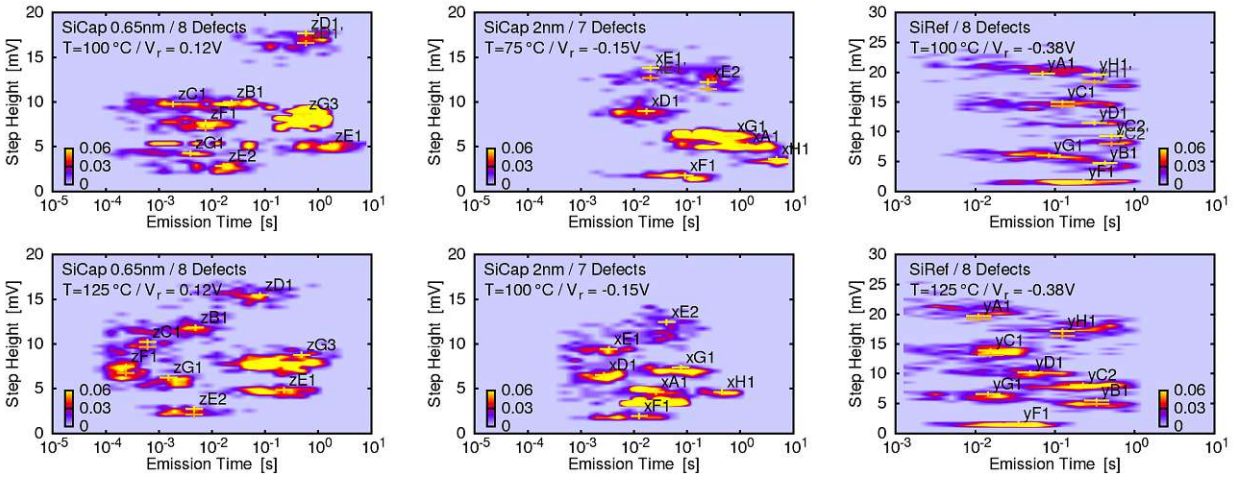

Figure 9.9.: The defects identified in the three different pMOSFET types are collected in spectral maps at two different temperatures (**left**: $t_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$, **middle**: $t_{\mathrm{SiCap}} = 2\,\mathrm{nm}$, and the reference Si devices **right**). As can be seen, the single clusters move towards shorter emission times when the device temperature is increased (compare **top** and **bottom** row) [MWJ1].

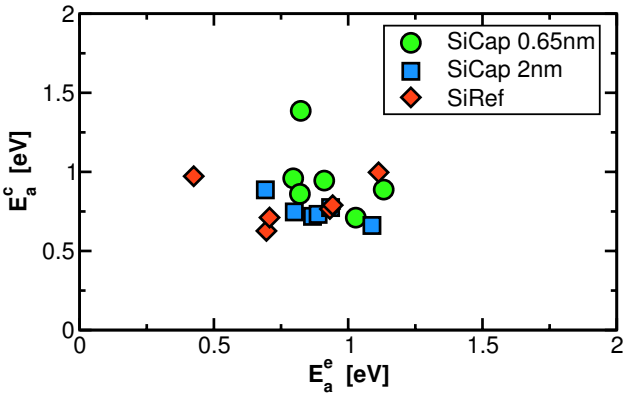

Figure 9.10: The 23 single defects in our nanoscale devices show a broad distribution of their activation energies for charge capture an emission [MWJ1].

transitions. To determine the thermal activation energies of charge capture and emission, the transition time characteristics of the single defects are recorded at different temperatures. Afterwards, the time dependence can be described by an Arrhenius' Law, see Section 5.3. The activation energies of 23 single defects are shown in Figure 9.10. A broad distribution of activation energies for charge capture and emission is found.

9.2.2. Modeling of Single-Defects

By probing the nanoscale SiGe devices over several month the capture and emission time characteristics and the bias and temperature dependence of various single defects has been extracted. Among these single defects, bias independent emission times, which are typically referred to as *fixed oxide traps*, and *switching traps* with bias dependent emission times are found, see Figure 9.11. Conversely, the capture time of the fixed and switching trap strongly depends on the NBTI stress

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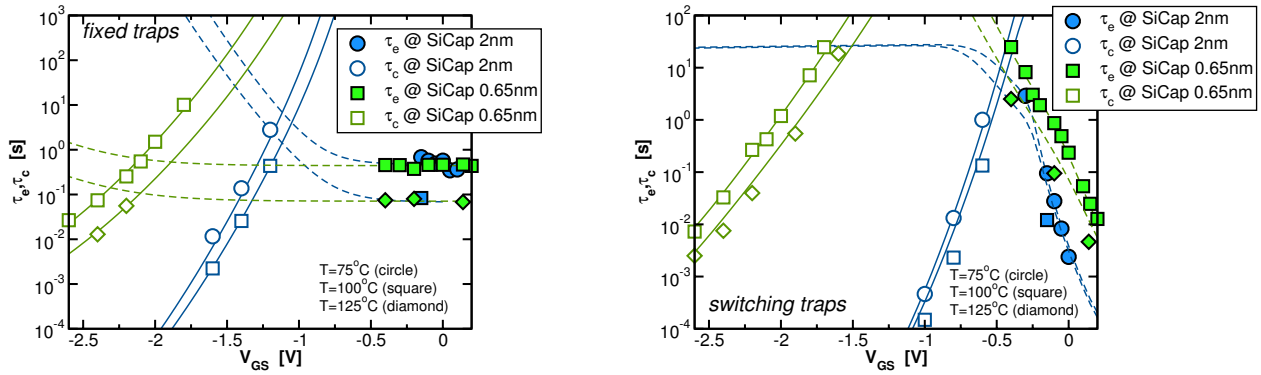

Figure 9.11.: (**left**) *Fixed hole traps* are found in the analyzed devices with bias independent emission times around the threshold voltage. (**right**) In addition to fixed hole traps, *switching traps* with a strong bias dependence of the emission time are also found. The bias and temperature dependence of both cases are very well reproduced by the four-state NMP model [MWJ2].

bias. An increase of the device temperature affects both, the capture and emission time, and leads to shorter charge transition times.

To explain the bias and temperature dependent transition times, the four-state NMP model is used, see Section 4.3.3. The NMP transition rates are thereby calculated using our classical device Minimos-NT, and the initially calibrated device structure. Using our simulation framework the defect parameters of the four-state NMP model are adjusted to reproduce the experimental capture and emission times of the single defects. As can be seen in Figure 9.11, the four-state NMP model explains the capture and emission time characteristics of the fixed oxide traps and switching traps very well. Note that in the particular context of our SiGe devices it was found to be of utmost importance that the four-state NMP model not only considers the charge exchange with the *conducting channel* but also with the *metal-gate* as recently demonstrated for very thin oxides [187].

When transition time characteristics of single defects are investigated using the four-state NMP model, the bias dependence of the capture time plays an important role because in the four-state NMP model it is determined by the trap depth, see Section 4.3.3.1. According to the NMP model, the charge capture time is given by

$$\tau_c = \tau_{12'} + \tau_{2'2}\left(1 + \frac{\tau_{12'}}{\tau_{2'1}}\right) \tag{9.4}$$

with τ_{ij} the first passage times between the individual states [177]. Considering the transitions $1 \rightarrow 2'$ and $2' \rightarrow 1$ as NMP barriers and the transition $2' \rightarrow 2$ as a thermal barrier, the capture time dependence on the stress bias is

$$\frac{\partial \tau_c}{\partial V_{G,s}} = -\beta q \underbrace{\frac{\partial \phi(x, V_{G,s})}{\partial V_{G,s}}}_{\phi'(x)} \left(\frac{1}{2}\tau_{12'} + \tau_{2'2}\frac{\tau_{12'}}{\tau_{2'1}}\right) \tag{9.5}$$

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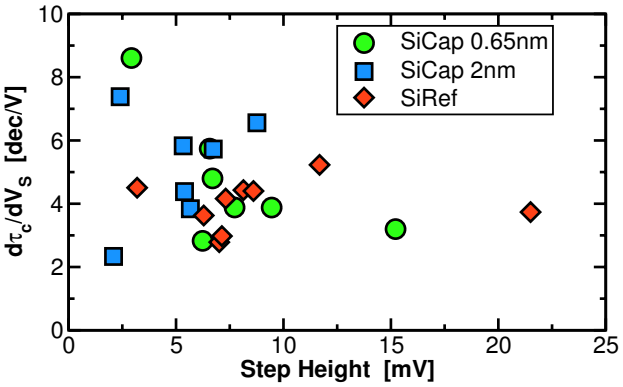

Figure 9.12: To check if any trend in the bias dependence of the capture times is present for a certain device technology, the bias dependence of τ_c is plotted versus the corresponding step heights. As can be seen, the capture times of all defects of all devices of the three technologies show similar bias dependence.

with $\beta = 1/(k_B T)$ and $\phi(x, V_{G,s})$ the potential inside the gate stack. For the employed gate stack we get

$$\phi'(x) = \begin{cases} x \leq t_{SiO_2} & 1/(1+\alpha^{-1}) \times x/t_{SiO_2} \\ x > t_{SiO_2} & 1/(1+\alpha^{-1}) + \\ & 1/(1+\alpha) \times (x - t_{SiO_2})/t_{HfO_2} \end{cases}$$

with $\alpha = (t_{HfO_2}/t_{SiO_2})(\epsilon_{SiO_2}/\epsilon_{HfO_2})$, whereas $x = 0$ is at the IL/SiCap interface. The farther the defect is away from the IL/SiCap interface the larger $\phi'(x)$ becomes and $\partial\tau_c/\partial V_{G,s}$ increases. Thus for a strong bias dependence of the capture time the defect must be located more closely to the MG, and in case of a weaker bias dependence the defect resides near the Si cap layer. As can be seen in Figure 9.12, among all device variants no correlation between the bias dependence of the capture time and the Si cap layer thickness has been found and thus a similar trap depth distribution among the device variants must be present.

9.3. NBTI in Large Area SiGe Transistors

Next, the recovery behavior of large-area SiGe pMOSFETs, W=1 µm and L=1 µm, subjected to NBTI stress is studied. In contrast to their nanoscale counterparts, where single defects can be studied, the average recovery of a large number of defects is recorded for these devices. The reason is that for an increasing device area A a smaller average contribution of a single charge $\eta_{um}/\eta_{nm} = A_{um}/A_{nm}$ is obtained (the indices *nm* and *um* denote the nanoscale and large-area devices, respectively).

To monitor the recovery of the large-area transistors, a conventional extended measure-stress-measure (eMSM) scheme is used [188]. Each eMSM cycle is recorded at the same stress and recovery bias conditions and at the same device temperature. For a measurement cycle the stress and recovery times are varied as given below.

$$\begin{pmatrix} t_s \\ t_r \end{pmatrix} = \begin{pmatrix} 1\,\text{ms} & 10\,\text{ms} & \dots & 10\,\text{s} & 100\,\text{s} & 1\,\text{ks} \\ 100\,\text{s} & 100\,\text{s} & \dots & 100\,\text{s} & 1\,\text{ks} & 10\,\text{ks} \end{pmatrix}$$

Furthermore, the gate bias during stress is varied in the range of $V_{G,s} \in [-1.6\,\text{V}, -1.7\,\text{V}, ..., -2.4\,\text{V}]$, the gate voltage during recovery is set to $V_{G,r} = -0.33\,\text{V}$ and the device temperature is not

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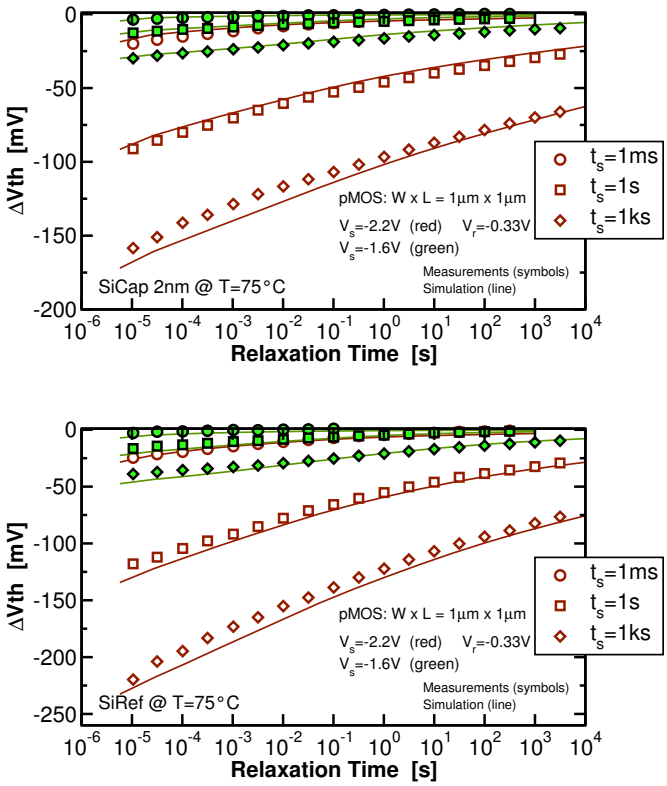

Figure 9.13: The recorded recovery on large-area devices subjected to NBTI stress with increasing stress times and two different stress biases for the devices with (**top**) $t_{\mathrm{SiCap}} = 2\,\mathrm{nm}$ and (**bottom**) the reference Si pMOSFET. The recovery characteristics for all cases can be well described by our simulations and the four-state NMP model. Furthermore, a considerably stronger stress bias dependence of the threshold voltage shift is visible for the devices with a SiGe quantum well which is also explained by our simulations [MWJ2].

changed during a complete eMSM sequence. For each measurement cycle a fresh device has been used.

As can be seen from the recovery traces shown in Figure 9.13 (symbols), the sensitivities of the DUTs to NBTI stress for all three different technologies follow the same trend as observed for the nanoscale devices, see Figure 9.7 (right). Again, the devices with $t_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$ show the smallest threshold voltage shift whereas the devices with $t_{\mathrm{SiCap}} = 2\,\mathrm{nm}$ as well as the reference devices degrade much more.

To reproduce the recovery behavior of the large-area devices the four-state NMP model is used together with a large defect distribution. The four-state NMP model nicely explains the ΔV_{th} recovery recorded at different stress times and biases, visible in Figure 9.7 (right) for the devices with $t_{\mathrm{SiCap}} = 2\,\mathrm{nm}$ and the reference transistor. Quite remarkably, the recovery of all three pMOSFETs is captured using the *same set of defect parameters* for the four-state NMP model. From the good fit we conclude that the trap parameters are a property of the gate stack rather that a property of the different channel layout. As a consequence, the device lifetime is solely determined by the band offsets in the channel/Si cap layer.

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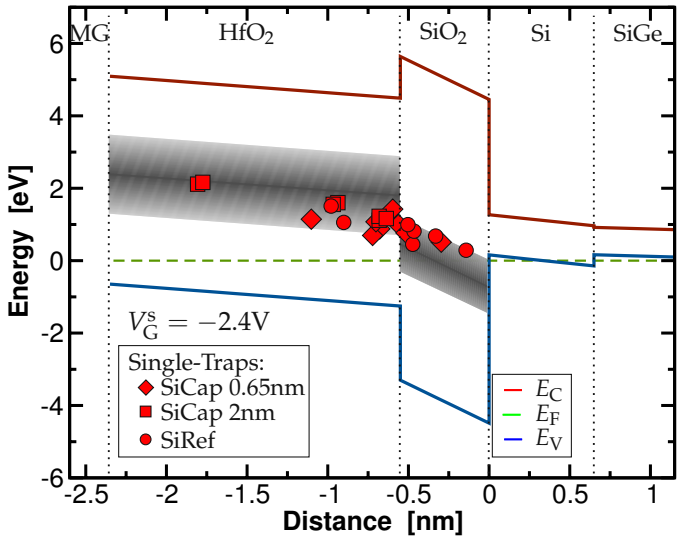

Figure 9.14: The band-diagram under stress bias conditions shows the defect bands used to explain the recovery of the large-area devices. Defects identified in the nanoscale devices are marked with larger symbols *diamond* for $t_{SiCap} = 0.65\,nm$, *square* for $t_{SiCap} = 2\,nm$, and *circle* for reference pMOSFET. The single defects are located in the HK and the IL for all three studied device variants [MWJ2].

9.4. Nanoscale versus Large-Area Devices

Based on the recent experimental studies using transistors with SiON or SiO_2 gate dielectrics, BTI in large-area and nanoscale devices has been attributed to defects with similar atomic configuration. Thus once the trapping kinetics of single defects is known, BTI in nanoscale and large-area and devices can be reproduced. In our particular case, 23 single defects have been identified in the three SiGe device variants. Afterwards, the four-state NMP model is used to explain the extracted charge capture and emission times of each of the 23 single defects. From these simulations the energetical and spatial defect position of the 23 single defects are obtained and shown in the band-diagram in Figure 9.14. In the band-diagram the single defects necessarily have a trap level above the Si Fermi level when stress bias is applied and a trap level below the the Si Fermi level when recovery bias is applied. Otherwise the defects would not contribute to NBTI at the studied bias conditions. As can be seen, the single defects are found to be located in both the HK and the IL for all three studied device variants. As the single defects of all three technologies show a similar stress bias dependence of their capture time the distribution of the trap depth is found to be similar for all three device variants.

In addition to the single defect simulations, the defect bands used to describe the continuous recovery behavior of the large-area devices, see Figure 9.13, is also shown in the band-diagram, see Figure 9.14. A good agreement is achieved between the defect band and the defect positions of the single defects estimated by the four-state NMP model.

To study the distribution of the capture and emission times (CET), the CET maps of large-area devices can be calculated directly from the measurement data using ((5.12)) and compared to those obtained from simulations, see Figure 9.15. As can be seen, the simulations reproduce the characteristics of the measurement data very well. According to (5.12), a narrow measurement window compared to simulations is achieved for the calculated CET maps due to experimental limitations.

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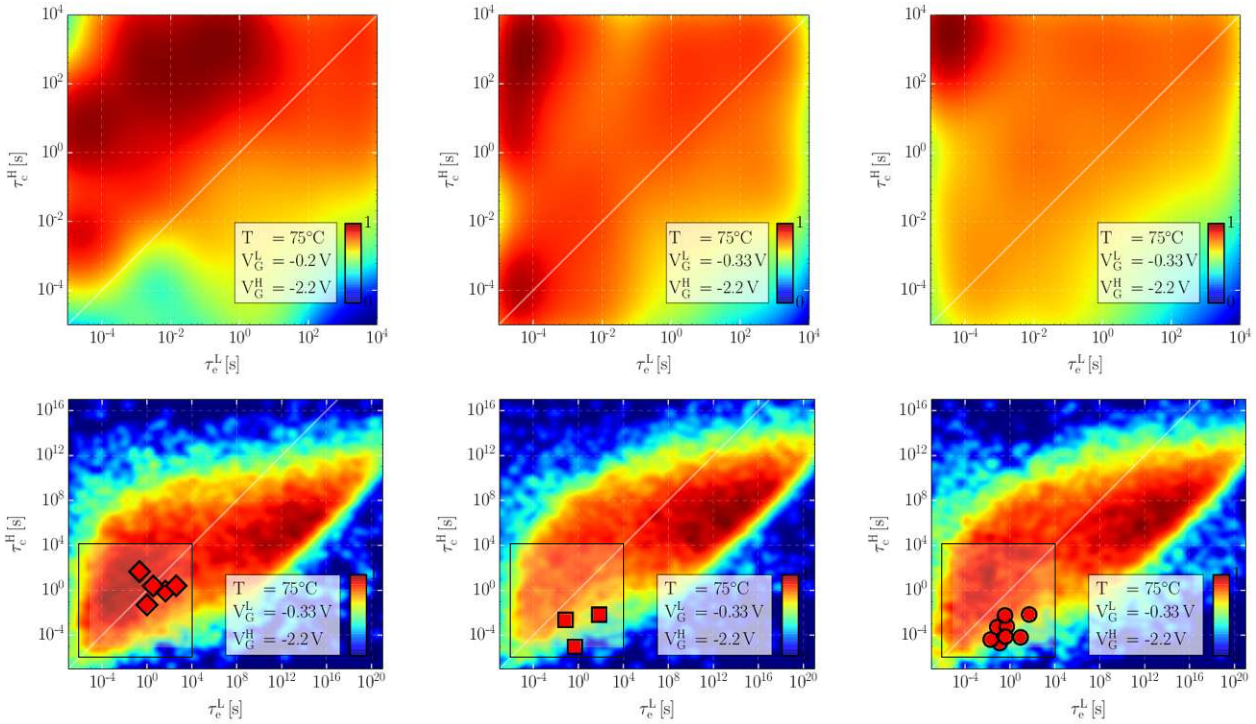

Figure 9.15.: The CET maps calculated directly from the measured recovery traces (**top row**) and the CET maps obtained from our simulations (**bottom row**) are compared for the three different structures (**left** for $t_{\mathrm{SiCap}} = 0.65\,\mathrm{nm}$, **middle** for $t_{\mathrm{SiCap}} = 2\,\mathrm{nm}$, and **right**) the reference Si pMOSFET. For the simulated CET maps, the measurement window (the axis ranges of the measured CET maps), is highlighted. As expected, the characteristics of the measured CET maps is well reproduced by our simulations. Additionally, the single defects from the nanoscale devices are shown (symbols) [MWJ2].

Furthermore, the CET datapoints from the analyzed single defects found in the nanoscale devices are marked in the CET maps together with the measurement window used for our TDDS experiments on nanoscale devices. As can be seen, the extracted single defects lie well inside the CET distribution.

Based on the previous simulations, the effective activation energies for charge capture $E_{\mathrm{A}}^{\mathrm{c}}$ and emission $E_{\mathrm{A}}^{\mathrm{e}}$ are calculated, see Figure 9.10. The continuous distribution shows the activation energies of the defect band used to explain the recovery of large-area SiGe devices. In addition, the activation energies from the single defect investigations are marked by symbols. As can be seen, both the distribution and the single data points are fully consistent. This confirms that a representative ensemble of single defects has been analyzed in this work.

Finally, the lifetime projections based on the experimental data shows that the threshold voltage shift saturates towards larger stress times, which thus deviates from the typically used power law. As such, a power law approximation results in significantly underestimated device lifetimes [MWJ1]. The device lifetimes extrapolated by using the calibrated model are shown in Figure 9.17. As can be seen, the SiGe devices with the thinnest Si cap provide a superior lifetime, easily outperforming the Si reference device.

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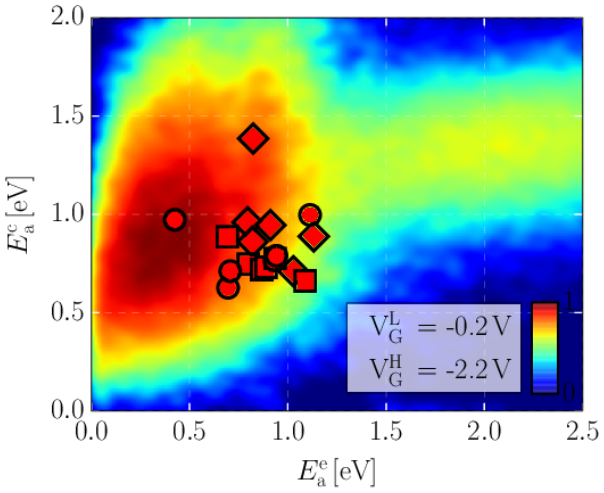

Figure 9.16: The simulated thermal activation energy distribution calculated from the defects of the device with $t_{SiCap} = 0.65\,nm$. In addition, the symbols show the activation energies of the single defects from the nanoscale transistors (*diamond* for $t_{SiCap} = 0.65\,nm$, *square* for $t_{SiCap} = 2\,nm$, and *circle* for reference pMOSFET). As can be seen, the single defects are spread over the same energy range as the simulated defects well, given the limits of the experiment [MWJ2].

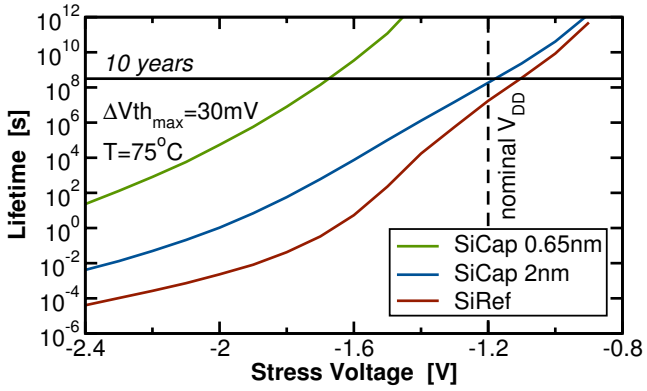

Figure 9.17: The lifetime estimation based on the unified model is shown against the applied gate bias. Quite remarkably, at the nominal operating voltage of $V_{DD} = -1.2\,V$ a lifetime of more than 10 years is easily achieved for the SiGe devices. In particular, the devices with a thin Si cap layer have an about four orders of magnitude higher lifetime although they show the lowest threshold voltage and thus have the highest overdrive voltage [MWJ2].

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10

Permanent Component of Negative Bias Temperature Instabilities

As discussed in the previous parts of this thesis, BTI is often considered to be the sum of a recoverable and a permanent threshold voltage shift. To understand both partial contributions to this puzzling phenomenon, tremendous efforts have been put towards an explanation of the observed threshold voltage shift. In contrast to the recoverable component, the study of the permanent threshold voltage shift is even more involved s it is mostly overshadowed by the former. According to the prevalent opinion, the permanent threshold voltage shift is due to single defects with large time constants, commonly referred to as interface states [143, 189, 149, 148, 190, 160, 191]. In the following a measurement sequence deliberately designed to study the recoverable and permanent component simultaneously is introduced. By performing ultra-long time experiments over several month, the evolution of the permanent threshold voltage shift is recorded and analyzed. To explain the newly collected data the hydrogen release model, see Section 4.4.2, is used.

10.1. Experimental Characterization of the Permanent Component

To monitor threshold voltage shift due to NBTI in pMOSFETs, simple stress/measure sequences are commonly used. We extended this procedure by a set of $I_{DS}(V_{GS})$ sweeps, recorded prior and after the stress/measure cycle is applied, see Figure 10.1. As can be seen, the ΔV_{th} accumulated during stress is not completely reversed after recovery. Obviously, a significant number of defects with very large time constants is present which determine the permanent component of ΔV_{th}. To access the remaining ΔV_{th} typically ten $I_{DS}(V_{GS})$ sweeps are measured after recovery thereby removing a significant amount of the trapped charge. Next, the permanent ΔV_{th} can be extracted at different gate biases using the $I_{DS}(V_{GS})$ sweeps, see Figure 10.2. We define the permanent

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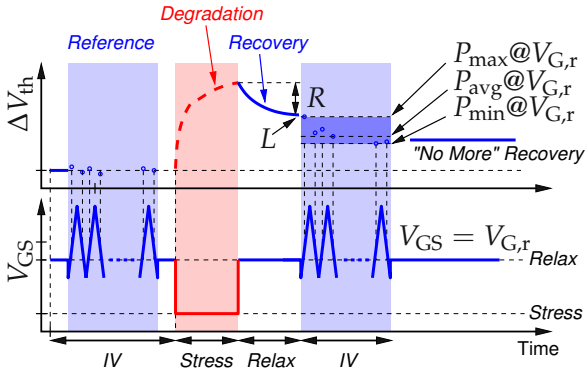

Figure 10.1: The measurement sequence used to determine the permanent component of NBTI is shown. (**top**) During stress the defects get charged, resulting in a threshold voltage shift ΔV_{th}. At the end of the recovery a significant ΔV_{th} remains which can be assessed by our modified measurement sequence. Using subsequent $I_{DS}(V_{GS})$ sweeps, a significant amount of the charge trapped during stress is removed and thus a basically flat recovery is observed at the end of the proposed measurement sequence. (**bottom**) As can be seen, prior and after the stress/measure cycle ten additional $I_{DS}(V_{GS})$ sweeps are performed [MWC7].

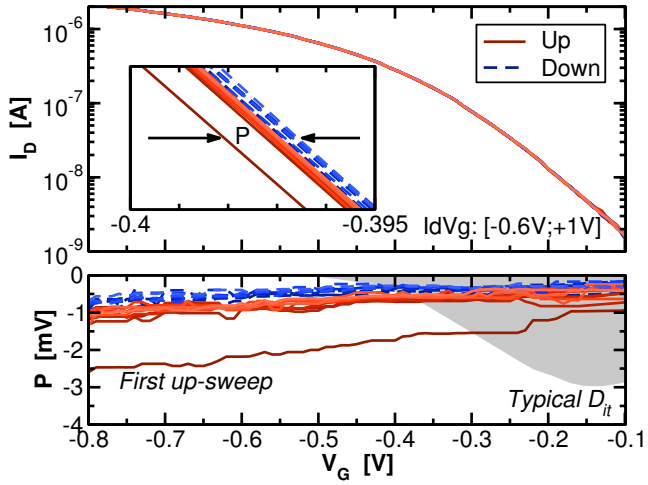

Figure 10.2: (**top**) The $I_{DS}(V_{GS})$ sweeps are used to extract the permanent contribution P to the total ΔV_{th}. (**bottom**) The voltage range of the $I_{DS}(V_{GS})$ sweeps allows to evaluate P at different gate biases. As can be seen, during the first up-sweep P is significantly larger, a consequence of the large number of trapped charges available immediately after the recovery cycle. In the subsequent sweeps only a weak change of P is visible. In addition, the location of the interface states D_{it} is shown [141]. At the corresponding gate biases a strong impact of interface states would be expected. These interface states are typically aligned 0.25 eV above the valence band, but no particular shift is observed in this region [MWC7].

component as the difference in the gate voltage between the down-sweep $V_G^{\downarrow}$ and corresponding up-sweep $V_G^{\uparrow}$ of the measured $I_{DS}(V_{GS})$ sweeps

$$P(V_G^{\downarrow}) = V_G^{\downarrow} - V_G^{\uparrow}(@I_{DS}(V_G^{\downarrow})), \tag{10.1}$$

extracted at a certain gate bias by considering the same drain-source current. Remarkably, P extracted from the first $I_{DS}(V_{GS})$ sweep performed from inversion to accumulation is strongly reduced towards decreasing absolute gate bias. This is a consequence of a larger number of traps remaining charged at the end of the recovery phase. In contrast, the analysis of the subsequent $I_{DS}(V_{GS})$ sweeps show a nearly flat P dependence on V_{GS}. As the interface states are typically supposed to be the main culprit for P, a peak arranged slightly above the V_{th} of the pMOSFET is expected. Figure 10.2 b shows the area where contributions of interface states are expected, cal-

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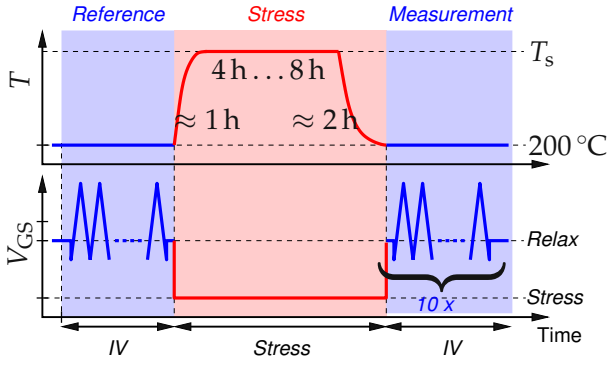

Figure 10.3: The measurement sequence used to monitor P over several month employs the temperature acceleration of charge trapping. At a reference temperature of 200 °C 20 $I_{DS}(V_{GS})$ sweeps are performed before the device is stress at higher temperature. Again, after cooling back to the reference temperature, 20 $I_{DS}(V_{GS})$ sweeps are recorded. Note that the stress bias is applied during heating and cooling phases. To obtain an accurate description by simulations these phases have to be considered [MWC6].

culated considering D_{it} at 0.25 eV above the valence band [141]. However, no contribution is this region is measured. Finally,

$$P_{min} = \min(P) \tag{10.2}$$

is taken as a measure for the permanent component remaining after our proposed measurement sequence.

In order to elucidate the evolution of P, the TMI together with a computer controlled furnace is used. The latter is necessary to achieve defined device temperatures and controlled temperature gradients when the temperature is changed. Using our sophisticated setup, P is studied over several month on a single transistor mounted into a conventional ceramic package. As the time constants of the defects responsible for P are very large, temperature accelerated experiments are performed, see Figure 10.3. To minimize the measurement noise, the permanent component of ΔV_{th} is again extracted using equation (10.2).

10.2. Results of Voltage Sweep Technique

Next, the impact of stress/recovery time and gate bias range of the $I_{DS}(V_{GS})$ sweeps on the permanent ΔV_{th} is studied using large-area transistors. Afterwards, the proposed method is applied to nanoscale pMOSFETs.

10.2.1. Large-Area Transistors

As mentioned before, whether a defect contributes to P or not depends on whether its transition times are "small" or "large". Considering a pMOSFET used in complex circuits with cycled on and off times, the question arises how the stress and recovery times impact P. Figure 10.4 shows the behavior of P extracted from our measurements performed with different duty cycles of t_s/t_r on a large-area SiON pMOSFET ($W = L = 10\,\mu m$). As can be seen, the measured P appears to be independent of the duty cycle of the selected stress and recovery times. This trend would not be visible if only recovery traces are used to study P, as the full threshold voltage shift strongly depends on the stress and recovery time. In contrast, a notable impact on P is observed at different gate voltage ranges used for the $I_{DS}(V_{GS})$ measurement, see Figure 10.5. The more the gate bias

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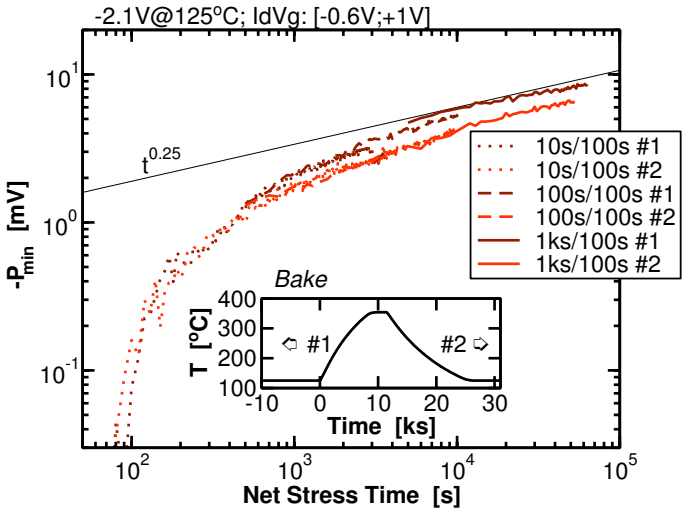

Figure 10.4: P is evaluated for different stress/recovery times on a large-area pMOSFET. As shown, P appears independent of t_s/t_r. After experiment #1 the device is baked at 350 °C. Afterwards, i.e. experiment #2, the same stress/recovery cycles have been applied. Although a slightly smaller P is observed the behavior is found to be consistent. Additionally, using a simple power law would lead to overestimated P at stress times < 10 ks and thus does not provide a reliable description of P [MWC7].

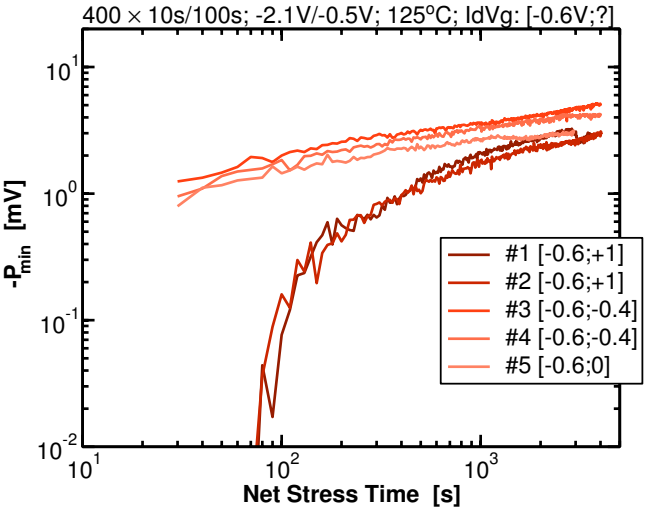

Figure 10.5: A significant impact on P is observed for different gate voltage ranges used for the $I_{DS}(V_{GS})$ sweeps. For a narrower voltage range a larger remaining P is observed. The larger V_{GS} gets (depletion/accumulation) the smaller P becomes [MWC7].

is increased, that means. the more the pMOSFET operates in depletion and accumulation, the smaller P gets. This is a consequence of the large amount of charge which is removed during accumulation.

10.2.2. Nanoscale Transistors

In agreement to TDDS investigations using nanoscale transistors, discrete charge capture and emission events are clearly visible in the $I_{DS}(V_{GS})$ sweeps. These discrete steps allow a clear identification of single defects, see Figure 10.6. Among the studied defects various types where found consistent with *fixed oxide traps* and *switching traps*. Due to our experimental limit the lowest accessible trap level was approximately 230 mV below the Fermi-level. However, interface states are located around 250 mV. Thus no interface state could not be clearly detected. To overcome this limitation, the current measurement resolution of the TMI is enhanced for further investigations.

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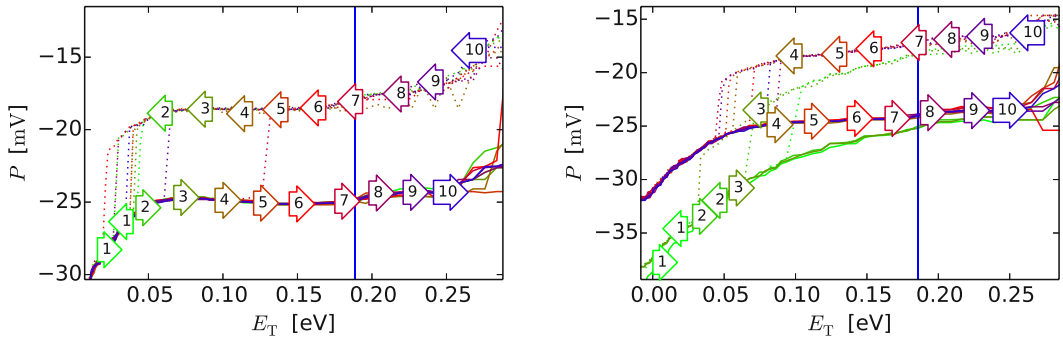

Figure 10.6.: The $I_{DS}(V_{GS})$ sweeps show discrete emission events produced from single defects. The number inside the arrows give the index and the arrows the direction of the sweep. (**left**) A very slow switching trap is visible which has been created during stress. (**right**) In general several traps can be clearly seen during the sweeps [MWC7].

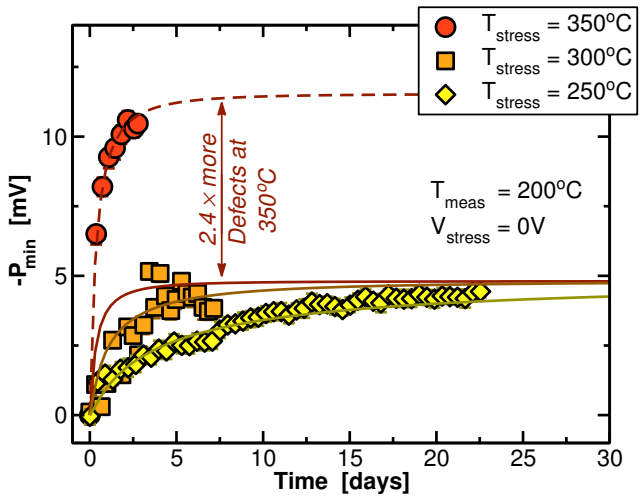

Figure 10.7: Even at zero volt applied at all terminals the permanent ΔV_{th} of the pMOSFET drifts slowly. At higher temperatures the accumulation of P is accelerated. The lines are calculated based on normally distributed activation energies [192, MWC6].

10.3. Permanent Component and the Hydrogen Release Model

So far the recoverable component of BTI has been successfully explained using the four-state NMP model. For simplicity, the DW model had been used to describe P. Although the latter explains the limited amount of experimental data available at that time, it does not rely on a correct physical mechanism. In order to provide a accurate description of the permanent threshold voltage shift the HR model has been introduced. The HR model relies on chemical reactions between H atoms with defects and hydrogen transport through the oxide. These mechanisms are supported by DFT calculations.

At the beginning P is studied on a large-area pMOSFET subjected to zero volt at all four terminals of the transistor, $V_D = V_{GS} = V_S = V_B = 0\,V$. Subsequently, $I_{DS}(V_{GS})$ sweeps are recorded and P extracted. Quite remarkably, a drift of P was found over several days, see Figure 10.7. At higher temperatures P gets more pronounced, a consequence of newly created defects. Note,

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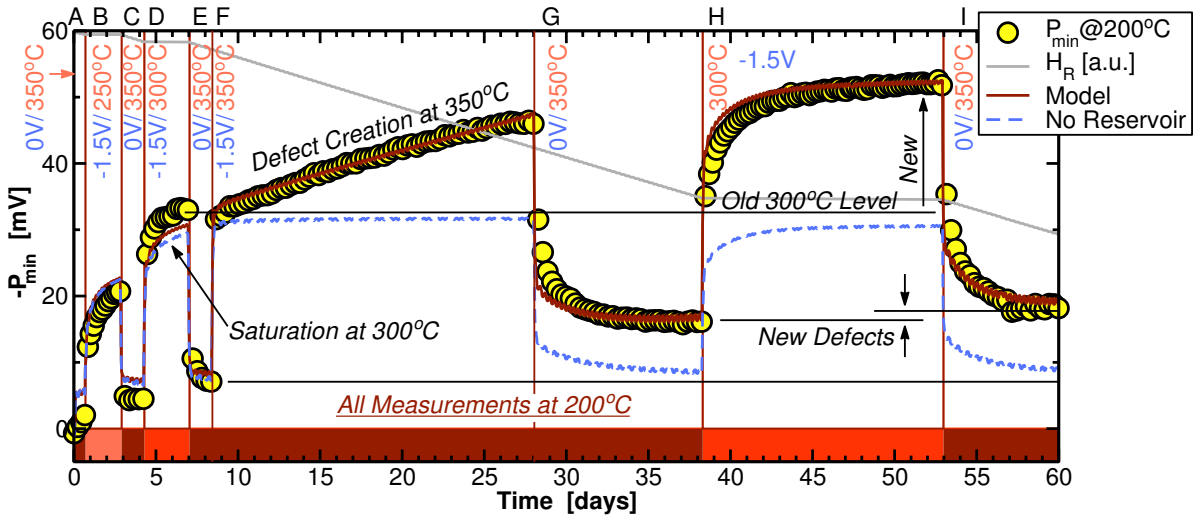

Figure 10.8.: During the long term experiment the stress voltage and the temperature is varied. To measure the $I_{DS}(V_{GS})$ sweeps and analyze P, the temperature was switched back to $T = 200\,°C$. During stress phases with $V_{G,s} = -1.5\,V$ (B,D, and F) a lot of new defects are created and thus P increases. In contrast, P only changes slightly at cycles A,C, and E where $V_{G,s} = 0\,V$. During phases G and I a considerable reduction of P is visible. At the end of the cycles the latter shows a slightly higher P due to additional defects with very long time constants created in phase H. First, the HR model is evaluated considering a fixed total number of reactive H atoms (blue dashed). As can be seen, phase F, where a large number new defects are created, is not covered by this model. Next, the HR model considers an H_2 reservoir located at the gate side. With this extension the HR model explains the behavior of P in all phases well [MWC6].

during fabrication a forming gas anneal process step with a duration of typical $t \approx 30\,min$ at $T \approx 400\,s$ is performed. Compared to the time scale of defects determining P, several days up to months, see Figure 10.7, the annealing step is an order of magnitude smaller. Furthermore, earlier publications assumed that P simply to be baked "away" at higher T. This notion has to be carefully reconsidered, since also at zero bias a significant amount of P is accumulated, albeit on a very large time scale.

Figure 10.8 shows the characteristics of P extracted from our first long exploratory time experiment. A single large-area pMOSFET has been probed for sixty days. The stress bias was switched between $V_{G,s} = 0\,V$ and $V_{G,s} = -1.5\,V$ while the device temperature was changed to 250 °C, 300 °C and 350 °C. After each stress cycle the temperature is switched back to 200 °C where the $I_{DS}(V_{GS})$ sweeps are recorded. From each voltage sweep cycle a new P is obtained. Figure 10.8 clearly shows a large increase in P during the stress phases with $V_{G,s} = -1.5\,V$. In contrast, when $V_{G,s} = 0\,V$ is applied, P changes only slightly. The characteristics of P recorded over several month can be nicely explained by the HR model.

A second long-term experiment has been performed on a virgin pMOSFET with dimensions $W = L = 10\,\mu m$. This time the stress bias of $V_{G,s} = -1.5\,V$ is applied during $T = 300\,°C$ cycles. Again, P is extracted from 20 $I_{DS}(V_{GS})$ sweeps performed at $T = 200\,°C$. Figure 10.9 shows the characteristics of P recorded from measurements during 90 days. Quite remarkably, although the device is heavily stressed during phase D, the permanent component decreases. This degradation

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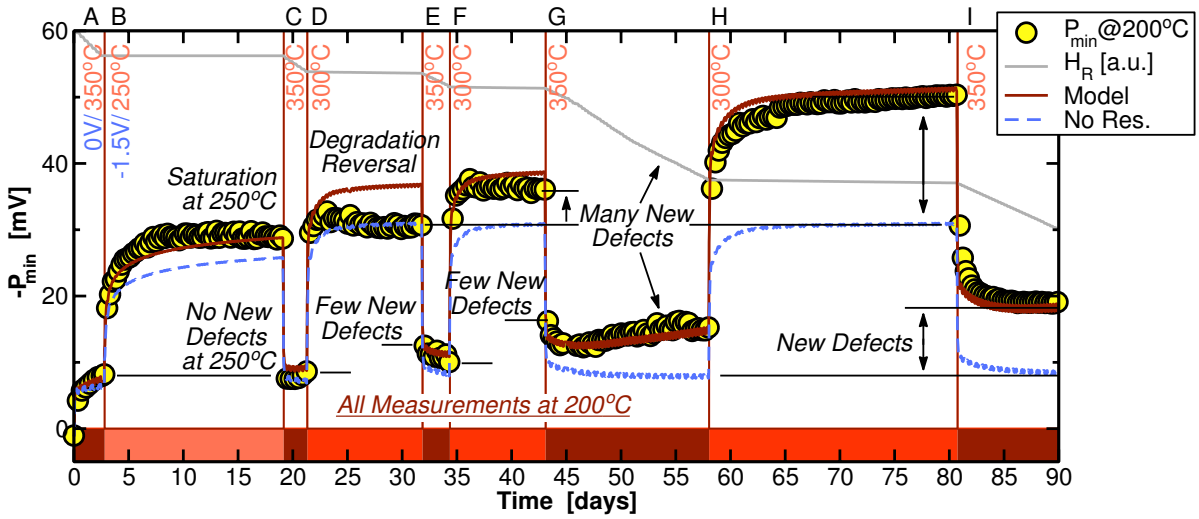

Figure 10.9.: The second long term experiment is performed with alternating $V_{G,s} = -1.5\,V / T = 300\,°C$ and $V_{G,s} = 0\,V / T = 350\,°C$ cycles. During phase B a lot of P is built up and saturates, however, during the subsequent phase C all these defects can get neutralized and P is settled at the same level as in phase A. Next, during phase E and F a small number of new defects are created. Furthermore, a reversal of the degradation has been observed during E and F. During the stress cycle H performed at $V_{G,s} = -1.5\,V / T = 300\,°C$ many new defects are created. As can be seen, the HR without H_2 reservoir can not reproduce the experimental data, however, by considering the proposed H_2 reservoir the HR model covers the behavior of P [MWC6].

reversal behavior is due to defects with an energy level close to the valence band edge which are annealed in phase B and can not be recharged again during phase D. Except for the degradation reversal, which requires closer inspection, the HR model again is able to explain the experimental data very well.

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11 MOSFET Characterization Array

To study the immunity of a particular device technology to BTI or HCD only a handful of devices from the same wafer is typically studied. With the measurement data and simulations from these investigations in hand the susceptibility of these technology to BTI and HCD is afterwards predicted. The devices used in these studies are thereby least often directly aligned next to each other on the wafer. As a consequence, the device variability which is unavoidably introduced during the device fabrication process can cause slight variations of the experimental data. Such variations are particularly important in nanoscale devices where different RDD distributions can lead to significant device-to-device variations, which are in case of RDD mainly notable by variations of the device threshold voltage. Nonetheless, in order to understand a particular technology, a detailed characterization of a large number of single defects measurable only at nanoscale devices is necessary. Therefore a statistically relevant number of devices have to be probed. In order to suppress the device-to-device variations for such a rigorous reliability study as good as possible transistor arrays can be employed. The big advantage of transistor arrays is that due to the densely packed transistors die-to-die and across wafer variations between seemingly identical devices can be excluded. For this purpose special test structures containing numerous transistors organized as an array, can be used. Figure 11.1 compares the number of devices for different structures using the same chip area. As can be seen, a large number of transistors can be accessed when transistors are

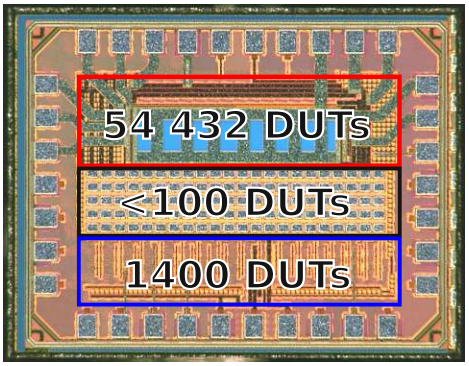

Figure 11.1: The micro-photography shows the number of transistors for (**top**) an array structure, (**middle**) single devices, and (**bottom**) a pipelined array [193] available at chip areas of the same dimensions, after [194].

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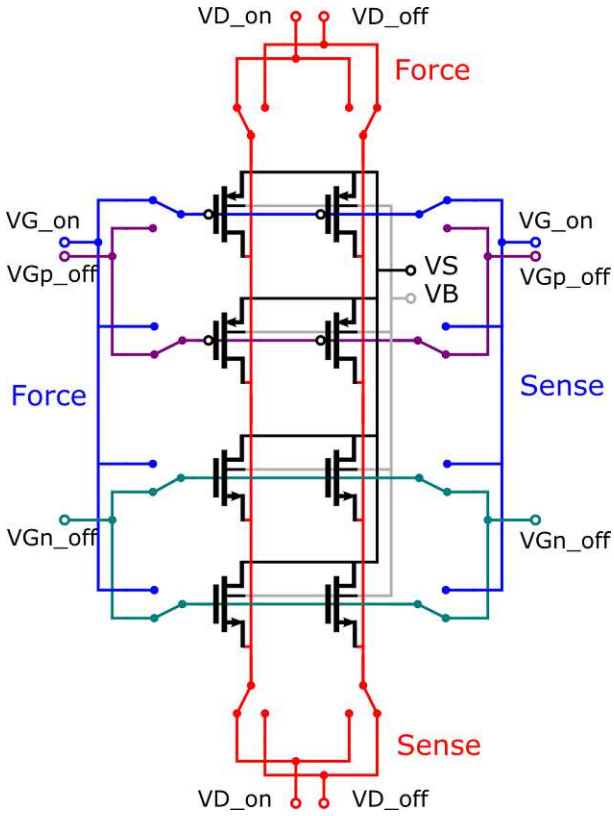

Figure 11.2: The schematic of the array structure shows nMOSFETs and pMOSFETs arranged in a large device matrix. All devices share a common source and common bulk connection whereas the drain and gate connections are controlled by electrical switches. To assure accurate voltage levels at the drain and gate contact, Kelvin pads (sense and force) are used, after [194].

organized as arrays [195].

In the following, the concept of the recently fabricated test structure is presented. The array, solely controlled by the TMI, is used to collect measurement data from numerous single defects. Finally, measurement results of the first investigations are presented.

11.1. Array Structure

To evaluate charge trapping in high-k metal gate (HKMG) MOSFETs, the test array was fabricated in a commercial 28 nm HKMG technology. All fabricated devices are connected to a common source and a common bulk contact, see Figure 11.2. In contrast, the electrical path between the external gate and drain pins and the corresponding terminals of the selected DUT are controlled by an additional integrated circuit. It is important to note that the drain and gate connections to the devices are separated into V_D and V_{GS} pins for the transistor which is currently measured and into the analog signals $V_{D,off}$, $V_{Gp,off}$, and $V_{Gn,off}$ connecting all the appropriate terminals of the corresponding transistors remaining in their "off" state. To study the impact of the gate area on the average step height of a charge capture and emission event, the number of active traps and the trapping kinetics of transistors with different geometries are available, summarized in Table 11.1. For instance, it has been reported that the average step height of a single trap and the number of

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W | L	30 nm	90 nm	3 × 30 nm	150 nm
100 nm	*	*	*	*
200 nm	*			
300 nm	*			

Table 11.1: The device geometries of the transistors available in the array structure. For each gate area 4536 single pMOSFETs and nMOSFETs are available. A long gate device is emulated by serially stacked transistors (3 × 30 nm structure), after [194].

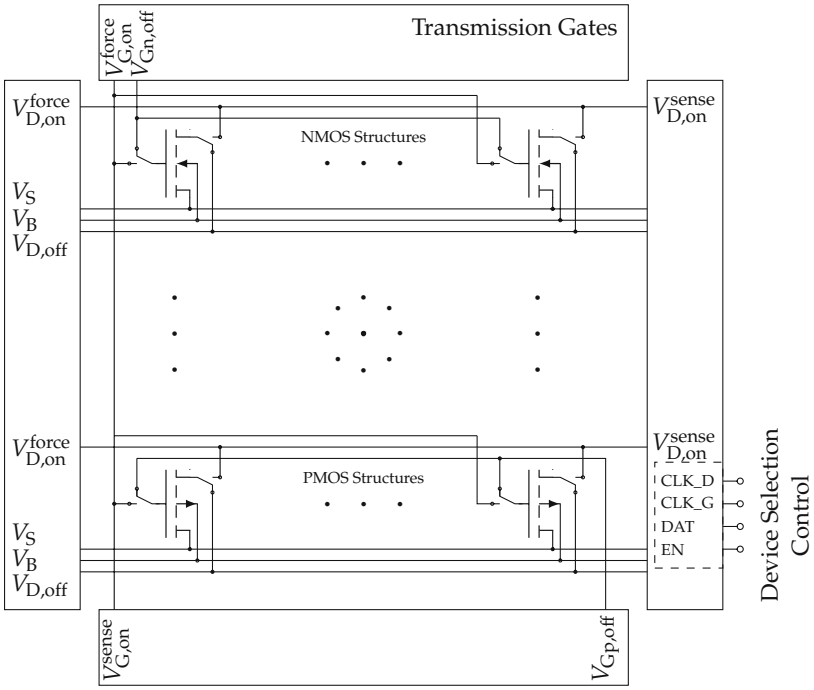

Figure 11.3: The test chip and the control components, digital control lines and transistors is shown. Both transistors types, namely pMOSFETs and nMOSFETs, with different geometries are available within this test structure. The drain and gate terminal of the selected DUT are separated from the corresponding terminals remaining transistors while common source and bulk connections are used. For device selection four control lines are available, after [194].

active traps scale with the device area as $\eta_s = \eta / A$ and $N_{T,s} = N_T \times A$, respectively. Using the designed test structure, these relations can be verified for the high-k technology.

The overall test structure, including circuitry electronic for device selection as well as all external lines, is shown in Figure 11.3. To allow Kelvin sensing, the gate and drain signals have transmission gates placed on each side of the structure. Additionally, the device selection uses shift registers controlled by three digital signals, “clock”, “data” and “enable”, for the gate and drain connection.

11.2. Experimental Setup

The experimental setup used to probe the devices is shown in Figure 11.4. Note that the reliability characterization array is entirely controlled by the TMI. Therefore the TMI is configured with two VUs, providing six analog voltages for V_D, V_{GS}, V_S and V_B share a common output, $V_{D,off}$, $V_{Gp,off}$, and $V_{Gn,off}$. The drain-source current is monitored using a modified version of the DCU. As the

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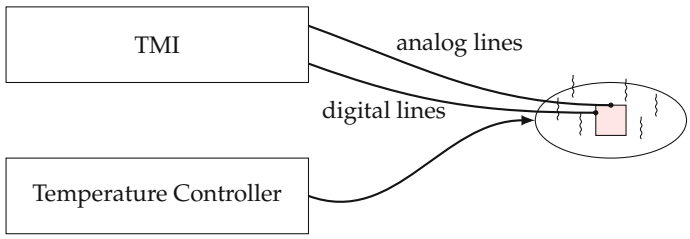

Figure 11.4: The transistor array is entirely controlled by the TMI with digital and analog signals electrically isolated. To allow temperature accelerated tests, the structure is mounted onto a heater together with a temperature sensor controlled by an external hardware. Both controllers and the measurements are monitored by the jobserver, see Section 6.3.

Table 11.2: The optimized values for the terminal voltages of the array structure are summarized for pMOSFETs and nMOSFETs.

	V_S	V_B	$V_{Gp,off}$	$V_{Gn,off}$
nMOSFET	0.15 V	0.15 V	0.3 V	0 V
pMOSFET	1.65 V	1.65 V	1.8 V	1.5 V

array requires a user selectable, non-zero source potential, the SCU has to be used for drain-source monitoring. In this context, it is worth to note that the TMI is able to provide the six analog voltages, and thus replaces three general purpose Keithley instruments. Thereby the total costs of the setup are reduced by a factor of around 15–20.

Another very important issue is the reduction of the noise level, especially for high-precision, low current, measurements. For this purpose, the analog and digital power supply, as well as all signal lines, are electrically isolated. Furthermore, the temperature is a crucial parameter in all experiments. For instance, the charge capture and emission transitions caused by single defects are very sensitive to the device temperature. Thus the test chip is mounted onto an external heater which allows to apply defined temperatures in the range of 25 °C up to 150 °C. In addition, defined temperature profiles can be applied similar to polyheater device structures [139].

To study the detrimental impact of NBTI and PBTI at the same technology, the test array contains n-channel and p-channel devices. The entire chip is designed to operate at $V_{DD} = 1.8\,V$. Although the break-down voltage of the gate stacks is much higher, a stress voltage exceeding V_{DD} will damage to the transmission gates. Hence, the voltages at the terminals must not exceed V_{DD}, however, negative voltages are necessary to characterize pMOSFETs. This requires different source potentials depending whether a n-channel or a p-channel MOSFET is measured. The corresponding voltages applied at the terminals and the resulting voltage ranges are summarized in Table 11.2 and Table 11.3. It is notable that using the deliberate set of biases from Table 11.2 a significant reduction of the leakage current is measured, see Figure 11.5. Furthermore, the effective gate bias range to study charge trapping is extended especially around the threshold voltage.

11.3. Results

The big advantage of such a test structure is the easy and reliable device selection. For instance, any contact issue as typically occur when a probe station is used can be avoided. In addition,

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	V_D	V_{GS}	$V_{Gp,off}$	$V_{Gn,off}$
nMOSFET	−0.15 V to 1.65 V	−0.15 V to 1.65 V	0.15 V	−0.15 V
pMOSFET	−1.65 V to 0.15 V	−1.65 V to 0.15 V	0.15 V	−0.15 V

Table 11.3: The available voltage ranges for the transistor array are calculated using the values from Table 11.2 considering a nominal $V_{DD} = 1.8\,V$.

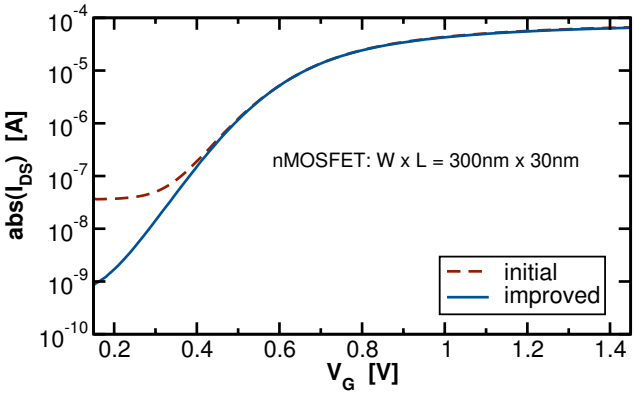

Figure 11.5: A typical $I_{DS}(V_{GS})$ characteristics recorded for a nMOSFET from the test array using the TMI. By using optimized values for the terminal voltages, see Table 11.2, a significantly reduced leakage current is measured.

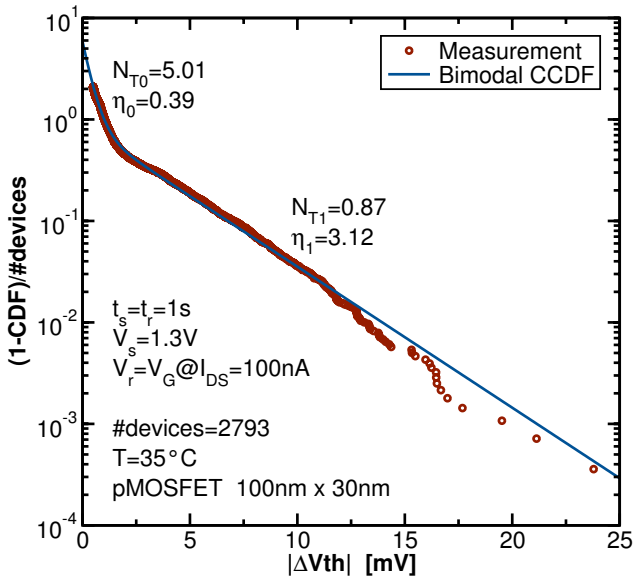

Figure 11.6: A bimodal CCDF of step heights is extracted from a large number of pMOSFETs. In accord with the CCDFs measured from our SiGe pMOSFETs, see Section 9.2.1, the first part of the CCDF stems from charge transfer interactions with the high-k layer, whereas the tail of the CCDF results from emission events between the SiO_2 and the conducting channel. This is supported by the larger active trap density N_{T0} compared to N_{T1}.

due to thermal expansions, the probes usually have to be realigned during and after temperature changes. Although the latter can be overcome by using devices mounted into ceramic packages, the number of directly accessible devices still remains very small. Both issues can be addressed using characterization arrays.

So far, the TDDS has been used to extract the CCDF of step heights from pMOSFET with $W \times L = 100\,nm \times 30\,nm$, see Figure 11.6. As can be seen, the step heights are bimodally distributed in agreement with previous investigations [169, MWJ1].

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It has to be noted that the experimental setup using the MOSFET array structure is still under development, thus only few results are available yet. However, major advances in understanding the charge trapping kinetics in high-k technology and device variability are expected from this considerable extended database.

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12 Conclusions and Outlook

In this last Chapter a short summary of the presented work is given followed by an outlook for further development of our experimental setups and future investigations to deepen the understanding of bias temperature instabilities.

12.1. Conclusions

To ensure the failure resistant operation of complex integrated CMOS circuits, the reliable functionality of MOSFETs has to be guaranteed. Due to the fast progress in the scaling of the transistor geometries, state-of-the art MOSFETs have reached the deca-nanometer regime. The time-to-failure of such nanoscale transistors is considerably affected by BTI which is due to charge trapping at single defects located in the dielectrics and at the semiconductor/dielectrics interface.

Over the last decades many efforts have been made to discovery the mechanism behind BTI. Most of them were carried out on large-area transistors. However, only the average response of a huge number of defects can be studied in such devices. In order to understand the physics behind the trapping mechanism responsible for the degradation of the device performance, the charge trapping kinetics of single defects has to be properly resolved. For this the time-dependent defect spectroscopy has been proposed. Using TDDS, discrete threshold voltage shifts caused by single defects can be studied individually in modern nanoscale transistors. As a consequence, the bias and temperature dependent capture and emission times of single defects can be studied in considerable detail. To explain the trapping kinetics the four-state non-radiative multiphonon model is used.

The bottleneck to perform TDDS studies has been the availability of a suitable measurement setup which supports all requirements of the TDDS. Commercial measurement setups are typically applied to study BTI in large-area transistors. Usually such setups suffer from limitations in handling, measurement speed or limited controlability and are mostly combinations of custom-made circuits with general purpose instruments. In order to guarantee unlimited control of the mea-

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surement sequences and to ensure signal integrity, the time-dependent defect spectroscopy measurement instrument has been developed. The TMI is designed to rigorously study single charge trapping in nanoscale transistors. This is possible because the TMI provides a very high current measurement resolution in the sub-picoampere regime and allows to sample the data with high frequencies up to 1 MHz. Particularly notable is the modular design of the TMI which allows a flexible adjustment of the configuration for its use in combination with computer-controlled furnaces, probestations or standalone applications. An additional benefit of the TMI is the long-term stability regarding uninterrupted measurements. So far single traces up to 1 Ms have been recorded and long-time experiments up to eight month have been performed without any interrupt.

As NBTI in pMOSFETs is commonly studied, the initial single charge trapping measurements using TDDS were performed on these devices. It was found that charge emission times can have bias-independent or bias-dependent characteristics, *fixed oxide traps* versus *switching traps*, whereas the charge capture time was observed to be strongly bias-dependent. Furthermore, charge trapping was found to be thermally activated. This raises the question whether single defects causing PBTI in nMOSFETs show a similar response of their transition times to different biases and temperatures or not. Similar to the pMOS case, the characterized single defects causing PBTI showed fixed oxide trap and switching trap behavior. Additionally, charge trapping was found to be thermally activated with activation energies in the same range as measured for pMOSFETs. As a consequence, the same trapping mechanism has to be responsible for NBTI in pMOSFETs and PBTI in nMOSFETs. This idea is supported by DFT calculations which demonstrated that single defects can also contribute to electron trapping. Finally, we demonstrated that the trapping kinetics of the analyzed electron traps can be well explained by the four-state NMP model.

Charge trapping was also studied in quantum-well high-k SiGe transistor. These devices were initially introduced to further enhance the performance of pMOSFETs as they exploit a higher channel mobility. However, a particular immunity to NBTI was observed for these devices. In order to explain this puzzling immunity, we studied single defects in nanoscale device variants with two different Si cap layer thicknesses and a reference device. The reduction of NBTI was found to be due to a beneficial re-alignment of the defect band in the oxide with respect to the conducting channel, which is a consequence of the Si cap layer. Using the four-state NMP model the charge trapping kinetics of 23 single defects and the continuous recovery behavior of the large-area counterparts could be explained. Finally, based on the measurement data and the performed simulations, the lifetime of the SiGe devices is demonstrated to easily outperform the lifetime of conventional Si transistors.

Finally, the permanent component of BTI was studied. To explain the permanent threshold voltage shift, the double-well model was used so far because of its simplicity, however, a more accurate description of the permanent contribution was needed particularly for these SiGe devices. Therefore, long time experiments over eight month were performed using the TMI. It was found that even at zero bias at all four terminals, a significant drift of the threshold voltage shift is observed. This shift gets more pronounced at higher temperatures and at higher biases. By using the newly developed hydrogen release model the permanent threshold voltage shifts observed in our experiments were described very well. This is achieved by creation of new defects at the channel site due to the reaction of precursors with hydrogen species. Thereby the required hydrogen is pro-

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vided as interstitial hydrogen which is released at the gate side and moves towards the interface. Close to the interface the interstitial hydrogen can become trapped and new defects are created. These newly created interface defects have very large time constants and therefore contribute to the permanent threshold voltage shift.

12.2. Outlook

During stress/measure experiments BTI was observed to recover already when the gate voltage changes from stress to recovery bias. During this switching cycle, which is approximately 200 ns in our setup, the threshold voltage shift produced by single defects can not be evaluated. Nonetheless, as charge trapping is very sensitive to the device temperature, cryogenic temperatures might be used to shift the charge trapping events which occur in the switching phase into our experimental window. This would allow to study the trapping kinetics of single defects with ultra-fast emission time constants. However, it has to be noted that charge capture is also strongly temperature dependent. At cryogenic temperatures, the charge capture time increases too, and as a consequence only a reduced number of single defects might become charged. To circumvent this limitation, a sophisticated setup which allows to stress at high temperatures and to recovery a low temperatures would be required.

By analyzing the measured recovery data the charge capture and emission events of single defects can be extracted and afterwards explained using the four-state NMP model. In our SiGe investigations the simulated charge capture and emission times were calculated considering the four-state NMP model for charge transitions between the metal gate and the single defect, and charge transitions between the conducting channel and the single defect. In order to substantiate the simulated transition rates for charge trapping between the single defect and the metal-gate, single-defect SILC and conventional charge trapping visible in the drain-source current has to be monitored. Therefore the TMI has to be extended to monitor the gate and drain-source currents with very high measurement resolutions simultaneously.

In order to provide the whole spectra of well-established semiconductor characterization techniques the TMI can be extended to perform C(V) measurements and charge pumping measurements. For both methods the hardware and software has to be adjusted which, due to the modular design, can be achieved with reasonable effort. Furthermore, an extension of the sampling unit using an FPGA would *(i)* improve the sampling frequency and *(ii)* increase the available data memory. Both features would allow the TMI to properly resolve RTN signals with very short capture and emission times over a very long time. Additionally, the *fast-VT* method could also be integrated into the TMI.

In summary, the TMI is a powerful measurement instrument which provides all necessary features for the successful characterization of single defects. Due to its modular design, which is separated into the voltage unit, data acquisition unit and device connector unit, the TMI can be individually adjusted to the experimental requirements. Furthermore, the TMI can be used in combination with computer-controlled furnaces and modern, partially semi-automatic, probestations. The external components are thereby controlled by a jobserver, which also organizes the measurement queues.

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In future investigations the large list of features already provided by the developed framework is planned to be further extended by commonly used characterization techniques like charge-pumping or C(V) measurements. Nonetheless, the TMI together with the developed software toolset can be already considered as a state-of-the art semiconductor characterization framework.

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List of Publications

Publications in Scientific Journals

[MWJ1] **M. Waltl**, A. Grill, G. Rzepa, W. Goes, J. Franco, B. Kaczer, J. Mitard, and T. Grasser. "Superior NBTI in high-k SiGe Transistors - Part I: Experimental". In: *IEEE Transactions on Electron Devices* (2016). (submitted).

[MWJ2] **M. Waltl**, G. Rzepa, A. Grill, W. Goes, J. Franco, B. Kaczer, J. Mitard, and T. Grasser. "Superior NBTI in high-k SiGe Transistors - Part II: Theory". In: *IEEE Transactions on Electron Devices* (2016). (submitted).

[MWJ3] Y. Illarionov, **M. Waltl**, G. Rzepa, J.-S. Kim, S. Kim, A. Dodabalapur, D. Akinwande, and T. Grasser. "Long-Term Stability and Reliability of Black Phosphorus Field-Effect Transistors". In: *ACS Nano* (2016). (submitted).

[MWJ4] R. Stradiotto, G. Pobegen, C. Ostermaier, **M. Waltl**, A. Grill, and T. Grasser. "Characterization of Interface Defects with Distributed Activation Energies in GaN-based MIS-HEMTs". In: *IEEE Transactions on Electron Devices* (2016). (submitted).

[MWJ5] Y. Y. Illarionov, G. Rzepa, **M. Waltl**, T. Knobloch, A. Grill, M. M. Furchi, T. Mueller, and T. Grasser. "The Role of Charge Trapping in MoS_2/SiO_2 and MoS_2/hBN Field-Effect Transistors". In: *2D Materials* (2016), pp. 035004-1–035004-10.

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[MWJ7] Y. Y. Illarionov, **M. Waltl**, A. D. Smith, S. Vaziri, M. Ostling, M. C. Lemme, and T. Grasser. "Bias-Temperature Instability on the Back Gate of Single-Layer Double-Gated Graphene Field-Effect Transistors". In: *Japanese Journal of Applied Physics* 55.4S (2016), 04EP03.

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[MWJ8] T. Grasser, K. Rott, H. Reisinger, **M. Waltl**, F. Schanovsky, and B. Kaczer. "NBTI in Nanoscale MOSFETs – The Ultimate Modeling Benchmark". In: *IEEE Transactions on Electron Devices* 61.11 (Nov. 2014), pp. 3586–3593.

Contributions in Conference Proceedings

[MWC1] G. Rzepa, **M. Waltl**, W. Goes, B. Kaczer, J. Franco, T. Chiarella, N. Horiguchi, and T. Grasser. "Complete Extraction of Defect Bands Responsible for Instabilities in n and pFinFET". In: *IEEE Symposium on VLSI Technology and Circuits*. 2016.

[MWC2] Y. Illarionov, R. Rzepa, **M. Waltl**, H. Pandey, M. Lemme, and T. Grasser. "A Systematic Study of Charge Trapping in Single-Layer Double-Gated GFETs". In: *Device Research Conference (DRC)*. 2016.

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[MWC21] T. Grasser, G. Rzepa, **M. Waltl**, W. Goes, K. Rott, G. Rott, H. Reisinger, J. Franco, and B. Kaczer. "Characterization and Modeling of Charge Trapping: From Single Defects to Devices". In: *Proceedings of the International Conference on IC Design Technology (ICIC)*. 2014, pp. 1–4.

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[MWC25] T. Grasser, K. Rott, H. Reisinger, P.-J. Wagner, W. Goes, F. Schanovsky, **M. Waltl**, M. Toledano-Luque, and B. "Advanced Characterization of Oxide Traps: The Dynamic Time–Dependent Defect Spectroscopy". In: *Proceedings of the International Reliability Physics Symposium (IRPS)*. 2013, pp. 2D.2.1–2D.2.7.

[MWC26] **M. Waltl**, P.-J. Wagner, H. Reisinger, K. Rott, and T. Grasser. "Advanced Data Analysis Algorithms for the Time–Dependent Defect Spectroscopy of NBTI". In: *Proceedings of the International Integrated Reliability Workshop (IIRW)*. 2012, pp. 74–79.

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