Master's Thesis

Ge-based Reconfigurable Transistors: A Platform Enabling Negative Differential Resistance

submitted in partial fulfillment
of the requirements of the degree of
Master of Science

at Technische Universität Wien
Institute of Solid State Electronics

under supervision of
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Vienna, July 2021

Abstract

With information and communication technology being ubiquitous in everyday life, the functional diversification of transistors constitutes an alternative approach to deliver enhanced circuit performance beyond the limits imposed by miniaturization. In this sense, scaling is reaching physical limits, where doping-free reconfigurable field-effect transistors (RFETs) allow to overcome this limitation by combining programmable n- and p-type operation in a single device. Nowadays, RFET research focuses on further functional diversification and adaptability, which are disruptive approaches for advancing electronics beyond the static capabilities of conventional complementary metal-oxide-semiconductor (CMOS) based architectures. In this work, these two issues are targeted by utilizing monocrystalline and monolithic Al-Ge-based nanowire (NW) and nanosheet (NS) heterostructures. The main advantage of the Al-Ge system is its reliable and well-defined Schottky junction, whereas other metal-Ge junctions tend to form germanides, exhibiting high variability and thus often leading to unreliable electrical characteristics. Hence, an experimental procedure to evaluate the total effective activation energy to inject electrons and holes into the Ge channel is established. Further, nanometer-scale Ge departs from its bulk counterpart and delivers unique electronic transport mechanisms that can be exploited at the device level. Thereto, a highly interesting transport mechanism is the transferred-electron effect, enabling negative differential resistance (NDR). In this respect, the NDR characteristic was thoroughly investigated and characterized on the proposed material system. Analysis of more than twenty NW devices lead to profound relations between NDR performance metrics and the channel geometry. Evaluating different gate-architectures, an Al-Ge-Al based RFET is accomplished as well as complemented with NDR-functionality, leading to a new type of device, the NDR-mode RFET, which comprises both mechanisms. In concerns of adaptability, a deterministic top-down fabrication scheme for RFETs was pending. Here, NSs fabricated from Germanium-on-Insulator (GeOI) substrates enable an opportunity to overcome this limitation, transferring the RFET-concept to this platform, and thus enabling the realization of deterministic top-down RFETs and to explore different gating regions.

The proposed device concepts may pave the way for future high-performance and low-operation-power circuits by enhancing the RFET and NDR mechanisms, even in a single type of device. The unique fusion of electron- and hole conduction together with NDR expressivity in a universal Ge transistor holds the promise of enabling energy efficient reconfigurable circuits with mulit-valued operability that given their inherent adaptability, represent prospective components for emerging artificial intelligence electronics.

Kurzfassung

Die Informations- und Kommunikationstechnologie ist im täglichen Leben allgegenwärtig. Um weitere Performance-Steigerungen zu gewährleisten, stellt die funktionale Diversifizierung von Transistoren einen Ansatz dar, um elektronische Geräte zu verbessern und zu erweitern. Da zudem die Skalierung an die physikalischen Grenzen stößt, bieten dopingfreie rekonfigurierbare Feldeffekttransistoren (RFETs) eine Lösung an, diese Limitierung durch die Kombination eines programmierbaren n- und p-Typ-Betriebs in einem einzigen Bauelement zu gewährleisten. Heutzutage konzentriert sich die RFET-Forschung auf die funktionale Diversifizierung und Anpassungsfähigkeit, die bedeutende Lösungsansätze für die Weiterentwicklung der CMOS-basierten Elektronik über die statischen Fähigkeiten der konventionellen Architekturen hinaus darstellen. In dieser Arbeit werden diese beiden Themen durch die Verwendung von monokristallinen und monolithischen Al-Ge-basierten Nanodraht- (NW) und Nanosheet- (NS) Heterostrukturen kombiniert. Der Hauptvorteil des Al-Ge-Systems ist sein zuverlässiger und gut definierter Schottky-Übergang, während alle anderen bekannten Metall-Ge-Übergänge dazu neigen, Germanide zu bilden, deren Kontakteigenschaften stark von Prozessparametern abhängen und daher eine Vielzahl unterschiedlicher Phasen aufweisen. Daher wurde in dieser Arbeit die effektive Aktivierungsenergie zur Injektion von Elektronen und Löchern in den Ge-Kanal von Al-Ge-Al basierten FETs ermittelt. Weiters unterscheiden sich Ge-Strukturen im Nanometerbereich stark von Ge-Bulk, und ermöglichen elektronische Transportmechanismen, die auf Bauelementebene genutzt werden können. Ein hochinteressanter Transportmechanismus ist dabei der Transfer-Elektronen-Effekt, der einen negativen differentiellen Widerstand (NDR) ermöglicht, welcher im Al-Ge System untersucht und charakterisiert wurde. Die Analyse von mehr als zwanzig NW-Bauelementen führte zu tiefgreifenden Beziehungen zwischen NDR-Leistungsmetriken und der Kanalgeometrie. Durch die Evaluierung verschiedener Gate-Architekturen wird sowohl ein Al-Ge-Al-basierter RFET realisiert, als auch mit NDR-Funktionalität ergänzt, was einen NDR-Mode RFET ermöglicht. Im Hinblick auf die Anpassungsfähigkeit stand ein deterministisches Top-Down-Fertigungsschema für RFETs noch aus. Hier bieten NSs, die auf Germanium-on-Insulator (GeOI)-Substraten hergestellt werden, die Möglichkeit, diese Limitierung zu überwinden, das RFET-Konzept auf diese Plattform zu übertragen und so die Realisierung von deterministischen Top-Down-RFETs und die Erforschung verschiedener Gating-Regionen zu ermöglichen.
Die hier präsentierten Bauelementekonzepte könnten den Weg für zukünftige hochleistungsfähige und stromsparende Schaltungen ebnen, da die einzigartige Verschmelzung von Elektronen- und Löcherleitung zusammen mit der NDR-Funktionalität in einem universellen Ge-Transistor endet. Dies könnte zu rekonfigurierbare Schaltungen auf Basis mehrwertiger Logik führen, welche aufgrund ihrer Anpassungsfähigkeit potenzielle Komponenten für kompakte und energieeffiziente Elektronik für Systeme mit künstlicher Intelligenz darstellen.

Acknowledgement

Completing the master's program "Microelectronics and Photonics" at TU Wien means a lot to me. Especially, after graduating at a University of Applied Sciences and the additional effort to pursue this degree would not have been possible without the enormous support and encouragement of many friends. During the last years I have gained a lot of experience in a broad context. In this respect, I also want to thank the TU Wien Space Team for providing such an inspiring and enthusiastic environment. Special thanks go to the following persons:

Walter M. Weber
Walter, who introduced me to RFET technology and always gave essential hints in respect to the manifold effects of NWs or GeOI NSs. The inspiring and motivating discussions of results and ideas are always a pleasure! Without you I would not have been able to extract such nice results. Thank you very much for the nice group-meetings and for taking time!

Masiar Sistani
Masiar, who supported me in basically all aspects. From clean-room fabrication to measurement techniques and also in personal concerns. Starting in my first year at TU Wien, Masiar introduced me to the fascinating world of Ge NWs and their impressive electrical and optical effects. Moreover, always involving me in new ideas and discussing them provided an awesome culture of conversation. For this and many, many more I want to thank you. I did not only find a perfect mentor but also a very good friend in you!

Kilian, Boris, David and Zlatan
Kilian, Boris, David and Zlatan, who did their bachelor's thesis during my time at the Institute of Solid State Electronics. Thank you for your inspiring questions and good discussions we had on Ge NWs, NDR and RFETs.

Madlen
Madlen, who unconditionally supports me all the time. Thank you so much for always standing by my side and your blessed words during stressful times. Without you I would not be where I am now. I love you!

Sonnwendgasse WG
The boys from the Sonnwendgasse WG and around. It was an awesome time living together, drinking beer, enjoying time with you and so much more fun activities. Thanks for making my time in Vienna so enjoyable!

Contents

Chapter 1

Introduction

With the technological realization of semiconductor devices – and in particular transistors – in the 1950s, new circuit concepts were introduced, which allowed the development of paradigms and devices, which significantly affect our daily life in many aspects.[1] In this context, Gordon E. Moore predicted that the number of transistors on an integrated circuit, and hence its processing power, doubles every 18 months.[2] This progress ensures high computation and performance metrics for modern telecommunication and computer applications and can be extended to artificial neural network concepts, to name a prominent one.[3] Although, the first transistor was realized with Ge,[4] the most successful contributor in this context is the Si metal-oxide-semiconductor field-effect transistor (MOSFET) due to its stable and high-quality native oxide SiO_2 serving as insulator. However, continuously shrinking feature sizes of Si MOSFETs leads to fundamental scaling limits, as increased leakage currents and relatively high supply voltages, which restrict enhancing the performance of modern devices.[5, 6] Nevertheless, it needs to be considered that Si-technology is optimized for complementary metal-oxide-semiconductor (CMOS) process integration and is still the material of choice for many applications due to its excellent processing capability.[7, 8] To overcome the scaling limitation and therefore enhance novel device concepts, it is mandatory to use new materials, processes and device architectures. Out of the wide range of alternatives, low-dimensional Ge structures such as nanowires (NWs) or nanosheets (NSs) exhibit unique electrical properties.[9–11] The high charge carrier mobility of Ge in comparison to Si is the most important property in this context. From a processing point of view Ge and SiGe nanostructures are CMOS compatible, which allows the integration into established Si-technology flows, specifically in p-type MOSFETS, and enhances the performance of high-end very-large-scale integration (VLSI) systems.[1, 12] This fact allows extensions of established concepts and therefore enables "More-than-Moore" paradigms. To access the promising properties of Ge, such as strong quantum confinement and high charge carrier mobility,[13, 14] it is necessary to use structures in the nanometer-scale regime. Moreover, high-quality and well-defined metal-

semiconductor contacts need to be established, as the injection of charge carriers highly depend on the interface and its incorporated energy barrier.[15] A possibility to enable such contacts is the use of metal-semiconductor heterostructures, which are fabricated by contacting the semiconducting material with metal contacts and consequently exchanging the semiconductor with metal by thermally induced diffusion processes.[16–18] In this context, intense research was carried out to form silicides and germanides, respectively. However, these silicides and germanides need to be carefully engineered due to the difficult processing mechanism and the formation of inter-metallic phases, e.g. Ni_xGe_x, Ni_xSi_x.[19] A highly interesting transport mechanism exhibited by heterostructures is the realization of negative differential resistance (NDR) devices by accessing the transferred-electron effect in a reconfigurable field-effect transistor (RFET) platform. RFETs are transistors which are capable of merging the electrical properties of unipolar n- and p-type field-effect transistors (FETs) into a single type of device and were firstly described in the 2000s.[20] Remarkably, RFETs do not require doping in contrast to conventional FETs. This is enabled by the heterostructure approach, embedded in a Schottky barrier FET (SBFET), and the possibility to locally tune the electrostatic potential of the semiconducting channel. Thereto, a device layout with independent gates is used to induce additional energy barriers in the channel, enabling to suppress the undesired charge carrier type and therefore favouring n- or p-type operation, respectively.[21–23] This approach enables the reconfiguration of circuits even during runtime and additionally ensures new concepts in the area of hardware security.[24, 25] Si- and Ge-based RFETs with Ni contacts were already shown.[19, 26] In the work "20 Years of Reconfigurable Field-Effect Transistors: From Concept to Future Applications" T. Mikolajick *et al.* illustrated the development progress of RFETs as shown Figure 1.1.

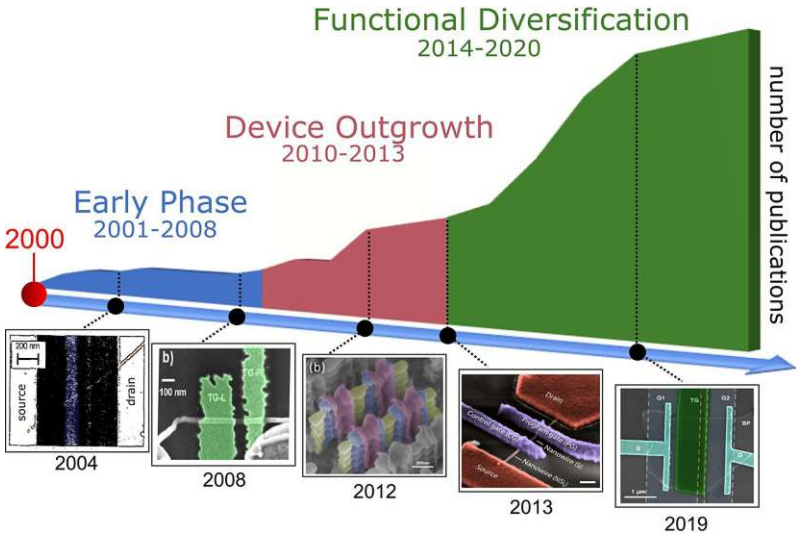

Figure 1.1: *T. Mikolajick et al. extracted the number of RFET-related publications over time. As illustrated, the era of functional diversification of RFETs started in 2014. Figure from [20].*

This illustration clearly depicts that the time for further functional diversification of

RFETs already started in 2014. To further push this trend, the realization of NDR devices is considered in this thesis. So far, most NDR devices were fabricated by group-III/V materials such as GaAs or GaN.[27, 28] In this respect, it needs to be distinguished between different mechanisms leading to NDR, which are mainly attributed to resonant tunneling and to the transferred-electron effect. Resonant tunneling diodes (RTDs) are primarily realized by group-III/V semiconductors or SiGe,[27, 29] whereas the transferred-electron effect, also known as Gunn-effect, is based on applying sufficiently high electric fields and therefore enabling scattering of hot electrons from a energetically favorable low mass conduction band valley to an energetically close heavy mass valley.[30, 31] Most notably, the transferred-electron effect is evident in group-IV semiconductors as Ge.[32, 33] NDR devices enable monostable-bistable transition logic elements (MOBILEs),[34] which were already shown to be operated as both, NAND and NOR gates.[35] Another important and promising application is the concept of multi-valued logic (MVL) gates.[36] However, the application of state-of-the-art NDR devices is limited. Firstly, the integration of III/V-based devices within CMOS technology is complicated and cost-intensive[37] and secondly, the observation of NDR is limited so far to low temperatures,[32, 33] the transient behavior of surface traps[38] or plasmon-induced hot electron injection.[39]

In this work, the realization of NDR devices embedded in a RFET platform is presented by utilizing monolithic Al-Ge-Al nanometer-scaled heterostructures embedded in (SB)FETs. Thereto, the individual physical phenomena are priorly investigated separately before finally combining the RFET- and NDR-mechanism in a single type of device. Moreover, the fabrication and operation of RFETs on GeOI substrates is proven. Therefore, various gating concepts – namely back- and top-gate schemes – are investigated. In this context the geometrical as well as thermal influence is analyzed in dependence of relevant performance metrics. The utilized approach allows to overcome major limitations of state-of-the-art devices and finally presents a new device, which merges RFET- and NDR-functionality in a single type of device.
Starting with Chapter 2, the theoretical aspects of the underlying physical phenomena, from a materials science as well as transport mechanism point of view, are discussed. Moreover, already realized device concepts are presented. Chapter 3 gives insights on the device integration of NWs and NSs and further evaluates the actual fabrication of the proposed (SB)FET devices. Additionally, the utilized measurement equipment and characterization methods are described. Chapter 4 presents and discusses the obtained results by utilizing back- and top-gate (SB)FET devices. An experimental approach to extract the total effective activation energy for the injection of electrons and holes is given. Moreover, the RFET- and NDR-concept are analyzed and characterized separately before combining both approaches into a single type of device. Finally, a deterministic top-down RFET approach based on Germanium-on-Insulator (GeOI) is presented. To conclude this chapter, a benchmark comparison of already published RFETs as well as RFETs realized in this work is given and discussed. Chapter 5 summarizes the obtained results and gives suggestions to further improve and enhance the presented device architectures.

Chapter 2

Theory

The following chapter addresses the theoretical aspects necessary for the work on Al-Ge-Al heterostructure nanodevices with special attention to the underlying physical phenomena, which allow the realization of RFETs and to enable the accessibility of NDR. Section 2.1 analyzes the utilized semiconducting material – Ge, followed by a general discussion about semiconductor nanostructures, particularly considering low-dimensional Ge NWs and NSs. Finally, in the end of the first section the implementation of NWs and NSs into nanometer-scaled heterostructures is discussed. Section 2.2 describes the transport mechanisms and therefore the physical background, which is employed to access the functionality of RFETs and the exhibition of NDR. Finally, Section 2.3 gives an overview of existing RFET concepts and NDR devices, and shows their limitations and enhancement possibilities.

2.1 Materials

In this section the main properties of Ge are discussed. Especially, its unique suitability and characteristic for nanoelectronic applications is presented. Moreover, important differences to other semiconductor materials are discussed to underline its advantage for the proposed devices – namely RFETs and NDR devices. Finally, characteristics of semiconducting nanostructures and in particular of Ge as well as the implementation of these structures into metal-semiconductor heterostructures are described in Section 2.1.2 and Section 2.1.3, respectively.

2.1.1 Germanium

Ge was firstly extracted by Clemens Winkler in 1886 by isolating Ge from *argyrodite*.[40] It is a metalloid and a group-IV chemical element and is therefore in the same group as Si. This indicates the same electron configuration in the valence shell and hence indicates

similar chemical properties, since they tend to gain, lose, or share valence electrons in the same way.[41] An important fact is that Ge – as well as Si – crystallizes in the diamond structure and further allows the formation of high-purity crystals.[42] In the context of this work, the most relevant property of Ge is its semiconducting characteristic, expressed by its electronic band structure. More precisely, bulk-Ge is an indirect semiconductor with a band gap of $E_g = 0.66\,\text{eV}$ at room temperature.[12] In comparison to Si with a band gap of $E_g = 1.11\,\text{eV}$, the Ge band gap is approximately half of the band gap of Si. Due to the smaller band gap of Ge, its use in MOSFETs exhibits relatively larger leakage currents in comparison to Si.[9] In contrast, a narrower band gap also allows to reduce the supply voltage and thus the threshold voltage V_{TH}.[9, 19] As shown in Figure 2.1, Ge has an indirect band gap spanning between the conduction band minima and the valence band minima at the Γ-point and is located at the L-point ($k = \langle 111 \rangle$). The direct band gap with $E_{\Gamma 1} = 0.80\,\text{eV}$ is at the Γ-point ($k = \langle 000 \rangle$) and is only $0.14\,\text{eV}$ larger than the indirect band gap energy E_g. Due to this low energy difference, band gap engineering, by e.g. induced strain, allows to access light-emitting properties and hence paves the way for light-emitting diodes or even lasers.[43, 44] Another important feature is the second conduction band – highlighted in red in Figure 2.1 with its valley at ΔE. Note that the difference between the indirect band gap E_g and ΔE is only $0.19\,\text{eV}$ and therefore enables the nonlinear transferred-electron effect, which is also known as the Gunn-effect.[30, 33] Applying sufficiently high electric fields, it allows to transfer electrons from the first conduction band to the second conduction band. Thus, leading to a change of the effective mass m^*. This effect leads to NDR, which is described in Section 2.2.2 in more depth.

Remarkably, bulk-Ge has the highest hole mobility μ_p of all single-element and common group-III/V semiconducting materials, as shown in Table 2.1. In this respect it needs to be considered, that nanometer-scaled structures, as well as strained materials exhibit different mobilities.[9, 22] However, to get an impression, the stated values are used for discussion. In comparison to Si, also the electron mobility μ_n of Ge is approximately 2.5 times larger. Therefore, Ge is widely known as a high-mobility semiconductor for CMOS applications. In state-of-the-art MOSFETs – and in particular for p-MOSFETs – SiGe has established itself to compensate the relatively low hole mobility μ_p of Si.[46] In general, the charge carrier mobility characterises the velocity of charge carriers – namely electrons and holes – which are accelerated by an electric field. This parameter is of high importance for high-frequency operations and moreover directly influences the current I.[47] In Section 2.2.2 further details regarding the charge carrier mobility are given, as this parameter highly determines the exhibition of NDR.

These facts make Ge a promising material for electronic applications and especially for FETs.[9, 49, 50] However, in the past, Ge has only been playing a minor role in transistor technology due to higher fabrication costs, and due to the fact that its native oxide GeO_x is unstable, soluble in water and exhibits very high interface trap densities up to 10^{15} cm^{-2}.[51] In contrast to Ge, Si naturally produces the high quality oxide SiO_2, which is a good insulator and stable at high temperatures and ambient conditions.[42] To overcome

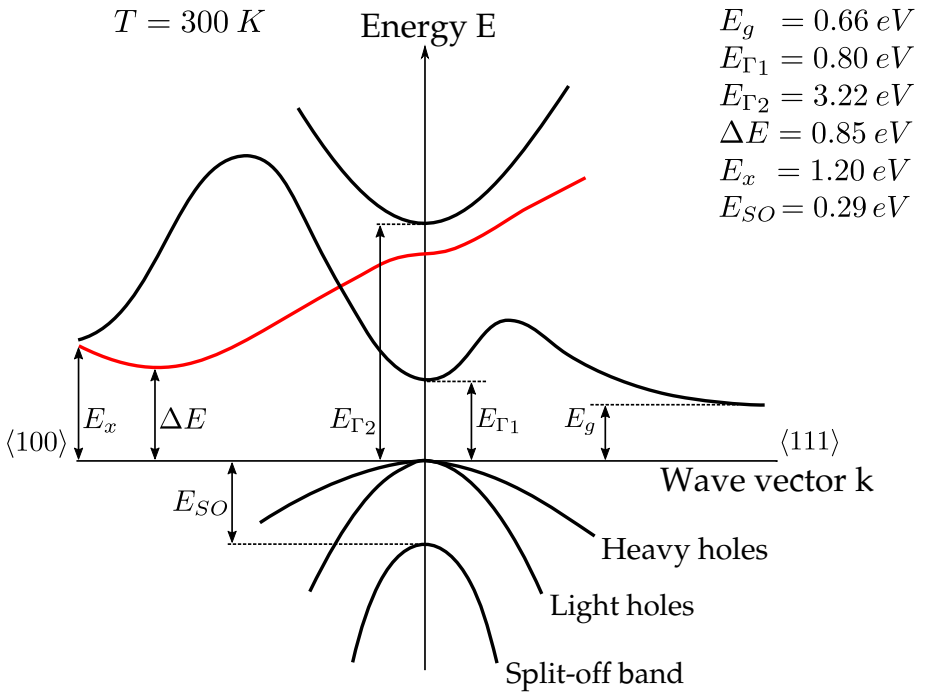

Figure 2.1: *Energy band structure of Ge at* 300 K. *The indirect band gap with* $E_g = 0.66$ eV *is located at* $k = \langle 111 \rangle$ *(L-point). The direct band gap* $E_\Gamma = 0.80$ eV *is at the* Γ*-point* ($k = 0$) *and is only* 0.14 eV *higher than the indirect band gap. Remarkably,* ΔE *(red curve) is only* 0.19 eV *higher than the band gap energy* E_g *and thus enables the transferred-electron effect. Figure adapted from [45].*

these disadvantages, interface engineering approaches are necessary.[49, 52]

2.1.2 Semiconductor Nanostructures

6Due to Gordon E. Moore's law and the capability to produce nanometer-scaled devices, the realization of such devices allows to exploit new features and properties of semiconductors, which are inaccessible in bulk materials and in conventional planar transistor technologies.[50, 53] Besides the fact, that the miniaturization of MOSFETs down to the nanometer-regime, reduces the inverter delay and power consumption,[54, 55] it also potentially allows to access quantum effects. These quantum effects significantly change the electrical, chemical and mechanical characteristics of the involved semiconducting material.[14, 56] In general, the electronic density of states (DOS), which describes the number of possible energy states per unit energy and volume, is affected by quantization. The profound effect which results from downscaling bulk structures to nanostructures is that the DOS changes from a continuous and parabolic energy spectra to an energy spectra with either constant terraces (2D) or discretized singularities (1D).[42] This leads to strong signals in many electronic and optical applications at the corresponding energies and in general to modified transport. Due to the reduced dimensions the movement of charge

	Material						
Mobility	**Ge**	**SiGe***	**Si**	**GaAs**	**InAs**	**InP**	**InSb**
$\mu_\mathbf{n}$ **(cm²/Vs)**	3900	1396-4315	1400	8500	40000	5400	77000
$\mu_\mathbf{p}$ **(cm²/Vs)**	1900	450-865	450	400	500	200	850

Table 2.1: *Electron and hole mobility μ_n and μ_p of most common semiconductors. Out of all shown semiconductors Ge has the highest hole mobility μ_p. Table adapted from [42].*
**...The charge carrier mobility of SiGe highly depends on the Si-to-Ge ratio in the SiGe alloy.[48]*

carriers is restricted to specific directions – in this context it is often spoken of 3D (bulk), 2D and 1D (e.g. NWs or NSs, quantum dots) materials. Structures with geometrical dimensions close to, or smaller than the exciton Bohr radius a_B^*, allow strong quantum confinement.[57] As Ge has an exciton Bohr radius of $a_B^* = 24.3\,\text{nm}$, the quantum confinement effects take place at larger structural sizes in comparison to Si with an exciton Bohr radius of $a_B^* = 4.9\,\text{nm}$.[58] As stated in Section 2.1.1, NWs or NSs can fulfill these requirements and will be from now on considered in the context of this work. Note that, many nanoelectronic concepts and devices were already shown on these structures.[10, 49, 53, 59] Another effect which is observed by quantum confinement is that the band gap respectively band structure changes correspondingly, and therefore enables band structure engineering approaches.[14, 60] This is of high importance as the band gap energy directly correlates with the on- to off-current ($I_{\text{ON}}/I_{\text{OFF}}$) ratio, which is a relevant figure-of-merit (FOM) for transistors.[19] A published work by B. Yu *et al.* shows that Ge NW FETs can have high on-off current ratios between 10^4 - 10^6. In that work an on-current in the nA- to μA-regime and an off-current in the pA-regime was observed. Furthermore, the switching energy is 3 to 6 orders of magnitude lower in comparison to a top-down conventional FET.[49] These facts, in combination with the properties of Ge, stated in Section 2.1.1, promote the utilization of NW and NS Ge-based platforms for nanoelectronic applications.[10, 11, 59] In Figure 2.2, a NW and NS structure, with their corresponding geometry definitions are shown.

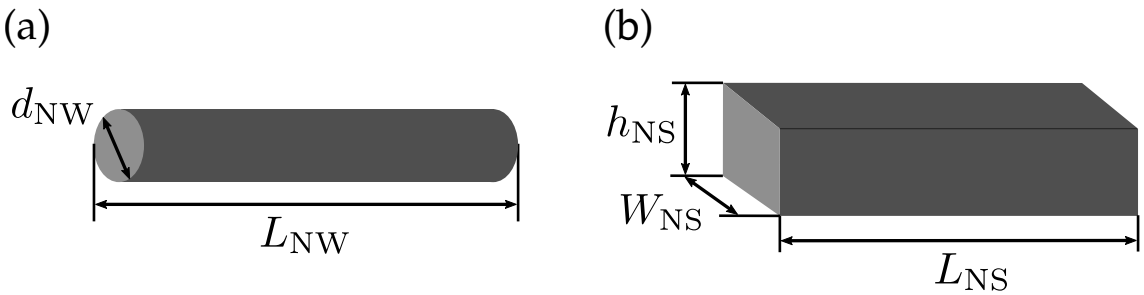

Figure 2.2: *Schematic representation of (a) a NW with diameter d_{NW} and length L_{NW} and (b) a NS with height h_{NS}, width W_{NS} and length L_{NS}.*

At first sight the only difference between NWs and NSs seem to be the geometrical shape. However, from a device integration as well as a materials science point of view the two

concepts do highly differ. Thus, leading to a different electrical characteristic. These issues are discussed in more depth in Section 3.1.1, where the differences from a fabrication perspective as well as from a materials science point of view are analyzed.

2.1.3 Metal-Semiconductor Heterostructures

For the realization of electronic devices it is of high importance to produce reliable contacts. The main purpose is to establish well-defined contacts, which lack ideally of interface traps, and reduce the contact resistance. Untreated metal-semiconductor contacts reveal large Schottky barriers, which need to be considered, as the barrier height highly influences the electrical characteristic of the heterostructure.[61] A more precise discussion regarding this topic is given in Section 2.2.1, where the physical foundation of Schottky barriers is described. However, the fabrication mechanisms are depicted in the following. To establish well-defined and improved metal-semiconductor junctions, thermal diffusion processes of metals into NWs or NSs are investigated. Many works were published in the past, which focus on the formation of silicides and germanides, including Cu[62] and Ni[63]. Note that mainly germanide phases suffer from inherent variability and unpredictability in phase formation, leading to different barrier heights and electrical characteristics.[64–66] Lately, Al showed remarkable results without the formation of inter-metallic phases, allowing Al to replace Ge and thus creating a metal-semiconductor heterostructure with an atomically sharp interface. This is enabled by the high diffusion coefficient of Al in Ge.[67] Moreover, utilizing Al, good electrical and mechanical properties are allocated.[68] In contrast to Ni in Si or Ge, the diffusion of Al in Ge does not show a high variation, indicating a reliable and sophisticated diffusion process. This allows to create high-quality metal-semiconductor heterostructures without any electron diffraction X-ray spectroscopy (EDX)-measurable Al contamination in the Ge segment.[11, 67] This is attributed to the asymmetric diffusion behavior, as the diffusion of Ge in Al as well as self-diffusion (Al in Al) is rather fast, while the diffusion of Al in Ge is extremely slow as depicted in Table 2.2.[18]

	Aluminium	**Aluminium**	**Germanium**	**Germanium**
in	Aluminium	Germanium	Aluminium	Germanium
D (cm^2/s)	6.0e-12	3.2e-11	1.3e-25	9.9e-25

Table 2.2: *Diffusion coefficients of the Al-Ge system at $T = 623\,K$. It can be obtained that the diffusion of Al in Al as well as Al in Ge are 13 and 14 orders of magnitude higher in comparison to Ge in Al and Ge in Ge.*

As shown in Figure 2.3, the exchange reaction respectively diffusion of Al in Ge is triggered by rapid thermal annealing (RTA). A similar fabrication scheme but restricted to an alloy formation is commonly used for the fabrication of NiSi-Si-NiSi or NiGe-Ge-NiGe heterostructures.[64] In this respect, the growth rate of Ni-silicide and Ni-germanide in Ge (∼10 nm/s at 450 °C)[69] is comparable to the Al exchange reaction in Ge (∼7.5 nm/s at 400 °C)[11]. Additionally, it needs to be considered that a large variability in NiGe alloy formation is evident.[69] Utilizing RTA, the temperature and annealing time can be

varied and thus allows to create various lengths L_{Ge} of the Ge segment, even down to a few nm.[67] Experimentally, it was shown that for the Al-Ge system a temperature of 300 °C leads to sufficient diffusion rates as well as flat and atomically sharp interfaces.[67] In addition, colored scanning electron microscopy (SEM) images, are shown in Figure 2.3d,e, revealing the final Al-Ge-Al heterostructure, based on a NW and NS, respectively.

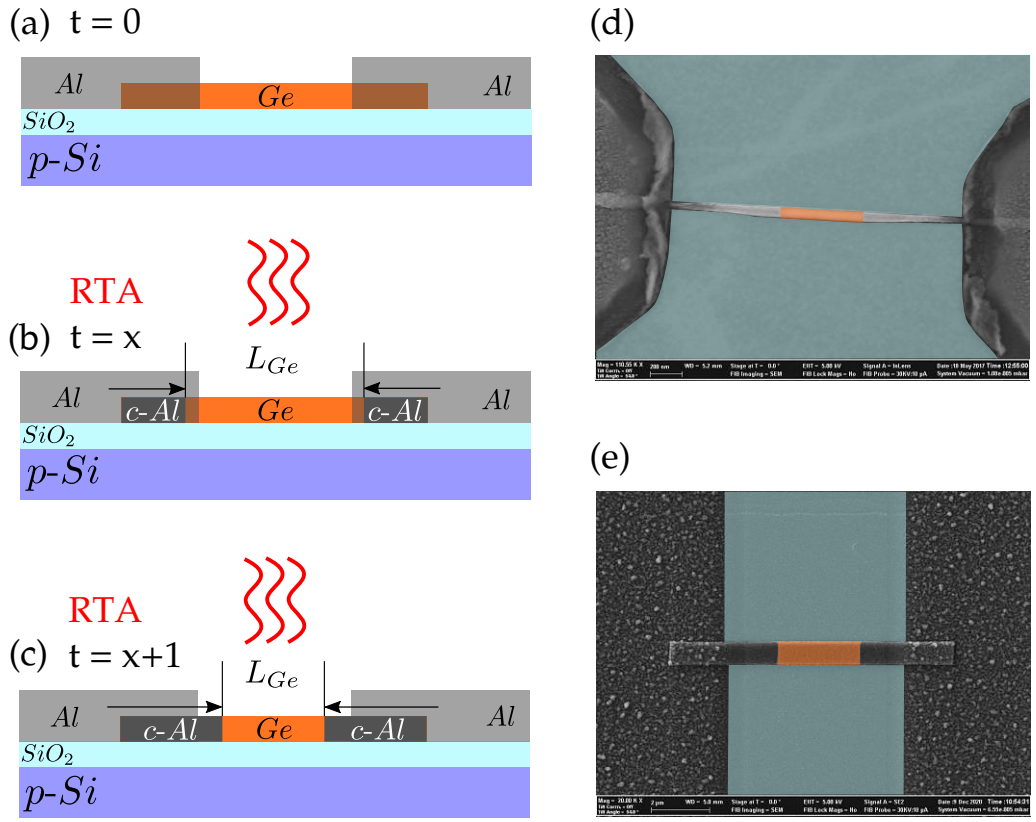

Figure 2.3: *Schematic representation of the Al-Ge exchange in a NW or NS, where (a) shows the contacted Ge segment with Al at t = 0 and (b,c) shows the annealing steps performed by RTA after time t = x and t = x+1. SEM images (d) and (e) show colored SEM images of an Al-Ge-Al NW and NS heterostructure, respectively.*

To prove the monolithic and abrupt Al-Ge junction, a (high-resolution) transmission electron microscopy ((HR)TEM) analysis was performed, as shown in Figure 2.4. Thus, proving the absence of any inter-metallic phase and Al in the Ge. Additionally, the presented image reveals the perfect crystalline order of Ge as well as of Al – indicated as c-Al.

Remarkably, during the exchange process the physically deposited Al orders itself and changes in specific cases to single-crystal Al (c-Al). Thus, it needs to be considered that NW and NS Al-Ge-Al heterostructures exhibit strain due to a lattice mismatch of (c-)Al (4.05 Å) and Ge (5.65 Å). For NW-based heterostructures, a rotation of 18° is evident,[67] whereas NS-based devices exhibit a rotation of 6° between the Al and Ge layer.[11] Note

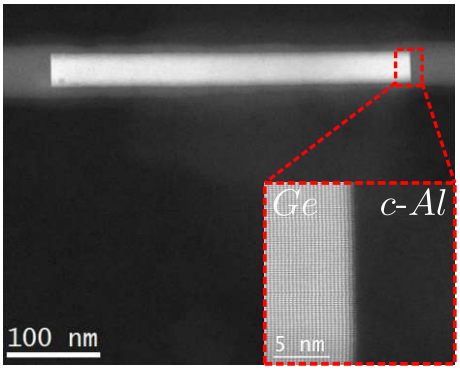

Figure 2.4: *HRTEM image of an Al-Ge junction, which reveals its high crystalline order and its abrupt interface. In the Ge-segment no Al inter-mixing can be observed.*

that, these rotations enable strain minimization and lattice relaxation. Nonetheless, it also needs to be considered that induced strain leads to changes of the electronic band structure, and thus enables advantages for certain applications.[70] Another important aspect in this context is the crystal orientation. Its influence can be classified from two perspectives. Namely, its effect on the metal-semiconductor exchange mechanism, as well as on the electronic band structure. The effect of the crystal orientation on the Al-Ge exchange was experimentally investigated on Ge NS devices by L. Wind and M. Sistani, *et al.*, by consequently rotating the Ge-layer in steps of 22.5° from the original $\langle 110 \rangle$ direction to a $\langle \bar{1}10 \rangle$ direction.[11] In conclusion, no significant dependence of the Al-Ge exchange rate was observed. Hence, leading to an advantage for wafer-scale integration of Al-Ge-Al NS heterostructures. A detailed study of the electronic band structure in dependence of the crystal orientation was carried out in various works.[71, 72] It was observed that the crystal orientation indeed affects the band structure and band gap of the semiconducting material, and therefore leading to band gap engineering approaches, which allow to tune certain FOM parameters.[19] Moreover, for thin diameter NWs quantum confinement effects lead to distinctly different electronic structures, depending on the crystal orientation. An important aspect which was neglected so far is the deposition of an oxide atop the semiconducting material, acting as a passivation layer. Hence, preventing degradation and ensuring a more reliable electrical behavior of the proposed heterostructure nanodevices.[73] Especially, from an electrical point of view this additional layer highly influences the transport mechanism, as interface traps, border traps and fixed charges affect the electrical characteristic of the proposed devices.[51, 74] In this respect, no conclusive statement regarding a dedicated origin of these traps have been identified yet.[75, 76] Most notably, charges between oxides have been observed for many years and have been explained only phenomenologically. Another discussed origin are incorporate dipoles. Nevertheless, the fabrication procedure and chemical composition, as well as the influence on the electrical characteristic is discussed in depth in Section 3.1.1.

Implementing the presented nanometer-scaled heterostructures into FET architectures, it

can be concluded that the Al-Ge material system bears a huge potential for (SB)FET architectures. Considering Al for contact fabrication, inter-mixing of the metal and semiconductor is inhibited, and is therefore preventing undesired doping of the semiconductor (here: Ge). Utilizing the substrate as back-gate and adding additional top-gates atop the heterostructure, the incorporated energy bands as well as the energy band landscape at the Al-Ge junctions can be tuned. Thus, enabling the realization of RFETs even without doping.[77, 78] A great advantage which comes with NW- or NS-based FET architectures is the possibility to create Ω-shaped gates.[79] This enables to gate the semiconducting material equivalently over the surface and side-walls. The fabrication of gate-contacts and its functional mechanism is described in more detail in Section 3.1.2.

2.2 Transport Mechanisms

Understanding the transport mechanisms in nanometer-scaled devices is important to exploit e.g., injection of charge carriers or quantum effects. Moreover, the performance of metal-semiconductor junctions are of remarkable importance in this context, as they highly influence the electrical characteristic. In the scope of this work, two different approaches are classified. Firstly, the metal-semiconductor-metal heterostructure is investigated. Special attention needs to be paid due to the fact that two Schottky contacts are involved in the proposed Al-Ge-Al system. The relevant theory and its implications for the realization of nanoelectronic devices are presented in Section 2.2.1. Secondly, the Ridley-Watkins-Hilsum theory,[31] describing the Gunn-effect, also denoted as transferred-electron effect, is discussed in detail, as this mechanism depicts the exhibition of NDR. In this context, relevant NDR FOM parameters and their characteristics are presented as well. These topics are examined in Section 2.2.2.

2.2.1 Metal-Semiconductor Junctions

In the following, the metal-semiconductor junction – namely Al-Ge – is investigated in detail. If not other stated, the theoretical aspects were taken from the book "Metal-Semiconductor Contacts" by E.H. Rhoderick and R.H. Williams.[61]
From a general point of view, a Schottky barrier is an energy barrier, which assembles as a metal and semiconductor are brought into contact. The Schottky barrier can exhibit a rectifying effect, which depends on the charge carrier transport direction, determined by the polarity of the applied bias voltage and on the attuned height of the Schottky barrier. In the simplest form, the height of this barrier is determined by the metal work function ϕ_m and the electron affinity χ of the semiconductor. Utilizing $q\phi_m$ the mean energy is obtained, which an electron needs, to be emitted to vacuum. The semiconductor work function ϕ_s merely depends on the Fermi level E_{F_S} and is based on a statistical approach. In general, for semiconductors the electron affinity χ respectively $q\chi$ determines the mechanism to elevate an electron from the conduction band to the vacuum level E_{vac}. For further considerations, Figure 2.5 shows the Schottky barrier formation through the band diagram formalism. Although, the used nanometer-scaled heterostructures in this work consist of an intrinsic semiconductor material, both – p- and n-type semiconductors

are considered in this illustration, as it gives a good insight on the band bending mechanism at the metal-semiconductor junction. Note that, utilizing the band diagram formalism to describe Schottky barriers, three main assumptions are taken into account.[42]

- The contact between the metal and the semiconductor must be intimate and without the presence of any other material layer (such as an oxide).
- No interdiffusion of the metal and the semiconductor is taken into account.
- There are no impurities at the interface between the two materials.

In correlation with Figure 2.5, this allows to deduce the following equations for the metal work function (Equation 2.1) and the electron affinity (Equation 2.2), where E_{vac} is the energy level of the vacuum, E_{F_m} is the Fermi energy level of the metal and E_c is the energy level of the conduction band.

$$q\phi_m = E_{\text{vac}} - E_{F_m} \tag{2.1}$$

$$q\chi = E_{\text{vac}} - E_c \tag{2.2}$$

In a next step the Schottky barriers for electrons $q\phi_{Bn}$ (Equation 2.3) and holes $q\phi_{Bp}$ (Equation 2.4) can be deduced.

$$q\phi_{Bn} = q(\phi_m - \chi) \tag{2.3}$$

$$q\phi_{Bp} = E_g - q(\phi_m - \chi) \tag{2.4}$$

where E_g is the band gap energy, which can therefore also be ideally expressed as the sum of the Schottky barriers for electrons $q\phi_{Bn}$ and holes $q\phi_{Bp}$.

Bringing the metal and semiconductor into contact, the metal and semiconductor Fermi levels level out by establishing equilibrium, i.e. by a charge carrier flow. Thus, leading to band bending of the incorporated energy bands in the semiconductor. Consequently, the conduction band E_c, the valence band E_v and the vacuum energy E_{vac} in the semiconductor region show band bending towards the metal contact. Hence, the in-built voltage V_{bi}, which is acting similarly to a threshold voltage, is exhibited. In the case that a bias voltage of V_{bi} is applied, the flat-band condition is fulfilled. The in-built voltage V_{bi} can be expressed as depicted in Equation 2.5.

$$V_{bi} = \phi_m - \phi_s \tag{2.5}$$

A major topic in the scope of real Schottky barriers, is the issue of Fermi level pinning. In an ideal scenario, Al and Ge would lead to a Fermi level pinning close to the mid-gap energy, as the Fermi level of Al – denoted by the metal work function $\phi_m = 4.20\,\text{eV}$ – is close to the Fermi level of intrinsic Ge ($\chi = 4.00\,\text{eV}$ and $E_g = 0.66\,\text{eV}$). Thus, leading to similar

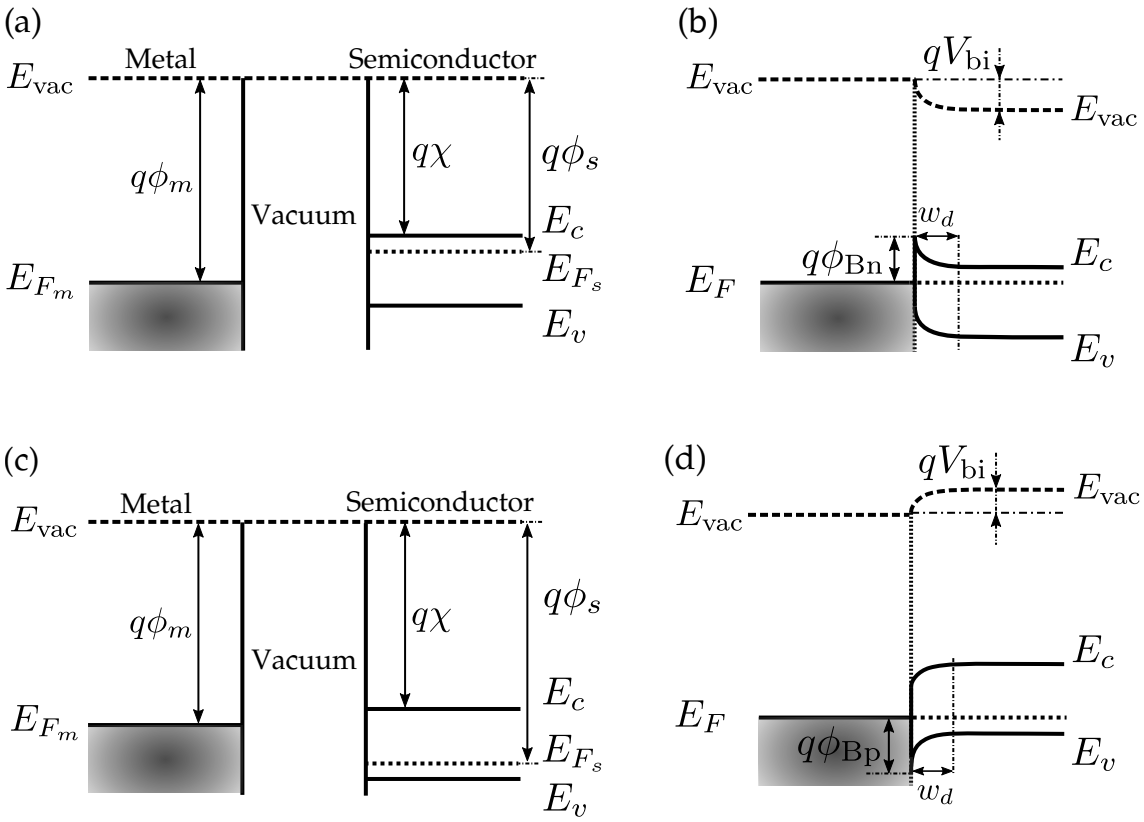

Figure 2.5: *Schottky barrier formation through the band diagram formalism. (a) shows the metal and a n-type semiconductor when separated, whereas (b) illustrates the metal and n-type semiconductor when brought into contact. (c) and (d) show the same concept, but for a p-type semiconductor. In (b) and (d) the typical band bending and the exhibition of V_{bi} is visible.*

barrier heights for electrons and holes. However, for real metal-semiconductor junctions, surface and interface trap states need to be considered, as they dominate the electrical characteristic of the barrier. In consequence, these states lead to Fermi level pinning, which means that an asymmetric barrier for electrons and holes can exist. Hence, causing a dominant n- or p-type transport mechanism through the Schottky barrier. This issue then leads to asymmetric electron- and hole currents. Figure 2.6 illustrates the influence of these surface traps on the Schottky barrier and indicates the effect of Fermi level pinning. The presented illustration depicts an intrinsic semiconductor.

In general, Fermi level pinning results from an equilibrium condition of the free surface of a semiconductor, which is different from bulk materials, because the surface of a semiconductor does not have a band gap in contrast to a bulk semiconductor. In the case of an infinite bulk semiconductor, the Kronig-Penney model and Bloch's Theorem are used to derive the E(k) relations. Consequently, solving the Schrödinger equation allows to determine "forbidden" E(k) values, which determine the band gap in bulk materials. Note that

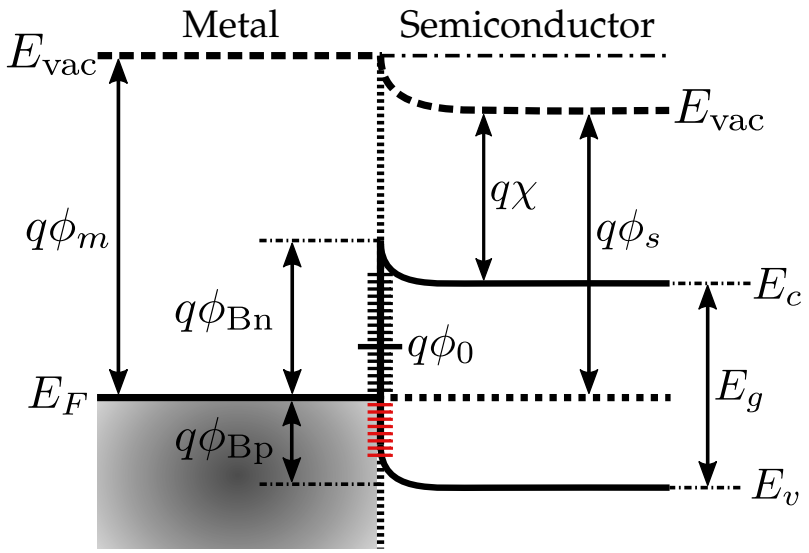

Figure 2.6: *Effect of surface states on the Schottky barrier, which lead to Fermi level pinning in thermal equilibrium. Surface states which are below the Fermi level (red) are filled and therefore pin the Fermi level to the energy, which leads to equilibrium (CNL). Uncharged surface traps above the Fermi level (black) are empty.*

this is only valid for an infinite collection of one-dimensional potential wells separated by narrow barriers.[42] As this concept cannot be applied for the surface of a semiconductor, a different model needs to be used. Namely, that the interface consists of a continuum of localized energy states within the band gap. These energy states can be considered as traps, but do not origin from defects or impurities, and can be empty – depicted by the black bars in Figure 2.6 – or filled – depicted by the red bars in Figure 2.6. It is common to define the energy $q\phi_0$, which indicates the energy that the Fermi level must assume if the surface is electrically neutral. If states below ϕ_0 are empty, the surface has a net positive charge, while states above ϕ_0 determine negative charges when filled. Hence, states below ϕ_0 are described as donor-like (positive when empty) and states above ϕ_0 as acceptor-like (negative when filled). In the absence of surface states, the Fermi level is pinned to the mid-gap energy, as there is no net charge. In consequence, this level is named charge neutrality level (CNL). Note that even clean cleaved surfaces of Ge have a high density of surface states.[74] In this scenario, ϕ_0 does not lie at the same position as the Fermi level due to a net charge at the surface, which produces an electric field in the semiconductor, which causes bending of the energy bands and thus leading to Fermi level pinning. Thanailakis and Northrop found that the density of states for Ge is in the range of 2×10^{17} eV^{-1} m^{-2}. Moreover they proposed that the CNL is only 0.13 eV above the top of the valence band.[15]

In the past, many works were published regarding the strong Fermi level pinning close to the valence band of Ge, leading to a dominant p-type conduction in Ge-metal systems.[80–82] In contrast, Si shows mid-gap Fermi level pinning for many metals.[83] For the realization of CMOS-compatible transistors, symmetric n- and p-type conduction is mandatory,

demanding a symmetric Schottky barrier height (SBH) for electrons and holes in the case of thermionic emission. In this respect, various approaches were analysed to de-pin the Fermi level of Ge. These concepts mainly rely on the implementation of a high-κ layer between the semiconductor and metal.[84, 85]

Applying a bias voltage and considering the band bending mechanism at the metal-semiconductor interface, leading to energy modifications of the bands, and thus contributing to various charge carrier transport mechanisms. Figure 2.7 depicts involved mechanisms which contribute to charge carrier transport, and thus determine the total current through the Schottky barrier. Note that the illustrated bands are valid for the case that no bias voltage is applied, whereas actual transport mechanisms only take place in the case of an applied bias.

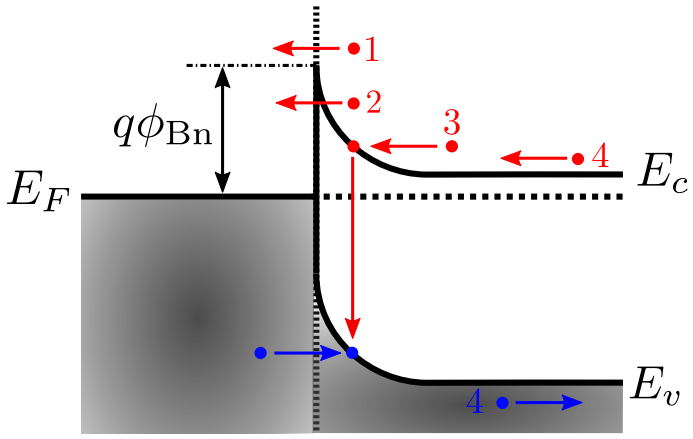

Figure 2.7: *Transport mechanisms involved at the Schottky barrier upon the application of a bias voltage. The total current through a metal-semiconductor consists of (1) thermionic emission of charge carriers over the barrier, (2) tunneling of charge carriers through the barrier, (3) recombination in the depletion region and (4) diffusion of electrons or holes. Figure adapted from [42].*

The major contribution is due to thermionic emission, denoted by (1). This transport mechanism consists of an electron which is elevated to an energy, at which it can easily overcome the barrier. The second transport mechanism is direct charge carrier tunneling denoted by (2) in Figure 2.7. The contribution of tunneling increases significantly in the case that the bands show strong bending to an extent that the thickness of the barrier is getting thinner and thus, allowing charge carriers easier quantum mechanically to tunnel through the barrier. This mechanism is also well-known as Fowler-Nordheim tunneling.[42] Tunneling can also be set into relation to the transmission probability $T \propto \exp(-a\phi_b)$, where a is the width of the barrier at the corresponding energy and ϕ_b is the barrier height. Hence, tunneling directly affects the effective Schottky barrier height (eSBH), as charge carriers effectively experience a lower Schottky barrier. Moreover, it was shown that mechanical stress can be used to tune the tunneling probability.[86] Recombination (3) and diffusion (4) are only of minor interest, as they do not significantly contribute

to the charge carrier transport. In Figure 2.7, the transport mechanism is considered for electrons, however is equally valid for holes as well.
It needs to be considered that from an experimental point of view the different transport mechanisms cannot be entirely distinguished from each other, as only the total current through the Schottky barrier can be measured. However, trends of certain transport mechanisms are evident. For a detailed analysis of the contributions, corresponding models and simulations need to be utilized.

As an approximation, the current through the Schottky barrier can be calculated according to Equation 2.6, as deduced from the thermionic emission theory.

$$J = J_0[\exp(qV/k_BT) - 1] \tag{2.6}$$

where J is the current density at the Schottky barrier. J_0 is defined in Equation 2.7.

$$J_0 = A^*T^2 \exp[-q(\phi_b - \Delta\phi_{bi})/k_BT)] \tag{2.7}$$

where A^* is the Richardson constant and T is the temperature. It needs to be considered that in this work an experimental study of the metal-semiconductor barrier is performed. In this thesis, the expression $\phi_b - \Delta\phi_{bi}$ will be named "eSBH" from now on, as an experimental evaluation does not allow to determine the Schottky barrier explicitly. This can mainly be attributed to the fact, that the contribution of tunneling cannot be accurately determined by electrical measurements only. A detailed analysis on how to obtain the eSBH of the proposed Al-Ge-Al heterostructures is given in Section 3.2.3.

Finally, considering the complete Al-Ge-Al nanometer-scaled heterostructure with its metal-semi-conductor junctions and considering the previously discussed aspects regarding the strong Fermi level pinning close to the valence band in Ge-metal semiconductors,[81] the structure can be illustrated through the band diagram formalism, as shown in Figure 2.8.

It can be deduced that p-type operation is dominant in the proposed Al-Ge-Al SBFET heterostructure. Considering the substrate (violet) as back-gate and consequently applying a positive or negative voltage, the incorporated energy bands can be tuned. Hence, leading to the typical SBFET characteristic.[10] Applying a positive back-gate voltage, the bands are getting pulled downwards, whereas applying a negative voltage pulls the band upwards. Both mechanisms lead to thinner barriers and do therefore, increase the probability of tunneling. In case of applying a bias voltage, the whole band diagram gets tilted. Thus, allowing charge carriers to flow in dependence of the back-gate and bias potential. In theory, this enables the SBFET to operate in n- and p-type conduction mode. Further details, regarding this device architecture and functional mechanism are discussed in Section 3.1.2.
Another essential feature of SBFETs is its capability to tune the energy band landscape directly at the metal-semiconductor junctions by placing top-gates atop the Al-Ge interfaces. This allows to tune the injection capabilities by influencing the barrier heights and

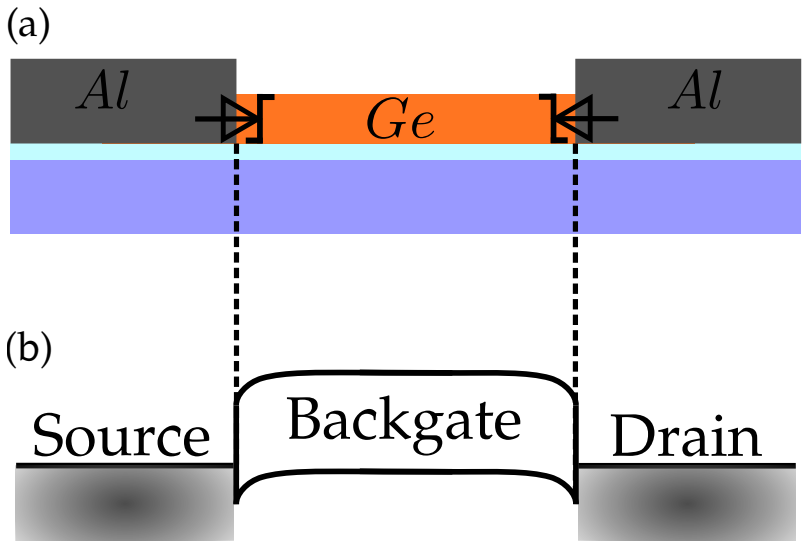

Figure 2.8: *Al-Ge-Al heterostructure implemented in a (SB)FET architecture, where (a) shows the heterostructure with the two involved metal-semiconductor junctions. Consequently, leading to the band diagram shown in (b). Due to surface states, the Fermi level is pinned close to the valence band, and hence leading to a dominant p-type characteristic.*

depletion widths, and thus enables to control the injection of different charge carriers into the semiconducting channel. Hence, leading to a platform suitable for the realization of RFETs, as already shown in previous works.[21] In this work various top-gate architectures are analyzed and the road to an actual RFET is depicted in Section 4.3.

2.2.2 Transferred-Electron Effect

The transferred-electron effect describes a transport phenomena, which occurs by applying sufficiently high electric fields and therefore, allowing hot electrons to scatter from one conduction band to another conduction band. Due to different properties of the two involved bands, i.e., the degree of curvature, certain effects are observed. The transferred-electron effect was firstly observed by Gunn in 1963 on GaAs structures.[30] However, in principal, this effect can be described by the Ridley-Watkins-Hilsum theory.[31] It is of high importance due to its exhibition of NDR, which allows to exploit various "More-than-Moore" concepts.[34, 87] In the scope of this work, the proposed Al-Ge-Al heterostructure is used to analyze this effect. The band structure of Ge, as depicted in Figure 2.9, illustrates its capability for the realization of NDR devices.

As the conduction band edge E_c of Ge lies only 0.19 eV below the minimum of the second conduction band, electrons can be transferred from the $\langle 111 \rangle$- to the $\langle 100 \rangle$-reservoir by applying sufficiently high electric fields. The inset in Figure 2.9 shows the influence of the band curvature on the effective masses m^*, respectively the electron mobilities μ_n. For further considerations, Equations 2.8 and 2.9 give the definition and direct relation to the

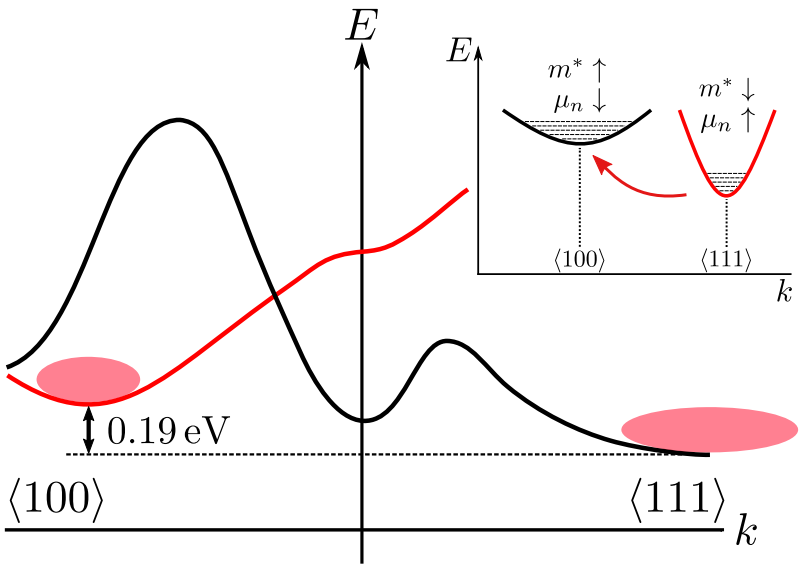

Figure 2.9: *Schematic illustration of the transferred-electron effect in Ge. Applying a sufficently high electric field, electrons from the ⟨111⟩-reservoir (low m^*, thus high μ_n) can be transferred to the ⟨100⟩-reservoir (high m^*, thus low μ_n). The inset depicts the influence of the band curvatures on the electron mobilities μ_n.*

velocity v – and in consequence to the current I of the accelerated charge carriers.[42, 88] The definition of mobility can be derived by starting with Newton's Second Law, stated in Equation 2.8, where a is the acceleration between collisions, $F = -qE$ is the electric force exerted by the electric field and m^* is the effective mass of the electron.

$$a = \frac{F}{m^*} \tag{2.8}$$

Furthermore, the velocity v can be expressed by considering the mean free time τ_c as described in Equation 2.9.

$$v = a\tau_c = -\frac{e\tau_c}{m^*}E = \mu_n E \propto I \tag{2.9}$$

This derivation allows to set the current I in relation to the effective mass m^*, respectively to the electron mobility μ_n. In conclusion, the whole process can be described as followed: Hot electrons are scattered from the energetically favorable conduction band valley at ⟨111⟩, characterized by a low effective mass m^* to a heavy mass valley nearby.[30] Although, the ⟨000⟩-valley is energetically closer to the ⟨111⟩-valley, the coupling constant between ⟨111⟩ and ⟨100⟩ is significantly higher and is thus preferred.[89] This can be attributed to the few DOS of the ⟨000⟩-valley (Γ-point). Consequently, as schematically illustrated in the inset of Figure 2.9, the transferred-electron effect in Ge is most likely to apply from the ⟨111⟩- to the ⟨100⟩-valley. The respective effective mass in the relevant regions are $m^*_{\langle 111\rangle} = 0.288\ m_0$ and $m^*_{\langle 100\rangle} = 0.082\ m_0$.[89] In general, the manifestation of

the transferred-electron effect is increasing in correspondence to a low occupation of the second conduction band. In this context, low temperatures and un-doped semiconductors (here: Ge) lead to a more pronounced effect.
As depicted, hot electrons are necessary for accessing the transferred-electron effect. This is achieved by consequently increasing the applied bias voltage and measuring the current, which results in a current-voltage (I/V) characteristic. The transferred electrons in the ⟨100⟩-valley have a higher electron mass m^*, and thus a lower electron mobility μ_n. This results in a negative slope of the current I.[90] Hence, leading to NDR, as shown in Equation 2.10.

$$r_{\text{diff}} = \frac{\mathrm{d}V}{(-)\mathrm{d}I} \tag{2.10}$$

For the characterization of the NDR, various performance metrics respectively FOMs can be extracted from the I/V characteristic. The typical NDR characteristic, as well as basic parameters, are illustrated in Figure 2.10. Note that two different NDR curves are shown, as the valley voltage V_V can exhibit a plateau which is indicated by V_{PT}.

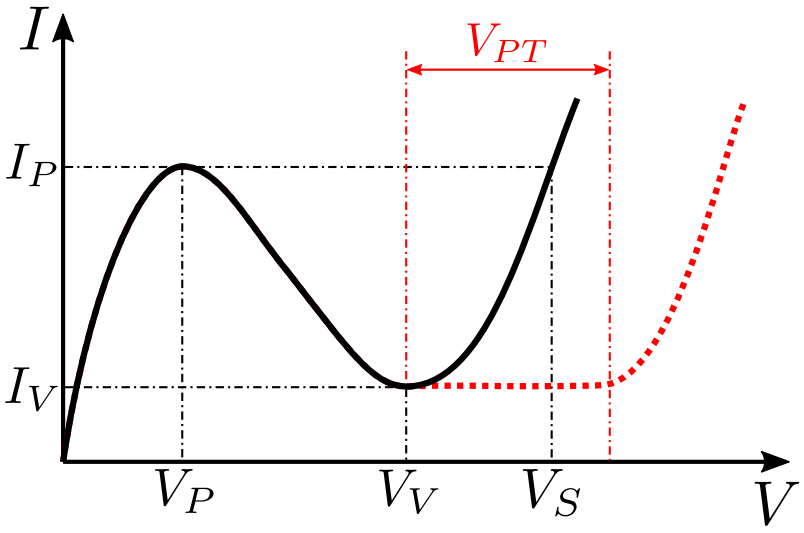

Figure 2.10: *Typical NDR I/V characteristic with its relevant parameters. The stated currents and voltages are used to characterize the NDR performance. The red-dotted curve shows a NDR characteristic with a voltage plateau V_{PT} in the valley.*

Extracting the parameters depicted in Figure 2.10, certain performance metrics can be evaluated.[91] Characterizing NDR devices, the most important FOM is the peak-to-valley current ratio (PVCR), which is defined according Equation 2.11.

$$\text{PVCR} = \frac{I_P}{I_V} \tag{2.11}$$

The PVCR is a unit-less parameter that must be greater than unity to observe NDR. A significantly larger PVCR is desirable for many logic applications to precisely distinguish between the peak- and valley-state.

The peak-current density J_P is another important metric for NDR devices and is defined according to Equation 2.12.

$$J_P = \frac{I_P}{A} \tag{2.12}$$

where A is the cross-sectional area of the device. For high-speed and RF applications, a high J_P is desired to access a fast charging/discharging behavior. In contrast, a low J_P is desired for low-power circuit applications as this parameter is directly related to the power consumption.
The voltage span $V_V - V_P$ is a metric to characterize the width of the NDR region. Moreover, by including the difference current $I_P - I_V$, the so-called current span, it allows to determine the slope of the NDR region, also denoted as conductance $G = 1/R_S$. Thus, the voltage span is a function of the series resistance R_S and in consequence tuning of the NDR region, by varying the series resistance is possible. A large R_S can even make V_P equal to V_S, with a corresponding zero voltage span. Another important FOM is the voltage swing defined by $V_S - V_P$. This parameter determines the broadness of the NDR valley. In this context another important parameter – the valley voltage plateau V_{PT} needs to be considered, as this parameter is directly related to the voltage swing. The voltage plateau is illustrated by the red-dotted NDR characteristic in Figure 2.10.

Utilizing the presented mechanisms and metrics it allows to realize and characterize NDR devices. It needs to be considered that in the past the exhibition of NDR was restricted for group-IV semiconductors, due to limitations of temperature[32, 33] or due to transient effects of surface traps[38, 92]. Hence, group-III/V semiconductors were mainly used, due to their dedicated property for the fabrication of quantum-wells and thus enabling the realization of RTDs. However, in the scope of this thesis the transferred-electron effect is considered for the exhibition of NDR. In this respect, the temperature and dopant concentration need to be considered, as they are major limitations for the observation of NDR. Due to higher charge carrier populations in the conduction bands, caused by elevated temperatures or high dopant concentrations, a pronounced NDR is inhibited. In this context, the proposed Al-Ge system reveals a huge advantage in comparison to other metal-Ge systems, due to its non-existent inter-metallic phase as well as a non-perceivable contamination of Al in the Ge segment. Thus, enabling a reliable platform for the realization of NDR devices.
Emerging nanoelectronic concepts, as MOBILE or MVL gates require circuits with multiple NDR regions.[34, 36] An example for an actual circuit is the utilization of parallel NDRs, exhibiting different V_P and V_V. As discussed, this is so far restricted by the series resistance R_S, which is determined by the geometry of conventional NDR devices. In this work, concepts are presented, which allow to de-couple the NDR position from the geometry by electrostatically tune V_P and V_V. The realization and characterization of tunable NDR devices are presented in Section 4.4 and 4.5. Two relevant state-of-the-art NDR devices are discussed in the following section, Section 2.3.

2.3 State-of-the-Art Devices

As already depicted, the presented nanometer-scaled Al-Ge-Al heterostructure allows to exploit the realization of RFETs and NDR devices. In the past, the functionality of these concepts were proven in various works.[19, 20, 32, 38, 93] Remarkable results of the RFET functional mechanism were shown on the basis of Si and Ge, but were mostly realized by utilizing Ni contacts, and thus leading to the formation of silicides and germanides.[20, 22] The actual devices consist of multiple gates, allowing to tune the incorporated energy bands as well as explicitly the energy landscape at the metal-semiconductor junctions.[23] Hence, allowing a programmable transistor solution to switch between n- and p-type operation. The realization of NDR devices mainly focused on group-III/V semiconductors, implemented in quantum wells – also well-known as RTDs.[27, 91] Nevertheless, promising Ge-based approaches were shown as well.[32, 33, 93, 94]
Section 2.3.1 gives an insight on published works of Si- and Ge-based RFETs, whereas Section 2.3.2 gives an overview of state-of-the-art Ge-based NDR devices. For both device concepts limitations and performance enhancements are discussed.

2.3.1 RFETs

The concept of RFETs was first described in the early 2000s.[20] The goal was to suppress the high off-currents, which are evident in ambipolar Schottky barrier thin film transistors. An important advantage of SBFETs is the use of un-doped semiconductors. By consequently placing two top-gates atop the Schottky barriers, it allows to electrostatically dope the semiconductor by tuning the energy region at the Schottky barriers. Accordingly, enabling to switch between n- and p-type operation. Hence, this concept allows to suppress the undesired charge carrier leading to a low off-current. One gate – denoted as control-gate (CG) – is placed directly on the source-sided Schottky junction. Therefore, allowing to turn the transistor on and off. The second gate is placed at the drain-sided Schottky junction and allows to set the polarity – namely to n- or p-type – by actually altering the polarity of the applied gate voltage. In consequence, this gate is called the polarity-gate (PG). Commonly, this functional mechanism is expressed by the band diagram formalism (as introduced in Section 2.2.1). A comprehensive work, based on Si NW was published by A. Heinzig *et al.* and is entitled "Reconfigurable Silicon Nanowire Transistors".[21] In that work the basic functionality of a RFET is depicted, as illustrated in Figure 2.11.

Sweeping V_{CG} and consequently setting V_{PG} to positive or negative values, a dominant n- and p-type operation can be obtained. It needs to be considered that the contacts are realized by $NiSi_2$ contacts, which exhibit different properties from a fabrication as well as electrical point of view in comparison to the Al-Ge system (see Section 2.1.3). Analyzing the transfer characteristic shown in Figure 2.11b, an asymmetry of factor 10 between n- and p-type operation is evident. In later works symmetry is achieved by strain engineering.[95, 96]

Another important contribution was done in the work "Enabling Energy Efficiency and

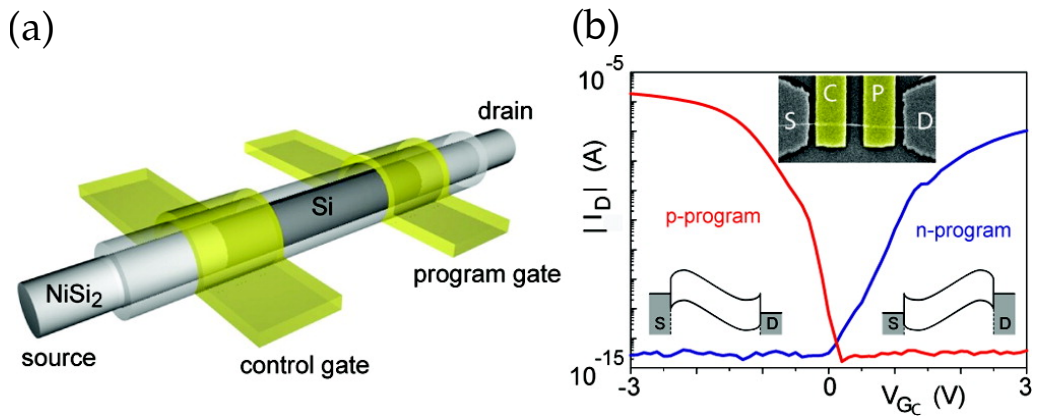

Figure 2.11: *Overview of the work "Reconfigurable Silicon Nanowire Transistors" by A. Heinzig et al., where (a) shows the schematic architecture of the Si NW RFET, realized with $NiSi_2$ contacts. (b) shows the transfer characteristic (I_D vs. V_{CG}) of the n- and p-type operation. The top inset in (b) shows the placement of the CG and PG and the bottom insets show the corresponding band diagrams. Images from [21].*

Polarity Control in Germanium Nanowire Transistors by Individually Gated Nanojunctions" by J. Trommer *et al.*, which shows remarkable results of a Ge-based NW RFET.[19] Figure 2.12 gives an overview of the architecture and results presented in the work by J. Trommer *et al.*

This work reveals the huge potential for Ge-based heterostructures by explicitly showing its suitability for RFET concepts. However, in the presented work Ni_2Ge contacts were used to pin the Fermi level close to the mid-gap energy of the Ge channel. Hence, taking its disadvantages into account. Figure 2.12c clearly depicts the mechanism of electronic doping, as the bands can be tuned by setting V_{PG} correspondingly, and thus allowing to suppress the undesired charge carrier. Applying a negative V_{PG} the bands are getting pulled upwards, enabling p-type operation, whereas applying a positive V_{PG}, tee device is operated in n-mode by consequently bending the bands downwards. Moreover, simulation results with Mn_5Ge_3 contacts are presented, which potentially lead to a symmetric transfer characteristic.

As briefly depicted, past RFET concepts are merely based on inter-metallic contacts, which highly differ in variability, and therefore lead to an unreliable electrical behavior. Also, experimental studies were mostly conducted on NW-based two top-gate solutions. So far the realization of RFETs with pure metal contacts, e.g. Al-Ge, as well as top-down schemes, for example based on GeOI, are pending. Most notably, simulation results already revealed the huge potential of an additional top-gate in the middle of the channel, acting as the CG.[19] Hence, leading to an even better suppression of the undesired charge carrier and thus enabling lower off-currents.
As stated in the introduction, the era of functional diversification of RFETs already started

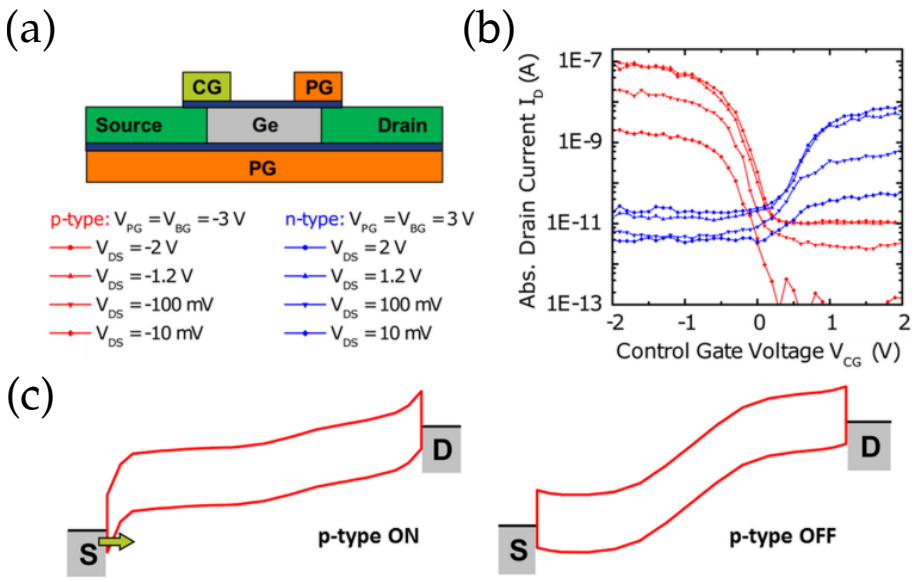

Figure 2.12: *Overview of the work "Enabling Energy Efficiency and Polarity Control in Germanium Nanowire Transistors by Individually Gated Nanojunctions" by J. Trommer et al., where (a) shows the device architecture with two independent top-gates. As illustrated in (b), the transfer characteristic depicts a pronounced n- and p-type operation. (c) shows the band bending mechanism for p-type conduction (left) and p-type suppression (right). Images from [19].*

in 2014.[20] In this context, material-related investigations, i.e. FinFETs, SOI, various contact metals, as well as the analysis of transport mechanisms, e.g. impact ionization, steep sub-threshold slope (SS), were already carried out. Moreover, first logic gates were realized by RFETs.[20] Besides the fact that Ge allows to reduce threshold voltages as well as enables energy-efficient solutions,[19] it allows to access the transferred-electron effect. Thus, may paves the way to further exploit the era of functional diversification of RFETs by enhancing the conceptual mechanism with NDR functionality.

2.3.2 NDR Devices

Aside of the description of the Gunn effect and related transferred-electron effect devices, addtional NDR devices were realized, which mainly consisted by the utilization of quantum wells and group-III/V semiconductors. In general, the NDR behavior in quantum well heterostructures is obtained by resonant tunneling effects. These type of devices are also well-known as RTDs.[91, 97] Another way to exploit the tunneling effect, and thus enabling NDR, is the Esaki tunneling diode, which is based on a similar concept.[42, 98] A detailed explanation of these group-III/V concepts is given in the work "Negative Differential Resistance Devices and Circuits" by Berger P.R. and Ramesh A.[91]
As this work focuses on Ge, important Ge-based state-of-the-art NDR devices are discussed in this section. A first step into the direction of Ge-based NDR devices was done by D. Kazazis *et al.* in the work "Negative differential resistance in ultrathin Ge-on-

insulator FETs". D. Kazazis *et al.* exploited GeOI for the realization of NDR devices.[32] However, NDR was merely observed at cryogenic temperatures down to 4.2 K. They claim that, beside the confined Ge between a LaYO and SiO_2 layer and trapping effects, the transferred-electron effect enables NDR. Figure 2.13 gives an overview of the device architecture and shows the NDR characteristics at $T = 77\,\mathrm{K}$ and $T = 4.2\,\mathrm{K}$.

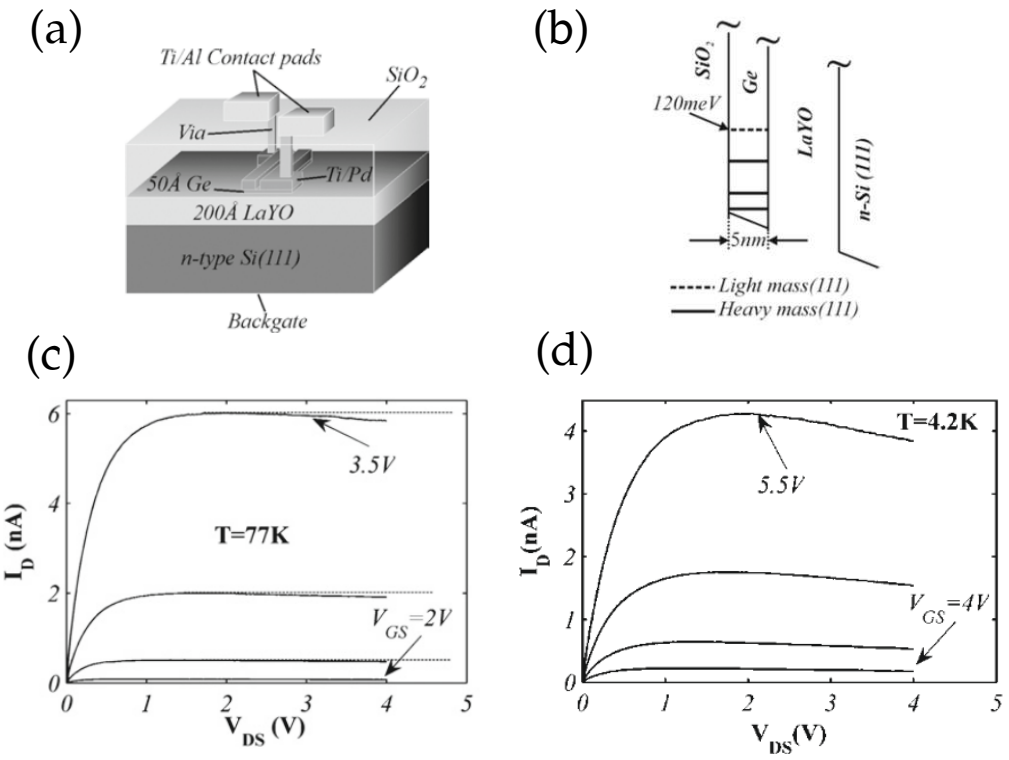

Figure 2.13: *Overview of the work "Negative differential resistance in ultrathin Ge-on-insulator FETs" by D. Kazazis et al., where (a) illustrates the device architecture and (b) the corresponding band structure of the proposed material system. The NDR I/V characteristics at $T = 77\,\mathrm{K}$ and $T = 4.2\,\mathrm{K}$ are shown in (c) and (d) respectively. Images from [32].*

In that work, the PVCR does not show high values even at relatively low temperatures. From a fabrication point of view it needs to be considered that LaYO is a complex technology. Nevertheless, the proposed material stack leads to high costs and efforts to be implemented in industrial applications.

A more promising concept was published by F.M. Brunbauer *et al.*, in the work "Gate-Tunable Electron Transport Phenomena in Al-Ge⟨111⟩-Al Nanowire Heterostructures".[33] Here, the device architecture consists of a bottom-up grown NW-based back-gate Al-Ge-Al heterostructure embedded in a FET architecture. Notably, the NDR characteristic showed remarkable results from a PVCR point of view. Moreover, the dedicated transferred-electron effect in Ge was mainly made responsible for the pronounced NDR. Figure 2.14 gives an insight on the used NW architecture and the obtained results.

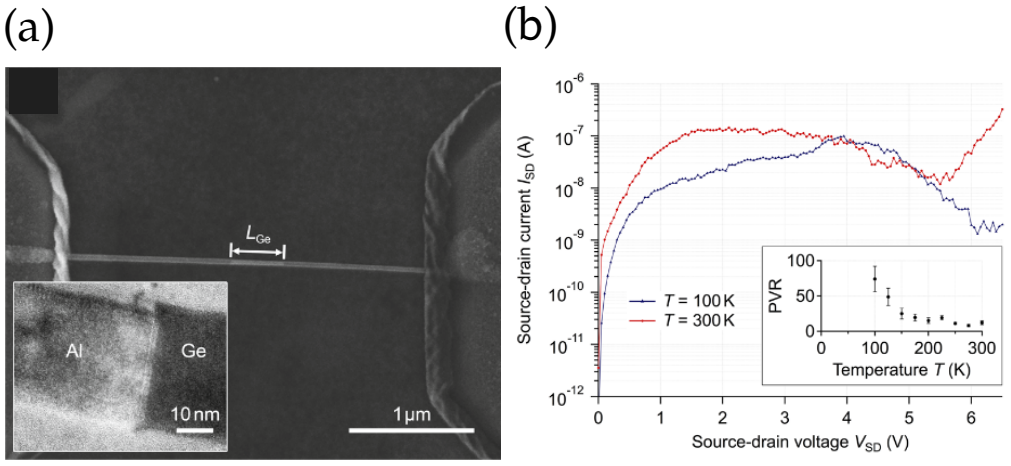

Figure 2.14: *Overview of the work "Gate-Tunable Electron Transport Phenomena in Al-Ge⟨111⟩-Al Nanowire Heterostructures" by F.M. Brunbauer et al., where (a) shows the device architecture, which is similar to the one used in this work. As illustrated in (b), the I/V characteristic, shows that the PVCR decreases with increasing temperature. Images from [33].*

F.M. Brunbauer *et al.* showed the capability of Al-Ge-Al heterostructures for NDR devices in a NW-based back-gate FET architecture. Remarkably, a PVCR of 42 even at room temperature was shown. In comparison to Esaki diodes, with a PVCR ranging from 106 to 1.2, comparable results were obtained.[91] Applying sufficiently high back-gate voltages even impact ionization was proven on the proposed devices.

In the scope of this work, the functional diversification and variability of RFETs shall be targeted by further enhancing and exploiting the underlying physical phenomena and architectures. Firstly, by utilizing Ge as the semiconducting material, the transferred-electron effect is accessed, and thus allows "More-Moore" paradigms. Secondly, GeOI approaches in the form of NSs allow the realization of top-down RFETs, and hence enabling variability. Moreover, by applying a multi-gate approach it is expected to enhance NDR performance metrics, in general. This can be attributed to the fact that top-gated architectures allow to influence the incorporated energy bands more precisely, and accordingly enabling a profound way of tuning. From a platform point of view, the used Al-Ge system ensures pure metal-semiconductor junctions, which further enhance the proposed solutions from a material perspective. Hence, preventing the formation of inter-metallic phases, and therefore enabling more reliable and re-producible device architectures.

Chapter 3

Experimental Techniques

For the realization and characterization of RFETs and NDR devices it needs to be ensured, that methods and techniques are utilized, which enable good handling of the devices and ensure reliable measurement access. Therefore, this chapter starts with the device integration onto a substrate respectively chip. Moreover, as briefly depicted in Section 2.3, the fabrication of top-gates needs to be done accordingly. Thus, enabling the realisation of RFETs and the enhancement of NDR devices by electrostatically tuning the energy regions of the incorporated bands. The integration and realization of the used FET devices is discussed in Section 3.1. Here, the main focus is set to differences between NWs and NSs from a fabrication and material point of view. Moreover, by utilizing back- and/or top-gates, the functional mechanism of band tuning is presented. After successfully embedding the proposed Al-Ge-Al heterostructures into back- or top-gated FET architectures, electrical characterization methods are necessary to evaluate the functionality and performance of the devices. In this respect, Section 3.2 is dedicated to the used measurement setup as well as the utilized characterization methods.

3.1 Device Integration

The device integration needs to ensure that proper handling and accessibility to conduct measurements is guaranteed. In this context, it needs to be distinguished between the integration of NWs and NSs, as the two concepts differ from a fabrication and material point of view. The related issues which arise from this fact are discussed in Section 3.1.1. After successfully placing. contacting and annealing (see Section 2.1.3) the NWs or NSs, nanodevices are obtained, which are integrated into a back-gated (SB)FET architecture. These back-gate FETs build the base for all presented device architectures. However, top-gates are mandatory for the realization of RFETs and for the enhancement of NDR devices. Therefore, Section 3.1.2 discusses the band bending, and thus tuning mechanisms of the two architectures, namely back-gate and top-gate FETs. Again, differences between

the NW- and NS-approach are considered.

3.1.1 Nanowire *versus* Nanosheet Integration

As briefly depicted in Section 2.1.2, certain differences from a fabrication and material point of view for NWs and NSs need to be considered. Besides the different geometries (NWs have a cylindrical cross sectional area, whereas NSs have a rectangular cross sectional area), this includes the starting materials as well as the final material stack after the deposition of the passivation layer.
The starting material for the NW-based devices were Ge NWs with diameters of approximately 30 nm, grown on a Si (111) substrate using the vapor-liquid-solid (VLS) process with germane (GeH_4, 2 % diluted in He) as precursor and a 2 nm thick sputtered Au layer as growth promoting catalyst.[99] The growth was performed in a low pressure hot wall chemical vapor deposition chamber. Subsequent to the growth, the Ge NWs were coated with 22 nm high-κ Al_2O_3 using atomic layer deposition (ALD), which acts as the oxide passivation layer. For the integration of NWs, it turned out that so called hexpad chips satisfy the requirements of proper device handling and enabling comprehensive measurement access. The hexpad chip consists of a 525 µm thick p-doped Si substrate and a 100 nm thick SiO_2 layer acting as back-gate oxide atop the Si substrate. Utilizing optical lithography, the hexpad structure, i.e. encompassing an hexagonal arrangement of contacts, is transferred to the substrate by consequently evaporating the 100 nm to 120 nm thick Au pads. Note that the back-gate contacts (yellow dots and triangular respectively rectangular areas in the schematic illustration of the hexpad chip shown in Figure 3.1) need to be done in prior to the field fabrication due to a mandatory etching of the SiO_2 oxide and thus enabling to contact the Si substrate. A schematic illustration of such a hexpad chip and an inset microscope image of a single field is shown in Figure 3.1.

By drop-casting the already Al_2O_3-passivated $\langle 111 \rangle$ Ge NWs on the chip, various NWs are placed all over the hexpad. An example for placed and already connected NWs can be seen in the microscope image in Figure 3.1. By utilizing SEM analysis, favourable NWs are localized within the fields and are then consequently connected by Al leads using electron beam lithography (EBL), sputtering and lift-off techniques. Note that before the deposition of the Al leads, a short HI dip needs to be performed to remove the Al_2O_3 passivation layer. Afterwards, the Al-exchange reaction can be initiated by utilizing RTA. By setting the temperature and duration accordingly, various lengths of the Ge segment can be adjusted (see Section 2.1.2). This finally results in an Al-Ge-Al NW heterostructure with abrupt metal-semiconductor junctions embedded in a back-gate (SB)FET architecture. SEM and TEM images of such devices are illustrated in Chapter 2.
The NSs are fabricated from intrinsic GeOI substrates compromising a 75 nm thick (100) oriented Ge device layer atop of a 150 nm buried SiO_2 (BOX) layer and a 500 µm thick Si substrate.[11] The Ge nanostructures were patterned using EBL and a SF_6-O_2-based reactive ion etching (RIE) process. Subsequently, the Ge structures were coated with 22 nm of Al_2O_3 deposited by ALD. Al pads contacting the Ge nanostructures were fabricated by

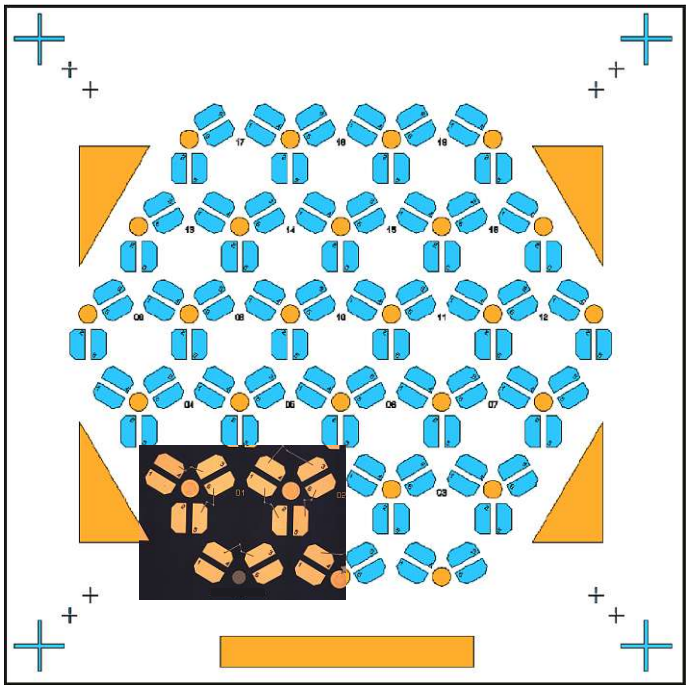

Figure 3.1: *The* 11 mm×11 mm *hexpad chip consists of 19 fields with six pads per field. The yellow dots, triangles and rectangle are connected to the p-doped Si substrate and can therefore be utilized as back-gate contacts. The inset shows a microscope image of field "1" with three already connected (back-gated) NW FETs.*

optical lithography, 125 nm Al sputter deposition, preceded by a 25 s buffered HF (7:1), 5 s HI dip (14 %) to remove the Al_2O_3 and the Ge oxide, and lift-off techniques. For the Al-Ge exchange the RTA process at a temperature of $T = 674\,\mathrm{K}$ in forming gas atmosphere is used. By utilizing this approach, various widths W_{NS} can be fabricated, as illustrated by SEM images in Figure 3.2.

Thus, NS-based approaches allow to perform profound investigations on the geometrical dependency of the electrical characteristic, as on the same substrate different geometrical dimensions can be realized. For fair performance comparisons between NSs and NWs the quasi-diameter d_{NS} of NSs needs to be considered. Therefore, Equations 3.1 and 3.2 depict how the quasi-diameter d_{NS} of NSs is derived.

$$A_{NS} \stackrel{!}{=} A_{NW} \tag{3.1}$$

where $A_{NS} = h_{NS}W_{NS}$ and $A_{NW} = \frac{d_{NW}^2\pi}{4}$. Consequently, A_{NS} can be set equal to $\frac{d_{NW}^2\pi}{4}$ and the quasi-diameter d_{NS} can be derived according Equation 3.2.

$$d_{NS} = \sqrt{\frac{4A_{NS}}{\pi}} \tag{3.2}$$

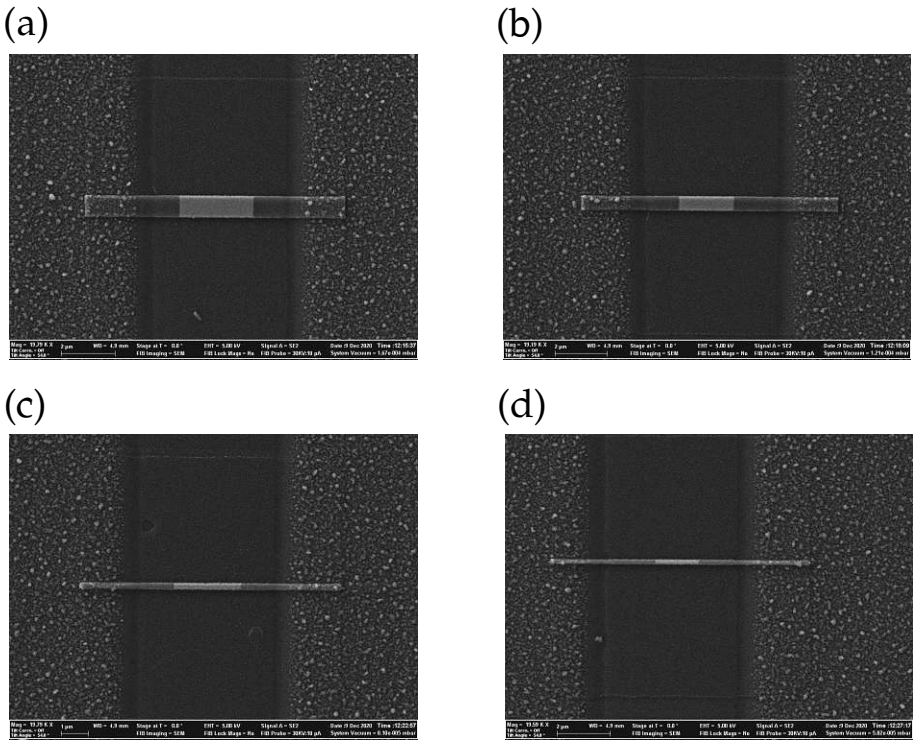

Figure 3.2: *SEM images show four different widths W_{NS} of NSs on a single chip, where in (a) $W_{NS} = 831\,\text{nm}$, (b) $W_{NS} = 541\,\text{nm}$, (c) $W_{NS} = 255\,\text{nm}$ and (d) $W_{NS} = 187\,\text{nm}$. Note that the height h_{NS} equals $75\,\text{nm}$ for all NSs.*

In contrast to the proposed NWs, as shown for example in Figure 2.2, NWs do not have a perfectly cylindrical shape, but have a more hexagonal shape, whereby the edges typically exhibit enhanced oxidation and rounding. Its origin hexagonal shape can be attributed to the growth mechanism of VLS-grown NWs.[100] Due to simplification reasons, in this work the cylindrical representation is used. A major difference from a fabrication and accessibility point of view between NWs and NSs is illustrated in Figure 3.3. As NWs are drop-casted onto the substrate, and are thus distributed randomly, NSs enable an organized placement of the nanostructures. This is enabled by the use of GeOI and a consequent patterning. Therefore, NSs bear a potential for wafer-scale integration.[11]

As briefly mentioned in Chapter 2, for the reliable and comprehensible utilization of nanometer-scaled heterostructures, additional steps are required to passivate the architectures. Therefore, an additional layer, acting as a diffusion barrier for H_2O is deposited around the semiconductor and thus terminates trap states, which highly influence the electrical behavior of the device. In consequence, this prevents degradation and a more controllable electrical behavior of the proposed nanodevices.[73] In the scope of this work the high-κ oxide Al_2O_3 is used for this purpose. In this respect, it needs to be considered that a GeO_x layer is always present although a consequent Al_2O_3 passivation of the NWs is done

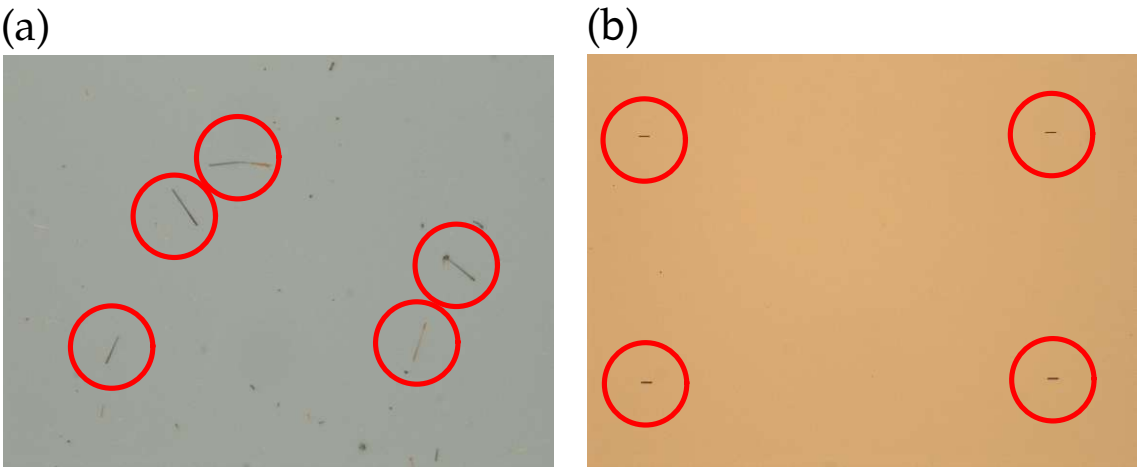

Figure 3.3: *From an integration point of view a remarkable difference is the distribution of the nanostructures, where (a) shows randomly distributed NWs and (b) shows NSs in an order matter.*

directly after the VLS growth without exposure to ambient air.[101] The issue which arises from the GeO_x layer is the high density of trap states which leads (due to charging and discharging processes) to an unreliable electrical behavior of the nanodevice.[74] For NSs the deposition procedure of the Al_2O_3 layer slightly differs. Although, after patterning the GeOI substrate, a fast transition to the ALD chamber for the deposition of the Al_2O_3 is done, the growth of GeO_x cannot be suppressed as the structure is exposed to ambient air for a short time. Therefore, a thin interfacial layer ($\sim$1 nm to 2 nm) of GeO_x needs to be considered for both, the NW- and NS-approach.[74] Figure 3.4 schematically shows the obtained material stack and a TEM image of a passivated Al-Ge-Al NW heterostructure without the GeO_x layer, as it can not be distinguishable visualized.

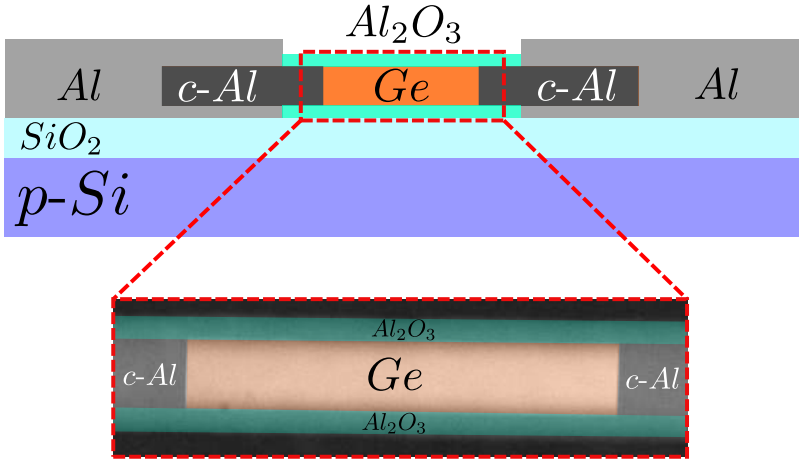

Figure 3.4: *Al-Ge-Al NW heterostructure coated by the indicated Al_2O_3 oxide passivation layer. The bottom illustration shows a colored TEM image of the proposed architecture. The GeO_x layer is not visualized in this illustration.*

Note that in Figure 3.4 the NW-based approach is shown, as the Al_2O_3 coats the complete NW. In contrast, NSs only have the Al_2O_3 passivation layer atop the structure. This fact leads to variations between NWs and NS in the electrical characteristic of the devices. The relevance of the passivation layer as well as of the GeO_x layer is discussed in the following. Surface and oxide traps of the involved oxides (GeO_x and Al_2O_3) are able to shift the semiconductor surface potential and thus can act as local gates due to their capability to be charged or discharged.[51, 74] Especially, the GeO_x layer accumulates charges on the Ge surface, and is hence made responsible to induce charge carrier trapping and de-trapping, which further leads to hysteresis in the I/V-characteristic. Moreover, influencing the channel mobility.[102] Previous experiments showed that the Al_2O_3 passivation layer pushes the band structure to an even more dominant p-type behavior and acting in consequence as acceptor-like traps by increasing the surface potential, and therefore leading to an upwards band bending at the interface.[73, 103] In this context it is also important to consider adsorbates which affect trap states on the surface of the passivation layer.[104] Here, water molecules (H_2O) dissolved in ambient air play an important role. By adsorption on the surface of the nanostructure, these molecules are able to increase the influence of the local gating effect by acting as additional surface charges.[105] Note that other passivation oxides such as e.g. HfO_2 or ZrO_2 tend to be more n-type dominant.[106] A method to overcome these issues could be for instance the removal/desorption of native GeO_x and the subsequent ordered stoichiometric thermal growth of GeO_2 and/or posterior Ge oxy-nitride formation in order to reduce the level of interface states at the dielectric/Ge interface.[12] For any following schematically illustrations of the proposed heterostructures the passivation layer will not be considered due to simplification reasons.

3.1.2 Realization of (SB)FET Devices

By contacting the NWs and NSs, and consequently annealing the structures, they are integrated into a back-gate (SB)FET architecture, which builds the base for all devices in this work. As the name suggests, the doped Si substrate acts as the common back-gate. To comply with the nomenclature in FET technology from now on the two Al contacts are denoted as drain- and source-contact, respectively. By applying a positive or negative voltage at the back-gate, the incorporated bands can be tuned, which is illustrated by the band diagram formalism in Figure 3.5.

The charge carrier transport, respectively the functional mechanism of the back-gate (SB)FET structure can be explained as followed: By applying a positive voltage V_D at the drain-contact, the potential at drain is shifted downwards, leading to an acceleration path for electrons as well as for holes due to a voltage difference V_{DS}. Note that the voltage V_S at the source-contact is kept constant at 0 V. If no back-gate voltage V_{BG} is applied the FET structure will be initially more p-type dominant, as discussed in Sections 2.2.1 and 3.1.1. Applying a voltage V_{BG}, the incorporated bands are tuned as depicted in Figure 3.5b. A positive V_{BG} (here: $V_{BG} = 30$ V) leads to a downwards band bending, and therefore prefers electron injection as illustrated by the red dot at the source-contact. This can mainly be attributed to the thinner barrier and thus enables charge carrier transport

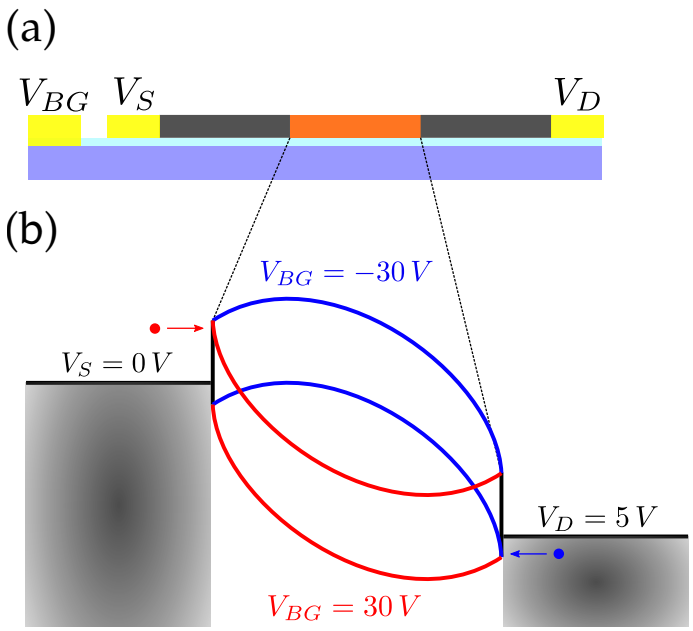

Figure 3.5: *(a) shows a schematic representation of the back-gate (SB)FET architecture with its corresponding voltages. The band diagram formalism is used to describe the charge carrier transport, as shown in (b). The values are examples and depend on the geometrical dimensions of the material stack.*

through tunneling. However, applying a negative V_{BG} (here: $V_{BG} = -30\,\mathrm{V}$), the bands are getting bend upwards and in consequence favour p-type conduction. Due to the Fermi level pinning close to the valence band, a good hole injection is possible.[83] Additionally, the Schottky barrier for holes gets thinner, whereas in contrast the overall barrier height for electrons increases. By utilizing the presented band diagram formalism most gating phenomena on (SB)FET structures can be explained in a good pictorial way.
Due to the relative thick back-gate oxide (100 nm SiO_2 for the NW-approach and 150 nm SiO_2 for the NS-approach), high back-gate voltages V_{BG} need to be applied for a proper gating mechanism. To overcome this issue the concept of top-gates is utilized. This allows to reduce the gate voltage, as a more controllable formation of the top-gate oxide (here: (22 nm Al_2O_3) can be fabricated. Thus, leading to a comparable electrostatic gating effect. Moreover, top-gates allow to tune the bands at dedicated positions within the incorporated energy bands. In a first step investigations on test structures were done to evaluate the minimum gap between two top-gates placed next to each other. It was shown that a distance of 200 nm needs to be guaranteed to fabricate reliable top-gate contacts. Figure 3.6 shows SEM images of a 150 nm and a 200 nm gap test structure.

For the actually fabricated devices Ω-shaped top-gates were fabricated using a combination of EBL, Ti/Au evaporation (8 nm Ti, 125 nm Au) and lift-off techniques. Figure 3.7 gives an overview of a two independent top-gate device and also illustrates the band bending mechanism in the case of two separated top-gates. In this representation of the band

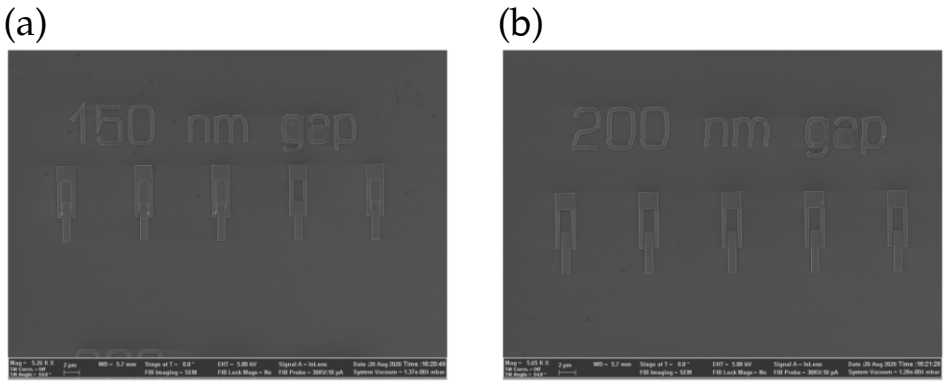

Figure 3.6: *The test structure shown in (a) with a gap size of* 150 nm *shows lift-off errors, and thus leading to short-circuits, whereas the test structure in (b) with a gap size of* 200 nm *showing sufficiently wide distances.*

diagram formalism, the back-gate voltage V_{BG} is set to 0 V due to simplification reasons.

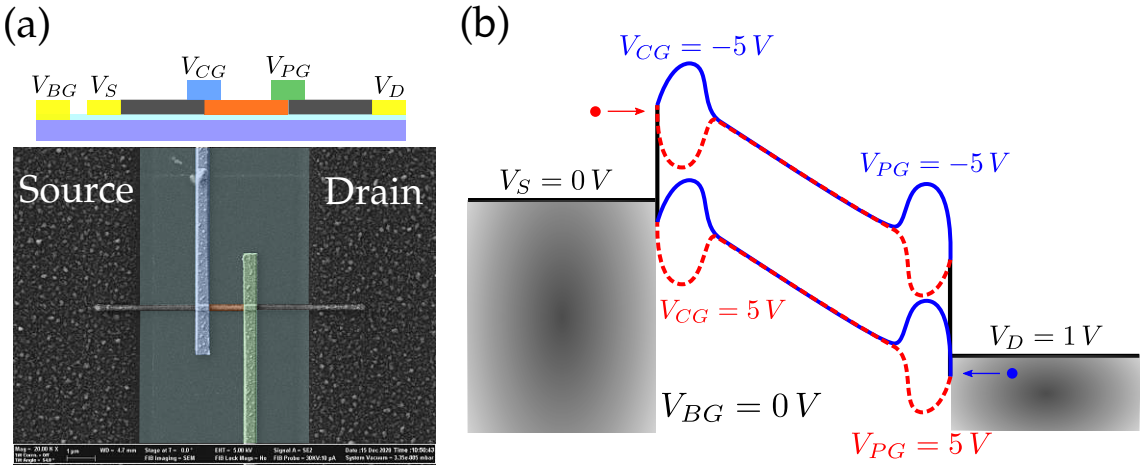

Figure 3.7: *(a) illustrates the schematic of a two independent top-gate device with corresponding voltages. Additionally, a colored SEM image illustrates the actually fabricated device. (b) reveals the functional mechanism of the device, where V_{PG} allows to set n- or p-type operation.*

As it can be deduced from the band diagram in Figure 3.7b, the two independent top-gate device compromises a concept for RFETs, as shown in Section 2.3.1. Setting V_{PG} correspondingly, n- or p-type operation can be programmed. The back-gate voltage V_{BG} is set to 0 V. Therefore, no additional band bending is evident. Moreover, V_{CG} is kept constant 0 V as well, as this gate is merely used to turn the transistor on and off. Finally, it can be obtained that V_{PG} is responsible to switch between electron or hole injection. Additionally, a consequent suppression of the undesired charge carrier type can be deduced. In this work various top-gate architectures are considered, which rely on the mechanism of electrostatically tune the incorporated bands of the proposed Al-Ge-Al heterostructures.

A summary of different top-gate architectures is given in Appendix A.

At first sight a thin NS with a comparable quasi-diameter does not appear to highly differ from its NW counterpart. However, due to a different oxide composition, the following two issues need to be considered.

- The total length of NWs is coated by the Al_2O_3 passivation layer, whereas only the top surfaces of NSs are covered by Al_2O_3. Thus, leading to a variation of the back-gating mechanism and the surface trap landscape.

- Due to the application of RIE, the surface of NSs is rougher than the surface of VLS-grown NWs. This leads to an un-steady surface of the NSs, and in consequence to a variation of the oxide thickness of the top-gate oxide. Hence, causing differences of the top-gating mechanism between NWs and NSs.

These differences as well as the geometrical variation of NWs and NSs get obvious within electrical characterization measurements, as discussed throughout Chapter 4.

3.2 Electrical Characterization

This section is dedicated to the measurement equipment and methods to verify the functionality and capability of the obtained devices. Here, special attention is given to characterization methods commonly used in FET technology. Firstly, in Section 3.2.1 the utilized measurement setup including the probe station and analyzer is presented. The following sections are then dedicated to the characterization techniques. Most of them are extracted in accordance to the book "Semiconductor Material and Device Characterization" by D.K. Schroder.[107] If not other stated, this book was used as reference. Beginning with Section 3.2.2, the evaluation of the output characteristic of FET devices, which in combination with thermal measurements is further used to extract the eSBH, is presented. The determination of the eSBH is then discussed in Section 3.2.3. The other major characterization method for FETs is the analysis of the transfer characteristic, which is described in Section 3.2.4. Utilizing the transfer characteristic, the transconductance g_m as well as the threshold voltage V_{TH} can be extracted. These topics are discussed in Section 3.2.5.

3.2.1 Measurement Equipment

Due to a wide range of performed measurements, two different setups were utilized in the scope of this work. In general, they can be divided into a probe station part and an analyzer part. Figure 3.8 shows images of the two probe stations, where Figure 3.8a shows the Karl Suss setup, which was mainly used for measurements at ambient conditions and for first investigations after fabrication. Figure 3.8b shows the cryogenic Lakeshore PS-100 probe station, which is capable to perform measurements in vacuum. Moreover, with its in-built thermal control stage, it allows to set reliable temperatures. In contrast,

the Karl Suss probe station is equipped with a self-built heating stage without a regulated temperature controller.

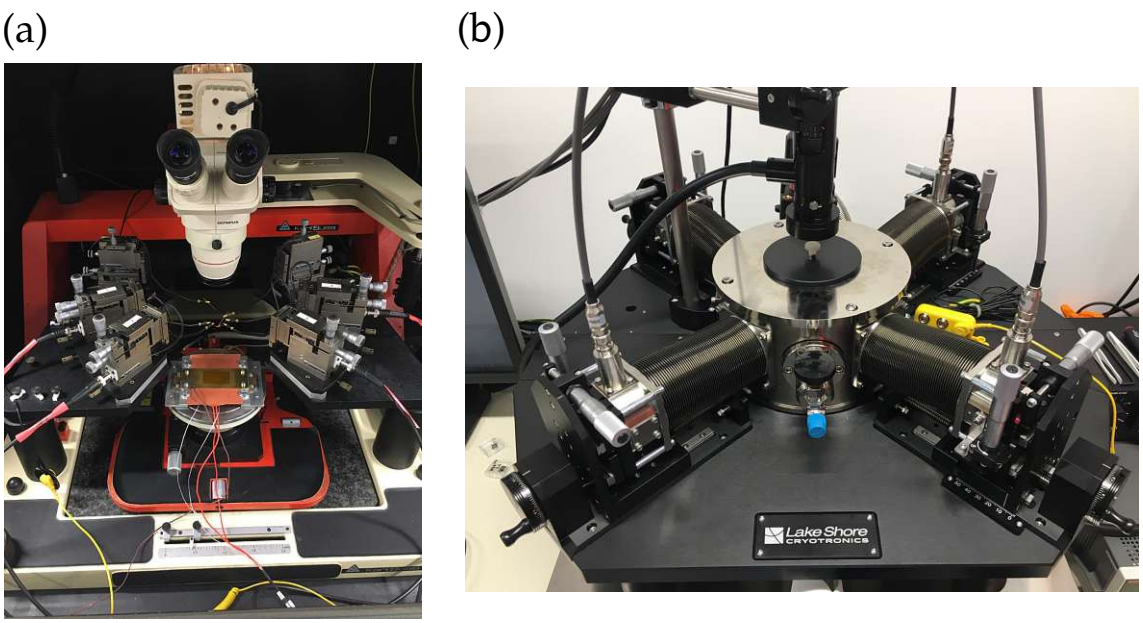

Figure 3.8: *Needle probe stations used in the scope of this work, where (a) shows the Karl Suss setup with the self-built heating stage and (b) the cryogenic Lakeshore PS-100 probe station. The Lakeshore setup is capable to perform measurements in vacuum and has an in-built thermal control stage.*

For electrical measurements, the Karl Suss setup is equipped with a HP 4156B semiconductor analyzer, which comes with four Source-Measure-Units (SMUs) and two Voltage-Source-Units (VSUs). SMUs are capable to apply a voltage and measure the current, whereas VSUs are only able to apply a certain voltage without any measurement possibilities. The cryogenic Lakeshore PS-100 probe station is equipped with a Keysight B1500A, and has four SMUs. Besides a more user-friendly and graphical user interface, the semiconductor analyzer has the same measurement capabilities as the HP 4156B analyzer.

3.2.2 Output Characteristic

The output characteristic of a FET is recorded by sweeping the drain voltage V_D and keeping the source voltage V_S constantly at 0 V. Thus, leading to a voltage difference V_{DS}, and therefore initiating a current I_D through the channel. This results in an I/V characteristic – I_D *versus* V_D. The back- or top-gate voltage(s) is kept at a constant value, and hence allows to characterize the device in a specific operation mode. By analyzing the shape (linear *versus* exponential) of the output characteristic at low V_{DS}, it is possible to evaluate the thermionic and tunneling emission of the charge carrier transport through the Schottky barrier. In the FET community it is common to plot the current I_D on a linear axis; n-type conduction in the first quadrant and p-type conduction in the third

quadrant of a xy-coordinate system.[42] In the scope of this work, also logarithmic plots were used to explicitly visualize the sub-threshold slopes (SS) and for better visualization of the transport regimes. As briefly depicted, gathering thermal-dependent output characteristics allows to determine the eSBH by additional evaluation methods presented in Section 4.2.
Another relevant feature which can be extracted from this I/V characteristic is the hysteresis behavior of the proposed devices. To analyze this characteristic a forwards sweep, e.g. sweeping V_D from $-4\,\mathrm{V}$ to $4\,\mathrm{V}$, followed by an immediate backwards sweep e.g. V_D from $4\,\mathrm{V}$ to $-4\,\mathrm{V}$, needs to be performed. As the GeO_x layer between the Ge channel and the Al_2O_3 passivation layer accumulates charge carriers due to trapping, a forwards sweep charges or discharges trap states, whereas a backwards sweep is then influenced by the change of the involved trap states, and therefore shows a different I/V-characteristic. Moreover, other trapping effects, e.g. adsorbates on the Al_2O_3 layer, also impact this behavior. For the visualization of the hysteresis, both, the forwards and backwards sweeping result need to be plotted.
Special attention needs to be given to top-gated devices, and especially to NDR devices, as sufficiently high electric fields – which result in relatively high drain-voltages, need to be applied, and thus may harm the involved oxides, which in worst-case damage the device. As a rule of thumb a maximum voltage of $1\,\mathrm{V}$ per $100\,\mathrm{nm}$ L_{Ge} can be applied, ensuring that the break-down field of $E_C = 100\,\mathrm{kVcm^{-1}}$ for bulk Ge is not exceeded.[42] The determination of the maximum gate voltages was evaluated experimentally after the fabrication, as the quality of the oxide highly influences this performance metric.[5] Due to the relatively thick back-gate oxide, a maximum gate voltage of $V_{BG} = 30\,\mathrm{V}$ can be applied for NW-based devices ($100\,\mathrm{nm}$ SiO_2), whereas $V_{BG} = 50\,\mathrm{V}$ for NS-based devices ($150\,\mathrm{nm}$ SiO_2).

3.2.3 Effective Schottky Barrier Height Measurement

In the work "Metal-Semiconductor Contacts" by E.H. Rhoderick and R.H. Williams various approaches for the extraction of the Schottky barrier height are discussed.[61] Note that the C/V- and I/V-method are mostly utilized for metal-semiconductor interfaces, whereas according D.K. Schroder the C/V-method is mainly used for doped Schottky contacts.[107] As in this work intrinsic Ge is used, the I/V(-T) approach is utilized, which relies on the thermionic emission theory. In general, this theory is valid for barrier heights larger than k_BT ($25.7\,\mathrm{meV}$ at $T = 300\,\mathrm{K}$) and small bias voltages to avoid barrier lowering, and thus significant tunneling currents. Moreover, the potential between the metal and semiconductor needs to be taken into account as well. In the scope of this work the standard $J(T, E)$ model for Schottky contacts cannot be utilized straight-forward, as the used Al-Ge-Al heterostructure does not fully compromise these boundary conditions. Nevertheless, the model can be utilized to get an approximation of the eSBH, which means that the total activation energy for the injection of charge carriers can be evaluated experimentally. The total activation energy includes contributions, which can be attributed to thermionic as well as tunneling emission. Moreover, in the proposed heterostructures two Schottky contacts are involved (see Figure 3.4). In the standard $J(T, E)$ model for,

i.e. Schottky diodes, the potential between the metal and doped semiconductor can be directly measured, whereas for SBFETs the electrostatic situation is much more complex because the potential at the semiconductor region cannot be directly determined by static electrical measurements. Different from a Schottky diode, the semiconductor potential depends on the applied gate- and drain-voltages and also on the accumulated charges inside the active region. In addition, the presence of the second Schottky barrier, i.e. at drain makes the calculation of the barrier height more complex, because within a given potential landscape, injection of holes from the drain junction can become considerable, especially for small-band gap semiconductors, such as Ge. Taking these given boundary conditions into account it is not possible to apply the physically correct expression. Therefore, only a rough estimation of the total effective activation energy of the system can be given. According E.H. Rhoderick and R.H. Williams the current through the Schottky barrier can be simplified in the case that the applied bias voltage exceeds $3k_BT/q$ (76 mV at $T = 300\,\mathrm{K}$). Equation 3.3 gives the simplified equation based on thermionic emission theory for the evaluation of the total effective activation energy. This model was used for the evaluation of the eSBH and will be considered from now on. Note that previous published works promote this model for determining the total effective activation energy.[108, 109]

$$J_{\mathrm{TE}}(T) = A^* T^2 \exp \frac{-q\phi_{\mathrm{eSBH}}}{k_B T} \tag{3.3}$$

where J_{TE} is the measured current density through the device, A^* is the effective Richardson constant, T is the corresponding temperature and $(q)\phi_{\mathrm{eSBH}}$ is the total effective activation energy, which is interpreted as the effective barrier height. Without knowing the exact value of A^* the total effective activation energy can be extracted by measuring the I/V-characteristic at different temperatures and applying the natural logarithm to extract the barrier height of the previous equation. Equation 3.4 shows the then obtained expression.

$$\ln \frac{J_{\mathrm{TE}}}{T^2} = \ln A^* - \frac{q\phi_{\mathrm{eSBH}}}{k_B T} \tag{3.4}$$

Thus, by plotting $\ln \frac{J_{\mathrm{TE}}}{T^2}$ (y-axis) as a function of $1000/T$ (x-axis), a so-called Richardson plot is obtained. Using the linear equation and setting the factors of the above equation correspondingly to $y = kx + d$, the individual parameters can be extracted. In the linear equation, d depicts the (natural logarithm) effective Richardson constant A^*. Hence, enabling to determine this parameter by evaluating the cross-point on the y-axis. Due to the simplified model used in the scope of this work, the extraction of A^* is not possible, as other unknown factors as the potential between the metal and semiconductor as well as the electron mass, are neglected. By analyzing the slope k the corresponding $q\phi_{\mathrm{eSBH}}$ can be determined for a specific drain bias voltage V_D as depicted in Equation 3.5.

$$q\phi_{\mathrm{eSBH}} = -k * k_B * 1000 \tag{3.5}$$

where k is the evaluated slope of the Richardson plot. Finally, $q\phi_{\mathrm{eSBH}}$ can be plotted over V_D for the evaluation of the total effective activation energy. Extrapolation of the data points to $V_D = 0\,\mathrm{V}$ is used to perform a careful estimation of the activation energy then, including initial effects of barrier lowering and tunneling at the tip of the barrier.

To plot and calculate the total effective activation energy a Python script written in this thesis was used, which allows to automatically determine the relevant values by merely feeding it with I/V measurements (I_D over V_D) at different temperatures. Measurement results and plots are thoroughly discussed in Section 4.2.

3.2.4 Transfer Characteristic

The transfer characteristic illustrates the gate-response of the transistor for a given bias voltage. Thus, allowing to determine the on- and off-current of the devices. In the scope of this work, transfer characteristics were evaluated for back-gate devices by sweeping the back-gate voltage V_{BG} and for top-gate devices by sweeping the control-gate V_{CG}. The drain voltage $|V_D|$ is kept at a constant value $>0\,\mathrm{V}$. Again, the actually applied voltages highly depend on the geometry of the devices as well as on the utilized oxides. In consequence, the drain current I_D changes accordingly, and therefore determines the on- and off-current. Moreover, transfer characteristics are an important tool for the evaluation of the SS.
Also, the transfer characteristic exhibits hysteresis, when a forwards and backwards sweep is done accordingly. Due to the application of relatively high voltages at the gate contacts, high energy trap states can be affected, i.e. fixed charges in the oxide, which result in higher time constants in comparison to interface trap states.[110] Therefore, special attention needs to be given to the measurement of the transfer characteristic, and especially when sweeping the back-gate voltage V_{BG}, as the relatively high capacitance of the back-gate contact needs to be considered as well. In this context time constants need to kept in mind.

In conclusion, the transfer characteristic is an important method to determine on- and off currents and their transition rates, expressed by the SS in mV/decade. Moreover, by analysing the transfer characteristic it allows to evaluate the transconductance g_m and the threshold voltage V_{TH} of the proposed transistors.

3.2.5 Extraction of the Threshold Voltage

According D.K. Schroder various approaches are utilized for the extraction of the threshold voltage V_{TH}.[107] In this work, the threshold voltage is merely evaluated for devices, which are operated as RFETs due to its relevancy. Here, a combination of two methods is used. Firstly, the transconductance g_m was obtained by calculating $g_m = \mathrm{d}I_D/\mathrm{d}V_{CG}$, where the corresponding data are extracted from the transfer characteristic. Afterwards, the vertical intersection of the peak transconductance and the transfer characteristic is determined. At this interception a tangent approximation at the transfer characteristic is set to evaluate the corresponding threshold voltage V_{TH}, which can be extracted at the intersection with the x-axis (V_{CG}). Measurement results and the actually extraction of the transconductance g_m and the threshold voltage V_{TH} are discussed in the RFET sections in Chapter 4.

Chapter 4

Results and Discussion

This chapter presents the conducted experiments and the actual realization of RFETs and/or NDR devices, which base on the theory presented in Chapter 2 and the characterization methods in Chapter 3. If not other stated, all measurements were conducted at ambient conditions at $T = 295\,\mathrm{K}$. In a first step the back-gate FET architecture is discussed in Section 4.1, directly followed by the evaluation of the eSBH for different device architectures in Section 4.2. Afterwards, the road to a functional Ge-based NW RFET is presented in Section 4.3. These investigations lead to profound insights on the utilized architectures and allow the realization of NDR devices, as presented in Section 4.4. Ultimately, the two concepts are merged within a new type of device, the "NDR-mode RFET", which is discussed in Section 4.5. Finally, the RFET-concept is transferred to GeOI substrates, and thus demonstrates its functionality on NSs. This is depicted in Section 4.6. The gathered FOMs of the presented RFETs are finally compared with existing RFETs in Section 4.7.

4.1 Back-gate FET Architecture

As the back-gated FET architecture builds the base for all devices in this work, this concept is considered prior the realization of actual devices. By evaluating its characteristic and extracting FOMs, important insights can be gained in correspondence to the used Al-Ge-Al heterostructures. Figure 4.1 shows a schematic illustration of a back-gated device with its corresponding voltages. Additionally, the band bending mechanism is illustrated in Figure 4.1a. Figure 4.1b shows the transfer characteristics of five back-gate NW-devices with different d_{NW} and L_{Ge}.

Due to the Fermi level pinning close to the valence band as well as the incorporated acceptor-like traps, all five NW-based heterostructures show a dominant p-type behavior. However, the curves can be classified into two different sets as depicted in Figure 4.1b,

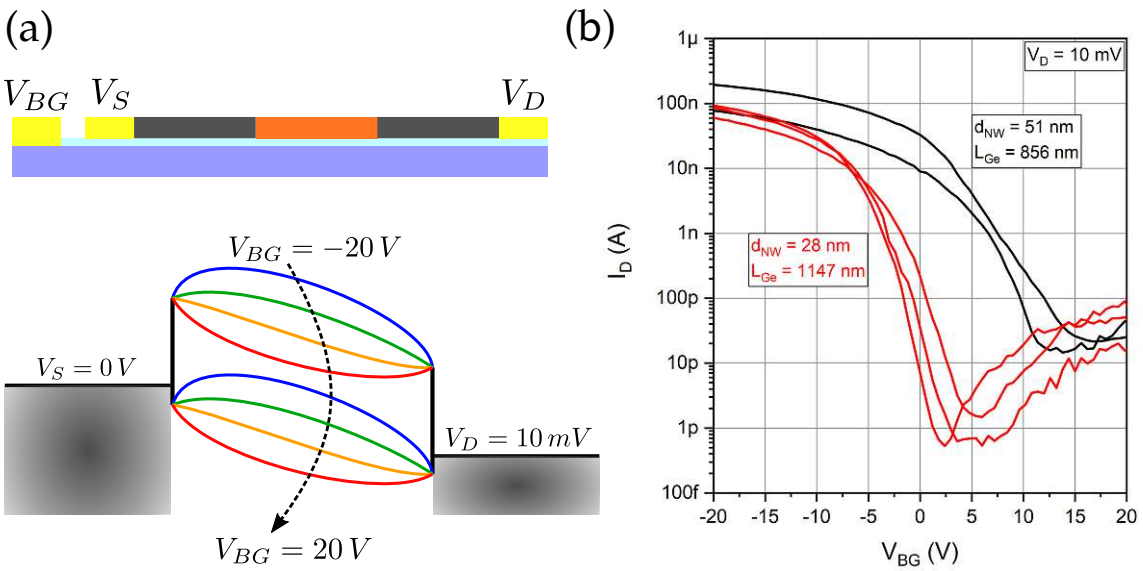

Figure 4.1: *In (a) the schematic with the corresponding voltages is shown, whereas in the bottom part of (a) the band diagram is illustrated. The transfer characteristic of five different NW-based heterostructure devices is shown in (b). It depicts the typical p-type dominant behavior of Al-Ge-Al heterostructures.*

where the red curves show measurements of NWs with an average d_{NW} of 28 nm and a L_{Ge} of 1147 nm. The black curves show measurements of NWs with an average d_{NW} = 51 nm and L_{Ge} = 856 nm. The longer, and therefore thinner NWs (red curves) show a dedicated ambipolar behavior with the intrinsic point close to 0 V, whereas shorter and thicker devices exhibit the intrinsic point at higher back-gate voltages (here: V_{BG} = 13 V). This phenomenon can be attributed to the fact, that the total surface area of the thicker NWs is approximately 40 % higher, and thus exhibits a higher density of surface trap states. Additionally, the volume of the thicker NWs is one order of magnitude higher, leading to a higher density of oxide traps. Thus, resulting in a shifted transfer characteristic due to local gating mechanisms.[74] Moreover, this fact directly influences the SS. Thicker wires show a SS of 6600 mV/decade, whereas thinner wires exhibit a SS of 1600 mV/decade. Evaluating the current at the intrinsic point, the off-state current density J_{OFF} can be deduced. For the thicker NWs J_{OFF} was determined to be one magnitude higher in comparison the thinner and longer wires. This again can be attributed to the local gating mechanism caused by trapping effects. Another important insight, which can be obtained from Figure 4.1b is the noisier current in the n-type regime at V_{BG} >0 V. This fact is attributed to the relatively large barrier for electrons, which causes stronger scattering effects due to a higher contribution of tunneling.[111] As depicted the utilized Al-Ge-Al system exhibits a high density of trap states, which act as local gates. Figure 4.2 shows the hysteresis behavior induced by these trap states.

It can be concluded that the first sweep of the back-gate voltage V_{BG} from −20 V to 20 V

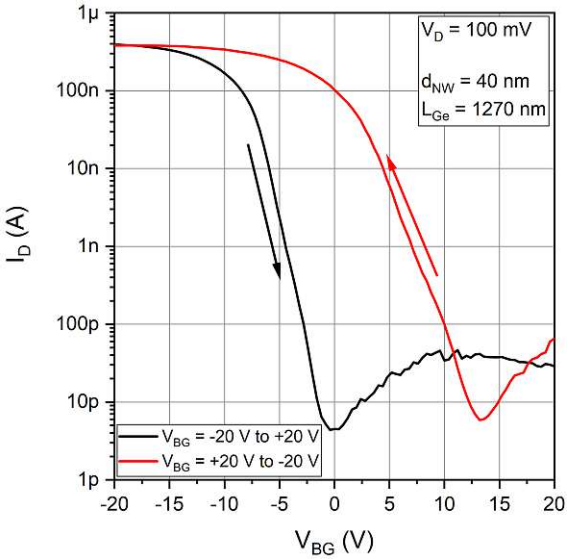

Figure 4.2: *During the first V_{BG} sweep from $-20\,\mathrm{V}$ to $20\,\mathrm{V}$ the presented device shows an ambipolar characteristic with the intrinsic point at $V_{BG} = 0\,\mathrm{V}$. A second sweep right afterwards shows a shift of the intrinsic point to $V_{BG} = 13.2\,\mathrm{V}$.*

causes changes of the charge state of involved traps, whereas a consequent backwards sweep from $20\,\mathrm{V}$ to $-20\,\mathrm{V}$ then shows a shift of the intrinsic point. This can be attributed to trap states, which get charged or discharged during the first sweep. Thus, leading to a hysteresis of the transfer characteristic. Due to a relatively high surface exposure to air, the hysteresis of back-gate devices is more distinct as for top-gate devices. To overcome this issue, fast and pulsed measurements of the back-gate voltage V_{BG} shall be applied. Hence allowing to minimize this effect by consequently setting the charge states to their initial states. Moreover, measurements in vacuum improve the hysteresis behavior. A more sustainable solution is to get rid of the GeO_x layer, which is mainly responsible for this behavior. This can be done, e.g. by desorption prior the Al_2O_3 deposition.
For a better understanding, temperature dependent measurements were conducted to analyze the charge carrier transport at elevated temperatures. A representative NW is used for measurements in Figure 4.3, where (a) shows the transfer characteristic and (b) shows the output characteristics for p-type conduction ($V_{BG} = -5\,\mathrm{V}$) and n-type conduction ($V_{BG} = 15\,\mathrm{V}$), respectively.

It is evident that the off-state current is increasing with elevated temperatures, as electrons are getting thermally excited and therefore contribute to the current I_D. The J_{OFF} at $T = 295\,\mathrm{K}$ was determined to be $0.046\,\mathrm{A/cm^2}$. This phenomena can also be observed for n-type conduction at $V_{BG} > 5\,\mathrm{V}$, which is consistent with semiconductor theory.[42] Interestingly, for p-type conduction at $V_{BG} < 5\,\mathrm{V}$ the current I_D even decreases with higher temperatures, as shown in the left plot of Figure 4.3b. This can be attributed to a decreasing total effective activation energy (eSBH) for the injection of holes. Further discussions are

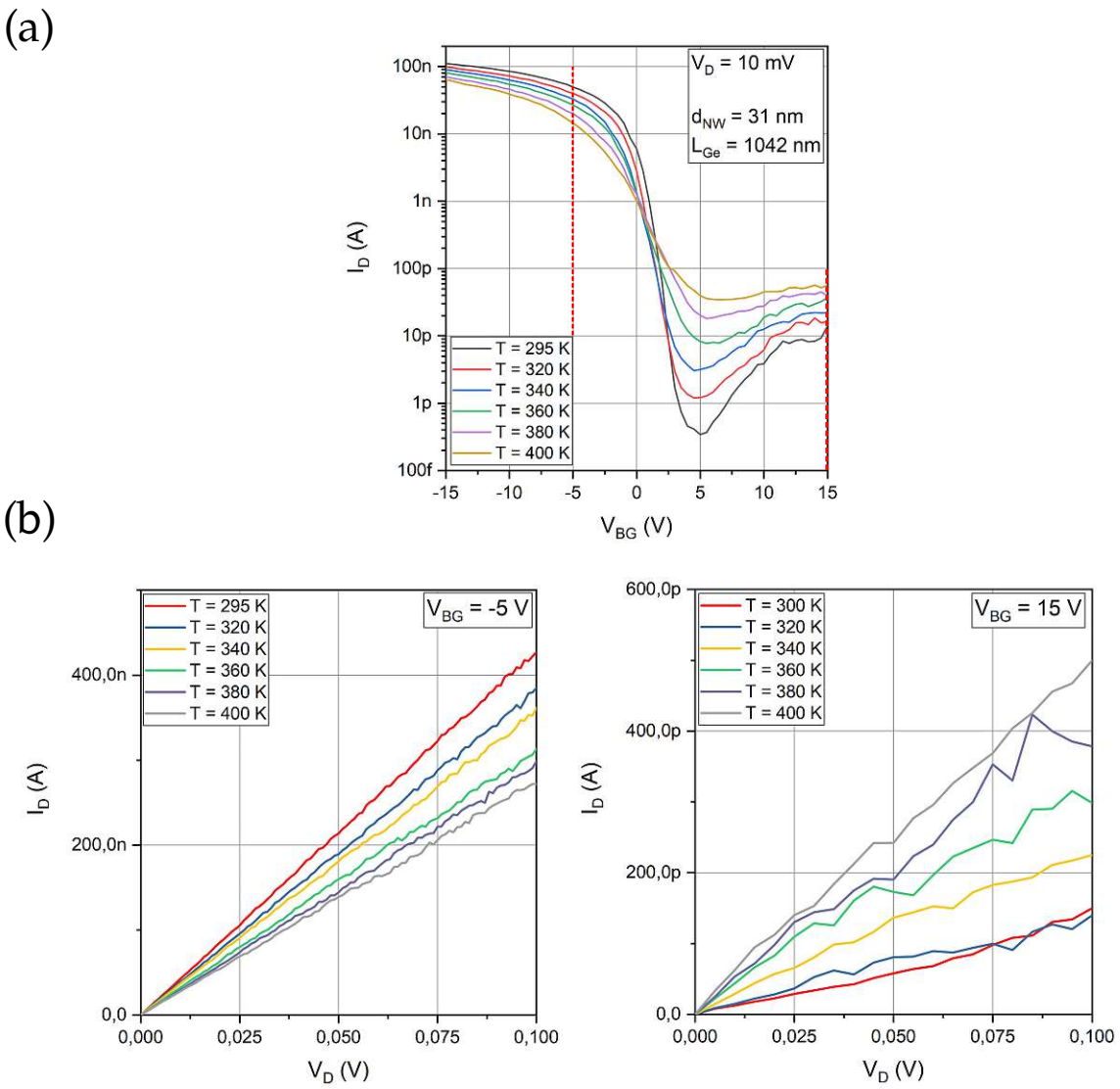

Figure 4.3: *(a) shows temperature-dependent transfer characteristics from $T = 295\,\mathrm{K}$ to $T = 400\,\mathrm{K}$. The vertical dashed lines indicate V_{BG}, at which the output characteristics (b) for p- and n-type conduction are measured.*

addressed in detail in Section 4.2. For NSs the transfer and output characteristic show similar results from a transport mechanism point of view. However, the SS has higher values and the intrinsic points are more shifted. The higher SS can be attributed to the fact that NSs have a thicker quasi-diameter d_{NS} and thus worse gating capabilities than NWs. By considering the height $h_{NS} = 75\,\mathrm{nm}$ and the width W_{NS} of the NSs the quasi-diameter d_{NS} was calculated according Equation 3.2. Figure 4.4 shows the transfer characteristics of two similar NS devices.

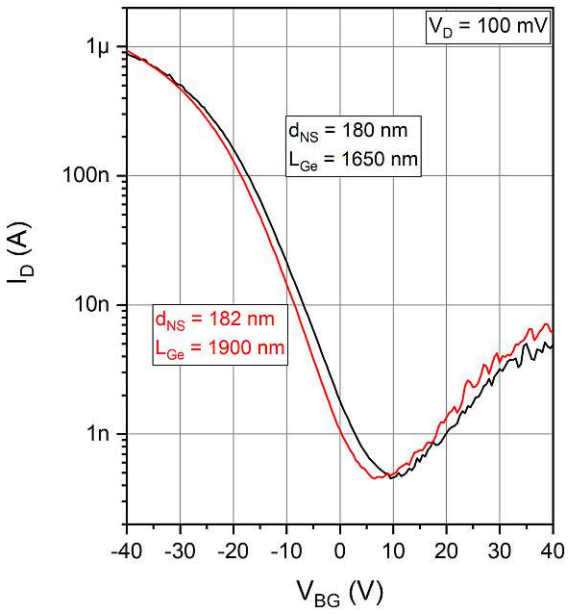

Figure 4.4: *Transfer characteristic of NSs with a quasi-diameter* $d_{NS} = 180\,\text{nm}$ *and* $182\,\text{nm}$. *The SS is less steep and the intrinsic point is shifted to positive* V_{BG}, *as relatively thick sheets are used.*

As expected the SS increases to a value of SS = 10 000 mV/decade due to the relatively thick quasi-diameter d_{NS} in comparison to the NW-based device shown in Figure 4.3. Note that a higher drain-voltage V_D was applied due to the fact that the utilized NSs are longer than the back-gated NWs. The NSs investigated in Figure 4.4 exhibit a J_{OFF} of $1.165\,\text{A/cm}^2$ at $T = 295\,\text{K}$, which is comparable with the off-current densities of the thicker NWs presented in Figure 4.1. Note that for the NSs a V_D of 100 mV was applied. To investigate the trapping properties of NSs, the hysteresis of the transfer characteristic is depicted in Figure 4.5.

It can be concluded that the missing GeO_x-Al_2O_3 interface at the bottom of NSs is responsible for the less pronounced hysteresis effect. Nevertheless, a hysteresis can be observed and thus shows the presence of trap states at the top GeO_x-Al_2O_3 interfaces as well as in the oxide. Moreover, defects induced by etching need to be considered for NSs.[10] Also NSs exhibit a positive shift of the intrinsic point from its initial V_{BG} of 0 V to a V_{BG} of 10 V.
The presented results depict an ambipolar transport mechanism of back-gate devices, allowing the conduction of electrons and holes. However, both regimes are highly asymmetric. This fact can be attributed to different injection capabilities of electrons and holes as well as different band bending mechanisms. Its influence on the energy bands is mainly determined by Ge and the used oxide stack, which promote a more pronounced p-type conduction.[112] In the following section, the injection capability of charge carriers is analyzed in detail.

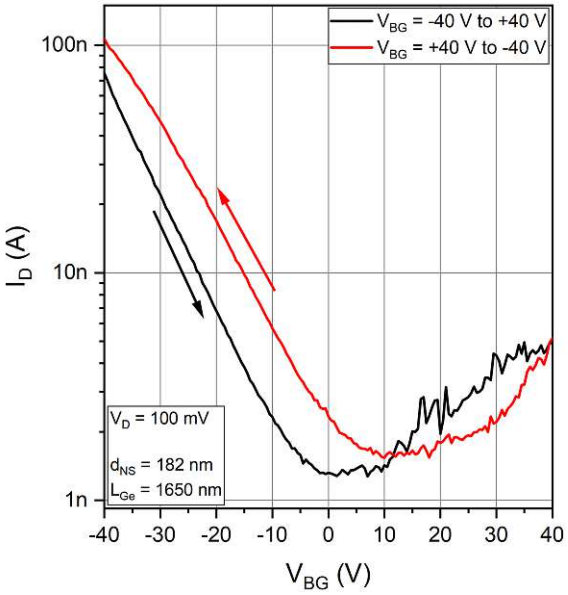

Figure 4.5: *In comparison to the hysteresis exhibited by NWs, the hysteresis of NS-based devices is much less pronounced. This can be attributed to the missing GeO_x-Al_2O_3 interface at the bottom of the NSs.*

4.2 Extraction of the Effective Schottky Barrier Height

The extraction of the eSBH, also denoted as total effective activation energy, is determined for NW- and NS-based Al-Ge-Al heterostructures. Analyzing the eSBH allows to describe the asymmetric transfer characteristic of the proposed device architectures, and additionally gives an experimental approach to quantitatively describe the injection capability of charge carriers into the Ge segment. Considering the effective barrier height, the term "eSBH" is used. In the case that the injection capability is discussed, the term "total effective activation energy" is considered and is denoted as E_{SB} in the shown figures of this section. Therefore, a membrane device with no gate (Section 4.2.1), a back-gate device (Section 4.2.2) and a global top-gate device (Section 4.2.3) are considered. The derivation and measurement procedure is explained in detail in Section 3.2.3.

4.2.1 Membrane Device

For first investigations of the eSBH, data of a NW placed on a Si_3N_4 membrane were used. This allows to exclude any influence of the gate contact, and therefore enables a more sophisticated way to extract the intrinsic effective barrier height of the Al-Ge system. Figure 4.6 shows the schematic illustration of the architecture and a SEM image of the proposed membrane device as well as relevant plots for the deduction of the eSBH.

According the I/V characteristic in Figure 4.6b, the un-gated NW shows a typical diode characteristic. Moreover, with increasing temperatures, the current increases, which is

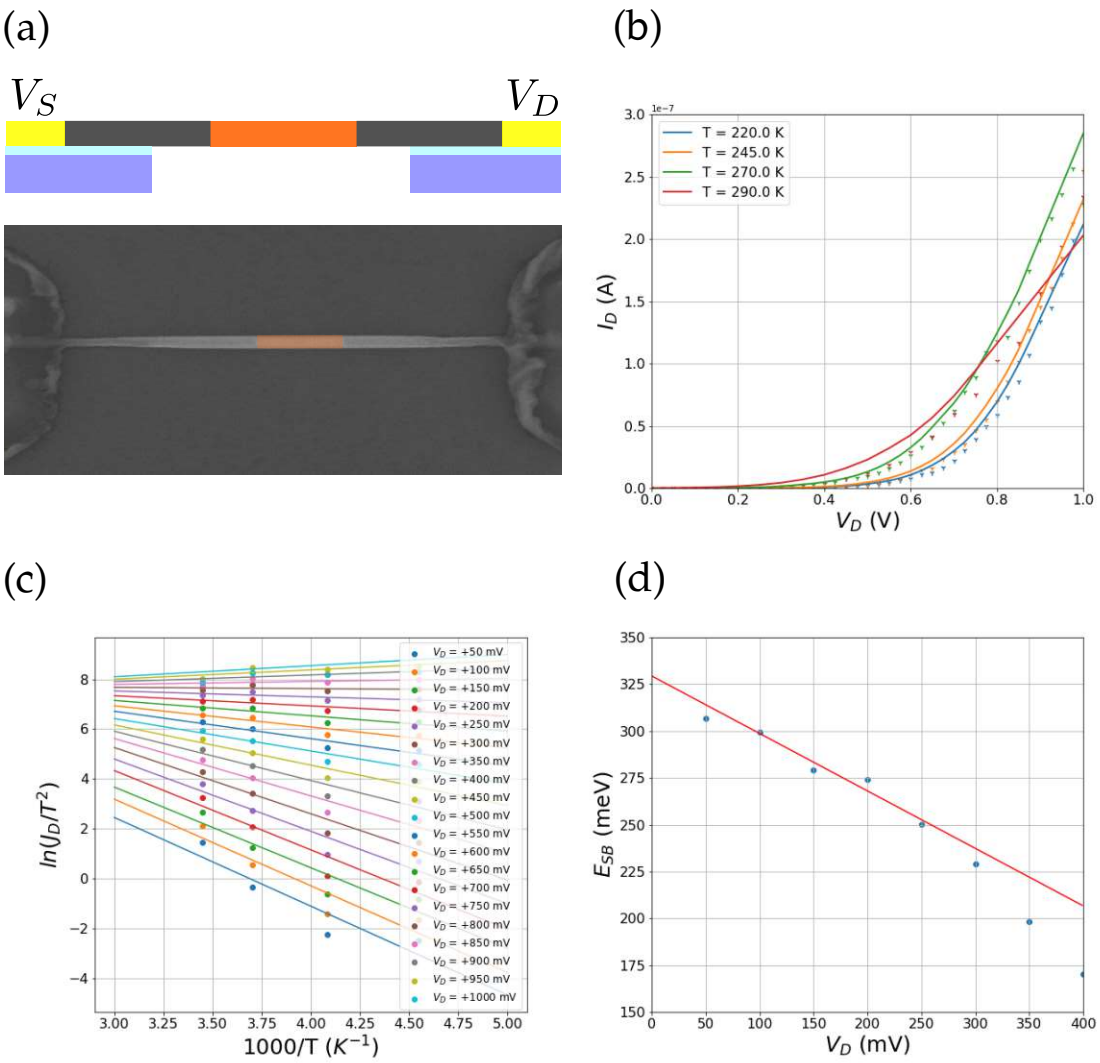

Figure 4.6: *The placement of the NW on a membrane allows to exclude any gating effects, as shown in (a). Following the procedure to obtain the eSBH (see Section 3.2.3), temperature dependent I/V characteristics were measured as shown in (b). By plotting the Richardson plot, shown in (c), the slopes can be extracted, which further lead to the total effective activation energy, denoted as E_{SB} in (d).*

in perfect agreement with semiconductor theory.[42] Thus, leading to negative slopes in the Richardson plot and further results in a positive total effective activation energy of 329.5 meV, which is evaluated by a linear fit as denoted by the red curve in Figure 4.6d. In theory, the SBH for bulk Al-Ge Schottky junctions was determined to be 200 meV.[15] The difference of 129.5 meV is caused by the fact, that the potential between the metal and semiconductor is neglected. Moreover, it is not considered, that two Schottky barriers are involved in the proposed Al-Ge-Al system. Nevertheless, the obtained value of 329.5 meV

can be utilized as a reference at the intrinsic point for gated devices.

4.2.2 Back-Gate Device

As the focus is set to the realization of RFETs, and thus to the injection and suppression capabilities of charge carriers, the total effective activation energy is evaluated in dependence of the gate-voltage. Therefore, in a next step the eSBH for a representative NW-based back-gate device was obtained. For any gated device the transfer characteristic needs to be evaluated prior to the extraction of the activation energy. This allows to identify the intrinsic point as well as dominant n- and p-type operation regimes. Due to consistency reasons the same device as shown in Figure 4.3 is reconsidered, and the corresponding points are identified accordingly, where $V_{BG} = -5\,\mathrm{V}$ is used to evaluate the activation energy for hole injection, $V_{BG} = 5\,\mathrm{V}$ for the intrinsic point and $V_{BG} = 15\,\mathrm{V}$ indicating the n-type operation. Figure 4.7 shows the transfer characteristic at $T = 295\,\mathrm{K}$ with the corresponding gate-voltages.

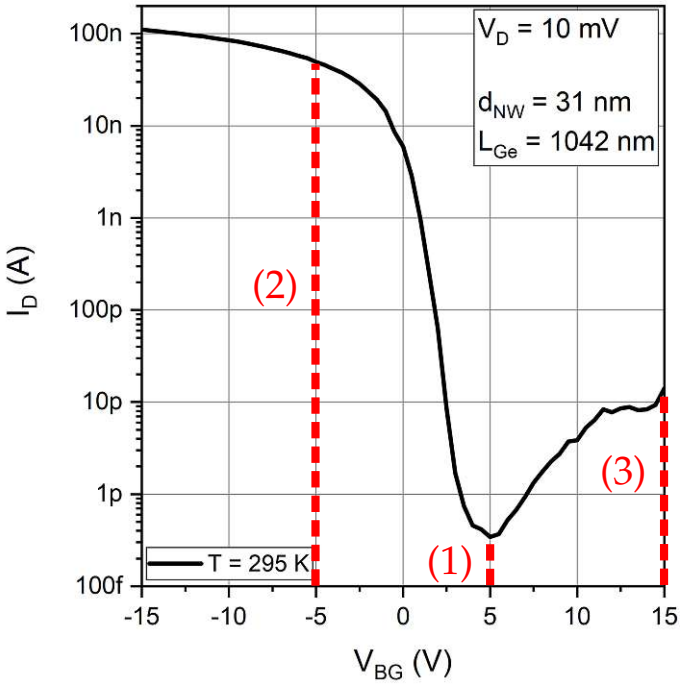

Figure 4.7: *The transfer characteristic of a NW-based back-gate device indicates (1) the intrinsic point at $V_{BG} = 5\,\mathrm{V}$, (2) the dominant p-type operation at $V_{BG} = -5\,\mathrm{V}$ and (3) the dominant n-type operation at $V_{BG} = 15\,\mathrm{V}$.*

For the evaluation of the actual activation energies at the stated gate-voltages, the same procedure as shown in Figure 4.6 was used. Table 4.1 gives an overview of the thereof evaluated energies at the three relevant regimes.

Remarkably, the intrinsic point at $V_{BG} = 5\,\mathrm{V}$ shows a similar activation energy as the

$\mathbf{V_{BG}}$	$-5\,\mathrm{V}$	$5\,\mathrm{V}$	$15\,\mathrm{V}$
$\mathbf{E_{SB}}$ **(meV)**	-102.2	317.7	115.5

Table 4.1: *The table indicates the evaluated energies at the three relevant points for the NW-based back-gate device. The intrinsic activation energy at* $V_{BG} = 5\,\mathrm{V}$ *correlates well with the energy extracted for the membrane device (*$329.5\,\mathrm{meV}$*; see Section 4.2.1).*

membrane device with $329.5\,\mathrm{meV}$. Therefore, it is supported that the simplified experimental model for the proposed Al-Ge-Al heterostructures also holds for back-gated architectures. Interestingly, the p-type conduction exhibits a negative activation energy, which correlates with the I/V-characteristic shown in Figure 4.3b. There it was shown that with increasing temperatures the current decreases. Similar results were also obtained for Ni-Ge junctions[93] and Ti-nSi junctions[113]. However, in the scope of the cited works, it is claimed that negative Schottky barriers heights are evident. Here, it needs to be considered that the total effective activation energy is determined and not the Schottky barrier height explicitly. Nevertheless, it can be stated that the hole injection does not experience any effective barrier due to the fact that the Fermi level pins close to the valence band. Moreover, the intrinsic Ge channel exhibits a more p-type dominant behavior, which is even strengthened by applying a negative back-gate voltage, and hence further bending the incorporated energy bands upwards. As expected n-type conduction shows a positive effective barrier height for electrons due to a high barrier for electrons and a high contribution of tunneling emission.
The same procedure to evaluate the activation energy of Al-Ge-Al GeOI-based NS back-gate devices was conducted as well. It needs to be considered, that the material stack and especially the oxide landscape differs from the NW-approach. Figure 4.8 shows the transfer characteristic of two NS devices and their activation energies for different back-gate voltages. Again, higher back-gate voltages are necessary due to the thicker back-gate oxide.

In the p-type operation regime the activation energy gets negative, which is correlating with previous investigations on NW-based devices. As expected, the maximum of the activation energy is reached at the intrinsic point. The total effective activation energy at the intrinsic point $V_{BG} = 10\,\mathrm{V}$ was calculated to be $320\,\mathrm{meV}$ for the back-gated NS devices. Remarkably, the two NS devices exhibit a similar activation energy at the intrinsic point as the membrane and back-gate NW devices. Therefore, it can be deduced that the back-gate oxide landscape only has a minor impact on the total effective activation energy and merely the metal-semiconductor junctions determine the effective barrier height. Note that this statement is only valid for back-gated architectures, without the influence of external metal work functions, i.e. by the absence of metallic top-gates atop the devices.

4.2.3 Global Top-Gate Device

By replacing the back-gate with a global top-gate (GTG) approach the gate-voltage can be reduced due to the fact that the top-gate oxide compromises of a thinner oxide. However,

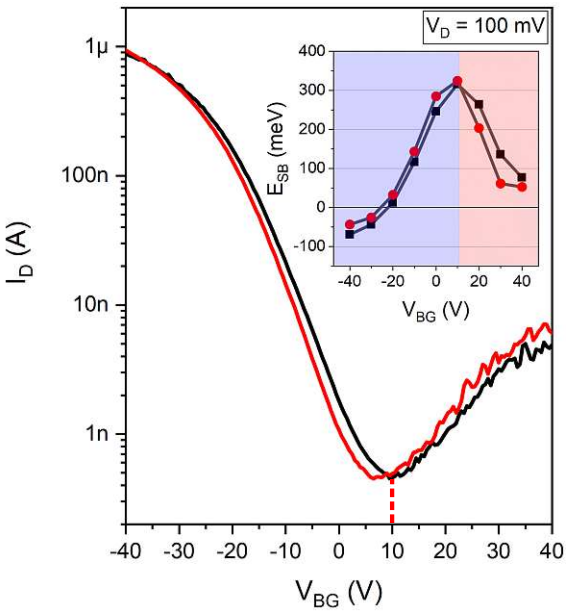

Figure 4.8: *The transfer characteristic shows two NSs with similar geometry properties, where the intrinsic point is at $V_{BG} = 10\,\mathrm{V}$. The inset shows the evaluation of the activation energies at selected back-gate voltages V_{BG}.*

the same gating mechanism is ensured, as the GTG covers the complete structure. Thus, enabling the extraction of the activation energy for GTG devices as well. Figure 4.9 depicts the architecture and shows a colored SEM image of the placed top-gate. As mentioned, no back-gate voltage needs to be applied, as the whole segment gets gated by the top-gate.

Applying a drain-voltage V_D and sweeping V_{TG}, the transfer characteristic is obtained as shown in Figure 4.10a. Moreover, Figure 4.10b shows the activation energy values for different top-gate voltages V_{TG}. Remarkably, the gate-voltages can be reduced from $|V_{BG}| = 15\,\mathrm{V}$ to $|V_{TG}| = 5\,\mathrm{V}$.

Here, transfer characteristics were gathered at different drain-voltages V_D from 1 mV to 1 V. In this context, the band bending mechanism is strengthened by applying higher drain-voltages. Thus, allowing higher contributions of n-type conduction by thinning the barrier for electrons, and therefore allowing a higher contribution of tunneling emission. Remarkably, the p-type SS remains constant for all drain-voltages. However, due to an increasing tunneling contribution at higher drain-voltages, the SS in the n-type regime increases with higher drain-voltages. In contrast to the back-gated device (see Table 4.1), the intrinsic point depicts a higher activation energy of 409.8 meV at $V_{TG} = 1\,\mathrm{V}$. The difference of 86.1 meV can be attributed to the different oxide material stack and the floating back-gate potential. Regarding the oxide material stack the work functions of Ti and Au, which build the top-gate stack, need to be considered as they have an impact on the (neglected) potential in the Ge channel. However, this contribution is not taken

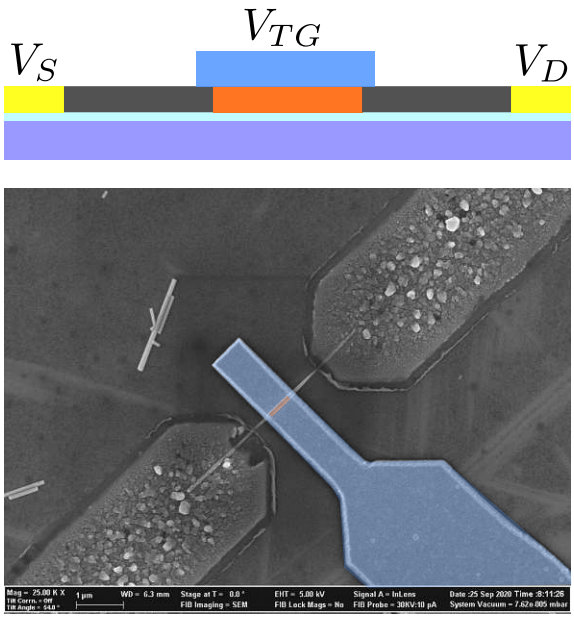

Figure 4.9: *The top illustration shows a schematic illustration of the GTG device. As the top-gate covers the complete segment no back-gate voltage is necessary. The bottom part shows a SEM image of the actually fabricated device.*

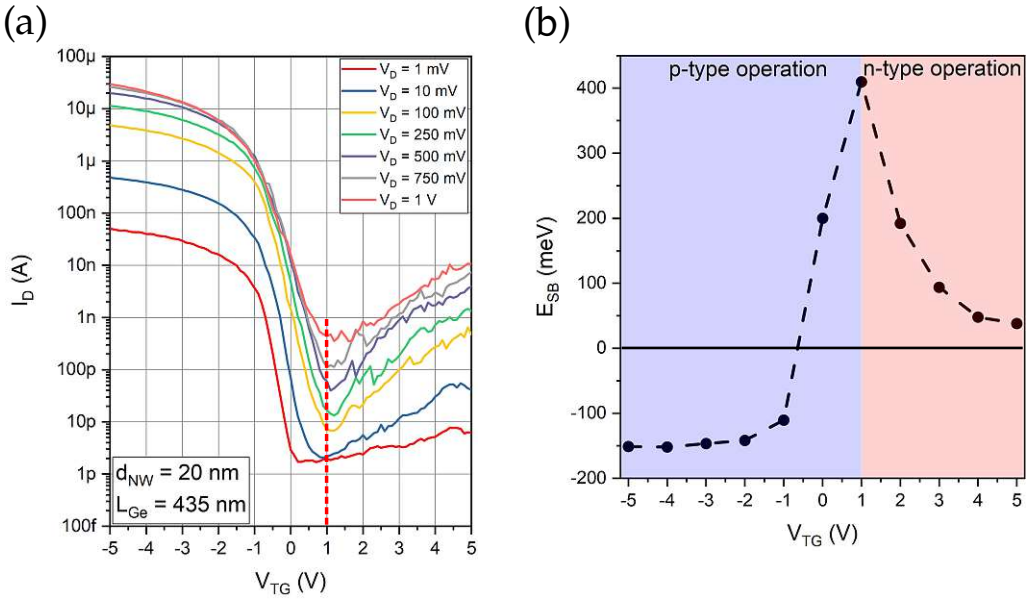

Figure 4.10: *(a) shows the transfer characteristic of the GTG NW device with the intrinsic point marked at* $V_{TG} = 1\,\mathrm{V}$*. Due to the thinner top-gate oxide (*$22\,\mathrm{nm}$*) lower gate-voltages can be applied. (b) shows the evaluated activation energies at selected top-gate voltages* V_{TG}*. A negative barrier is observed for dominant p-type operation.*

into account in the used model. Moreover, the back-gate contact is floating, and thus also influences the potential in the channel. Therefore, the top-gate architecture is not fully suitable for the experimental extraction of the eSBH of Al-Ge-Al systems.
Again, the GTG architecture is investigated on NS devices as well, and is depicted in Figure 4.11. Here, top-gate voltages V_{TG} of $\pm 12\,\mathrm{V}$ are applied. In comparison to NWs a top-gate voltage of $V_{TG} = \pm 5\,\mathrm{V}$ was sufficient to gate the devices. This variation can be attributed to the employed quasi-diameter $\mathrm{d_{NS}}$ which is much larger than the diameter of NWs. Moreover, the quality of the deposited Al_2O_3 might differ and hence allows to apply higher voltages.

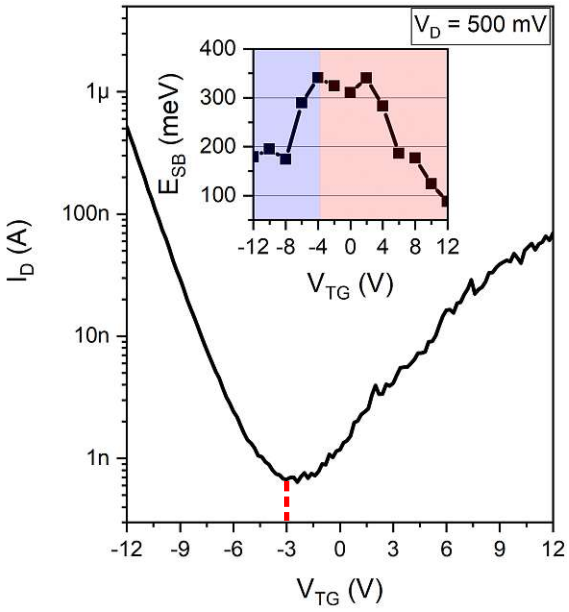

Figure 4.11: *The transfer characteristic has its intrinsic point at $V_{TG} = -3.2\,\mathrm{V}$. Due to limitations of the maximum applied top-gate voltage V_{TG}, the saturation state in the p-type regime is not visible. The inset shows the extracted eSBH values at certain top-gate voltages V_{TG}*

Remarkably, the activation energies in the p-type operation regime do not show a negative effective activation energy, which can be attributed to the fact that the saturation regime cannot be accessed on these devices. Note that the intrinsic point in the inset cannot be clearly distinguished, as in the range from $-4\,\mathrm{V}$ to $2\,\mathrm{V}$ a plateau is evident. It can be concluded that due to the different geometry, and thus due to a larger quasi-diameter $\mathrm{d_{NS}}$ the impact of the top-gate metal work functions is stronger, and therefore highly influences the evaluation of the activation energy for this architecture. Additionally, the rougher top-surface of NS may also contribute to this misbehavior. Hence, it can be concluded that this architecture is not suitable for the extraction of the eSBH as the influence of unknown parameters is highly dominant.

In conclusion, it can be stated the the extraction of the total effective activation energy can be properly extracted for back-gated devices implemented on a NW as well as NS

devices. The reference value of the activation energy of the membrane device, without any gate, perfectly correlates with the evaluated values for both, back-gated NWs and NSs respectively. As the used model neglects the potential between the metal and semiconductor, the top-gate approach cannot be properly utilized as the metal work functions of the top-gate material stack highly influences these parameters, and therefore leads to uncertainties in the used model. The negative activation energies in the p-type operation regime can be attributed to the strong Fermi level pinning close to the valence band as well as to the acceptor-like behavior of the proposed Al-Ge-Al system. Thus, it can be concluded that due to strong band bending no total effective activation energy is evident for the injection of holes. Note that, an effect of hole trapping or de-trapping during the measurement cannot be excluded. In contrast, the activation energies for electrons shows a positive eSBH throughout all investigations due to a much larger barrier for electrons. Table 4.2 gives an overview of all extracted values at the intrinsic point. The membrane device is denoted as NG (no gate) in Table 4.2. In the case that more than one device was evaluated, an average value is calculated.

	NW			NS	
	NG	**BG**	**GTG**	**BG**	**GTG**
$\mathbf{E_{SB}}$ **(meV)**	329.5	317.7	409.8	320.0	332.7

Table 4.2: *Comparison of activation energies, where green marked values indicate reliable values extracted from a membrane device (NG) and back-gate devices, whereas red marked values indicated unreliable values extracted from global top-gate (GTG) devices.*

4.3 Top-Gate FET Architectures

As discussed in Section 4.1, back-gate architectures are not able to suppress undesired charge carriers and thus do always exhibit an ambipolar behavior. The same is evident for the GTG architecture, which covers the complete segment including the metal-semiconductor junctions. This prevents these architectures to be utilized in the context of RFETs. For the realization of RFETs dedicated barriers in the incorporated bands need to be implemented, sufficiently suppressing the undesired charge carrier type. Previous works regarding RFETs showed that such barriers can be introduced by placing top-gates accordingly, and thus allowing to create barriers by electrostatic tuning of the bands.[22] In this section various top-gate architectures are investigated on the NW-approach. In this respect, single, two and three top-gate solutions are introduced and discussed. Note that for all considered band diagrams the back-gate voltage V_{BG} was assumed to be 0 V, as it merely bends the whole energy landscape and thus the bands upwards by applying a negative back-gate voltage respectively downwards by applying a positive back-gate voltage. Therefore, a linear progression is assumed in the un-gated regimes. In this section only remarkable FOMs are discussed at relevant points. A detailed discussion regarding FOMs of RFETs is given in Section 4.7.

4.3.1 Single Top-Gate Device

In a first step the single top-gate (STG) architecture is investigated, as it clearly depicts the effect of top-gates on the incorporated energy bands. Figure 4.12 shows a schematic illustration of a STG device and its incorporated band tuning mechanism. Additionally, a colored SEM image of an actual device is shown in Figure 4.12b. The width of the top-gate contact is 200 nm.

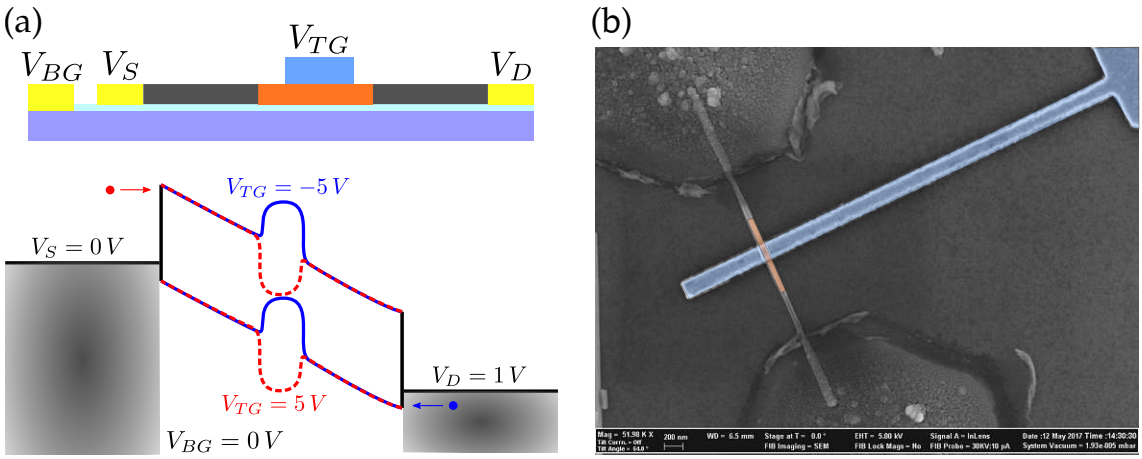

Figure 4.12: *(a) shows a schematic illustration of the STG device. In the bottom part the corresponding band diagrams are shown for $V_{TG} = \pm 5\,\mathrm{V}$. The top-gate allows to introduce an additional barrier in the middle of the channel. (b) shows a colored SEM image of an actually fabricated STG device.*

By applying a voltage V_{TG} at the top-gate contact an additional barrier is introduced in the middle of the channel. Negative top-gate voltages lead to an upwards band bending, favouring p-type conduction by suppressing electrons, whereas positive top-gate voltages lead to a downwards band bending, and thus suppressing holes. Considering the band diagram in Figure 4.12a, it can be deduced that in the case of applying a back-gate voltage V_{BG} the band bending mechanism acts much stronger, as also the un-gated regimes are getting bend accordingly. Moreover, the additional barrier acts as a potential well, where charge carriers can be accumulated. In the case that $V_{TG} = 5\,\mathrm{V}$ electrons are getting accumulated in the potential well, whereas holes are able to fill the potential well in the case that $V_{TG} = -5\,\mathrm{V}$. This can lead to positive feedback in the top-gate region and is able to further enhance the gating effect due to an amplifying mechanism.[114] However, applying a back-gate voltage V_{BG}, the surrounding energy landscape gets smeared out and the potential wells do not contribute that much in respect of positive feedback. Figure 4.13a,b shows the transfer characteristic for back-gate voltages $V_{BG} = -30\,\mathrm{V}$ and $V_{BG} = 30\,\mathrm{V}$, respectively.

As depicted in Figure 4.13b, no dedicated n-type operation can be achieved with this architecture as the single top-gate does not allow to overcome the issue of the strong Fermi level pinning and the initial dominant p-type behavior of the proposed Al-Ge-Al

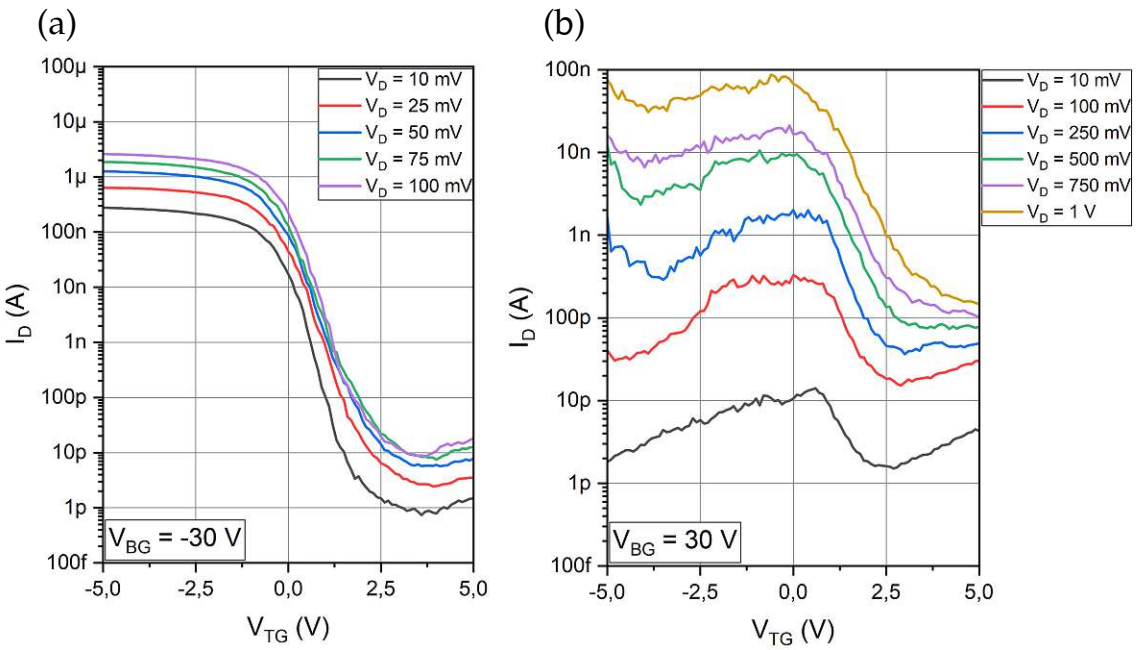

Figure 4.13: *(a) shows the transfer characteristic for a negative back-gate voltage V_{BG} of $-30\,\mathrm{V}$, leading to a dominant p-type conduction by suppressing electron transport. In contrast, (b) shows the case for a positive back-gate voltage $V_{BG} = 30\,\mathrm{V}$.*

system. Moreover, the dip at V_{TG} <0 V shows hole charging in the potential well until a sufficiently high $|V_{TG}|$ is reached, and thus discharging of the potential well is ensured. In p-type operation, as shown in Figure 4.13a, the SS of the device gets remarkably improved by more than a factor of three in comparison to best performing back-gate devices with a SS of 1600 mV/decade. Here the SS exhibits a value of 500 mV/decade, evaluated at V_D = 100 mV. This can be attributed to less involved surface and oxide traps in the utilized top-gate stack in comparison to the back-gate stack. To complete the investigations on this architecture, linear and logarithmic output characteristics were gathered for the STG device, as depicted in Figure 4.14.

Considering the logarithmic plots in Figure 4.14c,d, a remarkable difference is evident. For p-type conduction a relatively symmetric behavior can be observed for any V_D, whereas in n-type operation a strong asymmetry can be determined. The reason for this difference is again the strong Fermi level pinning close to the valence band, and thus the exhibition of a relatively large barrier for electrons. As already discussed in Section 4.2, holes do not experience an effective barrier height (proven by a negative activation energy), and in consequence leading to a symmetric output behavior. In contrast, electrons do experience an effective barrier, as it can be seen in the positive regime of V_D in Figure 4.14d, whereas for negative V_D the bend bending mechanism switches, as the potential at the source-contact is higher than the potential at the drain-contact. Thus, a neglectable effective barrier height is observed. Remarkably, this phenomena can merely be analyzed properly

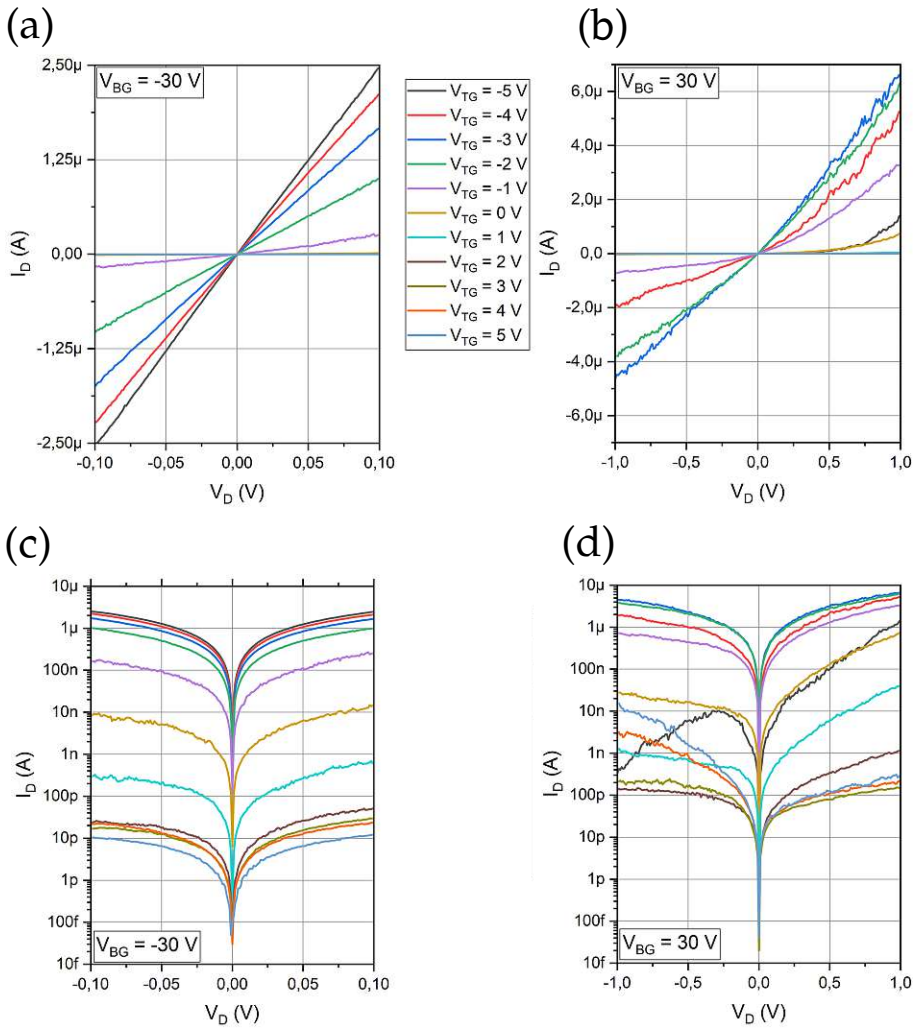

Figure 4.14: *(a) and (b) show the linear output characteristic for p- and n-type operation respectively. Here the noisy current for n-type operation is evident as well. (c) and (d) show the logarithmic representation of the output characteristic for p- and n-type operation. In the n-type operation regime the different transport mechanisms can be observed.*

in the logarithmic representation of the output characteristic.

4.3.2 Single Interface Top-Gate Device

In a next step the architecture of a single interface (top-)gate (SIG) device is investigated, as it allows to directly influence the injection of charge carriers into the Ge segment. Figure 4.15 illustrates the device architecture and its band bending mechanism. Here the width of the top-gate contact is 430 nm. Note that only half of the top-gate contact is covering the Ge segment.

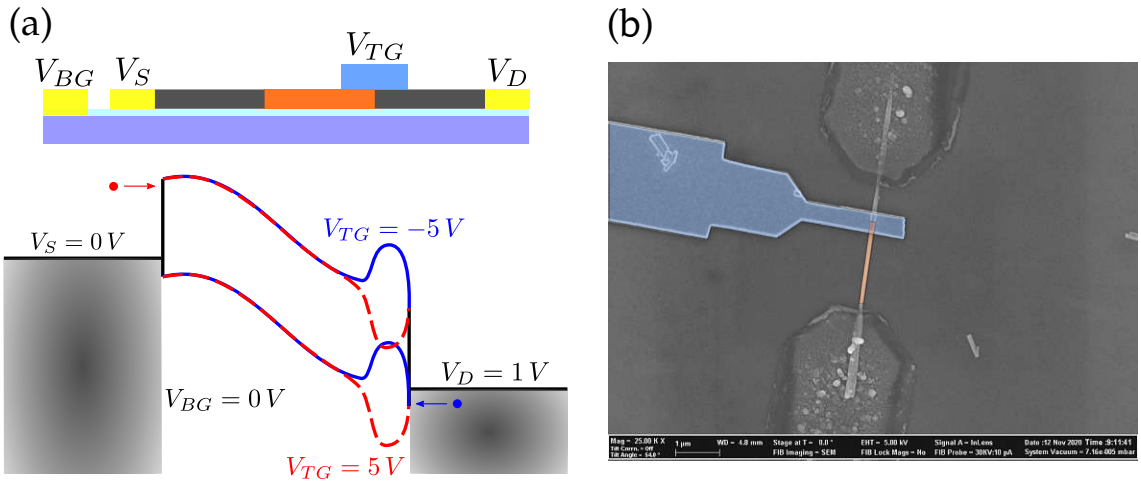

Figure 4.15: *(a) illustrates the device architecture and its incorporated band bending mechanism. The SIG device allows to explicitly introduce a barrier at the injection point. A colored SEM image of the actually fabricated device is shown in (b).*

As depicted by the band diagram in Figure 4.15a, the SIG architecture allows to introduce a barrier at the drain-contact. However, in the scope of the following investigations the drain- and source-contact were switched as well to investigate the influence of the top-gate position. In general, a top-gate atop the Al-Ge junction close to drain is denoted as PG, whereas a top-gate closer to source is named CG. Figure 4.16 shows the transfer characteristic, as well as a relevant output characteristic for the architecture depicted in Figure 4.15a, where the top-gate acts as the PG, and hence is closer to the drain-contact.

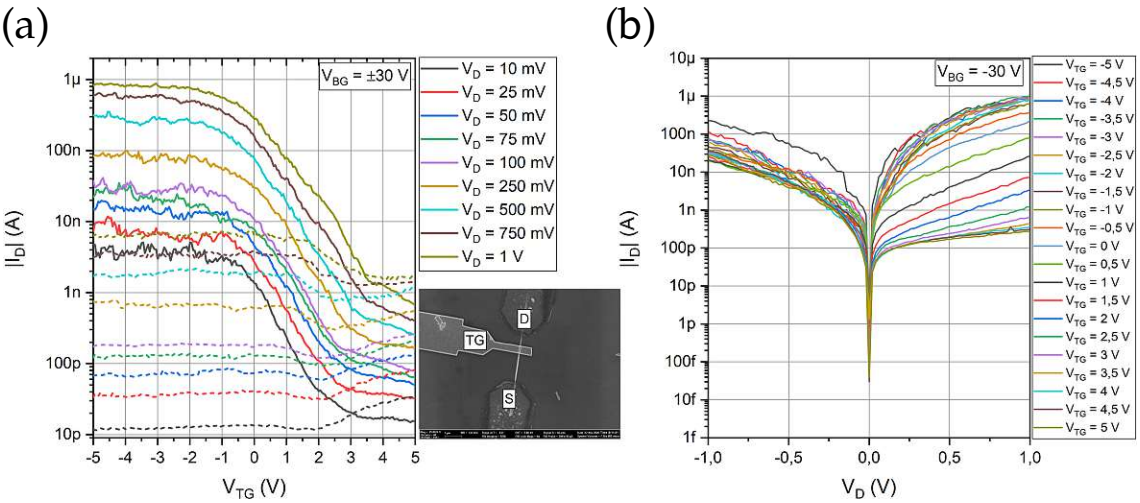

Figure 4.16: *(a) shows the transfer characteristic, where the solid curves are gathered at $V_{BG} = -30\,\mathrm{V}$ and the dashed lines depict the measurements at $V_{BG} = 30\,\mathrm{V}$. A similar behavior as for the STG is evident (see Figure 4.13). (b) shows the output characteristic at $V_{BG} = -30\,\mathrm{V}$.*

In general, a similar transfer characteristic behavior as for the STG is evident. However, at V_{BG} = 30 V a minor n-type conduction can be observed for low drain-voltages V_D. This can be attributed to a better electron injection in comparison to the STG device, as the energy landscape is directly tuned at the injection point. Moreover, enhancing a better suppression of holes. In the p-type regime the SS shows worse results (SIG: 1750 mV/decade; STG: 500 mV/decade), which might can be attributed to a different charge state of the involved trap states. The output characteristic shown in Figure 4.16b shows that in the negative regime of V_D the device cannot be properly gated, due to the fact that the drain potential is higher than the source potential, and thus leading to the accumulation of holes in this regime, which counteracts the electrostatic gating effect. This effect is illustrated in Figure 4.17 in more detail.

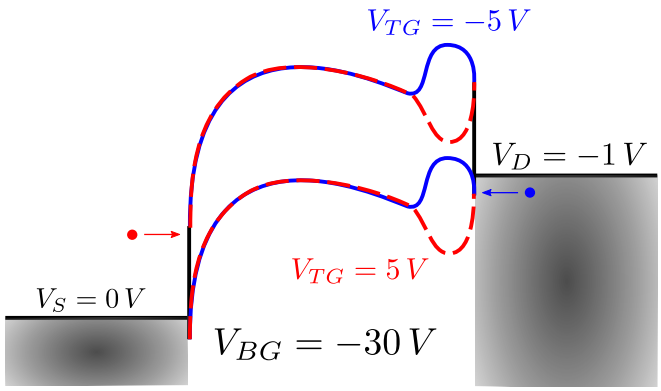

Figure 4.17: *Band diagram in accordance to Figure 4.16b for better understanding of the involved mechanism leading to the obtained characteristic at* V_D <0 V.

Completing investigations of the SIG architecture, V_D and V_S were exchanged, leading to the fact that the top-gate acts as the CG. Therefore, it is expected that no proper suppression can be guaranteed due to the missing PG, which ensures exactly this mechanism. Figure 4.18 shows the transfer characteristic as well as the output characteristic at V_{BG} = 30 V of the SIG device with the top-gate closer to the source contact.

Based on the transfer characteristic, it can be seen that no proper RFET functionality of the SIG device is enabled, as all currents rapidly increase with higher V_D, thus leading to the fact that no suppression of undesired charge carriers is evident. Moreover, no proper gating is possible as depicted by the output characteristic in Figure 4.18b. As this operation mode is only of minor interest to be operated as a RFET, no further investigations will be given at this point.
From the results obtained so far, it can be deduced that single top-gate devices cannot be utilized sufficiently for the realization of RFETs, due to the fact that no dedicated suppression of the undesired charge carrier type can be implemented. To overcome this issue additional barriers needs to be introduced.

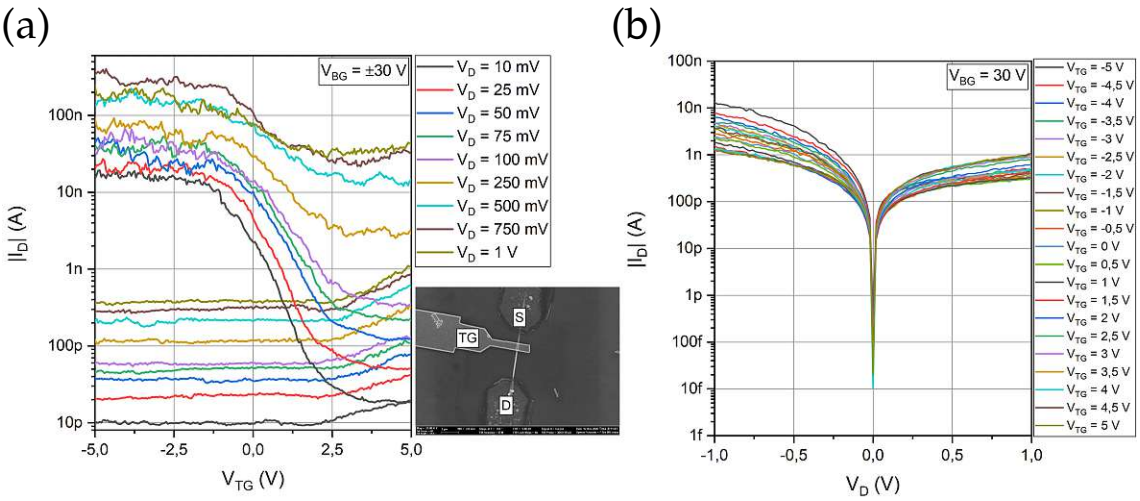

Figure 4.18: *(a) shows the transfer characteristic, where the higher currents determine p-type operation and the lower currents n-type operation. As no PG is utlized no proper suppression of the undesired charge carriers can be prevented. (b) shows the output characteristic at* $V_{BG} = 30\,\mathrm{V}$.

4.3.3 Dual Top-Gate Device

Adding an additional top-gate, a dedicated CG and PG can be introduced, where the CG allows to turn the transistor on and off, and the PG sets the transistor into n- or p-type. In the past, this dual top-gate (DTG) architecture was already proven to be suitable for RFETs.[19, 22] Similar to the SIG architecture, exchanging V_D and V_S lead to the same issues as explained in Section 4.3.2.[115] Figure 4.19 illustrates the device architecture and its incorporated energy band landscape. Again, a colored SEM image of an actually fabricated device is shown. Both top-gates exhibit a width of 400 nm.

By implementing an additional barrier at the source-contact, denoted as CG, it allows to additionally control the injection of charge carriers respectively the suppression of the undesired charge carrier type. In the DTG device architecture the PG determines which charge carrier type – holes or electrons – shall be favoured. This is again realized by setting a negative respectively positive voltage at the corresponding top-gate. Evaluating the transfer characteristic, its capability to be operated as a RFET can be determined. Therefore, Figure 4.20 shows transfer characteristics for sweeping V_{CG} and V_{BG}, whereas the PG-voltage kept constant at $\pm 5\,\mathrm{V}$ for p- and n-type operation respectively.

Interestingly, this architecture also does not allow a proper suppression of electron injection in p-type operation mode, as shown in Figure 4.20a. This can be attributed to the increasing CG-voltage thinning the barrier for electrons, thus increasing the transmission probability for electrons into the Ge channel. However, for low CG-voltages a remarkable p-type operation is enabled. By sweeping the back-gate voltage V_{BG} and keeping V_{CG} respectively V_{PG} constant, the band diagram introduced in Figure 4.19 can be used for

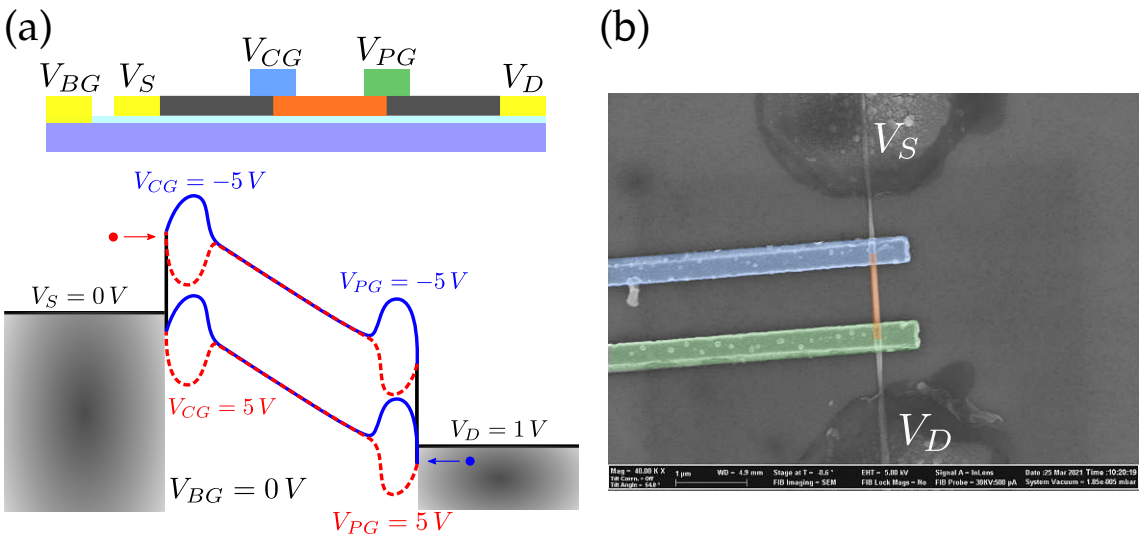

Figure 4.19: *(a) shows a schematic illustration of the DTG device, which makes use of a dedicated CG and PG atop the Al-Ge junctions. This allows to implement two barriers directly at the injection barriers. A colored SEM image of the actually fabricated device is shown in (b).*

explanation. Applying a positive V_{BG}, the barriers are getting even thinner as the back-gate voltage increases the gating effect of the CG and PG. Therefore, a dedicated n-type operation is observable. In contrast, by applying a back-gate voltage V_{BG} of $-30\,\mathrm{V}$, and hence bringing the device into p-type operation, a remarkable potential well for holes is generated, which charges holes and thus prevents proper gating. Moreover, a remarkable effect is evident in the output characteristic of the DTG device, as shown in Figure 4.21. Measurements were performed for p- and n-type operation.

In the p-type operation regime, depicted in Figure 4.21a, the typical MOSFET behavior is evident for V_D $<0\,\mathrm{V}$, which correlates with previous results. However, in the positive regime of V_D and at V_{CG} $>2\,\mathrm{V}$, a steep transition is evident. In combination with increasing V_D and thus constantly shifting the drain potential downwards, at a certain point (V_{CG} $>2\,\mathrm{V}$ and V_D $>100\,\mathrm{mV}$) this then causes a flood of electrons into the Ge channel, as it can be deduced from the band diagram, shown in Figure 4.19. For n-type operation a similar scenario can be observed *vice-versa*. In the negative regime of V_D the SBFET characteristic is evident, as at a certain point the slope of the current sharply changes its slope.

In the proposed Al-Ge-Al system, the DTG architecture does not lead to a sufficient RFET operation, due to the fact that a large NW segment remains un-gated. Therfore, no dedicated polarity control can be ensured, preventing pure n- and p-type conduction. Also considering the back-gate voltage V_{BG} does not contribute to an improvement.

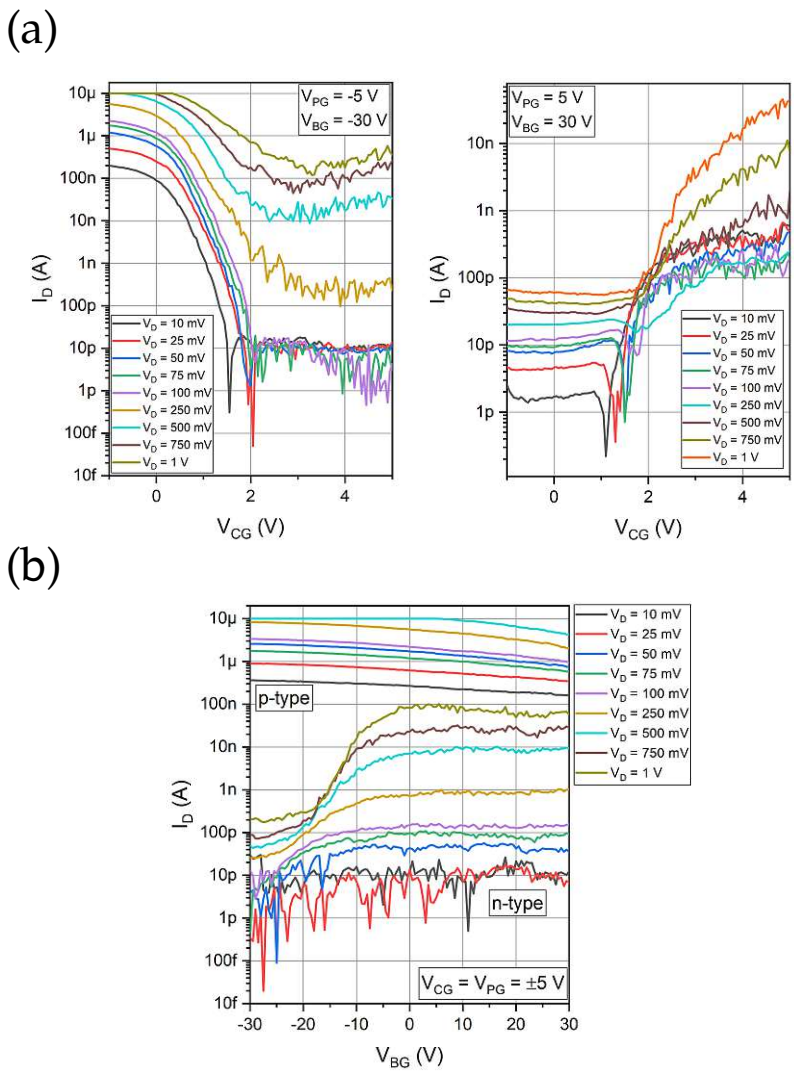

Figure 4.20: *(a) shows transfer characteristics for n- and p-type operation respectively. Note that still no proper suppression of electrons in p-type operation is achieved. (b) shows the transfer characteristic for sweeping V_{BG}.*

4.3.4 Triple Top-Gate Device

As depicted in Section 4.3.3, an architecture with two top-gates does not lead to a good RFET functionality. However, placing an additional top-gate in-between the two interface top-gates, and thus enabling another mechanism to tune the energy band landscape, leads to sufficient results. Basically, this concept combines the characteristics of the STG and DTG architectures and makes use of the advantages of these two concepts. Additionally, the un-gated Ge segments are minimized by introducing a barrier in the middle of the segment. In consequence, proper tunability with relatively good SS values was obtained for the STG device. However, the STG does not allow to sufficiently suppress the undesired

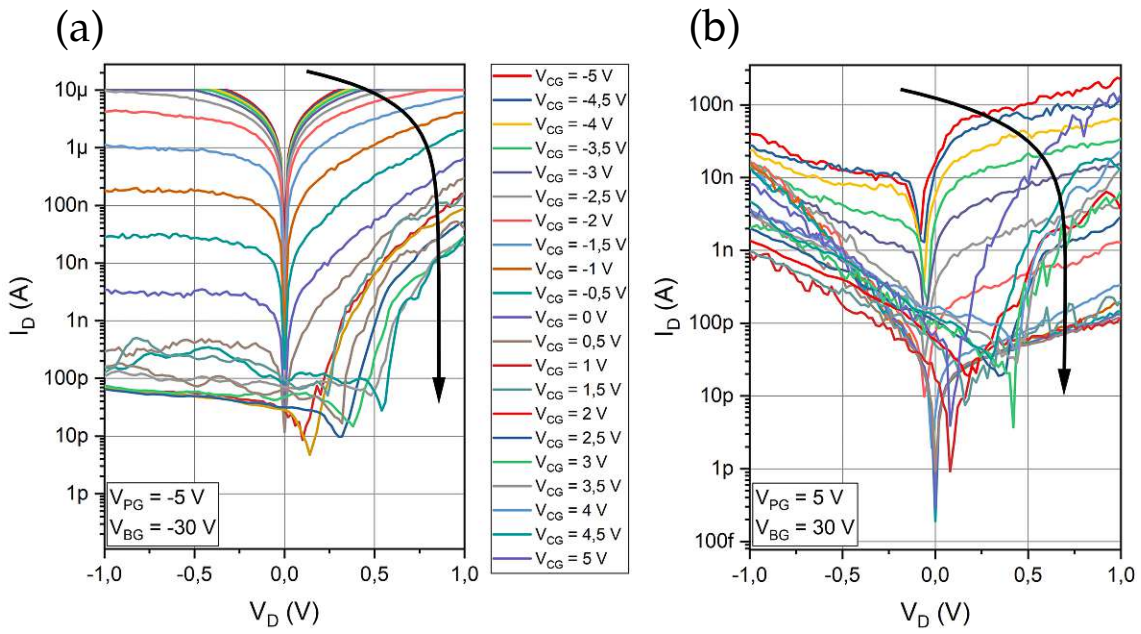

Figure 4.21: *(a) shows the output characteristic for p-type operation, whereas (b) shows the output characteristic for n-type operation as indicated in the left corners of the plots.*

charge carriers. This problem can be overcome by utilizing the DTG architecture, which already shows evidence of RFET operation. From an operation point-of-view, no back-gate voltage is necessary as the three top-gates fully cover and gate the underlying device. Figure 4.22 shows the architecture and band bending mechanism of a triple top-gate (TTG) device. The widths of the presented top-gates are 400 nm for the PGs and 500 nm for the CG. The gap between the individual top-gates is 200 nm.

The proposed configuration allows to set the traversing charge carrier type through the Ge channel by correspondingly set the PG-voltage to a negative (here: $V_{PG} = -5\,\mathrm{V}$) or positive (here: $V_{PG} = 5\,\mathrm{V}$) voltage and hence switching between p- or n-type operation respectively. The CG-voltage allows to turn the current flow through the device on or off. Importantly, it needs to be ensured that the un-gated regions are kept as small as possible to have perfect gating conditions. Note that the representation of the band diagram in Figure 4.22 shall merely depict the functional mechanism. In the actual devices the un-gated regions are not as large as illustrated. TCAD simulations have shown good operability with a spacing down to 10 nm.[116] Another important aspect in this context is the overlap of top-gate across the Ge channel and the PG-contact. A small overlap is necessary to obtain proper tunability, and hence enabling low off-current densities J_{OFF}, which further result in good SS properties. Figure 4.23 shows the transfer characteristics by sweeping V_{CG} and setting V_{PG} accordingly to set the RFET to p- or n-type mode. Moreover, the thermal dependency of the p- and n-type operation is shown.

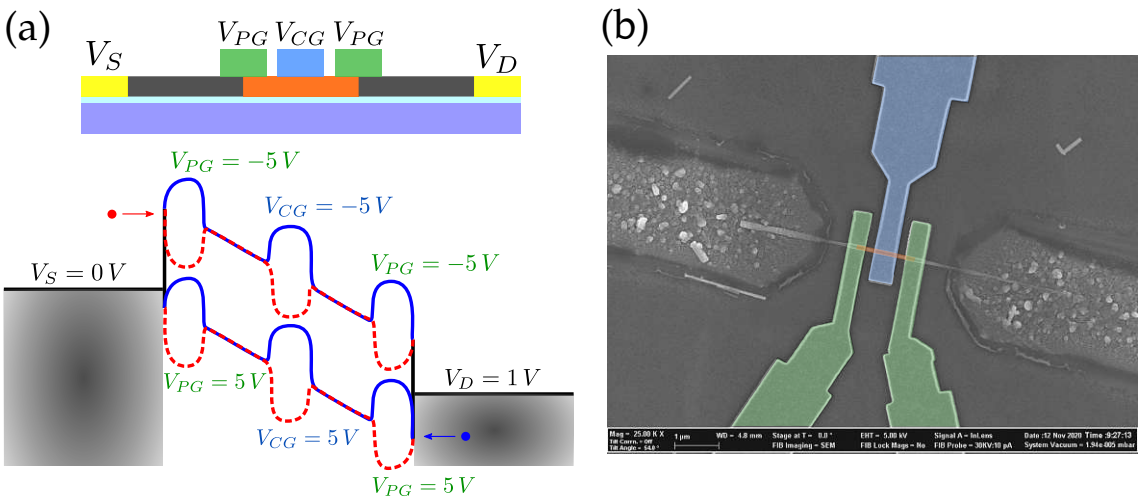

Figure 4.22: *(a) shows the TTG architecture and its incorporated energy band landscape. This architecture allows to introduce three independent barriers within the Ge segment. (b) shows a colored SEM image of the actually fabricated TTG device.*

As illustrated, proper suppression of the undesired charge carrier type can be achieved, and thus leading to proper RFET functionality. Consequently, the off-state current drops by one order of magnitude in comparison to the GTG device despite a low band-gap material being employed. Figure 4.23b illustrates the performance at elevated temperatures, where an increase of the off-state current as well as an increase of the SS is evident. This can be attributed to the fact that electrons are getting thermally excited and therefore contribute to I_D.[117] Regarding the FOMs of this RFET architecture the following statements can be deduced. Setting $|V_{PG}| = 5\,\mathrm{V}$, a total $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio of 3×10^5 and 4×10^2 is gathered for p- and n-type operation respectively. At $V_D = 1\,\mathrm{V}$, it is possible to achieve $J_{\mathrm{ON}} = 9.2 \times 10^5$ A/cm^2 in p-type operation and $J_{\mathrm{ON}} = 3.3 \times 10^3$ A/cm^2 in n-type operation. Remarkably, an off-state current density of $J_{\mathrm{OFF}} = 25$ A/cm^2 in p-mode and $J_{\mathrm{OFF}} = 25$ A/cm^2 in n-mode is evident and is about a factor of 10^3 smaller compared to a GTG device (see Section 4.7). As depicted in Section 3.2.5 the transconductance g_m and threshold voltage V_{TH} can be extracted from the transfer curves. Relevant plots and the extraction of V_{TH} are shown in Figure 4.24.

The peak transconductance g_m was evaluated to be 2.7 µS for p-type operation and 63.4 nS for n-type operation. Moreover, as depicted in Figure 4.24 the threshold voltage V_{TH} for p-type operation is $-1.4\,\mathrm{V}$ and $1\,\mathrm{V}$ for n-type operation. In a last step the output characteristic of the NW-based TTG RFET is analyzed in Figure 4.25. Note that merely the logarithmic representation is illustrated at this point, as it allows a more convenient analysis of the transport mechanism.

The output characteristics reveal the same features as already discussed. A clear MOSFET- and SBFET-behavior is evident in p-type operation at $V_{PG} = -5\,\mathrm{V}$. It can be distinguished

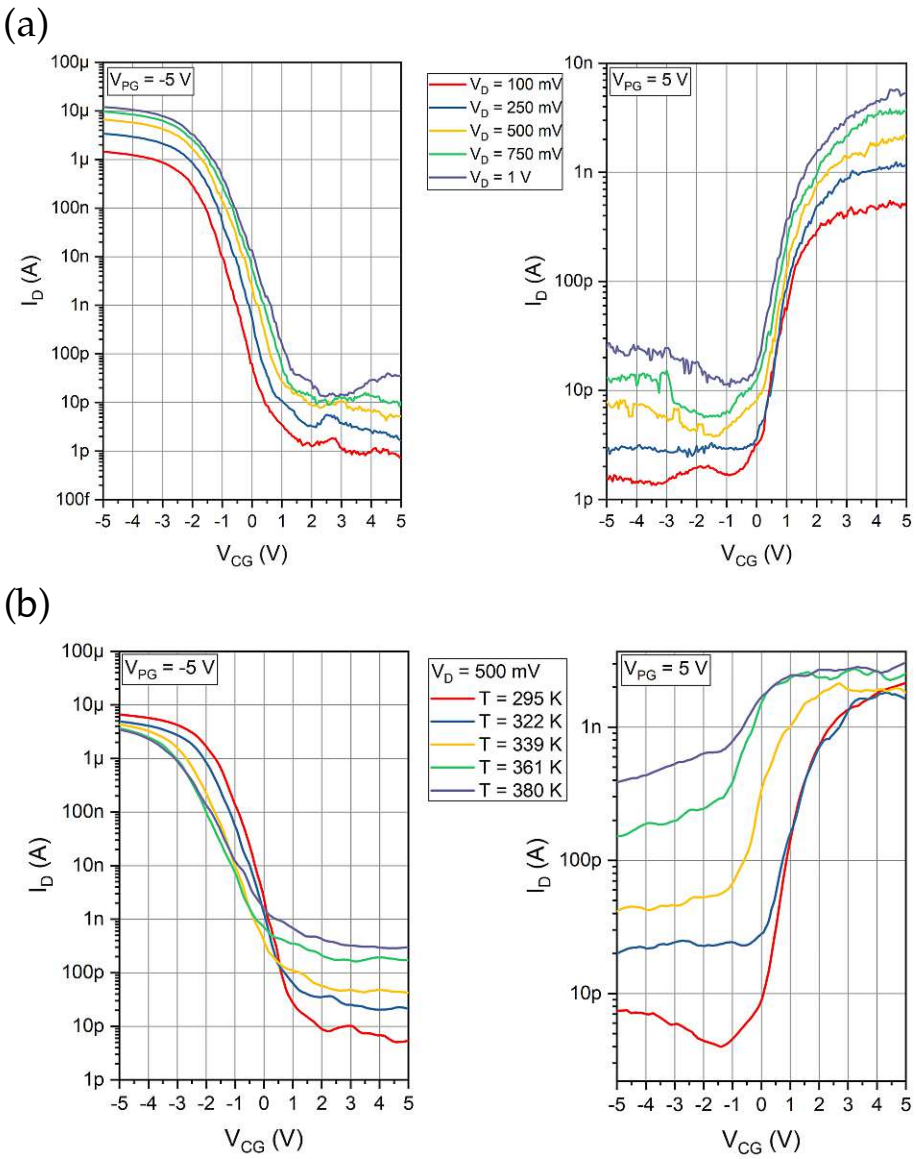

Figure 4.23: *(a) shows transfer characteristics for p- ($V_{PG} = -5\,\mathrm{V}$) and n-type ($V_{PG} = 5\,\mathrm{V}$) operation, respectively. The TTG architecture allows proper suppression of the undesired charge carrier types. (b) shows transfer characteristics at elevated temperatures and $V_D = 500\,\mathrm{mV}$.*

between V_D <0 V (MOSFET characteristic) and V_D >0 V (SBFET characteristic). Mainly, these topics can be assigned to the utilized Al-Ge-Al system and its incorporated energy band landscape. Visualizing the transport mechanisms by density plots, as shown in Figure 4.25b, allows to deduce regions, where charge carrier transport is evident in dependence of V_{CG} and V_D. For the visualization of the density plots shown in Figure 4.25b, a Python script developed in the scope of this work, was used.
In comparison to other device architectures, the TTG device revealed enhanced RFET

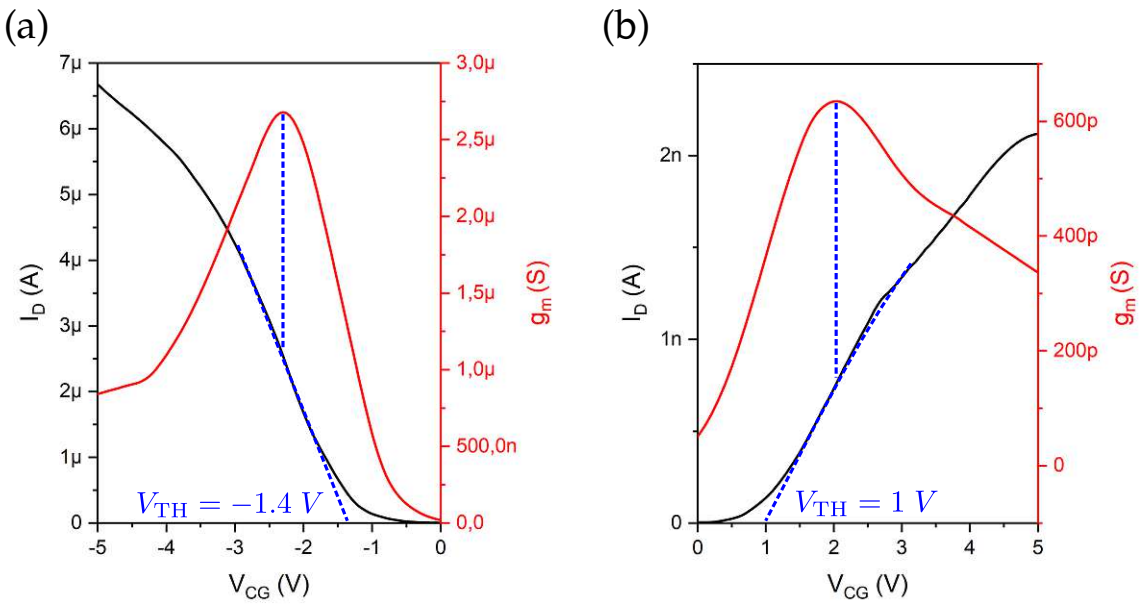

Figure 4.24: *By calculating g_m and evaluating its maximum, the threshold voltage V_{TH} can be extracted as shown in (a) for p-type operation and (b) for n-type operation.*

capabilities, which can be attributed to the PGs at the Al-Ge junctions, properly suppressing the undesired charge carrier type and the additional CG in the middle of the channel, allowing sufficient gating to turn the transistor on and off. Thus, enabling a reliable platform for the realization of RFETs. Note that relevant and important FOMs in the context of RFETs are presented and compared in Section 4.7.

4.4 NDR Devices

The capability of the exhibition of NDR in Ge nanostructures is thoroughly discussed from a physical point of view in Section 2.2.2. Here, the actual realization of Ge-based NDR devices is described. Section 4.1 already revealed that back-gate and GTG devices are not capable to be operated as RFETs due to the lack of a possibility to suppress a specific type of charge carrier. Nevertheless, n-type operation is evident in these devices. Therefore, these two architectures are thought to be optimal for the exhibition of the transferred-electron effect, which is utilized for the realization of NDR devices. As both architectures were already presented, in this section special attention is given to the electrical characterization and the extraction of relevant FOMs, introduced in Section 2.2.2. Firstly, NW back-gate devices are considered. Prior to the extraction of FOMs, a basic characterization of the observed effects was done. Figure 4.26 shows a representative output characteristic of a back-gate NW device at different (positive) V_{BG} values.

To access the electron-dominant transport regime a positive back-gate voltage V_{BG} is necessary, and thus bending the band downwards, enabling electron injection at the source-

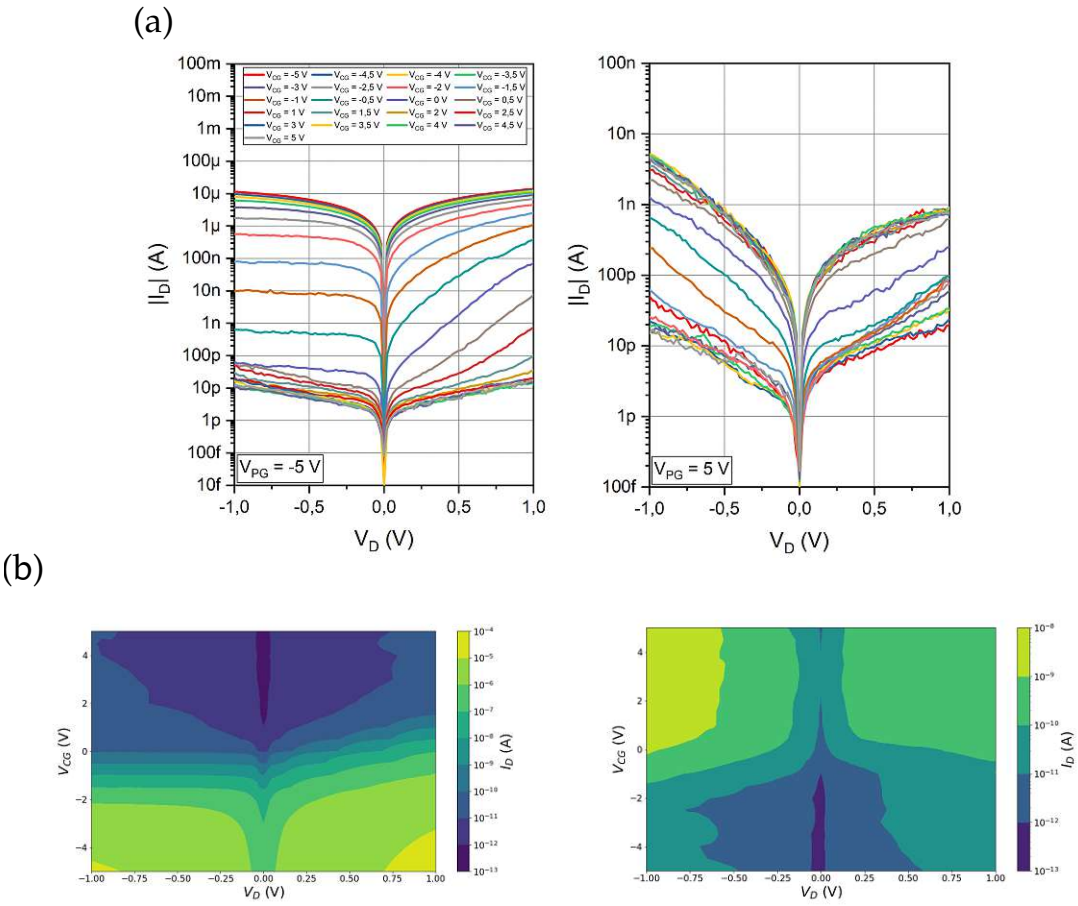

Figure 4.25: *(a) shows the logarithmic representation of the output characteristics for p-type ($V_{PG} = -5\,\mathrm{V}$) and n-type operation ($V_{PG} = 5\,\mathrm{V}$). By utilizing density plots shown in (b) the transport regimes can be visualized.*

contact. Moreover, the barriers are getting thinner and therefore, the contribution of tunneling emission is increased as well. By increasing the drain-voltage V_D sufficiently high, the expected transferred-electron effect indeed takes place. Hence, leading to the exhibition of NDR, as described in Section 2.2.2. Remarkably, by varying the back-gate voltage V_{BG} the PVCR $= I_P/I_V$ can be tuned as it can be observed in Figure 4.26. At $V_{BG} = 20\,\mathrm{V}$ its maximum of 27.5 is reached. In contrast, at $V_{BG} = 10\,\mathrm{V}$ the PVCR is 2.5. Figure 4.27 shows the critical electric field, which needs to be applied at the drain-contact to enable the transferred-electron effect. As the drain-voltage, and in consequence the electric field, highly depends on the length $\mathrm{L_{Ge}}$ of the device, its dependence was evaluated for different NW lengths. Remarkably, it was shown that an influence of the NW diameter $\mathrm{d_{NW}}$ can be excluded.

It is evident that an exponential decay with increasing channel lengths $\mathrm{L_{Ge}}$ is exhibited. For devices with $\mathrm{L_{Ge}} > 1\,\mu\mathrm{m}$ a constant electric field of E_{Transfer} of $1\times10^4\ \mathrm{Vcm^{-1}}$ is sufficient

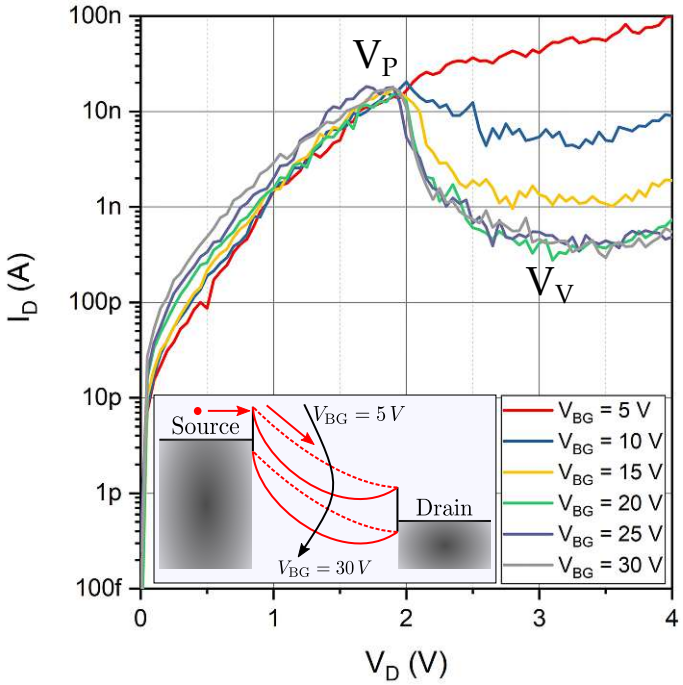

Figure 4.26: *It can be depicted that due to strong band bending – induced by V_{BG} – the PVCR is enhanced. The inset shows the band bending mechanism in the electron-dominant regime.*

to initiate the transferred-electron effect. In contrast, short lengths L_{Ge} lead to an electric field close to the break-down field of bulk Ge with $E_C = 100\,\mathrm{kVcm^{-1}}$.[42] The inset in Figure 4.27 shows the suggested physical phenomena. Due to scattering of hot electrons from the ⟨111⟩- to the ⟨100⟩-valley, these hot electrons release their energy gained from the electric field by creating electron-hole pairs. The continuation of this process results in high energetic electrons, and thus to an increased rate of electrons being transferred to the ⟨100⟩-valley.[94] The application of $V_{BG} > 0\,\mathrm{V}$ further enhances the lateral field at the same side, strengthening this effect. With decreasing channel lengths L_{Ge}, the acceleration path is decreasing as well, and thus results in less energetic electrons. This leads to the fact, that a significantly higher electric field needs to be applied to induce the transferred-electron effect. Moreover, the thermal performance at $T = 200\,\mathrm{K}$, 295 K and 350 K of a representative NW-based back-gate device was investigated, as shown in Figure 4.28.

As already shown on other Ge-based NDR devices,[32, 33] the PVCR increases with reducing the temperature. Here, the PVCR at $T = 200\,\mathrm{K}$ is 220, in comparison to a PVCR of 25 at $T = 295\,\mathrm{K}$. At $T = 350\,\mathrm{K}$ the PVCR merely exhibits a value of 5. The evaluation of a linear fit reveals that the PVCR decreases with a rate of $0.46\,\mathrm{K^{-1}}$. This phenomena can be attributed to thermally excited electrons, which are gathered in the ⟨100⟩-valley and do therefore not contribute to the transferred-electron effect and thus inhibits the exhibition of NDR. Moreover, it needs to be considered, that the ionization rate rises

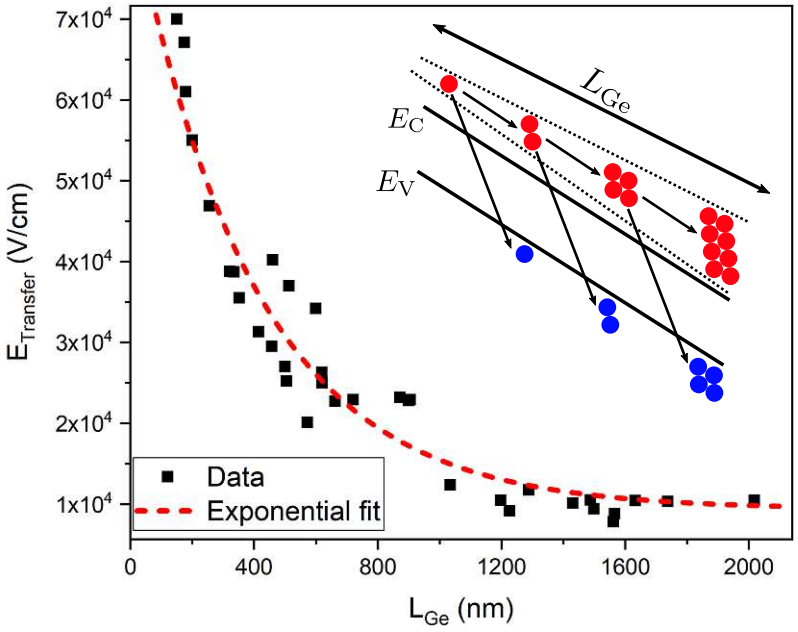

Figure 4.27: *Al-Ge-Al devices between* 150 nm *and* 2 µm *were evaluated in respect to the electric field which is necessary to obtain the transferred-electron effect. The inset illustrates the charge carrier scattering.*

with temperature. As more than twenty devices were evaluated, correlations between the geometry (Ge channel length L_{Ge} and NW diameter d_{NW}) as well as of the temperature, and the PVCR can be derived. In this respect, Figure 4.29 shows the dependency of the PVCR in accordance to the geometry and temperature.

It can be deduced that the PVCR slightly decreases with an increasing length L_{Ge} and diameter d_{NW}, as shown in Figure 4.29a. This can be attributed to an increasing resistivity of the longer and thicker NWs. Devices with a length L_{Ge} of <100 nm did not show any sign of NDR, which can be argued to be caused by the quasi-ballistic nature of such short Ge channels.[118] From a PVCR point of view best performing devices were found to have L_{Ge} = 150 nm and d_{NW} = 20 nm, which is just three times larger than the free mean scattering path in the proposed Ge NWs.[118] As already indicated and discussed (see Figure 4.28), the PVCR decreases with increasing temperature, as shown in Figure 4.29b. In comparison with existing Ge- and Si-based Esaki diodes, the PVCR at room temperature of the best performing device in this work is approximately a factor 20 larger.[98, 119]
As the PCVR directly correlates with the involved currents (I_P/I_V), no dedicated analysis of the peak-current I_P and the valley-current I_V are given here. However, the voltage dependencies (peak-voltage V_P, valley-voltage V_V and plateau-voltage V_{PT}) in relation to the channel length L_{Ge} are depicted in Figure 4.30. Evaluation of data showed that these voltages are independent of the NW diameter d_{NW}.

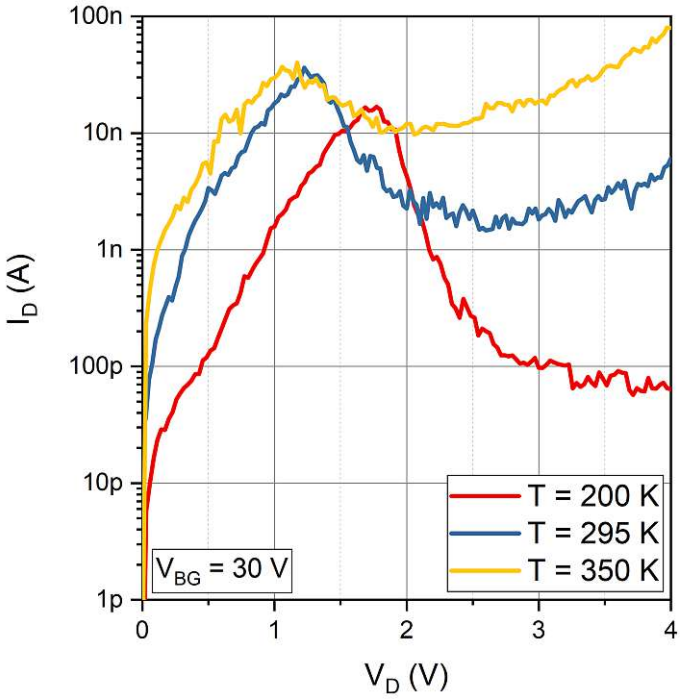

Figure 4.28: *The thermal dependence of NDR exhibited by NW-based back-gate device reveals its high thermal dependency. Remarkably, the PVCR can be significantly increased at low temperatures.*

In the NW-based back-gate NDR device the FOM-voltages show a linear-increasing dependency with the channel length L_{Ge}. The reason for this trend is that with an increasing length L_{Ge}, the series resistance of the device increases as well, and therefore shifts the whole NDR characteristic to higher voltages. This topic is discussed in Section 2.2.2. Finally, to reduce the gate-voltage from 30 V (back-gate device) to lower voltages, a GTG device with full coverage of the active region was fabricated and analyzed. Moreover, this allows to neglect the back-gate voltage and to decrease the top-gate voltage down to 5 V. As previously discussed, this enables an quasi-equivalent gating mechanism as for the back-gate device, and hence allows a similar tunability of the PVCR. Figure 4.31 shows NDR characteristics for different top-gate voltages V_{TG} of a GTG NDR device. Nevertheless, the gate tunability of PVCR is lower than with a back-gate architecture.

In conclusion, the systematic benchmark of the NDR metrics for back- and top-gate NW-based devices reveals its high potential for logic applications. In this respect, a pronounced PVCR is even evident at room temperatures. In comparison to existing platforms, PVCR values 20 times higher were extracted from the proposed Al-Ge-Al platform. This can mainly be attributed to the pure metal-semiconductor junctions, preventing contamination of the Ge segment. Additionally, enabling a possibility to tune PVCR by setting corresponding gate-voltages, it allows the realization of NDR devices for different applications.[91] Highly relevant for cost-efficient and industrial implementations, the presented

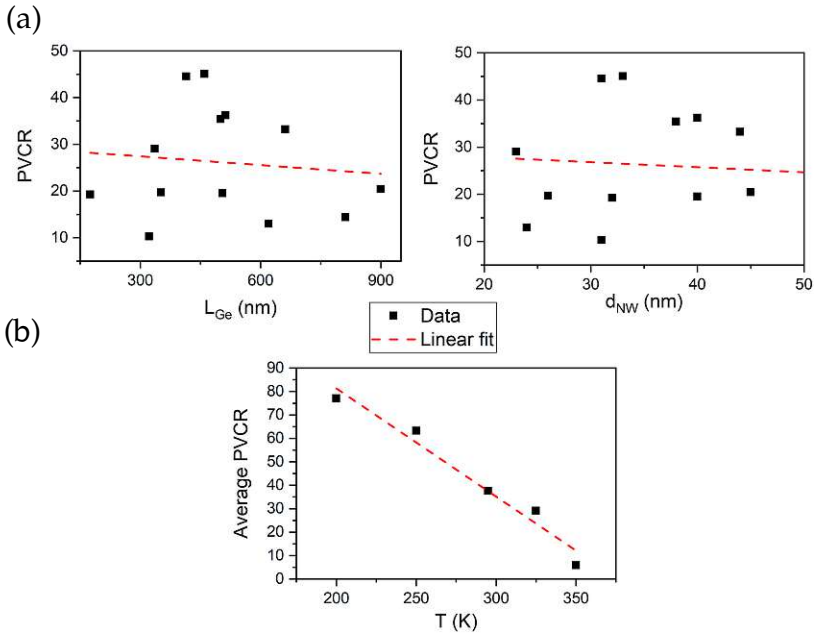

Figure 4.29: *(a) shows the geometry dependencies of the PVCR for twenty devices. Relatively longer and thicker NWs exhibit a less pronounced PVCR The thermal dependency was evaluated for ten devices and an average PVCR over temperature was calculated, as shown in (b).*

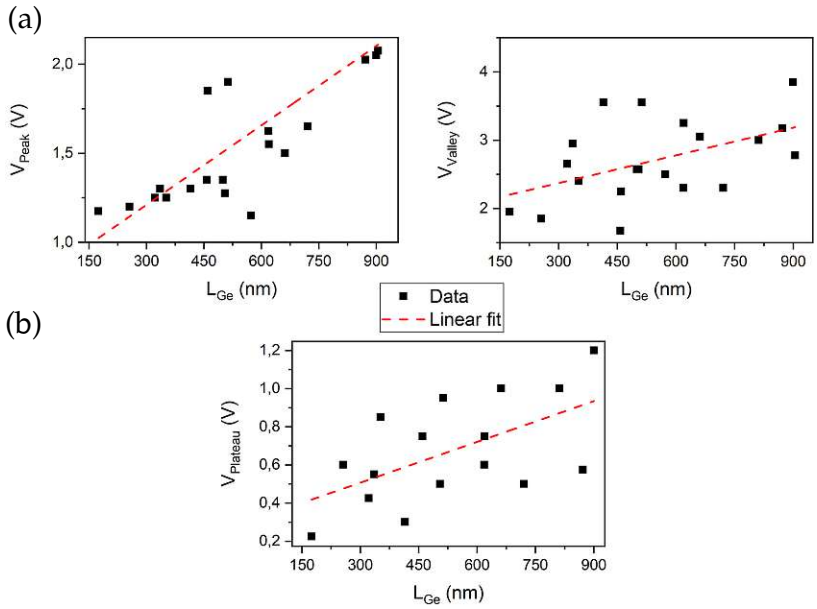

Figure 4.30: *(a) shows the peak- and valley voltage dependence in correspondence to L_{Ge}. In addition, (b) shows the plateau-voltage in relation to L_{Ge}, where this region is extended is evident for longer devices.*

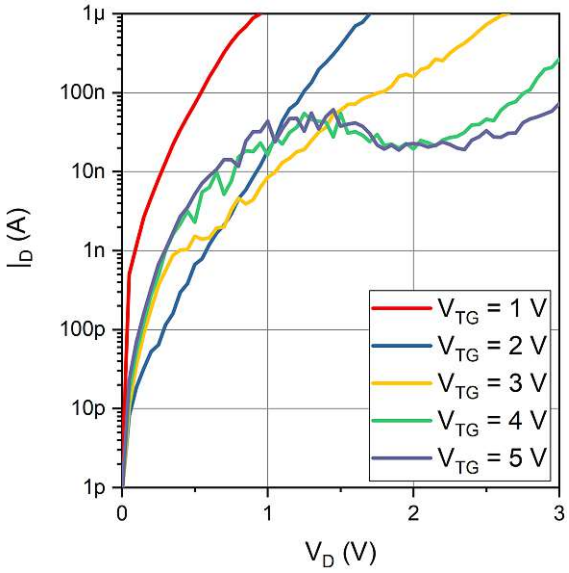

Figure 4.31: *The output characteristic of the GTG NDR device shows that by consequently applying higher top-gate voltages V_{TG} >4 V and increasing V_D, a pronounced NDR characteristic is obtained.*

approach is suitable for implementation in CMOS technology, and thus may paves the way to further exploit nanoelectronic circuits and systems.
Investigations on NSs did not show any signs of the transferred-electron effect, and hence inhibits the observation of NDR. Taking the structural sizes into account, it can be concluded that the utilized NSs exhibit a too large geometry for the realization of NDR devices. To overcome this issue, thinner Ge-layers of the GeOI substrate might lead to the observation of NDR.
It is important to mention that in the scope of this thesis, only quasi-static I/V measurements were performed. Fast and pulsed measurements, e.g. via pulsed measurement units were only possible for bias voltages V_D <3 V, limiting the ability to perform transient measurements. Future analysis would include these measurements in order to consider possible trapping and de-trapping effects as well as charging effects of the semiconductor on the NDR effect.

4.5 NDR-mode RFET

Investigations on NW-based TTG devices showed that the RFET mechanism, as presented in Section 4.3, can be merged with the gate-tunable NDR approach depicted in Section 4.4. This enables a completely new type of device, capable to merge the RFET mechanism (n- and p-type operation) with NDR functionality. This type of device is highly desired for MVL logic gates, which targets to replace conventional binary systems by operation schemes with higher radices.[120] Hence, implementing an operation scheme with higher

performance using fewer devices and interconnects compared to standard CMOS circuits, owing to higher functionality of MVL circuits can be envisaged.[121] Recently, a new MVL concept based on exploiting the monostable-to-multistable[91] nature of serially connected NDR devices was demonstrated, creating a staircase of holding states.[122] An example for a simple yet innovative logic element taking advantage of the NDR characteristic is the MOBILE concept, employing two NDR devices connected in series capable to perform both NAND and NOR operations.[35, 91] Furthermore, stacking more than two NDR devices, an efficient, and compact signed-digit NDR-based MVL adder combining a more than five-fold improvement in circuit propagation delay and a 15 times smaller area compared to common CMOS based circuits has been proposed.[123]
As both concepts were thoroughly discussed in Sections 4.3 and 4.4, merely the obtained results are discussed here. The utilized TTG architecture enables NDR operation implemented in a RFET, therefore from now on this type of device is named "NDR-mode RFET". Again, to access the transferred-electron effect, the RFET needs to be operated in the n-type operation regime, to favour electron transport. In this respect, the PG-voltage V_{PG} is set to 5 V. To enable NDR the CG-voltage V_{CG} needs to be set accordingly. Figure 4.32b shows the V_{CG}-dependent output characteristic of the NDR-mode RFET.

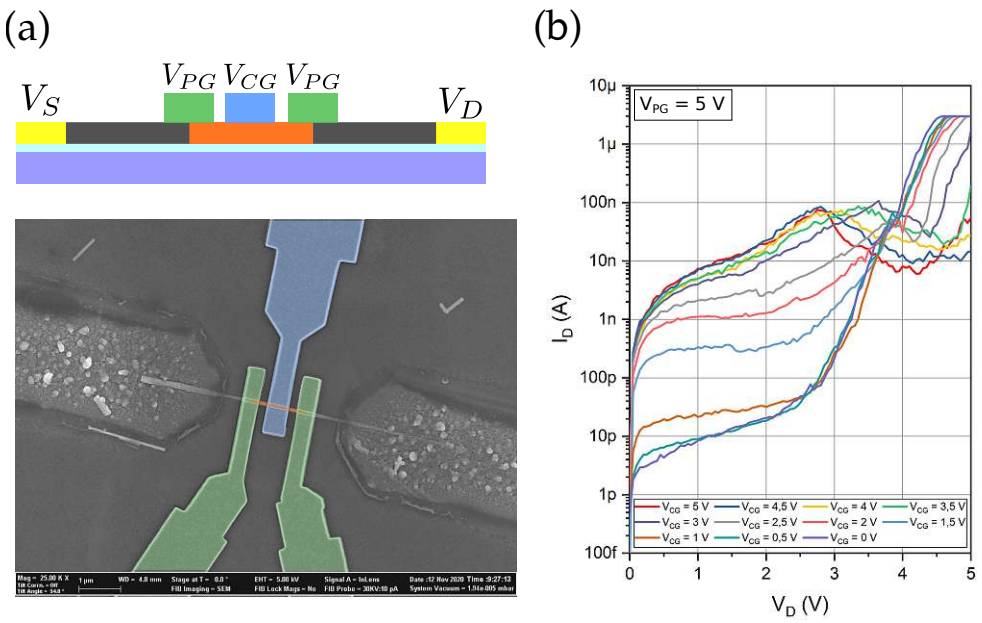

Figure 4.32: *(a) shows the utilized TTG architecture for the NDR-mode RFET device. The colored SEM image illustrates the top-gate placement. (b) shows the output characteristic in the n-type operation regime. Pronounced NDR is visible for* V_{CG} >3.5 V.

Most remarkably, it can be deduced that the peak-voltage V_P of the NDR characteristic can be modulated by V_{CG}. This allows to set the peak-voltage V_P of the NDR to values between 4.1 V and 2.7 V. Thus, enabling to quasi-tune the resistivity of the device by controlling the current flow through the device. In this sense, the exhibition of NDR and the position of the NDR region are decoupled from each other, by utilizing the TTG architecture. By

favouring electron-dominant transport ($V_{PG} = 5\,\mathrm{V}$) and applying a sufficiently high drain-voltage V_D, the transferred-electron effect is initiated, whereas V_{CG} then merely tunes the position of the NDR region by determining the current flow through the device, and thus quasi-tunes the resistivity of the Ge channel. This leads to a shift of the relevant FOM-voltages defining the NDR region. Hence, a serial circuit of NDR-mode RFETs, each supplied with different V_{CG}, allows to realize an I/V characteristic with several overlapping NDR regions that could be used for the MOBILE concept. Figure 4.33 gives a more detailed insight on the tunability of the peak-voltage V_P.

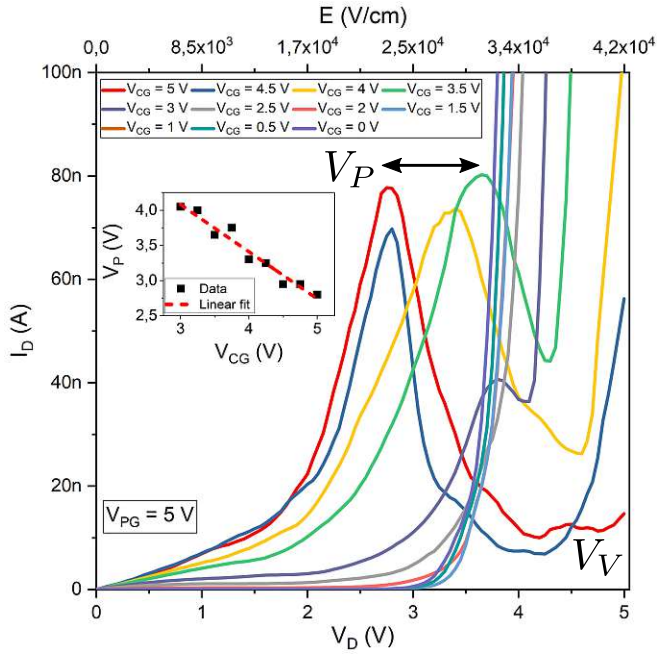

Figure 4.33: *The detailed linear representation of the NDR characteristic shows a pronounced capability to tune V_P by setting V_{CG} accordingly. The inset depicts the range of tunability.*

Importantly, NDR-mode RFET devices should allow to realize small footprint and energy efficient MVL concepts, where the radix is set by the number of devices connected in series. Notably, as shown by recent circuit simulations, exploiting such characteristics, complex logic functions such as multi-value adders revealing a significantly reduced circuit propagation delay could be realized.[123]
To investigate the thermal performance of the NDR-mode RFET, the PVCR was analyzed at several elevated temperatures. Figure 4.34 shows the T-dependent PVCR, evaluated at $V_{CG} = 5\,\mathrm{V}$.

Note that even at $T = 380\,\mathrm{K}$, NDR characteristic is evident, which is an important prerequisite for actual applications and proves the capabilities of the proposed device concept. Linearly fitting the data, the average PVCR decreases from 10.9 at room temperature ($T = 295\,\mathrm{K}$) to 1.2 at $T = 380\,\mathrm{K}$ with a rate of approximately $0.1\,\mathrm{K}^{-1}$. In comparison to the

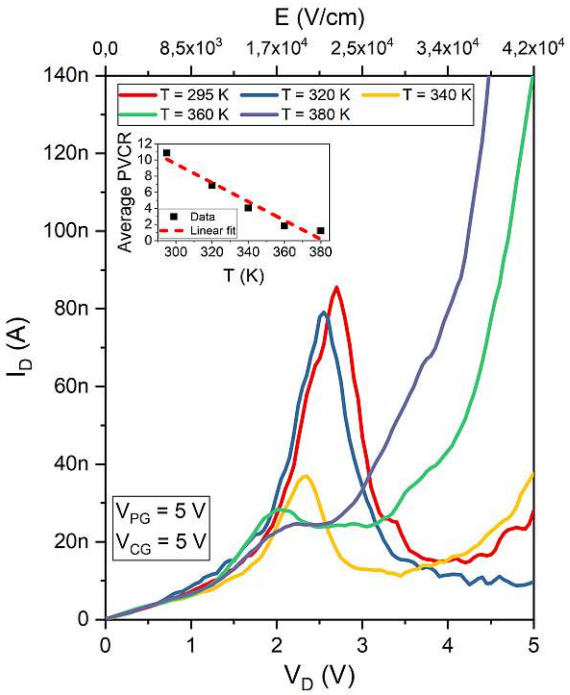

Figure 4.34: *The PVCR is decreasing over temperature for the RFET-NDR device as well. However, is still evident at* $T = 380\,\mathrm{K}$. *The inset depicts the average PVCR for three devices over temperature.*

back-gate NDR device, presented in Section 4.4, the rate is $0.46\,\mathrm{K}^{-1}$.

In conclusion, the presented device concept enables a modulation of both, the PVCR and the position of the NDR region. Hence, a serial circuit of devices, each biased with a different top-gate voltage applied at the CG, results in an I/V characteristic compromising several overlapping NDR regions, that could be used as MOBILE devices. Thus, allowing the realization of highly desired MVL circuits, enabling logic with extended radices. Moreover, it could allow the realization of static memory cells, switching logic circuits or small footprint and energy efficient computational MVL.

4.6 RFET on GeOI

As shown in Section 4.3.4, the RFET-concept based on the TTG architecture leads to proper RFET functionality. However, a wafer-scale integration of NWs is difficult with this approach. Therefore, the concept is transferred to the GeOI-based NS-solution, and thus may pave the way for actual wafer-scale integration. As the TTG concept is thoroughly discussed in Section 4.3, no additional information will be given here. Figure 4.35 shows the NSs TTG architecture and the transfer characteristic of the proposed device.

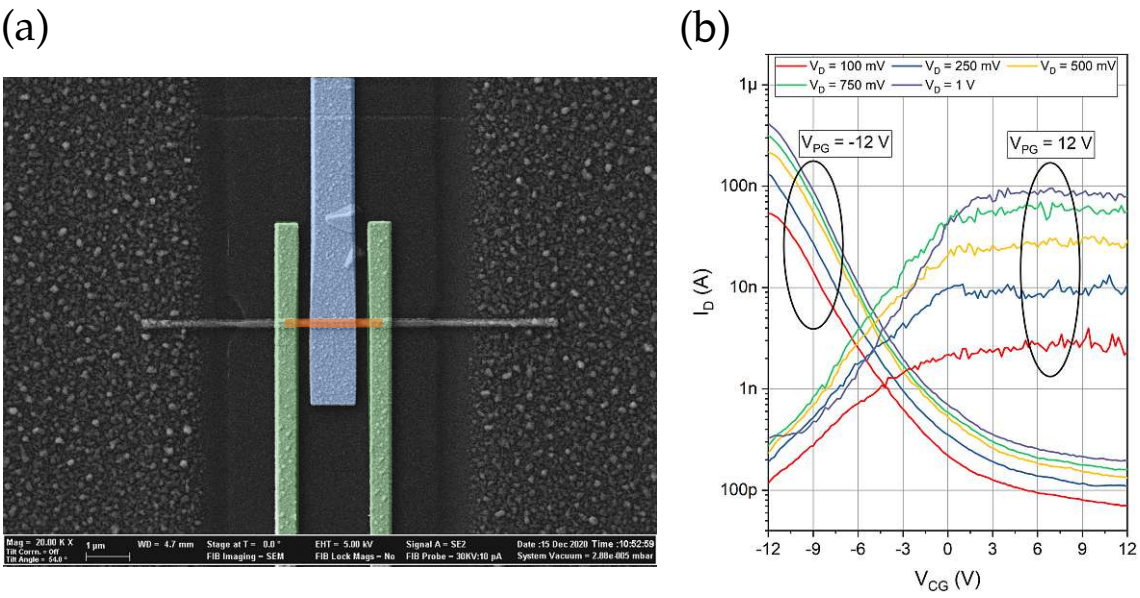

Figure 4.35: *(a) shows a colored SEM image of the actually fabricated NS-based TTG device. The PGs are colored green, whereas the CG is colored blue. (b) shows the corresponding transfer characteristic of the RFET for p- and n-type operation.*

As already described, the maximum top-gate voltage for the NS devices is ±12 V due to a different Al_2O_3 oxide quality and rougher Ge channel surface in comparison to NWs. The green-colored TGs shown in Figure 4.35a depict the PGs, which are hence used to set the polarity correspondingly to p- or n-type operation of the RFET. The blue-colored top-gate in the middle of the Ge channel is the CG, which allows to turn the transistor on and off. The transfer characteristic shown in Figure 4.35b reveals the capability of NS devices to be operated as RFETs. Applying $|V_{PG}| = 12\,\mathrm{V}$, a total on/off ratio of 2×10^3 and 2×10^2 is achieved for p- and n-type operation, respectively. Moreover, by applying $V_D = 1\,\mathrm{V}$, it was possible to achieve $J_{\mathrm{ON}} = 4284\ \mathrm{A/cm^2}$ in p-type operation and $J_{\mathrm{ON}} = 927.40\ \mathrm{A/cm^2}$ for n-type operation. Note that the saturation state of the p-type conduction is not visible as the whole transfer characteristic is shifted due to traps in the involved oxides. The off-current densities are $J_{\mathrm{OFF}} = 2.01\ \mathrm{A/cm^2}$ and $J_{\mathrm{OFF}} = 3.36\ \mathrm{A/cm^2}$ for p- and n-type operation, respectively. By utilizing the presented procedure (see Sections 3.2.5 and 4.3) to extract V_{TG}, values of $-7\,\mathrm{V}$ for the p-type operation and $-5.6\,\mathrm{V}$ for n-type operation were evaluated. A detailed comparison of the results is given in Section 4.7. To verify the concept of NS-based RFETs, thermal transfer characteristics were gathered, as shown in Figure 4.36a. Additionally, the transport regimes at $T = 295\,\mathrm{K}$ are depicted by current map plots, in Figure 4.36b.

The NS-based RFET shows the same thermal dependence as the NW-based RFET shown in Figure 4.23b. In p- and n-type operation mode the off-current increases with increasing temperature due to thermally excited charge carriers contributing to the charge carrier

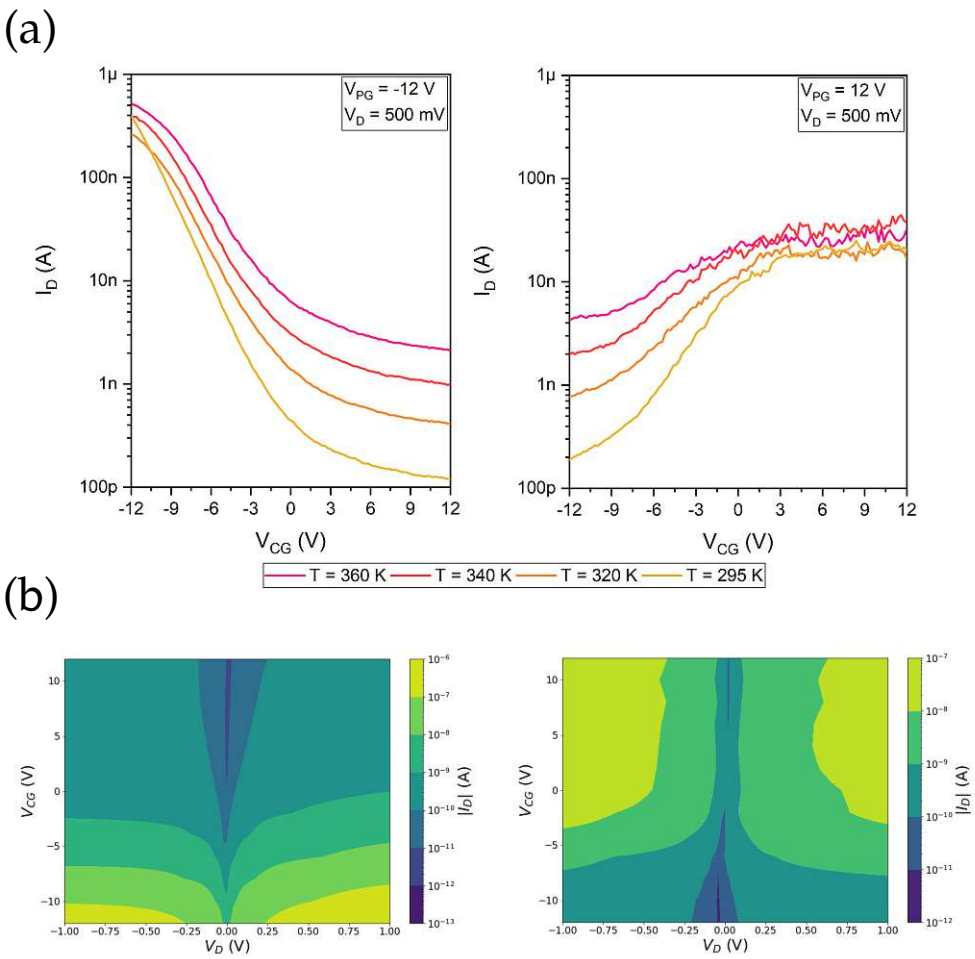

Figure 4.36: *(a) depicts the thermal performance of p- and n-type operation. (b) shows transport regimes for both, p- and n-type operation, at* $T = 295\,\mathrm{K}$.

transport. Remarkably, the on-current is not as significantly influenced at elevated temperatures, which depicts a more stable operation of the NS-based RFET device. This can be attributed to the higher contribution of tunneling *versus* thermionic emission in the on-state. As shown in Figure 4.36b, dominant transport regimes exist, correspondingly for p- and n-type operation. Moreover, the off-states of both operation regimes are clearly visible as well.

In conclusion, the RFET concept was successfully transferred to NS-based devices, realized on the base of a GeOI substrate. Thus, showing that a deterministic top-down fabrication scheme allows the realization of RFETs. To further enhance this concept and reduce supply voltages – especially of the involved top-gates, thinner high-κ oxides could be utilized. Thinning the Ge-layer, the exhibition of NDR is likely to be observed, leading to fact that the realization of a NDR-mode RFET can be fabricated for wafer-scale integration

as well. Unfortunately, the RFET concept on GeOI exhibits a strong asymmetry of the n- and p-type operation mode. This can be attributed to the relative high influence of the metal work functions of the top-gates, whereas the gate-effective surface on NW-based approaches is much smaller in comparison. Nevertheless, it was shown that a possible solution towards wafer-scale integration, enabling high-performance and low-power applications, can be realized. A detailed comparison of relevant FOMs is done in the following section, Section 4.7.

4.7 Benchmark of RFETs

To conclude the results section, a benchmark of various Ge-based RFETs is done. Therefore, the works from A. Heinzig *et al.* and J. Trommer *et al.*,[19, 21] presented in Section 2.3.1, are reconsidered. In this respect, also a Si-based RFET solution[21] is put in relation to the Ge-based RFETs. This allows to determine relevant differences from a material point of view. Moreover, in the VLS-grown Ge-NW solution by J. Trommer *et al.* different contact materials were used.[19]
As briefly depicted, a fair comparison is difficult due to the use of different geometries and therefore different supply voltages. It needs to be considered that the data sets of already published works are not available, and thus the benchmark relies on the stated values given in the corresponding papers. Hence, the extracted data from the NW- and NS-based RFET in this work were evaluated in accordance to the values in the mentioned works. Here, different architectures were evaluated. Therefore, GTG and TTG architectures are considered to depict the enhancement obtained by additional top-gates. Following parameters were extracted accordingly.

- I_{ON} and I_{OFF} of p- and n-type operation normalized to the circumference of the devices.
- J_{ON} of p- and n-type operation extracted normalized to the cross-sectional area of the devices.
- g_m of p- and n-type operation normalized to the circumference of the devices.
- V_{TH} of p- and n-type operation.
- SS of p- and n-type operation.

In the following tables, values stated in **bold** are relevant parameters for the realizied RFETs in this work.
The first parameter investigated is the on- and off-current I_{ON} and I_{OFF}, normalized to the circumference of the proposed devices. Table 4.3 shows the extracted values classified accordingly.

	p-$I_{ON}(\mu A/\mu m)$	p-$I_{OFF}(\mu A/\mu m)$	n-$I_{ON}(\mu A/\mu m)$	n-$I_{OFF}(\mu A/\mu m)$
J. Trommer (Ge)[19]	5.56	0.56e-3	0.47	1.67e-3
A. Heinzig (Si)[21]	94	0.15e-6	5.3	0.15e-6
NW GTG (Sec.4.3)	69.2	0.92e-3	0.65	-
NW TTG (Sec.4.3)	**52.8**	**0.06e-3**	**0.02**	**0.05e-3**
NS GTG (Sec.4.6)	2.22	8.62e-3	0.94	-
NS TTG (Sec.4.6)	**0.82**	**6.31e-3**	**0.16**	**0.37e-3**

Table 4.3: *Benchmark values of the on- and off-currents, I_{ON} and I_{OFF}, for p- and n-type operation.*

It needs to be considered that the work by J. Trommer extracts I_{ON} and I_{OFF} at $V_D = 2\,\mathrm{V}$, whereas the values of the other devices are extracted at $V_D = 1\,\mathrm{V}$. Remarkably, Si-based RFETs show the best performance, which can be attributed to a better injection of charge carriers by utilizing a material system ($NiSi_2$-Si-$NiSi_2$), which pins the Fermi level relatively at mid-gap. Moreover, with a band gap of $E_g = 1.11\,\mathrm{eV}$, Si enables lower off-currents. Remarkably, the off-currents of the Ge-based TTG devices realized in this work are significantly lower in comparison to the work of J. Trommer. This can be attributed to the use of a two top-gate approach of J. Trommer *et al.*, whereas in this work three top-gates are utilized. In this context, it is also evident, that the NW-based devices allow a better suppression in comparison to NS devices, which is enabled by a geometrically better gating mechanism. Another remarkable difference between NWs and NSs is that the NS-based devices exhibit a more dominant n-type conduction than the NW-based devices. From a p-/n-type symmetry point of view the devices presented in this work show the highest deviations, which can be attributed to the strong Fermi level pinning close to the valence band in the utilized Al-Ge system.

Table 4.4 shows the on-current densities J_{ON}, which are normalized to the cross-sectional area of the corresponding devices.

	p-$J_{ON}(A/cm^2)$	n-$J_{ON}(A/\mu cm^2)$
J. Trommer (Ge)[19]	38k	3500
A. Heinzig (Si)[21]	600k	34k
NW GTG (Sec.4.3)	3500k	2800
NW TTG (Sec.4.3)	**920k**	**3300**
NS GTG (Sec.4.6)	10.33k	4428
NS TTG (Sec.4.6)	**4.28k**	**927.40**

Table 4.4: *Benchmark values of the on-current density J_{ON} for p- and n-type operation mode.*

The NW-based TTG RFET shows the highest p-type on-current density in comparison to the other RFET concepts, which can be attributed again to the constituted Fermi level pinning near the valence band edge of the Al-Ge system. However, in comparison to other devices the n-type current-density is relatively low. Due to relatively large structural sizes

of the NS-approach only low current-densities are achieved. This could be improved by thinner Ge-layers of the GeOI starting material. The Si-based concept shows the best symmetry of all considered devices, which can be assigned to two issues. Firstly, the Fermi level pins closer to mid-gap and secondly, Si promotes better n-type conduction in comparison to Ge-based devices (see Table 2.1).

Next, the peak-transconductance g_m normalized to the circumference of the devices is presented for the different RFET solutions. As this parameter is mainly utilized to extract the threshold voltage V_{TH} for p- and n-type operation, only the RFET concepts are considered. Again, the values of the Ge-based RFET concept by J. Trommer were extracted at $V_D = 2\,\mathrm{V}$.

	p-g_m	n-g_m
J. Trommer (Ge)[19]	1.80 µS/µm	160 nS/µm
A. Heinzig (Si)[21]	6 mS/µm	7.50 nS/µm
NW GTG (Sec.4.3)	-	-
NW TTG (Sec.4.3)	11.90 µS/µm	39.22 nS/µm
NS GTG (Sec.4.6)	-	-
NS TTG (Sec.4.6)	0.14 µS/µm	0.28 µS/µm

Table 4.5: *Benchmark values of the transconductance g_m for p- and n-type operation mode.*

The peak-transconductance g_m shows a remarkable high value for p-type conduction of the Si-based RFET-concept, although being smaller than that of a MOSFET with similar geometries. Moreover, correlating with the high on-current shown in Table 4.3. As g_m indicates the reciprocal of the resistivity, it can be concluded that the Si-based RFET ensures better charge carrier transport. Comparing the NW-based TTG device with other Ge-based concepts, the transconductance is higher by one respectively two orders of magnitude. This can be attributed to the good tunability of the NW-based approach.
Utilizing the peak-transconductance and the extraction method explained in Section 3.2.5, the threshold voltages V_{TH} can be extracted for each device concept as depicted in Table 4.6.

	p-$V_{\mathrm{TH}}(V)$	n-$V_{\mathrm{TH}}(V)$
J. Trommer (Ge)[19]	-0.20	0.40
A. Heinzig (Si)[21]	-	-
NW GTG (Sec.4.3)	-	-
NW TTG (Sec.4.3)	**-1.40**	**1**
NS GTG (Sec.4.6)	-	-
NS TTG (Sec.4.6)	**-7**	**-5.60**

Table 4.6: *Benchmark values of the threshold voltage V_{TH} for p- and n-type operation mode.*

Remarkably, the NS-based TTG RFET shows a strong shift of the transfer characteristic,

which is evident for all investigated devices. This might be related to trap states in the relatively larger oxide surface area, and thus shifting the complete transfer characteristic. This can also be related to the large fraction of SiO_2/Ge interface traps between the BOX and device layer. Hence, leading to relatively high threshold voltages. J. Trommer *et al.* utilized Ni_2Ge-Ge contacts, and thus allowing to realize devices with lower threshold voltages and a more symmetric behavior. Nevertheless, in theory V_{TH} should be smaller in TTG-concepts in comparison to DTG-concepts.[22]

Finally, the sub-threshold slopes SS were analyzed of the considered concepts. Although the choice of V_D should not affect the SS in the thermionic regime, considering no drain-induced-barrier-lowering effects, the drain-voltages V_D need to be taken into account, as J. Trommer applied $V_D = 2\,V$, whereas $V_D = 1\,V$ in the other works.

	p-SS (mV/dec)	n-SS (mV/dec)
J. Trommer (Ge)[19]	150	215
A. Heinzig (Si)[21]	90	220
NW GTG (Sec.4.3)	600	1900
NW TTG (Sec.4.3)	**700**	**800**
NS GTG (Sec.4.6)	3600	1400
NS TTG (Sec.4.6)	**3000**	**5800**

Table 4.7: *Benchmark values of the sub-threshold slope SS for p- and n-type operation mode.*

The Ge-based RFET by J. Trommer *et al.* and the Si-based device by A. Heinzig *et al.* reached a remarkable SS. This is related to much smaller barrier heights, as in their work the Fermi level pins more mid-gap in comparison to the Al-Ge-Al devices investigated in this work. Especially, the NS-based approach shows explicitly high SS, which can be attributed to the relatively high structural sizes. It is expected that the SS highly improves by utilized TTG architectures due to the implementation of a linear displacement of the energy band landscape *versus* a barrier width modulation. However, in the scope of this work this was not evident. Therefore, additional investigations were done by utilizing the TTG device as a quasi-GTG device. The PG-contacts as well as the CG-contact were short-circuit connected to the same potential, and thus acting as a global top-gate device. To indicate any influences of the Al-Ge junctions, additional measurements were performed where V_{DS} is set to 1 V and V_{SD} is set to 1 V. Figure4.37 shows the results of these investigations.

Remarkably, the NW- and NS-based TTG device does not show any significant differences in the p-type conduction regime. However, in the n-type conduction regime two phenomena can be observed. Firstly, the curves are shifted and secondly, the slopes are slightly increasing, which is again against the expectation. These issues might can be attributed to a change of the charge state of involved traps, caused by the history of measurements. Additionally, these changes may be related to an asymmetry of the two Al-Ge contacts and its incorporated surface states. Especially, the NS-based TTG device shows a high varia-

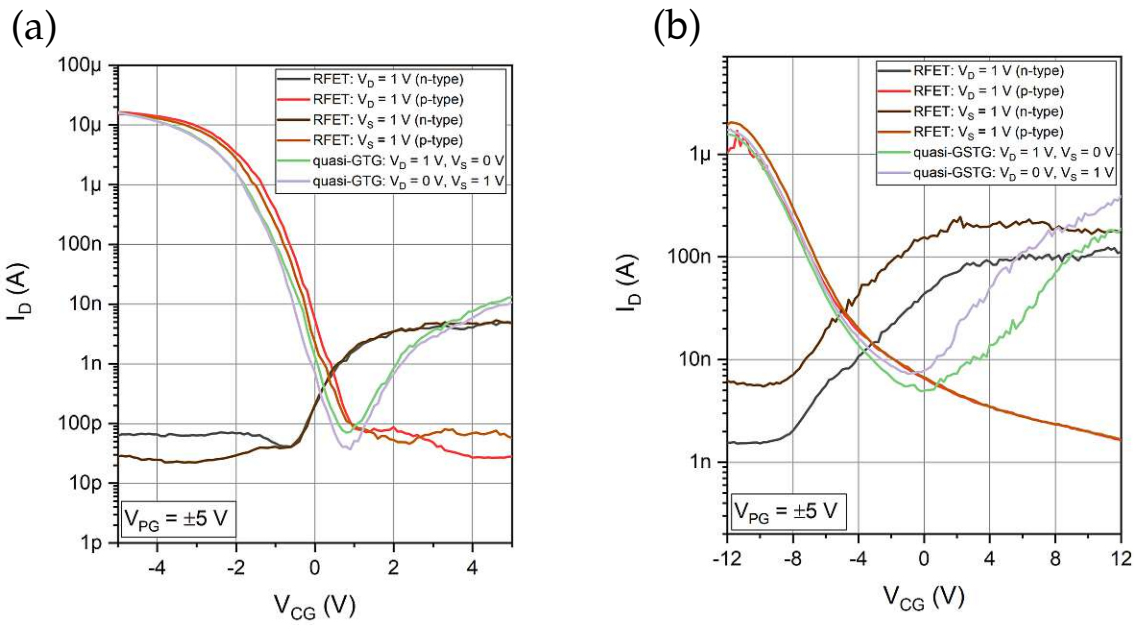

Figure 4.37: *TTG versus quasi-GTG SS comparison of (a) a NW-based TTG RFET and (b) a NS-based TTG RFET. Additionally, the devices were operated with exchanged drain- and source-contacts for sanity check the devices.*

tion, in the scenario of exchanged V_D and V_S. Hence, by the evaluation of the presented data no reliable statements can be given. Therefore, a different measurement approach might lead to more reliable and profound insights. For example, the measurements could be conducted at elevated temperatures to decrease charging/discharging time constants. Another solution is to use a pulsed measurement setup and hence reduce the influence of involved trap states.

In conclusion, a profound benchmark with existing device concepts is given, which indicates the advantages of the proposed devices as well as clearly depicts room for improvement. Especially, the strong Fermi level pinning close to the valence band highly influences the presented devices. Moreover, surface traps at the GeO_x-Al_2O_3 have a huge impact on the performance.

Chapter 5

Summary and Outlook

In this thesis a systematic study on the electrical characteristic of Al-Ge-Al heterostructures embedded in different (SB)FET architectures was carried out. Therefore, NW- and NS-based approaches were considered and evaluated from different perspectives. The main focus was to set to the realization of RFETs and NDR devices by utilizing the proposed material system. The base for all architectures is set by back-gate devices. As the charge carrier injection is of high importance for any electronic device, an experimental solution was obtained to extract the total effective activation energy to inject charge carriers into the Ge channel, and thus determining the capability of p- and n-type operation. It was shown that the proposed Al-Ge-Al system shows slightly negative effective barrier energies for the injection of holes, whereas an effective intrinsic barrier height of approximately 320 meV was evaluated. In comparison to bulk Al-Ge, this value is 120 meV higher, due to involved surface trap states. The negative barrier for holes can be explained by the strong Fermi level pinning close to the valence band of the Al-Ge system caused by surface traps of the Al-Ge system as well. Moreover,the acceptor-like behavior of the incorporated GeO_x layer also contributes to the p-dominant performance of Ge. For the injection of holes a barrier of approximately 90 meV was extracted, indicating the possibility for n-type conduction as well. Thus, various top-gate architectures consisting of one, two and three top-gates were fabricated and measured. Utilizing top-gates allows to introduce locally well-defined additional energy barriers, and hence enables to electrostatically tune the energy band landscape, leading to an explicit tunability of the device. In this context, the underlying transport mechanisms were investigated and thus the road to a well-functional RFET was set. It was shown that TTG devices exhibit the best RFET performance. This architecture comprises of two top-gates denoted as PG at the Al-Ge junctions, setting the device into p- or n-type operation. The top-gate in-between, denoted as CG, allows to turn the transistor on and off by implementing an additional barrier in the middle of the active region.
By considering Ge as the channel material, NDR features can be accessed. There are strong

indications that this effect can be attributed to the transferred-electron effect. This effect is described by scattering hot electrons from the band-gap valley to the second conduction band, which exhibits a lower electron mobility μ_n, and thus leading to the exhibition of NDR. The concept was proven for NW-based back-gate and GTG devices. It was shown that the PVCR can be tuned by the applied gate-voltage, allowing to enhance existing Ge-based NDR devices. Moreover, a profound analysis of more than twenty devices was done to extract any geometry dependencies of the NDR FOM parameters. In this context, it was shown that NWs with a length L_{Ge} of 150 nm and a diameter d_{NW} of 20 nm show the best performance for the realization of NDR devices. In comparison to existing Ge- and Si-based NDR devices a twenty times larger PVCR was observed with its maximum at 200. As the Ge-layer of the underlying GeOI substrate has a height h_{NS} of 75 nm and thus consequently exhibits a large quasi-diameter >100 nm even for the thinnest NSs, no signs of NDR were evident on NS devices. This issue can be overcome by thinner Ge-layers.
In the next step, the RFET- and NDR-concept were merged in a single type of device: the NDR-mode RFET, which is highly desired for MVL applications, due to its capability to modulate the NDR region with respect to the applied CG-voltage. By creating a serial circuit of these devices various NDRs with different characteristics can be set. In addition, these devices can also be operated as RFETs, and thus enabling a platform for logic circuits by merely utilizing a single type of device, which can also be integrated into CMOS compatible circuits.
For industrial applications wafer-scale integration is of high importance. Therefore, in an effort to show integrability, the RFET-concept was investigated on NS-based devices as well. Finally, the performance metrics of different RFET concepts were compared in a benchmark. Therefore, already published works based on Si and Ge NWs were considered for comparison with the NW- and NS-based RFETs in this work. Thus, leading to the following statements regarding further enhancement of the proposed devices. Due to the strong Fermi level pinning of the Al-Ge system close to the valence band good injection of holes is ensured, whereas the n-type charge carrier transport is inhibited. This issue could be overcome by the utilization of different contact materials as well as different channel materials. However, it needs to be considered that diffusion coefficients may differ and hence prevents well defined metal-semiconductor junctions. Moreover, utilizing other metals may lead to the formation of germanide contacts, which exhibit a high variability. This again influences the reliability and fabrication procedure of the underlying devices. Another opportunity is to induce strain and hence allows to increase the symmetry of p- and n-type conduction. In the context of symmetry, also different interface oxides may contribute to a more symmetric behavior. Importantly, desorption of the native GeO_x layer needs to be considered for further enhancement of the devices. This would also contribute to a less pronounced hysteresis, and thus leading to a more reliable performance. In this respect, the formation of Ge oxy-nitride or Si capping shall be considered as well. From a channel point of view SiGe alloys may lead to a more balanced n- and p-type operation, as the electron and hole mobility can be tuned by the Si-to-Ge concentration in the alloy.
Regarding NS devices obtained from GeOI, thinner Ge-layers would allow to access the NDR regime, consequently enabling the NDR-mode RFET approach, and thus ensuring

the realization of NDR-mode RFETs for wafer-scale integration. Moreover, the top-gate oxide could be reduced, and hence allowing to reduce the top-gate supply voltages. From a device integration point of view the presented platforms allow the realization of logic and MVL circuits, which is missing for the proposed devices so far.

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List of Abbreviations

Al	Aluminum
Al_2O_3	Aluminum Oxide
ALD	Atomic Layer Deposition
Au	Gold
BG	Back-Gate
BOX	Buried Oxide
CG	Control-Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CNL	Charge Neutrality Level
Cu	Copper
C/V	Capacitance-Voltage
DOS	Density of States
DTG	Dual Top-Gate (Device)
EBL	Electron Beam Lithography
EDX	Electron Diffraction X-ray Spectroscopy
eSBH	Effective Schottky Barrier Height
FET	Field-Effect Transistor
FOM	Figure-of-Merit
GaAs	Gallium Arsenide
GaN	Gallium-Nitride
Ge	Germanium
GeH_4	Germane
GeOI	Germanium-On-Insulator
GeO_x	Germanium Oxide
GTG	Global Top-Gate (Device)
H_2O	Water
He	Helium
HF	Hydrogen Fluoride
HfO_2	Hafnium Oxide
HI	Hydroiodic Acid
InAs	Indium Arsenide
InP	Indium Phosphorus

InSb	Indium Antimony
I/V	Current-Voltage
LaYO	Lanthanum Yttrium Oxide
MOBILE	Monostable-Bistable Transition Logic Element
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MVL	Multi-Valued Logic
NDR	Negative Differential Resistance
NG	No Gate (Membrane)
Ni	Nickel
NiGe	Nickel Germanium
NiSi	Nickel Silicon
NS	Nanosheet
NW	Nanowire
PG	Polarity-Gate
PVCR	Peak-to-Valley Current Ratio
RFET	Reconfigurable Field-Effect Transistor
RIE	Reactive Ion Etching
RTA	Rapid Thermal Annealing
RTD	Resonant Tunneling Diode
SBFET	Schottky Barrier Field-Effect Transistor
SBH	Schottky Barrier Height
SEM	Scanning Electron Microscopy
Si	Silicon
Si_3N_4	Silicon Nitride
SIG	Single Interface (Top-)Gate (Device)
SiGe	Silicon Germanium
SiO_2	Silicon Dioxide
SMU	Source-Measure-Unit
SOI	Silicon-on-Insulator
SS	Sub-Threshold Slope
STG	Single Top-Gate (Device)
TEM	Transmission Electron Microscopy
TG	Top-Gate
Ti	Titanium
TTG	Triple Top-Gate (Device)
VLS	Vapor-Liquid-Solid
VLSI	Very-Large-Scale Integration
VSU	Voltage-Source-Unit
ZrO_2	Zirconium Oxide

List of Symbols

A^*	Richardson constant
a_B^*	Exciton Bohr Radius
$\mathrm{A_{NS}}$	Cross-sectional area of NSs
$\mathrm{A_{NW}}$	Cross-sectional area of NWs
D	Diffusion Coefficient
$\mathrm{d_{NS}}$	Quasi Cross-section of NSs
$\mathrm{d_{NW}}$	Cross-section of NWs
E_c	Conduction Band Energy
E_C	Break-down (Electric) Field
E_F	Fermi Energy
E_{F_m}	Fermi Energy of the Metal
E_{F_s}	Fermi Energy of the Semiconductor
E_g	Band gap Energy
E_{SB}	Total effective activation energy
E_v	Valence Band Energy
E_{vac}	Vacuum Energy
G	Conductance
g_m	Transconductance
$\mathrm{h_{NS}}$	Height of NSs
I	Current
I_P	Valley-Current (NDR)
I_V	Peak-Current (NDR)
J	Current Density
J_P	Peak-Current Density (NDR)
k	Wave Vector
k_B	Boltzmann Constant
$\mathrm{L_{Ge}}$	Ge-segment Length
m_0	Rest Mass of Electrons
m^*	Effective Mass of Electrons
μ_n	Electron mobility
μ_p	Hole mobility
ϕ_{Bn}	(Schottky) Potential Barrier for Electrons

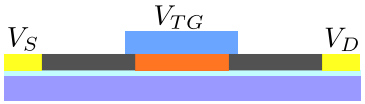
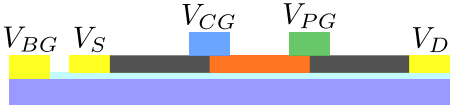
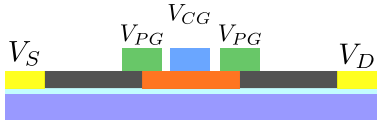
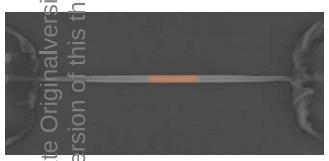
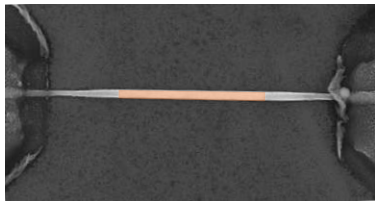
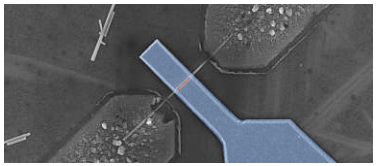
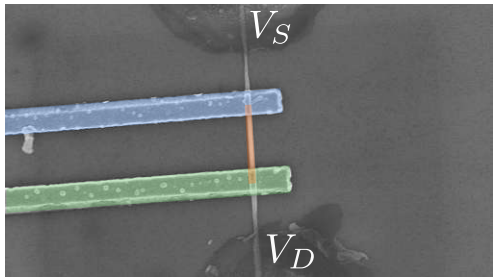
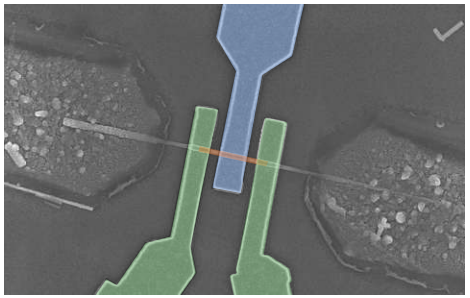
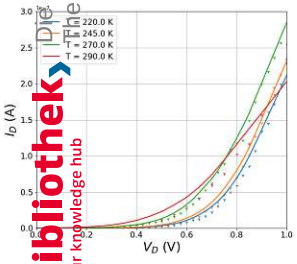
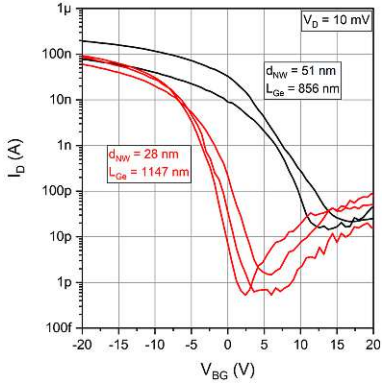
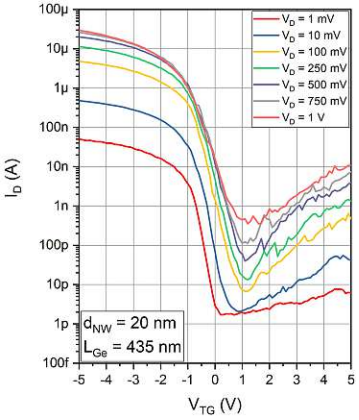
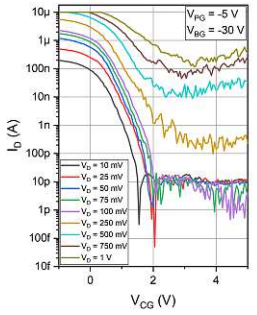
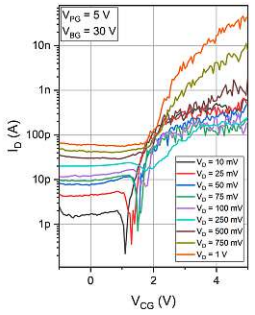
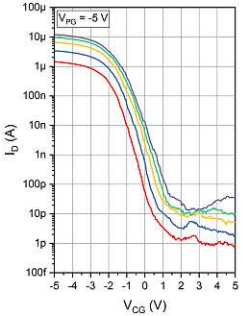
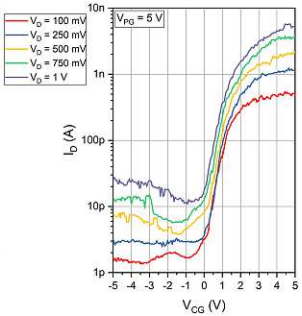
ϕ_{Bp}	(Schottky) Potential Barrier for Holes
ϕ_m	Metal Work Function
ϕ_s	Semiconductor Work Function
q	Elementary Charge
r_{diff}	Differential Resistance
R_S	Series Resistance (NDR)
T	Temperature
V	Voltage
V_{BG}	Back-Gate Voltage
V_{bi}	Built-in Voltage
V_{CG}	Control-Gate Voltage
V_D	Drain Voltage
V_{DS}	Drain-Source Voltage
V_P	Peak-Voltage (NDR)
V_{PG}	Polarity-Gate Voltage
V_{PT}	Plateau-Voltage (NDR)
V_S	Source Voltage
V_{TG}	Top-Gate Voltage
V_{TH}	Threshold Voltage
V_V	Valley-Voltage (NDR)
w_d	(Schottky) Depletion Width
W_{NS}	Width of NSs
χ	Electron Affinity

Appendix A

Overview of Architectures

The appendix consists of an overview of most important architectures investigated in this work. It shall summarize their general characteristics and capabilities of operation. As shown on the next page, the schematic architecture, SEM images and transfer characteristics are shown and classified accordingly.

Remarks:
For the membrane (no gate) device the I/V characteristic is used, as no transfer characteristic can be measured. Regarding the top-gate architectures, it needs to be considered that the top-gate oxides compromise of a 22 nm Al_2O_3 layer. In the shown images and figures, NW architectures are used.

Membrane (NG)	Back-Gate (BG)	Global Top-Gate (GTG)	Dual Top-Gate (DTG)	Triple Top-Gate (TTG)
				
- no gate involved - only NW platform	- V_{BG} gates device - NW and NS platform	- V_{TG} gates device - NW and NS platform	- V_{CG} gates device - V_{PG} sets polarity (n- or p-type) - NW and NS platform	- V_{CG} gates device - V_{PG} sets polarity (n- or p-type) - NW and NS platform
				
I/V characteristic 			 	 

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I declare, that I have authored the present work independently according to the code of conduct, that I have not used other than the declared sources and that I have explicitly marked all material quoted either literally or by content from the used sources. This work was not yet submitted to any examination procedure neither in Austria, nor in any other country.

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Vienna, July 2021 .....

Raphael Böckle