Dissertation

Microstructural and electrical characterization of Si/4H-SiC heterojunction diodes

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Institut für Sensor- und Aktuatorsysteme
Technische Universität Wien

Dipl. Ing. Fabian Triendl – 01226462

Supervision:
Univ. Prof. Dr. Ulrich Schmid

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Betreuer:

Prof. Ulrich Schmid, TU Wien

Gutachter:

Prof. Walter Weber, TU Wien

Prof. Martin Eickhoff, Uni Bremen

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Abstract

With the growing demand for high power, highly efficient, and fast switching power electronics, silicon carbide (SiC) is besides gallium nitride (GaN) the substrate material of choice due to its outstanding properties. For this stongly growing field of application SiC offers great potential, as this compound semiconductor has a wide band gap, a high thermal conductivity, a high mechanical strength as well as a high chemical resistance. In the last years, SiC wafers entered a price regime suited even for mass production and became available in up to 6-inch diameter with very low defect densities. Almost all conventional silicon (Si) based devices could be replicated in SiC technology. One of the most important and quite simple structures is the metal-semiconductor, or Schottky contact. This thesis investigates the potential when combining the well-established semiconductor Si with the wide band gap semiconductor 4H-SiC. The use of Si as contact material on 4H-SiC allows an adjustment of the Schottky barrier height in a wide range, by changing the Si doping concentration. In addition, the temperature stability and the overall temperature budget during device fabrication are enhanced, since most metal contacts alloy with SiC forming silicides, whereas Si is stable on SiC up to 1000 °C and even above. Heterojunction diodes based on Si/4H-SiC, which act as Schottky junctions, are fabricated using different growth and interface preparation techniques and are characterized electrically in a wide temperature range.

The first step was to investigate the growth of Si on monocrystalline 4H-SiC. By applying sputter-deposition techniques at temperatures below 600 °C only amorphous Si is grown. Investigations on the influence of different post deposition annealing steps at temperatures up to 1100 °C were performed to achieve recrystallization of the Si thin films on 4H-SiC. A different approach to enable the realization of low-temperature crystalline Si on 4H-SiC is metal-induced crystallization. By applying aluminum serving as crystallization promotor, the recrystallization temperature of Si on 4H-SiC could be reduced to about 200 °C. Disadvantageous is, however, that the homogeneity of the achieved films still needs further improvement. The direct growth of crystalline Si was studied using low-pressure chemical vapor deposition. A strong influence of the deposition temperature on the grain size and the preferred growth orientation is observed. Microstructural investigations of the samples were mainly performed with state-of-the-art scanning electron microscopy, transmission electron microscopy, and X-ray diffractometry.

Apart from the different growth techniques, the influence of interface pre-conditioning is investigated. Argon ion bombardment of the 4H-SiC surface prior to Si deposition shows promising results of Schottky barrier height tuning. Also the influence of amorphous a-SiC:H interface layers, with different thickness values below 4 nm, on the performance of conventional Ti/4H-SiC Schottky diodes was investigated. The impact of Schottky barrier inhomogeneities was found to be strong at p-Si/4H-SiC heterojunctions due to their large barrier height. A new fitting procedure based on Tung's model was applied to extract the density of the interface inhomogeneities in a wide temperature range.

All in all, the findings of this thesis proved the well-rectifying properties of the Si/4H-SiC heterojunction and the manufacturability using standard silicon micro technologies. Additionally, many theoretical and practical results of the growth and the electrical behavior significantly strengthened the knowledge about the Si/4H-SiC heterojunction interface.

Zusammenfassung

Durch die steigende Nachfrage nach leistungsstarken, hocheffizienten und schnell schaltenden Halbleiterbauelementen hat sich Siliziumkarbid (SiC) neben Galliumnitrid (GaN) als Leistungshalbleiter der Zukunft etabliert. Auf Grund seiner hohen Bandlücke, seiner hohen thermischen Leitfähigkeit, seiner hohen elektrischen Durchbruchfeldstärke, seiner hohen mechanischen Festigkeit als auch auf Grund seiner hohen chemischen Resistenz ist SiC für dieses stark wachsende Anwendungsgebiet hervorragend geeignet. Das Preisniveau und die Defektdichte von SiC Substraten bis zu 6 Zoll Durchmesser sind in den letzten Jahren so weit gesunken, um für die Massenproduktion verwendet werden zu können, sodass die meisten Silizium (Si) Bauelemente mittlerweile auch auf SiC Basis realisiert werden konnten. Eine der einfachsten, jedoch auch meist verwendeten Strukturen in der Halbleitertechnik ist der Metall-Halbleiter- oder Schottky-Übergang. Ziel dieser Doktorarbeit ist das Zusammenführen der etablierten Si-Technologie mit 4H-SiC. Die Verwendung von Si als Kontaktmaterial auf 4H-SiC erlaubt die Einstellung der entstehenden Schottky-Barriere in einem weiten Bereich durch Variation der Si-Dotierung. Zusätzlich ist die Si/4H-SiC Kombination bis über 1000 °C sehr temperaturstabil. Metallkontakte legieren oft schon bei weit niedrigeren Temperaturen mit SiC und bilden Silizit-Verbindungen. In dieser Arbeit werden so genannte „Heterojunction-Dioden" hergestellt und charakterisiert. Unterschiedliche Abscheide- und Kristallisationsmethoden von Si auf 4H-SiC werden untersucht und dabei ihr Einfluss auf die elektrischen Eigenschaften des Überganges ausgewertet.

Der erste Schritt war die Untersuchung des Silizium Wachstums auf monokristallinem 4H-SiC. Mit Sputterabscheidung bei Temperaturen unterhalb von 600 °C können nur amorphe Siliziumschichten abgeschieden werden. Die Rekristallisation des amorphen Si auf 4H-SiC wurde daher bei unterschiedlichen Temperaturbehandungen bis 1100 °C untersucht. Ein anderer Ansatz, um kristallines Si bei viel niedrigeren Temperaturen zu erhalten, besteht im Metall induzierte Kristallisieren. Durch die Verwendung von Aluminium, welches als Kristallisationskatalysator wirkt, kann die Kristallisationstemperatur von Si auf etwa 200 °C reduziert werden. Die Homogenität und damit die Qualität der mit diesem Verfahren erzielten Siliziumfilme ist aufgrund des teilweise noch am SiC-Substrat haftenden Aluminiums verbesserungswürdig und bedarf weiterer Optimierung. Das Abscheiden von kristallinem Si wurde mittels der chemischer Gasphasenabscheidung bei niedrigen Kammerdrücken untersucht. Ein starker Einfluss der Abscheidetemperatur auf die Korngröße und die Orientierung der Si-Schicht wurde beobachtet. Für die Untersuchung der Mikrostruktur wurden hauptsächlich Elektronenmikroskopie und Röntgenbeugung verwendet.

Zusätzlich zu unterschiedlichen Abscheideverfahren wurde auch der Einfluss der Probenvorbehandlung vor der Abscheidung untersucht. Die Behandlung der 4H-SiC Oberfläche mit Ar^+ Ionen vor der Si Abscheidung zeigt einen erfolgversprechenden Einfluss auf die Barrierenhöhe und die Qualität der Dioden. Weiters wurde der Einfluss von sehr dünnen, nur wenigen nm dicken a-SiC:H Interfaceschichten auf das elektrische Verhalten von konventionellen Ti/4H-SiC Dioden untersucht. Inhomogenitäten der Schottky Barriere zeigten einen besonders starken Einfluss bei p-Si/4H-SiC Dioden. Ein neuer Ansatz, der auf dem Tung Modell basiert, wurde vorgestellt, um die elektrischen Messungen auf Grund der Inhomogenitäten an der Grenzfläche theoretisch beschreiben zu können. Deren Dichte konnte dadurch in einem weiten Temperaturbereich extrahiert werden.

Die in dieser Doktorarbeit durchgeführten Untersuchungen betätigt die gleichrichtenden Eigenschaften der Si/4H-SiC Kombination und die Herstellbarkeit mittels Standard Silizium Mikrotechnologie. Viele praktische und theoretische Ergebnisse zum Wachstum und der elektrischen Eigenschaften liefern neues Wissen über die Si/4H-SiC Materialkombination.

Contents

1 Introduction

The demand for faster, smaller, and more efficient electronics is larger than ever. Especially in terms of power electronics, the increasing market of renewable energy and electric transportation systems shows a strong interest in new technologies, offering an enhanced efficiency. From the 113 PWh of worldwide total energy consumption in 2019, about 23% was used in electric form [1]. This fraction continuously increased over the last years. In 1973 only 9% were consumed and transferred electrically. Being able to increase the efficiency of electrical power conversion only by a small fraction will therefore have a major potential in saving energy. Until now, electronic devices in silicon (Si) technology served the market needs for both conventional and power electronics. Other semiconductor materials already took over Si in some applications, e.g. gallium arsenide for high-frequency amplifiers or optoelectronics.

For power electronics, wide band gap semiconductors offer a big potential, owing to their lower intrinsic carrier concentration. Especially silicon carbide (SiC) further scores due to its high thermal conductivity and high breakdown field strength. Therefore, the use of SiC as semiconductor material for electronics is extensively researched. The potential of SiC components, such as diodes and switches, are diverse and include emerging applications such as lightning, power factor correction, solar inverters, motor drivers, DC/DC-converters, and uninterrupted power supplies. Many companies are offering SiC-based components and many more are conducting research activities. Among them are companies like Infineon, Cree, Rohm, STMicroelectronics, Toshiba, and Mitsubishi. Especially the electric transportation sector (car, railways, e-bikes,…) and solar industry are examples, where SiC microelectronic devices can be an accelerating factor towards a more climate-neutral future. Toyota has already shown an all SiC power control unit for hybrid electric vehicles which increased the fuel efficiency by 5% (the goal is 20%) and a size reduction of up to 80% compared to Si-based units [2]. With the Model 3, Tesla also started to use full SiC inverters based on STMicroelectronics metal oxide field effect transistors (MOSFETs) [3]. SiC modules like inverters are available as all SiC modules, where all active power components are made in SiC, and as hybrid modules, where the switches are Si components, and only the diodes are done in SiC technology. All SiC modules offer the highest efficiency, followed by hybrid modules, but both approaches outperform all Si modules [4]. For solar energy conversion, inverters are necessary as well. General Electric introduced an all SiC inverter showing up to 99% conversion efficiency [2]. These were just some examples of SiC electronics that are already on the market, resulting in both a reduction of power loss and a lower size/weight. Nevertheless, the costs of these SiC microelectronic devices are still much higher than those for Si counterparts. Although the SiC components are more expensive, the overall system costs may be lower when applying SiC technology, as passive components can be reduced in size as higher switching frequencies are possible. Also, the thermal design is easier, resulting in compacter modules.

Yet, there is still much research to be done both theoretically and experimentally. SiC requires modified or even new fabrication routes compared to those being well-establised in Si microtechnology. Further research is not only required to improve the efficiency even more and reduce the costs but also some electronic components have not been reproduced in SiC on a commercial level, like the insulated gate bipolar transistor (IGBT). Furthermore, the packaging of the semiconductor dies needs to be improved to get the full potential of the substantially higher maximum junction temperature of SiC.

1.1 Goals of this thesis

In this thesis, the rather novel material combination of the well-established Si and the wide band gap semiconductor 4H-SiC is researched with the goal of fabricating rectifying heterojunction diodes (HJDs). Using highly doped Si contacts, HJDs can be produced that are similar to Schottky diodes in
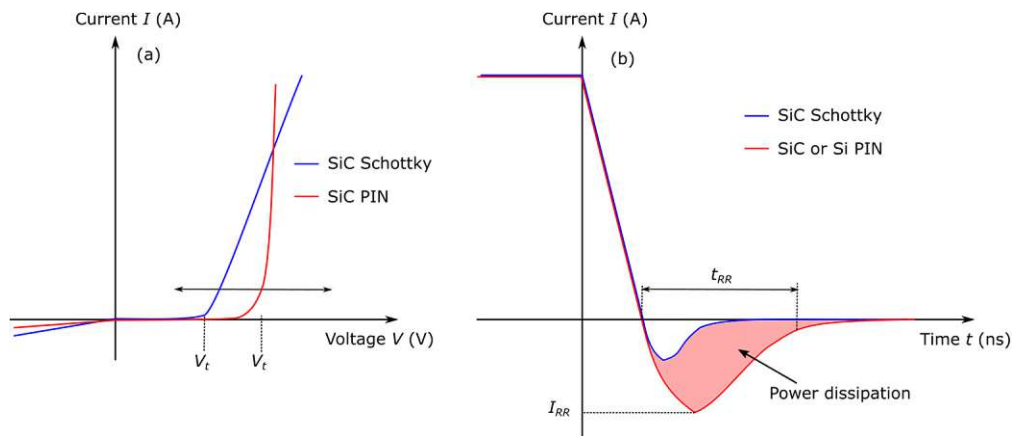
Figure 1.1: (a) Typical current-voltage characteristic of a SiC Schottky and a SiC PIN diode. (b) Forward-reverse current transition, showing the reverse recovery current of a Schottky and a PIN diode.

terms of current flow over the junction. The Schottky diode was the first commercially available SiC component and offers many advantages over the classic Si PIN diode, which is the competitor in terms of voltage and power rating [5]. Although introduced a long time ago, the proper fabrication of SiC Schottky diodes is still under research. Most common metallizations only result in rather high Schottky barrier heights (SBH) > 0.9 V. Furthermore, the resulting SBH is above-average sensitive to the deposition technique and to thermal treatments [6].

SiC PIN diodes, offering even higher blocking voltages than SiC Schottky diodes, are commercially available today. Voltages of several kilovolts have been demonstrated [7]. SiC Schottky, SiC PIN, Si PIN diodes, and some variations of them are the main diodes for high voltage power electronics. Figure 1.1a shows an illustration of the current-voltage (IV) characteristic of both, a SiC Schottky and a SiC PIN diode. As can be seen, depending on the intended application both diode designs have their advantages. Due to the large band gap of SiC, the turn-on or threshold voltage V_t of PN and PIN junctions is with about 3 V rather high, whereas Schottky diodes already start to conduct a significant current at much lower forward voltages due to typical barrier heights in the range of 0.9 to 1.5 V [6]. On the contrary, the on-resistance of Schottky diodes is much larger due to the low doped drift region, which results in a lower steepness in the IV curve. Although PIN diodes also have a large, low doped drift region, the resistance is low due to conductivity modulation [4], Therefore, PIN diodes offer a lower power loss at higher current densities. Also, their reverse leakage current is lower. For fast switching applications, Schottky diodes can have a huge advantage due to the lower reverse recovery current and
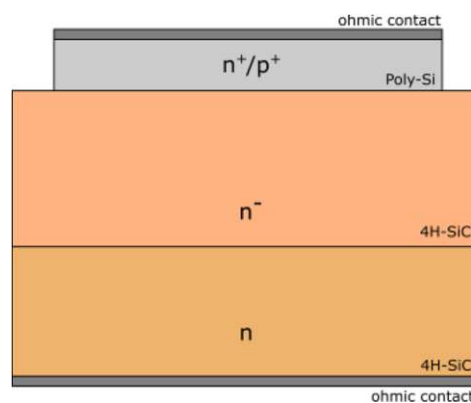
Figure 1.2: Schematic cross section of a Si/4H-SiC heterojunction diode.

time. Figure 1.1b illustrates the current through a diode when switched from a conducting state to a reverse-biased state at $t = 0$ s. The faster recovery time results from the unipolar nature of a Schottky junction. The switching losses scale linear with frequency and therefore Schottky diodes can reduce the power dissipation significantly at high frequencies. Modern SiC Schottky diodes are combining some of the advantages of the Schottky and the PN junction in the so-called junction barrier Schottky (JBS) diode.

Although already very mature, the demand for a wider variety of SBHs and higher thermal as well as longtime stability of the junction is given. Also, lower fabrication costs, especially reducing high-temperature steps are very welcomed, especially by industry.

The Si/4H-SiC HJD, as schematically illustrated in Figure 1.2, tries to replace the metal contact with a semiconductor contact. The Si top contact has the advantage of an adjustable SBH, via the Si doping concentration, although only rather highly doped Si contacts should be used to achieve both high breakdown voltages and a Schottky junction with thermionic emission current flow. Another advantage of Si is the large variety of possible deposition techniques. Furthermore, the thermal stability of Si/SiC is extremely high as alloying between the two semiconductors is unlikely.

The Si/4H-SiC material combination is therefore evaluated in this thesis, in terms of interface quality and its diode characteristics, to estimate the potential of doped Si as a contact material for the next generation of SiC Schottky diodes.

1.2 Structure of this thesis

After the introduction part, Chapter 2 will cover the fundamental material properties of SiC together with a historical timeline of SiC up to the present, including the state of the art. Furthermore, all the physics necessary for understanding the formation of a Schottky barrier and to calculate the key physical quantities within a band diagram are given in a general way, applicable to all semiconductors, but with the specific material properties for Si and SiC. More fundamentals are given in Chapter 3, which covers the basics of the used facilities and instruments for film deposition and characterization. Furthermore, the evaluation techniques for contact resistance and diode properties are described.

The next three chapters are dealing with the results and discussion of the conducted experiments. In Chapter 4, the experiments regarding Si thin film growth with sputter-deposition and low-pressure chemical vapor deposition (LPCVD) and the corresponding microstructural investigations are covered. Chapter 5 deals with metal-induced crystallization of the Si top layer. Finally, Chapter 6, includes all experimental work for diode fabrication and their electrical characterization, including different Si deposition techniques and surface pre-treatment methods. Additionally, an approach is included in this chapter where classic Ti/4H-SiC Schottky diodes are compared with those having an ultrathin a-SiC:H interlayers integrated between Ti top metallization and the 4H-SiC substrate.

Chapter 7 summarizes the findings of this thesis and gives suggestions for further experiments. A list of all used symbols followed by a list of the references is provided in the appendix.

2 Fundamentals and state of the art

In this chapter, the theoretical basics for the experimental and analytical methods used in this thesis are described. It starts with the material properties of silicon carbide together with a historical review, covers the basic semiconductor physics, and describes in more detail, the various types of semiconductor contacts and the involved physics. Whenever the amount of detail would exceed the scope of this thesis, recommended literature is given for further reading.

2.1 Silicon carbide - SiC

Silicon carbide is a group IV-IV semiconductor and as such is a compound of silicon and carbon in a ratio of one to one. Depending on the crystallographic arrangement of the Si and C atoms different polytypes of SiC arise (see Section 2.1.1). Depending on the polytype, the material offers a wide range of electrical and mechanical properties. Especially in terms of breakdown voltage and thermal conductivity SiC outperforms the well-established silicon and makes it very suitable for power electronic applications. Due to its band gap in the range of 2.4 to 3.3 eV, depending on the polytype, SiC is a so-called wide band gap semiconductor. For comparison Table 2.1 provides the band gap value and type of the band gap minima for various semiconductors.

SiC is used as an abrasive since the end of the 19th-century due to its extreme hardness and the first electrical experiments on SiC crystals date back more than 100 years. Until now, almost every basic Si device was realized using SiC [2]. However, not only microelectronic devices are emerging, but also high-temperature heating elements and micro-electro-mechanical systems based on SiC were developed due to the excellent material properties SiC offers. A detailed historical background on the evolution of SiC is given in Section 2.1.2.

Table 2.2 gives an overview of some material properties of the three most important SiC polytypes used in microelectronic as well as silicon for comparison. Remarkable are the higher band gap values by almost a factor 3, the more than twice the thermal conductivity, and the 10 times higher breakdown field strength. These properties are especially suitable for power electronics, where high field strength and power densities occur. The large band gap results in reduced leakage currents even at elevated temperatures due to the lower intrinsic carrier concentration. The high thermal conductivity enables a faster heat transfer out of the active region and therefore a higher power density.

Table 2.1: Band gap value and type of band gap minima of some commonly used semiconductors. [8]

Semiconductor	E_g (eV) @ 300 K	Type of band gap minima
Ge	0.67	indirect
Si	1.12	indirect
GaAs	1.43	direct
4H-SiC [3]	3.26	indirect
GaN	3.4	direct
AlN [4]	6.03	direct
C (diamond) [5]	5.5	indirect

Table 2.2: Selection of material properties of the three most important SiC polytypes and silicon at 300 K. [8]–[18]

	3C-SiC	6H-SiC	4H-SiC	Si
Band gap E_G (eV)	2.39	3.02	3.26	1.12
Electron affinity χ (eV)	4	3.45 - 4	3.1 to 3.6	4.05
Breakdown field E_b (MV/cm) @ $N_D = 10^{17}$ cm^{-3}	> 1.5	$\perp$ c-axis > 1 $\parallel$ c-axis 3.2	3	0.3
Permittivity ε_0 (low frequency)	9.75	$\perp$ c-axis 9.76 $\parallel$ c-axis 9.98	$\perp$ c-axis 9.76 $\parallel$ c-axis 9.98	11.8
Density ρ (g/cm^3)	3.21	3.21	3.21	2.33
Electron mobility $\mu_{n,max}$ (cm^2/Vs)	800	$\perp$ c-axis 420 $\parallel$ c-axis 60	$\perp$ c-axis 800 $\parallel$ c-axis 900	1450
Hole mobility $\mu_{p,max}$ (cm^2/Vs)	40	100	125	480
Thermal conductivity κ (W/cmK)	3.2	3.6	3.7	1.5
Melting point T_m (K)	2830	2830	2830	1415
Typical donor atoms and ionization energies ΔE_D (meV) (hexagonal and cubic lattice site)	N: 50	N: 85, 140 P: 80,110	N: 50, 92 P: 54,93	P: 46 As: 54
Typical acceptor atoms and ionization energies ΔE_A (meV)	Al: 200	Al: 240 B: 300	Al: 200 B: 285	B: 44 Al: 69

Another important feature of SiC is that is the only compound semiconductor forming the native oxide SiO$_2$ when oxidized [19]. The much higher breakdown field strength allows SiC to be used for unipolar devices (e.g. Schottky junctions) up to very high voltages, where the Si technology can only compete in a PIN diode arrangement with large, low doped, drift regions having long reverse recovery times and lower working temperatures [2], [20]. The longer reverse recovery times increase the losses linearly with switching frequency. Using SiC Schottky diodes, power supplies can be operated at much higher switching frequencies, allowing for higher efficiency and lower volume. All these aspects promote SiC-based devices and modules to achieve much higher efficiencies compared to Si counterparts, resulting in low energy consumption, thus serving as a substantial part in the transformation to a fossil-fuel-free world.

Besides these benefits, there are also a few disadvantageous material properties. The very high melting point and chemical resistance make SiC a perfect material for harsh environments but cause challenges in the manufacturing process. Conventional semiconductors (e.g. Si and Ge) are usually grown out of the molten material. For SiC pressures higher than 10^5 atm and temperatures > 3200 °C are needed to create a stoichiometric melt. A production under these conditions is not profitable outside research
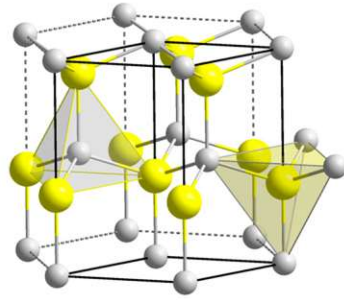
Figure 2.1: Lattice structure of α-moissanite, a naturally occurring silicon carbide. It is most frequently found in the wurtzite lattice structure which corresponds to the 2H polytype. The bilayers are along the (0001)-layer (horizontal plane). In this polytype they are stacked in A, B sequence. Si-atoms: big-yellow, C-atoms: small-grey.

facilities. Today the most commonly used technique for growing monocrystalline SiC is a modified Lely method, which accounts for more than 90% of the supplied SiC wafers [21], [22]. SiC powder is heated to temperatures > 2000 °C where it starts to sublimate. The vaporized SiC particles (Si, SiC_2 and Si_2C) condense on a cooler seed wafer at the top of the chamber. Other important technologies for SiC growth are high-temperature chemical vapor deposition (CVD), liquid phase epitaxy, and sublimation epitaxy [23]. For thermal oxidation of SiC, very high temperatures are needed, otherwise, the oxidation rate is very low, and diffusion processes are almost impossible in conventional quartz furnaces. The high temperatures, usually in excess of 1600 °C, also require precautions to reduce the Si out-diffusion and hence graphitization of the SiC surface [24], [25]. Etching and grinding rates are much lower compared to Si and the growth of epitaxial layers is a very expensive process and requires much expertise. In addition, special off-axis wafers are required to preserve the polytype of epitaxial layers [19]. Also, the doping of SiC is challenging due to the rather deep defect centers of most dopant elements and the high activation energies needed to make them electrically active [19]. For n-type doping, nitrogen has a rather shallow energy level on hexagonal carbon sites of about 50 meV, comparable to phosphorus in silicon with 46 meV. But for p-type doping, aluminum is the best choice having an ionization level around 200 meV resulting in incomplete ionization at room temperature. All in all, some of the material parameters listed in Table 2.2 are still inaccurate and must be used with care, compared to the well-investigated semiconductor silicon. The crystal structure of all SiC polytypes besides 3C results in an anisotropy of some material properties, which must also be considered.

2.1.1 Crystal structure and polytypism

Like most composite materials SiC crystallizes in many different lattice structures. This property is called polymorphism. A special case of polymorphism is polytypism. The different polytypes arise from different stacking sequences of identical close-packed planes. The uniqueness of SiC is that more than 200 different polytypes are already identified. Silicon carbide is composed out of stacked tetrahedral layers, whereas the distance between the Si-C atoms is very close along a certain direction. These layers are referred to as Si-C-bilayers. In Figure 2.1 the bilayer structure can be illustrated as an example of a moissanite crystal, which corresponds to the 2H polytype. These bilayers are identical in two dimensions but differ in the stacking sequence in the third dimension (along the c-axis). Figure 2.2 shows a top view of a SiC bilayer structure along with all three possible atom configurations (A, B and C) a neighboring layer can have. On top of a layer with A-configuration, the next layer can be placed in B or in C-configuration, and so on. In the following figures, the Si and C atoms are combined as a SiC atom pair for convenience. The different stacking sequences of A,B or C layers lead to one cubic polytype (3C-
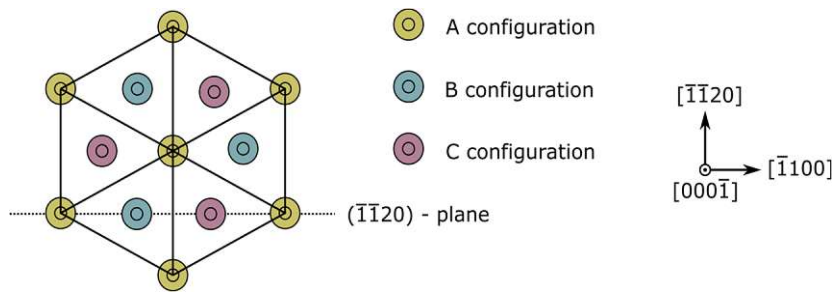
Figure 2.2: Top view of hexagonal close packed SiC indicating the 3 possible layer positions A, B and C. For convenience, the Si-C tetramers have been replaced by SiC pseudo atoms.

SiC or β-SiC), plenty of hexagonal polytypes (2H-, 4H-, 6H-,... or α-SiC) and rhombohedral polytypes (15R-, 21R-, 27R-SiC, etc.) [26]. In this so called Ramsdell notation, the number stands for the number of layers until the stacking sequence repeats itself, and the letter stands for the corresponding type of the crystallographic lattice. Figure 2.3 shows the stacking sequence of five important polytypes. The 2H hexagonal lattice structure with AB… sequence is called wurtzite crystal structure and the ABC… sequence of the 3C polytype corresponds to a zinc-blende structure, whereas the Si and C atoms form two interpenetrating face-centered cubic lattices. All the other SiC polytypes are combinations of zinc-blende and wurtzite structures. 4H-SiC has a cubic to hexagonal ratio of 1:1, 6H-SiC 2:1, and 15R-SiC a ratio of 3:2.

For the notation of crystallographic orientations, Miller indices are used. Round brackets identify a specific lattice plane e.g. (311) and curved brackets a set of symmetrically equivalent planes e.g. {100} ≡ (100), (010), (001), (-100), (0-10) or (00-1). Directions are notated by square brackets e.g. [100] is normal on the (100) plane, and symmetrically equivalent directions by angle brackets e.g. <100>. Figure 2.4 shows high-resolution transmission electron microscopy images of a 4H-SiC crystal in two different orientations, 90° oriented to another. The insets are the corresponding fast Fourier transformation (FFT) patterns of the images, respectively. In both images, the [0001] direction (c-axis) points upwards. In Figure 2.4a, which has the same orientation as the schematic illustrations in Figure 2.3, the stacked nature of the 4H-SiC polytype is clearly visible, although no difference between Si and C atoms is observable due to their proximity. In Figure 2.4c, no stacking sequence, and no atomic
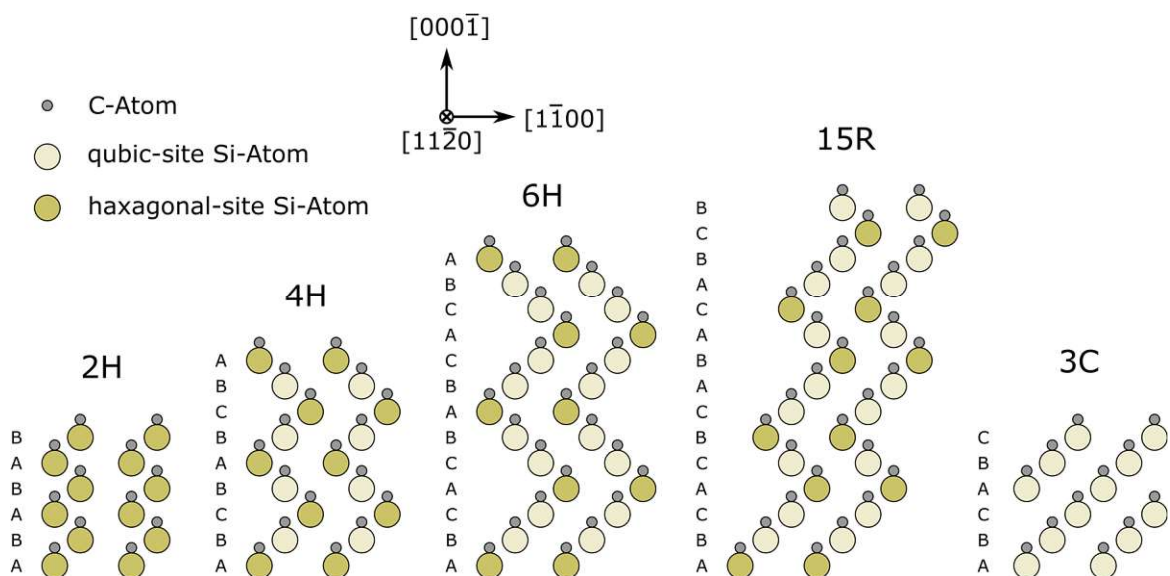
Figure 2.3: Stacking sequence of five different SiC polytypes.
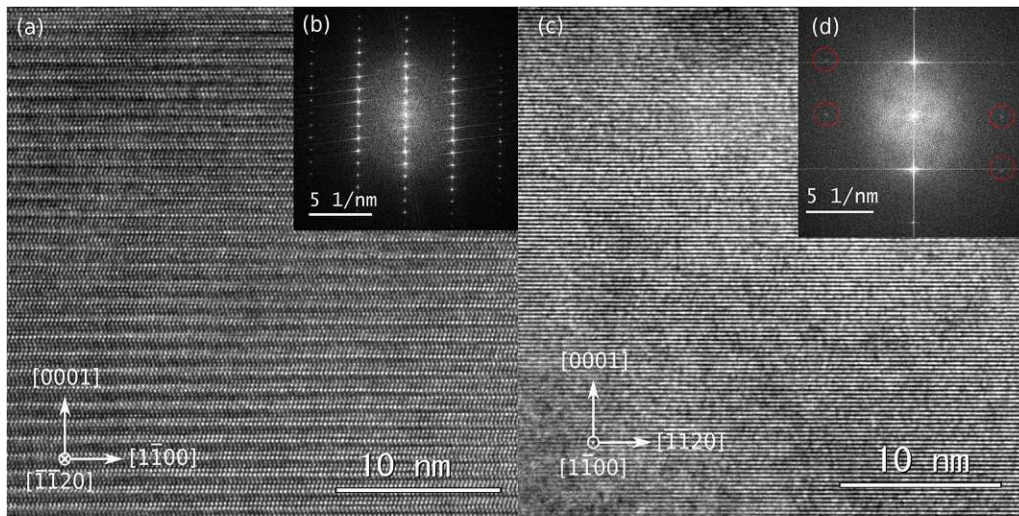
Figure 2.4: High resolution transmission electron microscopy images and fast Fourier transformation patterns of 4H-SiC with the zone axis (axis normal to the image plane) being either (a) the [-1-120] or (c) the [1-100] direction.

features in the [-1-120] direction are detectable. This is due to the interatomic spacing of only 0.154 nm along the <-1-120> direction. Still, weak "quasi diffraction" spots in the fast Fourier transform pattern are observable corresponding to this plane spacing (marked with red circles). The lattice orientation in this image corresponds to a view from the right on the lattices depicted in Figure 2.2 and Figure 2.3. Images taken from this orientation do not provide information about the SiC polytype as the atoms lie on top of each other, independent of the stacking sequence.

Owing to the layered structure of the Si-C bilayers, all hexagonal polytypes show anisotropy of some material parameters normal to and parallel to the c-axis. For example, the breakdown field strength is the highest along the c-axis [27]. Only the cubic 3C polytype is isotropic to directions normal to each other [13]. Because of the composition by Si-C bilayers along the c-axis the top plane (0001) is terminated with silicon atoms and is labeled as Si-face, while the opposite plane (000-1) is called C-face. The two faces have different properties like etching and oxidation rates and also differ in the defect density at the SiO_2/SiC interface [28]. Also, the growth of epitaxial layers is more challenging on the C-face, resulting in a predominant use of the Si-face for the active junction of semiconductor devices [19]. Commonly used SiC wafers for electronic devices are the 4H and 6H polytype and are usually cut a few degrees off the c-axis (typically 4°) to reveal the stacking order for subsequent epitaxial growth processes.

2.1.2 Evolution and state of the art of SiC devices

The long history of SiC-based devices dates back more than 100 years when Edward Goodrich Acheson successfully synthesized the first SiC crystals in 1891 [29]. The newly created material was named Carborundum and was mainly used as abrasive material due to its extreme hardness. Soon after the first synthetization, the rectifying properties of SiC crystals with metal electrodes, forming a preliminary form of a Schottky diode, were discovered by George W. Pierce [30]. From then on SiC crystals were used as radio detectors. After discovering the rectifying properties, another phenomenon of forward biased metal/SiC contacts was observed by Round [31], namely the emission of light on the negative electrode, although it was not commercially used until many years later. In the early 1930s the SiC varistor was developed by the Bell Laboratories for overvoltage protection of installations and electronics. SiC-based varistors are still in use today.

The Acheson process for SiC synthetization was cheap and reliable, but the quality and size of the produced SiC crystals were not acceptable to reproduce the newly discovered transistors, which were manufactured on silicon substrates. In 1954 a new method for producing higher-quality SiC crystals, based on high-temperature sublimation of SiC powder, was patented by Jan Anthony Lely, named after him [32]. This new process was able to produce larger, low defect crystals, suitable for device fabrication in research level. Several improvements and modifications of the Lely process, like using a temperature gradient and a seed crystal to control the polytype, led to today's common process for growing SiC boules [33]. Using this "modifies Lely method" large-diameter boules with controlled polytype are producible.

In the 1980s SiC gained attention by research as material for electronic devices. Before the classical Si devices could be fabricated in SiC technology, the processing of the new material had to be studied in detail. That included etching, epitaxial layer growth, doping, and the experimental determination of the semiconductor parameters of all the available SiC polytypes. The commercialization of SiC semiconductor devices began 1987 when Cree Reaserch Inc. was founded. One year later, the first blue LED, based on 6H-SiC was fabricated and sold. Due to the low efficiency of this indirect band gap semiconductor, blue and UV LEDs were soon produced using nitride semiconductors with SiC as substrate serving as a heat sink due to its high thermal conductivity.

With the increasing demand for high voltage, high temperature, and low loss switching devices, SiC became the material of interest for power electronics. The 4H-SiC polytype was the material of choice due to the higher band gap and higher electron mobility compared to 6H-SiC. In 1992 the first 4H-SiC based Schottky diode with blocking voltages of about 400 V was demonstrated [34]. Over the next years, ever higher breakdown voltages were achieved. Until now Schottky diodes with breakdown voltages exceeding 10 kV have been reported with 4H-SiC substrates [35]. The first commercially available SiC Schottky diode was introduced to the market in 2001 by Infineon. The market release of mass production on 4-inch wafers in 2005 and 6-inch wafers in 2012 led to a strong increase in 4H-SiC production by various competitors.

First switching devices were introduced soon after. After the JFET in 2006, the first SiC MOSFET was available for sale in 2011. A few years after the availability of unipolar SiC devices, also bipolar devices like PIN diodes and bipolar junction transistors were introduced. PIN diodes of tens of kilovolt blocking voltage are possible in 4H-SiC [7], [36]. Still in research and not commercially available are SiC IGBTs and SiC thyristors. As prototypes, 4H-SiC IGBTs with 27 kV blocking voltage and 20 A forward current capability were already demonstrated [37].

Regarding Si/SiC heterojunction devices, no commercial products are available yet. On a research basis, several publications utilizing the Si/SiC heterojunction for devices are available. The first Si/SiC heterojunction was electrically characterized by Henning et al. confirming its rectifying properties [38]. Depending on the heterojunction configuration used (doping type of Si and SiC), a wide spread of resulting SBHs were found. The n-Si/n-4H-SiC heterojunction was found to give SBHs as low as 0.7 V, whereas the highest barrier, with over 2.3 V, was found using the n-Si/p-4H-SiC combination. In the following years, several experimental and theoretical studies of Si/SiC heterojunction diodes have been published [39]–[48], confirming the initial results of Henning et al. who demonstrated the SBH dependence of Si/SiC heterojunctions with different doping types. Another interesting application for the Si/SiC heterostructure is the use as non-UV light detectors [49], [50]. Due to its wide band gap of over 3 eV, which translates to wavelengths of 400 nm and less, most SiC polytypes are only selective to UV-light. To facilitate the properties of SiC, to withstand harsh environments and the good thermal conductivity also in non-UV applications, Si/SiC heterojunctions were fabricated showing a photo-response of the IV characteristic to visible light, but with a low sensitivity.

Also switching devices have been realized by combining Si and SiC. Hoshi et al. [51] demonstrated a unipolar switch featuring a Si/4H-SiC heterojunction, by controlling the barrier height via an insulated gate, forming a heterojunction tunneling transistor with a low on-resistances of $2.9\,\text{m}\Omega\text{cm}^2$. A heterojunction bipolar transistor fabricated by surface-activated-bonding of Si and SiC substrates was characterized by Shigekawa et al. [52]. Although operational, with a maximum current gain of 10, the device technology needs further research. A high density of defects is assumed to be present at the wafer interface forming the Si/SiC heterojunction [43], [46].

Si on top of SiC, was also used to reduce the large number of interface defects when oxidizing 4H-SiC thermally to form metal-oxide-semiconductor (MOS) devices. Depositing a Si layer on SiC, which forms carbon-free SiO_2 is a possible route to reduce the density of interface defects in SiC MOS devices [53].

Also, the Ge/4H-SiC heterojunction was investigated, showing similar well rectifying properties [54], [55].

Although the history of SiC is long, the intense research as material for semiconductor devices began only about 30 to 40 years ago. In this rather short period of time, many achievements in substrate quality and availability, as well as manufacturing technology, have been made. Compared to the research history of silicon components, which is around twice as long, SiC has almost caught up and has trumped Si in almost all areas of power electronics. Much literature deals with the history of SiC and its component launch, where I want to highlight especially references [2], [19], [56] as most informative sources being worth reading.

2.1.3 High-temperature semiconductor devices

The application of semiconductor devices at elevated temperatures is limited due to many reasons [57]. The increasing junction leakage current and the variation of device parameters with temperature are intrinsic limiting factors towards high-temperature application. The increasing leakage current results from the increasing intrinsic carrier density n_i with temperature, as well as from the increasing thermal voltage. The intrinsic carrier concentration strongly depends on the band gap, hence the corresponding semiconductor. An increase of n_i close to or beyond the dopant concentration N_D will dominate any
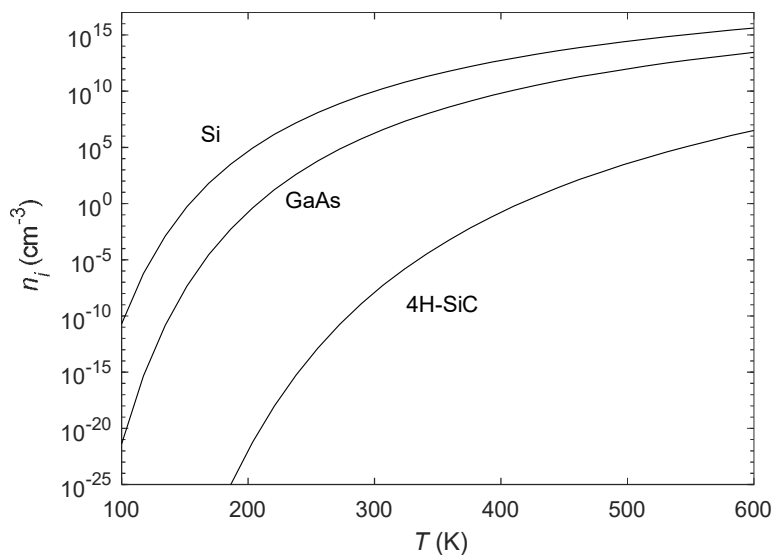
Figure 2.5: Intrinsic carrier concentration n_i over temperature for three important semiconductors.

doping profile as present in e.g. p-n-junctions. Other important device parameters like the carrier mobility and the thermal conductivity will deteriorate with increasing temperature due to enhanced phonon scattering. This can lead to out of specification operation or in the worst case to a total failure of the device. Figure 2.5 shows the intrinsic carrier concentration of Si, GaAs, and 4H-SiC over a wide temperature range. In silicon, n_i can already exceed low donor concentrations in the range of 10^{15} cm^{-3} at temperatures above 250 °C. Temperature-induced carrier generation in reverse-biased junctions is responsible for enhanced leakage current levels. Due to the exponential temperature dependence, the leakage currents will quickly increase to intolerable values. As will be seen in the next section, both limitations are strongly related to the value of the band gap. Therefore, large band gap semiconductors are suitable for high-temperature operation, if other limiting properties like dopant diffusion, thermal conductivity, and chemical reactivity can be controlled as well. Another important aspect worth mentioning is the resistance of a material against chemical reactions at elevated temperatures. The high temperatures required for SiC to initiate e.g. alloy formation or oxidation make it a suitable material for high-temperature electronics, as well as for harsh environment sensors. For comparison, the oxide thickness after dry, thermal oxidation at 1000 °C for 2 h is about 100 nm for Si(111) and 6 nm for 4H-SiC(0001) [58], [59].

2.2 Semiconductor fundamentals

In this section, the basic semiconductor equations needed for analytical and numerical calculations as well as for data evaluation are discussed, assuming the reader to have basic knowledge about semiconductors. The equations in the following do not specifically apply for SiC but hold for every semiconductor material. For 4H-SiC and Si, sources of the used values and approximations are provided. There is a wide variety of symbols in the literature and often the same symbols are used for different physical quantities. When comparing different sources, great care must be taken to ensure the correct symbol is defined for the same quantity and unit. At the end of this thesis, a list of symbols is given including their definition and physical unit.

2.2.1 Basic theory

Energy-band diagrams of p- and n-type semiconductors are depicted in Figure 2.6 along with all important symbols of the energy levels and the potentials. The band gap E_G is the energy difference between the conduction band edge E_C and the valence band edge E_V. The electron affinity χ_s is the potential difference between the conduction band edge and the vacuum energy level E_{vac}. The semiconductor work function $q\phi_s$ is the energy difference between the Fermi energy level E_F, short Fermi level (FL) and the vacuum level, using the elemental charge q. The potential difference between the FL
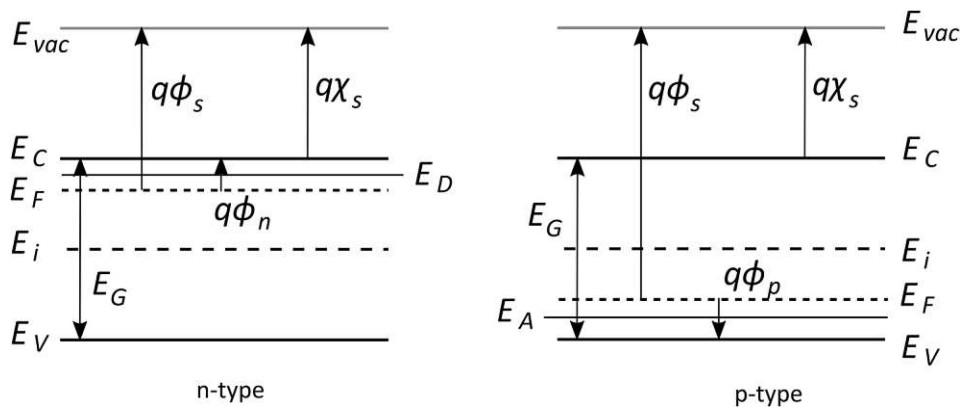
Figure 2.6: Energy-band diagrams of n- and p-type semiconductors with all important symbols. Potentials are defined from arrow shaft to arrowhead ($q\phi = E_{\text{head}} - E_{\text{shaft}}$).

and the conduction band (or valance band for p-type) is called Fermi potential $\phi_n (\phi_p)$. In the depicted band diagrams also an ionization energy E_D for donor like impurities and E_A for acceptor like impurities is illustrated. The intrinsic Fermi level E_i is calculated as

$$E_i = \frac{E_G}{2} + \frac{kT}{2} \ln\left(\frac{N_V}{N_C}\right), \tag{2.1}$$

where k is the Boltzmann constant, T the absolute temperature, and N_V and N_C are the effective densities of states in the conduction and valence band, respectively. For undoped (intrinsic) semiconductors $E_F = E_i$ and at $T = 0$ K it is exactly centered in the band gap. For Si, at nonzero temperatures, it is slightly closer to the valence band edge due to a higher effective density of states in the conduction band. The effective densities of states in the conduction and valence band are calculated according to

$$N_C = 2M_c \left(\frac{2\pi m_{dc}^* kT}{h^2}\right)^{3/2} \quad (2.2) \qquad N_V = 2 \left(\frac{2\pi m_{dv}^* kT}{h^2}\right)^{3/2}, \quad (2.3)$$

where M_c is the number of equivalent minima in the conduction band and m_{dc}^* and m_{dv}^* are the density of states effective masses for electrons and holes, respectively and h is the Planck constant [14]. To evaluate the effective density of states, the relatively recent model by Couderc et al. [60] is used. It provides constants for a polynomial fit of the density of states effective masses, valid in a wide temperature range. For 4H-SiC Wellenhofer and Rössler [61] calculated m_{dc}^* and m_{dv}^* and Hatakeyama et al. [62] derived a polynomial fit which can be used for calculations. Care must be taken, if M_c is included in the density of states effective masses or not. For Si, $M_c = 6$, but it is already included in m_{dc}^* by [60]. For 4H-SiC, $M_c = 3$ and it is not included in the m_{dc}^* expression of [62].

The intrinsic carrier concentration and the mass-action law are given by

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_G}{2kT}\right) \quad (2.4) \qquad\qquad np = n_i^2 \quad (2.5)$$

The mass-action law is only valid for non-degenerate semiconductors in thermal equilibrium [14], [63]. To calculate the equilibrium carrier concentrations for electrons n and holes p the product of the total number of states and the occupation probability must be calculated for every energy in the conduction and valence band, respectively, and summed up. Depending on the doping concentrations a semiconductor is considered degenerate or non-degenerate. If the dopant concentration is near or beyond the effective density of states, the Fermi level approaches the band edges or even lies outside of the band gap. By definition, a semiconductor is considered as degenerate if E_F is at least $3kT$ away from the band edges [14], [63]. In the following discussion, the more general Fermi-Dirac statistic is used for the occupation probability function to account for degenerate semiconductors, because very high doping concentrations are used in the experiments. These calculations are valid for non-degenerate semiconductors as well, although Boltzmann statistics can be used as a good approximation. Using Fermi-Dirac statistics, including the Fermi-Dirac integral $F_{1/2}$, the carrier concentrations are calculated by [14]

$$n = N_C \frac{2}{\sqrt{\pi}} F_{1/2} \left(\frac{E_F - E_C}{kT}\right) \quad (2.6)$$

$$F_{1/2}\left(\frac{E_F - E_C}{kT}\right) = \int_{E_C}^{\infty} \frac{[(E - E_C)/kT]^{1/2}}{1 + \exp\left[(E - E_F)/kT\right]} \frac{dE}{kT} \quad (2.7)$$

$$p = N_V \frac{2}{\sqrt{\pi}} F_{1/2} \left(\frac{E_V - E_F}{kT} \right) \qquad (2.8)$$

$$F_{1/2} \left(\frac{E_V - E_F}{kT} \right)$$
$$= \int_{-\infty}^{E_V} \frac{[(E_V - E)/kT]^{1/2}}{1 + \exp \left[(E_F - E)/kT \right]} \frac{dE}{kT} \qquad (2.9)$$

Doping was already mentioned above and is responsible for shifting the Fermi level away from its intrinsic level. Dopants are introduced in a certain concentration into the semiconductor material given as donor concentration N_D and acceptor concentration N_A. Depending on the temperature and the ionization energy of N_D or N_A, not all dopant atoms might deliver a charge to the conduction or valence band, hence contribute to current flow. The ionized dopant concentration is given by

$$N_D^+ = \frac{N_D}{1 + g_D \exp \left(\frac{E_F - E_D}{kT} \right)} \qquad (2.10) \qquad N_A^- = \frac{N_A}{1 + g_A \exp \left(\frac{E_A - E_F}{kT} \right)}, \qquad (2.11)$$

where g_D and g_A are the ground-state degeneracy factors for donor and acceptor impurities, respectively. They are equal to $g_D = 2$ and $g_A = 4$. E_D and E_A are the ionization energies of the dopants, using the same reference point as the Fermi level. Actual ionization energies are often given in respect to the conduction band edge for n-type impurities ($\Delta E_D = E_C - E_D$) and to the valence band edge for p-type impurities ($\Delta E_A = E_A - E_V$). Especially at lower temperatures the relatively deep dopant ionization energy levels of 4H-SiC require the consideration of the ionized dopant concentrations. In 4H-SiC impurities have two ionization energies, depending on whether they are located on a cubic, or hexagonal lattice site. In 4H-SiC the cubic to hexagonal ratio is 1 to 1 and therefore the distribution of e.g. nitrogen donors is also 1 to 1 [17]. In the calculations, both donor levels can be considered or an effective ionization energy $\Delta E_{D,eff}$ is applied. In case of nitrogen doping, $\Delta E_{D,eff} \sim 70$ meV, which is about the average of the two individual energy values [64].

For highly doped semiconductors the formation of a dopant band occurs, and the assumption of a single impurity level is no longer valid. Also, dopant-induced band gap narrowing (BGN), as will be discussed soon, will dominate at high doping concentrations. Both, the formation of dopant bands and the BGN will reduce the ionization energy of the dopants. At very high doping concentrations the dopant bands will eventually touch the conduction or valance band edge, resulting in very high conductivity and a degenerate state due to the high doping concentration. This is the so-called Mott (metal-insulator) transition. For silicon, the incomplete ionization model proposed by Altermatt et al. [65], [66] is used, which considers this effect. The equations and the corresponding parameters for silicon are not repeated here but can be found in the references. For doping concentrations in excess of approximately 10^{18} cm^{-3} the Equations (2.10) and (2.11) should be replaced by the corresponding equations of the cited model. Due to the low doping of the 4H-SiC epi-layer the classic approach is sufficient.

Using $n = N_D^+ + p$ and $p = N_A^- + n$, thus combining Equations (2.6),(2.8) and (2.10) for n-type and (2.8),(2.6) and (2.11) for p-type materials, the Fermi level can be calculated by numerically solving the following equations

$$N_C \frac{2}{\sqrt{\pi}} F_{1/2} \left(\frac{E_F - E_C}{kT} \right) = \frac{N_D}{1 + g_D \exp \left(\frac{E_F - E_D}{kT} \right)} + N_V \frac{2}{\sqrt{\pi}} F_{1/2} \left(\frac{E_V - E_F}{kT} \right), \qquad (2.12)$$

$$N_V \frac{2}{\sqrt{\pi}} F_{1/2} \left(\frac{E_V - E_F}{kT} \right) = \frac{N_A}{1 + g_A \exp \left(\frac{E_A - E_F}{kT} \right)} + N_C \frac{2}{\sqrt{\pi}} F_{1/2} \left(\frac{E_F - E_C}{kT} \right). \qquad (2.13)$$

Another consequence of high doping concentrations is BGN. The band gap of a semiconductor decreases with increasing doping concentrations. This effect has many theoretical reasons. At high doping concentrations, the discrete defect energy levels start to form defect energy bands, which can even spread beyond the band edges. Also, carrier-carrier and carrier-impurity interactions result in a decrease of the band gap [67], [68]. For doping concentrations above 10^{18} cm^{-3} BGN should be taken into account to reduce errors in calculations and experimental data evaluation. Several models for describing the band gap narrowing have been proposed, most of them focused on n-type Si. As the epitaxial drift layers of the SiC are rather low doped, BGN effects do not have to be considered in the SiC. But the highly doped Si layers are strongly affected by this effect. Lindefelt [69] proposed a model for band gap narrowing of SiC polytypes along with values for Si. In his model, he splits up the band gap narrowing in conduction and valance band displacements. Both band edges are shifted, hence tend to come closer to mid-band due to doping effects. The band displacements are calculated for n-type materials as:

$$\Delta E_C = A_{nc} \cdot \left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{4}} + B_{nc} \cdot \left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{2}} \tag{2.14}$$

$$\Delta E_V = A_{nv} \cdot \left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{4}} + B_{nv} \cdot \left(\frac{N_D^+}{10^{18}}\right)^{\frac{1}{2}} \tag{2.15}$$

and for p-type as:

$$\Delta E_C = A_{pc} \cdot \left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{4}} + B_{pc} \cdot \left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{2}} \tag{2.16}$$

$$\Delta E_V = A_{pv} \cdot \left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{3}} + B_{pv} \cdot \left(\frac{N_A^-}{10^{18}}\right)^{\frac{1}{2}}. \tag{2.17}$$

Coefficients of these equations can be found in [69], [70] for Si and 3C, 2H, 4H and 6H-SiC. The total band gap narrowing is $\Delta E_G = -\Delta E_C + \Delta E_V$. For example, using Si, a doping concentration of $N_A = 10^{19}$ cm^{-3} reduces the band gap at room temperature by 56 meV which equals to 5%. Not considering BGN can cause errors e.g. when calculating the theoretical barrier height of a heterojunction.

Another important characteristic of the band gap is its temperature dependency. The increase in the interatomic spacing with increasing temperature leads to a decrease in band gap. One of the most frequently used relationships was proposed by Varshni [71]

$$E_G(T) = E_G(0) - \frac{\alpha T^2}{T + \beta}. \tag{2.18}$$

Model parameters are the band gap value at zero temperature $E_G(0)$ and two constants α and β. Although this simple model shows weaknesses at very low temperatures, it is widely used due to its simplicity and availability of parameters for most semiconductors. Values for 4H-SiC are $E_G(0) = 3.285$, $\alpha = 3.5 \cdot 10^{-4}$ eV/K and $\beta = 1.1 \cdot 10^3$ K [72].
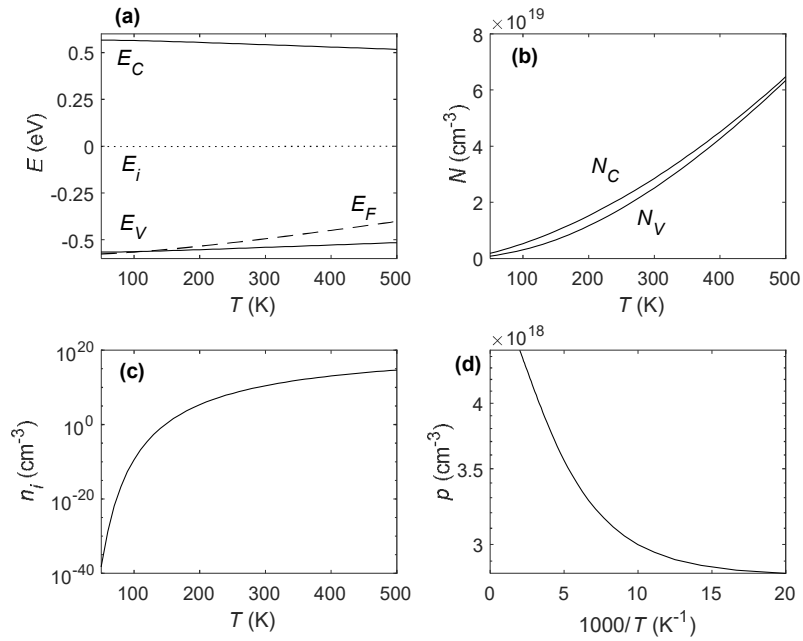
Figure 2.7: Calculated semiconductor properties for p-Si over temperature. (a) energy band diagram, (b) effective densities of states, (c) intrinsic carrier concentration and (d) hole concentration with $N_A = 5 \cdot 10^{18}$ cm^{-3}.
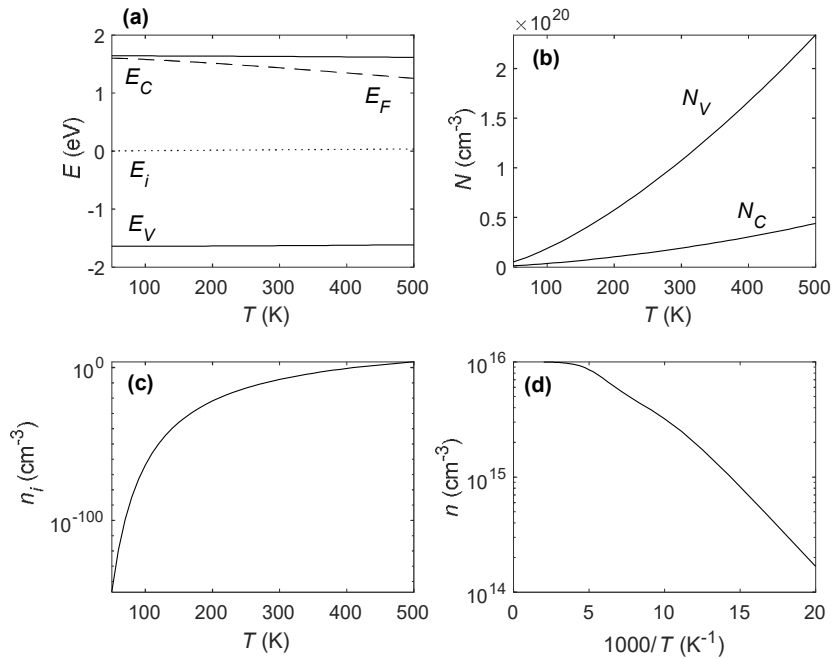
Figure 2.8: Calculated semiconductor properties for n-type 4H-SiC over temperature. (a) energy band diagram, (b) effective densities of states, (c) intrinsic carrier concentration and (d) hole concentration with $N_D = 10^{16}$ cm^{-3}.

A slightly more precise model is the Pässler model [73] which calculates $E_G(T)$ according to

$$E_G(T) = E_G(0) - \left(\frac{\varepsilon_p \Theta_\mathrm{p}}{2}\right)\left[\sqrt[p]{1 + \left(\frac{2T}{\Theta_\mathrm{p}}\right)^p} - 1\right]. \tag{2.19}$$

This model is used in the calculations of this thesis using the parameters for 4H-SiC of $E_G(0) = 3.267$ eV, $\varepsilon_p = 3 \cdot 10^{-4}$ eV/K, $\Theta p = 450$ K, and p = 2.9 [74].

For silicon the even more exact model by Donnell and Chen [75] is used,

$$E_G(T) = E_G(0) - S'\langle\hbar\omega\rangle\left[\coth\left(\frac{\langle\hbar\omega\rangle}{2kT}\right) - 1\right]. \tag{2.20}$$

This model also requires the zero-temperature band gap along with two constants, *S'* and the average phonon energy $\langle\hbar\omega\rangle$. For Si $E_G(0) = 1.166$, *S'* = 1.49, and $\langle\hbar\omega\rangle = 25.5$ meV can be used [75].

Using the equations and models introduced above, the band diagrams and carrier concentrations of highly doped Si and moderately doped 4H-SiC are calculated and plotted in Figure 2.7 and Figure 2.8, respectively.

Over the wide temperature range of 50 to 500 K used in the calculations, a significant change in the Fermi level and also in the band gap is visible. Not considering the temperature and dopant dependencies can result in large errors, especially as this temperature range is typical for device characterization.

2.2.2 Incomplete ionization

As was already mentioned above, depending on the temperature, the doping concentration, and ionization energies, not all introduced impurities are contributing to the free carrier concentration in the semiconductor bands because they are not ionized. This effect is called incomplete ionization. In this section, the consequences of incomplete ionization will be discussed, and examples are given to emphasize when it is necessary to account for this phenomenon. Additionally, to the well-known static effect of incomplete ionization, namely a lower-than-expected carrier concentration, hence a higher-than-expected semiconductor resistivity, the dynamic effects of incomplete ionization will be discussed briefly.
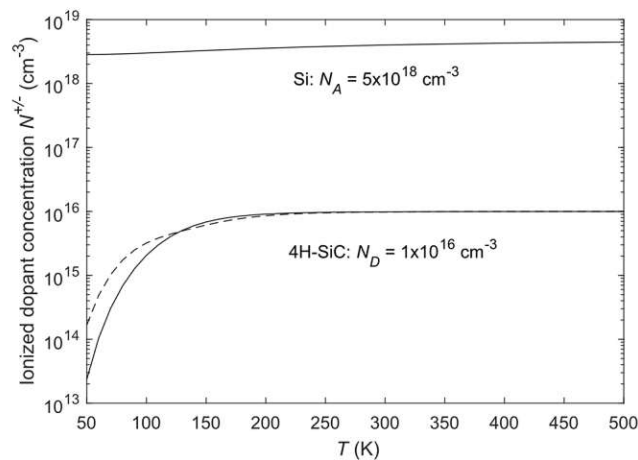
Figure 2.9: Ionized donor and acceptor concentrations over temperature for 4H-SiC and Si, respectively. For 4H-SiC the solid line represents the use of an effective ionization energy $E_{D,eff} = 70$ meV and the dashed line uses a 1 to 1 distribution of nitrogen donors on cubic and hexagonal sites.

As a first illustration of the impact of incomplete ionization the example of highly p-doped Si and moderately n-doped 4H-SiC as used in the previous section is continued. Using Equations (2.10) and (2.11) the amount of ionized dopants is calculated at a given temperature based on the density of introduced dopants N_D or N_A and the energy level of the impurity type with respect to the conduction or valence band edge, respectively. The ionization energies of the most common dopants are given in Table 2.2. The calculated ionized dopant concentration over temperature for Si and 4H-SiC is depicted in Figure 2.9. In this example, it is visible that Si is hardly affected by incomplete ionization due to the very shallow dopant energy level of boron of only 44 meV above the valance band edge. Even at 50 K, about half of the dopants are ionized. The relatively low doped 4H-SiC shows a much stronger dependence of N_D^+ on temperature. In this example an effective ionization energy of $\Delta E_{D,eff}$ = 70 meV [64] is used, as well as the more exact approach using 50% hexagonal and 50% cubic doping sites with $\Delta E_{D,h}$ = 50 meV and $\Delta E_{D,c}$ = 92 meV [15], [17]. Down to a temperature of about 120 K, the use of only one effective ionization energy instead of two is justifiable. At 50 K only slightly more than 1/1000 of the impurities are ionized. But at a more realistic lower operation temperature limit, say 250 K, about 96% of the dopants are ionized and the effects on device performance are negligible.

As a further example, the ionized dopant concentration in 4H-SiC for different base dopant concentrations between $1 \cdot 10^{16}$ and $1 \cdot 10^{19}$ cm^{-3}, for both nitrogen (N) and aluminum (Al) impurities are depicted in Figure 2.10. At higher concentrations the n-type dopant nitrogen starts to be affected by reduced ionization at room temperature. At T = 300 K and $N_D = 1 \cdot 10^{19}$ cm^{-3}, which is a common doping concentration for bulk wafers, the ionized concentration is only $2.3 \cdot 10^{18}$ cm^{-3}. This can already lead to a significant reduction of the bulk resistivity and needs to be considered. Using p-type 4H-SiC with the common dopant aluminum and its relatively deep ionization level of about 200 meV [16], the ionization concentration at room temperature is far below the dopant concentration. Again, assuming T = 300 K and $N_A = 1 \cdot 10^{19}$ cm^{-3} only $3.4 \cdot 10^{17}$ cm^{-3} are electrically active. At cryogenic temperatures, the concentration of ionized aluminum atoms can be neglected compared to typical background impurity concentrations [76]. In the above example, an important phenomenon was neglected, namely the Metal-Insulator or Mott transition. At very high dopant concentrations, the dopant atoms are no longer independent, but can form clusters which have a different interaction with the semiconductor crystal. This results in a broadening of the impurity density of state to an impurity band and the reduction of the dopant ionization level [65]. For Al-doped 4H-SiC with doping concentrations $N_A > 10^{19}$ cm^{-3} the
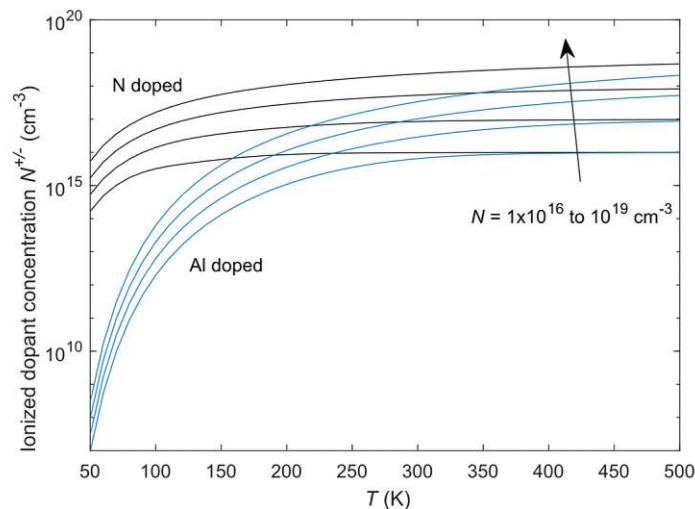
Figure 2.10: Ionized donor and acceptor concentrations of 4H-SiC doped with N and Al with base concentrations of 10^{16}, 10^{17}, 10^{18} and 10^{19} cm^{-3} over temperature.

ionization energy will strongly decrease, resulting in a higher degree of ionization. At doping concentrations close to the Al solubility limit of $2 \cdot 10^{20}$ cm^{-3} in 4H-SiC, very high conductivity values are achivable even at very low temperatures [77].

What has been discussed until now was "static incomplete ionization". The word static implies, that all time-dependent processes are completed, and the system reached thermal equilibrium. It was shown that the effect of incomplete ionization is negligible for Si and almost negligible at non-cryogenic temperatures for low doped n-type 4H-SiC, which is often used in epitaxial drift layers. Using high n-type concentrations or p-type 4H-SiC the effect of incomplete ionization on the semiconductor resistivity is huge, significantly reducing the free carrier concentration compared to the amount of dopants introduced into the crystal. This can have a substantial impact on device properties due to an increased bulk resistivity and should be considered in calculations.

Continuing in the static regime, but introducing an electric field, a potential distribution, hence band bending ψ_{bb} will arise in the semiconductor. This will for example be the case in the depletion region of a Schottky contact. In contrast to the potential free neural region, the ionization terms from Equations (2.10) and (2.11) will become [78]

$$N_D^+ = \frac{N_D}{1 + g_D \exp\left(\frac{E_F - E_D}{kT}\right) \times \exp\left(\frac{q\psi_{bb}}{kT}\right)} \tag{2.21}$$

$$N_A^- = \frac{N_A}{1 + g_A \exp\left(\frac{E_A - E_F}{kT}\right) \times \exp\left(-\frac{q\psi_{bb}}{kT}\right)}. \tag{2.22}$$

If one assumes infinitely fast ionization, the same equations can also be used for nonequilibrium cases by substituting the Fermi levels by their quasi-Fermi levels [79]. By definition, with respect to the n-type bulk, ψ_{bb} is negative if the bands are bent upwards and positive with respect to the p-type bulk if bend downwards. Considering the case of a Schottky contact on n-type semiconductors, ψ_{bb} is therefore negative in the depletion region. As a consequence, the new term introducing the band banding results in almost complete ionization in the depletion region of a semiconductor so that in the equation for the width of the depletion region of e.g. a Schottky junction the total dopant concentration N_D needs to be implemented and not the ionized fraction N_D^+, how it is often done wrongly. Doping profiling by capacitance-voltage technique always gives the total dopant concentration. Assuming they are ionizable, hence incorporated in the lattice.

Until now, either a static situation or an infinitely fast ionization was assumed. In reality, the process of emitting or capturing an electron or a hole by an impurity takes a certain time. Introducing the dynamic model of ionization, a time dependence of the ionization is given by [80]

$$\frac{\partial N_D^+}{\partial t} = -(e_n + c_n n)N_D^+ + e_n N_D \tag{2.23}$$

$$\frac{\partial N_A^-}{\partial t} = -(e_p + c_p p)N_A^- + e_p N_A, \tag{2.24}$$

with capture and emission coefficients $c_{n,p}$ and $e_{n,p}$. From now on only the equations for n-type impurities will be given for the sake of simplicity, changing to p-type is straightforward. The capture and emission coefficients follow from

$$c_n = \sigma_n v_{th,e} \qquad (2.25) \qquad\qquad e_n = \frac{\sigma_n v_{th,e} N_C}{g_d} \exp\left(-\frac{E_C - E_D}{kT}\right), \qquad (2.26)$$

with σ_n being the capture cross-section and $v_{th,e}$ the electron thermal velocity

$$v_{th,e} = \sqrt{\frac{kT}{m_{th,e}^*}}, \qquad (2.27)$$

whereas $m_{th,e}^*$ denotes the thermal velocity effective mass for electrons. This value differs from the density of states effective masses [81], but due to the lack of proper values for 4H-SiC the latter values are implemented in the calculations [61]. From the time dependency (2.23) an ionization time constant can be defined as

$$\tau_n = \frac{1}{e_n + c_n n}, \qquad (2.28)$$

which simplifies to $\tau_n = 1/e_n$ in the absence of carriers, e.g. in the depletion region. This ionization time constant is equivalent to the time constant determined with deep-level transient spectroscopy (DLTS) or admittance spectroscopy (AS) [82].

The ionization time constant was calculated for nitrogen doped n-type 4H-SiC and Al doped p-type 4H-SiC as a function of temperature. Several models for the capture cross-sections are discussed in the literature. For simplicity, a temperature-independent constant value of 10^{-15} cm^2 is used for the capture cross-section of nitrogen and 10^{-14} cm^2 for aluminum dopants [83], [84]. Depicted in Figure 2.11 is the strong temperature dependence of the ionization time constants. The nitrogen donor was split up into cubic and hexagonal sites because in terms of ionization time, their difference in ionization energy has a strong impact. With about $5 \cdot 10^{-11}$ s, the N_h dopants are the fastest at room temperature, and even as low as 50 K they exhibit a time constant of about 10 µs. The nitrogen on cubic sites is slower, with $2.6 \cdot 10^{-10}$ s at room temperature and 0.2 s at 50 K, respectively. The slowest ionization time is calculated for the Al dopants with $3.8 \cdot 10^{-10}$ s at room temperature and about $5 \cdot 10^8$ s (16 years) at 50 K. As mentioned above, the calculated time constants are estimations based on the assumption of constant capture cross-sections, but provide a good reference point to assess if dynamic incomplete ionization needs to be considered.

If the voltage applied to a semiconductor device is changed within time scales around the ionization time constant or below, the device properties will be altered. Neudeck [85] was the first to observe a reduction of the breakdown voltage of 4H- and 6H-SiC pn-junction diodes when applying ultrashort (1 ns) reverse pulses. Also, when performing device characterization at low temperatures, the effect of incomplete ionization might cause misinterpretation of the measured quantities. As an example, if one measures the capacitance-voltage characteristics of a 4H-SiC Schottky diode on Al-doped substrates, a standard measurement frequency of 1 MHz will already result in a decreased capacitance at 160 K and below. Of course, the effect of incomplete ionization and the response of the traps to a measurement frequency similar to their time constants is a well-known method, explicitly used in DLTS and AS, but on the other hand its influence is often forgotten.
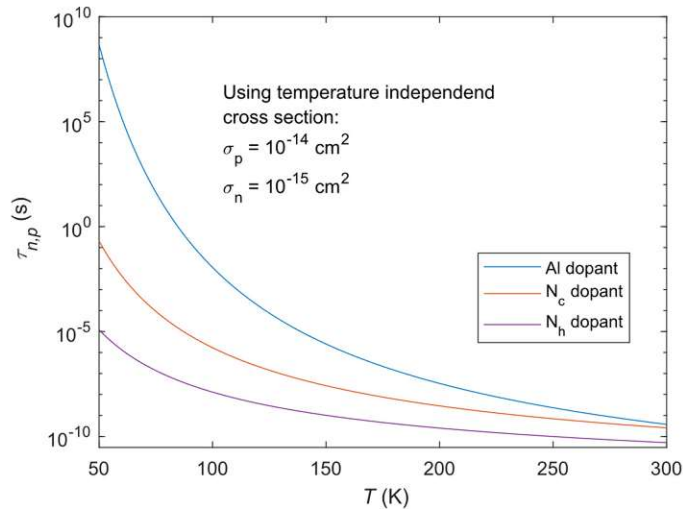
Figure 2.11: Calculated ionization time constants for Al and N doped 4H-SiC over temperature.

This section discussed the important topic of incomplete ionization, of both static and dynamic cases. Considering incomplete ionization becomes more important as new wide band gap and ultrawide band gap semiconductors with only deep dopant levels (e.g. diamond) are more frequently researched. It was shown that also 4H-SiC can be affected, both by a reduction of the bulk resistivity due to static effects and by a reduced field strength due to dynamic ionization effects.

2.3 Contacts to semiconductors

In this section, the theoretical basis for contacts to semiconductors is provided. The two contacts essential for this thesis are the metal-semiconductor (MS) and the semiconductor-semiconductor contact, the latter is called heterojunction. Depending on their type of conductivity they are further divided into ohmic contacts and Schottky contacts. Other types of semiconductor contacts, like pn-contacts or contacts to insulators are not in the scope of this work.

2.3.1 Schottky contacts

One of the most important contacts in the semiconductor industry is the rectifying metal-semiconductor contact named after Walter Schottky, who first described the barrier formation of this contact type [86]. In Figure 2.12 a schematic illustration of a Schottky contact (SCs) along with its band diagram is depicted. In Figure 2.12a a simple device with a Schottky contact on top and an ideal ohmic contact on the bottom and the arising depletion region is shown. The capacitance of the depletion region of width W_d is called depletion capacitance C_d. The corresponding band diagram in Figure 2.12b shows the band banding at zero bias along with all important quantities. Separated, the bands of both the metal and the semiconductor are flat. After bringing them in contact, charge carriers will flow from the side with the higher Fermi level to the one with the lower, i.e., in this case, electrons from the semiconductor to the metal, as energetically lower states are available in the metal. This continuous until a repelling force of the remaining ionized dopants balances the charge transfer. Due to this process, the Fermi-levels become lined up and the semiconductor bands are bent on the interface giving rise to a depletion region and a potential barrier with a Schottky barrier height ϕ_B. The built-in voltage ψ_{bi} is equivalent to the amount of band bending ($\psi_{bi} = \psi_{bb}$). The Schottky-Mott rule allows a theoretical calculation of the barrier height using the metal work function ϕ_m and the semiconductor affinity χ_s

n-type semiconductor:
$$\phi_B = \phi_m - \chi_s \tag{2.29}$$

p-type semiconductor:
$$\phi_B = \frac{E_G}{2} + \chi_s - \phi_m. \tag{2.30}$$

This barrier acts as blockage for electrons from the metal into the semiconductor, whereas electrons can pass over the barrier from the semiconductor in the metal, as the applied voltage shifts the semiconductor bands upwards. As one can see in the band diagram, the banding of the semiconductor bands can also be downwards if $\phi_m < \phi_s$. Then there is no barrier anymore and the metal-semiconductor is called an ohmic contact. For p-type semiconductors, holes are the involved charge carriers and the condition for ohmic contacts is reversed.
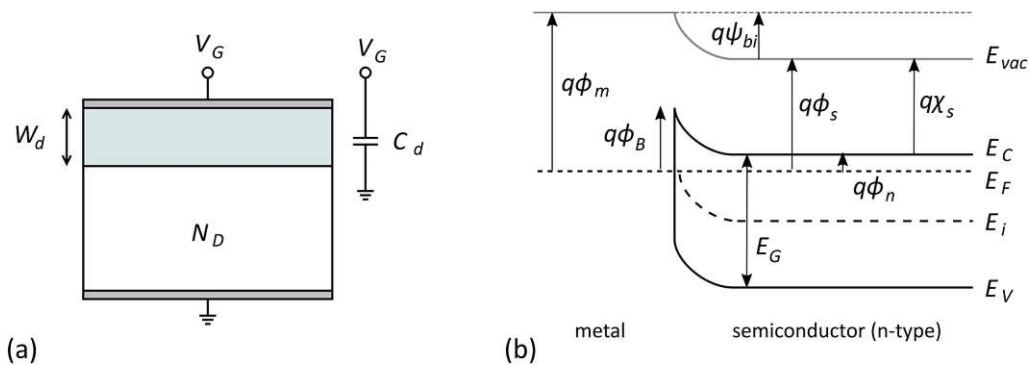
Figure 2.12: (a) Schematic of a semiconductor with a Schottky contact on the top and an ideal ohmic contact on the bottom. The depletion region is shown along with a capacitor as its equivalent circuit. (b) Band diagram of a metal-semiconductor under zero external bias, forming a Schottky barrier.

In reality, the barrier height formation is dependent on more than on the difference between the metal work function and the electron affinity. Surface reconstruction and bond formation between metal and semiconductor disturb the potential energy distribution of the bulk and the simple Schottky-Mott rule does not apply anymore. This effect is called "Fermi-level pinning" and is further discussed in its own section.

2.3.2 Heterojunctions

A heterojunction is a junction of two different semiconducting materials, in contrast to a homojunction, where the two materials are of the same type of semiconductor. Depending on the type of doping of the two semiconductors, the junction is called isotype, if they are of the same type (i.e. n-n or p-p), or anisotype, if they are of opposite doping type (i.e. n-p or p-n). Figure 2.13 depicts the energy band diagrams of two semiconductors with different band gap and opposite doping type in both the separated and the connected state. Most of the quantities are already defined in the previous section. New are the band offsets ΔE_C and ΔE_V, which are the offsets of the conduction band edges and the valence band edges of the two semiconductors, respectively. Furthermore, there are now two built-in voltages ψ_{bi1} and ψ_{bi2} which account for the band bending in each semiconductor. Combined they give the total built-in voltage ψ_{bi}. Anderson [87] first described the band alignment and the electrical current flow in a heterojunction diode. He came up with a simple rule, like the Schottky-Mott rule, for the band offsets. The Anderson rule, or sometimes called electron affinity rule, gives the following equations for the band alignments,

$$\Delta E_C = q(\chi_{s2} - \chi_{s1}) \qquad (2.31) \qquad \Delta E_V = (q\chi_{s1} + E_{G1}) - (q\chi_{s2} + E_{G2}). \qquad (2.32)$$
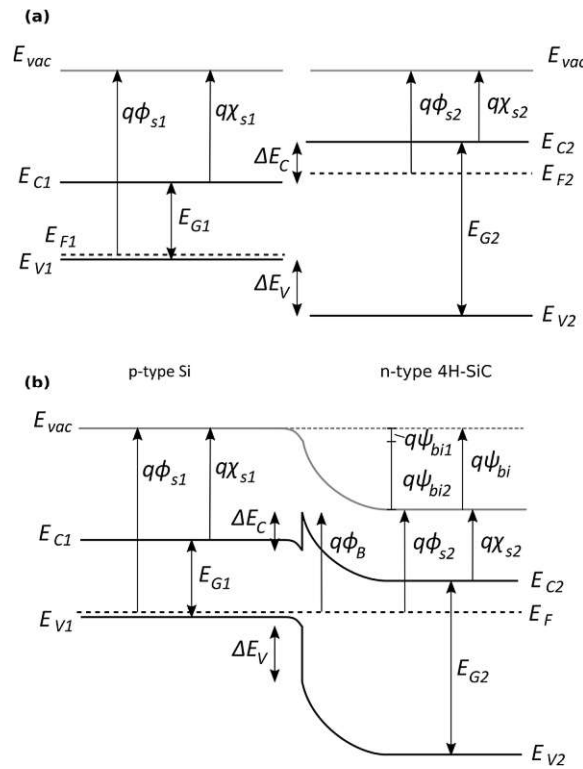
Figure 2.13: Energy band diagram of (a) two separated semiconductors with different band gap and of opposite doping type and (b) brought into contact, forming an anisotype heterojunction.

Like the Schottky-Mott rule, the Anderson rule tries to estimate the band alignment at the surface with bulk related quantities. These equations are affected by the same shortcomings as the Schottky-Mott, because the surface chemistry is neglected and the interface formation is estimated using bulk properties. Deposition techniques, surface cleaning, and the crystal orientation change the real band offset. Further information about the band alignment considering interatomic interactions can be found in [88], [89].

In contrast to a Schottky-contact, in a heterojunction both semiconductor bands can align when brought into contact, resulting in two built-in voltages and two depletion regions. Only if the difference in doping is high $N_1 \gg N_2$, the potential drop and the depletion can be considered to be confined only in the low doped semiconductor. Expressions for the depletion width and capacitance for the general case of two regions can be found in [14], [87]. Figure 2.13 shows the band structure of two semiconductors before and after bringing them in contact. The arising band structure can be quite different depending on the doping type and dopant concentration as well as on the band gap of the two semiconductors. In case of an anisotype heterojunction with rather similar doping concentrations, the current flow over the junction can be described in good approximation by diffusion [14]. In case of an isotype junction, the device can be considered as a unipolar device, as only one type of carrier is contributing to the current flow. The current flow is dominated by thermionic emission over the formed barrier at the junction. The current-voltage characteristic of isotype heterojunctions is similar to the thermionic emission equation known from Schottky-contacts, but differs in terms of temperature dependency and reverse characteristics. For a detailed derivation, reference is again made to [14], [87].

An important case for both, isotype and anisotype heterojunctions is if one of the semiconductors is much higher doped than the second one. Then the junction can be approximated as a Schottky junction, where the highly doped semiconductor acts like a metal [38], [90]. In this case, the same equations as for Schottky contacts can be used to determine e.g. the current flow or the device capacitance.

2.3.3 Current over Schottky barriers

The current-voltage relationship of a homogenous SB junction can be derived via the thermionic emission theory as [91],

$$I(V) = I_s \left[\exp\left(\frac{\beta V}{\eta}\right) - 1 \right], \tag{2.33}$$

with η (often found as n, but not to be confused with the electron concentration) is the ideality factor and $\beta = q/(kT)$. The saturation current is given by

$$I_s = A^* A T^2 \exp(-\beta \phi_B), \tag{2.34}$$

with A^* being the Richardson constant (for 4H-SiC: $A^* = 146$ A/K^{2}cm^2 [92]). The barrier height ϕ_B has been defined elsewhere. Equation (2.33) works very well to describe the current flow in a homogenous Schottky barrier with a uniform barrier height ϕ_B. The ideality factor also accounts for any deviations from solely thermionic current flow and is different than unity if field emission or thermionic field emission contributes to the device current. The higher the doping concentration of the semiconductor at the interface the thinner is the depletion width, hence the barrier. Therefore, the ratio between field emission to thermionic emission current will increase [14]. For example, at ohmic contacts the barrier is willingly kept thin to allow tunneling [14]. This is done by a higher doping concentration near the surface. Also, inhomogeneities in the barrier height across the junction can cause η to be greater than 1 and to be voltage-dependent [93], [94]. A more in-depth discussion about inhomogeneities is given in 2.3.5.
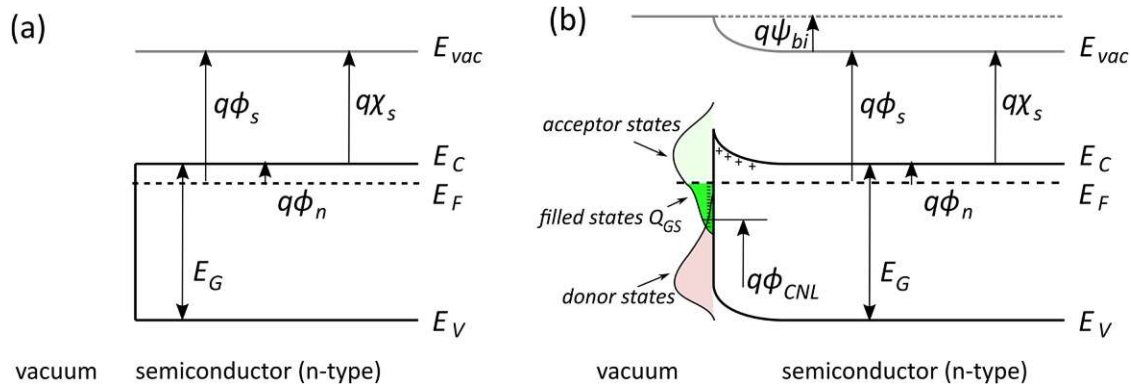
Figure 2.14: Explanation of Fermi level pinning on the semiconductor surface. (a) Energy band diagram of a semiconductor without surface pinning and (b) semiconductor with strong pinning due to surface charges.

2.3.4 Fermi-level pinning

As discussed above, the Schottky-Mott rule Eqs. (2.29) and (2.30) as well as the Anderson rule for heterojunction band offsets Eqs. (2.31) and (2.32) are only rough estimations, because they use bulk properties to calculate effects on the interface between two surfaces. Decades ago, severe weaknesses of these simple equations to calculate the barrier height between semiconductors and metals were observed [95]. The influence of ϕ_m on the SBH was much less pronounced than expected. The conclusion is, that there must be some charge arrangement at the interface that "screens" the bulk work functions of the two materials to a certain degree. A parameter called "S-parameter" was introduced as a measure of the deviation from the Schottky-Mott rule [95]. S follows from the slope of the SBH over the metal work function

$$ S = \frac{\partial \phi_B}{\partial \phi_m}. \tag{2.35} $$

$S = 0$ corresponds to no dependence of the SBH on ϕ_m and $S = 1$ means the Schottky-Mott rule applies. A dependence of S on the type of semiconductor was found a long time ago, for example rather high S values for compound semiconductors with high ionicity [96]. Germanium has a very low S-parameter [97]. The weak validity of the Schottky-Mott rule is often attributed to an effect known from semiconductor surfaces, namely Fermi-level pinning (FLP) [95].

To understand the concept, the FLP on a semiconductor surface, exposed to vacuum is discussed first. The reconstruction of surface atoms will create active states in the band gap, they are labeled as surface states, or gap states D_{GS}. These surface states can be of acceptor and donor type and have a certain energetic distribution inside and beyond the band gap. The point in energy, where the net surface charge equals zero is designated as the charge neutrality level (CNL). All acceptor states above the CNL are empty, hence neutral and all donor states below the CNL are filled, hence neutral [98]. Figure 2.14 illustrates the influence of surface states on the band alignment of a semiconductor surface. In Figure 2.14a, the n-type semiconductor does not have a significant amount of surface states, or the CNL coincides exactly with the bulk FL, therefore no band banding occurs. In Figure 2.14b a strong distribution of acceptor and donor like states is present with the CNL approximately in the middle of the forbidden band. For intrinsic semiconductors, the overall FL would equal the CNL. If the bulk is doped n-type with the bulk FL above the CNL, like in this example, a charge transfer of the electrons from the bulk to the surface states will occur until equilibrium is reached. The surface becomes negatively charged with the surface charge Q_{GS}, while the same amount of positive charge is present in the semiconductor and represents the space charge region. For most semiconductors, the CNL lies roughly in the middle of the band gap [99].
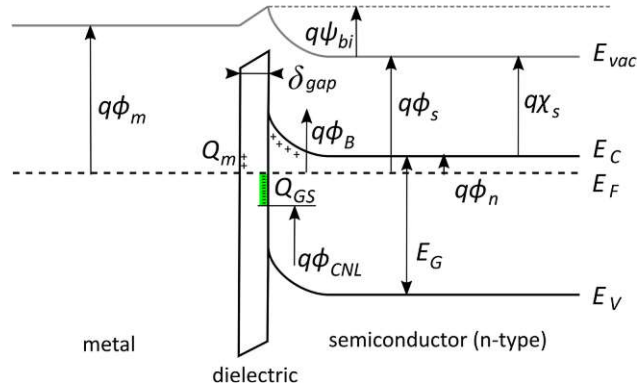
Figure 2.15: Fixed separation model of a metal-semiconductor contact with a thin dielectric separation layer. A uniform surface charge distribution is present on the semiconductor surface and stays unchanged after contact formation.

The same concept is frequently applied to MS contacts and is taken responsible for the observed FLP [95]. Known as the "fixed-separation model" a small gap of dielectric material with width δ_{gap} is assumed to be separating the semiconductor and the metal by a few Angstroms to be able to preserve the semiconductor surface charge distribution despite the large density of states of the metal and without any new charge arrangement due to bond formation. Figure 2.15 shows the band diagram of a metal/n-type semiconductor contact with a surface charge density D_{GS} on the semiconductor/dielectric interface. After band alignment the semiconductor surface is charged with Q_{GS}, while the charge neutrality is maintained through $Q_{GS} + Q_m + Q_S = 0$. Q_S is the semiconductor charge. Due to the surface charges on either side of the dielectric gap, this gap represents an interface dipole that screens the work function difference between the metal and the semiconductor, hence alternating the expected SBH. The SBH can be expressed as [100]

$$\phi_B = S_{GS}(\phi_c - \chi_s) + (1 - S_{GS})(E_g/q - \phi_{CNL}),\qquad(2.36)$$

with S_{GS} being

$$S_{GS} = \left(1 + \frac{q^2 \delta_{gap} D_{GS}}{\varepsilon_{gap}}\right)^{-1},\qquad(2.37)$$

where ε_{gap} is the permittivity of the gap dielectric layer. This S_{GS} can be identified as the S-parameter introduced above as a measure if experimentally obtained contacts follow the Schottky-Mott relation. Equation (2.36) is frequently used to explain the influence of FLP on the measured SBH. If S is close to 1, the second term can be neglected, and the equation becomes the Schottky-Mott equation. If S is small, the second term becomes dominant, pinning the FL towards the CNL and making it independent of ϕ_m. The presence of an insulating gap between metal and semiconductor seemed reasonable at the time when the theory was introduced, when cleaning and deposition techniques were not that evolved, and no techniques existed to visualize such thin layers. Nowadays devices with epitaxial quality, having no dielectric layer, can be produced, still not obeying Schottky-Mott and Anderson rule. Additionally, if a dielectric layer would be present at the interface, it would also influence the surface state distribution of either the metal and the semiconductor as chemical bond formation will take place towards the dielectric, introducing new states as well as interface dipoles [95], [101]. The fixed separation model is a rather simple model but proved wrong in truly describing the reason for the observed work function screening [95].

Another well-known concept is that of metal-induced gap states (MIGS) [102], now under the more realistic assumption of direct contact between metal and semiconductor. A tail of the metals wave function penetrates into the semiconductor, creating states inside the band gap [95], [101]. These states are physically located slightly inside the semiconductor and not directly at the interface. Assuming this MIGS to be located some distance away from the interface fulfills the same purpose as the gap introduced in the fixed separation model, namely to physically separate the interface charge from the metal to form a dipole layer. Under this assumption, the same concept of a charge distribution D_{MIGS} and a CNL can be used together with Equation. (2.36) without the need for the physically unrealistic gap layer. Nevertheless, the MIGS model also has its weaknesses and necessary assumptions like the independence of the MIGS distribution on the type of metal, and that the CNL needs to be an intrinsic semiconductor property. This assumptions disagree with simulations [95], [101], [103].

The most likely process being responsible for the screening of the work functions and hence the pinning of the FL on the interface is a rather complex process involved in the formation of dipoles during contact formation. The keyword in the interface formation is "chemistry". When bringing a metal and a semiconductor, or two semiconductors, in contact, completely new bonds are forming, and all electronic states are rearranging. Charge transfer takes place through the entire energy range of occupied states in the metal and the semiconductor, inside and beyond the band gap. A detailed overview of the complex topic of interface chemistry and contact formation is given in an excellent review of Tung [95]. Although the fixed separation and the MIGS model described above have their known weaknesses, they are widely applied in characterizing Schottky contacts and heterojunctions. The qualification of FLP via the extraction of the S-parameter and ϕ_{CNL} of experimentally measured ϕ_B over ϕ_m plots is straightforward and state of the art. These parameters are suitable for qualification and comparison of e.g. deposition methods and surface preparation techniques.

Effects of FLP can be reduced and tailored by some measures. For example, the semiconductor Ge is known to have extraordinarily strong FLP close to the valence band edge. By inserting an ultra-thin insulating layer (e.g. GeO_x) between semiconductor and metal the FL could significantly be unpinned [104]. Also by amorphization or depositing of an amorphous semiconductor layer between the MS interface, the FL will be pinned closer to the middle of the band gap [97].

Also, 4H-SiC Schottky diodes are affected by FLP, although it is rather weak [105]–[107]. For Si/4H-SiC heterojunction diodes rather high FLP is observed when produced by surface activated bonding [43], [46]. Due to the relatively high S-parameter of 4H-SiC SCs, no real reduction of FLP, but a shift of the CNL is observed with thin insulating layers [108]. Intentionally amorphized surfaces [106], [109] or the creation of a surface near SiC_xO_x layer [110] can be used to intentionally pin the Fermi level close to mid-band with SBHs in the range of 0.8 to 1.2 eV.

2.3.5 Inhomogeneous SBH

Parts of this section have been published in [94].

The presence of a locally non-homogenous interface and hence an inhomogeneous spatial potential distribution is quite obvious, especially if junctions are not of epitaxial quality. Most MS interfaces are made out of a polycrystalline metallization, consisting of regions with different crystallographic orientations and grain boundaries, leading to different interface reconstructions, hence charge distributions, and as a consequence different barrier heights. Also, unintentional contaminations of small particles and crystal defects in the substrate can account for a local variation of the SBH. Even the random distribution of dopant atoms close to the surface can lead to small deviations of the local SBH [95]. First experiments regarding the determination of the inhomogeneous barrier height date back to the 1980s [111]–[113]. The consideration of SBH inhomogeneities can be mandatory as they can be responsible for deviations from ideal IV-curves, showing double or multiple bumps in the semi-log IV data [114]–[118], unusually high and bias dependent ideality factors [119], [120], as well as non-linear Richardson plots [111], [121]. Also, deviations from the SBH derived from IV and capacitance-voltage (CV) measurements are frequently observed when interface inhomogeneities are present [122].

A simple and intuitive approach to derive the current transport over an inhomogeneous junction, comprising of regions with SBHs $\phi_{B,i}$ of areas A_i is to consider them as parallel current paths where each region has a current flow described by Equation (2.33), giving in total

$$I(V) = \sum_i I_i = A^* T^2 [\exp(\beta V) - 1] \sum_i A_i \exp(-\beta \phi_{B,i}).$$

(2.38)

Figure 2.16 shows a schematic illustration of such an interface, comprising out of a homogenous background with a SBH of $\phi_B{}^0$ along with several patches with higher or lower SBH than the background. The deviation of an individual SBH patch to the background is Δ_i. This approach is called the parallel conduction model [123] and works well for individual patch sizes larger than the semiconductor Debye length [124]. Werner and Gütter [121] derived a theory based on the parallel conduction model, assuming a Gaussian distribution of the SBHs. Tung [93], [125] was the first to propose a model to describe barrier height inhomogeneities considering the pinch-off effect and was able to describe most of the measured deviations from ideal IV curves and ideality factor effects like the T0-anomaly [126], [127]. His theory considers the effect of the surrounding high barrier region on the potential distribution around a patch with lower SBH. Especially at small patch sizes, low doping
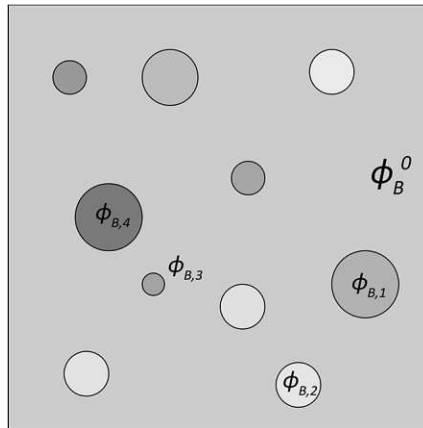
Figure 2.16: Top view of a MS interface with circular patches, representing barrier height inhomogeneities. The homogenous background with a SBH of $\phi_B{}^0$ is distorted by patches of higher or lower SBH $\phi_{B,i} = \phi_B{}^0 - \Delta_i$.

concentrations and high forward biases, the potential in the depletion region underneath such a patch does not fall off linearly, but bulges up close to the surface, creating a potential barrier higher than the surface potential. The new potential barrier is designated as "saddle-point potential". This so-called potential pinch-off is responsible for the observed doping and voltage dependencies of the barrier height inhomogeneities. Using a single dipole approximation, Tung was able to derive an analytical solution to calculate the saddle-point potential as functions of voltage, doping concentration, temperature, and the radius and depth of the low SBH patch in good agreement to numerical simulation [128]. Ballistic electron emission microscopy measurements of artificially generated inhomogeneous SBs were able to prove the model of pinch-off proposed by Tung [129], [130]. Good results of fitting the Tung model and a Gaussian distribution of patch parameters were achieved on different SCs, further validating its ability to describe the current transport of most real SCs [119], [131], [132].

Including the Tung model, the total current over an inhomogeneous SB can be described as a combination of patches that are pinched-off ("p-o"), patches that are not pinched-off ("not p-o"), and the current over the homogenous background like

$$I = \sum_{i}^{\text{"not p-o"}} I_{i,\text{npo}} + \sum_{i}^{\text{"p-o"}} I_{i,\text{po}} + I_{\text{bg}}. \tag{2.39}$$

The individual current fractions follow by

$$\sum_{i}^{\text{"not p-o"}} I_{i,\text{npo}} = A^* T^2 \sum_{i}^{\text{"not p-o"}} A_i \exp(-\beta\phi_{B,i}) \left[\exp\left(\beta V - \beta I_i \frac{\rho_s t_{epi}}{A_i}\right) - 1\right] \tag{2.40}$$

$$\sum_{i}^{\text{"p-o"}} I_{i,\text{po}} = A^* T^2 \sum_{i}^{\text{"p-o"}} A_{i,\text{eff}} \exp(-\beta\phi_{B,i,\text{eff}}) \left[\exp\left(\beta V \right. \right.$$
$$\left. \left. - \beta I_i \left(\frac{\rho_s}{2\sqrt{A_{i,\text{eff}}\pi}} \arctan\left(\frac{2t_{\text{epi}}}{\sqrt{A_{i,\text{eff}}/\pi)}}\right)\right)\right) - 1\right] \tag{2.41}$$

$$I_{\text{bg}} = A^* A_{\text{bg}} T^2 \exp(-\beta\phi_B^0)\left[\exp(\beta V - \beta R_s I_{\text{bg}}) - 1\right]. \tag{2.42}$$

All three components are based on the TE Equation (2.33). In the case of not pinched-off patches, the interface is divided like in the parallel conduction method with each patch having its individual area A_i and SBH $\phi_{B,i}$. The pinched-off patches are described basically in the same way, but with each patch having an effective area $A_{i,\text{eff}}$ and an effective SBH $\phi_{B,i,\text{eff}}$ that can differ from their actual area and SBH if interactions are neglected. In contrast to the not pinched-off patches, these effective parameters are dependent on the doping concentration, the applied voltage, and the temperature. Due to the partially very small cross-sectional areas of the pinched-off patches, the series resistance of a patch can be very spreading in nature and is therefore considered in the most general case for circular shaped pads [95], [133]. The last contribution is that from the background, which is the region between the patches, which is assumed uniform in barrier height. Other quantities used in the equation are the SiC epi-layer thickness t_{epi}, the resistivity ρ_s of the epi-layer, and the overall device series resistance R_s, which mainly consists of the ohmic contacts to the p-Si and to the SiC.

Tung [125], [128] found a good approximation to describe the pinch-off effects using a point-dipole approximation. He showed that circular patches with a radius R_0 and a barrier height ϕ_B^0-Δ can be described using a single patch parameter
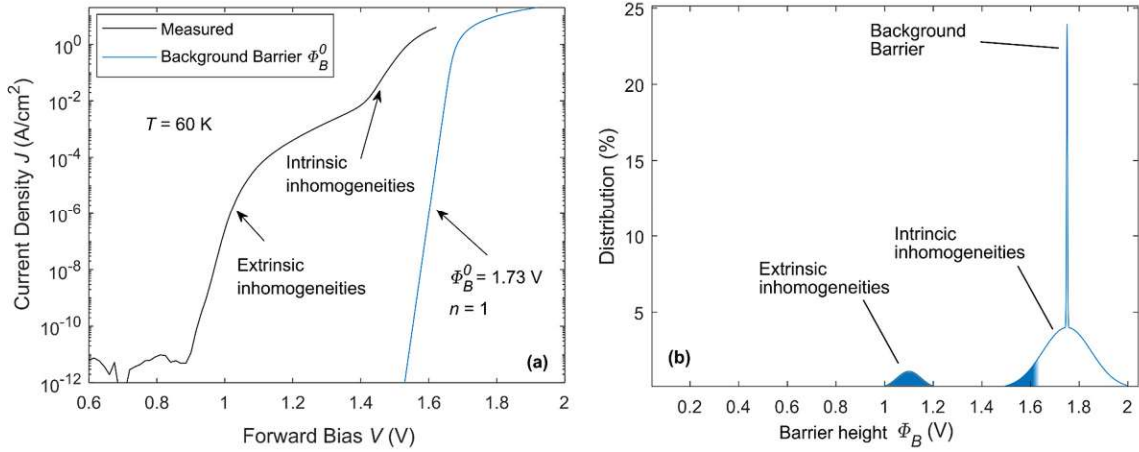
Figure 2.17: Measured IV characteristic at $T = 60$ K of an p-Si/4H-SiC heterojunction diode along with the theoretical IV curve of a diode with a uniform barrier of ϕ_B^0 at $T = 60$ K. Two regions of the measured curve are assigned which are assumed to be dominated by a Gaussian distribution of barrier inhomogeneities of rather intrinsic and extrinsic source, respectively. (b) Schematic illustration of the barrier height distribution at a certain voltage. Blue filled areas indicate barriers that contribute to the current transport.

$$\gamma = 3\left(\frac{\Delta R_0^2}{4}\right)^{\frac{1}{3}}. \tag{2.43}$$

Using this patch parameter, the effective SBH, the effective area, and the effective ideality factor of a patch with a patch parameter γ_i can be calculated by

$$\phi_{B,i,\text{eff}} = \phi_B^0 - \gamma_i \left(\frac{\psi_{\text{bb}}}{\eta_s}\right)^{\frac{1}{3}}, \tag{2.44}$$

$$A_{i,\text{eff}} = \frac{4\pi\gamma_i}{9\beta}\left(\frac{\eta_s}{\psi_{\text{bb}}}\right)^{\frac{2}{3}}, \tag{2.45}$$

$$\eta_{i,eff} = 1 + \frac{\gamma_i \eta_s^{-\frac{1}{3}} \psi_{\text{bb}}^{-\frac{2}{3}}}{3}, \tag{2.46}$$

with $\psi_{\text{bb}} = \phi_B^0 - \phi_n - V$ being the band bending and $\eta_s = \varepsilon_s / (qN_D)$. Band bending and built-in potential are related via $\psi_{\text{bi}} = \psi_{\text{bb}}(V = 0)$. Here and for the calculation of the depletion width W_d, the carrier concentration N_D is assumed to be the total number of donors, hence complete ionization is assumed. This assumption is valid and mandatory if the device is operated in static mode (as described in the section about incomplete ionization.). During current-voltage-temperature (IVT) characterization, this condition is usually met even at very low temperatures.

To further emphasize the need of considering SBH inhomogeneities, Figure 2.17 depicts a measured IV curve, along with an ideal one. Especially at lower temperatures, when the energetical distribution of charge carries is very sharp, due to the Fermi-Dirac distribution, the current will predominantly flow through the lowest SBH patches. The plot in Figure 2.17a shows an IV curve of a p⁺-Si/4H-SiC heterojunction diodes measured at $T = 60$ K, exhibiting strong nonidealities in the form of a double bump. Additionally, an ideal IV curve is plotted using the barrier height evaluated using the CV method from the same diode, which is close to the average background barrier ϕ_B^0. The discrepancy between

29

measurement and the ideal curve is not only present at low forward biases, when the low SBH patches are conducting, but also at very high biases when the series resistance already starts to limit the current.

In Figure 2.17b, a distribution of SBHs at a certain bias is illustrated, which can best be used to describe the measured IV curve. Two gaussian SBH distributions along with the background barrier ϕ_B^0 are assumed to be responsible for the deviations compared to ideal behavior.

The first distribution is assumed to consist of low SBH patches with rather large size of mostly "extrinsic" origin e.g. contaminations. Depending on the source of the contamination, several distributions of extrinsic origin might exist. The second distribution is centered around the average background barrier ϕ_B^0 and is assumed to be of "intrinsic" source like defects in the semiconductor, dopant fluctuations, and variations in the surface potential due to e.g. grain boundaries. Intrinsic inhomogeneities are relatively small-sized patches. Similar assumptions of multiply patch distributions have been made before [113]–[116]. The distribution in this illustration is not to scale. The background is assumed to cover most of the interface area. The blue filled area in the distribution represents the barriers that are contributing to the current flow. This region of contribution is strongly temperature and voltage-dependent. This describes the shape of the measured IV characteristic, especially at low temperatures very well. At lower forward voltages, only the extrinsic inhomogeneities contribute to the current flow until they are satisfied and an ohmic current limiting starts to dominate. If the voltage is further increased, the intrinsic barrier distribution starts to contribute as well, allowing for a strong increase of the current. At low temperatures, the ohmic saturations starts to limit the current flow before the background barriers can even contribute to the current. At higher temperatures, the charge carrier distribution is no longer as sharp, but much more blurred as a result of the Fermi-Dirac distribution. Therefore, the background barrier contributes to the current flow as well and artifacts of inhomogeneities are barely visible.

Depending on the manufacturing method, cleanroom quality, and very importantly the surface preparation method, inhomogeneities can have a major impact on the measured IV curves, hence on the device performance, especially at low and moderate temperatures. If the measured IV curves show strong distortions, the corresponding ideality factors, determined by fitting the thermionic emission model, are often high and voltage-dependent. Also, the deviations between CV and IV extracted SBHs are large in the presence of SBH inhomogeneities, making these values less suitable for quantitative comparison. The implementation of the Tung model might be necessary to estimate the real SBH distribution. Also, the influence of different manufacturing parameters or surface preparation steps on the quantity of inhomogeneities might be monitored by applying Tung's model to experimental data.

2.3.6 Ohmic contacts

The ohmic contact is a non-rectifying contact between a metal and a semiconductor with a linear and symmetric IV characteristic and is needed for the realization of almost every semiconductor device. Ideally, the contact resistance is zero. As discussed above, the SBH of a MS contact can be estimated by the Schottky-Mott rule. For an ideal ohmic contact, the built-in voltage must be zero, therefore the Schottky-Mott rule gives the condition $\phi_m <= \phi_s$ for an ohmic contact to n-type semiconductors and $\phi_m >= \phi_s$ to p-type semiconductors [8]. On moderately doped n-type semiconductors ϕ_s is slightly lower than the electron affinity χ_s. On p-type semiconductors, ϕ_s is much larger, by a value of almost the band gap spacing. Effects like FLP can further complicate the formation of an ohmic contact by pinning the Fermi level near the middle of the band gap, making the ohmic behavior rather independent of the corresponding metal work function. If no metallization can be found to form proper ohmic contacts, an often-used approach to achieve or even lower the ohmic contact resistance of MS contacts is the usage of a high semiconductor doping concentration. The high doping concentration will result in a very thin depletion region and hence, Schottky barrier. If the doping concentration is high enough, tunneling through the barrier will dominate resulting in an ohmic current characteristic. The highly doped regions can locally be generated by e.g., ion implantation or diffusion.

In case of SiC, the formation of low resistance ohmic contacts is challenging due to the high band gap. The condition for n-type ohmic contacts is barely meet by any metal [6] due to the rather low electron affinity of 4H-SiC of about 3.1 to 3.6 V [138], especially considering the high-temperature stability needed for power electronics. For p-type 4H-SiC metals with a work function larger than 6eV would be needed to fulfill the condition $\phi_m > \phi_s$ of ideal ohmic contact formation due to the wide band gap [6]. Pure metals with such a large work functions do not exist and only some metal oxides show work functions that high [139]. Although no ideal ohmic contact is possible to 4H-SiC, low SBH Schottky contacts can have quite ohmic like behavior. By additionally using high doping concentrations and high temperature rapid thermal annealing, ohmic contacts with contact resistance values below 10^{-6} Ωcm^2 could be achieved on n-type 4H-SiC [140]. For n-type 4H-SiC the best candidates are metals and combinations of Ni, Ti, Ta and Pt [141], [142]. On p-type 4H-SiC, slightly higher contact resistances are found by combining Al, Ti and Ni [141], [143], [144]. Annealing temperatures for ohmic contact formation is between 800 and 1050 °C. A list providing the latest research of ohmic contacts to SiC using various metals and surface treatments can be found in [6], [140].

Due to the non-ideal nature of ohmic MS contacts, a contact resistance is always present. Figure 2.18 provides a schematic illustration of three MS contacts and distinguishes between two cases of current flow. A lateral (horizontal) flow of current between metal contacts in a conductive film (e.g. semiconductor) and a vertical current flow between two opposite metal contacts separated by a conductive substrate. Figure 2.18(b) shows an equivalent circuit of a current flowing between Metal 1
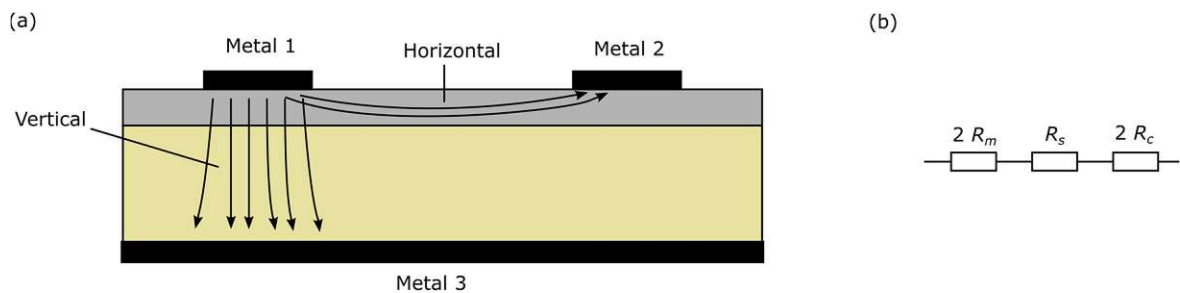

Figure 2.18: (a) Illustration of vertical and horizontal current flow between metal contacts on a semiconductor substrate with a thin semiconducting layer. (b) Equivalent circuit of metal 1 to metal 2 current path. No current flow in the substrate is assumed here.

and Metal 2, while no current flow through the substrate is assumed in this case. The total resistance R_t which would be measured, when probing between the two contacts is composed out of three components. The spreading resistance of the metal contacts R_m, the resistance of the semiconductor film R_s and the contact resistance R_c. Using highly conductive metals (e.g. Copper, Aluminum, …) and thick enough films the metal resistance can normally be reduced to such an extent that it no longer has any influence on the total resistance. The semiconductor resistance depends on the device design (track(trace), film or bulk). It is usually given in either the resistivity ρ_s in (Ωcm) or in case of a thin film or a surface near doping layer as the sheet resistance R_{sh} in (Ω/sq). The sheet resistance is a special unit used to specify the resistance of films with uniform thickness t_s and is related to the resistivity by $\rho_s = R_{\text{sh}} \cdot t_s$. The usual quantity when comparing contact resistance values is the contact resistivity or specific contact resistivity ρ_c in (Ωcm^2). It needs to be distinguished from the specific interfacial resistivity ρ_i which is only the resistivity of the interface itself, whereas ρ_c also includes the resistive contributions of the materials directly above and below the interface. The contact resistance is always defined at zero voltage. More information and theoretical evaluations of the interfacial resistivity ρ_i of metal-semiconductor contacts can be found in [82]. Measurements usually give ρ_c because the measurement of only the interface resistance is almost impossible. Some measurement techniques are introduced in Section 3.3.1.

2.4 Metal-induced crystallization

Metal-induced crystallization (MIC) is a well-known process to reduce the crystallization temperatures of amorphous semiconductors substantially below their solid phase crystallization (SPC) temperatures with a metal as a catalyst. This phenomena has first been discovered in the late 1960s for a-Ge [145] and later for a-Si [146] and has been widely investigated since then [147]–[149]. In the case of a-Si, crystallization temperatures as low as 150 °C have been achieved in contrast to over 600 °C needed for SPC without the presence of a metal catalyst. The process is widely used in photovoltaic technology, for thin-film transistors (TFTs), data storage applications, and other applications where a low-temperature budget is mandatory [149]. The much lower temperatures needed to form c-Si are of interest especially in price-sensitive mass production. Amorphous silicon can be deposited at high rates at low temperatures using plasma-assisted processes. The subsequent crystallization at much lower temperatures requires less energy compared to heating to several hundred degrees. Also, the combination with temperature-sensitive materials like polymer substrates is possible when applying MIC [150].

In the past, numerous studies about MIC, especially using Al and Si on SiO$_2$ have been performed, investigating the influence of temperature, time, and film thickness [149], [151]–[156]. Also, non-conventional semiconductors have been successfully crystallized, for example, zinc tin oxide using tantalum as a crystallization catalyst [157]. If monocrystalline substrates are used, even epitaxial crystallization of the amorphous semiconductors can occur [158]–[160]. The usage of MIC in combination with SiC substrates is rarely investigated [161]. On the other hand, MIC has been used successfully to crystallize a-SiC [162].

MIC can be divided into two species, a combination of amorphous semiconductors with compound forming metals (e.g. Ni, Cu, Pt,...) and metals forming simple eutectic binary systems (non-compound forming) (e.g. Al, Au, Ag,…) [148], [152].

Compound forming metals like to alloy with the amorphous semiconductor to form compounds at moderate temperatures. In case of Si and the often-used metal Ni it will form silicides like NiSi$_2$. Grains of this compound then move through the a-Si leaving behind <111> oriented traces of c-Si [163], [164]. This effect can be used to achieve directed crystallization in certain areas. Lee and Joo [165] developed

a process using Ni to laterally crystallize a-Si under the gate oxide of a TFT, using about 100 °C lower temperatures than classic TFT crystallization processes, at the same time achieving better device properties. This process, where covered regions (e.g. by a gate oxide) are crystallized laterally starting at the exposed side facets, is called metal-induced lateral crystallization. The lateral crystallization has a speed of about 1.6 µm/s and can therefore be faster than conventional SPC of a-Si. The crystallization temperature of the compound forming metals is generally higher than for non-compound forming metals. Knaepen et al. [148] conducted a comprehensive *in-situ* heating X-ray diffractometry (XRD) study to determine the crystallization temperature of a-Si combined with various metals.

If non-compound forming metals are in contact with amorphous semiconductors a different process is involved. The presence of a metal can significantly weaken the relatively strong covalent bond between semiconductor atoms, in case of silicon the Si-Si bonds. This strong bond is responsible for the high bulk crystallization temperatures of semiconductors [166]. This phenomenon is called metal-induced bond-weakening and is caused by an effect called Coulomb screening. The semiconductor atoms in close proximity to the metal are therefore able to move relatively free at low temperatures [167]. These "quasi-free" atoms can diffuse along the metal/semiconductor interface or along metal/metal interfaces, present at grain boundaries (GBs). Calculations and *in-situ* transmission electron microscopy (TEM) investigations revealed a GB-wetting to be thermodynamically favorable for the Al/a-Si system [168]. Wetting and diffusion along GB take place at temperatures as low as 150 °C. The nucleation of the free Si atoms in the metal GBs becomes thermodynamically favorable followed by a subsequent grain growth. If the metal and the semiconductor are present in form of stacked thin layers, this process of diffusion and crystallization can lead to a full layer exchange between metal and semiconductor, called metal-induced layer exchange (MILE). The MILE process is schematically illustrated in Figure 2.19.

The diffusion, the nucleation, and the subsequent crystal growth are thermodynamically driven processes with the aim of lowering the overall energy. In the following, these thermodynamics are discussed for the 4H-SiC/a-Si/Al system based on the model of Wang et al. [152]. The following equations are suitable for all kinds of material combinations if the required material parameters are known as a function of temperature. The thermodynamics of Al induced MIC has been well studied and can be split into three steps [152], [168], [169]: (1) grain boundary wetting, (2) Si nucleation, and (3) Si grain growth. All these processes are based on the minimization of the energy of a system consisting of bulk materials, surfaces, and interfaces. Compared to the Si/Al system, the MIC process on SiC introduces another interface, namely that to the SiC, requiring additional calculations to estimate its influence. For the calculations, the surface energies $\gamma_{\langle a \rangle}$ of all surfaces and the interface energies $\gamma_{\langle a \rangle, \langle b \rangle}$ of all interface combinations are required. Table 2.3 lists all parameters needed for these calculations. Brackets are used to distinguish between amorphous {} and crystalline ⟨⟩ phases. Especially for SiC it is difficult to find appropriate values for the interface energies. Widely scattered results even for the
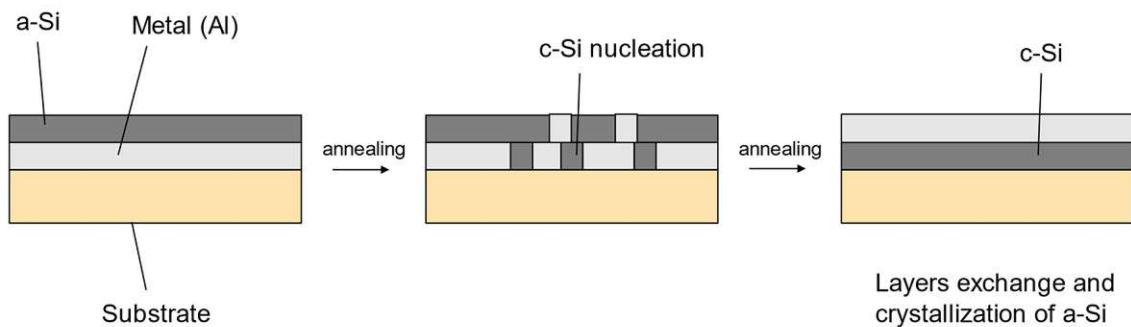

Figure 2.19: Schematic illustration of the crystallization and layer exchange process of mic using Al.

Table 2.3: Surface and interface energy parameters used for thermodynamic calculations. If not mentioned otherwise, no temperature range was specified.

Parameter	Value (J/m^2)	Comments
$\gamma_{\langle Si\rangle}$	1.37	[117], [126], [128],[129],T~200–300 °C
$\gamma_{\{Si\}}$	0.98	[152], [170]–[172],T~200–300 °C
$\gamma_{\langle Al\rangle}$	0.94 to 1.13	[152], [173]
$\gamma_{\langle SiC\rangle}$	2.899 to 3.535	[174], 4H-SiC, Si-face
$\gamma^{GB}_{\langle Al\rangle}$	0.38	[168]
$\gamma_{\langle Si\rangle\{Si\}}$	0.085	[152], [170]–[172],T~200–300 °C
$\gamma_{\langle Al\rangle\{Si\}}$	0.08	[152], [170]–[172],T~200–300 °C
$\gamma_{\langle Al\rangle\langle Si\rangle}$	0.44	[152], [170]–[172],T~200–300 °C
$\gamma_{\langle SiC\rangle\langle Si\rangle}$	1.875 to 2.03	[175]
$\gamma_{\langle SiC\rangle\{Si\}}$	1.489	[176], from liquid Si
$\gamma_{\langle SiC\rangle\langle Al\rangle}$	2.69 to 3.515	[173], [174]

surface energies of the two faces are found. The most recent and reasonable values were used for the calculations. Usually, also no temperature dependencies are available, but very weak dependencies are normally found for interface and surface energies [152], [172]. Without exact values and proper temperature dependencies only rough estimations are possible if a process is likely to occur or not in the 200 to 300 °C MIC temperature range. In well-studied systems like the Al/Si system also temperature dependencies of the thermodynamic quantities are available, also allowing an estimation of the temperatures when certain processes will start to be thermodynamically favorable. If not directly available, interface energies are calculated from the work of adhesion W_{ad} using the simple approximation $\gamma_{\langle a\rangle,\langle b\rangle} = \gamma_{\langle a\rangle} + \gamma_{\langle b\rangle} - W_{ad}$ [177], because this value is found more often. For the $\langle SiC\rangle\langle Si\rangle$ interface, only interface energies of the Si(220)/6H-SiC(10-10) interface could be found. The interface energy for the $\langle SiC\rangle\{Si\}$ interface was taken from liquid Si/SiC measurements and extrapolated down to 250 °C assuming a linear temperature dependency.

The first process for MIC and especially MILE is grain boundary wetting. It has been shown theoretically and by *in-situ* observations, that Si is able to diffuse along Al-GB at temperatures as low as 150 °C. Thermodynamically the wetting of an interface by a-Si is favorable if the interface energies of the two newly generated interfaces (with the a-Si) are lower than that of the original interface. For diffusion along Al-GBs and at the SiC/Al interface it follows:

$$\Delta\gamma_D^{Si\ in\ Al\ GB} = \gamma_{\langle Al\rangle}^{GB} - 2\gamma_{\langle Al\rangle\{Si\}} \tag{2.47}$$

$$\Delta\gamma_D^{Si\ at\ Al/SiC\ interf} = \gamma_{\langle SiC\rangle\langle Al\rangle} - \gamma_{\langle SiC\rangle\{Si\}} - \gamma_{\langle Al\rangle\{Si\}}. \tag{2.48}$$

The positive driving force resulting from the presence of Al-GBs was already shown [152], but also for the SiC/Al interface using the whole range of available energies a positive driving force between 1.12 to 1.95 J/m^2 is found. The huge spread is a direct consequence of the large scatter in the original data, but even for the worst-case scenario, a positive driving force remains. Therefore, diffusion of bond weakened Si atoms is likely to occur in the temperature range of 200 to 300 °C, even though the uncertainty in using $\gamma_{\langle SiC\rangle\{Si\}}$ from liquid Si at much higher temperatures is high. The positive driving force associated with Al-GBs was shown to require "high-angle" GBs [168].

The second process towards a MIC-induced layer exchange is nucleation. The nucleation of a semiconductor is usually hindered because the interface of two crystalline materials often has a higher interface energy than that between a crystalline and an amorphous phase. Therefore, a thin amorphous

layer, like in a wetted GB, is often thermodynamically stable at an interface. The crystallization energy $\Delta G^{\text{Cryst}}_{\{Si\}\to\langle Si\rangle}$ is the energy required for the transition from the amorphous to the crystalline phase. For Si it is $-8.8 \cdot 10^8$ J/m^3 at about 250 °C [152]. The negative sign indicates that energy is released during crystallization. But as mentioned before, the energy required to break strong covalent bonds between amorphous semiconductors first needs to be overcome to allow the crystallization to occur. By dividing the energy difference of the interface energies by the crystallization energy the result has the physical quantity of length. This length is referred to as critical thickness h. For example, the critical thickness of the a-Si wetted SiC/Al interface calculates to

$$h^{\text{Si in Al/SiC interf}}_{\langle SiC\rangle\{Si\}\langle Al\rangle} = \frac{\gamma_{\langle SiC\rangle\langle Si\rangle} + \gamma_{\langle Si\rangle\langle Al\rangle} - \gamma_{\langle SiC\rangle\{Si\}} - \gamma_{\langle Al\rangle\{Si\}}}{-\Delta G^{\text{Cryst}}_{\{Si\}\to\langle Si\rangle}} . \qquad (2.49)$$

Again, by taking the spreading in available values into account, h was found to be between 0.85 and 1.02 nm. For a-Si it was shown that nucleation can only occur inside wetted metal GBs. The effect of metal-induced bond weakening, mentioned before, is only affecting the first two atomic monolayers (MLs) of the a-Si (about 0.44 nm) [152]. For nucleation, hence the transformation of a-Si to c-Si the thickness of bond weakened "quasi-free" Si atoms is required to be equal to, or larger than the critical thickness. For Si nucleation, at the Al/a-Si interface, the critical thickness was calculated to be ~4 ML (0.88 nm) at 150 °C and lower with increasing thickness. Due to the bond weakening distance of only ~2 ML no nucleation can occur on Al/a-Si interfaces. Therefore, two Al/a-Si interfaces, namely a wetted GB, are required to achieve the critical thickness to thermodynamically favor the crystalline phase. For reference, if using germanium (Ge) instead of Si, nucleation at the only one Al/a-Ge interface is thermodynamically possible above ~50 °C [152]. In the SiC/a-Si/Al configuration, the Al can only be in contact with the a-Si at one side, resulting in only 0.44 nm bond weakened Si, which is much less than the estimated critical thickness of at least 0.85 nm. Therefore, the calculations would suggest no crystallization to be possible at the wetted Al/SiC interface. This result should be considered carefully as the quality of the used parameters, especially for $\gamma_{\langle SiC\rangle/\langle Si\rangle}$ and $\gamma_{\langle SiC\rangle\{Si\}}$ include a high uncertainty. Until more precise data are available, or the phenomenon has been observed with direct measurements such as *in-situ* TEM, the crystallization of Si at the SiC/Al interface remains unclear.

The third and last process is the growth of the newly nucleated Si grains. For calculating the growth process of an amorphous semiconductor onto an already crystalline semiconductor in direct contact the same concept of a critical thickness as in Equation (2.23) is used. The interface of interest is now the a-Si wetted Si/Al interface, hence Si/a-Si/Al. In Equation (2.23) only the interface energies of the newly formed and the old interfaces need to be adjusted accordingly. It was shown already that the growth of c-Si is favorable at the Al/c-Si interface with new material diffusing along the interface [152]. The grain growth at the SiC/c-Si interface is unlikely, as no interface to a metal is present any more, hence no bond weakened "quasi-free" Si atoms are available at this interface. Therefore, the most likely scenario is assumed to be a diffusion of a-Si along the Al GBs and if not already recrystallized also along the SiC/Al interface. Nucleation will then occur at the Al GBs, followed by grain growth.

An interesting consequence of the fact that nucleation of Si can only take place in Al-GBs, but the continuation of the growth is also possible at the c-Si/Al boundaries is the MILE. The growth of the Si grains is therefore mostly lateral. This lateral grain growth induces compressive stress in the Al and tensile stress in the a-Si supporting the migration of Al towards the a-Si, while the a-Si diffuses along the Al/c-Si interface and incorporates itself in the Si crystals [149]. Finally, the two layers are exchanged, and the amorphous silicon has turned in to poly-Si.

Although most of the thermodynamics on the SiC surface is still subject to debate due to the lack of data, the basics of the thermodynamic concepts of MIC were presented and can be used on different semiconductor/metal combinations if the appropriate quantities are known.

3 Experimental methods

Divided into three parts, the experimental methods for fabrication and characterization of microstructural and electrical properties used in this work are explained.

3.1 Microtechnologies

The first part of the experimental methods focuses on the used fabrication methods for thin film deposition and sample preparation.

3.1.1 Surface preparation and cleaning

The first and perhaps most important step in device fabrication is the surface preparation of the wafers [178], [179]. This step is crucial, especially for microelectronics, where the surface of the wafer becomes an electrically active interface. Also, for the oriented crystalline growth of homoepitaxial or heteroepitaxial layers, the cleaning of the substrate prior to deposition on an atomic scale has the highest importance, as the yield and therefore the financial outcome per wafer can be increased dramatically with proper surface preparation.

Impurities can be grouped into (i) contamination films (e.g. native oxide, organic films), (ii) discrete particles (metals, dust …), and (iii) absorbed atoms [178].

Cleaning processes can be divided into two groups, chemical and physical cleaning. Chemical cleaning processes are often wet solutions made of basic and acidic mixtures, which are able to etch native oxides, remove particles by a slight under etching, and dissolve metallic and organic contaminants [180]. Chemical cleaning can also be done by dry etching using e.g. H_2 or HCL at elevated temperatures [181]. Organic contaminations like residual photoresist can be removed easily using O_2 plasma treatment [180]. Physical cleaning is usually based on the removal of particles or atoms by the transfer of mechanical energy. A purely physical method would be ion sputter etching, where the surface is bombarded with ions and the first few atomic layers including contaminations are removed. The main advantage is, that this could be done *in-situ* prior to deposition without breaking the vacuum, preventing any new surface contaminations. The downside is the surface-near amorphization, which can have a strong impact on film growth and electro-mechanical properties. The use of ultrasound and/or jet forming nozzles, which are physical methods, are often combined with wet chemical solutions to enhance the cleaning performance.

One very common cleaning method, which is widely used in industry and was used for the sample preparation in this theses, is the standard Radio Corporation of America (RCA) [182] cleaning process. The RCA clean consists of two solutions SC-1 and SC-2. SC-1 is made out of H_2O, $NH_4OH(30\%)$, and $H_2O_2(30\%)$ in a ratio of 5:1:1 and effectively removes organic residues and some metals. SC-2 consists of H_2O, $H_2O_2(30\%)$, and $HCl(37\%)$ in a ratio of 6:1:1 and removes the remaining traces of metallic (ionic) contaminants. The tolerances of the mixing ratios are not critical and depend on the corresponding concentration. Only electronic grade chemicals and deionized (DI) water must be used. Both solutions are usually heated to 75–80 °C and the cleaning time is between 10 and 15 min. Employing ultrasonic treatment during cleaning is recommended. Optional steps are a clean in acetone and isopropanol to effectively remove gross organic residuals before the RCA clean. Also, a short hydrofluoric acid (HF) dip prior to and after the SC-1 solution, which removes any oxide residuals from the previous step might be done.

Independent of the cleaning process, the wafer should be processed direct after the cleaning.

3.1.2 **Sputter-deposition**

Sputter-deposition or sometimes "sputtering" is a technique frequently used in microelectronic, MEMS, and other industries to apply functional thin film of rather high quality and purity [183]–[185]. Usual film thicknesses are in the range of 1 nm to a couple of micrometers. It is considered a physical vapor deposition (PVD) process like evaporation, although reactive sputtering involves chemical processes as well [186].

Sputtering is the bombardment of a target material with energetic particles. It can be used for the removal of target material e.g. ion sputter etching (ISE) or to further investigate the sputtered secondary particles (Secondary Ion Mass Spectroscopy). If the sputtered secondary particles are intended to redeposit on a substrate, the process is called sputter-deposition. One of the state-of-the-art techniques is magnetron sputter-deposition, which will be discussed in detail.

A schematic view of a magnetron sputtering system is provided in Figure 3.1. The deposition process is performed inside a vacuum chamber. In the chamber, the target holder (cathode) and substrate holder (anode) form a capacitor like arrangement. A magnetron sputter system differs from a "conventional" sputtering system by having strong permanent magnets located behind the sputtering target. These magnets produce a strong magnetic field in the vicinity of the target. A vacuum pump is plugged to the vacuum chamber usually with an electrically controllable shutter to regulate the gas flow and therefore the chamber pressure. Typically, the pump system consists of two stages: a rough pump (rotary vane pump or roots blower) and a high vacuum pump, often a turbopump. Base pressures in the range of $1 \cdot 10^{-6}$ to $1 \cdot 10^{-8}$ mbar are used. The lower the base pressure, the less residual gases, e.g. O_2 can be incorporated in the film during deposition.

For sputtering, a process gas is introduced into the chamber with a defined flow rate. In combination with the regulated outlet to the pump, a back pressure in the range of several μbar is typical during sputtering. Argon, being an inert gas is frequently used as sputtering gas. A sputtering variation called reactive sputtering uses more reactive sputtering gaseous species like O_2, N_2 or CH_4 which react chemically during the deposition process. An alternating current (AC) or direct current (DC) generator, which is connected between the target and the substrate allows the sputtering gas to ionize and to generate a plasma. The plasma is highly conductive and consists of many free electrons and positively charged Ar^+ Ions, indicated by the numbers (1) and (2) in Figure 3.1. In DC mode the ionized gas atoms
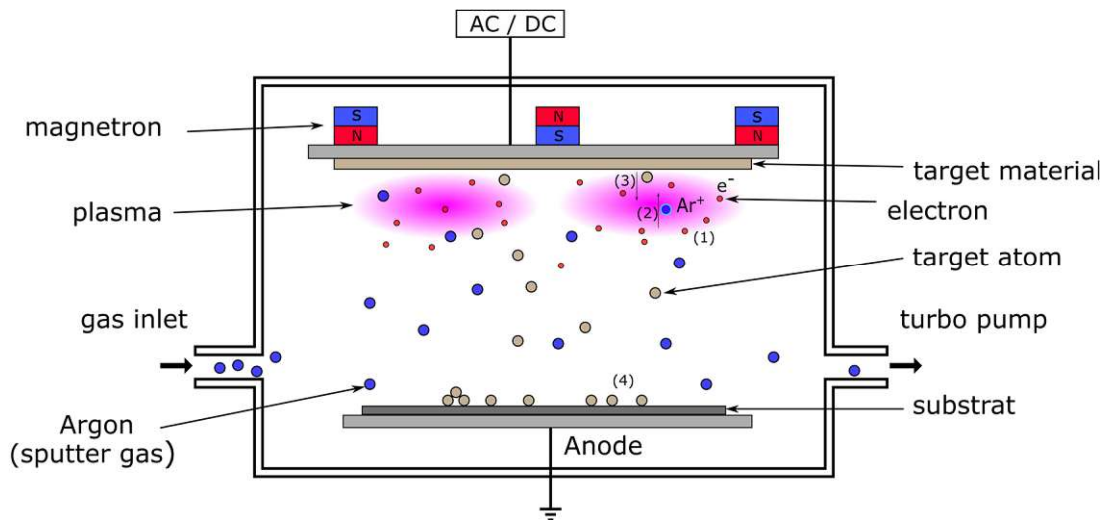
Figure 3.1: Schematic view on a sputtering process.

(e.g. Ar⁺) are accelerated towards the target (cathode), which is on negative potential. In AC mode the direction of acceleration is controlled by the size difference in cathode and anode (self-biasing) or via an externally applied bias. The permanent magnets behind the target lead to a higher ionization rate due to Lorentz force, forcing the electrons in a cycloid trajectory. This can enhance the sputtering rate dramatically compared to conventional sputtering systems. For normal operation, DC sputtering is preferred because it is the simplest approach. AC sputtering can although have advantages when the target material is nonconductive (*e.g* AlN, SiO_2, …).

The accelerated ions with energies of several 10 eV collide with the target and can either interact inelastically by producing secondary ions or elastic where the impulse is transferred via a collision cascade until a target atom is emitted, as illustrated by number (3) in the figure. The threshold energy of the sputtering atom needed to knock out an atom from the target depends on the material and is in the order of 10 to 30 eV. The sputtered target atoms will undergo lots of collisions with gas atoms on their way through the vacuum chamber until they deposit on the substrate or unwanted parts like the chamber walls. This happens because the mean free path of the sputtered atoms is much shorter than the distance between target and substrate at typical sputtering pressures in the μbar range. As a consequence, effects like sidewall deposition in trenches occurs.

Important sputtering parameters that can be controlled are the plasma power, the sputtering pressure, the gas flow, and the distance between the target and substrate, and the target temperature. All these parameters influence the deposition rate and the quality (crystallinity, homogeneity, density…) of the film.

3.1.3 Chemical vapor deposition

Chemical vapor deposition and all its variants are, besides PVD, one of the most important deposition technologies in microelectronics and microsystems technology. It differs from PVD in the way the raw material (precursor) is supplied. In CVD processes, it is supplied in the gas phase or from a vaporized liquid source (bubbler), as opposed to a solid target in PVD processes. Depending on the chamber pressure and the energy source to trigger the chemical process for film growth the CVD technique is grouped into several categories. The two main ones related to this dissertation are plasma-enhanced chemical vapor deposition (PECVD) and LPCVD. Both techniques work at reduced pressures and differ mainly in the way the energy to dissociate the gaseous precursors is provided. The PECVD system uses a plasma discharge and usually moderate temperatures up to about 500 °C, whereas LPCVD systems work at temperatures up to usually 1200 °C. Another categorization of CVD systems is the construction of the reactor. Common reactor designs are tube, barrel, and single wafer (shower head). Depending on
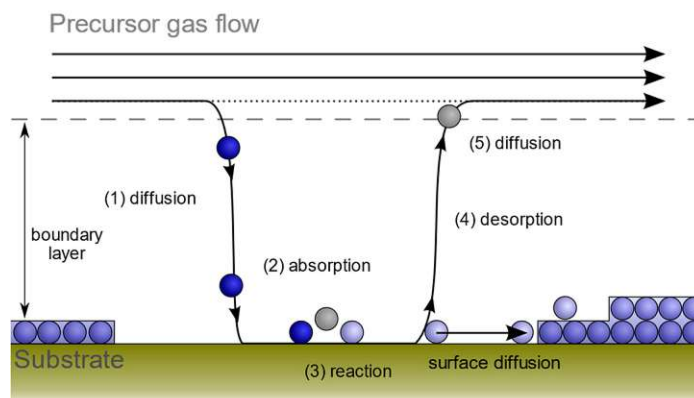
Figure 3.2: Typical sequence of reaction steps in a CVD process. Modified after [187]
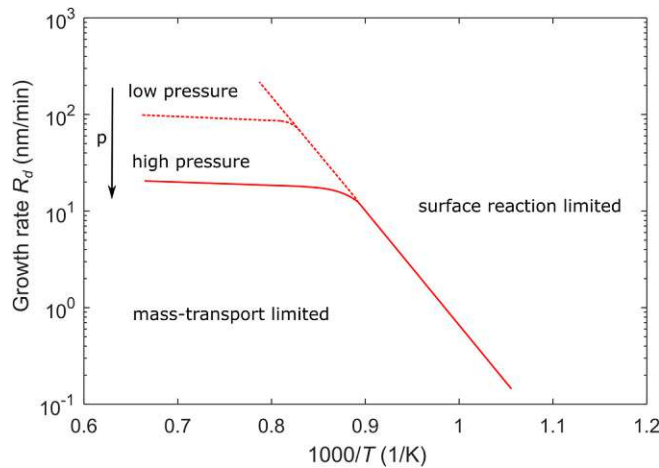
Figure 3.3: Typical growth rate of CVD processes over temperature. The influence of the chamber pressure on the growth rate is also shown. The reactant partial pressure is kept constant in this example.

the location of the heat source, reactors can also be classified as hot or cold-wall type. In a cold-wall reactor only the substrate is heated, whereas in a hot-wall reactor the whole chamber is at an elevated temperature.

Most films can be deposited by both methods, CVD and PVD. Both have their advantages and disadvantages [188], [189]. For example, CVD systems are usually more complex and require more maintenance. Also, the precursor gases for most films are very toxic and explosive. A huge difference lies in the film coverage, whereas most PVD techniques only deposit surfaces facing the source, e.g. the target, whereas CVD techniques can cover any hot surface including deep trenches [184], [190]. Also, the microstructure of the deposited films can differ substantially. Due to the high temperatures compared to PVD, most semiconductors are deposited in crystallized form or even epitaxial, whereas PVD techniques usually result in amorphous or polycrystalline films unless the substrate is heated.

A typical sequence of reaction steps in a CVD process is illustrated in Figure 3.2 [191]. From the continuous, laminar flow of precursor gas, some molecules are able to diffuse through the boundary (1) layer to the substrate surface and get absorbed (2). The boundary layer is the surface near region where the gas flow decreases towards zero at the surface. The absorbed molecules then might undergo a chemical reaction (3), resulting in reaction products, or desorb without reaction. The reaction products will desorb (4) from the surface and diffuse out of the surface near region until they are removed by the gas stream (5). Depending on the surface temperature, the absorbed and reacted molecules on the surface are able to diffuse on the surface until they get incorporated into the growing film.

Since the steps in the growth process are sequential, the slowest one will determine the deposition rate. As a consequence, two main regimes are distinguished in CVD processes. The mass-transport limited regime, where the transport of new reactants hence, their diffusion through the boundary layer to the surface is limiting the growth process, and the reaction limited regime, where the chemical reaction on the surface is the slowest step and limits the overall growth rate. A typical graph of the growth rate as a function of the temperature, including the influence of the pressure is depicted in Figure 3.3. At low temperatures, the growth process is governed by the reaction limited regime and at high temperatures by the mass-transport limited regime. The growth rate R_d, hence growth velocity, of an LPCVD process can be modelled as [192]

$$R_d = \frac{C_g}{N} \frac{k_f h_g}{k_f + h_g},$$

(3.1)

with N being the density of the deposited solid, C_g, the concentration of the reactant gas species, k_f the forward reaction rate of the surface reaction, and h_g the gas transport rate.

In the surface reaction limited regime ($k_f < h_g$), the growth rate is an exponential function of the temperature, following the Arrhenius equation for chemical reactions.

$$k_f = k_0 e^{-\frac{E_A}{k_B T}}, \tag{3.2}$$

with the activation energy E_A and the temperature being the dominant quantity.

In the mass-transport limited regime ($k_f > h_g$), the temperature dependence is low, but the total chamber pressure will influence the deposition rate. The transport rate is given by

$$h_g = \frac{D_g}{\delta(x)}, \tag{3.3}$$

with D_g being the diffusivity of the reactant and $\delta(x)$ the boundary layer thickness. The boundary layer thickness varies inside the chamber position x. D_g and δ are both functions of the total pressure, but the influence on the diffusivity is stronger. A higher total pressure will reduce the diffusivity and hence, reduce the transport rate. As can be seen in Figure 3.3, the transition between the two regions depends on the total chamber pressure as it influences the diffusivity of reactants through the boundary layer.

Increasing the deposition temperature even further will eventually decrease the deposition rate again, as all precursors are consumed until they reach the sample by deposition on the chamber walls (in hot-wall reactors only) or due to gas-phase nucleation [193]. According to Equation (3.1) the reactant concentration C_g directly influences the growth rate. Atmospheric pressure chemical vapor deposition (APCVD) has therefore higher growth rates as the reactant concentration is usually higher. Due to the lower pressure, LPCVD systems are predominantly operated in the reaction limited regime towards much higher temperatures than APCVD systems. This results into a much more homogenous film coverage and the possibility to deposit also deep trenches. The actual growth rate and the film quality are sensitive to changes in partial pressures, flow rates, and temperature. Also, the geometry of the deposition chamber and the position as well as the orientation of the sample influence the gas flow rate across the sample and hence, the deposition rate. Therefore, CVD processes require a high knowledge of the involved processes by the operator. On the other hand, the possibility to vary many parameters gives a lot of flexibility to tune the film quality.

An overview of CVD processes in general can be found in [192], [194]. A very detailed study about the pyrolysis of monosilane, which is used for Si film deposition in this thesis was done by Purnell et al. [195].

3.1.4 Etching

An important step in the fabrication of microelectronic and micromechanical devices is pattering of structures by etching. Etching can be divided into dry and wet etching, whereas dry etching can be physical or chemical or a combination.

Only a compact overview of these etching techniques used in this thesis for device fabrication is given.

Prior to any etching step, a suitable etchant and etching technique must be selected. The selection depends on the material that needs to be etched under consideration of the selectivity to other materials on the sample. If several etchants are suitable the one with the highest selectivity, highest etch rate and lowest toxicity might be the preferred choice. A comprehensive collection of etchants and their etching

Table 3.1: List of materials and etchants used during this thesis. In addition, some selected material are listed serving as mask.

Material to etch	Etchant	Selective to
Al	Phosphoric acid: 85 % H_3PO_4 at 80 °C	Si, SiO2, most metals
SiO_2, Ti, Hf	BOE (buffered oxide etch): 40% NH_4F and 49% HF in a 8:1 ratio	Si and most metals
Si, Mo	Isotropic silicon etch: 49% HF + 65% HNO_3 + H_2O in a 1:7:2 ratio	Au, Pt, Ir
Pt, Mo	Aqua regia: 37% HCl + 65% HNO_3 + H_2O in a 9:3:8 ratio at 60 °C	Si, SiO_2, Si_3N_4, Cr, Nb

rates of different materials can be found in [196]. Before etching, the areas that should not be etched need to be protected by a mask. This mask is usually photoresist because it is easy to pattern by standard photolithography. Under certain circumstances, (e.g. high-temperature etching processes or low selectivity to photoresists) hard masks of solid materials are used.

If no suitable etchant solution is available the "lift-off" technique might be an option, although it is limited to thin films and low-temperature processes and special photoresists with undercut edges are needed.

Table 3.1 lists all materials needed to be etched for device fabrication in this thesis, along with the corresponding etchant and some selective materials, which could serve as a mask to that etchant. For most of the listed materials also dry-etching is possible. Etching of the deposited poly-Si was also tested successfully using SF_6 plasma in a reactive ion etching equipment. In the end, the wet etching was selected as dry etching is much more time consuming, being a vacuum process.

3.2 Microstructural and chemical measurement techniques

In the following, some of the most frequently used microstructural characterization techniques of this thesis are described.

3.2.1 Electron microscopy

Scanning electron microscopy (SEM) and TEM and its analytical methods are crucial tools for material research and microelectronics. Both are dependent on the very short wavelength of high-energy electrons. For example, electrons with 50 V acceleration voltage have a de Broglie wavelength of about 0.17 nm. By increasing the voltage to 50 kV, the wavelength decreases to only 5 pm [197]. This wavelength is much smaller than that of light used for optical microscopy (400 to 800 nm) and is therefore suitable for much higher resolution imaging. In contrast to other short wavelength radiation (e.g. X-rays), electron beams are rather easy to focus and to deflect by magnetic lenses.

In the 1930s, TEM was the first kind of electron microscope that was invented. A conventional TEM consists out of three lenses to produce a parallel electron beam at the sample and a magnified version of

the transmitted beam on a screen. Modern TEMs have additional intermediate lenses for better imaging and usability. The fact that a TEM magnifies the transmitted electron beam, the sample needs to be thin enough to allow enough electrons to transmit through the sample. The sample preparation for TEM is therefore destructive. Using grinding and subsequent ion beam milling the sample can be thinned to 10 to 100 nm at certain regions, being ideal for high magnification imaging. If specific regions of a specimen are of interest a more time-intensive preparation using focused ion beam must be used. By exploiting not only the amplitude of the transmitted electron beam but also the phase information of this transmitted wave, high resolution (HR) images with subatomic resolution are achievable. An electron diffraction pattern can also be generated by TEM. Electrons deflected by parallel lattice planes generate a diffraction pattern in the image plane of the objective lens. Instead of the real image, the diffraction pattern can be magnified on the screen, giving useful information about the crystal structure and orientation of the specimen. Because the sample area from which the diffraction pattern can be recorded can be selected with an aperture, it is called selected area electron diffraction (SAED). Another important mode during TEM analysis is the scanning transmission electron microscopy (STEM) mode. It works like a SEM using a focused electron beam but still uses the transmitted electron signal for imaging. Modern TEMs available on the market can achieve resolutions down to about 60 pm using lens-aberration correction and an acceleration voltage of 300 kV, respectively.

The SEM was invented a few years after the TEM because it is more complex to control a scanning electron beam across a sample surface. A SEM uses the possibility of electrons being backscattered by a matter surface. This can be either a backscattered primary electron, or a secondary electron emitted by an atom after interaction with a primary electron. When an electron beam hits matter several different
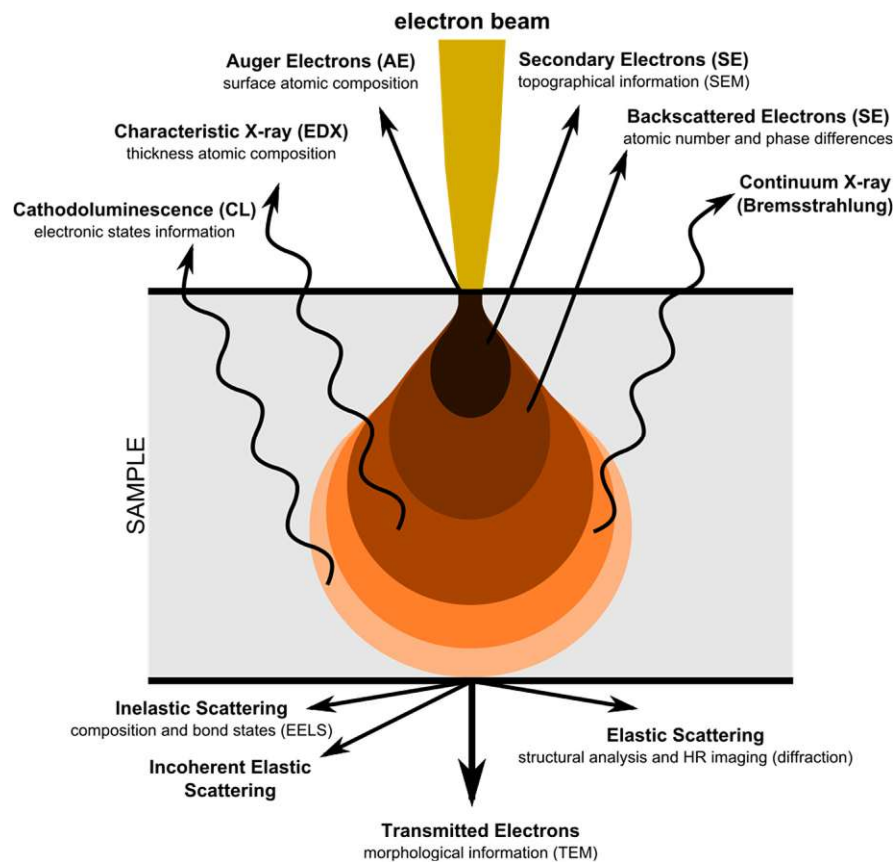
Figure 3.4: Schematic illustration of an electron beam indenting into matter including secondary radiation products generated by the beam. [198]

interactions can occur resulting in various secondary radiations of different wavelengths as illustrated in Figure 3.4 A big advantage of SEM over TEM is the much easier and often non-destructive sample preparation. Also, it offers the possibility to observe the sample surface, rather than a thin bulk region. Nevertheless, the achievable resolution is with about 1 nm way above that of TEM and not in the atomic scale.

As can be seen in Figure 3.4, several secondary radiations emit from the specimen due to the interactions with the electron beam. Several analytical techniques take advantage of these emissions to acquire further information about e.g. the chemical composition of the sample. The by far most frequently used technique is energy-dispersive X-ray spectroscopy (EDX), which uses the emitted characteristic X-rays for elemental analysis. Another interesting technique is electron energy loss spectroscopy (EELS) which also provides information about the elemental composition of a sample, but can, among others, also be used to determine information about the density of states.

More about the topic of electron microscopy can be found in [197], [199].

3.2.2 X-ray diffraction

A particularly important technology in crystallography, chemistry, and thin-film analysis is XRD. This technique uses the principle of diffraction of X-ray radiation on the crystal lattice of a material. X-rays are used because the wavelength of this radiation is in the order of the lattice spacing of most crystalline materials (i.e. 0.1 nm to 10 nm). Like X-rays, neutron, electron, and ion beams also interact with atoms, hence diffract from periodic structures. Therefore, they are able to provide information about the lattice. In conventional XRD systems X-ray sources are mainly based on the X-ray emission spectrum of either Cu, Co, or Cr. Depending on measurement requirements, sources with larger or smaller wavelengths are used, also the suppression of fluorescents might be a reason to exclude a specific source material. As a standard, XRD equipment exploits Cu, and especially the Cu $K\alpha$ radiation with $K\alpha1$ = 154.0598 pm and $K\alpha2$ = 154.4426 pm. In contrast, the wavelength of electrons at 200 kV used in TEM is only 2.7 pm.

To describe diffraction phenomena and to understand the corresponding XRD spectra the Braggs-law is introduced [200]

$$n\lambda = 2d\sin(\theta), \tag{3.4}$$

with n being a positive integer, λ being the wavelength of the used X-ray source, d the lattice spacing, and θ the angle of incidence. Figure 3.5 schematically depicts the Bragg-law. If an indenting beam scatters elastically from a lattice atom (actually it scatters from a shell-electron), a secondary spherical wave is emitted from the atom. A superposition of many of these scattering induced secondary spherical waves over many atomic layers only produces a plane wave if the Bragg condition is met [201]. An equivalent condition to describe the diffraction on a crystallographic lattice is the Laue condition, according to Max von Laue [201]. It takes advantage of the reciprocal space to describe the phenomena using
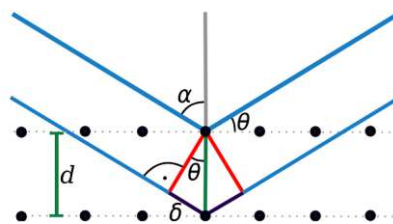
Figure 3.5: Schematic illustration of the Bragg-condition on an atomic lattice level.

$$\Delta \vec{k} = \overrightarrow{k_s} - \overrightarrow{k_i} = \vec{G}, \tag{3.5}$$

with the wave vector $\vec{k} = 1/\lambda$. $\overrightarrow{k_i}$ is the incoming wave vector and $\overrightarrow{k_s}$ the scattered one. $\vec{G}$ is a vector of the reciprocal lattice. The reciprocal lattice vector $\vec{G}$ is related to the lattice constant via $\vec{G} = 1/d$, if $\vec{G}$ is normal to the lattice planes. A good tool for visualizing the Laue condition in the reciprocal space is the Ewald's sphere. It is a sphere with radius $1/\lambda$ with the center being the origin of the real space (the crystal to be measured). From that origin, the wave vector of the incoming beam constructs a sphere. The Laue condition is fulfilled if a triangle can be constructed with two reciprocal lattice points that intercept the sphere and the origin. The construction of the Ewald sphere is depicted in Figure 3.6 for (a) large wavelength radiation (X-rays) and (b) high energy electrons as present in TEM.

Different geometries and detector designs are used for different circumstances. In thin-film analysis, the most frequently used setups are in the Bragg-Brentano (BBG) and the grazing incident angle diffraction (GIXD) configuration, respectively [201].

BBG is so popular because it can be used for powders, poly- and monocrystalline as well as for thin-film analysis. Figure 3.7 shows a simplified schematic illustration of a BBG XRD instrument. The two most important scan modes are the 2θ-scan and the ω-scan. In 2θ-scan mode, the 2θ angle is swept. $\omega = \theta$ is maintained during the scan. This scan mode gives the various intensities of crystal lattices orientated normal to the surface. The ω-scan or rocking curve scan is used to determine the orientational distribution of a certain lattice plane. 2θ is set to the angle of the reflection of interest. Then the sample, (or the detector and the source) are tilted, meaning $\Delta\omega$ is swept. The illustration in the figure does not depict any beam optics like shutters and monochromators to modify the resolution and other properties of the instrument. Depending on the intended application these optics can be adjusted. Important is to apply the same optics when comparing XRD measurements of different samples, as the optic can have
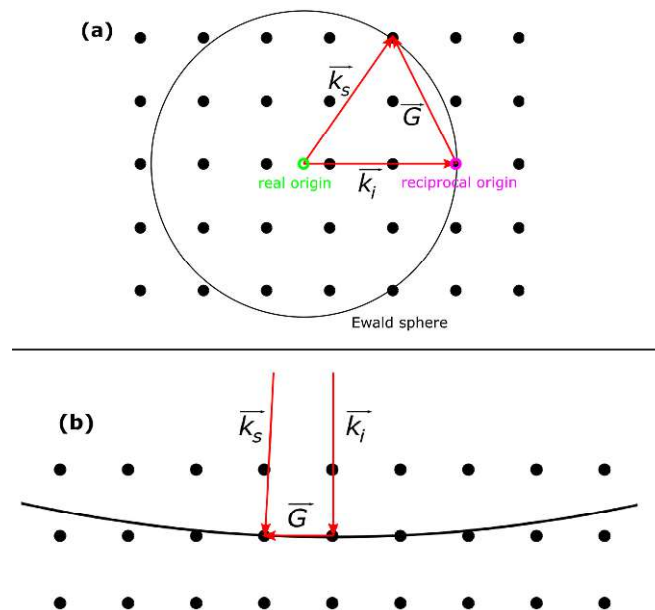
Figure 3.6: Illustration of the Laue condition using the Ewald's sphere for (a) X-rays with rather low wavelength and (b) high energy electrons with a large wavelength.
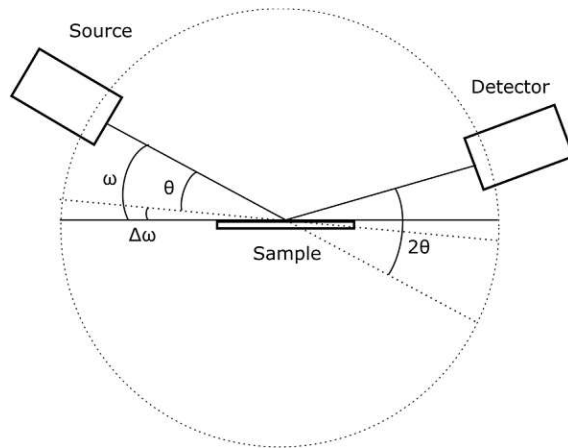
Figure 3.7: Schematic illustration an XRD in Bragg-Brentano geometry.

a major impact on peak broadening and peak intensity. Other angles, that might be adjustable or swept during a scan in some XRD instruments are the azimuthal angle φ, which is equal to a spinning of the sample, and the χ-angle, which represents tilting out of the Goniometer plane.

In the XRD measurements of this thesis, only the BBG configuration is used. GIXD is also a very commonly used technique, especially when observing very thin films, or when the substrate-related peaks are disturbing the peaks of interest.

An often-used approach to estimate the average grain size d_g of polycrystalline samples or powders is the Scherrer equation [202], [203]

$$d_g = \frac{K\lambda}{b\cos(\theta)},$$
(3.6)

where K is the shape factor, λ is the wavelength of the used X-ray source, b is the full width half maximum peak intensity and θ is the Bragg angle, both in radians. $K = 0.9$ was used for all calculations [204], [205]. It must be pointed out that due to both, the different grain shapes, and the intrinsic peak broadening of the XRD equipment, the values for the mean grain size represent only rough estimates. However, an assessment of the trend is possible. For grain sizes larger than a few 100 nm, the instrument-related peak broadening is stronger than the effect of grains and therefore it restricts the use of the Scherrer equation to fine-grained structures.

A very detailed description of XRD techniques, along with theory and examples are given in [201].

3.2.3 Secondary ion mass spectrometry

The secondary ion mass spectroscopy (SIMS) is a frequently used method in material science as well as in semiconductor science. It is a mass spectroscopy method, which gives the elemental composition of a specimen surface. SIMS requires an ultra-high vacuum environment during operation.

In contrast to other elemental spectroscopy techniques often available in semiconductor manufacturing labs like EDX or X-ray fluorescence, SIMS has the advantage of being surface sensitive, while offering sensitivity values down to 60 ppm. The elemental composition is only detected from the first two to three atomic layers of the surface. [206]

A SIMS is usually composed out of two ion guns having an incidence angle of 45° to the sample surface, an electron gun, and a mass analyzer. Depending on the type of mass analyzer used, SIMS is divided in several sub-categories. The two most common arrangements are based on a quadrupole or on a time-of-
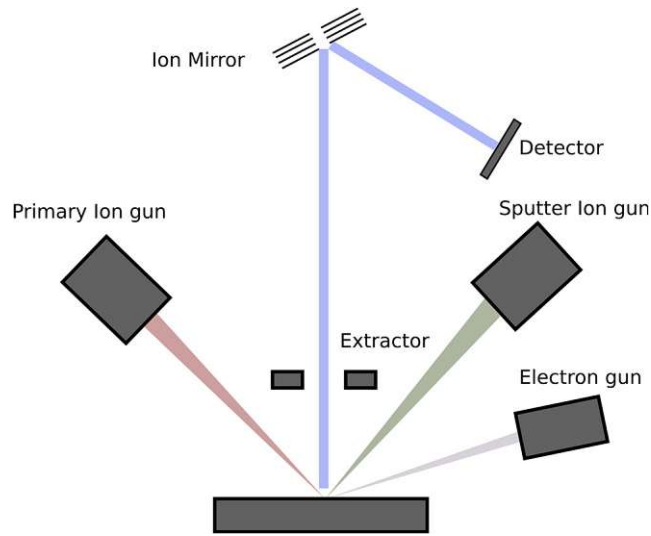
Figure 3.8: Simplified schematic of an ToF-SIMS

flight (ToF) mass analyzer. As the latter instrument is used for the measurements in this thesis, it is described in more detail. A simplified illustration of a ToF-SIMS, without any beam optics, is shown in Figure 3.8.

The first ion gun is used to generate the primary ion beam, which is focused on the sample surface. The ions, which are usually (O_2^+, Cs^+, Ga^+, Ar^+ or Bi^+) or sometimes ionized molecules, generate a collision cascade in the specimen, resulting in the extraction of secondary ions. These secondary ions are directed towards the time-of-flight detector using an extractor. The time-of-flight detector consists of a flight path of length L_f, which is usually equipped with an ion mirror to redirect the ions and to extend the flight path. In addition, this component can also be used to reduce the kinetic energy distribution of the ions and therefore increase the spectrometer resolution [207]. At the end of the flight path an ion detector (microchannel plate) is arranged. The dependence of the ion mass to charge ratio m/z on the velocity, hence the time the ion needs to pass the flight path L_f is given by

$$\frac{m}{z} = \frac{2Vt_f^2}{L_f^2},$$ (3.7)

where V is the extraction voltage (usually 2 to 8 kV), z the quantized charge number, and t_f the time-of-flight [208]. The polarity of the extraction voltage is used to select positive or negative secondary ions for further analysis.

Due to the correlation of the mass/charge ratio on the time of flight, a spectrum can be recorded by recording the detector intensity over time. For continuous measurements, either the primary ion source or the extractor needs to be operated in pulsed mode. The second ion gun often called sputter gun is applied for depth profiling to remove a layer of the sample by sputtering using a high current ion beam (Ar^+, Cs^+, O_2^+,...). An additionally equipped electron gun is needed to reduce surface charging.

The SIMS can be operated in three modes, namely high-resolution mass spectroscopy, ion imaging, and depth profiling. The high-resolution mass spectroscopy is used to obtain the surface mass spectra of a certain spot on the specimen by applying an ultrashort primary ion pulse followed by measuring the flight time of the secondary ions. Images of the elemental composition can be obtained if this procedure is repeated by scanning the measurement location on the sample surface. Using this ion imaging technique lateral resolutions down to 250 nm are possible [208]. The third method is used to obtain

depth profiles of the elemental composition. Using the sputter gun, a layer of the substrate is removed, followed by a measurement cycle using the primary ion gun. The depth profiling is of special interest for semiconductor science as it can be used to measure doping profiles of several hundred up to micrometers depth with extremely high accuracy. By combining ion imaging and depth profiling even 3D elemental profiling is possible.

3.3 Electrical measurement techniques

Apart from the microstructural characterizations, electrical characterization of new materials and material combinations are mandatory for evaluating their performance, especially for microelectronic device applications. Electrical device characterization is defined as the response of a device to an electrical stimulus. Almost every measurement technique is based on the measurement of voltage, charge, or charge movement on the response of either an applied signal, radiation, temperatures, or other factors that can influence the device, such as mechanical deformation. The most frequently used measurement techniques relevant to the devices in this study are IVT measurements and capacitance-voltage-temperature (CVT) measurements.

3.3.1 Contact and sheet resistance measurement

The contact resistance, or for better comparability the specific contact resistivity R_c, is an important quantity, especially for characterizing ohmic contacts. The measurement of the contact resistance of a metal-semiconductor contact often goes along with the measurement of the semiconductor resistance. Depending on the applied technique, either both can be extracted out of the measurement data or one of them needs to be known or one being insignificant.

The simplest setup one may think of is the two-terminal method, with a semiconductor substrate with two round metal contacts of known radius r and distance as shown in Figure 3.9. The total resistance between the two contacts R_t is composed out of the contact resistances R_c, the metal resistances R_m, and the semiconductor resistance R_s like describe and depicted in Section 2.3.6 and Figure 2.18. The total resistance can also be modeled as

$$R_t = 2R_c + 2R_{sp} + 2R_m. \tag{3.8}$$

The semiconductor resistance was replaced by the spreading resistance R_{sp}, which accounts for the resistance of the semiconductor directly under the contact. Due to the spreading nature of the current flow, the majority of the semiconductor resistance is originating from the semiconductor adjacent to the contacts. This holds true if the semiconductor is thick and the area covered by the contacts is small
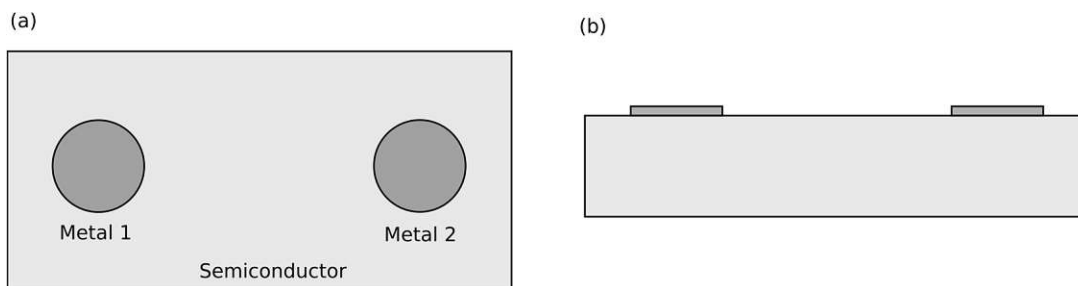
Figure 3.9: (a) Top view of a semiconductor substrate with two circular metal pads. (b) Cross section of same structure.
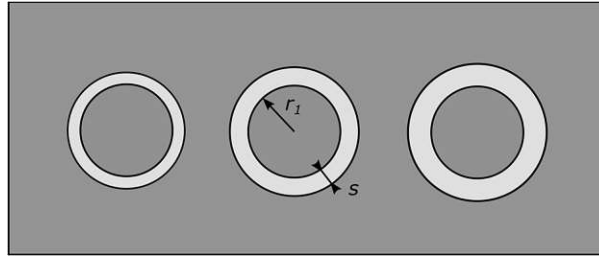
Figure 3.10: Example of CTLM structures. The inner metallization with radius r_1 is kept constant and the gap spacing s changes between the structures. The gray parts are metal, the light gray rings show the underlying semiconductor

compared to the total area. The resistances of the metal pads, the probing contact, and the wiring are included in R_m. In the case of circular metal pads and uniform doping, the spreading resistance can be approximated by [82], [133]

$$R_{sp} = \frac{\rho_s}{2\pi r} \arctan\left(\frac{2t_s}{r}\right), \tag{3.9}$$

with t_s being the thickness of the semiconductor and ρ_s the semiconductor resistivity. If $t_s \geq r$ or if the contacts are located opposite to each other, the current flow underneath a contact can assumed to be vertical. This yields to a contact resistance of

$$R_c = \frac{\rho_c}{r^2 \pi}. \tag{3.10}$$

One now can extract the specific contact resistance ρ_c by a simple measurement of the total resistance assuming the semiconductor resistivity is known, and a contribution of R_m is negligible. Unfortunately, this technique is very inaccurate and requires knowledge of the semiconductor resistivity and requires a certain thickness of the semiconductor. Small errors in the calculated spreading resistance can lead to large errors in the extracted contact resistance [82].

Due to these restrictions, more comprehensive approaches have been evaluated over time which also works for thin semiconducting films. Basically, the knowledge of the semiconductor resistance is always necessary for measurement with only two contacts. Introducing a third or even more contacts allows the evaluation of the contact resistance as well as the semiconductor sheet resistance, hence its resistivity.

CTLM

Of all the known techniques the circular transfer length method (CTLM) [209], [210], [82] or often called circular transmission line method will be described in detail, as it is very simple to implement and does not suffer from current crowding, like in rectangular-shaped electrode configurations.

An example of CTLM structures is depicted in Figure 3.10. A semiconductor bulk or thin-film covered with the metal from which the contact resistance is to be measured is patterned in a way that rings with different gap spacings s free of metallization are realized, exposing the underlying semiconductor. The inner radius r_1 is kept constant. A uniform thickness and doping of the semiconductor are assumed for the following evaluation.

The resistance R between the inner and the outer metallization is measured for every gap spacing. A 4-wire measurement configuration with a current force and a sensing probe should be used for accurate measurement results. For the determination of ultra-low contact resistances values even several current forcing probes can be arranged around the ring [211].

The resistance between the inner and outer metallization can be calculated by the simplified equation [210]

$$R = \frac{R_{sh}}{2\pi}\left[\ln\left(1 + \frac{s}{r_1}\right) + \frac{L_t}{r_1} + \frac{L_t}{r_1 + s}\right] \tag{3.11}$$

under the condition $r_1 > 4L_t$ [212]. A new quantity called transfer length L_t is introduced. In thin semiconductor sheets, the current flow is mainly horizontal towards the metal contact. The current density is the highest on the edges of the opening (exposed ring) and reduces underneath the metallization. The transfer length is defined as the distance from the outer edge of the metal contact towards the point where the potential has dropped to 1/e of its value at the edge.

$$L_t = \sqrt{\frac{\rho_c}{R_{sh}}}. \tag{3.12}$$

Equation (3.11) can be rewritten in the same linear form as used in the conventional transmission line method (TLM)

$$R = \frac{R_{sh}}{2\pi r_1}(s + 2L_t)C_c, \tag{3.13}$$

with C_c being a correction factor

$$C_c = \frac{r_1}{s}\ln\left(1 + \frac{s}{r_1}\right), \tag{3.14}$$

accounting for the circular geometry.

A plot of the measured and corrected resistor values as a function of the gap spacing is depicted in Figure 3.11. The corrected resistance values should show a linear relationship with s. The slope of the linear relation equals $R_{sh}/2\pi r_1$, the y-axis intercept equals $2R_c$ and the x-axis intercept equals $2L_t$ as can be seen
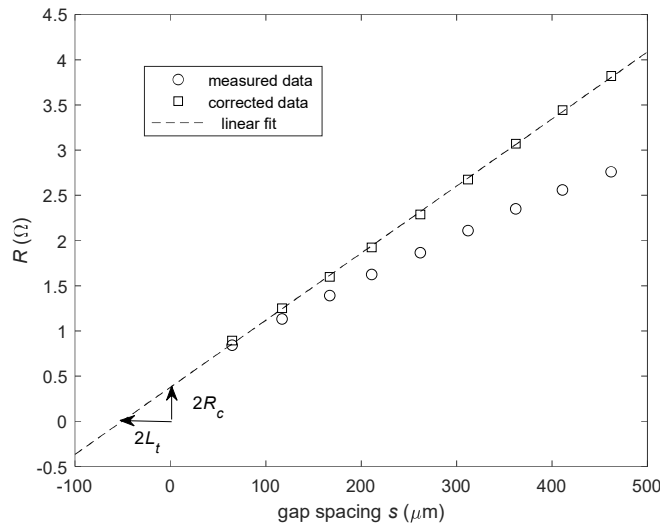
Figure 3.11: CTLM data of a 1500 µm thick poly Si film with Mo contacts. Inner contact radius r_1 = 540 µm and nine different gap spacings ranging from 65 to 465 µm in 50 µm steps are used. Raw resistance and corrected resistance data are shown along with a linear fit using the least squares method giving a coefficient of determination of 0.9995.

in Equation (3.13). The sheet resistance of the semiconductor follows from the extracted slope multiplied by $2\pi r_1$. Multiplication with the film thickness t_s gives the resistivity of the semiconductor ρ_s. Using Equation (3.12) one can calculate the specific contact resistivity $\rho_c = R_{sh} \cdot L_t^2$.

3.3.2 Current-voltage characterization

For the characterization of most semiconductor devices, the IV measurement and analysis techniques are of high importance. Here the focus lies on Schottky and Schottky-like heterojunction diodes, especially on the extraction of the SBH using forward IV and IVT characteristics.

Considering an ideal SC, the current flow follows the TE Equation (2.33). In forward direction, the current shows an exponential dependence on the voltage. Figure 3.12 depicts a measured forward-biased IV characteristic of a Ti/4H-SiC SC in a semilogarithmic plot. When plotting the current logarithmically, a linear region will be visible between $V > 3kT/q$ and up to the characteristic point where the series resistance starts to limit the current. By applying a linear fit to this linear region, the two most important SC parameters, namely the SBH and the ideality factor can easily be obtained by rearranging Equation (2.33) to

$$\phi_B = \frac{kT}{q}\ln\left(\frac{AA^{**}T^2}{I_s}\right) \tag{3.15}$$

$$\eta = \beta\,\frac{dV}{d(\ln(I))}. \tag{3.16}$$

The saturation current I_S or the saturation current density $J_s = I_s/A$ follows from the y-axis intercept and the slope of the linear fit corresponds to $(d(\ln(I))/dV)$. This method fails if the IV curve is strongly distorted by SBH inhomogeneities. In this case, the characterization might be applied at higher temperatures, when the distortions become weaker or a more sophisticated fitting model considering inhomogeneities must be used.
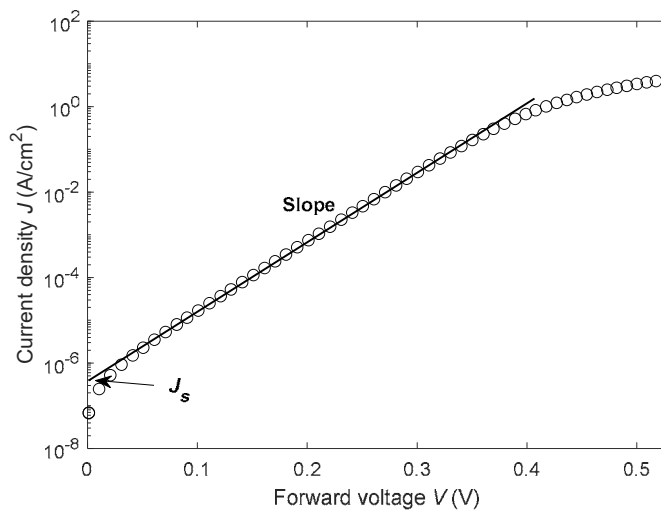
Figure 3.12: Current -Voltage characteristics of a Ti/4H-SiC Schottky diode, together with a linear fit applied to the linear region of the data.

Another frequently used technique to determine the SBH is based on current-voltage-temperature measurements and sometimes referred to as activation energy method. A rearrangement of Equation (2.33) to

$$\ln\left(\frac{I}{T^2}\right) = \ln(AA^*) - \frac{q(\phi_B - V_F/\eta)}{kT} \tag{3.17}$$

gives a linear relationship when plotting $\ln(I/T^2)$ over $1/T$. This plot is called Richardson plot. $q(\phi_B\text{-}V_F/\eta)$ corresponds to the activation energy E_A. The current values for plotting should be taken at $V_F \gg kT/q$. Ideally, the saturation current I_s, obtained from linear interpolation of Equation (2.33), as described before, is used in Equation (3.17) corresponding to $V_F = 0\ V$ [14], [82]. The currents from reverse biased junctions might not be used, as effects like image force lowering and tunneling will introduce errors. The advantage of this method is, that the SBH can now be obtained out from the slope without knowing the active area A of the contact. If the area is known, the Richardson constant A^* can be obtained from the y-axis intercept.

If the series resistance of an SC needs to be extracted as well, Equation (2.33) is first adjusted to include the series resistance by replacing $V = V - IR_s$. Assuming $V > 3kT/q$ and rearranging this equation according to Cheung [213] will result in

$$\frac{dV}{d(\ln(I))} = R_s I + \frac{\eta kT}{q}. \tag{3.18}$$

Another linear relationship is obtained by plotting $dV/(d(\ln(I))$ over I, giving R_s as the slope and the ideality factor η via the y-axis intercept.

This was just a most compact overview of some frequent used evaluation approaches. More details can be found in [82].

3.3.3 Capacitance-voltage characterization

Another frequently used method is the CV technique. An advantage of this method is that it can also provide a depth profile of the doping concentration. The capacitance is usually measured using a high-frequency AC signal, whereby a DC bias is applied and slowly swept. The voltage sweep is conducted in reverse bias but can start at low forward biases. The capacitance of an SC due to the arising depletion region calculates as follows [14]

$$C(V_R) = \frac{A\varepsilon_s}{W_d} = \sqrt{\frac{A^2 q \varepsilon_s N_D}{2(\psi_{bi} + V_R - (kT/q))}}. \tag{3.19}$$

The equation is then rearranged to

$$\frac{1}{C'^2} = \frac{2(\psi_{bi} + V_R - (kT/q))}{q\varepsilon_s N_D}. \tag{3.20}$$

The capacitance C was now replaced by the capacitance per unit area C'. Plotting $1/C'^2$ over V_R is called a Mott-Schottky plot and should give a linear response, as long as the doping concentration is homogenous in depth. Figure 3.13 shows a CV measurement and the Mott-Schottky plot together with a linear fit. The x-axis intercept of a linear fit gives the built-in voltage ψ_{bi} in the form of $(-\psi_{bi}+kT/q)$. This is needed to calculate the SBH via [82]
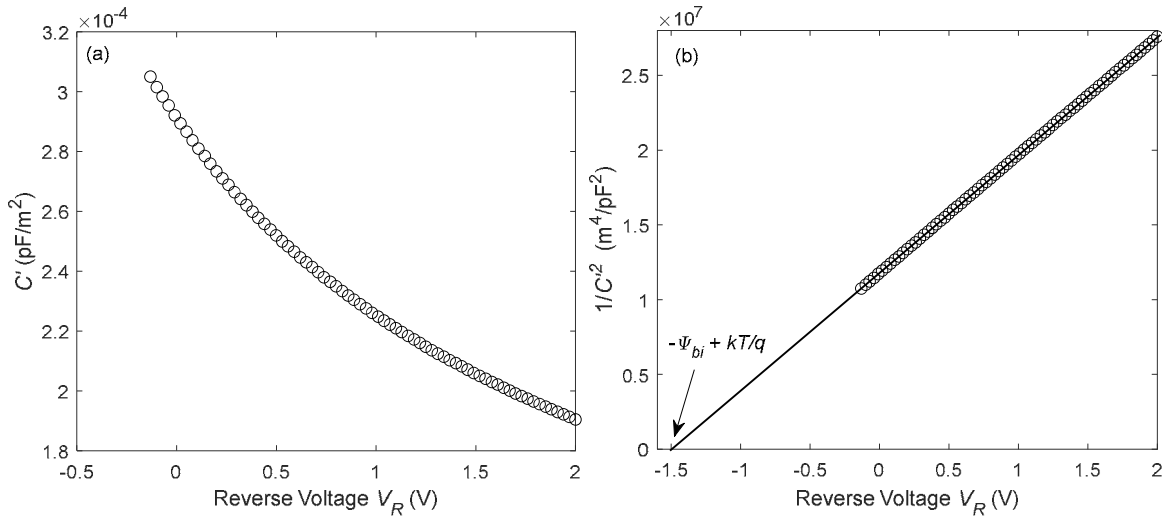
Figure 3.13: (a) Capacitance-Voltage characteristics of a p-Si/4H-SiC heterojunction diode. (b) Plot of the measured capacitance per unit area over voltage along with a linear fit.

$$\phi_{B,CV} = \psi_{bi} + \phi_n - \Delta\phi. \tag{3.21}$$

The Fermi potential ϕ_n can be calculated analytically. $\Delta\phi$ is the image force lowering, which becomes small for low doping concentrations and might be neglected [14]. Using the slope of the fit, one can also estimate the doping concentration of the semiconductor underneath the metal contact by

$$N_D = \frac{2}{q\varepsilon_s}\left[-\frac{1}{d(1/C'^2)/dV}\right]. \tag{3.22}$$

The SBHs obtained by the CV method often strongly deviate from those measured with IV techniques. This is mainly due to inhomogeneities in the SBH as well as interface charges. The IV method usually gives lower SBH values, as the current predominately flows through the lowest barriers. The IV SBH value is a more practical value as it is the SBH the device will have in its actual operation. When applying the CV method no static currents are flowing, and the obtained SBH is more an average of the total SBH, assuming a Gaussian distribution of SBHs [55], [214].

4 Growth and characterization of Si on 4H-SiC

In this chapter, the results of the microstructural analysis of different Si deposition techniques on 4H-SiC substrates are presented and discussed. First, sputter-deposition of Si is investigated. Because sputter-deposition only leads to amorphous layers, the influence of different post-deposition annealing steps, as well as the influence of a high boron concentration, as needed for diode contacts, are investigated. For the same reason, sputter experiments using *in-situ* heating were conducted, but due to equipment-related restrictions limiting the maximum substrate temperatures to about 400 °C, no films with indications of a crystalline phase could be deposited. To assure a low temperature budget for crystallization of the amorphous Si films, metallic thin films are introduced as crystallization agents. This topic is discussed in the next chapter. Next, the growth of Si on 4H-SiC was investigated using LPCVD at different pressures, gas flow rates, and temperatures. The microstructure of the deposited films was investigated using SEM, TEM, and XRD to determine the crystallinity, the grain size, and the crystallographic film orientation with respect to the substrate properties. Also, atomic force microscopy (AFM) was used to determine the surface roughness of these films. Finally, the doping of the Si films applying either spin-on dopants and subsequent diffusion, or using doped targets is measured using different techniques and the results are discussed.

If not mentioned otherwise, all measurements were conducted using the following equipment with the mentioned parameters and configuration. XRD measurements are performed with an X'Pert MPD Pro diffractometer from Malvern PANalytical exploiting the Cu-K$_\alpha$ radiation line in Bragg-Brentano configuration. The incident and diffraction beam paths are equipped with 0.04 rad Soller slits. The incident beam path is further equipped with a 10 mm incident beam mask, a 2° anti-scatter slit, and a 0.5° divergence slit. The distance to the sample is 100 mm. The diffraction beam path has an anti-scatter slit with 5.5 mm width and an X'Celerator line detector. For TEM investigations a FEI TECNAI F20 transmission electron microscope operated at an acceleration voltage of 200 kV was used. The TEM samples were prepared as conventional cross-sections, ground, polished, and thinned by a Gatan Pips II. SEM investigations were done with a Hitachi SU8030 SEM at an acceleration voltage in the range of 2 to 5 kV.

4.1   Introduction

Growth of silicon on SiC has been reported using both, chemical vapor deposition [38], [215]–[219] and physical vapor deposition techniques [41], [94], [220], [221]. Another method to achieve Si/SiC heterostructures is surface activated bonding (SAB) [43], [46], [47], [52], [222], [223], although it is not a growth method it will be mentioned here as it has been conducted quite often. MIC is barely reported to form crystalline Si on SiC [161].

Si thin films prepared by SAB are of perfect monocrystallinity, however, they require a lot of raw material and complex separation processes for thin epitaxial layers. The growth of Si on SiC by vapor phase deposition techniques is more challenging, as its growth characteristic is strongly influenced by the lattice mismatch between the two materials. If the deposition temperature is below 600 °C, Si will mainly grow in its amorphous phase, requiring post-deposition annealing to form a polycrystalline microstructure [224], [225]. Due to the different crystallographic systems of Si and xH-SiC (x stands for all hexagonal SiC polytypes), as well as due to the different lattice constants of 5.43 Å for Si and 3.08 Å for xH-SiC along the a-axis [226], the lattice mismatch is huge. For illustration purposes, a schematic is presented in Figure 4.1 visualizing the interfacial crystallographic configuration of the Si/xH-SiC heterostructure in the two most common growth orientations (normal to the surface) of Si,
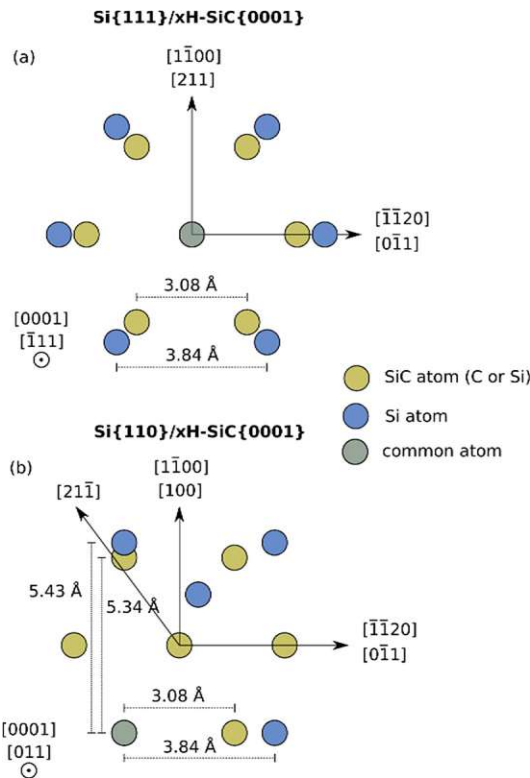
Figure 4.1: Schematic illustration of the cleaved Si/SiC surface of (a) the Si{111}/xH-SiC{0001} heterostructure and (b) the Si{110}/xH-SiC{0001} heterostructure. Three index miller orientations are denoted to the Si crystal, four index notations to the SiC. [242]

namely Si<111> and Si<110>. The xH-SiC surface is the Si-face which corresponds to the {0001} plane. Despite the large lattice mismatch, epitaxial growth of the Si{111}/xH-SiC{0001} heterostructure was achieved, which can be attributed to the rather low domain mismatch of only 0.26% between the atoms along the Si<110> and xH-SiC<11-20> orientations if the domain size equals 4:5 atoms [218]. The Si{110}/xH-SiC{0001} heterostructure has a cubic and a hexagonal surface structure, hence more than one misfit orientation. The atomic misfit along the Si<110>/xH-SiC<11-20> direction has again a 4:5 domain mismatch of only 0.26% and along the Si<100>/xH-SiC<1-100> direction the misfit is 1.68% with a 1:2 domain ratio [227].

4.2 Sputter-deposited Si on 4H-SiC

Parts of this section have been published in [220].

In this section the quality of sputter-deposited Si thin films is investigated along with the influence of different PDA treatments on the film quality. Extensive XRD and TEM studies will investigate the microstructure of the Si films and especially the interface quality on 4H-SiC substrates. Additionally, results regarding the influence of the film thickness and the deposition temperature are presented. For reasons of comparison a sample with an LPCVD Si film was also included in the evaluation.

4.2.1 Experimental details and pre-investigations

As substrates, 4H-SiC wafers from SiCrystal are used. The wafers are cut 4° off-axis and are nitrogen-doped with a bulk resistivity of 0.015 to 0.028 Ωcm. Prior to deposition, the substrates were ultrasonically cleaned in acetone followed by a hydrofluoric acid etch and an RCA cleaning process (as
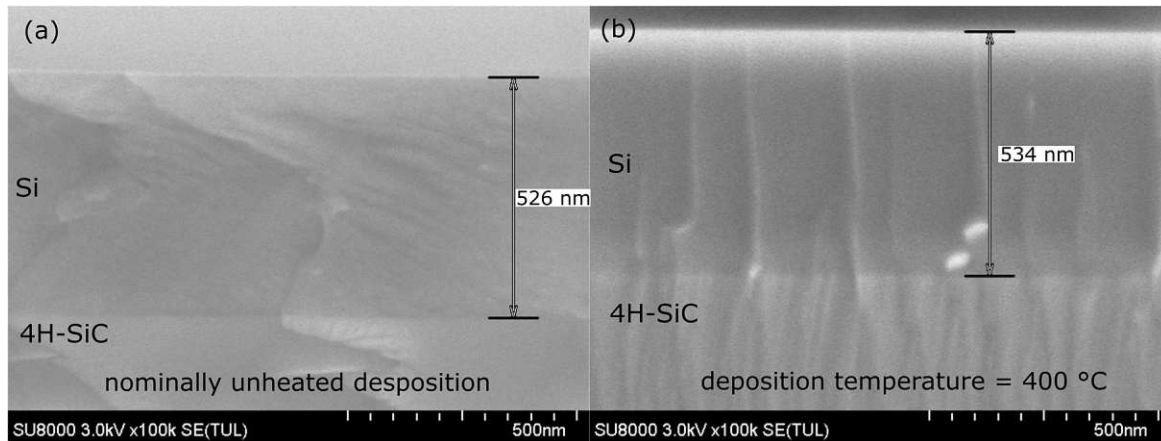
Figure 4.2: Cross-sectional SEM images of test depositions to determine the deposition rate and to observe any influence of the sample heating on the deposition rate.

described in Section 3.1.1). If not mentioned otherwise, all depositions were performed on the Si-face of the 4H-SiC wafer.

The first experiments towards sputter-deposited Si films on 4H-SiC involve the determination of the deposition rate. Different silicon targets, all 6 inches in diameter, were used in the course of this thesis. For the microstructural investigations, a nominally undoped target with unknown background doping concentration but a known purity of 99.999% was used. All sputter experiments were performed on a Von Ardenne LS730S DC magnetron sputtering system using DC sputtering. For the deposition of the Si films the same parameters, well-established for metallic thin films were applied. This includes a sputtering power of $P = 500$ W, a chamber pressure of $p = 0.3$ Pa, and a gas flow of 60 sccm argon (Ar). The sample holder was either not actively heated, and is therefore only affected by plasma-induced self-heating, or actively heated from the bottom with 100% heater power, which equals to about 400 °C. Using these parameters different test samples were prepared and sputter-deposited for 7 min (420 s). Figure 4.2 shows SEM images of a sample deposited under unheated conditions and at about 400 °C sample temperature. No significant difference in the film thickness, nor in the microstructure could be observed, within the resolution capability of the SEM. The film thickness is also known to vary by about
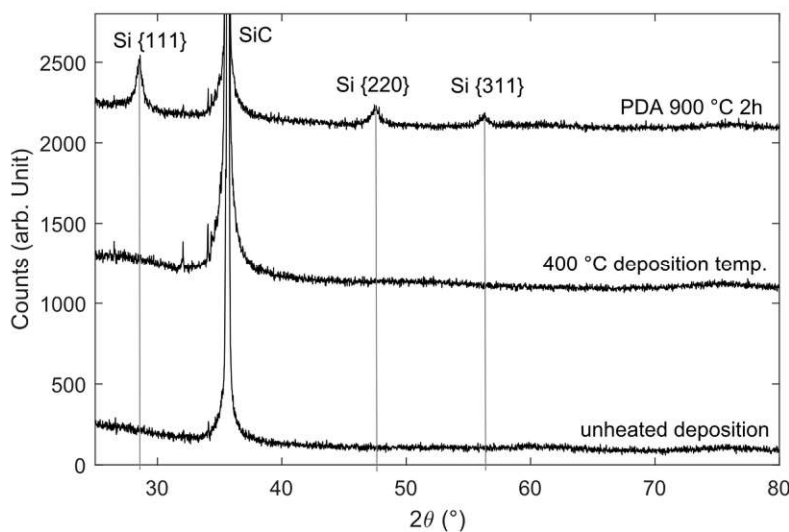
Figure 4.3: XRD diagrams of sputter-deposited a-Si, without heating and at 400 °C deposition temperature. For comparison a sample exposed to a PDA at 900 °C shows Si diffraction peaks.

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Table 4.1: Sample list of sputter-deposited samples with different post-deposition annealing parameters

Sample Name	Thickness t (nm)	PDA Temperature (°C)	PDA Time (h)	PDA Heating Rate (°C/min.)
A1	100	1000	2	5
A2	500	1000	2	5
A3	1500	1000	2	5
A4	500	800	20	5
A5	500	900	20	5
A6	500	1100	20	5
A7	500	1000	0.017	5
A8	500	1000	20	5
A9	500	1000	2	2
A10	500	1000	2	10
A11	500	1000	2	600
A12	500	-	-	-

20% between the center and the edge of the round sample holder, representing a distance of only 2 inches (5.1 mm) [228], [229]. Almost all experiments were conducted on small wafer pieces (1-2 cm^2 area) and not on full wafer scale. Therefore, care was taken to place the samples only within a radius of about 2-3 cm around the center of the holder. However, some variation in film thickness is still expected. With the above-mentioned parameters the deposition rate of Si was measured to about 1.25 nm/s. To verify the absence of any crystalline phases in the *as-deposited* samples at unheated conditions and 400 °C, XRD measurements have been performed as depicted in Figure 4.3. No signs of Si related peaks are detectable in any of the samples. A polycrystalline sample is included in Figure 4.3 as well for reasons of comparison. It can be concluded that no crystalline Si can be deposited with the introduced sputtering equipment and PDA is required.

All PDA processes were performed in a quartz furnace in a high purity Ar atmosphere, which was evacuated before Ar inlet and heating. The standard PDA parameters are 1000 °C for 2 h at a heating rate of 5 °C/min., while the cooling down phase was not controlled. The reference sample with the LPCVD Si was deposited using SiH$_4$, a chamber pressure p = 16 Pa, and a temperature of T = 620 °C. The LPCVD deposition rate was measured to be about 5 nm/min.

The samples of the following experimental series are divided into two groups. Samples of group A are sputter-deposited on the Si-face of the 4H-SiC substrate at nominally unheated conditions. Afterward, the samples are annealed under the conditions listed in Table 4.1. All samples have a Si layer thickness of approximately 500 nm except for samples A1 and A3, to investigate the influence of the thickness. The annealing took place at temperatures ranging from 800 to 1100 °C, at annealing times between

Table 4.2: List of samples with special properties. Samples B1 to B4 are sputter-deposited, whereas B5 was deposited with LPCVD and was not annealed after deposition.

Sample Name	Thickness t (nm)	Specific Treatments and Properties
B1	500	B doped via diffusion
B2	500	PDA annealing + B doped via diffusion
B3	500	SiC C-face
B4	500	deposition temperature T_{dep} = 400 °C
B5	500	LPCVD Si 500 nm; no PDA

1 min and 20 h as well as with heating rates from 2 up to 600 °C/min. Additionally, an unannealed sample, labeled as A12, with 500 nm Si thickness is added for comparison. In contrast, all samples of group B were treated differently compared to those of group A. In detail, the samples B1 and B2 were sputter-deposited with 500 nm a-Si like the other samples but followed by a boron doping using the spin-on dopant solution B155 from Filmtronics with a boron concentration of 4%. The drive-in took place in air at 1000 °C for 5 h. B1 was doped in the *as-deposited* state, while B2 was annealed using the standard parameters prior to the diffusion process. On sample B3 the Si film was deposited on the C-face and underwent the standard PDA procedure. Sample B4 was heated to $T_{dep} = 400$ °C during sputtering and again was annealed using the standard PDA parameters. The Si layer of sample B5 was grown using LPCVD. A summary of the group B samples is provided in Table 4.2.

A Bruker Dimension Edge atomic force microscope was applied to determine the sample topography and the surface roughness. Scan areas of $5 \cdot 5$ µm^2 were measured and the arithmetic average roughness R_a and the root mean squared roughness R_q were calculated.

4.2.2   Results of XRD investigations

In order to obtain information about the crystallinity and texture, XRD measurements were performed. To investigate the crystallographic influence from the underlying 4° off-axis 4H-SiC substrate the orientation of the sample with respect to the source/detector plane must be known. Therefore, a first XRD measurement was necessary to align the crystallographic orientation of the sample with the measurement equipment. Therefore, the Bragg-Brentano symmetrical goniometer setup was tilted by an angle of $\omega = 4°$. The Bragg angle was set to the strongest reflection at $2\theta = 35.5°$ corresponding to the 4H-SiC{0004} reflection. When fixing the latter angle, a scan of the specimen rotation axis (φ-scan) gives only one reflection when the {-1-120} plane is parallel to the source/detector plane. The determined sample orientation φ is then the reference for all further measurements. For each sample, a Bragg-Brentano 2θ-scan is performed from 25° to 72° to cover all major Si reflections [230]. To get further information about the orientation of the grains, rocking curves (ω-scans) are performed for the two major Si peaks at $2\theta = 28.4°$ and 47.3°. Figure 4.4a shows the XRD diagram of the unannealed sample A12 and the annealed sample A2. The unannealed sample shows no distinctive peaks, as the *as-deposited* Si is amorphous. At the sample A2, four Si peaks, corresponding to Si{111}, Si{220}, Si{311} and Si{400} are clearly visible. Due to the 4° off-axis orientation of the specimen the substrate-
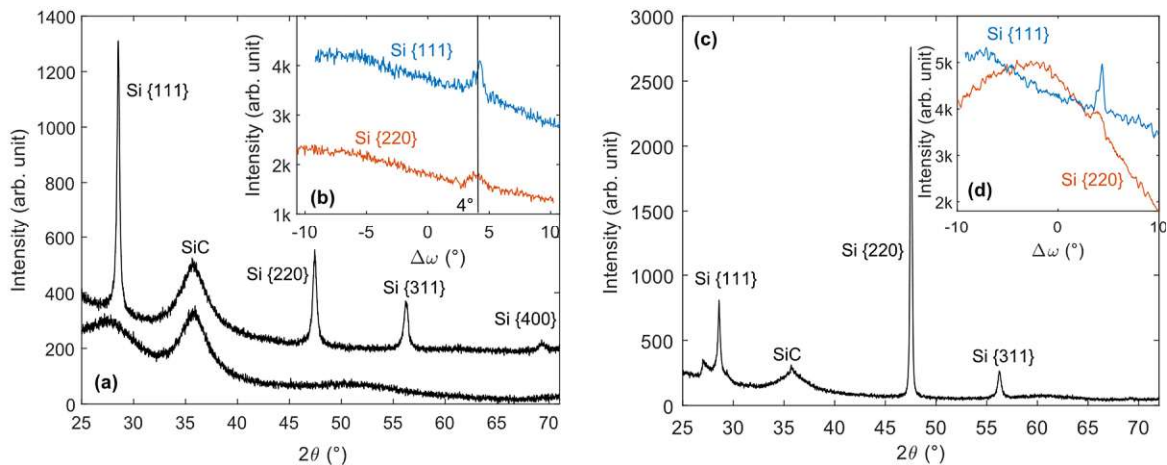

Figure 4.4: (a) XRD diagram (2θ-scan) of sample A12 (lower curve) and A2 (upper curve). (b) Rocking curves (ω-scan) of the Si{111} and Si{220} peaks of sample A2. (c) XRD diagram of the LPCVD sample with the rocking curves of the Si{111} and Si{220} peaks in the inset (d).

related SiC{0004} peak is only less pronounced. Figure 4.4b shows the measured rocking curves of the Si{111} and the Si{220} reflections. Both scans show a rather high intensity in the whole ω range, as well as a slight slope most probably due to the reduction of exposed sample area. The overall high intensity, however, indicates a uniform distribution of grain orientations. All sputtered and post annealed samples show this flat omega dependency, indicating no distinct grain orientation. At about $\omega = 4°$, a slight bulge in the intensity is visible. This bulge in the rocking curve characteristics was found to be independent of the deposited thin film and the 2θ angle. It can thus be attributed to an artifact due to the extremely high crystallinity of the substrate resulting in an increase of background noise when the substrate is oriented parallel to the scanning plane. Figure 4.4c shows the XRD diagram of LPCVD sample B5 together with the rocking curves of the Si{111} and Si{220} diffraction angle in the inset (d). The Si{220} rocking curve of the LPCVD sample was found to be the only crystallographic plane showing some degree of orientation in the form of a very broad peak. This finding is consistent with TEM analysis showing crystals orientated normal to the 4H-SiC surface but with up to +/- 10° tilting, as can be seen in the next section.

Figure 4.5 shows further results extracted out of the 2θ-XRD diagram of the three most dominating Si peaks. In Figure 4.5a the average grain size d_g is plotted for each sample. The grain size was evaluated using the Scherrer Equation (3.6). It must be pointed out that due to both the different grain shapes and the intrinsic peak broadening of the XRD equipment, the values for the mean grain size represent only rough estimations. However, an assessment of the trend is possible. In all samples, the <111>-oriented grains are the largest with a mean size between 16 and 46 nm. Only the LPCVD sample deviates from this trend with the <220> oriented grains being the largest with almost 60 nm mean size. The latter parameter decreases with increasing Si layer thickness. The 100 nm thin sample has an about 50% larger grain size than the 1500 nm thick sample. Strain-energy induced crystallization is suspected to happen at the a-Si/SiC interface due to the different coefficients of thermal expansion as reported for the a-Si on SiO$_2$ system [231]. The additional energy increases the growth rate close to the interface and thus the overall mean grain size in thin films with a large interface to bulk ratio. The increasing grain size with higher annealing temperatures as well as longer annealing times is expected [232], [233]. In addition, an influence of the ramp rate during annealing is observed. The fast-annealed sample with 10 °C/s shows the smallest grains, whereas those annealed with 10 °C/min. and slower show within the measurement accuracy the same average grain size. This result is attributed to the strongly temperature depended nucleation rate within a-Si films. The fast heating to high temperatures causes the nucleation of many grains, whereas the slow rate will only allow a few nuclei to form, which than grow fast enough to prevent the formation of others [232]. The samples B1 and B2, which were boron-doped prior and after annealing, show a slightly larger mean grain size than sample A2, which can be directly compared in terms of annealing time, as other annealing parameters are kept constant. The increased grain size of the highly boron-doped samples is not surprising, because an increased impurity concentration significantly increases the growth rate of grains but not the nucleation rate, resulting in an overall larger grain size [234]–[237]. Also, no difference is found between the C-face and the Si-face SiC, as well as any impact arising from the substrate heating during Si deposition.
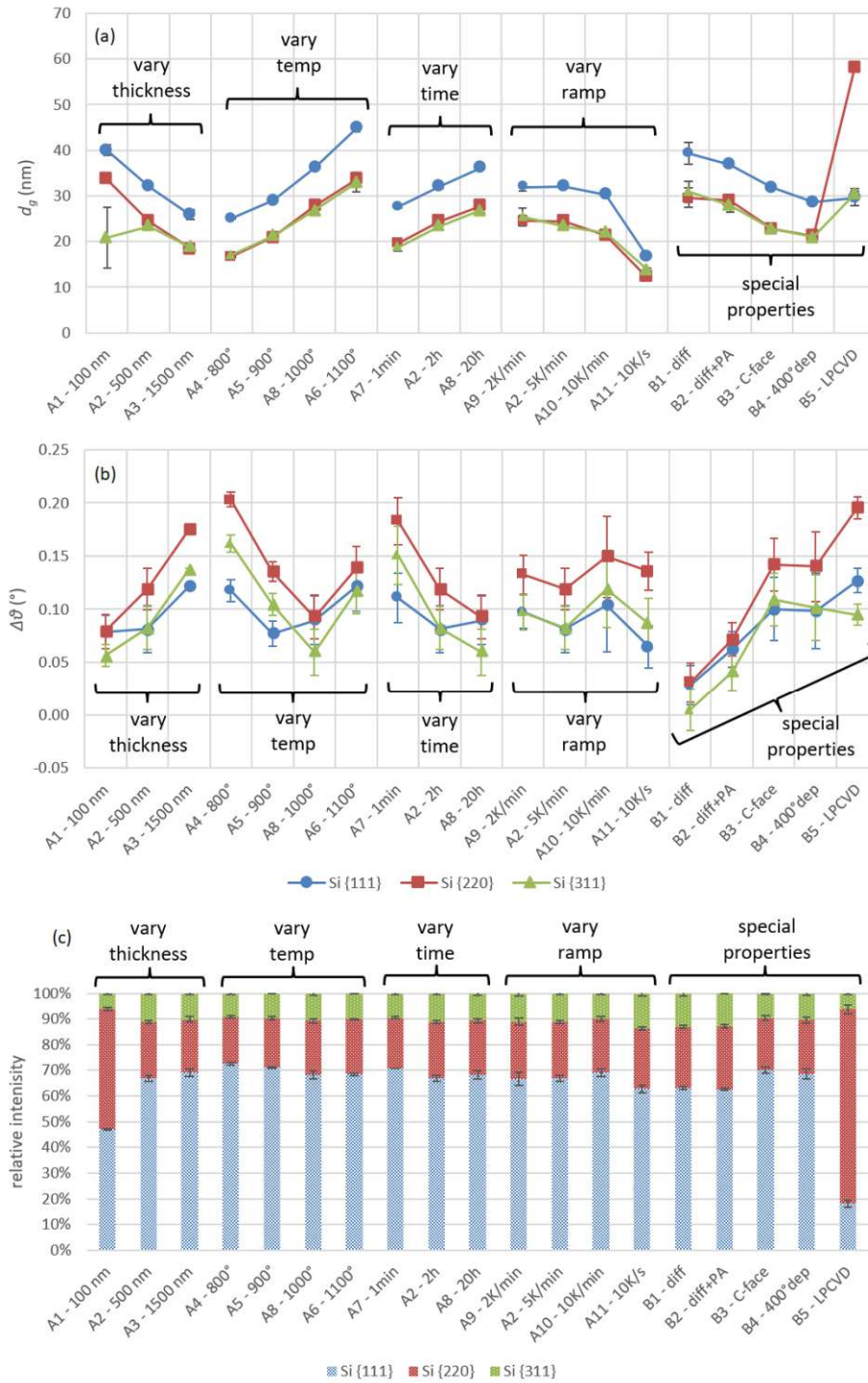
Figure 4.5: Results of the XRD data evaluations. All measurements are repeated three times and the average value is plotted. Error bars represent the standard deviation. (a) Average grain sizes of different samples calculated using the Scherrer equation. (b) Relative peak shift compared to a reference standard Si powder. (c) Relative distribution of the peak intensities of the three most pronounced peaks related to Si{111}, Si{220}, and Si{311}.

In Figure 4.5b the peak shift $\Delta\theta$ to the diffraction angles reported in the NIST Standard Reference Material 640e for silicon powder is depicted. All samples show positive values of $\Delta\theta$ for all three orientations. Positive $\Delta\theta$ values translate to smaller lattice spacings compared to the stress-free silicon reference and indicate the presence of compressive stress inside the grains. For the samples with varied

thickness and annealing time a correlation between grain size and peak shift is notable, so that larger grains correspond to a lower stress inside the grain and hence, in the film. In addition, the samples with different annealing temperatures show the same trend, except that annealed at 1100 °C, which has a larger $\Delta\theta$. The LPCVD sample B5 has the largest XRD peak deviation $\Delta\theta$, but it must be noted that it is characterized in the *as-deposited* state and no annealing process was performed for potential stress reduction [238]. The sample B1, which was heavily boron-doped by diffusion, shows almost the expected 2θ angles for stress-free silicon. The peak shift $\Delta\theta$ shows an overall higher standard deviation. This can be attributed to the sensitivity of the peak position on the sample surface position. When mounting the sample on the holder a small error in leveling the sample zero plane is expected.

Figure 4.5c shows the relative peak intensities of the three diffraction signals. The intensity distribution of all samples, except A1 and B5, is typical for randomly orientated polycrystalline silicon [239], whereas samples A1 and B5 show a more pronounced Si{220} peak indicating a dominance of grains oriented in that direction. A more dominant growth of {220} in LPCVD Si on Si-face SiC has been reported before [215]. The stronger dominance of the Si{220} peak in the 100 nm thick layer of sample A1 is interesting because it deviates from the peak intensity distribution expected for randomly oriented grains. Again, strain-energy induced crystallization is assumed to be responsible for the observed thickness dependency. The highest stress is close to the interface, as the stress gets reduced inside the bulk by rearrangement of the amorphous silicon. A dominant growth of <111> oriented Si along the stress direction is predominantly because of the high Young`s modulus associated with this crystallographic direction [231]. If two of the four <111> directions grow parallel to the surface the <110> direction is normal to the surface. Therefore, a dominating Si{220} peak in the thinnest sample is observed, whereas the random orientation of the bulk crystallization compensates this effect in the thicker samples. The crystallization on the C-face 4H-SiC and the deposition at 400 °C did not show any deviation from the sample A2 which was annealed using the same PDA parameters and having the same layer thickness. Therefore, a deposition at elevated temperature dose not bring any advantage as it is still amorphous and no improvement of the crystallinity was observed after PDA compared to unheated deposition.

4.2.3 Results of TEM and AFM investigations

From this sample series, five specimens were selected and prepared for TEM investigation. Figure 4.6 shows TEM cross-sections of the Si layer of the samples A1, A6, B1, B5, and A12. These samples were chosen because they showed promising results in the XRD measurements, such as high grain size or a dominant Si<220> orientation. Additionally, the *as-deposited* amorphous sample A12 was chosen to document the film quality prior to annealing. The polycrystalline microstructure of the Si films is clearly visible in the images. On the sample surface of A1 and A6, an oxide layer of approximately 33 nm is visible, as shown in Figure 4.6a and b. Surface oxidation did happen during PDA due to the residual oxygen in the furnace. The sample B1 does not have the oxide layer, as it was etched in HF to remove the spin-on dopant layer. What directly strikes, is the difference in surface roughness across the different samples. The samples, which have been crystallized from their amorphous phase, show a rather smooth surface, whereas the highly boron-doped sample has a slightly rougher surface. This can be attributed to the larger grain size and to the removal of the drive-in diffusant oxide. The LPCVD deposited Si layer
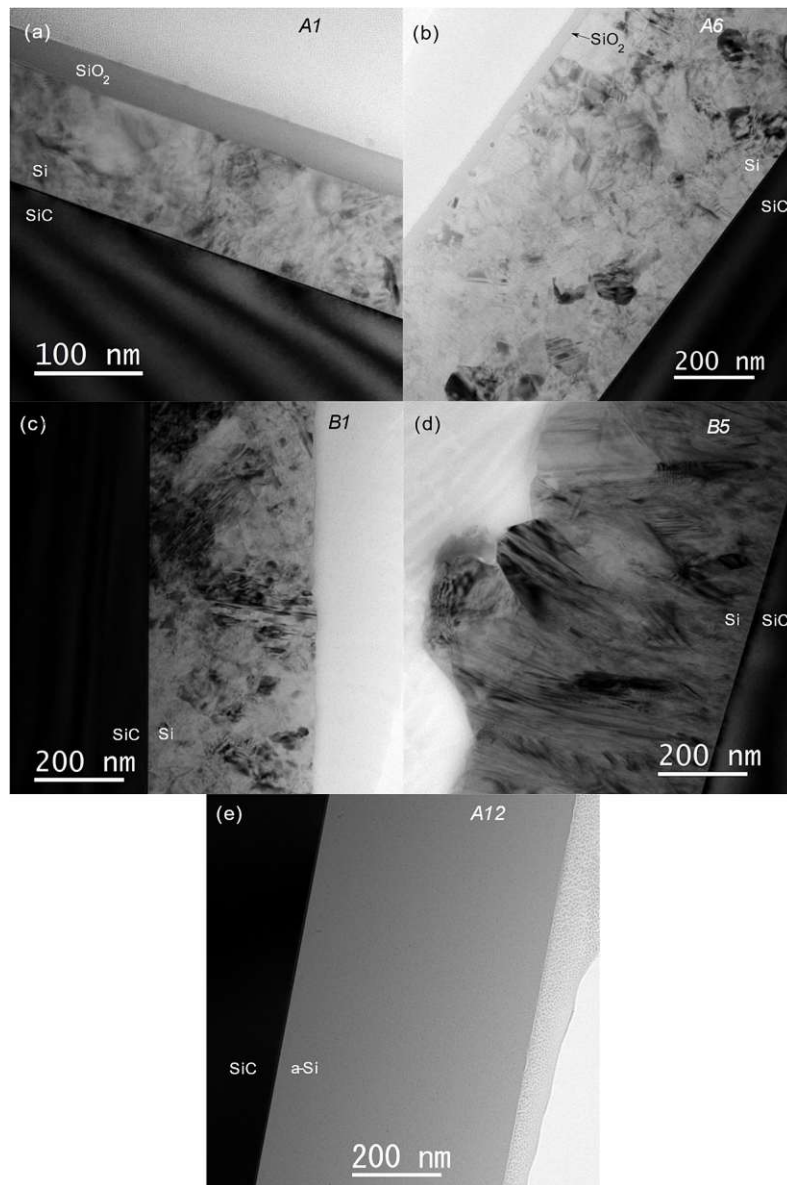
Figure 4.6: Cross-sectional TEM analyses of samples (a) A1, (b) A6, (c) B1 and (d) B5. (e) As-deposited sample A12, showing the amorphous silicon prior to annealing. The black areas in the images belong to the 4H-SiC substrate.

of sample B5 shows the roughest surface. Variations in film thickness are up to 50% of the mean film thickness. This finding is typical for *as-deposited* crystalline silicon, as some grains dominate during the growth process and overgrow those with a slower-growing direction. In addition, a clear tendency of orientational growth normal to the interface is indicated by shadowing effects. However, high-resolution transmission electron microscopy (HRTEM) and the XRD rocking curves did not give any indication of hetero-epitaxial growth. The LPCVD deposition temperature of 620 °C was too low to overcome the interface formation energy for this growth regime. As will be discussed in Section 4.3, a deposition temperature of 900 °C is needed for epitaxial growth. The *as-deposited* sample A12, depicted in Figure 4.6e, shows a smooth amorphous layer without any signs of crystallinity. As expected for amorphous layers, the surface appears very smooth.
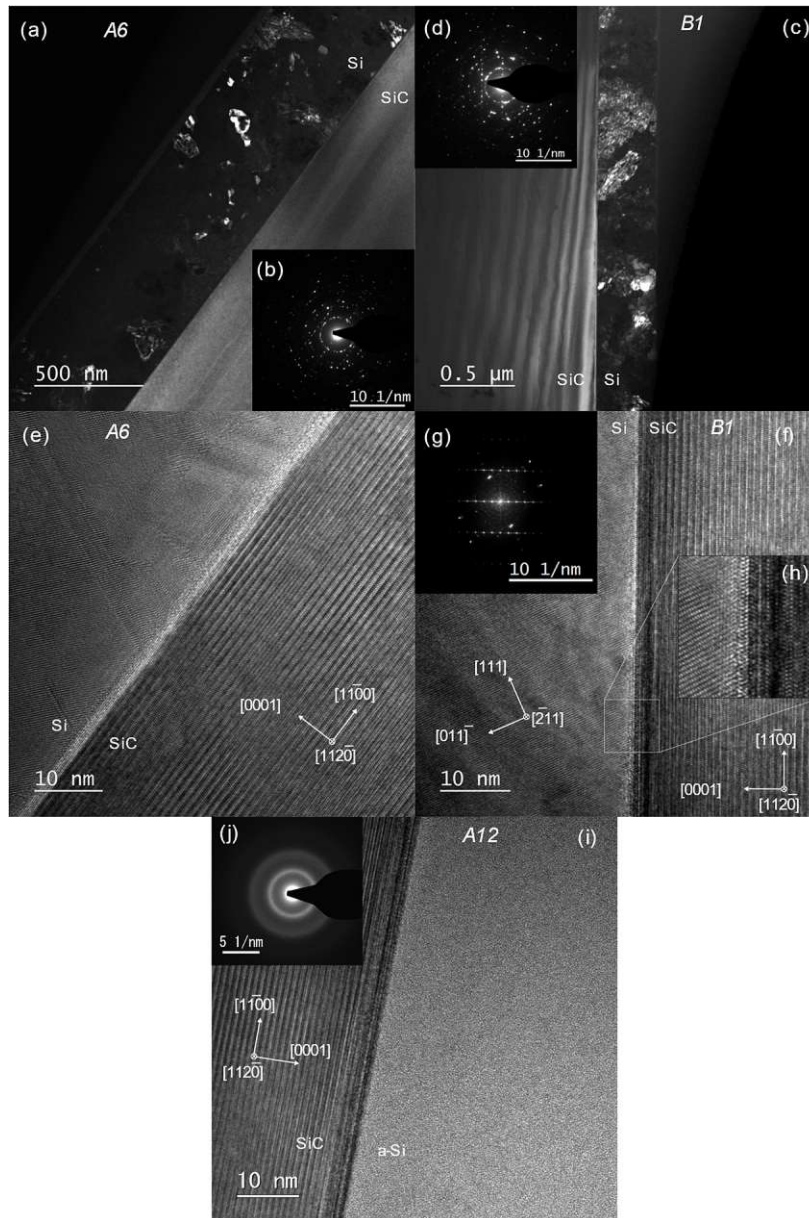
Figure 4.7: TEM investigations of the samples A6 (a and e with inserts), B1 (c and f with insets), and A12 (i with inset). (a) and (c) show dark-field images of these samples. Insets (b) and (d) show the SAD patterns from an area of about 800 nm in diameter centered in the middle of the Si film. Inset (j) shows the SAD of sample A12 from an area of about 300 nm in diameter. Figures (e), (f) and (i) are high-resolution TEM images of the interface region. (g) is an FFT diffraction pattern of the displayed image and (h) shows a magnified region of the interface.

Figure 4.7 shows detailed TEM investigations of the sample A6, which was annealed at 1100 °C, the highly boron-doped sample B1, and the *as-deposited* sample A12. The upper two images (a) and (c) are dark field images of these two samples. This imaging mode is preferred to display the polycrystalline microstructure and to estimate the grain size. In sample A6, different grain size values ranging from a few nm up to 150 nm are observable in the selected section. This is in good agreement with the mean grain size determined by XRD measurements. Sample B1 shows significantly larger grains, with dimensions up to 500 nm. Here the deviations from the corresponding values from XRD is larger. The insets (b) and (d) in Figure 4.7 show the SAD patterns. Both show a rather uniform distribution of

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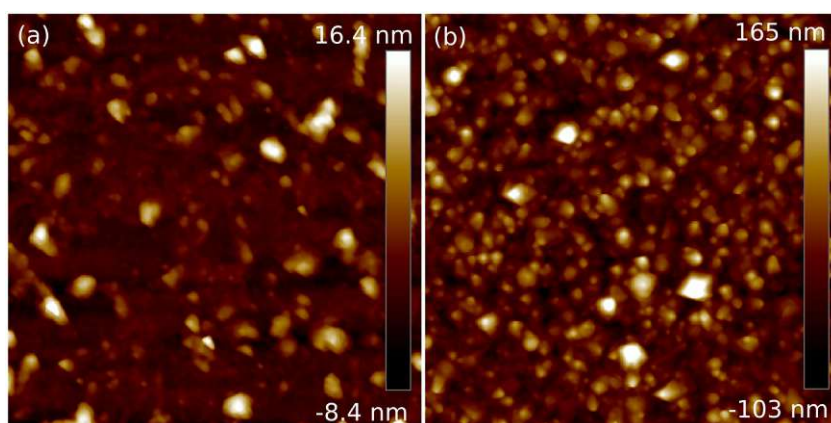
Figure 4.8: Typical AFM images of the surface topography of (a) sample A1 and (b) B5. The scan area is 5 · 5 µm^2.

diffraction points, thus matching the XRD results and confirming a polycrystalline silicon layer with no preferred orientation. To investigate the influence of the 4H-SiC substrate on the Si crystallization HRTEM images of the interface region were taken. Images of the samples A6, B1, and A12 are depicted in Figure 4.7e, f, and j, respectively. The TEM preparation is made in such a way that the 4H-SiC{11-20} plane is parallel to the cross-section. Therefore, the zone axis could be aligned easily with the [11-20] direction and the pattern of the 4H-stacking sequence is visible. Arrows indicate the orientation of the substrate. Figure 4.7f additionally shows the orientation of a large Si grain. The high-resolution image of sample A6 shows that there is no epitaxial transition to the substrate. Different grains with different orientations, stacking faults as well as twins are visible. The interface itself appears sharp with no amorphous regions or any alloying so that any chemical reactions can be excluded. In the HRTEM image of the boron-doped sample B1, the interface between 4H-SiC and a single Si grain is visible. Due to grain sizes of several 100 nm, a large portion of the interface region appears monocrystalline in the high-resolution images. Figure 4.7g shows a FFT pattern calculated out of the entire image area and Figure 4.7h shows a magnified region of the interface. The crystal orientation of the Si grain was determined with the help of CrysTBox [240], [241]. The FFT pattern clearly indicates the diffraction spots of the different lattices. The three parallel lines of closely separated spots represent the 4H-SiC and the other spots are from the Si grain. The Si pattern is representative of the orientation according to the arrows in Figure 4.7f. Although a very sharp interface with no stacking faults is present, no orientational correlation between the two crystalline constituents is observed and hence, the interface cannot be labeled as hetero-epitaxial. HRTEM images taken from different interface regions show similar results, thus giving confidence in the findings and interpretations made above. Figure 4.7i and j present high-resolution images of the *as-deposited* amorphous sample and the corresponding diffraction pattern, respectively. In accordance with the XRD measurements, no crystalline or nanocrystalline fractions are present in the silicon film, thus making this film a good starting point for recrystallization experiments.

Atomic force microscopy measurements were performed to determine the surface roughness of the various samples. All samples had been etched in hydrofluoric acid prior to AFM analyses to remove any surface oxide. Figure 4.8 shows the surface topography of two selected samples A1 and B5. The arithmetic average roughness R_a and the root mean squared roughness R_q were calculated using the whole scan area of 5 · 5 µm^2. With $R_a = 34.9$ nm and $R_q = 45.6$ nm the LPCVD sample exhibits the roughest surface topography. The highly boron-doped sample B1 has a roughness of $R_a = 9.1$ nm and $R_q = 13.4$ nm, respectively. This can be attributed to the larger grain size of this sample. All the other samples appear much smoother. A minor influence on the Si layer thickness is notable. The 100 nm Si

thin film measured R_a = 3.1 nm and R_q = 4.1 nm, the 500 nm Si sample R_a = 1.2 nm and R_q = 1.9 nm, and the 1500 nm Si measure R_a = 0.7 nm and R_q = 0.9 nm, respectively. The decrease in roughness with increasing film thickness can be attributed to a more homogenous film thickness of the amorphous film prior to crystallization as well as to smaller mean grain size values observed in thicker films. All the other samples are in the range of the 500 nm Si (±10%) and no major influence of the annealing conditions on the surface roughness could be observed. The second boron-doped sample B2 exhibits a similar surface structure to B1. Compared to the LPCVD polycrystalline silicon, the surface roughness could be reduced by more than a factor of twenty using sputter-deposition and PDA.

4.2.4 Conclusion

The possibility of using sputter-deposition to form Si/4H-SiC heterostructures was investigated. Extremely smooth, amorphous films could be deposited with about 1.25 nm/s at 500 W. Even at the highest possible deposition temperature of 400 °C no crystallinity was observed. Therefore, the crystallization behavior of sputtered a-Si films on 4H-SiC was investigated when exposed to different post-deposition annealing conditions. Key parameters were the annealing temperature, the annealing time, as well as the heating rate, and the drive-in conditions for doping. XRD measurements showed a trend for the presence of larger mean grain size values with increasing annealing temperatures and times, as well as for slower heating rates. In addition, the corresponding influence on the peak shift and hence, the stress inside the grains were discussed. The smallest difference from standard Si powder was found for thinner films and longer annealing times. The highly boron-doped samples appear to have the lowest stress level and the largest grain size. This is in excellent agreement with TEM analyses demonstrating that the doped films have grains of several 100 nm in size. TEM and HRTEM imaging of selected samples confirmed the polycrystalline nature of all deposited films after high-temperature loading. Very sharp and distinct interfaces but without any indication for solid-phase epitaxy were found. Although requesting an annealing step, the biggest advantage of sputtered Si films was the extremely smooth surface topography of less than 1 nm mean squared roughness for a 1500 nm thick Si sample, compared to LPCVD Si with a corresponding roughness value above 45 nm. Sputtering together with PDA might be suitable for forming Si/4H-SiC heterostructures, for both electrical and electromechanical application scenarios. In Chapter 6, the electrical characteristics of sputtered Si/4H-SiC heterojunctions are investigated.

4.3 LPCVD deposited Si on 4H-SiC

Parts of this section have been published in [242]

LPCVD is a well-established deposition technique for growing polycrystalline and epitaxial films. The possibility to vary many parameters like the pressure, the temperature, the gas flow rates, and the gas sources in a wide range makes it a perfect tool for evaluating new material combinations. Also, the possibility to apply different *in-situ* pre-conditionings and etch steps based on e.g., H_2 or SF_6 is given. As discussed in the beginning of this chapter, LPCVD has already been used successfully to form Si/6H-SiC heterostructures with the plane orientations depicted in Figure 4.1. Despite the large lattice mismatch of about 20%, the Si{111}/xH-SiC{0001} and the Si{110}/xH-SiC{0001} heterostructures were realized [38], [215]–[219]. The possibility to operate at temperatures even above 1000 °C at low pressures, makes LPCVD an ideal candidate for investigating the growth of Si on 4H-SiC. In contrast to sputter-deposition the temperature required for direct crystalline growth is easily met, still allowing reasonable deposition rates. Several depositions have been performed varying the reaction to carrier gas ratio, the total pressure, and the temperature. After finding deposition parameters giving reasonable film thicknesses and uniform film coverage, all parameters but the temperature were kept constant.

Figure 4.9: SEM images of LPCVD Si deposited at (a) 900 °C and (b) 1080 °C varying the total pressure, the silane flow and the time.

4.3.1 Experimental details

4H-SiC substrates from Cree Inc. with a bulk resistivity of 0.015 to 0.028 Ωcm and a 4° off-c-axis cut have been used for the experiments. Si deposition was done on the Si-face of the wafer, which is equipped with a 5 µm thick epitaxial layer of $N_D = 1.6 \cdot 10^{16}$ cm^{-3}. Prior to deposition, the samples were cleaned using acetone, hydrofluoric acid, and an RCA cleaning solution. All depositions were done in a Firstnano EASYTUBE 3000EXT hot-wall LPCVD furnace using pure silane (SiH$_4$) as silicon precursor and hydrogen (H$_2$) as carrier gas. The samples were placed on a quartz holder arranged horizontally to the gas flow. Prior to the Si deposition, the sample was etched in H$_2$ atmosphere for 10 min at 1000 °C to achieve an atomically flat, hydrogen-terminated surface [181]. One sample did not get the H$_2$ treatment but was exposed to SF$_6$ during heating up to 1080 °C. After the H$_2$ or SF$_6$ treatment, the furnace was evacuated and regulated to the desired deposition temperature. When the peak temperature was reached the process gas inlet was opened using a variable flow of SiH$_4$ and a fixed flow of 300 sccm H$_2$. The deposition pressure was regulated by the pump speed. After the deposition was finished the chamber was cooled down in vacuum and flooded with N$_2$.

The first sample series consisted out of only two deposition temperatures, 900 and 1080 °C. At 900 °C, three depositions were performed at a rather high pressure of 1.895 torr and 3 sccm SiH$_4$ flow rate and at lower pressures with two different flow rates (0.3 torr, 3 sccm and 0.5 torr, 10 sccm). The H$_2$ flow was always kept constant at 300 sccm. Due to the constant H$_2$ flow, a variation of the SiH$_4$ flow rate corresponds to a change of the SiH$_4$ partial pressure. At these samples the influence of the total pressure and partial pressure on the resulting film quality was investigate. At the highest possible temperature of 1080 °C also three samples were deposited using only low pressures and the following parameters: 0.3 torr, 3 sccm SiH$_4$; 0.5 torr, 10 sccm SiH$_4$; and SF$_6$ pre-etch, 0.5 torr, and 10 sccm SiH$_4$.

After evaluating with SEM and XRD the film thickness and microstructure at these deposition parameters, a low pressure of 0.5 Torr and a SiH$_4$ flow of 10 sccm turned out to give a reasonable deposition rate. By keeping the latter parameters constant, the deposition temperatures were varied between 700 to 1080 °C in the next sample series. The deposition time was set to 180 min. Again, SEM
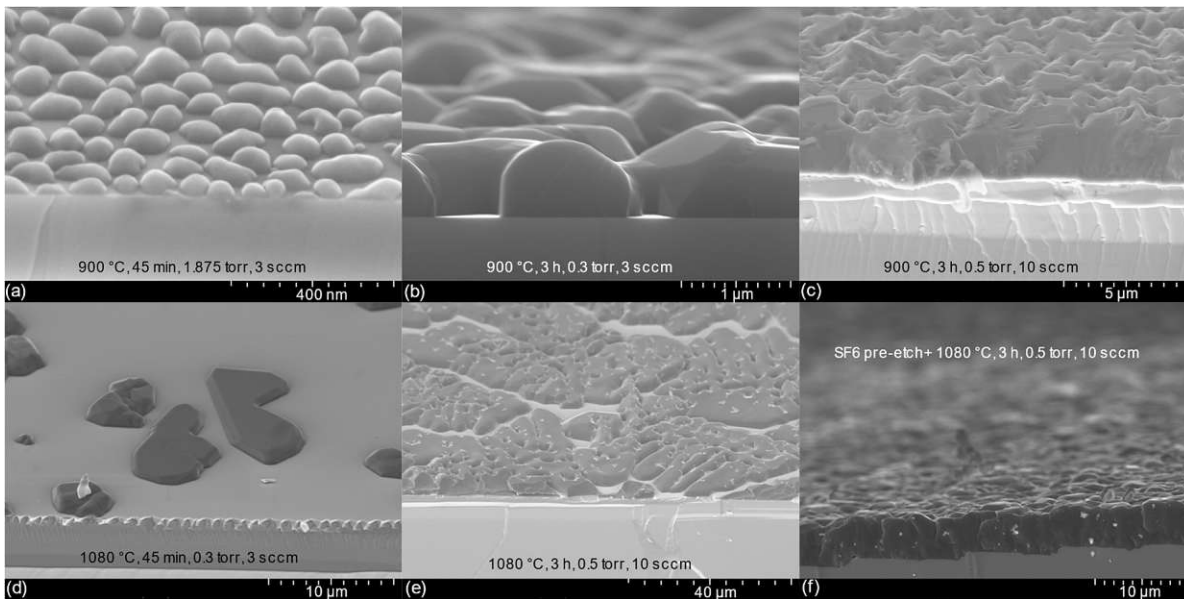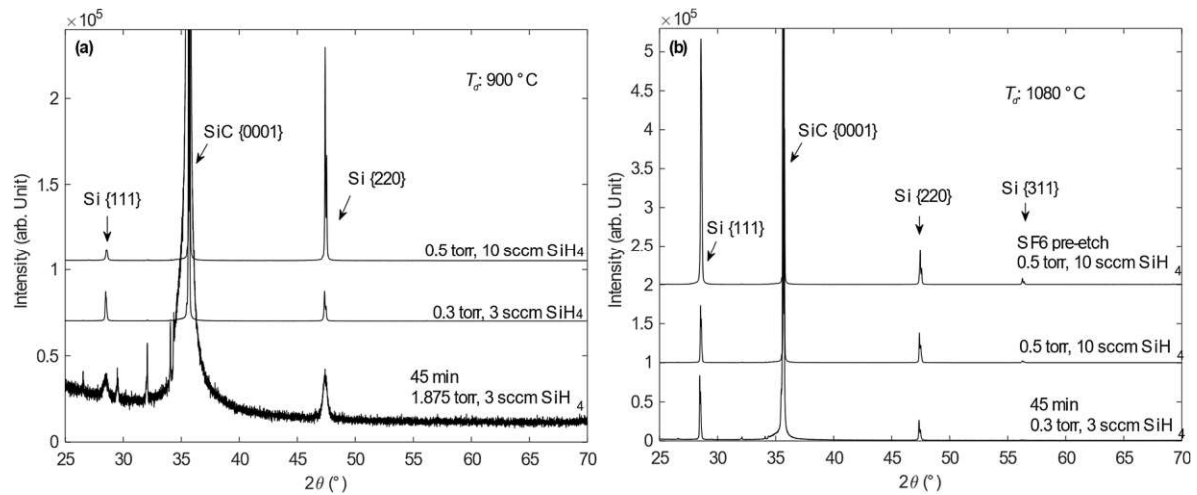
Figure 4.10: XRD diagrams of LPCVD Si deposited at (a) 900 °C and (b) 1080 °C varying the total pressure, the silane flow and the time.

and XRD were applied for microstructural analysis. Some promising samples were selected and prepared for TEM analysis.

4.3.2 Results and discussion

The first 6 samples were investigated with XRD in Bragg-Brentano configuration and with cross-sectional SEM under an angle to observe both, the surface and cross-sectional microstructure. Figure 4.9 shows the SEM micrographs of the samples subject to different deposition conditions. One immediately notices the large microstructural difference between the samples. Using 900 °C, 1.875 torr, and 3 sccm SiH_4 flow, and a deposition time of 45 min, a dense distribution of Si islands with about 100 nm height was achieved. A very similar picture of Si island growth was observed by Gammon using 900 °C MBE deposition [54]. It was concluded that the pressure is too high and the deposition time is too short to achieve a closed film with reasonable thickness. Lowering the pressure to 0.3 torr and increasing the deposition time further to 180 min did significantly increase the film thickness to about 1 μm, as depicted in Figure 4.9b, although the film is still not closed. Lowering the total pressure will increase the transport rate, but as the partial pressure of SiH_4 was also reduced, by keeping the flow rates constant, no overall increase of the deposition rate is expected. Considering the 4 times longer deposition time, the deposition rate still increased compared to the samples synthesized with higher total pressure. Due to the lower pressure the higher gas flow rate presumably led to a more even distribution of reactants in the chamber. At high pressure, a strong gradient of the deposited chamber wall was observed. Almost all the precursors were consumed in the first few cm, leaving a much lower concentration at the sample. This is a disadvantage of the used hot-wall reactor type, leading to precursor depletion due to deposition on all hot parts. On the next deposition, the pressure was only slightly increased to prevent precursor deletion, but the SiH_4 flow rate was increased from 3 to 10 sccm, leaving the H_2 flow constant, hence resulting in a 333% higher SiH_4 partial pressure. As expected, according to Equation (3.1), the higher precursor concentration will result in a higher deposition rate. Figure 4.9c shows the sample deposited using 10 sccm SiH_4 flow. Although not visible very well the thickness is with about 2.2 μm more than twice as thick, as the previous deposition. Also, the film appears close, with no more openings to the substrate.

Next, depositions at the highest possible chamber temperature of 1080 °C are performed. Due to the previous findings, the total pressure was kept low. The first run was performed at 0.3 torr and 3 sccm SiH_4, with the results shown in Figure 4.9d. A covering of very isolated Si islands, representing Volmer–

Weber growth mechanism [243], with 1 to 2 µm height is found using 45 min deposition time. The islands appear very sharp and crystalline. Due to the large lattice mismatch, an island-type growth regime is expected. Fissel et al. [221] found a critical thickness of 1.4 monolayers for MBE grown Si on 6H-SiC before island formation takes place. To improve the film coverage and thickness, the conditions were again changed to 0.5 torr and 10 sccm SiH_4 flow. Doing so, the coverage and thickness could be improved as shown in Figure 4.9e, but still, no closed film was possible. Another approach to improve the homogeneity of the Si film was tried, by changing the 4H-SiC surface topography using SF_6 etching at 1080 °C. Using SF_6 plasma, high etch rates of SiC are possible [244]. To the best of the author's knowledge, no publication regarding SF_6 etching of 4H-SiC without plasma assistance is available. SF_6 decomposition will be strong at temperatures above 600 °C [245], therefore an etching effect will be assumed. Using the same Si deposition parameters as before, but with the SF_6 pretreatment, a different surface and microstructure was obtains as shown in Figure 4.9f. Although keeping the Si deposition parameters the same, the film thickness changed to about 4.2 µm and the film is completely closed. The underlying 4H-SiC substrate shows strong etching damage in the form of long terraces. The newly formed terraces exhibit a larger step height than one would expect from the 4° off-axis cut of the substrate and therefore their formation is attributed to be due to the gas flux direction. The reason for the increased deposition rate remains open. Residual SF_6 might undergo gas-phase reactions with the SiH_4, resulting in species with a higher deposition rate. When introducing dopant gases like PH_3 or B_2H_6, also strong effects on the growth rate and gas phase reaction of SiH_4 were observed [246]. Also chlorine has an positive effect on the growth rate on both Si and SiC epitaxy [247].

Figure 4.10a and b depict the 2θ scan intensity data of the samples deposited at 900 and 1080 °C, respectively. The first deposition at 1.875 torr pressure exhibited the lowest signal due to the thin Si coverage and shows therefore the noisiest data. All depositions show the presence of Si{111} and Si{220} textures. Only slight reflections attributed to Si<311> oriented crystals are found in the high temperature deposited samples at 0.5 torr. The ratio between the two main orientations is quite balanced with the exception of a dominant Si<220> orientation on the sample with 900 °C and 0.5 torr and a dominant Si<111> orientation using the SF_6 pretreatment. A TEM image and detailed evaluation of the XRD result of the SF_6 treated sample will be given below.

With the information obtained in these preliminary experiments, a rather low deposition pressure of 0.5 torr and a SiH_4 flow of 10 sccm was selected as optimal parameters to achieve a reasonable film thickness and a closed film at least at 900 °C. Therefore, these parameters were kept constant for the main experiment, where the deposition temperature was varied between 700 and 1080 °C. The SF_6 treatment was not used for further experiments and diode fabrication, although it resulted in a high deposition rate and a closed film at the highest temperature. A separate set of experiments needs to be conducted in the future to evaluate the performance of this treatment at different temperatures and gas concentrations.

Altering the deposition temperature

SEM images of the samples at all deposition temperatures are depicted in Figure 4.11. All images were recorded at the same magnification for direct comparison. The samples deposited at 700, 800 and 900 °C appear to have a similar microstructure with a closed Si film morphology. The samples deposited at higher temperatures consist of rather large grains, which have grown together with their adjacent neighbors in many regions on the surface. This increased grain growth resulted in non-closed or even dewetted film characteristics so that regions are detectable where the SiC surface is still exposed. This situation becomes worst at 1080 °C deposition temperature. Cross-sectional SEM images have been used to measure the film thickness at several points and to calculate the deposition rate. Figure 4.12a shows the calculated deposition rate over the deposition temperature. Starting at about 13 nm/min at
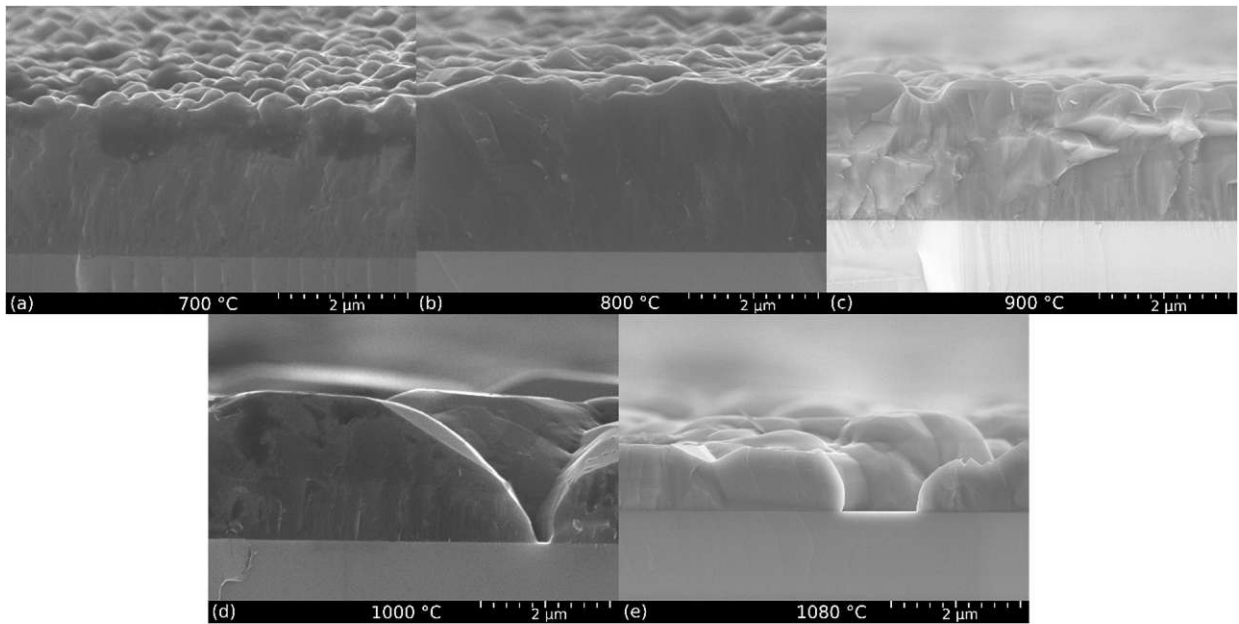
Figure 4.11: Cross-sectional SEM images of samples deposited at five different temperatures. The pressure was constant at 0.5 torr and the SiH_4 flow rate was 10 sccm.

700 °C, the maximum deposition rate is detected at the 800 °C sample with almost 15 nm/min. With increasing temperature, the deposition rate decreases, but also the standard deviation increases strongly due to the preferred island-like grain growth instead of closed film growth, which makes an accurate evaluation of the deposition rate difficult. The initial increase in the deposition rate from 700 to 800 °C might be attributed to the enhanced reaction kinetics at this temperature range, while any further increase of the deposition temperature did not result in higher deposition rates. Based on the latter result, the growth kinetics above 800 °C are assumed to be transport-limited by the precursor gases, not by the chemical reaction, hence no significant difference in the growth rate over the wide temperature range is notable [248]. The trend to lower deposition rates at temperatures >800°C might also be attributed to precursor depletion due to the hot-wall reactor type. As mentioned before, at the higher deposition
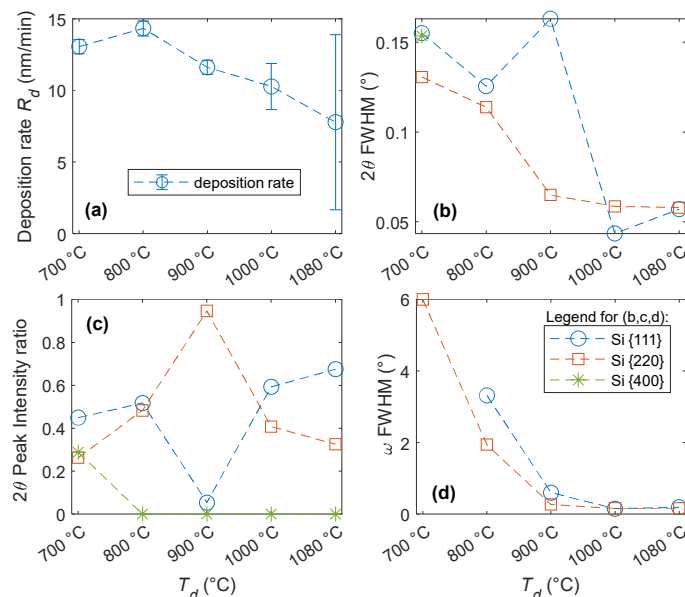
Figure 4.12: (a) Deposition rate, (b) 2θ FWHM, (c) relative peak intensity, and (d) ω FWHM as a function of deposition temperature.
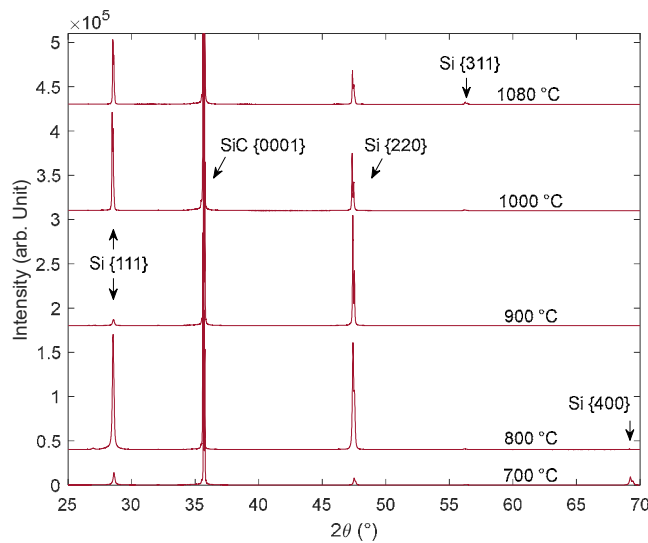
Figure 4.13: XRD diagrams of Si layers deposited at different temperatures on 4H-SiC substrates.

pressure this effect was observed. Also, at this reduced pressure, some gradient in the precursor concentration is expected.

Figure 4.12b and c show the FWHM and the relative peak intensity of the 2θ XRD measurements, respectively. The corresponding XRD diagrams are depicted in Figure 4.13. The sample deposited at 700 °C shows an even distribution of Si{111}, Si{220} and Si{400} reflections with the largest FWHMs in the range of 0.15°, indicating the presence of a fine-grained, polycrystalline microstructure. At an increased deposition temperature of 800 °C, the Si{400} peak completely vanished leaving only Si{111} and Si{220} peaks with an FWHM of about 0.13°. At 900 °C deposition temperature almost exclusively <110> oriented Si is observed in the XRD pattern with a peak FWHM of 0.065°. The weak Si{111} reflection showed a much higher FWHM of 0.16°. When increasing the deposition temperature to 1000 °C the Si{111} peak returned, being even stronger than the {220} reflection. Both are very sharp with FWHMs of about 0.043 and 0.058 for Si{111} and Si{220}, respectively. At 1080 °C, a similar XRD pattern is observed, with a slightly more pronounced Si{111} and a very weak Si{311} peak. FWHMs are around 0.057° for both peaks.

Additionally, to the 2θ measurements, rocking curves (ω-sweeps) were performed at the two main reflections Si{111} and Si{220}. The resulting FWHMs of the two peaks as a function of the deposition temperature are depicted in Figure 4.12d. At the lowest deposition temperature of 700 °C, the Si{111} reflection was too broad to specify an FWHM, and the Si{220} reflection was misaligned by an FWHM of 6°. A polycrystalline texture with almost random grain orientation can be attributed to this film. With increasing deposition temperature, the ω-FWHM decreases. At 1000 °C deposition temperature and above, the FWHM was between 0.15 and 0.2°, being at the resolution limit of the instrument, so that the real FHWM of the films might be below that value.

A strong influence of the poly-Si thin film texture on both the deposition temperature and the silane partial pressure was reported in [249]. Using the texture zone model of Joubert et al. [249] to map the depositions performed in this work, the 700 °C sample is located in the transition between randomly and <100> textured, whereas all higher deposition temperatures are in the randomly oriented zone if one assumes no further zones at higher temperatures. Indeed, the 700 °C deposition is the only one showing <100> oriented texture in the XRD data. At a deposition temperature of 800 °C, however, the XRD data

lacks any <100> texture. Above 800 °C the orientation of the Si film is believed to be governed by the crystal structure of the underlying SiC substrate.

Pérez-Tomás et al. [41] who used molecular beam epitaxy (MBE) to grow Si on Si-face 4H-SiC also observed the coexistence of both, Si<111> and Si<110> oriented films at elevated temperatures, although the almost unique Si<110> growth orientation found in our study at 900 °C deposition temperature was not observed. This is not surprising, as MBE is a quite different deposition technique than LPCVD. Xie et al. [215] also used H_2 pretreatment and LPCVD to deposit Si on the Si-face of 6H-SiC substrates at different temperatures. Although less pronounced, a dominant Si{220} growth was observed at 900 °C, followed by a reversal to pronounced Si{111} at higher temperatures, being in accordance with the experimental results of this thesis. Being in line with Xie et al. it is assumed, that below 900 °C not enough thermal energy is available to overcome the surface energy of the 4H-SiC to form an epitaxial interface. Above, the growth of either <110> and/or <111> oriented Si is thermodynamically favorable.

To further study the Si growth and the interface quality, the samples deposited at 800, 900, and 1000 °C were prepared for TEM imaging. Figure 4.14 shows the interface region of the sample synthesized at 800°C deposition temperature. Similar to the XRD results, the sample shows no homogenous single-phase microstructure, but many stacking faults and changes in crystallographic orientation. A FFT diffraction pattern was calculated from the image and is shown in the inset of Figure 4.14b. The diffraction pattern also shows a widespread in Si{111} and some Si{220} plane reflections. TEM images of the whole film thickness (not shown) indicate an increasing grain size with increasing distance from the interface. Many nucleation sites are assumed to be responsible for the rather random microstructure at the interface, whereas only some grains dominate the growth with increasing film thickness. At Si deposition temperatures of 800 °C and lower no heteroepitaxial interface could be achieved on 4H-SiC.

The interface of the sample with a deposition temperature of 900 °C is shown in Figure 4.15. The image shows a region of the interface with two grains, on the left with the Si{111}/4H-SiC{0001} and on the right with the Si{110}/4H-SiC{0001} heterostructure orientation. Insets (b) and (c) are the FFT patterns of the corresponding grains, which have been used to identify the crystal orientations, indicating a
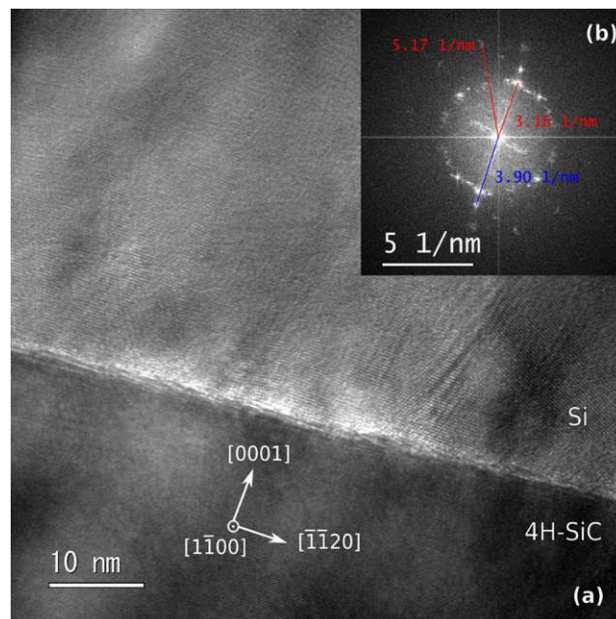
Figure 4.14: (a) HRTEM image of the Si/4H-SiC interface of the sample deposited at 800 °C. Inset (b) is a calculated FFT diffraction pattern of the image.
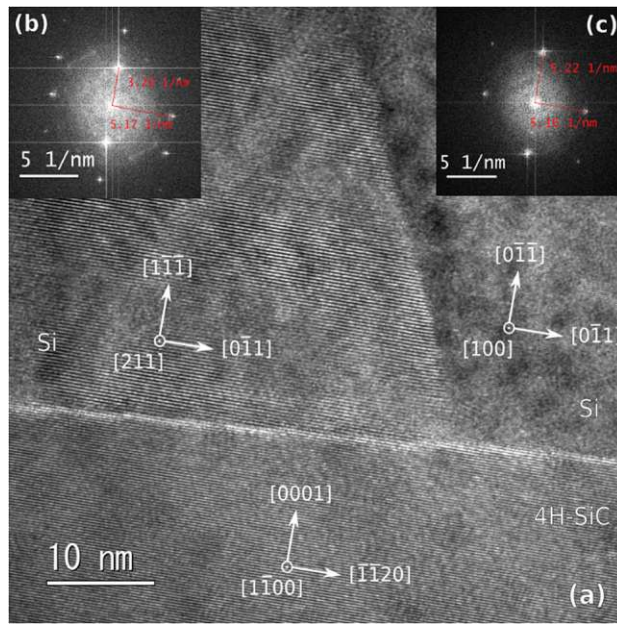
Figure 4.15: (a) HRTEM image of the Si/4H-SiC interface of the sample deposited at 900 °C. Insets (b) and (c) are calculated FFT diffraction patterns of the left and right grain, respectively.

monocrystalline microstructure in both regions. The Si grains show a parallel plane orientation to the SiC and no sign of surface reaction is visible. In addition, the steps due to the 4° off-axis cut of the 4H-SiC did not introduce any distortion to the Si lattice. The in-plane orientations are Si[0-11]//4H-SiC[-1-120] for both, the Si{111} and the Si{110} layers, being in accordance with previous experiments and the schematic illustration in Figure 4.1. At a deposition temperature of 900 °C the interface can be considered epitaxial.
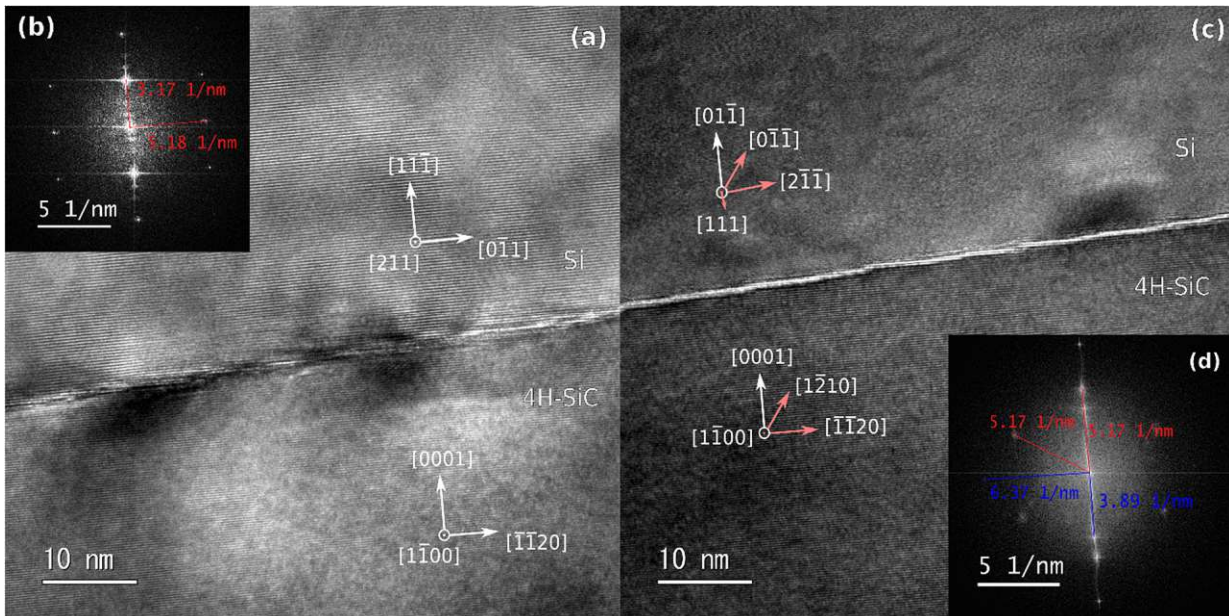
Figure 4.16: HRTEM images of the Si/4H-SiC interface of the sample deposited at 1000 °C at different positions, (a) and (c) are showing different orientations of the Si film at different sites. Insets (b) and (d) are calculated FFT diffraction patterns of the corresponding image. In (c) the crystal direction in the interface plane are light red and the one normal to the interface is white.

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Figure 4.16 shows two interface regions of the Si/SiC heterostructure deposited at 1000 °C. At this deposition temperature, large grains with the same grain orientation are observed. In Figure 4.16a and inset (b) the Si{111}/4H-SiC{0001} heterostructure and Figure 4.16c and inset (d) the Si{110}/4H-SiC{0001} heterostructure are depicted. As found by XRD measurements, both Si growth orientations are present, whereas much more grains with the Si<111> growth direction are found. The Si{111} layer shows again the expected Si[0-11]//4H-SiC[-1-120] in-plane orientation. The image showing the Si layer grown as Si{110} shows a different in-plane orientation compared to the 900 °C sample in Figure 4.15. The FFT diffraction pattern indicated the in-plane orientation of Si[2-1-1]//4H-SiC[-1-120]. This grain, indicating a different in plane orientation, was further investigated by tilting the sample in the TEM. This investigations showed, that it is in the expected in-plane orientation but the Si layer is rotated by 60° resulting in Si[0-1-1]//4H-SiC[1-210]. Taking a look at Figure 4.1, one can see that rotating the Si{110} plane by +/- 60° results in an equivalent in-plane orientation. Therefore, the Si[2-1-1] and 4H-SiC[-1-120] directions are only 5° apart, resulting in a diffraction pattern that might mistakenly be interpreted as Si[2-1-1]//4H-SiC[-1-120]. Again, a heteroepitaxial connection can be confirmed. The sample deposited at 1080 °C is also regarded to be heteroepitaxial, confirmed by XRD rocking curves. Again, the terraces of the 4H-SiC did not seem to influence the quality of the grown epitaxial Si layer.

With both the TEM and the XRD results, the following assumptions regarding the growth process at different deposition temperatures can be made. At deposition temperatures of 700 and 800 °C, the interface formation energy for epitaxy is not reached, hence no epitaxial connection to the 4H-SiC substrate is achieved, resulting in random nucleation, similar to the growth on amorphous substrates. At 900 °C, both Si{111}/4H-SiC{0001} and Si{110}/4H-SiC{0001} interfaces were formed during growth. The dominance of the <110> orientation might also be due to an enhanced growth rate of the <110> oriented Si facets. Above, both orientations were found to have an epitaxial connection to the Si, but the dominance of the Si<110> orientation reduced. More accurate simulations of the interface formation energies of the Si/Si-face 4H-SiC system are required for an in-depth analysis of the observed findings.

SF_6 pretreatment

Also, the sample undergoing SF_6 pretreatment followed by 1080 °C Si deposition was prepared for TEM measurements and the XRD data were evaluated further. The FWHMs of the Si{111} and the Si{220} peak were found to be 0.067° and 0.092°, respectively, being, therefore, broader than the deposition at the same condition without the SF_6 treatment. The ω-FWHM of the same two reflections was measured to be 0.45° and 0.83°, again being broader than without SF_6 treatment. The peak broadening could also be due to the increased film thickness, giving the most signal from the surface near lattice. The interface might be of higher orientational quality, as is observed in TEM.

An HRTEM of the interface is shown in Figure 4.17. Despite the large-scale surface roughness in form of terraces visible in the SEM image, a strong increase of surface roughness on the nanometer scale is noticeable. Despite the rough interface, the Si layer at the interface appears to be monocrystalline and well oriented to the 4H-SiC orientation in form of the Si{111}/4H-SiC{0001} heterostructure with the Si[0-11]//4H-SiC[-1-120] in-plane orientation, as observed before.

Figure 4.18 shows an optical micrograph of the sample surface after the Si was removed. The terraces visible in SEM are well noticeable. But also, random distribution of etch pits are visible all around the substrate surface. Sometimes they show a hexagonal shape, sometimes a circular one. Similar etch patterns on SiC surfaces have been observed before, e.g., using high-temperature molten KOH etching [250]. The etch pits are attributed to defects of the SiC lattice. Depending on their shape, they are either threading edge dislocations (circular), screw dislocations (shallow hexagonal) or micropipes (deep
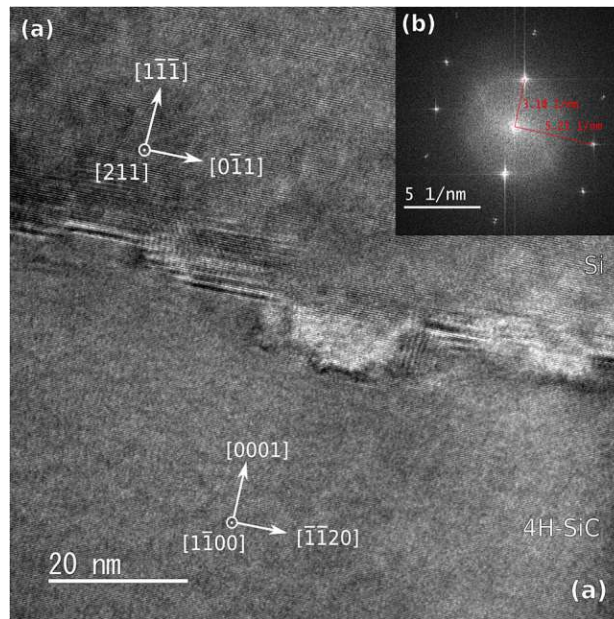
Figure 4.17: HRTEM images of the Si/4H-SiC interface of the sample with SF_6 pretreatment and Si deposition at 1080 °C. Inset (b) shows a calculated FFT pattern of the Si part of the image.

hexagonal) [250]. None of the observed pits are assumed to be due to micropipes, as the density of micropipes is extremely low (<1 cm^{-1}).

Due to the massive etch damage and the uncertainties in the involvement of residual SF_6 during the deposition process, this sample was not used for diode fabrication. Further investigations are required.

The five samples with different deposition temperatures were doped and further processed to form HJDs. The electrical results are presented in Section 6.4.

4.3.3 Conclusion

The growth of Si on 4° off-axis 4H-SiC substrates was investigated using different LPCVD deposition parameters. After finding reasonable film coverage and growth rates at a pressure of 0.5 Torr and at gas flow rates of 10 sccm SiH_4 and 300 sccm H_2, the temperature was varied between 700 and 1080 °C. The growth rate was in the range of 7 to 15 nm/min with the maximum at 800 °C deposition temperature. Si
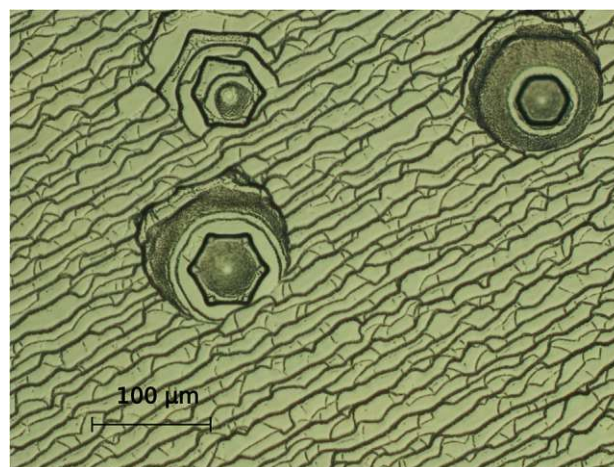
Figure 4.18: Surface optical microscope image of the sample with SF_6 pretreatment and subsequent Si deposition at 1080 °C

films deposited at 1000 °C and above did not show a closed Si film coverage. Using XRD and TEM, the growth of mainly Si<111> and Si<110> was confirmed. At 900 °C deposition temperature an almost only <110> oriented and closed Si film could be deposited. A deposition at temperatures between 900 and 1080 °C showed heteroepitaxial growth of Si on 4H-SiC, without any distortion due to the off-axis orientation of the substrate. Also, SF_6 etching prior to Si deposition was investigated, resulting in the highest deposition rate and a very rough but epitaxial interface at a deposition temperature of 1080 °C. A high density of rather deep etch pits limits the use for most applications.

Future research should focus on different substrate pretreatments. The influence of H_2, SF_6, other etchants or plasma that may change the surface topography of the SiC prior Si deposition. Additionally, a variation in the deposition temperature during growth could be used to achieve epitaxial connection and a closed film, simultaneously.

4.4 Doping of the Si-film

For almost all electrical devices the deposited Si film needs to be doped with both the correct type and concentration. There are several possibilities to achieve a doped Si-film.

One common technique is the deposition of already doped films, by adding the dopants during growth. In CVD processes gaseous precursors, containing the desired dopants, are introduced in low concentrations during deposition. For the common dopant species boron and phosphorus, these gases are PH_3 and B_2H_6. Both are extremely toxic and explosive, therefore not all CVD equipments are able to deal with this kind of gases due to safety restrictions. The latter applies to the LPCVD equipment used in this thesis, therefore any LPCVD films were nominally undoped. Using PVD techniques like evaporation or sputtering a deposition of already doped films is possible applying either co-evaporation/co-sputtering or by using evaporation materials or targets already containing the desired dopant. Evaporation is more difficult in this respect, as the vapor pressures and melting points of the semiconductor material and the dopant material may differ substantially. Using sputter-deposition, sputter rate variations of different elements due to the presence of a compound target are low and allow to sputter-deposit films with almost the same chemical composition as the target. If the sample is not heated above the crystallization temperature of the semiconductor the resulting film is of amorphous phase, and the majority of the dopants are not electrically active.

The second approach is doping via diffusion. Both, diffusion from the gas phase, often requiring toxic gases, or from the solid phase are widely used. Liquid phases may also be available. Due to its simplicity and lack of toxicity, the diffusion from the solid phase was applied in this study. A wide variety of materials, being in its elemental form or as compounds, containing the dopant species, are available. For this thesis liquid, spin-on dopants from either "Desert Silicon" or "Filmtronics" were used. These liquids mostly consist of Si, O, and the dopant species, e.g. B or P in form of some complex compounds together with solvents. After applying them by spinning, dipping, or spraying, the solvent evaporates resulting in a glass layer with a certain dopant concentration, this process is known as sol-gel process [251]. Afterward, the films need to be heated to temperatures between 800 and 1200 °C to allow the dopants to diffuse from the glass film into the underlying semiconductor. The final doping concentration and profile are sensitive to: the initial concentration of the dopant species in the spin-on-glass layer, the thickness of this layer, the diffusion temperature, and the time. Finally, the glass layer can be removed with HF.

Figure 4.19: SIMS depth profile of the boron concentration of a sample with 500 nm Si on 4H-SiC, sputter-deposited from a undoped Si target followed by spin-on doping and diffusion at 1000 °C for 30 min.

A third method for doping is by implantation. Implantation provides a certain dopant profile, buried under the surface, while the dose can be adapted very precisely. Disadvantages are the lattice damage, which requires additional annealing for healing and activation of the implanted dopants. This technique was not used in this thesis, as it is not ideal for doping thin films, without unintentionally implanting the underlying SiC.

4.4.1   Spin-on dopant

The first sputter-deposition experiments were performed from an undoped Si target. For diode fabrications, rather highly doped Si films are required, to restrict any depletion region to the SiC substrate and to achieve a good ohmic contact to the Si.

For p-type doping, the boron-containing solution B155 from Filmtronics was used. After applying 2 layers by spin coating, and a drive-in at 1000 °C for 30 min under air atmosphere, the final dopant concentration was determined by SIMS and the electrical resistivity was measured with the van der Pauw (VDP) method [252]. The SIMS measurements were performed by the Institute of Chemical Technologies and Analytics at TU Wien with a ToF SIMS 5 from Iontof operating using Bi$^+$ primary ions and Cs$^+$ sputter ions. For quantification of the actual dopant concentration, a reference of Si containing the desired dopant in a known concentration was provided. The depth profile of the boron concentration of the sample with 30 min 1000 °C drive-in is depicted in Figure 4.19. The Si film of about 500 nm thickness shows a uniform doping concentration of about $2.4 \cdot 10^{19} \text{cm}^{-3}$. The high boron concentration at the interface can be attributed to either a real boron accumulation at the interface or an often observed artifact of ToF-SIMS, the matrix-effect [253]. The matrix-effect is a shortcoming of the SIMS technique. The secondary ion emission also strongly depends on the surrounding chemical environment. As a consequence, huge errors up to orders of magnitudes are possible when evaluating the concentration of an element near interfaces or in different environments as the used standard [254]. Also, the apparent concentration of about $1 \cdot 10^{18}$ cm^{-3} in the SiC at sputter times of more than 1000 s needs to be considered with care. At a dopant drive-in temperature of 1000 °C any active doping of the 4H-SiC, which usually requires temperatures in excess of 1500 °C for diffusion and activation can be neglected [255], [256]. Although low-temperature diffusion of SiC was shown to be possible, it involves oxidation and/or silicidation of the surface to enhance silicon and carbon out-diffusion, allowing
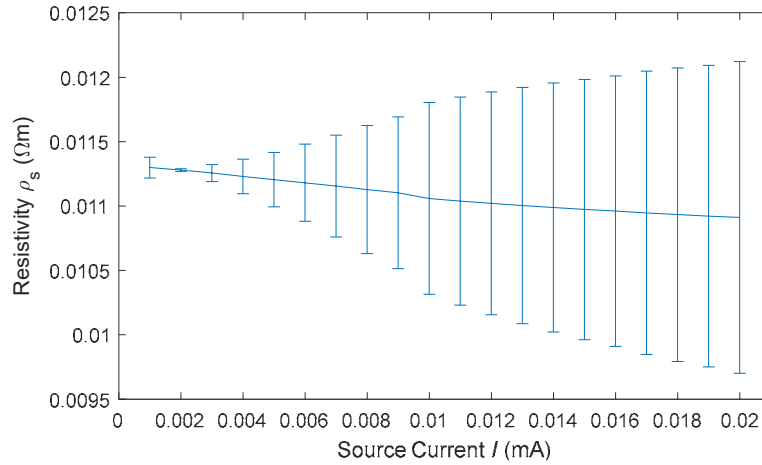
Figure 4.20: Semiconductor resistivity obtained with VDP method for different source currents of the sample with 500 nm Si, at 1000 °C and 30 min boron drive in.

impurity in-diffusion [257], [258]. Therefore, it is reasonable to exclude any significant doping of the 4H-SiC underneath the Si. Therefore, the strong interface signal is attributed to either the matrix-effect or background noise due to the low sensitivity of the experimental setup. With the used setup and measurement parameters a single count of Boron represents a doping concentration of about $1.3 \cdot 10^{17}$ cm^{-3}. With this low sensitivity and the moving average filter, only some occasional counts result in an apparent high doping concentration. For high sensitivity doping profile measurements SIMS with a quadrupole or magnetic-sector detectors are more suitable [259], as they can focus on a specific atom, whereas ToF acquires a whole mass spectrum with a very high mass resolution. But for the high dopant concentrations investigated in this study the available ToF-SIMS was satisfactory. To verify the measured dopant concentration and its electrical activity, VDP measurements were conducted on a custom-built setup. The deposited Si-film was therefore patterned in the form of a four-leaf clover. The measurement technique directly provides the film resistivity if the film thickness is known. Figure 4.20 shows the measured resistivity over the measurement source current. Rather low currents were used to prevent too high voltages, restricting the measurement to the Si film. As can be seen in the figure, the resistivity stays rather constant at about $11 \cdot 10^{-3}$ Ωm. To link the semiconductor resistivity and the carrier concentration (activated doping concentration, $p \sim N_A^-$), the carrier mobility is necessary according to

$$\rho_s = \frac{1}{q\mu p}. \tag{4.1}$$

The mobility μ is not constant, but depends on the doping concentration, and for polycrystalline films also strongly on the grain size [260]. For bulk semiconductors, the mobility decreases with increasing impurity concentration due to scattering. Polycrystalline materials exhibit a much lower mobility, with a strong dependence on the grain size due to depletion of the grains and additional scattering at GBs. At very high dopant concentrations and an average grain size between 50 and 100 nm, the mobility is assumed to be in the range between 3 and 10 cm^2/Vs [260], [261]. A VDP setup with a controllable magnetic field would be necessary to conduct Hall-measurements, which allows the extraction of both, the resistivity, and the mobility. Solving Equation (4.1) for p with these mobilities and the measured resistivity, the carrier concentration lies in the range of $0.7 \cdot 10^{19}$ to $2.3 \cdot 10^{19}$ cm^{-3}, which is very close to the measured boron concentration of about $2.4 \cdot 10^{19}$ cm^{-3}. Considering the tolerance of the used
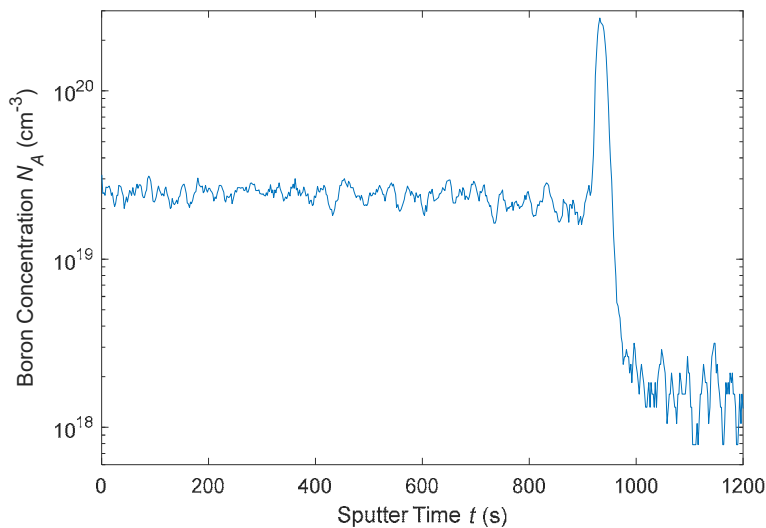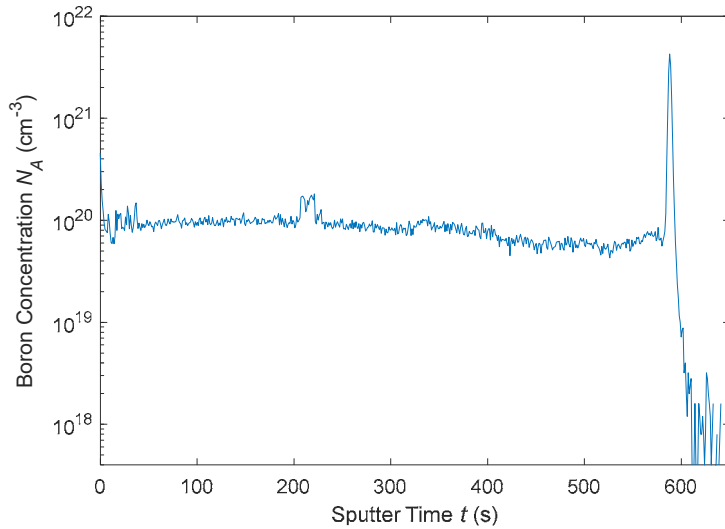
Figure 4.21: SIMS depth profile of the boron concentration of a sample with 500 nm Si on 4H-SiC, sputter-deposited from a highly boron doped Si target and PDA at 1000 °C for 2 h.

SIMS reference and the deviation between total concentration and electrically active concentration, the match between SIMS and electrical measurement is good, giving proof to a high concentration of about $2 \cdot 10^{19}$ cm^{-3}.

4.4.2   Pre-doped sputtering targets

After the successful doping of the sputter-deposited Si-film using spin-on dopants, another doping approach was tested, by ordering pre-doped Si sputter targets. A highly boron and a highly phosphorus-doped target were used. Both were supplied by SPM AG and are monocrystalline with a purity of 6N. The boron-doped target is specified to have a resistivity of <0.005 Ωcm and the phosphorus one <0.02 Ωcm.
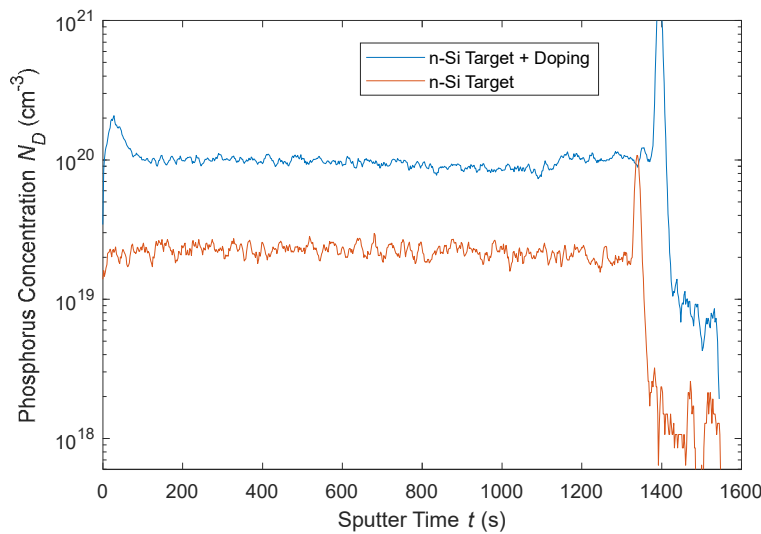
Figure 4.22: SIMS depth profile of the phosphorus concentration of two samples with 500 nm Si on 4H-SiC. Both are sputter-deposited from a highly phosphorus doped target and PDA at 1000 °C for 2 h. The sample shown as the blue curve was additionally doped by a spin-on doping solution containing phosphorus.

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After deposition and PDA for crystallization, the samples were analyzed in SIMS. The depth profile for the boron-doped sample is depicted in Figure 4.21. It shows a constant doping profile with an average concentration of $9 \cdot 10^{19}$ cm^{-3}, and the same interface effect as the sample doped by diffusion. The results from the sample deposited from the phosphorus-doped target are given in Figure 4.22 by the orange curve. It shows an average of $2 \cdot 10^{19}$ cm^{-3}, which is in line with the lower bulk resistivity of the target. Because no lower resistivity target was available, the phosphorus-doped Si was additionally doped using a spin-on solution with a drive-in at 1000 °C for 2 h. Doing so, an even distribution of about $9 \cdot 10^{19}$ cm^{-3} was achieved.

4.4.3 Contact resistance measurements

First experiments showed that it is possible to measure Si/4H-SiC HJDs by probing the top Si contact directly with a needle, but the contact resistance is high and influences the overall series resistance too much. Therefore, additional metallization of the Si-contact was necessary. To evaluate the contact resistance of a metallization on the Si, the CTLM structure was used. Although the tunnel current will be dominant for such high semiconductor doping concentrations, the metallization was selected to result in a low SBH to the silicon. On p-type Si, Mo was used as metallization, and on n-type Si, Hf.

The contact resistance was measured using the CTLM method with CTLM structures with ring spacings between 50 and 450 µm as described in 3.3.1. For the Mo/p-Si samples also the influence of the Si-film thickness between 250 and 1500 nm was investigated. The p-Si was sputter-deposited from the boron-doped target. Figure 4.23 shows IV measurements between two Mo pads on p-Si to confirm the linear IV characteristic. As can be seen, on both, the thin and the thick p-Si films, the Mo metallization results in a linear, and therefore ohmic IV characteristic. The results of the CTLM evaluations are depicted in Figure 4.24. Shown are results for different PDA temperatures and environments. All samples show a trend towards a decrease of both specific contact resistivity and semiconductor resistivity with increasing film thickness. This may also be attributed to an enhanced carrier mobility with film thickness. Not much difference on both resistivity parameters between the different annealing conditions is observed, except for the sample annealed at 900 °C in vacuum exhibiting a film resistivity above average. For all further device fabrications, the annealing was performed at 1000 °C under vacuum in
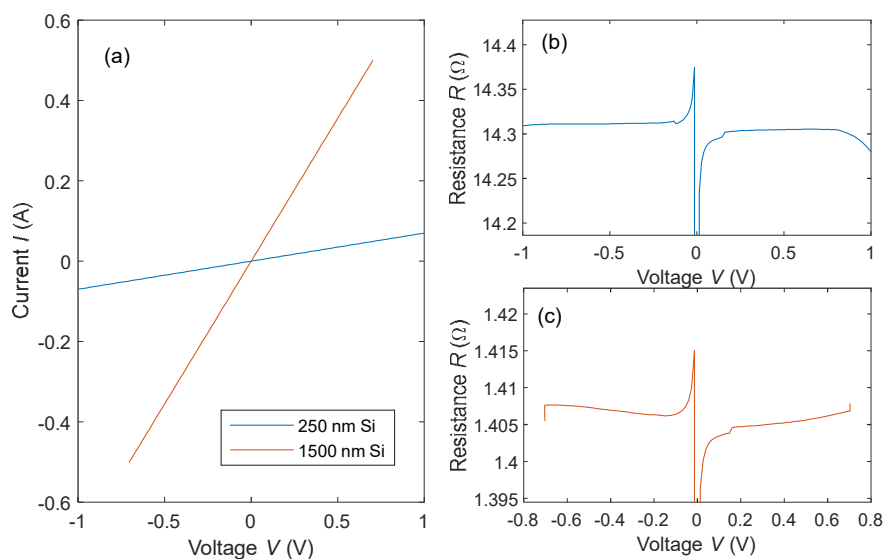
Figure 4.23: (a) IV measurements and extracted resistance (b,c) measured between two Mo contacts on p-Si of 250 and 1500 nm thickness.
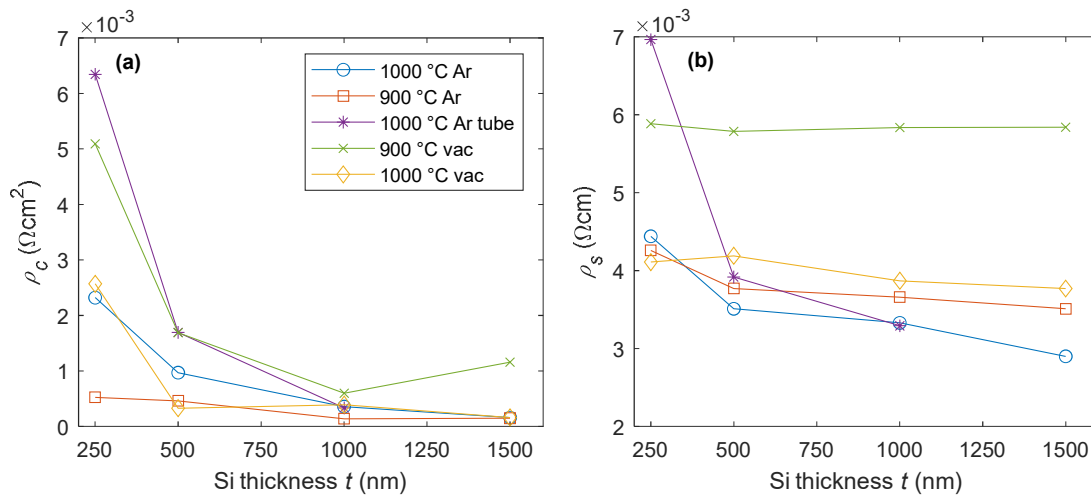
Figure 4.24: Specific contact resistivity ρ_c (a) and film resistivity ρ_s (b) of Si-films on 4H-SiC sputter-deposited from a highly boron doped Si target over Si film thickness, for different PDA conditions. The 1000 °C Ar tube sample was annealed in a quartz tube furnace, the others in an RTA oven.

an RTA equipment. Again, using Equation (4.1) and a mobility in the range between 3 and 10 cm^2/Vs results in a carrier concentration between $1.6 \cdot 10^{20}$ to $5.5 \cdot 10^{20}$ cm^{-3}. For the actual diode fabrication, the Si film was at least 500 nm thick, and the contact resistance is, therefore, less than 100 mΩ for metallizations with 700 µm diameter.

The specific resistance was also evaluated for Hf/n-Si contacts. Using the n-Si without additional spin-on doping did not result in a contact resistance being low enough. Therefore, for diode fabrication, the n-Si was sputter-deposited from the n-Si target and was additionally doped by diffusion. A specific contact resistance on 700 nm thick Hf/n-Si samples was measured to be $2.2 \cdot 10^{-3}$ Ωcm^2, being higher than the p-Si contact resistance, but still acceptable for diode characterization. The semiconductor resistivity was extracted to be $39 \cdot 10^{-3}$ Ωcm.

In summary, Si-films with a high doping concentration of either n- or p-type could successfully be prepared by either spin-on doping and diffusion or by sputter-deposition from a pre-doped sputtering target. For n-type Si-films the doping concentration from the doped target was not sufficient to provide good electrical contact, therefore these samples require an additional doping step by spin-on diffusants. The concentration was measured by SIMS and verified electrically using VDP and CTLM, resulting in overall good agreement between the methods. CTLM also confirmed low resistance ohmic contact of Mo to p-Si and Hf to n-Si, for use as a top contact material for final diode preparation.

5 Metal-induced crystallization of Si on 4H-SiC

Due to the high solid-phase crystallization temperature of Si, a direct crystalline deposition requires quite a high temperature, usually in excess of 600 °C [224], [225]. As has been shown in the sputter experiments, even at the highest substrate heating power, which equals a temperature of about 400 °C, only amorphous Si could be deposited. MIC could be an approach to reduce the temperature budget, thus allowing crystalline growth or a post-deposition crystallization at a much lower temperature. It is widely used in the industry as a cheap alternative to high-temperature processes, but also epitaxial films can be realized with MIC [158]–[160].

5.1 MIC experiments *in-situ* the sputter-deposition chamber

The beneficial properties of some metals on the crystallization temperature of most semiconductors are well known [148], therefore the usage of a "seed-layer" was evaluated in a first experimental series. The idea was to use a thin layer of a metal, acting as a crystallization agent to lower the crystallization temperature of Si, to be able to sputter-deposit crystalline Si *in-situ* using the integrated heater at about 400 °C.

The first series consists out of 16 samples, where several parameters have been altered. For the seed-layer the two most commonly used non-compound forming metals Al and Au [148], [152] have been used with layer thicknesses of 10 and 100 nm, deposited on a well cleaned 4H-SiC wafer on the C and Si-face in unheated condition. Directly after the metal deposition, the samples were heated to about 400 °C, followed by a deposition of Si. The Si layer was chosen to be 100 nm, but two different deposition powers of 50 and 500 W were used. This results in deposition rates of about 0.125 and 1.25 nm/s and, hence deposition times of 800 and 80 s, respectively. The deposition rate is believed to make a difference, as the rate of crystallization will most certainly be the limiting process, as a higher flux of incoming Si might be counterproductive. The fabricated films were investigated with XRD and SEM. The 2θ-scans of the samples with Al-layer are depicted in Figure 5.1 and those with Au in Figure
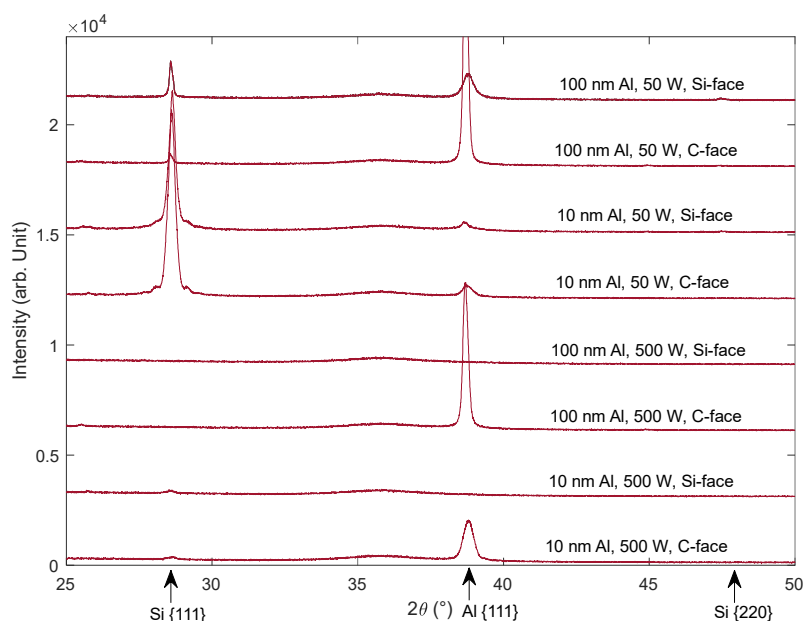
Figure 5.1: XRD diagrams (2θ-scans) of Si samples sputter-deposited at 400 °C on an Al seed-layer.
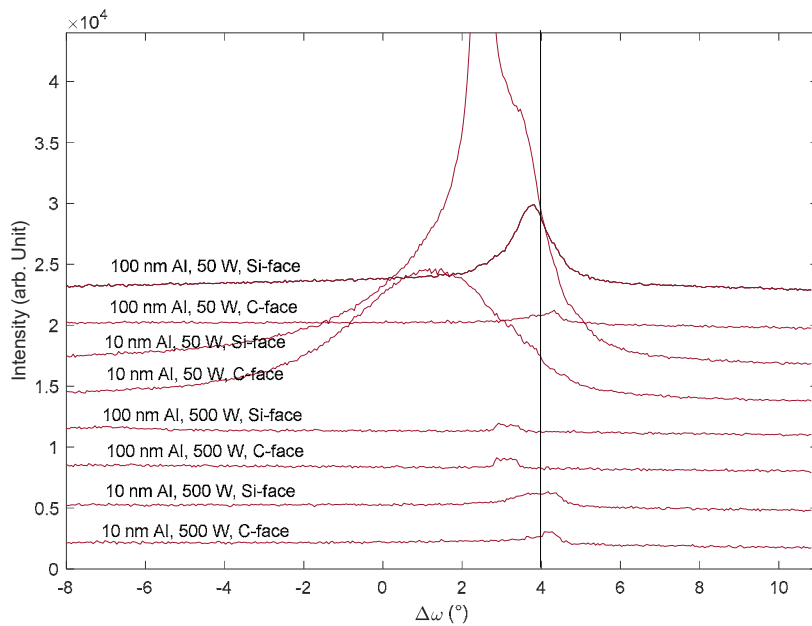
Figure 5.2: Rocking curves (ω-scans) of Si samples sputter-deposited at 400 °C on an Al seed-layer. The rocking curves are performed at the Si{111} diffraction angle.

5.3. The lack of any 4H-SiC peaks is because the samples were not recorded spinning, but were oriented in a way that the 4H-SiC{-1-120} plane is parallel to the source/detector plane. Additionally, rocking curves (ω-sweeps) were measured on the Si{111} diffraction angle. The scans are shown in Figure 5.2 and Figure 5.4 for Al and Au, respectively. Starting the discussion with the Al-layer samples, using the high Si deposition power of 500 W, no distinct Si-related peaks are visible, except the very weak diffractions of Si{111} using 10 nm Al thickness. What further strikes, is the absence or weakness of the Al{111} peak on the samples deposited on the Si-face. This can be attributed to the same reason no
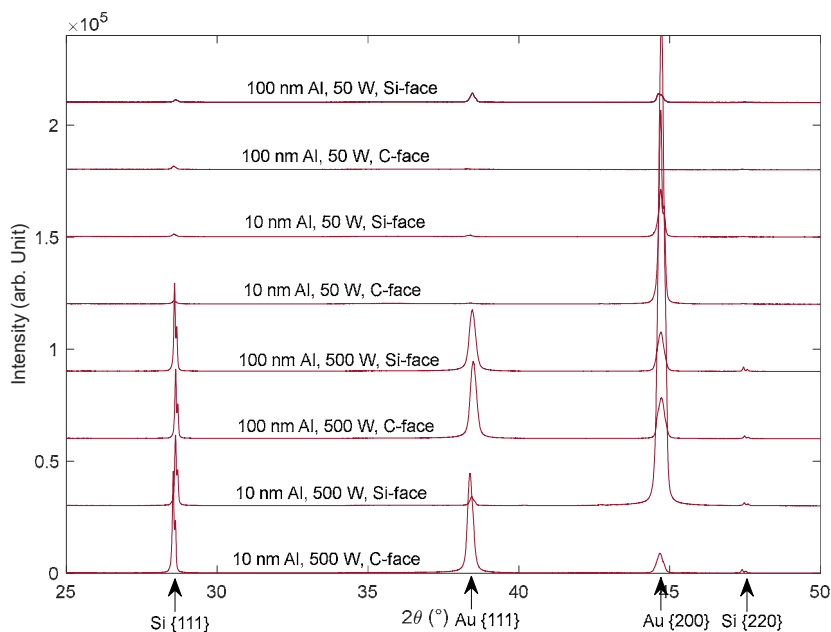
Figure 5.3: XRD diagrams (2θ-scans) of Si samples sputter-deposited at 400 °C on an Au seed-layer.

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4H-SiC peak is visible. This means the Al is oriented in the same direction as the substrates c-axis, hence a substrate-oriented growth of the Al on Si-face SiC is assumed (this will be confirmed later). Using the lower deposition power, giving the incoming Si atoms more time to diffuse through the Al, sharp Si{111} peaks are found. Especially using 10 nm Al, a strong Si{111} and no Si{220} diffractions are found on both SiC faces. Although all signals appearing in this diagram are from lattice planes that are not substrate oriented, the rocking curve measurements of Figure 5.2, also give information about the oriental distribution of the Si. The samples using 500 W show no signal except for the artifact of the substrate around 4°, confirming the absence or random texture of any crystalline Si. At 50 W power, the rocking curves show that the Si grains on C-face are not substrate oriented. On Si-face the ω-peaks are shifted towards 4°, indicating some orientational preference. The lack of the substrate orientation of the C-face might also be due to the lower surface quality of the C-face preparation. The Si-face is chemical-mechanical polished and the C-face optical polished.

Using Au as seed-layer, the diffraction patterns differ a lot. Now, very sharp Si{111} peaks, clearly showing the double peak, representing the X-ray spectra, are observed using the high deposition power of 500 W. Using 50 W, the Si{111} peaks are barely visible using the same scaling. Another important difference is the dominant orientation of the Au film. At 500 W Si deposition, and therefore a shorter time at elevated temperature, the Au is <111> and <200> oriented. After the longer heat treatment using 50 W, the Au almost completely changed its texture to {200}. A similar change in the preferred orientation of Au was also observed using *ex-situ* annealing, which is shown later. This texture change, and also the reduced Si signal at this low Si deposition power might be attributed to the longer time at high temperature. At the low power, the sample will certainly be longer at temperatures exceeding the metal-semiconductor eutectic temperature of the Au/Si system of 363 °C [262]. Above this temperature, the creation of a eutectic melt is likely, which will result in a different diffusion and recrystallization process of both, the Au and the Si. The rocking curves of the sample with Au seed-layer confirm a dominant Si{111} signal at the high deposition power and a flat response at low power. The rocking curve peaks are centered around 0°, meaning random recrystallization and the lack of any substrate orientation, independent of the 4H-SiC face.
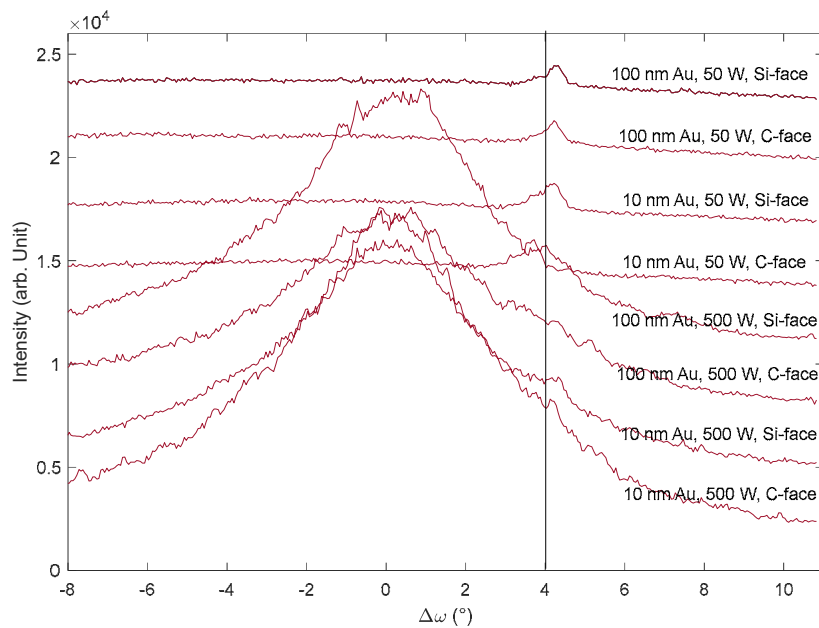
Figure 5.4: Rocking curves (ω-scans) of Si samples sputter-deposited at 400 °C on an Au seed-layer. The rocking curves are performed at the Si{111} diffraction angle.

SEM micrographs of some selected samples are depicted in Figure 5.5. The first three images show the surface of the samples using Al seed-layers and Si deposition at (a) 500 W and (b and c) 50 W. A clear difference in the surface structure is visible. Using 500 W only some small regions of brighter color and undefined shape are present. Using 50 W, the same bright regions are larger and show a more defined shape. A close-up of one of these bright spots is shown in (c). EDX analysis showed the bright, often hexagonal structures, to be mainly Al. The surrounding shows a dominant Si signal. It appears like the underlaying Al is working its way through the growing Si film, similar to the well-known layer exchange
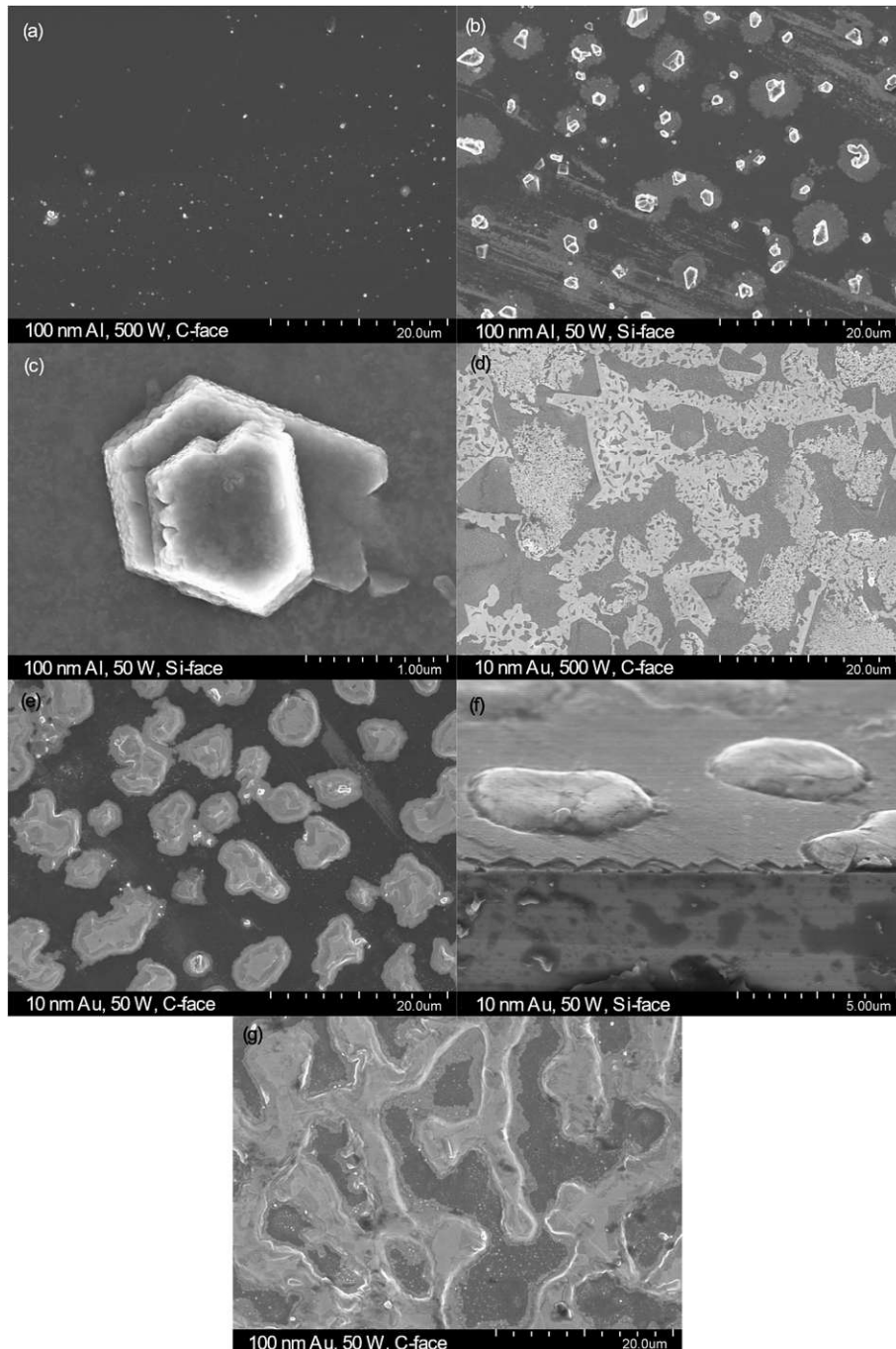
Figure 5.5: SEM micrographs of some selected samples with (a-c) Al and (d-g) Au seed-layer. 100 nm Si was sputter-deposited at 50 or 500 W sputtering power during substrate heating at 400 °C.

process. But the Al is not forming a layer but reorganizes itself to several hundred nm high mostly hexagonal-shaped structures, or pyramids.

The surface structure of the samples with Au seed layers of different thickness and Si deposition powers are shown in Figure 5.5d-g. Using 500 W, the XRD showed almost no crystalline Si and the Au being present in both, <111> and <200> orientation. In the SEM micrograph (d) the sample shows an irregular sheet of Au, with many openings being on top of a layer that is assumed to be mostly a-Si. A completely different appearance is found using 50 W, confirming the different XRD results. The surface clearly shows roundish islands, which appear like they have been liquified and then frozen. EDX indicated these islands to be Au and the surrounding being Si. The last image (g) shows the sample using 100 nm Au and 50 W, indicating the thicker Au layer resulted in a denser coverage of Au on the surface.

The conducted experiments show that the temperatures reached using the *in-situ* substrate heater of the sputter equipment was sufficient to initiate Si recrystallization during deposition. Apart from the temperature, many parameters, like the layer thicknesses and the deposition rate of the Si are crucial for further improvements. Due to the unsatisfying film quality, no further investigations regarding the *in-situ* MIC process were conducted, but further focus was led on the well-known "*ex-situ*" MIC process. Nevertheless, the results indicated it is possible to deposit crystalline Si at relatively low temperatures (<400 °C) in a sputtering equipment with "seed-layers".

5.2   *Ex-situ* MIC experiments

Parts of this chapter have been published in [263] *and* [264].

Metal-induced crystallization with non-compound forming metals like Al, Ag or Au, is known to initiate a metal-induced layer exchange. As first results of *in-situ* MIC indicated an onset of a layer-exchange and at least on Si-face 4H-SiC also signs of epitaxial recrystallization, experiments with bi-layers of metal/a-Si followed by an annealing step were conducted.

For all the following experiments 4H-SiC wafers from Cree with a 4° off-axis cut were used as substrates. An RCA clean was performed prior to deposition. A stack of metal followed by a-Si is DC-sputter-deposited with a power of 500 W on Si- or C-face SiC without breaking the vacuum. The
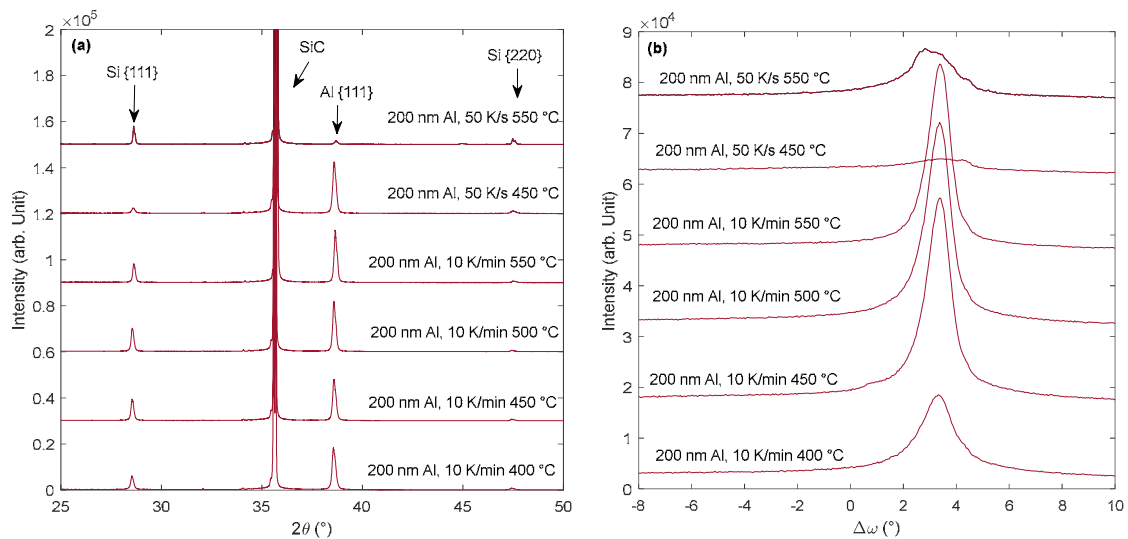
Figure 5.6: (a) XRD diagrams (2θ-scans) and (b) rocking curves (ω-scans) of samples with 200 nm Al / 200 nm a-Si subject to different annealing conditions. The annealing duration was kept constant at 1 h. The rocking curves are performed at the Si{111} diffraction angle.

annealing step to achieve crystallization was performed in a quartz furnace in Ar atmosphere. The furnace was evacuated prior to heating. From the high number of samples processed in the evaluation of the MIC process on SiC, some are presented in the following.

5.2.1 MIC using Al at various annealing conditions

Using *ex-situ* annealing, a wide variety of parameters is available that will influence the final result. To understand the influence of the annealing, the Al/a-Si ratio was kept constant at 200 nm / 200 nm. The XRD diagrams and rocking curves of some samples undergoing different annealing conditions e.g. different temperatures, heating rate, and duration are depicted in Figure 5.6 and Figure 5.7.

Between 400 and 600 °C annealing temperature, the XRD diagrams appear rather similar. At 350 °C, the Si signal is strongly reduced. At the highest temperature of 700 °C, the Si exhibits the strongest diffraction signal, but the Al signal changed strongly. It clearly undergoes a transformation from being dominantly <111> oriented to a random texture. This is indicated by the appearance of other Al related diffraction peaks. This can be attributed to the formation of a eutectic melt, like discussed before on the Au samples. The eutectic temperature of the Al/Si system is about 577 °C [265]. The heating rate, which was altered to be 2 K/min, 10 K/min, and 50 K/s, shows an influence on the recrystallization process. Lower heating rates seem to be beneficial to the crystallization process, similar to the solid phase crystallization of Si (see 4.2.2.). One sample was annealed for 10 h, instead of 1 h, showing no noticeable difference in the diffraction diagram. After an annealing step at 600 °C, the process might be finalized already after 1 h. Lower temperatures might require longer annealing times, as will be seen later. The rocking curves (ω-scans) of the Si{111} diffraction show all the Si grains to be oriented off the surface normal (0°) but tilted towards the off-axis orientation of 4°. The peak center which is slightly off the 4° angle might be attributed to the Nagai tilt [266] being a direct consequence of the different c-axis lattice constants. The difference in signal strength correlates to the signal intensity of the 2θ-scans.

Figure 5.8 shows a TEM image of a sample after 600 °C annealing together with an EDX elemental map to identify the Al and Si regions. In the TEM image, several grains are clearly detectable. No more amorphous regions were found anywhere on the sample. Also, no complete layer exchange is observed,
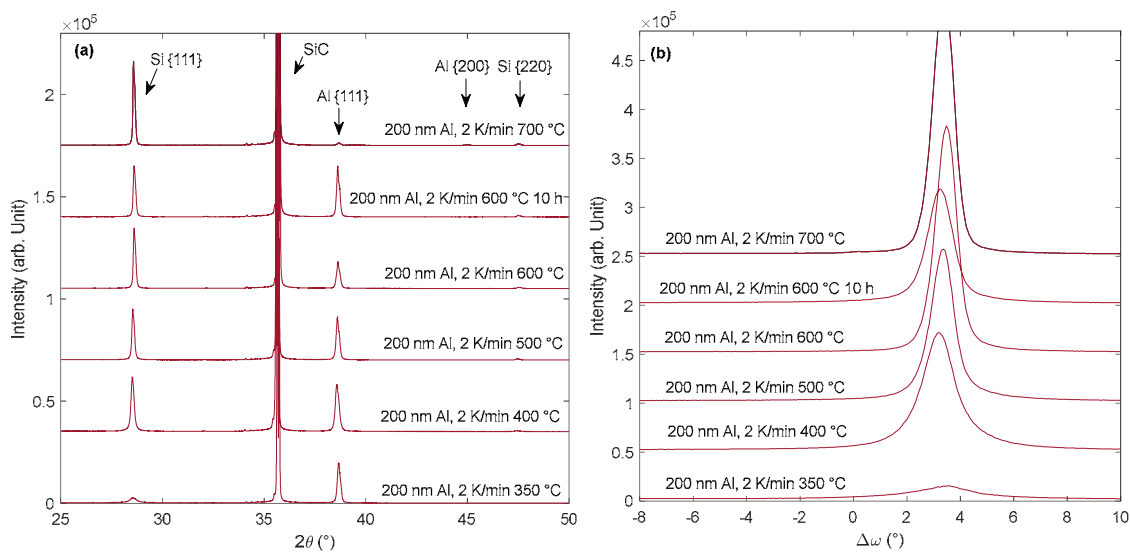
Figure 5.7: (a) XRD diagrams (2θ-scans) and (b) rocking curves (ω-scans) of samples with 200 nm Al / 200 nm a-Si subject to different annealing conditions. Except one sample the annealing duration was kept constant at 1 h. The rocking curves are performed at the Si{111} diffraction angle.
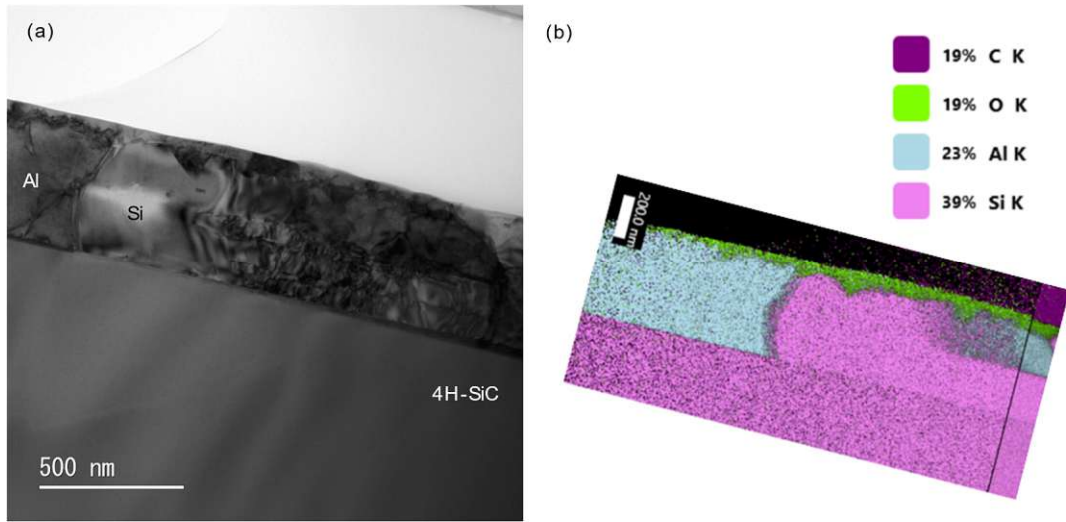
Figure 5.8: (a) TEM image a sample annealed at 400 °C for 1 h at 2 k/min. (b) EDX elemental map of approximately the same position.

as some grains are expanding across the whole film thickness. After performing EDX measurements the left part of the TEM image turned out to be Al, and the large bright grain being Si. Further right a more complete layer exchange is found by the interface region being Si with Al on top. The whole surface is covered by a layer with high oxygen content. Although annealing was performed in Ar atmosphere, residual oxygen must have reacted with the Al or a-Si, forming this layer.

To further study the influence of the MIC process on 4H-SiC using Al, the influence of the substrate face was investigated. A stack of about 300 nm Al and 300 nm a-Si was sputter-deposited with a power of 500 W on Si and C-face SiC without breaking the vacuum. The two surfaces are of different qualities, the Si-face is chemical-mechanical polished, and the C-face optical polished. Annealing was performed at 400 °C for 2 h with a ramp of 2 °C/min.

XRD measurements of *as-deposited* and annealed samples are shown in Figure 5.9a. The *as-deposited* samples only show the substrate peak of {0001} 4H-SiC and a strong {111} Al peak. After annealing at 400 °C three Si related peaks appeared on both faces. The {111} texture is by far the most pronounced, indicating an oriented crystallization and no polycrystalline microstructure. The FWHM is measured to about 0.11° for Si and C-face SiC, respectively. To further investigate the orientation of the crystalline Si in respect to the substrate, rocking curves of both the {111} Si and the {111} Al peaks were done and are shown in Figure 5.9b and c. For these measurements, the sample was oriented such that the 4° off-axis <1120> direction is either parallel or perpendicular to the scan axis. The rocking curves of the *as-deposited* samples only give an Al related peak with an FWHM of 0.7° in <1100> direction and 1° in <1120> direction indicating an epitaxial growth of Al{111} during sputter-deposition. After annealing, the Si{111} rocking curves show distinctive peaks, centered at $\Delta\omega = 0$ and $\Delta\omega = 3.7°$ for the Si-face and at $\Delta\omega = 0$ and $\Delta\omega = 2.6°$ for the C-face sample. The fact, that the Si grows off-axis and not normal to the surface, as well as the dominance of the <111> orientation are regarded as strong indicators for heteroepitaxial recrystallization. As mentioned earlier, the slight shift from the 4° off-axis to 3.7° and 2.6° for the Si- and C-face might be explained by the Nagai tilt.

SEM images were recorded before and after annealing and are depicted in Figure 5.10. The *as-deposited* sample clearly shows two well-separated layers of Al and a-Si. After annealing an almost complete layer exchange was observed. In some areas, the Al is still connected to the SiC, which is also indicated by the presence of off-axis Al peaks in the rocking curves of the annealed samples. To complete the layer
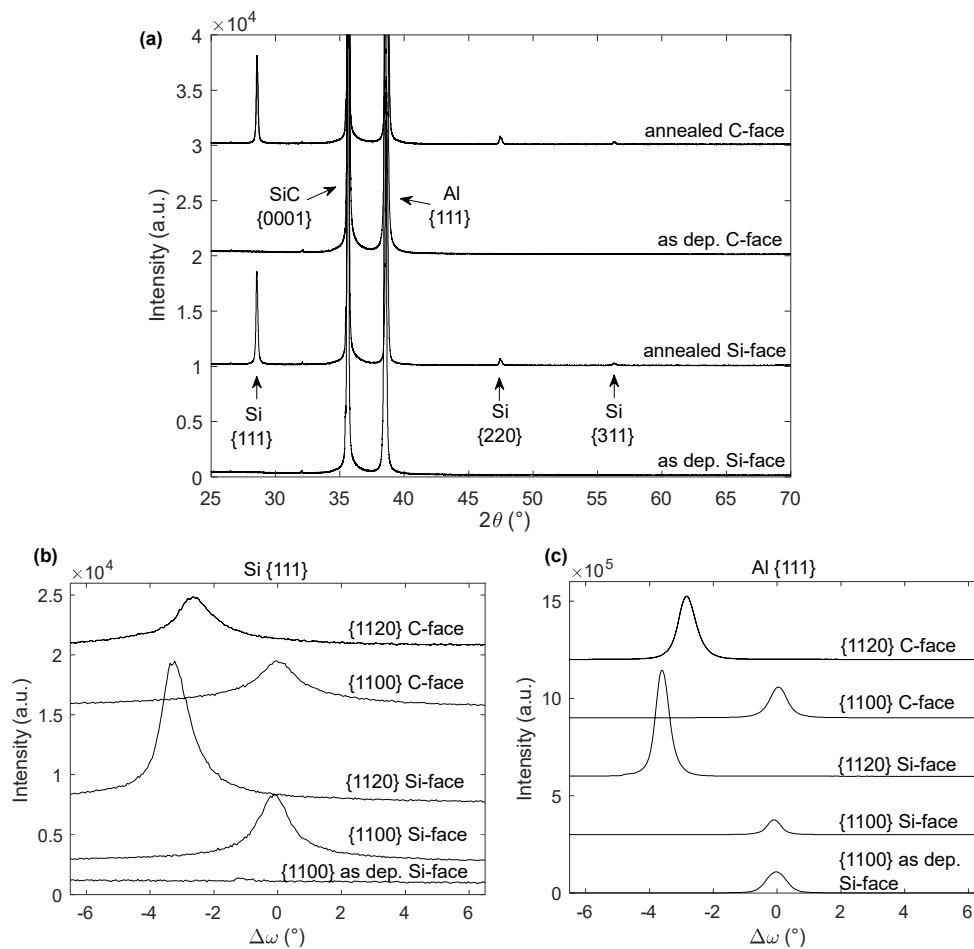
Figure 5.9: (a) XRD diagram (2θ-scans) of *as-deposited* and 400 °C annealed samples. (b) Rocking curves (ω-scans) of the Si{111} peak of the *as-deposited* and the annealed samples with the detector plane parallel and perpendicular to the off-axis direction. (c) Rocking curves of the Al{111} peak.

exchange, a different thermal treatment, or a variation in the film thickness ratio might be necessary. The samples on C-face SiC showed no notable difference in SEM imaging to those with a Si-face and are therefore not depicted.

No major difference was observed performing Al-induced crystallization experiments of Si and C-face 4H-SiC. This is in contrast to the *in-situ* MIC experiments where no orientational preference was found on the C-face. This difference is attributed to the not well-defined surface roughness of the C-face which may vary a lot between wafers. Nevertheless, no closed Si film, required for electrical contacts could be achieved on either side, requiring further experiments.

5.2.2 *In-situ* XRD annealing

To get more information about the temperature level where the Si crystallization starts, XRD measurements as a function of temperature were performed on both SiC faces.

To record XRD diagrams as a function of sample temperature an *in-situ* heatable chamber (Anton Paar HTK 1200N) was used equipped with a micromanipulator stage for correcting the height at elevated temperatures. Measurements were performed between 50 and 400 °C in 5 °C steps in He atmosphere. The heating rate was set to about 2.2 K/min.
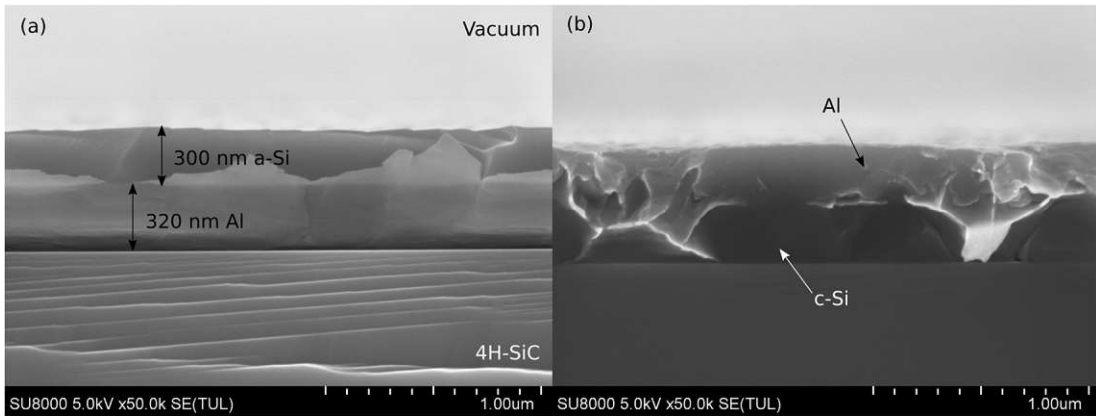
Figure 5.10: Cross-sectional SEM images on Si-face SiC. (a) As deposited sample. (b) Sample annealed at 400 °C.

Figure 5.11 shows color plots of the measured intensity (counts) over angle and temperature. The Si{111} peak was measured in the 2θ as well as in the ω regime to monitor orientational changes. The samples were mounted with the <1120> direction parallel to the scan-axis so that an off-axis epitaxial crystallization to the SiC should be visible. On both SiC faces, the presence of a peak starts to appear at about 220 °C. At around 360 °C, the peak starts to become much stronger on the Si-face and at about 350 °C on the C-face. This two-step crystallization has been observed before but the real cause remains unclear [148]. It is surprising that even at temperatures as low as 220 °C the silicon starts to crystallize on the SiC surface using the substrate as template. However, the silicon rocking curve peaks are rather broad, which can be attributed to the formation of islands rather than a closed film. It has already been shown that diffusion of Si atoms along Al GB occurs at temperatures below 200 °C [152] and that epitaxial growth of SiGe on Si substrates is achievable using MIC. It is reasonable to assume a similar process of GB diffusion followed by crystallization on 4H-SiC to be the involved process. A relative
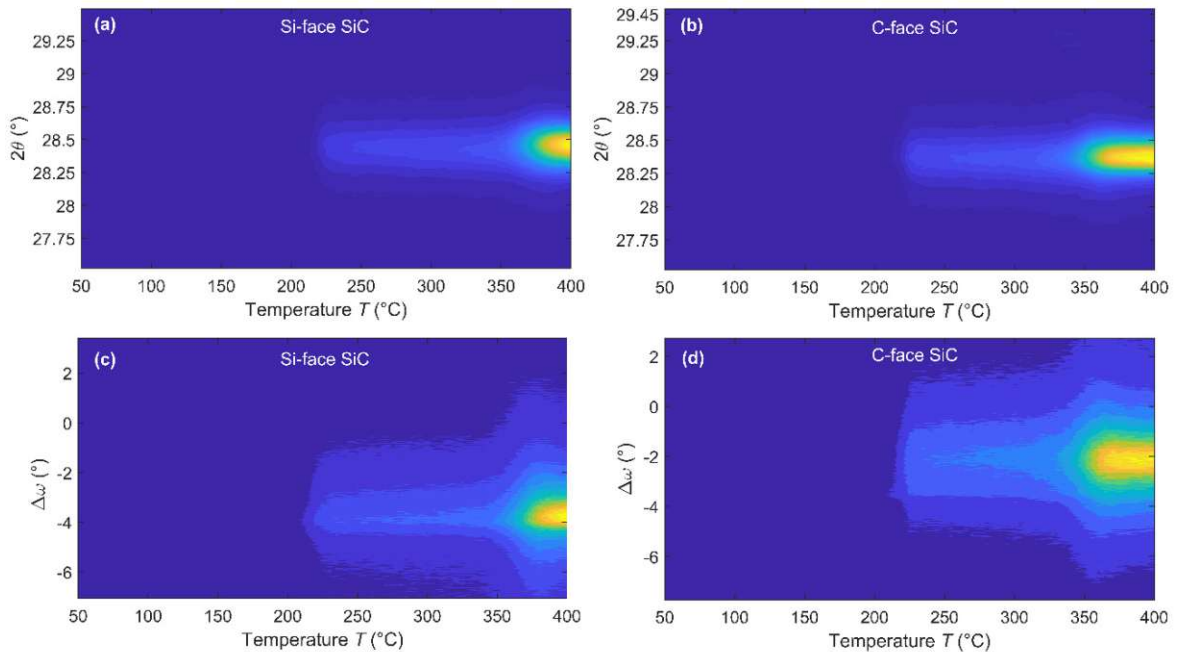
Figure 5.11: XRD measurements during *in-situ* heating. Scan axis is parallel to the <1120> direction (off axis direction). Brightness is linearly related to intensity. (a) XRD diagram of the Si{111} peak on Si-face SiC and (b) on C-face SiC. (c) Rocking curve of the Si{111} peak on Si-face SiC and (d) on C-face SiC.

low domain mismatch of 0.26% between Si{111} and 4H/6H-SiC{0001} could make an epitaxial growth possible at these low temperatures.

5.2.3   Al, Au, and Ag induced crystallization

Next, not only Al, but, three different non-compound forming metals, namely Al, Au, and Ag, were investigated in terms of their use as a crystallization agent for Si on 4H-SiC. All three materials have been extensively studied in combination with Si and Ge [149], [267]. In the previous experiments, the successfully low-temperature crystallization of Al/a-Si on 4H-SiC substrates using MIC was shown. *In-situ* XRD measurements indicated the onset of substrate-oriented crystallization at temperatures as low as 220 °C. Therefore, rather low annealing temperatures of 200 to 275 °C and rather long annealing times of 105 h have been chosen for the next set of experiments. One sample was annealed at a higher temperature of 600 °C, which is still under the SPC temperature of Si, but high enough for any MIC process to occur. The layer thickness was chosen to be 250 nm of metal and 250 nm of Si. Many publications reported on the optimal layer thicknesses and the ratios between metal and semiconductor [155], but it is rather challenging to find the optimal combination of thickness, ratio, temperature and time, to achieve a fully covering c-Si film [153], [268].

Figure 5.13 shows XRD diagrams (2θ-scans) along with rocking curves (ω-scans) of the most pronounced Si diffraction of the annealed samples. Figure 5.13a, representing the Al sample, shows a peak corresponding to Si{111} at temperatures as low as 200 °C. With increasing temperature this peak becomes more intense, as well as low-intensity Si{220} and {311} reflections start to appear. The ratios between the different peak intensities indicate a strong dominance of the <111> orientation. This strong diffraction signal was also used to perform the rocking curves shown in Figure 5.13d. A clear orientation, towards the SiC<0001> (c-axis) direction, corresponding to about 4° off the surface normal is observed. Although a layer exchange is possible at 600 °C, being higher than the eutectic temperature of the Al/Si system (~577 °C), the formation of a Si network in the top Al layer is likely [265].

In Figure 5.13b and e, the results for the sample applying Au as catalytic metal are shown. Despite the rather huge signal of the Au layer, small Si{220} diffraction signal are observed after 200 and 225 °C, with a strong increase starting at 250 °C. At this temperature, also the Au-film starts to change its crystallographic orientations. The corresponding rocking curve of the {220} Si peak shows a slight orientation towards the off-axis direction, but it is diminishing with higher annealing temperatures. Although the Au-Si system does not have any stable compound phases in this temperature range, it will form metastable phases of e.g. Au_3Si during annealing, being responsible for MIC processes happening at such low temperatures [152], [269]. Starting at 250 °C, the sample also changed its surface color to gold, indicating that a layer exchange has occurred [270]. Closer investigation after removing the gold reveals no fully covering c-Si film, but rather large, several µm thick islands of c-Si. At the highest conducted annealing temperature of 600 °C, which is substantially above the metal-semiconductor eutectic temperature of the Au/Si system of 363 °C [262], only an incomplete layer exchange was observed. The XRD data also indicated a change from an initially strongly <111> oriented Au layer to several dominant orientations. In addition, the ω-distribution of the Si{220} and Si{111} (not shown) indicates the lack of any substrate-induced orientation. Similar results of an incomplete layer exchange of the Au/Si systems annealed at temperatures above the eutectic temperature have been published before [270]. The formation of a eutectic melt will most likely hinder the grain boundary diffusion of a-Si to the interface and thus, the subsequent layer exchange. Due to this finding and the fact that Au is
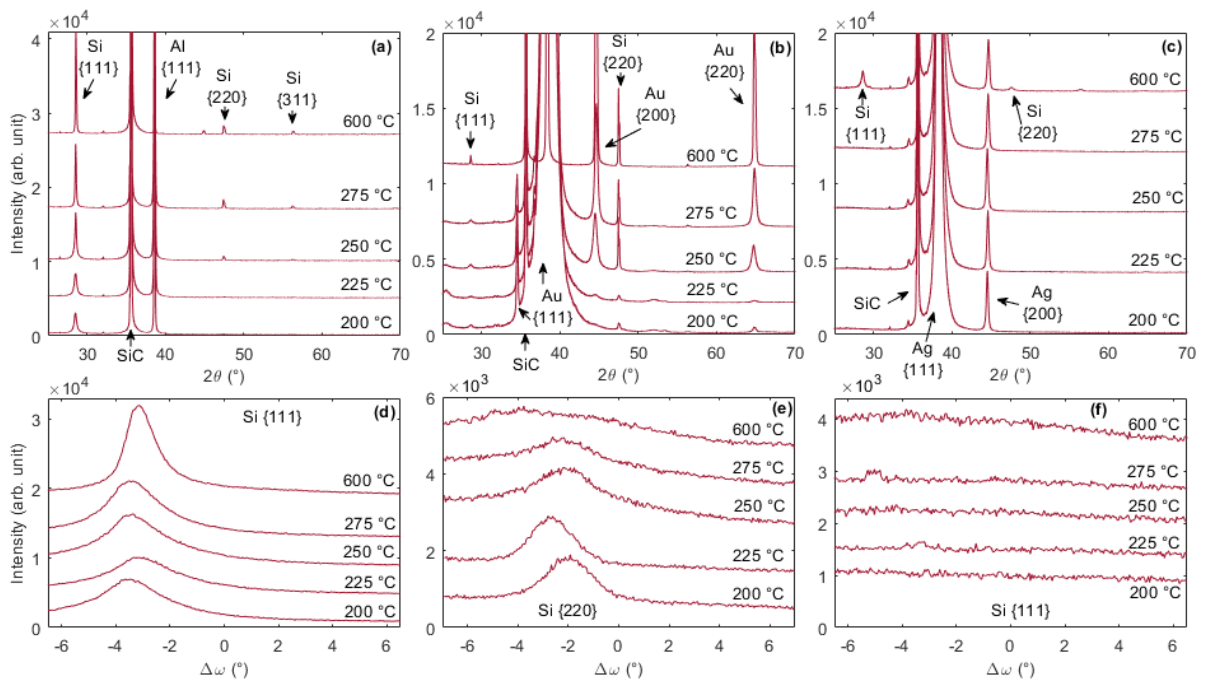
Figure 5.13: XRD diagrams after various annealing temperatures, whereas in (a) Al (b) Au and (c) Ag serves as catalytic metal. The lower Figures depict rocking curves of the strongest Si peak for each metal catalyst. (a) Si{111} rocking curve of Al sample, (b) Si{220} rocking curve of Au sample and (c) Si{111} rocking curve of Ag sample.

absolutely not complementary metal oxide semiconductor (CMOS)-compatible, as it generates a deep-level recombination center in Si, Au is ruled out for further investigations.

Finally, Ag was investigated, shown in Figure 5.13c and f. With about 400 °C the crystallization temperature of a-Si in contact with Ag is rather high compared to Al and Au [152], [271]–[273]. This is confirmed by the absence of any crystallized Si regions at low temperatures. Only the sample annealed at 600 °C showed several Si related peaks. Their relative intensities indicate a rather polycrystalline texture. This is in line with the absence of any preferred orientation of the Si{111} peak in the rocking curve measurements.
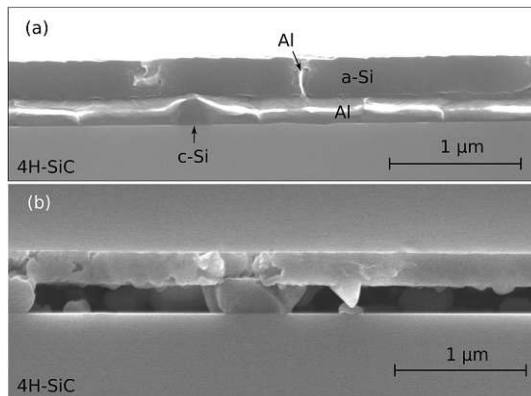
Figure 5.12: Cross-sectional SEM images of the sample using Al and 250 °C annealing temperature. (a) original, (b) after Al etching.

The results gained so far from the pre-investigations on MIC performance using these three different metals clearly favor the use of Al. Well-oriented c-Si at very low temperatures could be demonstrated. Additionally, Al acts as a good p-dopant for silicon with no defect centers having energy levels deep in the band gap. The amount of electrically active dopants was found to be below the actual Al concentration and can be influenced via the MIC temperature [153], [274], [275]. Post deposition annealings at higher temperatures can lead to an almost full ionization of the Al [276]. Due to the above reasons, further investigations of MIC on 4H-SiC are focusing on Al as catalytic metal. For microstructural investigations, one Al sample was prepared in cross-sectional view for SEM analysis. In Figure 5.12 the sample annealed at 250 °C is shown with Al (a) and after etching the Al in H_3PO_4 (b). The image clearly shows that the crystallization and hence the layer transfer was not completed yet. Some crystalline Si parts are already visible on the 4H-SiC surface, as well as some Al clusters in the a-Si. After etching the Al, a clearer view of the crystallization progress is possible. At many locations, c-Si islands began to form where originally the Al film was, leaving behind voids in the film above. Most of the remaining upper film can be assumed to be amorphous, however, there is evidence of the onset of crystallization at the previous Al/a-Si interface. To get even more insight in the process, a sample was prepared for TEM after 24 h annealing at 275 °C. Two regions of the film are shown in Figure 5.14. The microstructure is similar to the SEM image, but this time the Al was not etched. Some things are worth mentioning. Most of the Al is still present as a uniform film on the SiC surface and most of the Si is still in its amorphous phase, confirming the thermal budged was insufficient to complete the crystallization process. Especially in Figure 5.14a, the onset of layer exchange is visible. A large portion of Al was replaced by Si. The process of diffusion along grain boundaries, subsequent growth of the Si grain, and stress-induced rejection of the Al were already discussed in the theoretical part, but here it is clearly visible. But a second site of crystallization is visible. Next to the black "Si" label also crystalline growth of Si is happening. As will be seen later when dealing with very thin Al layers, small parts of Al are lifted from the film diffusing through the a-Si leaving behind c-Si pillars. This will result in a network of c-Si on top of a semi-closed c-Si film after Al removal. One possibility that might prevent this effect is the insertion of a thin oxide layer between Al and a-Si [149], [277].

The thermodynamic procedure of MIC indicates that the microstructure of the metal layer has a major effect on the final result. Most MIC experiments are performed on glass or other amorphous substrates
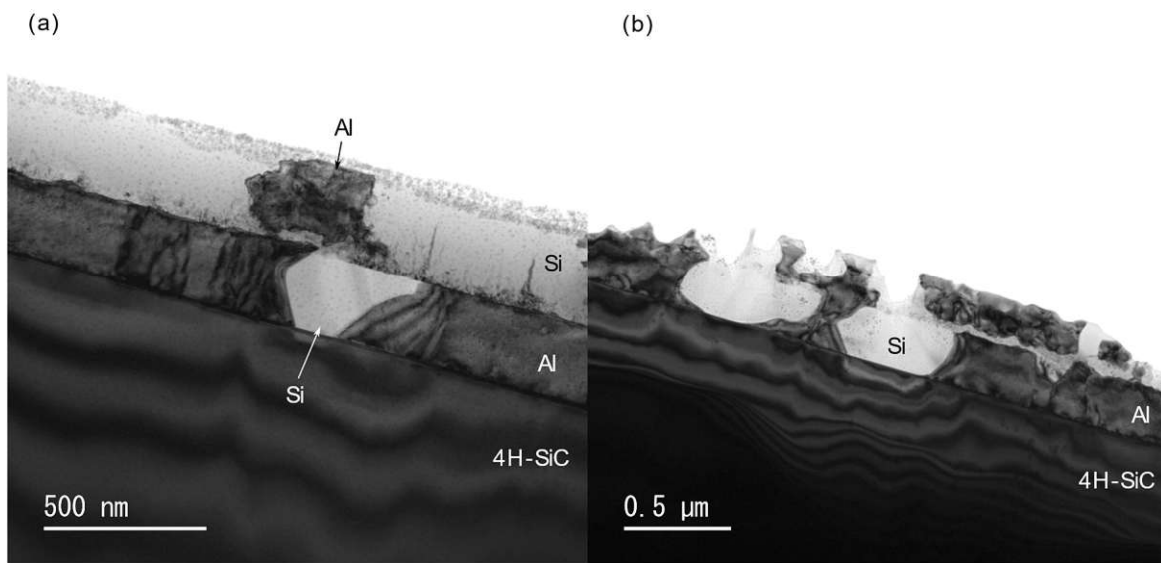
Figure 5.14: TEM micrographs of a sample with 250 nm Al and 250 nm a-Si annealed at 275 °C for 24 h.

often resulting in polycrystalline metal layers without any texturing. If crystalline substrates are used, a biaxial or even epitaxial growth of the metal can occur.

To further investigate the influence of the metal microstructure on the MIC process, the orientation of the *as-deposited* metal films on the 4H-SiC substrate is investigated using XRD rocking curves, and the Al/4H-SiC interface is additionally investigated by TEM. Figure 5.15(a) depicts the (ω-scans) of Al, Au, and Ag using the {111} reflection. Despite the Ag sample, the *as-deposited* metals only exhibit the {111} peak in XRD diagrams. The Ag{111} and Ag{200} peaks exhibit 2θ FWHMs of 0.161° and 0.270°, whereas the <111> orientation has a 200 times higher intensity than the <200> orientation and was therefore selected for ω-scans. The peaks in the rocking curves show a well-oriented Al film with an FWHM of 0.8°, an Au film, with a low degree of texturing and an FWHM of 3.6° and an Ag film without any substrate orientation and a rather large FWHM of 7.5°. All three metals have the same face-centered cubic (FCC) structure and almost identical lattice constants of 4.046 Å, 4.065 Å, and 4.079 Å, for Al, Au, and Ag, respectively [278]. The much higher sputter rate of the heavy elements Au and Ag compared to Al might be a reason for the weak orientational growth [279].

Despite the lattice mismatch of about 7% between Al(110) and 4H-SiC(1100) a highly textured, almost epitaxial film could be grown as visible in Figure 5.15b. The SAED pattern in Figure 5.15c confirms the epitaxial connection by showing both, the reflections of the Al and the substrate.

To summarize this section, the MIC process has been evaluated at rather low temperatures applying Al, Au, and Ag. Only the Al metal showed rather well oriented and preferentially Si<111> crystallization already at 200 °C. SEM investigations revealed no completion of the crystallization process even after 105 h of annealing. The good orientation of the Si grains obtained using Al is attributed to the very crystalline epitaxial growth of the Al on 4H-SiC.
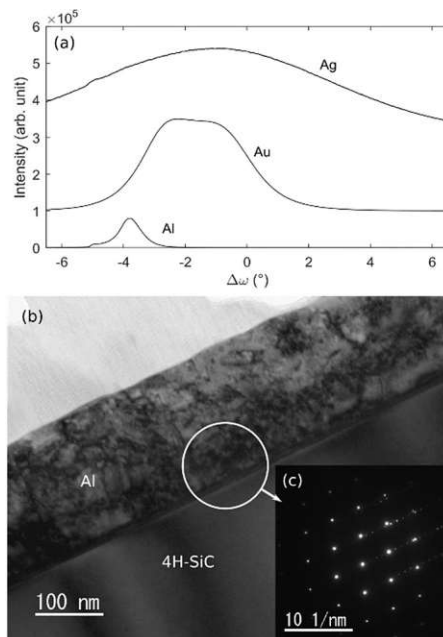
Figure 5.15: (a) XRD rocking curves of the different a-Si/metal bilayers prior to annealing. (b) TEM image of the Al/4H-SiC interface prior to annealing. (c) SAED pattern of the marked region.
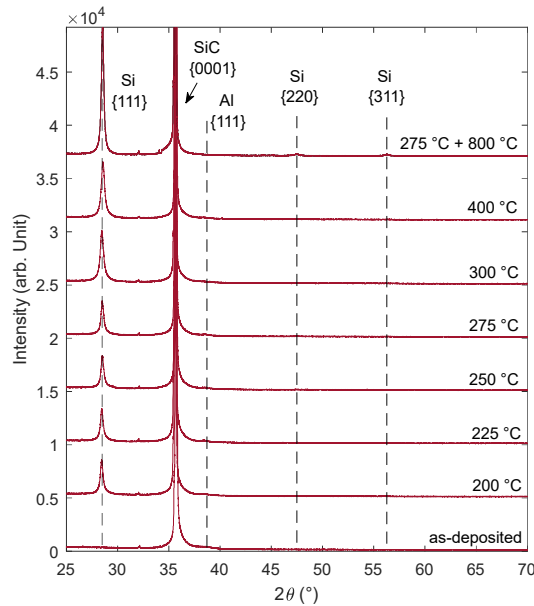
Figure 5.16: XRD diagram of Al/Si bi-layers (10 nm/250 nm) in the *as-deposited* state and after various annealing temperatures. Annealing times were 105 h for low temperatures and 24 h for the second annealing step at 800 °C.

5.2.4   Al-induced crystallization using very thin Al layers

Due to the incomplete crystallization and large amounts of remaining Al on the SiC interface, a sample run with very thin Al layers was prepared. The 10 nm Al, 250 nm a-Si bi-layers were fabricated by sputter-deposition and annealed at temperatures between 200 and 300 °C, as well as at 400 °C for 105 h. One sample was annealed at 275 °C for 105 h, followed by an annealing step at 800 °C for 24 h. The second, high-temperature annealing step was used to crystallize any remaining a-Si by SPC. The idea behind using very thin Al layers is to allow a-Si to diffuse down to the SiC substrate and crystallize at the interface or in Al-GBs close to the interface. In thick Al layers, a major part of the crystallization will happen in Al-GBs far above the substrate, working its way down by sequential stress-related replacement of Al by c-Si [169].

XRD diagrams of the *as-deposited* and annealed samples are depicted in Figure 5.16. The measurement results look quite similar to those presented in Figure 5.13a using 250 nm Al and 250 nm a-Si. A closer look reveals no signs of other Si peaks than the Si{111}, whereas the previous run showed the appearance of other orientations starting at 250 °C. Only the sample which was annealed a second time at 800 °C displays very weak Si{220} and Si{311} reflections, which is not surprising giving the fact that 800 °C is high enough to trigger random nucleation and grain growth anywhere in the remaining a-Si. Nevertheless, with a peak ratio of 97.44% {111} to 1.32% {220} to 1.24% {311}, the sample annealed twice is very well <111> oriented with few randomly orientated polycrystalline regions. One also notices the absence of any Al-related peaks. Only in the *as-deposited* state and at low annealing temperatures a slight bulge in intensity at the expected Al{111} diffraction angle is visible. This can be attributed to the low density of Al, being not able to reflect enough X-rays with only 10 nm thickness. Also, the strong signal from the SiC bulk expands beyond the position of the expected Al diffraction angle, giving rise to a higher background intensity, covering almost any Al signal. After annealing some Al is dissolved in the Si and some Al grains are expected to be tilted leaving even less Al{111} to be measurable.
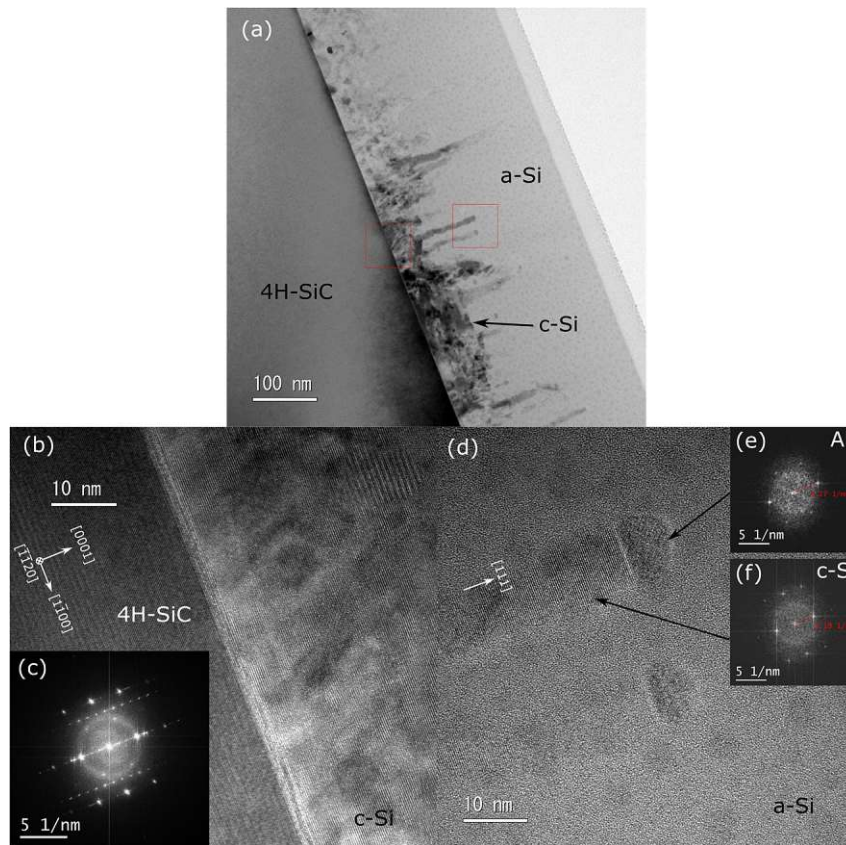
Figure 5.17: TEM images of the sample with 10 nm Al and 250 nm Si annealed at 225 °C for 105 h. (a) low magnification TEM image with two red squares indicating the region where the HRTEM images (b) and (d) were taken. (b) HRTEM image from the interface region, (c) FFT diffraction pattern of (b). (d) HRTEM image of c-Si rods growing out of an Al grain along with FFT diffraction patterns of the Al and the Si parts.

In order to gain a deeper insight into the microstructure and the completeness of the MIC process, the sample annealed at 225 °C was prepared for TEM analysis. In Figure 5.17a a low magnification TEM image of the annealed film is depicted, clearly showing that only about one-third of the film is completely crystallized. There is no smooth boundary between c-Si and a-Si, but narrow, elongated pillars of c-Si can be seen starting from a continuously crystallized region. It is very similar to the
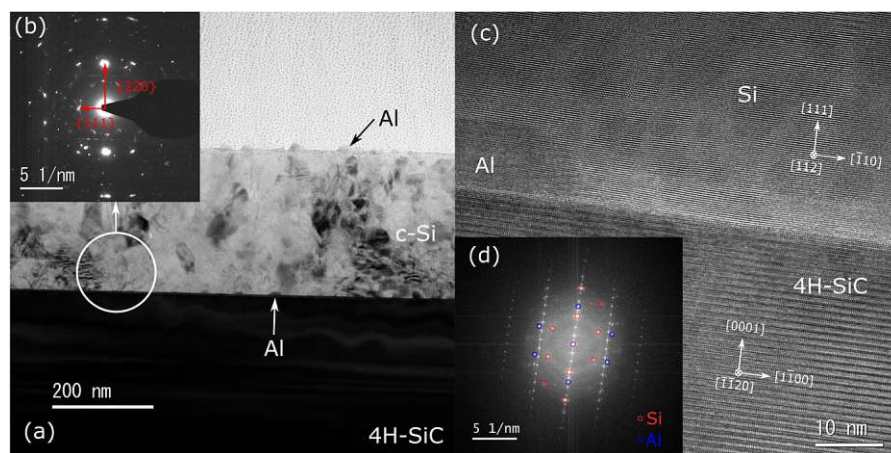
Figure 5.18: (a) TEM image of the sample which underwent a second 800 °C 24 h annealing step. (b) SAED pattern of the marked region. (c) HRTEM image of the interface region with the corresponding FFT diffraction pattern in (d).

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crystallization on top of the thicker Al layer shown in Figure 5.14, but using the very thin Al, it appears that all the Al lifts and only the c-Si stays behind. Magnified HRTEM images of the two areas marked by red squares are depicted in Figure 5.17b and d. The interface region in Figure 5.17b shows a completely crystallized c-Si film with <111> orientation perpendicular to the interface. The calculated FFT diffraction pattern in Figure 5.17c confirms the epitaxial connection of the Si to the 4H-SiC, showing almost exclusive diffractions belonging to Si{111} and to the 4H-SiC substrate. Figure 5.17d shows HRTEM images of the c-Si pillars. On top of the pillar, an Al grain of about 10 nm width and 8 nm height with a rounded tip and a flat interface to the underlying c-Si pillar is detected. The width of the growing c-Si pillar matches the width of the Al grain. The FFT patterns in the insets (e) and (f) confirm the two parts being Al and c-Si with their <111> direction being equal to the growth direction.

The continuous growth of such a pillar is thermodynamically favorable as discussed above. Only at the Al/c-Si interface, the growth of Si is possible whereas new nucleation at the Al/a-Si is not possible at this temperature. The question about how the Al grains initially lift from the SiC surface stays open because the nucleation of Si at the Al/SiC interface was not likely, although diffusion of a-Si, and consequently wetting of the SiC/Al interface will occur, especially due to the very thin Al layer. Further investigations by e.g. TEM *in-situ* heating experiments are required to observe if the lifting of the Al grains is stress-induced or due to Si nucleation under the Al.

Although the crystallization was not finished after 105 h at temperatures in the 200 to 300 °C range, the interface near regions appeared completely crystalline and well oriented. Therefore, additional high-temperature annealing steps could be used to complete this process, preferentially by taking the already available crystalline parts as a template.

In Figure 5.18 TEM images of the sample with a second, high-temperature annealing step are provided. The sample appears rather grainy but completely crystallized in the low magnification image. A SAED pattern taken from the marked region is depicted in Figure 5.18b. It shows both, strong reflections of <111> Si normal to the interface, but also plenty of diffraction spots indicating randomly oriented grains. The appearance of additional orientations was also noticed by the additional peaks in the XRD diagram. On the surface, agglomerated Al in form of a thin layer and bigger grains is found. A closer look also indicates some residual Al islands close to the interface region. To further investigate the interface quality, an HRTEM image is shown in Figure 5.18c along with its corresponding FFT pattern in Figure 5.18d. The image was intentionally taken from a region where residual Al is present. The residual Al has the height of the originally deposited Al film and appears to be still in epitaxial connection to the 4H-SiC. Also, the c-Si in the surrounding regions is fully crystallized and well <111> oriented. The findings indicate that not all of the Al is lifted off by diffusion and the crystallization process. Due to the high crystallinity of the Al, there might be too few GBs to allow a-Si to diffuse perfectly underneath the Al, thus enabling a layer exchange, independent if it is a stress-related lift-off or a crystallization directly at the SiC/Al interface. Further experiments, altering the Al layer thickness and Al deposition parameters, resulting in a higher density of GB will be required to minimize the density of remaining Al at the interface.

5.2.5 ISE treatment prior deposition

To further illustrate the importance of the metal's microstructure, two samples were prepared with 200 nm Al and 200 nm a-Si on Si-face 4H-SiC. One sample underwent an ISE treatment with Ar ions at 500 W for 20 s at a pressure of 5 µbar prior to the Al and Si deposition. Both samples were measured using XRD and SEM prior and after annealing at 400 °C for 2 h at a 5 °C ramp rate to observe the influence of the ISE pre-treatment on the MIC process. The XRD results are shown in Figure 5.19. The *as-deposited* samples already show a difference in the microstructure. Both show no crystalline Si parts,
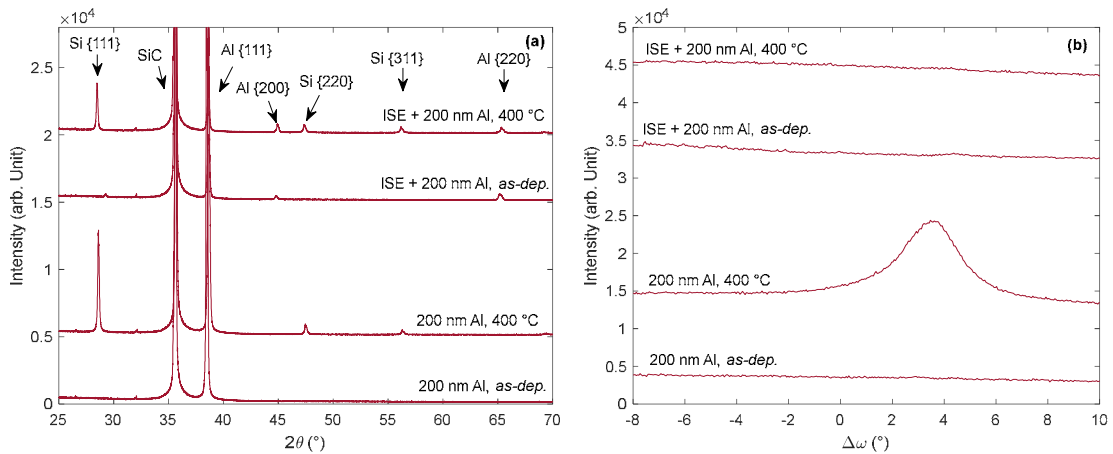
Figure 5.19: (a) XRD diagrams (2θ-scans) and (b) rocking curves (ω-scans) of samples with 200 nm Al / 200 nm a-Si *as-deposited* and after 400 °C 2 h annealing. One sample underwent ISE treatment prior Al deposition. The rocking curves are performed at the Si{111} diffraction angle.

but the Al, which is only {111} textured without ISE shows a more random texture after ISE, indicated by the presence of Al{200} and Al{220} diffractions. As the previous investigations already showed, sputter-deposited Al is epitaxially connected to the 4H-SiC. The destructive properties of the ISE treatment amorphizes the 4H-SiC surface, leaving no crystal information for any orientational growth. After thermal annealing, both samples exhibit similar Si diffraction signals. The sample subject to ISE treatment shows slightly less intensity. Rocking curves show the most dominant difference in the orientational distribution of the Si{111} signal. The sample without ISE shows the usual trend of an off-axis orientation, whereas the ISE treatment resulted in no orientation preference of the Si{111} grains.
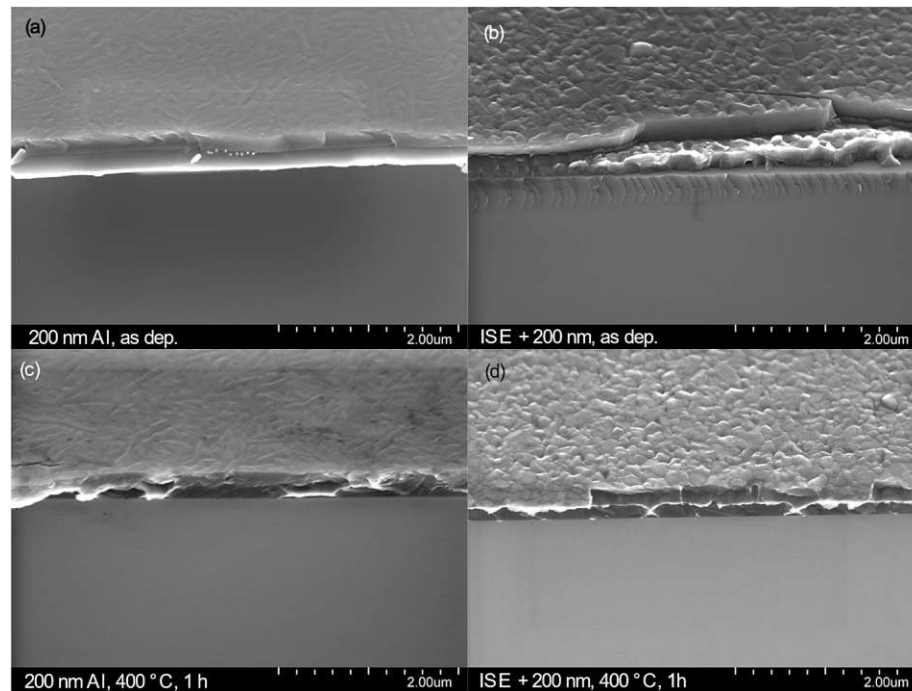
Figure 5.20: SEM cross sections under 45° of samples with 200 nm Al and 200 nm Si. (a and c) "normal" (b and d) with ISE treatment prior Al deposition.

SEM cross-sections taken under an angle of 45° are shown in Figure 5.20. Again, a noticeable different microstructure is visible in the *as-deposited* state. Without ISE, no clear interface is visible, as the Al sticks very well to the SiC. With ISE, the Al has a much higher roughness, and the adhesion seems to be worse, as the layers easily separated at the cleaved edge. The rough surface on the top a-Si layer is only a replica of the underlying Al surface. After thermal annealing, a layer exchange is detectable on both samples. As seen in previous samples, residual Al is in contact to the 4H-SiC surface on many sites. Using ISE, the continuity of the c-Si layer improved significantly. Although, as the rocking curves indicated, the Si is of polycrystalline microstructure, which is not surprising due to the lack of any template.

This example clearly demonstrated the importance of the Al microstructure on the MIC process. Although the randomly textured Al, which is achieved using ISE, results in a more complete layer exchange, presumably due to the higher density of high angle GBs and the lower adhesion to the substrate, the resulting c-Si layer is also completely polycrystalline with no preferred orientation.

5.3 Conclusion

In summary, the MIC process was investigated using 4H-SiC as a substrate for epitaxial crystallization of Si. *In-situ* MIC experiments showed the possibility of sputter-depositing crystalline Si on 4H-SiC using seed-layers and deposition at elevated temperatures well below the temperatures needed for direct crystalline deposition. Only non-closed films could be produced using this technique, but further experiments using different Si deposition rates might overcome this issue.

Then the focus was led on *ex-situ* annealing facilitating the well-known layer exchange process of MIC. The variety of possible parameters is huge. Among the different film thicknesses of the metal and Si, also the different annealing conditions play an important role. The use of Al, Au, and Ag as catalytic agents was investigated, clearly indicating the superior performance of Al, also acting as a good p-type dopant to Si. Using Au, no continuous Si film, but several μm thick agglomerated c-Si islands were found and Ag did not show any signs of Si crystallization in the range of 200 to 275 °C. Both are also not CMOS compatible. Using Al, well oriented c-Si grains were observed at annealing temperatures as low as 200 °C. Al was found to grow epitaxial on 4H-SiC, having a big influence on the final c-Si/4H-SiC interface quality. Very thin Al layers of only 10 nm thickness were evaluated to facilitate the diffusion of a-Si to the 4H-SiC interface. Among the thicknesses of the two layers, also the annealing temperature, duration, and ramp rate are important parameters. The temperature should not exceed the eutectic temperature of the used metal/semiconductor system to prevent extensive diffusion and intermixture. The microstructure of the involved metal seems to play an important role in the MIC process. The epitaxial quality of the Al seems to be crucial for the epitaxial recrystallization of the Si. On the other hand, the high quality of the epitaxial Al with a low density of GBs will hinder a complete layer exchange. Different deposition techniques of the Al should be compared in further experiments. Another approach is the intentional oxidation of the Al prior Si deposition, to form a thin permeable interface of AlO_x in between Al and a-Si, which will favor the layer exchange process [149], [277].

Results of heterojunction diode characterizations fabricated using low-temperature MIC, followed by recrystallization at higher temperatures are given in 6.5.

Due to the well-reduced temperature budget, the MIC process might not only be interesting for material combinations that cannot withstand too high temperatures, but it may also reduce the overall fabrication cost. With further research also the Si/4H-SiC heterojunction can benefit from this low-temperature technique.

6 Characterization and evaluation of Si/4H-SiC diodes

The chapter starts with a theoretical evaluation of the expected SBH of selected heterojunction combinations as a function of contact semiconductor doping concentration and temperature. Next, the basic fabrication steps towards Si/4H-SiC HJDs are presented and discussed. Tung's model of inhomogeneous SBH distribution is successfully fitted to Si/4H-SiC diodes, revealing many details about the SBH distribution on the interface. The heterojunctions fabricated using LPCVD and MIC were prepared as HJDs and characterized electrically. Additionally, techniques to alter the SBH using Ar⁺ bombardment of the 4H-SiC interface prior Si deposition are discussed. The chapter is completed with an experimental series showing the influence of inserting ultrathin amorphous SiC layers on conventional Ti/4H-SiC Schottky diodes as a measure to tailor the SBH.

6.1   Evaluation of 4H-SiC heterojunctions diodes

Based on the theory about the basic semiconductor equations from Section 2.2.1 and about heterojunctions and Schottky contacts from Section 2.3, this section estimates the expected SBH of some heterojunctions to 4H-SiC. Si, as well as 3C-SiC are investigated as contact materials for heterojunction formation. As substrates n-type as well as p-type 4H-SiC are investigated with a doping density of $N = 2.6 \cdot 10^{16}$ cm^{-3}, which corresponds to the doping concentration of the epitaxial layers presented in the experimental section. Although only n-type 4H-SiC is used for diode fabrication, also p-type 4H-SiC
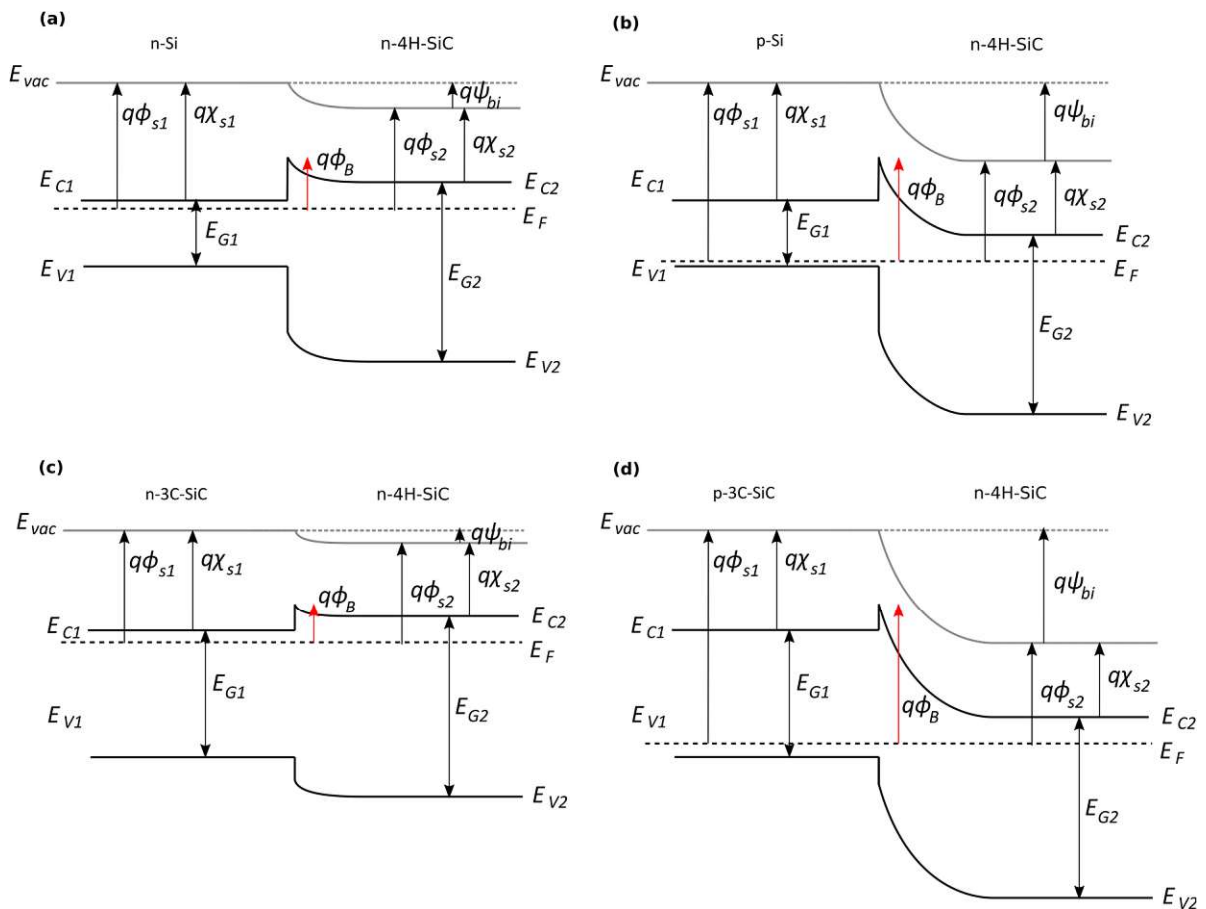
Figure 6.1: Schematic illustration of the band diagram of (a) n-Si, (b) p-Si, (c) n-3C-SiC, and (d) p-3C-SiC contacts to n-4H-SiC. The diagrams are not based on the exact energy and potential values, but close enough, to allow a visual representation of the band alignment and the corresponding SBH.

is considered in the calculations to estimate its potential. The SBH is calculated as a function of the contact material doping concentration and temperature. A contact doping of both n-type and p-type is investigated with a concentration ranging from $N = 2 \cdot 10^{17}$ cm^{-3} to $2 \cdot 10^{20}$ cm^{-3}. With a doping concentration of the contact material being much larger than that of the substrate, the band bending is limited mostly to the substrate. With this assumption, the heterojunction can be modeled like a Schottky contact with the semiconductor work function equal to the metal work function of a Schottky contact.

For better understanding, the band diagrams of n and p-Si as well as n and p-3C-SiC to n-type 4H-SiC are depicted in Figure 6.1. What can be seen immediately is the much less band bending and hence SBH using n-type contacts. With p-type contacts the resulting SBH is increased by almost the band gap of the contact material. The band offsets, although not labeled in the figure, stay the same with different contact doping types. Also, the approximation of no band bending in the contact semiconductor is illustrated in this figure. From the schematic illustrations it can be estimated that the SBH of n-type 3C-SiC contacts will be smaller than of n-Si ones due to the lower electron affinity of 3C-SiC. And due to the increased band gap, the p-3C-SiC SBH will be larger compared to p-Si. In the band diagram and the following evaluations, the ideal band alignment, after the Schottky-Mott and Anderson rule is assumed using the Schottky-Mott Equation (2.29) for n-type and (2.30) for p-type 4H-SiC. This, however, is only a rough estimation as many effects influencing the SBH are neglected as discussed above. Nevertheless, it allows an estimation of the SBH and will allow us to determine which trend the contact doping type, concentration, and temperature will have on the SBH. Nonidealities will of cause alter this value, but the trend and the influence of the doping will still have a major impact on the final SBH.

To estimate the SBH all the semiconductor parameters are calculated as discussed above, also as a function of temperature. Most of the used values and models were already discussed, therefore only new
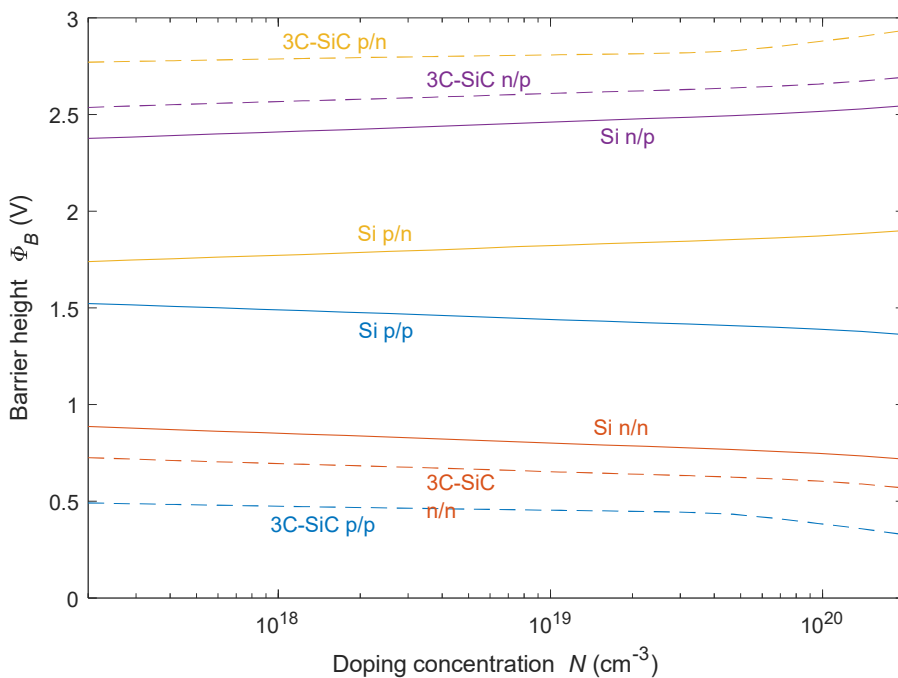
Figure 6.2: Theoretical SBH at T = 300 K of all investigated combinations of Si/4H-SiC (solid lines) and 3C-SiC/4H-SiC (dashed lines) heterojunctions over the doping concentration of the contact semiconductor. The doping concentration of the 4H-SiC was kept constant at N = 2.6x10^{16} cm^{-3}.

parameters, especially for 3C-SiC are given here. Room temperature values of 4.05 V for Si, 3.3 V for 4H-SiC and 3.9 V for 3C-SiC were implemented as electron affinities. Especially for SiC the values in literature spread over a wide range, so that an average of the published values was used [138]. The 3C-SiC was assumed to be nitrogen-doped for n-type and aluminum-doped for p-type with ionization energy levels of 47 meV [280] and 200 meV [18], respectively. Due to the rather high doping levels of the contact semiconductor, also the effect of metal-insulator transition ionization needed to be considered [77]. As discussed above, this effect reduces the ionization energy level with high doping concentrations. Due to the lack of data the values for n-type Si were used for n-type 3C-SiC (as the ionization levels are almost equal) and for the p-type 3C-SiC the values of p-type 4H-SiC were used. For the temperature dependency of the 3C-SiC band gap the Varshni model was used with parameters from [281]. The zero-temperature band gap of 3C-SiC is with 2.39 eV in between that of Si and 4H-SiC. Doping dependent band gap narrowing was also considered for 3C-SiC after Equations (2.14) and (2.15) using values from [70]. To calculate the densities of states, the density of states effective masses of $m_{dc}^* = 0.35m_e$ and $m_{dv}^* = 0.6m_e$ [281] were used. No dependence of temperature could be found for the latter quantities.

To give an overview, Figure 6.2 shows the calculated SBHs at room temperature over the contact doping concentration of all eight heterojunction combinations. A wide span of SBHs from 0.33 V for highly doped p-3C-SiC/p-4H-SiC to 2.93 V for highly doped p-3C-SiC/n-4H-SiC was found. The 3C-SiC/4H-SiC heterojunctions show the lowest and the highest barrier heights, whereas the isotype heterojunctions (p/p and n/n) result in low and the anisotype (p/n and n/p) in high SBHs. All the evaluated SBHs for the Si heterojunctions are in between the those based on 3C-SiC. The n-Si/n-4H-SiC heterojunction calculated the lowest SBHs with 0.72 to 0.88 V, depending on the doping concentration
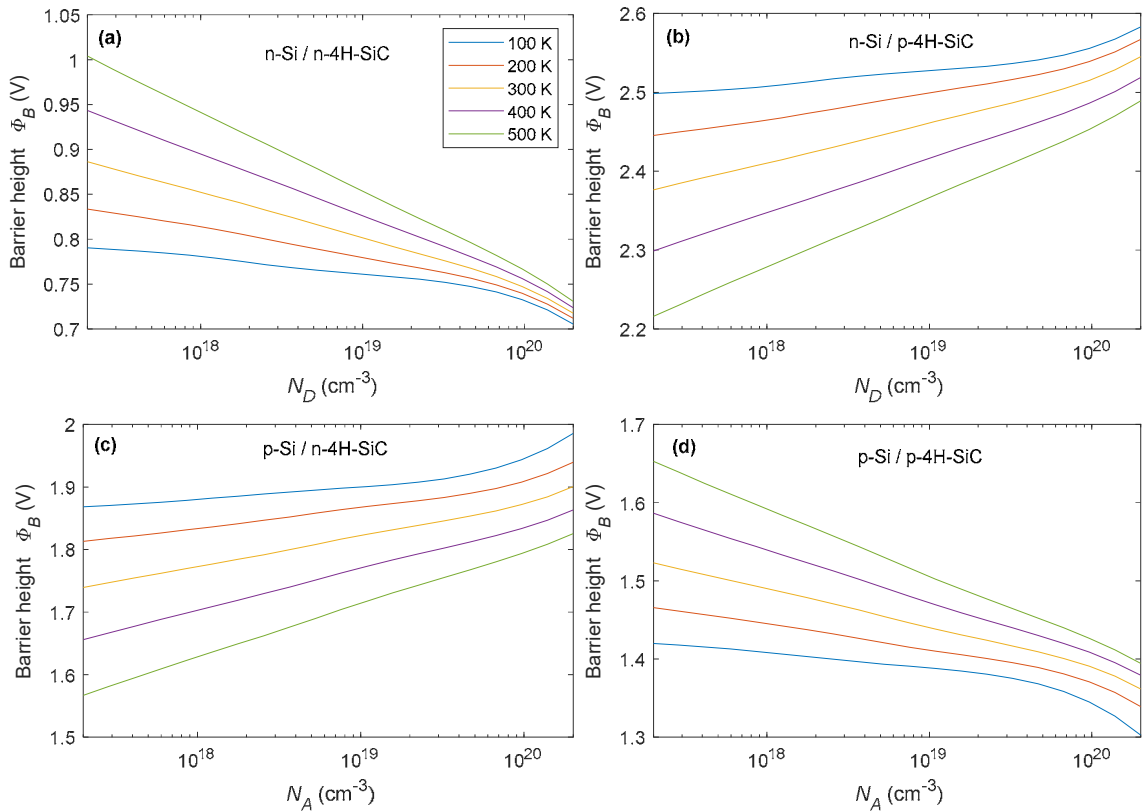
Figure 6.3: Theoretical SBH of all four Si/4H-SiC heterojunction combinations over Si doping concentration at several temperatures.
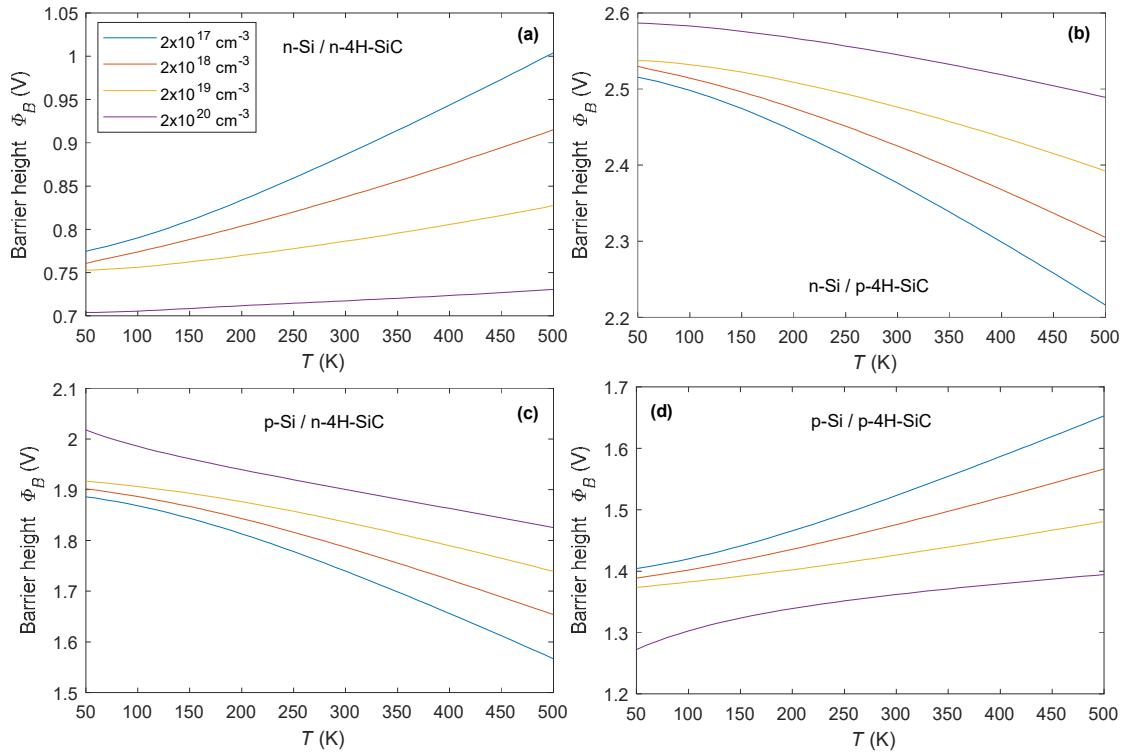
Figure 6.4: Theoretical SBH of all four Si/4H-SiC heterojunction combinations over temperature for several Si doping concentrations.

and the highest of around 2.45 V in the n/p configuration. The remaining p/p and p/n heterojunction combinations cover the middle of the SBH spectrum with around 1.45 and 1.8 V, respectively. All isotype heterojunctions show a decrease in SBH with increasing contact semiconductor doping concentrations, whereas all anisotype show an increase. The absolute degree of change with concentration is similar across all combinations, but especially for the low SBH heterojunctions the influence of the doping concentration is significant. The p-3C-SiC/p-4H-SiC calculated to have a SBH of 0.49 V for a 3C-SiC doping concentration of $2 \cdot 10^{17}$ cm^{-3}, and at $2 \cdot 10^{20}$ cm^{-3} it decreases to 0.33 V which is a decrease of 33%.

More detailed results at different temperatures and also as a function of the temperature are shown in Figure 6.3 and Figure 6.4 for Si contacts and Figure 6.5 and Figure 6.6 for 3C-SiC contacts. At lower temperatures, the dependence of the SBH on the contact doping concentration reduces, whereas it increases at higher temperatures, for both Si and 3C-SiC contacts. The SBH curves of the p-type 3C-SiC contacts show a rather unexpected kink. This can be attributed to the metal-insulator transition, resulting in a strong increase of ionized dopants which also affects the Fermi level and subsequently the resulting SBH. In Figure 6.5c and d one can see the kink, at high doping concentrations. At low temperatures, the kink already starts at about $3 \cdot 10^{18}$ cm^{-3}, and at 500 K this effect is only visible at very high doping levels in excess of $8 \cdot 10^{19}$ cm^{-3}. Regarding temperature dependence of the arising SBHs, the Si and 3C-SiC contacts show the same trend of a positive temperature coefficient of the SBH for isotype heterojunctions and a negative coefficient for anisotype ones. The higher the contact doping concentration, the lower is the temperature dependence of the SBH.

For the Si/4H-SiC system, especially Henning et al. [38] conducted experimental studies for all heterojunction combinations, showing similar results to those calculated. Highly crystalline
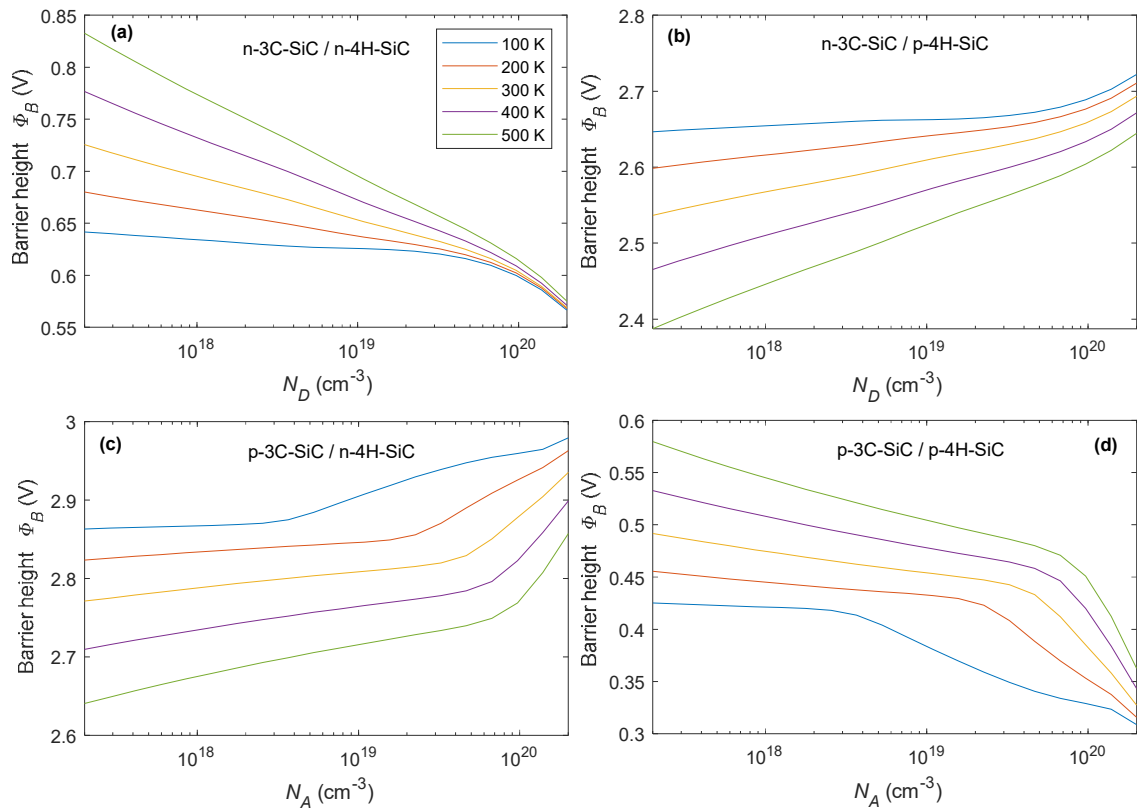
Figure 6.5: Theoretical SBH of all four 3C-SiC/4H-SiC heterojunction combinations over 3C-SiC doping concentration at several temperatures.

heterojunctions fabricated using high-temperature deposition or wafer bonding resulted in a stronger deviation of the theoretical values, most likely due to stronger FLP [41], [44], [46]. For the 3C-SiC/4H-SiC heterojunction system only one study using the n/n doping combination is available [282]. With an IV SBH of 0.75 V, it matches the expected ideal value well, but the ideality factor was very high and the deviation to the CV evaluated SBH was huge, indicating massive interface inhomogeneities or FLP.

The conducted calculations provide a good basis to tailor the SBHs given the influence of the contact doping type and the contact doping concentration as well as the temperature. Although the real SBH will differ from this ideal value due to FLP, SBH inhomogeneities, and image force lowering, it allows estimating the ideal value that can be reached when the above effects can be sufficiently suppressed. It also shows that 3C-SiC as a contact material to 4H-SiC is not ideal, as it results in only rather low or rather high SBHs. Si on the other hand gives with SBHs of about 0.8 and 1.8 V to n-type 4H-SiC, reasonable barrier heights for advanced heterojunction diodes.
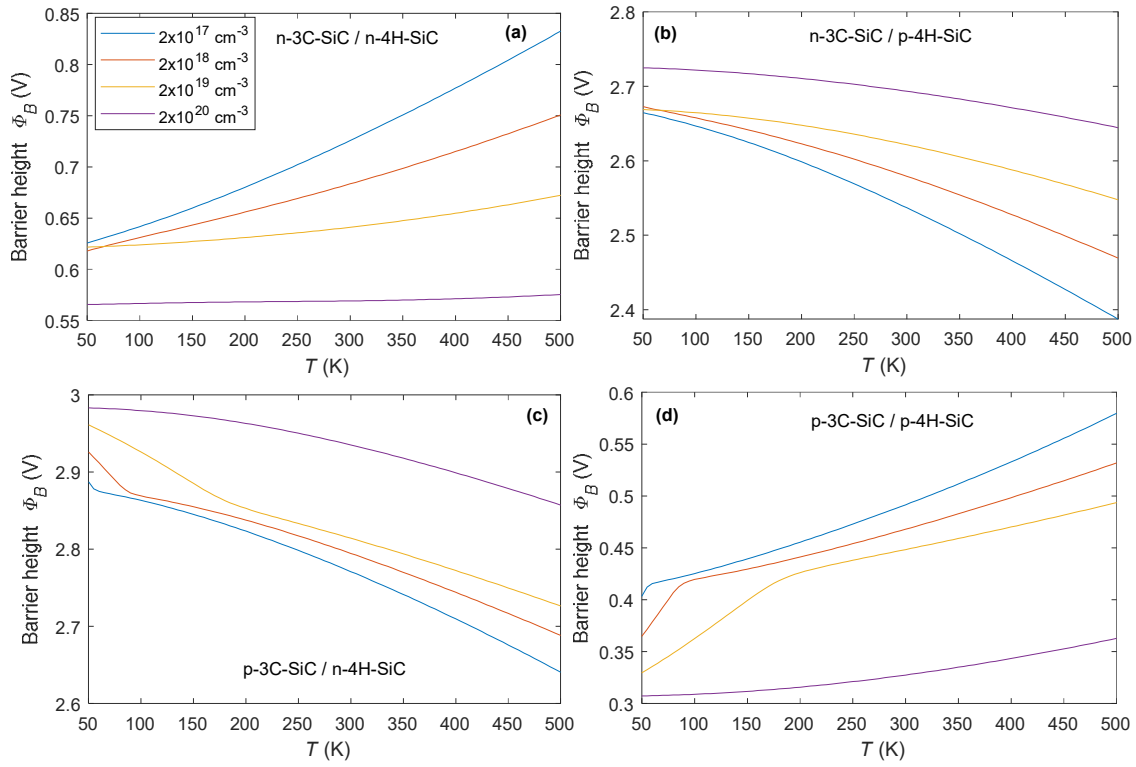
Figure 6.6: Theoretical SBH of all four 3C-SiC/4H-SiC heterojunction combinations over temperature for several 3C-SiC doping concentrations.

6.2 Diode fabrication routes

In this chapter the basic fabrication steps of the Si/4H-SiC heterojunction diodes investigated in this thesis are described. The starting point is a bare 4H-SiC wafer supplied by Cree with a base nitrogen doping concentration of 0.015 to 0.028 Ωcm and 4° off-c-axis cut. On the Si-face the wafers are equipped with a 5 µm thick epitaxial layer with a nitrogen doping concentration of about $2.6 \cdot 10^{16}$ cm^{-3}. The wafers are cut in rectangular pieces of about $12 \cdot 10$ mm, to allow easier handling and to maintain the orientation information. On the backside, the sample number was scribed with a diamond scriber. Due to these measures, the crystal orientation of the pieces is always known. For some microstructural experiments (e.g. Si-crystallization and MIC) wafers from SiCrystal with the same orientation and base doping were used but without an epitaxial layer. The substrate used and any special pre-treatments are mentioned in the respective section.

A schematic illustration of the device fabrication process at some important states is depicted in Figure 6.7. The fabrication steps between the depicted states are described in Table 6.1. For device characterization in forward-direction, the simplest junction configuration namely a planar, circular active contact was realized. More advanced structures have the main purpose of increasing the reverse withstanding voltage by reducing the sharp edge effect [14]. For moderate reverse biases, the simple planar structure is adequate, having the advantage of faster fabrication, thus allowing the variation of more parameters.
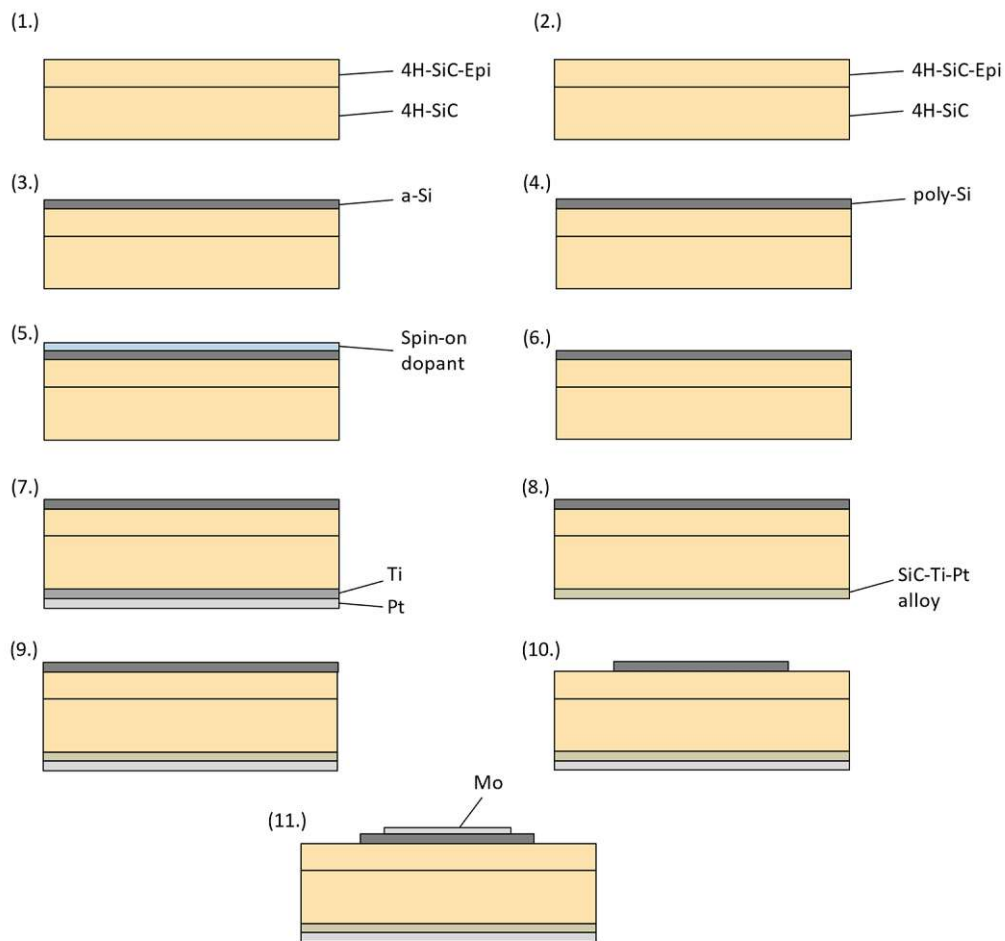
Figure 6.7: Schematic illustration of important fabrication states of Si/4H-SiC heterojunction diodes. The processes between the depicted states are described in Table 6.1.

Table 6.1: List of fabrication process steps according to the enumerated process states of Figure 6.7 for Si/4H-SiC HJDs.

Process step	Description
1. → 2.	**Cleaning:** Starting point is a diced substrate. Acetone with ultrasonic assistance was used to remove any organic contaminations and particles remaining from dicing. Next step was a HF dip, followed by an RCA clean (details about the solution can be found in 3.1.1). After the final dip in DI water, the sample is dried with compressed N_2.
2. → 3.	**Si deposition**: The freshly cleaned substrates are now ready for deposition and should be loaded immediately without leaving the clean room environment. Sputter-deposition was used for a-Si deposition. If LPCVD is used for Si deposition, the following crystallization step can be skipped.
3. → 4.	**Crystallization**: The a-Si needs to be crystallized. A tube oven with high vacuum capability was used to anneal the samples at 1000 °C for 1 h with slow ramp. Other high purity inert gas environments might be used, but the residual oxygen concentration must be very low to prevent strong oxidation. Nevertheless, an HF dip was done after crystallization to remove any oxidation residuals.
4. → 5.	**Doping**: The Si layer needs to be highly conductive, therefore spin-on dopants with a high phosphorus or boron concentration have been applied. After some trial runs dip coating turned out to be the best procedure to apply an even layer of the liquid. After dipping the backside is cleaned with isopropanol. Then the samples are backed for 10 min at 220 °C to harden the spin-on glass. The final drive-in was done in air environment at 1000 °C for 1.5 h. If pre-doped Si targets were used this step might be skipped.
5. → 6.	**Glass stripping**: After the drive in, the hardened glass layer can be stripped with BOE or concentrated HF.
6. → 7.	**Ohmic contact deposition**: Now the ohmic contact on the back is formed by sputter-depositing 200 nm Ti and 200 nm Pt. The additional Pt was found to enhance the contact by preventing Ti oxidation. Another metal known to form a good ohmic contact to 4H-SiC is Ni.
7. → 8.	**Ohmic contact formation**: Annealing at 1000 °C for 1 min was performed in a rapid thermal annealing oven to initiate alloy formation between the SiC/Ti/Pt to achieve a good ohmic contact.
8. → 9.	**Protection layer**: Another Pt layer of 200 nm thickness is deposited on the back side for better electrical contact and to protect the formed contact alloy from the following steps.
9. → 10.	**Si pattering**: Using photolithography, circular pads of resist are patterned on top of the Si to serve as etch mask. An isotropic silicon etch (for details see 3.1.1) was used for patterning. The etch rate is very fast. About 10 s are needed for about 500 nm Si. The 4H-SiC stays unaffected.
10. → 11.	**Top metallization**: For a better electrical contact (lower on-resistance) a top metallization is applied on the Si contact. The pattering of the metallization needs to be done as a separate step. Doing both, metal, and Si etching, using one etch mask will result in under etching due to the fast etch rate of Si. This leads to metal touching the SiC on the edges of the pads. To prevent this a second photolithography step was used with slightly smaller pad sizes than the Si pads. Pad sizes between 600 and 900 µm in diameter have been used (see details of each experiment). The metal pads are about 100 µm smaller. For p-Si Mo was used as top metallization and for n-Si Hf was used.

6.3 Modeling of inhomogeneous Si/4H-SiC heterojunction diodes

Parts of this section have been published in [94].

In this section, HJDs were realized by sputter-depositing polycrystalline p-Si on monocrystalline n-type 4H-SiC. These devices were characterized electrically over a large temperature range from 60 to 460 K to evaluate SBH inhomogeneities. The relatively high SBH the p-Si/4H-SiC heterojunction is well suited to investigate SBH inhomogeneities, as low barrier regions of small size will stand out from the high SBH background. The theoretical aspects of inhomogeneous SBH distributions were already discussed in Section 2.3.5 and serve as the basis for the modeling presented in this section.

6.3.1 Experimental details

Thoroughly cleansed, 4H-SiC substrates supplied by Cree Inc. with a nitrogen bulk doping concentration of $N_D = 10^{19}$ cm^{-3} and a 5 µm thick epitaxial layer with $N_D = 2.6 \cdot 10^{16}$ cm^{-3} are used as substrates. An approximately 1 µm thick layer of a-Si was sputter-deposited from a highly boron-doped Si target ($\rho < 0.005$ Ω cm) with 6 N purity using a sputtering power $P = 500$ W and a chamber pressure $p = 0.3$ Pa. The sample was not actively heated during film synthetization, so that only plasma-induced self-heating took place. The *as-deposited* samples underwent a PDA step to crystallize the a-Si to poly-Si. The PDA process was carried out in a quartz tube furnace in high vacuum (< 1 mPa) for 2 h at 900 °C and 1000 °C, respectively. The further process steps towards a HJD are described in detail in Section 6.2. The active interface area of the HJDs was 0.5 mm^2.

Electrical measurements were conducted in a dark, electrically shielded cryo/heating chamber under vacuum in a temperature range of 60 to 460 K in 20 K steps. IV measurements were done with a Keysight B2985A electrometer from 0 to -20 V in 500 mV steps and from 0 to 2 V in 15 mV steps while setting the current compliance to 20 mA. CV measurements were done using an Agilent 4294A high precision impedance analyzer at 1 MHz test frequency in a voltage range of -2 to 0.5 V. The voltage sweep direction was from negative to positive values and back.

6.3.2 IVT and CVT measurements

In this section, the classic evaluation methods, as described in Section 3.3, for both, IVT measurements using the TE equation, and for CVT measurements are applied to determine the SBH. SBHs determined from IV measurements are designated $\phi_{B,IV}$ and those from CV as $\phi_{B,CV}$.

Figure 6.8a and b show the measured IVT data of two selected, representative diodes with PDA temperatures T_{PDA} of 900 and 1000 °C, respectively. No major deviation was found between different diodes, which justifies the selection of these two for the fitting experiments. Especially at low measurement temperatures, strong deviations from the ideal, linear characteristics are observed. Two, or in some cases even three bumps in the IV data are present. These bumps are representative for regions with lower SBH than on average being present across the diode area. At low temperatures, the current is predominantly flowing through regions with the lowest SBH until they become saturated. At temperatures $T > 300$ K, the curves start to become more ideal and at $T > 400$ K, the IV curves are almost linear. This behavior is as expected because at elevated temperatures enough charge carriers can pass directly over the higher background barrier, whereas the current fraction over the relatively small regions with a low SBH is limited and hence, has a negligible impact on the overall device performance. In Figure 6.8c and d, IV measurement cycles of six diodes originating from the same two wafers are depicted at two temperatures. All measured diodes show similar characteristics with multiple bumps at $T = 100$ K, predominantly in a region where the current flow is dominated by low SBH patches. At 300 K, the deviations become even smaller.
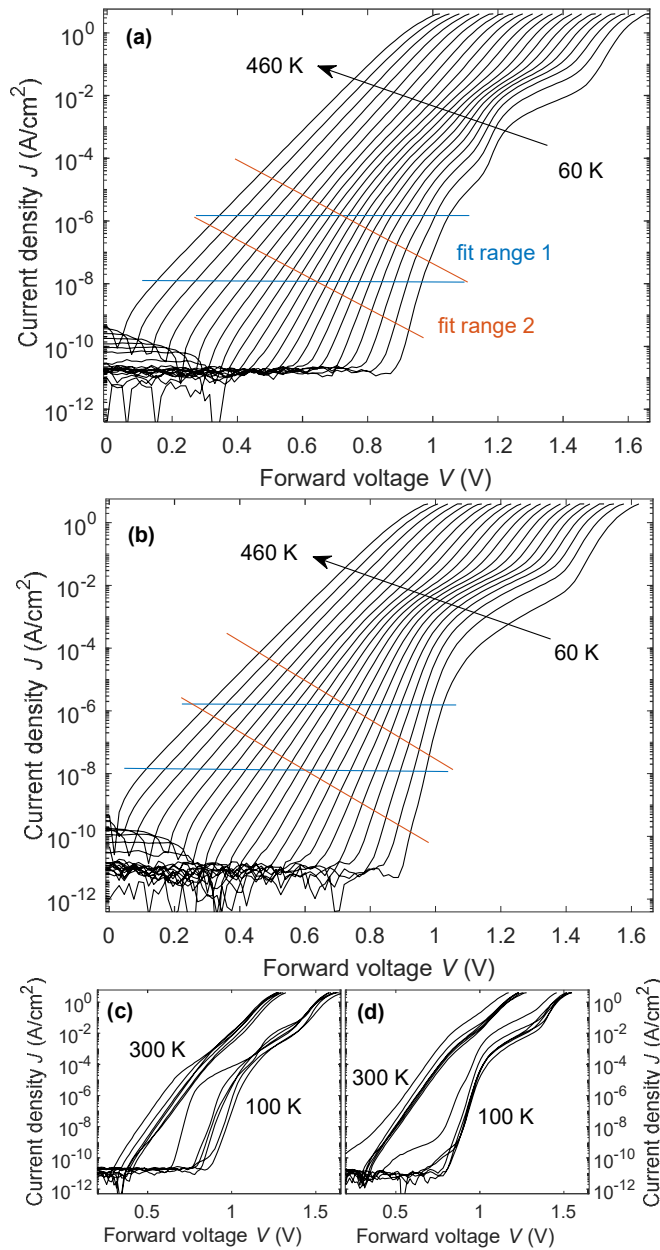
Figure 6.8: IVT measurements of heterojunction diodes annealed at (a) T_{PDA} = 900 °C and (b) T_{PDA} = 1000 °C. Lines indicate two current ranges used for fitting. (c) and (d) show at two temperatures the superposition of six diodes of the same wafer annealed at 900 and 1000 °C, respectively.

In the depicted IVT data, two current regions are indicated, which are used for fitting. Fit range 1 covers a constant current density interval independent of the measurement temperature, whereas fit range 2 is temperature dependent, thus accounting for the huge measurement temperature range.

The reverse characteristic of the same two diodes is depicted in Figure 6.9. Below room temperature the reverse current up to -20 V is within the noise spectrum of the measurement setup. Above room temperature a high temperature dependence of the reverse leakage current is observed as expected from the TE Equations (2.33) and (2.34). The voltage dependence will mainly be due to image force lowering and due to the voltage dependent pinch-off of the low SBH patches. Despite the presence of low SBH patches, the reverse leakage current is relatively low, being dominated by the high background barrier. Similar to the forward bias measurement, the low SBH patches will only dominate the current flow at
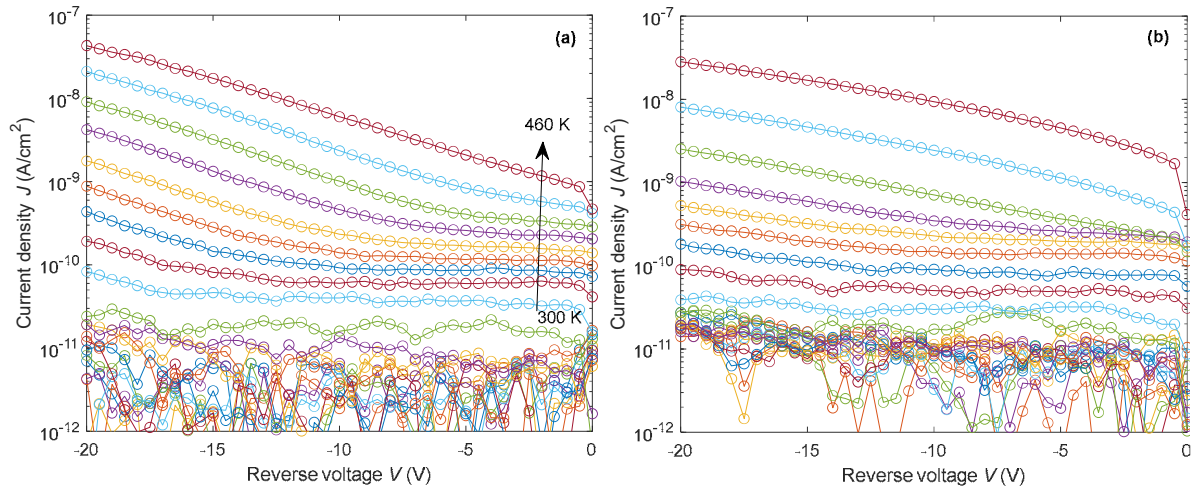
Figure 6.9 Reverse IV characteristic of the representative diode annealed at (a) 900 °C and (b) 1000 °C.

low temperature. At these low temperatures, the leakage current is, however, below the measurement capabilities. At higher temperatures, the major current contribution will be from the average background as a consequence of the larger thermal voltage, hence broad carrier distribution.

The extracted diode properties of the two diodes are shown in Figure 6.10. In the upper two graphs, $\phi_{B,IV}$ and η are plotted as a function of temperature. The extracted parameters from these two different fit ranges match very well at elevated temperatures. At lower temperatures, however, the deviations become more dominant. This is obvious as the IV curves are no longer linear, but slightly curved, resulting in bias-dependent $\phi_{B,IV}$ and η values, which is common for inhomogeneous SCs [119], [120], [125]. Due to the non-linearity of the IV curves at low temperatures, the extracted values are strongly
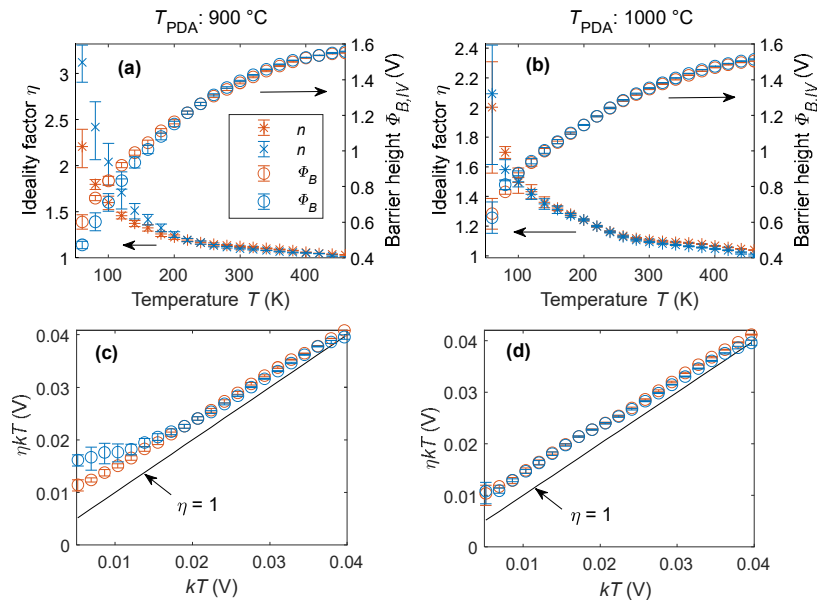
Figure 6.10 (a)(b): Extracted SBH $\phi_{B,IV}$ and ideality factor n of the two diodes displayed in Figure 6.8. (c)(d) Plot of ηkT over kT showing the temperature dependence of the ideality factor. The straight line indicates the ideal case of $\eta = 1$. The colors correspond to the two fit regions shown in Figure 6.8. Error bars indicate the 95 percent confidence interval of the parameter due to fitting.
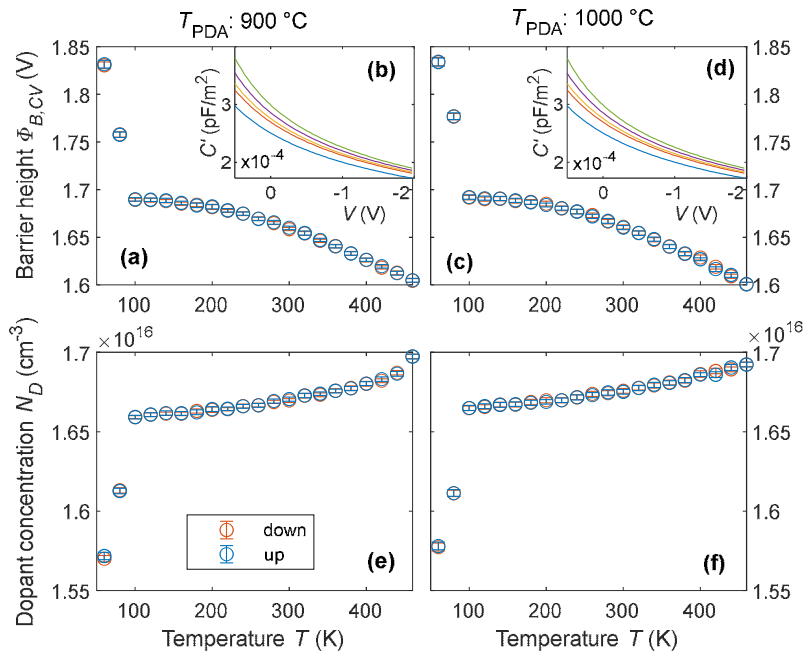
Figure 6.11: SBH $\phi_{B,CV}$ and doping concentration N_D evaluated using CV measurements in a temperature range of 60 K to 460 K at 1 MHz test frequency. The sweep direction was altered between upwards (up) and downwards (down). Left figures annealed at T_{DPA} = 900 °C, right figures at T_{DPA} = 1000 °C. Insets (b) and (d) show the raw CV data at 60, 100, 200, 300 and 400 K from bottom to top. Error bars indicate the 95 percent confidence interval of the parameter due to fitting.

dependent on the applied fitting range and need to be considered carefully. Furthermore, a strong temperature dependence of both parameters is observed. The SBH is very low in the range of 0.4 to 0.6 V at 60 K but increases substantially with temperature until it tends to saturate. For the 900 °C annealed sample this device parameter almost reaches a value of 1.56 V at T = 460 K, while it is 1.52 V for the 1000 °C annealed sample. This difference of about 40 mV in the maximal SBH at these two annealing temperatures is seen across many samples. This deviation is attributed to different crystallographic properties, e.g. grain size, in the poly-Si film due to the different annealing temperatures [220].

At the lowest measurement temperatures, the ideality factor is very high, ranging between 2 and 3, and decreases towards 1 as the temperature is increased. At room temperature η is already below 1.1 and reaches values as low as 1.03 at T = 460 K. The lower two plots depict the temperature dependence of η in a different form along with the ideal case of $\eta = 1$. This way of plotting is ideal for identifying the temperature dependence of η [127]. The measured ideality factors are almost parallel to the unity slope, therefore representing the T0-anomaly. Only at the lowest temperatures, a slight deviation from the straight line is visible, reflecting a starting contribution of tunneling currents. The T0-anomaly is typical for inhomogeneous MS contacts and the theory by Tung explains it very well [125].

To further investigate the fabricated HJDs, CVT measurements have been conducted between 60 and 460 K at a test frequency of 1 MHz comprising of an up-and downward voltage sweeps to detect any hysteresis. The SBH and the semiconductor doping concentration have been evaluated at every temperature for both sweep directions.

The extracted parameters are depicted in Figure 6.11. All graphs have in common, that the measuring points at the lowest two temperatures deviate strongly from the overall trend. These data points do not

reflect the true value but are artifacts from the beginning resonance of the dopant states. At these low temperatures, the time constant of the cubic site nitrogen donor start to match with the measuring frequency, resulting in measured capacitances different from those given by the depletion width [283] (see Section 2.2.2). When neglecting these data points, the SBH values using the CV method $\phi_{B,CV}$ are about 1.7 V at low temperatures, whereas this parameter slightly decreases to 1.6 V at $T = 460$ K. The second sample, which was annealed at 1000 °C, shows the same trend in SBH. The shape of the measured temperature dependence of the SBH agrees with the predicted trend of decreasing SBH with temperature (see Figure 6.4c). It strongly deviates from the IVT obtained values, because the CV method gives the mean SBH $\phi_B{}^0$ across the whole diode area [122], [284]. Despite these differences, the extracted SBH values of both methods are in good agreement at high temperatures. The measured doping concentration is within the specifications of the 4H-SiC epitaxial layer as given by the manufacturer. No notable difference between the two sweep directions is observed, indicating no hysteresis effects.

6.3.3 Fit using 2 Gaussian distributions

In a first approach, the IVT data of the 1000 °C annealed heterojunction diode depicted in Figure 6.8b is fitted using the Tung model, with the approximation of all patches being affected by pinch-off.

Equations (2.40a-c) defined the individual contributions of the current flow over an interface with an inhomogeneous SBH distribution. For the purpose of fitting, a Gaussian distribution of these SBH inhomogeneities is assumed, as already determined experimentally [119], [131], [132]. Although Tung also provided a specific equation considering a Gaussian distribution of the patch parameter γ_i, this theory does not consider the resistive effects of individual patches [119]. Therefore, the Gaussian distribution of patch parameters is discretized using a mean patch parameter γ_0 and its standard deviation σ_γ via

$$P(\gamma_i) = \frac{d}{\sigma_\gamma \sqrt{2\pi}} \exp\left(-\frac{(\gamma_i - \gamma_0)^2}{2\sigma_\gamma^2} \right). \tag{6.1}$$

Table 6.2: List of parameters used for fitting the measured IVT data. [*a] Additional parameters applied during the fitting procedure considering pinched-off and not pinched-off patches. [*b] Additional parameters applied during the fitting procedure when assuming three patch parameter distributions.

Fit Parameter	Description	Expected temperature dependency
$C_{p,1}$	Density of patches of the intrinsic distribution	no
$\gamma_{0,1}$	Mean value of the extrinsic distribution. Centered around $\phi_B{}^0$	no
$\sigma_{\gamma,1}$	Standard deviation of the intrinsic distribution	weak
$C_{p,2}$	Density of patches of the extrinsic distribution	no
$\gamma_{0,2}$	Mean value of the extrinsic distribution	weak
$\sigma_{\gamma,2}$	Standard deviation of the extrinsic distribution	weak
$C_{p,3}$ [*b]	Density of patches of the extrinsic distribution	no
$\gamma_{0,3}$ [*b]	Mean value of the extrinsic distribution	weak
$\sigma_{\gamma,3}$ [*b]	Standard deviation of the extrinsic distribution	weak
$\phi_B{}^0$	Mean background SBH	yes
ρ_s	4H-SiC epi-layer resistivity	yes
R_s	Series resistance	weak
σ_p [*a]	Shape parameter of the weight function	no
Δ [*a]	SBH difference of a patch from the background	yes

The discretization width d of γ_i must be chosen in a way to normalize $\sum_i P(\gamma_i) = 1$. With a discretization of the patch parameter γ_i, the number of patches with a certain γ_i is $C_p P(\gamma_i)$. C_p is the total number of patches and $C_p P(\gamma_i)$ is the number of patches with the same patch parameter, depending on the discretization. Using this discretization, the current over an inhomogeneous interface does not have to be summed up for each individual patch, but patches with the same parameter γ_i can be treated jointly and the series resistance can still be considered. Therefore, Equations (2.40) and (2.41) translate to (6.2) and (6.3) in which the index i is now the number of discretization steps.

The IVT data of Figure 6.8b clearly shows a double bump, indicating the need of at least two barrier height distributions. Therefore, two Gaussian distributions of the patch parameter γ_i are used for the fitting procedure, representing the extrinsic and the intrinsic patch distribution, the latter is centered around ϕ_B^0. All relevant parameters used for fitting are listed in Table 6.2. The indices of the fit parameters indicate the distribution to which they belong. For example, $C_{p,1}$ is the density of the first distribution counted from high barriers downwards. Some of the parameters displayed in Table 6.2 are not used in the first fit. For the patch densities and the mean patch parameter of the intrinsic distribution, no temperature dependency is expected, and hence, they were kept constant. Least-squares fits of Equations (2.39), (2.42), and (6.3) were conducted. The optimal values for the temperature-independent quantities were determined by performing the fit several times, varying these constants until the error was minimized. The resulting fit curves are depicted in Figure 6.12a, while labeling the optimized temperature-independent quantities in the figure. Those, which are temperature dependent, are depicted in Figure 6.12d.

$$\sum_i^{\text{"not p--o"}} I_{i,\text{npo}} = A^* T^2 \sum_i^{\text{"not p--o"}} (1 - P_{\text{po}}) C_p A_i \exp\left(-\beta \phi_{B,i}\right) \left[\exp\left(\beta V - \beta I_i \frac{\rho_s t}{A_i}\right) - 1\right] \tag{6.2}$$

$$\sum_i^{\text{"p--o"}} I_{i,\text{po}} = A^* T^2 \sum_i^{\text{"p--o"}} P_{\text{po}} C_p P(\gamma_i) A_{i,\text{eff}} \exp\left(-\beta \phi_{B,i,\text{eff}}\right) \left[\exp\left(\beta V \right.\right.$$
$$\left.\left. - \beta I_i \left(\frac{\rho_s}{2\sqrt{A_{i,\text{eff}}\pi}} \arctan\left(\frac{2t}{\sqrt{A_{i,\text{eff}}/\pi)}}\right)\right)\right) - 1\right] \tag{6.3}$$

The quality of the fitting procedure is estimated by the root-mean-square error (RMSE), which is also plotted as a function of temperature. At the lowest temperatures investigated, the fit is very accurate, only the region of the resistive current limit of the extrinsic inhomogeneities is not reflected very well. The measured IV data increase with voltage stronger than an ohmic limit would allow. This might be addressed either by small amounts of patches in between the two assumed Gaussian distributions or by the effect of Pool-Frenkel ionization happening underneath the small patches. Very high current densities, hence field strength could result in partially enhanced dopant ionization underneath the conducting patches even at these low temperatures. Nevertheless, due to the already very complex model, these effects are not considered. Starting at about 160 K, the fit starts to get worse, especially at low bias values, regardless of the starting parameters or the values of the temperature-independent parameters. An in-depth analysis showed that the steepness, hence ideality factors, of the IV curves in these regions is larger than Tung's model would predict. Even a single low SBH patch would not be able to reproduce the measured IV characteristics in this bias and temperature range, thus demonstrating the main limitation of the Tung model. To calculate the pinch-off effects and therefore the effective SBH and effective areas, Tung approximates a circular area of lower SBH using a single point-dipole and shows, that this approximation is well justified if the patch radius is much smaller than the semiconductor depletion width ($R_0 \ll W_d$). The intrinsic inhomogeneities are usually very small in size and consequently, meet this pre-request. The extrinsic inhomogeneities, however, originating mostly

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from external contaminations are assumed to be much larger, in the range of 10 to 100 nm in radius and cannot be approximated by a single point-dipole. An exact solution of the potential distribution underneath such semi-large patches is only possible by a numerical solution of the Poisson equation or in very good approximation by a dipole layer instead of a point-dipole, requesting high computing power. If the patches are large enough, they can be considered as not pinched-off and are describable with the parallel-conduction model and Equation (6.2). Sullivan and Tung came up with a condition whether pinch-off effects are occurring, depending on the patch radius, the patch SBH depth, the semiconductor doping, and the applied voltage

$$\frac{\Delta}{\psi_{\mathrm{bb}}} > \frac{2R_0}{W_d}.$$

(6.4)

In the case of the diodes investigated in this study, the extrinsic SBH patches are likely in a range where they fulfill this condition depending on the applied bias, but still the condition $R_0 << W_d$ is not fulfilled in most cases. Due to the combination of doping concentration and size of the extrinsic low SBH patches, a treatment as only pinched-off is just as impossible as a treatment as only not pinched-off. In order to continue working with the classic Tung model, the following workaround was chosen. In the Eqs. (6.2) and (6.3) the parameter P_{po} is introduced as a weight function of the pinch-off to not pinch-off ratio. $P_{\mathrm{po}}(R_{\mathrm{crit}}/R_0) = 1$ is equivalent to 100% of the patches being affected by pinched-off at a certain voltage and patch parameter. For the weight function P_{po} several functions have been tested. By requesting some basic conditions like being a differentiable function, $P_{\mathrm{po}}(R_{\mathrm{crit}}/R_0 << 1) = 0$, $P_{\mathrm{po}}(R_{\mathrm{crit}}/R_0 >> 1) = 1$, and $P_{\mathrm{po}}(R_{\mathrm{crit}}/R_0 = 1) = 0.5$ the cumulative distribution function of the log-normal distribution was chosen as weight function. It is defined as
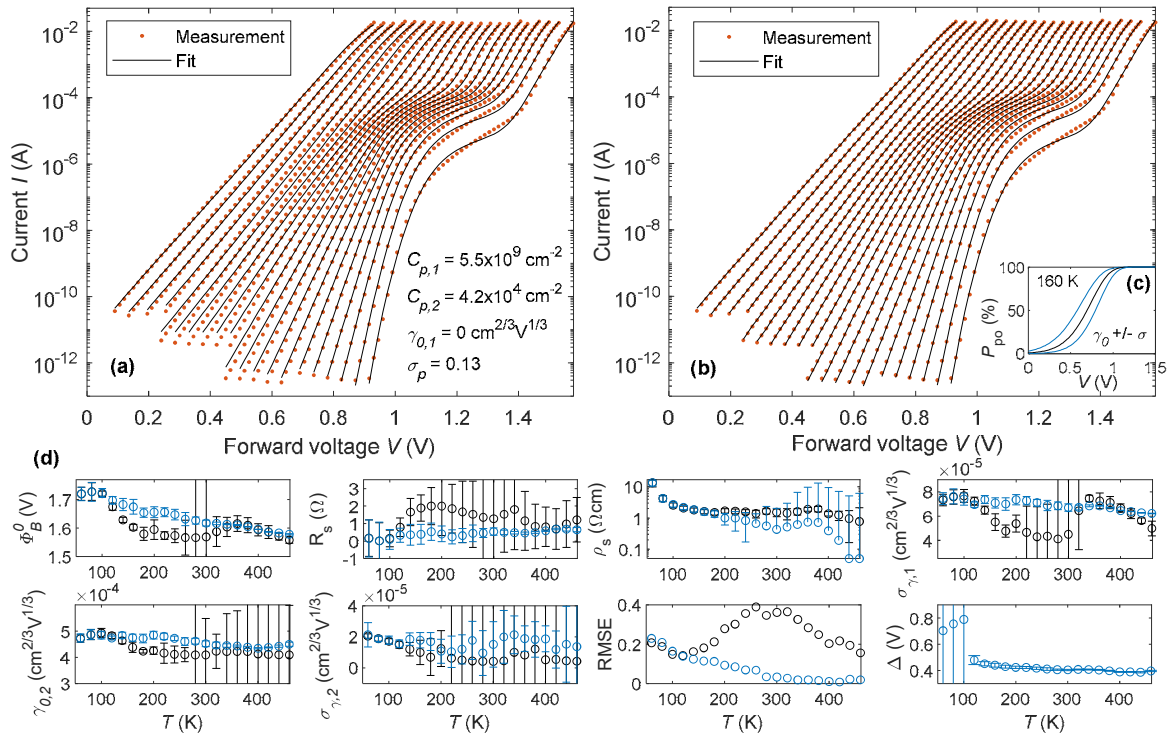
Figure 6.12: (a) Measured data and least-squares fit of the 1000 °C annealed sample. (b) Same data as in (a) while the fit considers the not pinched-off patches. (c) Weight function for pinch-off to not pinch-off ratio. (d) Fitting parameters as a function of temperature. Black belongs to (a); blue belong to (b). The temperature-independent fit parameters are the same and are labeled in (a). Error bars indicate the 95 percent confidence interval of each fitting parameter.

$$P_{\text{po}} = \frac{1}{2} + \frac{1}{2}\,\text{erf}\left(\frac{\ln(R_{\text{crit}}/R_0)}{\sqrt{2}\sigma_p}\right), \tag{6.5}$$

where $R_{\text{crit}} = \Delta W_d/2\psi_{\text{bb}}$ follows from Eq. (6.4) and indicates the critical radius where pinch-off is assumed to occur and σ_p is a shape parameter used in the log-normal distribution. Until now, R_0 and Δ were not distinguished, because of the use of the patch parameter γ. However, for considering the not pinched-off patches this has to be done. Therefore, Δ is now used as an additional fit parameter. Using Eq. (2.43) R_0 can be calculated for every γ_i. Another approximation that was done here is to assume Δ not to be of Gaussian distribution, but only the patch radius R_0. Assuming the extrinsic patches to be mainly of the same source of contamination, they may be of similar SBH but vary slightly in size. Now for every γ_i and every voltage V, P_{po} can be calculated, and the current contributions from Eqs. (6.2) and (6.3) can be weighted accordingly. Figure 6.12c shows P_{po} over V at $T = 160$ K for the mean patch parameter $\gamma_{0,2}$ plus/minus its standard deviation $\sigma_{\gamma2}$ used for a fit. As can be seen, the point where the patch radius $R_0 = R_{\text{crit}}$, hence $P_{\text{po}} = 0.5$ is at voltages where the IV curve is dominated by these patches, causing the fitting problems due to the assumption that all the patches are now pinched-off. The approach shown here is only a rough approximation, but it allows to continue the fit without affecting the other fit parameters e.g. the intrinsic inhomogeneities. Figure 6.12b shows the fitting results applying the new approach along with the fit parameters in Figure 6.12d in blue. The RMSE could significantly be reduced. The fluctuation and hence the confidence interval of the other fit parameters as a function of temperature could also be reduced giving more physically meaningful results. In the following the fit parameters, and their temperature dependence is analyzed for the second approach using a combination of pinch-off and not pinch-off patches. The temperature-independent values are labeled directly in the figure and are the same for both approaches. They have been determined iteratively by several fitting procedures until the overall RMSE was minimized.

High patch densities for the intrinsic inhomogeneities $C_{p,1}$ of around $5.5 \cdot 10^9$ cm^{-2} have been found which is similar to values reported earlier [117]. The extrinsic patch density is orders of magnitudes lower and about $4.2 \cdot 10^4$ cm^{-2}. Although the extrinsic patch size is in the range of to the grain size of the used poly-Si contacts [220], the low density of the extrinsic patches and the huge difference from the background ϕ_B^0 rules out any contribution of the grain structure of the poly-Si. The fit parameter σ_P determining the shape of the P_{po} function was found to be around 0.13. The background SBH ϕ_B^0 exhibits a slight temperature dependence, as expected due to the temperature dependence of the band gap and the Fermi levels. The series resistance R_s is rather fluctuating in its value, especially at low temperatures. This is due to the poor fit in the transition region, which results in a large scatter. Values in the range of 0.5 to 1 Ω with a slight increase with temperature seem reasonable, considering the two ohmic contacts plus the resistance of the needle contact. The bulk resistivity of the 4H-SiC epi-layer exhibits rater high values at the lowest temperature investigated. This can be attributed to carrier freeze-out and the error from the fitting procedure due to an increase of the ohmic current fraction above average in the transition region. Towards room temperature, the resistivity approaches 1 Ωcm, which is still too high for the used doping concentration [285], but it can be attributed to the abnormal curve shape in the transition region. Towards higher temperatures the impact of the resistivity to the overall curve shape decreases, which translates to higher uncertainties and fluctuating values. The standard deviation of the extrinsic inhomogeneities is slightly temperature-dependent and decreases from about $7.5 \cdot 10^{-5}$ cm$^{2/3}$V$^{1/3}$ to about $6.1 \cdot 10^{-5}$ cm$^{2/3}$V$^{1/3}$. This decrease is in line with the decrease of ϕ_B^0. The mean value and the standard deviation $\gamma_{0,2}$ of the extrinsic patches are constant in the whole temperature range at around $4.7 \cdot 10^{-4}$ cm$^{2/3}$V$^{1/3}$, whereas its standard deviation $\sigma_{\gamma,2}$ starts to show strong uncertainties at $T > 200$ K, where the influence of the extrinsic inhomogeneities starts to diminish. The last fit parameter is Δ and is estimated to be around 0.4 V to 0.5 V. At very low temperatures its uncertainty strongly increases because the patches at low temperatures are mainly pinched-off and this parameter does not contribute to the IV shape anymore.

The measured IVT curves could be fitted quite accurately using Tung's model and a double Gaussian distribution for the intrinsic and extrinsic inhomogeneities, respectively. The extracted parameters of the extrinsic inhomogeneities must be considered with care in the temperature range of about 160 K to 400 K where the approximation with the weight function is used. But, the course of the fit parameters is very uniform over the whole temperature range, independent if this range is dominated by the approximation or not. This gives confidence in the validity of the assumptions and approximations made.

6.3.4 Fit using three Gaussian distributions

In addition, an attempt to fit the representative diode annealed at 900 °C was done, as illustrated in Figure 6.8a. It shows a more complex characteristic with three bumps in the IV data. Therefore, three Gaussian distributions are assumed to be necessary for accurate modeling, based on the parameters listed in Table 6.2. Due to the reasons explained above only the new approach, assuming a partial pinch-off of the extrinsic SBH patches is implemented. Figure 6.13a shows the measurement data points together with the reproduced curves and the temperature-independent parameters. Those being temperature-dependent are shown in Figure 6.13b. The measured data could be modeled very accurately by three independent Gaussian distribution functions, as the maximum RMSE was with 0.057 even lower than at the device annealed at 1000 °C (RMSE: 0.23). The intrinsic patch density was found to be in the same
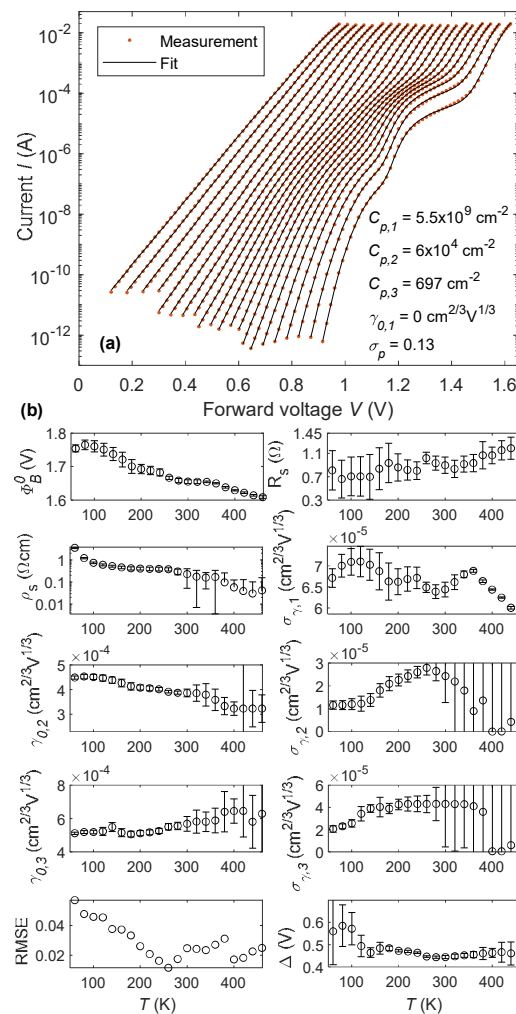
Figure 6.13: (a) Measured data and least-squares fit of the 900 °C annealed sample. (b) Fitting parameters as a function of temperature. Error bars indicate the 95 percent confidence interval of each fitting parameter.

order as in the previous sample, and the first extrinsic distribution was found to be about 40% higher. Also, their mean values and standard deviations are comparable to the previous fit. Due to the two bumps at lower currents, the problem with the transition region is much less pronounced, allowing a more accurate fit at low temperatures. Now the resistivity value starts at values slightly above 1 Ωcm at the lowest temperature investigated. Towards room temperature a very realistic value, for the used doping concentration, in the range of 0.4 Ωcm is found. At even higher temperatures the fluctuations and the confidence interval increase due to the limited influence of the parameter at high temperatures. The additional third distribution, only present in this sample, shows a patch density of around 700 cm^{-2}. With an active diode area of 0.5 mm^2, this translates to only 3.5 patches. This rather low patch density explains why this third bump is only visible in some of the measured diodes. The possibility to extract the patch density is a good measure to compare different manufacturing processes in terms of their influence on the low SBH patch densities. The remaining temperature-dependent fit parameters show the same trend and comparable values as the ones of the previous fit. Starting at about 300 K the confidence intervals of certain fitting parameters indicate a transition between two temperature regimes. At low temperatures, the IV characteristic is predominantly shaped by the extrinsic inhomogeneities. The fitting parameters of the intrinsic parameters have a marginal influence on the IV curve which results in larger confidence intervals. At high temperatures, however, the IV curve is mainly shaped by both the intrinsic inhomogeneities and the background barrier resulting in large fluctuations in the extrinsic fitting parameters. Despite the three Gaussian distributions of patches modeled here, small amounts of patches with randomly distributed SBH must be assumed to be present in every SC, causing additional uncertainties in all evaluation methods.

6.3.5 Comparison of barrier heights

Figure 6.14 shows a comparison of the SBH using different evaluation methods on the same two heterojunction diodes. Using the proposed fitting model, the background barrier ϕ_B^0 could be evaluated using the measured IVT data at all temperatures, even if strong non-idealities were present. The TE IVT data show strong deviations from the CVT evaluated SBH, whereas the latter show higher values across the whole temperature range, as expected. Only at higher temperatures, they start to approach similar values. This often-seen deviation is due to the current flowing predominantly through the lowest SBHs present at the interface. The SBH evaluated by IVT data is, therefore, reflecting the effective barrier height a device will have in real-world applications, but due to the unknown effective area, this SBH value is physically rather questionable and not well suited for comparing different Schottky diodes. Although evaluated using completely different methods, the SBHs from CVT measurements and the ones from the IVT data using the fit of the Tung model deviate only by a maximum of 4% across a temperature range of 400 K. This is regarded as a most excellent result given the influence of image force lowering and interface defects to the CV data. In addition, a decrease of about 140 mV in SBH is determined between 60 and 460 K, based on the temperature-related band gap and Fermi level changes of the two semiconductors, thus providing again confidence for the validity of the used method and the other evaluated parameters. This high degree of agreement also justifies the use of the chosen weight function to account for the weakness of the Tung model to deal with the presence of medium-sized patches.
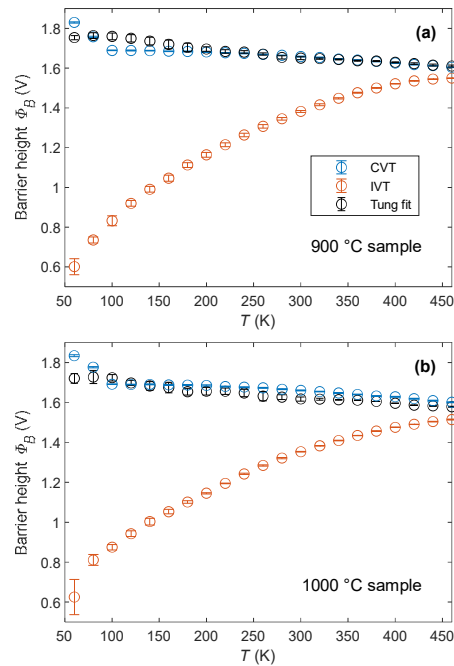
Figure 6.14: Comparison of the SBHs gained from IVT data evaluated by thermionic emission theory, IVT data evaluated by the Tung model and by CVT data. Shown are the two representative diodes annealed at (a) 900 °C and (b) 1000 °C.

6.3.6   Conclusions

Using the heterojunction p-Si/n-4H-SiC, the realization of diodes with a rather high SBH in the range of 1.65 V was possible, promising excellent rectifying properties. IVT characterizations in forward direction between 60 and 460 K revealed many nonidealities in the IV curve, especially at lower temperatures. This finding together with the deviation of the extracted SBHs between IVT and CVT indicated the presence of SBH inhomogeneities at the interface. As a consequence, this heterojunction architecture with its rather high SBH is ideal to analyze the influence of patches with low SBH on the device characteristics. Comparisons with theoretical predictions showed at least two separate types of inhomogeneities. Inhomogeneities with a low density and low SBH are assumed to be of predominantly extrinsic source due to e.g. local contaminations. In contrast, inhomogeneities with a higher concentration and a mean SBH around the background SBH are assumed to be of intrinsic source. Tung's model of inhomogeneous SCs was applied to fit the measured data. Depending on the shape of the IV curves, two, or even three Gaussian distributions of SBHs in form of Tung's patch parameter were used for fitting. Due to the relatively large size of the extrinsic patches in combination with the rather high doping level in the depletion layer, the Tung model started to fail at these temperatures. A combination of pinched-off and not pinched-off patches together with a weight function was implemented as a workaround, resulting in excellent fitting results. This approach enabled the estimation of both the densities and the patch parameters of the different patch distributions as well as to extract physically meaningful values for the background SBH from quite distorted IV curves even at low temperatures. The intrinsic patch densities were found to be about $5.5 \cdot 10^9$ cm^{-2}, whereas the extrinsic densities were orders of magnitudes lower. In case of the diode with three pronounced bumps only 3.5 patches per diode were found to be responsible for the lowest IV bump. The extracted densities can be used as measures to find and reduce low SBH contaminations depending on different process parameters. A comparison with the CVT extracted SBH values gives confidence in the validity of this approach across a wide temperature range of 400 K. In the near future, Schottky-type interfaces with defined, local

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inhomogeneities generated artificially on SiC substrates with different doping levels and a comparison of the fitted model with BEEM measurements would give more insight in the electrical device performance to verify the validity of the assumptions and approximations made for modeling the experimental data.

6.4 LPCVD heterojunction-diodes

Parts of this section have been published in [242]

To study the quality of the LPCVD grown Si/4H-SiC heterostructures of Section 4.3 electrically, heterojunction diodes were fabricated by applying spin-on dopants to form n+-Si/n-4H-SiC and p+-Si/n-4H-SiC junctions. At a dopant drive-in temperature of 1000 °C any active doping of the 4H-SiC, which usually requires temperatures in excess of 1500 °C for diffusion and activation can be neglected [255], [256]. The Si is highly doped to serve as Schottky contact so that the complete band bending is confined in the SiC epitaxial layer and the Si top contact can be electrically connected by a needle prober. Although it increases the series resistance, no additional top metallization was used, as it would short-cut the Si on the sample with non-closed film regions. A backside ohmic contact was realized using Ti/Pt and a 1000 °C annealing step for 1 min.

6.4.1 Results and discussion

Room temperature IV measurements of the fabricated diodes are depicted in Figure 6.15, for both n- and p-type silicon. One interesting feature is the strong dependence of the IV characteristic on the
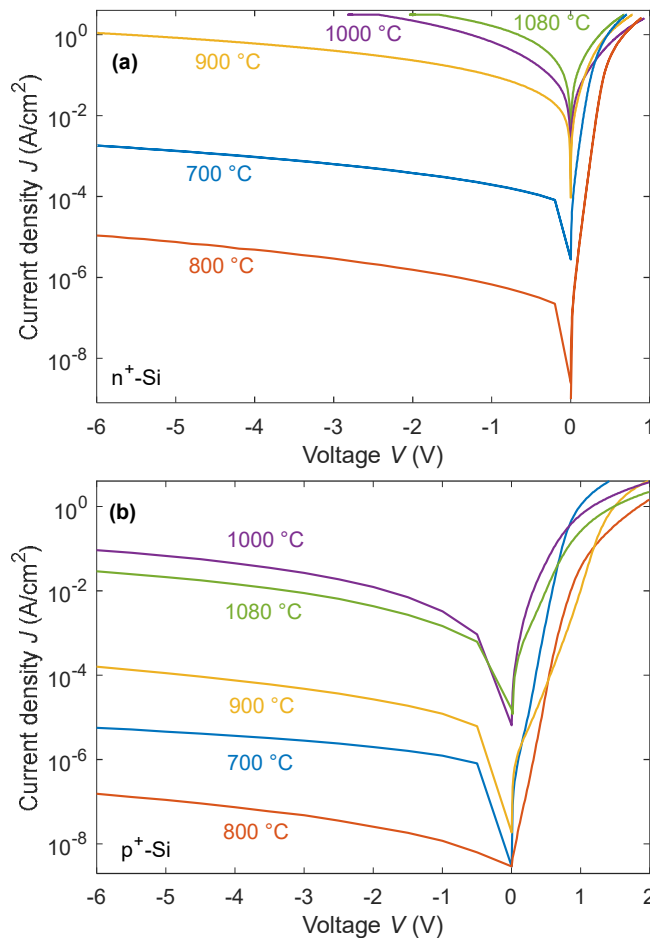
Figure 6.15: IV measurements of (a) n+-Si/n-4H-SiC and (b) p+-Si/n-4H-SiC heterojunction diodes with different Si deposition temperatures.
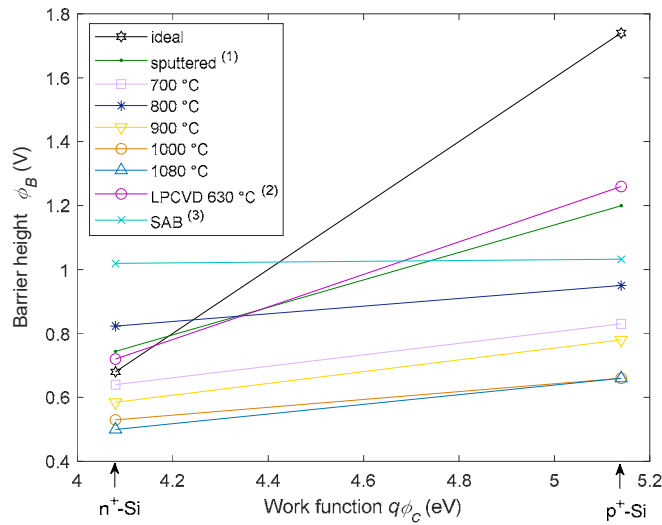
Figure 6.16: Plot of the SBH over semiconductor work function for n and p-type Si/n-4H-SiC contacts. Along with the calculated ideal curve and the five diodes produced in this study the plot includes: (1) own measurements of sputter-deposited and post annealed Si contacts [286], (2) low temperature (630 °C) LPCVD deposited poly-Si contacts [38], and (3) SAB fabricated and post annealed contacts (SBH was extracted from the IV plots) [46].

LPCVD deposition temperature. The sample deposited at 800 °C showed the lowest leakage currents and hence, the highest SBH ϕ_B for both n- and p-Si, followed by the 700 °C deposited sample. With higher deposition temperatures the leakage current levels increased, whereas the p-Si showed lower leakage currents than the n-Si, which is expected, due to the larger work function of p-Si compared to n-Si. The n-Si/4H-SiC HJD deposited at 800 °C has with about 1.14 the best ideality factor among these LPCVD HJDs. It is in the range of the HJDs realized by sputter-deposition and specific PDA, respectively.

Under the presence of FLP, the dependence of the SBH on the contact work function for n-type semiconductors (n-type SiC) can be expressed using Equation (2.36) with the S-parameter ($S = S_{GS}$).

$S = 1$ would lead to the ideal Schottky-Mott relation. The SBHs of all IV measurements are evaluated with the thermionic emission current model and are plotted in Figure 6.16 as a function of the work function $q\phi_c$ of the Si contact. The work functions were calculated for n+- and p+-type Si assuming a doping concentration of $2.6 \cdot 10^{19}$ cm^{-3}. This assumption is satisfactory as a variation of one order of magnitude more or less would only translate to an error in ϕ_c of max. +/- 0.08 V. Despite the data of the five different deposition temperatures of this study, additional data points were added from standard literature for reasons of comparison. The theoretically predicted curve was calculated with a χ_s of 3.3 V [138] for 4H-SiC, which represents an average among the widespread of reported values. SBHs from sputter-deposited highly n- and p-doped Si/4H-SiC heterojunction diodes produced in our lab were included [286]. LPCVD heterojunctions deposited at 630 °C from Henning et al. [38], as well as heterojunction diodes, prepared based on SAB were also inserted in Figure 6.16 [46].
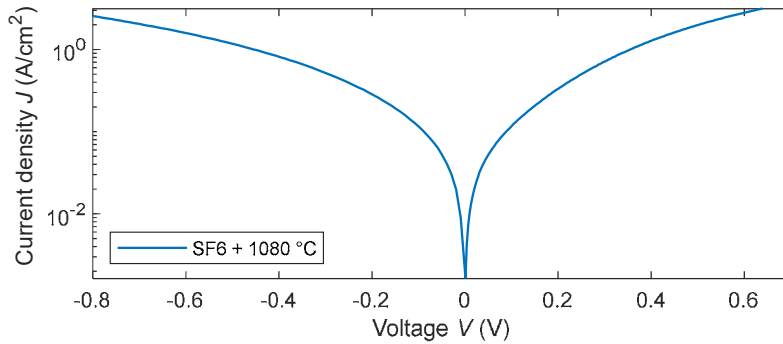
Figure 6.17: Room temperature IV characteristic of the LPCVD sample with SF$_6$ pre-treatment.

Next, the *S*-parameter was extracted from the slopes in Figure 6.16 according to Equation (2.35) and the CNL was calculated using Equation (2.36). Although the extraction of a slope from a straight line which is based only on two data points gives rise to uncertainty, this approach provides a good estimation due to the large $\Delta\phi_c$ of the oppositely doped Si contacts used in all these studies. The ideal case results in SBHs of 0.78 V for n$^+$-Si and 1.84 V for p$^+$-Si, with an *S*-parameter of 1. The *S*-parameter and the CNL of the samples depicted in Figure 6.16 are given in Table 6.3. The samples with the highest *S*-parameters of 0.51 and 0.43 are the LPCVD sample of Henning et al. and the sputter-deposited sample, respectively. The SBHs of the n$^+$-Si contacts almost meet the expected ideal SBH value, whereas the p$^+$-Si SBHs of these two contacts are well below the expected ideal value, this might also be due to the strong influence of SBH inhomogeneities on IV measured SBH [94]. All the LPCVD samples from this study show quite low *S*-parameters between 0.12 and 0.18. The highest pinning effect resulting in an *S* of about 0.012 is extracted from the diodes produced by SAB. The calculated CNL does not vary that much and is centered around 2.5 V above the valence band edge. For reference, the calculated Fermi level of the 4H-SiC epitaxial layer with $N_D = 2.6 \cdot 10^{16}$ cm^{-3} is about 3.05 V above the valence band edge at room temperature.

A possible cause for the observed FLP is the presence of high amounts of unsaturated or polarized bonds at the interface, giving rise to an interface dipole layer [95]. A similar strong FLP was observed on 4H-SiC being subject to high-temperature treatments resulting in surface graphitization [287], [288]. Although the temperatures used in this work are not high enough to allow the formation of such graphene-like, C-rich buffer layer, the reasons for the observed FLP might be similar.

The presence of high amounts of unsaturated dangling bonds at the interface might be responsible for the FLP. As described in Chapter 4, the heteroepitaxial Si/4H-SiC interface has a large lattice mismatch, but a good domain matching with domain sizes of 4:5 and 1:2 depending on the Si orientation. Li et al. [219] calculated the misfit dislocation densities of the Si{111}/xH-SiC{0001} and Si{110}/xH-SiC{0001} heterostructures with in-plane orientations like depicted in Figure 4.1 to be $4.87 \cdot 10^{13}$ cm^{-2} and $1.22 \cdot 10^{14}$ cm^{-2}, respectively. The high density of misfit dislocations in epitaxial Si/4H-SiC heterojunctions can explain the measured IV characteristics. The higher the degree of epitaxy, the higher the density of misfit dislocations, hence electrically active interface traps. Low-temperature depositions did not form a heteroepitaxial connection to the SiC, maintaining its stable surface reconstruction with fewer interface defects. This effect can also be used to intentionally adjust the SBH

Table 6.3: Extracted *S*-parameter and charge neutrality level using Figure 6.16.

	Sputtered	**700 °C**	**800 °C**	**900 °C**	**1000 °C**	**1080 °C**	**LPCVD**	**SAB**
S	0.43	0.18	0.12	0.18	0.12	0.15	0.51	0.012
ϕ_{CNL}	2.51	2.62	2.4	2.69	2.74	2.78	2.57	2.21

via the Si deposition temperature. At the highest deposition temperature, almost ohmic behavior could be achieved using n-Si on a low doped epitaxial 4H-SiC layer.

The LPCVD sample, which underwent SF_6 pre-treatment followed by 1080 °C Si deposition was also electrically characterized and is shown in Figure 6.17. It shows no more rectifying IV characteristics anymore. The rectification ratio, taken at -0.5 V and 0.5 V, is calculated to be 1.7. The reason for this almost ohmic contact behavior remains open. It could be seen as an extreme case of FLP, whereas the CNL must be high enough, to result in a very low barrier. The extremely rough, but still epitaxial interface might give rise to a large number of defects, resulting in strong FLP. Because the etch rate of the SF_6 treatment is unknown, the low doped epitaxial layer might be etched completely, resulting in a Si/4H-SiC heterojunction on highly doped SiC. This, in combination with strong FLP, could explain the almost symmetric IV characteristic. Due to the unsatisfactory results, regarding the interface quality (etch damage) and the IV characteristic, not suitable for heterojunction formation, the SF_6 treatment was not further investigated. The results suggest a possible use for ohmic contacts. Further investigation of the involved etch process, the influence on the Si growth, and the interface chemistry of SF_6 are required.

6.4.2 Conclusion

Electrical characterizations of n^+-Si/n-4H-SiC and p^+-Si/n-4H-SiC heterojunctions prepared by spin-on doping of the Si showed a strong dependence of the rectifying properties with Si deposition temperature. Higher deposition temperatures resulted in lower barrier heights, hence higher reverse leakage currents. An evaluation of key parameters such as the *S*-parameter and the CNL and a comparison with Si/4H-SiC heterojunction prepared by other approaches suggested a strong increase of FLP with the degree of heteroepitaxy. The highest FLP was found at samples fabricated by SAB, followed by those deposited at the highest LPCVD temperature. High densities of misfit dislocations due to the large lattice mismatch are assumed to be responsible for high interface state densities resulting in strong FLP. Different pre-deposition treatments and variations in other LPCVD parameters, like pressure or gas flow ratios might reduce the strong influence on the deposition temperature. Using SF_6 pre-treatment, almost ohmic device characteristics were found, although introducing strong etch damage, limiting the usage in real device structures. Nevertheless, heterojunction diodes with pronounced rectifying properties could be produced and the possibility to adjust the SBH by the deposition temperature might also be stated as beneficial to tailor the performance for future device applications.

6.5 MIC heterojunction diodes

As presented in Section 5.2.4, using very thin Al layers and low temperature annealing a very crystalline and substrate-oriented Si layer could be achieved in the interface near regions. One sample was annealed a second time at 800 °C for 24 h for complete crystallization and is depicted in Figure 5.18. This sample was further prepared as an HJD for electrical characterization. At first, all remaining Al on the surface was removed using phosphoric acid. Ti/Pt bilayers were sputter-deposited on the backside followed by a rapid thermal annealing step to form a good ohmic contact. On the front, Al electrodes were sputter-deposited and circular diode structures were etched. The poly-Si pads had a final diameter of 800 µm with centrally arranged 700 µm Al pads on top for better electrical contact. IVT and CVT measurements were made in a temperature range of 300 to 460 K in 20 K steps.

6.5.1 Results and discussion

The IVT data of the prepared HJD of the sample annealed at 275 °C for 105 h and at 800 °C for 24 h is depicted in Figure 6.18a at three measurement temperatures. A well-rectifying characteristic is present at all temperatures. In the forward direction a double bump is visible in the semi-logarithmic plot.
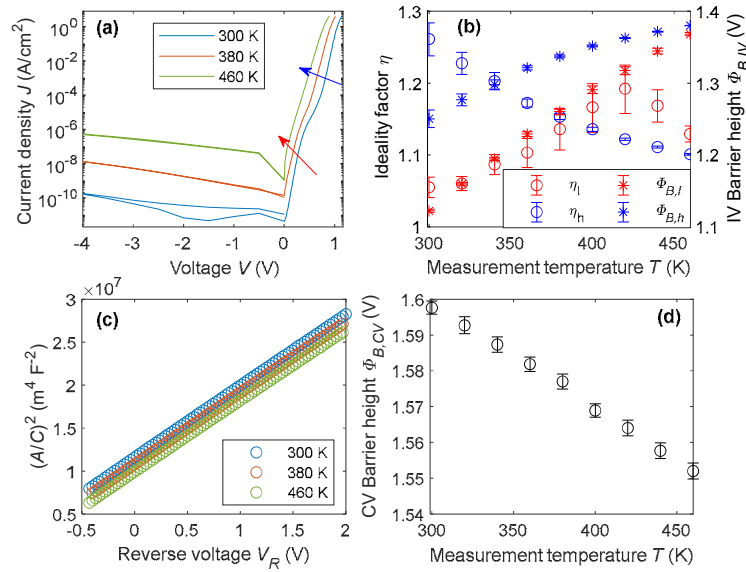
Figure 6.18: (a) IVT data of the manufactured heterojunction diode. (b) SBH and ideality factor η using two different current ranges of the IVT data for fitting. The used low "l" and high "h" current range are represented in (a) by the arrow and correspond to the used plot colors. (c) depicts the measured capacitance transformed for fitting along with the extracted SBH in (d).

Multiple bumps in the forward IV characteristic of Schottky or heterojunction diodes are frequently observed, like on the p-Si/4H-SiC heterojunctions characterized in Section 6.3 and can be attributed to an inhomogeneous SBH distribution at the interface [94], [125]. Although, it should not be as pronounced at room temperature if it is due to "normal" contaminations and is therefore attributed to the residual Al on the interface. This first strong increase at low forward voltages can be attributed to the Al-islands on the surface conducting the current (see Figure 5.18). The Al/4H-SiC Schottky junction has a much lower SBH than the p-Si/4H-SiC heterojunction [38], [289]. When the current through the Al/SiC junction becomes saturated, the IV curve starts to flatten again, before the actual p-Si/4H-SiC heterojunction starts to conduct. To evaluate the barrier height the thermionic emission equation was fitted in two current regions indicated by the blue and red arrow. The extracted SBHs ϕ_B and ideality factors η are plotted as a function of temperature in Figure 6.18b. In the low current region, where the Al islands mainly contribute to the current flow the barrier height is low, about 1.12 V at 300 K and increases almost linear towards 1.37 V at 460 K. The ideality factor starts with 1.05 at almost unity, indicating the presence of a high-quality Al/4H-SiC junction. With increasing contributions of the p-Si/4H-SiC junction, the ideality factor first increases towards 1.19 before it decreases again to about 1.12 at the maximum temperature of 460 K. The extracted data of the high current region (blue arrow in Figure 6.18a) almost only reflects the p-Si/4H-SiC heterojunction. The SBH starts at much higher values at about 1.25 V and increases towards 1.38 V. The ideality factor is also higher, starting at about 1.27 and approaching 1.1 at 460 K.

Also, CVT measurements using a test frequency of 1 MHz are conducted. The measured capacitance is plotted in the form of A^2/C^2 in Figure 6.18c for three temperatures. This plot is used for linear fitting and extraction of the SBH. The CVT-determined SBHs are plotted in Figure 6.18d as a function of temperature. The SBH decreases slightly with temperature as was measured before (see Figure 6.11) and is higher than the IV SBH at all temperatures. This is due to the presence of SBH inhomogeneities. The SBH extracted using IV techniques needs to be considered as effective SBH, whereas the CV SBH can be seen as average SBH [55], [122], [125]. With CV SBH values between 1.6 and 1.55 V, it is about

0.1 V lower than the CV SBHs evaluated using boron doped p-Si/4H-SiC heterojunction [94], the slightly lower SBH might be due to a lower active dopant concentration in the Si film.

6.5.2 Conclusion

A Si/4H-SiC HJD was successfully prepared using MIC. A very thin Al layer, resulting in an almost epitaxial interface with low densities of residual Al, followed by a high-temperature annealing step for complete crystallization were applied. IV and CV measurements revealed good rectifying properties, although small amounts of Al still in contact with the substrate are responsible for a strong increase in the forward IV curve at low voltages, due to the low SBH of the Al/4H-SiC junction. The usage of very thin Al layers is promising, enabling the characterization of first device prototypes. Nevertheless, further investigations to reduce the amount of residual Al at the interface are necessary. Different deposition parameters resulting in a higher GB density and the variation of the Al film thickness are only two parameters that need to be adjusted carefully.

6.6 Ion sputter etching to adjust the SBH

Parts of this section have been published in [286]

This section will focus on an experimental series about the influence of ISE treatment on the 4H-SiC surface prior to Si deposition to form Si/4H-SiC HJDs.

Besides the choice of the top contact material, the influence of surface cleaning and surface treatment on the SBH has been extensively investigated [290]–[292]. Also, ultrathin intermediate layers [293], [294], [108], [110] and ion bombardment of the surface prior to metal deposition have been performed [295], [296], [106], [109], [297]. In summary, the conclusion can be made that surface treatments to remove contaminations and oxides from the interface are crucial and thermal annealing strongly balances the influence of different surface preparation techniques. But, the main drawback of ion bombardment is that amorphous regions with high defect densities are generated which results in strong FLP [106], [109]. This approach of artificial FLP can be used to adjust the SBH if the unpinned junction is very high or low, or if the Fermi level is pinned close to the band-edges [97], [298].

Si/4H-SiC heterojunctions fabricated by surface-activated bonding showed a rather low impact on the Si doping type, which can be attributed to strong FLP [43], [46]. Due to the huge difference in band gap between Si and 4H-SiC, rather large conduction as well as valence band offsets of about $\Delta E_C \sim 0.5$ eV and $\Delta E_V \sim 1.5$ eV result. This translates to rather high SBHs in the range of 1.5 to 2 V for the p-Si/n-4H-SiC and rather low SBHs of about 0.8 V, and hence high leakage currents, for the n-Si/n-4H-SiC heterojunction [38], [48], [94]. An approach for adjusting the SBH in the wide range between 0.8 and 1.8 V and simultaneously reducing the impact of SBH inhomogeneities at the interface could stimulate further research activities within the broad application spectrum of Si/4H-SiC heterojunction devices, like diodes [39]–[48], switches [51], [52] or photodetectors [49], [50].

In this experimental study, the influence of ISE as a standard surface cleaning technique on the electrical properties of both n and p-Si/4H-SiC junctions was investigated, whereas top contact formation was achieved by silicon sputter-deposition and subsequent post-deposition annealing. The advantage of using sputter-deposition rather than the more common chemical vapor deposition of silicon is, that most of the modern sputtering equipment is equipped with an integrated ISE unit. Despite a surface-near amorphization due to the Ar ion bombardment, this allows *in-situ* cleaning of e.g. 4H-SiC substrates followed by a-Si layer deposition without breaking the vacuum. The results are split into two parts, in the first part simulation and experimental results of the ISE sputtering process on 4H-SiC are presented.

Table 6.4: ISE parameters with simulated ion penetration depths and its standard deviations (SD) in SiC, as well as the measured thickness of the amorphous region and the experimental ISE etch rates.

RF-ISE power (W)	ISE time (s)	Self-bias Voltage V_{DC} (V)	Mean penetration depth t and its SD (nm)	Measured amorphous region thickness (nm)	Etch rate (nm/min)
50	5, 15, 45, 135	515	1.8 / 0.6	not measured	0.83
200	5, 15, 45, 135	1030	2.5 / 0.9	3.1	2.86
600	15	1650	3.3 / 1.2	4.15	6

The second part focuses on the influence of different ISE treatments on electrical key parameters of poly-Si/4H-SiC HJDs.

6.6.1 Experimental details

4H-SiC substrates from Cree Inc. with 4° off-axis cut were used for the experiments. The bulk resistivity was 0.015 to 0.028 Ωcm n-type with a 5 µm thick epitaxial layer on the Si-face with about $N_D = 1.6 \cdot 10^{16}$ cm^{-3}. The cleaned substrates were placed in the sputtering system, with the Si-face up where ISE sputtering was performed using a 13.56 MHz radio-frequency (RF)-plasma according to the parameters listed in Table 6.4. The common parameters comprised a chamber pressure p = 0.5 Pa, a gas flow of 60 sccm Ar and a target-substrate distance of 65 mm. Due to the construction of the plasma chamber, the ionized Ar$^+$ atoms are accelerated towards a grounded extraction grid with an acceleration voltage of approximately V_{DC}, which is monitored by the RF-generator. This acceleration voltage can be used to estimate the maximum ion energy of the Ar$^+$, when bombarding the substrate surface. This maximum energy has been used to estimate the penetration depth, as well as sputter yields of SiC using SRIM-2013 [299].

For every ISE parameter, two samples were manufactured to form p-Si/4H-SiC and n-Si/4H-SiC heterostructures. In addition, samples without ISE were fabricated as references. Directly after ISE, without breaking the vacuum, 700 nm of a-Si were sputter-deposited from either a highly boron or a phosphorus-doped Si target. After deposition, the samples underwent a PDA at 1000 °C for 2 h to crystallize the a-Si and to annihilate structural damages in the SiC due to ion bombardment [220]. Two samples were prepared using lower PDA temperatures of 800 and 900 °C for 2 h, respectively. For diode fabrication, Ti/Pt ohmic contacts were formed on the back using rapid thermal annealing at 1000 °C for 1 min.

As the n-type Si turned out to be not conductive enough, an additional doping step using a phosphorus-containing spin-on dopant was applied followed by drive-in annealing at 1000 °C for 1.5 h. Finally, circular pads were patterned to form individual diodes with a diameter of 800 µm.

To perform SRIM simulations a mean value of 3 g/cm^3 has been implemented for the density which is in between amorphous and crystalline SiC. Surface and bulk binding energies of amorphous SiC have been assumed as $E_{Si,bulk}$ = 6.6 eV, $E_{C,bulk}$ = 10.2 eV, $E_{Si,surf}$ = 4.7 eV and $E_{C,bulk}$ = 7.4 eV [300], whereas displacement energies are $E_{d,Si}$ = 41 eV, $E_{d,C}$ = 16 eV [301] for silicon and carbon atoms, respectively.

To determine the sputter etch rate during ISE, parts of the surface have been masked with about 4 µm thick photoresist followed by ISE etching for several minutes. After removal of the mask, the etched steps have been measured using an atomic force microscope.

TEM measurements were performed at an acceleration voltage of 200 kV. IVT and CVT measurements were done with a Keysight B2985A electrometer and with an Agilent 4294A high precision impedance analyzer at 1 MHz test frequency in a voltage range of -2 to 1 V, respectively.

6.6.2 Ion sputter etching and interface formation

SRIM simulations with the parameters given in the experimental section were conducted to estimate the thickness of the amorphous region in dependence on the ISE power. When applying the self-bias voltage V_{DC} as an indicator for the maximum ion energy the penetration depths listed in Table 6.4 were obtained. Due to the Gaussian-like depth profile, the mean depth together with the standard deviation (SD) are given. The maximum thickness of the amorphous layer formed by ISE is expected to be the mean depth plus one SD. Additionally, the sputter yield of the impinging ions under perpendicular incidence (i.e. 0° to the surface normal) with respect to the substrate is calculated. The actual angle might vary between -20° and +20° due to ion scattering in the plasma. Simulations show sputter yields for $E_{Ion} = 510$ eV of
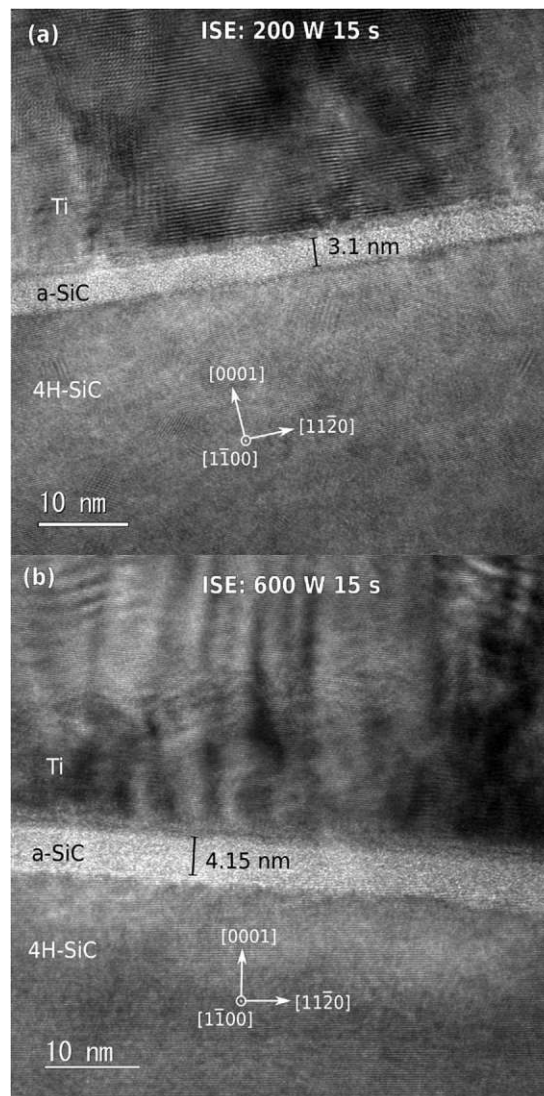
Figure 6.19: HRTEM images of 4H-SiC surfaces after ISE treatments (a) 200 W for 15 s and (b) 600 W for 15 s. For a better contrast of the amorphous region, a Ti layer was sputtered on top. The 4H-SiC region in (a) shows some lattice distortions (circular fringes with Moiré pattern), that are attributed to copper re-deposition during sample preparation.
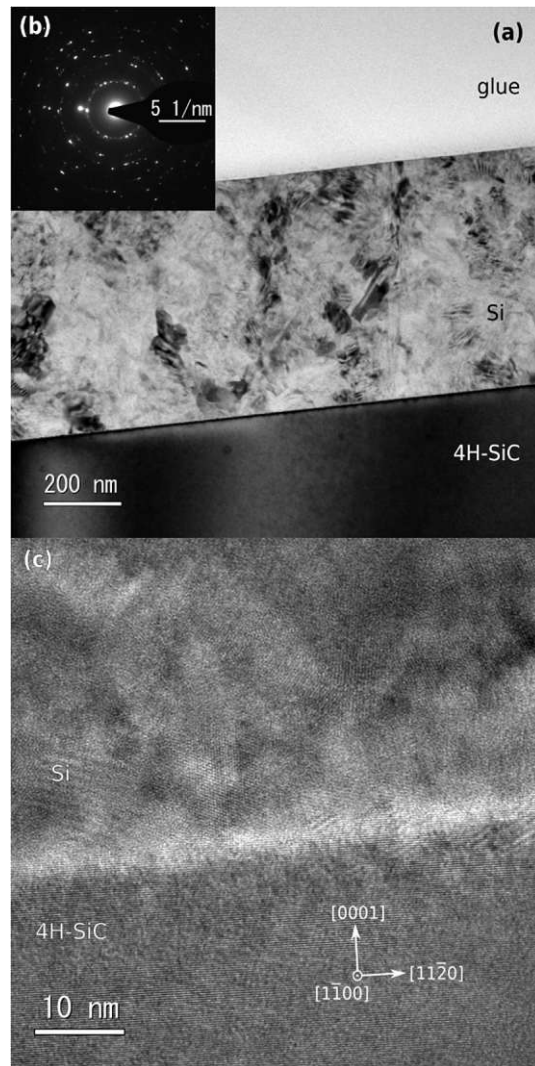
Figure 6.20: TEM images of the sample with 200 W for 15 s ISE after p-Si deposition and annealing at 1000 °C. (a) Overview with (b) a SAED pattern of the Si film and (c) HRTEM of the interface region.

0.26 atoms/ion in total and 0.17 atoms/ion and 0.09 atoms/ion for Si and C, respectively. The yields increase with increasing ion energy, but the Si/C ratio stays rather constant at about 2. The higher sputter yield of Si follows from the lower surface binding energy and was confirmed experimentally [300], [302]–[304]. To verify the calculated penetration depths TEM measurements of samples treated with 200 W for 15 s and 600 W for 15 s with ISE have been performed. High-resolution transmission electron images of those two samples are depicted in Figure 6.19. A Ti layer was deposited on the sample after ISE treatment to have a better contrast for TEM imaging. The sample with 50 W ISE was not prepared for TEM, the amorphous layer is expected to be too thin for accurate thickness measurements. The measured values of the latter parameter are also given in Table 6.4 and are in excellent accordance with the simulated penetration depths when assuming an amorphization introduced at the mean depth plus one SD.

Additionally, the ISE-related etch rate is measured and given in Table 6.4. With etch rates as low as 0.83 nm/min, the removal of material is almost negligible at 50 W for 5 s. Nevertheless, at higher ISE powers and longer sputter times, a few nanometers are removed from the surface besides to the amorphization.

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A sample with 200 W and 15 s ISE treatment followed by a 700 nm sputter-deposited a-Si and annealing at 1000 °C is also investigated with TEM. Figure 6.20a shows an overview image of the whole Si film and in the inset (b) a SAED pattern taken from the Si film. The Si film completely crystallized during the high-temperature annealing step and shows a polycrystalline microstructure with very low surface roughness. An HRTEM image of the interface region is depicted in Figure 6.20c. A comparison to the *as-deposited* state, given in Figure 6.19a, shows that the originally more than 3 nm thin amorphous SiC interface layer is no more present. The a-Si/a-SiC/4H-SiC interface transformed into a poly-Si/4H-SiC interface without a sharp, but a blurred transition characteristic. The formation must be attributed to the ISE treatment prior to a-Si deposition. The crystallization behavior of sputter-deposited a-Si on 4H-SiC was investigated before without ISE treatment up to 1100 °C [220]. The Si films on untreated surfaces are polycrystalline with grain size and texture comparable to that of the surfaces treated with ISE, as shown in Figure 6.20a, but with a sharp and distinctive interface without any signs of chemical reactions nor any epitaxial connectivity (see Section 4.2 for comparison). A thorough investigation of the interface region of the ISE treated and recrystallized sample based on FFT diffraction patterns revealed lattice spacing values that could be attributed to 3C-SiC recrystallization directly at the interface. This assumption is supported by findings reported in [305], where amorphous SiC was found to recrystallize to cubic SiC at temperatures as low as 850 °C. It is although unclear if the whole a-SiC layer recrystallized to carbon enriched Si and 3C-SiC or if it partially recrystallized to 4H-SiC in a solid-phase crystallization process. The solid phase recrystallization of amorphized SiC induced by ion implantation was shown to occur at temperatures below 900 °C [306], [307] and is therefore definitely possible at an annealing temperature of 1000 °C. Due to the high-temperature load, it is reasonable to assume that both processes take place simultaneously. Although samples with different ISE powers and times are not investigated in TEM, a similar interface with complete recrystallization of all amorphous regions can be assumed after annealing at 1000 °C.

6.6.3 Electrical characterization

Heterojunction diodes with different ISE treatments and with either p- or n-type Si top contacts have been electrically characterized. Forward biased IV data at different measurement temperatures of a p-Si/4H-SiC diode without and with ISE (i.e. 200 W for 15 s) are depicted in Figure 6.21a and b, respectively. For the latter device, a shift towards lower voltage values is noticeable, as well as IV characteristics being closer to the ideal theoretical prediction. Assuming a thermionic emission current flow, which is valid if the Si is doped much higher than the SiC the IV behavior follows as described in Section 3.3.2.

Using the ISE treatment at 200 W for 15 s the SBH and the ideality factor could be reduced in the whole temperature range. At room temperature, the SBH decreased from about 1.22 to 1.10 V compared to no ISE, whereas the ideality factor decreased from 1.16 to 1.07. What is even more important is the change in the temperature dependence of the two parameters. The untreated sample has SBHs ranging from 1.22 to 1.37 eV in the temperature range of 300 to 420 K, whereas the ISE treated sample only varies from 1.10 to 1.13 V. This high parameter stability over the measurement temperature, as well as the good agreement to SBHs measured with CV, as shown in Figure 6.22 and Figure 6.23 indicate a locally low scatter in SBHs after ISE treatment.

For all ISE parameters, the IV SBH $\phi_{B,IV}$ and the ideality factor η were evaluated from forward-biased IV measurements and the CV SBH $\phi_{B,CV}$ from CV measurements at 1 MHz test frequency. The results for p-Si/4H-SiC HJDs are depicted in Figure 6.22. Clearly, the SBH is reduced independent of the ISE parameters compared to the reference sample without ISE treatment. The IV, as well as the CV, evaluated SBHs show a trend towards increasing values with increasing ISE time. If the SBHs at a constant ISE time of 15 s are compared, a decrease with ISE power is notable. The ideality factor also
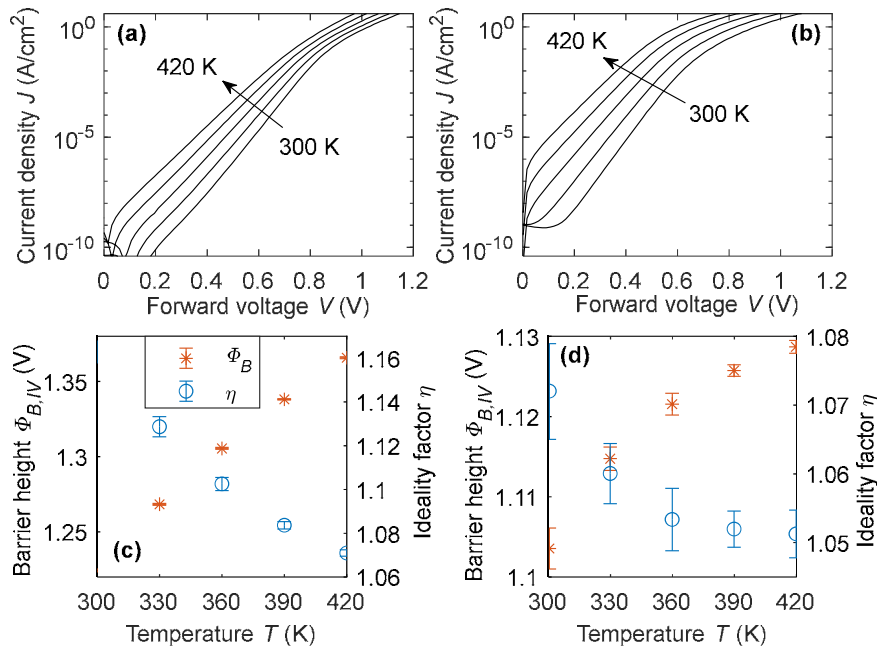
Figure 6.21: Forward biased IVT measurements of p-Si/4H-SiC heterojunction diodes (a) without and (b) with ISE (*i.e.* 200 W for 15 s) treatment. (c) and (d) present both the ideality factor and the SBH of the devices characterized in (a) and (b).

shows a slight dependence on the ISE parameters, namely an increase with time. The lowest ideality factors for all measurement temperatures are deduced from the 200 W sample at rather short ISE times. With a room temperature minimum of η of 1.06 using 200 W and 5 s ISE, the ideality factor could be reduced drastically from about 1.24 without any ISE treatment. Another important influence of ISE is the strong reduction of the temperature dependence of the ideality factor and the high consistency between IV and CV SBHs. Without ISE treatment, the IV SBHs show a strong temperature dependence and with average values of 1.2 V from IV and 1.68 V from CV characterization a huge discrepancy. This finding is frequently reported and is most likely attributed to a large local scatter in Schottky barrier height inhomogeneities [94], [122], [125]. A wide distribution of different SBHs, centered around the result from CV analysis is assumed to be present at the interface. Independent of ISE treatments, but especially when applying 200 W, this temperature dependence, and the deviation between IV and CV SBHs are reduced to a minimum. In detail, after an ISE treatment at 200 W for 5 s the IV-related SBH only varies between 1.088 and 1.109 V in a temperature range of 120 K. At 300 K, the IV and CV SBHs differ by only 86 mV.

The series resistance was also evaluated using Cheung's method as described in Section 3.3.2. No effort was made in lowering the device series resistance nor was the measurement setup optimized for measuring low resistance values. Nevertheless, a trend of increasing series resistance using ISE was found. From values around 0.7 Ω without ISE, the series resistance increased to around 3 Ω with ISE, but independent of the parameters. Also, the reverse characteristic was recorded up to -20 V, giving no unexpected behavior and is therefore not plotted. The amount of leakage current correlated with the extracted SBH, as is expected. Although no measures were taken to enhance the breakdown capabilities and the HJDs are simple planar contacts, they easily survived reverse bias voltages of -210 V, which was the maximum of the used test setup.

From the conducted investigations, it can be concluded that an RF power of 200 W and short ISE times seem to have the most promising effect on diode parameters like ideality factor and SBH homogeneity.

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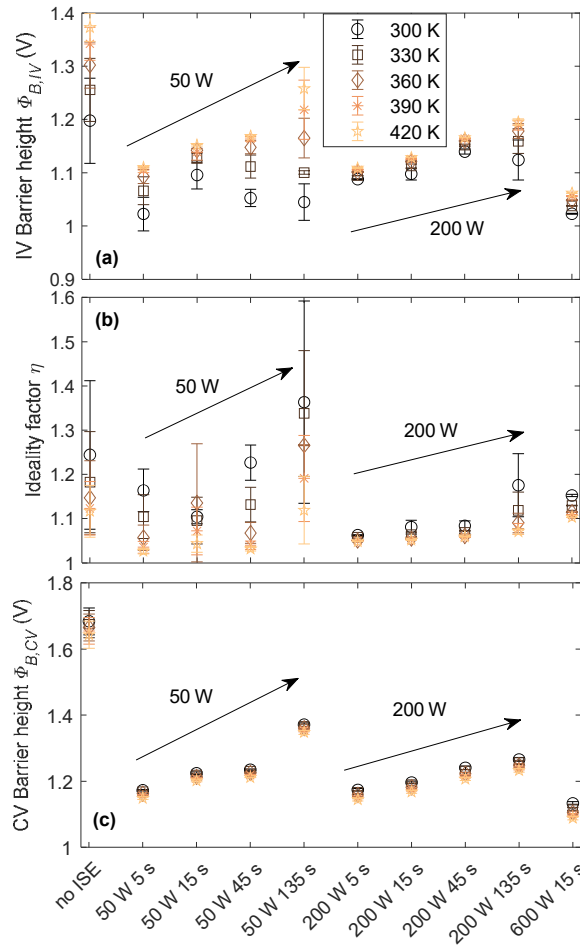
Figure 6.22: p-Si/4H-SiC diodes: (a) IV SBHs, (b) ideality factors η and (c) CV SBHs for various ISE parameters and temperatures. Every data point is averaged from three measured diodes, with the error bars representing the standard deviation.

The same data evaluation was performed on n-Si/4H-SiC HJDs and is depicted in Figure 6.23. As theory predicts, the SBH of the untreated sample is with around 0.7 to 0.8 V much lower than those with a p-type Si top contact. This is due to the much lower semiconductor work function of n-doped Si. In contrast to the p-Si/4H-SiC HJDs, the ISE treatment led to an overall increase of the SBH compared to no ISE. Again, an increase with increasing ISE time is observed. Varying the RF power at a constant ISE time of 15 s seems to have only a minor influence. At room temperature, the maximum change of the IV SBH was accomplished using an ISE treatment of 200 W for 135 s. The ideality factor could also be reduced except when applying the highest ISE power of 600 W. In contrast to the p-Si samples, the 50 W treatment shows the lowest ideality factors of 1.033 at 300 K and even lower at elevated temperatures. The same temperature dependence and discrepancy between IV and CV SBHs are observed at the untreated n-Si/4H-SiC diodes. It is, however, less pronounced, most likely due to the much lower SBH, which gives less probability of e.g. contaminations with even lower SBH. Also, on n-Si/4H-SiC HJDs ISE treatment significantly improved the stability over temperature, hence the homogeneity of the HJDs. In addition, the deviation between different diodes could be greatly reduced.

It is worth mentioning, that the SBH variations over temperature and between devices are lower on the ISE treated n-Si/4H-SiC samples compared to the p-Si/4H-SiC samples. Even after the homogenization due to ISE, some degree of SBH inhomogeneities will be present at the interface. Only inhomogeneities with a lower SBH, than the average, will significantly influence the IV curve, and hence, the extracted
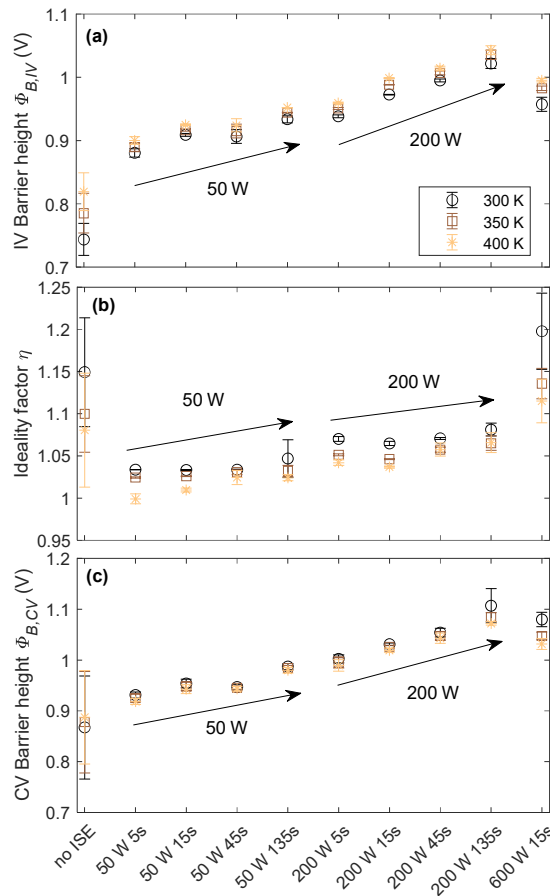
Figure 6.23: n-Si/4H-SiC diodes: (a) IV SBHs, (b) ideality factors η and (c) CV SBHs for various ISE parameters and temperatures. Every data point is averaged from three measured diodes, with the error bars representing the standard deviation.

SBH [55], [94], [119], [125]. Therefore, on the p-Si/4H-SiC samples, having a higher SBH, the presence of small regions with a lower SBH will have a stronger impact on SBH scattering than on those with lower SBH.

Finally, two additional samples were fabricated using p-Si contacts. Both samples were ISE treated at 50 W for 15 s prior Si deposition. These two samples were annealed at lower PDA temperatures of 800 and 900 °C, respectively, to investigate if the annealing temperature has an influence on the electrical characteristic. Together with the original sample, annealed at 1000 °C, and the sample without ISE treatment the extracted parameters are depicted in Figure 6.24. Compared to the sample annealed at 1000 °C, the lower annealing temperature resulted in lower SBH, both using IV and CV evaluation. At the lowest PDA temperature of 800 °C, almost no fluctuation over temperature and across samples is visible. The ideality factor could further be decreased. From a room temperature value of about 1.24 without ISE to 1.10 using 1000 °C annealing to values as low as 1.027 using 800 °C annealing. This investigation suggests lower annealing temperatures to be beneficial to the diode properties, although previous studies showed smaller Si grain size if recrystallization is conducted at lower temperatures [220].

For reasons of comparability, both the n-Si and the p-Si/4H-SiC HJDs are depicted in Figure 6.25 at $T = 300$ K. The rather large SBH difference of the oppositely doped HJDs can be reduced with ISE. At the highest ISE power of 600 W, the extracted IV SBHs differ by less than 100 mV. When applying the ISE pre-treatment in combination with the corresponding Si doping, the whole range of SBHs from 0.74
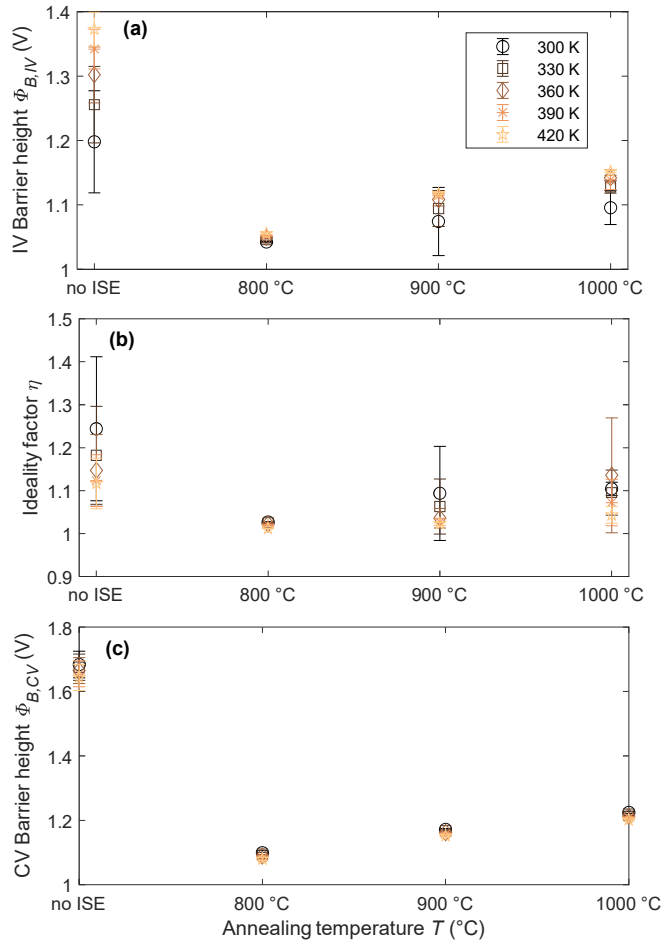
Figure 6.24: p-Si/4H-SiC diodes: (a) IV SBHs, (b) ideality factors η and (c) CV SBHs over annealing temperature. ISE parameters were 50 W, 15 s. Also, the sample without ISE is shown as reference.

up to over 1.2 V can be covered (even higher when controlling the interface inhomogeneities), while decreasing the ideality factor and improving the stability over the measured temperature range.

As can be seen in Figure 6.25, the SBHs tend towards values in the range of 1.1 V as a result of ISE treatment, for both n- and p-type Si. The microstructural analysis using TEM indicated that after ISE and post-annealing the abrupt Si/4H-SiC interface transformed into a smooth transition region from Si to 4H-SiC with some indications of 3C-SiC at the interface.

This specific junction might be modeled as a graded Si/4H-SiC heterojunction with a few nm transition layer thickness where the band gap and the electron affinities transform from Si to 4H-SiC. According to the TEM image the transition region is somewhere between 3 and 15 nm, this will very likely also depend on the used ISE power. Theoretically, a graded interface, instead of an abrupt one, would result in a reduction of the SBH due to a rounding of the tip of the arising potential barrier. The expected lowering of the SBH is seen in the p-Si/4H-SiC by a reduction of the SBH due to ISE treatment. Contradictory, the n-Si/4H-SiC shows an increase of the SBH with ISE, although also here the SBH is supposed to decrease with a graded transition region. Nevertheless, due to the low thickness of the graded region, no significant lowering of the SBH is expected. Simulations showed only 30 mV SBH reduction for a p-Si/4H-SiC heterojunction with 5 nm lineal graded band gap. Therefore, and due to the contradictory behavior on n-Si heterojunctions, a more dominant mechanism must be taken responsible for the observed change in SBH.
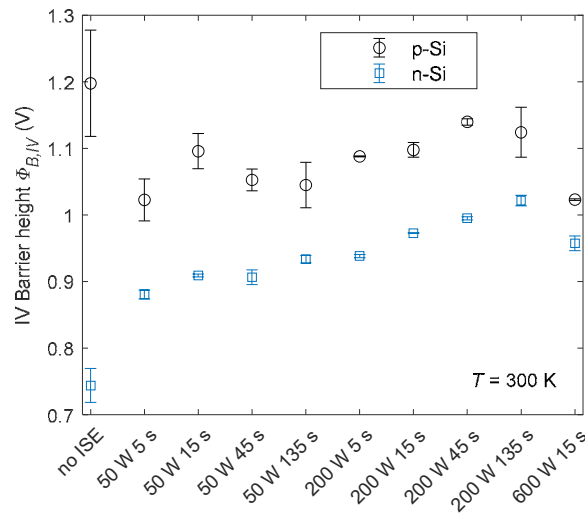
Figure 6.25: Room temperature IV SBHs of both n-Si and p-Si/4H-SiC HJDs after different ISE treatments.

Therefore, the strong change in SBH is attributed to non-stoichiometric recrystallization at the interface, resulting in many defects, hence increased FLP. With increasing power and time, the interface region will presumably have a higher carbon content due to the higher sputter yield of Si [300], [302]–[304]. These carbon defects are assumed to introduce a new charge neutrality level, pining the Fermi level towards a level of 1.1 V. Depending on the ISE parameter the degree of FLP will change, and the SBH will decrease towards 1.1 V from higher levels at p-Si and increase from lower levels when applying n-Si, as illustrated in Figure 6.25.

Additionally, to the overall strong change in SBH introduced by ISE sputtering and annealing, the used ISE parameters show an influence on the SBH distribution, hence homogeneity. As discussed, and proved experimentally, the ISE has an amorphization as well as an etching effect. The etching properties of the ISE will significantly reduce the influence of SBH inhomogeneities from extrinsic sources. This includes contaminations of the surface with particles, oxides, and other spatially varying chemical residues on the surface. This homogenization effect of the interface on a microscopic scale is noticeable by a reduction in the temperature variation of the SBH and a good agreement between IV and CV SBHs. The homogenization effect is also acting on a macroscopic level, as the variation across different diodes is reduced significantly. The results suggest that this homogenization is already sufficient at ISE times as low as 5 s. Very long ISE sputter times seem to reduce the homogeneity again.

Apart, from the homogenization, an increase in SBH with increasing ISE time is observed. It is assumed, that this is not due to the increased etching depth with time, but rather due to the increasing degree of amorphization and the change in the stoichiometry of the a-SiC region. The higher sputter yield of Si will result in a C-rich amorphous layer. It is further assumed, that at the short ISE times used in this study, the concentration of carbon in the a-SiC region will increase with ISE time, and eventually, an equilibrium will be reached. Longer sputtering times should therefore only result in an increased etch depth.

The influence of the PDA temperature on the diode properties requires further investigation. The lower temperature is believed to favor the crystallization of Si, whereas the amorphized SiC will most likely not recrystallize completely, resulting in a different interface transition region depending on the temperature. Further studies, including HRTEM imaging of interfaces annealed at lower temperatures, are required. Lowering the PDA temperature even further might eventually result in worse properties as not all the Si will transform into a crystalline state.

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6.6.4 Conclusions

In this work, the effect of ISE sputtering on the 4H-SiC surface has been studied using SRIM simulations and was confirmed by measurements for several ISE powers and durations. An ISE power of 200 W resulted in an amorphization of about 3.1 nm thickness. The material removal of the ISE was found to be relatively low under the investigated conditions. At the highest plasma power of 600 W, only an etch rate of about 6 nm/min was measured. Thermal annealing of sputter-deposited a-Si on the ISE treated 4H-SiC resulted in complete recrystallization of both the film and the interface. The originally sharp transition between Si and the untreated 4H-SiC was modified to a smooth interface due to the ISE procedure. Additionally, indications about the presence of 3C-SiC after recrystallization were directly found at the interface. Electrical characterizations of p-Si/4H-SiC and n-Si/4H-SiC heterojunction diodes were performed for all ISE parameters, showing a strong impact on the SBH, the ideality factor, and their temperature dependencies. On p-Si/4H-SiC HJDs, 200 W ISE treatment resulted in the best diode characteristics with ideality factors as low as 1.06 at room temperature with almost no deviation among different diodes as well as over the temperature range. Diodes using n-Si showed even lower ideality factors below 1.05. Using a lower PDA temperature of 800 °C on the p-Si/4H-SiC samples resulted in a further decrease of η to 1.027 and fewer fluctuations in the SBH. All in all, ISE treatment prior to a-Si deposition, including subsequent post-annealing, is a promising and straightforward approach to increase diode ideality, to reduce interface inhomogeneities, and to decrease the scatter between different diodes, along with the possibility to tune the SBH in a certain range, by varying the ISE power and time.

Future work could investigate the influence of non-inert sputter gases for ISE, e.g. N_2 or O_2, which may also have a doping effect on the interface region. The influence of different PDA temperatures needs to be studied further, as lower temperatures indicated even better diode properties, at least using p-Si contacts. Also, the influence of the ISE treatment on the diode's series resistance should be evaluated further and optimized.

6.7 a-SiC:H interlayer to adjust the SBH of Ti/4H-SiC diodes

Parts of this section have been published in [298]

Although not directly related to the Si/4H-SiC heterojunction, an experimental series was conducted, investigating the influence of ultra-thin a-SiC:H interlayers between 4H-SiC and a metal. In contrast to the previous experimental series, where the 4H-SiC was amorphized using ISE, an a-SiC:H layer is deposited by PECVD, followed by sputter-deposition of a metal contact.

The ability to adjust the SBH of a Schottky diode is most important. The use of other metals with different work functions is a straightforward approach to tailor the SBH, but strong FLP can minimize the effect of the metal work function on the SBH. Also, some metallizations are not or less suited for device integration due to e.g. environmental restrictions (hazardous substances), price and availability, adhesion problems, temperature or chemical stability aspects.

Therefore, new approaches to adjust the SBH without changing well-established materials for top metallization are widely investigated. The insertion of ultrathin dielectric layers is known to unpin the Fermi-level and a dependence of the dielectric thickness on the final SBH was found [95], [108], [308]–[311]. With increasing interface layer (interlayer) thickness, however, the ideality factors deteriorated significantly, also the on-resistance often increases when adding an interlayer. The insertion of defect-rich amorphous films can also be used to modulate the SBH by increasing the FLP towards the charge neutrality level of the new film [97], [110]. The latter amorphization, typically occurring during Ar plasma cleaning of the SiC surface, also results in strong FLP, which can be reversed by annealing [106],

[109]. The amorphization of the SiC by ion bombardment leads to non-stoichiometric a-Si_xC_y due to different sputtering yields of Si and C [286], [300], [303]. In addition, organic interlayers have been used for this purpose and showed the possibility of barrier height adjustment [312], [313]. In the case of 4H-SiC Schottky contacts, the effect of FLP is weak, the linear dependency of the SBH on the metal work function has a slope (*S*-parameter) of around 0.7 [105], [106], [314]. Consequently, the integration of a defect-rich interlayer to enhance FLP is a promising route to adjust the SBH without changing the top metallization. Alloy formation by thermal annealing between metals and semiconductors is another way to adjust the SBH, as the resulting phases might differ in work function compared to the original metal [315]–[317]. Often a large difference between the metal work function and the corresponding silicides is found [318].

Therefore, the possibility of SBH modulation utilizing both, the increase of FLP by defect-rich interlayers and the alloy formation after thermal annealing were investigated. PECVD grown a-SiC:H layers of different thicknesses integrated in Ti/4H-SiC diodes were characterized with electrical as well as microstructural analysis techniques. Additionally, the influence of thermal annealing at 600 °C in vacuum was investigated. Alloy formation between Ti and the a-SiC:H is achieved with less thermal budget compared to crystalline 4H-SiC due to its amorphous nature, being able to tune the SBH and reducing SBH inhomogeneity effects [94], [319]–[322].

6.7.1 Experimental Details

4H-SiC substrates from Cree Inc. with 4° off-axis cut, n-type bulk doping with a resistivity of 0.015 to 0.028 Ωcm, and an epitaxial layer with N_D ~ 1.6 · 10^{16} cm^{-3} on the Si face were used. Before top contact deposition, the substrates were thoroughly cleaned using hydrofluoric acid and RCA cleaning solutions. On the backside (C-face) 200 nm Ti and 200 nm Pt were sputter-deposited and annealed at 1000 °C for 1 min to form an ohmic contact. Subsequently, the substrates were again cleaned using hydrofluoric acid and deionized water. The Schottky contacts were formed on the low doped epitaxial layer, being the Si-face of the substrate. The a-SiC:H is grown in an Oxford instruments PlasmaLab 100 ICP-CVD system using 6.5 sccm SiH_4 and 13.5 sccm CH_4 diluted with 50 sccm Ar at a chamber pressure of 0.8 Pa and an inductively coupled plasma power of 1000 W at 250 °C substrate temperature. The second plasma source, connected to the substrate holder (table excitation) was not activated. More details about the properties of the used a-SiC:H films were published previously [323], [324]. Interlayer thicknesses between 0.7 to 4 nm were prepared. Due to the high plasma power, the deposition rate is high at 0.17 nm/s resulting in short deposition times ranging from 4 to 24 s. As a reference, a conventional Ti/4H-SiC Schottky diode without (w/o) interlayer was fabricated. Next, the 200 nm thin Ti metallization was sputter-deposited at 500 W and 0.3 Pa pressure. Prior to annealing, the deposited Ti layer was patterned to form circular contacts with 700 µm in diameter. Annealing was done in a rapid thermal annealing oven under vacuum (< 0.01 Pa) at 600 °C for 5 min. After electrical characterization annealing was performed a second time for 10 min at 600 °C. IV and CV measurements of *as-deposited* and annealed diodes were measured at 300, 350, 400, and 450 K in the dark and under vacuum using a Keysight B2985A electrometer and Agilent 4294A high precision impedance analyzer at 1 MHz test frequency, respectively. XRD was performed using a X'Pert MPD Pro diffractometer from Malvern PANalytical in Bragg-Brentano configuration using the Cu K_α radiation line. TEM measurements were done on an FEI TECNAI F20 operated at 200 kV acceleration voltage.

All diodes of this study were characterized three times, electrically and microstructurally: in the *as-deposited* state after 5 min at 600 °C, and after another 10 min at 600 °C annealing.

6.7.2 Electrical characterization

Figure 6.26 shows forward IV measurements at $T = 300$ K of (a) a conventional Ti/4H-SiC diode without interlayer and (b) with 2 nm interlayer prior to and after the two annealing steps, respectively. The diode without interlayer shows quite ideal diode characteristics before and after annealing, whereas the IV curve was shifted towards higher voltages after the annealing steps. An increase in SBH after annealing was seen before with different top metallization systems [320], [325]–[327]. The second annealing for another 10 min did not shift the IV curve significantly but resulted in a slightly more ideal curve shape. In contrast, the diode characteristics with a 2 nm a-SiC:H interlayer exhibits, in the *as-deposited* state, a much higher turn-on voltage and a strong current limiting at enhanced forward bias values. In addition, a hysteresis was observed between ramping the voltage up and down (not shown) which indicated a charge built up in the defect-rich amorphous interlayer. After annealing, however, almost ideal characteristics were observed when assuming thermionic emission current flow. In addition, the hysteresis completely vanished. A second annealing step was able to shift the IV characteristic towards lower voltage levels while maintaining the ideal shape.

The SBH, the ideality factor η, and the series resistance R_s were extracted out of the IV measurements according to Section 3.3.2 at all measurement temperatures using the thermionic emission model [14].

For extracting R_s Cheung's method [213] was applied. The series resistance must be understood to be composed out of the intrinsic device resistance and the setup-related resistance originating from wiring and contracting. The external contribution should be similar for all measured diodes and will therefore not influence the observed trends.
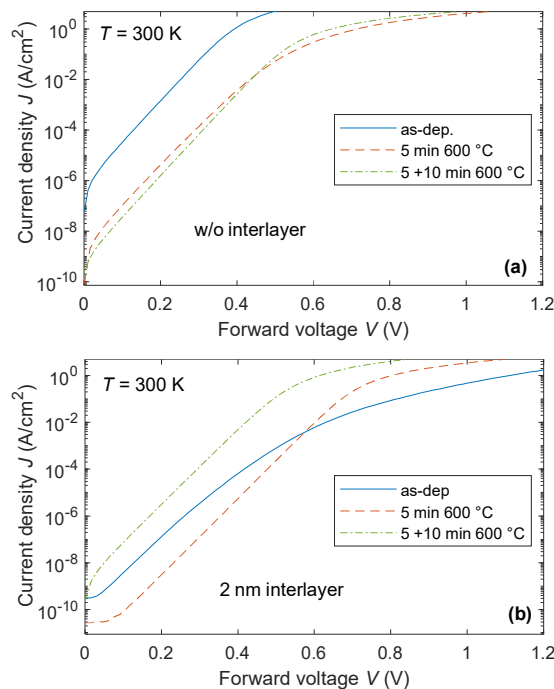
Figure 6.26: Forward IV measurements of (a) Ti/4H-SiC diode without (w/o) interlayer and (b) Ti/a-SiC:H/4H-SiC diode with 2 nm interlayer. Both devices are measured in the as deposited state, after annealing steps at 600 °C for 5 min and after another 10 min.

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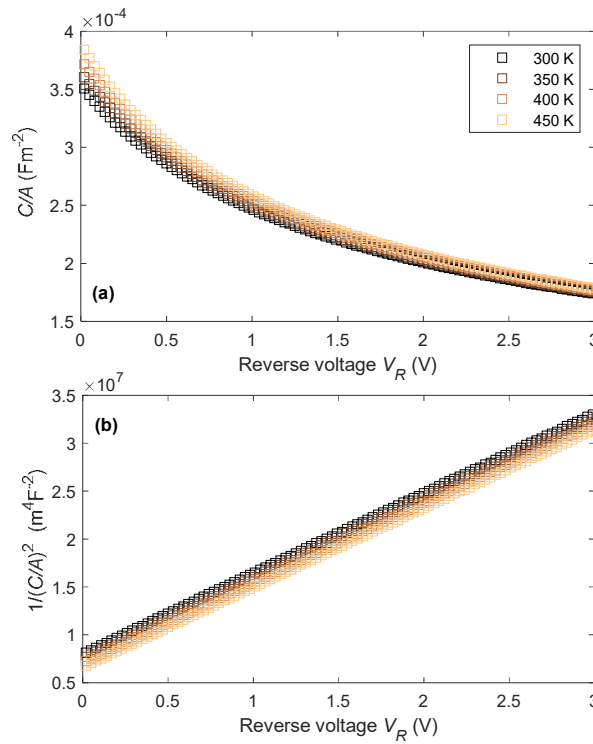
Figure 6.27: (a) Raw CV measurement data over temperature as well as rearranged $1/C^2$ plot over temperature used for fitting the Ti/a-SiC:H/4H-SiC diode with 2 nm interlayer in the *as-deposited* state.

Figure 6.27 shows the measured CVT data over the reverse bias V_R of the diode with 2 nm interlayer in the *as-deposited* state as reference. The SBH was evaluated using the CV data as described in Section 3.3.3.

All extracted diode parameters are depicted in Figure 6.28. At the as-*deposited* conventional Ti/4H-SiC diode an IV SBH of around 0.78 V and an ideality factor of 1.09 were measured at room temperature. Rather high ideality factors and strong temperature-dependent SBHs were found at the unannealed samples with an interlayer. Due to the defect-rich nature of the amorphous films, strong FLP is suggested to be responsible for the increase in SBH by more than 0.25 V compared to the diode w/o interlayer. The extracted SBH and ideality factor did not show any dependence on film thickness in the *as-deposited* state. The series resistance, however, increased as the a-SiC:H becomes thicker. The lowest R_s of about 2 Ω was measured w/o interlayer, whereas the sample with a 4 nm thin interlayer measured the highest value of about 6 Ω at room temperature. Due to the dielectric nature of the deposited a-SiC:H layer an increase with interlayer thickness is expected, as it can be regarded as an additional resistance connected in series.

The first annealing step led to extremely low ideality factors below 1.05 and IV SBHs in the range of 1.1 to 1.2 V, whereas the conventional diode w/o interlayer only exhibits a room temperature IV SBH of around 0.9 V and slightly higher ideality factors. The SBHs extracted from CVT measurements are given in Figure 6.28c demonstrating slightly higher values compared to the IVT SBH, most likely due to the presence of SBH inhomogeneities. For a better comparison Figure 6.28e shows the difference
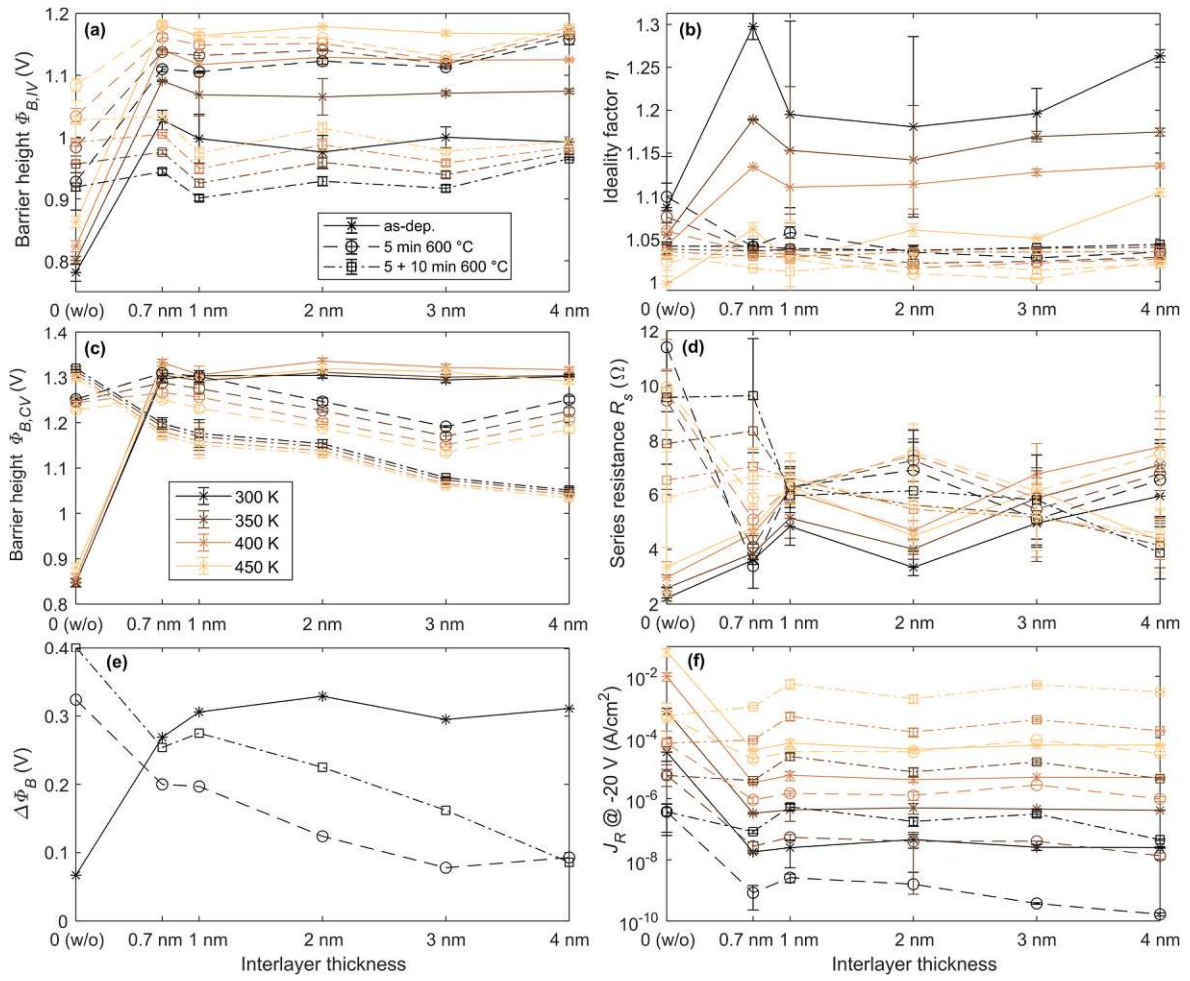
Figure 6.28: Extracted parameters of the diodes from IVT and CVT measurements as a function of interlayer thickness. Line style represents the annealing treatment and color the measurement temperature. Data points are averaged from three diodes. (a) IVT SBH, (b) ideality factor η, (c) CVT SBH, (d) series resistance R_s and (f) the reverse current density J_R at -20 V. (e) Shows the difference in SBHs of CV and IV measurements at 300 K.

between CV and IV SBHs ($\Delta\phi_B = \phi_{B,CV} - \phi_{B,IV}$) at 300 K. The deviation is lowest at 3 nm interlayer thickness and worst at the conventional diode after annealing. Due to the trend reversal of $\phi_{B,CV}$ at 4 nm a-SiC:H thickness, the 5 min annealing time at 600 °C was presumably not long enough to complete interface stabilization by a finished recrystallization or alloy formation process. The series resistance of the diode w/o interlayer strongly increased after annealing, being the highest of all after the first 5 min annealing step. All the other series resistance values scatter around 6 Ω with no distinct trend. Also, surface oxidation can be taken responsible for the increase in R_s after thermal annealing.

To complete interface stabilization a further annealing step for 10 min on the same temperature level was performed. Doing so, the room temperature IV SBH of the samples with interlayer was drastically reduced to values between 0.9 and 0.96 V while maintaining the good ideality factors. The SBH of the conventional Ti/4H-SiC diode did not change significantly, being now at the same level as the diodes with an interlayer. In contrast, the CV SBH is much stronger affected by the interlayer thickness. Now the sample with 4 nm interlayer thickness shows the lowest deviation between IV and CV SBHs as well as the lowest temperature dependence, thus indicating low defect concentrations and a reduction in local SBH inhomogeneity. The conventional diode reveals the strongest temperature dependence of the IV

SBH and a deviation in SBH between IV and CV of 0.4 V at room temperature. The lowering of the SBH after further annealing is attributed to a completed interface alloying between defect rich a-SiC:H and the Ti. Also, the series resistance did change after a second annealing and shows the reverse trend on interlayer thickness than before annealing. At room temperature, R_s decreases from about 9.5 Ω at the diode w/o interlayer to about 3.9 Ω with 4 nm interlayer thickness. The change of R_s with thermal annealing might be correlated to the interface homogeneity. If the interface is composed out of a small number of low SBH patches, the overall area contributing to the current flow is small, hence the series resistance is large and also bias dependent [94], [95]. Reverse biased IVT measurements have been conducted as well. The reverse current density at a bias of -20 V is shown in Figure 6.28f. The diodes annealed for 5 min show the lowest leakage current, being in accordance with the highest IV SBH. Overall, the measured leakage current density is in good agreement with the IV SBH.

Using different interlayer thicknesses and two different annealing durations at 600 °C the SBH could be varied over a wide range. The lowest IV SBH was found on the conventional diode in the *as-deposited* state to be 0.78 V with an ideality factor of 1.09. The strongest increase of 49% to 1.16 V was achieved using 4 nm interlayer and 5 min, 600 °C annealing, while lowering the ideality factor to 1.035. The usage of a-SiC:H interlayers and different annealing durations and presumably temperatures is suitable for adjusting the SBH over a wide range, whereas the series resistance is not increasing very much.

6.7.3 Discussion of Fermi level pinning and annealing effects

The main processes affecting the SBH are assumed to be FLP for the *as-deposited* samples with interlayer, and the alloy formation between SiC and Ti after annealing.

Due to the defect-rich nature of amorphous semiconductors the Fermi level of the a-SiC:H layer is assumed to be near mid-band [328]. Therefore, a strong band bending is introduced in the 4H-SiC epi-layer to align its Fermi level which is close to the conduction band to near mid-band at the interface. The strong increase of CV SBH by more than 400 meV, compared to no interlayer, indicates that the SBH is no more dominated by the metal work function. The thickness of the interlayer also does not show a significant influence, so that already the 0.7 nm a-SiC:H layer sufficiently pins the Fermi level. Comparably strong FLP was found when the 4H-SiC surface was amorphized by ion bombardment prior to metal deposition [106].

Both, the amorphous and the crystalline SiC are expected to react with Ti at 600 °C, whereas the crystalline SiC will react much slower [329]. The expected reaction products are mainly TiC and Ti_5Si_3. The formation of the ternary phase Ti_3SiC_2 is not expected to form below 1000 °C [329], [330]. The increased SBH of the annealed diodes compared to conventional Ti/4H-SiC diodes is assumed to be due to the formation of an ultrathin interfacial layer of TiC and Ti_5Si_3. Bow et al. [331] found that annealing Ti and 6H-SiC at 700 °C will form 1-2 nm <111> oriented TiC directly at the SiC surface, followed by Ti_5Si_3. Because of the higher chemical affinity of Ti for C than for Si, a TiC layer will initially form on the interface. The remaining Si will subsequently form Ti_5Si_3 on top of the TiC [332], [333]. With a work function of about 4.7 eV [334]–[336] the (111) TiC surface would give much higher SBHs than Ti and Ti_5Si_3 with corresponding values of about 4.33 eV [337] and 3.71 eV [318], respectively. The formation of an ultrathin <111> oriented TiC film on the 4H-SiC surface after annealing could explain the increase in SBH after annealing of the conventional Ti/4H-SiC Schottky diode. Porter et al. [338] measured the SBH of Ti/6H-SiC Schottky junction before and after annealing at 700 °C for 20 and 60 min, and found IV SBH of 0.83 V in de *as-deposited* state and 0.86 V and 0.9 V after annealing. This is in good agreement with our results of 0.78 V in the *as-deposited* state and 0.92 V after 600 °C 15 min annealing. Therefore, no significant changes in the SBH are assumed if annealing is performed up to

700 °C or for a longer period of time, than performed in this study. Much higher temperatures in excess of 900 °C will be needed to initiate Ti_3SiC_2 formation and to lower the SBH again.

The samples with interlayer will form the same reaction products after annealing, with the additional effect of reducing the strong FLP of the amorphous interface layer. The presence of different reaction products with different work functions creates an inhomogeneous SBH distribution at the interface and can therefore be taken responsible for the observed difference in SBH obtained from IV and CV analyses. The smallest deviation was observed at the sample with the thickest interlayer after two annealing steps. The 4 nm a-SiC:H requires more than 5 min to complete alloy formation with Ti, but after another 10 min it showed the electrically most homogenous interface. The conventional Ti/4H-SiC diode, however, showed after annealing the strongest deviation in SBH between IV and CV, which is attributed to the formation of a thin interfacial layer of TiC, with small patches of Ti or Ti_5Si_3 being still in contact with the SiC. This inhomogeneity in chemical composition translates to a locally varying SBH causing the difference in the measured IV and CV SBH. IV techniques measure the effective SBH, which is given by the current flow over the lowest SBH patches, whereas CV techniques give an average SBH over the whole interface area [94], [122].

6.7.4 Microstructural characterization

XRD measurements were performed at all samples independent of the a-SiC:H interlayer thickness or annealing time. Figure 6.29a shows a selection of XRD diagrams. One *as-deposited* sample and the samples annealed for 5 min at 600 °C are depicted. All a*s-deposited* samples, showed the same XRD diagram, therefore only that w/o interlayer is illustrated as reference. The *as-deposited* samples exhibit
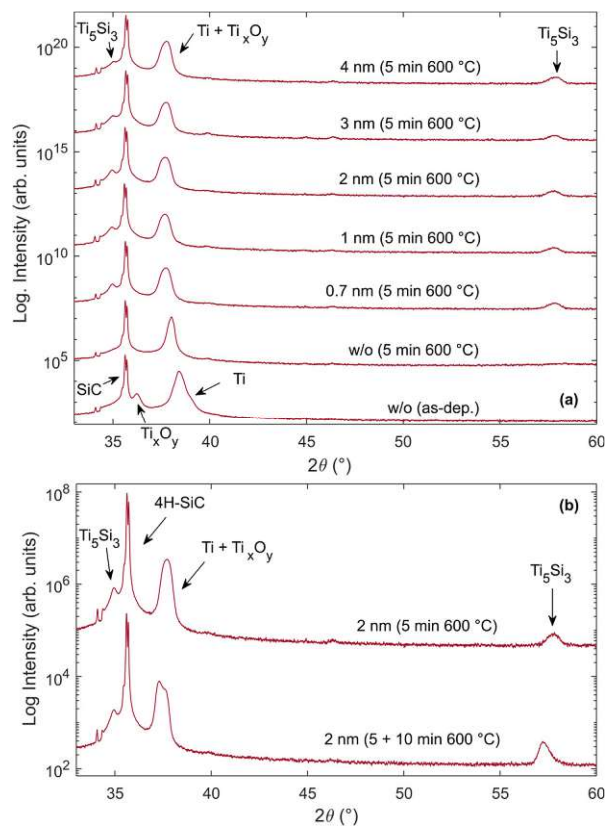
Figure 6.29: XRD measurements with logarithmic intensity scale of (a) samples with different interlayer thickness and (b) the 2 nm interlayer sample after different annealing times.

Ti, Ti_xO_y, and 4H-SiC related peaks. After annealing at 600 °C Ti_5Si_3 related peaks could only be identified in the samples with a-SiC:H interlayer. The sample w/o interlayer did not show any diffractions within the sensitivity range of the XRD. The Ti-related peak shifted after annealing, which is attributed to enhanced mechanical stress and the formation of Ti_xO_y, which has lattice constants similar to Ti. An expected TiC{111} peak would overlap with the 4H-SiC peak and hence, could not be confirmed. The amorphous nature of the a-SiC:H film facilitated the alloy formation compared to the chemically less active monocrystalline 4H-SiC surface resulting in the low-temperature formation of Ti_5Si_3 and presumably TiC. Figure 6.29b compares the 2 nm sample after 5 and 5+10 min annealing. The additional annealing time increased the Ti_5Si_3 related peaks, as well as it resulted in further oxidation
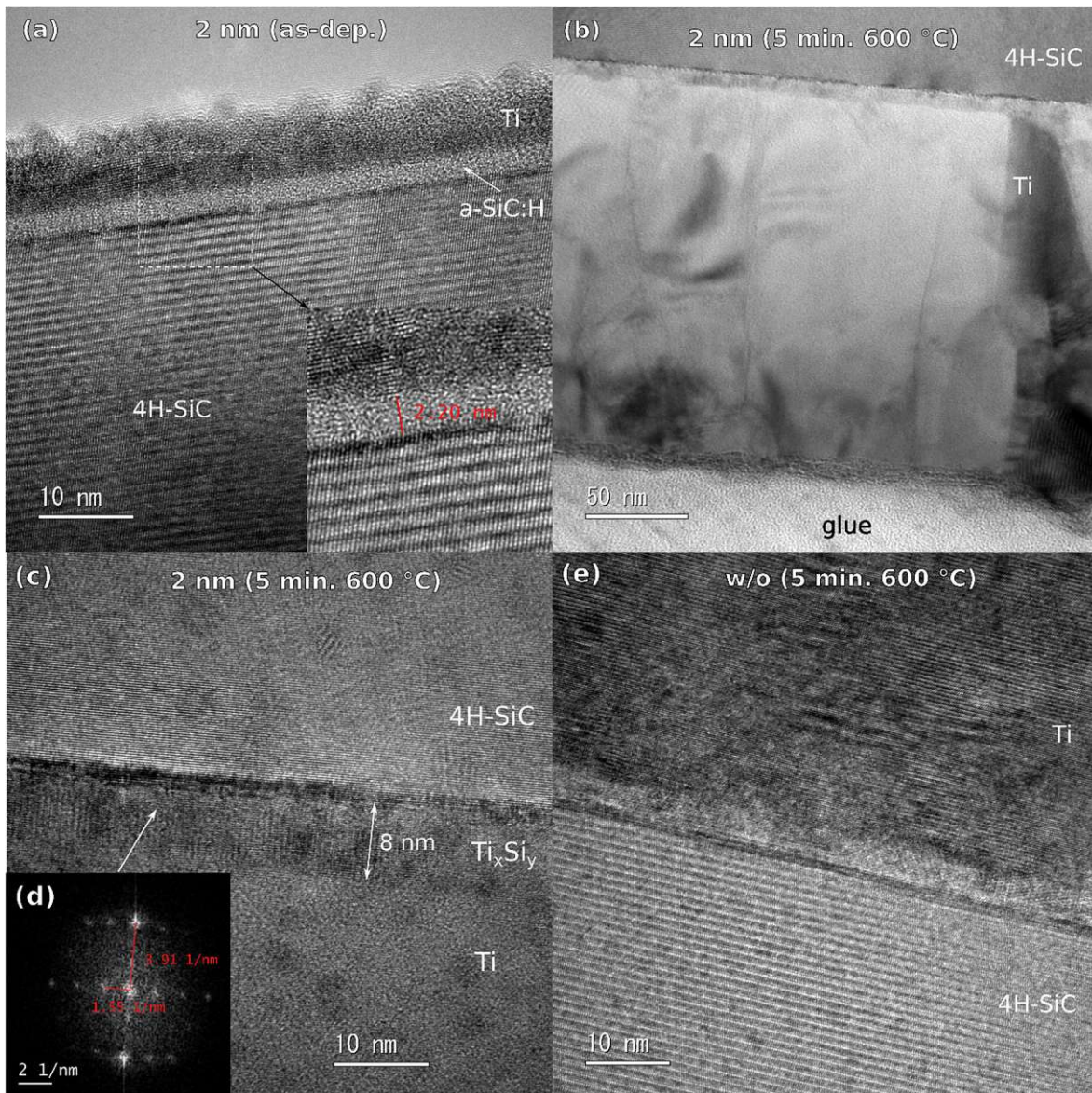
Figure 6.30: TEM measurements of the sample with 2 nm interlayer (a) *as-deposited* and (b) and (c) after 5 min 600 °C annealing. Sample w/o interlayer after annealing is shown in (e). Inset (d) contains an FFT diffraction pattern of the alloy region.

of the Ti on the surface. Also, after the second annealing, no Ti_5Si_3 related signal was observed in the conventional diode w/o interlayer.

The sample w/o and with 2 nm thick a-SiC:H were prepared for TEM imaging. The TEM analysis in Figure 6.30a confirms both the amorphous nature and the expected film thickness of 2 nm by measuring a value of about 2.2 nm. No signs of alloy formation are found in the *as-deposited* state. The same sample was investigated after an annealing step for 5 min at 600 °C. Figure 6.30b shows the cross-section of the whole Ti film and Figure 6.30c a magnified view of the interface region. Close to the interface, an intermixture layer of approximately 8 nm thickness is detectable. Local FFT was used to evaluate the diffraction pattern, confirming the interlayer to be Ti_5Si_3, as shown in Figure 6.30d. No indication of the presence of TiC was observed. The carbon might still be present interstitially or it has effused out together with the hydrogen. Figure 6.30e shows the sample w/o interlayer after 5 min annealing. Near the interface, some signs of alloy formation are visible, but less pronounced compared to the sample with interlayer, thus supporting the results from the XRD measurements where the presence of Ti_5Si_3 could not be confirmed. Given the chemical elements C, Ti and Si involved, the presence of small patches of TiC and Ti_5Si_3 is likely, although not confirmed. The very thin reaction layer on the interface compared to the relatively thick reaction layer of 8 nm at the sample with 2 nm interlayer can be taken as responsible for the strong inhomogeneity effects seen in electrical measurements. Different phases with different work function might be in direct contact with the 4H-SiC.

6.7.5 Conclusion

In conclusion, the insertion of ultrathin interlayers of a-SiC:H is a straightforward approach to modify the SBH compared to conventional Ti/4H-SiC diodes. The *as-deposited* state is affected by strong FLP, attributed to the defect-rich amorphous layer, resulting in non-ideal diode characteristics with a strong temperature dependence of the SBHs. Although the diode ideality deteriorated, the SBH could be increased from about 0.78 V at conventional diodes to over 1 V. Negligible influence on the thickness of the interlayer was found.

Annealing at 600 °C results in the formation of mainly Ti_5Si_3 at the interface, which resulted in much more ideal diode characteristics. No signs of TiC were found in any sample, but it is expected to be present as a very thin layer. The SBH was increased after annealing at all diodes, although using the interlayer even more. Longer annealing is assumed to stabilize the interface by completing alloy formation and increasing the crystallographic properties of the intermixture layer. After 5+10 min annealing at 600 °C the IV SBH was found to be between 0.9 and 0.96 V at room temperature at all diodes. The temperature dependence and the deviation between IV and CV SBH were the worst for conventional Ti/SiC diode and best using 4 nm interlayers.

The integration of a-SiC:H interlayers combined with a variation of annealing temperature and time is suitable to adjust the SBH of 4H-SiC Schottky diodes over a wide range by maintaining almost ideal IV characteristics. From the lowest IV SBH of 0.78 V measured on the *as-deposited* sample w/o interlayer, the SBH could be increased by 49% to 1.16 V on the sample with 4 nm interlayer after 5 min annealing. By changing the annealing duration and interlayer thickness a wide range of SBH values with potentially lower SBH inhomogeneities than on conventional Ti/4H-SiC Schottky diodes could be achieved.

Ultrathin a-SiC:H interlayers might also be used in combination with Si as contact material, although, the high temperature needed for Si deposition or recrystallization would most likely lead to a recrystallization of the a-SiC:H and the Si, similar to the previous section, but without the cleaning and homogenization effect of the ISE.

7 Summary and outlook

7.1 Summary

In this thesis, the Si/4H-SiC heterostructure was investigated with resepct to both microstructure and interface quality as well as electrically, forming heterojunction diodes. Theoretical calculations were performed, investigating the potential of heterojunction diodes using different doping concentrations for the Si or 3C-SiC top contact. Due to the wide range of Schottky barrier heights which can be realized with Si/4H-SiC junctions and the possibility to deposit Si with industry-standard equipment, this heterojunction configuration was examined in detail, providing new knowledge to the community, and providing a base for the fabrication of more complex device structures.

Si was grown on industry-standard 4° off-axis 4H-SiC substrates using different deposition techniques including sputter-deposition and low-pressure chemical vapor deposition. Sputter-deposition resulted in only amorphous Si layers, even with *in-situ* heating up to 400 °C. For electrical purposes, a crystalline Si is necessary, requiring PDA. Different PDA parameters, varying the temperature, the time, and the heating rate, revealed the possibility to crystallize a-Si on 4H-SiC without any visible interface reaction. With a typical grain size of 30 nm all samples were polycrystalline without any epitaxial connection to the SiC. Higher temperatures, longer annealing times, lower heating rates, as well as high boron content in the a-Si resulted in larger grains. A big advantage of sputter-deposited and post deposition annealed Si layers, not only on SiC, is its low surface roughness, especially compared to deposition techniques resulting in a crystalline growth. With approximately the same layer thickness of 500 nm Si, a mean squared surface roughness of 1.9 nm was achieved with sputter-deposition and PDA whereas LPCVD resulted in 45.6 nm.

In the next step, LPCVD was used for direct crystalline deposition of Si on 4H-SiC. Due to the large number of adjustable parameters, having an influence on the deposition, only the temperature was varied between 700 and 1080 °C, with the pressure and gas flows fixed at values that gave a reasonable film thickness and coverage. Due to the used hot-wall reactor, precursor depletion dominates at higher pressures or lower gas flow rates, resulting in a lower gas velocity. The growth rate was in the range of 7 to 15 nm/min with the maximum at a deposition temperature of 800 °C. No closed film coverage was achieved at deposition temperatures of 1000 °C and above. The dominant growth directions of the films were Si<111> and Si<110>, verified with XRD and TEM analyses. Both orientations were found at all deposition temperatures, whereas at 900 °C the Si film was almost only <110> oriented without the presence of any voids. A deposition at temperatures between 900 and 1080 °C showed heteroepitaxial growth of Si on 4H-SiC, without any distortion due to the off-axis orientation of the substrate. Pre-treatment of the 4H-SiC with SF_6 prior to Si deposition was investigated as well, resulting in the highest deposition rate of about 23 nm/min and a very rough but epitaxial interface at a deposition temperature of 1080 °C. Although an epitaxial connection was found, the interface turned out to be very rough and the film shows a high density of rather deep etch pits, limiting the use for most applications.

For a direct deposition of crystalline Si using sputter-deposition Al and Au seed layers were utilized, taking advantage of their catalytic effect known as MIC. Experiments *in-situ* the sputter-deposition chamber were preformed with the heater integrated in the substrate holder, demonstrating the possibility to deposit crystalline phases of Si on 4H-SiC at about 400 °C. Nevertheless, with the deposition parameters investigated, only non-closed films could be produced with both Au and Al seed layers. Therefore, the focus was led on *ex-situ* annealing, facilitating the well-known layer exchange process of MIC. Among different film thickness ratios between metal and Si, also different annealing conditions play an important role. Al, Au, and Ag were investigated to evaluate their potential for the crystallization

of a-Si on 4H-SiC, clearly indicating the superior performance of Al, serving simultaneously as a good p-type dopant to Si. Au and Ag did not give satisfying results, additionally, they are both not CMOS compatible. Al/a-Si stacks resulted in well-oriented c-Si grains at annealing temperatures as low as 200 °C. Using very thin Al layers of only 10 nm thickness and low annealing temperatures resulted in a high-quality recrystallization of Si near the SiC surface. Besides the thicknesses of the two layers, also the annealing temperature, duration, and ramp are important parameters. In addition, the microstructure of the metal layer seems to play an important role in the MIC process. Al was found to have an epitaxial connection to 4H-SiC, being crucial for the epitaxial recrystallization of the Si, although high-quality metal layers with a low grain boundary density are disadvantageous for layer transfer. Due to the well-reduced temperature budget, the MIC process is also interesting for material combinations that cannot withstand a high thermal load. Thin epitaxial Si layer on SiC, generated with Al-induced MIC might also serve as seed layers for epitaxial thickening.

Heterojunction diodes have been fabricated using Si grown on 4H-SiC with the above-mentioned techniques. The Si was highly doped, either by applying a highly doped target material, or spin-on doping, or doping due to Al diffusion during the MIC process.

Theoretical calculations suggested a rather high SBH of about 1.6 V for the p-Si/4H-SiC heterojunction and a low SBH of about 0.8 V using n-Si as top contact. HJDs realized with sputter-deposition and subsequent PDA confirmed the theoretical expected SBH, although especially on the p-Si/4H-SiC junction, the IV evaluated SBH was much lower due to inhomogeneities of the SBH. Extensive fitting based on Tung's model was performed giving insight into the distribution of inhomogeneities.

HJDs with LPCVD deposited Si strongly deviated from the expected calculated SBH values. Similar to HJDs fabricated with surface activated bonding, a high density of misfit dislocations at the epitaxial interface is assumed to be responsible for a strong FLP. S-parameters and CNLs have been evaluated for the HJDs with different Si deposition temperatures and were compared with Si/4H-SiC heterojunctions prepared by other approaches, suggesting a strong increase of FLP with the degree of heteroepitaxy. By applying a SF_6 pre-treatment, almost ohmic device characteristics were found, although introducing strong etch damage, limiting the usage in real device structures. The possibility to adjust the SBH via the Si deposition temperature and pretreatments like SF_6 etching might also be exploited advantageously in future device architectures.

A Si/4H-SiC HJD was successfully prepared with MIC technique. Two annealing steps, one at low temperature to initiate interface recrystallization at a thin Al layer and a second one at higher temperature for complete recrystallization were used. The device showed well-rectifying properties, but due to the remaining Al islands at the interface a double bump in the IV characteristic is observed. No further doping step was required, as the Al already serves as good p-type dopant.

Sputter-deposited Si/4H-SiC HJDs with n and p-Si as top contact material were produced, whereas the influence of Ar$^+$ ISE treatment on the 4H-SiC surface prior Si deposition was investigated. ISE treatment in combination with PDA resulted in a smooth interface transition region showing more ideal diode characteristics. The ideality factors of the diodes could be reduced, as well as the variation between samples and at different temperature levels was minimized. The best results were achieved with ISE parameters of 200 W. Also the PDA temperature indicated to have an influence on the diode properties. A p-Si/4H-SiC sample with 50 W, 15 s ISE treatment and 800 °C, 2h PDA showed the lowest ideality factor of 1.027. Nevertheless, the series resistance was increased after ISE treatment. All in all, ISE treatment prior to a-Si deposition, including subsequent post-annealing, is a promising and simple approach to produce high-quality heterojunctions for diodes and other applications.

Finally, the insertion of ultrathin layers of a-SiC:H at the interface of Ti/4H-SiC Schottky diodes was investigated. In the *as-deposited* state, the interlayer resulted in worse diode characteristics and strong hysteresis. After thermal annealing at 600 °C for 15 min, the diode properties could be stabilized due to silicide formation, showing lower ideality factors than conventional Ti/4H-SiC Schottky diodes. By varying the interlayer thickness and the annealing temperature, the SBH can be controlled in a wide range.

7.2 Outlook

The experiments conducted in this thesis could only cover certain aspects of the large range of possible growth methods, deposition parameters, and interface preparation techniques of Si/4H-SiC heterostructures. The fabricated HJDs represent only the simplest, and hence most straight forward device architecture based on this junction for proof of concept investigations. In the following, some suggestions and inspirations for further experiments will be given.

Regarding the Si deposition, the conducted experiments suggested a rather strong impact of interface defects, e.g. misfit dislocations on the diode properties due to FLP. Polycrystalline, non-epitaxial Si films resulted in SBHs with a better match to the theoretically expected values. Nevertheless, the quality of the epitaxial films fabricated with LPCVD technique is low due to an incomplete coverage and should further be investigated by a variation of the pressure, the gas flow ratios, or different Si sources. If these closed epitaxial films still suffer from strong FLP, high-temperature annealing steps might be performed for defect passivation. Also sputter-deposition equipment, capable of *in-situ* heating up to temperatures >600 °C, allowing the direct deposition of polycrystalline Si, might be an interesting approach for a fast deposition of pre-doped Si layers without the need of PDA.

Different interface pre-treatments showed a very promising influence on the diode properties. Especially ISE treatment prior to sputter-deposition of the Si should therefore be optimized. Different ion species for ISE could be used, as e.g. O_2 or N_2 might have an additional doping effect in the interface transition region. Furthermore, the PDA temperature was found to have an influence in increasing the device homogeneities even more. For LPCVD, SF_6 pretreatment showed an unexpected increase of deposition rate, a high epitaxial interface, and almost ohmic device characteristics. Lower temperatures might allow to reduce the disadvantages of etch pits.

The MIC process, despite all its complexity, offers also great potential for improvements. Different deposition techniques and parameters of the Al, resulting in a higher density of GBs, should be compared in further experiments. Another approach is the intentional oxidation of the Al prior Si deposition, to form a thin permeable coverage of AlO_x in between Al and a-Si, which will favor the layer exchange process.

Apart from improving the deposition process, the fabrication of more complex device structures should also be in the focus of future activities. The HJDs should be prepared with proper edge termination, to investigate the influence of the different pretreatment and deposition techniques on the breakdown characteristics. As a next step, a dual-heterojunction diode, by alternating p- and n-Si regions could be fabricated, taking advantage of the high and low SBH of the two junctions. Also, switching devices might be fabricated. Field-effect transistors or bipolar junction transistors could be fabricated in 4H-SiC. Whereas in the case of a BJT, the SiC might serve as the collector, taking up the higher field strength. The SiC might also only be used as a high thermally conductive substrate for lateral Si devices fabricated on top [339].

All in all, the Si/4H-SiC material combination is very promising and will certainly stimulate further research and industry-driven activities in the future.

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List of symbols

Symbol	Definition	Unit
$\langle \hbar \omega \rangle$	Parameter of the BGN model after Donnell and Chen [75]	eV
2θ	Angle of diffraction	°
A^*	Richardson constant	A/K^2cm^2
$A_{nc}, A_{nv}, A_{pc}, A_{pv}$	Coefficients of the BGN model after Lindefelt [69]	---
b	Full width half maximum peak intensity	°
C	Capacitance	F
C'	Capacitance per area	F/m^2
C_c	Correction factor	---
C_d	Depletion capacitance	F
C_g	Concentration of the reactant gas species	$1/cm^{-3}$
c_n	Electron capture coefficient	cm^3/s
C_p	Density of patches of the intrinsic distribution	$1/cm^2$
c_p	Hole capture coefficient	cm^3/s
d	Lattice spacing	m
d_g	Grain Size	m
d_g	Average grain size	m
D_g	Diffusivity	m^2/s
D_{GS}	Density of gap states	$cm^{-2}eV^{-1}$
E_A	Acceptor ionization energy	eV
E_A	Activation energy	eV
E_b	Breakdown field strength	MV/cm
E_C	Conduction band edge energy	eV
$E_{C,bulk}, E_{C,surf}$	Bulk and surface binding energies of carbon	eV
E_D	Donor ionization energy	eV
$E_{d,C}$	Displacement energy of carbon	eV
$E_{d,Si}$	Displacement energy of silicon	eV
E_F	Fermi energy level	eV
E_G	Energy band gap	eV
E_i	Intrinsic Fermi level	eV
E_{Ion}	Ion energy	eV
e_n	Electron emission coefficient	1/s
e_p	Hole emission coefficient	1/s
$E_{Si,bulk}, E_{Si,surf}$	Bulk and surface binding energies of silicon	eV
E_V	Valence band edge energy	eV
E_{vac}	Vacuum energy level	eV
$\vec{G}$	Reciprocal lattice vector $\vec{G} = \Delta\vec{k} = 1/d$	1/m
g_A	Acceptor ground-state degeneracy factors	---
g_D	Donor ground-state degeneracy factor	---
h	Critical thickness for crystallization	m
h_g	Gas transport rate	nm/min
i	index	---
I	Current	A
I_{rr}	Reverse recovery current	A

I_s	The saturation current	A
J	Current density	A/cm
J_F, J_R	Forward and reverse current density	A/cm
J_s	The saturation current	A/cm
K	Shape factor of the Scherrer equation (~0.9)	---
k_f	Forward reaction rate	nm/min
$\vec{k_i}$	Incoming wave vector	1/m
$\vec{k_s}$	Scattered wave vector	1/m
L_f	Flight path in ToF detectors	m
L_t	Transfer length	m
M_c	Number of equivalent minima in the conduction band	---
m_{dc}^*	Density of states effective masses for electrons	kg
m_{dv}^*	Density of states effective masses for holes	kg
$m_{th,e}^*$	Thermal velocity effective mass for electrons	kg
n	Concentration of free electrons	cm^{-3}
n	Index	---
N	Density of the deposited solid	1/cm^3
N_A	Acceptor concentration	cm^{-3}
N_A^-	Ionized acceptor concentration	cm^{-3}
N_C	Effective densities of states in the conduction band	cm^{-3}
N_D	Dopant concentration	cm^{-3}
N_D^+	Ionized donor concentration	cm^{-3}
n_i	intrinsic carrier concentration	cm^{-3}
N_V	Effective densities of states in the valence band	cm^{-3}
p	Concentration of free holes	cm^{-3}
p	Pressure	torr or bar
P	Power	W
P_{po}	Weight function	---
Q_{GS}	Surface charge of gap states	C
Q_m	Metal charge	C
Q_S	Semiconductor charge	C
R	Resistance	Ω
r	Radius	m
R_0	Radius of low SBH patch	m
R_a	Root mean squared roughness	m
R_c	Contact resistance	Ω
R_{crit}	Critical radius	m
R_d	Growth rate	nm/min
R_m	Resistance of metal contact	Ω
R_q	Arithmetic average roughness	m
R_s	Series resistance, or series of the bulk semiconductor	Ω
R_{sh}	Sheet resistance	Ω/sq
R_t	Total resistance	Ω
S, S_{GS}	Slope of the SBH over the metal work function	---
S'	Parameter of the BGN model after Donnell and Chen [75]	---
T	Temperature	K, °C

t	Time	s
t_f	Time of flight	s
T_d	Deposition temperature LPCVD	°C
t_{epi}	Thickness of low doped epitaxial layer	m
T_m	Melting point	K
T_{PDA}	Post deposition annealing temperature	°C
t_{rr}	Reverse recovery time	s
t_s	Thickness of a layer	m
V	Voltage	V
V_R	Reverse Voltage	V
V_t	Threshold voltage	V
$v_{th,e}$	Electron thermal velocity	m/s
W_{ad}	Work of adhesion	eV
W_d	Depletion layer width	m
z	Quantized charge number	C
α	Parameter of the BGN model after Varshni[71]	eV/K
β	Parameter of the BGN model after Varshni[71]	K
β	Reciprocal of thermal potential, q/kT	V^{-1}
γ	Tungs patch parameter	cm$^{2/3}$V$^{1/3}$
$\gamma_{\langle a \rangle}$	Surface anergy of material a	eV
$\gamma_{\langle a \rangle,\langle b \rangle}$	Interface energy between material a and b	eV
δ	Boundary layer thickness in CVD systems	m
ΔE_A	Acceptor ionization energy in respect to valence band edge	eV
ΔE_C	Conduction band offset	eV
ΔE_D	Donor ionization energy in respect to conduction band edge	eV
ΔE_V	Valence band offset	eV
ΔG	crystallization energy	J/m^3
δ_{gap}	Thickness of the dielectric layer in the fixed separation model	m
Δ_i	SBH different of low SBH patch i from background	V
$\Delta \omega$	Sample Tilt	°
ε_0	Vacuum permittivity (8.854×10^{-12} C/Vm)	C/Vm
ε_{gap}	Permittivity of the dielectric layer in the fixed separation model	m
ε_s	Permittivity of semiconductor	C/Vm
η	Ideality factor (often n)	---
η_s	$\varepsilon_s / (qN_D)$	---
θ	Angle of incidence	°
κ	Thermal conductivity	W/cmK
λ	Wavelength	m
μ	Mobility	cm^2/Vs
μ_n	Electron mobility	cm^2/Vs
μ_p	Hole mobility	cm^2/Vs
ρ	Density	g/cm^3
ρ	Resistivity	Ωcm
ρ_c	Specific contact resistivity	Ωcm^2
ρ_i	Interfacial resistivity	Ωcm^2
ρ_s	Semiconductor resistivity	Ωcm

σ_n	Electron capture cross section	cm^2
σ_p	Hole capture cross section	cm^2
σ_p	Shape parameter used in the log-normal distribution	---
σ_γ	Standard deviation of Gaussian patch distribution	$cm^{2/3}V^{1/3}$
τ_n	Ionization time constant	s
φ	Azimuthal angle	°
ϕ_B	Schottky barrier height	V
$\phi_{B,CV}$	Schottky barrier height evaluated from CV measurements	V
$\phi_{B,IV}$	Schottky barrier height evaluated from IV measurements	V
ϕ_B^0	Homogenous background SBH	V
ϕ_c	Contactt material work function	V
ϕ_{CNL}	Charge neutrality level	V
ϕ_m	Work function of metal	V
ϕ_n	Fermi potential from conduction band edge to fermi level	V
ϕ_p	Fermi potential from valence band edge to fermi level	V
ϕ_s	Work function of semiconductor	V
χ, χ_s	Electron affinity of a semiconductor	eV
ψ_{bb}	Band bending	V
ψ_{bi}	Built in voltage	V
ω	Angle of incidence	°

List of publications

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