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Diploma Thesis

Compact Modelling of Transient Response of Multifinger Devices

Submitted in satisfaction of the requirements for the degree of

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by

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ABSTRACT

In order to ensure an effective and a proper function of an ESD protection device, a SPICE type simulation is strongly recommended. However, SPICE type compact models of multi-finger ESD devices are not widely available, especially those that describe high-current characteristics and physical phenomena, such as snapback, that are extremely important for ESD protection.

What distinguish multi-finger SCR ESD models from other SCR circuit models are : the current source that models the avalanche source, the resistor that models substance resistance and the RC line between the fingers to model the delay of diffusion the carriers.

The main aim of this thesis is to find good approaches for modeling these factors and thus for modeling entire multi-finger ESD SCR devices, such as the device from the paper [1]“Simultaneous and Sequential Triggering in Multi-Finger Floating-Base SCRs Depending on TLP Pulse Rise Time”.

In this thesis two compact multifinger ESD protection device models were presented for SPICE type transient simulation. The first model is a model of the device from [1], which is tested, as in the paper, against Transmission line pulses (TLP). While the second model is a model of an asymmetric multifinger ESD protection device, that takes more modelling factors into account, and is tested against power surge. A close look is further taken at the parameters of the model and their effect on the trigger behavior.

Hossam Eldin Jomar - May 2021

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Last but not least, many thanks to my family for supporting me every step of the way.

Hossam Eldin Jomar - May 2021

CONTENTS

LIST OF FIGURES

LIST OF SYMBOLS

ADS	Advanced Design System
ESD	Electrostatic Discharge
SCR	Silicon Controlled Rectifier
TLP	Transmission Line Pulse
VF-TLP	Very Fast Transmission Line Pulse
SOI	Silicon On Insulator
IC	Integrated Circuit
IEC	International Electrotechnical Commission
DUT	Device Under Test
RT	Rise Time
BJT	Bipolar Junction Transistor
SFT	Sequential Finger Triggering
HBM	Human Body Model
TCAD	Technology Computer Aided Design
SDD	Symbolically Defined Device

1 INTRODUCTION

1.1 Thesis Organization

The central focus of this thesis is the provision of ADS simulation models for multifinger ESD protection devices, their qualitative analysis and the investigation of the dependency of each parameter of the model on its triggering behavior.

We start, in chapter 1, with a motivating introduction about multifinger ESD protection devices, its testing standards and the pulse used in each standard. We define each pulse and show the main differences between them. Before starting to model an entire ESD device, in chapter 2 we take a closer look at a single finger (a single SCR) and its components, we browse the effecting factors on its IV characteristics and understand its functionality by observing its transient response on an TLP pulse.

The first modeled device in this thesis is a multifinger ESD protection device, as described in [1], that consists of 16-finger floating-base SCR devices fabricated on lightly p-doped Silicon-On-Insulator (SOI) and being tested with a TLP pulse. In chapter 3, we define this device physically and then we discuss our model design. We further calibrate our model to match the IV curve of the device from [1] and configure the model to show similar behavior. Afterwards we start with the transient simulation and analysis by applying a TLP pulse on it. First we analyze the trigger behavior of our model and then we discuss the main parameters of the model and their dependency on the trigger delays of the individual fingers. At the end of chapter 3, to summarize the chapter, we compare three kinds of IV curves for the studied device.

After modelling the TLP response of an ESD protection device, in chapter 4, we will go beyond that and model another multifinger ESD device that is going to be tested with a power surge.

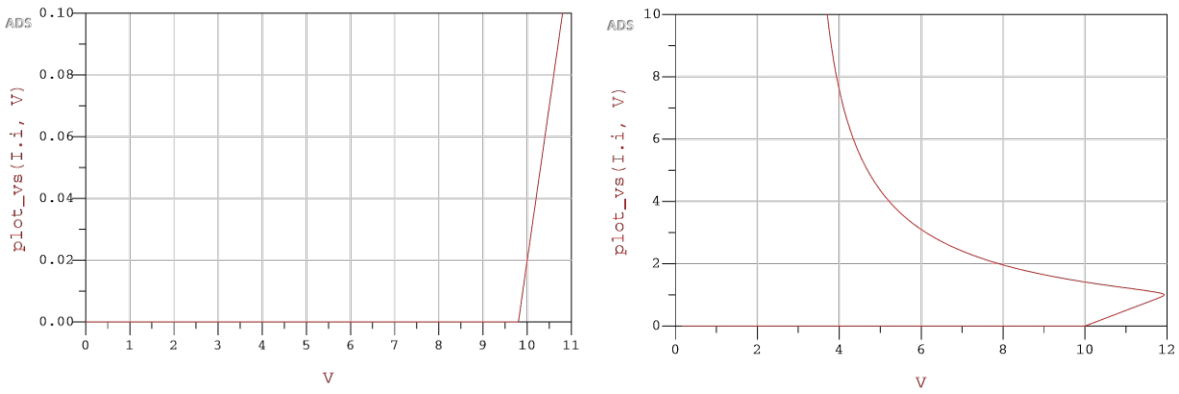
The new model is described in chapter 4 and so is the model configuration. We also analyze the trigger behavior of this model and study the effect of some parameters on it.

1.2 ESD Protection

1.2.1 ESD Protection Devices

Electrostatic discharges can cause huge damage to integrated circuits (ICs) and other sensitive components in circuit boards. Therefore, such ICs and boards are nowadays equipped with ESD protection devices. The main aim of an ESD protection device is to shunt high current discharges by creating low-impedance discharging paths and to clamp voltage on the core circuitry to a safe level in order to avoid breakdown of insulators and damage in the IC [2], which can be caused by an ESD event.

The two typical I-V characteristic of an ESD protection, as shown in figure 1.1, are simple turn on and I-V snapback. Devices with I-V snapback characteristic can usually handle higher currents, especially the SCR (Sillicon Controlled Rectifier or just Thyristor) devices, which may serve as a very good ESD protection due to its deep snapback I-V characteristic, and which will be used as an ESD device in this thesis.



a) b)

Figure 1.1 Typical ESD characteristics : a) simple turn on , b) snapback

1.2.2 IEC Transient Immunity Testing

Given the fact that failures due to ESD will be perceived as poor quality and a reliable circuit protection should be accomplished, immunity standards are needed to determine the minimum requirements for equipment manufacturers.

That's why the International Electrotechnical Commission (IEC) has developed immunity testing standards for system level ESD. Three of these standards deal with transient immunity [3]:

a) IEC61000-4-2 ESD Standard:

The IEC61000-4-2 ESD standard is the basic standard for testing electrostatic discharge immunity . It defines immunity requirements for electrostatic discharges which can be coupled into the system directly or through radiation. It applies a defined current waveform at a certain voltage level from a simulator.

Figure 1.2 shows an ESD current pulse waveform according to IEC61000-4-2 standard.

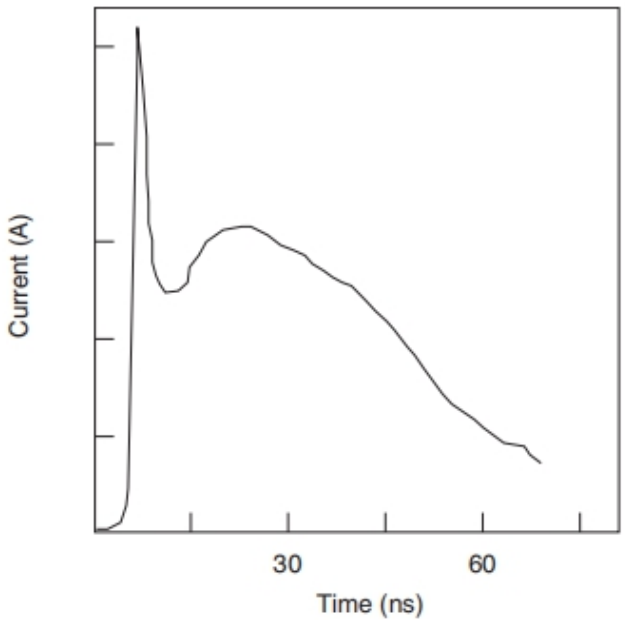


Figure 1.2 Current pulse waveform according IEC 61000-4-2 [2]

b) IEC61000-4-4 ESD Standard:

This standard is specialized with fast transient immunity. A specified burst waveform is applied via a defined coupling on the device to investigate its immunity.

c) IEC61000-4-5 ESD Standard:

The IEC61000-4-5 ESD standard has been developed for “surge testing”.It addresses the transient conditions caused by lightning strikes and switching. It defines the 1.2/50 us (V) - 8/20 us (I) combination wave. Figure 1.3 shows the IEC 61000-4-5 surge test pulse open circuit waveform.

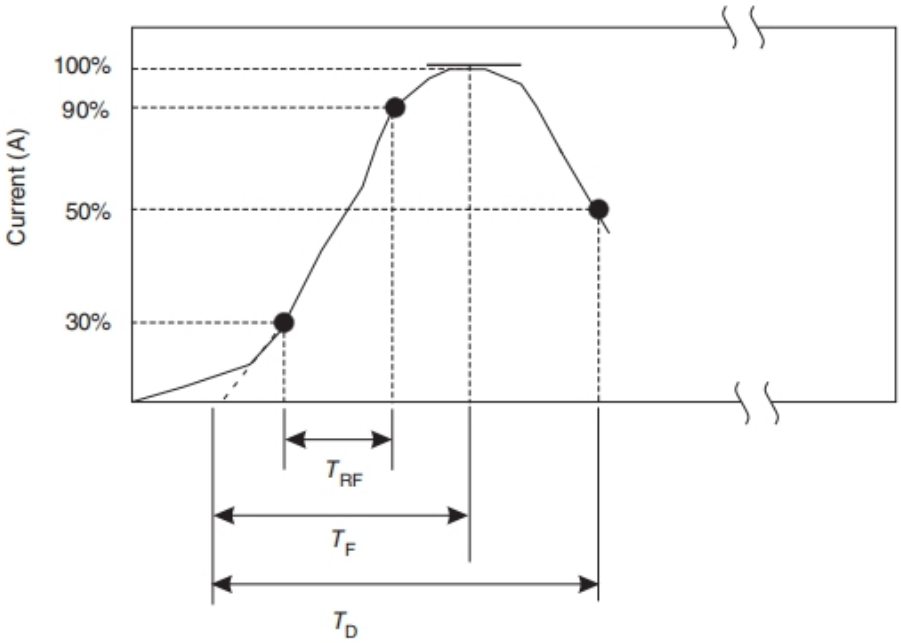


Figure 1.3 Current pulse waveform according IEC 61000-4-5 [2]

1.2.3 The Importance of Transmission Line Pulse and Power Surge

Since the wave duration and the rise time of The IEC61000-4-2 ESD standard are in the range of nanoseconds, a **Transmission Line Pulse (TLP)** tester is used to provide the current wave that is very similar to the IEC61000-4-2 to investigate the immunity according to this standard.

TLP is a test method that applies a rectangular pulse to a component with rise time of 10ns and fall time of 100ns. In some cases a faster rise and fall time is used (1ns/10ns) and the pulse is called “Very Fast Transmission Line Pulse (VF-TLP)”.

TLP testing has seen considerable growth in the ESD. This form of testing was used first to study human body model (HBM) [2] in on-chip ESD, but it is now also a very

effective tool to check the IEC61000-4-2 standard immunity in system level ESD. It is a very useful test method, that helps to investigate specific device parameters in the time domain, such as I-V characteristics in which we are interested in this thesis.

Nevertheless, TLP is too fast for the IEC61000-4-5 standard and lightning strikes simulations and this is where **The Power Surges** comes in. The only way to evaluate the immunity of components according the IEC61000-4-5 standard is to apply the 8/20 us current wave that simulates the surge.

Surges usually have a fast rise, followed by a slower fall we approximate it in this thesis with the positive part of a sinusoidal signal (see figure 1.4).

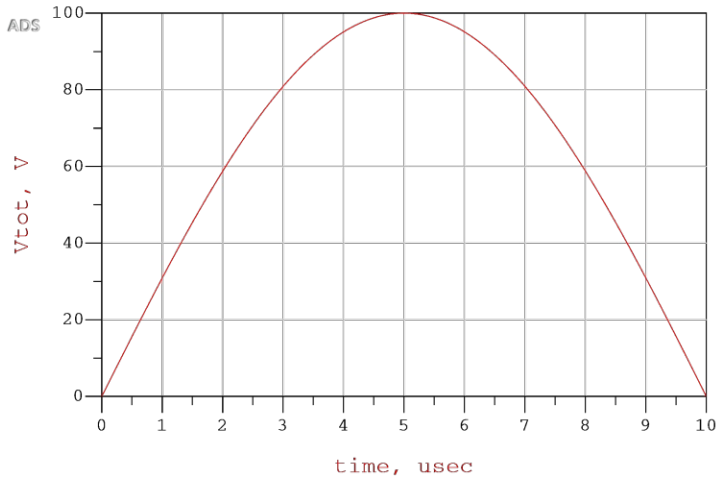


Figure 1.4 Voltage surge waveform generated by ADS

The main different between TLP and surge is the time domain which is in the range of nanoseconds at TLP but in microseconds at surges. Since both test pulses are mostly common on ESD testing and since this large difference in time domain makes the device under test (DUT) reacts very differently to each pulse wave, both these pulses will be treated in this thesis.

1.2.4 Multifinger ESD Protection Devices

Multifinger ESD protection devices are multiple parallel devices, in which sometimes a common control component, such as a gate of a thyristor, is used. By connecting the gates of the single fingers, in case the finger is a thyristor, in a parallel connection to form a multi-finger ESD protection, the ESD device can bypass a higher level of electrostatic charge than one finger [4].

In this case, it is more beneficial to have all fingers of a multifinger ESD protection triggered to maximize the amount of current that can be handled by the protection. That's why simultaneous and sequential triggering has received much attention in the literature recently [1] [2] [4].
It is found that the fingers trigger simultaneously when the rise time is very short but they trigger sequentially when the rise time is long (in the range of nanoseconds) [1].

"Simultaneous and Sequential Triggering in Multi-Finger Floating-Base SCRs Depending on TLP Pulse Rise Time" is the name of a work [1], that analyze in detail the triggering mechanism of multi-finger floating-base SCRs as a function of TLP once for short rise time (RT=300ps) and once for long rise time (RT=10ns) both experimentally and by TCAD simulation.

16 finger SCR devices fabricated on p-doped silicon-on-insulator (SOI) substrate were studied in [1]. For RT=10ns a sequential finger triggering (SFT) has taken place and the following behavior was observed:

-Slow and fast triggering processes were found, as illustrated in figure 1.4, with long and short trigger delay (τ_{long}=15-150ns) (τ_{short} = 3-5 ns).

-Each triggering of a finger pair leads to a voltage drop.

-Triggering delay depends on current density: Larger delays were observed when more fingers triggered and shorter delays were observed with higher currents (see also figure 1.5).

The start point of this thesis will be to model the ESD protection described in the above mentioned work and to compare the behavior of the model with the behavior described in the work.

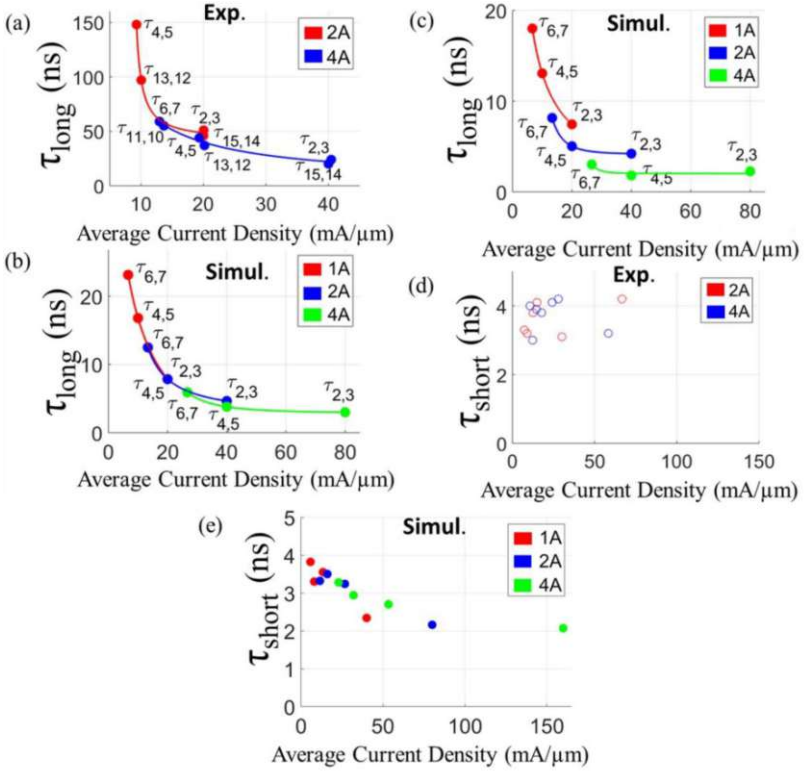


Figure 1.5 Experimental (a,d) and simulated (b,c,e) long (a-c) and short (d,e) time delays between the triggering of fingers as a function of average current density J; R is 0 Ω in (b) and (e) and R = 1 Ω in (c). $\tau_{i,i+1}$ labels in (d) and (e) are omitted due to interwoven values. Taken from[1]

2 MODELLING AN SCR

Advanced Design System (ADS) is the name of the simulator used in this thesis. This simulator is very accurate and it supports DC analysis, transient analysis, and all the tools that we will need in this work.

Before we begin modeling entire devices, let's take a closer look at the model of a single SCR, which is the main component in our device.

2.1 SCR Model

The SCR essentially consists of a PNPN structure and it can be viewed, as illustrated in Figure 2.1, as two bipolar transistors [4] :

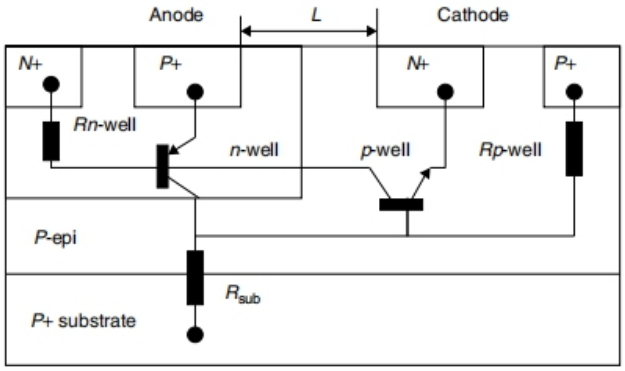


Figure 2.1 Cross section of a lateral SCR in a CMOS process showing the parasitic *pnp* and *npn* transistors. *Rn*−well is the *n*-well resistor, *Rp*−well is the pwell resistor, and *R*epi is the resistance of the epi layer. The low-resistance (5mcm) substrate is assumed to be at 0V, taken from [4]

-pnp transistor is formed by the anode as the emitter, the n-well as the base, and the p-well as the collector.

-npn transistor is formed by the cathode as the emitter, the p-well as the base, and the n-well as the collector.

In this thesis, the SCR will be modeled by the equivalent circuit shown in Figure 2.2. Rnwell and Rpwell denote the well resistances.

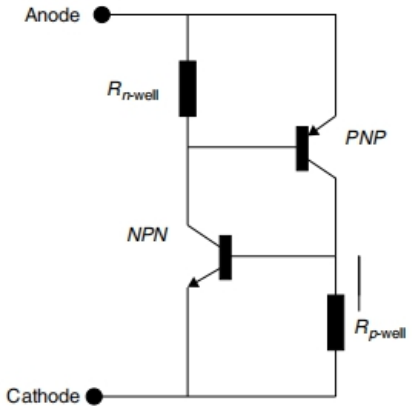


Figure 2.2 SCR Model

2.1.1 BJT Model

Although we are using the predefined ADS model of the BJT transistor, it's not only sufficient but also necessary to have a close look at the ADS BJT Model in order to set the parameters properly and to predict their effect on the behavior of the entire Model.
The BJT Model used in ADS is called the Gummel-Poon Model, which is complicated and models all the DC and AC characteristics of a bipolar transistor [5]. However, if we define only some of its parameters, we can reduce it to the model shown in Figure 2.3.

This model is nonlinear and it models the transient behavior good enough.
We will set the resistors R_C, R_E, and R_B, which represent the series resistance of the semiconductor, to zero and we will see the effect of the resistance of the material later separately (by adding R_{top} and R_{bot}).

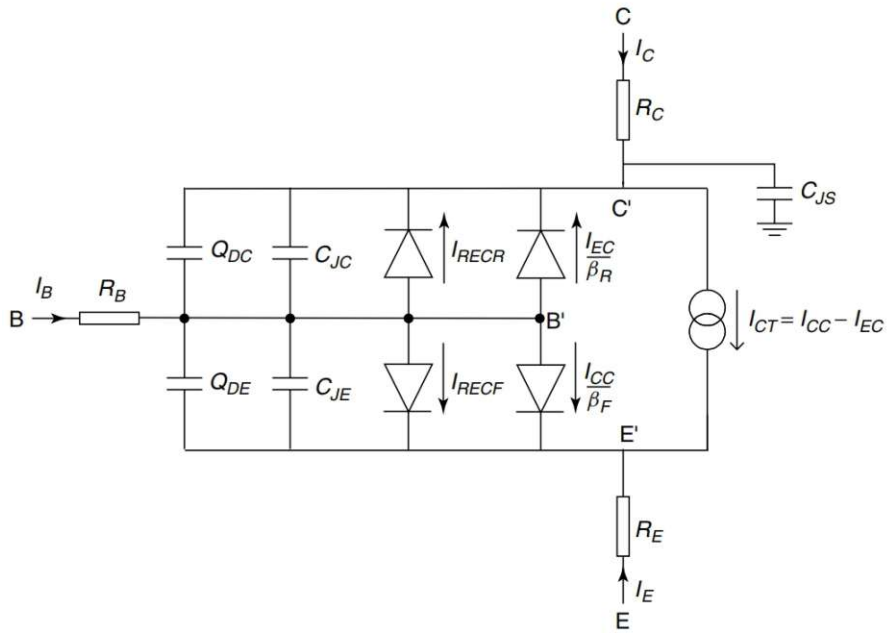


Figure 2.3 The non-linar hybrid-π model of BJT [5]

By assuming a fast transistor we can also neglect Q_{DC} and Q_{DE}, which represent the charge due to the mobile carriers in the transistor.

The capacitors C_{JC} and C_{JB} represent the collector/base and the emitter/base depletion capacitances and are of great importance for the proper simulation of a transient model.

2.1.2 Avalanche Source

Avalanche breakdown is the process that causes the SCR to trigger without applying an additional plus on its Gate, which is the case when the first SCR triggers in our model.

It's necessary, therefore, to have a good model for avalanche breakdown, which can most simply be modeled as a current source.

The PNPN structure of SCR - as shown in figure 2.4 - has three junctions. The first and the third junction J1 and J3 are already forward biased in our model. Only J2 is reversed biased in the off-state and the SCR triggers only when J2 undergoes avalanche breakdown.

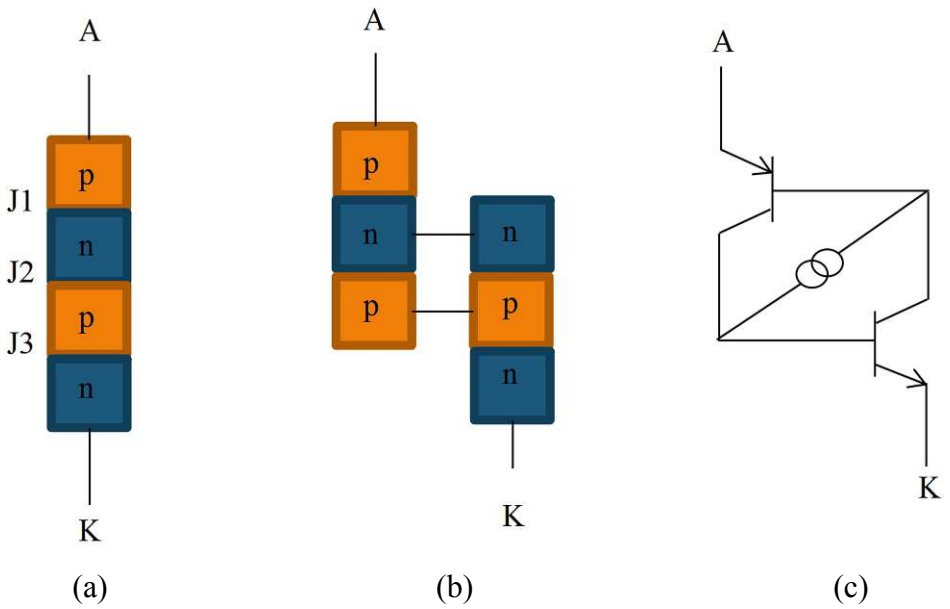


Figure 2.4 SCR Structures : (a) Basic Structure (b) Structure of Two Transistor Model (c) Two Transistor Model with avalanche source

So the Avalanche source should be placed between the base of each BJT and the collector of the other, where exactly J2 takes place (see figure 2.4 c).

In [6] and [7] was the current of the avalanche source in a BJT approximated to:

$Iav_{BJT}=(M-1)(Ic)$

M is the multiplication factor and it can be written as $M = \frac{1}{1-(\frac{Vbc}{Vbd})^n}$

Where Vbd is the avalanche breakdown voltage.

By assuming that both transistors have the same Vbd we can conclude the avalanche current of the SCR :

$Iav=(M-1)(Ic1+Ic2)$

In order to model this current and voltage controlled current source in ADS we need to use a 4 port SDD (Symbolically Defined Device), which is a component in ADS that helps to create equation based, user-defined, nonlinear components like the avalanche source in our case. The basic of the submodel in Fig. 2.5 has been provided by H.Karaca, the author of paper [1].

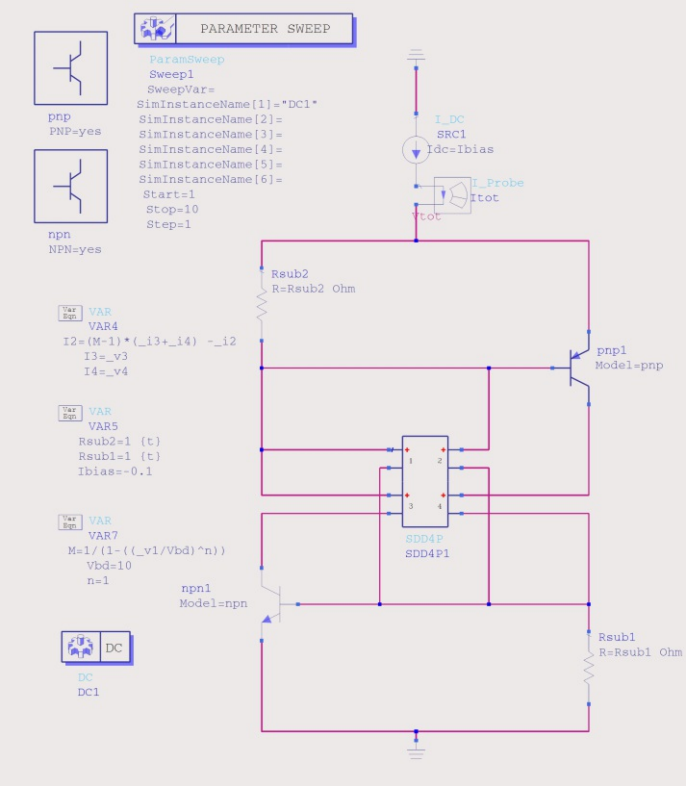


Figure 2.5 SCR Model with Avalanche Source

Figure 2.5 illustrates how the avalanche source is modeled by using a 4 port SDD: Ports 3 and 4 are used to measure the collector current of both BJTs. Port 1 is used to measure the Voltage Vbc which is the same for both transistors and Port 2 is used to generate the current.

Besides this current and voltage controlled current source, there are some other simple alternatives to model the effect of avalanche breakdown. The simplest model can be a resistor between the bases of the transistors that allow the current to flow in the second junction J2.

Another way to model it is by using a voltage controlled current source that generates a current Iav=(M-1)*10^{-12} . We noticed that the current here doesn't depend on the currents Ic1 and Ic2, as it was in the main model, it is a function of M, which depends only on Vbc.

In this thesis, a DC simulation of all three Models of avalanche breakdown is carried out in order to observe and compare their IV characteristics. The results are shown in figure 2.6.

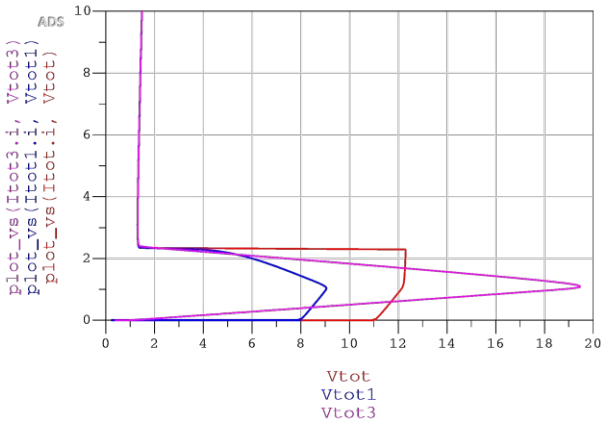


Figure 2.6 I-V characteristic of the SCR model with avalanche source
The read curve for Iav=(M-1)(Ic1-Ic2), the blue curve for Iav=(M-1)*10-12 , and the magenta curve when we set R=50 to model avalanche breakdown

Although these alternatives don't have the same level of accuracy, they still can provide a very similar IV characteristic. However, for the rest of the work, we are going to use the most accurate model, which is the current and voltage controlled current source we mentioned at the beginning.

2.1.3 SCR Triggering by External Base Current Pulse

In the model of multi-finger ESD devices only first finger triggers without gate pulse. All the other fingers should be triggered by applying a pulse on their gates. Thus, it is beneficial to model this type of triggering and compare it with the first one to see how the pulse affects the I-V characteristics.

To achieve this, a DC simulation of an SCR with an external base current pulse was built as in Figure 2.7 and the I-V curve was plotted with and without external base current. The parameters are given in table 2.1.The SCR used consists of 2 BJT with $\beta npn=\beta pnp=2$, Resistor $R_{nwell}=4.7\Omega$, and without R_{pwell}.

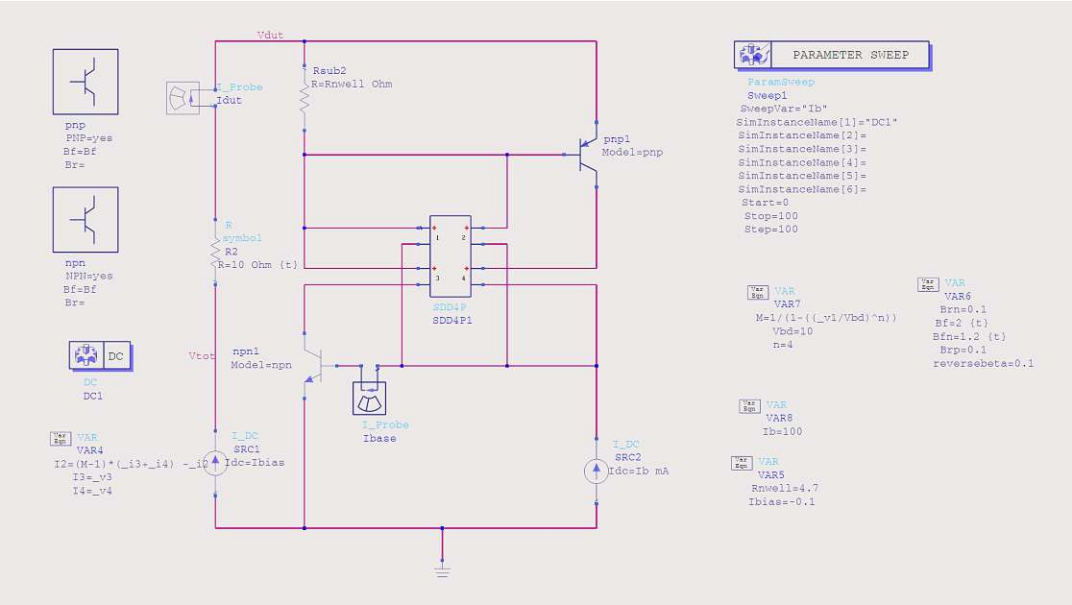


Figure 2.7 Schematic of SCR with avalanche source and external current

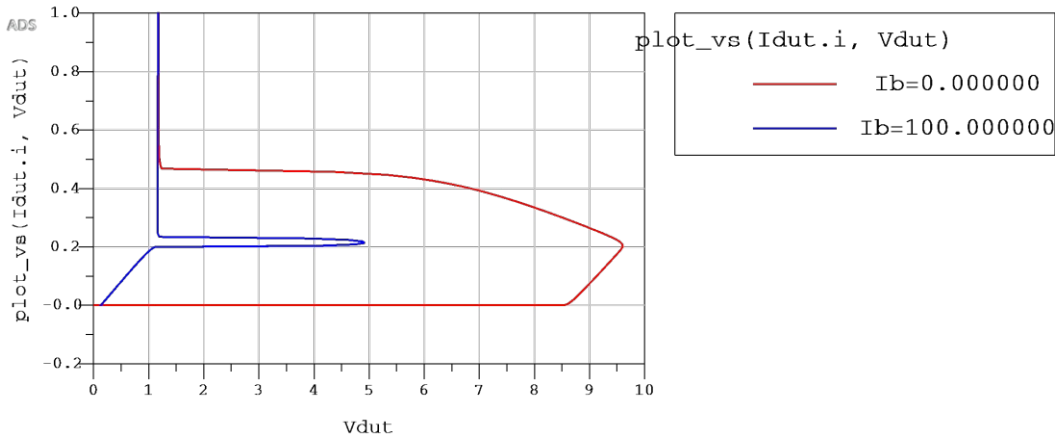


Figure 2.8 I-V characteristics of SCR with and without external current Ib

We can see in figure 2.8 that the trigger voltage decreases, as expected, by adding the external base current. We notice also that the current starts to increase at very low voltages in the case of external pulse and then it stabilizes at 200mA. The npn transistor triggers due the external current source and a current flows through the collector equals β*Ib =2*100m=200mA.

Then, when a higher voltage is reached, the pnp transistor also triggers and we can say that the entire SCR triggers.

2.2 Transient Response of SCR

To characterize the transient response of SCR a TLP Model is used. In this model, our device is supplied with a transient voltage source that generates a square voltage Vtot

(see Figure 2.9). Furthermore to model the internal resistance of the source, a resistor R is in series connected to the source. The circuit parameters are given in table 2.1.

Rise Time	10ns	Pulse width	500ns	βnpn	2	Rnwell	4.7 Ω
Fall Time	10ns	Pulse amplitude	50V	βpnp	2	Rpwell	∞

Table 2.1 the circuit parameters of the SCR transient model

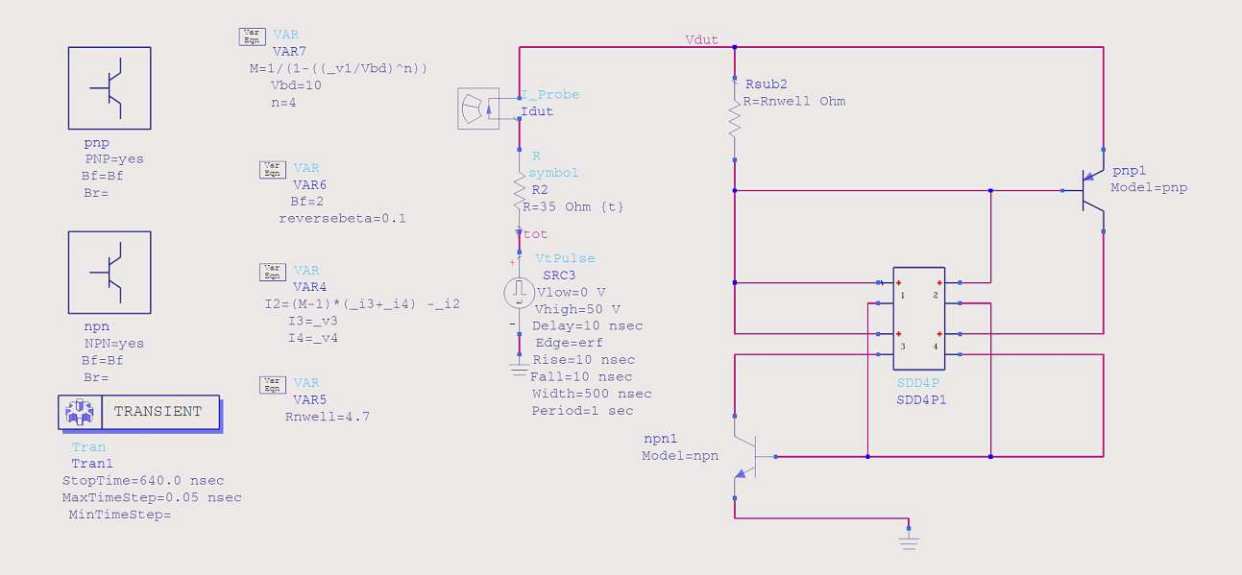


Figure 2.9 Transient model of SCR

From Figure 2.10 it is easy to see that the voltage on the device under test V_{dut} drops to a safe level (holding voltage) once the device triggers and in this particular moment the current start to flow through the device. Later when the current falls below the hold current I_{hold} , the voltage jump a bit, and then it decreases again when the pulse ends.

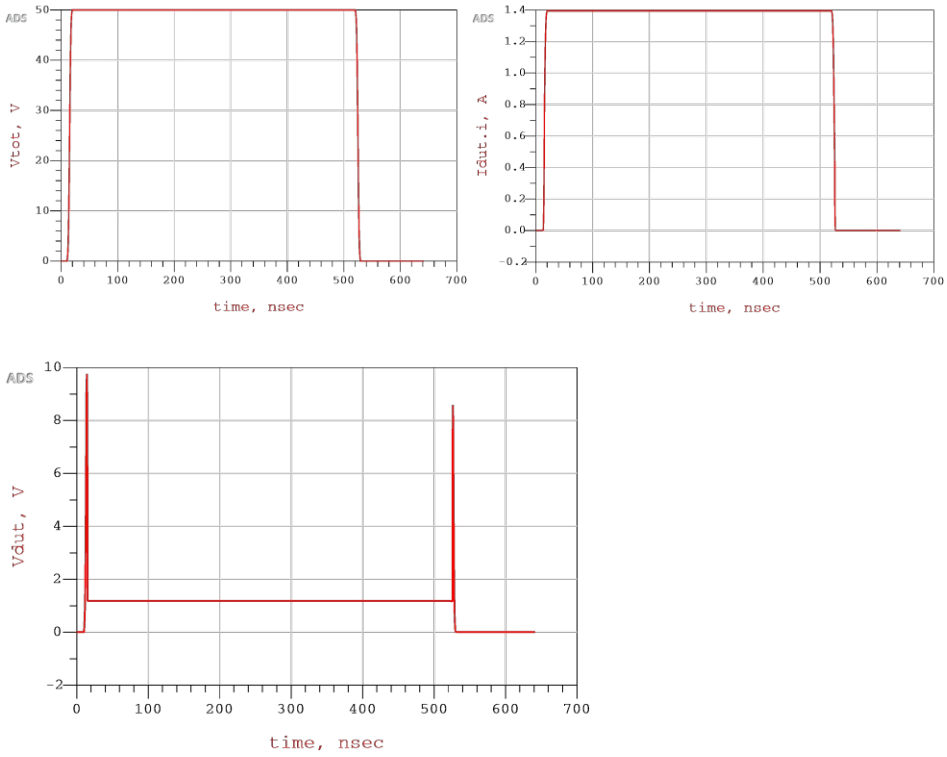


Figure 2.10 The generated wave Vtot, the voltage on the device Vdut, and the current Idut as a function of time

Figure 2.11 shows I-V characteristic obtained from the transient model. We can see that the IV curve while the voltage is increased differs from the IV curve while the voltage is decreased.

When the voltage exceeds the trigger voltage Vtr the device triggers and the voltage starts to drop with increasing the current. It reaches the on-state of the SCR with a current that is higher than the hold current and that explains the hysteresis loop in the I-V curve.

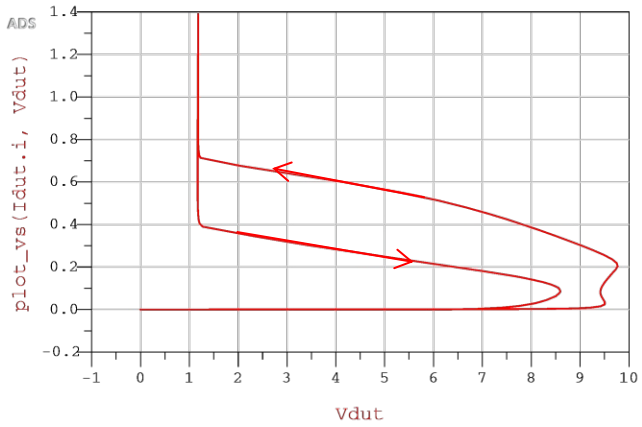


Figure 2.11 I-V characteristics from transient simulation

3 MODELLING TLP RESPONSE OF A MULTIFINGER ESD DEVICE

3.1 Model Definition

As mentioned in section 1.2.4, the initial point of this thesis is modeling the ESD protection device of [1]. As shown in figure 3.1 this device consists of 16-finger floating-base SCR devices fabricated on lightly p-doped Silicon-On-Insulator (SOI).

The n+ emitters of the npn transistor are grounded, the p+ emitters of the pnp are stressed positively and all the fingers are coupled via the same p-substrate.

The initial idea was to model the fingers as two bipolar transistors (see section 2.1). Only the first finger is equipped with an avalanche source to trigger because only the first finger in the real device triggers due to avalanche breakdown.

The rest of the fingers are coupled via RC transmission lines and they trigger each other. In Order to get a proper model of the coupling, we have to understand the triggering behavior of fast and slow processes and the origin of each of them, which is going to be explained using Figure 3.2.

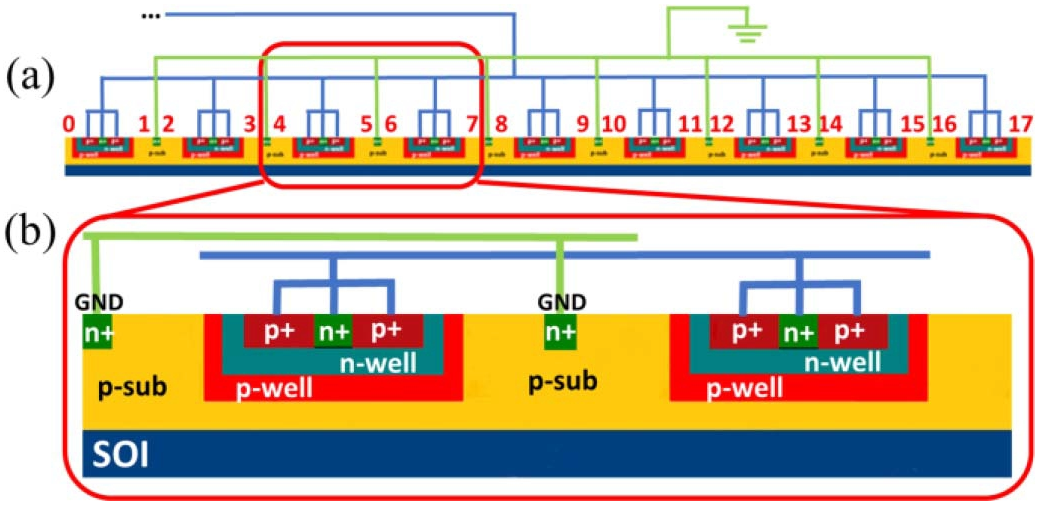


Figure 3.1 (a) Modeled 16-finger floating base SCR structure (b) Enlarge image for four fingers taken from [1]

The fast process happens because of strong electron injection from one n-well to another one i.e. from point B to point B´ in Figure 3.2, so we connect these points in our Model.

The main reason of the slow process on the other hand is that the same p-well serve two fingers. So as shown in Figure 3.2 we connect C to C´ which represents the sides of the p-well.

To simulate carrier diffusion between fingers and to assure a delay between triggering the fingers, the fingers are connected via RC networks.

The n-well, which is represented by the base of the npn and the collector of the pnp transistor in our model, is connected to the positive source via a resistor Rnwell that represents the resistance of the n-well.

Since the resistance of the p-well is added to the resistance of p-sub and they both form a big resistance together, Rpwell will be considered infinity in our model.

To simulate carrier diffusion between fingers and to assure a delay between triggering the fingers, RC network is placed between the fingers.

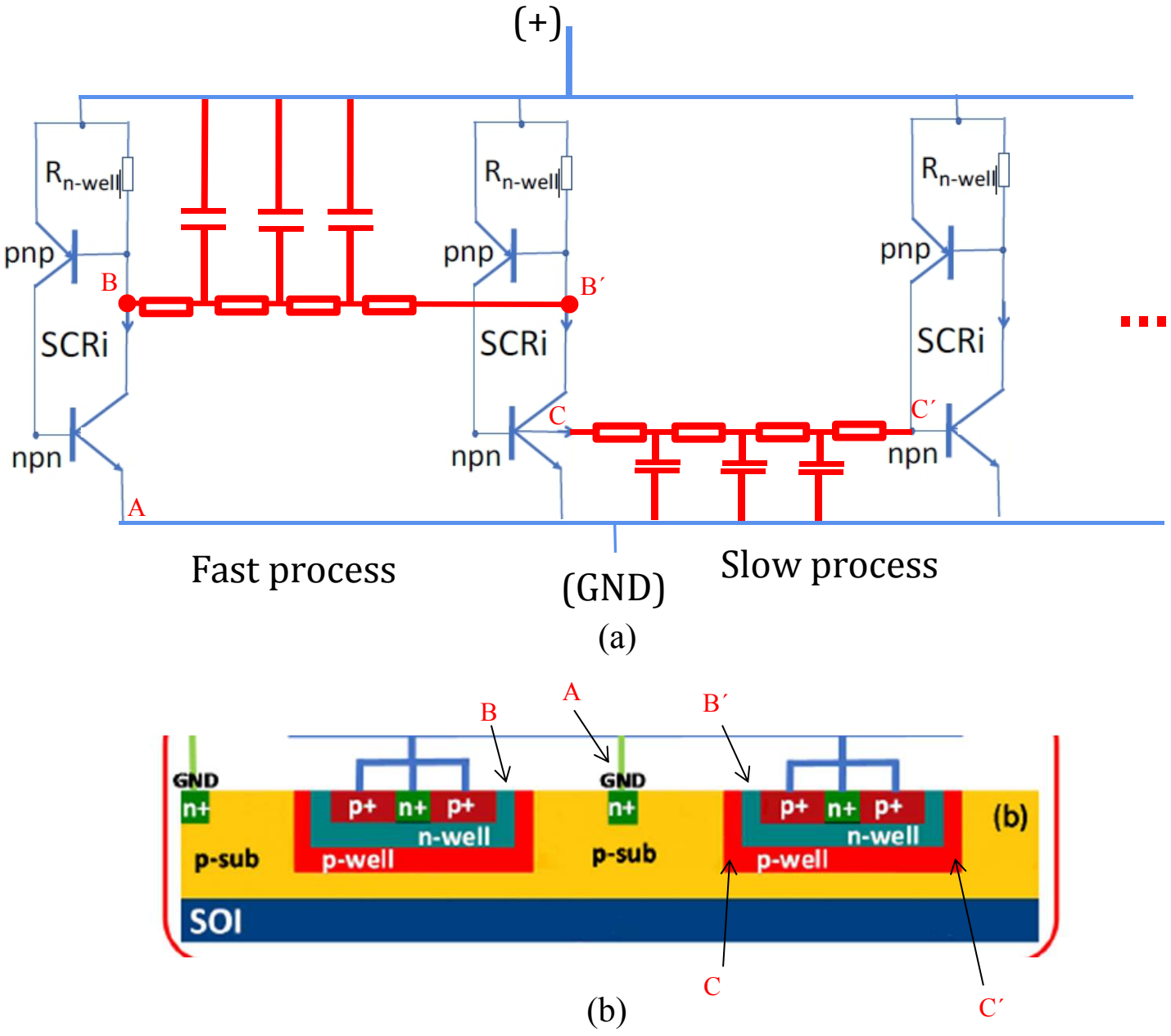


Figure 3.2 Modelling fast and slow processes. Relation between the (a) lumped element representation and (b) device cross section. The figure was taken from slides of D.Pogany.

The TLP tester will be modeled as a ramping voltage source with a 50Ω resistance.

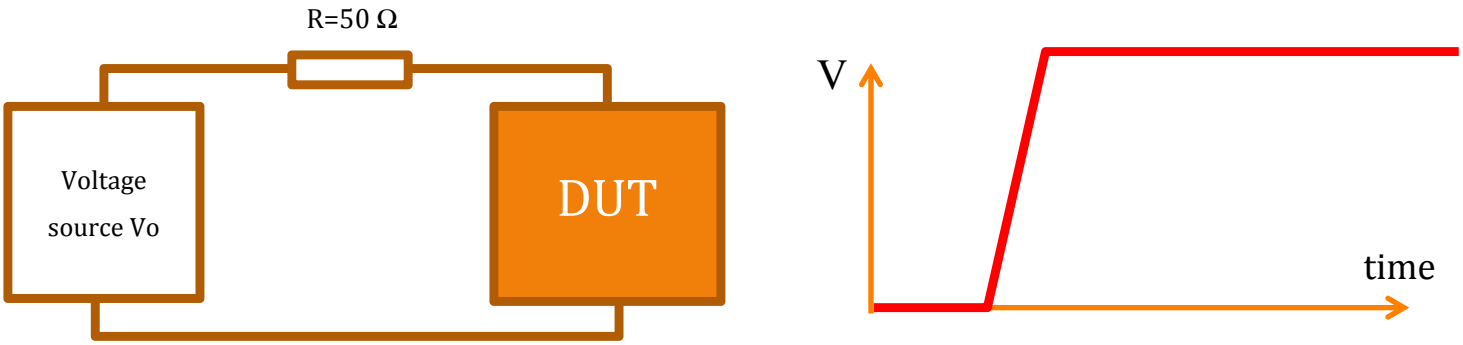
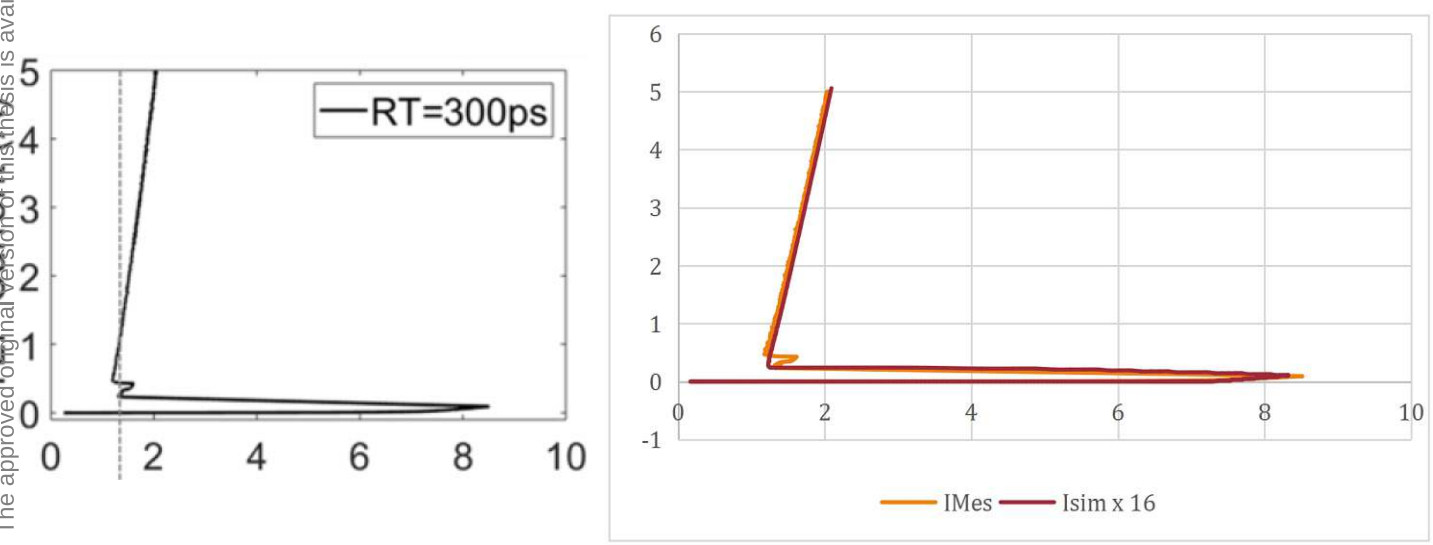


Figure 3.3 The model of the TLP tester

3.2 Calibration and Adjustment

The first step to simulate the above described device properly is to adjust the single SCR of the model so that its I-V characteristic matches the one published in the paper [1] (see figure 3.4 a).

Since the I-V curve in the paper is made for the whole device which consists of 16 fingers, the current should be divided by 16 to get the I-V curve of a single SCR.



(a) (b)

Figure 3.4 IV curve of the device (a) published in [1] (b) comparison between [1] and the values of the simulation x16

A DC simulation for a model of single SCR was carried out (see figure 3.5) and the parameters of the model were changed to match the I-V curve from the paper. In this simulation, the source current Idut was swept from 0 to 1A and the IV curve was plotted.

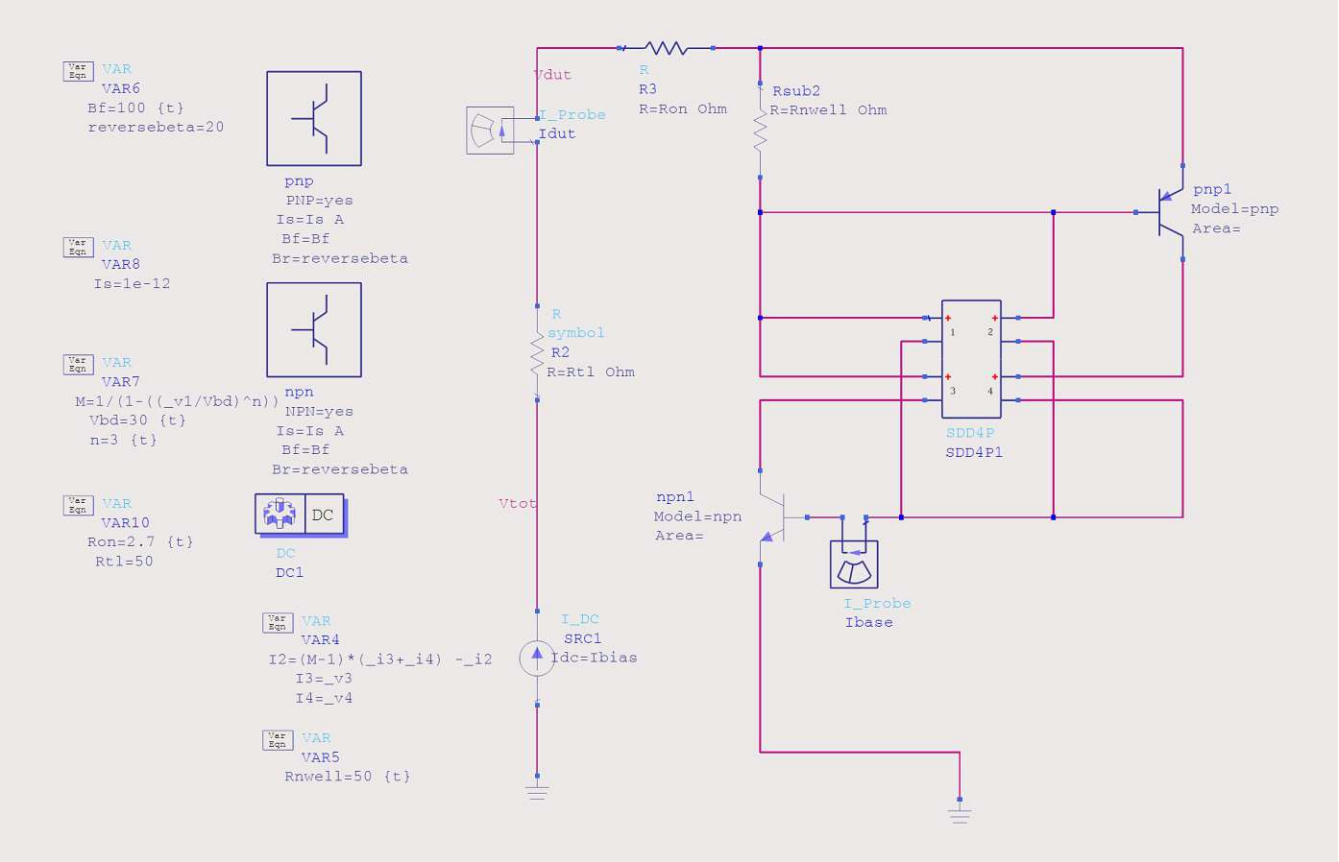


Figure 3.5 Schematic of the Simulation used to calibrate the single finger

These parameters were calibrated :

-Avalanche source parameters (Vbd_{bjt}, n): as mentioned in section 2.1.2, the multiplication factor of the avalanche can be written as $M = \frac{1}{1-(\frac{Vbc}{Vbd})^n}$.

By changing Vbd_{bjt} and n in the equation the avalanche current Iav changes and therefore Vbd of the SCR will change as well.

-Rnwell: changing Rnwell causes the trigger current to change and thus the slope of the line between breakdown point and trigger point in the IV curve.

-BJT transistors parameters (β,Is): assumed that these two parameters are the same in both BJT, meaning that βnpn=βpnp=β and Is,npn=Is,pnp=Is.

These parameters have a big effect on almost all the critical points of the IV curve (I_{hold}, V_{hold}, Itr, Vtr ...).

-Ron: This resistor is placed in series with the SCR and it represents the metal resistance in the real chip. Ron determines the slope of the IV curve in the ON state.

The calibration was done in such a way that an approximation is achieved using feasible parameters. Table 3.1 shows the parameters obtained.

Vbd_{bjt}	n	Rnwell	β	Is	Ron
12	3	50Ω	5	1pA	2.7Ω

Table 3.1 parameters of the calibrated model

3.3 Model Configuration

The model defined in 3.1 was simulated using ADS. 12 Finger were connected via fast and slow process RC transmission lines and supplied by a TLP tester.
The same calibrated SCR from part 3.2 was used in this simulation with the same parameters.

Figure 3.6 shows a simple schematic of the model. This figure has been provided by D.Pogany, and is used here to explain the model configuration. Furthermore it will be used many other times in the thesis after modifying it to explain different current paths in the devices.

As shown in figure 3.6 each fast process RC network in this model consists of 9 elements: 5 resistors with R1= 10 mΩ and 4 capacitors with C1=200 pF. Slow process RC networks have the same number of elements but with different values namely: R2=10 Ω and C2=200 pF.

The metal resistance is represented by two resistors connected to each finger in series. Rtop between the finger and the source, where Rbot between the finger and the ground.

At the beginning of this simulation, we will neglect this metal resistance (Rtop=Rbot=0) so that we added it later and take a closer look at its effect on the triggering behavior.

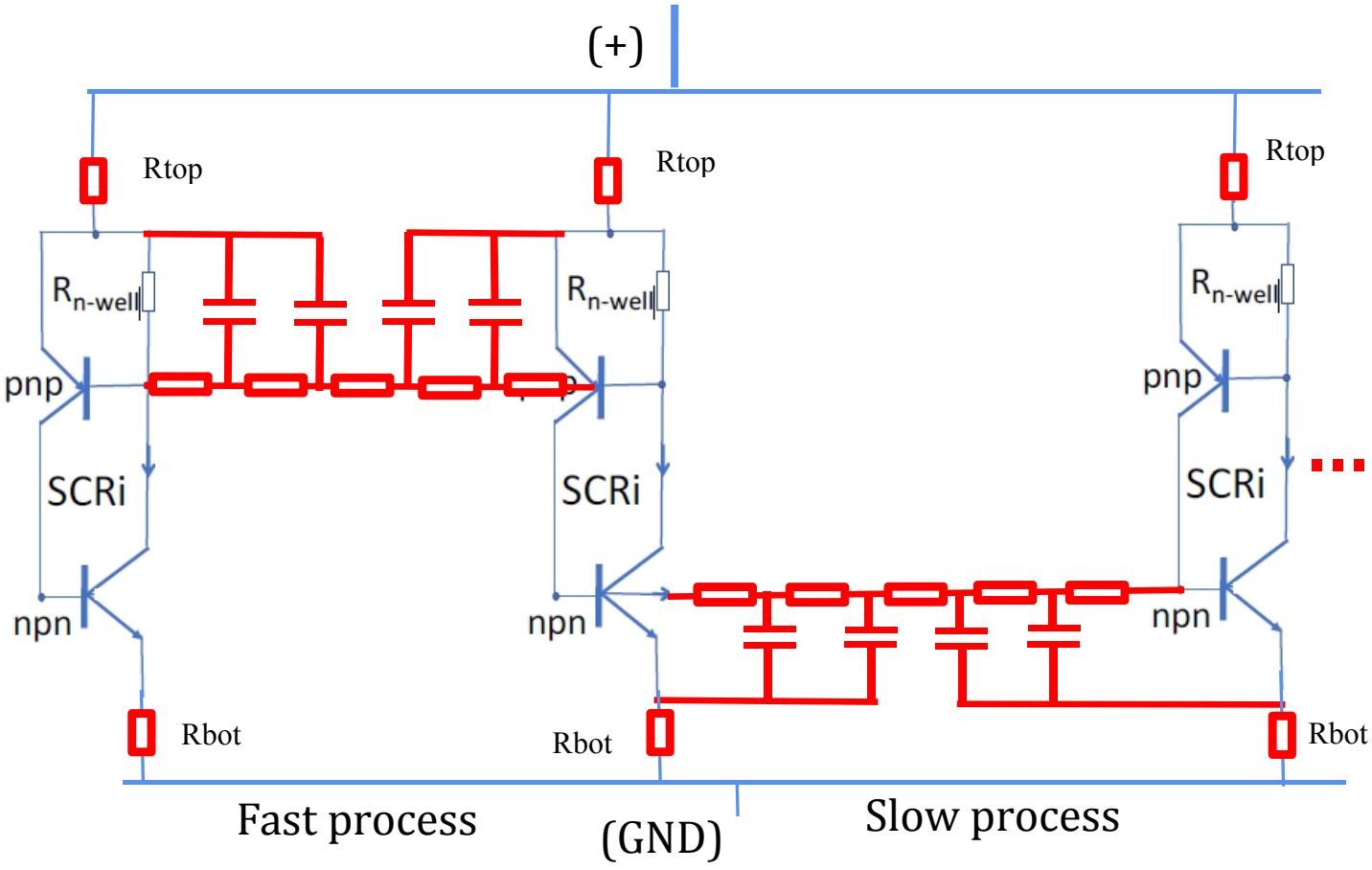


Figure 3.6 Simple schematic of three fingers of the simulated model. The figure was taken from slides of D.Pogany.

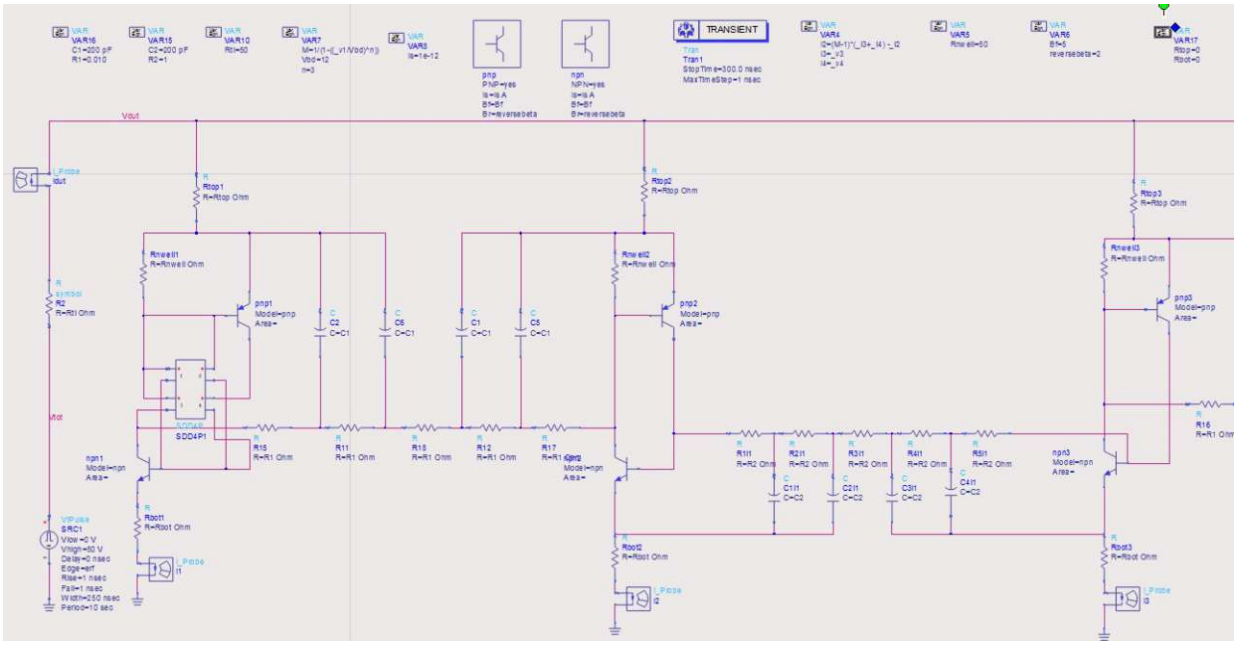


Figure 3.7 Ads schematic of the first 3 fingers of the simulated model

As in figure 3.3 the Source is connected to a resistor Rtl= 50Ω and it generates one voltage rectangular pulse with an amplitude of Vmax=50 V, width=250 nsec, Rise time = 1 nsec, and fall time = 1 nsec (see figure 3.8).

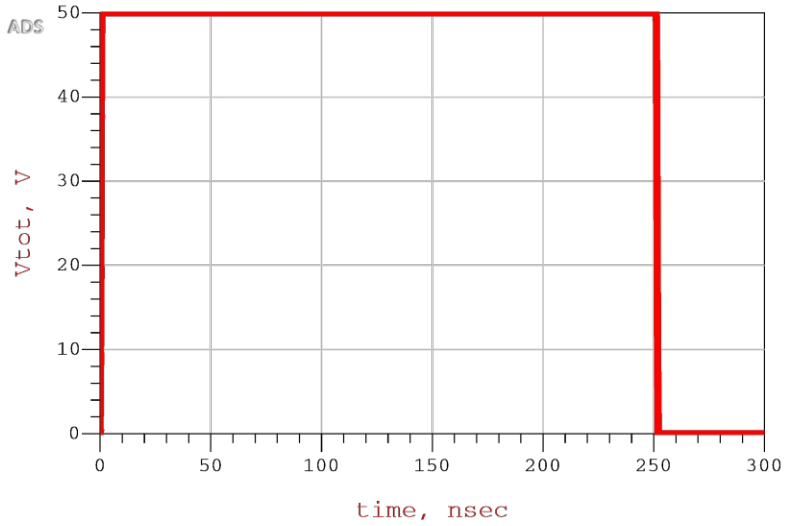


Figure 3.8 The generated voltage pulse by the source

3.4 Simulation Results and Model Behavior

After configuring the model the simulation was run and the following results were observed:

3.4.1 Total Voltage and Total Current (Vdut, Idut)

The voltage on the whole device Vdut increases at the beginning and reaches a peak of about 41V and then drops to about 0.7V when the first finger triggers and remains at this value until the pulse has ended.

The Current Idut increases at the beginning as well and reaches its maximum of about 1 A when the Voltage reaches its minimum.

As expected, this behavior corresponds to the typical behavior of an ESD protection device.

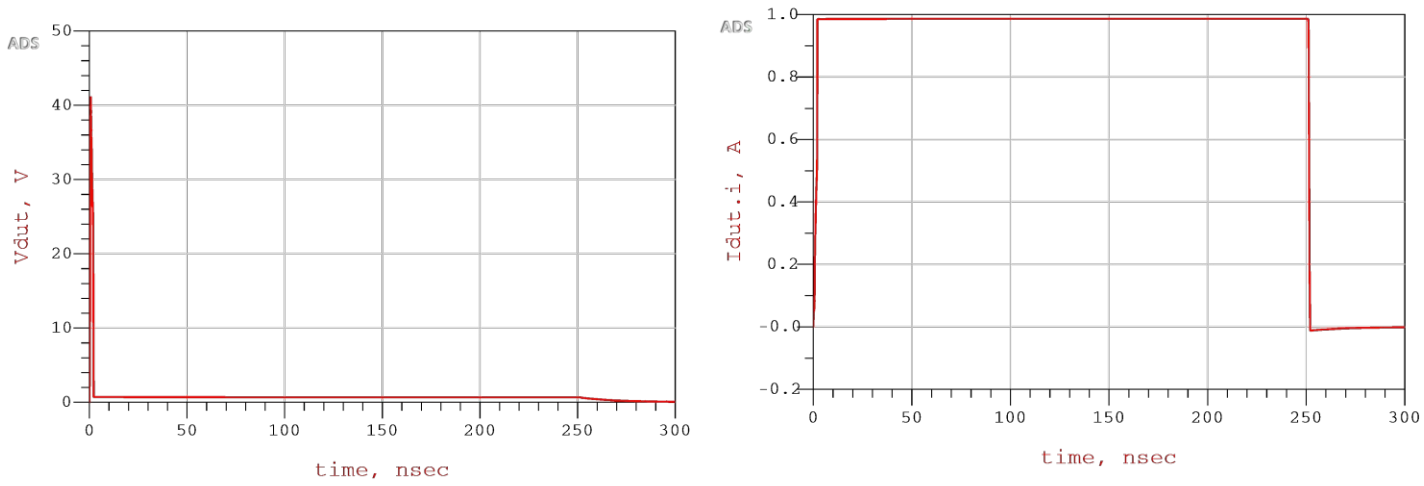


Figure 3.9 Total voltage on the device Vdut and total current Idut

3.4.2 Analysis of Trigger Behavior

The individual currents through each SCR were measured to help characterize the trigger behavior of the fingers.

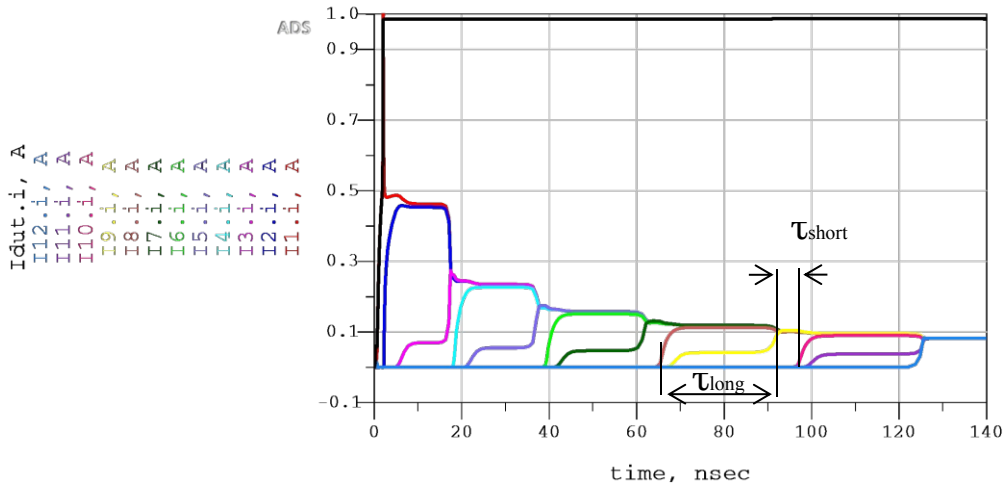


Figure 3.10 The individual currents and the delays τshort and τlong

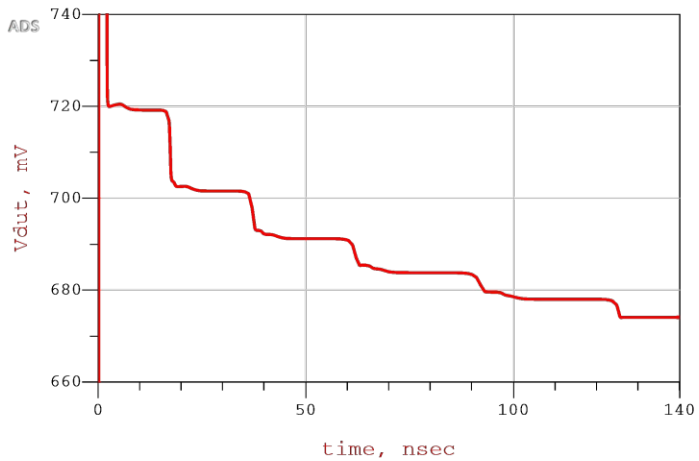


Figure 3.11 The voltage on the device Vdut. Enlarged ignoring the first peak

From figure 3.10 we can identify two triggering delays, namely: the delay of the slow process τ_{long} and the delay of the fast process τ_{short}. To explain the origin of each delay we will take the triggering of SCR9 and SCR10 as an example.

As shown in figure 3.12, after triggering the finger SCR8, the slow process RC transmission line causes a small delay τ_{rc9} until the pulse reaches the base of the npn transistor of SCR9. This delay doesn't depend on the number of the triggered fingers N and it has the same value in each slow process.

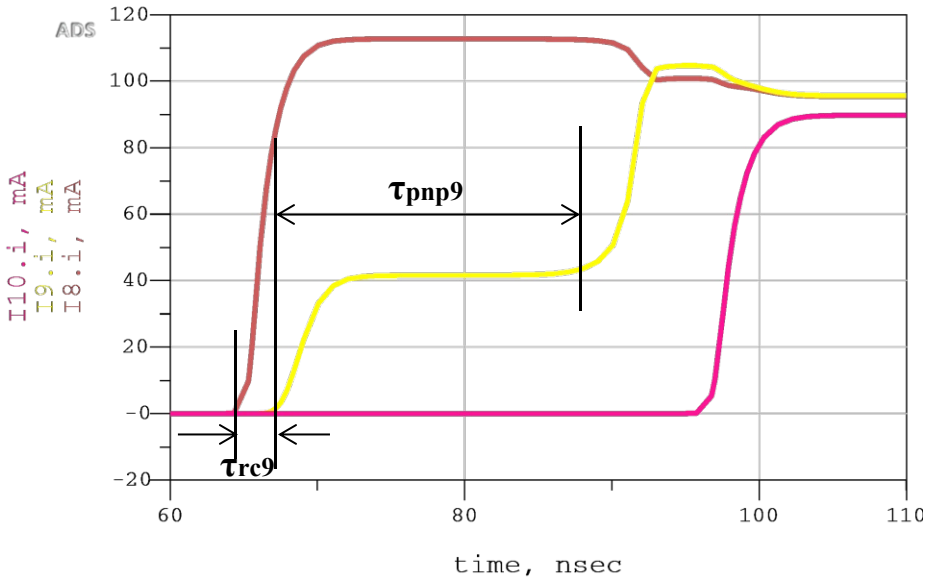


Figure 3.12 The individual currents I8, I9,I10, and the delays τ_{rc9} and τ_{pnp9}

When the pulse Ib9 arrives at the base of the npn transistor, it triggers instantly and a collector current is induced Ic9=β.Ib9=5.Ib9 (see figures 3.13 and 3.14).

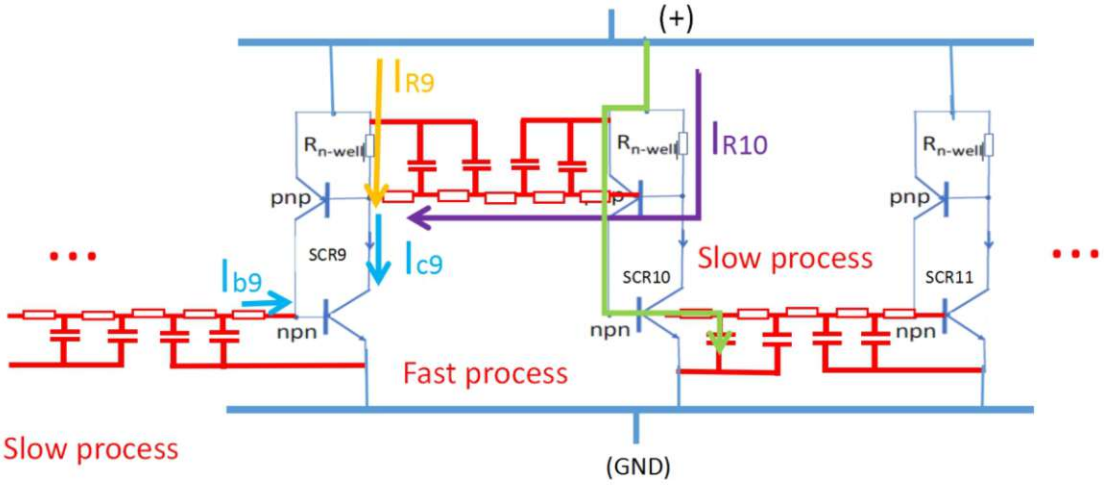


Figure 3.13 Triggering SCR9 and SCR10.

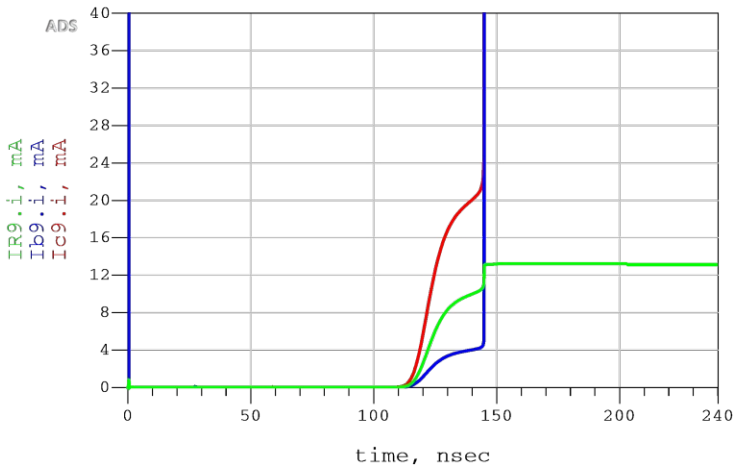


Figure 3.14 The currents Ib9, Ic9 and IR9

Half of the current Ic9 flows from Rnwell9 (IR9 the orange arrow in figure 3.13) and the other half from Rnwell10 through the fast process RC line (IR10 the purple arrow in figure 3.13).

The current I9 in this phase is smaller than the current through any previous finger, as we see in figures 3.10 and 3.12, because the pnp transistor didn't trigger yet and the current is flowing through the resistor Rnwell.

Ic9 increases by increasing Ib9 and so do the currents IR9 and IR10. When IR9 and IR10 became large enough to produce enough voltage on the resistors Rnwell9 and Rnwell10 for the BE junction of the pnp transistor, both pnp transistors of SCR9 and SCR10 trigger at the same time and then we can say that SCR9 triggered properly and the slow process is over.

Let's call the delay from triggering the npn transistor until triggering the pnp transistor **τ_{pnp}.** And we add the number of the SCR afterwards if we want to refer to a certain trigger process e.g. **τ_{pnp9}** (as in figure 3.11)**.**

τ_{pnp} depends on the number of the triggered fingers N and the current through each finger (Idut/N) because the bigger the current through the finger is, the bigger the triggering current Ib in the base of the npn of the next finger is, the bigger Ic through the collector, and therefore the faster the pnp triggers.

When the pnp transistor of SCR10 triggers, the current flows through it and charges the capacitors in the next RC line (the green arrow in figure 3.13) until the voltage V_{BE} of the npn transistor reaches the trigger threshold and the npn transistor triggers. This process causes the short delay τ_{short} and it depends on the current through each finger (Idut/N) as well.

3.5 Trigger Delay Dependencies on Various Parameters

In this section, some parameter changes were made in the model in order to observe the effect of these changes on the triggering delays and explain the effect physically.

We use the same model and the same configuration of part 3.4 and observe the currents when one parameter is changed. After each simulation, the results were exported to a Matlab script that shows both trigger delays τ_{long} and τ_{short}.

3.5.1 The Total Current Idut

To change the current Idut, the voltage of the source was changed. Since the resistance of the source is equal to 50 Ω, by neglecting potential drop on DUT the current Idut can be approximated as $Idut \approx \frac{Vtot}{50}$.

We apply voltage of 25, 50, 100, 150 and 200 V to get Idut of 0.5, 1, 2, 3, and 4 A and observe how the behavior changes accordingly.

Figure 3.15 shows that both trigger delays τ_{long} and τ_{short}, as mentioned in 3.4.2, depend of the current density (Idut/N) and they decrease with increasing Idut (see also figure 3.14).

Increasing the total current leads to increment of the trigger currents (e.g Ib9 in figure 3.11) and therefore the transistors trigger faster and the delays decrease.

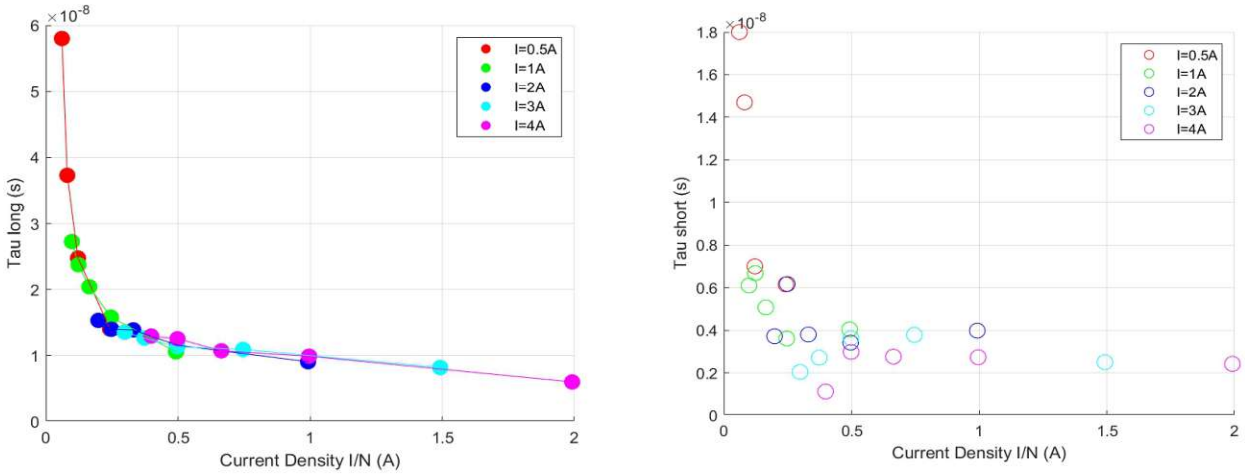


Figure 3.15 Short and long time delays between the triggering fingers as a function of current density when different values of Idut

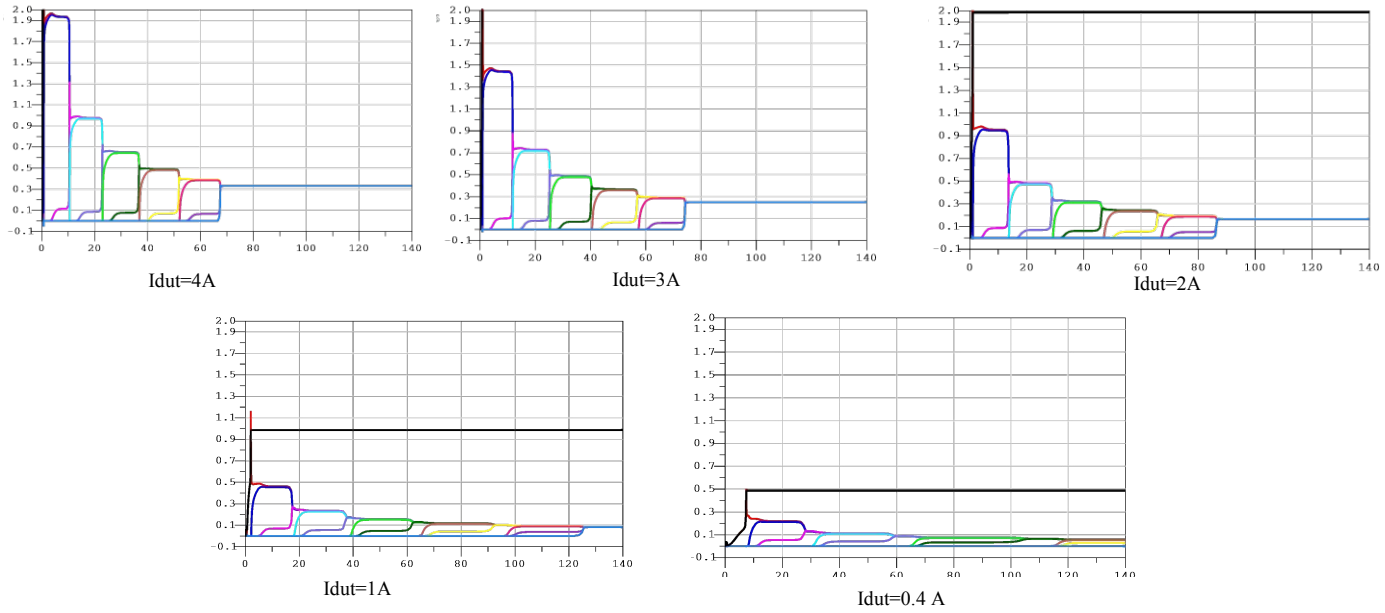


Figure 3.16 The individual currents with values of Idut

3.5.2 The Base Emitter Junction Capacitance Cbe

As mentioned in 2.1.1, the ADS model of the BJT contains capacitances which represent the limitation of the operating speed of the transistor. In this section we will increase the capacitance Cbe, which represents depletion layer capacitance, once for the pnp transistor and once for the npn transistor and observe its effect on the triggering behavior.

This section is about analyzing the effect of a large Cbe. Since Cbe in our model is very small (35 fF) , a large Cbe of 400pF was added separately to each transistor.

3.5.2.1 Adding Cbe to the npn Transistor

Figures 3.17 and 3.18 show that adding Cbe to the npn transistor causes τ_{short} to became considerably larger, and the long delay τ_{long} became a bit larger as well. To explain the reason behind the increment of the delays we will take the triggering of SCR5 and SCR6 as an example.

We mentioned in section 3.4.2 that the long delay τ_{long} consists of two parts: the first part τ_{rc} is the shortest part and it defines the time from the point of triggering the previous finger to the triggering of the npn transistor. The second and the large part τ_{pnp} is the time between triggering the npn and triggering the pnp transistor.

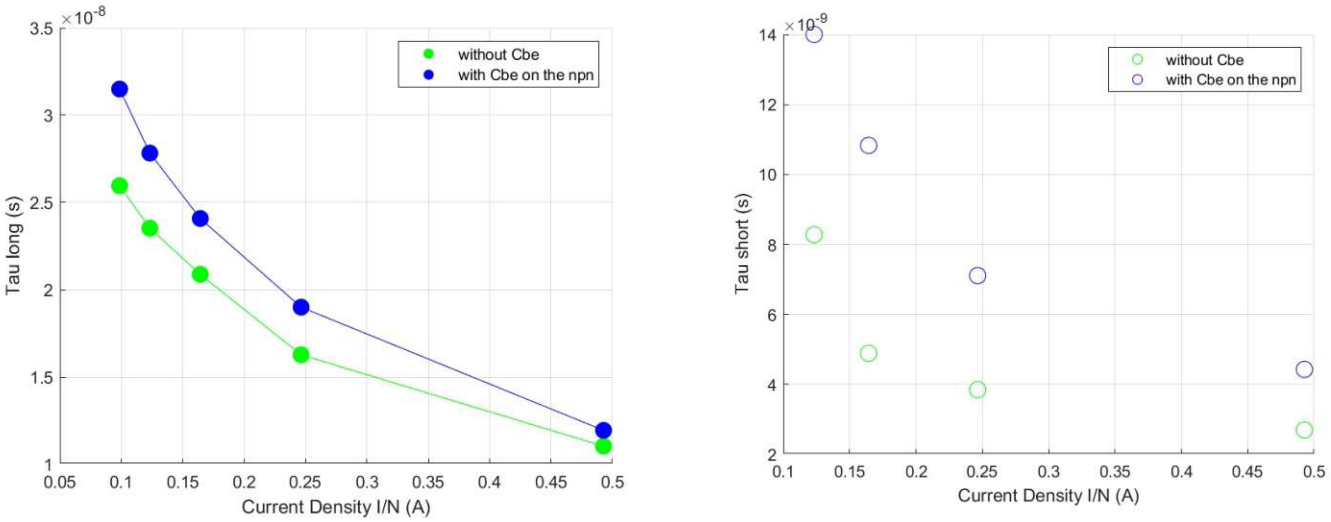


Figure 3.17 Short and long time delays between the triggering fingers as a function of current density with and without Cbe on the npn transistor

The delay τ_{rc} caused by the slow process RC line increases by adding Cbe because the capacitor Cbe is added to the line. Since τ_{rc} is only a small part of the long delay τ_{long}, we notice that the increment is relatively small comparing to the whole delay.

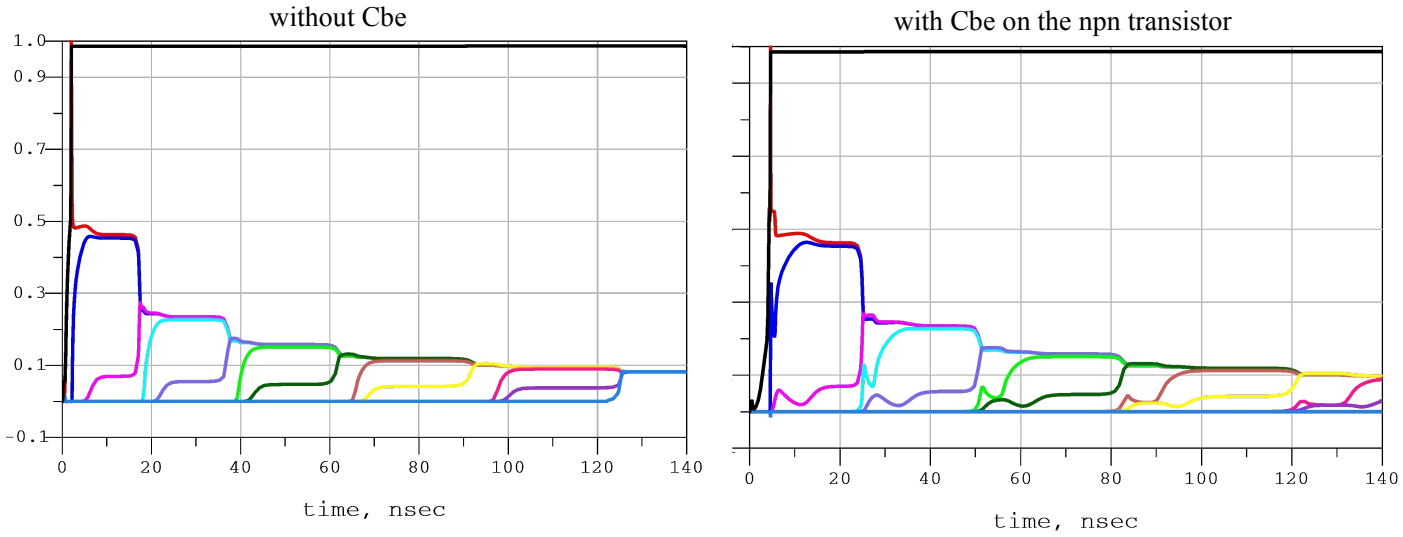


Figure 3.18 The individual currents with and without Cbe on the npn transistor

We notice from figures 3.19 and 3.21 that the current I5 during the delay τ_{rc} is not zero, as the case without Cbe, but it consists of the current through Cbe5.

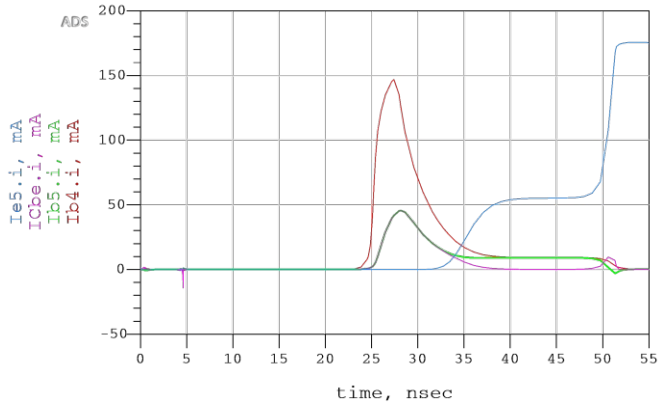


Figure 3.19 The currents Ie5, Icbe, Ib5 and Ib4 with values of Idut with and without Cbe on the npn transistor

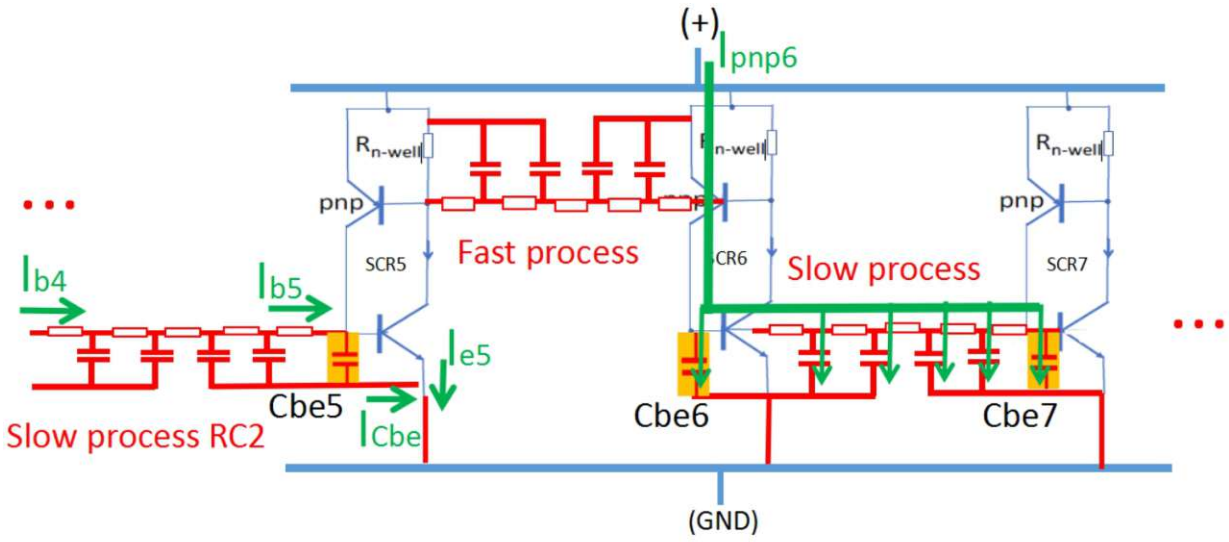


Figure 3.20 Schematic of the fingers 5, 6, and 7 that shows the currents Ipnp6, Ie5, Icbe, Ib5 and Ib4

After triggering the pnp in SCR5 and SCR6, it needs more time to get the npn transistor of SCR6 triggered because the current Ipnp6 needs to charge more capacitors to reach the voltage of the BE junction (see figure 3.20). That's why the short delay τ_{short} increases considerably. We notice also that the current I6 during the delay τ_{short} is not zero because of the leaking current through Cbe6. We also see a rise in the current I7 because of the current through Cbe7.

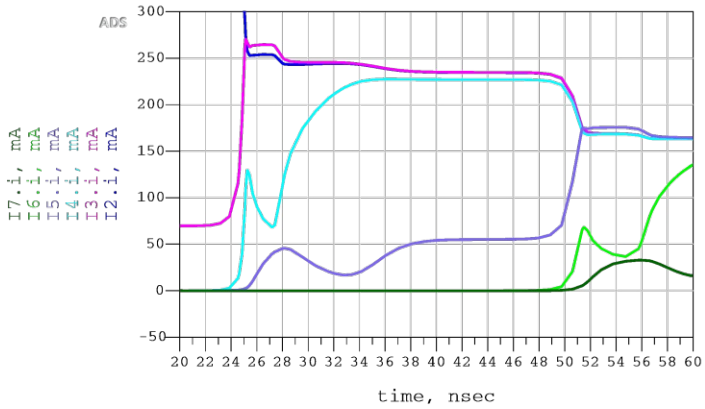


Figure 3.21 The currents I2 to I7 with adding Cbe on the npn transistor

3.5.2.2 Adding Cbe to the pnp Transistor

As shown in figures 3.22 and 3.23, τ_{long} increases by adding Cbe to the pnp transistor but τ_{short} on the other hand doesn't show any noticeable changes.

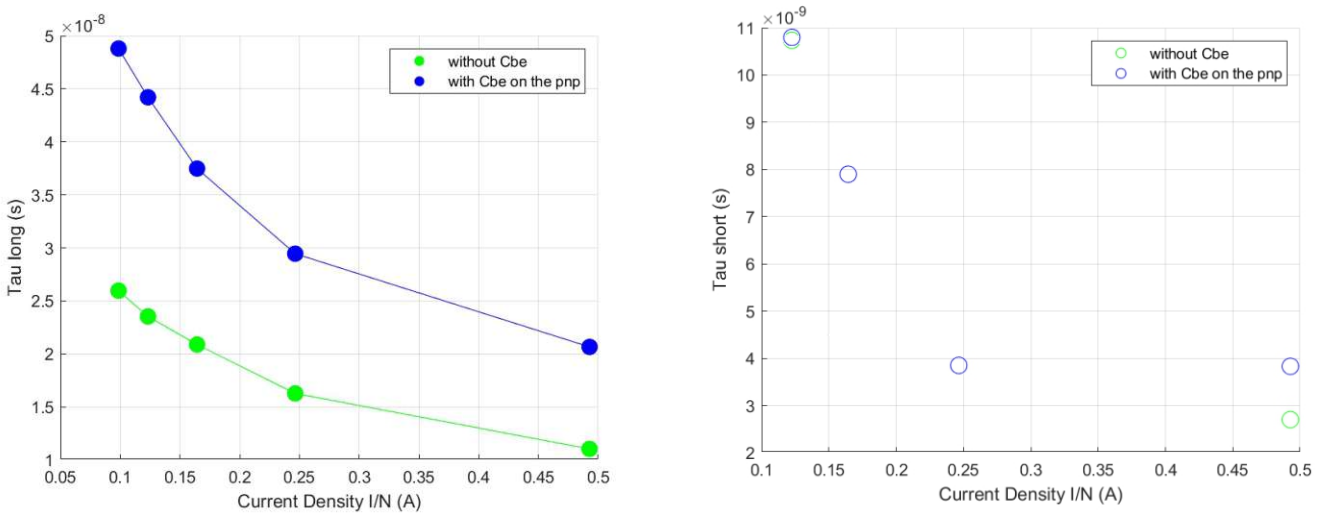


Figure 3.22 Short and long time delays between the triggering fingers as a function of current density with and without Cbe on the pnp transistor

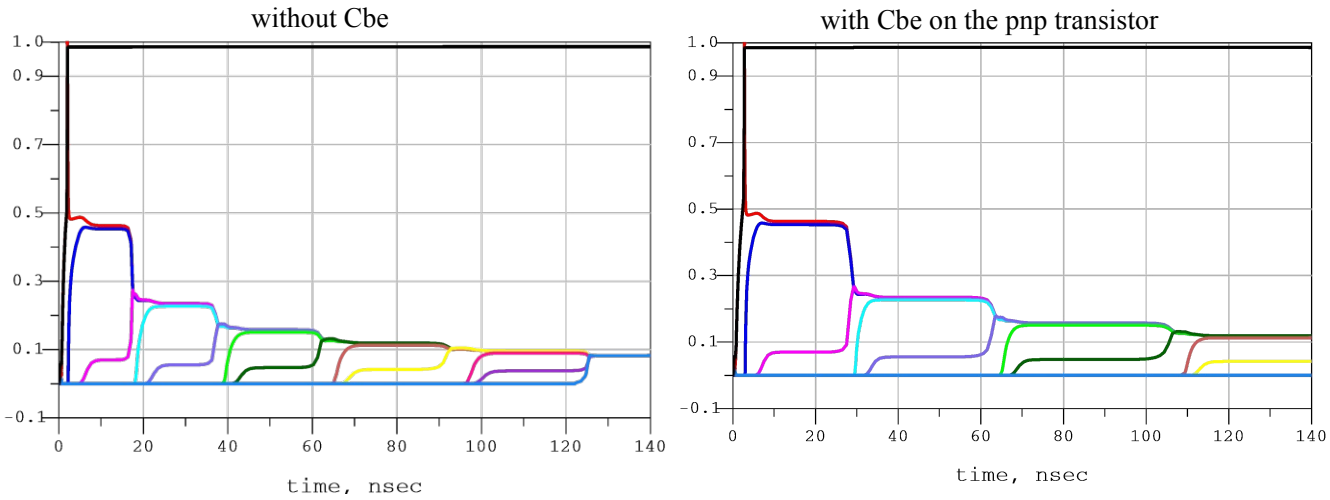


Figure 3.23 The individual currents with and without Cbe on the pnp transistor

The delay τ_{rc} doesn't get affected by adding Cbe to the pnp, only τ_{pnp} does change.

τ_{pnp} increases because part of the current driven to the emitter of the npn transistor comes through Cbe (see figure 3.24). So the current through the resistor Rnwell will decrease and it will need more time to reach the efficient current that makes the voltage on the resistor enough to trigger the pnp transistor.

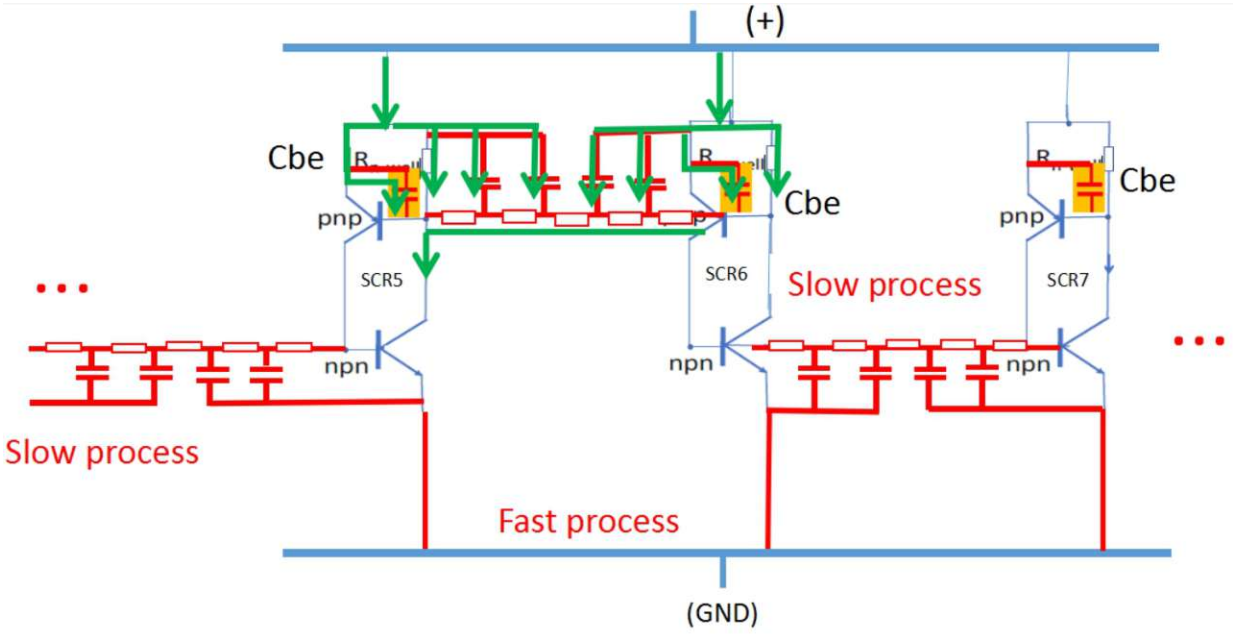


Figure 3.24 Schematic of three fingers that shows where the current of the emitter of the npn transistor comes from in the case when Cbe is added to the pnp.

3.5.3 Effect of Beta

In our model, we have βnpn=βpnp=5 which is a relatively small beta. In this section we will increase the beta, which can be given as $\beta = \frac{Ic}{Ib}$, once for the pnp transistor and once for the npn transistor, and observe its effect on the triggering behavior.

The triggering of SCR5 and SCR6 will be taken as an example to explain the changes in the triggering behavior after increasing each beta.

3.5.3.1 Increasing Beta of the npn Transistor

Increasing βnpn caused a big effect on the delay τ_{long}. Thus, βnpn were increased only from 5 to 10.

We can see from figures 3.25 and 3.26 that τ_{long} became significantly smaller by increasing βnpn but τ_{short}, however, didn't get affected.

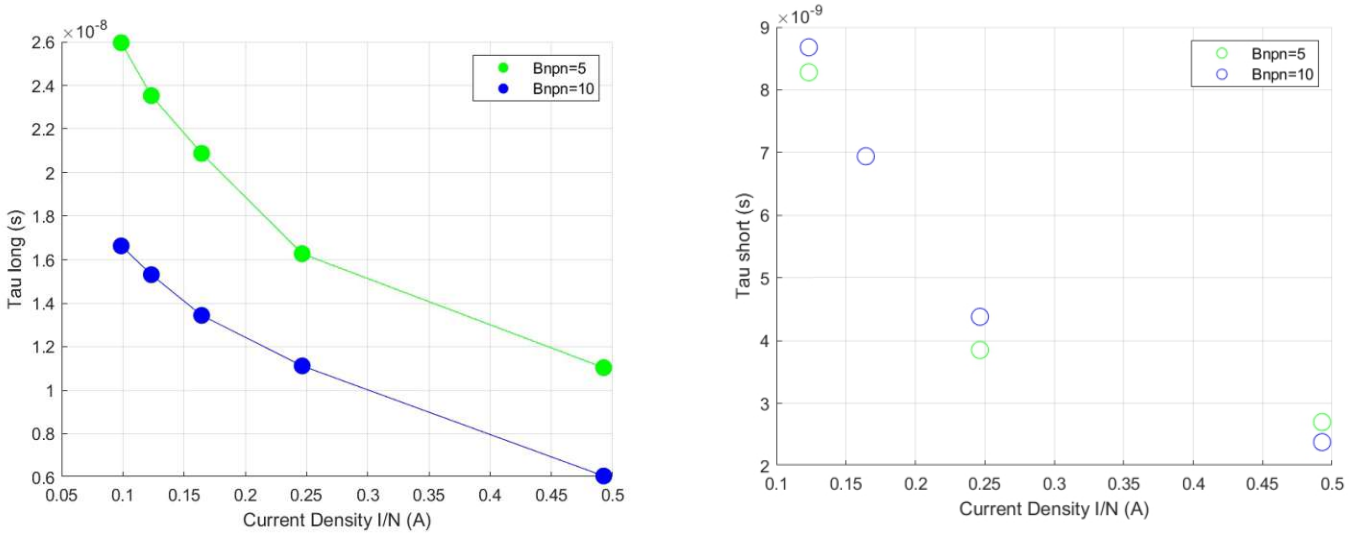


Figure 3.25 Short and long time delays between the triggering fingers as a function of current density for different values of βnpn.

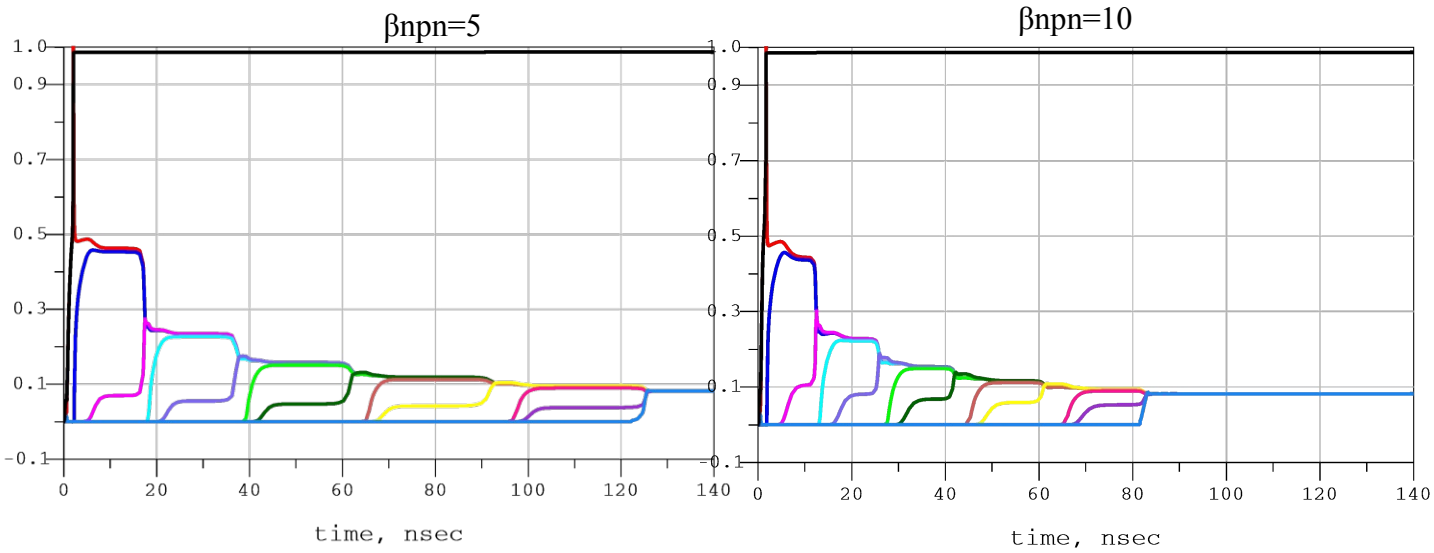


Figure 3.26 The individual currents for different values of βnpn

As shown in figure 3.27, when the signal via bottom RC line reaches the base of the npn transistor (the green arrow in figure 3.27), the current driven to the collector results from Ic=βnpn *Ib. If βnpn increases, Ic5 increases and the voltage on the resistor Rnwell increases, and reaches, therefore, the trigger voltage of the BE junction faster, which entails that τ_{long} becomes shorter.

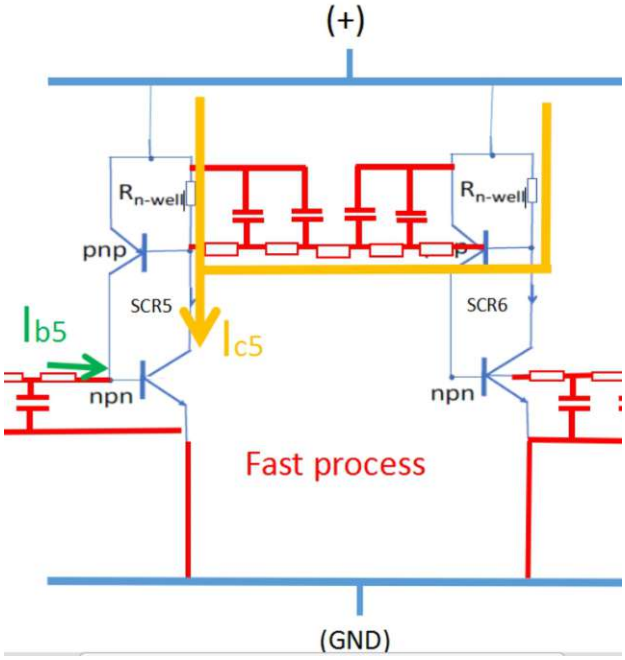


Figure 3.27 Schematic of SCR5 and SCR6 that shows the trigger current Ib5 and the driven collector current Ic5

βnpn=5 βnpn=10

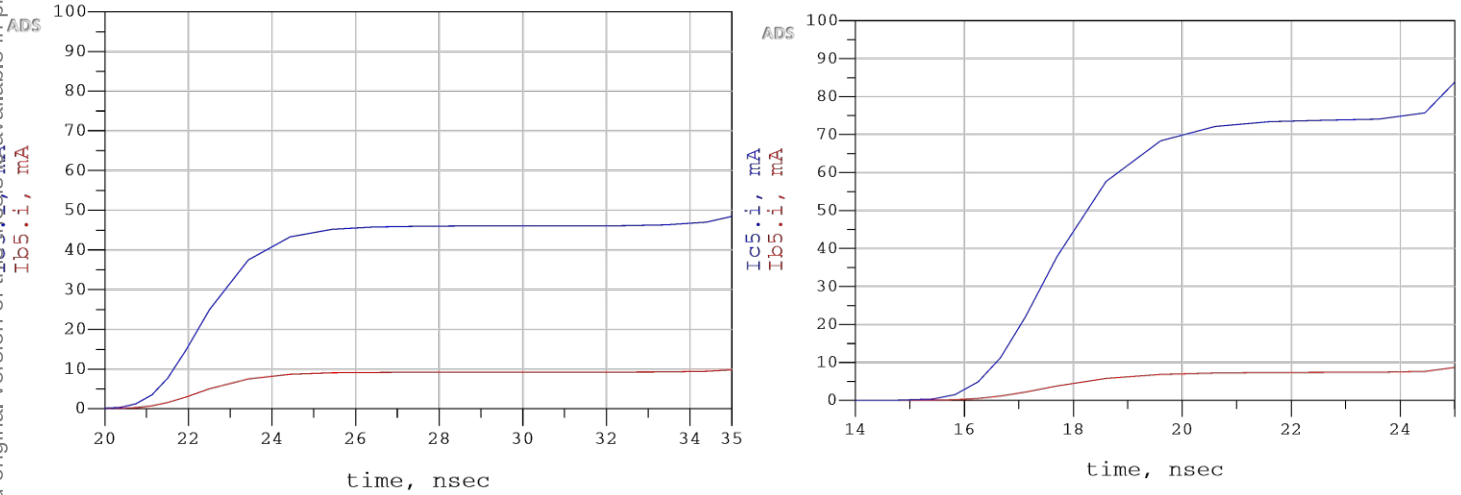


Figure 3.28 Ic5 and Ib6 as a function of time for different values of βnpn

3.5.3.2 Increasing Beta of the pnp Transistor

The effect of increasing beta of the pnp is not as significant as the one caused by increasing beta of the npn transistor. That's why βpnp had to be increased to 100 in order to show the effect.

The short delay τ_{short} gets smaller by increasing βpnp. The long delay τ_{long}, however, doesn't change (see figures 3.29 and 3.30).

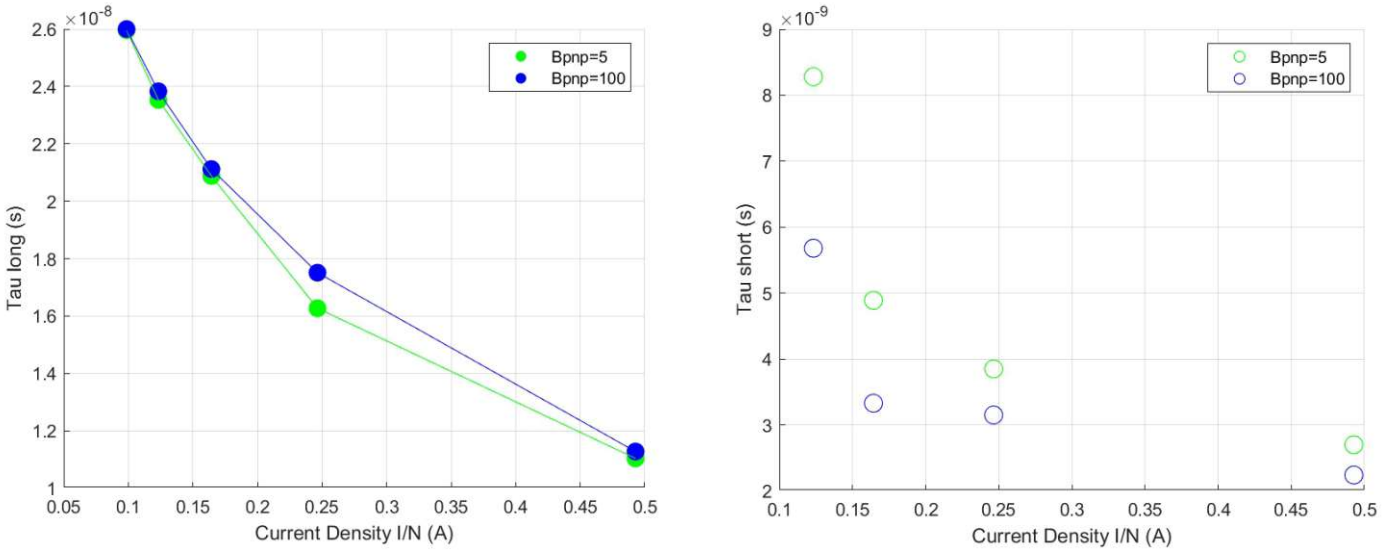


Figure 3.29 Short and long time delays between the triggering fingers as a function of current density for different values of βpnp.

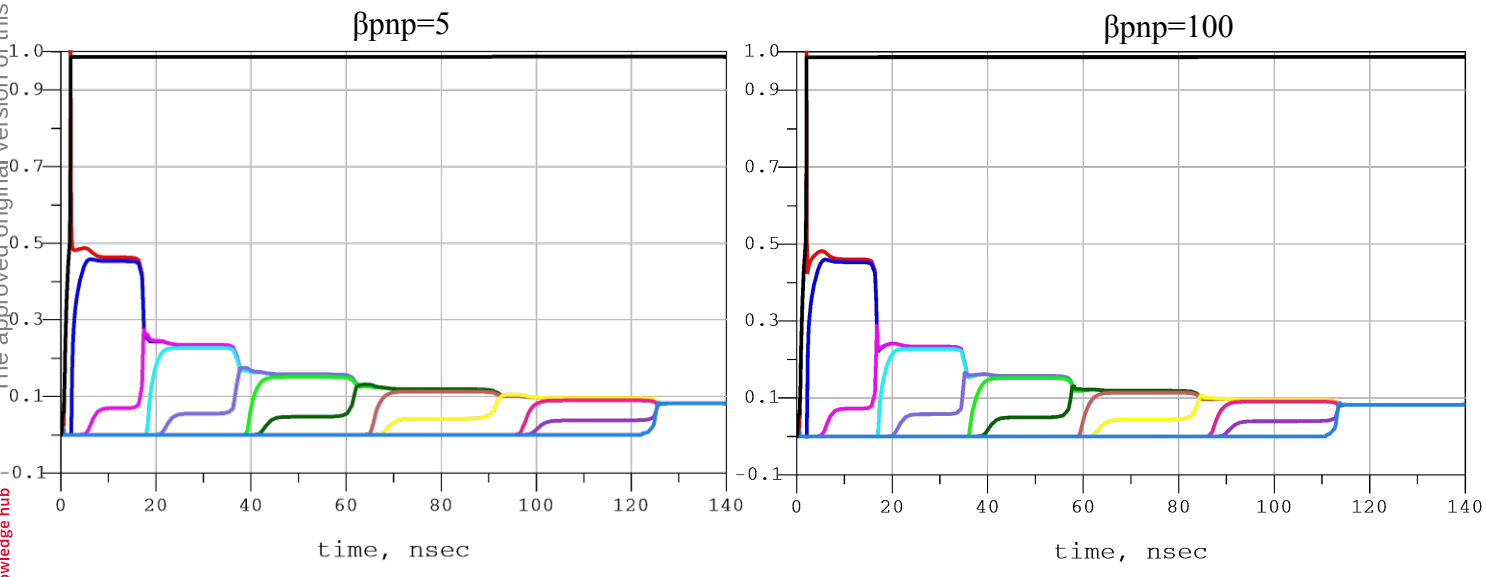


Figure 3.30 The individual currents for different values of βpnp

When it comes to the pnp transistor, α is more essential. So let's speak in terms of alpha.

As in figure 3.29, if βpnp increases, $\alpha = \frac{\beta}{\beta+1}$ increases, and so does Ic= α *Ie, which makes Vbe of the npn transistor increases faster and the transistor triggers therefore faster. Thus τ_{short} becomes smaller.

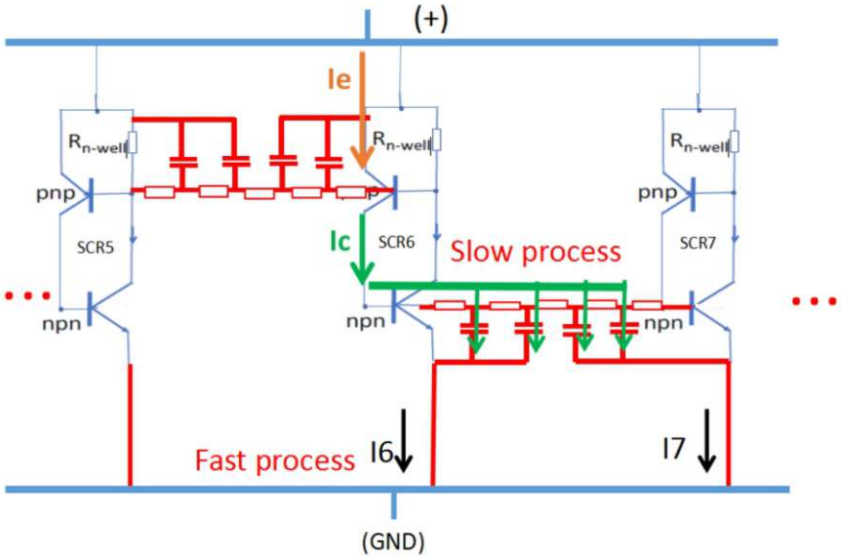


Figure 3.31 Schematic of SCR5, SCR6 and SCR7 that shows Ie and Ic of the finger SCR6 after triggering the pnp transistor.

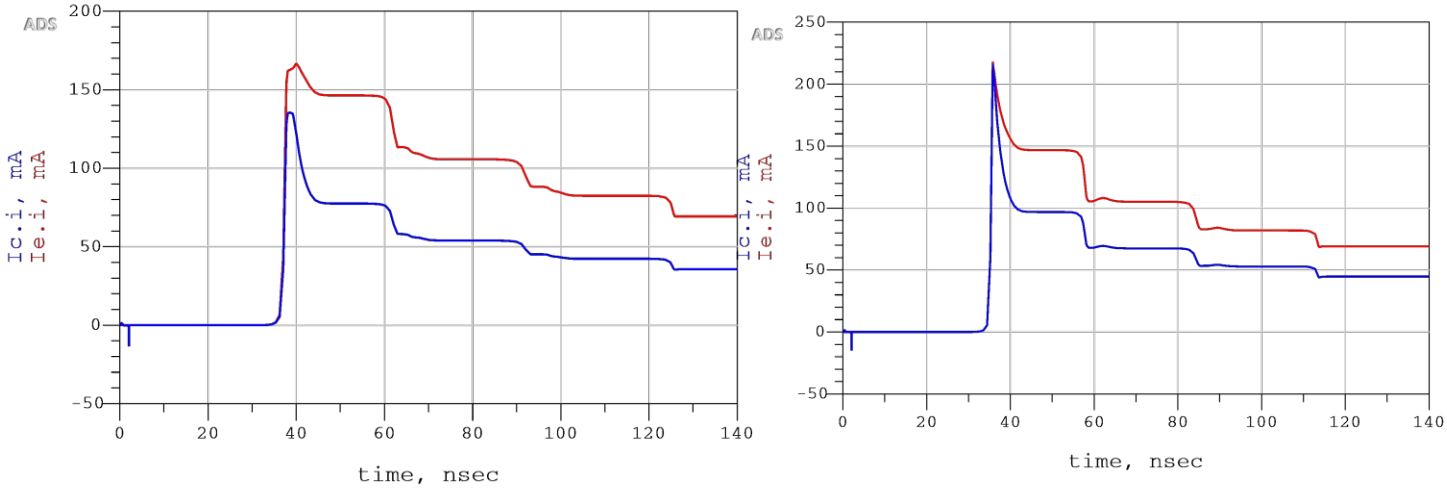


Figure 3.32 Ic and Ie of the pnp transistor of the finger 6 (see also Figure 3.31)

3.5.4 The Metal Resistance

So far the metal resistance has been neglected both before the finger and after the finger. This resistance is considered in this section and it was represented once with Rtop before the finger and once with Rbot after the finger.

3.5.4.1 Rtop

Adding Rtop=3Ω doesn't cause any noticeable change neither in the short delay τ_{short} nor in the long delay τ_{long}. Surely if the resistor added was larger it might increase the delays but since 3Ω was too small comparing to Rnwell=50 Ω no big changes were noticed (see figures 3.33 and 3.34).

Adding Rtop decreases Idut and makes its dependency on the number of triggered fingers (N) clearer. The more fingers trigger the smaller the total resistance of the model is.

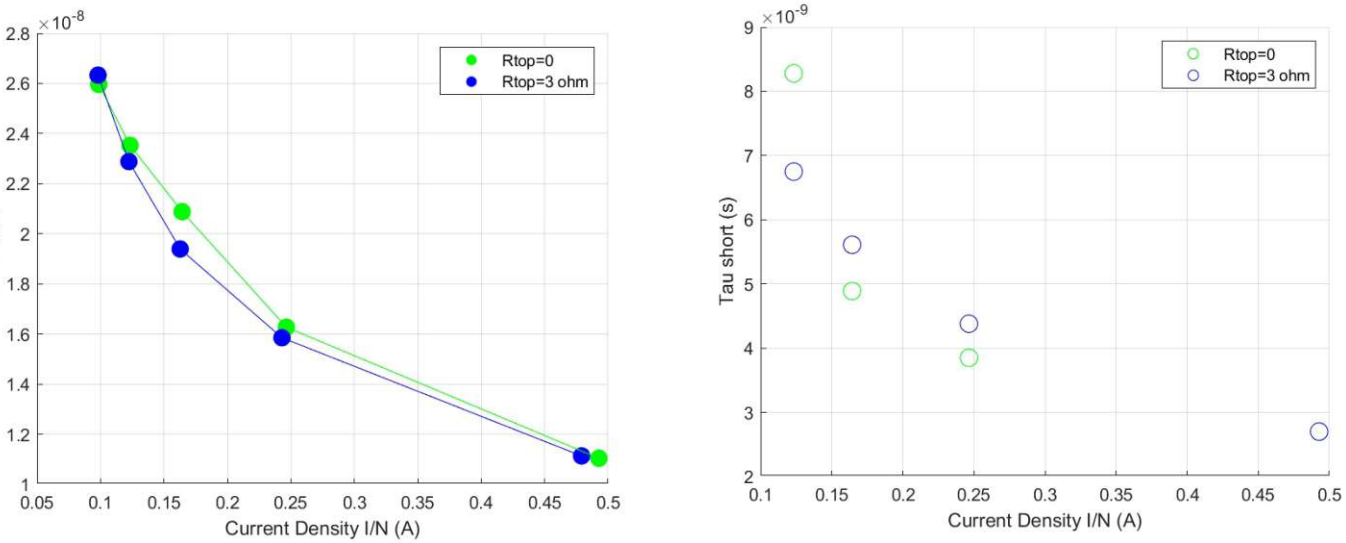


Figure 3.33 Short and long time delays between the triggering fingers as a function of current density with and without Rtop

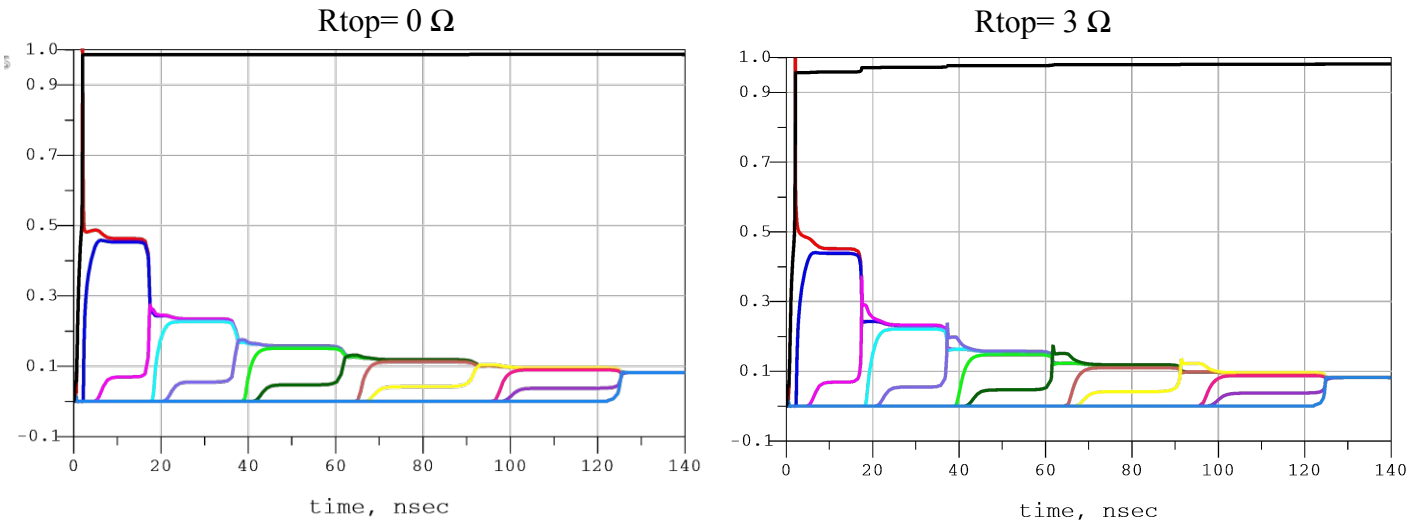


Figure 3.34 The individual currents with and without Rtop

3.5.4.2 Rbot

Adding Rbot affected the long delay τ_{long} so much. Hence, only Rbot = 500 mΩ were added to each finger.

Figures 3.35 and 3.36 show that the long delay τ_{long} gets smaller by adding Rbot= 500 mΩ while the short delay τ_{short} doesn't show any changes. To illustrate this point we will take the triggering of SCR4 and SCR5 as an example with help of the figure 3.37.

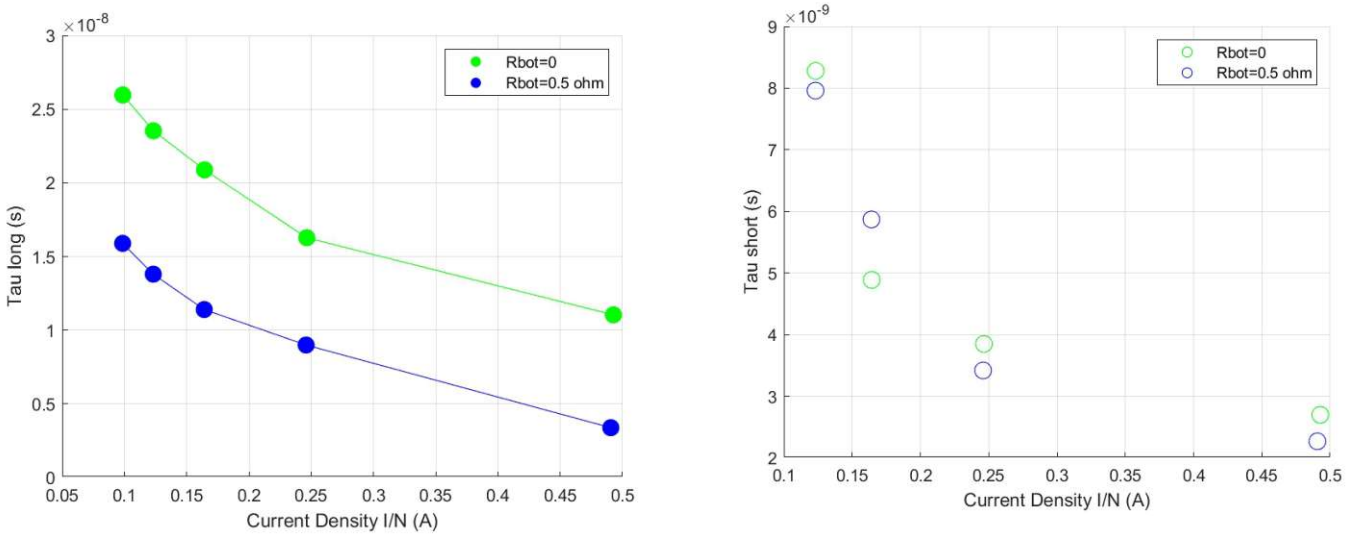


Figure 3.35 Short and long time delays between the triggering fingers as a function of current density with and without Rbot

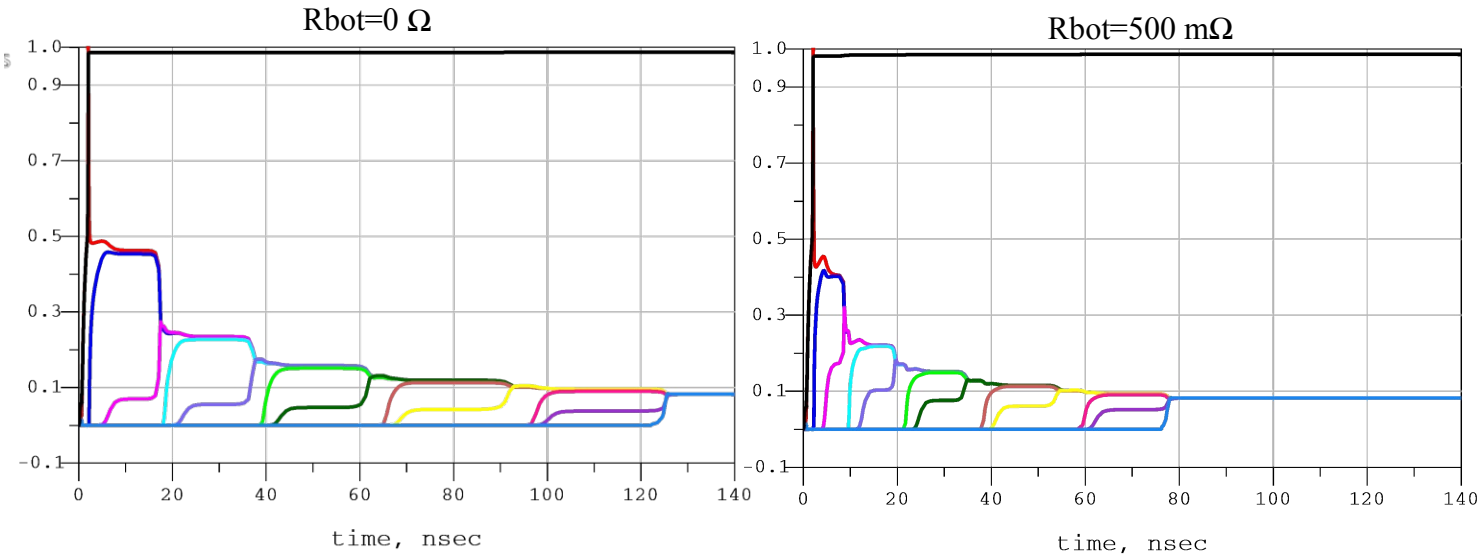


Figure 3.36 The individual currents with and without Rtop

When the npn transistor of SCR4 triggers, the current Icb4 (which flows from the collector of the pnp transistor to the base of the npn transistor and shown in Figure 3.37) splits into two parts(see figure 3.37).

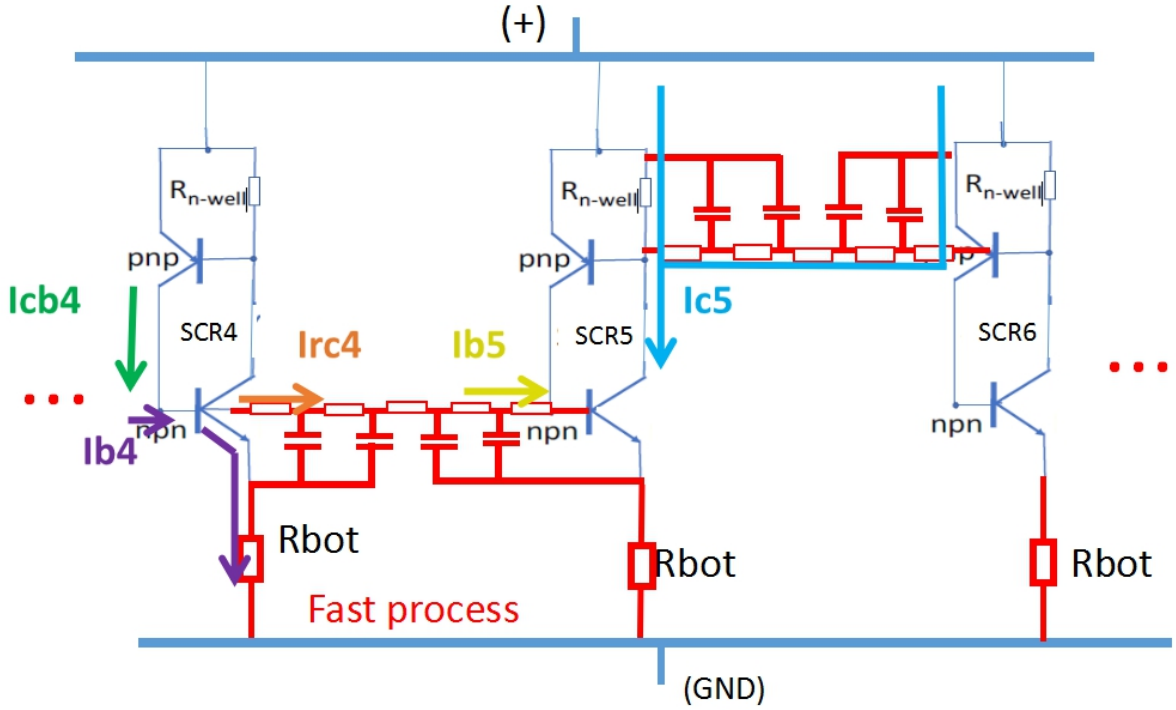


Figure 3.37 Schematic of SCR4, SCR5 and SCR6 that shows Icb4, Ib4, Irc4, Ib5 and Ic5 after triggering the npn transistor of SCR4.

The first part Ib4 flows to the base of the npn transistor, which leads to a current from the emitter Ie4=(β+1)*Ib4 (see the purple arrow in figure 3.37).

The second part Irc4 flows through the RC line to the base of the npn of SCR5.

By adding Rbot, Ib4 decreases and all the currents Irc4, Ib5, Ic5 increase. That makes the pnp of SCR5 and SCR6 trigger faster.

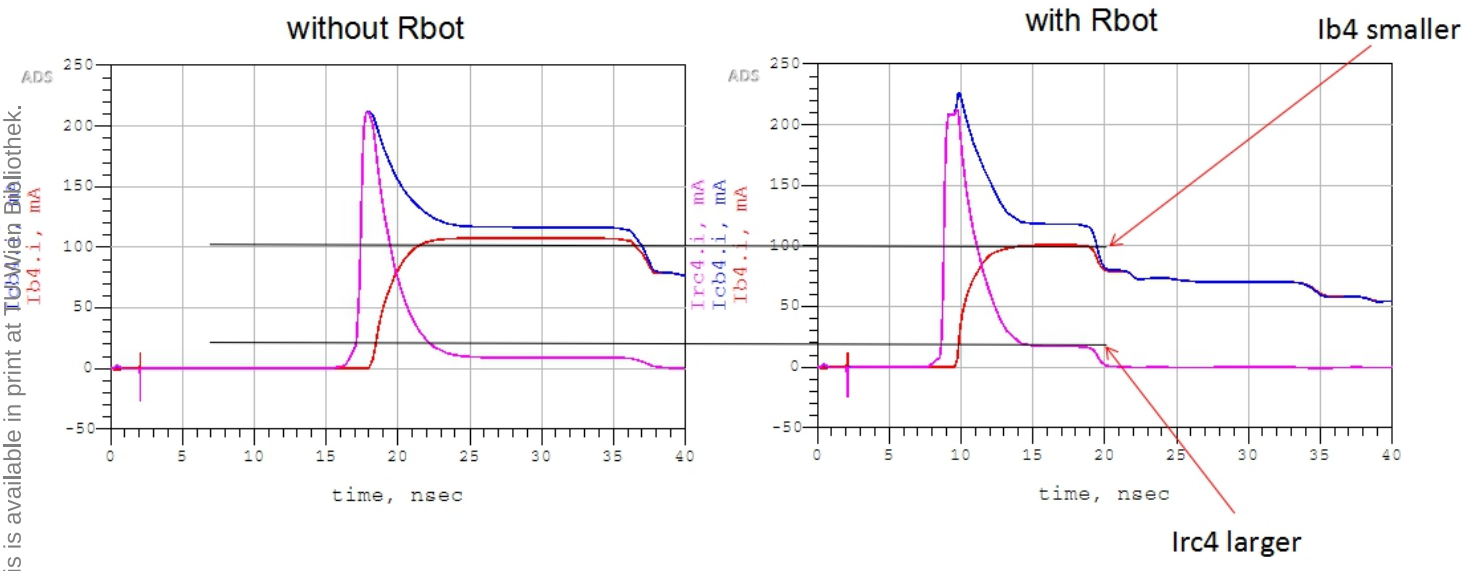


Figure 3.38 Irc4, Icb4 and Ib4(see also Figure 3.37)

3.6 IV Characteristics

In this section, we will get the IV curve in several ways and observe the advantages and disadvantages of each separately.

3.6.1 TLP IV Characterisation

TLP is a very useful tool to characterize ESD protection devices. In this test, a certain voltage pulse Vtot was applied to the device from the source. When the pulse is applied, the total current Idut is measured and averaged over a certain time window and so is the voltage on the device Vdut, and thus a point of the curve is obtained.

By applying different pulses and measuring the currents and voltages in the same time window, the whole I-V curve can be obtained.

A voltage pulse of 25, 50, 100, 150 and 200 V is applied and the results were extracted to a Matlab code that calculates the averages of Idut and Vdut over a time window of 200ns.

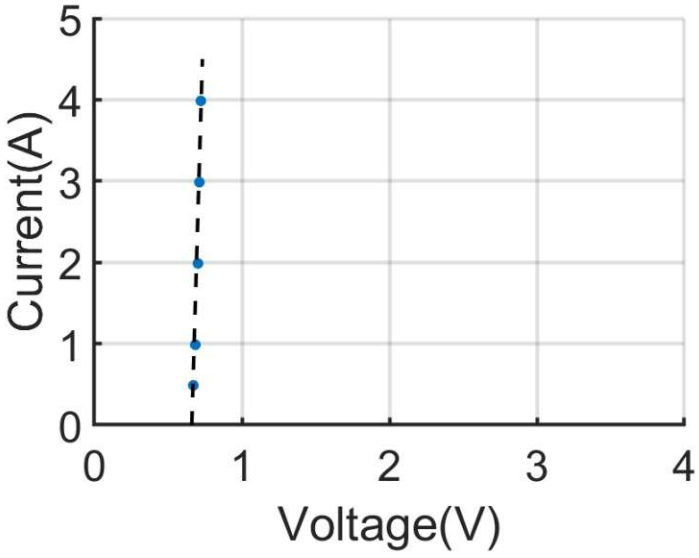


Figure 3.39 200ns TLP IV curve

Figure 3.39 shows the TLP test curve obtained from the Matlab script. This method is very good for showing the after-triggering phase. It is difficult, however, to see the triggering of the individual fingers on this graph or even to see the trigger voltage or the hold current of the device.

3.6.2 DC Sweep

Another way to form the IV curve is by running a dc simulation on the model and plotting the curve either while increasing or while decreasing the voltage source.

The fingers in our model trigger sequentially, which leads to zigzag IV characteristics and that is what we want to show from the DC sweep IV curve.

Figure 3.40 shows that the IV curve by sweeping down differs from the one that results from sweeping up and that the steep of the IV curve depends on the number of the triggered fingers in the device.

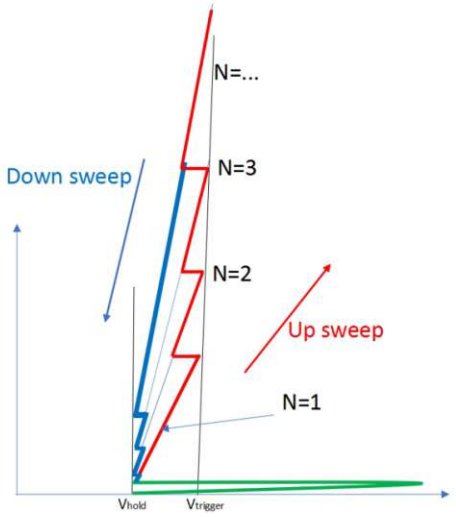


Figure 3.40 IV curve of a multifinger ESD protection device by sweeping up and down

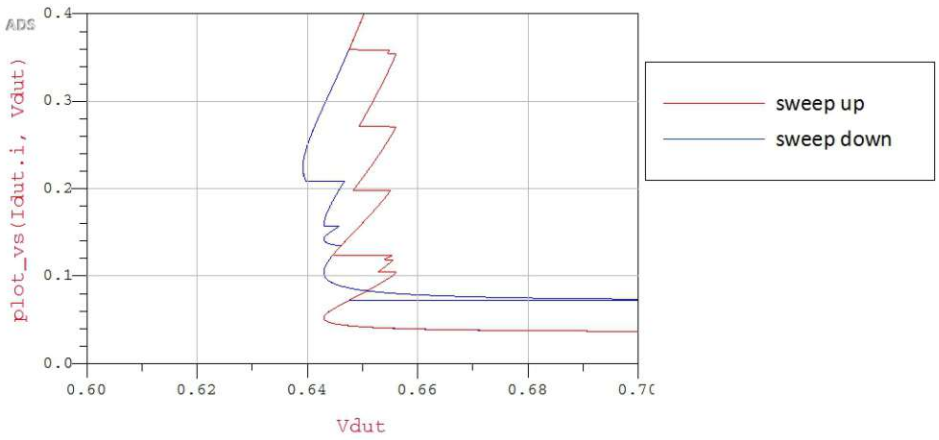


Figure 3.41 DC sweep IV curve

Figure 3.41 is the IV curve obtained from DC sweep. This zigzag curve shows the behavior of the device when each finger triggers as the current rises. The triggering at low trigger voltage is due to coupling between fingers.

3.6.3 IV Curve from each Flat Part of the Voltage Transient

In [1] the IV Data representation for current/voltage values is extracted from each flat part of the voltage transient in between the triggering of finger pairs with common GND. The times of extraction are color-coded and the number of triggered fingers N are indicated by round arrows.

Another Matlab code is used to obtain this IV curve representation for our model an the result is shown in figure 3.42.

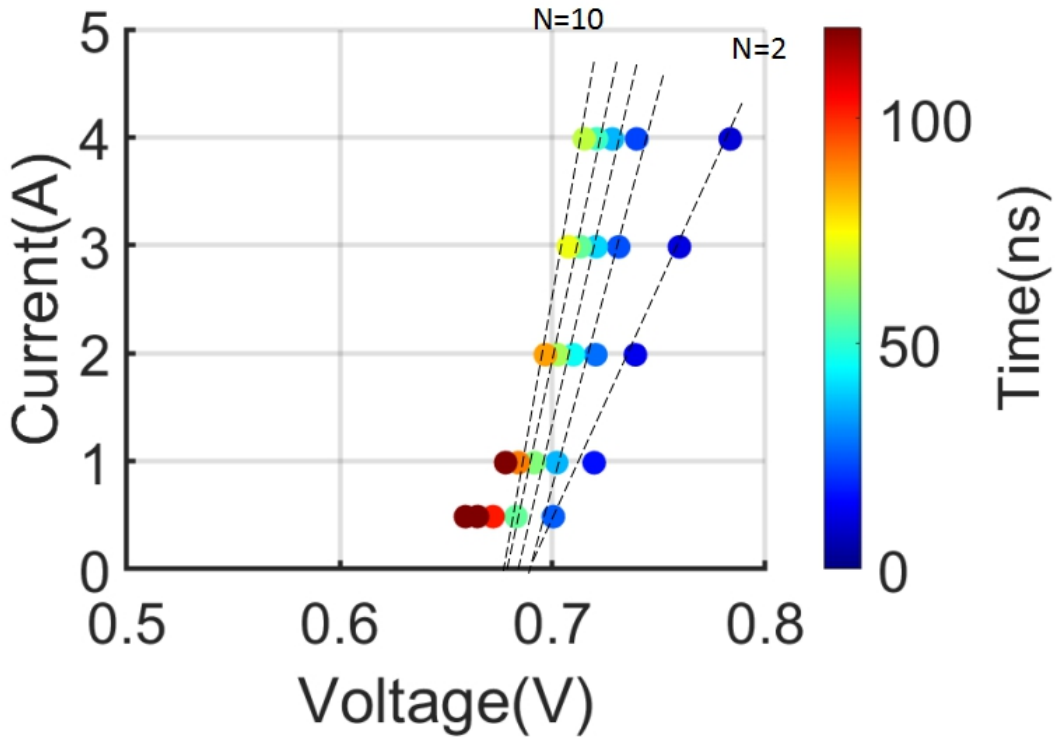


Figure 3.42 IV curve of a multifinger ESD taken from each flat part of the voltage transient

This representation shows the IV curve for different N values very clearly and also the extraction times of the fingers. The values taken from low voltages are not precise that's why we see that some points vary from the IV line.

4 MODELLING SURGE RESPONSE OF AN ASYMMETRIC MULTIFINGER ESD DEVICE

4.1 Model Definition

After modelling the TLP response of the ESD protection device of [1] in chapter 3, in this chapter, we will go beyond that and model another multifinger ESD device.

The modeled ESD device in this chapter, as shown in figure 4.1, consists of 8 fingers. The fingers themselves are modeled in exactly the same way as in chapter 3. The whole model, however, has two essential differences from the one in chapter 3.

Here also we should mention that, figure 4.1 has been provided by D.Pogany, and is used here to explain the model definition and it will be used many other times in the thesis after modifying it to explain different current paths in the devices.

The first difference is the applied voltage pulse, which is a surge pulse in this chapter and not TLP like the previous chapter.

The second one is that the initial finger in this model (the first finger to trigger) is not the first finger of the left side as it was in the previous chapter, but it is in the middle between

other fingers, as illustrated in figure 4.2. It is the fifth finger from the left, which means the **P**osition of **I**nitial **F**inger PIF=5.

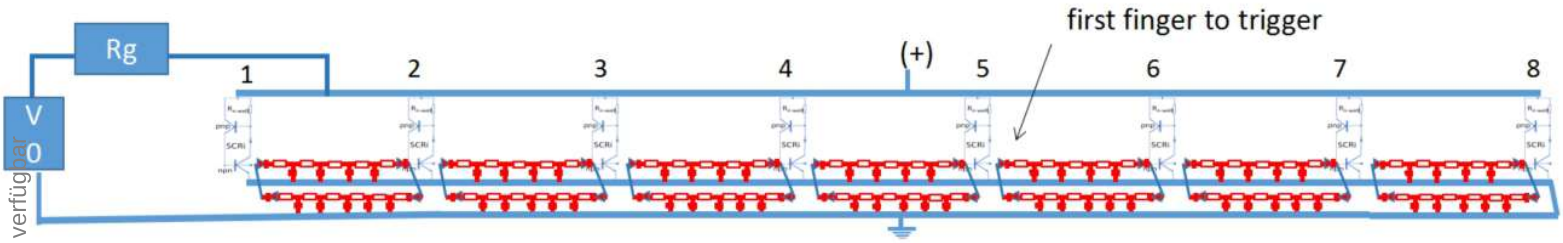


Figure 4.1 Simple schematic of the simulated model . The figure was taken from slides of D.Pogany.

Furthermore, the ESD device is asymmetric, which means that the triggering delay depends on the direction of triggering movement. This is because the device itself is long and there are different diffusion lengths for spreading the base current toward the right and left direction.

This asymmetry will be model by having two RC lines with two different lengths between every two fingers (see figure 4.2). Each RC line models the diffusion in one direction.

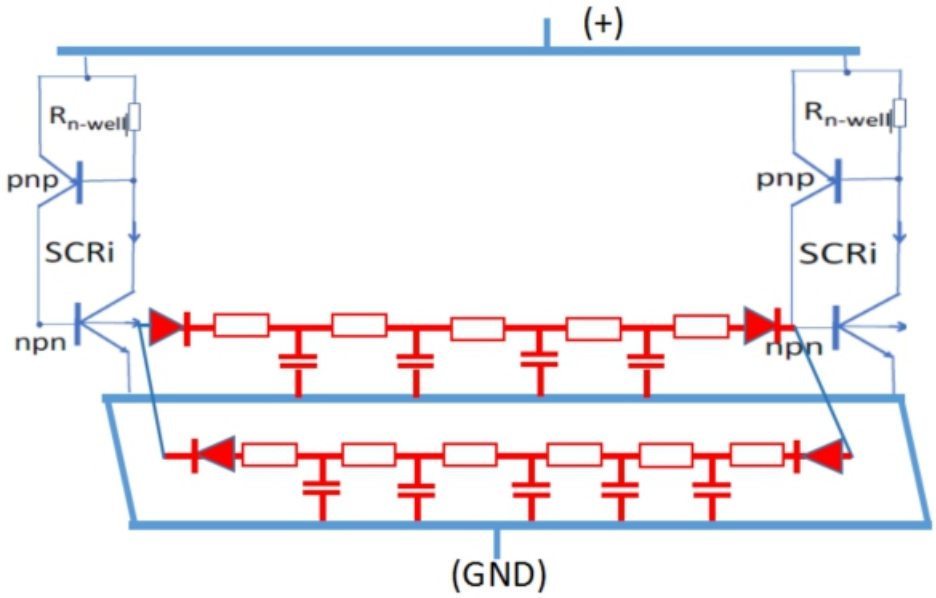


Figure 4.2 Simple schematic of two fingers of the simulated model. The voltage controlled resistor is depicted, for simplicity, by diode symbol.

In order to control the flowing direction and to avoid a current leak in the opposite direction, a voltage controlled resistor is set from both sides of the RC line that changes from 1mΩ to 10kΩ depending on the direction. The voltage controlled resistor was chosen since a diode makes a diode makes a potential drop in forward direction, which is unwanted.

4.2 Model Configuration

The defined model was simulated using ADS. 8 Finger were connected via two sets of RC lines as illustrated in figure 4.2 and supplied by a voltage source (surge generator).

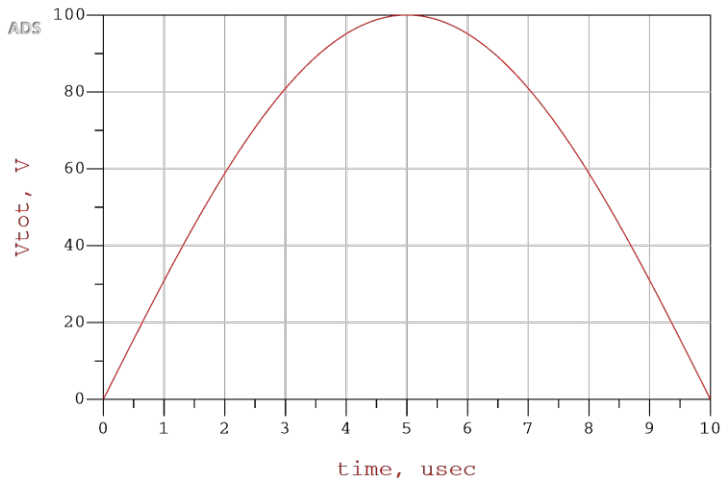


Figure 4.3 The generated surge by the source

Figure 4.3 shows the generated surge, which is half sinusoidal pulse and can be given as:

$$Vtot(t) = 100.\,sin(\frac{2\pi t}{20\ us}) \qquad for \qquad 0 < t < 10us$$

The Source used to generate this surge is a sinusoidal source that is connected to a resistor Rg=10Ω . Its amplitude is set to 100 V, its frequency is set to 50Hz (to get a wavelength of 20us).

The voltage-controlled source of the RC line was implemented using SDD with one port that changes its resistance between 1mΩ and 10kΩ depending on the sign of the voltage.

As shown in Figure 4.2 the left direction line consists of 5 resistors and 4 capacitors,

while the right direction line consists of 6 resistors and 5 capacitors with R= 8mΩ and C=800 pF.

The same calibrated SCR from part 3.2 was used in this simulation with the same parameters.

The metal resistances Rtop and Rbot are also neglected in the beginning of this chapter and they will be added and observed separately later.

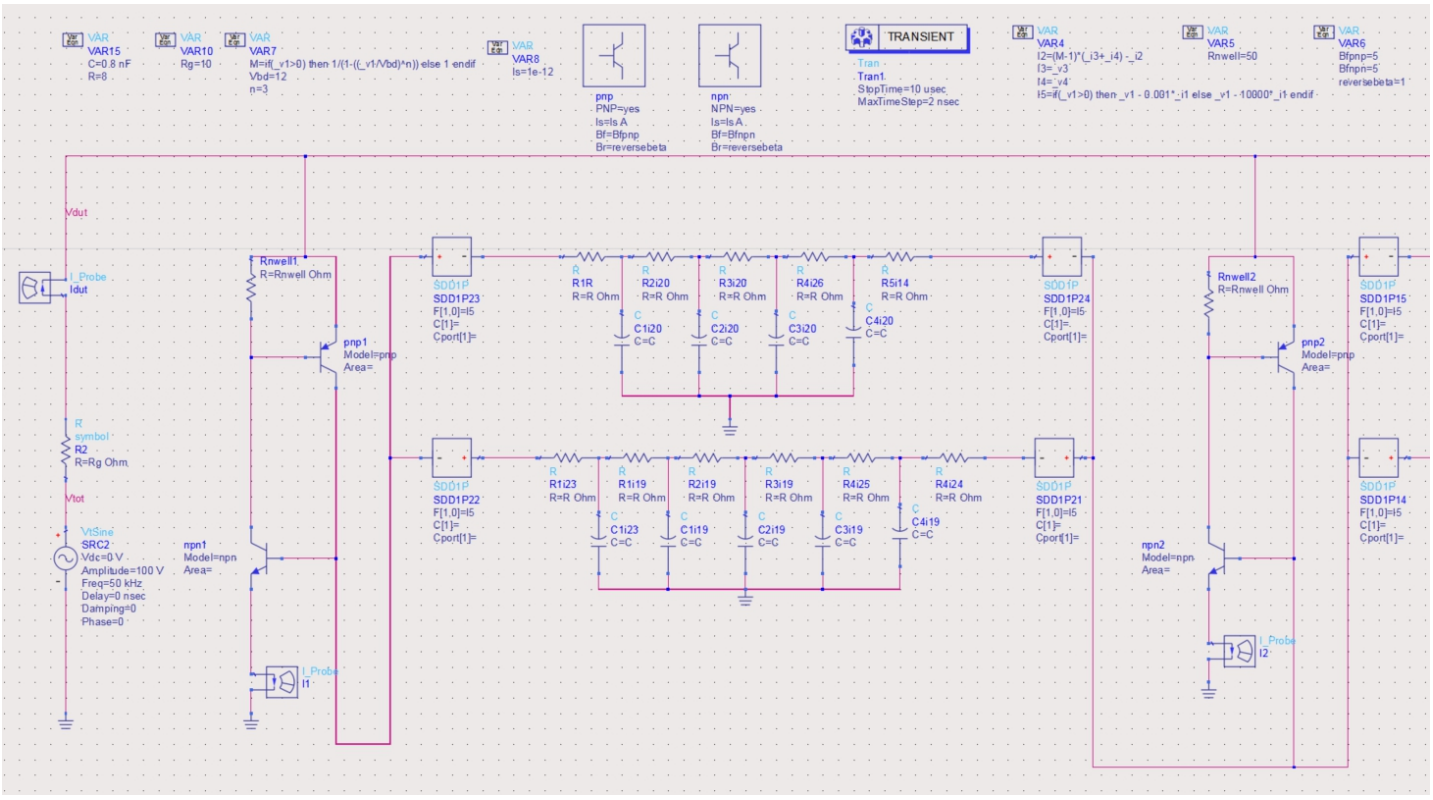


Figure 4.4 ADS schematic of the first 2 fingers of the simulated model

4.3 Simulation Results and Model Behavior

After running the simulation for 10 us, the following results were observed:

4.3.1 Total Voltage and Total Current (Vdut, Idut)

The voltage on the whole device Vdut has the same sinusoidal shape as the source but with drops when each finger trigger (see figure 4.5).

Triggering the first finger causes a huge drop, the second drop is smaller and the third is even smaller, and so on.

As shown in figure 4.6, also the Current Idut has the same sinusoidal shape of the surge and it reaches its maximum of about 10 A when the surge reaches its maximum (100 V).

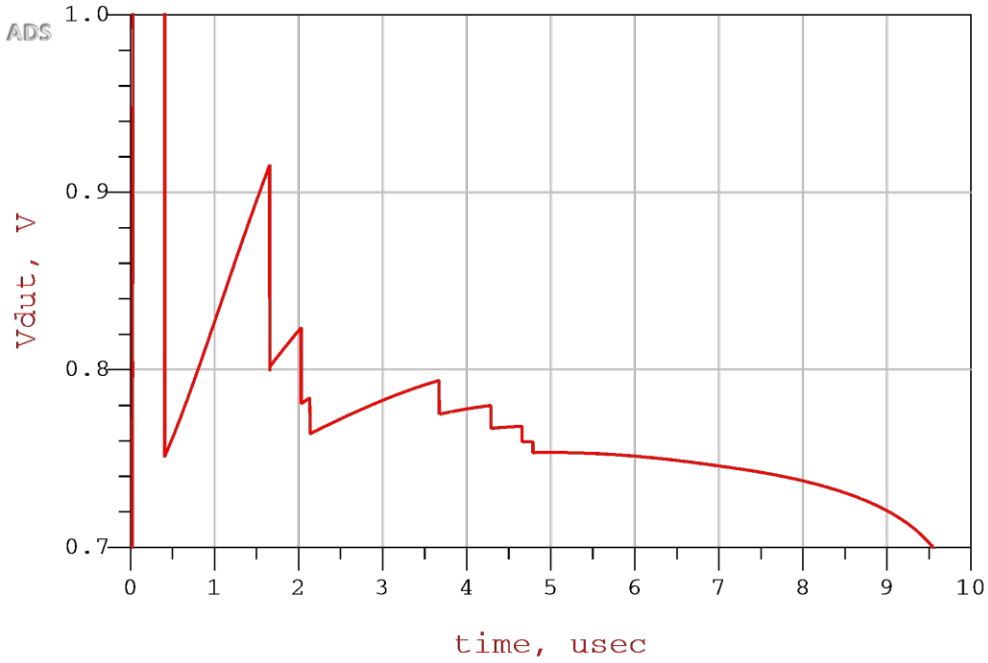


Figure 4.5 Total voltage on the device Vdut (enlarged)

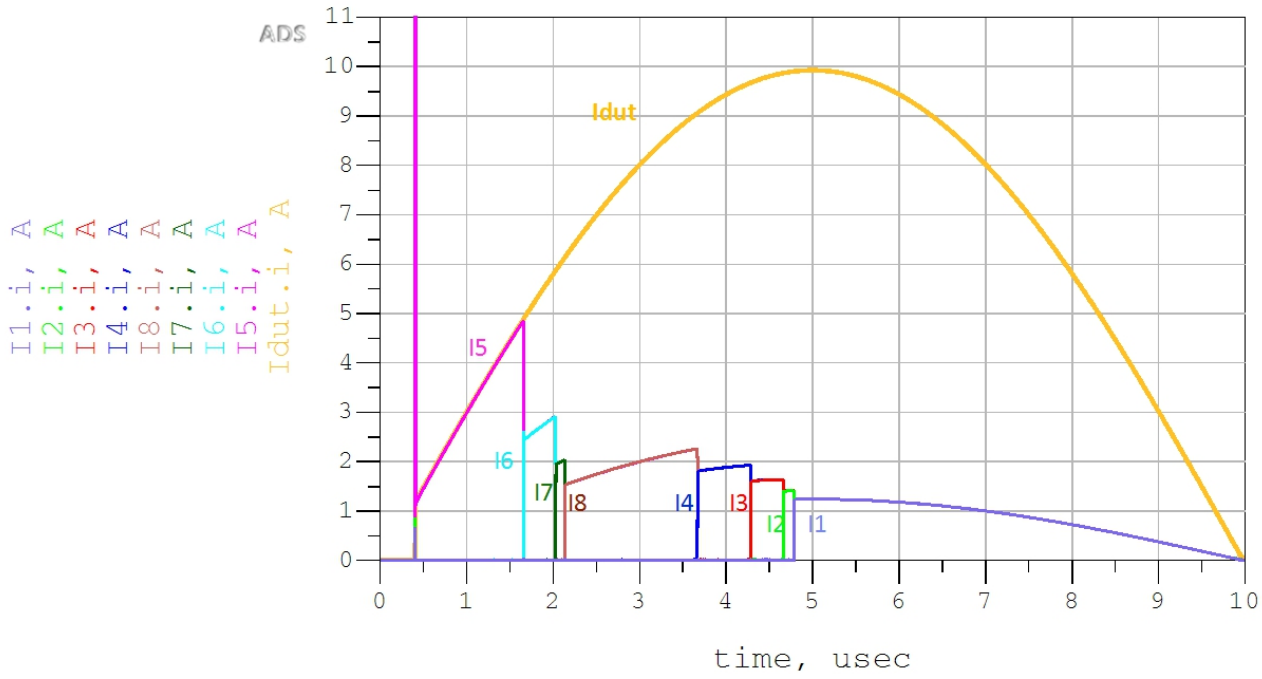


Figure 4.6 The total current and the individual currents

4.3.2 Analysis of Trigger Behavior

To characterize the trigger behavior of the fingers the individual currents through each finger were measured (Figure 4.6).

As mentioned in 4.1, PIF was set to 5 which means that the fifth finger is the first finger to trigger. The other fingers though, as shown in figure 4.6, trigger in this sequence : (5 -> 6 -> 7 -> 8 -> 4 -> 3 -> 2 -> 1).

From this sequence, it's easy to notice that the fingers on the right hand side trigger before the ones on the left hand side. That makes complete sense since the RC lines in the left direction are longer (see figure 4.2) which makes the delay for moving to the left side larger ($\tau_{Left} > \tau_{Right}$).

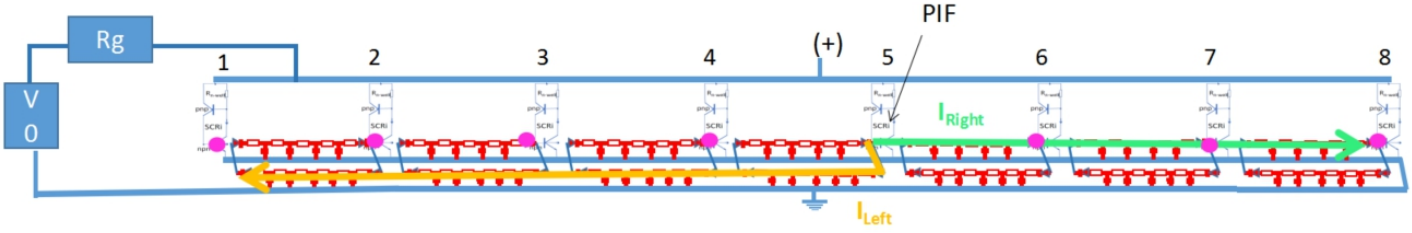


Figure 4.7 Schematic of the model that shows the currents after triggering of SCR5

Another reason that makes the fingers on the right hand side trigger faster is that the number of the fingers on the right side is smaller.

When the initial finger SCR5 triggers, the current flows from its base to both directions(I_{Left} and I_{Right} in Figure 4.7). I_{Right} is a bit larger (as shown in figure 4.8) because the resistance seen from SCR5 to the right side is smaller than the one to the left side.

The orange and the green arrow in figure 4.7 represent the current paths of I_{Left} and I_{Right}, where the current along the line can gradually change.

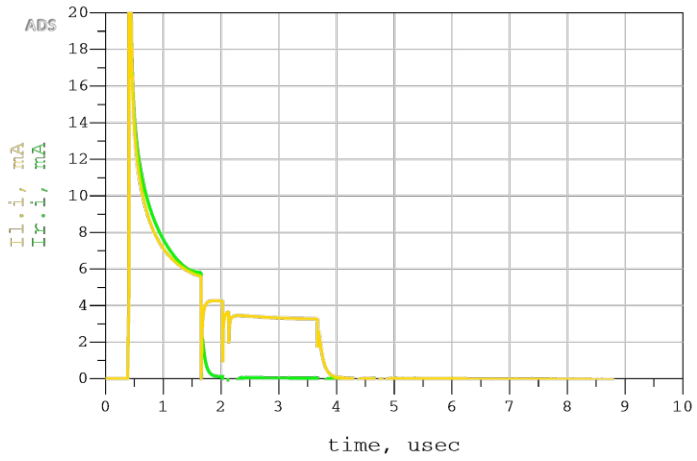


Figure 4.8 I_{Left} and I_{Right} (Il and Ir)

These currents increase the potential of the bases of all the npn transistors (the pink points in figure 4.7), which increases the voltage Vbe of all of them (see figure 4.9) especially SCR4 and SCR6 which are the closest to the source (SCR5).

When Vbe of the npn transistor of SCR6 reaches the BE junction voltage (0.6 V), SCR6 triggers and a larger current flows from it to the right side instead of I_{Right} which was flowing from SCR5. The fingers 7 and 8 trigger successively in the same way and so for the fingers 4,3,2 and 1.

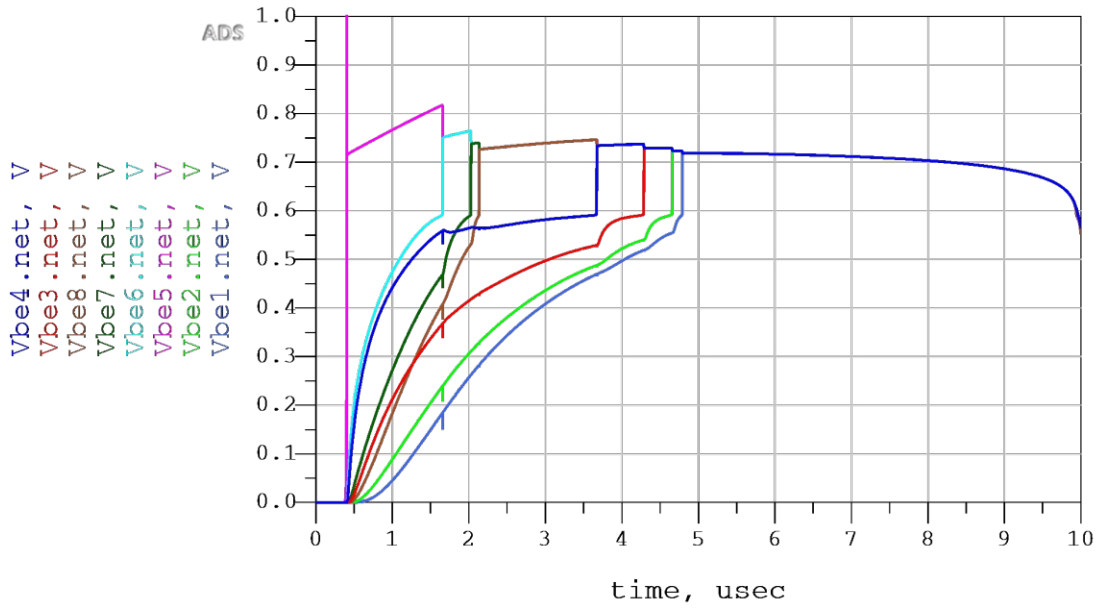


Figure 4.9 Vbe of the npn transistor of all the fingers

4.4 Trigger Behavior Dependencies on Various Parameters

Just like in the previous chapter some parameter changes were made in this section to observe the effect of these changes on the triggering behavior and explain the effect physically.

As an initial point, the same configuration of 4.2 was used and the currents were observed when only one parameter is changed.

4.4.1 The Total Voltage Vtot

In this section, the amplitude of the source voltage was increased from 100V to 200V to observe the effect of the increment on the delays.

As expected, the delays became shorter by increasing the source voltage (see figure 4.10).

Increasing Vtot causes Idut to increase, which in turn leads to increment of the trigger currents and therefore the transistors trigger faster and the delays diminish.

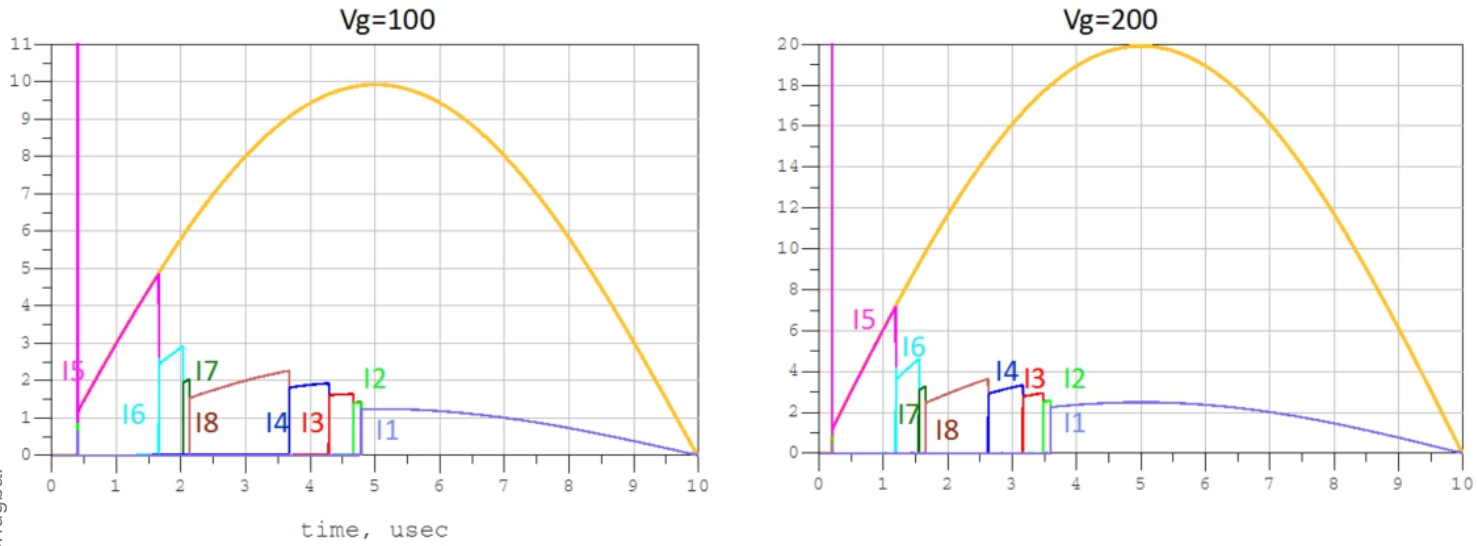


Figure 4.10 The individual currents before and after increasing the voltage

4.4.2 Beta

As mentioned before we use in our model βnpn=βpnp=5. In this section, β will be increased from 5 to 100, which means that α will be increased from 0.83 to 0.99, once for the pnp transistor and once for the npn transistor and its effect on the triggering behavior will be observed.

4.4.2.1 Increasing Beta of the npn Transistor

Increasing βnpn caused a notable effect on the delays. We can see from figure 4.11 that the delays decrease significantly by increasing βnpn. We can also notice that the fingers near the initial finger got affected more than the other fingers.

Figure 4.12 shows the currents in the node next to the base of the npn transistor to explain the role of βnpn with the triggering behavior. After increasing βnpn, a smaller current Ib flows into the base of the transistor, and a larger trigger current "It" flows towards the other fingers, which mainly causes the delay reduction.

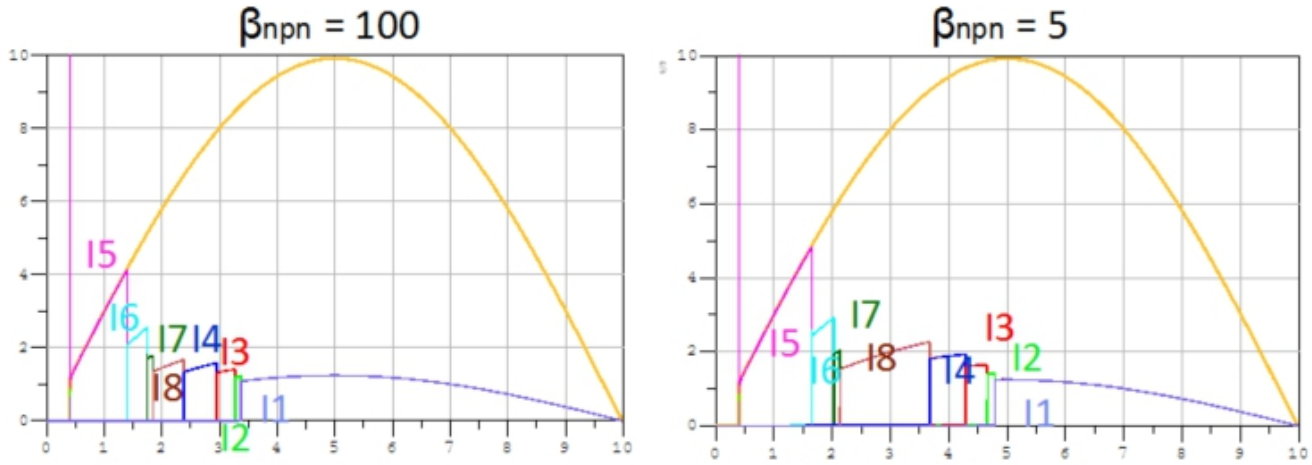


Figure 4.11 The individual currents before and after increasing βnpn

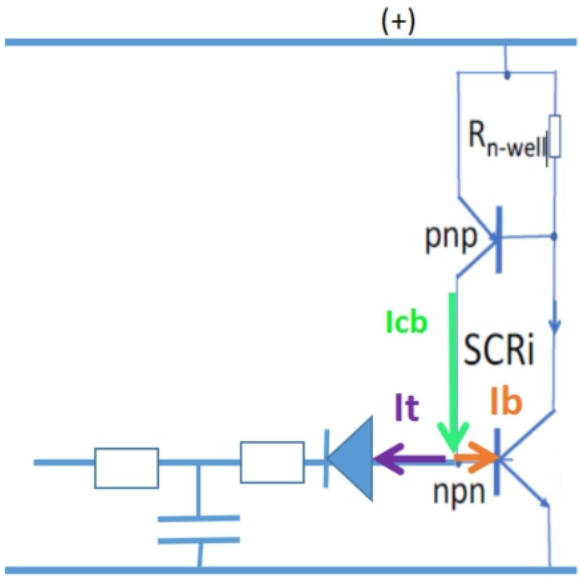


Figure 4.12 The currents It, Ib and Icb after triggering

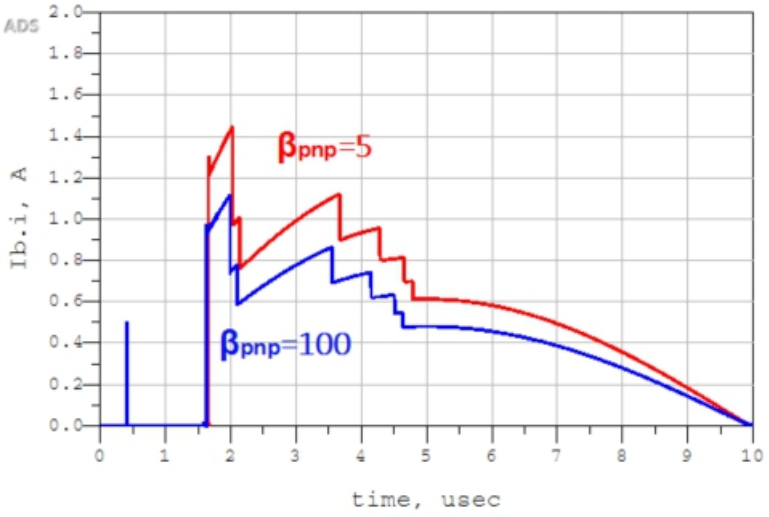


Figure 4.13 The current Ib before and after increasing beta. Taken from SCR6

4.4.2.2 Increasing Beta of the pnp Transistor

Increasing βpnp causes a slight decrease in the delays, as we can see in figure 4.14.

However, the consequence of increasing beta of the pnp is not as notable as the one caused by increasing beta of the npn transistor.

To understand the effect of βpnp, the main currents of the pnp transistor, which are shown in figure 4 .15, are important.

With Ie is constant, increasing βpnp= Ic/Ib will cause Ib to decrease and Ic to increase (as shown in figure 4.16).

Since the collector of the pnp transistor is connected to the RC lines, an increase in Ic leads to an increase in the trigger current, which makes the delays a little smaller.

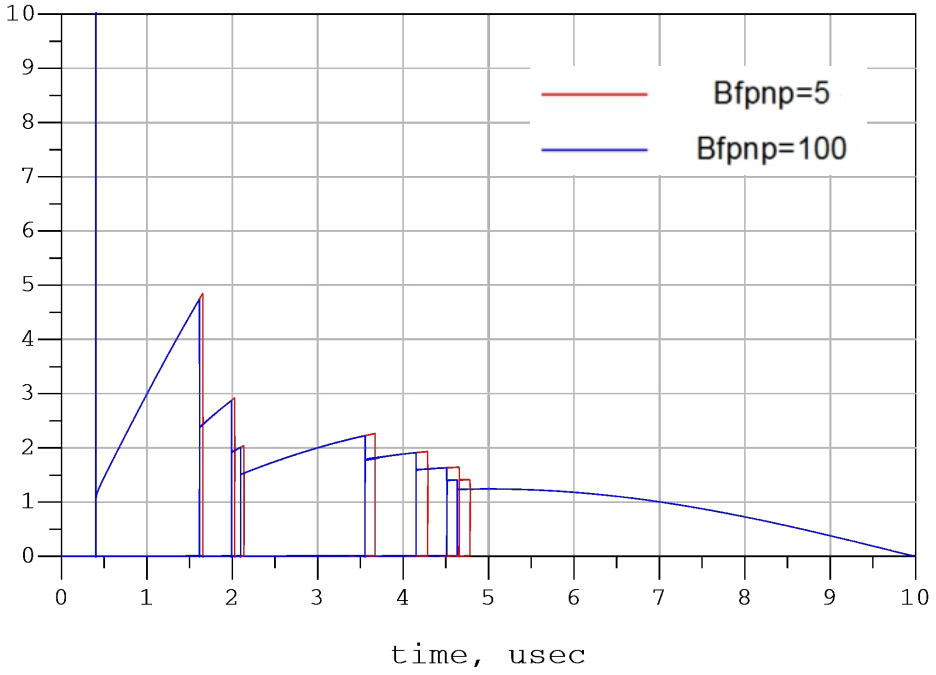


Figure 4.14 The individual currents before and after increasing βpnp

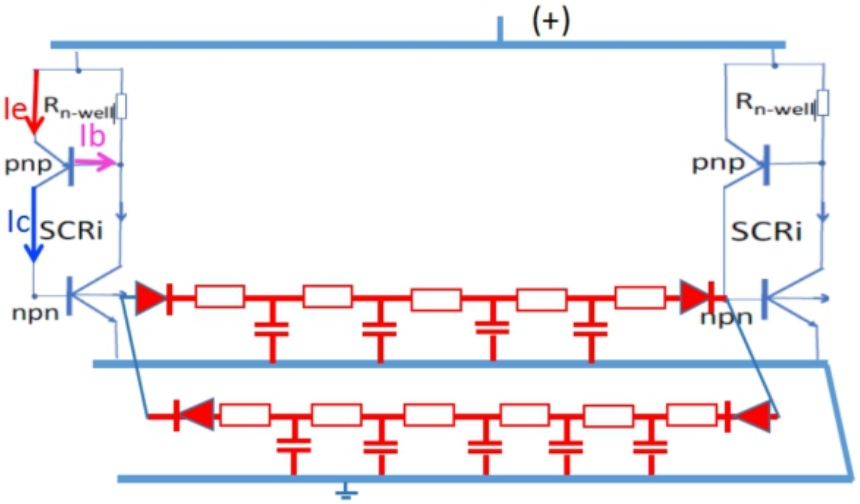


Figure 4.15 Simple schematic of two fingers that shows the main currents of the pnp transistor

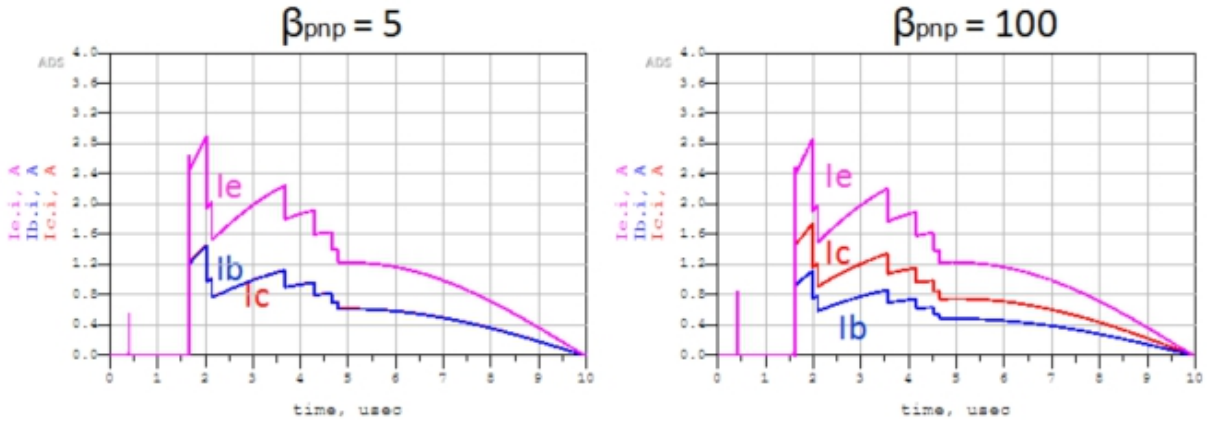


Figure 4.16 The main currents of the pnp transistor before and after increasing βpnp

4.4.3 Missing Finger

To observe the effect of a missing finger on the delays, SCR4 was disconnected without making any other changes.

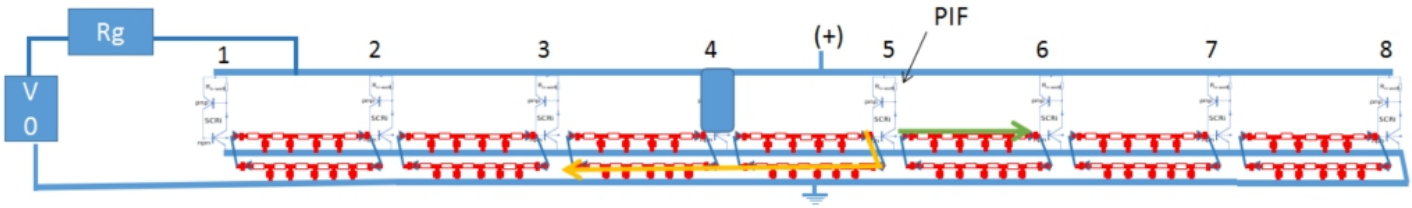


Figure 4.17 Simple schematic of the model after disconnecting SCR4

First, when the simulation was run, the first 4 fingers didn't trigger because the line between SCR5 and SCR3 got too long, as shown in figure 4.17.

So the source voltage was necessary to increase from 100V to 300V in order to trigger all the fingers.

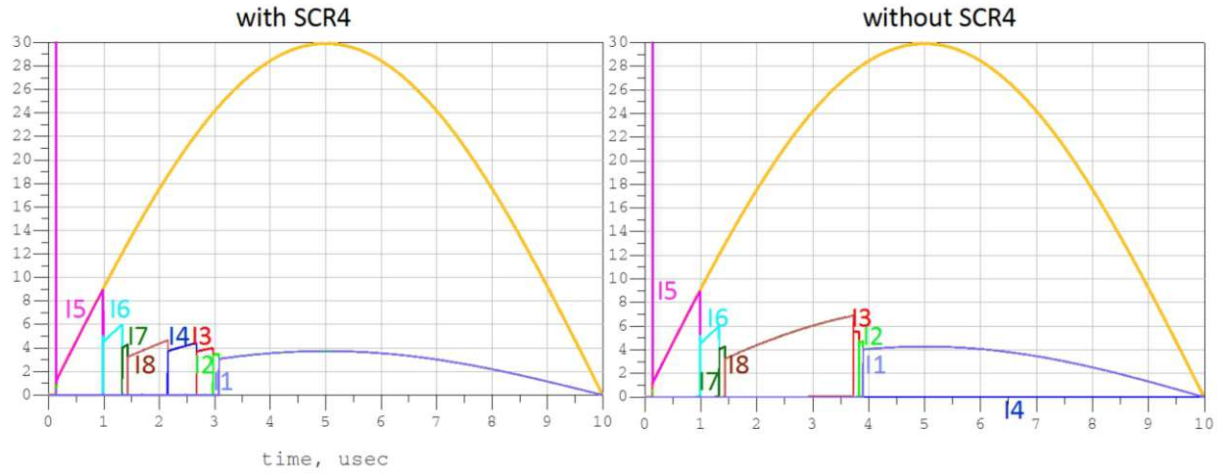


Figure 4.18 The individual currents with and without SCR4

Since the RC line between SCR3 and SCR5 became considerably long, the trigger delay of the fingers 1,2, and 3 increases (see figure 4.18).

Vbe of the npn transistor of SCR6 reaches BE junction voltage before SCR3 because the RC line between SCR5 and SCR6 is much shorter than between SCR5 and SCR3 (see figures 4.17 and 4.19).

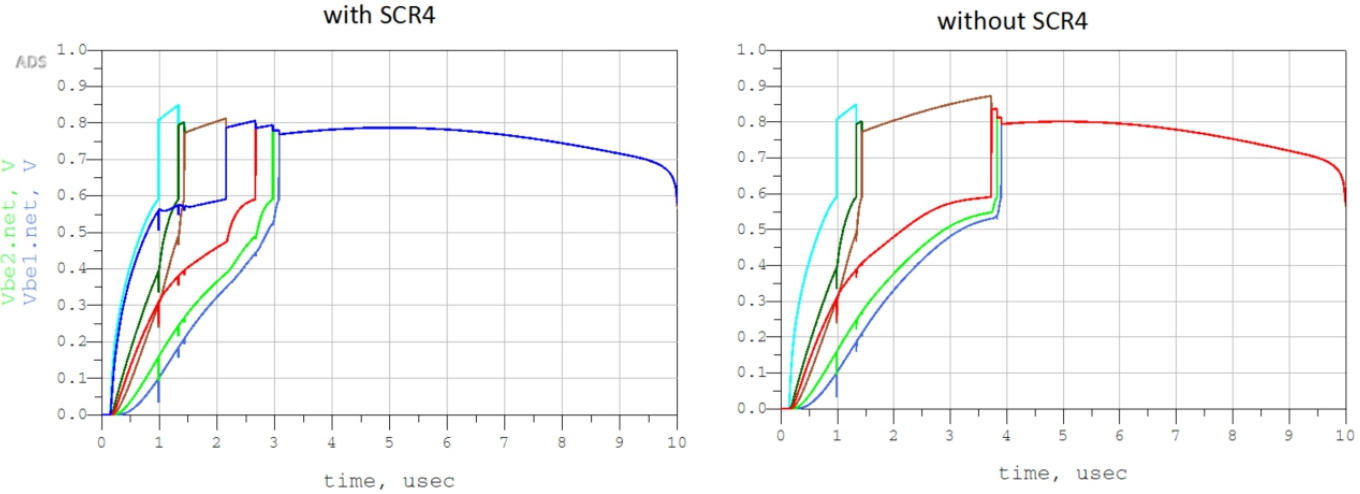


Figure 4.19 Vbe of the npn transistor of the fingers with and without SCR4

4.4.4 Varying Position of the Initial Finger (PIF)

In this section, the position of the initial finger was moved to the left. So became the initial finger the 4th finger from the left (see figure 4.20).

As shown in figure 4.21, Changing PIF has changed the triggering sequence completely and left hand fingers triggered first. The fingers triggered in this sequence :

4 -> 3 -> 2 -> -> 1 -> 5 -> 6 -> 7 -> 8

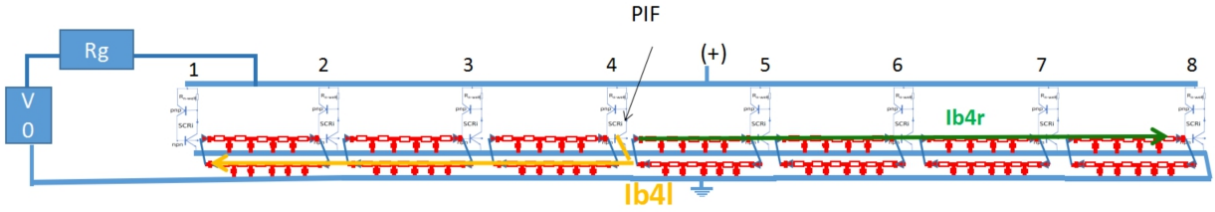


Figure 4.20 Simple schematic of the model after changing PIF to 4

Moving the initial finger in a certain direction reduces the delay in that direction and increases the delay in the opposite direction because the shorter the path of the triggering current is, the faster Vbe of the npn transistor will increase and vice versa (e.g. in figure 4.20 the current Ib4l charges 3 RC lines while Ib4r charges 4 of them).

It should be mentioned that, the green and orange arrow also in figure 4.20 refers to the current paths of Ib4l and Ib4r, where the current along the line can change.

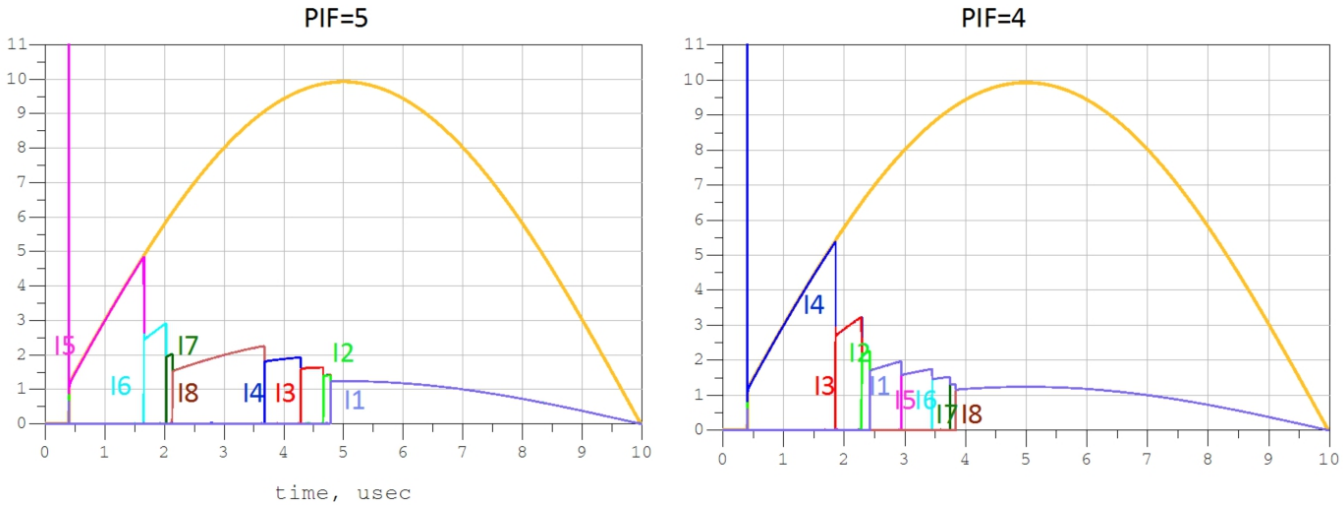


Figure 4.21 The individual currents before and after changing PIF

4.4.5 The Metal Resistance

In this section, the metal resistance is considered and it was represented once with Rtop before each finger, as in figure 4.22, and once with Rbot after each finger.

4.4.5.1 Rtop

Figure 4.23 shows that, after adding Rtop=1Ω to the model, the delays got a bit longer and the currents got a bit smaller.

Adding Rtop reduces the voltage on each finger. So this effect is similar to the effect of decreasing the source voltage amplitude and it has the same consequences.

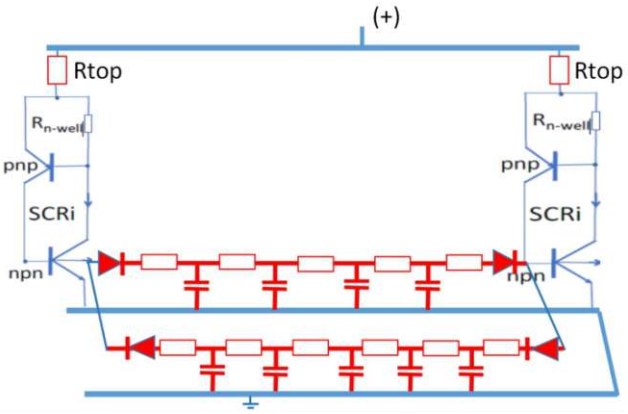


Figure 4.22 Schematic of two fingers with Rtop

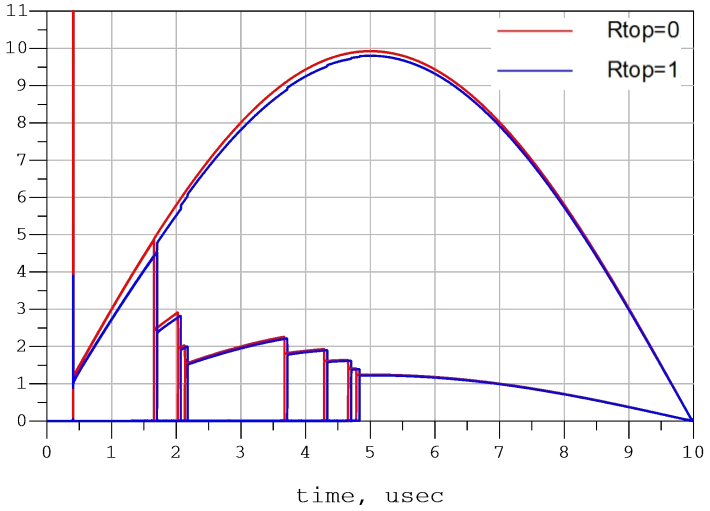


Figure 4.23 The individual currents with and without Rtop

4.4.5.2 Rbot

Adding Rbot causes a large decrement in the delays (see figure 4.24). Therefore, only Rbot = 200 mΩ was added to each finger and was enough to show its effect.

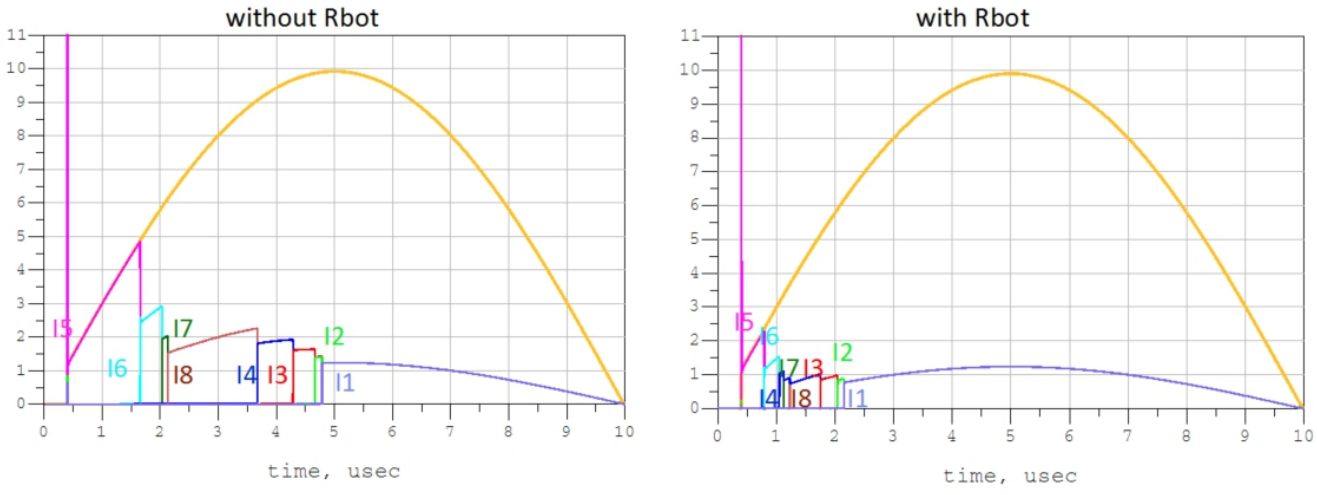


Figure 4.24 The individual currents with and without Rtop

Figure 4.25 shows the currents that got affected by adding Rbot and causes the delays to decrease. Adding Rbot decreases the emitter current of the npn transistor and that leads to a decrement of the base current as well ($Ib = \frac{Ie}{1+\beta}$).

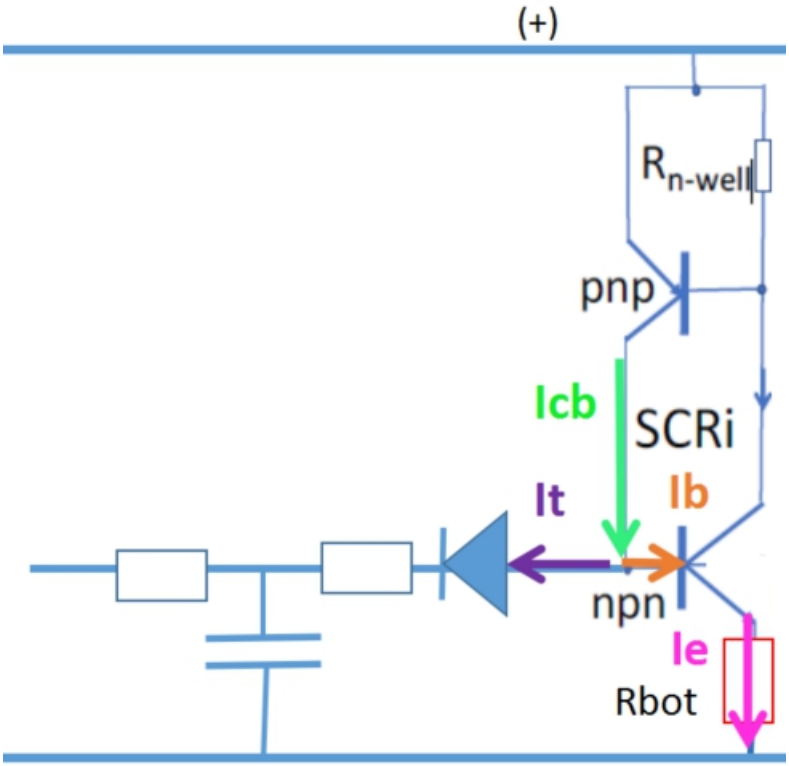
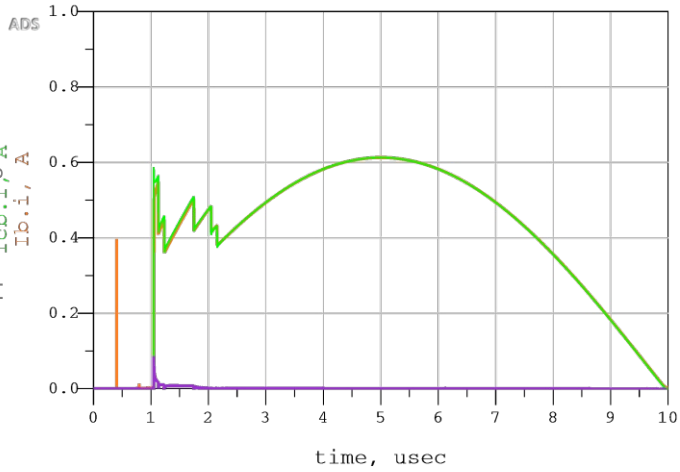
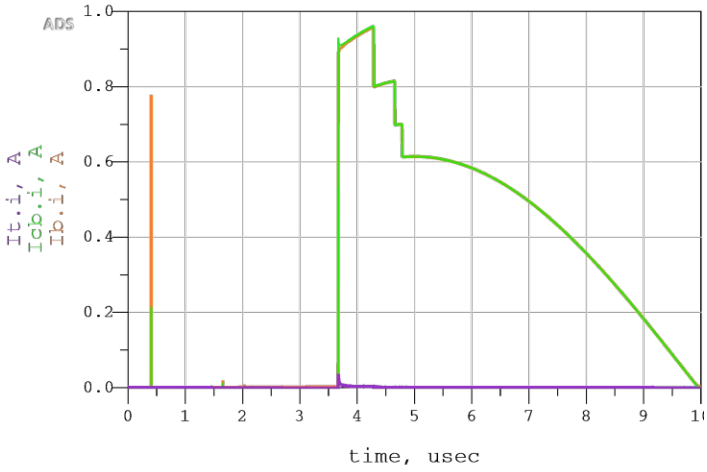


Figure 4.25 Schematic shows the currents that got affected by adding Rbot and causes the delay to decrease



(a)



(b)

Figure 4.26 The currents Ib, It and Icb (a) before adding Rbot and (b) after adding Rbot. Taken from SCR6

By adding Rbot a smaller current “Ib” flows into the base of the npn and a larger current “It” flows in the RC lines (see figure 4.26). That’s why the delays decrease.

This effect is similar to the effect of increasing βnpn because Ib of the npn transistor is decreased in both cases.

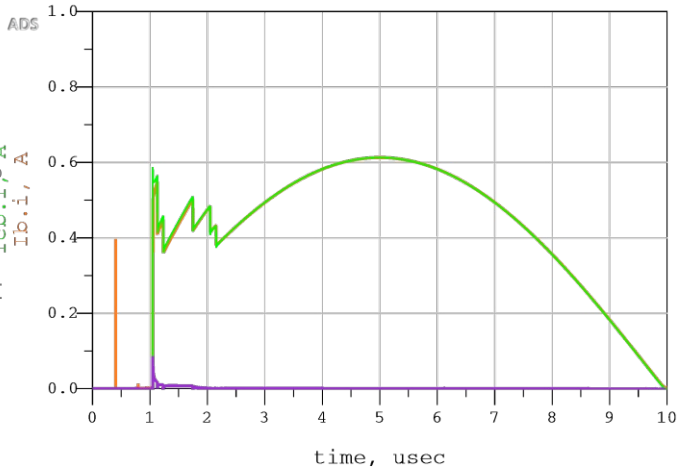
4.5 Triggering by Rising and Falling Edge

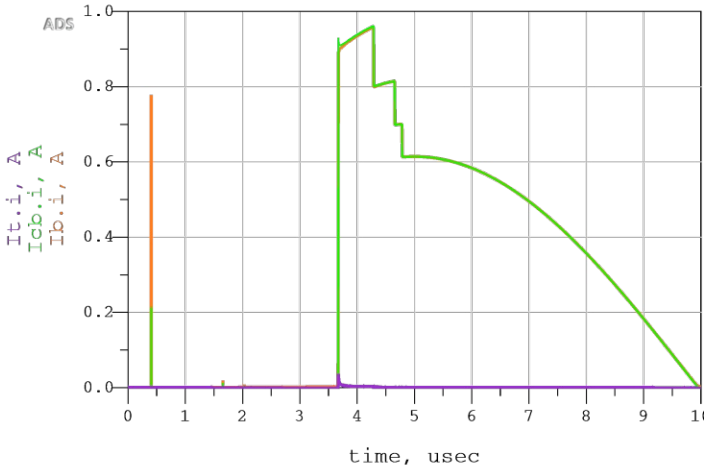
We can notice from the results in this chapter that all fingers triggered on the rising edge of the surge. Even by changing the parameters, this fact didn't change.

A parameter was found in this thesis that can be increased to reach a device that triggers not only on rising edge but also on falling edge. This parameter is the capacitor C of the RC line.

To show this effect, a simulation was run using a new model with new RC lines which have larger capacitors. In this new model the same amount of resistors and capacitors were used but with different values R=2 Ω , C=12 nF.

Figure 4.27 shows the individual currents after increasing C , we can see that most of the fingers trigger also on falling edge. Here it is questionable whether such a large capacitance is physically justified. A large diffusion capacitance can, however, exist in forward biased pn junction [5]. This possible effect is out of the scope of the thesis.





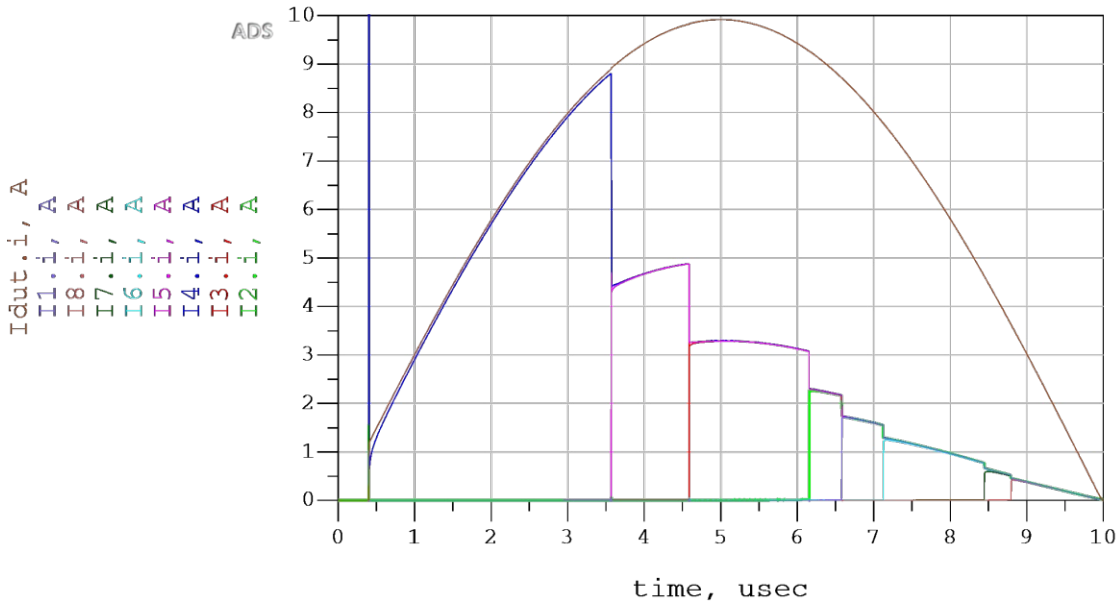


Figure 4.27 The individual currents after increasing C (the new model)

5 CONCLUSION AND FUTURE WORK

5.1 Conclusion

Based on the paper [1]“Simultaneous and Sequential Triggering in Multi-Finger Floating-Base SCRs Depending on TLP Pulse Rise Time”, two compact multifinger ESD protection device models with SFT were developed for SPICE type simulation. This thesis has also carried out a qualitative analysis of the models and found the main parameters that influence the trigger behavior. Both models show a sequential finger triggering behavior with slow and fast triggering processes.

The model developed in chapter 3 is supplied by a TLP pulse, which has the advantage that it can characterize the model by the TLP IV curve as done in parts 3.6.1 and 3.6.3.

The RC lines in the model of chapter 3 are isolated, which means that no current reaches the gate of the SCR finger unless all the previous fingers are triggered. This is not the case in the model from chapter 4 when the missing finger and the position of the initial finger affect the trigger behavior.

The model in chapter 4 is stressed by a surge, which has a larger time domain than TLP.

Trigger delay in chapter 4 depends on the direction of triggering movement, which represents the physical situation of a long device.

In both models, the npn transistor has a greater influence on the trigger behavior than the pnp transistor, e.g., increasing βnpn causes a greater decrease in delays than increasing

βpnp, adding Cbe to the npn transistor causes a larger increment of the delays than to the pnp transistor, adding Rbot has a greater effect than Rtop.

It has also been observed that increasing the voltage source always causes a decrease in delays.

If a calibrated model is developed, the compact modelling, as presented in this thesis, can be used to predict the triggering behavior without the necessity of TCAD simulation. This can shorten the development cycle for the ESD-safe chip design.

5.2 Future Work

There are a number of directions that this work can be taken to improve the models and the modeling methods.

In this thesis, two models were presented. The model in chapter 3 has the advantage that the trigger pulse is isolated between the fingers. The model in chapter 4 has the advantage that the model is more real due to the asymmetry of the RC lines. We could achieve both benefits by combining the two models into a model like the one in figure 5.1.

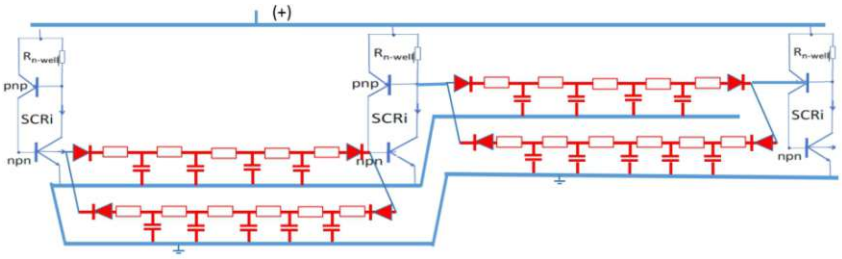


Figure 5.1 Schematic of the combined model

In addition, we can model the currents deep in substrate in future work by placing another RC line perpendicular to the original RC line as in figure 5.2.

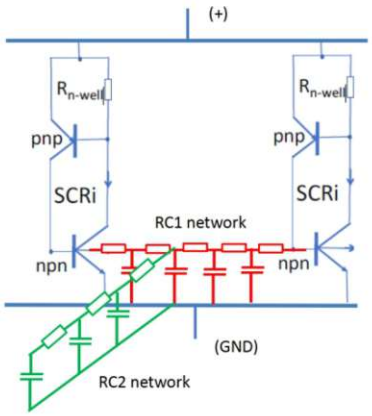


Figure 5.2 Modelling the depth of the chip. Taken from slides of D.Pogany.

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