Diploma Thesis

Negative capacitances in TIA applications

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THE ROAD TO WISDOM

The road to wisdom?—Well it's plain and simple to express:
Err
and err
and err again,
but less
and less
and less.

— Piet Hein —

ABSTRACT

Large area photodiodes (PDs) are advantageous for long distance optical data transmission in free space, but impact the bandwidth and noise performance of the transimpedance amplifier (TIA) that converts and amplifies the photocurrent, due to significant parasitic capacitance. Negative equivalent capacitance can be generated at the input of the TIA via the Miller effect to compensate the PD capacitance. However, the impact of negative capacitance on TIA stability, noise performance and frequency response has not been thoroughly studied so far. These characteristics are vital to ensure a functioning TIA implementation and to meet bit error rate (BER) or distance requirements. This thesis presents a rigorous study of stability and noise in shunt-feedback TIAs with negative capacitance. Although the focus is on generality, a CMOS three-inverter TIA is used as a prime example throughout this work. Pre-layout simulations and analytic modeling are used to approach the problems. Stability limits for the loop gain and closed-loop transimpedance are derived analytically. Thereby it is shown that negative capacitance can provoke a state with unstable loop gain, but overall stable transimpedance. The dependency of input referred noise on negative capacitance is expressed analytically, and it is shown that noise can be optimized by setting a specific amount of negative capacitance. An approximation for this optimal capacitance is derived. At the optimal point the input referred root mean square (RMS) noise current improves by up to $-6\,\mathrm{dB}$ compared to the same TIA without negative capacitance.

Kurzfassung

Großflächige Photodioden (PDs) bringen Vorteile für die optische Freiraumübertragung von Daten, verschlechtern jedoch das Verhalten des nachfolgenden Transimpedanzverstärkers (TIA), der den Photostrom verstärkt und in eine Spannung konvertisch. Insbesondere erhöht sich durch die größere Fläche die parasitäre Kapazität der PD, welche die Bandbreite des TIA schmälert und dessen Rauschverhalten nachteilig beeinflusst. Um diesem Verhalten entgegenzuwirken kann über den Miller-Effekt eine negative äquivalente Kapazität am Eingang des TIA erzeugt werden, welche die parasitäre Kapazität kompensiert. Die Auswirkungen der negativen Kapazität auf das Frequenzverhalten, die Stabilität und das Rauschverhalten von TIAs wurden in der Literatur bisher unzureichend untersucht, obwohl diese Eigenschaften essenziell für eine funktionierende Realisierung, und für die Erfüllung von Spezifikationen der Bitfehlerrate (BER) oder Übertragungsdistanz, sind. Diese Diplomarbeit präsentiert eine rigorose Untersuchung des Stabilitäts- und Rauschverhaltens von parallel rückgekoppelten TIAs (shunt-feedback TIAs) mit negativer Kapazität. Der Fokus liegt dabei auf der Allgemeingültigkeit der Ergebnisse, obwohl in der gesamten Arbeit ein dreistufiger CMOS Inverter-TIA als primäres Anwendungsbeispiel dient. Zur Untersuchung der Problemstellungen werden pre-layout Simulationen sowie analytische Modelle herangezogen. Die Stabilitätsgrenzen der Schleifenverstärkung und der Transimpedanz des geschlossenen Systems werden analytisch hergeleitet. Anhand dieser Grenzen wird gezeigt, dass durch negative Kapazität ein Zustand mit instabiler Schleifenverstärkung auftreten kann, während die Transimpedanz stabil bleibt. Weiters wird die Abhängigkeit des eingangsbezogenen Rauschens von der negativen Kapazität analytisch ausgedrückt. Es wird gezeigt, dass Rauschen durch bestimmte Werte negativer Kapazität minimiert wird. Eine Näherung des optimalen Wertes für die negative Kapazität wird hergeleitet. Im Minimum ist eine Verbesserung des Effektivwerts des eingangsbezogenen Rauschstroms um bis zu $-6\,\mathrm{dB}$, im Vergleich zum selben TIA ohne negative Kapazität, gegeben.

ACKNOWLEDGEMENTS

CONTENTS

Acronyms

PSD power spectral density. 21–24, 33–36, 38, 44, 48, 50

RF radio frequency. 3

RMS root mean square. v, 21, 23, 24, 44, 45, 47, 51

RSD root spectral density. 21

SFG signal flow graph. 7, 8, 13, 20, 24, 33, 49, 53, 54

SPAD single-photon avalanche diode. 2

TIA transimpedance amplifier. v, vii, 2–9, 11, 16, 24, 27, 29, 32, 33, 36–42, 44, 48, 50, 51, 57, 58

TTC time and transfer constants. 49

WSS wide-sense stationary. 21

1 Introduction

1.1 Motivation

Optical transmission plays a key role in contemporary digital communication systems. Information is encoded, modulated and transmitted via different media, such as glass fibre, plastic optical fibre (POF) or free space. The latter variant is also known as optical wireless communication (OWC). At the receiving end a photodetector converts the optical signal into an electrical signal – typically an electrical current – at a given conversion rate: the so-called responsivity R. Common photodetectors are photodiodes (PDs), such as pin-PDs, avalanche photodiodes (APDs) and single-photon avalanche diodes (SPADs). The output current of the PD is amplified and converted to a voltage signal by a transimpedance amplifier (TIA), which is the first, and therefore the most critical, amplifier in the receiver. In long distance transmissions the incident optical signal power can be fairly weak, resulting in a low-amplitude electrical signal. Hence, the *sensitivity* of the TIA is of utmost importance.

Electrical sensitivity is defined as the minimum acceptable peak-to-peak input current to achieve a certain bit error rate (BER) at the output of the receiver [25]. Furthermore, optical sensitivity is defined as the minimum acceptable average incident optical power to achieve a certain BER [25]. Thus, optical sensitivity comprises electrical sensitivity. Since the BER depends on output noise, the sensitivity of an amplifier is directly related to its noise performance. To further improve the achievable distance in OWC applications, one could employ a PD with large area to increase the received optical power. However, the parasitic capacitance C_{PD} of the PD increases with area as well and is detrimental to the TIA bandwidth and noise performance [25]. To counteract the loss in bandwidth, the transimpedance must be lowered for a given TIA circuit topology. Although this change may seem reasonable, it deteriorates noise performance and therefore nullifies the initial improvement. The question arises: Is there a way to have both, large PD area and good TIA noise performance, at the same time?

Recently, Li and Yue [14] proposed the concept of negative equivalent capacitance to compensate a part of C_{PD}, while maintaining (or even increasing) the effective transimpedance of the TIA. Thereby, the input referred noise (IRN) current is decreased. The negative capacitance is implemented exploiting the Miller effect in a three-inverter amplifier. This
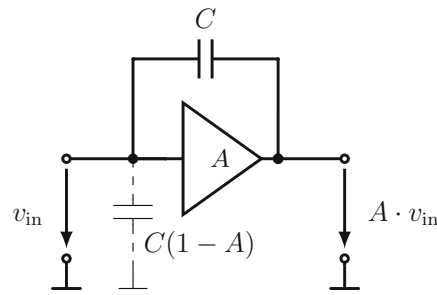
Figure 1.1: Miller effect at the input of a voltage amplifier.

effect occurs when the two terminals of a capacitor are connected to the input and output of a voltage amplifier – see Figure 1.1. The total voltage across the capacitor is $v_{in}(1 - A)$, where A is the voltage gain of the amplifier. Since there is a strict relationship between charge, voltage and capacitance, the capacitor's charge is

$$Q = C \cdot v_C = C(1 - A)v_{in}. \tag{1.1}$$

However, from the point-of-view of the input it seems as if Q is solely caused by v_{in}. Thus, the equivalent capacitance seen at the input is $C' = C(1 - A)$ (dashed in Figure 1.1). The Miller effect is usually associated with inverting amplifiers ($A < 0$) with high gain ($|A| \gg 1$), where it results in an equivalent input capacitance much larger than the actual C. On the other hand, if the gain is larger than one and positive, Equation (1.1) shows that the equivalent input capacitance becomes negative.

1.2 State of the art

This section reviews the state of the art of negative capacitance applications. The latest developments in TIA circuits are not discussed here, to emphasize the focus on negative capacitance.

The notion of negative (equivalent) capacitance is not new per se, however, applications thereof differ with respect to the intended functionality. Bandwidth, noise and impedance matching are of particular interest in both, radio frequency (RF) amplifiers as well as TIAs for optical transmission. Negative capacitance can be applied to improve either of these characteristics.

Neutralization. In RF electronics, impedance matching and tuning are essential for good performance of any design. The transistors that compose an RF amplifier introduce additional parasitics that may detune the circuit. Moreover, they create parallel paths between input and output, resulting in bidirectional signal propagation. Capacitances between input and output (e.g. the gate-drain capacitance in FET-based amplifiers) are particularly troublesome as they are subject to the Miller effect. To annihilate the effects of parasitic capacitances, *neutralization* techniques [12] – sometimes also

(a) Basic concept of input node neutralization.

(b) Practical realization of neutralization in differential amplifiers via cross-coupled capacitors.
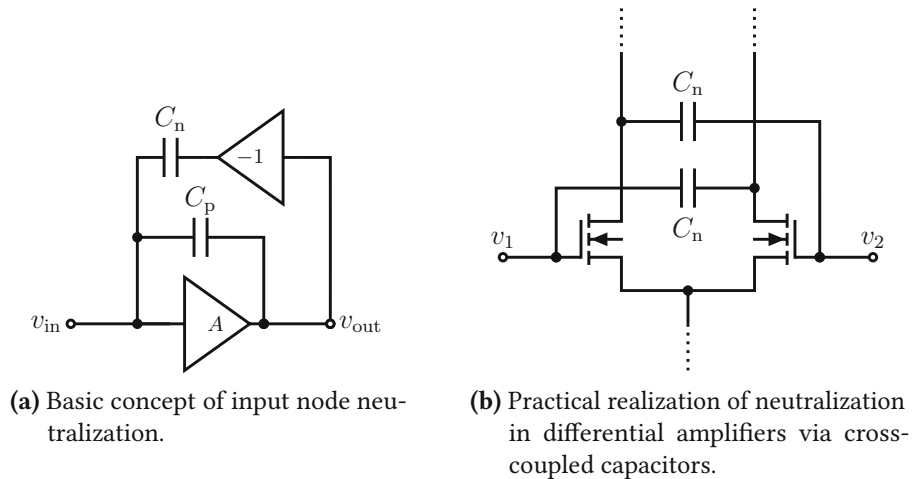
Figure 1.2: Neutralization in amplifiers: (a) Basic concept, (b) Practical implementation.

referred to as unilateralization [7, 23] – can be applied. The fundamental idea of neutralization is always the same: Figure 1.2a shows an amplifier with gain A and parasitic capacitance C_p. In order to neutralize the charge of C_p at the node of interest (e.g. the input node), the same quantity of opposite charge must be injected at the input node. To do so, an inverting unity-gain buffer is connected to the output and drives the neutralization capacitor C_n, which has the same capacitance as C_p. Practical implementations often employ differential amplifiers, because they naturally exhibit complementary gains. Hence, there is no need for a unity-gain buffer. Cross-coupled neutralization capacitors are used to compensate the gate-drain (or base-collector) capacitance [7, 12] – see Figure 1.2b.

Ramzan et al. used the cross-coupling neutralization for impedance matching and broadbanding (see below) in [19] to implement a wideband low noise amplifier (LNA) in $0.13\,\mu\mathrm{m}$ standard CMOS technology. According to the authors, the achieved performance is similar to other LNAs, but less supply voltage, power and area were required. In [1], Asada et al. implemented the cross-coupling neutralization for unilateralization in a $60\,\mathrm{GHz}$ power amplifier using a $65\,\mathrm{nm}$ CMOS process. It is shown that the unilateralization improves amplifier stability. Together with an optimized transmission line, a total power gain of $23.2\,\mathrm{dB}$ was achieved.

Broadbanding. Bandwidth extension of TIAs is usually achieved by placing an inductor between two parallel capacitors to split a dominant pole into two less dominant poles [25]. Negative capacitance is an alternative broadbanding technique that can be used instead of inductive bandwidth extension.

In 1993, Vadipour demonstrated capacitive bandwidth extension in a discrete bipolar differential amplifier [27]. Bandwidth was increased from $20\,\mathrm{MHz}$ to $86\,\mathrm{MHz}$ while maintaining a flat frequency response without peaking. This major improvement was

achieved by using a feedback capacitance that is larger than the capacitance needed for neutralizing the base-collector capacitance. The exact value was derived using the flat frequency response constraint. Galal and Razavi used the cross-coupling neutralization principle from Figure 1.2b to implement the front-end of each gain cell in a $10\,\mathrm{Gbit/s}$ limiting amplifier [5]. Together with two other techniques, namely inductive peaking and active feedback, a $-3\,\mathrm{dB}$ bandwidth of $9.4\,\mathrm{GHz}$ was achieved. In [22], Shem-Tov et al. present a fully differential operational amplifier (OPAMP) in a $0.18\,\mu\mathrm{m}$ standard CMOS process. Negative capacitance was implemented via a buffer with gain[1] $A = 0.6$ that follows the operational transconductance amplifier (OTA) core, with the aim to reduce the overall output capacitance. The latter defines the second smallest pole, which affects the unity-gain frequency and phase margin of the OPAMP. Post-layout simulations showed a unity-gain frequency of $392\,\mathrm{MHz}$ with a phase margin of $73°$ when loaded with $1\,\mathrm{k}\Omega$ in parallel to $2\,\mathrm{pF}$, whereas the same OPAMP without negative capacitance achieves $251\,\mathrm{MHz}$ and $37°$, respectively. In the simulation-based study [3], Comer et al. conclude that broadbanding via negative capacitance is most beneficial to high-gain amplifiers. This is because the high load resistance required for high gain, together with (parasitic) load capacitance solely define the $-3\,\mathrm{dB}$ corner frequency. A case study employing TSMC's $0.25\,\mu\mathrm{m}$ CMOS process shows that the bandwidth of a cascoded differential amplifier can improve by a factor of up to 54, whereas the bandwidth of a composite cascode stage increases by a factor of up to 77. All improvements were made while retaining flat frequency response and gain.

The work by Li and Yue [14], which is the incentive for this thesis, is best characterized as a broadbanding application. By employing a feedback capacitance of $C = 12.5\,\mathrm{fF}$, the bandwidth of a three-inverter TIA in $40\,\mathrm{nm}$ CMOS is extended from $1.2\,\mathrm{GHz}$ to $3\,\mathrm{GHz}$. Compared to a regular three-inverter TIA with $3\,\mathrm{GHz}$ bandwidth, the transimpedance of the three-inverter TIA with negative capacitance (3INV-TIA-C) is $5.7\,\mathrm{dB}$ higher, which results in a noise improvement of $-1.8\,\mathrm{dB}$. Stability is not examined. The work that comes closest to [14], and thus also to this thesis, is [8], wherein capacitive broadbanding for shunt-feedback TIAs is studied. The authors designed a differential TIA in a $0.18\,\mu\mathrm{m}$ SiGe BiCMOS process with a target transimpedance of $500\,\Omega$ and $5.5\,\mathrm{GHz}$ bandwidth. With a feedback capacitance of $C = 20\,\mathrm{fF}$, the bandwidth extends to $7.87\,\mathrm{GHz}$. The key conclusions are as follows: The negative capacitance approach introduces very little area, power and noise penalty. Furthermore, for high feedback resistance R_f, the newly added zero in the transfer function is located far above the $-3\,\mathrm{dB}$ bandwidth. The main disadvantage of this technique is the increase in group delay distortion.

Noise matching. Noise matching is a technique to reduce the IRN of an amplifier by presenting a modified source impedance to its input [25]. In [2], a MOSFET-based immittance converter circuit is employed to realize negative equivalent capacitance

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[1]Note that due to gain below unity the Miller effect is significant at the output of the buffer, but negligible at its input.

for power- and noise-matching at the input of a wideband LNA. The LNA was implemented in TSMC's $65\,\mathrm{nm}$ GP CMOS process. Measurement results show a noise figure of just $1\,\mathrm{dB}$ between $10\,\mathrm{MHz}$ and $2.8\,\mathrm{GHz}$.

1.3 Research questions

Except for [1], none of the papers presented in Section 1.2 examines stability issues related to negative capacitance. For C_{gd} neutralization applications, this might be reasonable due to the very small capacitances. In addition, the flat frequency response constraint in broadbanding applications [3, 27] exerts control on the poles of the transfer function (transimpedance) and thereby ensures stability. However, when applying negative capacitance for broadbanding and C_{PD} compensation in TIAs up to the point of zero net capacitance, stability might become an issue. We know from [14] that the noise performance of TIAs can be improved through an increase of R_{f} that counteracts the broadbanding effect. Still, the derivation of the IRN in [14] is based on the premise of very small feedback capacitance C, which might not hold in general. Furthermore, a discussion of the optimal choice of C with regards to noise is absent. Therefore, the purpose of this thesis is to answer the following research questions:

1. How does negative capacitance affect the overall behavior (gain, bandwidth, frequency response) of TIAs, in particular the three-inverter TIA?

2. Does negative capacitance interfere with the stability of the TIA?

3. What is the impact of negative capacitance on the noise performance of a TIA? Are there optimal and less optimal values of C with regards to noise?

In this thesis a combination of simulation and modeling is used to study the issues specified above. Ideally, one should corroborate the resulting findings with an implementation and experimental data from measurements thereof. However, circuit design, layout and fabrication are not within the scope of this work. The concept of negative capacitance is studied based on a given three-inverter TIA design, taken from [6]. The impact on group delay variation, that is pointed out in [8], is not examined in this work.

This work is organized as follows: Chapter 2 documents the developed models. In Chapter 3 the models are applied to analyze different aspects of TIAs with negative capacitance, in particular the issues specified by the research questions. Chapter 4 deals with (pre-layout) simulation results and compares theory to simulation. In Chapter 5 the results are compared to [14] and the applied methods are reflected on. The work concludes in Chapter 6.

2 Transimpedance amplifier modeling

2.1 Model types and purpose

The three major topics of this work are: Frequency response, stability and noise performance of TIAs with negative capacitance. Hence, the purpose of the modeling process is to depict the properties of interest as abstract as possible – to gain knowledge that is applicable to a range of TIA implementations – while remaining accurate enough to allow for exact statements about certain characteristics, such as stability limits.

All of the issues are related to the small-signal behavior of TIAs. Thus, small-signal models of idealized amplifiers and MOSFETs are the basis for the presented models. They are specified in the Laplace domain. Moreover, the models are not split with regards to the three issues; a combined model is used to assess all characteristics. The so-called Driving Point Impedance/Signal Flow Graph (DPI/SFG) method [18] is applied for detailed circuit analysis and modeling. While it is not widely adopted by the community, DPI/SFG was chosen for this work because it is a systematic approach to circuit analysis. In particular, DPI/SFG does not require as many assumptions and simplifications as other methods. For example, dummy loading for loop gain computation is not necessary, since the closed-loop circuit is not torn apart for the analysis. DPI/SFG also accounts for bidirectional signal propagation in amplifiers (e.g. due to parasitics) and output loading per default. Hence, circuits do not have to be rearranged into dedicated forward and backward paths – in contrast to the method described in Chapter 8 in [9], for example. The resulting models are signal flow graphs (SFGs) and the equivalent analytical transfer function(s) in the Laplace domain. For stability analysis the circuit models are converted into two-port descriptions. The two-port model is formally defined as

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}, \tag{2.1}$$

where i_1 and i_2 are the currents into port 1 and 2; whereas $v_1 = v_{\text{in}}$ and $v_2 = v_{\text{out}}$ are the voltages at those ports.

(a) Simple shunt-feedback TIA, **(b)** Simple three-stage voltage amplifier with capacitive feedback. after [25].
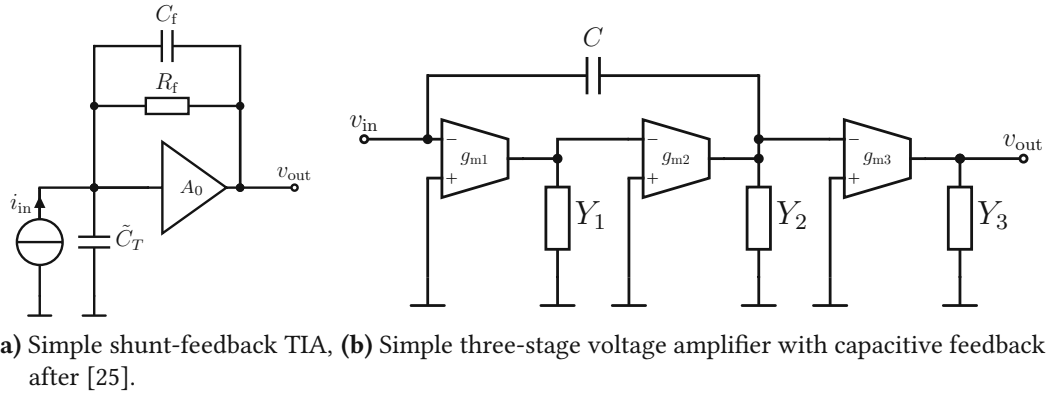
Figure 2.1: Simple TIA circuit models.

Another advantage of the DPI/SFG approach is that noise calculations are seamlessly integrated into the model. The individual noise sources directly contribute to either short circuit currents or node voltages and thus can be treated the same way as any other signal in the SFG.

2.2 Ideal amplifier model

Basic, highly simplified models often allow to draw conclusions that are not immediately apparent in complex detailed models. Therefore, a simple TIA model is derived first. Figure 2.1a shows a TIA circuit with shunt-feedback configuration. The amplifier has infinite bandwidth and output loading is neglected, but the gain is limited to the constant A_0. More specifically, only inverting amplifiers are considered, thus $A_0 < 0$. Since this work is associated with optical communication, the input signal source is modelled as an ideal current source with parallel capacitance. This is common practice for diode-based photodetectors [25, 28]. The overall transimpedance of this circuit for $C_f = 0$ is [25]

$$H(s) = \frac{\frac{A_0}{1-A_0}R_f}{1 + \frac{sR_f\tilde{C}_T}{1-A_0}}. \tag{2.2}$$

Substitution of $R_f \longrightarrow R_f/(1 + sR_fC_f)$ yields

$$H(s) = \frac{\frac{A_0}{1-A_0}R_f}{1 + s\frac{R_f(\tilde{C}_T+(1-A_0)C_f)}{1-A_0}}, \tag{2.3}$$

which can be approximated by

$$H(s) = -\frac{R_f}{1 - s\frac{R_f(\tilde{C}_T-A_0C_f)}{A_0}} = -\frac{R_f}{1 - \frac{s}{\omega_p}} \tag{2.4}$$

for high gain $|A_0| \gg 1$. For TIAs without negative capacitance $\tilde{C}_T$ is given by the capacitance of the PD C_{PD} and the input capacitance of the amplifier C_I [25]:

$$\tilde{C}_T = C_T = C_{\mathrm{PD}} + C_I \tag{2.5}$$

Their sum is commonly referred to as C_T. However, for TIAs with negative capacitance $\tilde{C}_T$ is modified, such that

$$\tilde{C}_T = C_{\mathrm{PD}} + C_I + C(1 - A_C) \approx C_{\mathrm{PD}} + C_I - CA_C, \tag{2.6}$$

where $C(1 - A_C) \approx -CA_C$ is the negative equivalent capacitance that results from the Miller effect ($A_C \gg 1$) due to internal feedback. C is the feedback capacitance and A_C is the voltage gain between its terminals. A_C depends on the specific circuit design: For example, if the amplifier is implemented via three stages, with C between the second stage output and the amplifier input, $A_C = A_1 A_2$ is given by the gain of the first and second stage.

2.3 Three-stage amplifiers

There are different possibilities to implement negative capacitance in combination with an inverting amplifier. Three-stage (inverting) amplifiers, however, are particularly interesting because they are naturally suited for negative capacitance applications. This is because both, positive and negative gain with respect to the input, is already present in the circuit. The positive gain between the input and the second-stage output is exploited for negative capacitance, as proposed in [14]. In this thesis, the three-inverter TIA is used as a prime example and is therefore modeled in detail. The models in this section abstract the amplifier without the outer feedback loop (R_{f} and C_{f}). Section 2.4 describes how the full transfer function, i.e. the transimpedance, is obtained.

2.3.1 First- and second-order models

Figure 2.1b shows a simple circuit model for a three-stage voltage amplifier, which will be used to derive first- and second-order two-port models. Each stage k consists of a transconductance amplifier with transconductance $g_{\mathrm{m}k}$ – e.g. an inverter or an OTA – that is configured as an inverting amplifier. The output of each stage is loaded by the admittance Y_k.

To begin with, we assume that the load is purely resistive, i.e. $Y_k = 1/R_k$. Based on this assumption the first-order model is developed as follows. The impedance seen at the output node of the circuit in Figure 2.1b is just R_3, that is

$$Y_{22\mathrm{A}} = \frac{1}{R_3}. \tag{2.7}$$

Moreover, there is no backwards gain (transadmittance) Y_{12A} through the amplifier, hence

$$Y_{12A} = 0. \tag{2.8}$$

The forward amplification of each stage can be written as

$$v_{\text{out},k} = -g_{\text{m}k} v_{\text{in},k} R_k = A_k v_{\text{in},k}, \tag{2.9}$$

where $A_k = -g_{\text{m}k} R_k$ is the gain of stage k. Without C, the total gain would follow from the product of the stage gains. However, due to the feedback via C there are two parallel paths from the input to the second stage output. Superposition is used to get the total second stage output voltage. At first, the contribution of the feedback path is calculated. C and R_2 effectively create a voltage divider, thus:

$$v'_{\text{out},2} = v_{\text{in}} \frac{R_2}{R_2 + \frac{1}{sC}} = v_{\text{in}} \frac{sR_2C}{1 + sR_2C} \tag{2.10}$$

Secondly, the output current due to the first and second amplifier is

$$i''_2 = -v_{\text{in}} A_1 g_{\text{m}2}, \tag{2.11}$$

whereas the impedance seen at the output of stage two is

$$Z''_2 = R_2 \parallel C = \frac{R_2}{1 + sR_2C}. \tag{2.12}$$

Therefore, the total output voltage of the second stage is given by

$$v_{\text{out},2} = v'_{\text{out},2} + i''_2 Z''_2 = \frac{-A_1 g_{\text{m}2} R_2 + sR_2C}{1 + sR_2C} v_{\text{in}} = \frac{A_1 A_2 + sR_2C}{1 + sR_2C} v_{\text{in}}. \tag{2.13}$$

Subsequently calculating the total output current of the third stage and solving for the forward transadmittance Y_{21A} yields

$$Y_{21A} = -\frac{A_3}{R_3} \frac{A_1 A_2 + sR_2C}{1 + sR_2C}. \tag{2.14}$$

Note that for $C = 0$ the well-known special case [9] is obtained:

$$Y_{12A} = -\frac{A_1 A_2 A_3}{R_3} \tag{2.15}$$

Lastly, the input admittance, which is solely caused by the feedback path, follows from

Equation (2.13) as

$$i_{\text{in},1} = v_{\text{in}} \left(1 - \frac{A_1 A_2 + sR_2 C}{1 + sR_2 C} \right) sC = Y_{11\text{A}} v_{\text{in}}, \tag{2.16}$$

$$Y_{11\text{A}} = sC \frac{1 - A_1 A_2}{1 + sR_2 C}. \tag{2.17}$$

In conclusion, the first-order two-port model of the three-stage voltage amplifier from Figure 2.1b is given by:

$$Y_{11\text{A}} = sC \frac{1 - A_1 A_2}{1 + sR_2 C} \tag{2.18}$$

$$Y_{12\text{A}} = 0 \tag{2.19}$$

$$Y_{21\text{A}} = -\frac{A_3}{R_3} \frac{A_1 A_2 + sR_2 C}{1 + sR_2 C} \tag{2.20}$$

$$Y_{22\text{A}} = \frac{1}{R_3} \tag{2.21}$$

The second-order model is obtained by substituting all $R_k \rightarrow 1/Y_k$ in Equations (2.18) to (2.21). Note that A_1, A_2 and A_3 become frequency-dependent due to the substitution and are therefore denoted by $A_1(s)$, $A_2(s)$ and $A_3(s)$, respectively. The resulting two-port model is:

$$Y_{11\text{A}} = sC \frac{Y_2(1 - A_1(s)A_2(s))}{Y_2 + sC} \tag{2.22}$$

$$Y_{12\text{A}} = 0 \tag{2.23}$$

$$Y_{21\text{A}} = -A_3(s)Y_3 \frac{A_1(s)A_2(s)Y_2 + sC}{Y_2 + sC} \tag{2.24}$$

$$Y_{22\text{A}} = Y_3 \tag{2.25}$$

2.3.2 The three-inverter TIA – Detailed model

Finally, a highly detailed model of a specific TIA implementation – namely the 3INV-TIA-C – is developed for accurate modeling of high-frequency behavior. Figure 2.2 shows the circuit of the three-inverter TIA [13, 14, 21] with external feedback (C_{f} and R_{f}), as well as internal feedback (C). The latter is responsible for creating negative capacitance at the input node, as discussed previously. The circuit consists of three CMOS inverter stages and diode-connected P-MOSFETs (D1 through D3) at the output of each stage, which set the DC operating point [13, 21]. Thus, no additional bias circuitry is needed.

All MOSFETs are represented by their high-frequency small-signal equivalent circuit (cf. Figure A.1b), and the overall equivalent circuit of the amplifier without the external feedback loop is simplified into Figure 2.3 (similar to [21]).
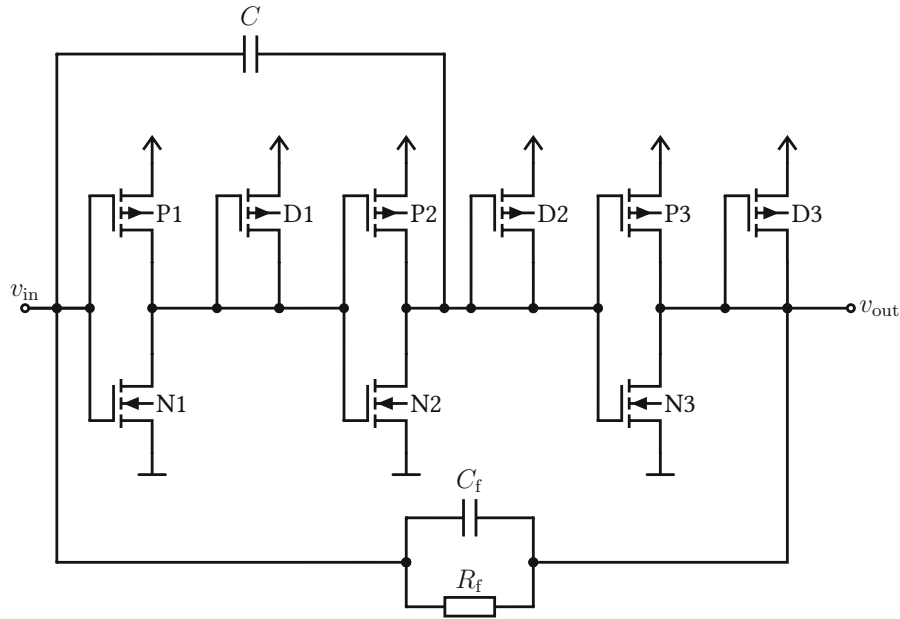
Figure 2.2: Circuit of the three-inverter TIA with internal and external feedback.

Here the admittances Y_i, $i \in \{1, 2, 3\}$ are given by

$$Y_1 = g_{mD1} + g_{dsD1} + g_{ds1} + s(C_{j1} + C_{D1} + C_{gs2}), \tag{2.26}$$

$$Y_2 = g_{mD2} + g_{dsD2} + g_{ds2} + s(C_{j2} + C_{D2} + C_{gs3}), \tag{2.27}$$

$$Y_3 = g_{mD3} + g_{dsD3} + g_{ds3} + s(C_{j3} + C_{D3}), \tag{2.28}$$

whereas the g_{mi} of each stage is the sum of PMOS and NMOS g_m, i.e.:

$$g_{mi} = g_{mPi} + g_{mNi}. \tag{2.29}$$

The capacitances and g_{dsi} are also the sum of PMOS and NMOS,

$$g_{dsi} = g_{dsPi} + g_{dsNi}, \tag{2.30}$$

$$C_{ji} = C_{jPi} + C_{jNi}, \tag{2.31}$$

$$C_{gsi} = C_{gsPi} + C_{gsNi}, \tag{2.32}$$

$$C_{gdi} = C_{gdPi} + C_{gdNi}, \tag{2.33}$$

and the diode capacitances in particular are given by

$$C_{Di} = C_{jDi} + C_{gsDi} + C_{gdDi} \tag{2.34}$$

for each stage.

The first step of the DPI/SFG method is to attach independent voltage sources to each undriven node (cf. Appendix A.1). The resulting circuit is shown in Figure 2.4. Now the
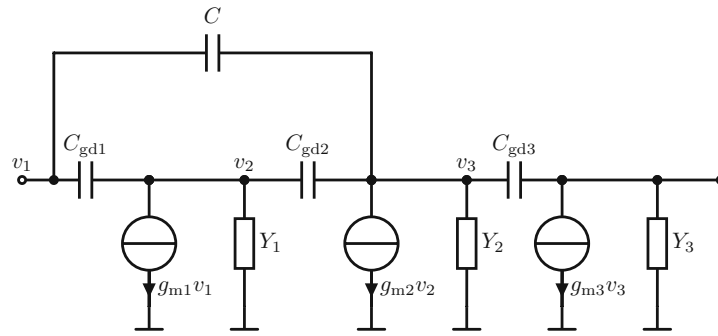
Figure 2.3: Simplified small signal equivalent circuit of the three-inverter TIA.
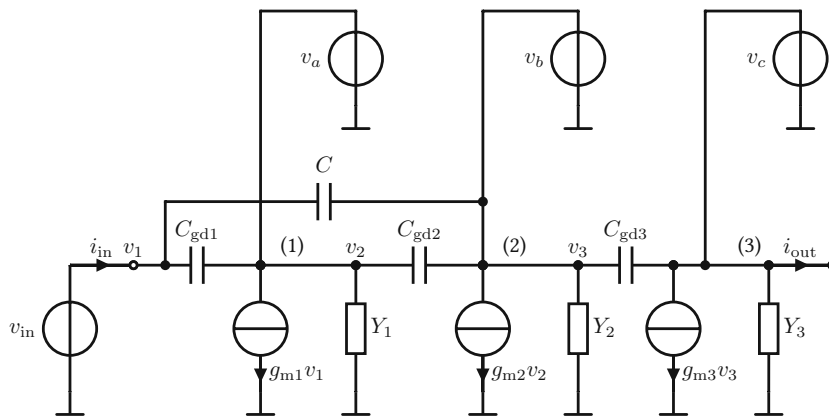
Figure 2.4: Small signal equivalent circuit of the three-inverter TIA for DPI/SFG analysis.

short circuit current into each source, caused by the other sources, is calculated:

$$i_{\mathrm{sc},a} = v_{\mathrm{in}}(sC_{\mathrm{gd1}} - g_{\mathrm{m1}}) + v_b sC_{\mathrm{gd2}} \tag{2.35}$$

$$i_{\mathrm{sc},b} = v_{\mathrm{in}}sC + v_a(sC_{\mathrm{gd2}} - g_{\mathrm{m2}}) + v_c sC_{\mathrm{gd3}} \tag{2.36}$$

$$i_{\mathrm{sc},c} = v_b(sC_{\mathrm{gd3}} - g_{\mathrm{m3}}) - i_{\mathrm{out}} \tag{2.37}$$

Note that it is important to include the output current. Furthermore, the driving point impedance (DPI) – actually the driving point admittance (DPA) – seen by each of the three sources is calculated:

$$Y_{\mathrm{DPI1}} = Y_1 + sC_{\mathrm{gd1}} + sC_{\mathrm{gd2}} \tag{2.38}$$

$$Y_{\mathrm{DPI2}} = Y_2 + sC + sC_{\mathrm{gd2}} + sC_{\mathrm{gd3}} \tag{2.39}$$

$$Y_{\mathrm{DPI3}} = Y_3 + sC_{\mathrm{gd3}} \tag{2.40}$$

Subsequently, the node voltages are expressed via $v = i_{\mathrm{sc}}/Y_{\mathrm{DPI}}$ one by one. The resulting relations are depicted in a SFG – see Figure 2.5. What follows next is the derivation of the two-port model from the SFG. Therefore, the special cases $v_{\mathrm{in}} = 0, v_{\mathrm{out}} = v_c \neq 0$
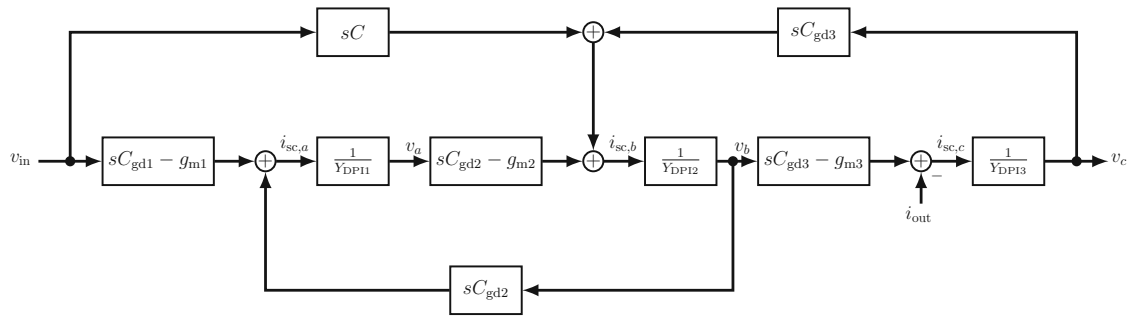
Figure 2.5: Full DPI/SFG model of the three-inverter TIA.
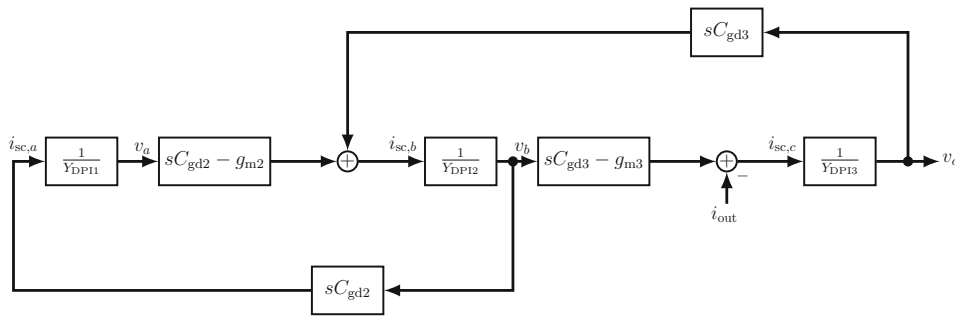
Figure 2.6: DPI/SFG model of the three-inverter TIA for $v_{\text{in}} = 0$.

(see Figure 2.6) and $v_{\text{in}} \neq 0, v_c = 0$ (see Figure 2.7) are analyzed to get $Y_{12\text{A}}, Y_{22\text{A}}$ and $Y_{11\text{A}}, Y_{21\text{A}}$, respectively. Solving for $i_{1\text{A}} = -i_{\text{sc},a}$ and $i_{2\text{A}} = v_c Y_{\text{DPI3}} - v_b(sC_{\text{gd3}} - g_{\text{m3}})$ in the first case ($v_{\text{in}} = 0, v_c \neq 0$) and dividing both currents by v_c yields:

$$Y_{12\text{A}} = \frac{-s^2 C_{\text{gd3}}(sC_{\text{gd1}}C_{\text{gd2}} + CY_{\text{DPI1}})}{Y_{\text{DPI1}}Y_{\text{DPI2}} - sC_{\text{gd2}}(sC_{\text{gd2}} - g_{\text{m2}})} \tag{2.41}$$

$$Y_{22\text{A}} = Y_{\text{DPI3}} - \frac{Y_{\text{DPI1}}sC_{\text{gd3}}(sC_{\text{gd3}} - g_{\text{m3}})}{Y_{\text{DPI1}}Y_{\text{DPI2}} - sC_{\text{gd2}}(sC_{\text{gd2}} - g_{\text{m2}})} \tag{2.42}$$

Subsequently, solving for $i_{1\text{A}} = v_{\text{in}}s(C_{\text{gd1}} + C) - v_a sC_{\text{gd1}} - v_b sC$ and $i_{2\text{A}} = -i_{\text{out}}$ in the second case ($v_{\text{in}} \neq 0, v_c = 0$) and dividing both currents by v_{in} yields:

$$Y_{11\text{A}} = s(C_{\text{gd1}} + C) - \frac{sC_{\text{gd1}}(sC_{\text{gd1}} - g_{\text{m1}})Y_{\text{DPI2}}}{Y_{\text{DPI1}}Y_{\text{DPI2}} - sC_{\text{gd2}}(sC_{\text{gd2}} - g_{\text{m2}})} +$$

$$+ \frac{sC\left[s^2 C_{\text{gd1}}C_{\text{gd2}} + sCY_{\text{DPI1}} + (sC_{\text{gd1}} - g_{\text{m1}})(sC_{\text{gd2}} - g_{\text{m2}})\right]}{Y_{\text{DPI1}}Y_{\text{DPI2}} - sC_{\text{gd2}}(sC_{\text{gd2}} - g_{\text{m2}})} \tag{2.43}$$

$$Y_{21\text{A}} = \frac{-(sC_{\text{gd3}} - g_{\text{m3}})\left[(sC_{\text{gd1}} - g_{\text{m1}})(sC_{\text{gd2}} - g_{\text{m2}}) + sCY_{\text{DPI1}}\right]}{Y_{\text{DPI1}}Y_{\text{DPI2}} - sC_{\text{gd2}}(sC_{\text{gd2}} - g_{\text{m2}})} \tag{2.44}$$
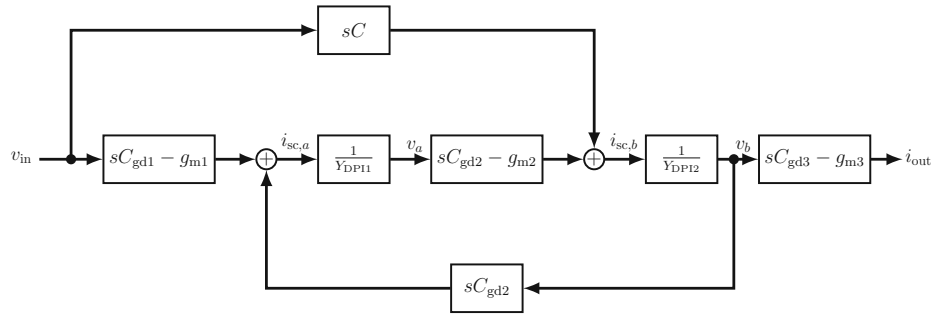
Figure 2.7: DPI/SFG model of the three-inverter TIA for $v_{\text{out}} = v_c = 0$.

Thus, the full high-frequency two-port model is given by Equations (2.41) to (2.44). By setting $C = 0$ the detailed model of the three-inverter TIA without negative capacitance (3INV-TIA) is obtained as a special case of the 3INV-TIA-C:

$$Y_{11A} = sC_{\text{gd1}} - \frac{sC_{\text{gd1}}(sC_{\text{gd1}} - g_{\text{m1}})Y_{\text{DPI2}}}{Y_{\text{DPI1}}Y_{\text{DPI2}} - sC_{\text{gd2}}(sC_{\text{gd2}} - g_{\text{m2}})} \tag{2.45}$$

$$Y_{12A} = \frac{-s^3 C_{\text{gd3}}C_{\text{gd1}}C_{\text{gd2}}}{Y_{\text{DPI1}}Y_{\text{DPI2}} - sC_{\text{gd2}}(sC_{\text{gd2}} - g_{\text{m2}})} \tag{2.46}$$

$$Y_{21A} = \frac{-(sC_{\text{gd1}} - g_{\text{m1}})(sC_{\text{gd2}} - g_{\text{m2}})(sC_{\text{gd3}} - g_{\text{m3}})}{Y_{\text{DPI1}}Y_{\text{DPI2}} - sC_{\text{gd2}}(sC_{\text{gd2}} - g_{\text{m2}})} \tag{2.47}$$

$$Y_{22A} = Y_{\text{DPI3}} - \frac{Y_{\text{DPI1}}sC_{\text{gd3}}(sC_{\text{gd3}} - g_{\text{m3}})}{Y_{\text{DPI1}}Y_{\text{DPI2}} - sC_{\text{gd2}}(sC_{\text{gd2}} - g_{\text{m2}})} \tag{2.48}$$

Furthermore, the gate-drain capacitances can be ignored in order to get a simplified, but less accurate model of the 3INV-TIA-C:

$$Y_{11A} = sC - \frac{sC\left[g_{\text{m1}}g_{\text{m2}} + sCY_1\right]}{Y_1(Y_2 + sC)} = sC\frac{Y_1 Y_2 - g_{\text{m1}}g_{\text{m2}}}{Y_1(Y_2 + sC)} \tag{2.49}$$

$$Y_{12A} = 0 \tag{2.50}$$

$$Y_{21A} = \frac{g_{\text{m3}}\left[g_{\text{m1}}g_{\text{m2}} + sCY_1\right]}{Y_1(Y_2 + sC)} \tag{2.51}$$

$$Y_{22A} = Y_3 \tag{2.52}$$

and of the 3INV-TIA:

$$Y_{11A} = 0 \tag{2.53}$$

$$Y_{12A} = 0 \tag{2.54}$$

$$Y_{21A} = \frac{g_{\text{m1}}g_{\text{m2}}g_{\text{m3}}}{Y_1 Y_2} \tag{2.55}$$

$$Y_{22A} = Y_3. \tag{2.56}$$
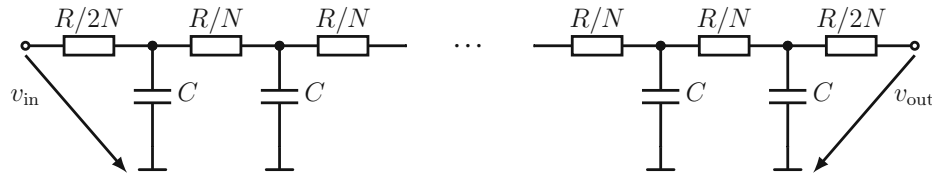
Figure 2.8: RC-chain circuit model of a polysilicon resistor.

2.3.2.1 Polysilicon resistor modeling

Until now, the passive components of the amplifier in Figure 2.2 have been assumed to be ideal components. However, parasitic capacitances are present in real integrated circuits, which influence the high-frequency behavior of those passives. The bandwidth of the feedback resistor R_f is of particular concern when modeling the frequency response of the TIA. Therefore, a model for highly resistive polysilicon resistors (RNP1 and RPP1) is developed based on [28].

The resistor consists of an n-type or p-type polysilicon placed on top of insulating field oxide (FOX), which is fabricated on top of the substrate (or a well). For the circuit-level model the overall resistance R is split into $N+1$ parts for symmetry, whereas its parasitic capacitance is split into N equal parts of $C = C_R/N$ each [28] – see Figure 2.8. C_R is the total parasitic capacitance given by

$$C_R = \frac{\varepsilon_0 \varepsilon_{\mathrm{SiO_2}} LW}{t_{\mathrm{ox}}}, \tag{2.57}$$

where L and W are the length and width of the polyresistor, respectively. t_{ox} is the thickness of the FOX and $\varepsilon_{\mathrm{SiO_2}}$ is its relative permittivity. Since the sheet resistance $R_\square$ of the polyresistor is fixed by the fabrication process, L depends on R and W. Assuming a linear layout without meandering, L can be computed via [28]

$$L = \frac{R}{R_\square} W. \tag{2.58}$$

The circuit model is now converted into its two-port representation, to aid the model integration later on. Since the circuit in Figure 2.8 is symmetric, its admittance matrix Y_{RNP} is also symmetric:

$$Y_{\mathrm{RNP}} = \begin{bmatrix} \frac{1}{Z_{11R}} & Y_{12R} \\ Y_{12R} & \frac{1}{Z_{11R}} \end{bmatrix} \tag{2.59}$$

The diagonal entries represent the impedance seen at either port if the other port is shorted. For the following calculation a short at the output is assumed. Starting at the output, it is evident that $R/2N \parallel C$. This term is subsequently added to R/N and the resulting impedance is again parallel to the second last C. Working our way backwards through the RC-chain we finally arrive at the input port were $R/2N$ is added to the remaining

impedance to get the total impedance

$$Z_{11R} = \frac{R}{2N} + C \parallel \left(\ldots + C \parallel \left(\frac{R}{N} + C \parallel \left(\frac{R}{N} + C \parallel \frac{R}{2N} \right) \right) \ldots \right). \tag{2.60}$$

The off-diagonal entry Y_{12R} determines the output short circuit current due to an input voltage. In analogy to before, the calculation starts at the output and progresses towards the input by iteratively applying the current divider rule. The output short circuit current through $R/2N$ merges with the current through the last C, then flows through the last R/N. Afterwards it merges with the current through the second last C and so on, until the input current is obtained. The input current is given by v_{in}/Z_{11R}. Dividing the final expression by the input voltage we obtain the product

$$Y_{12R} = -\frac{1}{Z_{11R}} \cdot \frac{\frac{1}{sC}}{\frac{1}{sC} + \frac{R}{N} + C \parallel \left(\ldots + C \parallel \left(\frac{R}{N} + C \parallel \frac{R}{2N} \right) \ldots \right)} \cdot \ldots$$
$$\ldots \cdot \frac{\frac{1}{sC}}{\frac{1}{sC} + \frac{R}{N} + C \parallel \frac{R}{2N}} \frac{\frac{1}{sC}}{\frac{1}{sC} + \frac{R}{2N}}. \tag{2.61}$$

The sign of Y_{12R} stems from the fact that the output short circuit current is counted negatively in the two-port model (i.e. it flows into the two-port). With the given two-port model, the transfer function $v_{\mathrm{out}}/v_{\mathrm{in}}$ of the polyresistor circuit from Figure 2.8 equates to

$$\frac{v_{\mathrm{out}}}{v_{\mathrm{in}}} = -Z_{11R} Y_{12R} \tag{2.62}$$

In this work, the number of elements in the RC-chain was set to $N = 10$. The model is applied in numerical analyses, as its complexity is hard to handle in a symbolic (hand) analysis. Furthermore, the sidewall capacitance and additional series resistance due to metal lines are not included in the model. To counteract differences between this model and simulation – which, according to its SPICE code, employs a behavioral model including voltage-dependent resistors – an effective oxide thickness $t_{\mathrm{ox,eff}}$ is used instead of the nominal value. Figure 2.9 shows the simulated and calculated transfer function (Equation (2.62)) for different widths W. The nominal oxide thickness is $t_{\mathrm{ox}} = 0.3\,\mu\mathrm{m}$, whereas the following effective oxide thicknesses have been determined empirically: For $W = \{2\,\mu\mathrm{m}, 0.8\,\mu\mathrm{m}, 0.5\,\mu\mathrm{m}, 0.35\,\mu\mathrm{m}\}$ the fitting process yields $t_{\mathrm{ox,eff}} = \{0.215\,\mu\mathrm{m}, 0.100\,\mu\mathrm{m}, 65\,\mathrm{nm}, 40\,\mathrm{nm}\}$, respectively. With these values the RC-chain model predicts the same $-3\,\mathrm{dB}$ bandwidth as the simulation. However, Figure 2.9 also shows that the transfer function of the model (dashed lines) decreases more rapidly compared to the simulation (solid lines). In theory, this should be an advantage of the model, because it is more conservative about the attenuation at high frequencies. Furthermore, as one would expect, the $-3\,\mathrm{dB}$ bandwidth increases for decreasing width W due to less parasitic capacitance.
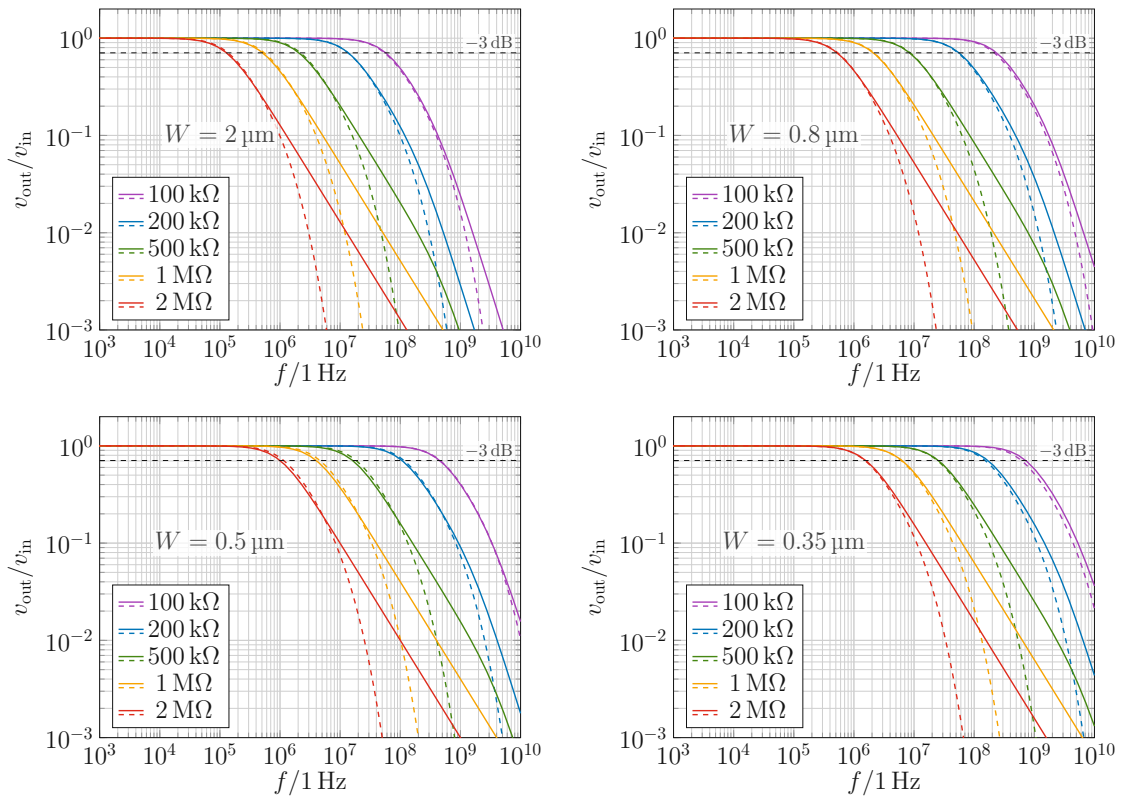
Figure 2.9: Simulated (solid) and calculated (dashed) transfer function of an n-type polysil-icon resistor for different widths W and different nominal resistance values. Linear layout without meandering is assumed.
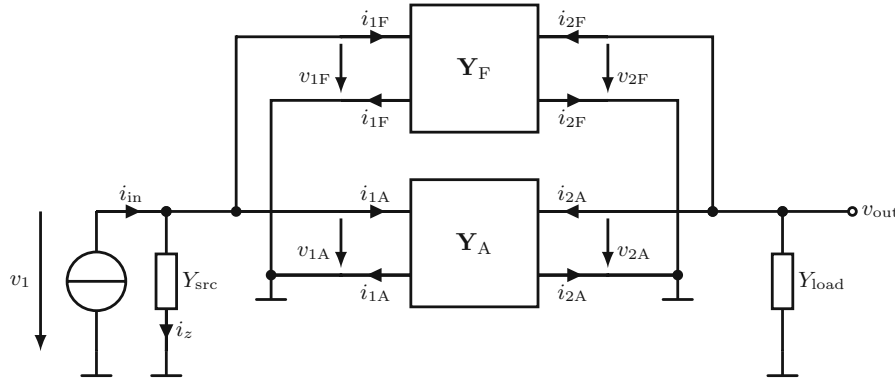
Figure 2.10: Generic amplifier model with feedback network.

2.4 Stability – The Z-method

The stability analysis in this thesis is based on the Hurwitz criterion, the (general) Nyquist criterion and the DPI/SFG method; more specifically, the so-called Z-method [18]. The latter was chosen due to its systematic approach, especially since it does not require to break any feedback loop for loop gain analysis. Hence, dummy loading is not necessary as the analysis accounts for loading as well as feedback within the amplifier itself. First, the Z-method will be derived, as shown in [18]. It is then applied to circuits with negative capacitance to obtain their loop gain. In addition, Appendix A.1.2 proves that the derived loop gain indeed determines the poles of the system transfer function (transimpedance), which is hinted at, but not shown in [18]. The general Nyquist criterion is briefly explained in Appendix A.2; whereas the Hurwitz criterion is not discussed, but can be found in literature [26].

Consider the general amplifier/feedback structure in Figure 2.10. The core amplifier and the feedback network's small signal behavior is described in terms of two-port model's ($Y_{11A}, Y_{12A}, Y_{21A}, Y_{22A}, Y_{11F}, Y_{12F}, Y_{21F}, Y_{22F}$). Furthermore, load and source admittances are included and thus fully accounted for in the calculation. Now the DPI/SFG analysis is applied to *any node in the outer feedback loop*. This step is essential to the Z-method in order to separate signals (currents) that propagate through the complete loop from those that flow to ground, e.g. via the output impedance of the amplifier. In this case, the output node is chosen as the target of the analysis.

Since $v_{1A} = v_{1F} = v_1$ and $v_{2A} = v_{2F} = v_2$, the AC short circuit current at the output is given by

$$i_{sc} = -i_{2A} - i_{2F} = -v_1(Y_{21A} + Y_{21F}) = -i_{in}\frac{Y_{21A} + Y_{21F}}{Y_{11A} + Y_{11F} + Y_{src}}. \tag{2.63}$$

The output DPA with $i_{in} = 0$ is

$$Y_{DPI} = \frac{i_{2A}}{v_{out}} + \frac{i_{2F}}{v_{out}} + Y_{load}, \tag{2.64}$$
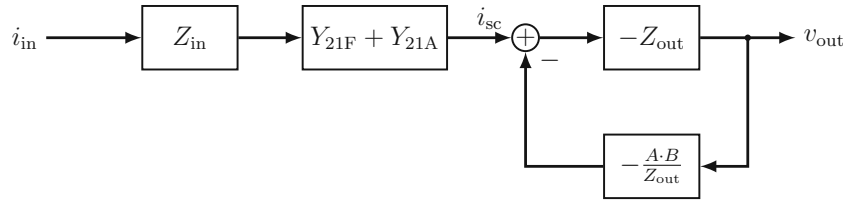
Figure 2.11: DPI/SFG model of the generalized amplifier.

where

$$i_{2\mathrm{A}} = v_1 Y_{21\mathrm{A}} + v_{\mathrm{out}} Y_{22\mathrm{A}}, \tag{2.65}$$

$$i_{2\mathrm{F}} = v_1 Y_{21\mathrm{F}} + v_{\mathrm{out}} Y_{22\mathrm{F}}, \tag{2.66}$$

$$v_1 = -v_{\mathrm{out}} \frac{Y_{12\mathrm{A}} + Y_{12\mathrm{F}}}{Y_{11\mathrm{A}} + Y_{11\mathrm{F}} + Y_{\mathrm{src}}}. \tag{2.67}$$

As a consequence, the DPA is

$$Y_{\mathrm{DPI}} = Y_{\mathrm{load}} + Y_{22\mathrm{A}} + Y_{22\mathrm{F}} - \frac{(Y_{12\mathrm{A}} + Y_{12\mathrm{F}})(Y_{21\mathrm{A}} + Y_{21\mathrm{F}})}{Y_{\mathrm{src}} + Y_{11\mathrm{A}} + Y_{11\mathrm{F}}}. \tag{2.68}$$

The overall transfer function $H(s) = v_{\mathrm{out}}/i_{\mathrm{in}}$ can now be computed. However, a few definitions aid in keeping the overview:

$$Z_{\mathrm{in}} = \frac{1}{Y_{11\mathrm{A}} + Y_{11\mathrm{F}} + Y_{\mathrm{src}}} \tag{2.69}$$

$$Z_{\mathrm{out}} = \frac{1}{Y_{22\mathrm{A}} + Y_{22\mathrm{F}} + Y_{\mathrm{load}}} \tag{2.70}$$

$$AB = -Z_{\mathrm{in}} Z_{\mathrm{out}} (Y_{21\mathrm{A}} + Y_{21\mathrm{F}})(Y_{12\mathrm{A}} + Y_{12\mathrm{F}}) \tag{2.71}$$

Here, Z_{out} is also called the "output impedance with loop gain zeroed" [18]; whereas AB is already the desired loop gain. With these definitions, the overall transfer function equates to

$$H(s) = \frac{i_{\mathrm{sc}}}{i_{\mathrm{in}}} \frac{1}{Y_{\mathrm{DPI}}} = \frac{-Z_{\mathrm{in}} Z_{\mathrm{out}} (Y_{21\mathrm{A}} + Y_{21\mathrm{F}})}{1 + AB}. \tag{2.72}$$

The resulting SFG is shown in Figure 2.11. Note that A and B are not defined separately at this point, and one could define the numerator of Equation (2.72) to be A. Regardless of this definition, only the loop gain AB is relevant for stability analysis. More specifically, Equation (2.72) shows that the zeros of $1 + AB$ are the poles of the system. Thus, we claim that it is sufficient to assess AB to determine the stability of the complete system – see Appendix A.1.2 for a proof.

As mentioned in Section 2.1, rearranging the circuit in Figure 2.10 into a dedicated forward and backward path and applying traditional circuit analysis (Kirchhoff's laws)

is possible. In fact, the resulting relationship (see Equation 8.50 in [9]) is identical to Equation (2.72). However, with DPI/SFG the explicit distinction of paths was not necessary at any point.

2.5 Noise

Noise in electronic circuits occurs due to zero-mean random processes that arise from different physical phenomena and manifests itself as random fluctuations in signals (voltages or currents). In addition to the zero-mean property, the random processes are at least wide-sense stationary (WSS), i.e. their mean and autocorrelation are invariant to time-shifts [16]. However, apart from a few exceptions, the amplitude of noise processes follows a Gaussian distribution; thus they are strict-sense stationary if they are WSS [17]. Noise is typically characterized via its (one-sided) power spectral density (PSD)[1] $S_{\mathsf{x}}(f)$. The two-sided PSD $W_{\mathsf{x}}(f)$ is defined as the Fourier transform of the autocorrelation function $r_{\mathsf{xx}}(t)$ of a WSS random process $\mathsf{x}(t)$, or equivalently, $r_{\mathsf{xx}}(t)$ is the inverse Fourier transform of $W_{\mathsf{x}}(f)$. This is the so-called Wiener-Khintchine theorem [20]:

$$r_{\mathsf{xx}}(t) = \int_{-\infty}^{\infty} W_{\mathsf{x}}(f)\mathrm{e}^{\mathrm{j}2\pi ft}\mathrm{d}f \tag{2.73}$$

At time-shift $t = 0$, the autocorrelation is equal to the mean power, which is identical to the mean square value of the signal [16, 20]:

$$r_{\mathsf{xx}}(0) = \varrho_{\mathsf{x}}^2 = \overline{x^2}(t) = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} x^2(t)\mathrm{d}t \tag{2.74}$$

Combining Equations (2.73) and (2.74) yields

$$r_{\mathsf{xx}}(0) = \overline{x^2}(t) = \int_{-\infty}^{\infty} W_{\mathsf{x}}(f)\mathrm{d}f. \tag{2.75}$$

Since the Fourier transform of real-valued, even signals (such as the autocorrelation of observable noise) is also real-valued and even [4, 20], there is a simple relation between one-sided and two-sided PSD. It follows from

$$\int_{-\infty}^{\infty} W_{\mathsf{x}}(f)\mathrm{d}f = \int_{0}^{\infty} (W_{\mathsf{x}}(f) + W_{\mathsf{x}}(-f))\mathrm{d}f = \int_{0}^{\infty} 2W_{\mathsf{x}}(f)\mathrm{d}f = \int_{0}^{\infty} S_{\mathsf{x}}(f)\mathrm{d}f \tag{2.76}$$

that $S_{\mathsf{x}}(f) = 2W_{\mathsf{x}}(f)$. Equations (2.75) and (2.76) reveal the very important relationship between the spectral characterization of noise sources and their root mean square (RMS) values,

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[1]Graphs often depict the square root of the PSD, which is called the root spectral density (RSD).

$$x_{\mathrm{RMS}} = \sqrt{\int_0^\infty S_{\mathsf{x}}(f)\mathrm{d}f}. \tag{2.77}$$

2.5.1 Sources of noise

This section gives an overview of noise sources based on [9], especially those that are relevant for MOSFETs.

Thermal noise is caused by random fluctuations in the thermal velocity of electrons. It has a Gaussian amplitude distribution and constant PSD, hence it is a form of white noise. Thermal noise occurs in any passive resistor. Its noise current PSD is given by

$$S_{\mathsf{i}}(f) = 4\mathrm{k_B}T\frac{1}{R}, \tag{2.78}$$

where $\mathrm{k_B}$ is the Boltzmann constant[2], R is the resistance in Ohm and T is the absolute temperature in Kelvin. In particular, the thermal channel noise contributing to the drain current of long-channel ($L > 1\,\mu\mathrm{m}$) MOSFETs is given by

$$S_{\mathsf{i}}(f) = 4\mathrm{k_B}T\frac{2}{3}g_{\mathrm{m}}. \tag{2.79}$$

However, for short-channel devices, the factor of g_{m} is larger than $2/3$. SPICE2 defines the thermal channel noise current PSD as [15]

$$S_{\mathsf{i}}(f) = 4\mathrm{k_B}T\frac{2}{3}(g_{\mathrm{m}} + g_{\mathrm{ds}} + g_{\mathrm{mb}}), \tag{2.80}$$

accounting for the drain-source resistance and the body-effect.

Flicker noise is often referred to as $1/f$ noise, since its PSD is proportional to $1/f$. Flicker noise is attributed to traps that randomly catch and release charge carriers of a DC current. A general definition of its noise current PSD is

$$S_{\mathsf{i}}(f) = K\frac{I_{\mathrm{D}}^a}{f^b}, \tag{2.81}$$

where K is a constant for a specific device, I_{D} is the drain DC current, a is a constant and b is a constant near unity. The SPICE2 flicker noise model is [15]

$$S_{\mathsf{i}}(f) = \frac{K I_{\mathrm{D}}^a}{C_{\mathrm{ox}}L_{\mathrm{eff}}^2 f^b}. \tag{2.82}$$

---

[2]$\mathrm{k_B} \equiv 1.380\,649 \cdot 10^{-23}\,\mathrm{J/K}$

Here, the oxide capacitance per unit area C_{ox} and the effective channel length L_{eff} are taken into account. Flicker noise often has a non-Gaussian amplitude distribution.

Shot noise is caused by charge carriers passing through a potential barrier, e.g. a pn-junction. The carriers move across the junction one at a time at random time instants. Although there is a net (DC) current of I, the random movements cause fluctuations seen as white noise. The noise current PSD of shot noise is

$$S_{\text{i}}(f) = 2\text{q}I, \tag{2.83}$$

where I is the DC current and q is the elementary charge[3]. The amplitude distribution of shot noise is Gaussian. In MOSFETs shot noise occurs at the gate. Hence, I in Equation (2.83) is the gate DC current, which is usually very small.

2.5.2 Noise calculations

If a random process $\text{x}(t)$ with PSD $S_{\text{x}}(f)$ is used as the input of a linear system $H(f)$, then the output $\text{y}(t)$ is also a random process with PSD [16, 17, 20]

$$S_{\text{y}}(f) = |H(f)|^2 S_{\text{x}}(f). \tag{2.84}$$

This is exactly what happens to noise signals that propagate from the noise source to the output of a linear circuit. More specifically, all noise (current) sources within an amplifier cause an output noise voltage PSD given by Equation (2.84) depending on the path from source to output. If all noise current sources are statistically independent, the output noise voltage PSD is equal to the sum of the individual noise contributions at the output [9], i.e.

$$S_{\text{v}}(f) = \sum_{k} S_{\text{i},k}(f). \tag{2.85}$$

The RMS output noise voltage is therefore given by:

$$v_{\text{n,RMS}} = \sqrt{\int_0^\infty S_{\text{v}}(f)\,\mathrm{d}f} \tag{2.86}$$

While this value is relevant for further analysis (e.g. BER), one is often interested in the equivalent IRN. The latter is a fictional quantity that allows to compare the signal of interest to noise at the input, rather than at the output, where the magnitude depends on the gain. It is defined as the input noise signal that results in the same RMS output noise voltage as the one that is actually observed at the output [25]. The IRN current PSD is obtained via the input referral function [25], which, in the case of the accumulated output noise voltage, is the inverse of the transfer function $Z(f)$. As we are dealing with PSDs, the square of

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[3]q $\equiv 1.602\,176\,634 \cdot 10^{-19}\,\text{A s}$

the absolute value has to be used:

$$S_\mathrm{i}(f) = S_\mathrm{v}(f) \left| Z^{-1}(f) \right|^2 \tag{2.87}$$

With that in mind, the RMS IRN current equates to [9, 24, 25]

$$i_\mathrm{n,RMS} = \sqrt{\int_0^\infty \frac{|Z(f)|^2}{|Z(0)|^2} S_\mathrm{i}(f)\,\mathrm{d}f}. \tag{2.88}$$

Note that the absolute value of the normalized transfer function[4] has to be used as a weighting factor within the integral to take into account the bandwidth of the TIA. That being said, if Equations (2.84) and (2.86) are substituted in Equation (2.88), it turns out that

$$i_\mathrm{n,RMS} = \frac{v_\mathrm{n,RMS}}{|Z(0)|}, \tag{2.89}$$

which coincides with the initial definition of IRN RMS current.

2.5.3 Model integration

As mentioned in Section 2.1, noise is conveniently added to an existing DPI/SFG model [18], such as the full 3INV-TIA-C model shown in Figure 2.5. In this particular circuit, the channel noise currents caused by the three MOSFETs in each stage (i_n1, i_n2, i_n3) add to the short circuit current of each stage – see Figure 2.12a. The total output short circuit noise current $i_\mathrm{sc,n}$ is a result of the stage noise currents and adds to the amplifier's output short circuit current $i_\mathrm{sc,c}$. The model for noise calculation in Figure 2.12a neglects the gate-drain capacitances to reduce complexity during analysis at the expense of model accuracy at high frequencies. However, the approach described in this paragraph would also be valid if gate-drain capacitances were included.

In addition to channel noise, there is noise from the feedback resistor R_f. Its noise current $i_\mathrm{n,R}$ adds directly to the input current, but also (with opposite sign) to the output short circuit current of the whole TIA – see Figure 2.12b. The amplifier's output short circuit noise current adds to the overall TIA output short circuit current as well. The SFG models in Figures 2.12a and 2.12b thus allow to compute the transfer functions that are necessary to get the output noise voltage PSDs via Equation (2.84). This derivation is performed in Section 3.3.

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[4]Lowpass behavior of $Z(f)$ is assumed in Equation (2.88). Hence, the transfer function is normalized to the DC gain $Z(0)$. For other transfer functions, the respective mid-band gain must be used; e.g. for bandpass behavior $Z(f)$ is normalized to the gain at the center frequency $Z(f_\mathrm{center})$.
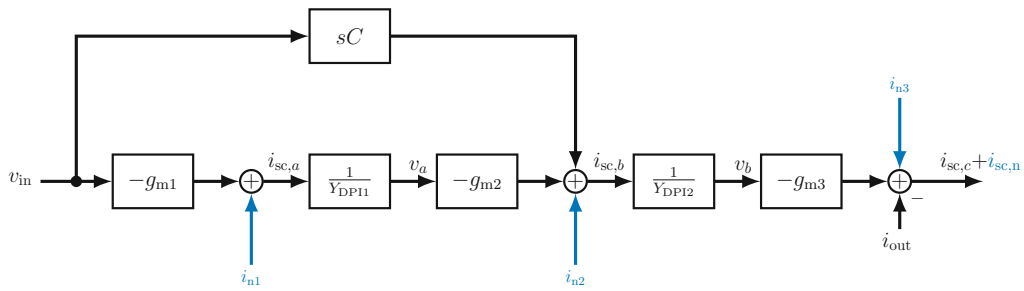
(a) Simplified DPI/SFG model ($C_{\mathrm{gd}} = 0$) of the three-inverter amplifier with noise sources (blue) and total output short circuit noise current.
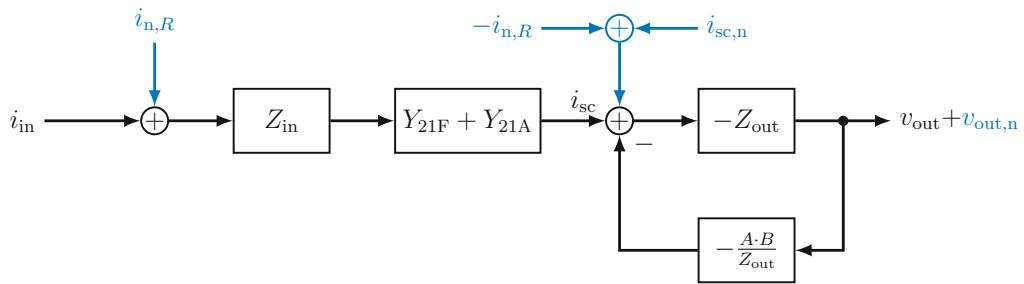
(b) TIA DPI/SFG model with noise sources (blue) and total output noise voltage.

Figure 2.12: Expanded three-inverter TIA DPI/SFG models that include noise sources.

3 Transimpedance amplifier analysis

3.1 Open-loop gain

Given the two-port model of any amplifier, its open-loop gain can be calculated via

$$A_v = -\frac{Y_{21A}}{Y_{22A}}. \tag{3.1}$$

For the fully detailed model of the 3INV-TIA-C (Equations (2.41) to (2.44)), the open-loop gain is therefore given by

$$A_v = \frac{(sC_{\mathrm{gd3}} - g_{\mathrm{m3}})\left[(sC_{\mathrm{gd1}} - g_{\mathrm{m1}})(sC_{\mathrm{gd2}} - g_{\mathrm{m2}}) + sCY_{\mathrm{DPI1}}\right]}{\left[Y_{\mathrm{DPI1}}Y_{\mathrm{DPI2}} - sC_{\mathrm{gd2}}(sC_{\mathrm{gd2}} - g_{\mathrm{m2}})\right]Y_{\mathrm{DPI3}} - Y_{\mathrm{DPI1}}sC_{\mathrm{gd3}}(sC_{\mathrm{gd3}} - g_{\mathrm{m3}})}. \tag{3.2}$$

If C is set to zero in Equation (3.2), the open-loop gain of the 3INV-TIA is obtained – cf. Equations (2.45) to (2.48):

$$A_v = \frac{(sC_{\mathrm{gd1}} - g_{\mathrm{m1}})(sC_{\mathrm{gd2}} - g_{\mathrm{m2}})(sC_{\mathrm{gd3}} - g_{\mathrm{m3}})}{\left[Y_{\mathrm{DPI1}}Y_{\mathrm{DPI2}} - sC_{\mathrm{gd2}}(sC_{\mathrm{gd2}} - g_{\mathrm{m2}})\right]Y_{\mathrm{DPI3}} - Y_{\mathrm{DPI1}}sC_{\mathrm{gd3}}(sC_{\mathrm{gd3}} - g_{\mathrm{m3}})} \tag{3.3}$$

Moreover, the simplified model (Equations (2.49) to (2.52)) can be used to get an approximation of the open-loop gain for the 3INV-TIA-C,

$$A_v = \frac{-g_{\mathrm{m3}}\left[g_{\mathrm{m1}}g_{\mathrm{m2}} + sCY_1\right]}{Y_1(Y_2 + sC)Y_3}, \tag{3.4}$$

as well as for the 3INV-TIA (Equations (2.53) to (2.56)),

$$A_v = \frac{-g_{\mathrm{m1}}g_{\mathrm{m2}}g_{\mathrm{m3}}}{Y_1 Y_2 Y_3}. \tag{3.5}$$

The effect of negative capacitance on open-loop gain can be seen by comparing Equation (3.4) to Equation (3.5). On the one hand, the additional feedback capacitor C adds a frequency-dependent forward path in parallel to g_{m1} and g_{m2}; on the other hand, it also loads the second stage as it adds to Y_2.

The gain of the individual stages is not directly given by the two-port model. However, it follows from Figure 2.5 that

$$v_a = \frac{1}{Y_{\text{DPI1}}} \left[v_b s C_{\text{gd2}} + v_{\text{in}} (s C_{\text{gd1}} - g_{m1}) \right], \tag{3.6}$$

$$v_b = \frac{1}{Y_{\text{DPI2}}} \left[v_a (s C_{\text{gd2}} - g_{m2}) + v_{\text{in}} s C + v_c s C_{\text{gd3}} \right], \tag{3.7}$$

where $v_{\text{out}} = v_c$. Plugging Equation (3.7) into Equation (3.6) and solving for v_a/v_{in} results in the first stage gain

$$A_{v,1} = \frac{v_a}{v_{\text{in}}} = \frac{Y_{\text{DPI2}}(s C_{\text{gd1}} - g_{m1}) + s^2 C_{\text{gd2}} C Y_{\text{DPI1}} + s^2 C_{\text{gd2}} C_{\text{gd3}} A_v}{Y_{\text{DPI1}} Y_{\text{DPI2}} - s C_{\text{gd2}}(s C_{\text{gd2}} - g_{m2})}. \tag{3.8}$$

Note that $A_v = v_{\text{out}}/v_{\text{in}}$. Now v_b/v_{in} can be derived from Equation (3.7) as follows:

$$A_{v,12} = \frac{v_b}{v_{\text{in}}} = \frac{A_{v,1}(s C_{\text{gd2}} - g_{m2}) + s C + s C_{\text{gd3}} A_v}{Y_{\text{DPI2}}} \tag{3.9}$$

Therefore, the second stage gain is given by

$$A_{v,2} = \frac{A_{v,12}}{A_{v,1}}, \tag{3.10}$$

and the third stage gain follows from Equations (3.2) and (3.9) as

$$A_{v,3} = \frac{A_v}{A_{v,12}}. \tag{3.11}$$

3.2 Stability

3.2.1 Closed-loop stability

At first, stability is analyzed via the basic shunt-feedback TIA circuit – see Figure 2.1a in Section 2.2. Equation (2.4) – reprinted here as Equation (3.12) – shows that there is a single pole that depends on R_{f}, C_{f} (in particular the Miller capacitance $-A_0 C_{\text{f}}$), $\tilde{C}_T$ and

A_0. Substitution of $\tilde{C}_T$ (Equation (2.6)) into Equation (3.12) shows that the system's pole is

$$H(s) = \frac{R_\mathrm{f}}{1 - s\frac{R_\mathrm{f}(\tilde{C}_T - A_0 C_\mathrm{f})}{A_0}} = \frac{R_\mathrm{f}}{1 - \frac{s}{\omega_p}} \tag{3.12}$$

$$\omega_p = \frac{A_0}{R_\mathrm{f}(C_\mathrm{PD} + C_I - CA_C - C_\mathrm{f}A_0)}. \tag{3.13}$$

As long as $\omega_p \leq 0$, the system is stable, but as soon as $\omega_p > 0$, the system is unstable. Note that if $C = 0$, ω_p can never become positive ($A_0 < 0$), hence the system is always stable; whereas $\omega_p > 0$ is possible if $C \neq 0$. Therefore, the condition for stability is given by

$$C_\mathrm{PD} + C_I - CA_C - C_\mathrm{f}A_0 \geq 0. \tag{3.14}$$

In other words, the total input capacitance including Miller effect must not become negative. Equation (3.14) can be rearranged to get a hard limit for the internal feedback capacitor C, i.e.

$$C < \frac{C_\mathrm{PD} + C_I - C_\mathrm{f}A_0}{A_C} = \frac{C_T - C_\mathrm{f}A_0}{A_C}. \tag{3.15}$$

For example, for $C_\mathrm{f} = 30\,\mathrm{fF}$, $C_\mathrm{PD} = 7\,\mathrm{pF}$, $C_I = 1\,\mathrm{pF}$, $A_0 = -316$ and $A_C = 84.4$ (cf. Table 4.1 and Figure 4.1), the limit is given by $C < 207\,\mathrm{fF}$.

3.2.2 Loop gain stability

Equation (3.15) already provides valuable information about the stability limit of the negative capacitance concept in general. Nevertheless, the three-stage implementation is examined next to obtain detailed insight. Therefor, the first-order model from Section 2.3.1 is applied. To simplify the analysis, the time constant $\tau = R_2 C$ is defined. Simulations and the numerical analysis indicated that the loop gain AB becomes unstable before the stability limit is reached – cf. Section 3.2.3 and chapter 4. AB is approximated by

$$AB \approx -Z_\mathrm{in}Z_\mathrm{out}Y_\mathrm{21A}Y_\mathrm{12F} = \frac{N_{AB}}{D_{AB}} =$$
$$= \frac{A_3(A_1 A_2 + s\tau)(G_\mathrm{f} + sC_\mathrm{f})}{[(G_\mathrm{f} + sC_\mathrm{f} + sC_T)(1 + s\tau) + sC(1 - A_1 A_2)][1 + R_3 G_\mathrm{f} + sR_3(C_\mathrm{f} + C_\mathrm{load})]} \tag{3.16}$$

if the amplifier's forward gain is much larger than the feedback networks forward gain $|Y_\mathrm{21A}| \gg |Y_\mathrm{21F}|$, and if the amplifier's backward gain is much smaller than the feedback network's backward gain $|Y_\mathrm{12A}| \ll |Y_\mathrm{12F}|$. This is a reasonable assumption for practical implementations of amplifiers and feedback networks, due to their intended use (forward amplification and feedback). The loop gain is unstable if its denominator D_{AB} has right half-plane zeros, or equivalently, if D_{AB} is not a Hurwitz polynomial. The latter condition

is now assessed via the Hurwitz criterion. D_{AB} is a third-order polynomial,

$$D_{AB} = a_0 + a_1 s + a_2 s^2 + a_3 s^3, \tag{3.17}$$

with coefficients (cf. Equation (3.16))

$$a_0 = G_{\mathrm{f}}(1 + R_3 G_{\mathrm{f}}), \tag{3.18}$$

$$a_1 = C_{\mathrm{f}}(1 + 2R_3 G_{\mathrm{f}}) + R_3 G_{\mathrm{f}} C_{\mathrm{load}} + (1 + R_3 G_{\mathrm{f}})(G_{\mathrm{f}}\tau + \tilde{C}_T), \tag{3.19}$$

$$a_2 = C_{\mathrm{f}}^2 R_3 + C_{\mathrm{f}}\left[(1 + 2R_3 G_{\mathrm{f}})\tau + R_3(\tilde{C}_T + C_{\mathrm{load}})\right] +$$
$$+ R_3 G_{\mathrm{f}}(C_T + C_{\mathrm{load}})\tau + C_T\tau + R_3 C_{\mathrm{load}}\tilde{C}_T, \tag{3.20}$$

$$a_3 = (C_{\mathrm{f}} + C_T)\tau R_3(C_{\mathrm{load}} + C_{\mathrm{f}}). \tag{3.21}$$

$a_i > 0$ for all $i \in \{0, 1, 2, 3\}$ is a necessary condition for the stability of AB. While a_3 is always positive, regardless of the choice of C, coefficient a_0 is only positive and non-zero if

$$G_{\mathrm{f}} > 0. \tag{3.22}$$

Since $R_3 G_{\mathrm{f}} > 0$ if Equation (3.22) is true, a relation for the second coefficient a_1 is found:

$$a_1 > C_{\mathrm{f}} + G_{\mathrm{f}}\tau + \tilde{C}_T = \tilde{a}_1 \tag{3.23}$$

Therefore, $a_1 > 0$ as soon as $\tilde{a}_1 > 0$. If we further assume fairly large R_{f}, i.e. $1/G_{\mathrm{f}} \gg R_2$, and $|A_1 A_2| \gg 1$, then

$$\tilde{a}_1 \approx C_{\mathrm{f}} - A_1 A_2 C + C_T. \tag{3.24}$$

As a consequence, $a_1 > \tilde{a}_1 > 0$ if

$$C < \frac{C_{\mathrm{f}} + C_T}{A_1 A_2}. \tag{3.25}$$

Due to the simplifications made, Equation (3.25) is also generally applicable to the idealized model from Section 2.2, although it stems from a particular TIA implementation. Likewise, assuming $1/G_{\mathrm{f}} \gg R_3$, the condition for $a_2 > 0$ is given by

$$C > \frac{R_3(C_{\mathrm{f}} + C_T)(C_{\mathrm{f}} + C_{\mathrm{load}})}{R_3 A_1 A_2 (C_{\mathrm{f}} + C_{\mathrm{load}}) - R_2(C_{\mathrm{f}} + C_T)} \tag{3.26}$$

if the denominator is negative. Otherwise, the greater-than sign must be changed to a smaller-than sign.

Using the same values as before[1] we find the stability limit of AB to be $C < 95.1\,\mathrm{fF}$ according to Equation (3.25), which is significantly lower than the limit for overall circuit

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[1] $C_{\mathrm{f}} = 30\,\mathrm{fF}$, $C_{\mathrm{PD}} = 7\,\mathrm{pF}$, $C_I = 1\,\mathrm{pF}$, and $A_C = A_1 A_2 = 84.4$
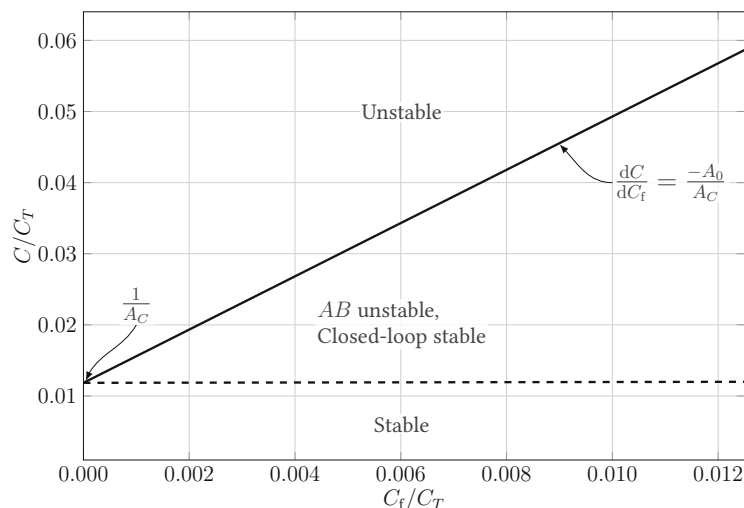
Figure 3.1: Permissible values of C for loop gain and closed-loop stability for $A_C = 84.4$ and $A_0 = -316$. The dashed line marks the transition from stable to unstable loop gain (Equation (3.25)), whereas the closed-loop system is still stable in this area. The solid line marks the closed-loop stability limit (Equation (3.15)).

stability derived previously. If it is further assumed that $R_2 = R_3 = 2\,\text{k}\Omega$, Equation (3.26) yields $C > -1665\,\text{fF}$. Hence it provides no useful information in this particular case. Note that all these conditions are necessary, but not sufficient for the stability of AB. However, they are sufficient for judging instability.

Equations (3.15) and (3.25) are illustrated in Figure 3.1. Both, C and C_f are normalized to C_T. It is evident that C_f has only marginal influence on the loop gain stability limit in the depicted range of values. On the other hand, the absolute stability limit of the closed-loop system increases by a factor of five over the same interval.

3.2.3 Numerical analysis

In principle the Hurwitz criterion can be applied to any open- or closed-loop transfer function of any model from Chapter 2. However, the complexity of the detailed models does not permit analysis by hand. Even if a computer algebra system (CAS) capable of full symbolic analysis was used, the key properties would most likely be overlooked due to the sheer amount of terms. Thus, part of the stability analysis was done numerically using MATLAB and the circuit parameters from the simulated design – see Table 4.1.

It was previously shown that the loop gain may become unstable for much smaller values of negative capacitance than the predicted absolute stability limit. More specifically, simulation and the numerical analysis led to the examination of loop gain stability, which resulted in Equation (3.25). Figures 3.2 and 3.3 show a numerical evaluation of the poles of the loop gain $AB(s)$ and transimpedance $Z(s)$, respectively. The poles are computed from the detailed model with ideal R_f, Equations (2.41) to (2.44). R_f and C_f are set to
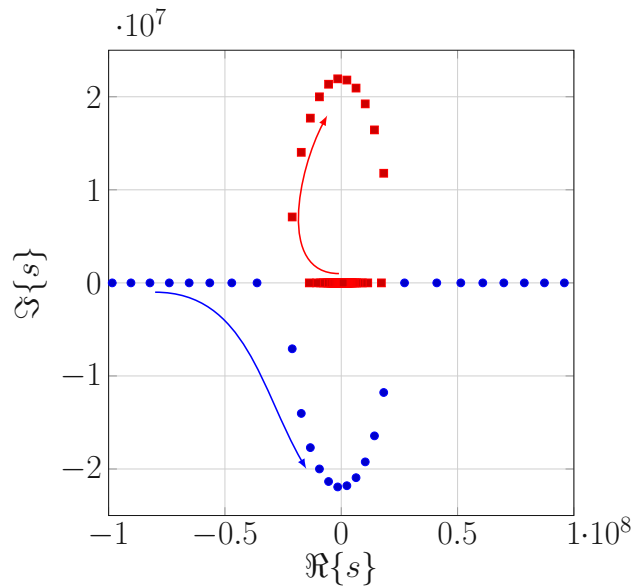
Figure 3.2: Numerical evaluation of the poles of loop gain AB for increasing negative capacitance, $C = [20\,\mathrm{fF}, 210\,\mathrm{fF}]$. The arrows indicate the direction of increasing C. Four additional real-valued poles reside in the left half-plane outside of the chosen axis limits. $R_\mathrm{f} = 150\,\mathrm{k\Omega}$ and $C_\mathrm{f} = 30\,\mathrm{fF}$ are constant.
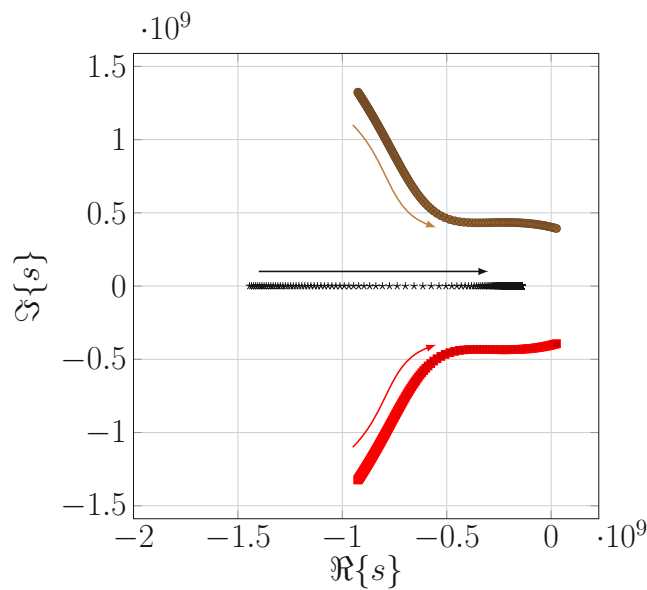
Figure 3.3: Numerical evaluation of the poles of the transimpedance $Z(s)$ for increasing negative capacitance, $C = [20\,\mathrm{fF}, 210\,\mathrm{fF}]$. The arrows indicate the direction of increasing C. One additional real-valued pole resides in the left half-plane outside of the chosen axis limits. $R_\mathrm{f} = 150\,\mathrm{k\Omega}$ and $C_\mathrm{f} = 30\,\mathrm{fF}$ are constant.

constant values. Figure 3.2 indicates that the first (red) and second (blue) pole of AB are real-valued and negative for small negative capacitance and move towards each other, until they split to become a conjugate complex pair. Their absolute value increases further as they move towards the imaginary axis. At $C \approx 112\,\text{fF}$ the pole pair crosses the imaginary axis, rendering $AB(s)$ unstable. For larger C, the poles move towards the real axis and eventually become real-valued, but remain in the right half-plane. Figure 3.3 shows the progression of the poles of $Z(s)$ over the same interval of C. The first (brown) and second (red) pole is a conjugate complex pair, whereas the third (black) and fourth (not shown) pole are real-valued and remain in the left half-plane. Hence, only the first and second pole are of interest. For increasing negative capacitance, the magnitude of the imaginary parts of the conjugate complex pair decreases until the turning point. At this point, $C \approx 112\,\text{fF}$ and the loop gain becomes unstable. However, as Figure 3.3 shows, the overall transimpedance $Z(s)$ remains stable, since all poles are in the left half-plane. Even for larger values than $112\,\text{fF}$, $Z(s)$ is stable. Nevertheless, the pole pair crosses the imaginary axis at $C \approx 200\,\text{fF}$. From there on, $Z(s)$ is unstable.

With this in mind, two findings are noted:

1. The theoretical limits for loop gain stability, Equation (3.25), and TIA stability, Equation (3.15), provide a reasonable approximation for the stability limits observed in the numerical analysis. That is, Equation (3.25) predicts $95\,\text{fF}$ for this specific design, whereas the numerical limit is $112\,\text{fF}$; and Equation (3.15) predicts $207\,\text{fF}$, whereas the numerical limit is $200\,\text{fF}$. The differences are attributed to the choice of R_f, which does not appear in the formulas, although further numerical analyses indicated that it impacts the stability limits by up to $\pm 20\,\text{fF}$ (for the given design).

2. Negative capacitance applications can result in a state where the loop gain AB is unstable while the overall transfer function is stable. If this is the case, the common phase margin criterion does not hold. Thus, the general Nyquist criterion (or equivalent criteria) must be applied – cf. Appendix A.2. Figure 3.4 shows the Nyquist plot (locus) of AB for $C = 70\,\text{fF}$, $C = 120\,\text{fF}$ and $C = 205\,\text{fF}$. For $C = 70\,\text{fF}$ no poles of AB reside in the right half-plane or on the imaginary axis. Thus, the Nyquist criterion requires a continuous phase change of $\Delta\varphi = 0$ for the vector that starts at $(-1, 0\text{j})$ and tracks the locus of AB. As Figure 3.4 shows, the total phase change of this vector is indeed 0, hence the transimpedance is stable. On the other hand, for $C = 120\,\text{fF}$ we require $\Delta\varphi = 2\pi$. Figure 3.4 shows that this is also the case, because the locus encircles $(-1, 0\text{j})$ counter-clockwise. Thus, the transimpedance is stable, although AB is unstable. However, at $C = 205\,\text{fF}$ the phase change requirement is still $\Delta\varphi = 2\pi$, but the locus ever so slightly fails to encircle $(-1, 0\text{j})$. Hence, the total phase change is 0, rendering the transimpedance unstable.
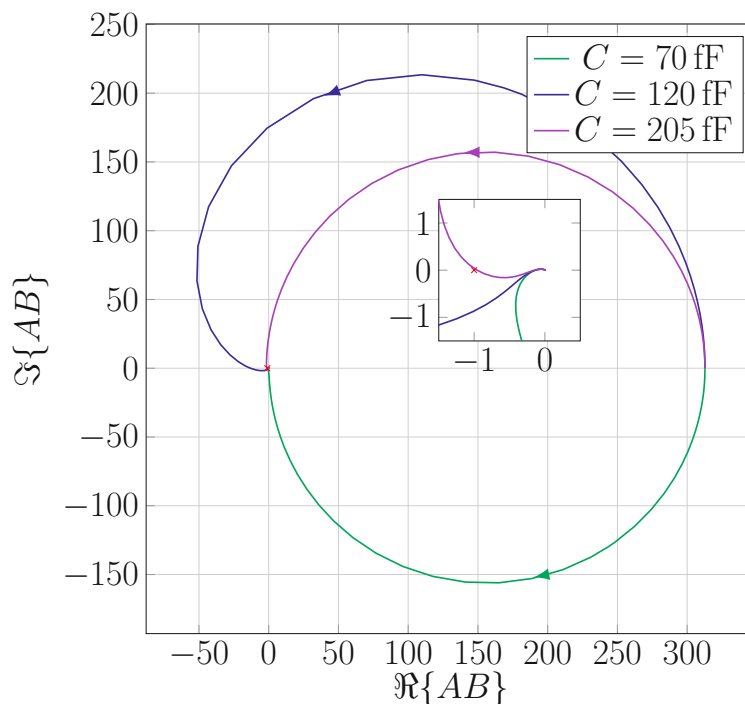
Figure 3.4: Nyquist plot of the loop gain AB for three different values of C. The inset shows a magnified version of the plot around $(-1, 0\mathrm{j})$.

3.3 Noise

3.3.1 Output noise

The first step in this noise analysis is to find the transfer functions between all the noise sources and the output of the 3INV-TIA-C. It is evident from the noise SFG model in Figure 2.12a that the output short circuit noise current of the amplifier is composed of the following terms:

$$i_{\mathrm{sc,n}} = \frac{g_{\mathrm{m2}}g_{\mathrm{m3}}}{Y_{\mathrm{DPI1}}Y_{\mathrm{DPI2}}} i_{\mathrm{n1}} - \frac{g_{\mathrm{m3}}}{Y_{\mathrm{DPI2}}} i_{\mathrm{n2}} + i_{\mathrm{n3}} \qquad (3.27)$$

Furthermore, the total output noise voltage of the complete TIA follows from the SFG in Figure 2.12b and is given by

$$v_{\mathrm{out,n}} = \left[i_{\mathrm{sc,n}} + i_{R,\mathrm{n}} \left(1 - Z_{\mathrm{in}}(Y_{\mathrm{21A}} + Y_{\mathrm{21F}}) \right) \right] \frac{-Z_{\mathrm{out}}}{1 + AB}. \qquad (3.28)$$

Equations (3.27) and (3.28) contain the complete transfer functions. Thus – if we denote the individual PSDs of i_{n1}, i_{n2}, i_{n3} and $i_{\mathrm{n}R}$ by $S_{\mathrm{i1}}(f)$, $S_{\mathrm{i2}}(f)$, $S_{\mathrm{i3}}(f)$ and $S_{iR}(f)$, respectively –

the total output noise voltage PSD is

$$S_{\mathrm{v}}(f) = \left[\left| \frac{g_{\mathrm{m2}}g_{\mathrm{m3}}}{Y_{\mathrm{DPI1}}Y_{\mathrm{DPI2}}} \right|^2 S_{\mathrm{i1}}(f) + \left| \frac{g_{\mathrm{m3}}}{Y_{\mathrm{DPI2}}} \right|^2 S_{\mathrm{i2}}(f) + S_{\mathrm{i3}}(f) + \right.$$

$$\left. + S_{\mathrm{iR}}(f) \left| 1 - Z_{\mathrm{in}}(Y_{\mathrm{21A}} + Y_{\mathrm{21F}}) \right|^2 \right] \left| \frac{Z_{\mathrm{out}}}{1 + AB} \right|^2. \tag{3.29}$$

This result is directly applicable for numerical analysis, but is not simplified further for symbolic analysis at this point.

What remains is to specify the respective noise current PSDs. MOSFET channel noise in each stage is modeled via the SPICE2 formulas, Equations (2.80) and (2.82), where L_{eff} is approximated by the total channel length L. Shot noise is neglected, based on the assumption of small DC gate current. The body effect does not occur in the circuit from Figure 2.2. Resistor noise is modeled by Equation (2.78). Consequently, the noise current PSD of each stage k is given by

$$S_{\mathrm{i}k}(f) = 4\mathrm{k_B}T\frac{2}{3}\left(g_{\mathrm{m}k} + g_{\mathrm{ds}k} + g_{\mathrm{md}k} + g_{\mathrm{dsd}k}\right) +$$

$$+ K_{\mathrm{n}k}\frac{I_{\mathrm{Dn}k}^{a_{\mathrm{n}k}}}{C_{\mathrm{ox}}L_{\mathrm{eff},\mathrm{n}k}^2 f^{b_{\mathrm{n}k}}} + K_{\mathrm{p}k}\frac{I_{\mathrm{Dp}k}^{a_{\mathrm{p}k}}}{C_{\mathrm{ox}}L_{\mathrm{eff},\mathrm{p}k}^2 f^{b_{\mathrm{p}k}}} + K_{\mathrm{d}k}\frac{I_{\mathrm{Dd}k}^{a_{\mathrm{d}k}}}{C_{\mathrm{ox}}L_{\mathrm{eff},\mathrm{d}k}^2 f^{b_{\mathrm{d}k}}}, \tag{3.30}$$

where $g_{\mathrm{m}k}$ is given by Equation (2.29), $g_{\mathrm{ds}k}$ is given by Equation (2.30) and $g_{\mathrm{md}k}$, as well as $g_{\mathrm{dsd}k}$ stem from the diode connected transistor in each stage. Assuming that all transistors have the same channel length L, the flicker noise in Equation (3.30) is simplified into

$$K_k\frac{I_{\mathrm{Dn}k}^{a_{\mathrm{n}k}}}{C_{\mathrm{ox}}L^2 f^{b_{\mathrm{n}k}}} = K_k\frac{I_k^{a_k}}{C_{\mathrm{ox}}L^2 f^{b_k}}, \tag{3.31}$$

where

$$K_k = K_{\mathrm{n}k} + K_{\mathrm{p}k}\frac{I_{\mathrm{Dp}k}^{a_{\mathrm{p}k}}}{I_{\mathrm{Dn}k}^{a_{\mathrm{n}k}}}f^{b_{\mathrm{n}k}-b_{\mathrm{p}k}} + K_{\mathrm{d}k}\frac{I_{\mathrm{Dd}k}^{a_{\mathrm{d}k}}}{I_{\mathrm{Dn}k}^{a_{\mathrm{n}k}}}f^{b_{\mathrm{n}k}-b_{\mathrm{d}k}}. \tag{3.32}$$

Furthermore, the conductances of each stage are summarized into

$$g_k = g_{\mathrm{m}k} + g_{\mathrm{ds}k} + g_{\mathrm{md}k} + g_{\mathrm{dsd}k}. \tag{3.33}$$

Therefore, the final PSDs are:

$$S_{i1}(f) = 4k_B T \frac{2}{3} g_1 + K_1 \frac{I_1^{a_1}}{C_{ox} L^2 f^{b_1}} \tag{3.34}$$

$$S_{i2}(f) = 4k_B T \frac{2}{3} g_2 + K_2 \frac{I_2^{a_2}}{C_{ox} L^2 f^{b_2}} \tag{3.35}$$

$$S_{i3}(f) = 4k_B T \frac{2}{3} g_3 + K_3 \frac{I_3^{a_3}}{C_{ox} L^2 f^{b_3}} \tag{3.36}$$

$$S_{iR}(f) = 4k_B T \frac{1}{R_f} \tag{3.37}$$

3.3.2 Input referred noise

As discussed in Section 2.5.2, Equation (2.87) defines the IRN current PSD as the output noise voltage PSD divided by the absolute value of the complete transfer function squared. Therefore, the transimpedance $Z(f)$ is specified first[2] – cf. Equation (2.72):

$$Z(f) = -\frac{Z_{in} Z_{out} (Y_{21A} + Y_{21F})}{1 + AB} \tag{3.38}$$

Equation (3.38) is further substituted into Equation (2.87) resulting in

$$S_i(f) = \frac{S_v(f)}{|Z(f)|^2} = \tag{3.39}$$

$$= \left[\left| \frac{g_{m2} g_{m3}}{Y_{DPI1} Y_{DPI2}} \right|^2 S_{i1}(f) + \left| \frac{g_{m3}}{Y_{DPI2}} \right|^2 S_{i2}(f) + S_{i3}(f) + \right.$$

$$\left. + S_{iR}(f) \left| 1 - Z_{in}(Y_{21A} + Y_{21F}) \right|^2 \right] \frac{1}{|Z_{in}(Y_{21A} + Y_{21F})|^2} \tag{3.40}$$

At this point, further assumptions are necessary to simplify and generalize Equation (3.40). Firstly, we assume that the noise contribution of the front-end, i.e. the first stage in the 3INV-TIA-C, is significantly larger than the noise of subsequent stages. This assumption is reasonable, because $S_{i1}(f)$ is amplified much more than $S_{i2}(f)$ and $S_{i3}(f)$, as it passes through stage two and three – see Equation (3.29). Secondly, we surmise that $|Z_{in}(Y_{21A} + Y_{21F})| \gg 1$, since it contains the forward transadmittance Y_{21A} of the amplifier. Moreover, Y_{21F} is neglected as it is usually much smaller than Y_{21A}. Applying these assumptions gives the following approximation for $S_i(f)$:

$$S_i(f) \approx \left| \frac{g_{m2} g_{m3}}{Y_{DPI1} Y_{DPI2} Z_{in} Y_{21A}} \right|^2 S_{i1}(f) + S_{iR}(f) = |\Theta|^2 S_{i1}(f) + S_{iR}(f) \tag{3.41}$$

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[2]For all following calculations we define $s = 2\pi f \mathrm{j}$.

Substituting the two-port model Equations (2.49) to (2.52) (all $C_{\text{gd}} = 0$) into the factor of $S_{\text{i}1}(f)$ in Equation (3.41) yields

$$\Theta = \frac{g_{\text{m}2}g_{\text{m}3}}{Y_{\text{DPI1}}Y_{\text{DPI2}}Z_{\text{in}}Y_{21\text{A}}} = g_{\text{m}2}\frac{G_{\text{f}} + s(C_{\text{f}} + C_T + C)}{g_{\text{m}1}g_{\text{m}2} + sCY_1} - \frac{g_{\text{m}2}sC}{Y_1(Y_2 + sC)}. \tag{3.42}$$

Evaluating Equations (3.8) to (3.10) for $C_{\text{gd}} = 0$ gives the open-loop gains

$$A_1(s) = -\frac{g_{\text{m}1}}{Y_1}, \tag{3.43}$$

$$A_2(s) = -\frac{g_{\text{m}2} + \frac{sC}{A_1(s)}}{Y_2 + sC} \approx -\frac{g_{\text{m}2}}{Y_2 + sC}, \tag{3.44}$$

where the approximation assumes that $|g_{\text{m}2}A_1(s)| \gg |sC|$. If we further assume that $|sCY_1| \ll g_{\text{m}1}g_{\text{m}2}$, based on the premise that the transconductances $g_{\text{m}1}$ and $g_{\text{m}2}$ are large and C is reasonably small, the factor Θ becomes

$$\Theta \approx \frac{1 + sR_{\text{f}}[C_{\text{f}} + C_T + C(1 - A_1(s)A_2(s))]}{R_{\text{f}}g_{\text{m}1}} = \frac{1 + sR_{\text{f}}(C_{\text{f}} + \tilde{C}_T(s))}{R_{\text{f}}g_{\text{m}1}}. \tag{3.45}$$

Substituting $s = \text{j}2\pi f$ into Equation (3.45) and subsequently inserting Equations (3.34), (3.37) and (3.45) into Equation (3.41) we get

$$S_{\text{i}}(f) \approx \frac{|1 + \text{j}2\pi f R_{\text{f}}(C_{\text{f}} + \tilde{C}_T(f))|^2}{R_{\text{f}}^2 g_{\text{m}1}^2}S_{\text{i}1}(f) + S_{\text{iR}}(f) = \tag{3.46}$$

$$= \frac{|1 + \text{j}2\pi f R_{\text{f}}(C_{\text{f}} + \tilde{C}_T(f))|^2}{R_{\text{f}}^2 g_{\text{m}1}^2}\left[4\text{k}_\text{B}T\frac{2}{3}g_1 + K_1\frac{I_1^{a_1}}{C_{\text{ox}}L^2 f^{b_1}}\right] + 4\text{k}_\text{B}T\frac{1}{R_{\text{f}}}. \tag{3.47}$$

Equation (3.47) is the input noise current PSD for shunt-feedback TIAs with negative capacitance (cf. Figure 2.1a), whose noise is dominated by the FET front-end and feedback resistor R_{f}.

Still, further simplifications can be applied. Assuming $|sC| \ll |Y_2|$ and neglecting other capacitances at the stage outputs $Y_i \approx 1/R_i$, the stage gains take on their DC values $A_i \approx -g_{\text{m}i}R_i$. In addition, it is reasonable to assume $g_{\text{m}1}R_{\text{f}} \gg 1$ [25]. With this in mind, Θ becomes

$$\Theta \approx \frac{s(C_{\text{f}} + \tilde{C}_T)}{g_{\text{m}1}}. \tag{3.48}$$

In analogy to before, we substitute $s = \text{j}2\pi f$ in Equation (3.48) and subsequently insert

Equations (3.34), (3.37) and (3.48) into Equation (3.41), which leads to

$$S_{\mathrm{i}}(f) \approx \frac{[2\pi f(C_{\mathrm{f}} + \tilde{C}_T)]^2}{g_{\mathrm{m1}}^2} S_{\mathrm{i1}}(f) + S_{\mathrm{iR}}(f) = \tag{3.49}$$

$$= \frac{[2\pi f(C_{\mathrm{f}} + \tilde{C}_T)]^2}{g_{\mathrm{m1}}^2} \left[4k_{\mathrm{B}}T\frac{2}{3}g_1 + K_1 \frac{I_1^{a_1}}{C_{\mathrm{ox}}L^2 f^{b_1}} \right] + 4k_{\mathrm{B}}T\frac{1}{R_{\mathrm{f}}}. \tag{3.50}$$

It is interesting how closely Equation (3.50) resembles the noise approximation of normal TIAs (without negative capacitance) with FET front-end, which is given by [24]

$$S_{\mathrm{i,FET}}(f) = \frac{4k_{\mathrm{B}}T}{R_{\mathrm{f}}} + \frac{(2\pi f)^2 C_T^2}{g_{\mathrm{m}}} 4k_{\mathrm{B}}T\Gamma, \tag{3.51}$$

where $C_{\mathrm{f}} = 0$, flicker noise is ignored and the thermal channel noise is expressed via the excess noise factor Γ. The main difference between Equations (3.50) and (3.51) – i.e. between TIAs with and without negative capacitance – is that C_T is modified to include the negative capacitance $-A_1 A_2 C$, resulting in $\tilde{C}_T$.

3.3.3 Noise optimum

Noise optima based on different constraints exist [24] and provide guidance for low noise TIA design. In this work, the optimal C for best noise performance at constant bandwidth is of great interest. The constant bandwidth constraint is derived from Equations (2.4) and (3.13) as

$$R_{\mathrm{f}}(C) = \frac{[R_{\mathrm{f}}]_{C=0}(C_T - A_0 C_{\mathrm{f}})}{C_T - A_C C - A_0 C_{\mathrm{f}}} = [R_{\mathrm{f}}]_{C=0} \frac{C_T - A_0 C_{\mathrm{f}}}{\tilde{C}_T - A_0 C_{\mathrm{f}}}, \tag{3.52}$$

where A_0 and A_C are the open-loop DC gains of the complete amplifier and across C, respectively. $[R_{\mathrm{f}}]_{C=0}$ is the feedback resistance at $C = 0$. For the following calculation, the flicker noise component is ignored, in analogy to [24]. Inserting Equation (3.52) into Equation (3.50), and Equation (3.50) into Equation (2.88) (squared) yields:

$$i_{\mathrm{n}}^2 = \int_0^\infty \frac{|Z(f)|^2}{|Z(0)|^2} \left[\frac{[2\pi f(C_{\mathrm{f}} + \tilde{C}_T)]^2}{g_{\mathrm{m1}}^2} 4k_{\mathrm{B}}T\frac{2}{3}g_1 + 4k_{\mathrm{B}}T\frac{\tilde{C}_T - A_0 C_{\mathrm{f}}}{[R_{\mathrm{f}}]_{C=0}(C_T - A_0 C_{\mathrm{f}})} \right] \mathrm{d}f = \tag{3.53}$$

$$= \frac{[2\pi(C_{\mathrm{f}} + \tilde{C}_T)]^2}{g_{\mathrm{m1}}^2} 4k_{\mathrm{B}}T\frac{2}{3}g_1 \int_0^\infty \frac{|Z(f)|^2}{|Z(0)|^2} f^2 \mathrm{d}f +$$

$$+ 4k_{\mathrm{B}}T\frac{\tilde{C}_T - A_0 C_{\mathrm{f}}}{[R_{\mathrm{f}}]_{C=0}(C_T - A_0 C_{\mathrm{f}})} \int_0^\infty \frac{|Z(f)|^2}{|Z(0)|^2} \mathrm{d}f \tag{3.54}$$

The two integrals define the noise bandwidths $\mathrm{BW}_{\mathrm{n2}}^3$ and BW_{n}, respectively [24]. Therefore, Equation (3.54) can be written as

$$i_{\mathrm{n}}^2 = \frac{[2\pi(C_{\mathrm{f}} + \tilde{C}_T)]^2}{g_{\mathrm{m1}}^2} 4k_{\mathrm{B}}T\frac{2}{9}g_1 \mathrm{BW}_{\mathrm{n2}}^3 + 4k_{\mathrm{B}}T\frac{\tilde{C}_T - A_0 C_{\mathrm{f}}}{[R_{\mathrm{f}}]_{C=0}(C_T - A_0 C_{\mathrm{f}})}\mathrm{BW}_{\mathrm{n}} = \tag{3.55}$$

$$= \xi_0(C_T - A_C C - A_0 C_{\mathrm{f}}) + \xi_2(C_{\mathrm{f}} + C_T - A_C C)^2. \tag{3.56}$$

Strictly speaking, the noise bandwidths depend on the shape of $Z(f)$, and thus on C. However, based on the simple transfer function from Equation (2.4) and the constant bandwidth constraint ($\partial\omega_p/\partial C = 0$) we assume that they are approximately constant in the following derivation. Differentiating Equation (3.56) with respect to C, setting the derivative to zero and solving for C yields the following optimum for C:

$$C_{\mathrm{opt}} = \frac{C_{\mathrm{f}} + C_T}{A_C} + \frac{\xi_0}{2\xi_2 A_C} = \tag{3.57}$$

$$= \frac{C_{\mathrm{f}} + C_T}{A_C} + \frac{9g_{\mathrm{m1}}^2}{8\pi^2 A_C[R_{\mathrm{f}}]_{C=0}g_1(C_T - A_0 C_{\mathrm{f}})}\frac{\mathrm{BW}_{\mathrm{n}}}{\mathrm{BW}_{\mathrm{n2}}^3} \tag{3.58}$$

Values of BW_{n} and $\mathrm{BW}_{\mathrm{n2}}$ for typical transfer functions are listed in [25]. For a first-order lowpass transfer function $\mathrm{BW}_{\mathrm{n2}}^3 = \infty$, thus the second term in Equation (3.58) is zero. On the other hand, for a second-order lowpass $\mathrm{BW}_{\mathrm{n}}/\mathrm{BW}_{\mathrm{n2}}^3 \approx 1/(3f_{3\,\mathrm{dB}}^2)$; therefore the second term is also very small in this case. For this reason, we will ignore this second term – and therefore also the constant bandwidth constraint with regards to resistor thermal noise – rendering the optimal capacitance

$$C_{\mathrm{opt}} = \frac{C_{\mathrm{f}} + C_T}{A_C}. \tag{3.59}$$

This is a remarkable result considering that it is the exact point where the loop gain of a TIA with negative capacitance becomes unstable – cf. Section 3.2.2, Equation (3.25). However, let us examine the input noise current PSD, Equation (3.50), at this optimum. Substitution of C in Equation (3.50) by Equation (3.59) yields

$$S_{\mathrm{i,opt}}(f) = 4k_{\mathrm{B}}T\frac{1}{R_{\mathrm{f}}}. \tag{3.60}$$

It turns out that the noise contribution of the front-end channel[3] completely vanishes. Although this result is desirable, it seems unlikely to be able to suppress the channel noise altogether.

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[3]More specifically, for the given simplifications, the factor of the second stage and third stage channel noise also vanishes. However, the derivation is not included in this work, as the front-end noise dominates.

4 SIMULATION RESULTS AND COMPARISON

Simulations were conducted in Cadence Virtuoso for a $0.35\,\mu\text{m}$ BiCMOS process using an existing three-inverter TIA design [6] that was modified to include C for negative capacitance at the input node – cf. Figure 2.2. Table 4.1 shows the extracted device parameters at the DC operating point. The load capacitance for all simulations is $C_{\text{load}} = 60\,\text{fF}$, whereas the feedback capacitance is $C_{\text{f}} = 30\,\text{fF}$. R_{f} was set based on the desired bandwidth, where two different bit rates were targeted: $14\,\text{Mbit/s}$ ($10\,\text{MHz}$ bandwidth) and $100\,\text{Mbit/s}$ ($70\,\text{MHz}$ bandwidth).

The purpose of these simulations is to verify the models and the derived analytical relationships. Furthermore, simulation aided the process of finding said relationships.

Table 4.1: Extracted device parameters of the CMOS three-inverter amplifier at its DC operating point.

| First stage		Second stage		Third stage	
Parameter	Value	Parameter	Value	Parameter	Value
g_{m1}	$14\,052.0\,\mu\text{S}$	g_{m2}	$1893.4\,\mu\text{S}$	g_{m3}	$1893.4\,\mu\text{S}$
$g_{\text{m,D1}}$	$480.4\,\mu\text{S}$	$g_{\text{m,D2}}$	$480.4\,\mu\text{S}$	$g_{\text{m,D3}}$	$480.2\,\mu\text{S}$
g_{ds1}	$139.81\,\mu\text{S}$	g_{ds2}	$17.57\,\mu\text{S}$	g_{ds3}	$17.57\,\mu\text{S}$
$g_{\text{ds,D1}}$	$5.97\,\mu\text{S}$	$g_{\text{ds,D2}}$	$5.97\,\mu\text{S}$	$g_{\text{ds,D3}}$	$5.97\,\mu\text{S}$
C_{j1}	$272.06\,\text{fF}$	C_{j2}	$37.57\,\text{fF}$	C_{j3}	$34.26\,\text{fF}$
$C_{\text{j,D1}}$	$13.94\,\text{fF}$	$C_{\text{j,D2}}$	$13.94\,\text{fF}$	$C_{\text{j,D3}}$	$13.94\,\text{fF}$
C_{gs1}	$967.00\,\text{fF}$	C_{gs2}	$117.99\,\text{fF}$	C_{gs3}	$117.99\,\text{fF}$
$C_{\text{gs,D1}}$	$48.68\,\text{fF}$	$C_{\text{gs,D2}}$	$48.68\,\text{fF}$	$C_{\text{gs,D3}}$	$48.68\,\text{fF}$
C_{gd1}	$59.870\,\text{fF}$	C_{gd2}	$7.412\,\text{fF}$	C_{gd3}	$7.412\,\text{fF}$
$C_{\text{gd,D1}}$	$2.998\,\text{fF}$	$C_{\text{gd,D2}}$	$2.998\,\text{fF}$	$C_{\text{gd,D3}}$	$2.998\,\text{fF}$
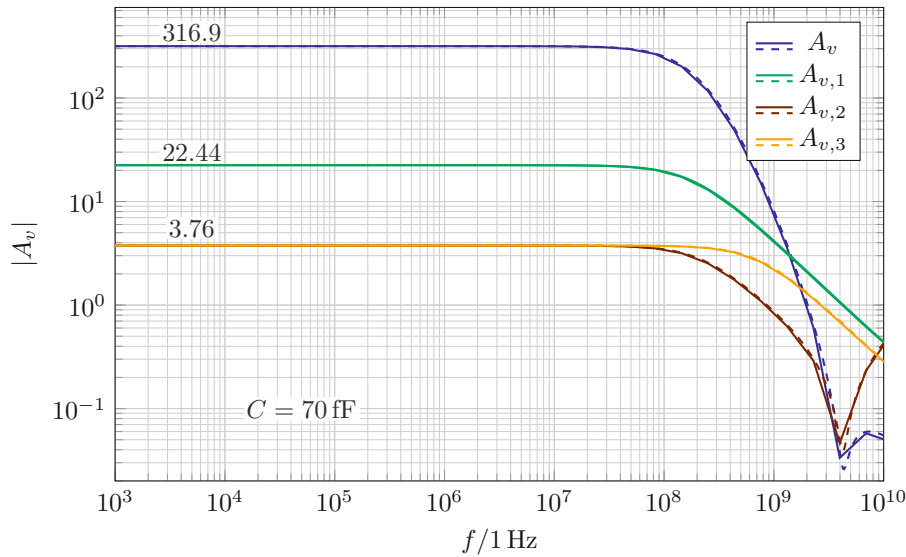
Figure 4.1: Simulated (solid) and calculated (dashed) open-loop gain of the three-inverter TIA with negative capacitance.

4.1 Frequency response

The frequency response of the 3INV-TIA-C is one of the main research questions specified in Section 1.3, because an accurate frequency response is a key foundation for the other analyses (stability, noise). That is why frequency response simulations were conducted first via an AC analysis between $1\,\mathrm{Hz}$ and $10\,\mathrm{GHz}$.

Firstly, the amplifier model from Section 2.3.2 is verified. The open-loop gain of the three inverter TIA is numerically evaluated for $C = 0\,\mathrm{fF}$, as well as $C = 70\,\mathrm{fF}$, using the open-loop stage gain formulas, Equations (3.2) and (3.8) to (3.11), from Section 3.1. Figure 4.1 shows the simulated (solid lines) and calculated (dashed lines) frequency response of the open-loop gains for the 3INV-TIA-C, whereas Figure 4.2 shows the open-loop gains of the 3INV-TIA. It is evident that the model accurately depicts the frequency response in both cases. The minor differences of the 3INV-TIA-C response at high frequencies are due to the lack of data points in this range in the simulation. Figure 4.1 further shows that $|A_{v,2}|$ (therefore also $|A_v|$), has a local minimum at approximately $4.5\,\mathrm{GHz}$. However, the cause of this minimum is not directly apparent from the open-loop analysis – cf. Equations (3.2) and (3.4). Upon further inspection, we find that only the term $g_{\mathrm{m1}}g_{\mathrm{m2}}+sCY_1$ in Equation (3.4) can result in a zero since the multplication of sC by $Y_1 = 1/R_1 + sC_1$ leads to s^2, which is real-valued and negative. Substitution of $s = 2\pi f\mathrm{j}$ into $g_{\mathrm{m1}}g_{\mathrm{m2}}+sCY_1$, taking the absolute value of this factor, and finding its minimum with respect to f yields

$$f = \frac{1}{2\pi}\sqrt{\frac{g_{\mathrm{m1}}g_{\mathrm{m2}}}{CC_1} - \frac{1}{2(R_1C_1)^2}}. \tag{4.1}$$
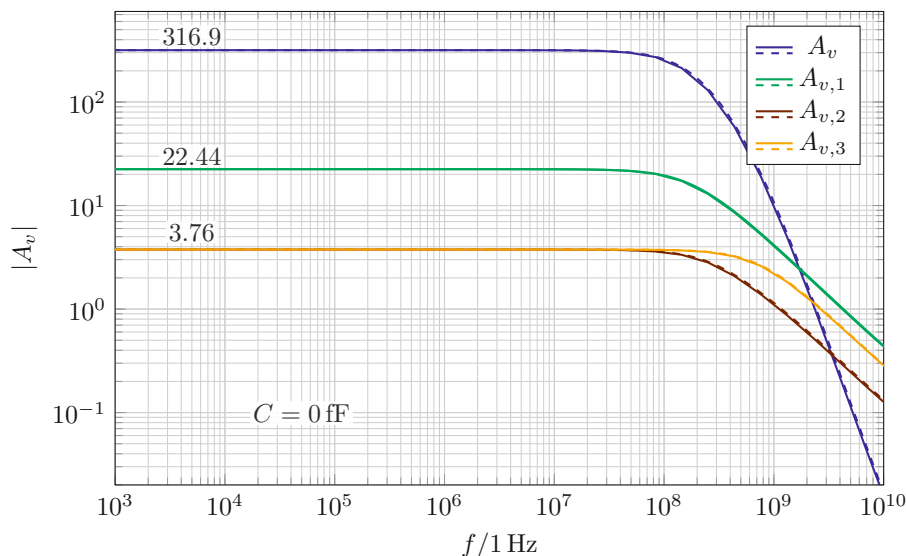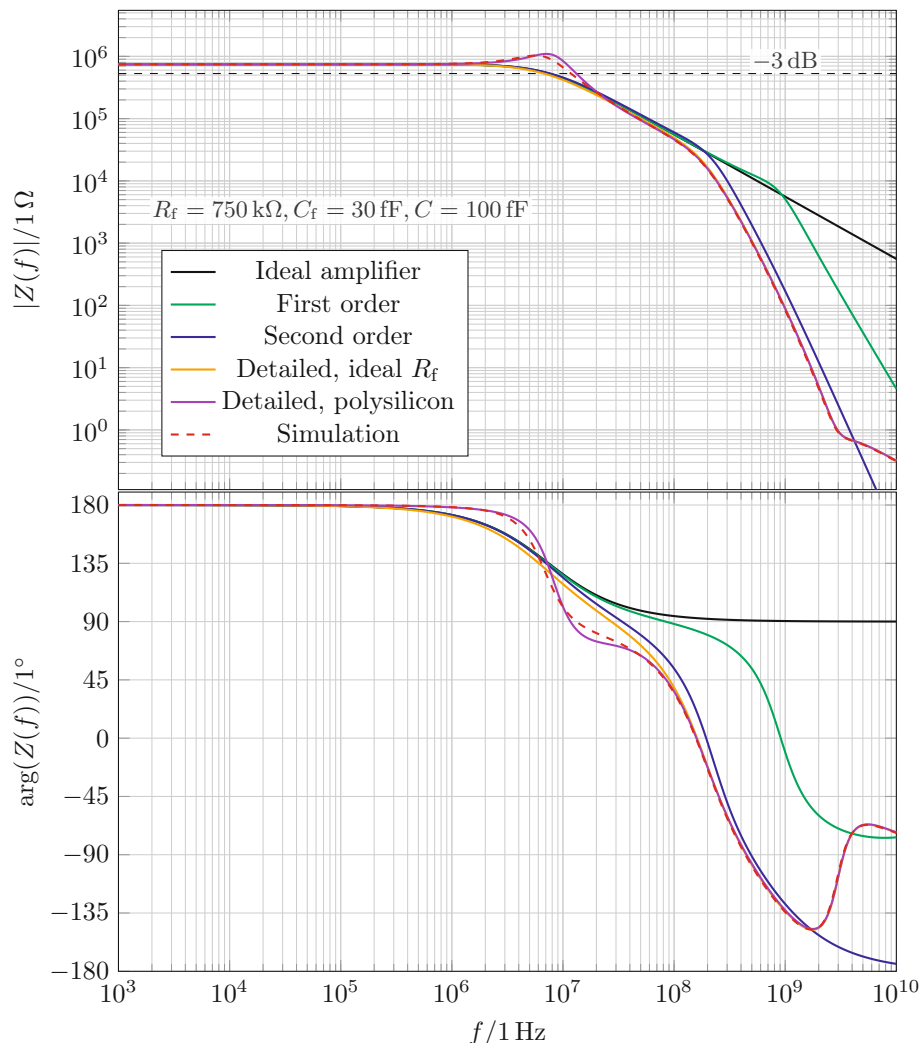
Figure 4.2: Simulated (solid) and calculated (dashed) open-loop gain of the three-inverter TIA without negative capacitance.

For the simulated design Equation (4.1) gives $f \approx 4.59\,\text{GHz}$, which is an adequate prediction of the frequency of the minimum encountered in Figure 4.1.

Secondly, the frequency response of the complete TIA, i.e. its transimpedance, is simulated and calculated for all models from Chapter 2 for a target bandwidth of $10\,\text{MHz}$ – see Figure 4.3. All of the models provide a reasonable approximation of the TIA $-3\,\text{dB}$ bandwidth. In fact, other simulations (not depicted here) showed that all models accurately predict the bandwidth if no peaking is present in the frequency response. As expected, Figure 4.3 shows that, for increasing level of model abstraction and simplification, the model deviates more from the simulated frequency response – especially with respect to the phase. Moreover, peaking that is caused by the polysilicon resistor can only be predicted by the fully detailed model including the RC-chain model of the resistor, that is Equation (2.72) in conjunction with Equations (2.41) to (2.44) and (2.62). Nevertheless, the second order model with ideal resistor is already a fairly good approximation for both, the absolute value of the transimpedance $Z(f)$ and its phase.

Finally, the broadbanding effect is studied. Table 4.2 shows the $-3\,\text{dB}$ bandwidth $f_{3\,\text{dB}}$ at constant R_f for different capacitances C. At $10\,\text{MHz}$ initial bandwidth ($R_\text{f} = 275\,\text{k}\Omega$), negative capacitance induced broadbanding increases the bandwidth by up to a factor of seven, before the circuit becomes unstable. On the other hand, for an initial bandwidth of $40\,\text{MHz}$ ($R_\text{f} = 80\,\text{k}\Omega$) the maximum bandwidth is three times its base value, whereas an improvement of factor two can be achieved for $70\,\text{MHz}$ initial bandwidth ($R_\text{f} = 54\,\text{k}\Omega$). These findings are in line with the conclusions of [3], i.e. that broadbanding improves the bandwidth of high-gain amplifiers the most. In the case of Table 4.2, the $10\,\text{MHz}$ variant has the highest gain (transimpedance) and exhibits the largest (relative) increase. Overall, the relative improvements shown in Table 4.2 are similar to previously reported values

Figure 4.3: Calculated (solid) and simulated (dashed) transimpedance frequency response of the three-inverter TIA with negative capacitance. All models were evaluated numerically for $C = 100\,\text{fF}$, $C_\text{f} = 30\,\text{fF}$ and $R_\text{f} = 750\,\text{k}\Omega$; thus the bit rate is $14\,\text{Mbit/s}$. The width of the polysilicon resistor is $W = 0.8\,\mu\text{m}$.

Table 4.2: Simulated bandwidth extension for three different initial bandwidths at different values of C. The initial bandwidths are set by R_f; the remaining design parameters are equal. Unstable points are omitted.

C	0 fF	50 fF	70 fF	100 fF	140 fF	160 fF	180 fF	200 fF
	10.2	13.5	15.6	20.6	38.4	58.0	69.9	72.4
$f_{3\,\text{dB}}/1\,\text{MHz}$	41.1	65.0	87.3	123.9	134.1	132	127.8	—
	71.6	135.4	154.8	162.8	158.3	153.4	—	—

Table 4.3: Simulated loop gain phase margin of the three-inverter TIA for different values of C and (ideal) R_f. Parameters that result in unstable loop gain, but stable transimpedance are marked by ○ (phase margin is not defined in these cases). Parameters that result in overall unstable behavior are marked by ×. The main diagonal shows parameter sets with equal bandwidth (70 MHz, $C_\mathrm{f} = 30$ fF).

R_f \ C	0 fF	30 fF	50 fF	70 fF	100 fF	120 fF	180 fF	200 fF	220 fF
54 kΩ	75.45°	58.81°	48.64°	39.06°	25.64°	○	×	×	×
66 kΩ	82.52°	67.20°	55.45°	45.42°	32.39°	○	○	×	×
76 kΩ	87.94°	71.02°	60.94°	49.66°	35.28°	○	×	×	×
90 kΩ	94.21°	76.61°	65.11°	54.62°	39.68°	○	○	×	×
117 kΩ	103.4°	84.46°	72.19°	61.04°	46.00°	○	○	×	×
145 kΩ	110.3°	90.09°	77.17°	65.67°	50.23°	○	○	○	×
265 kΩ	127.2°	101.8°	87.26°	75.04°	59.29°	○	○	○	×
295 kΩ	129.8°	103.3°	88.33°	76.22°	60.45°	○	○	○	×

in [8, 14, 27]. Bandwidth extension is not examined via the models from Chapter 2, because the good agreement between the frequency response of the models and simulation does not justify a separate examination – see Figure 4.3.

4.2 Stability

Stability simulations center around the frequency response of the loop gain AB. An AC analysis between 1 Hz and 10 GHz was conducted. Due to the simulation principle, see Figure A.3, there is a low frequency cutoff in the simulation. The values of AB are only valid at sufficiently high frequencies above this cutoff (e.g. 1 kHz). The frequency response of AB is not compared to the model in this section, because the accurate approximation of the open-loop gain (Figure 4.1) and transimpedance (Figure 4.3) implies the correctness of the model[1] of AB.

Table 4.3 shows the simulated loop gain phase margin for different values of R_f and C. As the loop gain becomes unstable, its phase margin is no longer a valid measure of stability – cf. Appendix A.2. The Nyquist criterion was applied to the simulation results in order to identify the parameter sets that result in stable or unstable transimpedance. Unstable loop gain with stable transimpedance is marked by ○ in Table 4.3, whereas overall unstable behavior (loop gain and transimpedance) is marked by ×. The results in Table 4.3 indicate that increasing values of C, which increase the bandwidth, degrade the stability of the three-inverter circuit, due to decreasing phase margin. Counteracting this change with higher feedback resistance R_f only helps to a certain extent, as can be seen by observing the main diagonal of Table 4.3, where the bandwidth is kept constant at 70 MHz. It is

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[1]Strictly speaking, the correctness of $Y_{11\mathrm{A}}$ is not implied, but it is assumed to be correct nonetheless.

evident that the increase of R_f does not fully compensate the loss in phase margin.

The maximum recorded C for which the loop gain is stable for all parameter sets is $C = 100\,\mathrm{fF}$, whereas it is unstable for $C \geq 120\,\mathrm{fF}$. Thus, the stability limit of AB is some point in the interval $]100\,\mathrm{fF}, 120\,\mathrm{fF}]$. Equation (3.25) predicts that AB becomes unstable at $C \approx 95\,\mathrm{fF}$, which is a reasonable, but not highly accurate approximation. Furthermore, Table 4.3 shows that the circuit becomes unstable for capacitances as low as $C = 180\,\mathrm{fF}$, but higher R_f can push this limit beyond $200\,\mathrm{fF}$. Stability analysis via Equation (3.15) predicts an absolute stability limit of $C \approx 207\,\mathrm{fF}$. Given that the analysis is based on the most basic model, derived in Section 2.2, we argue that Equation (3.15) is a sensible approximation.

In conclusion, the bandwidth extension via negative capacitance is a trade-off between stability and maximum bandwidth. Larger negative capacitance deteriorates stability. The analytical limits, Equations (3.15) and (3.25), provide a rough estimate for the loop gain stability limit and a good estimate for the overall stability limit.

4.3 Noise

When it comes to noise, the IRN current of the TIA is of particular interest. The output noise voltage PSD was simulated between $1\,\mathrm{Hz}$ and $10\,\mathrm{GHz}$. It was then integrated across the whole simulated frequency range (cf. Equation (2.86)) and divided by the simulated transimpedance at $f = 0\,\mathrm{Hz}$, i.e. $|Z(0)|$ (cf. Equation (2.89)), to get the IRN RMS current. This process was repeated for increasing values of C, while maintaining constant bandwidth by adjusting R_f appropriately. Moreover, the same procedure was performed for the modeled noise PSDs: Equation (3.40) (model 1), Equation (3.47) (model 2) and Equation (3.50) (model 3). Figure 4.4 shows the results of the simulation and the three numerical calculations for an ideal feedback resistor – polysilicon implementations are discussed below. To put the resulting RMS current into perspective, Figure 4.4 also shows the feedback resistor's thermal noise current $i_{\mathrm{n},R}$. The latter is computed from the respective values of R_f via Equation (2.78), multiplying this PSD with the noise bandwidth of a first order lowpass, i.e. $\mathrm{BW_n} = \pi/2 \cdot f_{3\,\mathrm{dB}} \approx 110\,\mathrm{MHz}$, and taking the square root [25].

Figure 4.4 shows that model 1 and 2 are almost identical. This validates the assumption that the IRN is dominated by the front-end, as model 2 only contains the front-end noise whereas model 1 incorporates noise from all three stages – see Equation (3.47) and Equation (3.40), respectively. In addition, both models agree well with the simulated IRN for $C < 120\,\mathrm{fF}$. For larger C, the models predict more IRN than the simulation. Figure 4.4 also proves what had already been surmised in Section 3.3.3: The simple noise model given by Equation (3.50) does not predict the simulated noise at all. It underestimates the IRN RMS current by far. However, Figure 4.4 confirms that all models and the simulation exhibit a noise optimum. In the case of the simple model, Equation (3.59) accurately predicts the optimum value of C ($94.8\,\mathrm{fF}$), where the front-end channel noise completely vanishes. In contrast, the noise optima of model 2, model 3 and the simulation occur at higher values of C. Hence, Equation (3.59) ($94.8\,\mathrm{fF}$) as well as Equation (3.58) ($96.1\,\mathrm{fF}$) merely
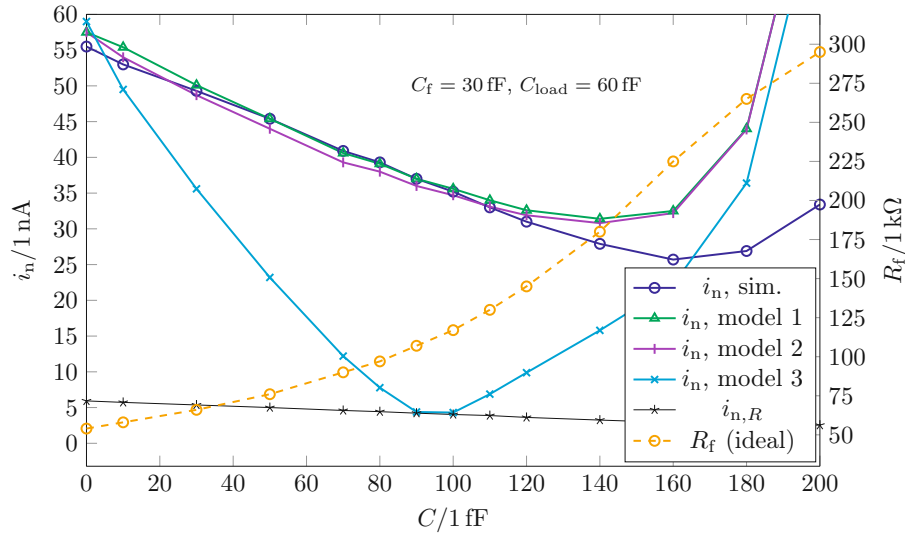
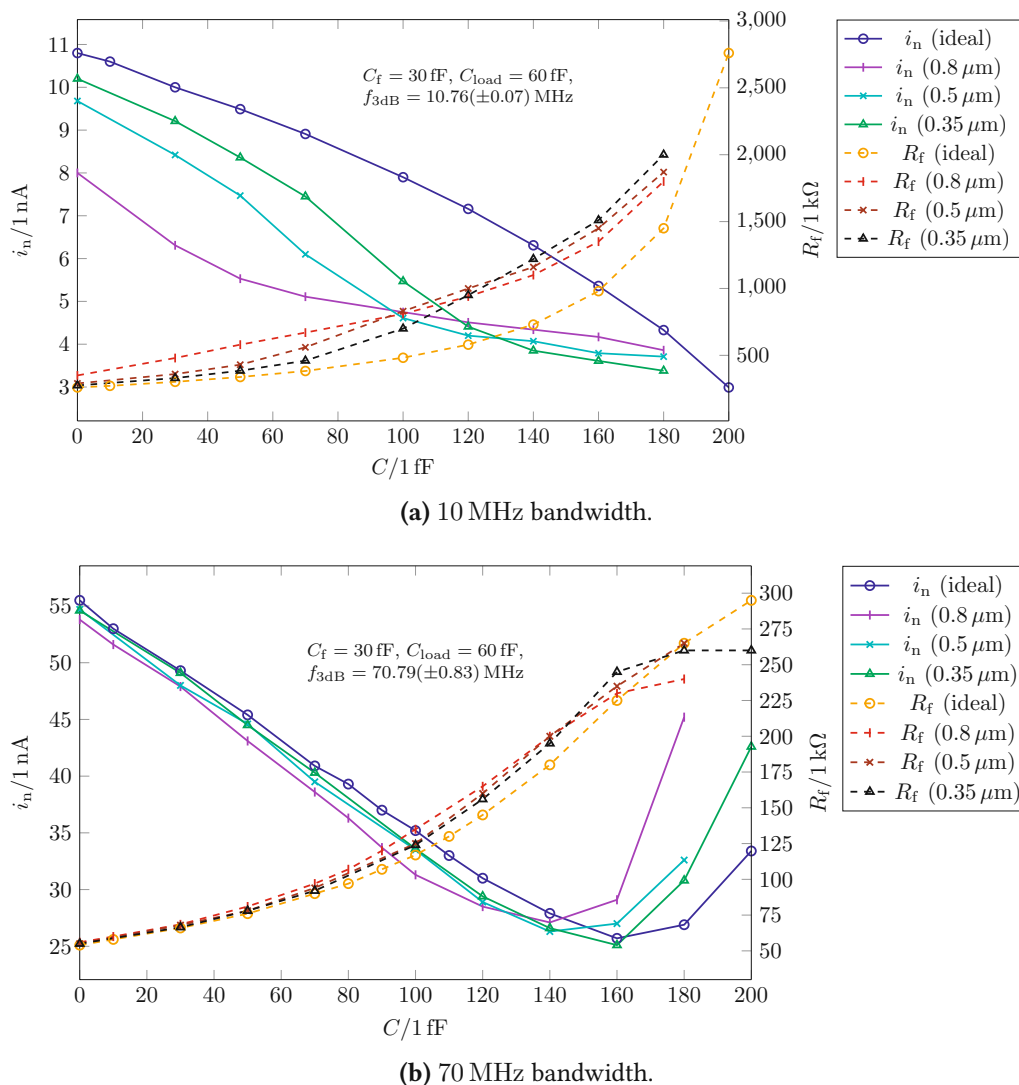**Figure 4.4:** Simulated and calculated input referred RMS noise current for increasing values of C at a constant bandwidth of $70\,\mathrm{MHz}$. Resistor thermal noise $i_{\mathrm{n},R}$, computed from the values of R_{f} and the noise bandwidth of a first order lowpass, is also shown for comparison.

provide an educated guess. For the $10\,\mathrm{MHz}$ variant (not depicted here) the models show a noise minimum at $C = 180\,\mathrm{fF}$, whereas in the ideal resistor simulation the noise keeps decreasing for increasing C, cf. Figure 4.5.

In conclusion, Equation (3.47) is a sensible model for IRN approximation due to its reasonable complexity and high accuracy. Strictly speaking, one could simplify Equation (3.47) even further by applying the $g_{\mathrm{m}1}R_{\mathrm{f}} \gg 1$ assumption, without loosing much accuracy[2].

How much does the IRN noise differ between the ideal feedback resistor and a polysilicon implementation, and how much does it depend on the chosen width? This question is answered by a set of simulations that is discussed next. The setup for these noise simulations is the same as described above. However, the IRN RMS current is simulated for the ideal resistor, as well as three different widths of n-type polysilicon resistors (namely $0.8\,\mu\mathrm{m}$, $0.5\,\mu\mathrm{m}$ and $0.35\,\mu\mathrm{m}$). Furthermore the simulations were conducted for both target bandwidths, i.e. $10\,\mathrm{MHz}$ and $70\,\mathrm{MHz}$. As Figure 4.5a shows, the IRN RMS current is vastly different between the individual implementations. However, the differences are directly related to the values of R_{f} required to satisfy the constant bandwidth constraint, which are also shown in Figure 4.5a. Unfortunately, the exact reason for the dissimilar behavior was not uncovered, but it seems that the width of the polysilicon resistor significantly impacts noise performance for high resistances. In contrast to Figure 4.5a, Figure 4.5b shows that there are only minor deviations between the four implementations for the $70\,\mathrm{MHz}$ variant. Values above $C = 160\,\mathrm{fF}$ result in intolerable amount of peaking in the transimpedance

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[2]For example, in the simulated design $g_{\mathrm{m}1}R_{\mathrm{f}}$ is always larger than 760, which is the value for the lowest feedback resistance at $C = 0$.

(a) 10 MHz bandwidth.

(b) 70 MHz bandwidth.

Figure 4.5: Simulated input referred RMS noise current at constant bandwidth, for different values of C and different implementations of R_f. The respective implementations are either the ideal resistor or an n-type polysilicon resistor (RNP1) with specified width. Two different bandwidths are shown: (a) $10\,\mathrm{MHz}$ ($14\,\mathrm{Mbit/s}$), (b) $70\,\mathrm{MHz}$ ($100\,\mathrm{Mbit/s}$). Unstable parameter sets are omitted.

frequency response, which leads to an increase in IRN. Additionally, the required resistance R_f increases to such an extent that the polysilicon resistors hit their bandwidth limit – cf. Figure 2.9. This is apparent from the flattening of the R_f curves in Figure 4.5b.

Figure 4.5 shows that negative capacitance substantially improves the noise performance of the 3INV-TIA-C. More specifically, for the ideal resistor the input referred RMS noise of the $10\,\mathrm{MHz}$ variant decreases from $10.8\,\mathrm{nA}$ at $C = 0\,\mathrm{fF}$ to $5.4\,\mathrm{nA}$ at $C = 160\,\mathrm{fF}$ ($-6.02\,\mathrm{dB}$ improvement); whereas the noise of the $70\,\mathrm{MHz}$ variant decreases from $55.5\,\mathrm{nA}$ at $C = 0\,\mathrm{fF}$ to $25.7\,\mathrm{nA}$ at $C = 160\,\mathrm{fF}$ ($-6.69\,\mathrm{dB}$ improvement).

5 Discussion

In this section the results of this work are briefly compared to [14]. Afterwards the chosen methods are reflected on.

The authors of [14] were able to improve the noise performance of a three-inverter TIA using negative capacitance. They argue that the improvement stems from the increase in R_f that counteracts the broadbanding effect of the negative capacitance. Larger R_f exhibit less thermal noise current – cf. Section 2.5.1. The improvement is also shown analytically, by providing a formula for the IRN PSD, based on [24] and the assumption[1] $C \ll C_T$. The latter is either a typographical error in the paper or a mistake in their derivation, since this work – in particular Equation (3.45) – clearly shows that the Miller effect with regards to C has to be considered in the IRN PSD. Thus, the assumption in [14] must read $|(1 - A_C)C| \ll C_T$. The results in [14] agree with their noise model, which indicates that the previous assumption is indeed true. This implies that the employed negative capacitance is very small. Unfortunately, the paper does not provide open-loop stage gains to calculate A_C in order to compare $(1 - A_C)C$ to C_T.

In opposition to the noise model in [14], this thesis reveals that the resistor thermal noise is not the only possible improvement, as the negative capacitance decreases the input node capacitance that scales the front-end channel noise, see Equations (3.47) and (3.50). Small input node capacitance is advantageous for the noise performance of TIAs [25], but usually C_T only depends on the PD and front-end transistor(s). With negative capacitance this dependency is relaxed.

Stability is not thoroughly analyzed in [14]. However, as mentioned above, the simulation results in [14] indicate that the design uses only very little negative capacitance for broadbanding. Therefore, stability should not be an issue. This conclusion is further supported by the fact that the change in phase margin reported in [14] is negligible. In contrast, this work shows that there are limits to stability if C is reasonably large – see Section 3.2 and the summary in Chapter 6.

The DPI/SFG method for circuit analysis was applied throughout this thesis, and it is now assessed retrospectively. Deriving the full DPI/SFG model of an amplifier entails

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[1]Note that C_F in [14] corresponds to C in this work, whereas C_f in this work is the outer feedback capacitance. No such capacitance is incorporated in the design in [14].

calculations that are generally of low complexity, but tedious nonetheless. With regards to the frequency response other methods, such as the generalized time and transfer constants (TTC) approach [10,11] (an evolution of the zero-value time constant method [9]), definitely have merit, especially for low-order approximations. However, for highly detailed approximations, such as the full 3INV-TIA-C model in this work, DPI/SFG involves less work than TTC. In terms of loop gain analysis for stability assessment DPI/SFG is probably the most usable method when compared to return-ratio or root locus techniques, in particular when it comes to simulation. This is because the loop is never opened in the actual circuit, thus all nodes are properly loaded and biased. Furthermore, no internal nodes of the transistor model need to be accessed, in contrast to the return-ratio technique for example. The noise analysis is reasonably simple with DPI/SFG. However, many assumptions are necessary to arrive at an elegant, yet accurate, noise model whose derivation from basic circuit models (without DPI/SFG) is likely less complex. Thus, not much is gained or lost by using DPI/SFG rather than another method. Overall, the author found the DPI/SFG approach valuable and particularly helpful when implementing numerical analyses, because the blocks of the SFG directly translate to variables (in MATLAB or any other program) that are much more accessible than a single transfer function.

6 Conclusion and outlook

Negative capacitance affects the characteristics of shunt-feedback TIAs, but is beneficial to both bandwidth and noise performance. In this work, it is shown that negative capacitance decreases the phase margin of the loop gain and can cause loop gain instability. The stability limit of the loop gain was derived analytically and is given by:

$$C = \frac{C_T + C_\mathrm{f}}{A_C}$$

This formula was found to provide a rough estimate of the loop gain stability limit observed in simulations, but it is not extremely accurate. Furthermore, stability of the TIA transfer function (transimpedance) is impaired by negative capacitance. Analytic analysis showed that the absolute stability limit is:

$$C = \frac{C_T - C_\mathrm{f} A_0}{A_C}$$

Stability limits observed in simulation are accurately predicted by this equation. The two equations provide evidence that the loop gain of inverting ($A_0 < 0$) shunt-feedback TIAs becomes unstable for smaller C than the transimpedance, resulting in a state of unstable loop gain and stable transimpedance. The only exception to this finding are circuits where $C_\mathrm{f} = 0$, where both stability limits coincide.

IRN due to front-end channel noise scales with the input node capacitance C_T in TIAs with FET front-end [24]. In this work, it is shown that the (partial) compensation of C_T by the negative capacitance $-A_C C$, which resulted in $\tilde{C}_T$, also scales the IRN. An accurate model for the IRN PSD – where the frequency dependency of $A_C(f)$ is taken into account in $\tilde{C}_T(f)$ – was derived:

$$S_\mathrm{i}(f) = \frac{|2\pi f(C_\mathrm{f} + \tilde{C}_T(f))|^2}{g_{\mathrm{m}1}^2}\left[4\mathrm{k_B}T\frac{2}{3}g_1 + K_1\frac{I_1^{a_1}}{C_\mathrm{ox}L^2 f^{b_1}}\right] + 4\mathrm{k_B}T\frac{1}{R_\mathrm{f}}$$

The squared input node capacitance in this formula facilitated the search for a noise

Table 6.1: Component values and target IRN RMS current of the different TIA variants that are planned for production.

Bit rate	R_f	C_f	C	i_n
	$350\,\mathrm{k\Omega}$	$30\,\mathrm{fF}$	$0\,\mathrm{fF}$	$8.0\,\mathrm{nA}$
$14\,\mathrm{Mbit/s}$	$600\,\mathrm{k\Omega}$	$30\,\mathrm{fF}$	$50\,\mathrm{fF}$	$5.5\,\mathrm{nA}$
	$810\,\mathrm{k\Omega}$	$30\,\mathrm{fF}$	$100\,\mathrm{fF}$	$4.8\,\mathrm{nA}$
	$56\,\mathrm{k\Omega}$	$30\,\mathrm{fF}$	$0\,\mathrm{fF}$	$53.8\,\mathrm{nA}$
$100\,\mathrm{Mbit/s}$	$125\,\mathrm{k\Omega}$	$30\,\mathrm{fF}$	$100\,\mathrm{fF}$	$31.0\,\mathrm{nA}$
	$200\,\mathrm{k\Omega}$	$30\,\mathrm{fF}$	$140\,\mathrm{fF}$	$27.1\,\mathrm{nA}$

optimum with regards to the IRN RMS current. It is shown that the optimal value of C is the stability limit of the loop gain. However, simulations indicated that the actual optimum may differ markedly from the analytical result.

At the time of writing, fabrication of several variants of the improved three-inverter TIA from [6] is planned – see Table 6.1. Some of these variants include negative capacitance for superior noise performance at data rates of $14\,\mathrm{Mbit/s}$ and $100\,\mathrm{Mbit/s}$. The feedback resistor R_f is implemented as a highly resistive n-type polysilicon resistor (RNP1) with a width of $0.8\,\mathrm{\mu m}$. Table 6.1 shows the expected IRN RMS current according to Figure 4.5. Experimental results of the fabricated integrated circuits will be used to assess, and hopefully corroborate, the theoretical analysis and simulations conducted in this work. Future studies will investigate the negative capacitance concept for other TIA circuits.

A Methodologies

This chapter gives an overview of the methodologies used and discusses why and how they can be used to solve the task at hand.

A.1 Driving point impedance / Signal flow graph (DPI/SFG)

In analog circuit design, the analysis and design process often requires deep insight and experience that is not easily obtained. Throughout this thesis the DPI/SFG method, which does not require extensive a priori knowledge, was applied several times. To the best of the author's knowledge, "Feedback in Analog Circuits" [18] by Agustin Ochoa is the first complete treatment of the DPI/SFG analysis method. Hence, this section is solely based on [18].

A.1.1 Basic DPI/SFG

At its core DPI/SFG relies on the Norton-theorem, which allows to represent any linear circuit by a single ideal current source and an impedance parallel to it. The equivalent circuit is derived with respect to one port of the original circuit and reproduces the exact behavior of this port. DPI/SFG applies the Norton-theorem to every node in a linear circuit. Thereby, the circuit characteristics appear in a factored form that can be mapped to a signal flow graph. The following steps have to be applied to the linear circuit:

1. Attach an independent voltage source to each node that is not already connected to one.
2. Calculate the DPI Z_{DPI} at each node, i.e. the impedance seen by the voltage source at the given node with respect to ground, while all other independent sources are zero.
3. Calculate the current i_{sc} into ground[1] at each node by setting the respective voltage source to zero and calculating the current into the source.

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[1] If the given linear circuit is the small-signal model of an amplifier circuit, then ground is actually AC ground.

(a) Common source circuit.

(b) Small signal equivalent circuit with additional voltage sources v_1 and v_2 for DPI/SFG.
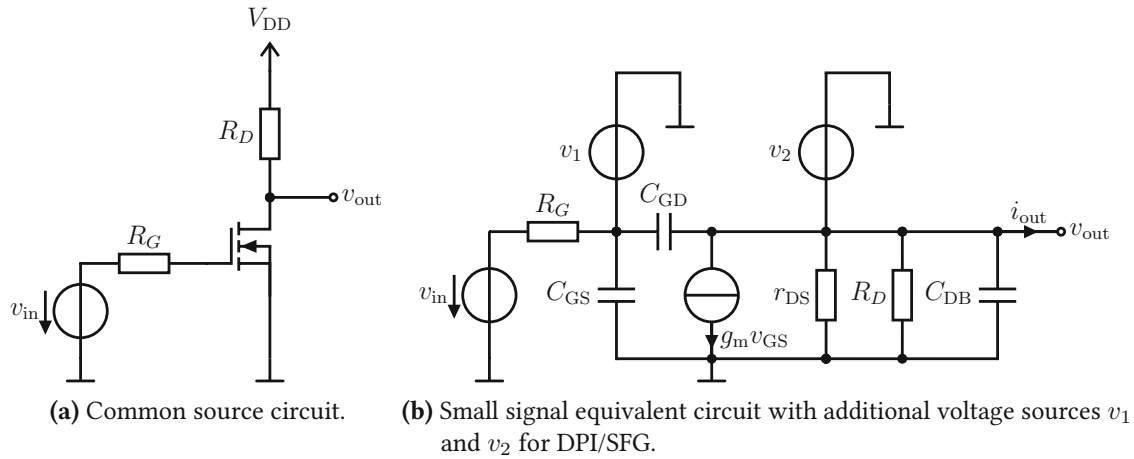
Figure A.1: An Example circuit to demonstrate the DPI/SFG method.

4. All node voltages can now be expressed by

$$v = Z_{\text{DPI}} \cdot i_{\text{sc}}. \tag{A.1}$$

5. Draw the SFG using the dependencies given by Equation (A.1).

As an example, consider the circuit in Figure A.1a. The high-frequency small signal equivalent circuit is drawn in Figure A.1b, where two additional sources were attached at non-driven nodes (Step 1). Now we proceed with the calculation of driving point impedances at each of the two nodes (Step 2) by zeroing all independent sources except for the one driving the node:

$$Z_1 = R_G \parallel C_{\text{GS}} \parallel C_{\text{GD}} = \frac{R_G}{1 + sR_G(C_{\text{GS}} + C_{\text{GD}})} \tag{A.2}$$

$$Z_2 = R_D \parallel r_{\text{DS}} \parallel C_{\text{DB}} \parallel C_{\text{GD}} = \frac{R_D r_{\text{DS}}}{R_D + r_{\text{DS}} + sR_D r_{\text{DS}}(C_{\text{DB}} + C_{\text{GD}})} \tag{A.3}$$

In Step 3, the short circuit currents of each node are calculated:

$$i_{\text{sc},1} = \frac{v_{\text{in}}}{R_G} + v_2 sC_{\text{GD}} \tag{A.4}$$

$$i_{\text{sc},2} = v_1 sC_{\text{GD}} - v_1 g_{\text{m}} - i_{\text{out}} \tag{A.5}$$

Finally, the terms are mapped to an SFG, which is shown in Figure A.2.

A.1.2 Feedback & stability: The Z-method

The previous example shows that the SFG of any circuit may have loops that indicate coupling between nodes in the circuit. One could easily calculate a "loop gain" from the
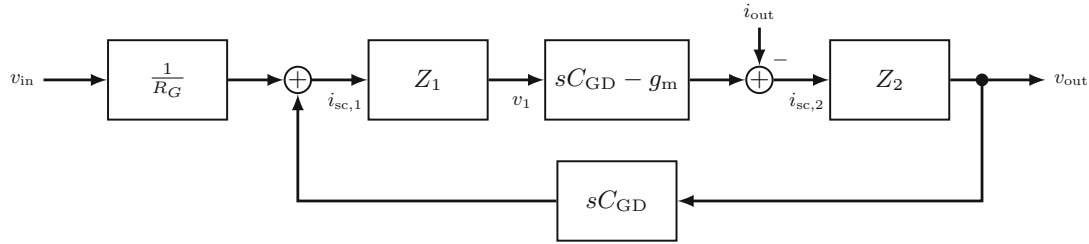
Figure A.2: Signal flow graph of the example circuit.

SFG shown in Figure A.2. However, in general this gain cannot be used to assess the stability of the circuit, because it results from algebraic expressions and thus is not a valid loop gain of the complete circuit. To define a loop gain that is useful for stability analysis, the Z-method has to be used – see Section 2.4 for an introduction.

Although the Z-method works as expected, two major issues have not been addressed so far, and the author of [18] does not provide a proof either:

1. Why is the loop gain defined by the Z-method suitable for stability analysis, whereas other algebraic expressions that emerge from the SFG are not?

2. Is stability of any circuit fully determined by the loop gain defined by the Z-method?

We will answer the second question first. Recall the generalized amplifier structure from Figure 2.10 with its DPI/SFG model (Figure 2.11). The output voltage is described by

$$v_{\text{out}} = \frac{i_{\text{sc}}}{Y_{\text{DPI}}} = i_{\text{sc}} \frac{-Z_{\text{out}}}{1 + AB} = i_{\text{in}} Z_{\text{in}} (Y_{21\text{A}} + Y_{21\text{F}}) \frac{-Z_{\text{out}}}{1 + AB}. \tag{A.6}$$

In Section 2.4 it was claimed that the loop gain AB fully determines the stability of the system. However, i_{sc} and Z_{out} may have poles too, which can be detrimental. Based on Equation (A.6), *two conditions* must be met for the circuit to be stable:

1. $i_{\text{sc}}/i_{\text{in}}$ and Z_{out} must be stable (i.e. must not have poles in the right half-plane).

2. $1 + AB$ must not have right-hand side zeros, i.e. the closed-loop in Figure 2.11 is stable.

It is straightforward to show that Item 2 is indeed a sufficient condition for overall stability: First, each term from Equations (2.71) and (A.6) is written in terms of numerator and denominator; both of which are polynomials of s:

$$Z_{\text{in}} = \frac{N_i}{D_i}, \quad Z_{\text{out}} = \frac{N_o}{D_o} \tag{A.7}$$

$$Y_{21\text{A}} + Y_{21\text{F}} = \frac{N_{21}}{D_{21}}, \quad Y_{12\text{A}} + Y_{12\text{F}} = \frac{N_{12}}{D_{12}} \tag{A.8}$$

$$AB = \frac{N_{AB}}{D_{AB}} = -\frac{N_i N_o N_{21} N_{12}}{D_i D_o D_{21} D_{12}} \tag{A.9}$$

These terms are further plugged into Equation (A.6),

$$H(s) = \frac{N_i}{D_i}\frac{N_{21}}{D_{21}}\frac{-\frac{N_o}{D_o}}{1 + \frac{N_{AB}}{D_{AB}}} = \frac{-N_i N_{21} N_o D_{AB}}{D_i D_{21} D_o (D_{AB} + N_{AB})} = \frac{N_i N_o N_{21} D_{12}}{D_{AB} + N_{AB}}. \tag{A.10}$$

The resulting expression shows that the poles of $H(s)$ only depend on the denominator and numerator of AB, as all other terms cancel each other.

To answer the first question, we can resort to simple nodal analysis to prove that the Z-method defines a valid loop gain function. If the node voltages of any linear circuit are subsumed in a vector $\mathbf{v}$, and the stimuli (currents) are subsumed in a vector $\mathbf{i}$, then Kirchoff's current law results in the linear system of equations

$$Y(s)\mathbf{v} = \mathbf{i}, \tag{A.11}$$

where $Y(s)$ is an admittance matrix that describes the coupling between individual nodes of the circuit. The solution for all the node voltages is thus given by

$$\mathbf{v} = Y^{-1}(s)\mathbf{i}. \tag{A.12}$$

There is no solution in case $Y(s)$ is singular, that is if $\det[Y(s_i)] = 0$. In fact, this equation defines the poles s_i of any possible v/i transfer function within the circuit [11]. Now the nodal analysis is done for the generalized amplifier with feedback shown in Figure 2.10. There are only two nodes, namely the output node and the input node. Note that there is no other stimulus current apart from i_{in}. The resulting linear system is

$$Y(s)\mathbf{v} = \begin{bmatrix} Y_{\mathrm{src}} + Y_{11A} + Y_{11F} & Y_{12A} + Y_{12F} \\ Y_{21A} + Y_{21F} & Y_{\mathrm{load}} + Y_{22A} + Y_{22F} \end{bmatrix} \begin{bmatrix} v_1 \\ v_{\mathrm{out}} \end{bmatrix} = \begin{bmatrix} i_{\mathrm{in}} \\ 0 \end{bmatrix} = \mathbf{i}. \tag{A.13}$$

Therefore, the determinant is zero if

$$(Y_{\mathrm{src}} + Y_{11A} + Y_{11F})(Y_{\mathrm{load}} + Y_{22A} + Y_{22F}) = (Y_{12A} + Y_{12F})(Y_{21A} + Y_{21F}). \tag{A.14}$$

In comparison, the loop gain resulting from the DPI/SFG analysis is given by

$$AB = -Z_{\mathrm{in}} Z_{\mathrm{out}}(Y_{12A} + Y_{12F})(Y_{21A} + Y_{21F}) = \tag{A.15}$$

$$= \frac{-(Y_{12A} + Y_{12F})(Y_{21A} + Y_{21F})}{(Y_{\mathrm{src}} + Y_{11A} + Y_{11F})(Y_{\mathrm{load}} + Y_{22A} + Y_{22F})}. \tag{A.16}$$

As we can see by substitution of Equation (A.14) into Equation (A.16), any pole given by Equation (A.14) yields $AB = -1$, and is therefore a root of

$$1 + AB = 0, \tag{A.17}$$

and vice versa. Thus, the loop gain defined by the Z-method is valid as it determines the exact same poles as the nodal analysis. It is therefore sufficient to use AB for assessing the stability of the circuit.
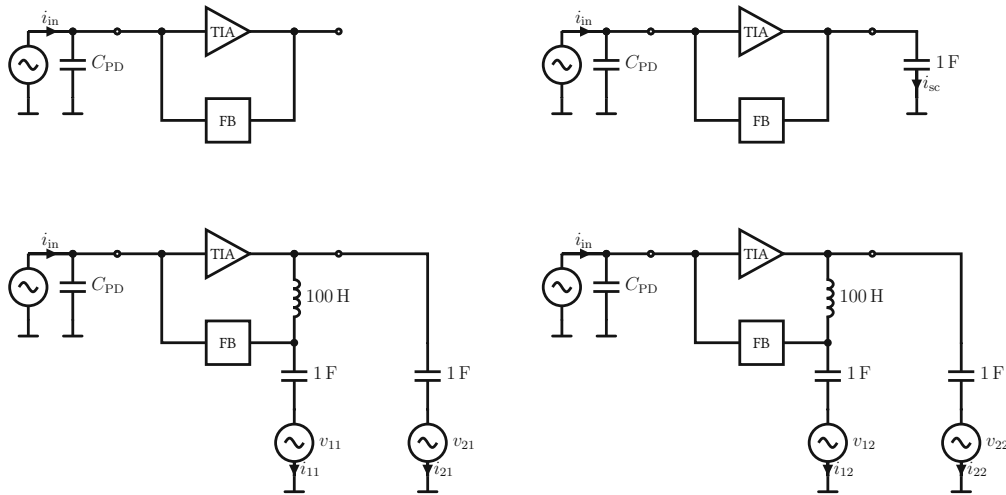
Figure A.3: Simulation setup for stability analysis, where "TIA" is the three-inverter TIA (with or without internal C) and "FB" is the feedback network (i.e. $R_f \parallel C_f$). The large capacitors and inductors ensure correct DC bias, but allow or block AC current flow, respectively. The top left circuit is the unaltered reference. The top right circuit is used to simulate the AC output short circuit current i_{sc}. The bottom left circuit determines i_{11}, i_{21}; here $v_{21} = 0$! The bottom right circuit determines i_{12}, i_{22}; here $v_{12} = 0$! Hence the circuits at the bottom simulate the superposition theorem. Output loading is also included in the simulation, but not shown here.

A.1.3 Using DPI/SFG for simulation

The Z-method is not only useful for analysis. Ochoa also describes an easy setup for loop gain simulation [18]. The core principle is to use four copies of the circuit – see Figure A.3: The first copy is an unaltered reference. The second copy uses a large, ideal capacitor (e.g. $1\,\mathrm{F}$) to create an AC short at the output node, while maintaining correct DC bias. In contrast, the third and fourth copy are modified by a large, ideal inductor (e.g. $100\,\mathrm{H}$) in the feedback path to create an open circuit for AC signals. Furthermore, an AC coupled voltage source is attached at each side of the inductor. The self- and cross-currents of each source – i_{11}, i_{22} and i_{21}, i_{12}, respectively – are simulated by applying the superposition principle. Hence, two copies of the circuit are necessary (the third and fourth one).

Once the self- and cross-currents are determined by simulation, Z_{out} and AB are given by the following relations [18]:

$$Z_{\text{out}} = \frac{1}{i_{11} + i_{22}} \tag{A.18}$$

$$AB = \frac{i_{12} + i_{21}}{i_{11} + i_{22}} \tag{A.19}$$

A.2 Nyquist stability criterion

The Nyquist criterion allows to draw conclusions about the stability of a closed-loop system, based on the characteristics of the open-loop system. Typically, the open-loop transfer function of an amplifier is stable, which is a necessary condition for the validity of simplified Nyquist criteria. More specifically, assessing stability via *phase margin* requires open-loop stability. Since this particular method is standard in analog circuit design, stability analyses can and will fail if the precondition is no longer satisfied. This section is dedicated to raising awareness of the general Nyquist criterion, because the simplified criteria do not always hold. It was shown previously that negative capacitance in TIA circuits is one such case.

In the following, a definition of the (general) Nyquist stability criterion, based on [26], is provided: Let $G_0(s)$ be the transfer function of the open loop. Furthermore, $G_0(s)$ is a proper[2] rational function. $G_0(s)$ has a total of n poles: P of them reside in the right complex half-plane; μ are on the imaginary axis; $n - P - \mu$ reside in the left complex half-plane. It can be shown that the closed-loop transfer function $H(s)$ also has a total of n poles: N of them reside in the right complex half-plane; ν are on the imaginary axis; $n - N - \nu$ reside in the left complex half-plane. The continuous phase change $\Delta\varphi_{\mathrm{S}}$ (discontinuities are neglected) of the closed-loop transfer function denominator $1 + G_0(\mathrm{j}\omega)$ for $\omega = 0$ to $\omega \to \infty$ follows from the location of the poles as

$$\Delta\varphi_{\mathrm{S}} = (P - N)\pi + (\mu - \nu)\frac{\pi}{2}. \tag{A.20}$$

Phase changes in counter-clockwise direction (in the Nyquist plot) contribute positively to $\Delta\varphi_{\mathrm{S}}$; clockwise changes negatively. The closed-loop system is stable if, and only if, $N = \nu = 0$. In other words, the closed-loop system has no poles on the imaginary axis or in the right half-plane. Hence, the Nyquist stability criterion is given by a special case of Equation (A.20), that is

$$\Delta\varphi_{\mathrm{S}} = P\pi + \mu\frac{\pi}{2}. \tag{A.21}$$

In practice, the phase change of $1 + G_0(\mathrm{j}\omega)$ is not measured with respect to the origin $(0, 0\mathrm{j})$. Instead, the phase change of $G_0(\mathrm{j}\omega)$ is measured with respect to the point $(-1, 0\mathrm{j})$. For example, if the open-loop system is stable ($P = \mu = 0$), the closed-loop system is stable if and only if $\Delta\varphi_{\mathrm{S}} = 0$. Hence, the Nyquist plot of $G_0(s)$ must not encircle $(-1, 0\mathrm{j})$. This special case is the foundation for simplified criteria, such as phase margin. On the other hand, if the open-loop system has two right-hand side poles, and no pole on the imaginary axis ($P = 2, \mu = 0$), then $\Delta\varphi_{\mathrm{S}} = 2\pi$ ensures closed-loop stability. Thus, the Nyquist plot of $G_0(s)$ must encircle $(-1, 0\mathrm{j})$ exactly once in counter-clockwise direction.

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[2] The degree of the numerator is less than the degree of the denominator.

LIST OF FIGURES

LIST OF TABLES

A Bibliography

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Wien, September 6, 2021