Master Thesis

A Germanium on Silicon on Insulator Based Reconfigurable Transistor Platform

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Abstract

In our modern world where more and more data is collected, the computational performance to process this information must also steadily increase. To keep up with rising demand, the transistor size is reduced to a point where the physical limitations are reached. To counteract these limitations, the use of novel material systems and the implementation of alternative device concepts are investigated. With this research the way is paved for a diversification of the functionalities of transistors.

In this thesis, a doping-free reconfigurable field-effect transistor (RFET) is fabricated. For this RFET a germanium (Ge) on silicon on insulator (SOI) wafer is used and is fabricated in a top-down fabrication. The Ge on SOI platform enables the advantages of Ge as semiconductor like the high hole mobility and bypasses the expensive and difficult to produce Ge on insulator technology. As contact material aluminium (Al) is used. The Al is thermally diffused in the semiconducting nanosheet, exchanging the semiconductor and forming a metal-semiconductor-metal heterostructure. Different passivation layers between the top-electrode and the semiconducting channel were investigated. Either a pure thermal silicon dioxide (SiO_2) or a combination of SiO_2 and a high-k dielectric like hafnium dioxide (HfO_2) and zircon dioxide (ZrO_2) have been tested. The SiO_2 is expected to have a low trap density at the interface between the channel and the top-electrode. Indeed, if a combination of SiO_2 and high-k dielectric is used, the nanostructure has a lower hysteresis than with a pure high-k dielectric. To form the SiO_2, the silicon capping layer on top of the Ge layer is used as sacrificial layer. There are two types of transistors fabricated and electrically measured in this work. The first is a Schottky barrier FET (SBFET) with only one top-gate. The second is a RFET with three independent top-gates. By using an extensive bias spectroscopy investigation the relevant characteristic properties of the fabricated structures are determined and compared to other existing RFET devices.

The goal of this thesis was to realise a RFET with a enhanced on-state conductance for both the n- and p-operation mode. Furthermore, the temperature stability of the RFET should be improved and the possibility to obtain a negative differential resistance (NDR) mode at room temperature should be investigated. The sample with the pure SiO_2 passivation has a high on-state current symmetry and a low hysteresis, but at temperatures above 50°C, the p-mode degrades strongly and shows a significant hysteresis. With the addition of HfO_2 in the passivation the on-state current symmetry worsens a little, but the hysteresis is still very low and the devices become temperature stable. The downside is that here the top-gate voltages must be higher to control the RFET. Finally, with the addition of ZrO_2 to the passivation on-state current symmetry is even better than with SiO_2 and the device is as temperature stable as with HfO_2 with a low hysteresis. Additionally the top-gate supply voltages are also the same as for pure SiO_2.

The presented RFETs based on Ge on SOI are showing the possibility to enable the design of high-performance adaptive circuits and therefore an increase of logic functions per chip. Beyond CMOS capabilities could potentially also be realised, for example for hardware security or artificial intelligence applications.

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Kurzfassung

In unserer modernen Welt in der immer mehr Daten gesammelt werden, muss die Rechenleistung zur Verarbeitung dieser stätig erhöht werden. Um mit diesem steigenden Leistungsbedarf mitzuhalten wurde die Transistorgröße zu einem Punkt reduziert, an dem physikalichen Limitationen erreicht wurden. Um diesen entgegenzuwirken, wurde die Verwendung von neuen Materialsystemen und alternativen Devicekonzepten erforscht. Mit dieser Forschung wurde der Weg für eine diversifikation der Funktionalitäten von Transistoren geschaffen.

In dieser Masterarbeit wird ein dotierungsfreier rekonfigurierbarer Feldeffekttransistor (RFET) gefertigt. Die RFETs werden in einer top-down Fertigung auf einem Germanium (Ge) auf Silizium auf Isulator (SOI) Wafer hergestellt. Die Ge auf SOI Platform erlaubt die Vorteile von Ge, wie die hohe Löcherbeweglichkeit, zu nutzen und die teure und schwer herzustellende Ge auf Isulator Technologie zu umgehen. Das als Kontaktmaterial verwendete Aluminium (Al) wird thermisch in die halbleitende Nanostruktur diffundiert, ersetzt dort den Halbleiter und formt eine Metall-Halbleiter-Metall Heterostruktur. Verschiedene Passivierungsschichten zwischen Top-Elektrode und Halbleiterkanal wurden untersucht. Entweder aus reinem Siliziumdioxid (SiO_2) oder eine kombination aus SiO_2 und High-k-Dielektrika wie Hafniumdioxid (HfO_2) und Zirkondioxid (ZrO_2) wurden getestet. Das SiO_2 weist eine geringe Störstellendichte am Interface zwischen Kanal und Top-Electrode auf. Wird eine Kombination von SiO_2 und High-k-Dielectrikum verwendet, dann hat die Nanostruktur eine geringere Hysterese als mit einem reinen High-k-Dielektrikum. Um dieses SiO_2 zu erhalten wird die Silizum-Kappe auf dem Ge als Opferschicht verwendet. Es wurden zwei Arten von Transistoren in dieser Arbeit gefertigt und elektrisch vermessen. Erstere ist ein Schottky Barrieren FET (SBFET) mit nur einer Top-Elektrode. Zweitere ist ein RFET mit drei Top-Elektroden. Über die Bias-Spektrokopie-Analyse wurden die relvanten Charakteristika der gefertigten Strukturen bestimmt, diese können dann mit bereits existierenden RFETs verglichen werden.

Das Ziel dieser Materarbeit war RFETs zu realisieren, die eine verbesserte On-State Konduktanz für sowohl den n- als auch den p-Operationsmodus aufweisen. Es sollte die Temperaturstabilität der RFETs verbessert werden und ob ein negativer differentieller Widerstand (NDR) Modus bei Raumtemperatur möglich ist, untersucht werden. Die Probe mit reiner SiO_2-Passivierung hatte eine gute On-State-Strom-Symmetrie und eine geringe Hysterese, aber bei Temperaturen über 50°C degradiert der p-Mode stark und zeigt eine große Hysterese. Mit dem Hinzufügen von HfO_2 in die Passivierung wird die On-State-Strom-Symmetrie etwas schlechter bei klein bleibender Hysterese und vorhandener Temperaturstabilität. Um den RFET voll auszusteuern müssen allerdings die Top-Gate-Spannungen erhöht werden. Mit der Ergänzung von ZrO_2 zur Passivierung wurde die On-State-Strom-Symmetrie besser und das Device ist genau so temperaturstabil wie mit HfO_2 bei einer immer noch geringen Hysterese. Zusätzlich sind die Top-Gate-Spannungen so gering wie bei reinem SiO_2.

Die präsentierten RFETs, basierend auf Ge auf SOI, zeigen die Möglichkeit zum Desing adaptiver Schaltungen die in breiten Anwendungsfeldern wie zum Beispiel in der Hardware-Sicherheit oder der künstliche Intelligenz eingesetzt werden können.

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Chapter 1

Introduction

In 1947 the first semiconducting transistor was built by John Bardeen and Walter Brattain at the Bell Laboratories and therefore a new field in science was born [1]. This technology has a steadily increasing impact on our every day lives, especially considering computers and smart-devices. There is a rising demand of processing power, so the performance of the devices must increase as well. For this increase of performance the transistor density has to rise, which means the transistor size has to be decreased. [2, 3] This trend was already seen in 1965 by Gordon E. Moore who predicted that the number of transistors in an integrated circuit will double every 18 months, which is known as Moore's law [4]. Even tough the semiconducting material of the very first transistor was germanium (Ge) [1], nowadays the most used semiconducting material is silicon (Si). Especially the metal-oxide-semiconductor field-effect transistor (MOSFET) is successful, because of the high-quality and stable native oxide SiO_2 that is used as an insulator. The native oxide offers a low trap density, which allows highly integrated and densely packed transistor circuits. Another advantage of Si is its well-known fabrication processes. [3, 5] However, the continuous shrinking of the devices has lead to the reaching of fundamental scaling limits, like higher leakage currents, which are caused by the tunneling of carrier charges through the thinner oxide layer. This restricts further performance enhancing of modern devices. [6, 7]
To overcome these restrictions, the focus of research now has shifted to other materials, new device architectures and technologies [2]. To improve the gate oxide thickness, new materials like high-k dielectrics are considered to use instead or in combination with SiO_2 [8]. Ge with the high mobility of its charge carriers is a promising alternative to Si, especially for increasing the switching speed. One big problem with Ge is the absence of a high-quality oxide, which can be used as a gate oxide in field-effect transistors or as surface passivation. To counteract this high-k dielectrics are also used on Ge. [9, 10] Because the Ge on insulator (GeOI) has a rather high cost and also exhibits processing issues it has hindered the utilisation of the advantages of Ge based MOSFETs. A low-

cost alternative to GeOI platforms are Ge on SOI platforms, here ultra-thin Ge layers are grown on a SOI wafer, with molecular beam epitaxy (MBE). [11, 12] Another important aspect is the contacting of the semiconductor with metal, here well-defined and high-quality metal-semiconductor contacts must be formed, because the injection of charge carriers highly depends on the interface and its energy barrier [13]. Such contacts can be formed as metal-semiconductor heterostructures. Those are formed by conducting a semiconducting material with metal contacts and exchanging the semiconductor with the metal by a thermally induced diffusion process [14–16]. The formations of silicides and germanides need to be carefully engineered, because of its difficult processing mechanisms and the formation of inter-metallic phases [17].
Instead of only down-scaling of the transistor size modern concepts are moving towards a diversification of functionalities, which is the so-called More-than-Moore domain. One of this alternative unconventional designs is the reconfigurable field-effect transistor (RFET), which allows to change the charge carrier operation type of the device during its run-time. This makes it an interesting candidate for applications like adaptive or neuromorphic computing and hardware security [18]. Another benefit of the RFET structure is, that doping with its challenges at nano-scale, is not required. For lower power consumption a n-MOS and a p-MOS transistor are combined, to get a complementary MOS (CMOS) circuit. Because of the different charge mobilities of electrons and holes in Si those two transistor types are fabricated with different sizes. This geometrical asymmetry can be overcome with RFETs, because the operation type is set by the applied voltage, which results in barrier and band bending and not with different doping and design concepts. A symmetric CMOS circuit can be realised by fabricating RFETs with equal or at least similar on-state currents for both charge carrier types. In this case both transistors can be used as n-type or p-type FET. [8, 19–22]
Another interesting aspect is that the Ge heterostructures exhibit a negative differential resistance (NDR), at this ultra-thin Ge the NDR can be shown at room temperature. [23] The NDR effect is very interesting for complex logic functions like adders, photodetectors and THz-oscillators. [24–27]

In this thesis the above mentioned emerging transistor design, the RFET, with Ge on SOI as semiconducting material and aluminium (Al) as connecting metal, is fabricated and electrically characterised. Because of the use of Ge on SOI technology, the RFET is not made out of pure Ge and therefore does not exhibit its asymmetry and hysteresis. For the electric characterisation two different types of transistors are created. The first one has only one top-gate (TG) placed over both metal-semiconductor junctions, which creates a Schottky barrier field effect transistor (SBFET) and the other one with three TGs (triple top-gate, TTG) two placed over the Al-Si-Ge junctions (program gates) and one in the middle of the channel (control gate). The electric evaluation of the performance of the devices is made at TTG structures. Also the influence of the dielectric layer is investigated. Besides SiO_2, two different high-k dielectrics are used as insulator between the channel and the TGs of the device. The two high-k material used in this work are hafnium dioxide (HfO_2) and zircon dioxide (ZrO_2). They are used in combination with a SiO_2 layer below. The devices are fabricated in a top-down approach, which makes it favourable for the

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semiconductor industry as it has the potential for wafer-scale processing. [22]
The purpose of the selected material system is to get a RFET configuration with a good on-state symmetry, relatively high on-state currents and reasonable low off-state currents, to get an energy-efficient, fast switching and adaptive device fabricated by a well-established process and without the need of doping. This would be a promising device for modern transistor applications. [17, 19, 20, 22]

The questions addressed in this thesis are if the chosen material system, the Ge on SOI platform, is suitable for the realisation of RFET devices, how its electrical properties fair against other existing RFETs on other material systems and finally how does the use of high-k dielectrics influence the performance.
Starting in the following chapter 2 - "Theory" the fundamental theory of the used materials is presented, as well as the formation of the metal-semiconductor junction and the RFET concept which is used in this work. In chapter 3 - "Experimental Techniques" an overview of the fabrication processes and techniques for the Al-Si-Ge-Al heterostructure is given and the characterisations methods for the electrical investigation are presented. Chapter 4 - "Results and Discussion" shows the final devices and the measurements and characterisation results are presented and discussed. And finally chapter 5 - "Summary and Outlook" summarises the gained results and gives an outlook to possible further investigations of the presented material system and devices and their possible field of application.

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Chapter 2

Theory

This following chapter has three sections which are covering the fundamental basics of this thesis. The first section, section 2.1 deals with the used materials and the relevant properties of those. Here the characteristics of Ge, Ge on Si on insulator (SOI) and the used dielectrics are discussed. Here also the difference between Si oxide and Ge oxide are shown. The next section, section 2.2 describes the formation of a metal-semiconductor junctions and the related charge carrier transport mechanisms which arise. In the last section, section 2.3 the concept of the reconfigurable field-effect transistor (RFET), as well as its associated structures and operation modes, is introduced.

2.1 Materials

In this section the properties of the used materials are presented. First the properties of Ge are discussed as well as the the advantages of Ge on SOI which is used in this thesis. Also the properties of the different dielectrics that are used, which are Si dioxide (SiO_2), hafnium dioxide (HfO_2) and zircon dioxide (ZrO_2) as well as the reason why SiO_2 is preferred over Ge oxide (GeO_x) and the the advantages of using high-k dielectrics are discussed.

2.1.1 Germanium

Ge was first discovered by Clemens Winkler in 1886. The element has a grayish-white appearance and is very brittle. It is placed in the fourth group in the periodic table of elements with the atomic number 32. Therefore it exhibits similar properties as Si. The average occurrence in the earth's crust is around 1ppm. This is rather scarce considering it cannot be found in large depositions with high concentrations [28]. Ge can mainly

be obtained as a by-product from zinc ores and the combustion from certain coals, also other materials like argyrodite, which is a sulfide of Ge and silver, and germanide (∼8% Ge content) contain Ge. In the semiconductor industry a crystalline Ge with ultra-high purity is required, which can be obtained by zone-refining techniques [29]. Ge has a melting point of 938.25°C and a boiling point of 2833°C. It crystallizes in a diamond crystal structure, which can be described as two face-centered-cubic (fcc) lattice structures, where one of those is displaced 1/4 of the main diagonal along the direction of this diagonal, as shown in figure 2.1a. Each Ge atom is surrounded by four other atoms positioned at the corners of a tetrahedron. They are connected by covalent bonds [30]. The lattice constant of this unit cell is $a = 5.66$Å at 0K (-273.15°C). The distance of the nearest neighbor in the lattice is $\sqrt{3}a/4$ [31]. In the diamond structure the atoms are sp^3 hybridized state and all available electrons can be shared so that only the bonding orbitals are occupied. So a fully occupied valence band and a conduction band are formed, which are separated by an energy gap [30]. Figure 2.1b shows the band structure of Ge, which shows the minimum of the conduction band at L and the maximum of the valence band at Γ, this results in an indirect band gap of $E_G = 0.66eV$. But at the Γ-point there is also a direct band gap of $E_G = 0.8eV$ [32].
Ge has a carrier mobility of $\mu_e = 3800cm^2V^{-1}s^{-1}$ for electrons and $\mu_h = 1820cm^2V^{-1}s^{-1}$ for holes, because of its light effective electron and hole mass. Compared to Si with $\mu_e = 1900cm^2V^{-1}s^{-1}$ and $\mu_h = 500cm^2V^{-1}s^{-1}$, those are significant higher. The hole mobility is the highest of all known semiconductor materials. Therefore it is very promising material. [29]

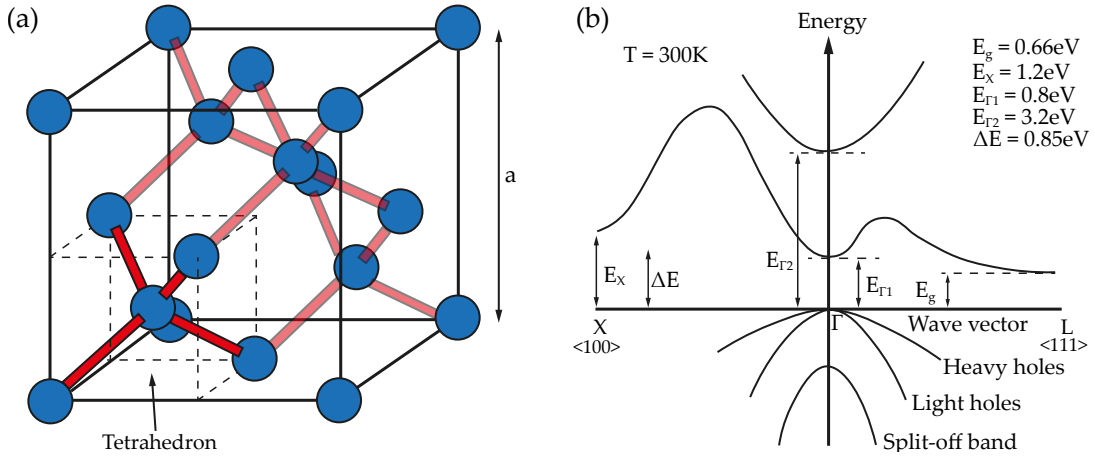

Figure 2.1: *Lattice structure and the band diagram of Ge. Subfigure (a) illustrates the diamond lattice of Ge with one of the associated tetrahedrons highlighted, while subfigure (b) shows the band diagram with the corresponding band-gap of Ge.*
Lattice structure adapted from [21], Band diagram adapted from [21, 33, 34]

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2.1.2 Germanium on Silicon on Insulator

In Si based technologies Si on insulator (SOI) is commonly used platform for modern transistor technology. This is related to a lower substrate capacitance and better electrostatic control, which leads to a leakage reduction [35]. To have both the advantages of SOI and the high carrier mobility of Ge, Ge on insulator (GeOI) constitutes an attractive platform for emerging nanoelectronic devices. However, GeOI has the big disadvantages of its high cost, quality limitations and difficult processing. In this regard, for this work, Ge on SOI, composed of an ultra thin Ge layer on a SOI platform was chosen as alternative. This provides a low-coast substitute to the expensive GeOI platform [11].
To grow the Ge on SOI substrates, a Ge-rich but pseudomorphic two-dimensional film with a low surface roughness is deposited by molecular beam epitaxy (MBE) on the Si device layer of a commercially bought SOI substrate.

2.1.3 Dielectrics

One way to further improve transistors metrics is to use so-called high-k dielectrics instead of the commonly used SiO_2. In the following subsections the properties of different oxides which were used in the fabrication of the RFETs, namely SiO_2, hafnium dioxide HfO_2 and zircon dioxide ZrO_2 will be described.

2.1.3.1 Silicon oxide vs. Germanium oxide

Ge has a very unstable native oxide which is also water-soluble. It easily decomposes into several Ge_yO_x sub-oxides. This strongly effects the morphology and electrical quality of the interface. The quality of the oxide layer strongly depends on oxidation temperature and pressure. The oxide layer consists of a mixture of GeO_2 and GeO. GeO_2 would be the preferred oxidation state to reduce the density of trap states at the interface. These trap states increase the off-state leakage current and sub-threshold turn-off. This mixture of different oxides decreases the performance of Ge-based devices, since this increases the gate leakage current and also reduces the high carrier mobility of Ge because of scattering. [36]

Si forms a very stable native oxide that can be easily grown and can be used as a high-quality gate oxide in FETs. It has numerous other applications in the semiconductor industry. The Si oxide used as dielectric in semiconductor devices is typically amorphous. In addition to the native oxide that forms when Si is exposed to air at room temperature, there are various techniques to fabricate amorphous SiO_2, such as thermally-induced growth, chemical vapour deposition, sputtering and evaporation. Thermally-induced growth can be achieved either with dry oxygen or with water at temperatures from 900°C up to 1100°C or even higher. The density of the film and the growing rate are strongly dependant on the temperature and the oxidation environment [37]. Chemically grown SiO_2 offers a very low interface trap density and low-temperature growing conditions within the nano-meter scale. [38]

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Amorphous SiO_2 has a dielectric constant of 3.9, a breakdown voltage of 10MV/cm, a bad-gap of $E_G = 9eV$, a refractive index of 1.46 and a melting point of about 1710°C. [21]

2.1.3.2 Hafnium oxide

To be able to down-scale the transistor structures even further, the oxide thickness must also be reduced. Is the oxide thickness below 2nm, then defects and tunneling become critical problems. Here so called high-k dielectrics can be used. The effective oxide thickness can be reduced to less then 1nm depending on the high-k dielectrics used. [21, 39]
The high-k dielectrics should replace Si dioxide and so there are many desired requirements for those. These requirements are the higher dielectric constant, a comparable band-gap for a low leakage current and a comparable electric breakdown strength. A thermodynamic stability up to 1000°C to be process compatible with CMOS fabrication is mandatory and the material should be processable with existing process technologies. Because those requirements are at least to some extent related to each other, a compromise must be found. The main requirements are the static dielectric constant, the band-gap and the electrical breakdown strength. [39]

One promising material is hafnium dioxide (HfO_2), which is used in these thesis. To fabricate a thin-film of HfO_2 there are different approaches like sputtering from a HfO_2 target, ALD, CVD, MBE growth or a wet chemical method. All these processes have different process parameters, with different advantages and disadvantages and result in a crystalline structure of the dielectric. The HfO_2 used in this work is grown by an ALD process, because this process offers the most control over the resulting HfO_2-layer while having the downside of a small growth rate. To achieve amorphous HfO_2 the process temperature of the ALD-process must be below 500°C. There are often multiple crystallographic phases because of interface strains due to lattice mismatch with the substrate. [39]

Amorphous HfO_2 has a dielectric constant of about 22-25, a breakdown voltage of 3.9-6.7MV/cm, a relative band-gab of 5.7eV (for amorphous HfO_2), its melting point is at about 2900°C and it is thermally and chemically stable when in contact Si. [39]

2.1.3.3 Zircon oxide

Another promising high-k dielectric material is zircon dioxide (ZrO_2), it is the second high-k dielectric used in this thesis. For thin-film deposition of ZrO_2 there are also different approaches like ALD, sputtering from a ZrO_2 target, CVD and a sol-gel method. As always all these processes have different advantages and disadvantages. For this work the ZrO_2 was also grown via an ALD process, because of the low deposition temperature and good conformity control of the process. Again there are low growth rates and a high vacuum required. The low-temperature crystallization of ZrO_2 leads to a poly-crystalline structure, which leads to increased leakage currents. [40]
ZrO_2 has a dielectric constant of about 22-24, a breakdown voltage of 3.3-5.7MV/cm and

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a relative band-gab of 5.8-7.8eV. Its melting point is at about 2680°C and it has a good thermodynamic stability in direct contact with Si. [40]

2.2 Metal-Semiconductor Heterostructures

To built electronic devices it is necessary to fabricate reliable contacts, this leads to metal-semiconductor junctions. Those will be discussed in the this section. Here the interplay between the metal, in this work aluminum (Al) and the semiconductor structure, here Ge and Si, are presented.
The metal is needed to connect the semiconductor structure to the rest of the electronic device by building a metal-semiconductor junction at the interface to the semiconductor. 2.2.1. [21]

The conducting material should establish a reliable, well-defined, abrupt junction with a low contact resistance and as little interface traps as possible. Here it is important to have a metal-semiconductor combination with no inter metallic phase formation.[41, 42]
The method used in this thesis to fabricate the required metal-semiconductor contacts is the thermally-induced diffusion of the metal towards the semiconductor structure. Here germanide-metallic compounds are formed. There are many different such compounds. The ones discussed here are the Al-Ge and the Al-Si-Ge heterostructures. The diffusion of Al in these materials exhibit an abrupt, reproducible junction from single-elementary Al to the semiconducting structure with no inter metallic phases. This increases the reliability and reduces the variability of the individual devices. [41]
The possibility that the Al-Ge-Si material system forms a reliable contact, free of inter metallic phases is based on the fact that the individual binary Al-Si and Al-Ge systems exhibit no inter metallic phase formation. To retain the crystalline form of the materials the process temperature should remain below the eutectic temperature of 577°C for Si and 420°C for Ge. [41]

The Al-Si-Ge system in this work, which comes from the Ge layer and the underneath located SOI layer, is formed by solid-state diffusion [41]. Here the diffusion coefficients between materials and within the material need to be taken into account. The diffusion coefficient of Si and Ge in Al and Al in Al are the highest of those, for a rapid thermal annealing process at 500°C. The Al replaces the out-diffusing Si and Ge and is supplied from the Al source due to self-diffusing.[41]

An important aspect to consider are the energy levels of metal impurities in metal-semiconductor heterostructures, also referred as metal-induced gap states (MIGS). Because this could have a big impact on the band structure and on the behaviour of the

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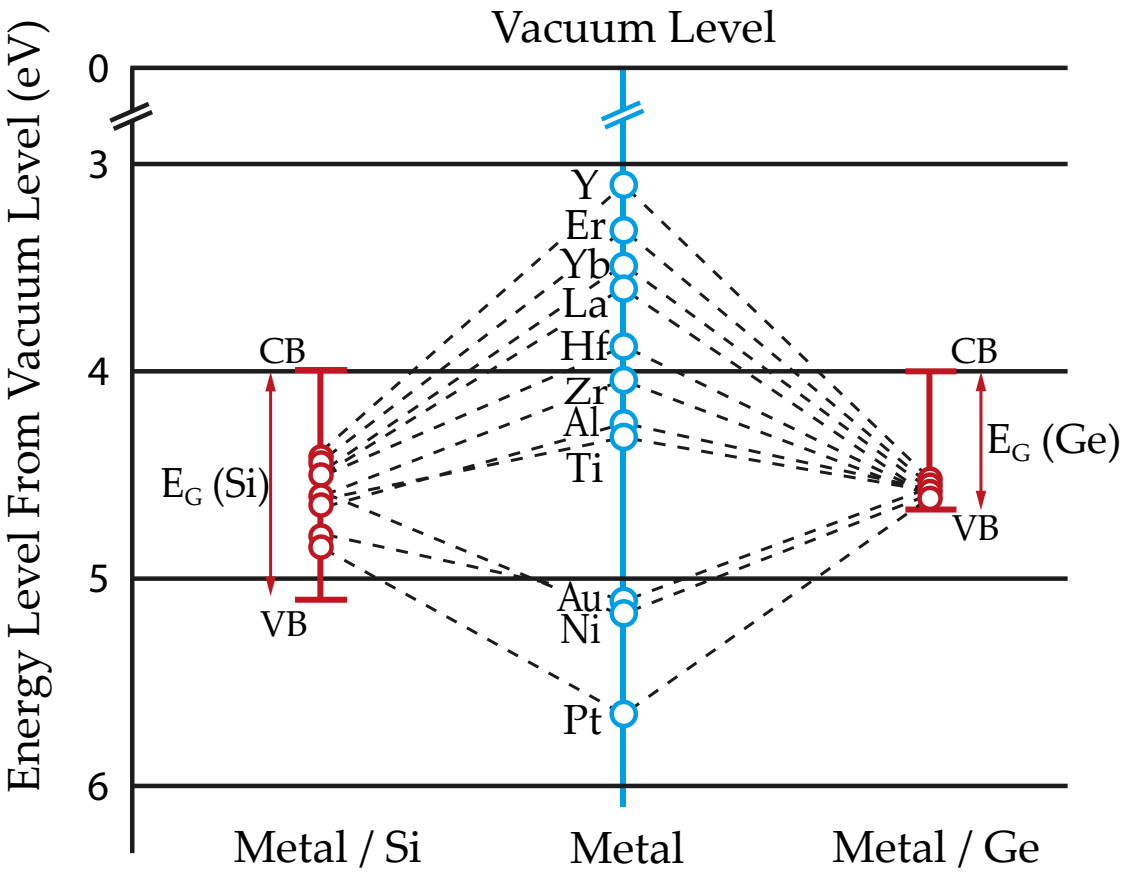

Figure 2.2: *Energy barrier heights of various metal-semiconductor junctions. For Si as the semiconductor material the pinning is mainly located in the middle of the band-gap, while for Ge the pinning level is close to the valence band.*
Adapted from [43, 44]

device. The ionisation energy for Al in Si is 57meV and 10meV for Al in Ge. [21, 41] In metal-semiconductor junctions the barrier height is mainly determined by the characteristics of the metal and the interface properties [21]. The resulting barrier height level (pinning level or Fermi-pinning level) within the band-gap of the semiconductor results from the used material. For pure Ge the Al-Ge barrier height is close to the valence band and in pure Si the Al-Si pinning level is close to the middle of the band-gap. This is shown in figure 2.2 where the majority of the metals obtain a Fermi-pinning level close to the mid-band-gap at the metal-Si contact or have a barrier height close to the valence band-gap at the metal-Ge contact. For Al-Si-Ge the pinning level is dependent on content of the components. [41, 43, 44]
The resulting heights of the pinning levels of different metals in contact to a semiconductor, as shown in figure 2.2, are theoretically described as a metal-semiconductor junction.

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2.2.1 Metal-Semiconductor Junction

When two different materials are brought in contact to each other while in thermal equilibrium, in this case Al and Ge or Si, the Fermi energies of the two materials equalize to the same level, which leads to band bending that is strongly dependant on the characteristics of the materials. The equalisation is achieved by charge carrier transport until charge neutrality is obtained. [21]
The properties of the junction mostly depend on the difference in the work functions of the materials. This defines their contact potential. In a metal the work function ϕ_m describes the difference between the vacuum level and the Fermi level. For the metal Al this has the value of $q\phi_{m,Al} = 4.2eV$ [13]. For a semiconductors the work function is defined as $\phi_S = \chi_S + \phi_n$, where χ_S is the electron affinity measured from the bottom of the conduction band E_C to the vacuum level E_{vac} and ϕ_n is the difference between E_C and the Fermi level E_F. [21, 45]

When the work function of the metal is higher then the one of the semiconductor ($\phi_m > \phi_s$) the energy bands of the semiconductor shift downwards. In this case electrons migrate from the semiconductor to the metal. If it is a n-type semiconductor the redistribution of the charges at the interface creates a depletion region near the junction. This leads to a similar behaviour as the p-n-junction at a regular diode. For a p-type semiconductor the extracted electrons are taken by the dopants and no depletion region is formed. Here the junction behaves similarly to an ohmic contact.[21, 45]
When the work function of the metal is lower than the one of the semiconductor ($\phi_m < \phi_s$) the energy bands of the semiconductor shift upwards. This causes the reversed behaviour. The n-type semiconductor forms an quasi ohmic contact and the p-type semiconductor shows a Schottky contact.[21, 45] This is shown in figure 2.3.

To get the contact potential ϕ_B, the difference between the metal work function and the electron affinity of the semiconductor must be calculated. This depends on the type of the semiconductor as shown in the following equations [21].

$$q\phi_{B,n} = q(\phi_m - \chi_S)$$

$$q\phi_{B,p} = E_G - q(\phi_m - \chi_S)$$

This approach assumes an ideal contact between semiconductor and metal with an abrupt junction without any interface layers, no interface surface states or dangling bonds. [21, 45] Interface traps will have an impact on the band bending, thus also on the resulting barrier height for the corresponding charge carriers. This means the charge of the initial barrier height not only depends on the work functions but also on the interface charge trap density. So a low interface state density, which means a reliable and reproducible interface between the materials, is crucial for the device. [21, 41, 45]

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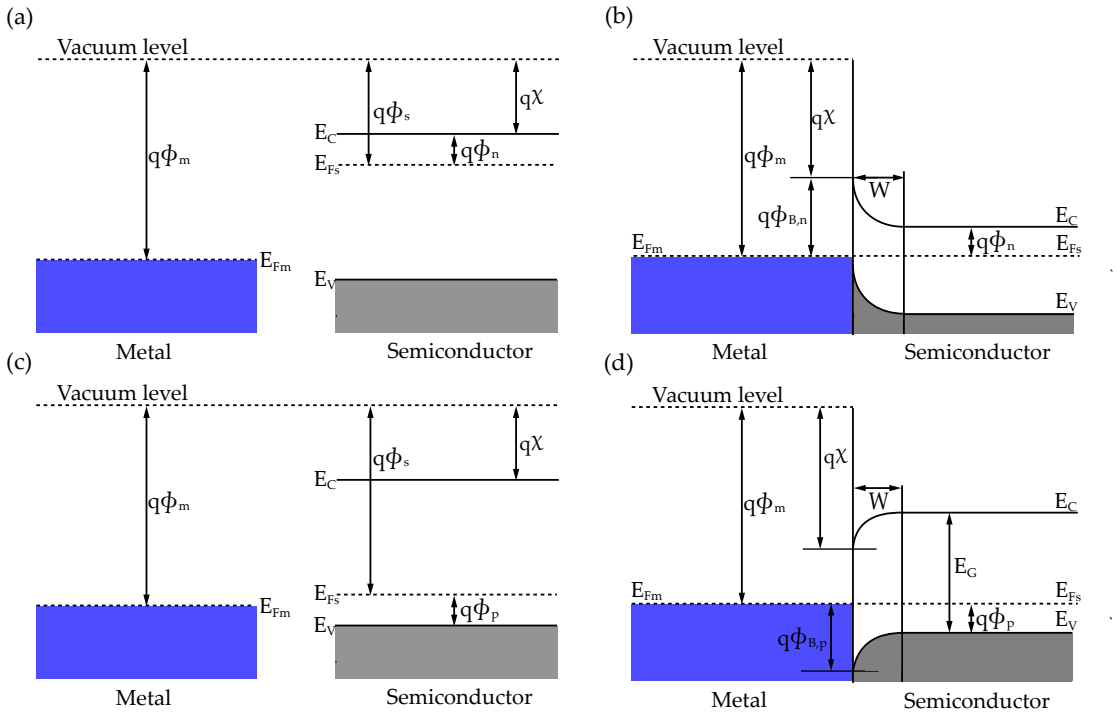

Figure 2.3: *Metal-semiconductor junction. Here the relevant parameters for the metal-semiconductor junction of both the metal and the semiconductor is presented in subfigure (a) for a n-type semiconductor and in subfigure (c) for a p-type semiconductor. When both materials are brought in close contact to each other, a band bending occurs, which depends on the type of the semiconductor and the individual work functions of the materials used. Subfigure (b) shows the n-type semiconductor function, and subfigure (d) the p-type semiconductor function.*
Adapted from [21, 45]

When a voltage is applied across the metal-semiconductor junction the bands bend further, which results in a change of the effective barrier height. This can lead, depending on the voltage, to a higher or lower charge carrier flow. The applied voltage leads to a bending of the semiconductor-sided band. The potential barrier on the side of the metal does not change. [21, 46]
The current transport in a metal-semiconductor junction is mostly determined by majority charge carriers, in contrast to the p-n-junction were it is based on the minority carriers. There are five basic transport processes when a forward bias is applied. Those are the thermionic emission of electrons from the semiconductor into the metal over the Schottky-barrier, illustrated with (1) in figure 2.4, the quantum mechanical tunneling of electrons through the barrier, shown at (2) in figure 2.4, the recombination in the space-charge region, (3) in figure 2.4, the diffusion of the charge carriers into the depletion region, illustrated with (4) in figure 2.4 and hole injection from the metal into the semiconductor (5) in figure 2.4. Because of interface traps there are also further leakage currents. These transport mechanisms are shown for a n-type semiconductor, but also accurate for a p-

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type semiconductor. [21, 46]
Those transport mechanisms can be categorised roughly into three types. The thermionic

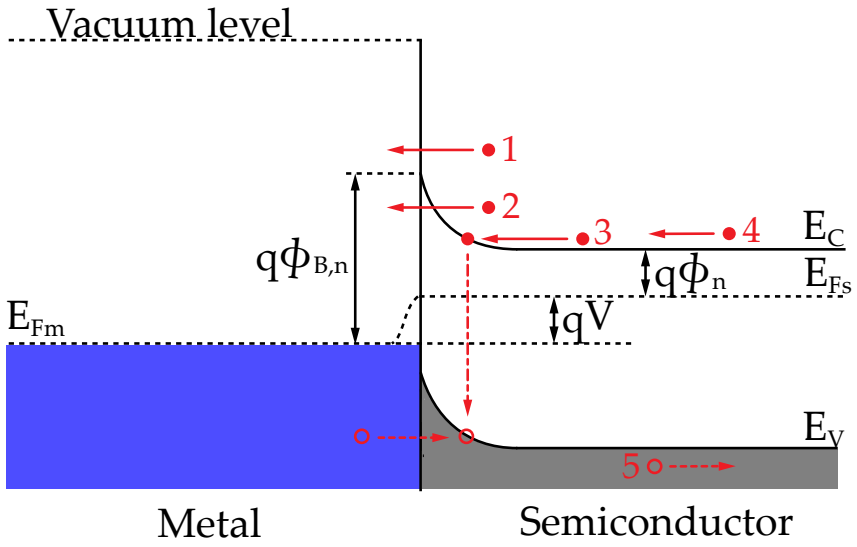

Figure 2.4: *Transport mechanisms of charge carriers, illustrated for electrons, arising at Schottky barriers. In total the charge carrier flow can consist of (1) thermionic emission, (2) tunneling, (3) recombination, (4) diffusion into the depletion zone and (5) holes injected from the metal into the semiconductor.*
Adapted from [21]

emission (TE) is identical with the thermionic emission current. The field emission (FE) is the tunneling current through the barrier where the energies are close to the Fermi-level. The thermionic-field emission (TFE) is a combination of both, where the charge carrier energy is not high enough to get over the barrier but the barrier at higher energy levels is thinner and therefore the tunneling probability is higher, which leads to a higher current. [20, 21]

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For a applied forward voltage V the resulting current through the ideal metal-semiconductor junction can be calculated with the following expression.

$$I = I_0 e^{\frac{qV}{k_b T}-1}$$

Here I_0 is the reverse saturation current, V the applied forward voltage and T the prevailing temperature. The reverse saturation current depends exponentially on the contact potential ϕ_B and the Richardson constant A^* as a proportionality factor.

$$I_0 = A^* T^2 e^{-\frac{\phi_B}{k_B T}}$$

This equation is important to extract the effective Schottky barrier height (eSBH), which is represented through the contact potential ϕ_B.[21, 45]

These metal-semiconductor heterostructures can be used for rectifying fast diodes [21]. If the semiconductor material is contacted on both sides with metal, it forms a metal-semiconductor-metal heterostructure. This leads to the Schottky barrier field-effect transistor SBFET with two individual Schottky contacts [20]. When a metal gate is added to the top, then a metal-insulator-semiconductor heterostructure is built, which is comparable to a metal-oxide-semiconductor (MOS)FET. This resulting SB-MOSFET has many advantages in fabrication and performance like an improved controllability of the leakage currents. [47] These SBFETs are the base of reconfigurable (R)FETs, which are introduced in the following section 2.3. [20]

2.3 Reconfigurable Field-Effect Transistor

In this section the reconfigurable field-effect transistor, or RFET for short, is introduced, as are some related aspects like the electrical transport through heterostructures for differed voltages.

The base for the RFET are two individual Schottky barriers which appear at the junction from metal to semiconductor. A RFET is a type of field-effect transistor, which can be set to a specific type of charge carrier transport, n-type or p-type, depending on an external applied condition, here a voltage. The first step to RFETs were made in the early 2000s, when on an ambipolar Schottky barrier thin-film transistor an additional gate was added to suppress high off-state currents. Following this a reconfigurable FET based on a carbon nanotubes channel with one gate on top and one on the backside, to control the polarity, was fabricated by IBM. To use CMOS processes for the fabrication the concept of RFETs must be brought to a Si base. Walter M. Weber et. al. [48] introduced a reconfigurable SBFET out of a $NiSi_2$/Si/$NiSi_2$ heterostructure and the concept of dual independent gating. In a work of Heinzig et. al. [49] the term reconfigurable was first introduced. [50, 51]

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There are several design possibilities for fabricating a RFET, regarding the gate arrangement of the heterostructure. With the one discussed here, the gates are implemented as top-gates, which means that the contact is located on top of the nanosheet to apply a voltage to control the corresponding band situation. Some typically used gate structures are single top-gate (STG), dual top-gate (DTG), triple top-gate (TTG) and multiple top-gate (N-TG). Another approach for reconfigurability is by using back-gates. In this work the single top-gate and triple top-gate configurations are used and will be further discussed. Those configurations are shown in figure 2.5.
First there is the STG, which is shown in subfigure 2.5a. Here, there is only one gate on top of both metal-semiconductor junctions. These two individual barriers are shifted simultaneously and therefore allow both electrons and holes to pass through the heterostructure, depending only on the applied voltage which results in an ambipolar behaviour. This can be compared to a conventional ambipolar MOSFET.
To distinct the charge carriers passing through the heterostructure there need to be at least a second gate, or as in the case of the TTG structure presented in subfigure 2.5b a third gate. The two gates, which lay over the metal-semiconductor junction are called the polarity or program gates (PG) and configure the corresponding charge carrier mode (n-type or p-type). The two PGs are often connected together, so that both have the same potential, as both Schottky barriers are shifted in the same way. In the middle of these two top-gates there is a third top-gate which is called a control gate (CG). This determines the current through the heterostructure. This CG is used to switch between on- and off-state of the RFET. In the following subsection 2.3.1, about electrical transport mechanisms, the band bending at the TTG RFET is discussed. [20, 51, 52]

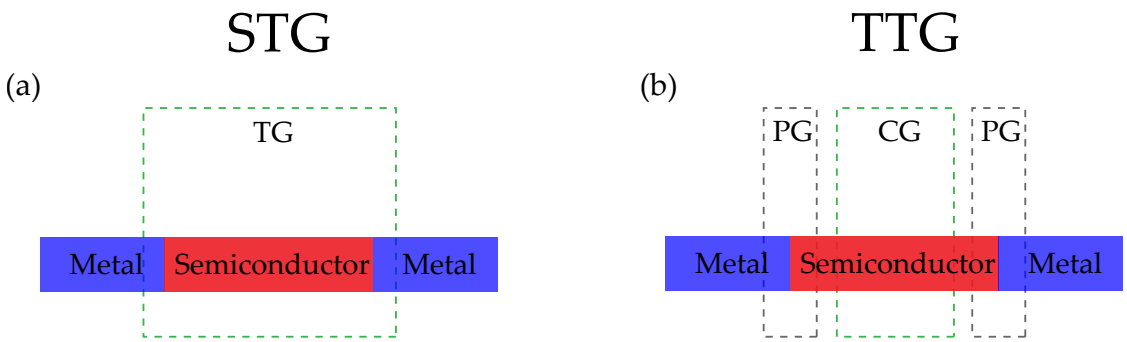

Figure 2.5: *The top-gate arrangements for the metal-semiconductor-metal heterostructure, which are used in this thesis. Subfigure (a) represents a single top-gate (STG) which is consequently a SBFET and subfigure (b) illustrates a RFET with three top-gates (triple top-gate, TTG).*

2.3.1 Electrical Transport Mechanisms

In this subsection the electrical transport mechanism, which can occur during the operation of a TTG RFET will be discussed. Because of the two different charge carrier types passing through the metal-semiconductor-metal heterostructure, which depend on

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the voltages applied at the two barriers, there are two different modes. Is the band bending in a way that holes $h+$ can pass, it is referred to as p-mode or p-type operation. If it is so that electrons $e-$ can pass, it is called n-mode or n-type operation. In figure 2.6 there are the four different cases for the RFET shown. The metal contact which represents the source is labeled with V_S, representing the source-voltage. The metal contact which represents the drain is labeled with V_D, representing the drain-voltage. Which of the contacts are source and drain makes no difference in this case. The source is set to a higher energy level, which corresponds to a lower voltage than the drain contact. This can be seen in figure 2.6. The p-type operation is depicted on the left side of figure 2.6 in subfigures 2.6a and 2.6c. Here, a negative voltage is applied to the PG, which results in a bending of the barriers to higher energy levels, so holes can pass the heterostructure in both cases. Is CG set to a negative voltage, as shown in subfigure 2.6a, then there is no further barrier for holes. This represents the on-state for the p-type operation. Is CG set to a positive voltage, as shown in subfigure 2.6c, then there is an additional barrier for the holes in the semiconductor itself, this represents the off-state for the p-type operation. The n-type operation is shown on the right side of figure 2.6, in subfigure 2.6b and 2.6d. Here, a positive voltage is applied to the PG, resulting in a lowering of the barrier and enabling electrons the passing through the heterostructures. Here subfigure 2.6b shows the off-state of the n-type operation. A negative voltage is applied to the CG, which introduces a further barrier within the semiconductor segment, so electrons cannot flow through the channel. Subfigure 2.6d shows the on-state of the n-type operation where a positive voltage is applied to the CG, which causes no additional barrier and results in an electron charge transport through the channel. [20, 51–53]

There are no specified voltage levels in the figures, because it should represent a very general situation. These levels should be chosen in a way that a sufficient amount of carriers is able to pass in the on-state and is rectified in the off-state. Also the dielectric between the gate and the channel must be capable of withstanding the set voltage.

2.3.2 Advantages over Standard CMOS

In this subsection the advantages of using RFETs will be discussed. The most important advantage of the SBFET is that there is no need for doping of the semiconductor, because the band structure of the heterostructure depends only on the metal-semiconductor junction and the bending of the Schottky barriers. This is also beneficial because doping in the nano-scale is very complex. [20]
Another positive aspect of the RFET is the ability to reconfigure the mode during operation of the device. This conductibility can save several transistors in a logic circuit, compared to CMOS technology. This reconfigurability is not only limited to single transistors, but can be expanded to whole logic circuits that can be reconfigured during run time. Therefore, logic circuits like NAND/NOR switches or more efficient XOR/XNOR circuits can be created. [52, 55, 56]
There is also an advantage in field and hardware security, especially at physically unclon-

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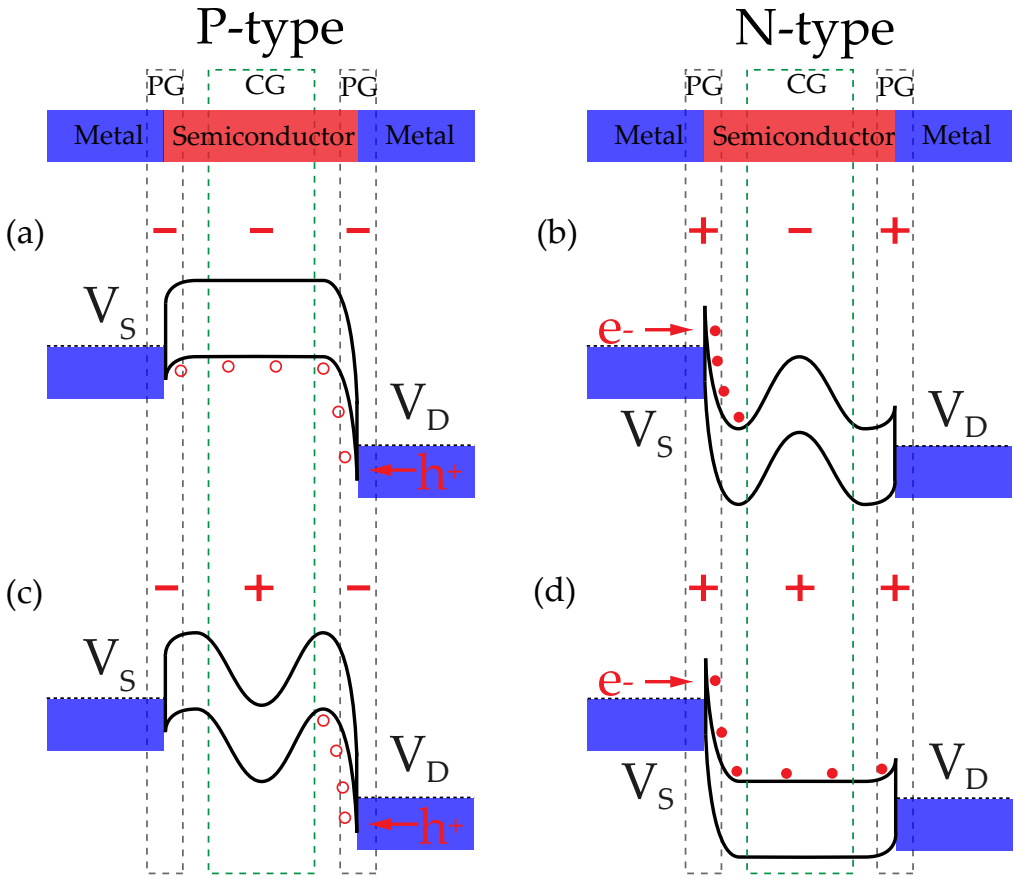

Figure 2.6: *Band bending of the metal-semiconductor-metal heterostructure band structure according to different top-gate voltage and source/drain voltage levels. Subfigure (a) and (c) represent the p-type mode (hole dominated) for the on-state (a) and the off-state (c). Similar to subfigures (b) and (d) for n-type mode (electron dominated), where (b) indicates the off-state and (d) the on-state.*
Based on [52, 54, 55]

able functions and side-channel attacks. [18, 57] Last but not least, the RFET concept also finds applications in the field of neural networks and artificial intelligence. [58]

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Chapter 3

Experimental Techniques

This chapter first focuses on the techniques and methods used to fabricate Ge on SOI RFETs. The second part deals with the electrical characterisation of the fabricated structures.
In section 3.1 the fabrication steps to realise the structures, from the Ge on SOI substrate to the finished STG or TTG structure, will be discussed.
In section 3.2 the electric measurement setup and the characterisation methods used are discussed. The characterisation methods include for example transfer characteristics, output characteristics, PG sweep characteristics, effective Schottky barrier height, effective activation energy and negative differential resistance.

3.1 Fabrication of Germanium on SOI based RFETs

The starting point of the fabrication of the Ge on SOI based RFETs is a Ge layer on SOI wafer. This Ge on SOI wafer consists of a Si substrate and a 100nm buried oxide (BOX) of SiO_2 on top, this is followed by an unstrained Si device layer of 20nm. These three layers form the basis SOI wafer on which the Ge layer is grown. Because of that a 10nm or 15nm buffer layer of Si is grown with MBE. Next the 4nm thick Ge layer is added also via the MBE. On top of the Ge layer a 3nm Si capping layer is added, to prevent the oxidation of the Ge layer. The composition of this initial wafer is shown in figure 3.2, note that the depicted layers are not true to scale in order to highlight the essential parts.

The layers were grown in a Riber SIVA-45 MBE system on SOI in [100] orientation. After a standard substrate cleaning process, the substrates were dipped in hydrofluoric acid (HF 1 %) to remove the native oxide before their introduction into the MBE chamber. The substrates were degassed at 700°C for 20 min. We have deposited a 10 nm thick Si buffer layer, and a 4 nm Ge layer, followed by a 3 nm thick Si capping layer, all deposited at

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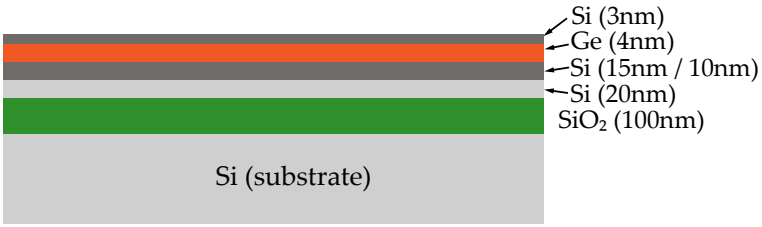

Figure 3.1: *Ge on SOI wafer stack used in this thesis. This shows the according cross-section with the related layers and the thickness of the stack indicated.*

a growth temperature 285°C. The low growth temperature for Ge layers are needed to suppress elastic and plastic strain relaxation.[59, 60]

To fabricate the RFET structures several processing steps must be taken to get the desired heterostructure. This includes lithography, sputtering, etching and vapor deposition. The structures are fabricated in a top-down fashion which results in so-called nanosheets instead of the nanowires, which are fabricated in a bottom-up approach. The following steps must be take to achieve the desired nanostructures:

1. Structuring of Ge nanosheets
   (a) Lithography (laser lithography)
   (b) Reactive-ion etching (RIE)
2. Surface passivation: forming of the gate-dielectric
3. Structuring of the source/drain (S/D)-pads
   (a) Lithography (laser lithography)
   (b) Removal of the dielectric at the S/D contact area
   (c) sputtering of Al
   (d) Lift-off
4. Formation of the metal-semiconductor-metal heterostructure
5. Structuring of the top-gates

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(a) Lithography (laser lithography (for STGs) and electron beam lithography (for TTGs))

(b) Evaporation deposition of Ti and Au

(c) Lift-off

The individual process steps are presented in the following subsection. The different structures, STGs and TTGs, are fabricated on the same chip in a similar fashion.

3.1.1 Structuring of Germanium Nanosheets

This first step of the fabrication defines the desired nanosheet. At this top-down approach the nanostructure is made out of the existing wafer stack. First, laser lithography is used, which can be parted into three steps: spin-coating the photoresist (AZ5214), which is an image reversal resist, baking at 100°C for 60s and laser writing of the structurs (HIMT MLA150 laser writer). The exposed photoresist is removed with a developer (AZ726MIF) and water treatment. The area of the nanosheet is now protected from the reactive-ion etching with SF_6/O_2 which is done for 50s. After this the remaining photoresist is removed via plasma cleaning and aceton.

3.1.2 Gate-Dielectric Formation

The next fabrication step is the passivation layer fabrication. This step is different for the various samples. The surface passivation is needed to implement the gates on top of the heterostructure, this is either an oxide or a dielectric.
To get the passivation layer, the Si surface of the wafer is oxidised via the dry thermal oxidation at a temperature of 900°C for three minutes. This is the same for all three samples. Then for one sample HfO_2 and for the other ZrO_2 is added with ALD at 250°C. This results in a layer with a thickness of around 3.4nm for HfO_2 and around 3.2nm for ZrO_2.
The addition of the high-k dielectrics was made among other things to shift the threshold voltages more to positive voltages, because at sample 1 with only SiO_2 it is to negative.

3.1.3 Structuring of Source/Drain-Contacts

The next step is the fabrication of the S/D-pads. Here, again a lithography step is needed, which is similar to the one at the nanosheet structuring. The only difference is that after the development of the resist every thing is covered except the S/D-pads. The S/D-pats are also defined by the laser writer. Before the Al can be deposited, the passivation layer beneath those must be removed. The thermally grown SiO_2 is etched wet chemically by HF, to be precise with a buffered HF (BHF) solution (7:1). The ALD grown HfO_2 and ZrO_2 are etched physically with a SF_6/Ar RIE process. It is crucial to etch trough the passivation layer to enable a connection to the nanosheet allowing the diffusion of metal into the semiconductor structure, which leads to the desired abrupt metal-semiconductor

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junction.
After this step the Al is added via sputtering and finally a lift-off process, where the underlying photoresist is removed and takes the Al on top with it.

3.1.4 Formation of Metal-Semiconductor-Metal Heterostructure

For the resulting RFET device the formation of a reliable and abrupt metal-semiconductor junction is crucial. This annealing step is made by a flash light rapid thermal annealing (RTA), with a temperature of 500°C in a nitrogen-hydrogen (N_2-H_2) atmosphere. To get a sufficient small semiconducting segment (around 1μm to 2μm) there are several annealing steps taken. This depends on the released contact area from the Al to the nanosheet. These steps vary for the fabricated samples between three and four steps, with a total annealing duration time less than 300s. The corresponding length of the diffused Al segment and the remaining semiconductor segment is captured with an optical microscope, because these dimensions are required for the TG fabrication, where the TGs must be placed over the metal-semiconductor junctions.

3.1.5 Structuring of Top-Gates

The last step in the fabrication of the RFETs is the fabrication of the top-gates, which lay on top of the nanosheet structure. These TGs shift the band structure so that the mode and the current strength through the heterostructure can be controlled. This process is similar for both STGs and TTGs, with different lithography masks.
Because the resolution needed for the TTG structure is much higher, electron beam lithography (EBL) is used. For the STG structure the resolution is similar to the one for the S/D-pads and so here, the laser writer can be used. The process steps for both exposure types are still similar. It starts with the spin-coating of the sample with the resist, for the EBL this is a polymethylmethacrylat (PMMA) resit (AR-P 679.04). For the laser writer the same resist as for the structuring of the nanosheets (AZ5214) was used. This is followed by the exposure with either laser light or electron beam and the resist is developed. After this the next process step is the evaporation of titanium/gold. Here, 10nm Titanium (Ti) and 100nm Gold (Au) are deposited via electron-beam evaporation. Ti has a better adhesion and also determines the work function and Au provides a better contact for the needle probing system and prevents the Ti from oxidising. The last step of the fabrication process is the lift-off step, where the resist and therefore the Ti/Au on top is removed via acetone. This releases the desired TGs above the nanosheet.

3.1.6 Final Structure

The final TTG RFET is shown in figure 3.2. Subfigure 3.2a shows a 3-D stack, subfigure 3.2b a cross-section and subfigure 3.2c a top-view. The contacting pads shown in subfigure 3.2a and 3.2c are only indicated thematically and so are not in scale, as are the single layers in the stack. Here, it can be seen that the PGs for the TTG structures are connected together. As seen in subfigure 3.2c the PGs are directly above the metal-semiconductor junctions, this is crucial for the functionality of the RFET, because otherwise the barriers

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can not be manipulated. Tho get the position of this junctions for the lithography mask the annealed samples are measured via an optical microscope.

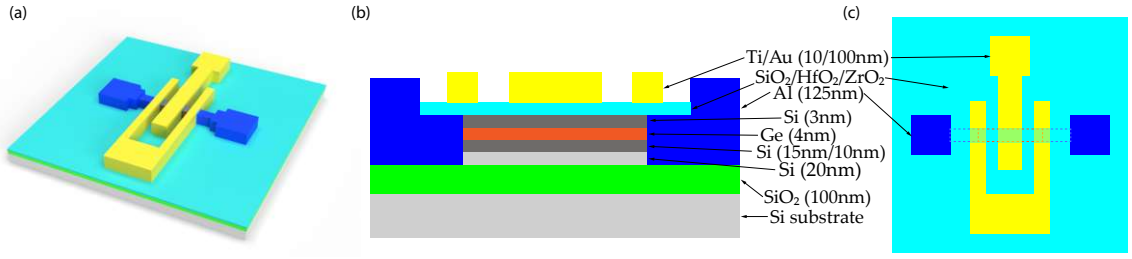

Figure 3.2: *Fabricated TTG RFET structures. Subfigure (a) shows the 3-D stack from the TTG RFET structure with indicated TGs and S/D-pads. Subfigure (b) shows the Cross-section of the TTG RFET with the layers and TGs indicated. Subfigure (c) shows the top-view of the RFET structures where the nanosheet, below the passivation layer, is indicated with dashed lines. The blues dashed lines represents the diffused Al, whereas the orange dashed line represents the semiconducting segment.*

The different RFET structures are fabricated on the same chip. On one chip 60 individual structures are placed. The number of STGs and TTGs vary from sample to sample, because which structure can be built is determined from the length of the semiconductor segment. This length is dependent on the fabrication process, especially the annealing process. Also because of the different segment lengths the dimensions of the individual gates and the gaps between them also vary between the different structures.

3.2 Electrical Characterisation of Germanium on SOI based RFETs

After the fabrication methods, the measurement setup and the methods to electrically characterise the samples need to be presented. The characterisation is needed to demonstrate their functionality and compare the electrical behaviour of the devices. Because the devices are RFETs typical FET characteristics, like transfer and output curves are measured. Also the effective activation energy is determined by using the temperature-dependent measurement of the output characteristics. The electrical characterisation of the nanostructures is based on the book "Semiconductor Material And Device Characterization" by D.K. Schroder [61].

The first subsection will introduce the measurement setup that was used, including the probe station and the analyzer. In the following subsections the transfer characteristic, output characteristic, the PG sweep characteristic, the effective Schottky barrier height measurement and the effective activation energy measurement methods will be discussed. Then the measurement and evaluation method of the negative differential resistance (NDR). And finally evaluation methods of the characteristics are presented.

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3.2.1 Measurement Setup

The electric characterisation was made by a measurement setup, which basically consists of two individual parts, those are the needle probe station and the connected analyzer. The probe station was a Cascade Summit 11000B-AP and was connected to a Keithley 4200-SCS semiconductor characterization system. The probe station features four micro manipulators with a range of motion of 1,27cm in X-, Y- and Z-direction and a resolution of $2\mu m$. The needle diameter is $19\mu m$. The analyzer is equipped with four source measurement units (SMUs) which can supply a certain voltage and measure the resulting current. The resolution of the measurement setup lays in the femto-ampere range. For the temperature-dependent measurements the built-in heatable chuck and the ERS Air Cool SP72 temperature controller are used.

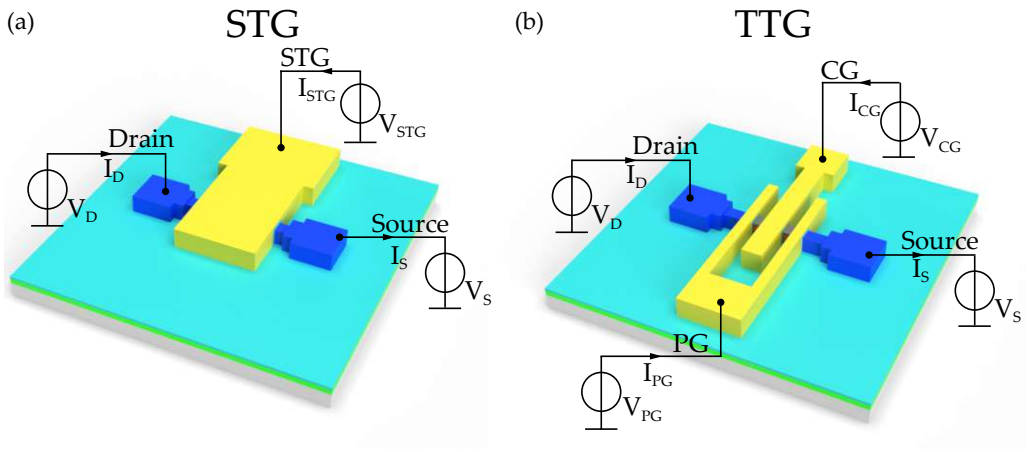

Figure 3.3: *Measurement setup for STG-devices in subfigure (a) and TTG-devices in subfigure (b), with the corresponding designations.*

The electrical connection and the designations of the different structures fabricated in this thesis are shown in figure 3.3. The measurement setup for the STGs are shown in subfigure 3.3a, where the S/D-pads and the STG is connected. As the devices are symmetric the choice of the source- and drain-pads is arbitrary. As indicated by the voltage source the voltage level can be set independently for both source and drain. The bias-voltage which is the voltage drop along the nanosheet is referred as V_{DS}. This also indicates the direction of the voltage, from drain to source. The current through the channel I_{DS} is referred to as I_D, because the difference between drain and source current is practically non existent for a properly functioning structure. The current through the STG should be insignificantly small or ideally zero, so the the current trough the nanosheet is only determined by the voltage set at the TG. The leakage current is defined by the current passing though the oxide and depends on the current strength through the channel. This leakage current reaches from femto- up to pico-ampere. If it reaches into the nano-ampere range, then there is a risk of destruction for the nanostructure. Mostly for the dielectric between the S/D-pads and the TG. This current can be measured by the source-measure-unit (SMU) which drives the TG or by calculating the difference between source and drain current.

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Subfigure 3.3b shows the measurement setup for a TTG structure with its designations. The difference to the STG structure is, that there is a CG connected to a voltage source V_{CG} and two PGs connected together to a fourth voltage source V_{PG}. Everything else mentioned above remains still valid.

3.2.2 Transfer Characteristics

The transfer characteristic shows the behaviour of the device for a changing voltage level at the TG and a fixed bias voltage. The curve shows the drain current I_D over the swept TG voltage. The absolute value of I_D is depicted. From these curves the on- and off-state currents as well as the threshold voltage V_{th} and the sub-threshold slope (STHS) for both n-type and p-type operation can be extracted.
For the STG-devices, as shown in subfigure 3.3a, the source- and drain-voltage levels will be set to a fixed value and the STG voltage will be swept. The expected behaviour is ambipoloar, which corresponds to the SBFET. This means for both a negative and positive TG voltage there is a current flow I_D through the nanostructure.
Considering the TTG-devices this ambipolarity is suppressed, because this is a reconfigurable device. To achieve this the PG voltage is set to negative levels for p-mode operation and to positive levels for n-mode operation. Similar to the STG measurement the bias-voltage remains set and the CG is swept. Because of the two different operation modes, there are two transfer curves representing p-type and n-type operation.

In this thesis the drain voltage level is mostly set to +1V and the source voltage level to -1V, this results in a bias-voltage V_{DS} of 2V. For the TGs the voltage levels are set in a way, so that there is a adequate control of the transfer curves, while not damaging the device. To select the n-type or p-type operation the PG is set to maximum positive or maximum negative voltage level. The CG or STG is swept from the one maximum value to the other maximum value. Here, for both modes the measurement is taken from the off-state to the on-state, this is called a "single" measurement. For a "double" measurement the sweep is also performed in the reverse direction, which means there is one single measurement from off- to on-state and then one from on- to off-state.
This transfer characteristic measurement is also taken as a function of the temperature. Therefore the built-in heating station and temperature controller are used for setting the required temperature. The transfer characteristics are taken from room temperature (24°C) in 25°C steps up to 125°C, which results in five temperature steps.
The outcome of this transfer characteristics are presented in the result chapter, for STG structures in section 4.3 and for TTG structures in section 4.4.

3.2.3 Output Characteristics

For the output characteristic the bias-voltage V_{DS} is swept and the drain current I_D is measured. The voltage level of the TG is fixed for the measurement of on I/V curve. This measurement is performed for several different TG voltage levels. If the TG is considered

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as an "input", the drain current in dependency of the applied bias-voltage symbolizes the "output" of the transistor [21]. This explains the name of this characteristic. The output characteristic consists of several output curves. The output characteristic will be plotted as a so-called colour map, this is a 2-D representation of the output characteristic with the bias-voltage V_{DS} on one axis and the "input" TG voltage on the other axis. This can therefore be referred to as bias spectroscopy. The current strength is represented in a related color scheme.

For the output characteristic measurement both the bias-voltage and the TG voltage are swept. For a STG device the swept voltage is the TG voltage V_{STG} and for a TTG device it is the CG voltage V_{CG}. The bias-voltages V_{DS} are swept in both cases. For the TTG configuration there are again two output characteristics, one for p-type and one for n-type operation.
The voltage levels for the output characteristic are similar to the ones for the transfer characteristic measurements. The bias-voltage V_{DS} is also applied symmetrically, which means $V_D = -V_S$, for all the different voltage levels during the sweep. The temperature dependency of the output characteristics are also measured. The temperature runs are again made from room temperature (24°C) up to 125°C in 25°C steps. This measurement data is also needed to determine the effective Schottky barrier height, subsection 3.2.5 and the effective activation energy, subsection 3.2.6.
These output characteristics measurements are presented in section 4.5 for STG devices and in section 4.6 for TTG devices in the results chapter.

3.2.4 PG Sweep Characteristics

The PG sweep characteristic shows a specific aspect of reconfigurable devices. Here, the transfer characteristics for different PG voltage levels V_{PG} for both n-type and p-type operation is captured. This measurement is again a two parameter sweep, this time with the CG voltage V_{CG} and the PG voltage V_{PG} as parameters and the drain current I_D is once again measured. The transfer curves are captured for different PG voltages, this means the PG sweep characteristic is a more general transfer characteristic. This measurement can only be performed at the TTG devices, because the STG devices cannot be reconfigured. The PG sweep characteristic shows the switching behaviour between p-type and n-type operation, of the device. So it shows at witch PG voltages p-type and n-type operation can be expected.

For the PG sweep characteristic the PG voltage V_{PG} is set to a constant value and the CG voltage V_{CG} is swept before the PG voltage is set to the next sweeping step. The voltage levels are chosen the same as for the transfer and the output characteristic. The bias-voltage is again set symmetrically as $V_D = -V_S$. The measurement shows at the beginning the characteristic behaviour for one charge carrier type and at the end the transfer characteristic of the other charge carrier type. This transfer curves are again

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plotted in a 2-D colour map, with V_{PG} on one axis and V_{CG} on the other axis, the current is again represented in the colour.
The PG sweep characteristic measurements are shown in the results chapter at section 4.7.

3.2.5 Effective Schottky Barrier Height Measurement

The effective Schottky barrier height (eSBH) depends on the materials used and the applied voltage along the heterostructure, as stated in the theory chapter at section 2.2. To get the eSBH there are several different approaches possible. The one used in this thesis is the current temperature approach or I/V(T)-approach according to Schroder [61]. In order to use the simplified assumptions as introduced in subsection 2.2.1, a few assumptions must be made. One being that the barrier height is grater than k_BT (25.85mV at 27°C) and a small bias-voltage to avoid the barrier-lowering effects. [21, 61, 62]
This introduced method is thought for conventional semiconductor-metal junctions. The complete heterostructure used in this work consists of two individual metal-semiconductor junctions, so the activation energy needed for the charge carrier flow trough the channel can be approximated as effective SBH (eSBH). It is also difficult to distinguish between the different transport mechanisms, as introduced in section 2.2.1. It is abstracted by the eSBH within the total current flow through the structure. The applied voltages on different gates also cause a much more complex situation, because the potential at the barriers depend on multiple sources. This also causes a charge carrier injection into the semiconductor segment, which effects the electrical circumstances at the interface. Because of all the issues it is difficult to find a physically correct expression for the resulting barrier height. Therefore the used method is only a careful estimation.
To determine the eSBH output characteristics at different temperatures must be measured. For this measurement only the STG devices are used, because they have the least complex configuration and so a better approximation can be made. The temperature is again swept from room temperature (24°C) up to 125°C in 25°C steps. The bias-voltage is only set to positive voltages and the STG voltage V_{STG} is chosen as for the corresponding transfer measurements.
The specific way how the eSBH is calculated is described in the master thesis of Andreas Fuchsberger [63]. His python scrips are used for the evaluation of the eSBH of this work. The measurement and evaluation results of the samples used are presented in the results chapter in section 4.8.

3.2.6 Effective Activation Energy Measurement

The eSBH is the effective activation energy of the heterostructure at the zero-bias point (V_{DS}), because of this the effective activation energy can be determined with the same method as described in the eSBH section in [63] without extrapolating the zero-bias point. For the effective activation energy the output characteristics over different temperatures are used. The temperatures are the same as for the eSBH measurements. The effective activation energy is captured at the TTG devices and so there are two activation energy

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maps for both p-type and n-type operation for the heterostructure. The activation energy maps are 2-D maps with the bias-voltage V_{DS} on one axis and the CG voltage V_{CG} on the other axis, the effective activation energy values are represented by the colour scheme.
For this measurement the voltages set are the same as for the output characteristic measurements, because those are used to calculate the effective activation energy. Again a more in depth look how the effective activation energy is calculated is provided by [63].
The results of the effective activation energy measurement of this thesis are shown in section 4.9 of the results chapter.

3.2.7 Evaluation of Characteristics

Some of the characteristic parameters of the structures can be extracted from the captured curves. The transfer characteristic is especially interesting. In this subsection the out of the transfer curves evaluated characteristics are introduced. These will be presented in the sections 4.10 and 4.11.
For RFETs one key figure is the symmetric behaviour of the different charge carrier operation types. But also the on-state to off-state current ratio is important, because it determines the (static) power consumption. For the power consumption also the threshold voltage V_{th} and the inverse sub-threshold slope (STHS) are of interest. [17, 20]
The symmetry of the on-state currents for operation modes of the RFET is evaluated. For both operation modes of the TTG structure the on-state and off-state drain currents are captured, as are the ratio from on-state current to off-state current. For this evaluations a Python script is used to extract the values out of the transfer characteristics of the individual structures. For every sample the mean value of ten representative TTG structures is calculated and used for the evaluation of this sample.

3.2.7.1 Threshold Voltage Evaluation

There are several methods to determine the threshold voltage V_{th}, according to Schroder [61]. For this thesis a combination of the linear extrapolation and the transconductance method is used. Therefore the fist step is to extract the transconductance g_m from the transfer characteristic. This is done by building the first derivation of the drain current I_D regarding the applied CG voltage V_{CG}, $g_m = dI_D/dV_{CG}$. Then a vertical line from the maximum of the transconductance to the corresponding transfer curve is drawn. At the intersection point at the transfer curve a linear tangent is applied. The threshold voltage is determined by the intersection of this linear tangent and the CG-axis. To have a better comparability to other values, the threshold voltage V_{th} is also determined directly from the transfer characteristic with the above mentioned Python script. Here, again the mean value of ten representative samples is taken for the evaluation.
The threshold voltages V_{th} for the different samples are presented in the subsection 4.10.1 of the results chapter.

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3.2.7.2 Sub-Threshold Slope Evaluation

For the evaluation of the inverse sub-threshold slope (STHS) the transfer characteristic is needed as well. Similar to the evaluation of the threshold voltage V_{th} the semi-logarithmic transfer curve is derived from the CG voltage V_{CG}. Here, the maximum value of the derivation at voltage values between on- and off-state is considered the sub-threshold slope. This evaluation is also implemented in the Python script.
The results of the STHS evaluation is presented in the subsection 4.10.2 of the results chapter.

3.2.8 Negative Differential Resistance Measurement

The negative differential resistance (NDR) is attributed to the transferred electron effect which is a transport effect and follows the Ridley-Watkins-Hilsum theory [64] and is also known as the Gunn-effect [65]. For this effect sufficiently high electric fields must be applied. This results in the transfer of electrons with a low effective mass, transported from the conduction band valley to a nearby heavy mass valley [65]. This electrostatically tunable NDR is observable in Ge devices at room temperature [23].

For the measurement of the NDR the drain current I_D is measured while the drain voltage is swept from 0 to a sufficient voltage where the NDR can be observed. In this case a drain voltage V_D of 5V is enough. The source voltage V_S is held at 0V. To again get a 2-D depiction of the parameter the STG voltage V_{STG} or CG voltages V_{CG} must be swept. In this case CG voltage V_{CG} sweep is made per hand, because between the measurement a 3min beak must be taken to prevent a degradation of the device. The voltage level of STG V_{STG} or CG voltage V_{CG} is set similar to the transfer characteristic measurement and then for every measurement reduced in 0.5V steps. For the TTG devices the PG voltage V_{PG} is set to the highest CG voltage used. For the TTG devices there was also a measurement taken where the CG voltage V_{CG} and the PG voltage V_{PG} are exchanged, so the sweep was performed at the PG voltage V_{PG} and the CG voltage V_{CG} was fixed.
The NDR is depicted in two different 2-D color maps. In both cases the STG voltage V_{STG} or the CG voltage V_{CG} is at one axis and the drain voltage V_D is on the other axis. The difference between the two color maps is the value depicted through the colour scheme. In the first case drain current I_D is depicted in the other case the derivation of the drain current I_D over the drain voltage V_D is shown.
The results of the NDR measurement of this thesis are shown in the results chapter in section 4.12 for the STG structures and in section 4.13 for the TTG structures.

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Chapter 4

Results and Discussion

In this chapter, the results of the fabrication and measurements, explained in chapter 3, will be presented.
In the first section the different samples with the different passivation layers will be discussed. A structural investigation with TEM and SEM images of the structures is included. In the next section, section 4.2, the overall project evolution is presented. Here, the different samples fabricated and the ideas behind the steps taken for improvement are discussed. After this the following sections show the the measurement results for the three samples, which are shown in the first section of the chapter. Here, measurements fore both STG and TTG devices are shown. The last sections present the evaluation of the characteristics transistor parameters and finally the comparison of the fabricated RFETs with other existing RFETs in literature.

4.1 Fabricated Devices

For this thesis, there where five samples fabricated and characterised on the basis of the introduced Ge on SOI wafer. The difference of those samples lay in the different passivation layers. A pure SiO_2 as well as an addition of HfO_2 and ZrO_2 are made, so that the influence of those different passivation layers could be investigated. In this section the fabricated devices are presented and their differences are discussed, according to the TEM investigation that has been made. Also the fabricated TG configurations are presented as SEM images.

To refer to the fabricated and characterised samples of this thesis the designations are made as follows.

- Sample 1, with pure SiO_2 as gate-dielectric

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- Sample 2, with SiO_2 and HfO_2 as gate-dielectric
- Sample 3, with SiO_2 and ZrO_2 as gate-dielectric
- Sample 4, with SiO_2 and a thinner ZrO_2 layer as gate-dielectric
- Sample 5, with both a thinner SiO_2 and ZrO_2 layer as gate-dielectric

As seen above, there are in total five samples with different gate-dielectrics made for this work. The order of the samples in the list reflect the fabrication order. For the first sample only SiO_2 was used, then a combination of SiO_2 and HfO_2 or SiO_2 and ZrO_2 and for sample 4 and sample 5 the thickness of the layers has been changed. This will be discussed in more detail in the project evolution section below.

The above mentioned TEM investigation is performed with a Tescan Lyra FIB/SEM and the images are the images are taken with a Thermo Fisher Scientific Titan Themis 200 G3 outfitted with a SuperX detector used for electron diffraction X-ray spectroscopy (EDX) maps. To determine the structure of the stack with the layer thicknesses and compositions two different cuts are performed. One TEM cut along the nanosheet structure, which means from drain to source pad, to get the cross-section of the front view. The other TEM cut across the nanosheet to identify the related layer thickness of the gate-dielectric. The cross-section of the front view is presented in figure 4.1 and the crosswise TEM cuts are presented in the subsections below, for the sample with pure SiO_2 as passivation in subsection 4.1.1 and the ones with SiO_2 and ZrO_2 passivation in subsection 4.1.2. For the sample with SiO_2 and HfO_2 as passivation no TEM investigation was made, but it can be assumed that it is very similar to the one with ZrO_2.

The high resolution scanning (HRS)TEM cut is indicated in subfigures 4.1a with the red cut line. Subfigure 4.1b shows the stack composition of the Ge on SOI wafer. As shown in figure 3.2 in the experimental techniques chapter, the wafer stack consists of a Si substrate, which is followed by a 100nm thick SiO_2 BOX and a 20nm unstrained Si layer, a 10nm MBE grown Si layer, the 4nm Ge layer and finally a 3nm Si capping. Those layers are indicated in subfigure 4.1b. It also can be seen that the Al only diffuses into the nanosheet which is released by etching and not into the BOX. In subfigure 4.1c the metal-semiconductor junction is shown more closely. Here, it can be seen that the Si cap together with the Ge layer and the Al are forming a Al-Si-Ge junction. In figure 4.1d an EDX image of the a Al-Si-Ge junction is shown. Here, it is shown that the Al (green) diffuses into the nanosheet and is exchanged completely with the other elements, here, Si (red) and Ge (blue). It should also be mentioned that the layer above the Si capping which can be seen in figure 4.1b in grey/white and in figure 4.1c in black is a carbon layer needed for the TEM investigation.

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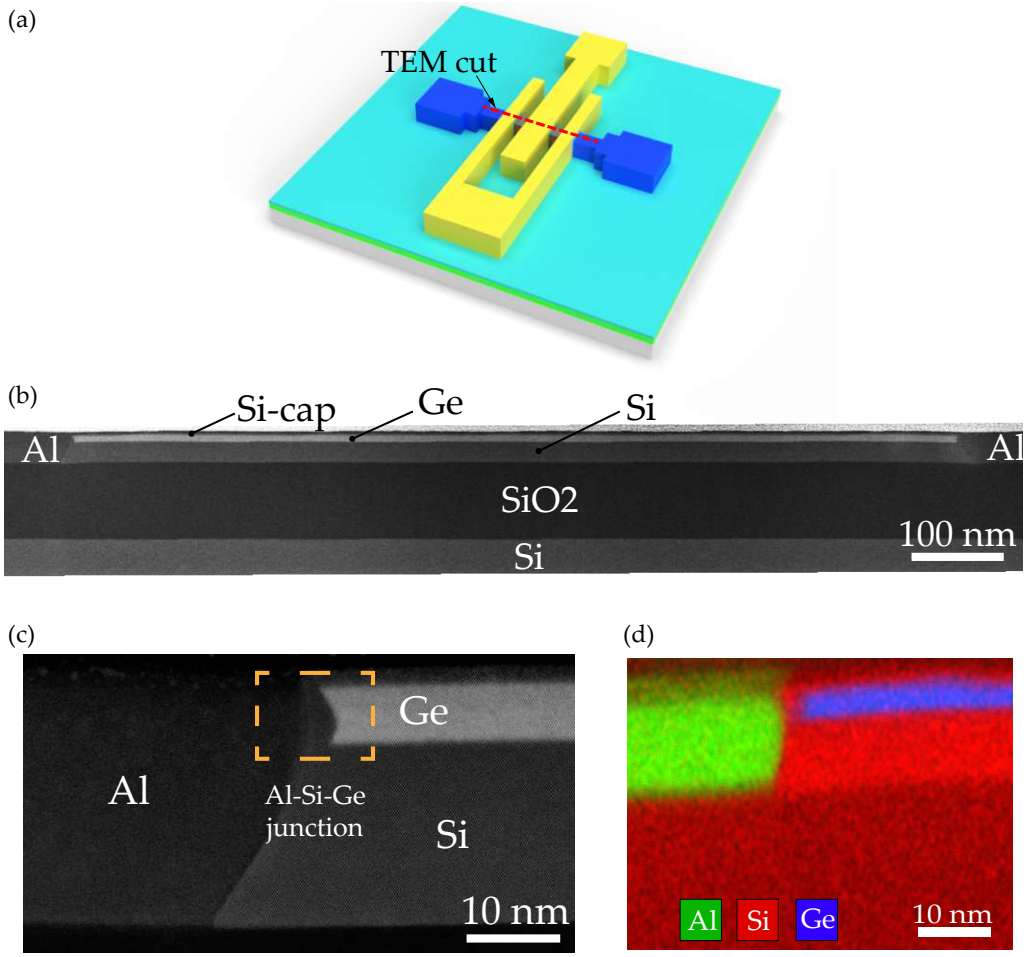

Figure 4.1: *Cross-section TEM cut of the front view of the corresponding wafer stack. Subfigure (a) shows the 3-D TTG model with the TEM cut indicated, subfigure (b) the HRSTEM image of the front view cross-section, subfigure (c) a detail view of the HRSTEM image at the metal-semiconductor junction and subfigure (d) the EDX image at the corresponding metal-semiconductor junction.*

Since there where two samples sent to the TEM analysis the next tow subsections will show the results of those.

4.1.1 Germanium on SOI based RFETs with SiO_2

This subsection shows the results for sample 1, with a passivation of pure SiO_2. This passivation was made via dry oxidation at 900°C for the duration of 3min. For a estimate of the oxide thickness an ellipsometer was used. For a more accurate result the TEM measurement was made.

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The images of the TEM and EDX scans of sample 1 are presented in figure 4.2. Here, figure 4.2a shows the TEM cut made to determine the oxide thickness and the layer composition transverse to the nanosheet including the TG. Subfigure 4.2b shows the HRSTEM along the cutting line. Here, it can be seen that on top of the layer stack as seen in figure 4.1 a SiO_2 layer is formed, which is followed by the Ti/Au for the TG. TEM images suggest that the Si capping is completely oxidized, which was intended. Because of the thinness of the Ge layer it is rather difficult to see.
So with this investigation it was shown that the passivation layer thickness of sample 1 is about 4.5nm.

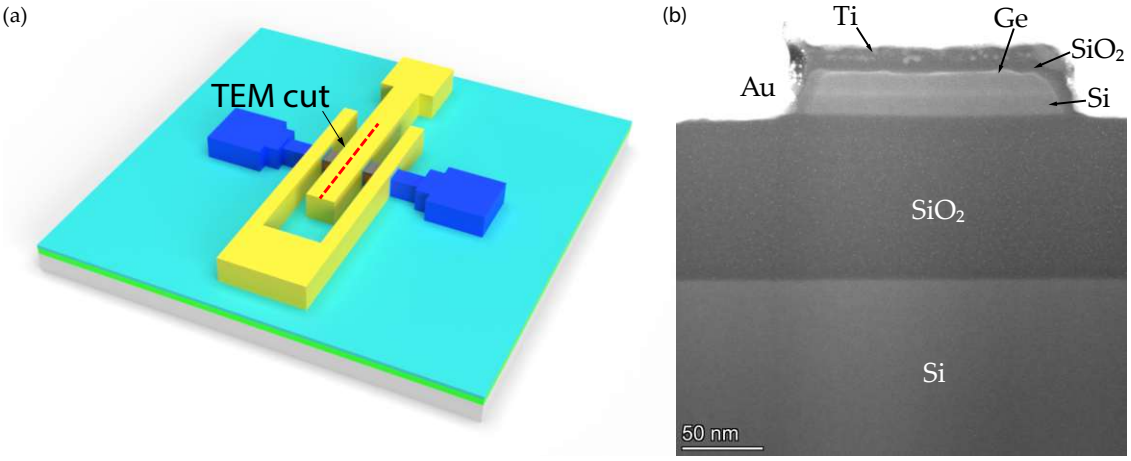

Figure 4.2: *Cross-section of the transverse TEM cut of the corresponding wafer stack including the TG layers of sample 1. Subfigure (a) shows the 3-D TTG model with the TEM cut indicated, subfigure (b) the HRSTEM image of the structural cross-section.*

4.1.2 Germanium on SOI based RFETs with ZrO_2

In this subsection the TEM analysis of sample 3 is shown. For sample 3 on top of the SiO_2, which was again dry oxidized at 900°C for 3min, a ZrO_2 layer was grown with the ALD at a temperature of 250°C. Again the oxide thickness was first estimated with the ellipsometer and then analyzed with the TEM.

The images of the TEM and EDX scans of sample 3 are presented in figure 4.3. Here, again figure 4.3a shows the 3-D TTG model where the TEM cut is indicated, to determine the layer composition of the fabricated stack including the TG and to determine the passivation layer thickness. The HRSTEM image is shown in figure 4.3b. The formed layers are labeled. Here, it can be seen that on top of the Ge on SOI stack the SiO_2 layer is built followed by the ZrO_2 layer and after the gate-dielectric the Ti/Au layer of the TG. Subfigure 4.3c shows the EDX scans and the more detailed depiction in subfigure 4.3d. Here, it can be seen that again the Si capping is completely oxidized to form the SiO_2 passivation. On top of the passivation the ZrO_2 layer can be seen and finally the Ti and Au layers of the TG can be seen.

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With this investigation it was determined that the passivation layer thickness of sample 3 is around 7.9nm, with the SiO_2 layer being 4.4nm and the ZrO_2 layer being 3.5nm.

For sample 2 there was no TEM analysis made, so the passivation layer thickness was only measured with the ellipsometer and was therefore estimated to 7.9nm, where the SiO_2 layer was around 4.5nm thick and the HfO_2 layer around 3.4nm.

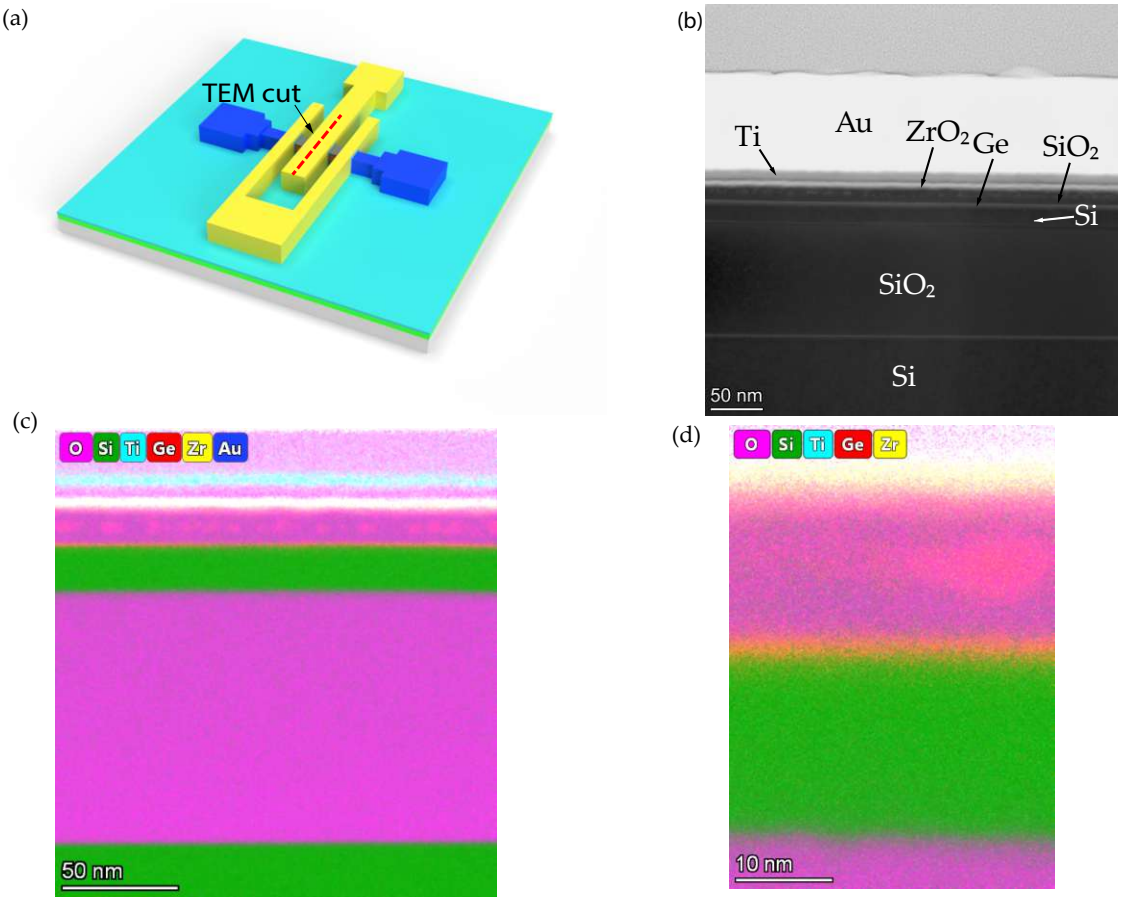

Figure 4.3: *Cross-section of the transverse TEM cut of the corresponding wafer stack including the TG layers of sample 3. Subfigure (a) shows the 3-D TTG model with the TEM cut indicated, subfigure (b) the HRSTEM image of the structural cross-section, subfigure (c) the EDX image of the structural cross-section and subfigure (d) the detail view of the EDX image from the corresponding structural cross-section and the according layer material composition.*

4.1.3 Fabricated Top-Gate Arrangements

After the different samples used in this work, this subsection now shows the different TG structures that were fabricated. Both STG and TTG configurations are used on all of the samples mentioned above. The following figure, figure 4.4, shows SEM images of those two TG configurations.

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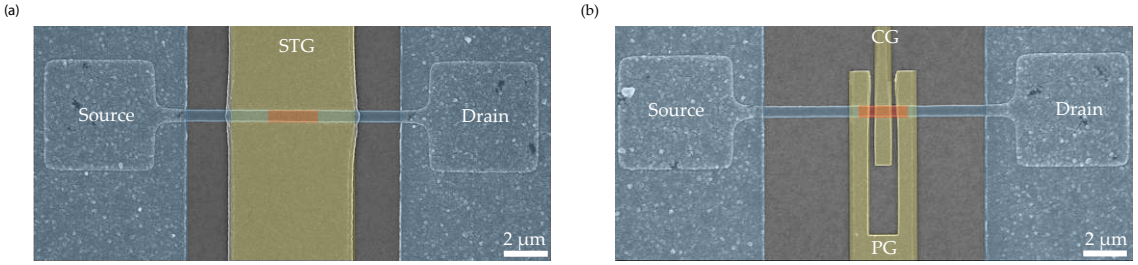

Figure 4.4: *SEM image of the different TG configurations used in this work with the associated TG desigantions. Subfigure (a) shows a coloured SEM image of a STG structure and subfigure (b) a coloured SEM image of a TTG structure.*

The SEM image of the TG arrangements are colourised for presentation clarity. Blue is used for the Al, red for the semiconducting segment and yellow for the Ti/Au. Also the S/D-pads and the TGs are designated like the ones used in the measurement setup described in the experimental chapter 3.2.1 in figure 3.3. Here, it can also be seen that the nanosheets are designed in a so-called T- or bone structure, which means that the end of the nanostructure is widened, in this case with a square. This is made to provide a bigger contact area, which enables a more reliable fabrication of the structure, because it is critical to have a good contact between the nanosheet and the added Al of the S/D-pads for the diffusion and so also for the formation of a reliable metal-semiconductor hetero-structure. The resulting semiconductor segment is only indicated, because it is not visible under the TGs in the SEM image. The dimensions of the in-diffused Al and the so resulting semiconducting segment are measured with a optical microscope before the TGs are placed.
Which TG configuration is used and its dimensions are dependent on the length of the semiconducting segment. For short segments, which are below 1.5μm mostly the STG configuration is used. Here, the top-gate has a width of 5μm and is the same for all STGs. For longer segments above 1.5μm the TTG configuration is used, because the PGs must lay above the metal-semiconductor junction, the resulting width for the TGs and the gaps between them vary. The width for the PGs lays between 450nm and 600nm and the gap between the PG and CG between 300nm and 350nm. The width of the CG is calculated from the length of the semiconducting segment and the chosen PG-width and gap-widths and lays between 400nm and 2μm.

The device dimensions, particularly the width, height and length of the channel are measured with different methods. The channel length which is the length of the semiconducting segment and the channel width which is again the width of the semiconducting segment are measured with an optical microscope, before the TGs are fabricated. Here, capturing the length of the semiconducting segment before the TG fabrication is necessary because the dimensions are needed to positions the TG in the correct location, especially for the TTG structures. The width of the channel are between 400nm and 1μm for the various

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samples of this work. The channel height, which is also the structure height of the nanostructure is taken from the TEM investigation. This measured channel height is about 32nm. These geometric characteristics are required, to determine, some of the electrical characteristics, like the current density through a device.

4.2 Evolution of the Project

As already mentioned in the chapter before, the numbering of the individual samples represent the fabrication order and therefore also the evolution of the project as a whole. This section will emphasise the ideas behind the selected various gate-dielectrics during this work and so the overall evolution. This projects evolution is best demonstrated by the transfer characteristics for the TTG RFET configuration of the different samples. This is depicted in figure 4.5.

The purpose of this project was to fabricate a RFET structures which have a good on-state-symmetry, that means the on-state currents in p-type operation and n-type operation should be as equal as possible. The On-state currents should also be reasonable high and the off-state current low.

For the first sample, sample 1, the Ge on SOI wafer was used with a passivation of pure SiO_2, because the Ge on the wafer is caped with Si so that no Ge oxide, but a native SiO_2 can form. The results of the TTG transfer characteristic of sample 1 are presented in subfigure 4.5a. The transfer characteristics exhibit two y-axis, the right one shows the corresponding absolute value of the drain current measured and the right one the associated drain current value normalised over the channel width. Here, the left y-axis is scaled equally for all subfigures of figure 4.5, but the scaling of the right y-axis depends on the corresponding width of the structures. Because of the similar widths of the nanosheets the range of the normalised y-axis are also similar. The transfer characteristics of sample 1 are captured at a symmetric bias-voltage V_{DS} of 2V and a PG voltage V_{PG} of +5V for the n-type operation and -5V for the p-type operation. Here, it can be seen, that the drain current I_D at the n-type operation is higher than the one of the p-type operation. The hysteresis for Ge already is quite good. But the threshold voltages V_{th} of both operation types are shifted to the left, so towards negative voltages. This has the effect that the RFET only barley turns off for the n-type operation at -5V.
To improve the threshold voltage V_{th} shift as well as the symmetry of the devices the next step was to fabricate to devices with high-k dielectrics. Here, hafnium dioxide HfO_2 and zircon dioxide ZrO_2 was used. HfO_2 has been chosen because it had been used at a previous project and showed good results with a HfO_2 and SiO_2 mixture. ZrO_2 was tested because it had the potential to shift the threshold voltage even further than HfO_2.

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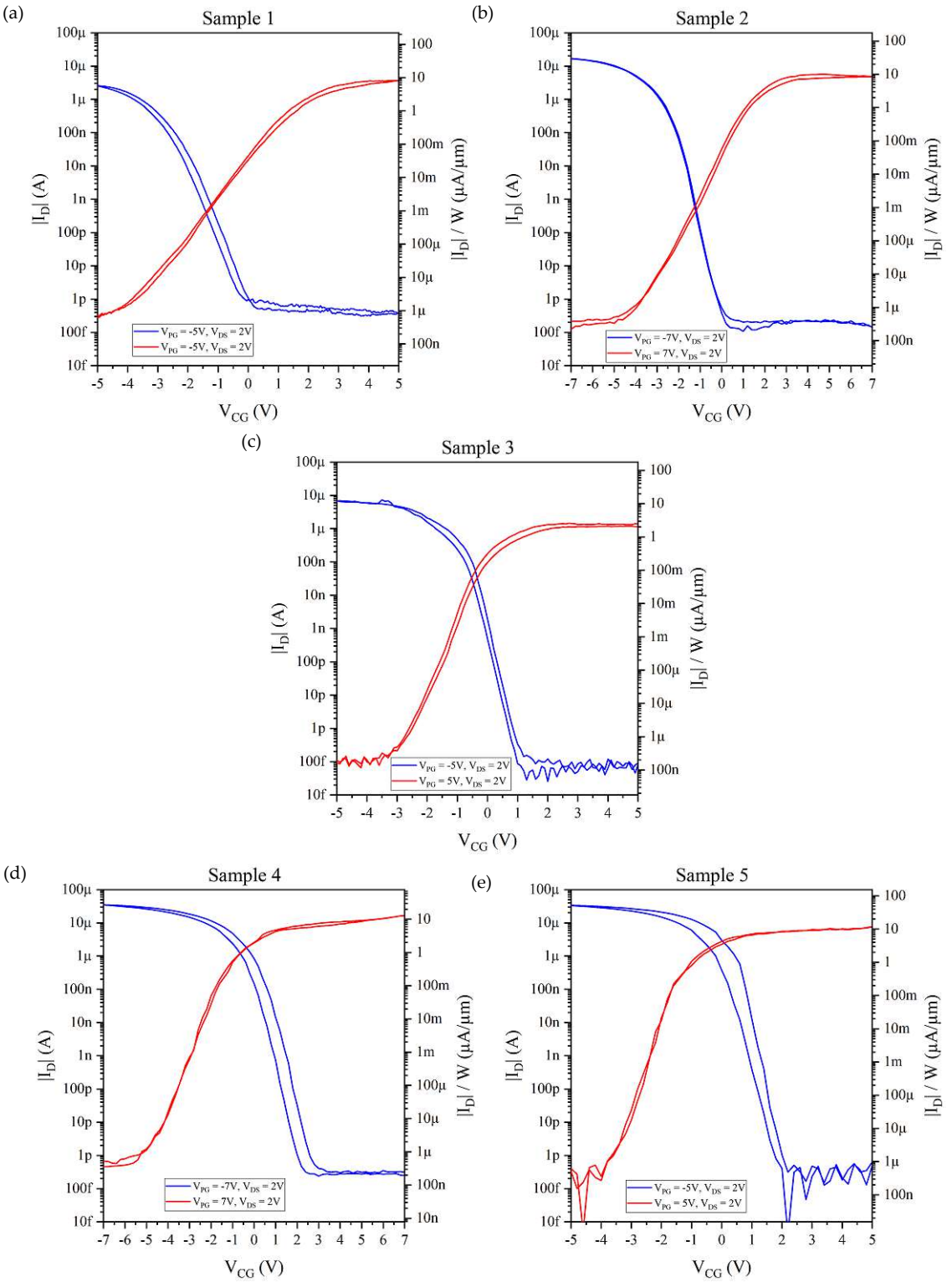

Figure 4.5: *Project evolution based on the transfer characteristics of a TTG structure from the various samples fabricated for this thesis.*

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The sample with HfO_2 is sample 2 and shown in figure 4.5b and the sample with ZrO_2 is sample 3 and shown in subfigure 4.5c. Both of these samples have preferable transfer characteristics, because both exhibit a very low hysteresis and a steep slope. The threshold voltages are shifted considerably to the left, for sample 2 to around -2V and for sample 3 to nearly -1V. This means both operation types clearly turn off. For the on-state symmetry the sample with ZrO_2, so sample 3, fairs a bit better than the one with HfO_2. The biggest difference between sample 2 and sample 3 are the PG voltage V_{PG} and the CG voltages V_{CG} used. Here, sample 2 needs +7V for n-type operation and -7V for p-type operation to saturate the RFET, also at 5V the on-state symmetry is much worse than for any other sample in this thesis. Sample 3 on the other hand can be fully operated with a PG voltage V_{PG} +5V for n-type operation and -5V for p-type operation and the same for the CG voltage V_{CG}. The bias-voltage V_{DS} is the same for both samples at 2V and applied symmetric.

Because of the better results in relation to the supply voltages and the better on-state symmetry the next two samples were fabricated with ZrO_2. Here, thinner dielectric layers were fabricated in the hope that the controllability of the samples would improve and a higher current could be reached. For sample 4 the ZrO_2 layer was reduced and for sample 5 the ZrO_2 and the SiO_2 layers were reduces. Sample 4 is shown in figure 4.5d and sample 5 in 4.5e. Unfortunately those two samples did not bring the desired improvements. For starters the hysteresis was worse than for all previous samples, especially for the p-type operation. Also for sample 4 again a higher PG voltage V_{PG} with +7V for the n-type operation and -7V for the p-type operations was needed to get the desired on-state symmetry and to reach the off-state for the n-type operation. This is very counter intuitive because with a thinner passivation layer a lower voltage was expected. The result is probably due to interface traps but this was not further investigated. Sample 5 had a similar behaviour regarding the gate voltages as sample 4, as can be seen in figure 4.5e. Here, a PG voltage of +5V for n-type operation and -5V for p-type operation was used, because at repeated measurements with 7V the RFET structures broke down. The bias-voltage V_{DS} was set at 2V and applied symmetrically for both samples.

Because of the higher supply voltage needed for sample 4 and the worse on-state current symmetry as well as the lower endurance of sample 5, the following electric characterisation of the structures is only shown for the first three samples with different passivation layers, so sample 1 with pure SiO_2, sample 2 with a combination of SiO_2 and HfO_2 and sample 3 with a combination of SiO_2 and ZrO_2. This is done according to the introduced electrical characterisation methods and evaluations in section 3.2 in the experimental techniques chapter. For the sake of completeness is has to be mentioned that the same measurements were also performed on sample 4 and sample 5.

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4.3 Transfer Characteristic - Single Top-Gate Structure

The transfer characteristic is very useful in order to get an impression of the abilities of the fabricated structures. Especially in regards to the on-state and off-state currents, as well as the symmetry of both operation types. With the STG transfer characteristic the voltages needed to control the transistor and how high the voltage can be at most are determined. The measurement setup which is used for this is introduced in subsection 3.2.1.

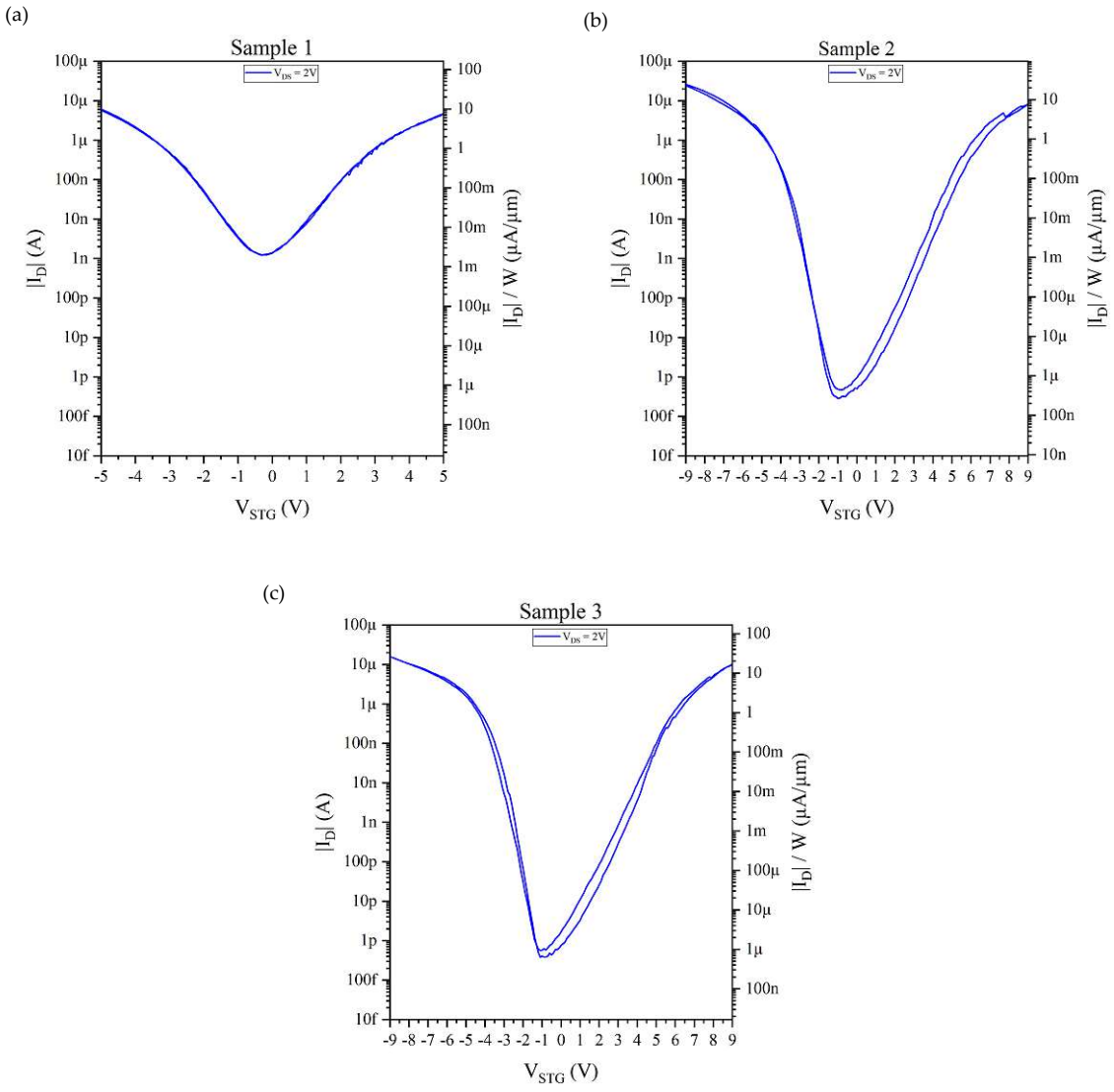

Figure 4.6: *STG transfer characteristics of sample 1 in subfigure (a), sample 2 in subfigure (b) and sample 3 in subfigure (c). Captured at room temperature (24° C) and in atmospheric ambient with a bias-voltage V_{DS} of 2V and a TG voltage V_{STG} swept from -5V (-7V) to +5V (+7V) and reverse ("double"-measurement)*

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The STG devices exhibit an ambipolar SBFET characteristic, which means by controlling both metal-semiconductor junctions simultaneously with the same voltage level no specific charge carrier type is suppressed.
In this section the transfer characteristic of representative STG structures for sample 1 to sample 3 are presented and discussed. The results are representative for all the different STG structures of each device. All of the shown transfer curves are captured in a "double"-measurement fashion. The bias-voltage V_{DS} is applied symmetrically and the different TG voltages V_{STG} are swept in an atmospheric ambient. The related measurement setup and the associated designations for the electrical STG characterisation are presented in figure 3.3 in the measurement setup subsection 3.2.1.

The transfer characteristics in figure 4.6 for the STG structure for all three samples are captured at room temperature (24°C) and in atmospheric ambient. The bias-voltage V_{DS} of 2V is applied symmetrically which means $V_D = 1V$ and $V_S = -1V$ respectively. For sample 1 the selected maximum TG voltage V_{STG} is +5V, while for sample 2 and sample 3 a maximum TG voltage of +9V was selected, because at +5V the structures did not reach their on-current saturation. The voltage is swept in a "double"-measurement from -5V (or -9V) to +5V (or +9V) and reverse. Subfigure 4.6a shows the STG transfer curve for sample 1, figure 4.6b the transfer curve for sample 2 and 4.6c the one for sample 3. All of the following measurements are captured as continuous measurements under the same conditions.
The left axis in all plots in figure 4.6 shows the absolute value of the drain current I_D and the right axis represents the corresponding value normalized by the channel width of the measured STG device.

When taking a look at figure 4.6a, which is the transfer characteristic of sample 1, it can be seen that the sample exhibits maximal on-state currents of 6.14μA (9.92μA/μm) at -5V and 4.62μA (7.46μA/μm) at +5V and a minimum current of 1.24nA (2m μA/μm) at -0.3V. So the off current of sample 1 is rather high, but the hysteresis of this sample is practically non existent. Because of the higher TG voltage V_{STG} samples 2 and 3 exhibit a higher maximum current. For sample 2 the maximal on-state currents are 25.91μA (24.26μA/μm) at -9V and 24.19μA (22.65μA/μm) at +9V and for sample 3 they are 15.72μA (26.07μA/μm) at -9V and 15.73μA (26.09μA/μm) at +9V. But also the minimum current are much lower for those two samples, with 288.69fA (270.3n μA/μm) at -1V for sample 2 and with 381.25fA (632.3n μA/μm) at -1.1V. The hysteresis for both sample 2 and sample 3 is still pretty low. The highest on-state currents and the lowest off-state currents are reached with sample 2. However the on-state symmetry of sample 3 is by far the best. For a better comparison of the transfer characteristics figure 4.8 shows all three characteristics in the same diagram, but only for TG voltages V_{STG} up to +5V (-5V), because sample 1 cannot be driven with 9V.

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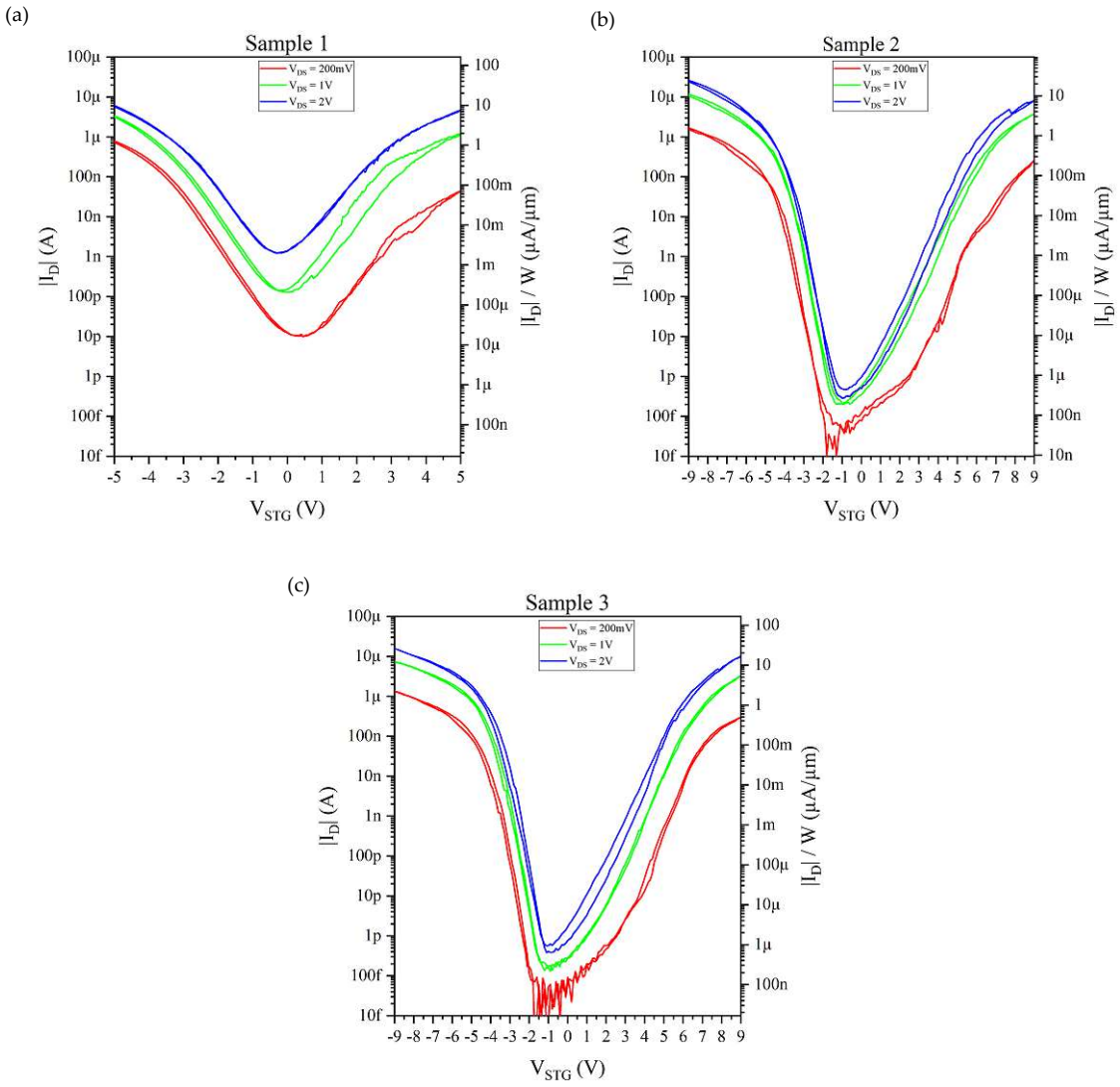

Figure 4.7: *STG transfer characteristic for different bias-voltage V_{DS} applied for sample 1 in subfigure (a), sample 2 in subfigure (b) and sample 3 in subfigure(c). for all samples the bias-voltages V_{DS} is applied in a symmetric fashion for 200mV (red), 1V (green) and 2V (blue), respectively at room temperature (24° C)*

To investigate the influence of various bias-voltages V_{DS} applied to the STG structures, the measurements of figure 4.7 are taken. The transfer curves are captured for symmetrically applied bias-voltages V_{DS} of 200mV (red), 1V (green) and 2V (blue) at room temperature (24°C) in a "double"-measurement form -5V to +5V and reverse for sample 1 and -9V to +9V and revers for sample 2 and sample 3. Looking at the first sample, sample 1, in subfigure 4.7a, as assumed the on-state and off-state currents fall with lower bias-voltages. Here, it can also be seen that for low bias-voltages the on-state symmetry for positive

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and negative TG voltages gets worse. Especially at positive voltages the current is much lower, than for negative voltages. But the off-state current also goes down considerably. A bit of a shift towards positive voltages considering the minimum point can be seen. A similar behaviour can be seen for sample 2 and sample 3. Here, the on-state symmetry does not suffer that much but still considerably. The best on-state symmetry for low bias-voltages can again be observed with sample 3. For the off-state currents at a bias of 200mV the measurement resolution is reached. Samples 2 and 3 barely show a shift of the minimum point. The best results for on-state symmetry is reached for a bias-voltage of 2V.

Figure 4.8 shows the direct comparison of the STG devices of the different samples. Here, the drain current is normalized over the according channel width of sample 1 (black), sample 2 (red) and sample 3 (blue) at room temperature (24°C). The problem is that for sample 2 and sample 3 much higher TG voltages are needed to get the maximum gain form the structure. Because of that the currents reached at +5V or -5V are considerably lower for sample 2 and sample 3, especially for positive voltages. The behaviour for sample 2 and sample 3 is very similar. With a TG voltage of only +5V (-5V) the hysteresis of sample 2 and sample 3 are nearly as good as for sample 1.

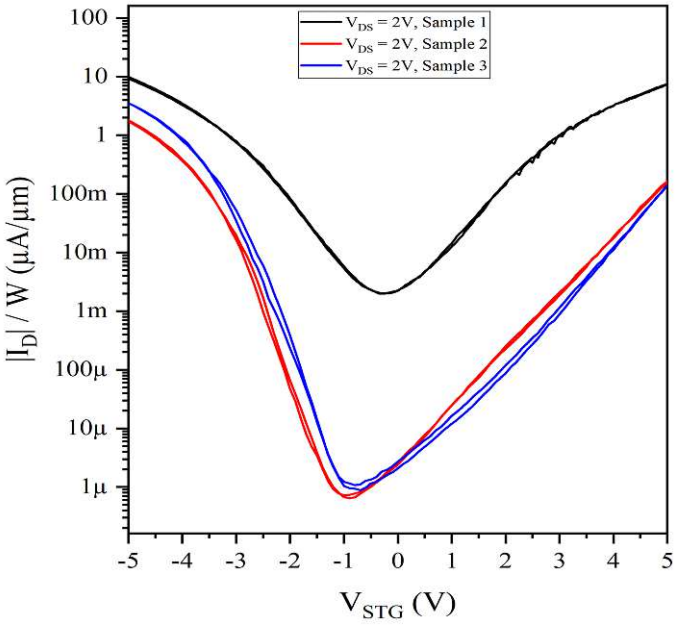

Figure 4.8: *STG transfer characteristic comparison of the drain current strength normalized by the channel width of the measured devices of sample 1 (black), sample 2 (red) and sample 3 (blue) for 5V TG voltage sweep. The TG voltage sweeps are performed in the "double"-measurement fashion with a symmetrically applied bias-voltage V_{DS} of 2V at room temperature (24° C).*

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4.3.1 Transfer Characteristics over Temperature

The last aspect to present in this section is the temperature dependent investigation of the corresponding STG transfer characteristics. Figure 4.9 shows the STG transfer characteristics of the three samples for different temperatures from room temperature (24°C) up to 125°C in 25°C steps. The bias-voltage V_{DS} is again 2V applied symmetrically. For sample 1 again a 5V transfer sweep was executed. This is shown in subfigure 4.9a. For samples 2 and 3 a 9V STG transfer sweep was performed. This can be seen for sample 2 in figure 4.9b and for sample 3 in 4.9c.

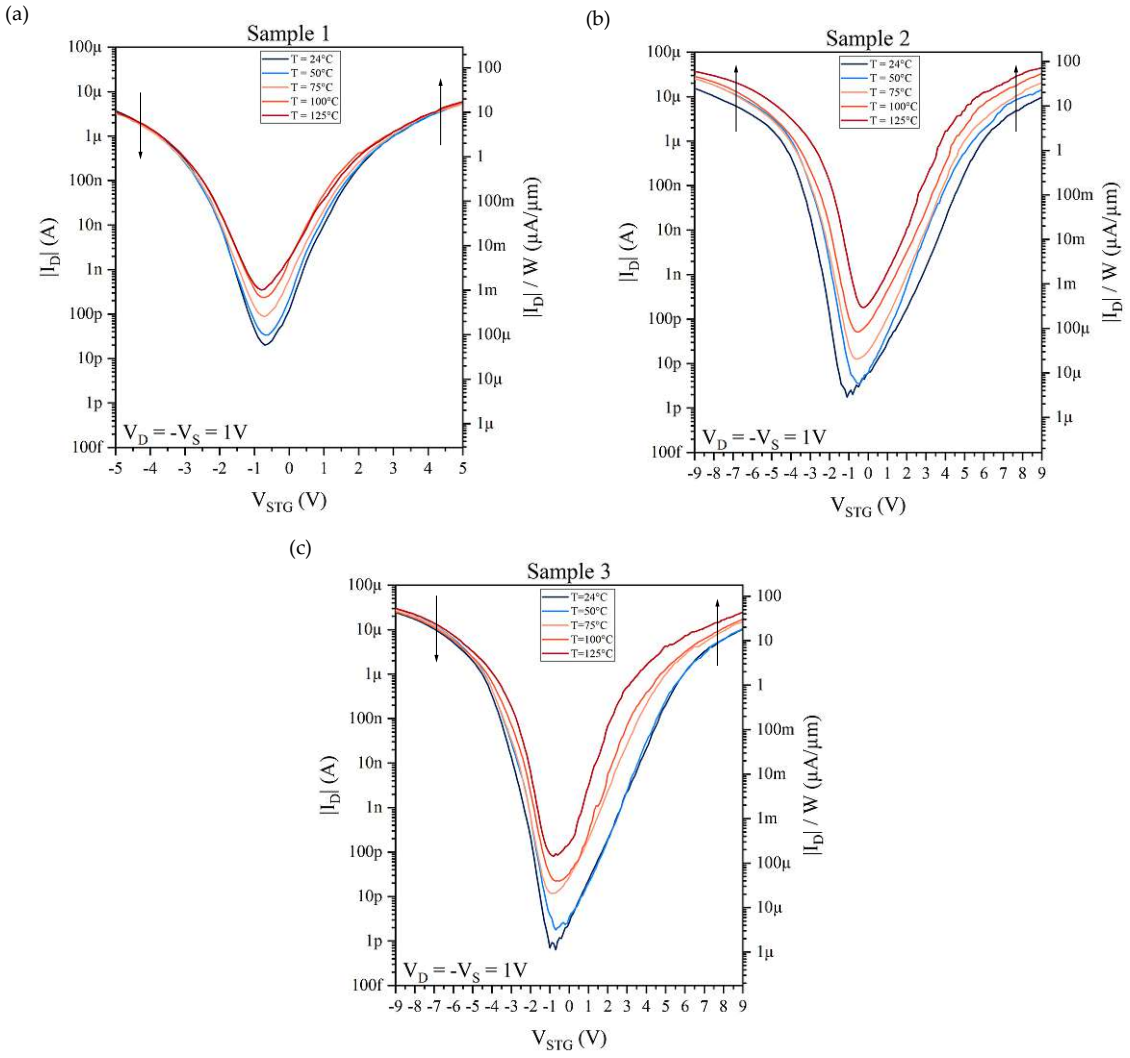

Figure 4.9: *STG transfer characteristic from a device of sample 1 in subfigure (a), sample 2 in subfigure (b) and sample 3 in subfigure (c) with a symmetrically applied bias-voltage V_{DS} of 2V at different temperatures starting from room temperature (24° C) up to 125° C in 25° C steps.*

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The measurement was performed as "double"-measurement, but because of the insignificant hysteresis only one direction of this sweep is shown in figure 4.9 to ensure a better readability. The temperature has hardly any influence on the hysteresis.

For sample 1 the on-state current barley shifts in any direction, so the temperature does not have a particular impact. The off-state currents increase with elevated temperature. The minimum point does not shift over the temperature. For sample 2 the on-state currents for both negative and positive TG voltages increase with rising temperatures, both in a similar manner. Also the off-state current again increases with the temperature ,but here, the minimum point shifts a little bit towards positive voltages. Interestingly for sample 3 the on-state current for positive TG voltages rise and at negative TG voltages there is a slight decrease in current. The off-state current also increases with rising temperatures but it does not rise the same for the different temperatures. Again no shift for the minimum point can be observed.

4.4 Transfer Characteristic - Triple Top-Gate Structure

After the transfer characteristics of STG devices of the different samples, the next aspect to present are the according transfer characteristics of the TTG devices fabricated on sample 1, sample 2 and sample 3. While with the STG devices the off-state current is represented by the minimum point of the transfer curve, the TTG device has a distinct off-state for both charge carrier type. On- an off-state of the corresponding n-type or p-type operation can be controlled via the CG voltage V_{CG}. Which operation type is used can be set with the PG voltage V_{PG}. According to this the transfer characteristic of a TTG device consists of two different transfer curves for the different operation types. This is also explained in section 3.2.2 in the experimental techniques chapter. The transfer characteristics of the different samples were measured with a symmetric bias-voltage and at different temperatures. The related measurement setup as well as the associated designations for the electrical TTG characterisation are presented in figure 3.3 in section 3.2.1. All measurements are performed in atmospheric ambient.

Figure 4.10 shows the transfer characteristics of TTG devices of sample 1 in figure 4.10a, of sample 2 in figure 4.10b and of sample 3 in figure 4.10c, all captured at room temperature (24°C). For all samples the bias-voltage V_{DS} is 2V and symmetrically applied. For sample 1 and sample 3 the PG voltage V_{PG} to set the operation mode is +5V for the n-type operation and -5V for p-type operation, for sample 2 the PG voltage is set to +7V for n-type operation and -7V for p-type operation. The operation type is indicated by the colour of the transfer curve, red for n-type operation and blue for p-type operation. The related CG voltage V_{CG} is swept, from off-state to on-state and reverse, which represents a "double"-measurement. So for the n-type operation the CG voltage V_{CG} is swept from -5V (-7V) to +5V (+7V) and reverse and for the p-type operation the CG voltage is swept

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from +5V (+7V) to -5V (-7V) and reverse. As it was the case with the STG plots here, also the left axis in all plots in figure 4.10 shows the absolute value of the drain current I_D and the right axis represents the corresponding value normalized by the channel width of the measured TTG device.

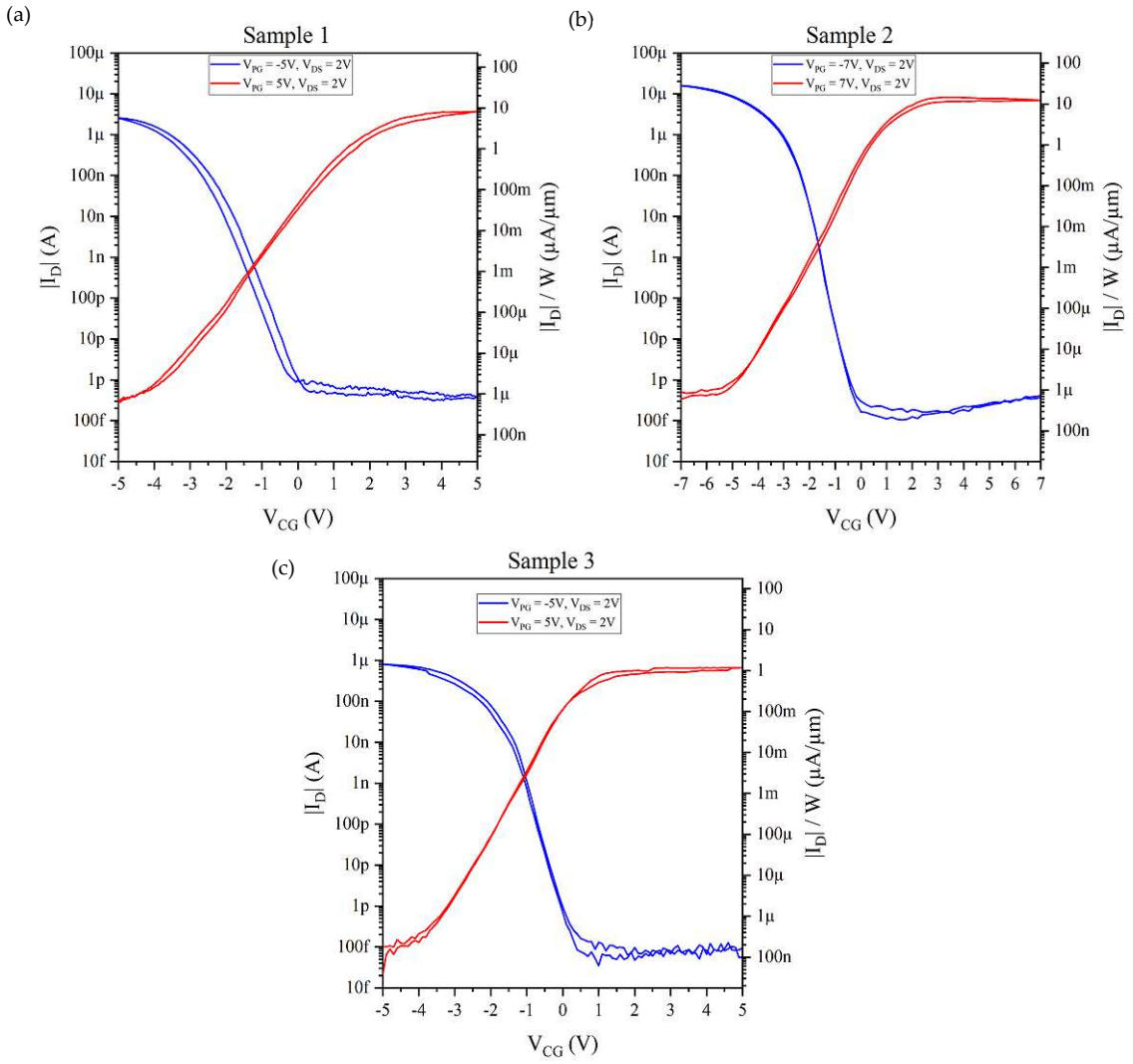

Figure 4.10: *TTG transfer characteristics of sample 1 in subfigure (a), sample 2 in subfigure (b) and sample 3 in subfigure (c). Measurements are performed at room temperature (24° C) and in atmospheric ambient, with a symmetrically applied bias-voltage V_{DS} of 2V and CG voltage swept from off-state to on-state and reverse ("double"-measurement) for each operation type. The operation type is set with PG voltage V_{PG}, of +5V (+7V) for n-type operation (red) and -5V (-7V) for p-type operation (blue) for all samples.*

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Now taking a look at the transfer characteristics, beginning with sample 1 shown in figure 4.10a. Here, the p-type operation has a on-state current of 2.57μA (5.71 μA/μm) and the n-type operation a on-state current of 3.71μA (7.90 μA/μm) so the on-state symmetry, which is indicated by the ratio of the different modes, lays by about 1.45. The off-state currents are 320.83fA (712.96n μA/μm) for the n-type operation and 319.03fA (708.96n μA/μm) for p-type-operation, which is much lower than the off current of the STG device on the same sample. This can explained by taking a look at the band structure of the RFET, shown in figure 2.6. Here, the CG introduces extra bending resulting in a lower off-sate current. For the evaluation of the on-state and off-state currents the minimum and maximum values of the transfer curves are taken and not the occurring value at the maximum CG voltages, so in this case +5V and -5V.
Sample 2, shown in subfigure 4.10b, has a n-type operation on-state current of 6.98μA (12.38 μA/μm) and a p-type operation on-state current of 16.01μA (28.39 μA/μm). This results in a on-state symmetry of 2.29. Which is still a very good value, but non the less a bit worse then for sample 1. The off-state currents for this sample are for the n-type operation 475.04fA (842.17n μA/μm) and for the p-type operation 164.88fA (292.34n μA/μm). These values are in the same ranges like for the STG structure, but here the off-state current was also very low.
Finally for sample 3 the on-state current for n-type operation is 659.16nA (1.17 μA/μm) and for p-type operation 809.15nA (1.23 μA/μm). This results in a on-state symmetry of 1.22. So the current is the lowest of all three samples but the on-state current symmetry is the best of all three samples. The off-state currents for sample 3 are for the n-type operation 94.63fA (167.49n μA/μm) and for the p-type operation 69.13fA (122.35n μA/μm). So the off-current is also the lowest of all three samples and even lower then the one of the STG structure on the same sample.

It should also be mentioned that STG and TTG devices cannot be directly compared with each other, because of their different structures and generally shorter channel length of the STG structures, so the comparison must be made with caution. A comparison of similar structures between the different samples is expressive, because of the different gate-dielectrics and the measurements are take with the same conditions.

In the next figure 4.11 the crossing point of the two operation types for the different samples is shown. Subfigure 4.11a shows sample 1, sample 2 can be seen in subfigure 4.11b and subfigure 4.11c shows sample 3. For sample 1 the crossing point lays at around -1.3V, for sample 2 this lays at -1.7V and for sample 3 at -1.1V. It was hoped that with the high-k dielectric the crossing point would shift more towards 0V, which would be the ideal case. For the ZrO_2 there was at least a shift in the right direction, for the sample with HfO_2 that was not the case. Another possibility to shift the curve even further would be a asymmetric bias-voltage, but when tried in this case the n-type operation current goes down considerably.

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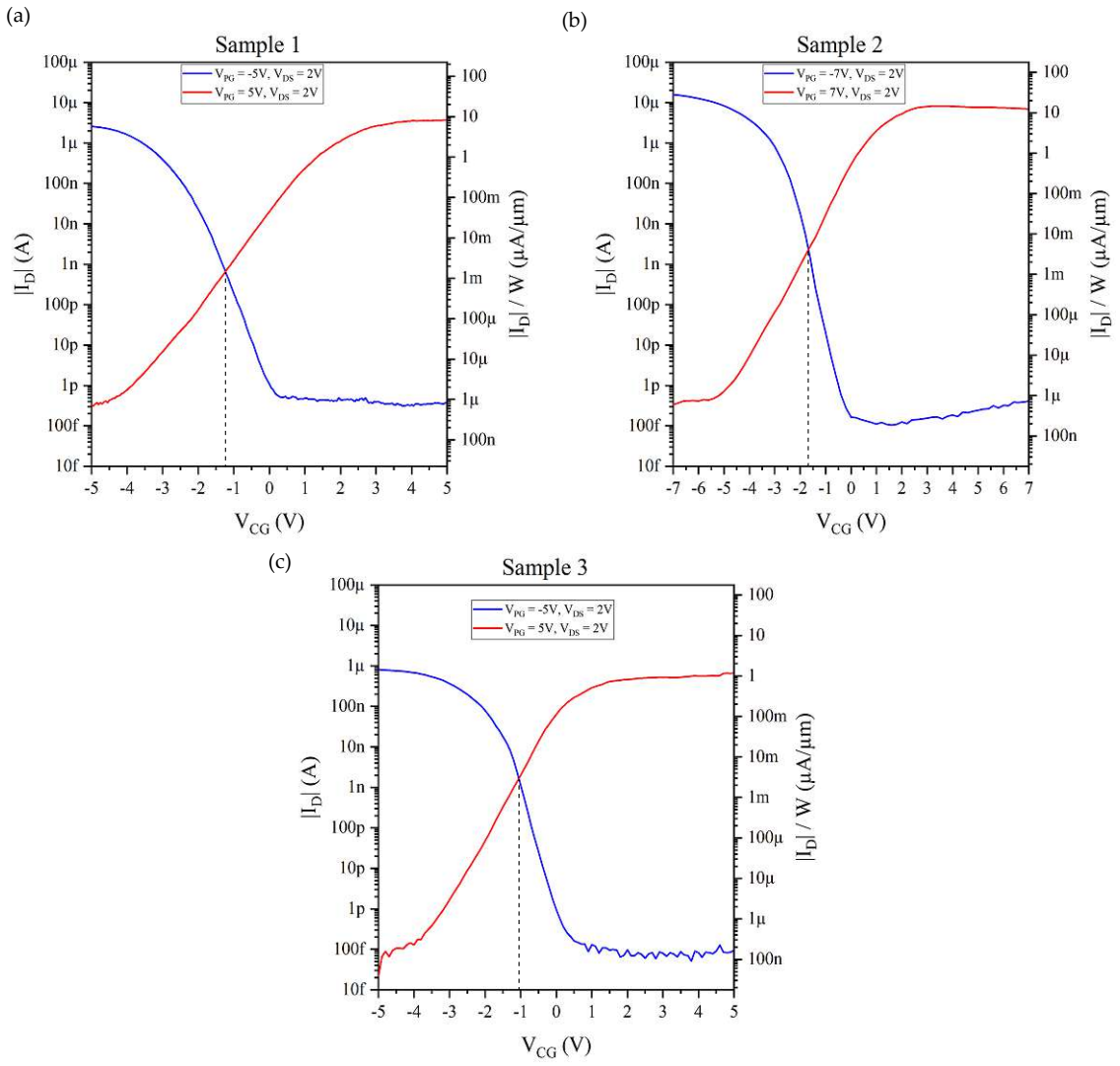

Figure 4.11: *TTG transfer characteristics of sample 1 in subfigure (a), sample 2 in subfigure (b) and sample 3 in subfigure (c), captured at room temperature (24° C) and in atmospheric ambient with a symmetrically applied bias-voltage V_{DS} of 2V. The operation type is set with PG voltage V_{PG}, of +5V (+7V) for n-type operation (red) and -5V (-7V) for p-type operation (blue) for all samples. The dashed line indicates the crossing point of the operation points for the different samples.*

To make a direct comparison between the three samples, figure 4.12 shows all transfer curves in one diagram. The drain current I_D is normalized over the related channel width for all three samples. The measurement conditions of for all samples are the same. This includes the applied voltages, the room temperature (24°C) and atmospheric ambient. The bias-voltage of 2V was applied symmetrically and 5V was applied for the TGs. In Figure 4.12 the transfer characteristic of sample 1 is blue, the one for sample 2 is red and

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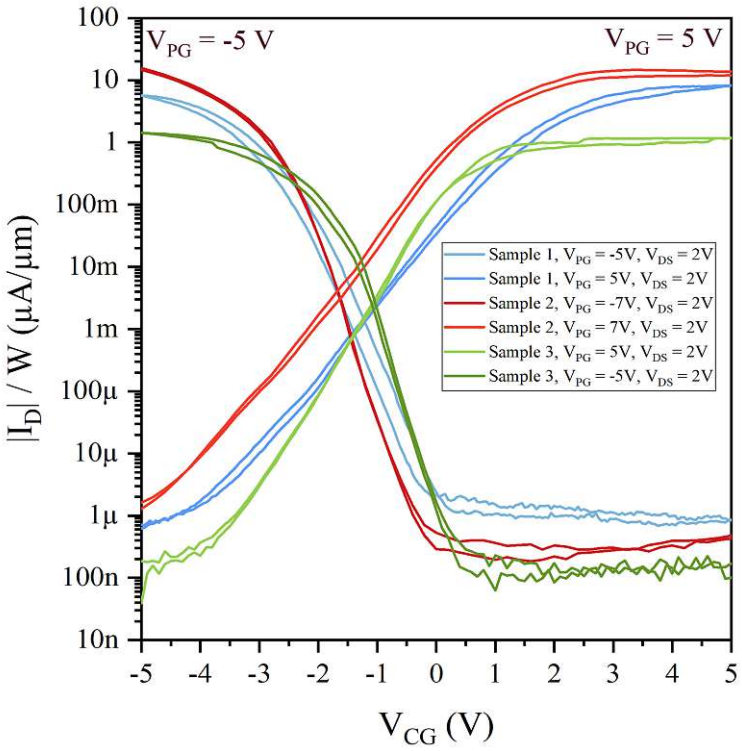

Figure 4.12: *Direct comparison of the TTG transfer characteristics of sample 1 (blue), sample 2 (red) and sample 3 (green) normalized to the channel width. Measurements are performed at room temperature (24° C) and in atmospheric ambient with a symmetrically applied bias-voltage V_{DS} of 2V and CG voltage V_{CG} swept from off-state to on-state and reverse ("double"-measurement) for both operation types. The operation type is set with the PG voltage, of +5V (+7V) for n-type operation and -5V (-7V) for p-type operation for all samples.*

for sample 3 it is green. When the samples are directly compared it can be seen that the currents for sample 2 are the highest, but also that at -5V the curve is not quite in the on-state yet, which means that here, higher voltages are needed. Even worse can this be seen for off-state for the n-type operation of sample 2. Sample 3 has the lowest current, but also the best on-state symmetry and it can be clearly seen that both on- and off-states are reached with 5V. The off-state currents are also the lowest. And finally the crossing point of the operation types of sample 3 is the closest to the desired 0V. The hysteresis for all three samples is very good.

4.4.1 Transfer Characteristics over Temperature

The last measurement which will be investigated in this section is the temperature dependent transfer characteristics for all three samples. The temperature measurements are presented in figure 4.13. The transfer characteristic over temperature for sample 1 are shown in figure 4.13a, for sample 2 in figure 4.13b and for sample 3 in figure 4.13c. For all three samples the bias-voltage V_{DS} of 2V was applied symmetrically and the structures of

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sample 1 and sample 3 were measured with 5V and at sample 2 with 7V. The measurements were take at five different temperatures beginning at room temperature (24°C) and with 25°C steps ending at 125°C.

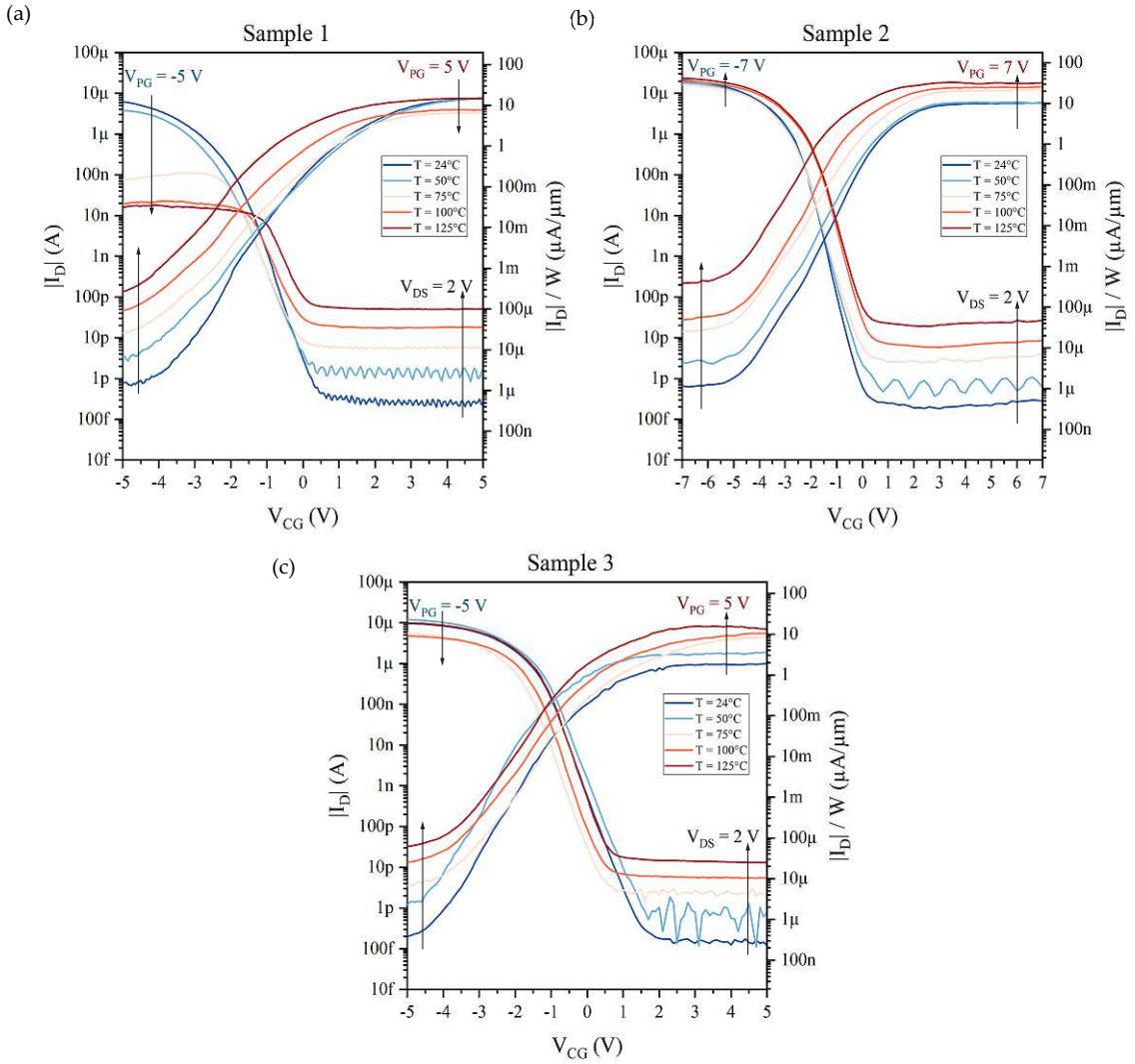

Figure 4.13: *TTG transfer characteristics of sample 1 in subfigure (a), sample 2 in subfigure (b) and sample 3 in subfigure (c) with a symmetric bias-voltages V_{DS} of 2V at different temperatures, starting from room temperature (24° C) up to 125° C in 25° C steps.*

Again the measurement was taken as a "double"-measurement, swept from off-state to on-state and reverse but are only depicted as a single measurement to improve readability of the plots.

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Taking a look at the measurement of sample 1, it can be seen, that the off-state current rises with the temperature quite steadily, but the on-state current has a different behaviour. For the n-mode the current stay the same at 50°C and then falls for 75°C and 100°C and finally for 125°C rises again to the same value as for room temperature. For the p-type operation it is even worse. The current falls for 50°C slightly and for 75°C drops down nearly two decades. For 100°C it decreases even further down until it stays constant up to 125°C. So it can clearly be seen that sample 1 is not stable over temperature. This weird behaviour, especially of the p-type current can probably be explained by the not gated areas of the RFET, since the STG structure did not exhibited this behaviour.
This extreme temperature dependency of the drain-current I_D is not present for the two samples with high-k dielectrics. The off-state current of sample 2 behaves very similar, as in sample 1, so it rises with the temperature. In this case the on-state current increases with the temperature as well. The n-type current rises by a bit and the p-type current stays nearly the same.
For sample 3 there is not such a clear picture as for sample 2. Only the off-state current increases steadily with the temperature. For the on-state current in n-type operation the current also rises over the temperature, but the slope does not stay the same. For the p-type operation the current rises for 50°C and falls for 75°C, but then rises again and for 125°C it is the same as for room temperature. This could be due to measurement tolerances, so the over all tendency is that the on-state current for p-type operation falls with temperature. But compared to sample 1, sample 3 it is much more temperature independent.

The increase of the off-state current for all devices can be attributed to the increased thermally generated charge carriers which are elevated over the Schottky barrier or a higher injection rate of charge carriers through the thermally assisted tunneling. Regarding the on-state current, except the one of the p-type operation in sample 1, it can be seen that it does not have a substantial increase, especially for the p-type operations of sample 2 and sample 3. The assumption here, is that the major charge carrier injection comes from tunneling, which is not very dependent on temperature. [17, 22, 41, 53]

4.5 Output Characteristic - Single Top-Gate Structure

The next measurements taken are the output characteristics of STG structures and TTG structures, using the methods described in the experimental techniques chapter in subsection 3.2.3. Like the section about transfer characteristics this section provides the output characteristics of representative STG devices of all three samples. The ambipolarity of the STG devices can also be seen in the output measurements.

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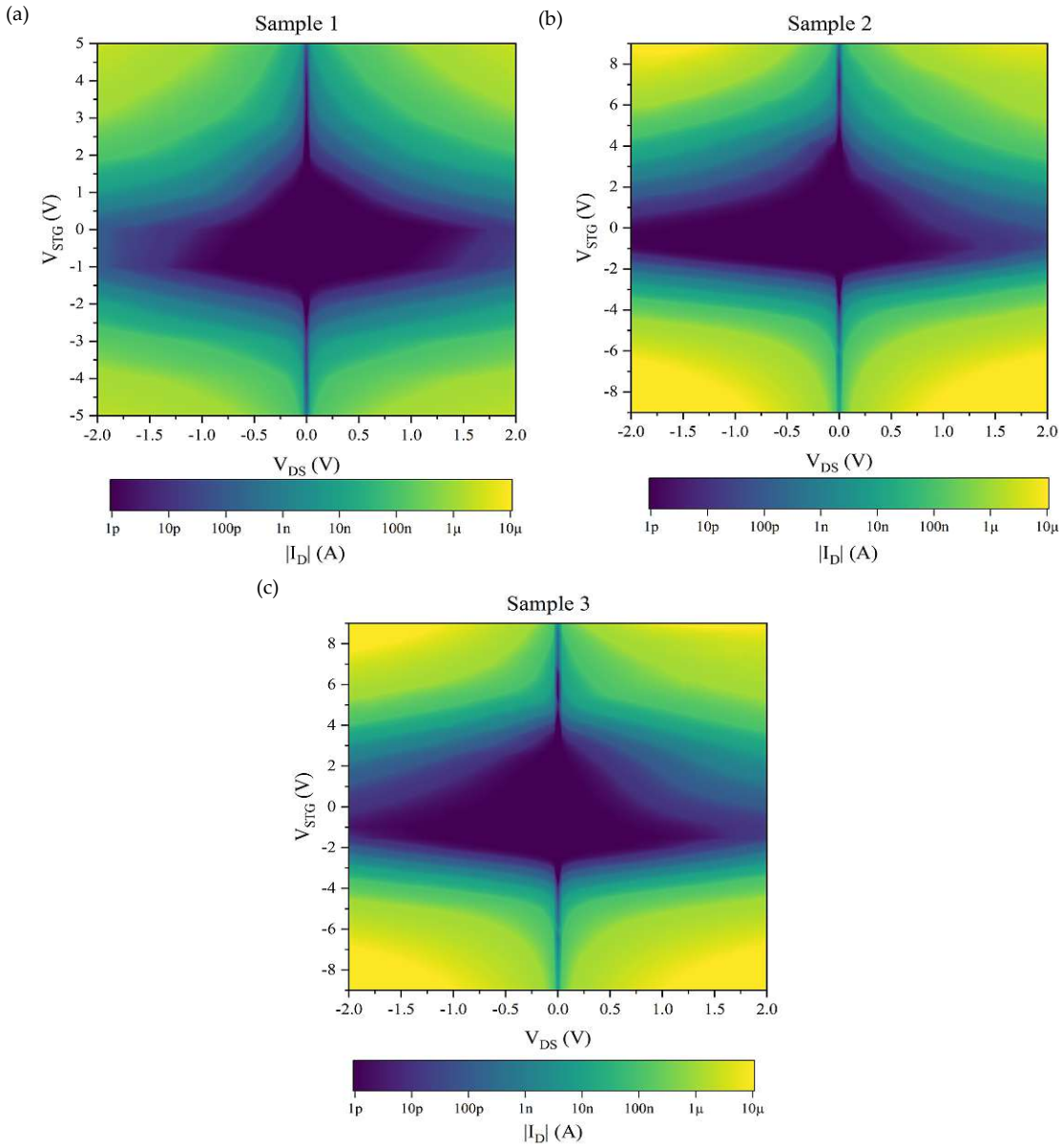

Figure 4.14: *Colour maps of the output characteristics (colour map) of sample 1 in subfigure (a), sample 2 in subfigure (b) and sample 3 in subfigure (c). All measurements are performed in a symmetric fashion sweeping the bias-voltage V_{DS} from +2V to -2V for various TG voltages from -5V to +5V in 500mV steps for sample 1 and for various TG voltages from -9V to +9V in 500mV steps for sample 2 and sample 3. All measurements are performed at room temperature (24° C).*

Figure 4.14 shows the color maps of the output characteristics of sample 1 in subfigure 4.14a, of sample 2 in subfigure 4.14b and of sample 3 in subfigure 4.14c. All these measurements are performed with a symmetric bias-voltage V_{DS} form -2V to +2V, which means that V_D starts at 1V and is swept to -1V while keeping $V_D = -V_S$. The TG voltages are

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swept from -5V to +5V in 500mV steps resulting in 21 individual output curves for sample 1 and from -9V to +9V in 500mV steps resulting in 37 individual output curves, for sample 2 and sample 3 respectively. Because the STG is a ambipolar device no charge carrier type is suppressed, which means both modes occur at once but with different current strengths. It can be seen that the n-type current which occurs at positive TG voltages V_{STG} is a bit lower than the p-type current which occurs at negative TG voltages V_{STG}. This can be seen in the color map on the smaller yellow regions at positive TG voltages V_{STG}, compared to the ones at negative TG voltage V_{STG}. These differences between the p-type and the n-type dominated current can be explained by having a look at the asymmetric Schottky barriers for the charge types in section 4.8. To get a higher current the voltage at the STG must be sufficient to shift the barriers enough. It should be remarked that even though the operation type currents are a bit different, all three samples exhibit a quite good symmetry which was also shown at the transfer characteristics. Comparing the three samples to each other it looks like sample 2 and sample 3 provide much higher currents than sample 1, but those two require a much higher TG voltage V_{STG}. It can be said, that the block out regions of sample 2 and sample 3 are bigger than of sample 1, which also explains the higher voltages needed to get a sufficient current. This indicates that the Schottky barriers of sample 2 and 3 are higher than of sample 1. Also the symmetry in respect of the changing current direction through the nanosheet is remarkable in all three samples. This means the devices exhibit a similar performance independent of the sign of the bias-voltage. The current from source to drain would be negative, therefore the absolute value of the drain current is plotted in the colour maps.
Generally speaking, it can be said that the colour maps of the output characteristics are a very useful tool to estimate the stability of a device considering for instance the voltage variations in a FET.

4.5.1 Output Characteristic over Temperature

Like with the transfer characteristics the next aspect to look at is the temperature-dependent behaviour of the output characteristics. Here, figure 4.15 present the output color maps of a representative device of sample 3 captured in 25°C temperature steps from room temperature (24°C) up to 125°C. Here, the applied bias-voltage is swept from -2V to +2V and the TG voltage is swept from -9V to +9V as for the previous output measurements. This time the TG voltage is swept in 1V steps resulting in only 19 output curves for a quicker measurement. This measurement is only depicted at sample 3 because the other two samples exhibit a similar behaviour. For a better comparison between the different subfigures the scale of the colour map is the same for all temperatures.
First it is obvious that the off-state currents, indicated in blue, are getting higher with increasing temperatures, due to the increased thermally generated charge carriers, as it was the case for the transfer characteristics. Here, it can also be seen that the on-state currents for the n-type operation rises slightly with the temperature and the ones for the p-type operation stay constant up to 125°C where they start to rise as well. This is also quite similar to the transfer characteristic.

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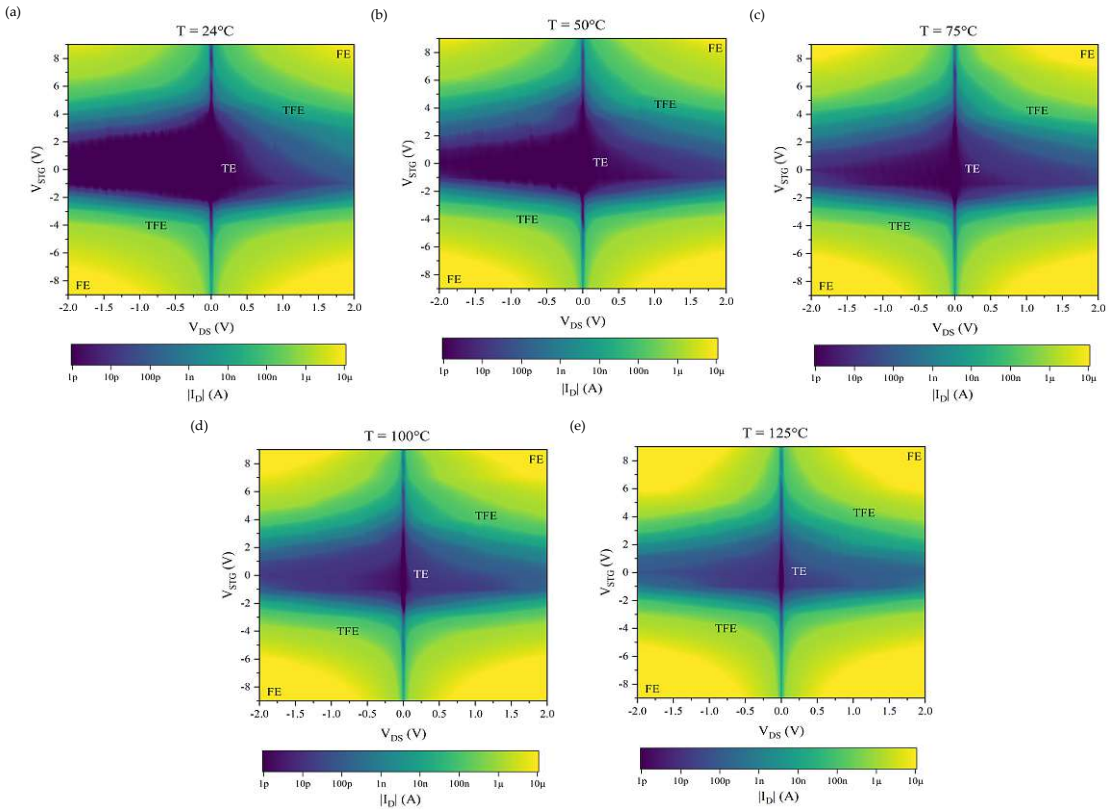

Figure 4.15: *STG output characteristics (color map) of a representative device of sample 3 with symmetric bias-voltage V_{DS} sweeping from -2V to 2V at different temperatures starting from room temperature (24° C) up to 125° C in 25° C.*
TE...thermionic emission, TFE...thermionic-field emission, FE...field emission

The temperature dependent behaviour of the individual parts of the output characteristic can be used to qualitatively identify the different transport mechanisms. This is because the tunneling dominated current through the barrier has a lesser temperature dependency than the thermionic emission dominated currents. So the thermionic emission regime (TE), the field emission regime (FE) and the thermionic-field emission regime (TFE) in between can be carefully estimated. [21, 22, 66, 67]
The different regimes are indicated in the color maps in figure 4.15, with TE in the blue parts (off-state), FE in the yellow parts (on-state) and TFE in the green part in between. So it can be concluded that the majority of the on-state current is caused by tunneling charge carrier transport, this is a typical characteristic for a SBFET. The off state is dominated by the thermionic emission. [22, 41] This also explains the difference of the current dependencies of temperature. The significant increase of the TE dominated current at the off-state with a positive eSBH and the slight change of the on-state current dominated by field emission for increased temperature. A closer look at the eSBH is taken at section 4.8.

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4.6 Output Characteristic - Triple Top-Gate Structure

Like for the STG output characteristic the measurement method for the TTG output characteristic is also described in the experimental techniques chapter in subsection 3.2.3. Here, again the TTG structure suppresses the undesired charge carrier transport with an additional TG. This results in two different modes, n-type and p-type. So the output characteristic consists of the output curves for both charge carrier types. This section also shows the colour maps of the output characteristics of the different samples. The related temperature investigation and transport regime considerations are made similar to the output section for STG devices above.
All measurements are recorded at room temperature (24°C) with a symmetrically applied bias-voltage V_{DS} swept from -2V to +2V for different CG voltages V_{CG} changed from -5V to +5V in 500mV steps for sample 1 and sample 3 resulting in 21 curves per sample and from -7V to +7V in 500mV steps for sample 2 resulting in 29 curves. The resulting mode is set with a PG voltage V_{PG} of +5V for n-type operation and -5V for p-type operation for sample 1 and sample 3 and with +7V and -7V for sample 3. The resulting colour maps are depicted in figure 4.16. Here, subfigure 4.16a and 4.16d show the output characteristic of sample 1, subfigure 4.16b and 4.16e the ones for sample 2 and subfigure 4.16c and 4.16f finally the ones for sample 3. The n-type operations are depicted in the subfigures 4.16a, 4.16b and 4.16c and in the subfigures 4.16d, 4.16e and 4.16f the p-type operations are shown.

In the 2-D representation the abilities of the structures are clearly shown, also the voltages stability can be seen. For a better comparability the color scheme of all colour maps is the same but as sample 2 needs a higher voltage to get a reasonable current this needs to be considered when comparing the different samples.
In accord to the applied bias-voltages the symmetry of all three samples exhibit two distinct areas for the on-state and so consequently also for the off-state. Especially the bias-voltage symmetry of sample 3 is remarkable for both operation states. Sample 1 and sample 2 exhibit a small difference at the n-type operation. Again it can be seen that for sample 1 the n-type operation current is slightly higher than the p-type operation current and that this is the other way around for the other two samples. For sample 3 the current starts rising for a CG voltage of -2V at the n-type operation and at -0.5V for the p-type operation. This is the nearest to the desired 0V of all three sample since for sample 1 the voltages are -2.5V (n-type) and -1V (p-type) and for sample 2 -3V (n-type) and -1.5V (p-type).
When comparing the output colour maps of the TTG structures to the ones of the STG structure it can be seen that the STG output characteristic is approximately composed of the two individual TTG output characteristics of the two different charge carrier operation types.

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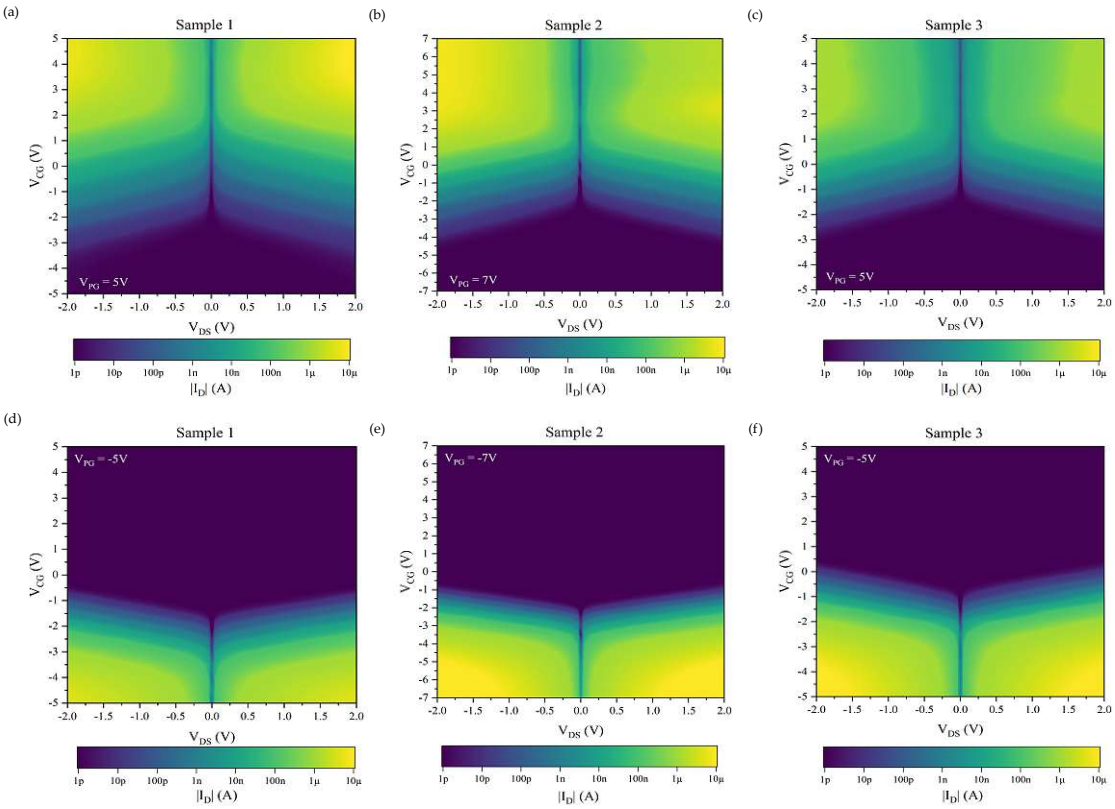

Figure 4.16: *Colour maps of the output characteristics of sample 1 in subfigures (a,d), sample 2 in subfigures (b,e) and sample 3 in subfigures (c,f) for both operation types. Subfigures (a), (b) and (c) depict the results in n-type operation (PG voltage $V_{PG} = +5V(+7V)$), whereas subfigures (d), (e) and (f) depict the results in p-type operation (PG voltage $V_{PG} = -5V(-7V)$). All measurements are performed in a symmetric fashion sweeping the bias-voltage from -2V to 2V for various CG voltages from -5V to +5V in 500mV steps for sample 1 and sample 3 and for CG voltages from -7V to +7V in 500mV steps for sample 3. All measurements are performed at room temperature (24° C).*

4.6.1 Output Characteristic over Temperature

Similar to the STG device the next step to consider is the temperature dependent behaviour of the output characteristic of the TTG device. Here, again the the output colour maps of a representative device on sample 3 are shown, because the exhibited behaviour is very similar for all three samples. Here, the output characteristics for both operation types are shown. Figure 4.17 shows the colour maps of the n-type operation for various temperatures starting from room temperature (24°C) up to 125°C in 25°C steps. Again the bias-voltage is applied symmetrically and swept from -2V to +2V and the CG voltage is swept form -5V to +5V in 500mV steps. The PG voltage is set to +5V for n-type operation and to -5V for p-type operation. The color maps for the p-type operation are shown in figure 4.18. Here, all the colour maps are scaled the same so that the comparison between those is easier.

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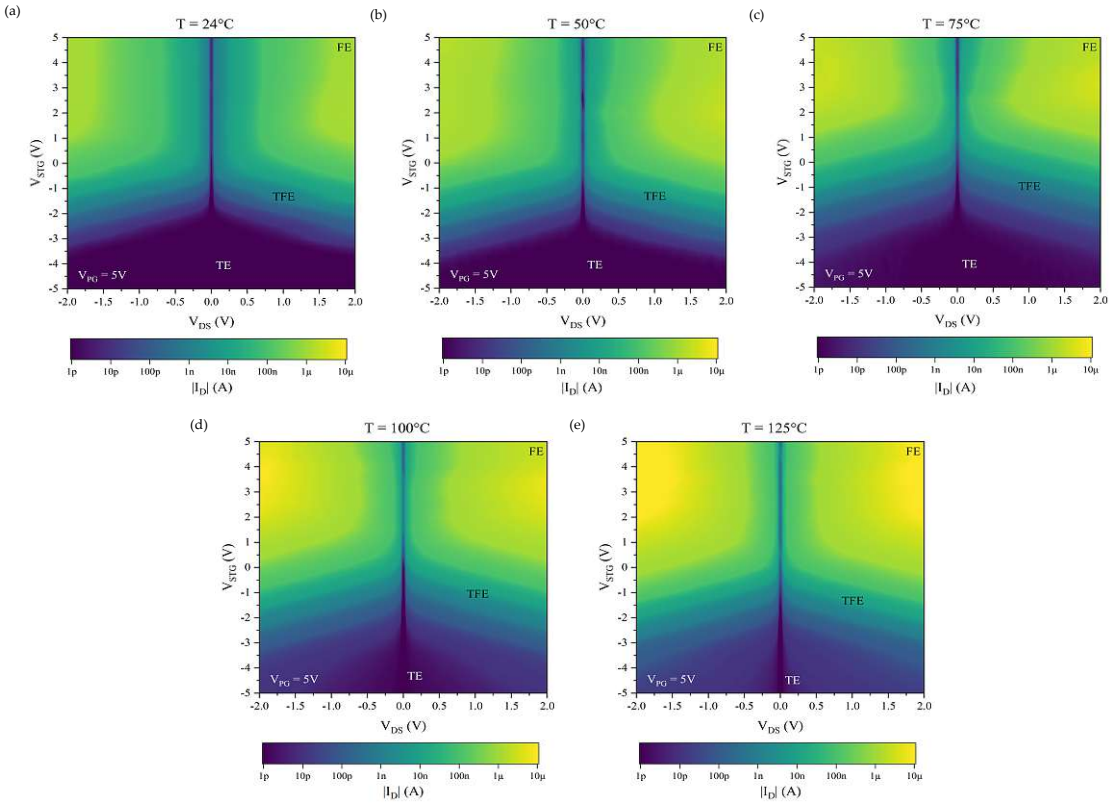

Figure 4.17: *TTG output characteristics (color map) of a representative device of sample 3 at symmetric bias-voltages V_{DS} swept from -2V to +2V for n-type operation (PG voltage $V_{PG} = +5V$) at different temperatures starting from room temperature (24° C) up to 125° C in 25° C. TE...thermionic emission, TFE...thermionic-field emission, FE...field emission*

When looking at the output characteristic for the n-type and p-type operation it can be seen that the off-state current increases with the temperature for both of them. While the on-state current of the n-type operation also rises with the temperature, the on-state current of the p-type operation falls slightly with the temperature. What is remarkable is that the principle function of the RFET structures as well as the STG structures are still intact even at temperatures up to 125°C, albeit with a increased off-state current.
The different transport mechanisms can be distinguished over the temperature dependencies of the various regimes, similarly to the STG devices. Like stated before, the thermionic emission (TE) dominated current exhibits a higher temperature dependency than the field emission (FE) dominated current, which is for the most part a tunneling current. [21, 22, 66, 67] Again, those regimes can be estimated carefully for the output characteristics and are indicated in the figures as TE for thermionic emission, TFE for thermionic-field emission and FE for field emission. The off-state current is indicated in blue and is dominated by the TE current resulting in a significant increase with rising temperature. The on-state current is indicated with yellow in the colour maps and is

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majorly caused by tunneling, so this is a FE current. [22, 41] The green areas between the on-state and off-state is carefully identified as the TFE regime.

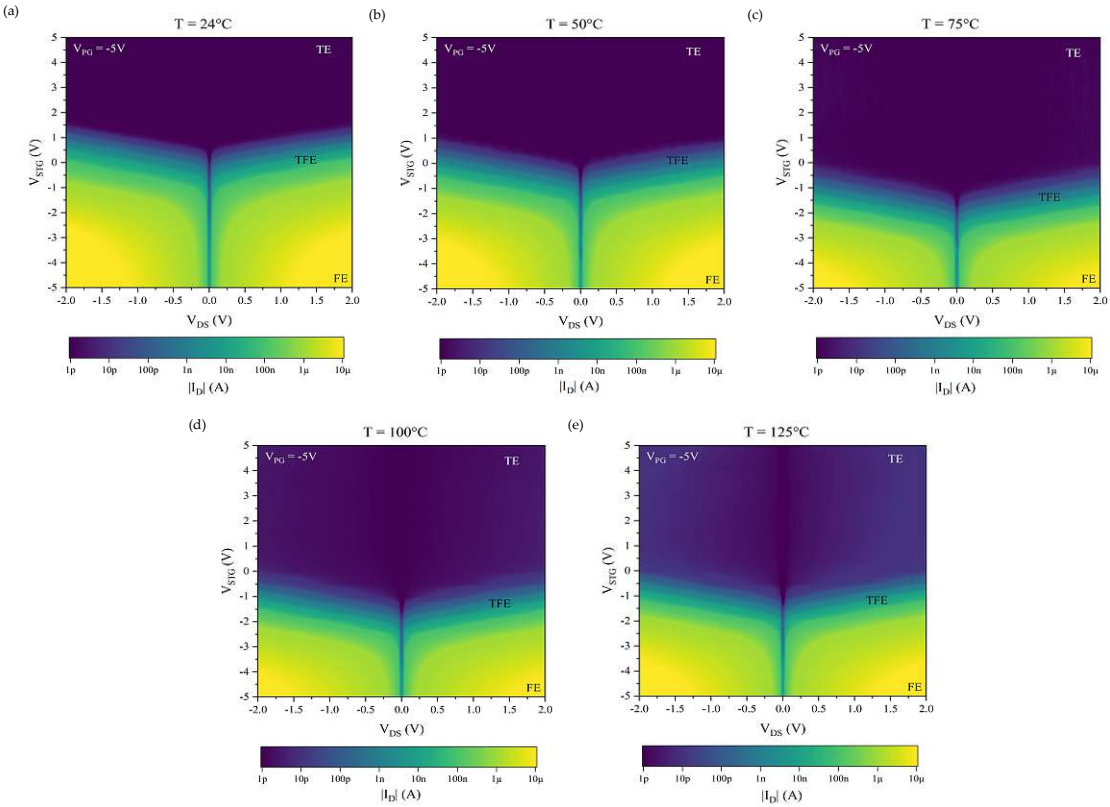

Figure 4.18: *TTG output characteristics (color map) of a representative device of sample 3 at symmetric bias-voltages V_{DS} swept from -2V to +2V for p-type operation (PG voltage $V_{PG} = -5V$) at different temperatures starting from room temperature (24° C) up to 125° C in 25° C steps.*

4.7 PG-Sweep Characteristic

The PG sweep characteristic provides information about the operation type switching of the TTG structure and so the expected transfer characteristics for various PG voltages. This is also explained in the experimental techniques chapter in subsection 3.2.4. The PG sweep will also be presented as a 2-D colour map, similar to the output characteristics. As mentioned before this colour map representations are useful for estimating the operation stability of the fabricated devices.

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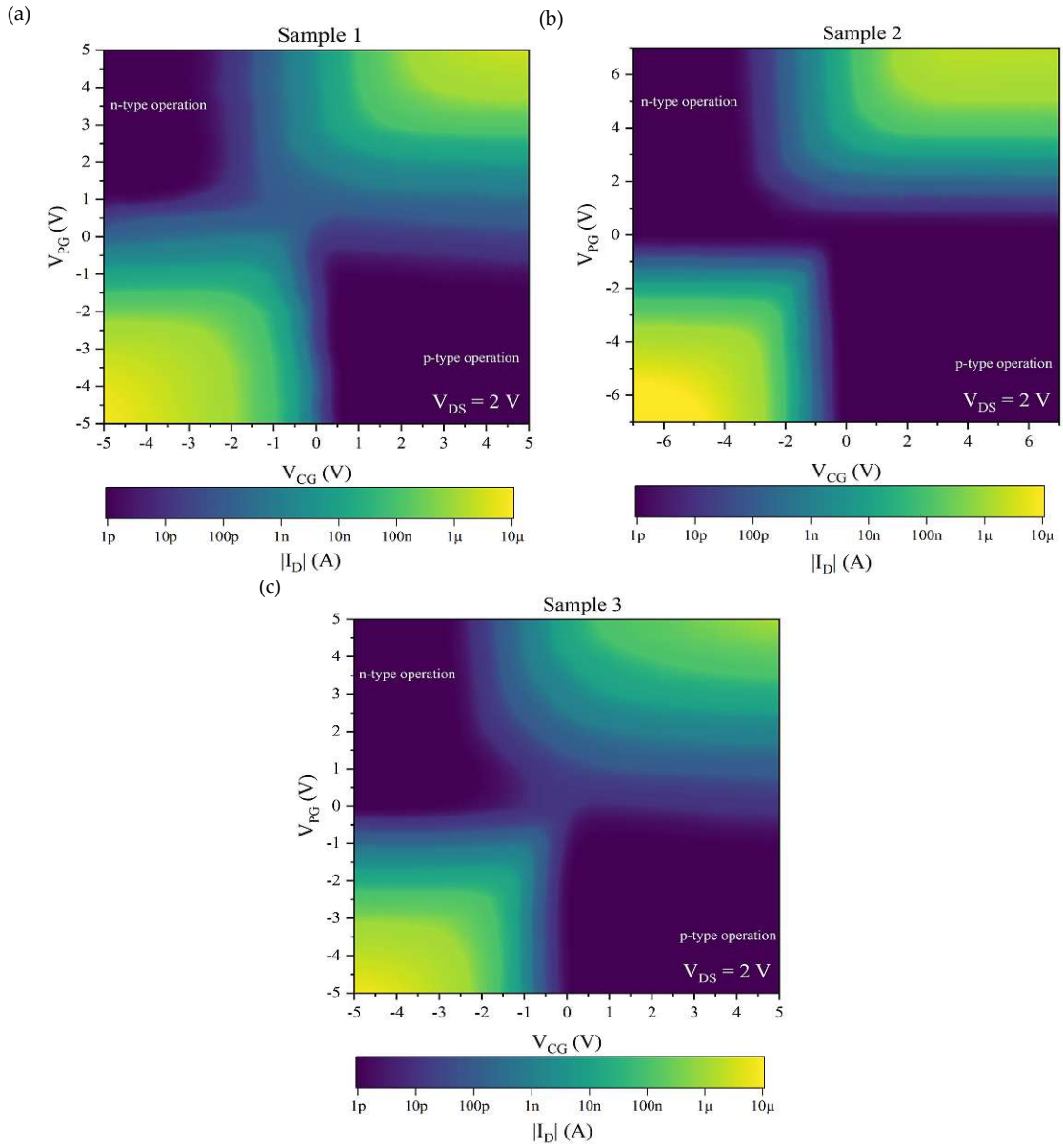

Figure 4.19: *PG sweep of TTG structures of sample 1 in subfigure (a), sample 2 in subfigure (b) and sample 3 in subfigure (c) presented in a colour map measured at room temperature (24° C). The measurement is performed with a symmetrically applied bias-voltage V_{DS} of +2V. Both the PG voltage V_{PG} and the CG voltage V_{CG} are swept from -5V (-7V) to +5V (+7V). The PG voltage steps are 500mV and the CG voltage steps are 100mV (200mV).*

Figure 4.19 shows the PG sweep characteristics of sample 1, in figure 4.19a, sample 2 in figure 4.19b and sample 3 in figure 4.19c. Those PG sweeps were measured with a symmetrically applied bias-voltage V_{DS} of 2V at room temperature (24°C) and the two sweeping parameters V_{PG} and V_{CG}. The CG voltage V_{CG} is swept from -5V to +5V in

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100mV steps for sample 1 and sample 3 and from -7V to +7V in 200mV steps for sample 2. The PG voltage V_{PG} is swept from -5V to +5V in 500mV steps for sample 1 and sample 3 and from -7V to +7V in 500mV steps for sample 2.

The off-state current is depicted in blue and the on-state current in yellow, for better comparability all colour schemes are scaled the same. When taking a look at the colour maps it can be said that there is the need of a sufficient PG voltage for all samples to obtain a distinct charge carrier operation type. It can be seen that for all three samples the n-type operation needs lower voltages to be turned off than the p-type operation. For the PG voltage there is a clean cut between n-type operation and p-type operation, especially for sample 2 and sample 3, while for sample 1 those two bleed a bit together at 0V. Again, the good on-state symmetry of sample 1 and sample 3 can be seen. However there is still an overall symmetry in respect to the n-type and p-type operations for all three samples with very distinct on-state and off-sate areas. This results in four nearly equal quarters, with the on-state of the n-type operation a bit larger, which represents the fundamental functionality of the RFET.

4.7.1 PG-Sweep Characteristic over Temperature

For the sake of completeness the temperature dependent behaviour of the PG-Sweep characteristic is also shown. Here, the PG sweeps of a representative device from sample 3 are shown, because once again the exhibited behaviour of all three devices is similar. Figure 4.20 shows the colour maps of the PG sweep for different temperatures starting at room temperature (24°C) up to 125°C in 25°C steps. The bias-voltage V_{DS} of 2V is applied symmetrically and CG voltage V_{CG} and PG voltage V_{PG} are swept form -5V to +5V, for the CG voltage in 100mV steps and for the PG voltage in 500mV steps. The colour maps here, also are scaled in the same manner, to get a better comparability.

Similar to the output characteristics it can be seen that the off-state current in both areas increases the same with the temperature. Comparing the areas of the off-state from 24°C with the ones from 125°C it can be seen, that at 24°C they are a bit bigger than those at 125°C. The on-state current in n-type operation also increases with the temperature. The on-state current in p-type operation nearly stays the same. Here, it can be seen that for higher temperatures the on-state symmetry gets a bit better.

4.8 Effective Schottky Barrier Heights

The effective Schottky barrier heights (eSBH) are determined like described in subsection 3.2.5 of the experimental techniques chapter and according to metal-semiconductor heterostructure section 2.2.1. The eSBH of all three samples is evaluated from the temperature dependent behaviour of the output characteristics. As stated in the aforementioned sections the metal-semiconductor-metal heterostructure of the SBFET STG structure is

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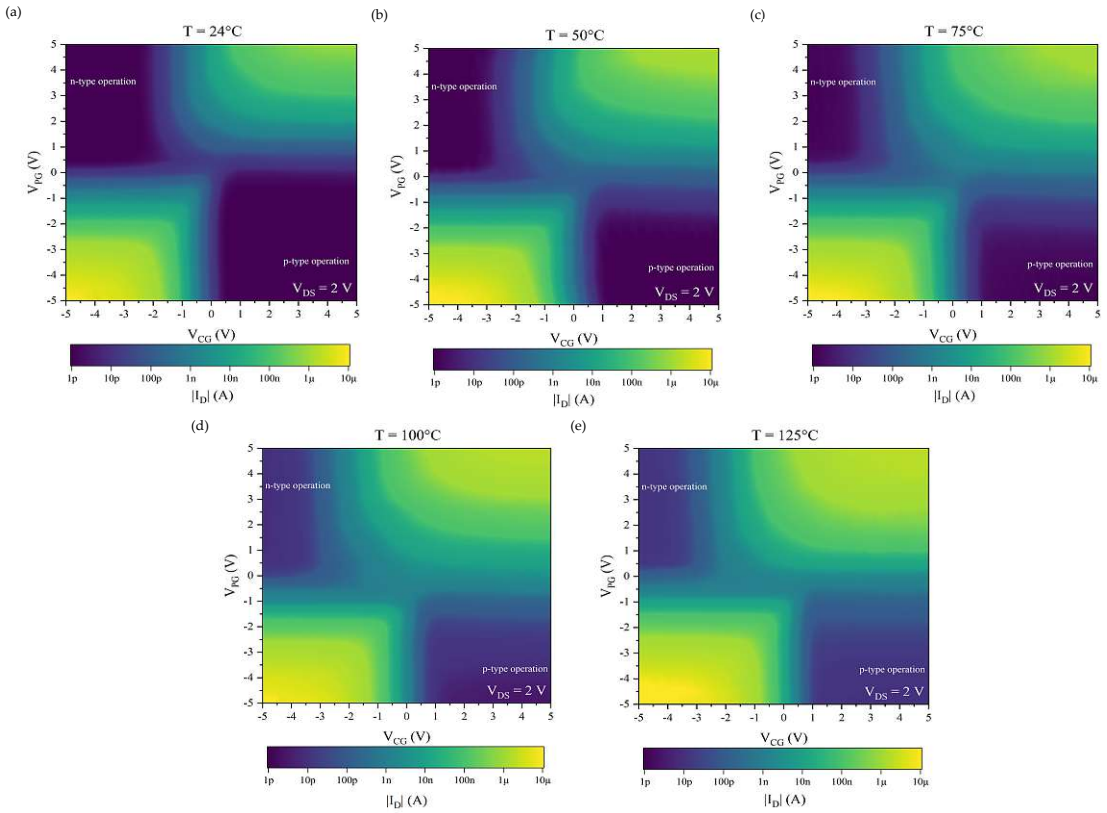

Figure 4.20: *PG sweep of a representative device of sample 3 with a symmetric bias-voltage V_{DS} of 2V. CG voltage V_{CG} and PG voltage V_{PG} are swept from -5V to +5V in 500mV steps at different temperatures starting from room temperature (24° C) up to 125° C in 25° C.*

abstracted into one effective barrier. The output curves are captured with a bias-voltage sweep from 0V to 1V in 5mV steps at temperatures starting from room temperature (24°C) up to 125°C in 25°C steps.

After performing the temperature measurements, the captured data can be evaluated and the eSBH for the samples can be obtained. Those are presented in figure 4.21. Subfigure 4.21a shows the eSBH of sample 1, subfigure 4.21b the one for sample 2 and subfigure 4.21c the one for sample 3. Here, the eSBH values are evaluated for three STG structures of each sample and the presented data depicts a statistical evaluation consisting of mean values (squares) and standard deviation (bars). For sample 1 the TG voltage was swept from -5V to +5V in 1V steps and for sample 2 and sample 3 the TG voltage was swept from, -9V to +9V in 1V steps. The dashed line indicates the minimum of the transfer curves of the related samples.
For sample 1 and sample 3 it can be seen that the minimum of the transfer characteristic, which marks the off-state, can be found at the same voltage as the maximum value of the eSBH. This would mean that for this voltage the current experiences the highest barrier

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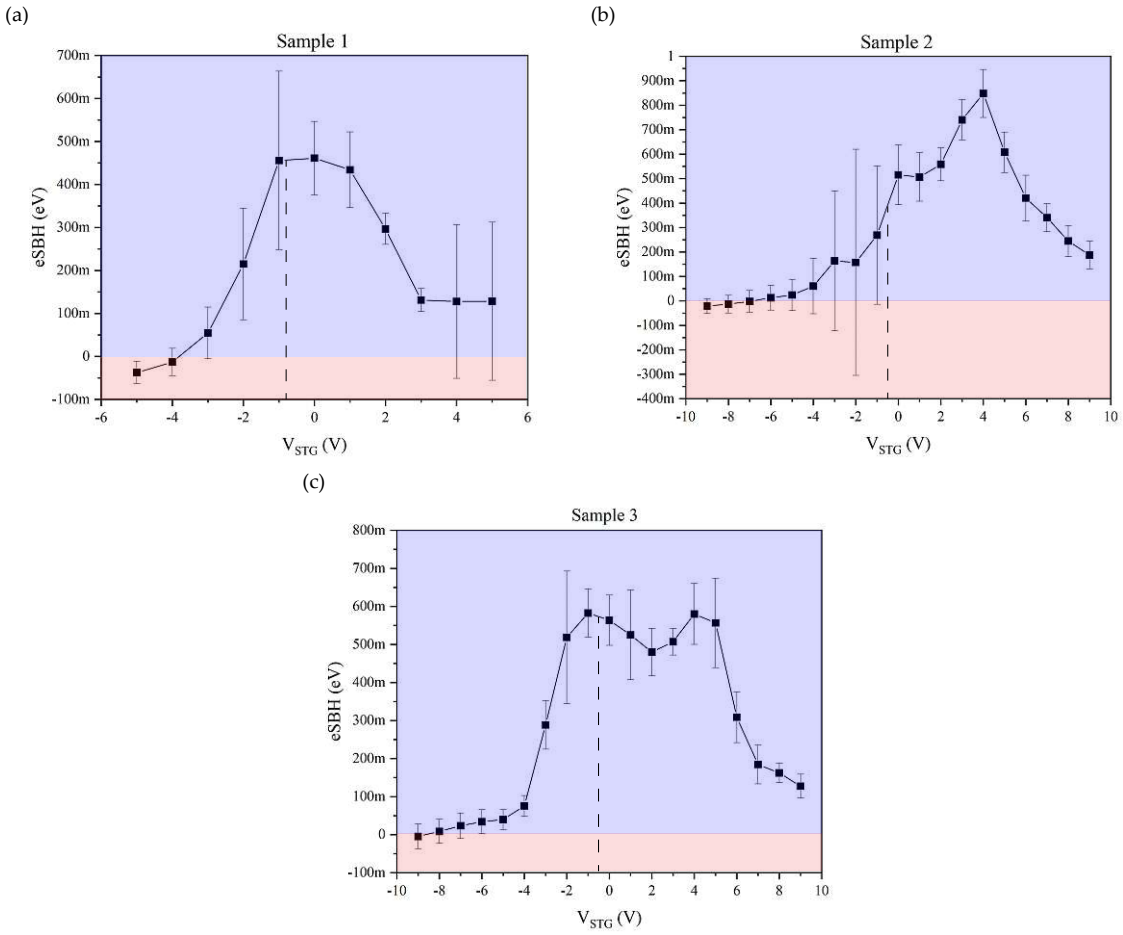

Figure 4.21: *Effective Schottky barrier for all three samples. Subfigure (a) shows the eSBH of sample 1, subfigure (b) the one of sample 2 and subfigure (c) the one for sample 3. The presented values are statistically evaluated over three different structures of each sample.*

and therefore is the lowest. This also means that the on-state currents, both for n-type operation at positive voltages and p-type operation for negative voltages, exhibit a much lower eSBH which results in a higher current. The second peak at around +5V for sample 3, is most likely a measurement error, because the transfer characteristic shows a similar behaviour like for a negative voltage where no peak can be seen. Even more puzzling is the eSBH curve of sample 2. Here, the minimum of the transfer curve is located around -0.5V and not like the highest eSBH value at +5V, even when considering the standard deviation. This could be due to wrong assumptions that are taken for the calculation of the eSBH, like stated in subsection 3.2.5 of the experimental techniques chapter, measurement errors or some surface states at the metal-semiconductor junctions. The Schottky barrier in its simplest explanation depends only on the work functions of the metal and semiconductor and so should be the same for all three samples. But from an experimental point of view and with the abstractions over the two metal-semiconductor junctions in mind, the effective Schottky barrier can also be seen as the effective activation energy for the zero-bias case.

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The occurring negative eSBH values indicate a transparent or ohmic contact and are a result of the abstraction of the effective activation energy. [45, 68] This means the used method considers the bias-current through the metal-semiconductor-metal heterostructure in dependency of the temperature and applies the commonly used simplified thermionic emission theory for an individual Schottky junction to obtain the barrier height. Here, the situation is different because the SBFET exhibits two junctions. Depending on the different applied TG voltages and the barrier bending, the resulting activation energy needs to enable current flow and therefore the eSBH can exhibit negative values. This can be seen in this work and also in literature [41, 53, 69]. According to the resulting eSBH the temperature dependent behaviour of the on-state and off-state current can be explained. So the decrease of the on-state currents in the p-mode with rising temperatures indicates the typical characteristic of a highly transparent contact and the rising on-state current in the n-mode and the rising off-state current is common for a Schottky contact. [21, 41, 42] How strong this change is depends on the dominant transport mechanisms. Here, the temperature dependency of the thermionic emission dominated off-state current is bigger and therefore the increase is higher as for the tunneling dominated on-state current. [21, 22, 66, 67]
The eSBH as presented above is extrapolated to zero-bias. For a more accurate and general statement for the STG characteristics, the related effective energy barrier for different bias-voltage must be looked at. This will be presented as a colour map with the TG voltage and the bias-voltage as parameters in the next section. Because the STG structure was already discussed in this eSBH investigation the next section will present the effective activation energy for TTG structures.

4.9 Effective Activation Energy

The effective activation energy of the metal-semiconductor-metal structures provide a more universal picture when compared to the eSBH evaluation in respect to the bias-voltage, as stated in the experimental techniques chapter in subsection 3.2.6. For the TTG structures the TG voltage is indicated by the CG voltage V_{CG} and the operation mode is set with the PG voltage V_{PG}, which results in two measurements and so two effective activation energy diagrams, one for each operation type. The calculated data points are plotted in a 2-D colour map and can be seen in figure 4.22. With these effective activation energy color maps a more reliable and resilient interpretation of the charge carrier transport mechanisms of RFETs can be done. [70]

Figure 4.22 shows the colour maps of the effective activation energy of a TTG structure of sample 1 in subfigures 4.22a and 4.22d, for sample 2 in figures 4.22b and 4.22e and for sample 3 in subfigures 4.22c and 4.22f. The applied bias-voltage V_{DS} was swept from -2V to +2V and the CG voltage V_{CG} from -5V to +5V for sample 1 and sample 3 and from -7V to +7V for sample 2. The n-type operations is set with PG voltage V_{PG} of +5V (+7V) and is shown in figures 4.22a to 4.22c and the p-type operation with a PG voltage V_{PG} of

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-5V (-7V) and is shown in subfigures 4.22d to 4.22f. The colour scheme for all samples is set from 0eV to 600meV for better comparability.

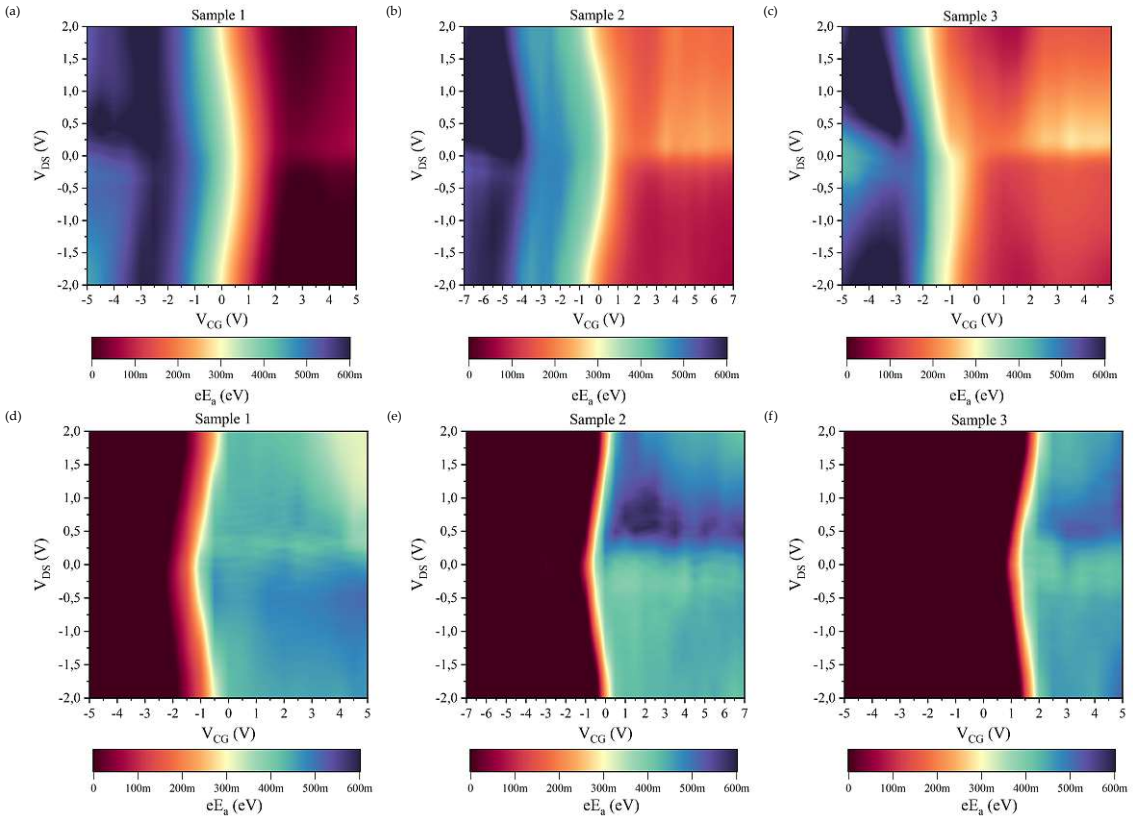

Figure 4.22: *Effective activation energy (color maps) of a TTG structure for sample 1, in subfigures (a) and (d), sample 2, in subfigures (b) and (e) and sample 3, in subfigures (c) and (f). Subfigures (a), (b) and (c) show the n-type operation (PG voltage $V_{PG} = +5V(+7V)$) and subfigures (d), (e) and (f) show the p-type operation (PG voltage $V_{PG} = -5V(-7V)$).*

Taking a look at the color maps, it can be seen that the activation energy depicts two explicit regions and are separated by a narrow regime at around 300meV, which is indicated with yellow in the colour scheme. For the n-type operation at positive CG voltages the activation energy exhibits small values which is indicated in red and means the electrons encounter a small barrier for positive voltages, whereas for negative CG voltage the barrier is high and indicated in blue. This proofs the basic functionality of the RFET, because the undesired charge carriers are suppressed. The small gradient of the effective activation energy at these two regions over the CG voltage variation means the injection capabilities are stable within the region. All three samples exhibit a similar effective activation energy for the n-type operation, only the CG voltage where the regimes switch are a bit different and for sample 1 the barrier in the positive voltage regime is lower than for the other two samples. Now for the p-type operation there is a similar picture regarding the two regimes, but as expected the low barriers are now at negative voltage and the high ones

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for positive voltages. Here, the dark-red area indicates a small or even negative energy barrier, which results in higher p-type on-state currents. Also the higher barrier for the positive CG voltages is a bit lower than the one for the n-type operation. Again the CG voltages for which the transition between the two regimes occur is a bit different for the three samples. For sample 1 it is again the lowest and for sample 3 the highest. Like for the n-type operation the gradient of the effective activation energy is small.

As mentioned in the experimental techniques chapter in section 3.2.6 and in the section above, the underlying theory to determine the effective activation energy only provides a careful estimation, especially for low-bias regions. Still some of the correlations between the temperature dependent characteristics and the effective activation energy can be explained. Like seen with the eSBH, the rise of the off-state and the n-type on-state currents can be explained with the positive energy barrier and the fall of the p-type on-state current. For sample 2 were it stays practically the same, it can be explained by the negative energy barrier. Also how much the currents change can be assessed. Obviously a high energy barrier means a lower current and vice versa. [21, 22, 66, 67]

4.10 Evaluation of Characteristics

As described in the experimental techniques chapter in subsection 3.2.7, to obtain the relevant transistor characteristics, the transfer characteristics of several devices of all three samples are captured and evaluated automatically with a Python script. These characteristics are used for a comparison of the RFET structures.
The following RFET parameters are evaluated for the used samples. All currents are evaluated for both operation types, as well as the on-state to off-state ratio, the threshold voltage and the inverse sub-threshold slope.

- On-state current I_{on}, the on-state currents normalized to the related channel width I_{on}/W and the according on-state currents densities J_{on}
- Off-state current I_{off}, the off-state currents normalized to the related channel width I_{off}/W and the according off-state currents densities J_{off}
- On-state to on-state ratio $I_{on,p}/I_{on,n}$ of the on-state currents of both operation types
- Off-state to off-state ratio $I_{off,p}/I_{off,n}$ of the off-state currents of both operation types
- On-state to off-state ration I_{on}/I_{off}
- Threshold voltage V_{th}

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- Inverse sub-threshold slope $STHS$

Here, it should be mentioned that the on-state currents are determined by evaluating the maximum value of the transfer curves and the off-state currents by evaluating the minimum value of the transfer curves. These currents are evaluated for both operation types. The on-state to on-state ratio, between the on-state current of the two operation types reflects the on-state symmetry of the TTG RFET. Therefore the off-state to off-state ratio shows the off-state symmetry of the RFETs. The evaluation of the threshold voltage and the STHS is presented in the subsections below.

To show the reliability and the reproducibility of the fabricated samples and the material system itself, the displayed values of the transistor characteristics are the average of ten representative TTG structures. The ten best devices for the particular characteristic were taken. The transfer characteristics for the evaluation are all measured at room temperature (24°C) and with a symmetrically applied bias-voltage V_{DS} of 2V. To select the operation type the PG voltage V_{PG} is set to +5V for n-type operation and -5V for p-type operation and the CG voltage V_{CG} is swept between these voltage levels, for sample 1 and sample 3, for sample 2 the same is done with a voltage level of +7V (-7V).

	Sample 1	Sample 2	Sample 3
$I_{on,n}$ (μA)	9.58	7.05	2.28
$I_{on,n}$/W $(\mu A/\mu m)$	19.43	13.98	3.83
$J_{on,n}$ (kA/cm^2)	492.52	353.15	93.64
$I_{on,p}$ (μA)	14.45	21.79	3.74
$I_{on,p}$/W $(\mu A/\mu m)$	29.32	43.23	13.23
$J_{on,p}$ (kA/cm^2)	846.08	1090.82	161.96
$I_{off,n}$ (fA)	4118.53	351.29	87.38
$I_{off,n}$/W $(\mu A/\mu m)$	8.36μ	696.87n	150.32n
$J_{off,n}$ (kA/cm^2)	204.53μ	16.82μ	3.75μ
$I_{off,p}$ (fA)	395.35	441.19	118.51
$I_{off,p}$/W $(\mu A/\mu m)$	802.25n	875.19n	198.57n
$J_{off,p}$ (kA/cm^2)	20.39μ	21.04μ	4.96μ

Table 4.1: *Comparison of the current parameter from TTG structures of all three samples fabricated at this thesis. For the comparison the mean value of the ten best devices of each sample are considered.*

The evaluated current-related values of the TTG devices of all three samples are listed in table 4.1. As seen before the off-state and on-state currents for sample 3 are the lowest. When comparing the values for the different samples it has to be kept in mind that the voltage for sample 2 is higher. Because of the lower p-type current of sample 3 there is a better symmetry of this sample.

In table 4.2 different ratios of currents shown in table 4.1 above are depicted. The values

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	Sample 1	Sample 2	Sample 3
$I_{on,p}/I_{on,n}$	2.14	3.31	1.96
$I_{off,p}/I_{off,n}$	0.46	0.86	0.99
$I_{on,n}/I_{off,n}$	14.84M	33.08M	20.30M
$I_{on,p}/I_{off,p}$	21.71M	134.91M	29.93M

Table 4.2: *Comparison of the current ratios from TTG structures of all three samples fabricated in this thesis. For the comparison the mean value of the ten best devices of each sample are considered.*

are the average of the individual ratios of ten selected devices, therefore they differ from the calculated ratios from the presented average current values. It can be seen that the on-state and off-state symmetry of sample 3 is the best, because the ratios are the closest to one. The on-state to off-state ratio is the highest for sample 2, but again here, it needs to be considered that the TG voltages for measurements of sample 2 were higher than for sample 1 and sample 3 and therefore a direct comparison is difficult. It can be seen that the on-state to off-state ratio of sample 3 is higher than for sample 1. This can also be seen in the transfer characteristic measurements in section 4.4.

4.10.1 Threshold Voltage

As mentioned before in this subsection the evaluation of the threshold voltage V_{th} is presented. The determination of the threshold voltage V_{th} values for the two operation types is described in subsection 3.2.7.1 of the experimental techniques chapter. Here, it can be said that a lower V_{th}, near to 0V, is preferred so that the required voltage levels and therefore the power consumption can be lowered [17, 20]. The evaluated threshold voltages are determined from transfer characteristics measured at room temperature (24°C), with a symmetrically applied bias-voltage V_{DS} of 2V and within a 5V TG measurement for sample 1 and sample 3 and a 7V TG measurement for sample 2, as stated above.
The evaluated threshold voltages V_{th} are presented in table 4.3 for the three measured samples. Here, it can be seen that for both samples with a high-k passivation the threshold voltage is much lower than for sample 1 with a pure SiO_2 passivation.

	Sample 1	Sample 2	Sample 3
$V_{th,n}$ (V)	1.00	0.12	0.32
$V_{th,p}$ (V)	-2.43	-1.59	-1.24

Table 4.3: *Threshold voltage values from TTG structures of all three samples fabricated at this thesis and both operation types. For the comparison the mean value of the ten best devices of each sample are considered.*

4.10.2 Sub-Threshold Slope

As it was the case for the threshold voltage the STHS was evaluated via a Python script, how this is done is explained in subsection 3.2.7.2 of the experimental techniques chapter. The STHS values are evaluated from TTG transfer characteristics captured at room temperature (24°C) with a symmetrically applied bias-voltage V_{DS} of 2V and within a 5V TG

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measurement for sample 1 and sample 3 and a 7V TG measurement for sample 2, as stated in the section above. Here, a lower STHS value is considered an improvement, because of the related reduction of dynamic power consumption and the increased switching speeds [17, 20].
Table 4.4 shows the evaluated STHS values for all three samples and both operation types. Now looking at the STHS values it can be seen that again sample 3 has the lowest for both n-type and p-type operation and again sample 1 is the worst.

	Sample 1	Sample 2	Sample 3
$STHS_n$ (mV/dec)	732.76	593.54	557.72
$STHS_p$ (mV/dec)	353.17	307.03	275.58

Table 4.4: *Inverse sub-threshold slope values from TTG structures of all three samples fabricated at this thesis and both operation types. For the comparison the mean value of the ten best devices of each sample are considered.*

4.11 Comparison of Transistor Characteristics

To set the fabricated Ge on SOI RFETs with different gate-dielectrics into perspective, the transistor characteristic parameters are presented in table 4.5 with different RFET structures from literature. To see the potential of Ge on SOI against GeOI a old sample using this technology was also measured. This GeOI sample has a 20nm thick Ge layer The conducting material used for this sample is also Al. Taken from [69] three additional samples were used as points of comparison. Two of those samples use Al-SiGe heterostructures with one sample having a SiO_2 and one having a HfO_2 passivation layer. The third sample using a Al-Si heterostructure with pure Si as semiconductor.

For all samples Al is used as contact material and Ti/Au is used for the TGs. All devices on the different samples are fabricated in a top-down procedure which results in nanosheets.
A direct comparison between the individual structures is rather difficult, because the devices are measured in different conditions, especially regarding the different TG voltages which were applied, but a general trend can be assessed. So when comparing the Ge on SOI samples of this thesis with the GeOI sample the big difference of the n-mode current, results from the fact that GeOI does only have a very small n-type current. Therefore the on-state symmetry of this sample is about two magnitudes higher than for the Ge on SOI samples. The hysteresis of the GeOI sample is much higher than for the Ge on SOI samples. Regarding the samples using GeSi it can be seen that the current here, is much higher than for the Ge on SOI samples, but especially for the one with HfO_2 as passivation layer the on-state symmetry is much worse than for Ge on SOI. The sample with pure Si has a very similar behaviour to the Ge on SOI samples, but with pure Si no NDR mode is possible.

In conclusion when considering the different characteristics of the listed devices it can

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be said, that the on-state symmetry has been improved considerably, but compared to the SiGe technology at the cost of lower on-state currents. Therefore also the off-state currents are for the Ge on SOI technology much lower. Here, it must be considered that the shown values are the average value of ten representative devices of the sample. Because of the highly symmetric behaviour it can be said that the Ge on SOI technology is very promising.

	Sample 1	Sample 2	Sample 3	GeOI 20nm	Al-SiGe (SiO_2) [69]	Al-SiGe (HfO_2) [69]	Al-Si [69]
$I_{on,n}$/W $(\mu A/\mu m)$	19.43	13.98	3.83	0.039	41.3	28.4	6.2
$J_{on,n}$ (kA/cm^2)	492.52	353.15	93.64	0.204	114.7	78.9	41.6
$I_{on,p}$/W $(\mu A/\mu m)$	29.32	43.23	13.23	10.95	85.7	174.4	11.8
$J_{on,p}$ (kA/cm^2)	846.08	1090.82	161.96	49.54	238.2	484.4	78.7
$I_{off,n}$/W $(\mu A/\mu m)$	8.36μ	696.87n	150.32n	501.13μ	24.0μ	10.0μ	300.0n
$I_{off,p}$/W $(\mu A/\mu m)$	802.25n	875.19n	198.57n	719.90μ	4.4μ	990.0n	280.0n
$I_{on,p}/I_{on,n}$	2.14	3.31	1.96	120.24	2.2	66.6	1.9
$I_{on,n}/I_{off,n}$	14.84M	33.08M	20.30M	70.52	1.9M	6.2M	21.0M
$I_{on,p}/I_{off,p}$	21.71M	134.91M	29.93M	21.47k	21.0M	420.0M	42.0M
$V_{th,n}$ (V)	1.00	0.12	0.32	1.34	0.79	0.67	1.8
$V_{th,p}$ (V)	-2.43	-1.59	-1.24	-0.01	-0.36	-0.02	-2.8
$STHS_n$ (mV/dec)	732.76	593.54	557.72	752.63	435.5	207.3	480.0
$STHS_p$ (mV/dec)	353.17	307.03	275.58	407.06	245.0	212.2	336.0

Table 4.5: *Comparison of the evaluated characteristic parameters of the Ge on SOI samples used in this work with other RFET devices in literature.*

4.12 Negative Differential Resistance - Single Top-Gate Structure

Through the use of Ge instead of Si as a channel, there is the possibility to get an electrostatically tunable negative differential resistance (NDR), which can be observed at room temperature. As stated in the experiential techniques chapter in subsection 3.2.8 the NDR in Ge is enabled by a the electron transfer effect. [23, 65, 71] The NDR mode is possible for STG and TTG structures. First the one for the STG structures will be presented. The NDR is only possible for positive voltages, because only electrons exhibit the transport mechanism necessary and so the bias-voltage was applied asymmetrically with a positive drain voltage V_D and a source voltage V_S of 0V. The TG voltages are also only swept with

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positive voltages. The measurements are taken at room temperature (24°C). The NDR can be measured over the drain current. This will be plotted as a 2-D colour map, to see the NDR directly. The derivation of the drain current over the drain voltage is also shown as a colour map. The NDR measurements that are presented here, were performed on sample 3, but all other devices also had shown a NDR.

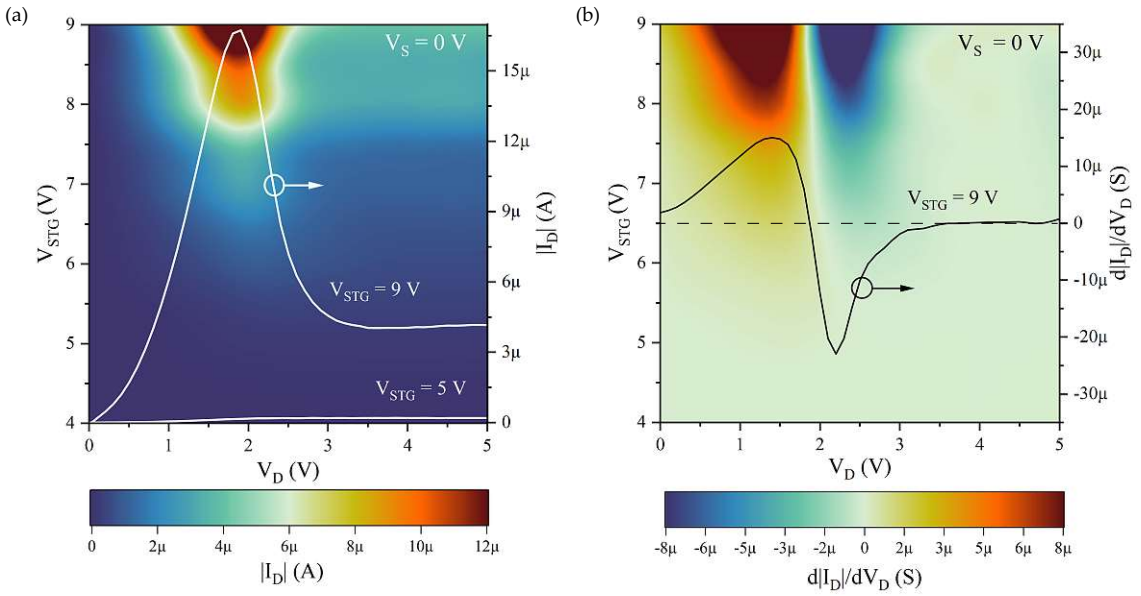

Figure 4.23: *Negative differential resistance (NDR) of a STG structure (colour maps) of sample 3. Bias-voltage V_{DS} is swept from 0V to 5V and the TG voltage V_{STG} from 9V to 4V. Subfigure (a) shows the drain current (white curves) and subfigure (b) the derivation of the drain current (black curve). The second axis from (a) shows the individual data curves for a TG voltage of 9V and 5V and in (b) it shows the derivation of the 9V curve.*

Figure 4.23 shows the colour maps of the drain current in figure 4.23a and of the derivation of the drain current over the drain voltage in figure 4.23b. The drain-voltage V_D was swept from 0V to 5V in 100mV steps and the TG voltage V_{STG} from 9V to 4V in 500mV steps. Here, it has to be mentioned that between the measurements at different TG voltages V_{STG} a pause of about three minutes was taken. The measurement was stopped at a TG voltage of 4V because no NDR peak could be observed anymore. When looking at subfigure 4.23a the curves represent the drain current for a V_{STG} of 9V and 5V to show the maximum peak and the point where the peak is nonexistent. With a peak current of 17.85μA (31.59 μA/μm) and a valley current of 3.99μA (7.07 μA/μm) a peak-to-valley-ratio (PVR) of 4.5 is reached, at a TG voltage of 9V. With lower TG voltages the current peak quickly becomes smaller and with a V_{STG} of 7V is practically nonexistent. The position of the current peak in relation to the drain voltages at which it occurs is practically the same over all TG voltages. Now looking at subfigure 4.23b where the derivation of the drain current over the drain voltage, so the differential resistance, is depicted, shows first an ohmic behavior indicated in red and afterwards the resistance increase and the non-ohmic

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plateau region of the NDR, indicated in blue. This increase of the resistance indicates the NDR, because it can clearly be seen that the differential conductance in this case is negative. The curve in the colour map depicts the derivation of the drain current for a TG voltage of 9V. Here, again it can be seen that the NDR for a TG voltage of 7V disappears.

4.13 Negative Differential Resistance - Triple Top-Gate Structure

After looking at the NDR of the STG structures now the ones of the TTG structures are investigated. Here, for the most part the things said for the STG structure still apply. The big difference here, is that there are two top-gates which can be swept, those two possibilities are shown in the following subsections. Again the drain current and its derivation will be plotted as 2-D colour maps, as it was the case for the STG structure. The measurements are also taken at room temperature (24°C).

4.13.1 NDR - V_{CG}-Sweep

Beginning with the more obvious choice the variation of the CG voltage at a fixed PG voltage. Again the bias-voltage is applied asymmetrically where the drain voltage V_D is swept from 0V to 5V in 25mV steps and a source voltage V_S of 0V. The PG voltage is set to the highest value of the CG voltage in this case 9V, as it was done for the previous measurements. The next subsections also show the reasoning for this. Finally the CG voltage is swept from 9V to 0V in 500mV steps There was a pause of three minutes between the different CG voltage steps, so that the NDR curve does not degrade.

Figure 4.24 shows the measured NDR colour maps. Subfigure 4.24a shows the drain current over the CG voltage and the drain voltage and subfigure 4.24b shows the derivation of the drain current over the drain voltage. When looking at figure 4.24a the two curves show the drain current at a CG voltage of 9V and 0V. Contrary to the STG device the NDR is clearly visible for most of the used CG voltages and even has a similar peak value. The peak value of the current lays at 13.37μA (20.45 μA/μm) and a valley value of 2.41μA (3.69 μA/μm), which results in a PVR of approximately 5.5. At 1V the peak vanishes, as can be seen at the 0V drain current curve the drain current also does not fall as much as for the STG device. Again the drain current peak occurs at the same drain voltages for the different CG voltages, so its position is stable. The periodic patterns along the CG voltages can be attributed to measurement artefacts. In subfigure 4.24b the NDR can be directly seen indicated at the blue area, which shows a negative derivation of the drain current over the drain voltage, meaning a negative differential resistance. Here, it can also be seen that the NDR can be observed until a CG voltage of 1V. The curve in the subfigure shows the derivation of the drain current at a CG voltage of 9V.

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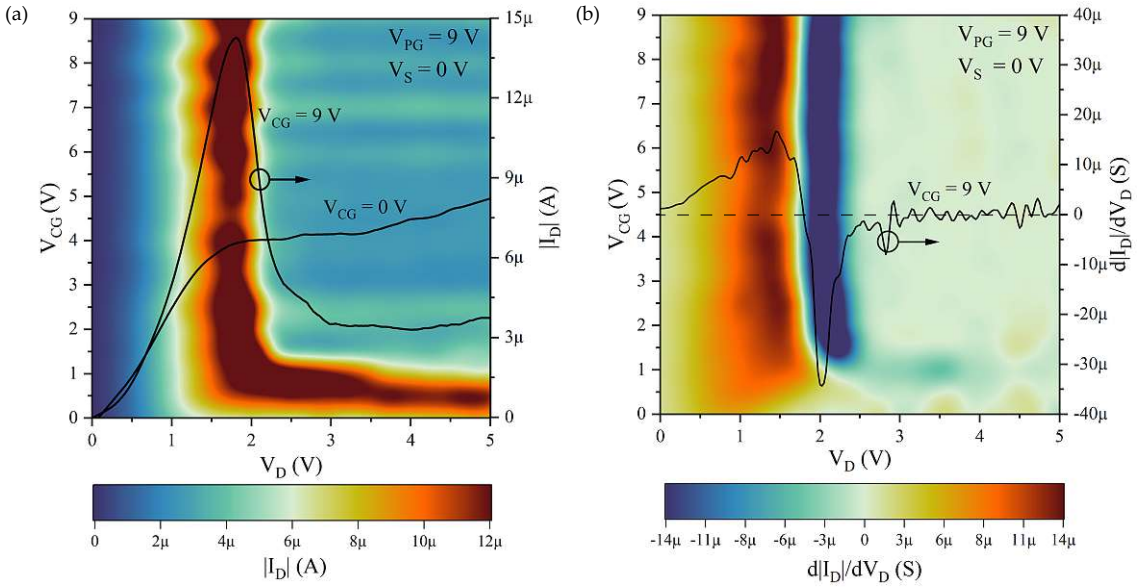

Figure 4.24: *NDR of a TTG structure (colour maps) of sample 3. Bias-voltage V_{DS} is swept from 0V to 5V and the CG voltage V_{CG} from 9V to 0V and PG voltage V_{PG} is set to 9V. Subfigure (a) shows the drain current (black curves) and subfigure (b) the derivation of the drain current (black curve). The second axis from (a) shows the individual data curves for a CG voltage of 9V and 0V and in (b) it shows the derivation of the 9V curve.*

4.13.2 NDR - V_{PG}-Sweep

The second parameter which can be swept is the PG voltage here, now the CG voltage is kept at a constant 9V and the PG voltage is swept from 9V to 2V with 500mV steps and a pause between the steps of three minutes was taken. The drain voltage V_D was again swept from 0V to 5V in 25mV steps with a fixed source voltage V_S of 0V. So the same measurement as before only the roles of CG and PG are switched.

Figure 4.25 shows the measured colour maps, where subfigure 4.25a shows the drain current over the PG voltage and the drain voltage and subfigure 4.25b shows the derivation of the drain current over the drain voltage. When looking at figure 4.25a the curves depict the drain current at a PG voltage of 9V and 4V. The peak value of the current lays at 16.34μA (24.98 μA/μm) and the valley value of 4.01μA (6.13 μA/μm), which means the PVR lays at 4.1. Here, it can clearly be seen that for PG voltages of under 7V there is no NDR anymore. There is no shift of the current peaks at the drain voltage over the PG voltage. The NDR can be clearly seen in subfigure 4.25b where it is indicated in the blue area. The disappearance of the NDR at PG voltages of 7V can be observed. The curve in the subplot shows the derivation of the drain current over the drain voltage at a PG voltage of 9V. This explains why the highest CG voltage is always taken as the PG voltage, because for lower PG voltages the NDR peak gets much smaller or disappears completely.

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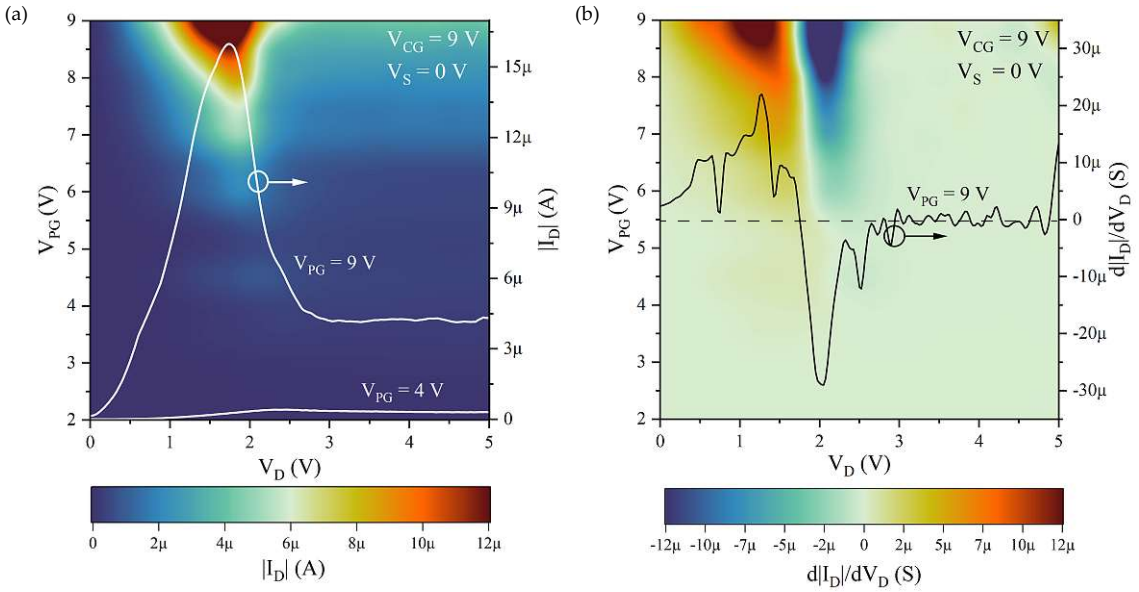

Figure 4.25: *NDR of a TTG structure (colour maps) of sample 3. Bias-voltage V_{DS} is swept from 0V to 5V and the PG voltage V_{PG} from 9V to 2V and PG voltage V_{PG} is set to 9V. Subfigure (a) shows the drain current (white curves) and subfigure (b) the derivation of the drain current (black curve). The second axis from (a) shows the individual data curves for a PG voltage of 9V and 2V and in (b) it shows the derivation of the 9V curve.*

In conclusion, it can be said that the Ge on SOI technology is a promising candidate for RFET devices considering the on-state symmetry and the possibility for a NDR mode at room temperature.

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Chapter 5

Summary and Outlook

For this thesis RFET structures are fabricated and electrically characterised. A Ge on SOI substrate was used to obtain Al-Si-Ge-Al multi-heterojunction contacts. The starting point for the devices is a SOI substrate on which a 4nm thick Ge layer is grown by MBE, at the partners JKU Linz. On top of this stack a sacrificial Si capping layer is added. This capping layer enables the formation of TG interfaces with a low trap density layer, because of the formation of a Si-SiO_2 interface. In order to form abrupt, reliable, reproducible contacts, a single crystalline Al was used and thermally activated diffusion of Al into the semiconducting nanosheet stack is performed. Two individual metal-semiconductor junctions are formed at the ends of the nanostructure, so the TGs can be places accordingly. To passivate the nanostructure either a pure thermally grown SiO_2 or a combination of thermally grown SiO_2 and a high-k dielectric like HfO_2 or ZrO_2 grown with an ALD process is used. Then the TGs are fabricated out of 10nm Ti and 100nm Au. As stated in the Project Evolution in section 4.2 in total five samples were fabricated, one with pure SiO_2, one with HfO_2 and three with ZrO_2 as passivation layer. The difference of the three samples with ZrO_2 passivation layer was the thickness and dielectric composition of the passivation. Only the sample with the thickest one was discussed in this thesis, because it exhibited the best results. Also the two samples with the different passivation layers are presented. Those three samples are compared to show the evolution of the samples. The TGs are realised as STG and TTG depending on the length of the semiconducting segment.

For the electrical characterisation of the RFET structures transfer characteristic, output characteristic and PG-sweep characteristic measurements are performed. The temperature dependent behaviour was investigated and from this data the eSBH and the effective activation energy was extracted. Also the RFET characteristic parameters are evaluated from the transfer characteristics. These measurements, with the exception of the PG-sweep, which shows the TG voltage dependent switching of the TTG structure, were performed for both STG and TTG structures. Additionally it had been shown that the fabricated

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structures are capable of being operated in a NDR mode. The NDR is also measured for both STG and TTG but only investigated in detail for the best performing devices, i.e. sample 3.
Because the fabricated devices use the same material system and are fabricated equally except for the passivation layer their performance can be compared in terms of the used passivation layers. Also the electric characterisation was made under the same conditions, with the only difference being the TG voltage for sample 2 which was 7V instead of 5V, so the current strength of sample 2 could not be compared directly. When looking at the three samples, it can be seen that introducing an additional high-k dielectric layer reduces the on-state current a bit, but the off-state current is drastically reduced. In case of sample 3 the on-state current symmetry is much better over a wider number of devices. A further goal for the samples with high-k dielectrics was to shift the threshold voltage towards more positive voltages especially for the p-type operation. This was achieved especially with sample 3, where now both threshold voltages are closer to 0V as desired. Also the STHS values for both operation types are the lowest and therefore the best for sample 3. As for the quite low on-state currents from sample 3. Here, a thinner passivation layer would be a possible solution this was tried for sample 4 and sample 5, where a bit higher currents were reached but the overall behaviour of the devices was worse. Therefore those were not shown in this thesis, never the less this approach should be pursued for further investigation. Another big improvement for the samples with the high-k passivation is the temperature stability of those. Where the on-state p-type operation current for sample 1 drops down for higher temperatures, for the other two samples it was very stable, with a hardly noticeable decay. The off-state current rises for all three sample but even for temperatures of 125°C still is acceptably low. The thermal stability of the samples with high-k dielectrics is exceptionally good up to temperatures of 125°C.
To obtain a comparison to a RFET using a GeOI material system an existing sample using 20nm Ge was also measured. This substrate system has the drawback that it is much more expensive. When looking at its electrical characterisation, the transistor characteristics are much worse. The most glaring issue is the practically non existent n-type operation current and therefore, the on-state symmetry suffers a lot, because the p-type operation current is quite similar to the one of sample 3. The off-state current for the GeOI sample is much higher than for all of the Ge on SOI samples. In terms of the temperature stability of the GeOI sample for the n-type operation, the on-state disappears because of the rising off-state current at a very low 50°C. Another point which needs to be considered is the quite high hysteresis for this GeOI sample, where non of the Ge on SOI samples show a noteworthy hysteresis. This sample also exhibits no NDR even though, Ge was used. The degraded performance of the GeOI sample is attributed to the low quality of the BOX.
So it can be clearly seen that because of the characteristic parameters of the used Al-Si-Ge-Al material system, this is very promising candidate for the fabrication of symmetric RFET structures.

From the point of view of the semiconductor industry it is favourable to fabricate transistor devices at a wafer-scale top-down production. Also the use of Ge on SOI is preferred over

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GeOI, because of its lower cost and easier fabrication process. Therefore, the top-down fabricated Ge on SOI RFETs presented in this work combine the chip-scale production from currently used technologies with the reconfigurability of the new one. Also the importance of the on-state symmetry can be seen when looking at CMOS circuits, where in order to get a symmetric behaviour the n-MOS and p-MOS transistors exhibit different sizes. A RFET device with similar on-state currents for both operation modes can replace the CMOS transistors with transistors of equal size, where the charge carrier type which is used, can be selected during operation of the transistor and has not to be specified at the fabrication. In order to use this technology for this purpose a reliable, reproducible and well established fabrication process, especially for the formation of the metal-semiconductor junction must be established. In addition the possibility to reconfigure the operation type enables more enhanced logic circuits with less transistors used in total. The fabricated RFET of this thesis can achieve a remarkably symmetric behaviour due to the used Ge on SOI itself and not through other additional actions taken. [19, 20, 22]

To offer an outlook, there are still aspects which can be investigated with this material system. The thickness of the passivation layer / gate-dielectric can be changed to get higher currents with the same TG voltage used, while still having the same reliability like the shown sample. The number of top-gates can be changed either to use the simpler dual top-gate or to integrate further gates to get the wired-logic ability of N-TG structures. The next step to the N-TG structures is to establish basic logic functions, like NAND or inverter circuits out of the Ge on SOI RFETs. Another approach to get higher currents is the parallel integration of multiple nanosheets between the S/D-pads, instead of the single ones used in this work. A good controlled diffusion process is necessary in order to contact the multiple metal-semiconductor junctions with the TGs. With the presented NDR mode of the Ge on SOI RFETs multi-level logic circuits can be fabricated and therefore systems which exceed the possibilities of CMOS technology can be obtained.

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List of Abbreviations

Al	Aluminum
ALD	Atomic Layer Deposition
Au	Gold
BG	Back-Gate
BHF	Buffered Hydrofluoric Acid
BOX	Buried Oxide
CB	Conduction Band
CG	Control-Gate
CMOS	Complementary Metal-Oxide-Semiconductor
CVD	Chemical Vapor Deposition
DTG	Dual Top-Gate
EBL	Electron Beam Lithography
eSBH	Effective Schottky Barrier Height
FCC	Face-Centered Cubic
FE	Field Emission
FET	Field-Effect Transistor
Ge	Germanium
GeO	Germanium Monoxide
GeO_2	Germanium Dioxide
GeOI	Germanium On Insulator
H	Hydrogen
HF	Hydrofluoric Acid
HfO_2	Hafnium Dixide
I/V	Current-Voltage
MBE	Molecular Beam Epitaxy
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
N	Nitrogen
Ni	Nickel
NDR	Negative Differential Resistance
N-TG	Multi Top-Gate
O	Oxygen

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PG	Polarity-Gate
PMMA	Polymethylmethacrylat
PVCR	Peak-to-Valley Current Ratio
PVD	Physical Vapor Deposition
RTA	Rapid Thermal Annealing
RFET	Reconfigurable Field-Effect Transistor
RIE	Reactive-Ion Etching
RTA	Rapid Thermal Annealer
S/D	Source / Drain
SBFET	Schottky Barrier Field Effect Transistor
SEM	Scanning Electron Microscopy
SF_6	Sulphur Hexafluoride
Si	Silicon
SiO_2	Silicon Dioxide
SMU	Source Measure Unit
SOI	Silicon On Insulator
STG	Single Top-Gate
STHS	Sub-Threshold Slope
TE	Thermionic Emission
TEM	Transmission Electron Microscopy
TFE	Thermionic Field Emission
Ti	Titanium
TG	Top-Gate
TTG	Triple Top-Gate
VB	Valence Band
ZrO_2	Zirconium Dioxide

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List of Symbols

A^*	Richardson Constant
χ_S	Electron Affinity
E_C	Conduction Band Energy
E_F	Fermi Energy
E_G	Band Gap Energy
E_V	Valence Band Energy
E_{vac}	Vacuum Level Energy
$q\phi_B$	Effective Schottky Barrier
ϕ_m	Metal Work Function
ϕ_s	Semiconductor Work Function
g_m	Transconductance
h	Planck Constant
I	Current
I_0	Reverse Saturation Current
I_D	Drain Current
I_{DS}	Drain Source Current
k_B	Boltzmann Constant
μ_e	Electron Mobility
μ_e	Hole Mobility
q	Elementary Charge
T	Temperature
V	Voltage
V_{CG}	Control Gate Voltage
V_D	Drain Voltage
V_{DS}	Drain Source Voltage
V_{PG}	Polarity Gate Voltage
V_S	Source Voltage
V_{STG}	Single Top-Gate Voltage
V_{th}	Threshold Voltage
W	Gate Width

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