Master's Thesis

Reconfigurable Si Field-Effect Transistors with Crystalline Al Contacts Enabling Adaptive Complementary and Combinational Logic

submitted in partial fulfillment
of the requirements of the degree of
Master of Science

at Technische Universität Wien
Institute of Solid State Electronics

under supervision of

Univ.Prof. Dipl.Ing. Univ. Dr.-Ing. Walter Michael Weber
and
Univ.Ass. Dipl.-Ing. Dr.techn. Masiar Sistani, BSc

by
Özgür Demirkiran, BSc

Vienna, July 2023

Statutory Declaration

I declare, that I have authored the present work independently according to the code of conduct, that I have not used other than the declared sources and that I have explicitly marked all material quoted either literally or by content from the used sources. This work was not yet submitted to any examination procedure neither in Austria, nor in any other country.

Erklärung zur Verfassung der Arbeit

Hiermit erkläre ich, dass die vorliegende Arbeit gemäß dem Code of Conduct – Regeln zur Sicherung guter wissenschaftlicher Praxis – ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel, angefertigt wurde. Die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet. Die Arbeit wurde bisher weder im In- noch im Ausland in gleicher oder in ähnlicher Form in anderen Prüfungsverfahren vorgelegt.

Vienna, July 2023 ...

Özgür Demirkiran

Abstract

The remarkable progress in electronics is marked by the continuous miniaturization of device sizes however, the ongoing scaling strategy, is not sustainable in the long term, as physical limits will be reached soon. Further, the increase in data processing requirements and the resulting complexity of signal routing on a chip has posed significant challenges in terms of raised power consumption and diminished reliability. In order to optimize the performance of information processing, it is crucial to introduce novel concepts. One potentially effective strategy involves the advancement of reconfigurable logic or neuromorphic devices. These reconfigurable field-effect transistors (RFETs) are characterized by their dynamic p- and n-channel switching behavior making them highly regarded as a potential breakthrough for future computer systems. RFETs offer the advantage over conventional complementary circuits that the transistor widths of n- and p-FETs do not need to be individually adjusted to achieve equal current densities, that enables the realization of multifunctional devices and dynamically reconfigurable complementary logic gates with a reduced number of devices compared to unipolar transistors.
In this regard, this master thesis deals with the fabrication of reconfigurable Field-Effect Transistors (RFET) using a top-down approach on a silicon-on-insulator (SOI) wafer. The thermally induced metal-semiconductor exchange reaction of Al and Si resulting in the formation of the underlying Al-Si-Al heterostructure, is a crucial process for ensuring the reliable and consistent occurrence of an abrupt transition. This exchange reaction process is essential for reproduceable contacts with defined properties. Silicon dioxide (SiO_2) serves as the gate dielectric, positioned between the semiconductor channel and the top gates. This material is chosen for its high purity and low charge carrier trapping, resulting in minimal hysteresis in the devices. Through a comprehensive statistical analysis, it is demonstrated that significant advancements have been made in key transistor parameters, such as the symmetry of on-currents from p-FET to n-FET. Moreover, these advancements have resulted in exceptional stability and reproducibility. Consequently, complementary logic gates could be manufactured using cascaded RFETs. The reconfigurability at the circuit level of an inverter comprised of two RFETs on a semiconductor nanostructure was effectively demonstrated. A reconfigurable MIN3-gate capable of dynamic switching between NAND/NOR operations was successfully implemented by integrating only three RFETs. An XOR/XNOR-gate with dynamic switching could be created using just four RFETs. Therefore, the quantity of devices can be decreased in comparison to circuits with traditional transistors. The gates possess a full-swing output voltage and share identical supply and signal voltages, indicating their potential to realize complex circuits and microprocessors with reconfigurable circuits.

Kurzfassung

Der bemerkenswerte Fortschritt der Elektronik ist durch die kontiuerliche Verkleinerung von Bauteilgrößen gekennzeichnet, wobei diese Skalierungsstrategie langfristig nicht mehr aufrecht zu erhalten ist, da die physikalischen Grenzen bald erreicht sein werden. Die Skalierung der Bauelemente bei zunehmenden Bedarf an Datenverarbeitung und somit der Komplexität der Signalführung auf einem Chip hat gleichzeitig zu Herausforderungen in Bezug auf erhöhten Stromverbrauch und verringerte Zuverlässigkeit geführt. Um die Leistungsfähigkeit der Informationsverarbeitung weiter zu steigern, müssen andere Konzepte eingeführt werden. Ein viel versprechender Ansatz ist die Entwicklung rekonfigurierbarer logischer oder neuromorpher Bauelemente. Diese rekonfigurierbaren Feldeffekttransistoren (RFET) zeichnen sich durch ihr dynamisches p- und n-Kanal-Schaltverhalten aus und gelten daher als eines der vielversprechendsten neuen Möglichkeiten für zukünftige Computersysteme. RFETs bieten gegenüber konventionellen komplementären Schaltungen den Vorteil, dass die Transistorweiten von n- und p-FETs nicht individuell angepasst werden müssen, um gleiche Stromdichten zu erreichen, dass die Realisierung multifunktionaler Bauelemente und dynamisch rekonfigurierbarer komplementärer Logikgatter mit einer reduzierten Anzahl von Bauelementen im Vergleich zu unipolaren Transistoren einhergeht. Diese Masterarbeit beschäftigt sich mit der Herstellung von RFETs auf einem Silicon-on-Insulator-Wafer (SOI) mittels Top-Down-Methode. Die thermisch aktivierte Metall-Halbleiter Austauschreaktion von Al und Si, die zur Bildung der zugrunde liegenden Al-Si-Al-Heterostruktur führt, ist ein entscheidender Prozess, um das zuverlässige und reproduzierbare Auftreten eines abrupten Übergang zu gewährleisten. Als Gate-Dielektrikum zwischen dem Halbleiterkanal und den Top-Gates wird Siliziumdioxid (SiO_2) verwendet, das aufgrund seiner Reinheit und der damit verbundenen geringen Ladungsträgerfangstellen für eine geringe Hysterese der Bauelemente sorgt. Durch statistische Untersuchung konnte gezeigt werden, dass sehr gute Werte der wichtigsten Transistorgrößen, wie z.b. die Symmetrie der On-Ströme von p-FET zu n-FET, erreicht werden und insbesondere eine ausgezeichnete Stabilität und Reproduzierbarkeit vorliegt. Damit konnten komplementäre Logikgatter aus kaskadierten RFETs hergestellt werden. Ein Inverter aus zwei RFETs auf einer Halbleiter-Nanostruktur wurde realisiert und die Rekonfigurierbarkeit auf Schaltungsebene erfolgreich demonstriert. Durch die Integration von nur drei RFETs konnte ein rekonfigurierbares MIN3-Gatter realisiert werden, das eine dynamische Umschaltung zwischen NAND/NOR ermöglicht. Mit nur vier RFETs kon- nte ein XOR/XNOR-Gatter mit dynamischer Umschaltung implementiert werden. Damit kann bezogen auf die Anzahl der Transistoren der Bauelementeanteil im Vergleich zu konventionellen Transistoren reduziert werden. Diese Gatter weisen einen full-output-swing und gleiche Versorgungs- und Signalspannungen auf, was deren Potential aufzeigt, um komplexe Schaltungen und Mikroprozessoren mit rekonfigurierbaren Schaltungen zu realisieren.

Acknowledgement

At the conclusion of a successfully completed work, I would like to take this opportunity to express my sincere gratitude to those people without whose assistance the work would not be attainable in this manner.

First, I want express my sincere appreciation to my supervisor Walter M. Weber, for your guidance and mentorship during my Masters thesis. Your expertise and constructive feedback in the group meetings with always clear explanations allowed me to delve deeper into the subject matter and gain new perspectives. The manner in which you effectively manage this working group alongside with your other commitments, consistently exhibiting a positive attitude and willingness for help, is truly remarkable.
I would also like to express my gratitude to my second supervisor Masiar Sistani. Your dedication and attention to detail have been indispensable and your insightful interpretations significantly improved the quality of the work and with your exceptional organizational skills you kept us on track throughout the entire process. But it wasnt just enjoyable to work together in the office, it was also great to discuss and share experiences with you outside of work.
Lukas Wind, also big gratitude to you, with whom I spent most of my time while working on this project. Your willingness to step in and help whenever needed was truly commendable.

I would also like to extend my thanks to the entire team as I always felt welcome and the inspiring environment, the meaningful discussions and all the insights were a great experience. Individually and collectively, you have all played an integral role in making this thesis a reality and I am grateful to have had such an incredible team, naming Martina Bazikova, Raphael Behrle, Andreas Fuchsberger, Kihye Kim, Melisa Mustajbasic and Daniele Nazzari.

The greatest appreciation goes to my family, including my parents, sister, and especially my brother. Words cannot fully capture the depth of my appreciation for all that you have done for me, even it has been sometimes a challenging journey the more I am profoundly grateful for your presence in my life.

Contents

Chapter 1

Introduction

The electronics industry has a profound impact on society over the period of the last five decades. The productivity of individuals and machines has witnessed a significant increase such as, the availability of information is now accessible within milliseconds and the vast majority of people now being linked to the rest of the globe. Additionally, there has been a notable advancement in machine intelligence, with certain machines exhibiting autonomous capabilities. The most important factor in these accomplishments is the progress made in semiconductor technology. The fundamental elements of a modern society's digital DNA are therefore semiconductors. They are of such significance that governments all over the globe are actively promoting, investing in, and protecting the intellectual property and manufacture of semiconductors. The most recent examples of these efforts are the European Chips Act and the United States CHIPS and Science Act. The development of modern semiconductors can be attributed to the necessity of reducing the size of electronic components in order to efficiently integrate advanced electronic systems into progressively smaller physical dimensions in a cost-effective manner. This phenomenon serves as the primary catalyst for technological progress and is associated with a fundamental principle commonly referred to as Moore's Law.[44]
The bipolar transistor was invented in 1947 by three researchers at the Bell Laboratories, William Shockley, John Bardeen, and Walter Brattain. In the year 1958, after a span of over a decade, Jack Kilby from Texas Instruments demonstrated the very first integrated circuit (IC). In the subsequent year, Robert Noyce and Gordon Moore, prominent figures at Fairchild Semiconductor, successfully designed the planar transistor. That invention served as a significant advancement for the contemporary semiconductor industry, as it unveiled the possibility of expanding the cost and operational advantages of transistors to all mass manufactured electronic circuits. Consequently, the semiconductor industry has experienced significant exponential growth since that period. The phenomenon, initially observed by Gordon Moore, involves the postulation made in 1965 regarding the doubling of component density every 18 months and circuit speed every two years.[44] Even though

the industry is getting closer and closer to the single atom physical barrier of circuit design, there are still attempts being made to develop alternatives to circuits that are implemented with traditional transistors. These alternatives, such as quantum and neuromorphic computing, have the potential to revolutionize the design and manufacturing processes of integrated circuits.

The motivation of the research in this thesis is motivated and originates in the bottleneck of the semiconductor sector, whose fast economic expansion over the last three decades has been fueled by shrinking transistor sizes. This scaling strategy, regardless of other technological issues, cannot be sustained in the long term due to physical constraints. Transistor designs with extended functionality have the ability to reduce the size of a circuit while increasing its functional space, allowing for ongoing growth of electronics after the end of classical scaling. The "big problem" below this technological node is the transistor structure.[30] The stringent conditions required for doping, such as ultra-shallow junctions, profiling implants at ever-smaller dimensions, the randomness of doping in small channel lengths, and low series resistance necessitating doping with activation above the solid solubility limit of silicon, are responsible for a number of issues with conventional MOSFETs. To tackle these and other challenges, alternative device topologies are being investigated to replace MOSFETs when traditional scaling fails. A structure of this type is the Schottky barrier MOSFET (SBFET). In this device, the issues associated with doping are removed entirely by constructing source and drain connections from metallic silicide or, as in the focus of this study, of pure aluminum. This device is not only more cost effective due to its easier manufacture, but its scaling properties are also superior to those of ordinary MOSFETs.[69] In particular, these junctions result in a low series resistance, offer a simple approach for producing ultra-shallow junctions, and circumvent the solid solubility constraint associated with doping. With regard to functional diversification, the concept of a reconfigurable field effect transistor (RFET) was introduced in the first decade of the 21st century, which are based on these Schottky barriers and, due to their architecture, enable the adjustment of the corresponding charge carrier type for a particular device at runtime and have thus positioned themselves as one of the alternatives to CMOS technology.[24, 74] On the basis of current data and observations, it is evident that CMOS will continue to dominate IC chip production in the coming years. In this regard, the CMOS compatibility of RFETs in this work provides a significant fabrication advantage that could be used to complement CMOS or enhance performance in specific application fields.

A primary objective of this work is a comprehensive experimental examination of the device functionality and to assess the viability of RFETs for practical applications, such as logic based circuits. For this purpose, the thesis starts in Chapter 2 with a description of the materials used and physical processes, which leads to the introduction of the SBFET and the RFET concept. Chapter 3 gives an overview of the fabrication and the electrical characterisation/evaluation of these devices, followed by a discussion of the results in Chapter 4, and finally a summary and outlook in Chapter 5.

Chapter 2

Theory

This chapter is primarily concerned with providing an overview of the fundamental theory that is of essential importance for the work presented here. Starting with the relevant materials used for the fabrication of the devices in section 2.1, the physical and chemical properties as well as their behaviour are explained. In particular, these are aluminum (Al), silicon (Si), silicon oxide (SiO_2) and the so-called silicon on insulator technology (SOI). This is followed by an explanation of the Schottky junctions in section 2.2.2 which are fundamental to these devices, including the underlying physical phenomena and behaviour of these interface. Based on this, the Schottky barrier field effect transistor (SBFET) is introduced to give the reader a proper introduction to the subject, see section 2.3. In the following sections 2.3.1 and 2.3.2, the basic concept of the reconfigurable transistor (RFET), its possibilities and further applications in logic gates, which are also covered in this thesis, are presented.

2.1 Materials

In this section, the materials aluminum (Al) and silicon (Si) are briefly introduced, on which the RFETs fabricated in this work are based including the native oxide of silicon (SiO_2), which acts as gate dielectric. Also an insight into the substrate used, namely the Silicon on insulator (SOI) is given. This part is then rounded off by an examination of the aluminum-silicon (Al-Si) System and the most important processes involved.

2.1.1 Aluminum

Aluminum is probably one of the elements that has been studied more thoroughly than almost any other in terms of its properties and processing, and its range of applications is correspondingly broad. In the periodic table it is located in the III - main group with atomic number 13 and has the property of being the lightest element within this group.

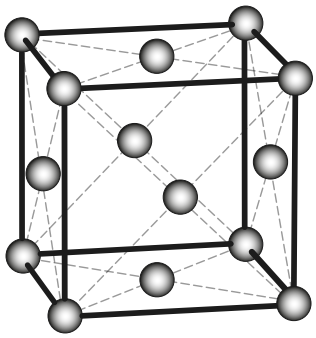


Figure 2.1: *Aluminum crystalline lattice with face-centered-cubic (fcc) structure. Atoms arranged at the corners and center of each cube face of the cell. Lattice constant is* $a_{\mathrm{Al}} = 4.049\,\text{Å}$ *[63].*

The crystal form of aluminum, like most metals, is face centered cubic (fcc) with a lattice constant of $a_{\mathrm{Al}} = 4.049\,\text{Å}$. Aluminum is the most conductive metal relative to its density due to its resistivity of $2.5 \times 10^{-8}\,\Omega\,\mathrm{m}$ [14]. This allows space-saving metallization in microelectronics, which is why it is used in preference to other metals such as copper or gold. In addition, copper and gold cause impurities in silicon, which are located in the middle of the bandgap, unlike aluminum. [22] These impurities cause recombination currents, which massively affect the functionality of devices.

Aluminum is extremely reactive with ambient oxygen, so exposed to air, a approximately 3 nm thick passivation layer of amorphous aluminum oxide (Al_2O_3) forms on any exposed aluminum surface within hundreds of picoseconds, which effectively protects it from further corrosion. [7] Compared to ceramic materials, its heat conductivity is relatively high $30\,\mathrm{W\,m^{-1}\,K^{-1}}$ [54]. In its most common crystalline form, known as corundum or α - aluminium oxide, it is suited for use as an abrasive due to its hardness. It has an elasticity modulus of up to 400 GPa in its pure form, is very mechanically stressable. Its high dielectric strength of $17 \times 10^6\,\mathrm{V\,m^{-1}}$ and high resistivity of $1.012 \times 10^3\,\Omega\,\mathrm{m}$ make it stand out as a particularly effective insulator. With a relative permittivity of 9 it therefore belongs to high-k materials in the broadest sense. [72] Al_2O_3 is non soluble in water and is only attacked by acids with a pH value below 4.5 or by alkalis above a pH value of 8.5. In addition, aluminum does not form a metal silicide with silicon, but the two materials interpenetrate in an induced crystallization process; this phenomenon is described in more detail in the following sections as it is of essential importance in the presented devices.

2.1.2 Silicon

Due to its importance in the semiconductor industry, silicon is the most studied semiconductor material. This importance can be attributed to the excellent properties of silicon dioxide (SiO_2), which can be easily obtained by thermal oxidation of the pure material. Silicon is abundant in the earth's crust, although it is not normally found in its pure form, but can be easily converted to its near-pure form using techniques that have been proven.

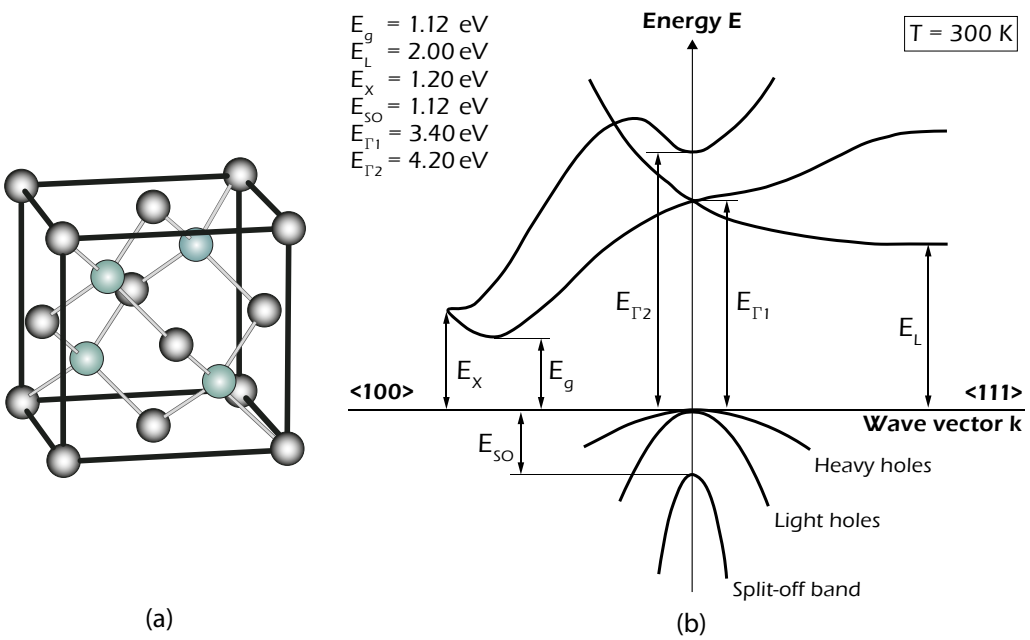


Figure 2.2: *(a) Silicon crystallographic structure. It has the diamond structure, which consists of two FCC (face centered cubic) structures with identical atoms -depicted as black and blue- shifted along the diagonal with respect to each other by (1/4, 1/4, 1/4) of the lattice constant* $a_{\mathrm{Si}} = 5.431\,\text{Å}$. *(b) Silicon band structure at* 300 K *with conduction band minima close to the X-valley in the crystallographic* $k = \langle 100 \rangle$ *direction and relevant band gap energies. Picture adapted from [49]*

Silicon is a group IV element with atomic number 14 and crystallizes in a cubic diamond structure. As depicted in figure 2.2, the diamond structure can be viewed as two face-center cubic (fcc) Bravias lattices moved along the diagonal by one-fourth of their length i.e. atoms in green are shifted relative to atoms in grey. Silicon is an indirect semiconductor with a band gap value of about $E_{\mathrm{g}} = 1.12\,\text{eV}$ at 300 K in the Δ - point [63][49], as evidenced by different wave vectors k for the conduction band minimum and the valence band maximum, which is why it is not favored for optoelectronic applications, although there are efforts by various approaches to make it usable. This band gap is not a constant value but is temperature dependent, it is inversely proportional and becomes smaller with increasing temperature.

The band structure in figure 2.2 can be described by solving the Schrödinger equation within the periodic crystal potential, for this there are different approaches which will not be discussed here, a good explanation can be found in [52]. The Brillouin zone indicates, that the conduction band minima for silicon are located on six equivalent identical Δ - lines along <100> - directions, this Δ - line is the energy dispersion along the straight line from point Γ to point X, and is often known as the Δ - line (for more details see [38, 58]). Typically, for diamond crystals such as silicon, the conduction band has three minima: one at k = 0 (called the Γ point), one along <111> - directions at the boundary of the first Brillouin zone (called L point), and one along <100> - directions near the zone

boundary, i.e. close to the X point, which represents the absolute minima. The valence bands consist of three subbands, a light hole band, a heavy hole band and a split-off band. At k = 0, the light hole band and heavy hole band are degenerate, however the energy of the split-off band is E_{SO} less.

In nearness of the conduction band minima, the energy dispersion relation $E(k)$ can be described by the parabolic approximation, notice that this relation looks like that of an electron in free space except that the free electron mass m_0 is replaced by the effective mass m_e^*; meaning that the electron responds to the outside world as if it had this mass, of course the real electron mass does not change

$$E_{\mathrm{k}} = E_{\mathrm{c}} + \frac{\hbar^2 k^2}{2m_e^*} \tag{2.1}$$

where E_c indicates the conduction band minima, $\hbar$ is the Planck constant and m_e^* is the effective mass of the electrons. With a well known $E - k$ relationship, the effective mass can be obtained from the second derivative of E with respect to $\hbar k$

$$m_e^* = \frac{d^2 E}{d(\hbar^2 k^2)} \tag{2.2}$$

Therefore, the narrower the parabola, the smaller the effective mass. For example GaAs has a very narrow conduction band parabola and the electron effective mass is $0.07m_0$, for silicon it is $0.19m_0$ (<100> - direction). Further, based on the Drude model it can be shown that, in the steady state and assuming an isotropic material, the following can be concluded for the mobility μ of the charge carriers, τ is the average relaxation time and indicates the scattering events

$$\mu = -\frac{q\tau}{m^*} \tag{2.3}$$

From this it can be seen that the mobility depends only on the band curvature due to the effective mass as well as on the scattering losses. For the mobility in silicon, one obtains $\mu_{\mathrm{n}} = 1400\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for the case of electrons and $\mu_{\mathrm{p}} = 450\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for the case of holes. The much higher electron mobility than that of the holes is a result of the smaller effective mass and the lower scattering probability of the electrons. [22, 49, 63]

In general, intrinsic Silicon has a weak electrical conductivity, but can be doped with other atoms, e.g. boron, aluminum, indium (trivalent) and phosphorus, arsenic, antimony (pentavalent) to increase the conductivity. Note, however, that the silicon used in this work is not doped.

2.1.3 Dielectrics

As mentioned before, whenever silicon is exposed to air, the Si-wafers surface oxidizes to silicon dioxide (SiO_2). This native SiO_2 with an approximately thickness of 10-20 Å is a high quality electrical insulator that can be also utilized as a barrier material during impurity implantation or diffusion. In semiconductor devices such as metal oxide semiconductor (MOS) transistors and multilevel metallization structures such as multichip modules, the SiO_2 layer plays a crucial function. One of the key processing issues that led to silicon becoming the predominant semiconductor material used in integrated circuits today was its ability to generate this stable native oxide. SiO_2 possesses a multitude of desirable qualities and benefits [32], in contrast to other materials that have one or more drawbacks, i.e. the layers are easily grown thermally on silicon or deposited on a variety of substrates, they are resistant to the majority of chemicals used in silicon processing and yet they can be easily patterned and selectively etched with specific chemicals or dry etched with plasmas, they prevent the diffusion of dopants as well as a wide variety of other unwanted impurities, the interface is stable over time and has a high-temperature stability up to 1873 K, which is essential for process and device integration. Compared to Al_2O_3, SiO_2 has a lower dielectric constant of 3.9 but is an excellent insulator with a high breakdown strength of 10 MV/cm, as a reference in air the value is about 30 kV/cm [63] and a wide band gap, at least 8 times higher than silicon.

Two types of processes are used to build thicker SiO_2 layers. The first is to undertake a thermal oxidation of silicon, which generates high quality interfaces between silicon and silicon dioxide, and the second is to deposit oxide layers via a chemical vapour reaction process, the so called CVD (chemical vapour deposition) technique. This method is used for filling trenches, creating a thin insulator between layers, and constructing a diffusion source or getterer. In the structures fabricated in the scope of the thesis, SiO_2 with former method was used exclusively as a dielectric. This thermally grown oxide can be obtained by two methods, whereby the following chemical processes of oxidation occur on the surface of the substrate in the presence of pure oxygen or water vapor conditions:

$$Si + O_2 \longrightarrow SiO_2$$

$$Si + 2\,H_2O \longrightarrow SiO_2 + H_2$$

First reaction is typically referred to as 'Dry oxidation' and is thermally grown, whereas the second, which takes place in the presence of water, is known as 'Wet oxidation'. When oxygen reaches the surface of Si, it can react with silicon to produce SiO_2. Initially, the growth of SiO_2 is a surface reaction only. However, once the SiO_2 thickness begins to increase, oxygen molecules must diffuse through the expanding SiO_2 layer to get into the silicon surface in order to react, so the speed of building this native oxide is first limited by the available reactants and later by the diffusion process itself. Wet oxidation reaches substantially higher oxidation rates than dry oxidation by up to four times resulting from

	SiO_2	Si_3N_4	Al_2O_3	$ZrSiO_4$	Y_2O_3	ZrO_2	Ta_2O_5	HfO_2	TiO_2
ϵ_r	3.9	7.5	9	12.6	15	23	25	25	40
E_g [eV]	9	5	8.7	6	5.6	5.8	4.4	5.7	3.5
ΔE_c [eV]	3	2	2.8	1.5	2.3	1.4	1.4	1.5	1.1
ΔE_v [eV]	4.9	1.9	4.8	3.4	2.2	3.3	1.9	3.1	1.3

Table 2.1: *Materials used as gate dielectric in semiconductor industry and the associated values of permittivity ϵ_r and band gap energy E_g. ΔE_c and ΔE_v indicates the conduction and valence band offsets. [8, 35, 53, 78, 83]*

the ability of hydroxide OH^- to penetrate through the already formed oxide much more rapidly than oxygen O_2. Both grown silicon dioxides are amorphous, the thermally grown dry oxide has a little higher density than wet oxide, resulting in a better oxide quality. During Si oxidation, temperature is the main ambient parameter that is used to control the growth of oxide, as it is increased, the oxidation rate can increase significantly. Also the hydrostatic pressure and the crystal orientation of the Si-wafer has an influence, so it is not oxidized at the same rate in each crystallographic orientation, according to relevant studies [36]. This Oxide growth appears to be quicker on <111> oriented Si than on <100> oriented Si, this orientations indicates also the upper <111> and lower <100> boundaries for oxidation rates, respectively, and all other Si orientations fall between these range. This is a result of the different silicon atom densities on the different crystal faces, since Si atoms are required to form the oxide, the presence of a greater number of bondable Si atoms on the <111> face cause the oxide to grow faster, as also demonstrated experimentally. [37]

Of course, other dielectrics can also be used, especially with regard to optimization and scaling of the devices. However, if the energy barrier between the gate and the semiconductor becomes to small, the quantum-mechanical tunneling effect comes into play. Utilizing dielectric materials with a greater dielectric permittivity is one way to counteract this impact. Numerous alternatives for SiO_2 with a "high-k" have been proposed, including TiO_2, ZrO_2, HfO_2, Y_2O_3, Al_2O_3, Ta_2O_5, and La_2O_3, as well as their respective silicates. Many of the original materials used were motivated by memory capacitor uses and have been adopted primarily owing to their maturity in memory capacitor applications. Nevertheless most of these materials are not thermodynamically stable in direct contact with Si (this is not a necessity for memory capacitors, as the dielectric is in contact with the electrodes, which are normally nitrided poly-Si or metal). Also, as band gap tends to change inversely with dielectric constant, one or both of their band offsets are too low, making them unsuitable for transistor use.

Nonetheless, various factors must be taken into account while appraising these materials. Aside from dielectric permittivity, the barrier height for electrons and holes on silicon, i.e. these values are equivalent to the band edge offsets with respect to silicon. Further relevant aspects are the quality of the interfaces to prevent scattering, which reduces the

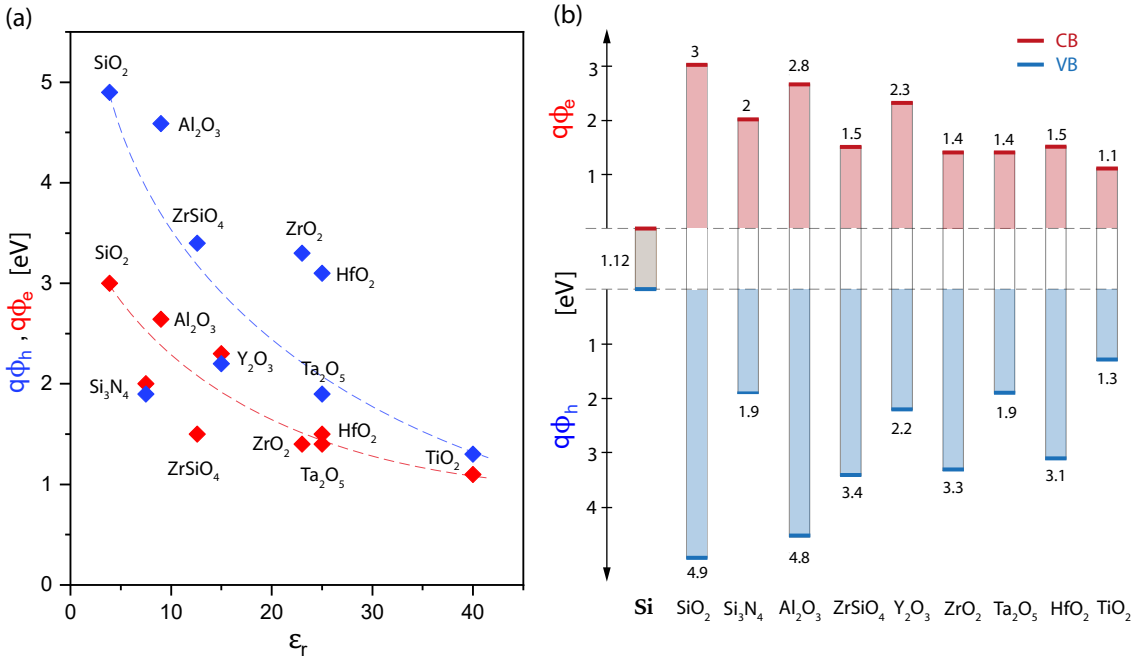


Figure 2.3: *(a) Shows the relationship of the permittivity to the height of the electron barriers (red) and to the height of the hole barriers (blue) for various dielectric materials. (b) Illustrates the conduction and valence band edges of different dielectric materials in relation to silicon with bandgap energy E_g=1.12 eV.*

carrier mobility in the channel, the trap concentration that leads to trap-assisted tunneling, the thermodynamic stability of the dielectric material on silicon, i.e. the material must withstand all subsequent processing steps, to name some crucial ones.

Table 2.1 is a listing of probable dielectric materials and their corresponding attributes that might replace silicon dioxide. Despite the fact that TiO_2 has a high permittivity of 80-120, depending on the technique of deposition, as mentioned before it has been demonstrated that it is thermodynamically unstable with Si [28]. Al_2O_3, one of the group III candidate dielectrics, is durable and stable with Si, has a bigger bandgap (8.7 eV), but a relatively low dielectric constant (9) that offers it as a short-term answer for industry demands. Several integration difficulties, including a high density of fixed charges have also been documented [6]. HfO_2 and ZrO_2 have high dielectric constants (20-25), strong stability on Si, substantial band offsets to operate as an electron and hole barrier, see figure 2.3, and can resist high annealing temperatures up to 1173 K. However, ZrO_2 interacts with Si substrate [27], leaving HfO_2 as the sole viable alternative to SiO_2. HfO_2 has numerous beneficial properties, including a high dielectric constant ($\approx$ 25), a high heat of formation ($\approx$ 271 kcal/mol), and band offsets of 1.5 eV and 3.4 eV, respectively, for electrons and holes. The fact that it is compatible with poly-Si and CMOS processing adds to its applicability.

The only factors that affect the tunneling current are permittivity, trap concentration, and barrier heights. When examining the barrier height and permittivity of various dielectrics in table 2.1, one notes a considerable trade-off between the barrier height and the dielectric permittivity. Dielectrics with a high energy barrier have a low permittivity, and vice versa, valid for electron (red) and hole (blue) barriers, as shown on the left of figure 2.3. It is obvious how the bandgap offsets for both cases, electrones and holes, become smaller as ϵ_r increases, as can be seen by the fitted curve. In the right part of figure 2.3, one can see the energetic conditions of the bands to each other. The height of the rectangles corresponds to the bandgaps of the individual materials, the areas given in transparent colors (red and blue) indicate the bandgap offsets for various dielectric materials with respect to silicon, the corresponding values are given. The dark blue and dark red lines represent the valence and conduction band edges respectively. Therefore, optimization is required to identify the optimal material.

2.1.4 SOI

The "Silicon on Insulator" term (SOI) is a designation for a chip-wafer technology with a special insulation layer embedded in the silicon substrate. The silicon oxide layer located between the bulk silicon substrate and the thin active top silicon layer, thus electrically isolating the devices from the underlying silicon substrate, is called buried oxide (BOX - typically 100 nm or more), usually of silicon dioxide SiO_2, illustrated in figure 2.4. By construction alone, SOI based transistors have a number of advantages over their typical bulk-Si counterparts, including diminished short channel effects, negligible drain to substrate capacitance, etc.

Unlike other semiconductor materials, silicon remains stable at high temperatures, so a perfectly designed passivation and insulation material such as silicon oxide can be grown on it. Based on this metal oxide semiconductor (MOS) transistors as classical silicon devices are fabricated on the surface of silicon wafers several hundred micrometers thick. However, they only cover the top micrometer on the surface of the silicon wafer, with the rest of the wafer serving as a mechanical support for the devices and this leading to some parasitic and unwanted interactions with the device.

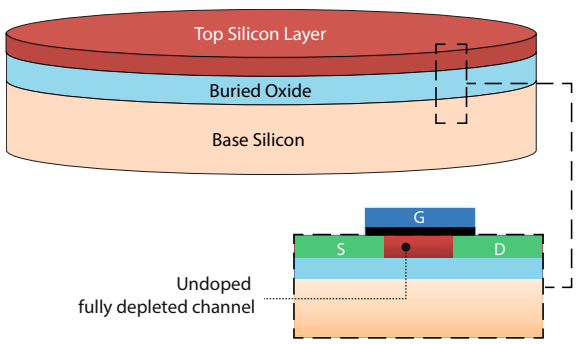


Figure 2.4: *SOI wafer with thin crystalline device layer on top and device structure out of this*

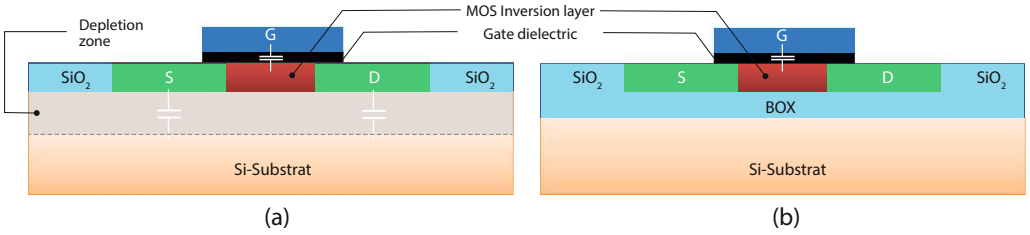


Figure 2.5: *Shows a simplified schematic diagram of the capacitances in (a) bulk-Si and (b) SOI - MOSFET. In SOI devices, the capacitance between the drain (source) and the substrate is negligibly small due to the dielectric constant of SiO_2, which is lower than that of Si, and the thickness of the BOX. This helps improve the switching speed of CMOS devices.*

As shown in figure 2.5, there are, along with the gate capacitance, parasitic capacitances such as, junction capacitance between the source or drain and the substrate. This junction capacitances in a MOSFET is mainly due to the depletion charge region between source/drain and the substrate. Therefore, in contrast to conventional transistors, which are manufactured directly on the bulk silicon wafer, the transistors on SOI are on a thinner silicon layer that is insulated from the bulk, resulting in significantly lower capacitance, so that the charges required until switching are reduced. The reduced switching times in this way enable higher clock rates and hence faster circuit operating speed as well as reduced coupling or interference through the substrate, which reduce overall noise[11, 31]. At the same time, this reduces power consumption, especially with regard to leakage currents due to non-existence of a leakage path to the substrate as the bulk is separated from the device by the oxide layer, which also results in smaller heat losses and makes it possible to operate with weaker and thus quieter cooling [66] [9].

SOI based devices are divided in two varieties, the partially depleted SOI (PDSOI) and fully depleted SOI (FDSOI) ones. In PDSOI devices, the top silicon layer thickness over the BOX forming the channel is too thick to produce a depletion charge fully controlled by the gate, meaning that the depletion region does not reach through the entire silicon channel to the body region, so a portion of body is undepleted and a quasi neutral zone is present beneath the formed channel, which may cause some charge accumulation. Since the body is not connected to any potential (floating body), the accumulated charge alters the threshold voltage of the devices and result in some undesirable effects, referred to as floating body effect or kink effect[33]. The key attribute of an FDSOI device is that the depletion region in the top layer is fully depleted and reaches all the way down to the BOX. Therefore, there is no quasi neutral body and thus free of the floating body effect. The resulting benefits include decreased leakage and improved electrostatic control and because of the extremely small dimensions, the channel does not need to be doped.

The untreated SOI wafer used within this work, which is industrial standard, consists of a 775 μm silicon substrate, a 100 nm thick BOX of SiO_2 and a 20 nm device layer with unstrained <100> oriented silicon.

2.2 Metal-Semiconductor Heterostructures

Heterostructures in general are frequently used as a fundamental component in high-tech semiconductor devices because of their valuable and alluring structural, interfacial, and electrical characteristics. A subtype of these are the metal-semiconductor (MS) heterostructures, in our case, it is specifically a metal to semiconductor transition between aluminum and silicon. This interface is of central importance in determining the performance of semiconductor devices since electrical contacts to semiconductors necessitate MS interfaces and, depending upon the barrier height, such interfaces will either show a moderate resistance to current flow in both directions, i.e. low barrier - classified as ohmic contact or a low resistance to current flow in one direction and a high resistance to current flow in the other direction, i.e. high barrier - classified as rectifying contact. Almost all electrical devices have MS interfaces, either as ohmic or rectifying contacts, which is why, contrary to what one might assume, it is one of the most crucial parts of micro- and nanoelectronics. It is generally known that the performance of most modern Si electronic devices is limited by contact resistances and it is far from easy to produce such excellent contacts.

Since the discovery of MS contacts rectifying nature, a lot of theoretical research has been into interpreting the electrical measurements in these systems, such as the I-V and C-V characteristics, and forecasting the values of the parameters that enter the models developed in this context. The most important of these parameters is the Schottky barrier height (SBH), which quantifies the difference between the Fermi energy of the metal and the band edge of the semiconductors carrier at the junction and therefore defines the transport characteristics of these interfaces. The models to describe this junction behaviour typically offer an accurate description of experimental data and the most sophisticated of these produce comparable predictions for the systems to which they are applicable. Despite this, the fundamental relevance of the SBH, the mechanisms that drive the formation of the Schottky barrier are still not fully understood and are still up for discussion [13].

The following sections goes through the physics required to understand electrical transport in Schottky barrier based transistors, especially with regard to the used material system within the scope of this work. Therefore, the aluminum-silicon compound are first introduced, and the diffusion mechanisms are discussed, followed by the formation of Schottky contacts, including the transport mechanisms and finally consider the deviations arising from real contacts.

2.2.1 Aluminum-Silicon System

Aluminum - silicon alloys (Al-Si) are widely used in practical applications and play an important role in semiconductor technology. In order to better understand this system and the processes involved, the Al-Si binary system is described briefly below. The system forms a eutectic at 577 °C and approximately 12.6 % silicon content, as seen in figure 2.6. Based on the system, alloys with less than 11 % silicon content are referred to as hypoeutectic, with 11-14 % as near-eutectic or eutectic, and alloys with more than 14 %

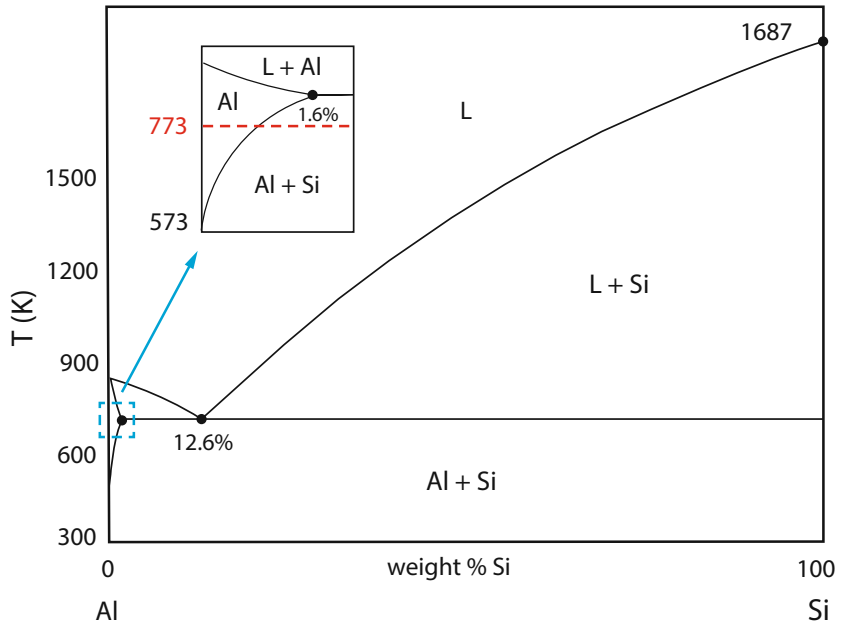


Figure 2.6: *The aluminum-silicon alloy phase diagram, inset shows the highlighted part in a zoomed-in view, including the temperature (red) that is important for the processes discussed later; based on [47]*

silicon content as hypereutectic[14]. In addition to the eutectic, the system forms two other phases, the Al-mixed crystal and primary silicon. The maximum solubility of the silicon in the Al-mixed crystal, assuming solidification at equilibrium, is 1.65 % at the eutectic temperature and drops significantly toward lower temperatures. At 300 °C, for example, it is only about 0.07 % [71][22]. Faster solidification can, however, can lead to a deviation of the maximum dissolved silicon content in the solid solution.

Our devices are based on Schottky junctions, in particular on the Al-Si heterostructure considered here. These junctions are crucial for the proper function of the transistors fabricated in this work. Therefore, it is essential to produce well defined contacts, which are ideally atomically sharp, free of interfacial traps, and have low contact resistances. To fabricate such monolithic heterostructures between elemental metal and Si is not a trivial affair. Even the smallest deviations from an atomically sharp transition can lead to undesired doping, which in this case is by no means intentional. This transitions formed are based on a thermally induced exchange reaction between the two reactants, a more detailed description follows in section 3.1. The system is brought to a specific temperature for a certain period of time where the exchange processes take place and lead to monolithic contact formation by the so-called rapid thermal annealing (RTA).

The underlying theory of this diffusion is based on Fick's laws, according to which atomic diffusion is mainly determined by temperature and the material concentration. For ho-

mogeneous and isotropic crystals, a concentration gradient leads to a particle flux J, described by Fick's first law 2.4. The diffusion coefficient D 2.5 is given by the temperature-independent diffusion constant D_0 and an exponential term with the activation energy E_A, the absolute temperature T and the universal gas constant R, $\frac{\partial c}{\partial x}$ describes the gradient of the concentration c in the direction x.

$$J = \frac{1}{A}\frac{\partial n}{\partial t} = -D\frac{\partial c}{\partial x}, \tag{2.4}$$

$$D = D_0 \exp\left(-\frac{Q}{RT}\right) \tag{2.5}$$

Together with the continuity equation -Ficks second law 2.6- the diffusion equation for constant D can be written as

$$\frac{\partial c}{\partial t} = \frac{\partial J}{\partial x} \tag{2.6}$$

$$\frac{\partial c}{\partial t} = D\frac{\partial^2 c}{\partial x^2}, \tag{2.7}$$

This differential equation of second order in location and of first order in time can therefore be solved by two boundary conditions for the spatial variable and one initial condition for the time. The values calculated in this way for the four possible diffusion processes are summarized in table 2.2.

Materials	Al in Al	Al in Si	Si in Al	Si in Si
cm^2s^{-1}	6.3×10^{-10}	2.0×10^{-20}	4.4×10^{-8}	6.5×10^{-19}

Table 2.2: *Diffusion coefficients of the Al-Si material system for T = 500 °C [18]*

As can be seen, the diffusion of Si into Al as well as the Al self-diffusion (i.e. Al into Al) is more than 10 orders of magnitude higher compared to the diffusion of Al into Si as well as the Si self-diffusion (i.e. Si into Si). Thus, Al atoms are fed through the already formed Al segment and settle in the junction region to the Si segment in the places of the out-diffusing Si atoms. Thus, we obtain well-definable Si segments that are highly variable in length, atomically sharp, and free of intermetallic phases, i.e., single-element metal-semiconductor heterostructures.

2.2.2 Metal-Semiconductor Interfaces

In the past several decades, metal semiconductor connections have been the subject of extensive research. Braun demonstrated the first Schottky contact in 1874 for metal sulfides [3]. It was not until 1938 that Walter Schottky [60] and N. F. Mott [45] developed a theoretical model to describe the rectification behavior of metal semiconductor contacts. The nature of metal semiconductor connections can also be ohmic (non-rectifying). In semiconductor devices and integrated circuits, ohmic contacts are widely utilized. References include extensive studies on the history, evolution, and theory of metal semiconductor connections can be found in [26] [57].

The Schottky-Mott Rule [46] is based on the superposition principle of electrostatic potential, which states that the charge distribution at an MS contact is identical to the superposition of the charge distributions of two isolated surfaces, since electrostatic potential energy arises only from charge distribution. This implies that the Schottky-Mott rule characterizes a non-interacting MS interface, formed without charge or atomic relaxation, indicating that dipole contributions on the surface to ϕ_m and ϕ_m remain unaffected during contact formation. It also involves an abruptly terminated interface that does not contain any localized states and that there is no intermediate layer between the metal and the semiconductor, e.g. in the form of a native oxide.

According to that, when the two materials come into direct contact, and if the work function in the semiconductor ϕ_s (relative to the free electron energy or vacuum level E_{vac}) is less than the metal work function ϕ_m, electrons from the semiconductor conduction band - which have higher energies than those of the metal - flow into the metal until the Fermi level on both sides coincide, as a consequence of thermal equilibrium, and due to the separation of charges at the MS interface, a potential barrier emerges. In the bulk semiconductor, the electron density in the conduction band compensates the uniform charge of the ionized donors, instead, as one approaches the metal. As electrons flow from the semiconductor into the metal, the electron density in the conduction band close to the interface diminishes exponentially. Since the distance between the conduction band edge E_c and the Fermi level E_F rises with decreasing electron concentration and the Fermi level E_F remains constant throughout the system in thermal equilibrium, the conduction band edge bends upwards as seen in 2.7. For an ideal contact, the height of the intrinsic n-barrier ϕ_{Bn} as well that for intrinsic p-barrier ϕ_{Bp} is given by

$$q\phi_{Bn} = q(\phi_m - \chi) \tag{2.8}$$

$$q\phi_{Bp} = E_g - q(\phi_m - \chi) \tag{2.9}$$

where ϕ_m is the work function of the metal, E_g the band gap energy and χ is the difference between the vacuum level and the conduction band edge, named electron affinity, expressed

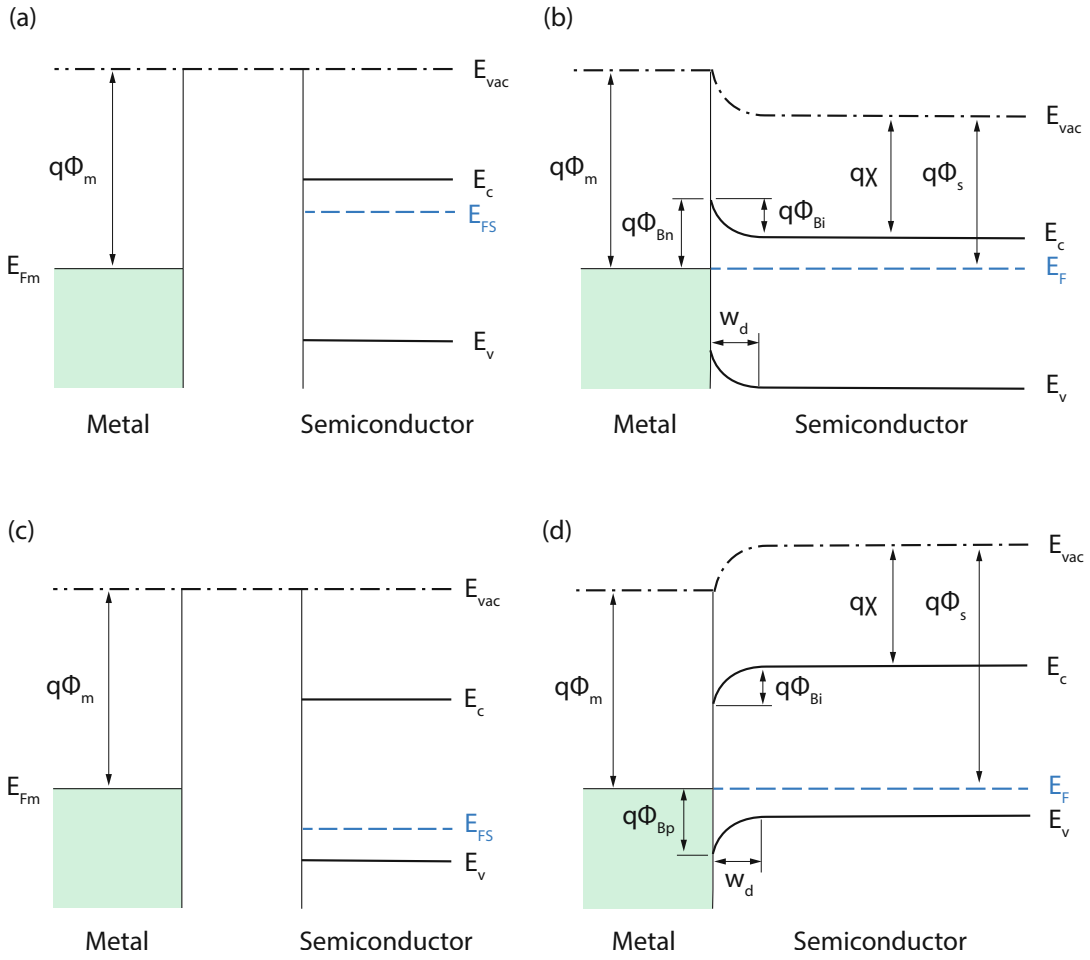


Figure 2.7: *Energy diagram of metal/n-type semiconductor with $\phi_m > \phi_s$ (a) before contact and (b) after contact; and energy diagram of metal/p-type semiconductor with $\phi_m < \phi_s$ (c) before contact and (d) after contact*

as follows

$$q\phi_m = E_{\text{Vac}} - E_{Fm} \tag{2.10}$$

$$q\chi = E_{\text{Vac}} - E_C \tag{2.11}$$

The electrons from the conduction band that cross into the metal leave behind a positive charge of ionized donors, depleting the semiconductor area close to the metal of mobile electrons. Thus, a positive charge is created on the semiconductor side of the interface, and the electrons that cross into the metal form a thin sheet of negative charge inside a very short distance.

Given that the Fermi level is in the conduction band and there are several carriers very close to he interface, the charge in the metal can be represented as a delta function. In the semiconductor, however, the Fermi level lies in the energy gap, and there are fewer carriers available to balance the surface charge on the metal. The intrinsic band bending ϕ_{Bi} of a semiconductor is then just equal to the difference between the two vacuum levels, which corresponds to the difference between the two work functions

$$q\phi_{Bi} = q(\phi_m - \phi_s) \tag{2.12}$$

The region of band bending where the charge differs from that of the bulk is named then as the depletion or space-charge zone w_d and consequently an electric field is produced between the semiconductor and the metal, see figure 2.7. This band bending inside the depletion zone, which behaves as a potential barrier for electrons, is approximately parabolic and is defined by the semiconductor donor distribution, as can determined by self consistently solving Poissons equation. This width can be calculated quite simply by determining the electric field E starting from the charge density, which is given by the charge neutrality condition and using the analysis following in the book of *Rhoderick* [57], the width is given by

$$w_d = \sqrt{\frac{2\epsilon\phi_{Bi}}{qN_d}} \tag{2.13}$$

where ϵ is the semiconductor dielectric constant, ϕ_{Bi} the above defined built in potential, q the absolute value of the electron charge and N_d the density of donors. That means, this approximations assumes that the free carrier concentrations drops rapidly from their equilibrium values in the bulk to a value that is negligibly tiny in the barrier space charge region, i.e. that the charge is constant. In reality, this transition occurs smoothly over a distance where the bands bend by around $3kT$, although the depletion approximation is precise enough for most applications. The potential and depletion widths can vary by an applied bias, and the preceding equations can be simply updated to account for this. A positive (negative) bias applied to the metal increases the number of carriers at the surface of the semiconductor, hence decreasing (increasing) the electrostatic potential and band bending. Under an applied bias V, the electrostatic potential and band bending ϕ_{Bi} are substituted in equation 2.13 by $\phi_{Bi} - V$, respectively.

For a p-type semiconductor, the bands are bent in the opposite direction and the interface area is hole-depleted. The formation of the bands is analogous as before with the same formalism, i.e. after contact, electrons flow from the metal into the semiconductor until the Fermi level is aligned. These electrons are minority carriers in the p-type semiconductor

and recombine with holes after reaching the semiconductor, forming a space charge layer of ionized acceptors cause the concentration of holes in the space charge region is negligibly small in comparison to the concentration of acceptor atoms, therfore the space charge region on the semiconductor side of the contact consists of a depletion layer whose thickness is determined by the concentration of ionized acceptor atoms. The correspondingly band diagram is shown in upper figure of 2.7 and the barrier height for holes are given in equation 2.9.

MS junctions are used particularly for their rectification characteristics in many practical applications [1]. However, most of the time, the metallic connections are only utilized to supply current to the active part of a device, so one would prefer that the connections in this situation to be ohmic. The two cases discussed so far, the n-type for $\phi_m > \phi_s$ and the p-type for $\phi_m < \phi_s$, represent the rectifying behaviour of the contacts. Exactly the opposite cases, namely for $\phi_m < \phi_s$ in the case of the n-type and for $\phi_m > \phi_s$ in the p-type case, represent the ohmic contacts. The contact is ideally ohmic, irrespective of the doping characteristics of the bulk semiconductor, when the SBH vanishes or, more accurately, is less than $q(\phi_s$ - $\chi)$. If we consider, for example, the n-type case with $\phi_m > \phi_s$ after making contact, again, just as for the Schottky contact, the conduction electrons are rearranged at the interface, i.e. in this case, however, due to the negative SBH, electrons flow from the metal into the conduction band of the semiconductor, leaving a positive charge on the metal and generating an accumulation of electrons on the semiconductor side of the interface, instead of retreating from it and so they overcompensate the charge of the ionized donors. This accumulation layer charge in the semiconductor is constrained near the surface and is effectively a surface charge. Since the concentration of electrons in the metal is so high, the positive charge on the metal side is also a surface charge confined near the MS contact. Clearly, no depletion area is formed in the semiconductor, and there is no potential barrier to the flow of electrons from the semiconductor to the metal or vice versa. Therefore, the region close to the interface has a greater concentration of electrons, whereas the bulk semiconductor region has the highest resistance in the system. Almost all of the externally supplied voltage, i.e. the potential difference drops throughout this bulk area for both current flow directions, and the absence of a potential barrier allows carriers to flow freely over the interface. Thus, it is evident that the current is dictated by the bulk region resistance and is independent of the applied bias direction.

Note that the preceding explanations of Schottky contacts are for n-doped or p-doped materials, i.e., only the majority carriers are taken into account. In intrinsic semiconductors, the Schottky barrier corresponds, for example, in the case of electrons to an ohmic contact for holes, and vice versa, when minority carriers are also taken into account. According to the description so far, the values of the Schottky barriers for electrons $q\phi_{Bn}$ and holes $q\phi_{Bp}$ both depend only on the work function of the contact metal $q\phi_m$ and are unrelated to other parameters. So, referring to the Schottky-Mott rule $q\phi_{Bn} = q(\phi_m - \chi)$, the given AlSi heterostructure with $\phi_m \approx 4.20eV$, $\chi \approx 4.05eV$ should have a barrier height of $\phi_{Bn} = 0.15eV$, but experimental measurements show that this value is in the range of $\phi_{Bn} = 0.8eV$, exactly this discrepancy need to be explained, because obviously there is

something else going on [22, 63]. Thus, in reality, other phenomena must be taken into account, such as the so called Fermi level pinning, which will be covered in more detail below. Note that the values of ϕ_m and χ in literature are often slightly different, as they depend on the atomic structure, i.e. crystal orientation, surface termination and also have a temperature dependency.

2.2.3 Fermi Level Pinning

As described before, the Schottky contact formation reaches equilibrium by migrating electrons from semiconductor to metal. These migrating electrons leave ionized donors behind and these produce a electric field and these electric field produces a potential barrier that opposes the migration of electrons. So when these two balance each other out, then equilibrium is reached. This is the ideal case of a Schottky junction formation but practical MS contacts do not appear to obey the above guidelines, in particular equations 2.8 and 2.9 shows that the barrier height ϕ_b increases linearly with the metal work function ϕ_m, but in many covalent semiconductors - like Si, Ge, GaAs - the barrier height is a less sensitive function of ϕ_m than given by the equations and in some cases it is almost independent of ϕ_m. As seen in figure 2.8, the Fermi level in traditional metal to Ge contacts is strongly pinned towards the Ge valence band edge due to the large density of interface states. Even for Si with a lower density of interface states, the perfect Schottky-Mott boundary is rarely obtained, and relatively independent of the metal involved, the pinning level is almost in the same range, resulting in a high electron and hole Schottky barrier Height (SBH) and hence, influencing the contact resistance.

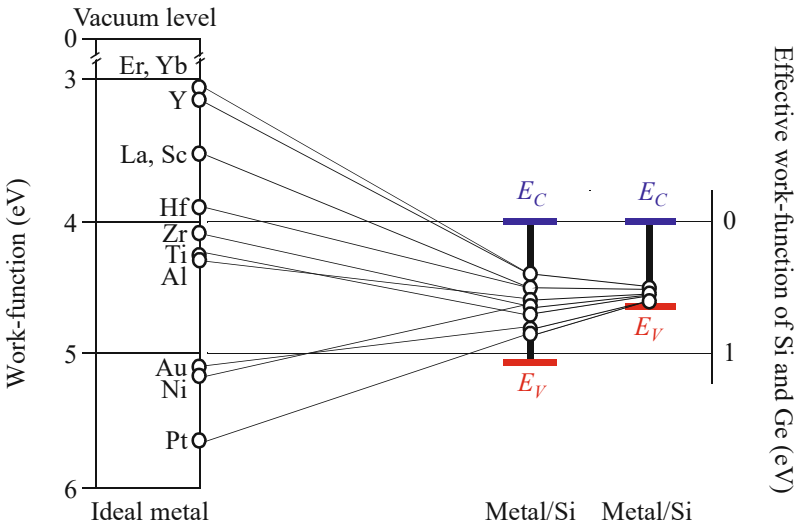


Figure 2.8: *Fermi level pinning in metal semiconductor heterostructures. Al pins at nearly one third from the valence band into the band gap of Si. [48] As comparison, in germanium, practically all materials pin at the edge of the valence band, which makes it almost impossible to build reasonable p-based transistors; adapted from [65]*

The insensitivity of the barrier height to the metal work function in covalently bonded

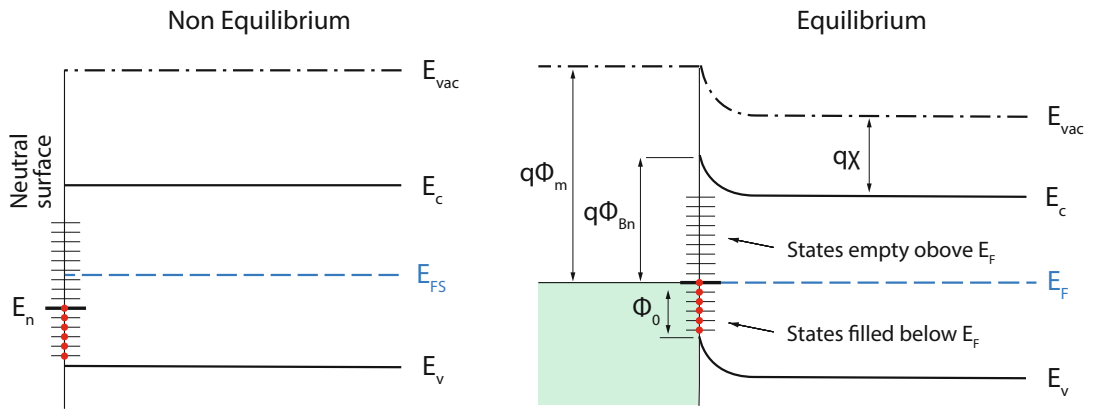


Figure 2.9: *Energy band diagram of an intrinsic semiconductor with surface states (a) semiconductor without any metal; not in equilibrium since Fermi level E_{FS} in the bulk does not coincide with the neutrality level E_n of the surface, (b) semiconductor in contact with a metal; positive charge at conduction band near the interface is balanced by a negative charge on the surface until equilibrium is reached $E_{FS} = E_n$.*

semiconductors was first explained by Bardeen [2], who pointed out the importance of localized surface states in determining the barrier height. Numerous models exist to explain this behaviour, however, this is not intended to be an exhaustive discussion of all existing models, but rather a brief description of the general concept which are sufficient to those. These models describe the electronic charge and the density of states at the interface, based on defect surface states of *Bardeen*, metal induced gap states (MIGS) of *Heine*, or extrinsic defects created by chemical rearrangement formed near the interface by making the MS contact. Also other mechanisms of defect formation at MS interfaces have been proposed, good explanations can be found in [15, 23, 42, 43]. So, taking into account a substantial density of these states, as shown in figure 2.9, the description of the processes has to be modified.

In general, surface by definition is a defect, where the periodicity of the crystal structure stops and the chemical nature of the surface is that there are some atoms sitting on the surface that dont have the sufficient number of neighboring atoms that it can bond to. So the surface contains a lot of incomplete chemical bonds, called the dangling bonds. These dangling bonds and incomplete bonds produce energy levels that are located within the band gap just as the defects and impurities in bulk produce energy levels that are located within the band gap. Central to the notion of Fermi level pinning is the concept of charge neutrality level (CNL) [10, 67] with energy value E_0, which position is such that when there is no band bending in the semiconductor the states are occupied by electrons up to E_0, acting donor like because they are neutral when occupied and are positive when empty, the states above E_0 behave as acceptor like and making so the surface electrically neutral. If electrons are filled to a point above the CNL, i.e. when the Fermi level is higher than the CNL, the first few atomic planes of the surface, has a net negative charge as depicted on the left figure in 2.9. Since the Fermi level is constant throughout all sections of a semiconductor, the CNL permits a unique relationship between the band bending at the

semiconductor surface and the surface state density. The nature of these defect states are not well known in general and there are many varieties of defect states that are possible depending on the exact termination of the surface. But in general, the density of surface states is known to be proportional to roughly $N^{2/3}$ where N is the atomic density and this number for silicon is about 10^{15}cm^{-2}, which is pretty significant number. And the energy level is spread out over a range because there are many different types of defect states which will have a different energy and it is generally known to peak around one third of the band gap from the valence band in Si and other semiconductors as well that has a diamond crystal structure [39, 64].

This is not specific to just real surface but also a similar situation for any hetero interface is given, in particular the considered Al-Si interface here. At this interface from semiconductor and metal there are a lot of these surface states or interface states producing these energy levels within the band gap, physically located at the interface. However, whether these states result from surface states [45] before formation of the contact i.e. when they are isolated, or from the penetration of metal electron wave functions into the semiconductor forbidden gap and store charge in the semiconductor [16], as surface states would do, or from chemical defects [1] generated near the interface while contacting, does not play a role in understanding the pinning issue, even if the physical background is completely different. So when the MS interface is formed and equilibrium is attained, the Fermi level in the semiconductor must change by an amount equal to the contact potential due to charge exchange with the metal and this is where these interface states come into play, namely, if the density of this interface states at the semiconductor surface is very high, charge exchange occurs primarily between the metal and the interface states, leaving the space charge essentially untouched. The number of electrons emitted by the interface states are enough to reach equilibrium, that means, that irrespective of the doping density one will always reach the same equilibrium state where the Fermi level position at equilibrium should be constant throughout the system. So the Fermi level position at equilibrium is determined mainly by the interface states and not the majority carrier concentration in the semiconductor which is controlled by doping. So note, not only that the conduction band electrons of the semiconductor migrate over to the metal there are additional sources of electron interface states emitting electrons and providing these carriers to the metal side in order to reach equilibrium. Thus the Fermi level position is fixed and it almost does not matter how lightly or how heavily doped the semiconductor is, or what metal is the interface partner, the Fermi level will always get stuck at a certain energy level and that phenomenon is called the Fermi level pinning [19]. As described above, these phenomena are naturally explained in terms of local neutrality and screening by localized interface states within the bandgap of any displacement of the Fermi level at the interface. The process of this screening is made clear in the models of *Bardeen* and *Heine* where any alteration of the Fermi level caused by a change of ϕ_m charges the surface states or MIGS and creates a dipole layer that acts to again the Fermi level change. So in fact, the SBH does not vary much with the metal work function ϕ_m, but it has an influence, whereas the atomic structures of MS contacts, and the sensitivity of the electronic structure to atomic relaxations, chemical bonding, defects, etc. is the main force of determining the SBH.

As mentioned above, a barrier is created at the MS junction over which a current transport can take place because of charge transport from the semiconductor to the metal or, of course also in the reverse direction if biased accordingly. As illustrated in figure 2.10 for a forward biased Schottky barrier, there are several prominent mechanisms of carrier transport across the MS interface, namely (1) thermionic emission over the top of the potential barrier (2) quantum mechanical tunneling through the barrier (3) tunneling via interface states (4) recombination in the depletion region (5) diffusion of majority carriers in depletion region (6) minority carrier injection in the neutral region.

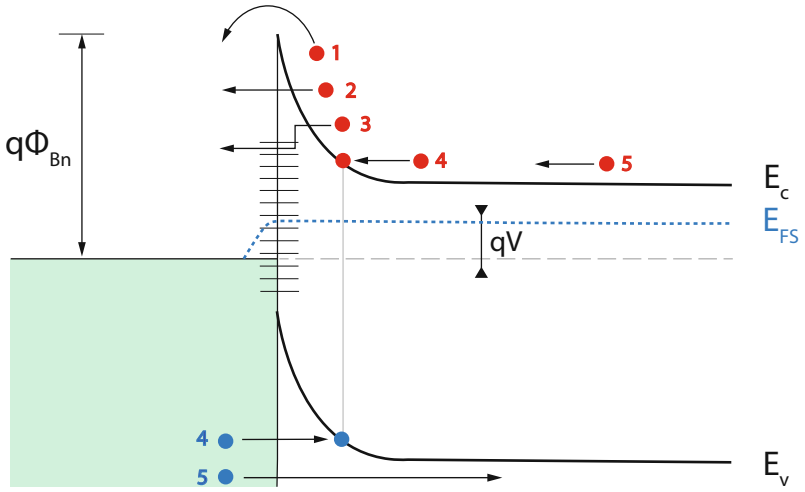


Figure 2.10: *Band diagram of a MS contact in forward bias and the associated transport mechanisms leading to the total carrier transport; (1) thermionic emission (2) tunneling through barrier (3) tunneling via interface states (4) recombination in depletion region (5) majority carrier diffusion (6) minority carrier injection. Adapted from [62]*

The major carrier transport processes among these transport mechanisms are tunneling and thermionic emission. Minority carrier injection and recombination are two less effective conduction methods that can be neglected, and are not considered in the context of this work when we analyse Schottky barrier field effect transistors. In general, the concentration of active carriers determines which process is dominant when the system is in equilibrium. At low doping concentrations, thermionic emission dominates electron transport since the depletion zone is too thick, resulting in limited or no tunneling across the interface. For strongly doped semiconductors, the thickness of the depletion region reduces, allowing carriers to more easily penetrate or tunnel through the barrier, and above a certain concentration of carriers, tunneling current begins to predominate. However, at room temperature this junctions shows rectifying behavior due to emission over the top of the barrier into the metal when electrons have enough thermal energy to overcome it and it is worth to mention that the Schottky barrier transistor is mainly a majority carrier device. This transport is either dominated by thermionic emission or by the diffusion process in the depletion region, with thermionic emission being more likely the bigger the Schottky barrier and band bending is. For the heterostructures analysed in this work, we

presume the former and consider the measurements and evaluations within the framework of the underlying thermionic emission theory. At low temperatures, tunneling is the major mechanism of transport through a Schottky barrier, either direct tunneling (field emission) at the quasi Fermi level or thermally activated tunneling (thermionic field emission), the quantities of these components are affected by temperature as well as active carrier concentration. This will be covered in more detail in the next section 2.3. In thermionic emission, the significant positive current is caused by a decrease in band bending in the semiconductor, which makes the transport of carriers from the semiconductor to the metal easier. In the case of forward bias, raising the bias causes a decrease in the band bending $q\phi_{Bi}$ and hence an increase in current and vice versa for the reverse case. Important to keep in mind that raising the magnitude of the bias does not affect the barrier $q\phi_{Bn}$ for electrons from metal to semiconductor, which results in the current getting saturated. In the tunneling domain, the transport is more complex and dependent on the intensity of the bias, respectively.

2.3 The Schottky Barrier Transistor

In contrast to a typical MOSFET, source and drain of an SBFET are made entirely of metal or metal silicide contacts that extend beneath the gate, which modulates the potential in the channel and are capable of functioning as n-type or p-type transistors. Therefore, the metal-semiconductor-metal (MSM) structure is composed of two back to back Schottky barriers, one forward biased and the other reverse biased, as illustrated in figure 2.11a. Note that, there is no gate oxide pictured, this is just for simplicity and remains throughout the thesis. If the barriers are not transparent to a current flow and there are no leakage channels in the contacts, current flow should be limited by transport across the reverse bias barrier. Remember that a reverse bias barrier represents current flow from the metal passing the barrier into the semiconductor. As previously mentioned, this barrier heights for electrons ϕ_{Bn} and holes ϕ_{Bp} are determined by the interaction at the MS junction and cannot be altered by doping concentration.

The various operating modes of the SBFET are schematically depicted in the band diagrams in figure 2.11. Subfigure (c) depicts the usual ambipolar transfer characteristic of a SBFET with $V_{DS} > 0$ and sweeping the gate voltage V_G from negative values to positive ones while subfigure (b) shows the corresponding circuit symbol for the case where the source is at zero potential and a positive voltage is applied to drain. As it is obvious from the characteristics, increasing the value of V_{DS} has no effect on the electron current, while the hole current grows exponentially for a certain point of view for the gate voltage V_G. In an electrostatically properly operating device, applying a certain V_{DS} has no effect on the barrier form or height at the source. Nevertheless, the drain voltage affects the form of the barrier on the drain side. Hence, the tunneling current through the drain side Schottky barrier increases exponentially as the tunneling probability of this barrier rises. As seen in the inset of figure 2.11, the barrier on the drain side becomes then thinner as V_{DS} gets more positive, or, to look at it another way, for positive V_{DS} values, V_{FB-D}

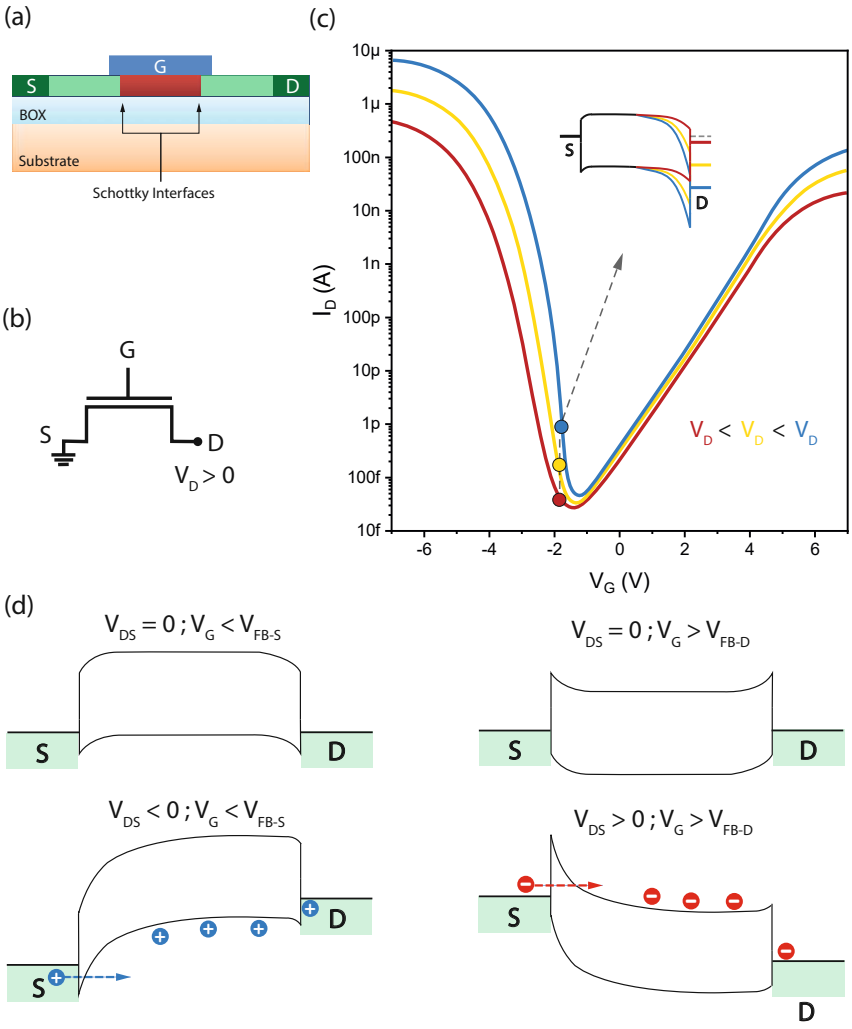


Figure 2.11: *(a) Scheme of a SBFET on SOI with marked interfaces (b) circuit symbol with source contact on ground level and variable V_D (c) typical transfer curve of the SBFET at different drain voltage levels V_D according to (b); the inset illustrates the band conditions for the marked points (different V_D) at one particular V_G (d) and (f) depicts the gated upward band bending with hole transports at $V_G < V_{FB-S}$. In (e) and (g) the corresponding gated downward band bending with electron transports at $V_G > V_{FB-D}$ is displayed.*

happens earlier, at greater negative V_G values and this implies that the current rises as V_{DS} grows.

In principle, at $V_G = 0$, the effective electron and hole barriers are large, making a tiny "off" state current achievable. The bands in the semiconducting area can be bent upwards or downwards depending on the applied gate potential V_G. In particular, the channel electron barrier height increases for $V_G < V_{FB-S}$ while the hole barrier height gets bigger for $V_G > V_{FB-D}$. With increasing absolute values of V_G the Schottky barrier at source

and drain occurs gets gradual thinner for the valence band at $V_G < V_{FB-S}$ and for the conduction band at $V_G > V_{FB-D}$. Now, if a bias voltage V_D is applied to the drain electrode, holes or electrons can inject from the source into the semiconducting channel and produce a drain current I_D with a magnitude proportional to the bias voltage with typical ambipolar behavior. The different cases can be seen in figure 2.11(d-g), (d) and (e) depicts the band conditions without biasing of source or drain, the band bending occurs by applying a gate voltage V_G alone. In (f) and (g) a positive and a negative voltage is applied to drain (relative to source potential). Applying a negative voltage, the energy level at the drain shifts to higher values, which also leads to band bending at the source and holes can tunnel through more easily (f). With positive voltage on drain, exactly the opposite happens, the energy level at the drain shifts to lower values, the band bending at the source increases and electrons can tunnel through more easily. Note that in the preceding explanations and band diagrams, the injection of charge carriers, namely the majority charge carriers, occurs always from the source side, depending on V_{DS} and V_G.

As mentioned earlier, mainly two charge carrier transport mechanisms are responsible for the injection of the carriers in the channel, which consists of thermionic emission and tunnelling through the barrier, depending on the applied gate voltage, which determines the channel potential and changes the energetic landscape. Through thermionic emission (TE), the thermalized charge carriers are able to pass over the maximal barrier point. In contrast to thermionic emission, which is a classical process, tunneling or field emission (FE) of carriers is solely quantum mechanical and can occur also in a thermal assisted way. This thermionic field emission (TFE) predominates the transport when carriers have sufficient thermal energy to tunnel through a piece of the barrier near the top, but not enough to reach the top to emit over it. Typically, this transfer happens at high temperatures and electric fields.

For a more precise understanding of which transport mechanisms act at which point, depending on the electrostatic situation, please take a look at figure 2.12, which gives a good insight in the quantitative behaviour. With positive voltage applied to the drain and sweeping the gate voltage, the corresponding bands are indicated in (b-e). The entire current I_D through the channel could be broken down into a hole and a electron branch to analyse the characteristic, but remember, there is in real no separation of those in a SBFET. In figure 2.12a, again the transfer characteristic is shown, with the total current I_D (black) and the subcurrents $I_{electron}$ (red) and I_{hole} (blue). Both currents $I_{electron}$, I_{hole} are split up into two distinct regions indicated as the thermal area and the tunneling area, which are separated by a transition point known as the flatband voltage V_{FB}, which is defined as the gate voltages at which tunneling through the barriers ϕ_{Bp} for holes and ϕ_{Bn} for electrons becomes nearly transparent. At this flatband voltage for holes V_{FB-D}, denoted with (3) in figure 2.12a, it is obvious from the related band diagram in 2.12d that the bands on the semiconductor side of the MS interface are flat at this gate voltage. Above flatband voltage ($V_G > V_{FB-D}$) and thus in the hole thermal region, the hole current is a pure thermionic emission over the valence band barrier into the channel. Applying a greater positive V_G lowers the valence band in the channel, increasing the barrier beyond

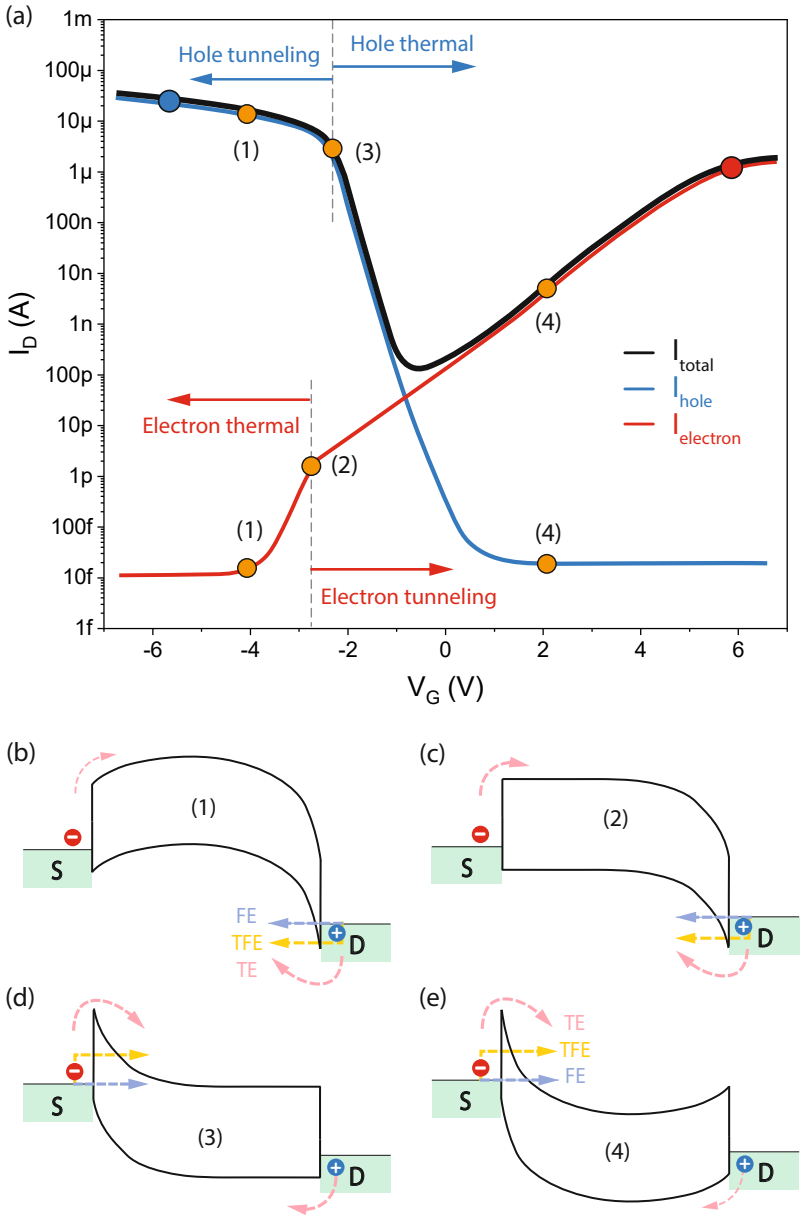


Figure 2.12: *Transfer characteristic of the SBFET with $V_D > 0$, $V_S = 0$ with virtually separated total current (black) in a hole portion (blue) and a electron portion (red) regimes and highlighted points in (a) and the associated band diagrams at this points in (b-e)*

ϕ_{Bp} and exponentially decreasing the hole current, represented in the associated band model with a thin arrow in (e). In contrast, the hole current in the hole tunnelling area ($V_G < V_{FB-D}$), denoted with (1), is a mix of thermionic emission and tunnelling processes, whereby the barrier for thermal emission of holes now is set to a fix ϕ_{Bp} and so the thermionic component no longer increases exponentially with decreasing gate voltage, illustrated in 2.12b. Contrary, the tunnelling component of the holes increases as the

tunnelling barrier becomes thinner as the gate voltage is getting more negative. At the same time, electrons also contribute to the current flow by travelling across the conduction band from source to drain to the total current. That contributions to the overall current happens exactly in the same manner as the hole current described above. Also here there is a thermal and a tunneling area for electrons in such a way that between (1) and (2) is the thermal region, whereas the region between (2) and (4) is the tunneling region, where (2) denotes the flatband voltage for electrons V_{FB-S}. The asymmetric situation described above has a minimum current point where the current is equal to the sum of a thermionic emission current via the valence band and a mixture of thermionic and tunneling current through the conduction band. Please take note that the intensity of the arrows representing TE should symbolically reflect the level of occurrence in the corresponding situation. In addition, the graphical representation of the length of the arrows or the depth of penetration into or through the barrier in the case of FE and TFE should serve as an indicator of the strength of the tunnel probability.

Especially it should be pointed out again the fact, that in the shown example in 2.12 the electron current varies exponentially with the applied drain voltage V_D whereas the hole current is independent of V_D. Also to be noted is that the fabrication of a high quality SBFET at room temperature necessitates that the thermionic current predominate the transport in the subthreshold region, while in the "on" state the Schottky barrier should be ideally transparent and direct and thermionic assisted tunneling become significant.

So the SBFET, as we have seen, have ambipolar transfer properties by its nature and therefore, in principle, offer the possibility of using the undoped semiconducting channel as either for electron and hole transport. In theory, this trait allows for complementary logic, however they are not implemented in todays integrated circuits since they have lower on-currents than ordinary MOSFET and significant gate induced drain leakage currents in the off state, resulting in a poor on to off ratio, which is critical in such circuit operation. But they are potential candidates for use in reconfigurable electronics, as we will see in the following section 2.3.1 by introducing the so called reconfigurable field effect transitor (RFET).

2.3.1 The RFET Concept

Till today, CMOS devices and interconnects have been effectively scaled down to reach faster speed, lower power, smaller size, and higher yields, resulting in todays FinFET, FD-SOI, High-k, and SiGe technologies. This concept of downsizing the physical feature sizes of digital functions, e.g. logic and memory storage, to increase density and thus reduction in cost per function and increase performance, e.g. speed and power, is reaching limits. After this "More Moore" era, new technologies and materials will be required to surmount the reached wall of physical limitations. Besides the "Beyond CMOS" approach, which is a transition from charge based to non charge based devices, i.e. based on spintronics, molecular states, photons, phonons, quantum states, and magnetic flux, there is an alternative concept to add more functionality through integration that does not neces-

sarily scale according to Moore's Law, but provides additional value due to new functional diversification at the chip and system level, which is classified as "More than Moore" [29, 59].

Considering a field programmable gate array (FPGA) with his flexible nature, which is based on multiplexing of information, one of the emerging problems becomes obvious. In general, these devices have several logic functions and memory blocks, however while the needed information is being routed at one block, the others are unable to handle data. Hence, in the end, there is a significant amount of functionality that is unused, but it still consumes power and area, resulting in increased cost and power consumption, respectively. Additionally, in a typical FPGA, the main area of the chip is covered by interconnects, meaning its all about routing information, resulting in significantly time latency, and no matter how great the individual technology is in there, these devices are very slow. So, state of the art FPGA uses only about 20% of the chip area for logic, while the rest is used really to route information within the chip. This interconnects are responsible for the delay times up to 80%, and along with it up to 60% of the power consumption, e.g. wires, connection boxes, routing switches and buffers, meaning there is also a power consumption issue from collecting information [34, 50, 61, 70].
So, this is the inspiration behind the hunt for a so called reconfigurable device and this device, what it does, it combines many functions of a transistor in one device. So for logic in CMOS, typically a n-FET and p-FET are combined making it complemantary and thus leads to power consumption. The problem is these functions are fixed because of processing, i.e. lithography and cannot be changed. So the idea is to look for an device, that can have these two functions in one, this is the reconfigurablity.

Instead of a single gate above the channel, by introducing two or more gate electrodes to the previously described SBFET, it is now possible to obtain a FET that is reconfigurable and capable of various operations. The aim is to obtain a high level of electrostatic control, which usually requires a high-k dielectric and a low dimensional geometry structure, with good gate control, allowing the transistor to conduct both electrons and holes while filtering out unwanted charge carriers by applying a local electric potential [40, 73]. In bulk structures it is almost impossible to get this level of control. Thus, in contrast to conventional complementary logic circuits, which combine separated p-type and n-type FET devices, reconfigurable FETs combine both types of FETs into a single nanostructure device reducing technological complexity. Moreover, these RFETs also provide the versatile reconfiguration of whole logic blocks, which can further reduce hardware complexity.

Hence, in the most basic architecture, a single semiconducting channel, a nanosheet (NS) in the scope of this work, that is oxidized, so there is a dielectric on top of it, is embedded in between a source electrode and an drain electrode, with split gates above the sharp interfaces as shown in figure 2.13, and this can be operated either as an n-FET or as a p-FET, referred to as dual top gate structure (DTG)[74]. So basically one gate is defined as program gate (PG) thus creating a high barrier, so the unwanted charge carriers in

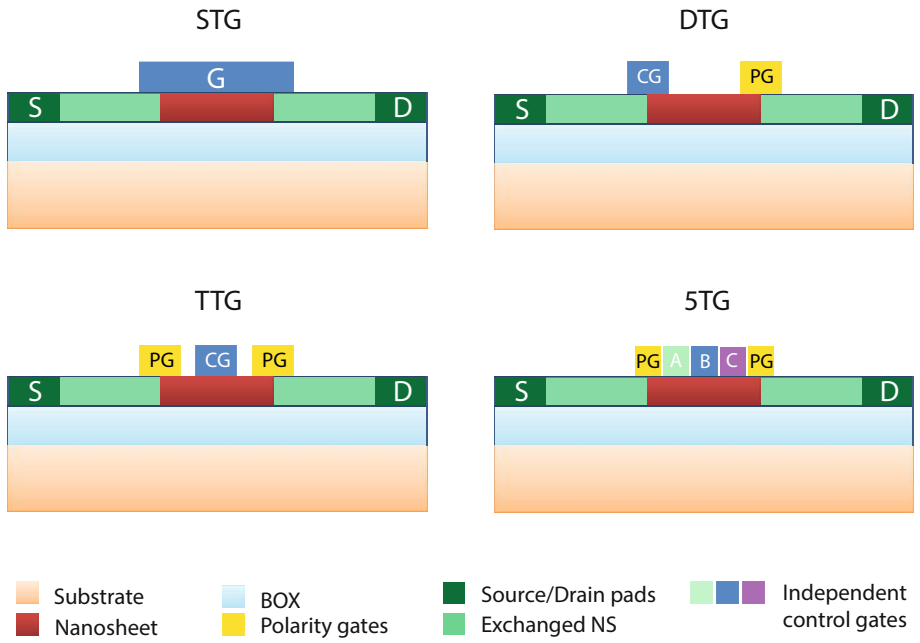


Figure 2.13: *Schematic illustration of an SBFET with ambipolar behaviour in (a) and several reconfigurable transistor concepts: (b) DTG with selective injection and modulation of charge carriers through independent PG and CG. (c) represents a TTG where polarity is selected at the MS junctions through PG, and charge concentration is controlled inside the channel with CG. (d) injection control as in TTG with additional gates above channel allowing wired logic functionality.*

the channel are blocked, while making the other barrier so thin that tunneling dominates and basically turn the device on. If all applied biases are just reversed then the n-FET becomes a p-FET and vice versa. Meaning, one get the second FET for free in the same device structure by just switching the control voltages. Figure 2.13 shows the different types of implementation options [25]. As a comparison, (a) shows the analysed SBFET with ambipolar behaviour, where the gate extends over both interfaces, thus changing the energy landscape as a whole. (b) shows the dual top gate (DTG) mentioned above, where the PG determines the type of charge carrier and the CG controls the modulation. In (c), a triple top gate (TTG) structure is shown, with three gate electrodes above the channel, where the PGs are located above the MS interfaces and the CG in the middle is responsible for the charge leveling within the channel. Optionally, these PGs can either be executed separately or connected together in order to obtain the same potential for both interfaces. Subfigure (d) shows a 5TG, in which the CG is virtually split into three independent gates, whereby so called logic wired-AND can be realised. In principle, there are no limits to the number of gates except for lithography based realisability.

In the remainder of this work, we will focus mainly on TTG structures, as these have special properties, especially with regard to the realisation of logic gates, and have accordingly been investigated the most. Figure 2.14a schematically shows a TTG structure in which the PGs are merged together and thus have one and the same potential. Figure 2.14b

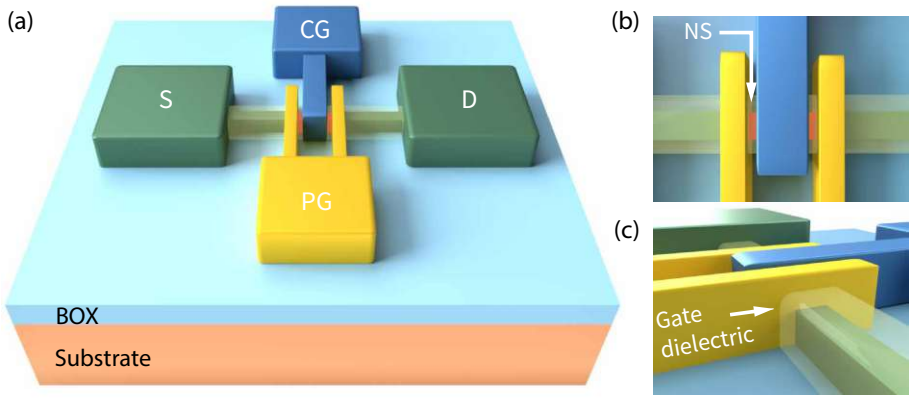


Figure 2.14: *(a) Schematic of a TTG-RFET showing all essential elements, (b) top view at the channel area with the nanosheet (NS) in red and the polarity gates (PG) directly above the MS junctions and (c) indicating the omega shaped gate surrounding of the dielectric covered NS*

shows that the PGs are each aligned atop the interface formed by the Si-NS and the c-Al, while figure 2.14c shows on the one hand the necessary dielectric, in our case SiO_2, and on the other hand the omega shape of the gate surrounding the dielectric-covered NS for the best possible electrostatic control.

The basic transport phenomena of these RFETs are in principle identical to the SBFET case. The only difference is that the additional gates more efficiently suppress the undesired type of charge carriers, as already briefly explained for the DTG configuration. However, the injection methods of TE, TFE and FE remain the same, as will be explained below for the TTG.

The merged program gates (PG) cover both drain and source junctions, while the control gate (CG) is positioned between these to cover the mid-channel part and modulate the conduction. The local voltage on PG, denoted as V_{PG} in the following, controls the two SB in such a way that depending on the polarity and the value the tunneling probability changes. When both V_{PG} and V_G are negatively biased, the conduction and valance bands bend upward, resulting in a thinning of the SB, through which holes can tunnel, as shown in figure 2.15a. The drain voltage is set to a positive potential $V_D > 0$, shifting the energy levels on the drain to lower values, which also influences the thinning of the SB on the drain side, as discussed in section 2.3. This injection into the valance band occurs via a combination of thermal emission and tunneling, and the device operates as a p-type transistor in the on-state. The higher the absolute value of V_{PG}, the thinner the SB becomes and the more tunneling gains the upper hand. At the same time the injection of electrons is suppressed at the source by the increased SB beyond ϕ_{Bn}. The device is turned off if V_{CG} changes its orientation, that is, if it becomes increasingly positively biased while V_{PG} remains negatively biased, the barrier inside the channel bends downwards and builds a wall against the hole flow, as depicted in figure 2.15b. In the same way, n-type behaviour

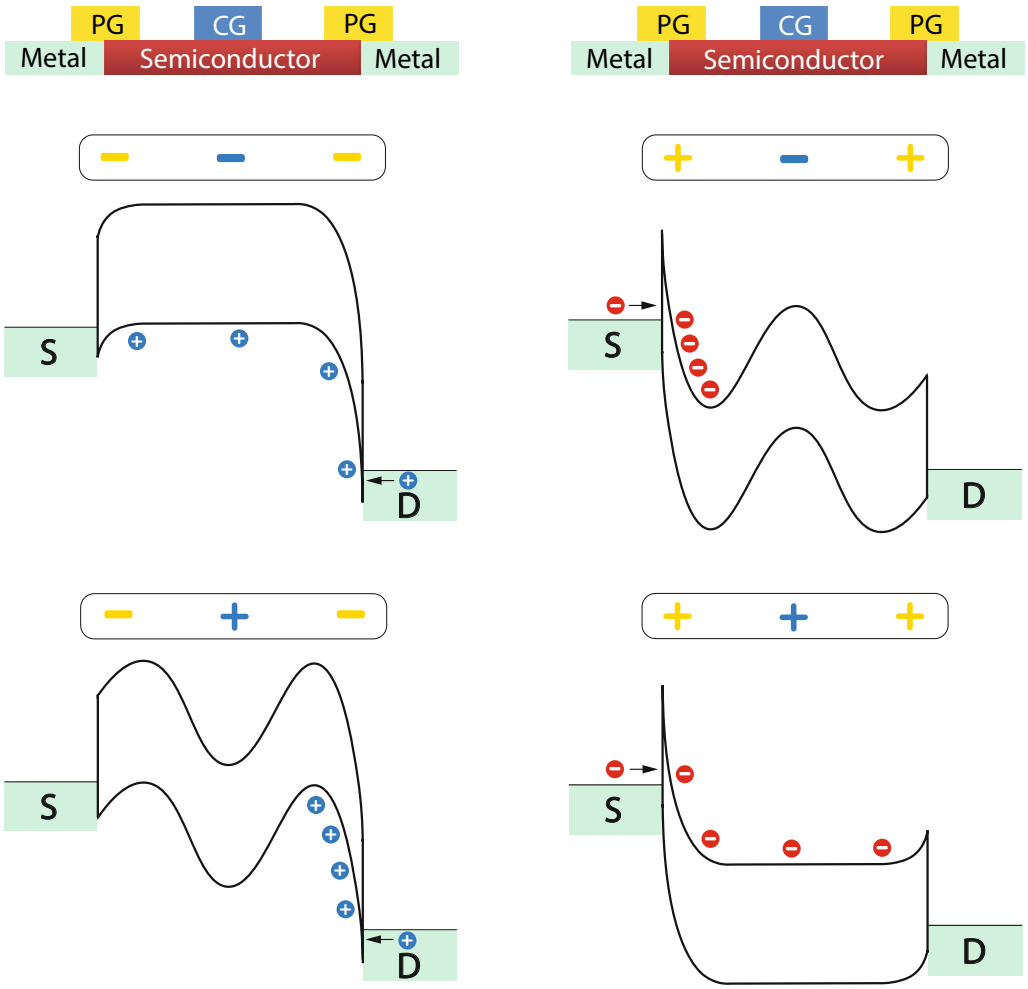


Figure 2.15: *(a) Schematic band diagrams for different configurations of a TTG with simultaneous SB gating and positive bias on drain. The carrier injection are indicated for holes and electrons; (a) shows the bands in the on-state for p-type mode and (b) depicts the off-state for p-type mode, (c) shows the off-state for n-type mode and (d) depicts the bands for n-type mode in the on-state.*

can be achieved in the same device by reversing the voltage levels for V_{PG} and V_{CG}. This means that the device operates as an n-type transistor in the on state when both V_{PG} and V_{CG} are positively biased, bending the bands of the whole channel downwards, so that electron flow can happen from one contact to the other, see figure 2.15d. Changing the polarity of V_{CG} to negativ, bends the band in the middle of the channel upwards, so injected electrons can not pass through the entire channel and an accumulation takes place, the device is in the off-state, as shown in 2.15c.

The transfer characteristics of the TTG are shown in figure 2.16. For comparison, the DTG, which was briefly mentioned, is also shown in dashed lines. The corresponding band diagrams at selected points are shown for each of the p-mode and n-mode, depending on CG and in addition the circuitry, i.e. the voltage levels at the contacts, are also shown

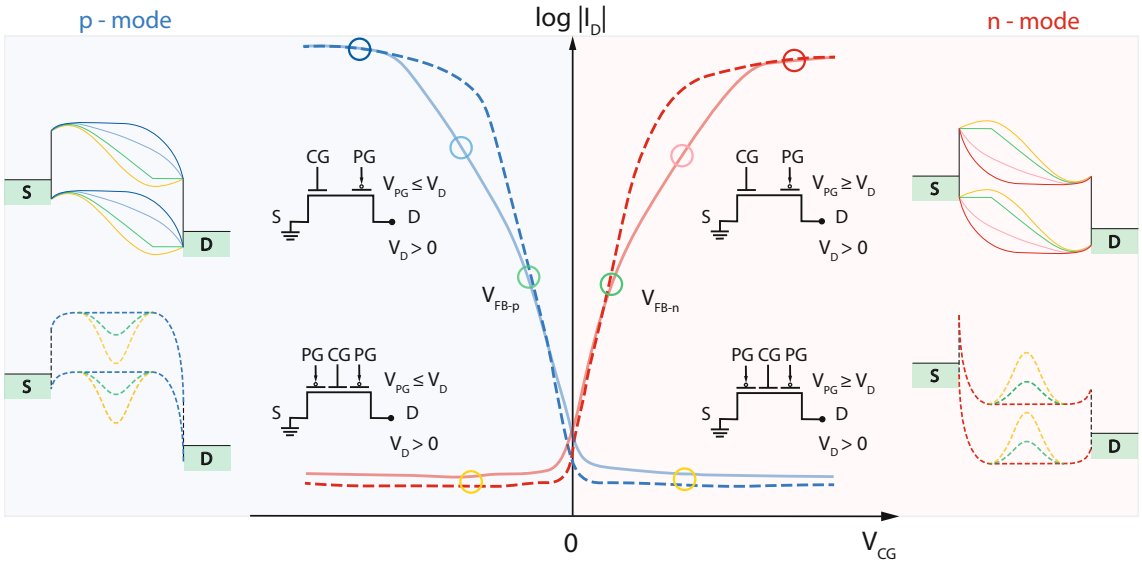


Figure 2.16: *Transfer characteristic of a DTG and TTG structure, the insets depicts the circuits symbols with the voltages applied and the band bendings at selected points to the left for p-type operation and to the right for n-type operation.*

as insets. With PG and drain and source at the given potentials, the RFETs show n-mode characteristics when CG is positive biased and p-mode characteristics when CG is negative biased. It can be seen that the difference lies in the steepness of the subthreshold regime, which is significantly steeper for TTG, which is unavoidable for circuit realizations and power consumption. This is due to the fact that the CG in the TTG structure only regulates a potential barrier for previously injected carriers in the channel, which is controlled by PG enabling injection across both barriers, while the CG in the DTG structure must also handle the injection at the source side in addition to the modulation. Precisely for this reason, namely when V_{CG} gets gradually smaller in absolute values and the band bending decreases until flat band conditions are reached, i.e. where the transition from tunnelling and thermionic emission to thermionic emission takes place, a kink can be seen where the slope changes, this behaviour is not observable in the TTG, since the injection is not affected by CG. Hence, to deliver a message, two gates are better then one, but three gates are better than two, meaning that the more gates one includes, the more functions complexity is possible to get.

Furthermore, there is a rule associated, which states that for creating circuits, the on currents of the n-mode must be as high as the ones for p-mode. This is known as current symmetry, and in typical MOSFETs where p and n are always fixed this is done by adjusting the width of the transistors. But in this case, obviously, this is an unwanted issue, since the same device should be capable for both operations. A very high fraction of the on-current is controlled only by tunneling, tunneling through the thin barrier controlled by the gates and for logic applications the threshold voltage region is decisive. To increase the electron currents versus the hole currents, then tunneling has to be more interest-

ing for electrons than for tunneling into the valence balance for holes. Considering the the Wentzel-Kramers-Brillouin (WKB) approximation in equation 2.14, note that there is a parabolic barrier in fact, nonetheless, for simplicity, this approximation assumes a triangular barrier but this does not really change too much the terms.

$$\Gamma \approx \exp\left(-\frac{4}{3} \cdot \frac{x_{Si} \cdot \sqrt{2m^*_{n,p}} \cdot \Phi^{3/2}_{Bn,p}}{q\hbar V}\right) \tag{2.14}$$

This tunneling depends on the barrier height, it depends on the bias V or applied field E, basically the width of the barrier divided by voltage and it depends on the effective mass of the charge carrier. Essential to note, in contrast to traditional MOSFETs, the limiting element of transport in these devices is not carrier mobility within the channel, but rather the injection rate through these barriers. In reference [73], mechanical stress is used to alter the silicon band structure, hence adjusting the effective tunneling mass of electrons m^*_n and holes m^*_p, to optimize the hole injection to electron injection ratio.

2.3.2 Logic Gates based on RFETs

Electrical components that can efficiently process information are essential for the creation of the majority of modern electronics and computational tools. In this sense, reconfigurable electronics with its flexibility are a potential candidate to optimize the use of existing hardware resources and improving processing efficiency. The most of todays reconfigurable circuits, such as the FPGA, are based on conventional Si circuits and make use of p-type or n-type FETs that have predetermined electrical properties. Hence, shifting the polarity of the bias does not result in the addition of any additional switching functions. So, in order to develop complex circuit architectures and finally actualize reconfigurable computing capabilities at the circuit level, these reconfigurable circuits need a lot of transistor resources. The RFETs presented offer the ability to provide many circuits within the same wafer area and is one of its many advantages. In general, there have been reports of RFETs being used in a variety of applications, including a variety of sensors and circuits. The application of the RFET as a light sensor is investigated in the reference [51] or as a biosensor in here [81]. Moreover, the performance of RFETs in logic circuits is discussed in many studies [24, 68, 76] and it has also been stated that RFET devices can be used in many circuitry applications [75]. Nevertheless, much past research on logic circuits has been on simulations rather than experimental proofing the functions, since integration necessitates good symmetry in both operating modes. The RFETs used in this work with its unique and reliable fabrication techniques, especially with regard to the materials used, allow device integration using current CMOS technology in a top-down fashion and can be utilized to gain more functionality per unit of area by using its intrinsic or extrinsic reconfigurability properties also on the system level, enabling to build more compact logic cells than in CMOS.

In general, for the transfer of the switching function via many gates, the input and output functions must be created in the same voltage range, to be able to build further cascading circuits. So, equal rise and fall times are prerequisite to create a inverter, 2-input NAND, NOR, XOR, and XNOR logic gates as have been considered within this thesis. As previously indicated, this requires compensating for the difference in electron and hole mobilities in Si to achieve an ideal switching point, for which the symmetry of the electrical characteristic is mandatory and note, that also a hysteresis free characteristics are a precondition to be independent from the initial state. Otherwise the absence of symmetry would shift the switching point in the case of an inverter away from $V_{DD}/2$, which makes a functional logic impossible.

See figure 2.17 for an inverter with one input and one output, with the output being the complement of the input. The inverter is built up by a series connection of a p-type transistor with an n-type transistor acting as pull-up (PUN) and pull-down (PDN) networks that make up a CMOS gate. The purpose of the PUN is to establish a link between the output and V_{DD} whenever the output of the logic gate is intended to take the value 1 in any given situation. In a similar way, the purpose of the PDN is to link the output of the logic gate to the GND when it is intended for the output of the logic gate to be 0. The PUN and PDN networks are built in a fashion such that, only one of these networks is conducting during steady state.

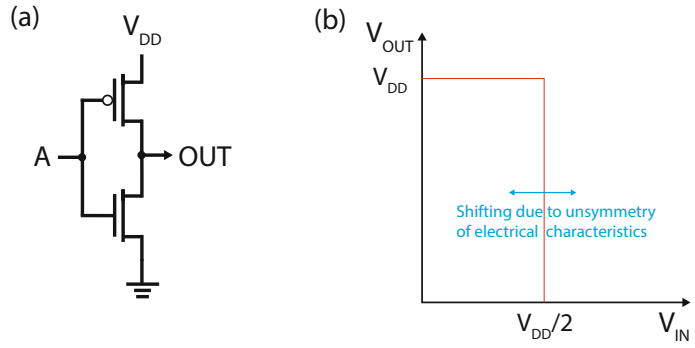


Figure 2.17: *(a) CMOS inverter with two transistors in series inverting the input A at output, (b) Transfer characteristic with ideally switching point and shape*

In classical CMOS, this inverter is fixed, but with RFETs, this inverter can be changed in configuration in a such way so that the upper transistor becomes an n-FET and the lower one becomes a p-FET by changing the voltages and the properties of the complementary inverter function are preserved, i.e., it has the same characteristics, indicating that regardless of the circuit configuration, the equivalent behavior is given and reconfigurability at the circuit level is possible. Several RFETs have been fabricated and evaluated as logic inverters in [25, 76, 82] to establish their proof of concept. Note, both circuits are logic inverters, although they use switched transistors.

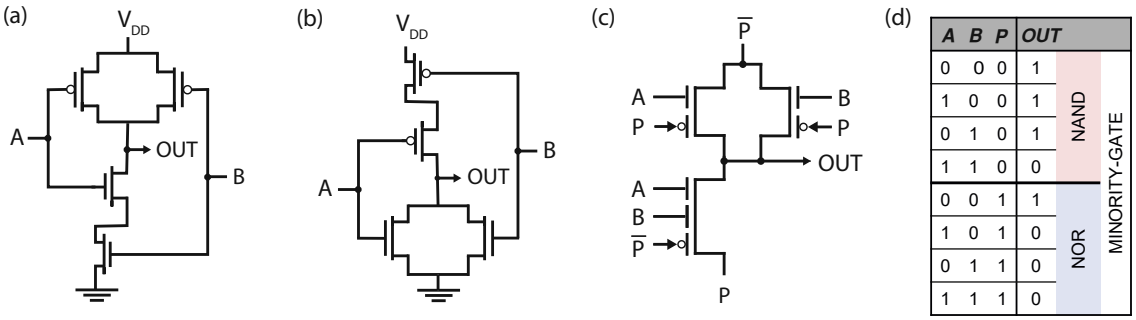


Figure 2.18: *CMOS realization of (a) NAND gate, (b) NOR gate, (c) RFET realization of complementary NAND/NOR (MIN) depending on P , (d) truth table of NAND/NOR (MIN) gate.*

In addition to the individual characteristics of the transistor and their functionality i.e. that one device can perform as a p-type or n-type FET, of course under the premise of symmetry, which is a necesssary condition for creating circuits there are even more symmetries in a system. So if there are symmetries in circuits that basically look kind of the same and just by changing P to N, one can gain really a lot of benefit. So its relevant to identify symmetries and the easiest symmetry is the NAND function and this is a really powerful gate in logic world, as all logic functions can be written either with NANDs or with NORs by interconnecting them. Hence, in the circuits depicted in figure 2.18a and 2.18b, its obvious that the way the transistors, the p-FETs and n-FETs are connected to each other, the two n-FETs in series and p-FETs parallel in (a), the circuits looks actually identical to each other, meaning that the connecting paths are the same. The only things that are different is that the voltage V_{DD} is inverted, so just flipping the cell in (a) and redefining all p-FETs as n-FETs and the other way around leading to (b), so with RFETs this can be done. Meaning, that with one design that can be connected like in figure 2.18 and with the input as zero or one, the polarity can be changed, but also the voltage V_{DD} and GND (or V_{SS} to be more general) can be flipped, which is exactly the idea of this design, that it is possible also to flip the supply voltages. The equivalent circuit build with RFETs is illustrated in figure 2.18c, and its obvious that a use of RFETs can result in a considerable decrease of hardware in circuits. So in fact, one can basically switch between the NAND and the NOR function which clearly indicates the way to generic functions, respectively, the truth table for this is shown in figure 2.18d.

So during runtime, each individual combination can be switched back and forth. So its not only for one type application and this can be done for many functions. Then comparing how many transistors are need with CMOS for a particular function and how many transistors to have these reconfigurable devices to get the same function, than one can see that the more and more complex the functions get, the more is the gain, so that fewer devices are need with RFETs. Especially considering the so called XOR (exclusive OR), they would be great to do arithmetic computations, but the resulting circuits out of these are very large and complicated to build in CMOS [17], why its preferred to keep the hands off it. In figure 2.19a and 2.19b the XOR and XNOR implementation at CMOS level is shown, where at least 8 transistors are need to get the logic function each. 2.19c

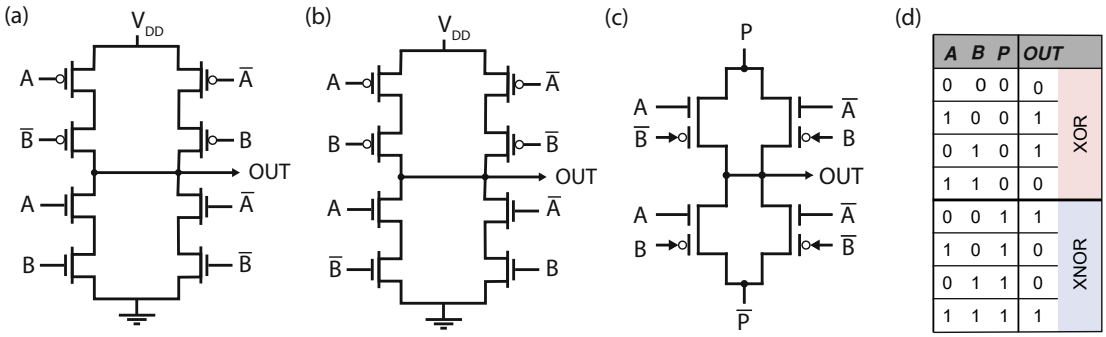


Figure 2.19: *CMOS realization of (a) XOR gate, (b) XNOR gate, (c) RFET realization of complementary XOR/XNOR depending on P , (d) truth table of XOR/XNOR gate.*

depicts the same logic function build with far less RFETs and additionally enabling to dynamic reconfigure the same structure either as XOR or XNOR.

This ability of the RFET approach therefore enables generic circuits that all look kind of the same and depend on the input can be programmed differently. Thus, it is hard to find out the function of the circuit providing a safety aspect in this way against reverse engineering. For explanations regarding the realisation, structure and behaviour of the logic gates briefly mentioned here, please refer to section 4.3.

As previously mentioned, having more gates results in more functionality, and even due to the fact that having more gates leads to a need of more periphery to steer these gates, nevertheless, considering all of this still leads to a gain in area and power consumption, using this RFET technology [56]. The difficulty lies in developing these RFETs in a reliable and well defined manner with regard to their electrical function and implementing the whole concept using current CMOS technologies, i.e. materials used, technological processes, etc.

Chapter 3

Experimental Techniques

In the following chapter, the fabrication methods, characterization techniques and main parameters of silicon nanosheet based transistors used for the work are described.

In general, the process steps for the fabrication of nanosheet devices can be divided into two procedures, the so called bottom-up processes and the top-down methods. The latter method was used to fabricate the presented devices throughout the work. This is followed by a description of the electrical characterization methods for nanosheet transistors that were relevant to the execution of this work. The transfer and output characteristics are presented, where in the former case the current modulation is shown by a change of the surface potential and the latter shows the quantitative scaling of the transistor output current with the source/drain voltage.

3.1 Fabrication of Aluminum-Silicon Based RFETs

The starting material for the fabrication is an SOI wafer with a $20nm$ thick slightly p-doped Si device layer. The procedure to create the necessary structures is started from this raw material, which is, by the way, a typical commercial wafer utilized in industry. The fabrication steps are illustrated in figure 3.1 and outlined as follows.

The nanostructure fabrication process begins with careful cleaning, following a precise cleaving as a first step. There are numerous ways suggested for cleaning the wafer, including using solvents like acetone and isopropyl alcohol, oxygen plasma, or an ultrasonic bath. The wafer is subsequently covered in photoresist (AZ5214) to expose the desired design on it. To enhance adhesion and eliminate the photoresists solvent, the sample is thereafter baked on a hot plate at 373 Kelvin, following, exposure occurs (1). There are a number of options for this; in this study, exposure using a laserwriter system - a method known as maskless lithography is used. Thus, using a UV light source (laser), the technique exposes

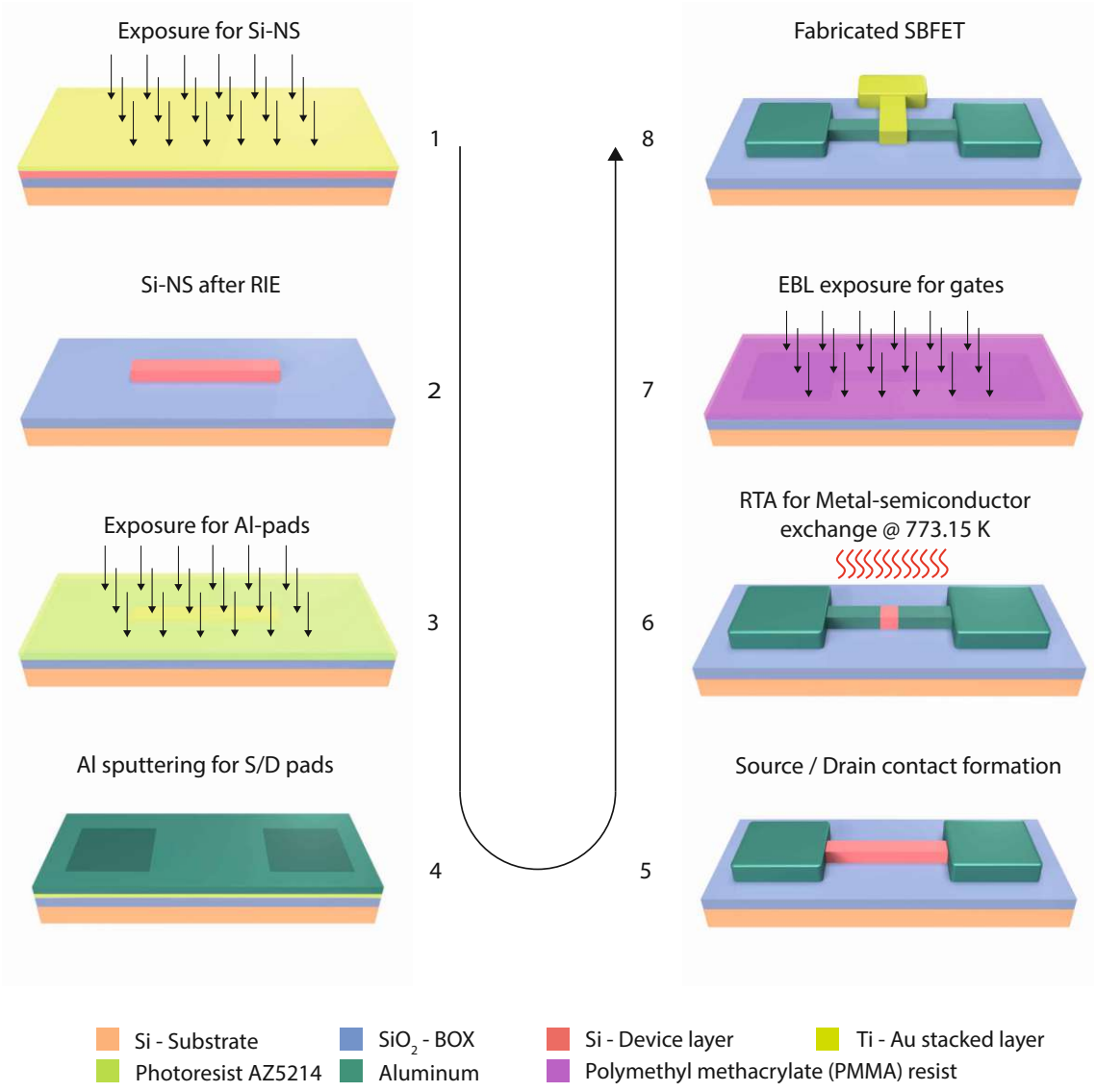


Figure 3.1: *Fabrication steps of a SBFET based on SOI*

a design pattern directly onto the resist covered substrate surface . The light pattern is chosen as binary on or off, much like in conventional mask based lithography, exposing the entire resist thickness. So a design can be changed minutes before it is exposed without time and cost constraints of a fixed mask. After developing, the samples were placed in a RIE etching chamber. The combination of SF_6 and O_2 etches away the silicon regions that are not covered by the resist with the aid of chemically reactive plasma. Reactive ions produced by this plasma are propelled onto the substrate surface, where they physically sputter the material and chemically react to produce highly steep etching patterns. Following that, acetone and isopropyl alcohol are used to remove the photoresist. Then running it through the plasma cleaning instrument so that an oxygen plasma may elim-

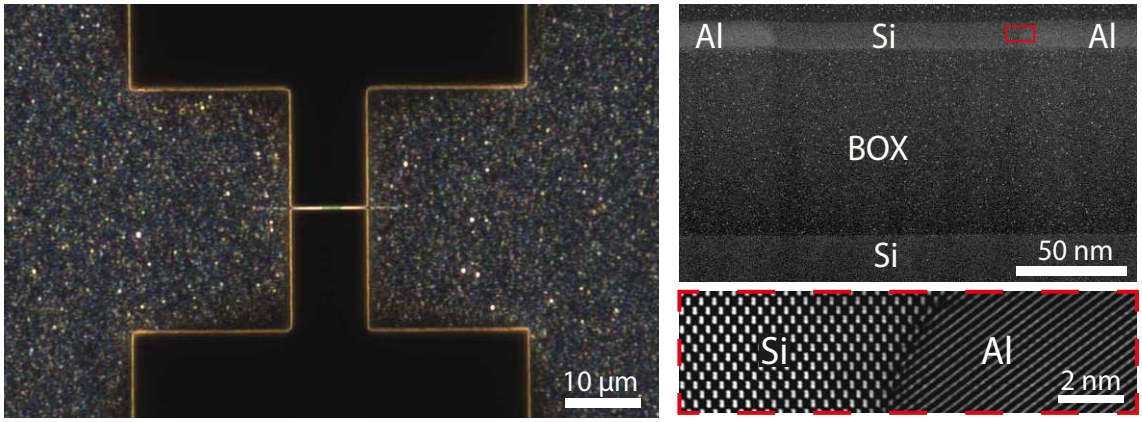


Figure 3.2: *Left image shows a microscope capture of a fabricated device without topgate i.e after the annealing process with a Si channel length of L_{Si}=2 µm. Top right shows a TEM image in cross-section of the fabricated Al-Si-Al heterostructure and the bottom right as a close-up view from the Al-Si interface of the highlighted area.*

inate any remaining resist, thus the Si sheets obtained in (2). In order to produce a high-quality SiO_2 gate oxide, thermal oxidation was performed at a temperature of 1174 Kelvin in an oxygen atmosphere for 10 minutes, and then annealing was carried out in a nitrogen atmosphere for the same amount of time. The exposure of the wafer occurs using the same resist and laser lithography settings as in step 1 (3). After developing the Al pads touching the Si nanostructures were created after the SiO_2 in the S/D contact region was removed by buffered hydrofluoric acid (BHF) dip etching to ensure a good electrical connectivity. To provide the best possible sputter result, two cleaning processes were performed, one for the sample holder and one for the target holder, followed by the 125 nm Al sputter deposition in 5 cyyles of 60 s each at a power of 50 W (4) and lift-off procedures with thermal support of acetone up to nearly its boiling point for better yields (5).

Rapid thermal annealing (RTA) at a temperature of T = 774 K in a forming gas environment to prevent unwelcome oxidation is used to trigger the Al-Si exchange process as described in section 2.2.1. As a result, monocrystalline aluminum replaces silicon in the nanosheet, atomic layer by atomic layer as the silicon diffuses out of the nanosheet and into the aluminum contacts. Al-Si-Al nanosheet heterostructures with atomically sharp Al-Si interface layers can be created using this thermally induced exchange mechanism [80]. Further reduction of the Si segment length is possible at a later stage by repeating the thermal treatment [4]. Based on statistical data, presetting the temperature and process duration ensures the production of the appropriate Si segment lengths.

Next, a distinction is drawn between structures with a single top gate and those with several top gates. In the first scenario, structuring procedures like those in points (1) and (3) are analogously carried out during the resist, lithography, and development phases of preparation. To center the top gates over the interfaces in structures with numerous top

gates, the gate positions must be measured and adjusted based on the diffusion lengths of the Al segments, i.e. on the location of the interfaces. However, because the distances between the individual gates as well as the lengths to S/D are quite tiny, electron beam lithography (EBL) is utilized because significantly higher resolutions are attainable. For structures with a single top gate, this is not necessary since the gate merely needs to be situated above the Schottky barriers and as the distances between the aluminum pads are not crucial, it is sufficient to just place the gate across the entire region.

Due to its theoretic resolution limit of less than 5 nm, the EBL, in contrast to optical lithography and the laser writer system, is appropriate for micro and nano patterning of single structures [5]. By sequentially scanning the polymethyl methacrylate (PMMA) resist layer applied to the sample by a focussed electron beam, patterning in EBL is carried out, thereby the polymer changes its chemical composition as a result of the accelerated electrons. The proximity effect, in which electrons are backscattered into the PMMA from the sample surface, limits the resolution. However, the time needed typically increases significantly, hence EBL is only utilized here as an addition to the other lithography techniques. Following the stages for mask formation by substrate coating, electron beam writing, and resist development, the structure is this time metallized by electron beam evaporation using Plassys rather than sputtered. This procedure involves the deposition of 10nm titanium followed immediately by 100 nm gold. Ti is vapor deposited at a rate of 0.05 nm/s, which serves the purpose of optimizing the workfunction, Ti also has a low contact resistance. Then a thicker layer of Au is applied, which has good mechanical stability for the tips to be applied later during the measurements, is relatively smooth and in addition, a very good lift-off is possible in terms of process technology. The fabrication of the sample is complete after another lift-off procedure in heated acetone up to 328,15 K to support the process and ultrasonic bath. Figure 3.3 depicts two of the respective devices after fabrication, further examples are shown in 4. The first is a laser-written STG and the second is an EBL patterned TTG; as can be seen, the distances between the gates are extremely short. An atomic force microscopy (AFM) image supports these small gate distances and also shows very nicely the spatial relationships - the height variations and at the same time the structural differences between the S/D areas and the gate areas as a result of the various processing steps.

3.2 Electrical Measurements

The electrical characterisation of the fabricated devices is conducted on two distinct setups. The needle probe station, shown in figure 3.4, has a total of seven micromanipulators for positioning the tungsten carbide measuring tips on the sample. This configuration is supported by an HP 4146A semiconductor parameter analyzer with four independently adjustable source-measure units (SMUs), two voltage-source units (VSUs) and two voltage measure units (VMUs). In addition, two Keysight EDU33212A function generators were integrated into the test setup for additional electrical measurements of the RFET-based circuits. The complete measurement apparatus is enclosed in a shielded cage to prevent

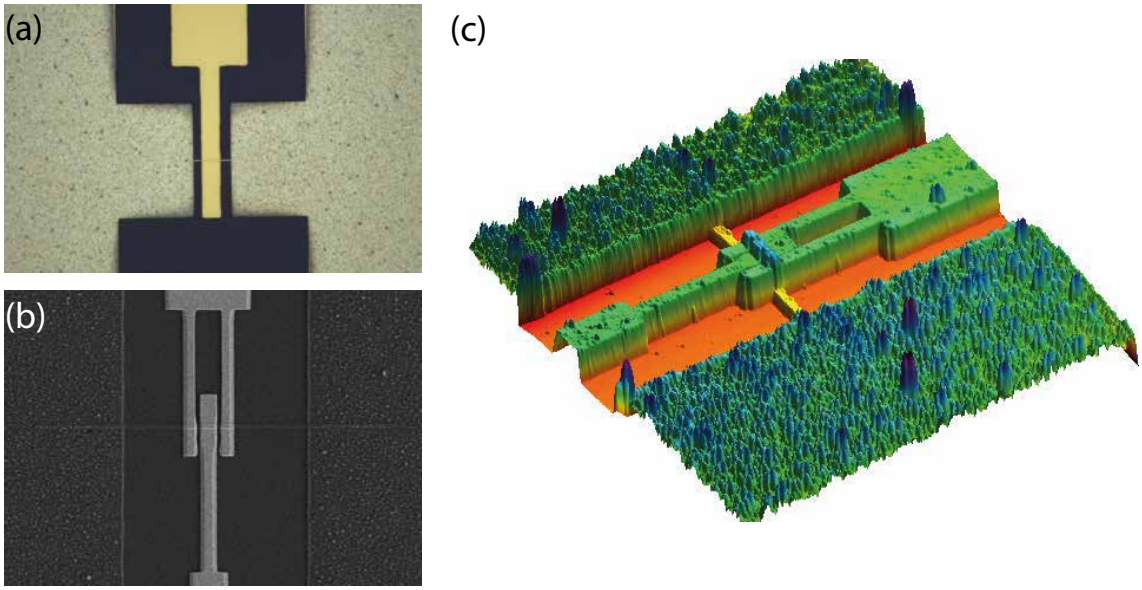


Figure 3.3: *(a) is a microscope capture of a STG device with a top gate covering the whole Si channel, with SiO_2 serving as the gate dielectric. (b) depicts a SEM capture of a TTG with small gaps between the gates; therefore, the CG is shrunk in width and two PGs are inserted atop the Al-Si interfaces. (c) shows an AFM view of a TTG, which demonstrates how small the gaps between the gates are. As a result of the vapor deposition process, the gate areas have a far smoother surface than the sputtered portions.*

electromagnetic field interference. The second measurement setup is the Lakeshore probe station, which is equipped with a Keysight B1500A, four SMUs, and a Keithley 2635A source meter unit. In this instance, measurements can also be conducted under vacuum.

The former configuration is employed for recording I/V characteristics, transfer characteristics, and input/output circuit behavior studies in general. In addition to recording I/V and transfer curves, the second setup is also utilized to record T/I curves.

3.2.1 Transfer Characteristic

The source/drain current I_D is shown in the transistor transfer characteristics as a function of the gate voltage V_{CG} at a fixed bias voltage V_{DS} and in conjunction with output characteristics, it constitutes the standard analysis used to describe electrical behavior of transistors in general. The electrostatic gate coupling has a significant impact on the transfer functions appearance and the ability to regulate the current, depending on the transistors shape, particularly the thickness and quality of the gate oxide. Note that, the electrostatic behavior are influenced by the presence of charges at the semiconductor interface due to the surface states and within the dielectric. The gate voltage cyclic sweeps may have an impact on the density and redistribution of those charges depending on the dielectric quality.

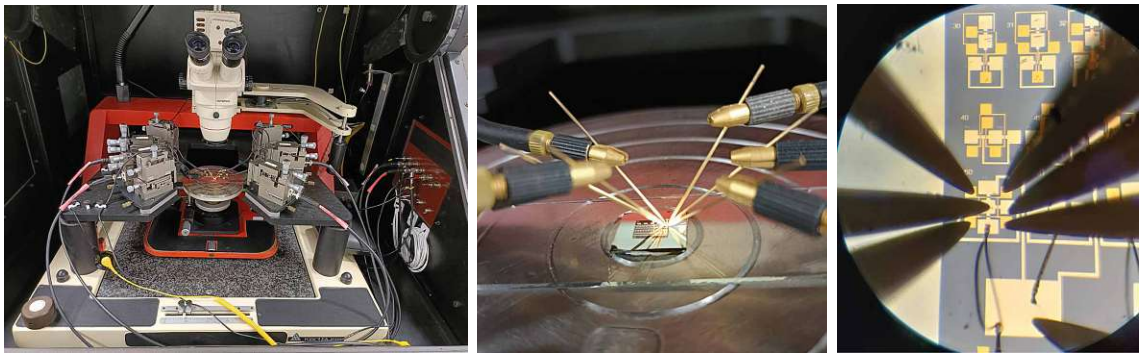


Figure 3.4: *Image on the left depicts the inside chamber of the measuring station, the micromanipulators, and the alignment microscope. In the middle image the tungsten-carbide tips, which are positioned on the sample sitting on a glass plate, can be seen. The shot on the right is a microscope image of the measurement of an XOR circuit employing seven measuring points; the delicate nature of this operation is noticeable.*

Therefore the drain to source voltage V_{DS} was varied while the currents were being recorded in order to quantify the characteristic. Starting from the negative maximum and moving toward the positive maximum, the nominal sweeping range of the gate voltage was restricted depending on the geometries of the transistor, i.e. thickness of the gate oxide and the NS itself. In the measurements for top-gated devices in this work, the range of a maximum -7 V to +7 V for the sweeping was applied. For back-gated measurements, that are not presented here but were also done to get a first overview of the characteristics the voltages must be much higher to have an electrostatic influence on the channel.

For the measurements of the realized different logic gates, the setup used for the characterization of the STG, TTG, 5TG, wired AND, and multigates had to be modified so that the transfer and output characteristics and logic switching of the devices could be analyzed. For this purpose, up to seven needles were used simultaneously; see figure 3.4 for an XOR to see how much space, or to be more precise, how little space, there is between the individual needles and therefore it is advisable to use caution in order to avoid short circuits or broken needles.

Another possibility to investigate these structures results from the existing PGs, which allow to change the injection capabilities of the Schottky barriers at the metal-semiconductor interfaces. Therefore this kind of measurement is only useful for structures which are reconfigurable, therefore not suitable for STG and of course not for normal transistors, because they are completely different regarding the configuration. This makes it possible to receive information about the transfer characteristics of the device for various V_{PG} and to establish a clear separation between the two modes and the reconfigurability of the device. The CG voltage V_{CG} and the PG voltage P are the two sweeping parameters used in this measurement. Because of this, the level of the PG voltage V_{PG} is held steady for the duration of the whole sweep of the CG voltage V_{CG} before moving on to the next stage of the V_{PG} sweep. The polarity gate voltage V_{PG} is plotted against the CG voltage V_{CG}

on separate axis, and a color scheme corresponding to the current amplitude is used as the "information plane" to represent I_D. Because individual transfer curves are obtained in a single measurement for a variety of PG voltages, this evaluation may be understood as a transfer spectroscopy because it represents a more generic example of the transfer characteristic.

3.2.2 Output Characteristic

In general, the output characteristics indicate the drain current as a function of the drain voltage at a variety of gate voltages. The output characteristics of the transistor will also be responsible for determining the operating point of the transistor, which refers to the voltage or current level at which the transistor will either switch on or off. The operating point of a transistor is critical since it is responsible for determining the amount of power that is dissipated by the transistor. Consequently, a voltage difference V_{DS} is created biasing either V_D and holding V_S at a zero potential or V_D and V_S in a symmetrical fashion, causing a current I_D to flow through the channel. This measurement is conducted using a fixed voltage level of the associated CG, resulting in one particular I-V curve. The constant voltage on PG, negative or positive enables the characterization of the device in both operation modi as n-type and p-type. In order to acquire a comprehensive picture, not only are individual output curves measured, but also a series of curves reflecting different voltage values at the CG, which gives an overall picture of the output characteristic. This then brings up the color map thats been presented in the results section. These color maps, also known as conduction maps, are representations in two dimensions of the output characteristic similar to the transfer spectroscopy explained above. The bias voltage V_{DS} is plotted against the CG voltage on separate axes and a color scheme that corresponds to the current strength is used as the "information plane" to visualize I_D. This maps are sometimes referred to as bias spectroscopy. These output curves can of course be additionally recorded at different temperatures to obtain useful information regarding the Schottky barriers.

Typically, the output characteristic is measured by sweeping both the bias voltage V_{DS} and the CG voltage V_{CG}. Therefore, the bias voltage V_{DS} is swept while the corresponding CG voltage V_{CG} is held at a fixed level until the sweep of the bias voltage is complete, at which point the CG voltage is swept in the next phase. As indicated in the theoretical section, the TTG structure can switch the operation modi to either n-type or p-type operation by setting PG accordingly. This results in two distinct output characteristics and, consequently, two output color maps, one for each mode.

3.2.3 Transient Measurement

Every transistor has the potential to be affected by transient response effects, which are characterized by a difference between the electrical output of the transistor immediately following a change in its input and the output of the transistor after that input has been maintained in a steady state or DC condition for a considerable amount of time and

of course this also applies to the design with RFETs. It should be mentioned that the operation of digital computing circuits is fully dependent on transients, which is why it is essential to investigate this behavior.

In this work, the transient measurements conducted by applying a voltage step to the input gates and observing the development in time of the currents flowing through the channel as well as the output voltage.

For the investigation of the transient processes, i.e. the switching behavior of the wired-AND structures and the logic gates as a result of injected square-wave signals, the same needle measurement setup was used, but with some extensions. In order to provide different frequencies, amplitudes, and phases for the inputs, up to two function generators with two channels each were incorporated into the logic gates circuitry. In addition, an initial oscilloscope was incorporated into the circuitry for synchronization founding and monitoring. However, it should be noted that due to the design and the comparatively long supply lines of the coaxial cables used and generally the open measurement setup, corresponding parasitic capacitances are of importance and thus the achievable frequencies are influenced, i.e. a low-pass characteristic sets in, as will become apparent later in the results section.

3.2.4 Extraction of Important Transistor Parameters

- Subthreshold swing SS

The relationship between the drain current and the gate voltage in the subthreshold range can be graphically represented on a semi-logarithmic scale as a linear function. A characteristic of the device can be defined based on its reciprocal slope. The gate swing is that gate potential change which causes a drain current change of one decade and is defined often as

$$SS = \frac{dV_G}{d(log(I_D))} \tag{3.1}$$

- Tranconductance g_m

Transconductance is a metric that quantifies the operational characteristics of both bipolar transistors and field-effect transistors (FETs). In General, when all other factors remain constant, a device with a higher transconductance value has the effect of providing greater amplification or gain and is defined as

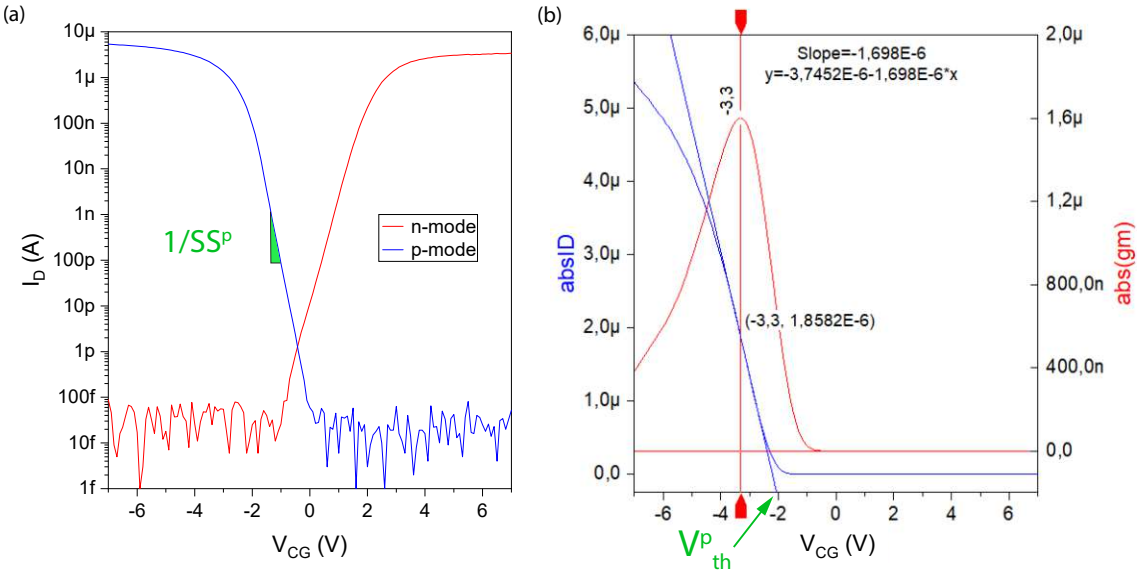


Figure 3.5: *Evaluation of the (a) inverse subthreshold slope (SS) and the threshold voltage with the transconductance method.*

$$g_m = dI_D/dV_{CG} \tag{3.2}$$

- Threshold voltage V_{th}

There are several methods available for extracting the threshold voltage (V_{th}), including the extrapolation in the linear region method, the transconductance extrapolation method, the transconductance change method or second-derivative method, the transconductance to current ratio method, the transition method, the non-linear optimization method, to name a few. Each of these methods yields slightly varying values of V_{th}. One such method is the transconductance extrapolation method which is used in this work and involves utilizing a transconductance (gm) versus gate voltage curve (V_G). This method involves determining the gate voltage axis intercept ($I_D = 0$) by linearly extrapolating the I_D-V_G curve at its maximum first derivative (slope) point $g_m = dI_D/dV_{CG}$, which corresponds to the point of maximum transconductance (g_m), as shown in figure 3.5b. One potential limitation of this otherwise valuable approach is the potential uncertainty in determining the maximum slope point. This uncertainty arises from the fact that the I_D-V_G characteristics may deviate from ideal linear behavior at gate voltages slightly above V_{th}. These deviations can be attributed to mobility degradation effects and the existence of significant S/D series parasitic resistances.

Chapter 4

Results and Discussion

There are essentially two major topics in this chapter to focus on. The first part discusses the reconfigurable transistor in light of and in compliance with the previously discussed theoretical consideration. We focus primarily on the TTG structure, introduced in 2.3.1, because it is also authoritative for the second part, but we will dare, if it appears necessary and meaningful for the understanding the view to the STG structure and draw comparisons. Doing that, the device structure will be taken into consideration first, and the structures behavior will then be analyzed through various measurements. The evaluation of the most crucial transistor parameters across a range of devices is used to conclude the first topic to show how stable and repeatable these structures are. The second part makes an effort to take things a step further by building functioning logic gates from these structures, namely an inverter, a NAND/NOR gate, and an XOR/XNOR gate, and to properly verify them in terms of functionality.

4.1 Device Structure

As already mentioned, the focus of this work is on the optimization of the TTG structures in order to be able to realize more advanced functions on the circuit level. For this purpose, various samples with different layer thicknesses were fabricated, which will be analyzed in the following. Figure 4.1a shows the basic structure of the TTG arrangement schematically, which is based on the SOI wafer discussed in the theory section 2.1.4.

Furthermore, two specific locations are shown in the same figure, one axial along the NS at the level of the Al-Si transition and one transverse to the axial direction of the NS in the center of the channel, each marked by cutting planes, the former in blue and the latter in red. At these planes, the structure of the fabricated sample was cut to obtain more information regarding layer thicknesses and composition through TEM and EDX images. As was already visible in picture 3.2 the transmission electron microscopy examination of

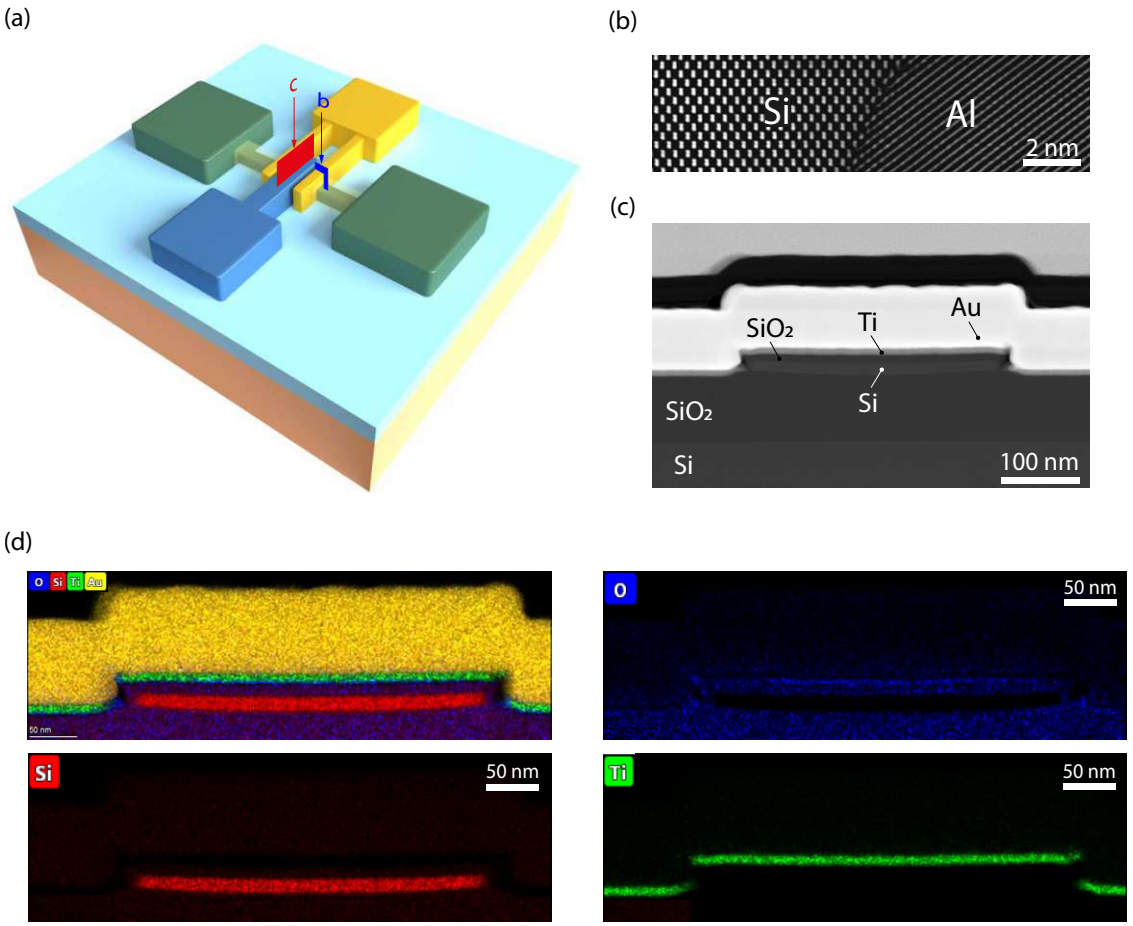


Figure 4.1: *Basic structure of the fabricated structures showing the individual layers. (a) Sketched representation of the TTG structure with indicated cut planes in blue and red. (b) HRSTEM image in longitudinal direction of the NS at labeled location (blue) as drawn in the sketch showing the Al-Si interface. (c) HRSTEM image from the cross section at labeled location (red) in the sketch showing the gate stack of the structure. (d) EDX image of the same cross section with the different layers plainly visible, represented in their totality in the first image and individually in the other images, where the exact penetration can be seen clearly.*

the sample did not uncover any indications of defects in the bulk Al as a result of the Al-Si exchange process anywhere along the heterostructure, and this holds also true for the area of the Al-Si transitions, which is of essential importance for the stability of the fabricated devices as can be seen in figure 4.1b where the abrupt Al-Si interface junction is shown in a cross sectional high resolution (HR)TEM image, which corresponds to the blue cutting plane in the schematic. When compared to bulk Al-Si junctions, nanoscale junctions exhibit neither the presence of defects nor the presence of intermetallic phases following the thermally induced exchange process. Furthermore, it is possible to see variations in the lattice constants and crystal orientations of the newly created single crystalline Al and the surviving Si segment at the abrupt contact. In spite of the fact that the remaining Si

segment had a diamond structure, the Al component of the heterostructure proved to have a face centered cubic (fcc) crystal structure. As indicated by the pattern, both crystals are oriented along a <110> zone axis with a mutual in-plane rotation with respect to one another, and this orientation automatically adjusts during thermal exchange reaction, most likely providing a reduction in mechanical strain to compensate for the lattice mismatch differences between Al and Si [80]. In this context, the annealing rates of the investigated TTG structures are evaluated and shown in figure 4.2. It can be observed that with an average value of 57.9 nm, fairly consistent rates are attained across all devices. This, in turn, demonstrates the diffusion process's high controllability for the targeted formation of appropriate junctions, as well as its repeatability. Note that the 40 values displayed pertain to the 20 devices investigated, implying that a pair of values always belongs to the same device because the Si-NS under study is subject to Al diffusion from both sides, in the figure indicated for one side as right and for the other side as left.

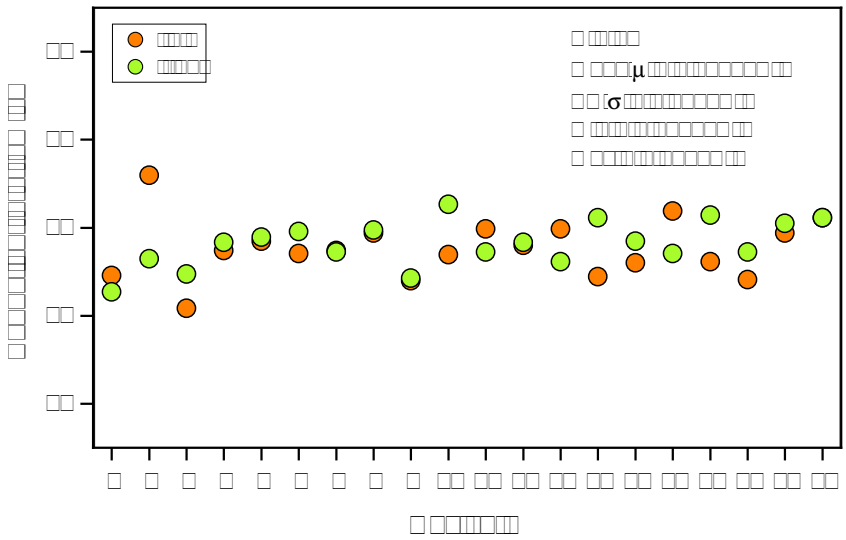


Figure 4.2: *Al-Si exchange rate of the considered 20 devices. Left and right represent the exchange rates of two different sides of the NS along the axial direction, the corresponding values are noted in the figure.*

These minor discrepancies in the exchange rate can be explained by the NS's slightly varying widths, which range from W = 317 nm to W = 485 nm. The exchange rate increases for smaller geometries and exhibits a $1/\sqrt{W}$ dependency, demonstrating that Al-Si exchange is surface limited [80].

In order to determine the layer composition and thickness of the entire device, not just the NS, so here the gate dielectric and the top gates are also taken into account, the figure shows a cross sectional high resolution (HR)TEM image of the transversal cut to the NS, which corresponds to the red cutting plane in the schematic. These additional layers, once the SiO_2 and once the Ti/Au top gate electrodes can be seen in figure 4.1c. It is important to note that during the process of forming SiO_2 by dry oxidation, which has

been carried out in the context of this work, the SOI that was mentioned at the beginning as a starting point with the mentioned layer thicknesses, or, to be more specific, the device layer, i.e. the Si, which is followed by the SiO_2 layer, is consumed in the formation of the oxide. Additionally, it is important to point out that the transformation of silicon into silica dioxide does not take place in an additive manner. This means that the total layer thickness of both sections combined before and after the dry oxidation process does not remain the same. By this process, the dry thermal oxidation at a temperature of 1174 Kelvin in an oxygen atmosphere for 10 minutes, and then annealing in a nitrogen environment for the same length of time the high-quality SiO_2 gate oxide was established. The TEM investigation indicated above is utilized to determine the corresponding thickness of the layers. The ellipsometer was also used to assess the passivation layer, however there are minor differences here. The numbers shown below for the final gate stack are for TEM measurements corresponding to figure 4.1c

- 100.4 nm - Au top gate
- 10.2 nm - Ti top gate
- 12.4 nm - Passivation layer SiO_2
- 15.4 nm - Unstrained device layer
- 102.2 nm - BOX
- Si - Substrate

For clarification, it should be noted that the layer on top of the Au layer in the figure is a carbon layer required for TEM studies, which is only applied after the electrical characterization of the sample. The first subfigure of figure 4.1d depicts an EDX picture of the corresponding gate stack as a whole, which belongs to cut plane c. The above-mentioned distinct layers are immediately evident. The Si-NS is sharp and free of impurities, the Ti likewise has a crisp contour, and the O is spread below and above the NS. On a closer look, there are also extremely little red dots in the O part, which represent the Si component of the SiO_2, but at a much lower concentration than in the NS area, which explains why it is not as obvious.

One more thing should be mentioned, for the realization of the logic gates an extra sample was made with the same gate stack structure as just presented. Only a shorter dry oxidation was deliberately carried out, exactly half the time of before, i.e. 5 minutes, in order to make the gate dielectric thinner and thus optimize it with regard to the voltages used, resulting in a Si device layer thickness of 16.4 nm and a SiO_2 dielectric thickness of 10.3 nm, this should be kept in mind when looking at the related results.

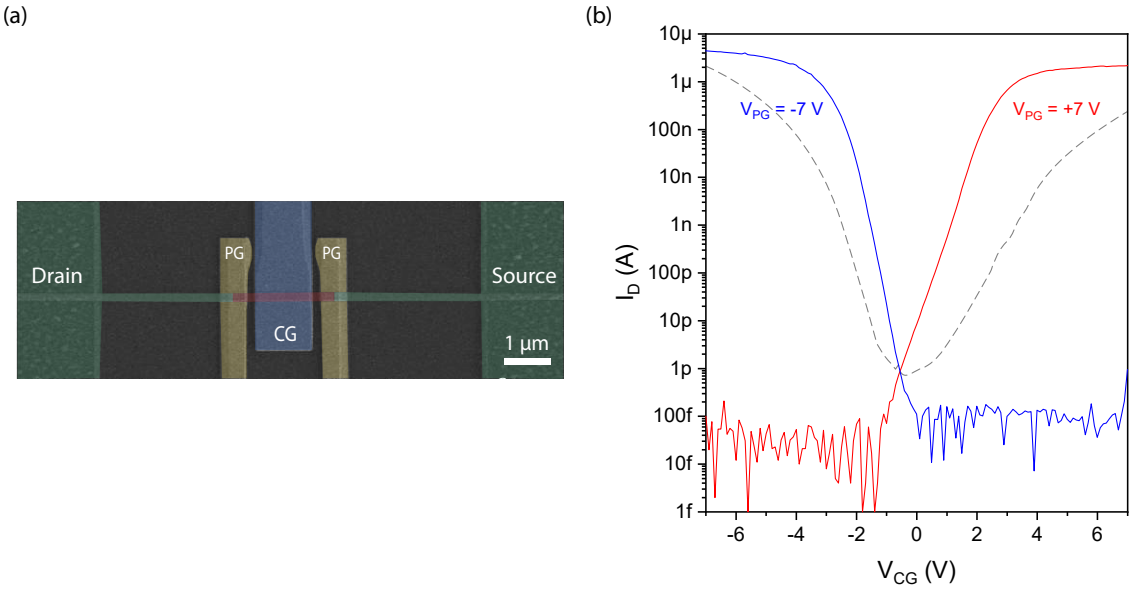


Figure 4.3: *(a) SEM image of a top-down fabricated triple top gated heterostructure, the red color segment indicates the Si channel. (b) shows the transfer characteristic of this TTG, red and blue depicts the characteristics when operated as RFET and in black when operated as a quasi-STG.*

4.2 Triple Top Gate

Depending on the electrical circuitry, the objective of the reconfigurable transistor is to establish a characteristic that corresponds to a unipolar p-FET or n-FET. This can be accomplished because only one kind of charge carrier is allowed to participate in the flow of current through an RFET, in contrast to the SBFET, which allows both electrons and holes to contribute to the drain current across the full switching range. This is accomplished by inhibiting the insertion of undesirable charge carriers as explained in the theoretical section 2.3. Figure 4.3a shows the SEM image of such a TTG structure. As can be seen, the PGs are positioned above the metal-semiconductor interfaces, the CG is centered above the channel. This three adjacent enclosing topgates along the NS allow for the coupling of MS barriers with two linked topgates and channel coupling with one independent topgate. The top gates can be supplied independently from each other, which is made clear in figure 4.3b and which is the motivation why the focus of this work is on the TTG structures, especially regarding unipolarity. If the top gates are operated independently of each other, i.e. the PG and CG, the p-characteristic (blue) and the n-characteristic (red) are obtained. The transfer characteristic in black corresponds to the case when this TTG structure is operated as a quasi-STG, i.e. operating as a SBFET, meaning when all potentials at the PGs and CG have the same values. It is quite clear that in the case of the TTG, the on-currents are higher in both p-mode and n-mode, and the off-currents are lesser then for the quasi-STG, meaning that the TTG structures show distinct off states with regard to the corresponding n-type or p-type operation as a result of the additional control gate (CG), and the subsequent suppression of undesired charge

carrier currents. Furthermore, a fundamental difference in the slopes can be seen, which is of great importance especially for the use in logic gates. Here, the behavior of a p-type transistor results from the blockade of electron injection due to a potential barrier. This is generated at the contact electrodes by a negative voltage which corresponds to a band bending in the direction of positive electron energy and vice versa for the n-type transistor, as was explained in section 2.3.1. Note that the injection barrier between the metal and semiconductor must be adequately tuned, and this requires proper positioning of the PG electrodes above the Al-Si junction. The measurements were performed at a polarity gate voltage of +7 V for the n-mode and -7 V for the p-mode. The control gate is swept from V_{CG} = - 7 V to V_{CG} = +7 V and then back to V_{CG} = -7 V, which indicates then the hysteresis.

On the following pages the results of the TTG are presented and analyzed, especially with regard to the necessary characteristics, which are essential for the use in cascaded circuits, and to the reproducibility and stability of the devices. All of the depicted transfer curves are acquired utilizing the double measurement technique, with a applied bias voltage V_{DS} and various top gate voltages V_{PG} and V_{CG} in an atmospheric ambient condition.

4.2.1 Transfer Characteristic

The tranfer charcteristic of the RFET are depicted in figure 4.4. At a positive PG voltage of V_{PG} = +7 V, as indicated by the red contours in both subfigures, the RFET functions as an n-type FET with electron induced current flow at positive CG voltages, with is swept from -7 V to +7 V in both directions, indicated by the arrows. The emerging barriers effectively block the gaps, resulting in extremely low off currents at negative V_{CG} by reducing reverse junction leakage. At V_{PG} = -7 V and negative CG voltages, the p-type is enabled, resulting in efficient hole conduction and electron blockage. However, we can see that this off-center point is not precisely in the middle at the value 0, but is slightly displaced toward negative values, which may indicate minor production-related irregularities. Notably, this measurement was not conducted with symmetrical bias voltages, i.e. V_S was always maintained at zero potential V_S = 0 V and V_D was always set to a higher potential, in this case V_D = 1 V. Onward is an evaluation of symmetrical bias voltages before considering the logic gates. As can be seen in the same subfigure, there is hardly any hysteresis in both operation modes, which indicates a very suitable interface and which is of highly interest for operating them in more sophisticated circuits. It is apparent that the p-type on state current, which is 3.91 μA, and the n-type on-state current, which is 2.34 μA, result in a remarkable on-state symmetry. This is shown by the ratio of the on-state currents, which is around 1.67. It should be noted that an important parameter here is the current related to the width of the channel, since the NS widths differ slightly. However, in order to avoid giving this value for all the individually considered structures and causing confusion, these values for all devices are summarized in a table at the end of the chapter. Additionally, by effectively suppressing the undesirable charge carrier type with appropriately high PG voltages, off-state currents for n-type and p-type operation are kept below the measurement setups resolution limit of 100 fA. The energy landscape,

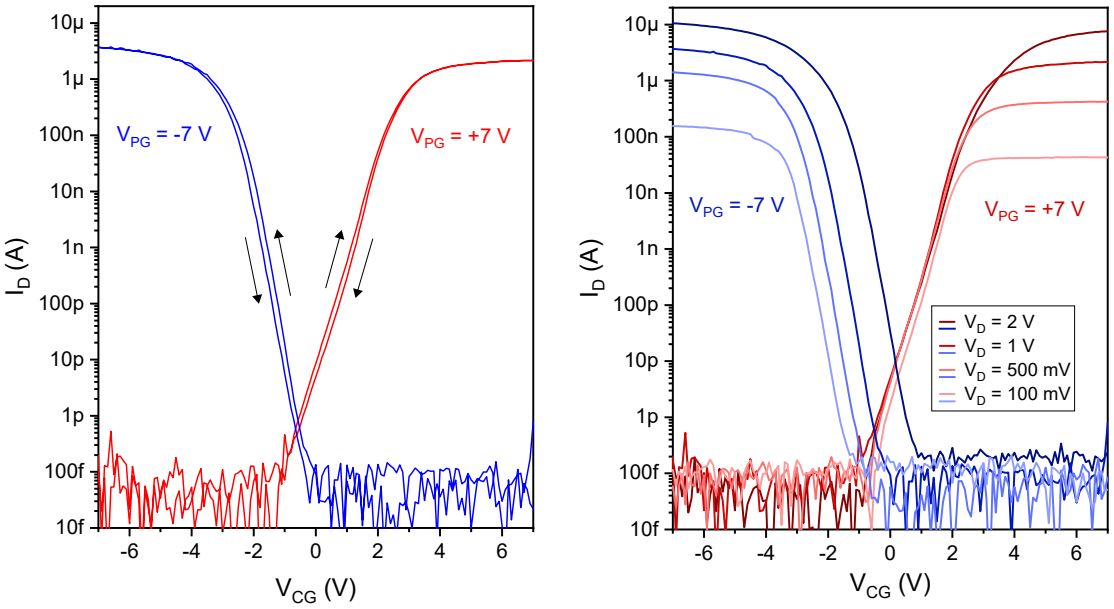


Figure 4.4: *Transfer characteristic of the TTG structure. (a) Double sweep measurement performed at room temperature (295 K) and atmospheric ambient conditions with applied bias voltage V_{DS} = 1 V and V_{CG} swept from +7 V to -7 V and reverse for each mode, which is set with by V_{PG}, for p-mode (blue) and for n-mode (red). (b) Shows for the same structure the transfer characteristic as one sweep measurement with the same PG and CG voltage as before at different bias voltages.*

which was covered in the theoretical section 2.3.1, may be used to explain this astoundingly good pinching off. Thus, an additional band bending in the channels midsection through the potential of the CG occurs and thus results in this smaller off-state current, especially in comparison to a STG, as it is also shown in figure 4.3.

In subfigure (b) the transfer characteristics of the same structure with the identical values of V_{PG} and V_{CG} as before are shown, only this time at different bias voltages. The measurements were also taken in double sweep mode but for clarity only one sweeping direction is shown. It should be noted that always the potential at V_D is changed, V_S always remains at zero potential. The measurements were performed at bias voltages of 100 mV, 500 mV, 1 V and 2 V, represented in this order by the increase in color intensity in the curves. It can be seen that in the case of 100 mV bias the on-currents in n-mode are 42 nA and in p-mode 175 nA, which results in a symmetry of the on-currents of 4.2. Now increasing the bias voltage from 100 mV, for example, at V_D = 500 mV bias voltage, the hop of the on-current in n-mode is much larger than the hop of the on-current in p-mode, expressed in numbers these are 492 nA in n-mode and 1458 nA in p-mode, thus a symmetry of the on-currents of 2.96 follows. And these different hops from n-mode on-current to p-mode on-current continue with further increase of the bias voltages, so that finally at a voltage of V_D = 2 V a symmetry of the on-currents of 1.41 results. This means as V_D is increased, the on-currents can be fine-tuned to optimize the symmetry. No

values can be given for the off currents, since, as already mentioned, the measuring system is not able to detect them. But it is recognizable at a closer look, that at 2 V bias voltage, the off-current of the p-mode increases, as it is just above the 100 fA line, which would be in accordance with the presented theory. Additionally it can be seen that the slope of both modes are in the same range and a change of the bias voltage has no influence on this, which is of course immensely important for cascaded circuits to be able to operate them at different voltages without a change of the switching behavior and secondly it is indispensable to guarantee a certain slope to enable fast switching at all. Here, too, the exact values are listed in table 4.1 over all devices.

Furthermore it can be seen immediately that with increasing bias voltage the off-point of the p-mode shifts to positive voltages CG, which causes the fanning visible in the figure, while the changed bias voltage shows no shift with respect to the off-point of the n-mode, the band structure explains why this is the case quite well. As indicated in the theoretical part, the application of a particular V_D has no effect on the barrier's shape or height at the source. Nonetheless, the drain voltage influences the barrier's shape on the drain side. Consequently, the tunneling current through the drain side Schottky barrier grows exponentially as the barrier's tunneling probability increases. Therefore, as V_D becomes more positive, the barrier on the drain side becomes thinner, implying that the current rises as V_D increases. If the sign of the bias voltage were reversed when considering the p-mode, a behavior of the same appearance as the n-mode would occur, i.e. without a fanning out for the transfer characteristic, since in this case with negative V_D the charge carrier injection occurs from the source side, which does not experience any potential change and thus the current remains approximately the same for a fixed CG value. It is possible to ascertain how and to what extent charge carrier injection occurs as a result of the barrier thickness based on where the potential is applied in relation to the two source-drain contacts. It should be noted that these measurements were performed subsequently, particularly in relation to the circuit implementation. How this appears in greater detail, for instance in the case of symmetrical bias voltages, i.e. V_D = -V_S, will be addressed in subsequent considerations.

Obviously, the controllability of the channel can improved by using e.g. high-k materials as gate dielectric, which was also initially considered in the context of the work, in order to reduce the applied voltages while maintaining high on-currents and the remaining characteristics. However, since the results of these RFETs with SiO_2 as gate dielectric were promising, especially with respect to the hysteresis, the on-current symmetry as well as the on/off-ratio of the respective currents, this necessity was abandoned. It is important to note that when incorporating an extra dielectric layer, such as hafnium oxide (HfO_2), additional considerations must be taken into account. In such a case, it is important to consider the potential shift of the transfer characteristic, specifically the threshold voltage, caused by the introduction of traps at the interface or the formation of dipole moments at the SiO_2-HfO_2 interface. These factors can significantly impact the threshold voltage, thus requiring careful handling and the establishment of an appropriate trade-off. However, for the realization of the logic gates, an optimization with respect to the SiO_2 was

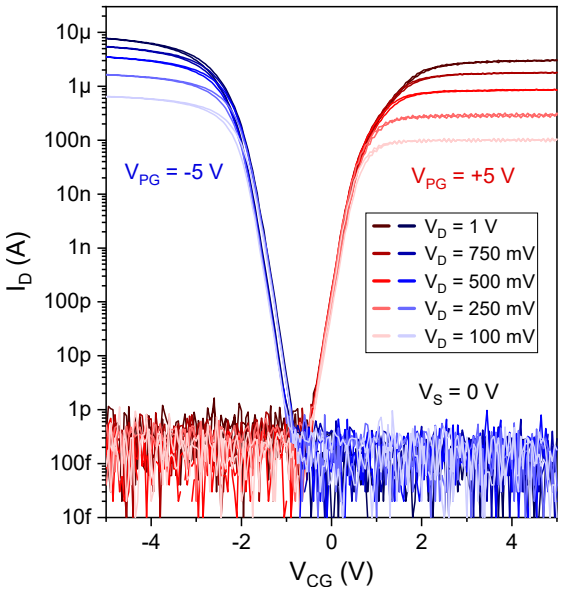


Figure 4.5: *Transfer characteristic of the TTG structure with thinned down SiO_2. Double sweep measurement performed at room temperature (295 K) and atmospheric ambient conditions with applied bias voltages V_D = 100 mV to V_D = 1 V by holding V_S at zero potential. V_{CG} swept from +5 V to -5 V and reverse for each mode, which is set with by V_{PG}, for p-mode (blue colors) and for n-mode (red colors), respectively.*

focused on in order to scale down the necessary voltage levels in a next step without losing the good characteristics.

The curves in figure 4.5 show the characteristics of the two modes from the sample with the thinned SiO_2 with a thickness of 10.3 nm. Compared to the previous case, it can be seen that the center is shifted to negative values in exactly the same way, which nicely demonstrates the reproducibility using the same material system and processes. Due to the thinner oxide, the applied voltage levels at PG and CG can be reduced, shown here for a voltage level of ±5 V, but it should be noted that also with ±4 V the same characteristics are achieved, i.e. the transistor can be steered out. And you can see clearly how the reduction of the oxide improves the influence of the top gates on the channel, because here on-currents of 3.7 μA are measured for the n-mode and 7.7 μA for the p-mode at a bias voltage of V_D = 1 V, resulting in a symmetry of the on-currents of 2.1. In direct comparison it can be seen that the on-currents are higher than with the thicker oxide where finally a voltage level of ±7 V was applied, whereas the symmetry is comparable of both cases. The previously mentioned fanning out is completely absent here, which is not related to a structural change but, as mentioned, is due to the injection mechanisms, which are influenced by the bias voltages. The source potential is always set to 0 potential, in the n-mode V_D is set to positive level, whereby the injection of the electrons takes place from the source side and thus with change of the bias voltage at V_D its barrier is hardly influenced. In p-mode, V_D is set to negative level to achieve the same behavior, whereby

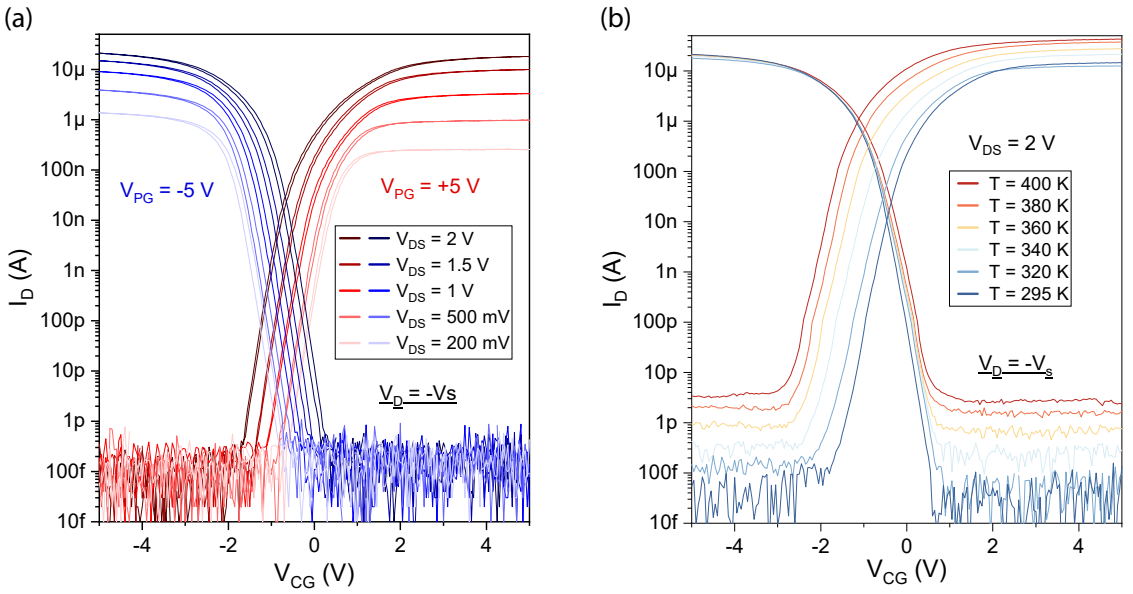


Figure 4.6: *Transfer characteristic of the TTG structure with thinned down SiO_2. (a) Double sweep measurement performed at room temperature (295 K) and atmospheric ambient conditions with symmetrical applied bias voltages V_{DS} = 200 mV to V_{DS} = 2 V. V_{CG} swept from +5 V to -5 V and reverse for each mode, which is set with by V_{PG}, for p-mode (blue colors) and for n-mode (red colors), respectively. (b) Single sweep transfer characteristic of the related device at symmetric bias voltage V_{DS} = 2 V at different temperatures starting from room temperature (295 K) up to 400 K in 20 K steps*

due to the energy landscape of the bands, the injection also takes place from the source side and thus in both cases there is no relevant influence by the bias voltage, so that no fanning out takes place. Note that the measurements here done in a double fashion and also presented in this way, however because of the superior quality of the SiO_2 gate dielectric, the device characteristics do not exhibit any hysteresis.

Finally, figure 4.6 shows the case of a symmetrical bias voltage applied for the same structure, i.e. $V_D = -V_S$. As can be seen, the behavior is basically very similar to the other operating modes, which was discussed above. However, the on-currents are somewhat higher in both modes with the same potential difference between source and drain, e.g. at V_{DS} = 1 V, i.e. 500 mV at source and -500 mV at drain, the n-mode on-current is 4.1 μA and the p-mode on current 9.1 μA, thus resulting in a comparable symmetry of 2.2 of the on-currents. What can also be noticed is that the cross points of n-mode and p-mode stay at the same VCG value regardless of the bias voltage that is applied, albeit slightly shifted toward negative values as in the other cases, but with a constant value. This representation is particularly useful for cascaded systems since, in these types of circuits, it is preferable to guarantee that as few voltage levels as feasible are preserved for the operation of the circuit.

Obviously, the thermal stability of the structures is also of great importance, as it must be ensured during operation; thus, these studies have also been conducted. Figure 4.6b depicts the transfer characteristics as single measurements from on-state to of-state for both modes at symmetrically applied bias-voltages V_{DS} of 2 V and the same V_{PG} and V_{CG} values as before, specifically V_{PG} at a positive or negative value of 5V depending on the mode and V_{CG} as the sweeping value between -5 V and + 5 V at various temperatures ranging from room temperature (295 K) all the way up to 400 K in 20 K increments. In the case of n-type operation, the on-state current as well as the off-state current for both modes increases with higher temperature with the increase being greater for the off-currents. On the other hand, the on-state current for p-type operation remains almost constant regardless of the temperature. The observed behavior can be adequately explained through the utilization of the injection mechanisms. In general, the observed rise in off-currents can be attributed to two factors: an increase in thermally generated charge carriers that surpass the Schottky barrier (TE), or a higher rate of charge carrier injection through thermally assisted tunneling (TFE). Moreover, it is evident that the increase in on-currents is significantly lower, particularly for the p-type operation where it is barely noticeable. This indicates that the change is contingent upon the prevailing transport, since the temperature dependence of tunneling (FE) dominated current, specifically the on-currents is lower in comparison to the thermionic emission dominated current and indicates therefore that the major charge carriers can be attributed to tunneling, which aligns well with the existing literature. [40, 79]. This fact has no significant influence on the slopes of both modes at different temperatures. Besides that, interestingly, it is worth noting that the on-current symmetry of the TTG structure initially improves as the temperature rises, then reverses as the temperature continues to rise and takes on worse values again. This is attributed to the quasi non changing p-type on-current and the increase in the n-type on-current. The observed phenomenon can be attributed to the disparity in barrier sizes between electrons and holes, resulting in distinct temperature dependencies in the on-region for each case. In the case of p-type, a highly transparent barrier is present, leading to the significance of tunneling. As a result, the current remains relatively constant or may even exhibit a slight decrease as the temperature increases. On the other hand, in the case of the n-type, there is a small Schottky barrier that remains in the on-region, which is the reason why the typical Schottky behavior is observed, where the on current increases as the temperature rises, as thermionic emission (TE) plays the dominant role in this scenario.

4.2.2 Output Characteristic

The measurement data is collected at room temperature of 295 K. The applied bias voltage, V_D, is varied from -2 V to 2 V, while the CG voltage is adjusted in increments of 500 mV ranging from -7 V to 7 V. The source voltage is again at a potential of zero. It is evident that both modi demonstrate the characteristic non-linear increase of the V_{CG} dependent current in the TTG structures. This can be observed in the semi-logarithmic representation depicted in figure 4.7, (a) for n-type and (b) for p-type operation.

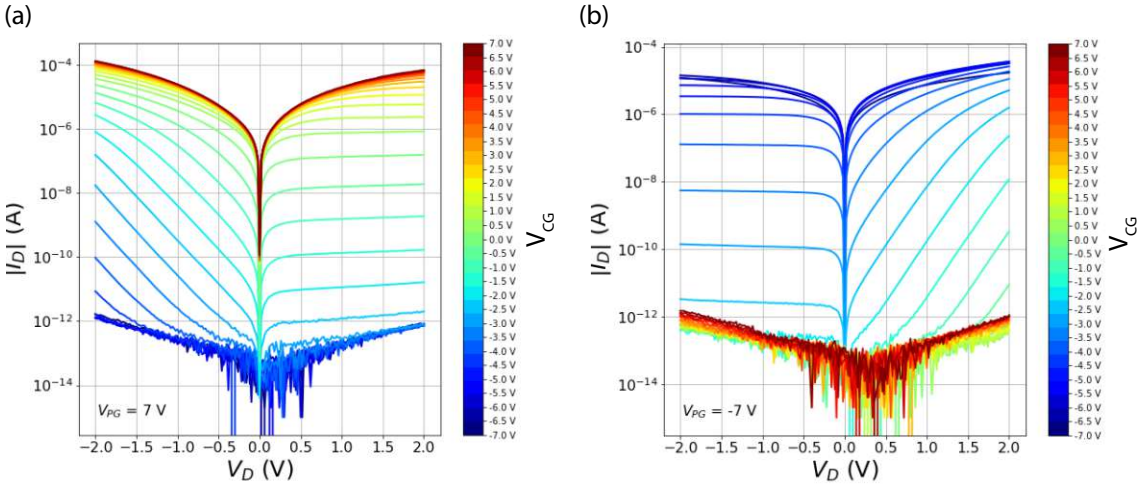


Figure 4.7: *Output characteristic in semi-logarithmic representation of the drain current over bias voltage V_D at different CG voltages V_{CG} performed at room temperature (295 K). (a) n-type operation and (b) p-type operation*

As can be seen the TTG devices demonstrate a highly symmetric behavior in terms of their output characteristics with respect to the applied bias voltage. The variations in the on-state currents of different charge carrier operation types can be attributed to the distinct effective Schottky barriers and the resulting Fermi-level pinning.

The measured data points can be compiled into a color-coded map of the output curves. These visual representations effectively demonstrate the performance capabilities of the structure and moreover, one acquires valuable insights into the stability characteristics of the structures. For the sake of completeness, switching from p-mode to n-mode and vice

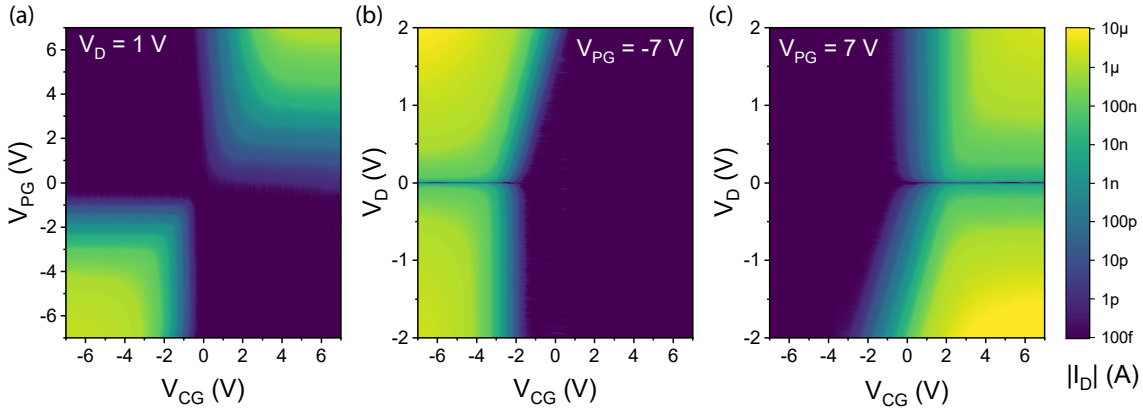


Figure 4.8: *(a) Shows the device behavior when switching from n- to p-operation, revealing the cut off of the current in this region, also referred as transfer spectroscopy. (b) and (c) shows semi-logarithmic conductance maps of the p-type (V_{PG} = -7 V) and n-type (V_{PG} = 7 V) operation separately.*

versa is shown in 4.8a. This representation originates from the transfer characteristic and is therefore also called transfer spectroscopy and should not be confused with the output characteristic. One notable observation in figure 4.8b & c is that a larger on-state area is observed for positive V_D in p-mode and for negative V_D in n-mode. That result was thoroughly examined in the theory section 2.3, and it can be attributed to this particular fact. When a positive voltage is applied to the drain electrode, the effective electron barrier exhibits an increase. Simultaneously, the barrier for hole injection diminishes, thereby potentially resulting in an enhanced flow of holes into the semiconductor material. Nevertheless, the application of a negative voltage to the metal electrode leads to a reduction in the work function of the metal. Consequently, this reduction causes a decrease in the barrier that impedes the movement of electrons. Simultaneously, the barrier for electron holes is elevated, resulting in an enhanced flow of electrons into the semiconductor.

The conductance maps reveal unipolar characteristics and well defined on- and off-states of the proposed Al-Si RFET in both operation modes and therefore allows to derive optimal operation points of the device. For the Al-Si-Al based RFET, an absolute value of $|V_{PG}|$ = $|V_{CG}|$ = 7 V and V_D = 1 V was determined for the ideal operation of logic gates, as this bias level sufficiently tunes the incorporated energy landscape of the semiconductor as well as drives an appropriate drain current.

To conclude this subsection and for completeness, the output characteristics of the TTG RFET structures of the circuit sample (i.e., the one with the thinner oxide) are shown as 2D-color maps in figure 4.9. Whereby subfigures (a)-(f) illustrates the color maps associated with the p-type operation (V_{PG} = -5 V), while subfigures (g)-(l) presents the n-type operation (V_{PG} = 5 V) for the thermal investigations conducted at different temperatures ranging from room temperature (295 K) to 400 K in increments of 20 K and symmetrically apllied bias-voltages V_{DS} ranging from -1 V to 1 V and sweeping V_{PG} from -5 V to 5 V. Observing the upper maps for p-type operation, it is evident that the off-state current exhibits an slightly increase at higher temperatures, while the on-state current remains relatively unaffected. However, there are notable distinctions in the case of n-type operation. It is observed that the off-state current rises slightly with increasing temperatures, while the on-state current also experiences a slight increase at higher temperatures, albeit not as significant as the off-state current. This aligns with the findings previously at the transfer characteristic regarding the thermal analysis of the same TTG structures in figure 4.6b. However, a distinct pattern emerges when observing the temperature increase, starting at 380 K and becoming significantly more pronounced at 400 K. In the provided image, there is evidence of an elevated current in the off region, indicated by the smearing of the blue area. Based on the results of the investigations, it has been determined that the current fractions observed are a result of oxide breakdown occurring from the gate side. It is noteworthy that the temperature dependent measurements of the transfer characteristics, as observed in figure 4.6b, did not exhibit any similar issues under identical measurement conditions. It is important to acknowledge that the measurements were conducted months later compared to the initial measurements, which makes it plausible that the sample may have undergone some form of degradation during this period.

Figure 4.9 also shows the different transport regimes already discussed in chapter 2.3 on the basis of the slopes of the transfer characteristics, these regimes can also be identified here. Given that tunneling is the dominant mechanism for current flow through barriers, it is observed to have less dependence on temperature compared to thermionic emission. As a result, the regimes of thermionic emission (TE), field emission (FE), and thermionic-field emission (TFE) can be estimated. The off-state current, as represented by blue sections in the color maps, is clearly dominated by TE current, while tunneling drives the majority of the on-state current and is represented by yellow sections with the green zones between depicts the TFE regime. Still, it is important to note that these predicted transport regions should be approached with reservation because it is typically very difficult to achieve a precise separation between the various regimes. Therefore, it should be interpreted more as a method of approximation rather than a precise statement.

4.2.3 Statistical Evaluation

On top of that, a comprehensive analysis and evaluation of twenty Al-Si-Al NS RFET devices was conducted. As previously stated, this evaluation pertains to the TTG structures featuring a thicker SiO_2 oxide layer, specifically with a thickness of 12.4 nm. The channel widths of these structures range from W = 317 nm to W = 485 nm. The voltage applied to the bias V_D terminal is set to 1 V, while the voltage applied to the V_S terminal is set to 0 V. The top-gate voltages V_{CG} were configured to ±7 V, depending on the mode, while V_{CG} was swept within a range of -7 V to +7 V.

The characterization of transistors involves crucial parameters such as on- and off-currents, on- and off-current density, on/off-current ratio, threshold voltage, subthreshold slope, and transconductance in both n- and p-type operation. These parameters are depicted in the figures 4.10 4.11 4.12 4.13 4.14 4.15. The transconductance is defined as the quotient of the output current divided by the input voltage. The determination of the threshold voltage is achieved by identifying the position of the maximum transconductance (g_m) derivative with respect to the gate voltage (V_g), i.e. calculating the derivative of the drain current. The subthreshold slope was determined by analyzing the transfer characteristic, as described in section 3.2.4.
The evaluated mean on-current normalized to the width of the NS is I^n_{on} = 6.24 μA/μm and I^p_{on} = 11.81 μA/μm and the off-currents $I^{n,p}_{off}$ are below the resolution limit of the measurement system. Here, the mean symmetry of the on-currents results to a factor of 1.9, as also stated in the previous subsection. Please be advised that the hysteresis was determined by computing the disparity between the threshold voltages V_{th} during the double measurement sweep. A hysteresis of 71 mV in n-mode and 110 mV in p-mode operation was extracted. The mean values and standard deviations of all significant determined values for a set of twenty NS based RFETs are documented in table 4.1.
The illustrations clearly demonstrate the exceptional stability and remarkable reproducibility of TTG structures based on NS. These characteristics provide a solid foundation for the design of cascaded circuits using these structures. However, prior to transitioning to the circuits, it makes sense to examine initial multi-CG RFETs.

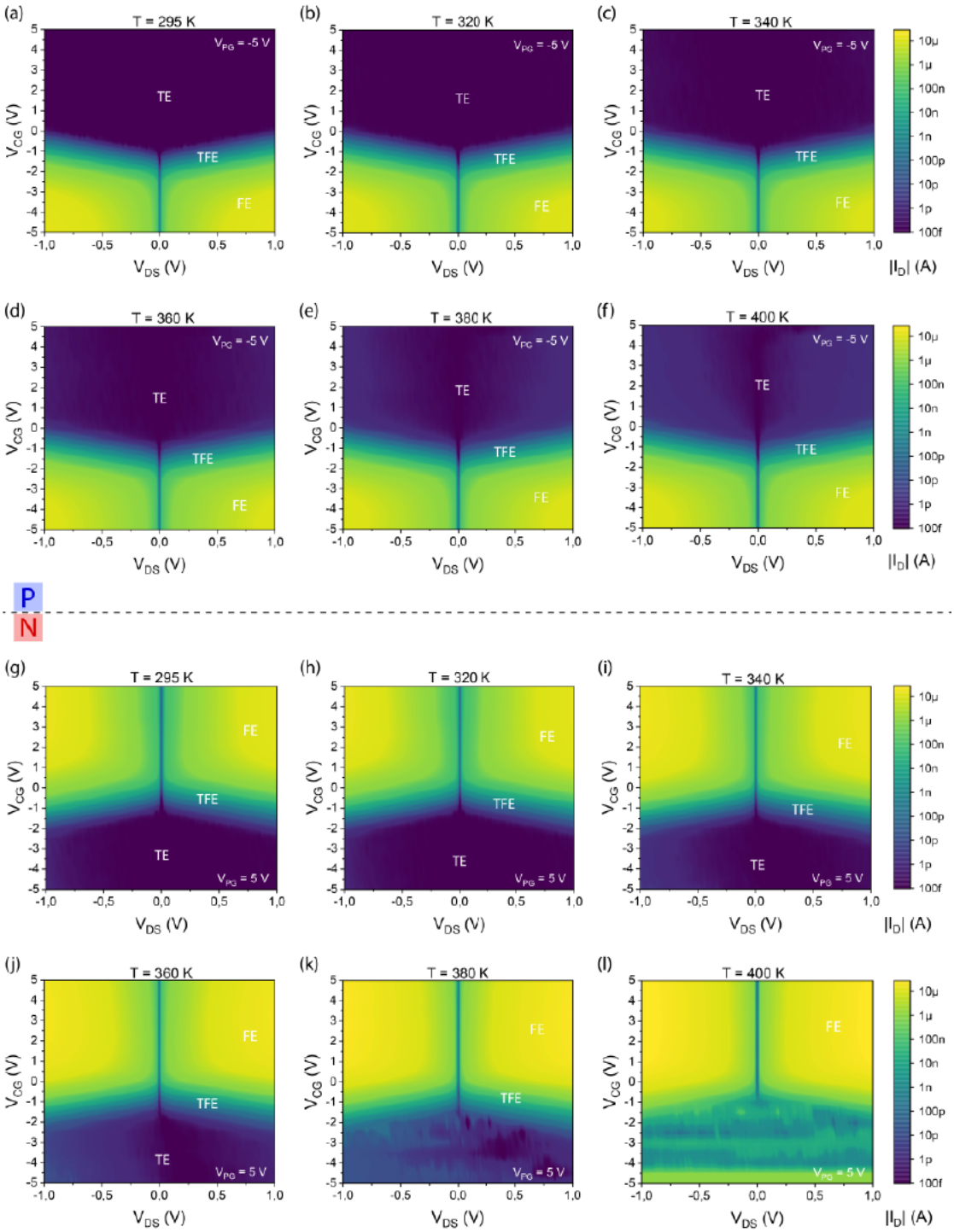


Figure 4.9: *Output characteristic of a TTG (colour map) at symmetric bias voltages V_DS of 2 V for (a-f) p-type operation (V_{PG}= -5 V) and for (g-l) n-type operation (V_{PG}= 5 V) at different temperatures from room temperature (295K) up to 400K in 20K steps.*

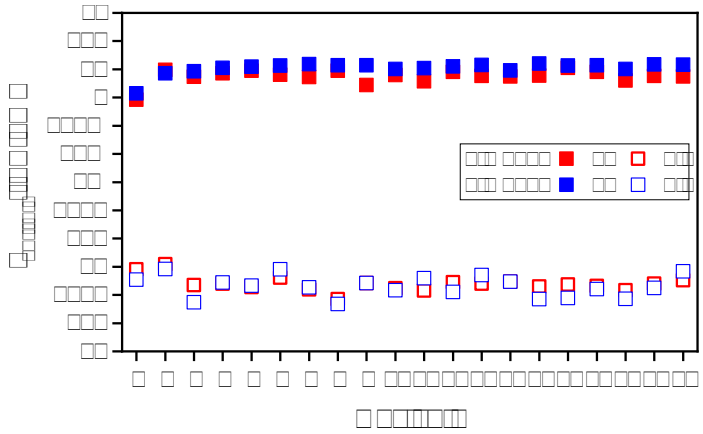


Figure 4.10: *on/off-current extraction out of 20 NS-RFETs*

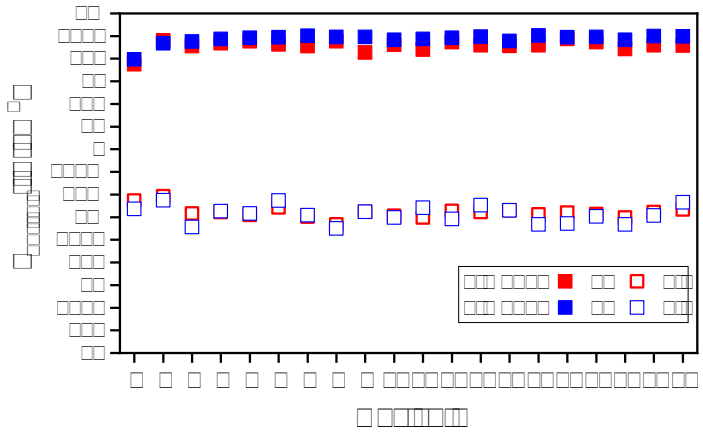


Figure 4.11: *on/off-current density extraction out of 20 NS-RFETs*

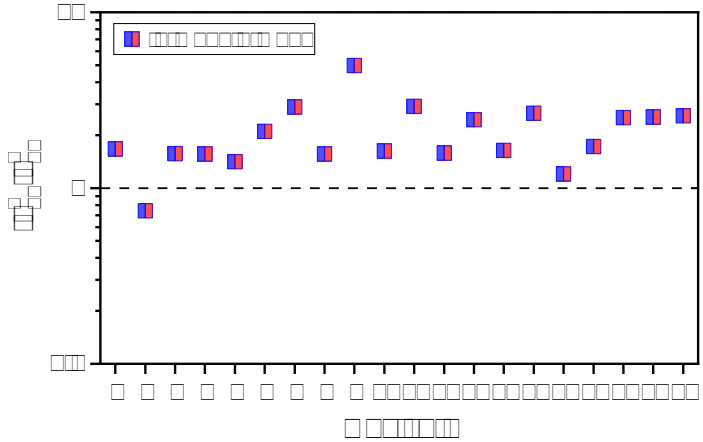


Figure 4.12: *on^p/on^n-current density extraction out of 20 NS-RFETs*

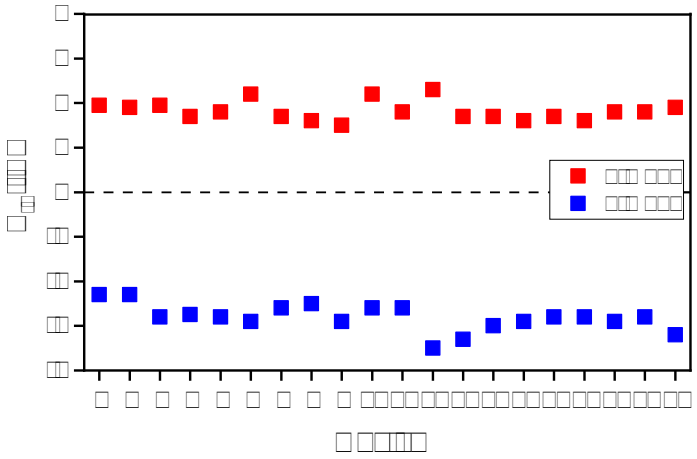


Figure 4.13: *Threshold voltage extraction out of 20 NS-RFETs*

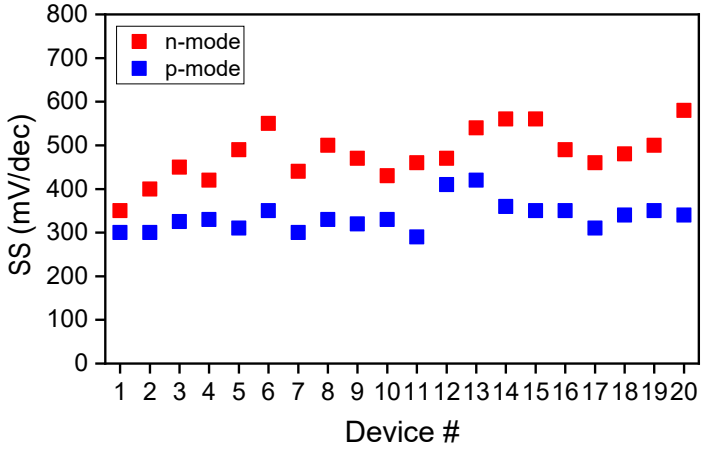


Figure 4.14: *Subthreshold slope extraction out of 20 NS-RFETs*

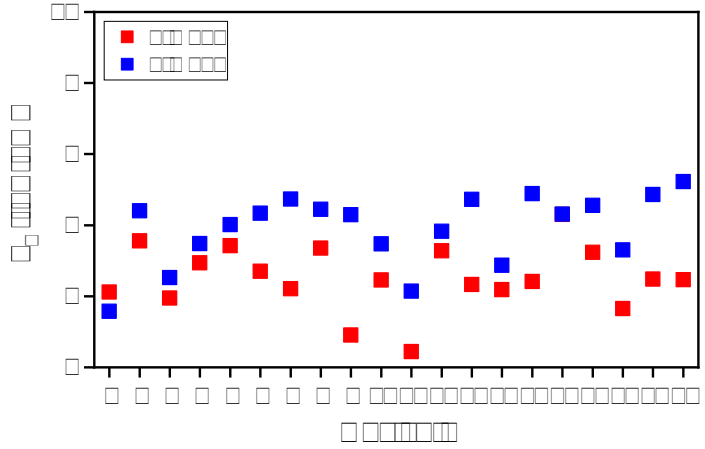


Figure 4.15: *Transconductance extraction out of 20 NS-RFETs*

	μ	σ
I_{on}^{n} $[\mu A]$	2.38	0.93
$I_{on}^{n\star}$ $[\mu A/\mu m]$	6.24	2.41
I_{off}^{n} $[\mu A]$	$1.16{\cdot}10^{-7}$	$1.01{\cdot}10^{-7}$
$I_{off}^{n\star}$ $[\mu A/\mu m]$	$3.05{\cdot}10^{-7}$	$2.65{\cdot}10^{-7}$
I_{on}^{p} $[\mu A]$	4.52	1.42
$I_{on}^{p\star}$ $[\mu A/\mu m]$	11.8	3.43
I_{off}^{p} $[\mu A]$	$1.08{\cdot}10^{-7}$	$8.88{\cdot}10^{-8}$
$I_{off}^{p\star}$ $[\mu A/\mu m]$	$2.86{\cdot}10^{-7}$	$2.43{\cdot}10^{-7}$
J_{on}^{n} $[kA/cm^2]$	41.63	16.1
J_{off}^{n} $[kA/cm^2]$	$2.03{\cdot}10^{-6}$	$1.77{\cdot}10^{-6}$
J_{on}^{p} $[kA/cm^2]$	78.73	22.86
J_{off}^{p} $[kA/cm^2]$	$1.91{\cdot}10^{-6}$	$1.62{\cdot}10^{-6}$
J_{on}^{p} / J_{on}^{n} [1]	1.9	0.9
V_{th}^{n} $[V]$	1.82	0.21
V_{th}^{p} $[V]$	-2.81	0.29
S^{n} $[mV/dec]$	480	58.58
S^{p} $[mV/dec]$	335.7	33.84
gm^{n} $[\mu S/\mu m]$	2.52	0.9
gm^{p} $[\mu S/\mu m]$	3.89	0.99
$Hysterises^{n}$ $[V]$	0.11786	0.0374
$Hysterises^{p}$ $[V]$	0.11786	0.08981

Table 4.1: *Overview of the mean values (μ) and their corresponding standard deviations (σ) extracted from a sample of twenty TTG-RFET devices. Please be aware that the values denoted with an asterisk (*) are relative to the width of the NS ($I^{\star} = I/Width$).*

4.2.4 Multi-CG RFET

The SEM images in figure 4.16a & d illustrate the implementation of a multi-CG RFET for a wired-AND gate with two and three inputs, respectively. The channel width in both structures is approximately equal. Significantly, the utilization of this concept allows for the expansion of input quantities in order to achieve multi-input logic cells, with the limitation being the higher resistance of long channel RFETs, resulting in a reduction of the drive current. These gates are designed by dividing the control gate (CG) into two and three separate gate electrodes. This configuration allows for the creation of additional energy barriers, which ensure that the RFET is activated only when a logic low signal

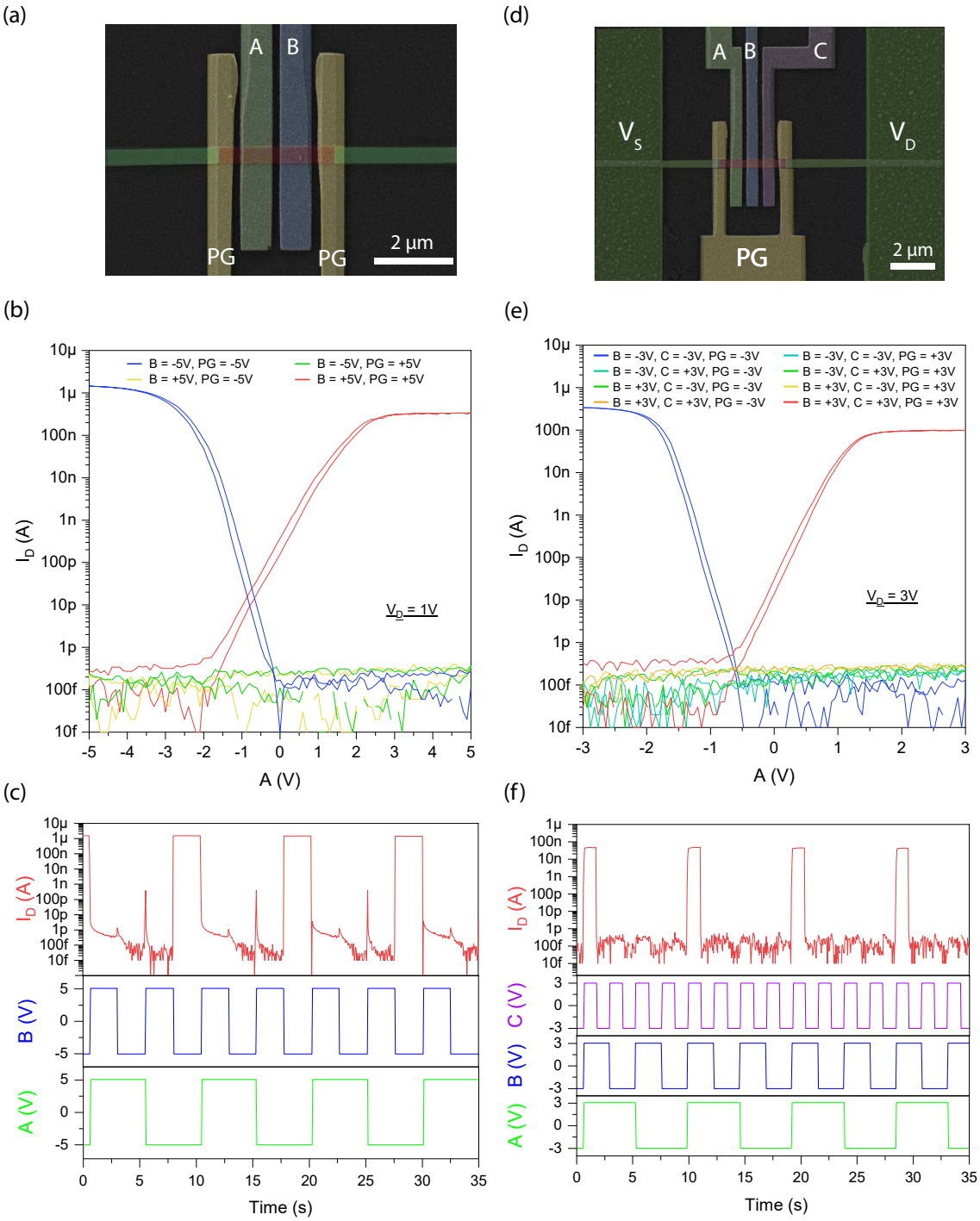


Figure 4.16: *(a) Colored SEM-image (b) transfer characteristic and (c) transient characteristic of a fourfold wired-AND (4TG). In (d) a colored SEM-image (b) transfer characteristic and (c) transient characteristic of a fivefold wired-AND (5TG). Input levels A, B and C*

is applied to both inputs of the two-input wired AND gate, and a logic high signal is applied to all inputs of the three-input wired AND gate. In the present scenario, the supply voltages V_D and V_S were selected as 3 V and -3 V, respectively. By alternately adjusting the input signals A, B, and C within a voltage range of ±3 V, a logic gate that requires only a single supply-rail was successfully implemented. Figure 4.16b & e depict the transfer characteristics of the wired-ANDs which exhibit a slight leftward shift of the crossing point. Additionally, both ANDs exhibit minimal hysteresis and small off-currents.

For the transient operation of the two and three input wired-AND gates, the inputs A, B, and C were coupled to square wave signals with frequencies of 0.1 Hz, 0.2 Hz, and 0.4 Hz respectively, the measurements were depicted in figure 4.16c & f. Upon examination of the transient trace of the output current I_{DD}, it is evident that the device effectively suppresses the current in the off-state. This suppression is achieved to a level that is below the noise floor of our measurement system. Furthermore, the device maintains on-currents of approximately 1.8 μA for the 4TG and 42 nA for the 5TG, respectively. As a result, the on/off ratio exceeds several orders of magnitude in both cases. The dissimilarity in the on-currents can be attributed to the utilization of distinct modes, specifically n-mode for the two-wired AND and p-mode for the three-wired AND. Additionally the segment lengths of the NS structures is different, so in fact a meaningful comparison in terms of the on-states cant be given. Significantly, by applying a voltage of V_{PG} = -3 V, thereby operating the RFET in p-mode, the flow of current through the device would only occur when a voltage of -3 V is applied to all inputs. The proposed RFET based wired-AND offers therefore an additional advantage by providing circuit and layout designers with a significant level of flexibility.

4.3 Logic Gates

After evaluating the RFET as a single device in terms of its electrical properties in the previous section and demonstrating that NS-based RFETs, without extra doping or stress introduction, have a reasonably good symmetric behavior with regard to the on-currents as well as other parameters like the threshold voltages, the subthreshold slopes are generally stable over numerous devices, and moreover, that a reconfiguration from p-type to n-typ and vice versa works safely without affecting functionality the step is paved to implement this reconfigurable feature on the device level also on the circuit level to create even more synergies and to become more efficient in general. A significant factor in this situation is that no additional supply voltages should be required for circuit implementation to enable the reconfiguration, which is especially crucial in circuit technology for design aspects.

4.3.1 Inverter

The above described well balanced performance of p- and n-type operation makes these devices suitable for application in electronic circuits. First, an inverter was considered, as it is the most fundamental logic gate in digital integrated circuits. Expected to give their complementary behavior, the inverter was fabricated using a pair of RFETs, of which one

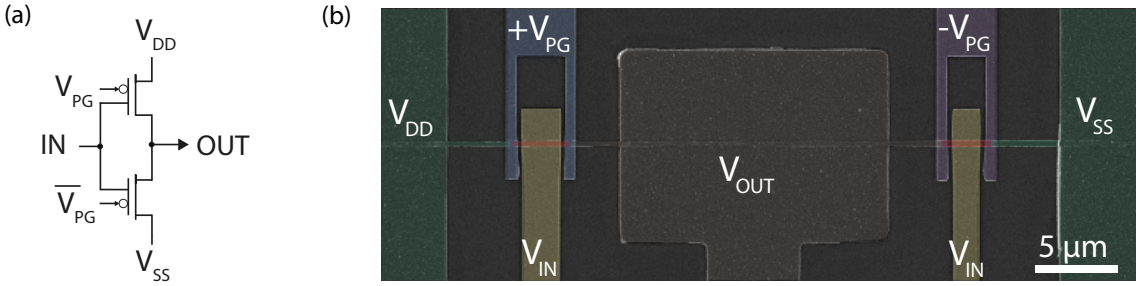


Figure 4.17: *Two RFETs with TTG structure were connected to build an inverter. The polarity gates (PG) are biased to form an inverter similar to CMOS, with a p-type and n-type transistor. In (a) the circuit layout and (b) shows a colored SEM image of the fabricated structure on a single nanosheet (NS).*

acts as a p-type and the other as an n-type, from a single long Si-NS, the Si beneath the Al output contact has been completely exchanged, resulting in two regions of Si channel surrounded by three gates each. Figure 4.17a and 4.17b depict the schematic diagram and a colored scanning electron microscopy (SEM) image, respectively. The Si channel is highlighted in red, covered by the PGs, which are biased the opposite way, positive V_{PG} for p-type and negative V_{PG} for n-type and the CGs, which are connected and carry the input signal V_{IN}. It is worth noting that even with perfectly balanced voltage levels for all input, output, and supply voltages, the devices that have been described are still able to perform their intended functions. That is, if V_{DD}=2 V is indicated in the following, V_{SS}=-2 V is then applied, resulting in a voltage swing of ΔV=4 V, this also applies to the Input high and low levels. The ability to run the whole circuit with only two levels is critical since it considerably simplifies the circuit construction by eliminating the requirement for extra supply voltages.

The inverter transfer characteristics were measured at various supply voltages between 2.5 V and 1 V, however, for clarity, only the curve at V_{DD}=2 V are shown in figure 4.18a, which exhibits complete logic full swing for the applied bias, but applies equally to all supply voltages. The switching occurs at about $V_{DS}/2$, which is a need for complementary implementations at low bias, i.e. with low operating power. Moreover, as can be seen from the figure, the current only flows during switching, which greatly decreases the overall energy consumption during operation, for V_{DD}=2 V its maximum value is I_D=194.2 nA. In figure 4.18b, voltage gains ($|dV_{OUT}/dV_{IN}|$) are calculated for a variety of supply voltages, and the results are displayed as a function of V_{IN}. The maximum voltage gain is always greater than 5, and it may reach up to 16 when the supply voltage is just 1.5 volts, fulfilling the requirement for logic application and is evidence of their potential uses in low operating voltage circuits, since this structure can be optimized further regarding the dielectric. When just voltage gain is considered, the inverter performs substantially better at low bias than at high supply voltage. Moreover, oscillations are noticed in the transition zone at a high supply voltage of 2.5 V, spreading the voltage gain region and lowering the maximum gain. When the inverter is supplied with low voltages, the transfer

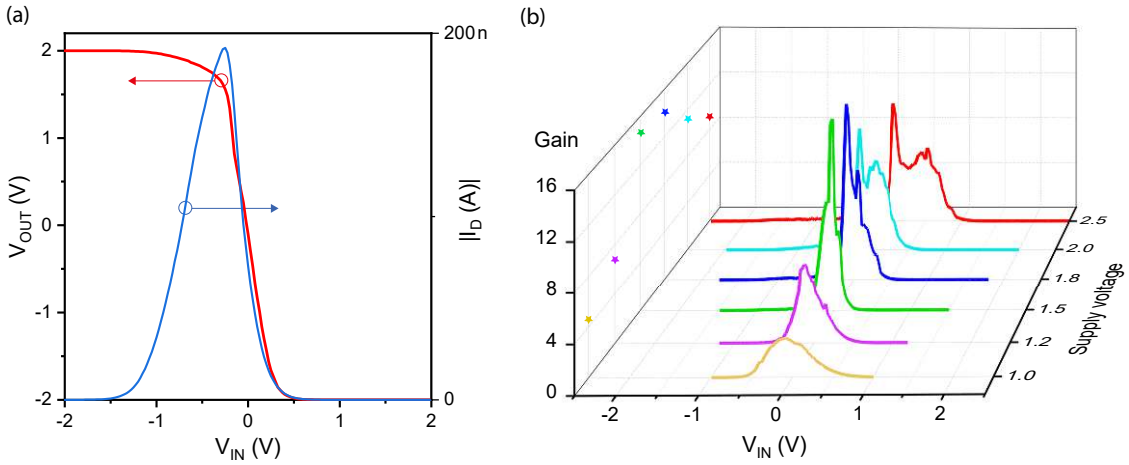


Figure 4.18: *(a) Shows the voltage transfer characteristics for $V_{IN} = 2V$ with a full swing output and the switching current at V_{DD}. (b) depicts the input V_{IN} dependent voltage gain under different supply voltages V_{DD} but note that the x-axis only covers the value range from -1 to 1, i.e. the range where the switching takes place, in order to visualize the gain characteristics more clearly.*

curves get sharper in the transition zone, resulting in a more abrupt transition region and consequently a bigger voltage gain than when the inverter is biased stronger. The oscillations can be attributed to dynamics of carriers in the Si channel that tune into and out of charge traps in the surrounding dielectric layer. This carrier dynamics can instantly modify the electrostatic potential of the channel and cause random variations in the transport characteristics. The kinetic energy of carriers in the channel grows with supply voltage, and the likelihood that carriers may tunnel into or out of a charge trap increases with gate voltage and drain voltage. As a result, fluctuations tend to develop at high supply voltages over low supply voltages. Hence, the scaled supply voltage can result in reduced electrical noise in logic gates.

In figure 4.19 the noise margin (NM) is shown, which is one of the most important considerations evaluating inverters for their robustness, and it may ultimately be used to establish the lowest acceptable supply voltage [21]. Because the standard techniques for extracting noise margin that appear in some textbooks do not give reliable values for a wide range of transfer characteristics, especially non ideal ones, the well developed area technique is more suitable to give reliable noise margin values for inverter and is one of the convenient ways to determine the noise margin range and has been used several times in the past for the analysis of complementary inverter characterization [12]. To quantify the noise margin, butterfly form transfer curves were created by simulating two back to back linked inverters, i.e. transfer curves with swapped V_{IN}-V_{OUT} (semi-transparent color) were added to the original ones (solid colors), as illustrated in figure 4.19a. The easiest technique to characterize noise margin is to maximize the size of a rectangle that fits between the inverter transfer curve and the mirrored inverter curve, and then find the inverters reliable noise margin values, regarding to the same figure. The noise margin, denoted by $NM_H = |V_{OH}$ - $V_{IH}|$ for logical high, is the tolerance range within which a

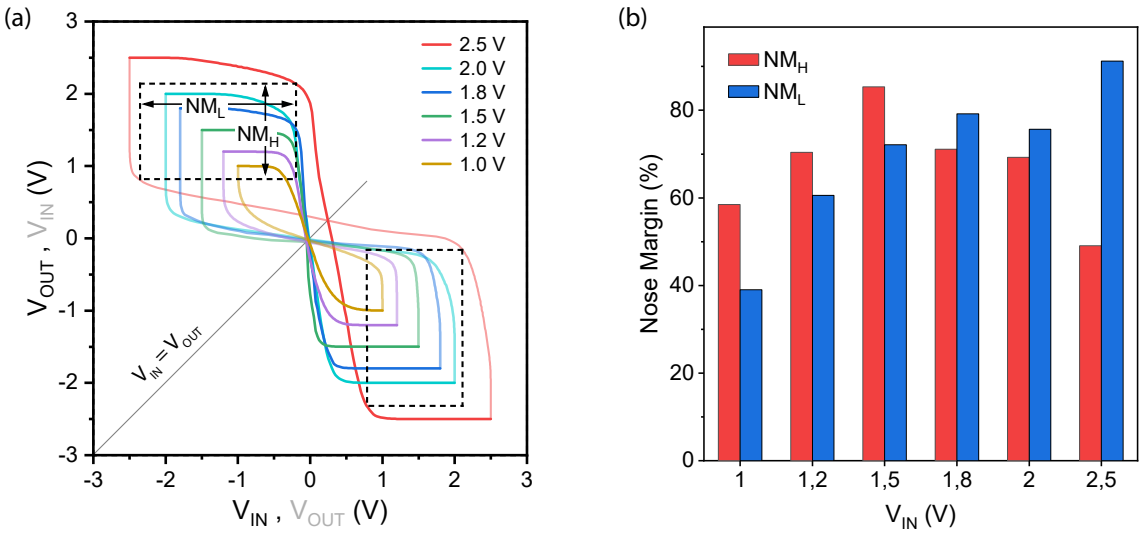


Figure 4.19: *Determination of the noise margin of the inverter. (a) illustrates the transfer characteristics at different V_{DD} with V_{IN} and V_{OUT} plotted interchangeably on x and y axis resulting in the butterfly shape. The maximum possible matching rectangle inside the transfer curve loop is sketched for $V_{DD} = 2V$. (b) shows the calculated noise margin low (NM_L) and noise margin high (NM_H) related to the particular V_{DD}.*

logical high signal may still be accurately received. The same holds true for noise margin, NM_L = |V_{IL} - V_{OL}|, which sets the tolerance range for logical low signals. V_{OH} and V_{OL} represent the highest and lowest output voltages, V_{IH} and V_{IL} the higher and lower input voltages at which the voltage gain of the transfer curve equals -1. Hence, low noise margins indicate circuits which are more sensitive to noise. In figure 4.19b the relative noise margins based on the supply voltage, i.e. noise margins normalized by the supply voltage, are depict. For supply voltages ranging from 1.2 V to 2 V, the inverter exhibits similar noise margin low (NM_L) and noise margin high (NM_H). For example, with a supply voltage of 1.8V, the inverter exhibits a NM_L=1.43 V and NM_H=1.29 V, which corresponds to 72% and 80% of their theoretical maximum of $V_{DD}/2$. A noise margin of 72-80% from the highest theoretical value is an impressive result, and is far above the required minimum value necessary for proper circuit functionality [20], indicating the inverters great resilience against unavoidable transistor parameter fluctuations and electrical noise and therefore the inverters potential for integration into more sophisticated circuit configurations. Remarkably, the inverter characteristic can be observed despite the fact that the supply voltage for V_{DD}=1 V is not even high enough to turn the transistors on, as stated in the previous section. This phenomenon can be attributed to the subthreshold operation of the transistors as the subthreshold currents are sufficient to switch the gate between logic low and logic high levels and offer enough gain to get acceptable transfer characteristics.

The inverters dynamic behavior was also investigated. Figure 4.20a depict the time dependent V_{OUT} of an inverter at a V_{DD}=2 V and a square wave V_{IN} of a frequency f=1Hz,

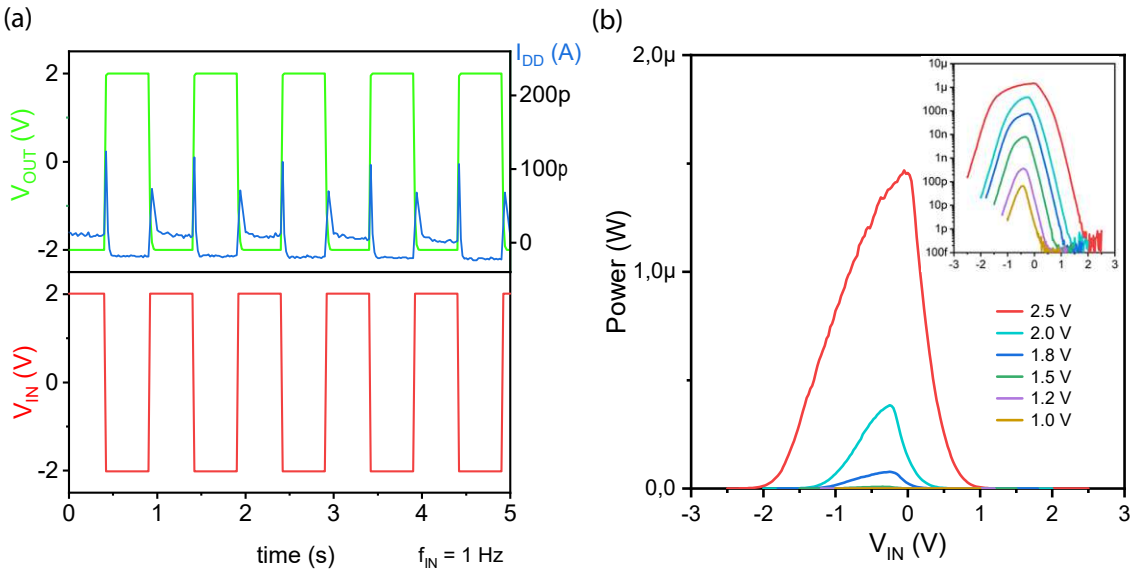


Figure 4.20: *Dynamic switching behavior and power consumption of an inverter. (a) Time dependent V_{OUT} at V_{DD} of 2V driven by square wave V_{IN} with frequency of $f_{IN} = 1Hz$. Logic switching behavior is clearly visible with sharp transition, the current flowing in the circuit is also indicated. (b) shows the power consumption characteristics of the inverter as a function of the input voltage for various V_{DD}. It is obervable from the inset, that as the voltage falls, the power declines disproportionately up to the picowatt range.*

with the input square waves peak and low values of 2V and -2 V, respectively. A negative voltage level (-2 V) is consequently regarded as a logic '0', while positive voltages (2 V) are considered as a logic '1'. As a result, the RFET based inverter delivers full output voltage swing while maintaining a low current flow, with modest peaks in the region of 100 pA only when switching the output stage, as is customary for a complimentary circuit design. At 1 Hz a logical switching behavior is shown, which should also be maintained for higher frequencies. However, the measurements carried out show that at higher frequencies the output cannot quite follow the input, which is certainly due to the measurement setup and overlap capacitive loads.

Figure 4.20b depicts the inverters power consumption (P=V_{DD} x I_{DD}) characteristics. Peak power consumption of nearly 1.5 μW is reached for V_{DD}=2.5 V. Clearly, the transient current is drastically reduced when the supply voltage is decreased. At the transition zone, the transient current achieves its maximum value and is subsequently referred to as the switching current. Hence, the majority of power is dissipated while charging and discharging, so the switching current is an excellent measure for determining the static power dissipation of a circuit [55, 77]. It is important to note that when the supply voltage is reduced from 2.5 V to 1.8 V, the switching current drops by more than one order of magnitude, resulting in a significant reduction in power dissipation from 1.5 μW to a value less than 100 nW that can be accomplished by reducing the supply voltage, as shown in the inset of figure 4.20b, note that the y-axis is logarithmic, while the outer y-axis is in linear

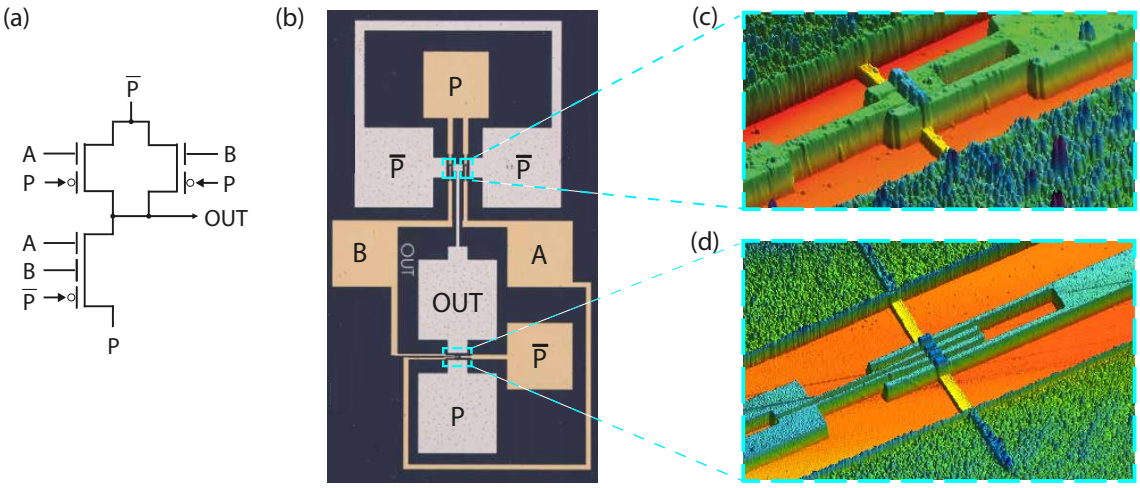


Figure 4.21: *(a) Schematic of the NAND/NOR circuit based on RFETs (b) Microscope image of the realized NAND/NOR gate with A, B representing the inputs applied to the CGs of the RFETs, while P and $\bar{P}$ (on the golden pads) represents the PGs and is powered by V_{DD} respectively V_{SS}, whereas P, $\bar{P}$ and OUT (on the silvery pads) are the source and drain contacts of the RFETs, respectively. The highlighted regions, i.e. the channel area are shown as captured AFM images on the right - in (c) a TTG, which occurs two times in the design and in (d) a wired-2AND.*

representation. This may be reduced even more to 0.3 nW by lowering the supply voltage to 1.2 V, while the noise margin values are still good NM_L=0.73 V (61%) and NM_H=0.85 V (71%) and relatively symmetrical. The static power consumption is significantly less than these values and is thus insignificant for both the '1' and '0' logical states. This low power consumption can be safely attributed to the improved cut off capability of the RFET in both operation modes.

4.3.2 NAND/NOR-Gate

The RFETs decisive advantage in terms of functionality is most readily seen when there is a rise in the overall level of complexity inside the circuit. In CMOS, a NAND gate typically consists of a parallel connection of two p-type transistors and a series connection of two n-type transistors, while another complementary gate, the NOR gate, consists of two n-type transistors connected in parallel and two n-type transistors connected in series, see 2.19 in 2.3.2. Therefore, from a purely conceptual point of view, both circuits are identical, only the roles of the n-type and p-type transistors are simply reversed, i.e. a symmetry relationship is given. As shown in figure 4.21a, it is possible to construct this circuit using 3 RFETs that have been properly designed.

In classical integrated circuits, the implementation of a NAND/NOR functional gate necessitates an extra selection element for the required function, which is achieved by integration of additional number of transistors, generally often realized using multiplexers. So, in the case of the NAND/NOR gate realized with RFETs, a preselection is made by selective

control of the ports, which eliminates the need for switching actions and therefore allows the integration of the multiplexer to be omitted, saving the transistors employed. This demonstrates that, as circuit complexity increases, the benefits of RFETs are gaining importance. Figure 4.21b depicts a picture of the fabricated circuit as seen via a microscope, including the designations of the respective pads. In this depicted pinout, the circuit has a NAND behavior, but can be converted to a NOR behavior using the polarity of the signal P and its inverted signal $\bar{P}$ by simply inverting the levels. Just two levels are required since P and $\bar{P}$, which are the PGs of the RFETs, are linked to the supply voltages at the source V_{SS} and the drain V_{DD}. The flow across the channel is determined by the input signals A and B, which are linked to the CGs of the RFETs and decide whether the channel is open or closed. It should be noted that this circuit is also fabricated in a single cycle on a substrate, with no further wiring necessary for functionality and electrical evaluation afterwards, which is advantageous in terms of external sources of interference and becomes more industrially relevant. The upper transistors have a TTG structure, while the lower transistor has a wired-2AND structure, i.e. an additional CG compared to the RFETs, which means that 2 transistors in series connection can be reduced to one transistor, compare reference which is another aspect of this proposed RFET architecture to replace numerous transistors with multiple gates, which helps to minimize the number of transistors in the circuit as well.

In 4.21c-d, the relevant structures, respectively the region around the channels are shown in the AFM image, with the extra CG in the lower one. It is worth noting that, in principle, there are no restrictions to the number of possible CGs as long as they are electrostatically decoupled from each other, and therefore more degrees of freedom are provided in designing circuits.

This experimentally demonstrated NAND/NOR gate circuit based on RFETs is also referred as polymorphic gate since it is a reconfigurable component capable of performing many logic functions. When V_{DD} is adjusted to a high level (in this example to positive voltages), the top two transistors operate in p-mode and act as the pull-up network, while the bottom transistor works in n-mode and acts as the pull-down network, thus the polymorphic gate therefore operates as NAND gate. When P is inverted, V_{DD} and GND, p-FETs and n-FETs, as well as the pull-up and pull-down networks, are exchanged, converting the circuit to a NOR gate. Figure 4.22 depicts the experimental output voltages of the NAND and the NOR gate as a function of inputs A and B, where a voltage level of 2.5 V was applied, i.e. all occurring values of P, $\bar{P}$, B exhibit the constant values of $\pm$ 2.5 V. The measurements are carried out at room temperature (295 K) and the input A is accordingly swept from +2.5 V to -2.5 V in equidistant intervals of 25 mV and back throughout the double measurement, the directions are indicated by the respective arrows in the figure.

The results are highly encouraging since the transfer characteristic has almost none (NAND gate in 4.22a) or very little (NOR in 4.22b) hysteresis. Moreover, in the case of the NAND

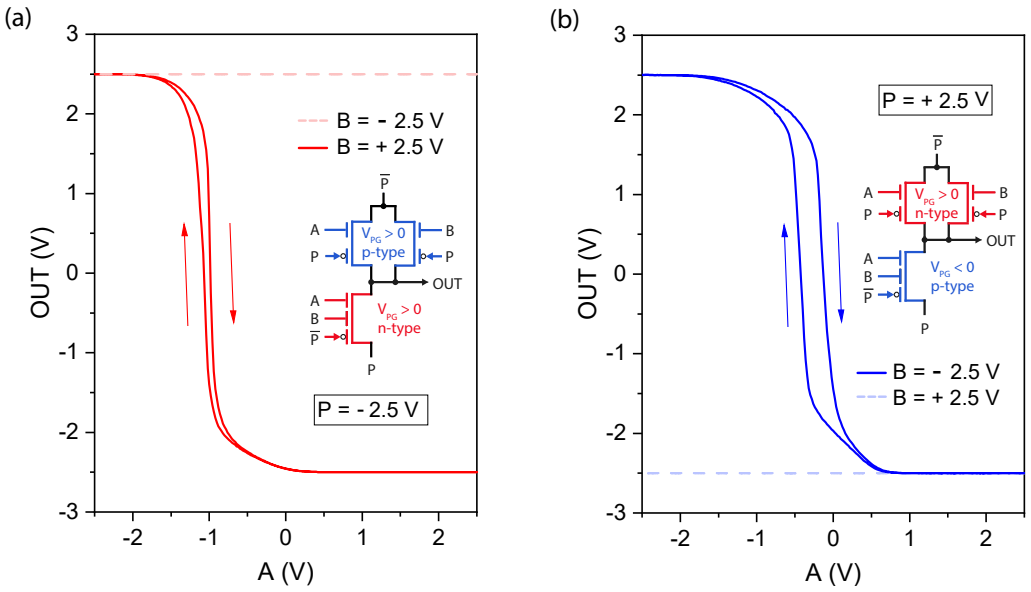


Figure 4.22: *Measured transfer characteristics of the experimental polymorphic gate (a) in the NAND and (b) NOR configurations as a function of inputs A and B at symmetry supply voltages $V_{DD} = 2.5$ V and $V_{SS} = 2.5$ V, respectively P and $\bar{P}$, showing the reconfigurability on circuit level. The insets depict the current transistor configuration in the circuit for each gate.*

gate, the switching is slightly shifted to negative voltages, whereas in the case of the NOR gate, the switching is quite precisely centered, presumably due to slight asymmetries in the fabrication of the three transistors used but this has no effect on the functionality. However, this can be improved by optimizing the process flow so that these switching occur exactly at zero point but most importantly, a smooth full swing occurs at the output with no substantial perturbations in the characteristic.

The following illustrates how the various functionalities can be distinguished. If P is low (-2.5 V), i.e. the whole circuit is programmed as NAND and assuming the inputs A and B are also low, the output is high (+2.5 V), if A is swept to high the output remains high, indicated by the dashed transparent red line in figure 4.22a. If now the input B is set high and A is low, then the output remains high, whereas now when sweeping the input A to high the output switches to low, indicated by the solid red line in the same figure and thus the full range of functions of the NAND circuit is provided. The inset reveals which transistors are working under these voltage levels in n-mode (colored red) and p mode (colored blue). Changing the constant voltage level applied on P to high, the circuit becomes a NOR gate. The outputs result in the same way as described before, if the inputs A and B are high, the output is low, if A is sweeped to low, the output remains low, indicated by the dashed transparent blue line in figure 4.22b. If the input B is set low and A is high, then the output remains low, whereas now when sweeping the input A to low, the output switches to high, indicated by the solid blue line in the same figure and thus the NOR behavior is proven. Again, the inset indicates which transistors run in n-mode (colored red) and p-mode (colored blue) under these mentioned voltage levels,

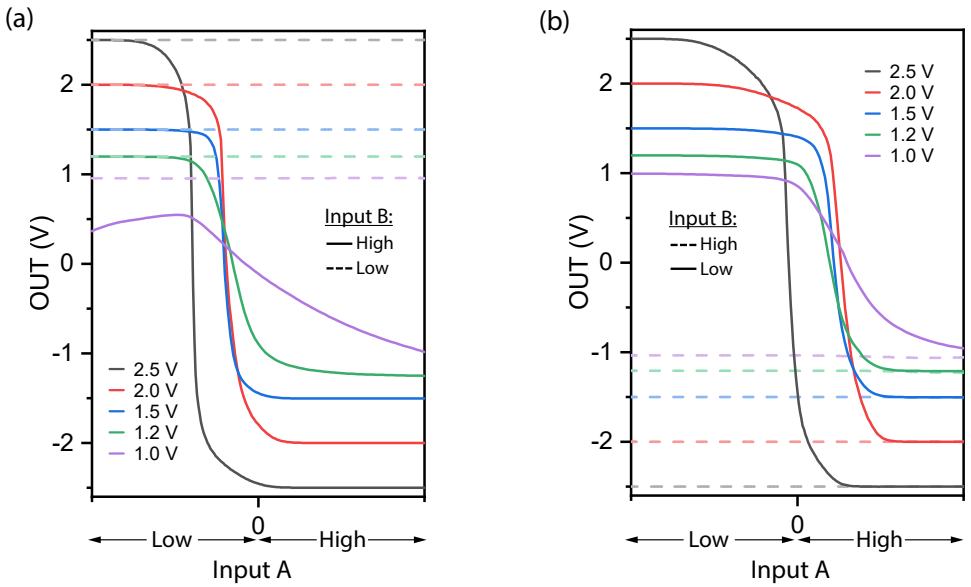


Figure 4.23: *Transfer characteristics at different supply voltages as a function of input A and B for (a) NAND gate and (b) the NOR gate.*

and it is instantly clear that the p-type transistors have become n-type transistors and vice versa in the same circuit configuration.

Figure 4.23a-b depicts again the experimental output voltages of the NAND and the NOR gate as a function of inputs A and B bit at various supply voltages this time, ranging from 1 V to 2.5 V in a single measurement, whereby two things are observable. On the one hand, the switching points for NAND and NOR for voltages smaller than 2.5 V are shifted to the right, i.e. to more positive voltages, in comparison to the 2.5 V curve viewed in the previous figure and corresponds to the black curves in this figure. This means that in the case of the NAND gate, the switching action slips clearly to the zero point, while in the case of the NOR gate, it is shifted slightly away from the zero point. However, all voltages have roughly the same switching point, with the exception of the 2.5 V curve mentioned. Second, for all voltages except the smallest, 1.0 V, a complete output swing occurs, and the high and low values are quickly attained. Nevertheless, at 1.0 V, the slope in the switching range is substantially flatter and thus the output does not manage to follow the input completely.

Remarkable that the inverter examined first in 4.3.1 exhibited exactly the same behavior, the 2.5 V curve was also shifted in its characteristic compared to the other voltages which has exactly the same swichting point, i.e. regardless of the respective circuit, the same voltage level exhibits qualitatively the same behavior, which is of great importance in terms of reproducibility and reliability.

In figure 4.24 color maps are presented to further highlight the stability of the these

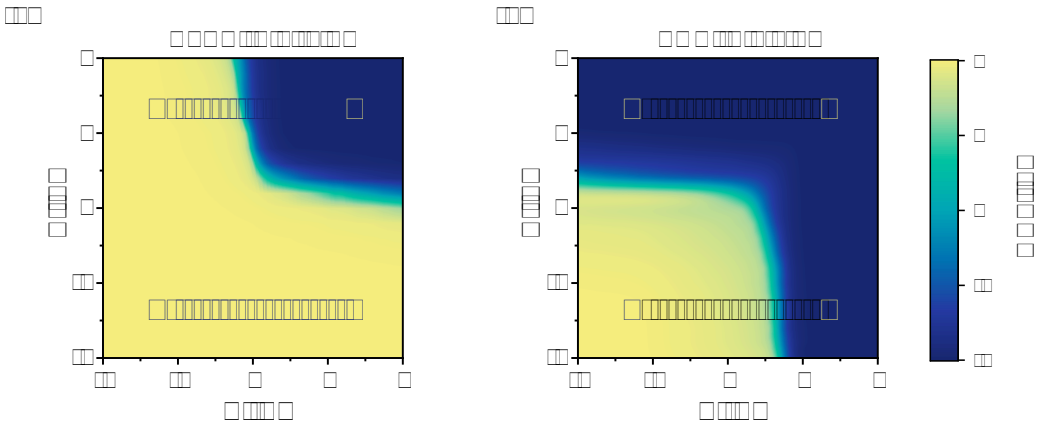


Figure 4.24: *Output voltages illustrated as color maps in (a) for the NAND gate and (b) for the NOR gate as a function of inputs A and B showing the switching operation.*

presented RFET based circuits, displaying the output voltage in relation to the voltages at the inputs A, B, and the supply voltage P. Because the polarity gates and the supply ports are coupled, fluctuations in V_{DD}, respectively V_{SS} are anticipated to have an influence on the RFETs V_{PG}, which may be expected to affect the operation of the gates. The results show that the gates are resistant to supply fluctuations since either mode in each gate can give outputs distinguishing between two distinct logic states. It is remarkable that the output keeps a highly constant value of 2V throughout a broad range of input voltages, resulting in a very robust functioning against input voltage variations as well as noise sources, which makes the circuit extremely resistant against these type of interferences.

When a third input is attached to P, the logic gate performs as a MIN gate, therefore increasing its functionality by switching between NAND and NOR and thus demonstrating the dynamic reconfiguration of the polymorphic gate. Figure 4.25 demonstrates the full swing behavior of this MIN gate at operating voltages of 2 V, with highly abrupt transitions between the logical output states for both NAND and NOR operation. Notably, the currents I_{DD} at the steady output states reveal values as low as 0.2 nA and 6 nA for both types, and only significant current is flowing during switching the output with peaks of up to 0.35 μA in the NAND mode and 0.8 μA in the NOR mode.

Further, figure 4.26a depicts the dynamic switching behavior of the gates, which illustrate the time dependent V_{OUT} of the MIN gate for voltage levels of $\pm$ 2 V, driven by square waves A, B, and P with various frequencies. It can be seen that during the first cycle of the inputs A and B, the gate is set as NAND, and the output is switched correspondingly, as can be read from the truth table in figure 4.26b. If P is set to high, which corresponds to the second cycle of the inputs, the circuit is reprogrammed to NOR and the outputs are adjusted correspondingly. This means, the polymorphic gates dynamic reconfigurability from NAND to NOR operation is observed, permitting the operation of a MIN gate, and is therefore offered in addition to dependable switching operation inside a single logical configuration. At these illustrated frequencies, logic switching behavior is obvious and

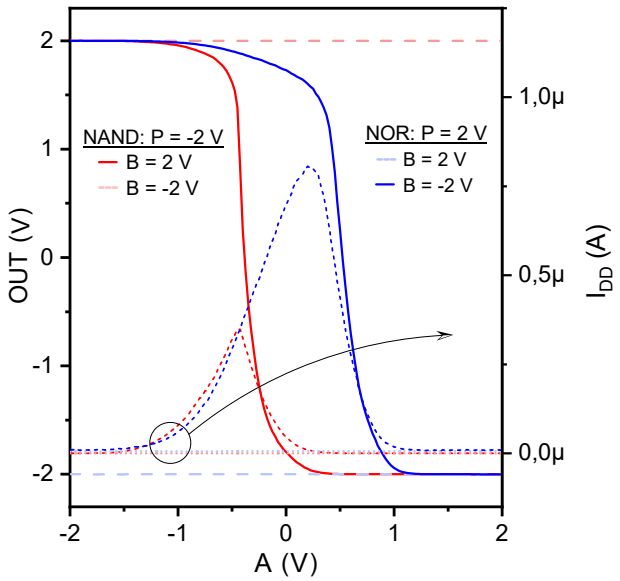
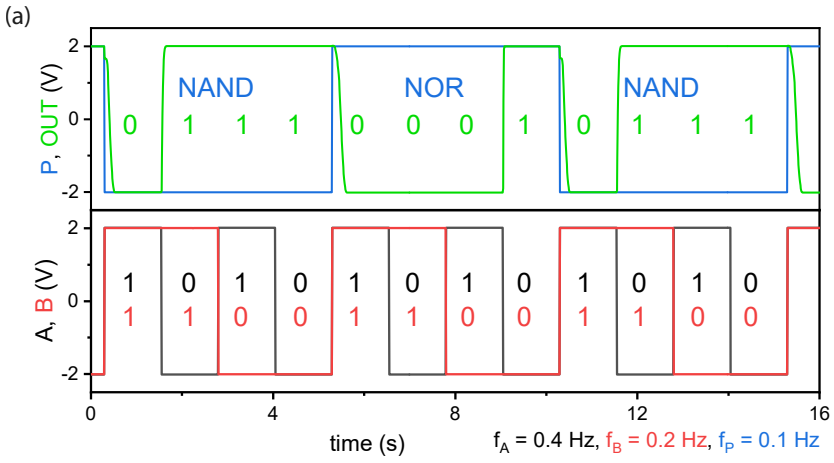


Figure 4.25: *Transfer characteristic of the MIN3 gate, either for NAND and for NOR operation and the corresponding currents (dashed curves) occurring during switching the output depicted by the right axis.*

should be noticed at higher frequencies as well.

The switching action from NAND to NOR and vice versa, can also be seen in figure 4.27. Here the behavior is seen when P is swept from -2 V to +2 V, the input A is also swept in this range, and B is set to constant levels of once -2 V and once +2 V. It can also be stated that input A is in responsible of switching the output within the respective gate, whereas P is responsible of switching between NAND and NOR. Because P regulates not



A	B	P	OUT		
0	0	0	1	NAND	MINORITY-GATE
1	0	0	1		
0	1	0	1		
1	1	0	0		
0	0	1	1	NOR	
1	0	1	0		
0	1	1	0		
1	1	1	0		

Figure 4.26: *(a) Dynamic switching response of the MIN gate to square waves on the inputs A, B and the polarity P and in (b) the corresponding truth table. With P on low ('0') or high ('1') toggling between NAND and NOR is possible.*

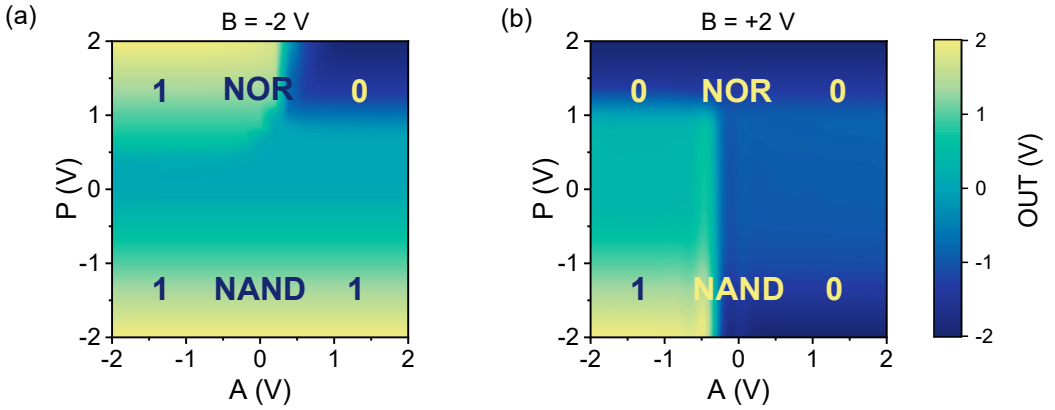


Figure 4.27: *Color maps depicting the polymorphic behaviour of the presented logic gate. The output voltages are shown in (a) for B at low level and in (b) for B at high level*

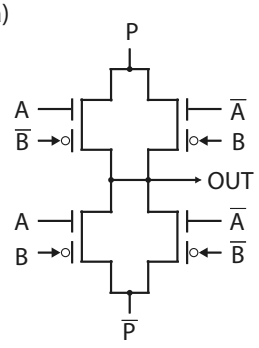
just the voltage on the PGs but also the bias voltage of the circuit, the transition between NAND and NOR operation is not as sharp and clear as switching between specific states within the gates. As stated previously, slight variations in the voltage level at P have a direct effect on the output level and is consistent with the previous observations.

4.3.3 XOR/XNOR-Gate

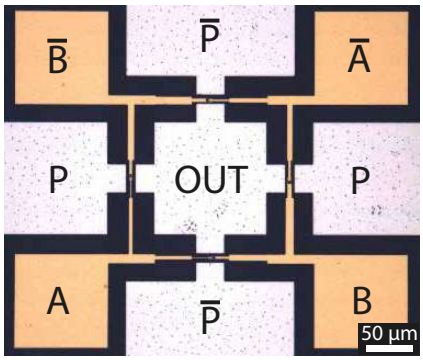
RFETs have the potential to enable the realization of highly advanced logical circuits, including the XOR/XNOR gates. These gates are challenging to implement using conventional CMOS technology. When examining a two-input XOR logical gate, where A and B are the input signals, figure 4.28b displays a microscopic image of the constructed structure consisting of four separate triple-top gate RFETs. Based on the circuit depicted in figure 4.28a, the PGs and CGs are linked to either the signals A and B, or their respective inverted signals $\bar{A}$ and $\bar{B}$. Furthermore, the drain and source pads are connected to the P and $\bar{P}$, and the output OUT components. Since the XOR/XNOR logic gates provide output logic values that are diametrically opposed to one another, the top and bottom networks each have different program configurations. When comparing XOR gates implemented with conventional transistors to those implemented with RFETs, it is observed that the latter can effectively reduce the number of transistors by 50%. This reduction leads to improved path delays and decreased power consumption as the quantity of inputs escalates, the aforementioned advantages become increasingly substantial.[41, 68] It is worth noting that the XOR/XNOR layout exhibits complete symmetry when compared to the NAND/NOR layout figure 4.21a, and that could potentially advantageous for applications requiring a large number of XOR functions.

Furthermore, owing to the adaptable characteristics of RFETs, the entire circuit can be inverted by utilizing the polarity input P, thereby enhancing functionality beyond that of CMOS. Therefore, this circuit has the capability to transition between XOR and XNOR modes dynamically on runtime by adjusting the voltage of P to positive or negative values, correspondingly. By applying fully symmetric operation voltages of ± 2 V the function

(a)



(b)



(c)

A	B	P	OUT	
0	0	0	0	XOR
1	0	0	1	
0	1	0	1	
1	1	0	0	
0	0	1	1	XNOR
1	0	1	0	
0	1	1	0	
1	1	1	1	

Figure 4.28: *(a) Schematic of the XOR/XNOR circuit based on four RFETs. In (b) a captured SEM image of the realized XOR/XNOR gate is illustrated, with A and B representing the inputs applied to the CGs and PGs of the RFETs, while whereas P and OUT are the source/drain contacts of the RFETs, powered by V_{DD} respectively V_{SS} and (c) shows the corresponding truth table. This design allows the circuit to be operated either as XOR or XNOR.*

was characterized. A logical high of +2 V and a logical low of -2 V were chosen for this purpose. In accordance with the information presented, Figure 4.29 illustrates the transfer characteristic for both modi of the gate. The output voltage exhibits a complete swing setting the voltages correspondingly. The voltage of the XNOR crosses the threshold of OUT = 0 V at A = -0.11 V and 0.25 V for B = 2 V and -2 V, respectively, while the XOR crosses the threshold of OUT = 0 V at A = -0.12 V and 0.45 V for B = -2 V and 2 V, respectively. Peak switching currents in the range of 700 nA are observed for the XNOR and about 383 nA for the XOR, while the current flow through the circuit is effectively suppressed at the distinct output states, with an I_{DD} value less than $I_{DD} <$ 30 pA. Additionally, it is worth noting that the currents in an XOR/XNOR polymorphic gate exhibits a greater symmetry compared to a NAND/NOR polymorphic gate from the previous considerations, thus suggesting that the XOR/XNOR gate type may offer enhanced resistance against side channel attacks.

Figure 4.30 illustrates the stable transient operation of the XOR-gate. The output voltage OUT transitions to a logic "1" when either input A or B is set to "1". Again, the frequencies for inputs A and B are very low at 0.1 Hz and 0.2 Hz, respectively. At higher frequencies, the output can no longer follow the input signals, but this is not due to the circuitry, but to the existing measuring station, since many unwanted parasitic capacitances has influence on the measurement. Of course, with an appropriate measurement system, this good transient behavior should be observable at many higher frequencies up to the GHz range. Additionally noteworthy, currents only appear at the switching event, which remain in the lower single-digit nA range.

By systematically varying the input voltages and graphing the recorded values using color maps, it becomes possible to make comprehensive evaluations regarding the stability of the device's operation and functionality. This is especially useful in assessing the impact

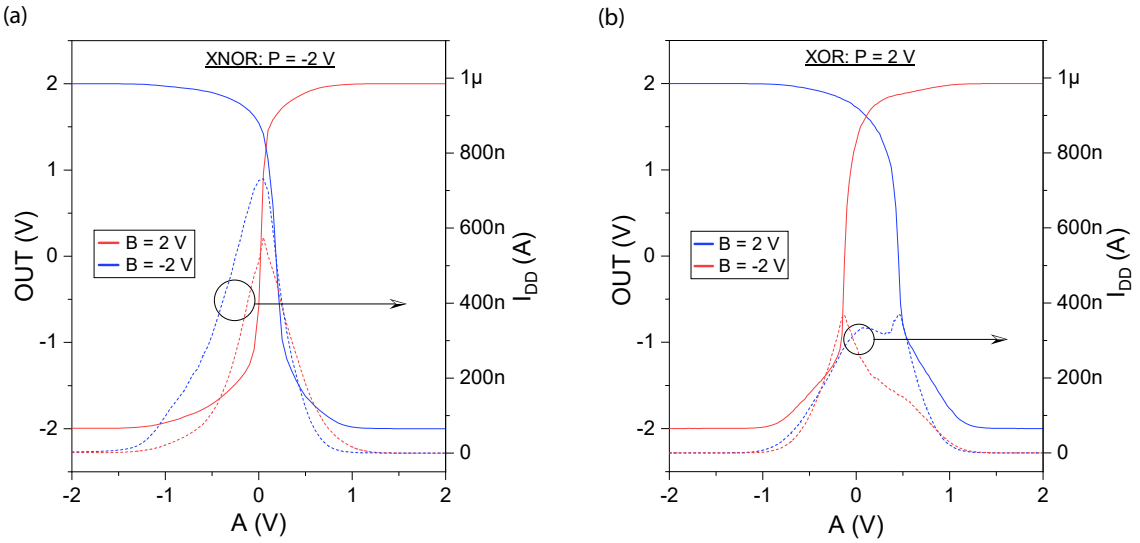


Figure 4.29: *Transfer characteristic and switching currents of the (a) XNOR-gate and (b) XOR-gate at symmetrically voltage levels.*

of voltage fluctuations within the circuit. Hence, figure 4.31 illustrates the output voltage levels obtained by manipulating the applied input voltage levels for an XNOR-gate in subfigure (a) and the XOR-gate in subfigure (b). The value of P is set to -2 V and 2 V for the XNOR and XOR operations, respectively. The reconfigurability of the RFET structures allows the same circuit to demonstrate both stable XNOR and XOR functionality, as evidenced by the four distinct high or low areas in the color maps, which depend on the logic operation and applied input voltage levels, which is quite remarkable considering the stability.

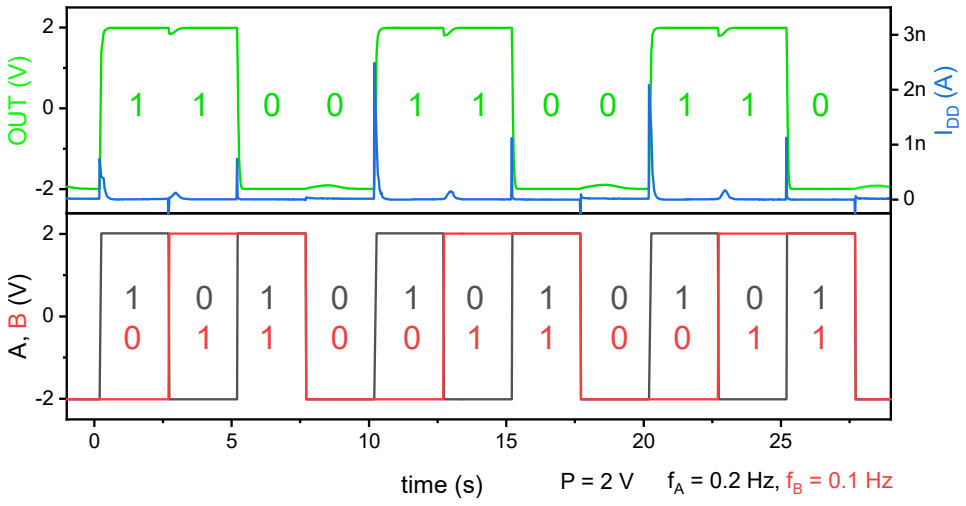


Figure 4.30: *(a) Transient response of the XOR-gate to square waves on the inputs A and B with high and low levels of 2 V and -2 V, respectively, for XOR operation at P = 2 V.*

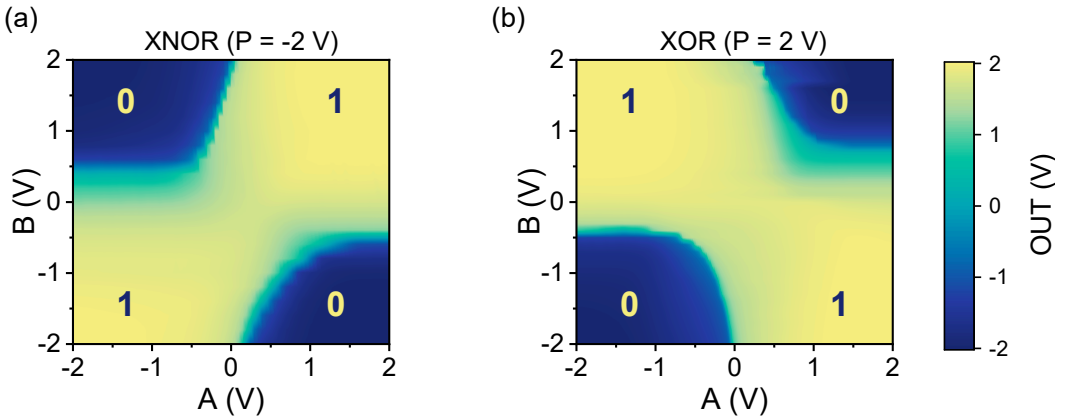


Figure 4.31: *Output voltages as a function of the inputs A and B with sweeping ranges from -2 V to 2 V, illustrated as color maps in (a) for XNOR operation at P = - 2V and in (b) for XOR operation at P = 2 V.*

The combination of inputs yields distinct truth tables in an electrical context, as described above. Please be aware that V_{PG} was also utilized as an input for the RFET. It is worth noting that the same circuit has the capability to exhibit an XNOR truth table by inverting the voltage.

In comparison to CMOS logic circuits, which necessitate the use of more than twenty transistors for the implementation of XNOR and XOR logic gate operations, with RFETs this can be achieved with fewer devices. Additionally, the ability to reconfigure logic operations is facilitated by simple alterations of the electrical signals. Hence, the utilization of these various functions can be expanded to a broader range when extended beyond the individual device level to the circuit level. The capability of logic reconfiguration has then the potential to be utilized as a functional unit in hardware programmable arrays. In the context of an RFET cell array, it is possible to implement combinational logics, such as an adder and a decoder, by just programming the individual cells offering excellent energy efficiency and functionality per chip.

Chapter 5

Summary and Outlook

Due to problems associated with the scaling of conventional transistors, transistor concepts with extended functionality, such as the here studied RFET, are considered as potential candidates to reduce the device complexity of a circuit and to increase its functional space and thus to produce electronic systems more complex, more efficient and more cost-effective and to offer open architecture possibilities for this purpose.

The basic architecture of this RFETs, which incorporates a metal-semiconductor-metal (MSM) heterostructure, is implemented from a Al-Si-Al material system. A silicon-on-insulator (SOI) wafer with a high-quality SiO_2 gate-dielectric and a low trap density obtained by thermal oxidation serves as the foundation for the devices. To achieve precise, consistent, reproducible, and single-elementary crystalline Al contacts, thermally induced diffusion of Al into the semiconducting nanosheet (NS) was performed resulting in two distinct MS transitions along the NS with subsequent exact placement of the omega shaped top gates around the channel. This device then integrates the functionalities of both p-MOSFETs and n-MOSFETs, respectively.

Through careful measurements of the electrical characteristics and different evaluation techniques, it was demonstrated that this RFETs has enhanced electrical properties, including minimal hysteresis, total on/off-current ratios of $1{\cdot}10^8$ with turn-off currents within the measurement limit and a I^p_{on}/I^n_{on} symmetry of 1.9. The current flowing through the RFET in the on-state is primarily influenced by carrier tunneling, while in the off-state, it is predominantly determined by thermionic injection. Decreasing the channel width and/or the gate oxide thickness enhances the tunneling fraction of the currents. The implementation of individually controlled Schottky barriers, along with an additional barrier positioned at the center of the channel, has demonstrated improved effectiveness in reducing off-state currents when compared to single-gate SBFETs. Furthermore, it was demonstrated through implementing ten parallel NS, that there is a notable enhancement

in the on-current I_{on}, while maintaining an acceptably low off-current I_{off}, which holds significance for power intensive electronics. In order to effectively demonstrate the adaptability of these structures, a two-input wired-AND gate and a three-input wired-AND gate was successfully implemented showing excellent dynamic switching abilities.

In contrast to conventional electronics, complementary circuits can be realized with only one type of transistor. For this, RFETs are configured as p- and n-type transistors. This has been demonstrated with this concept in the scope of this work and is the basis for functionally enhanced complementary circuits with ideal switching points. It was demonstrated that these Al-Si-based RFET devices can be used by integrating multiple RFETs into a single circuit layout to achieve reconfigurable combinational multifunctional logic, including an Inverter, NAND/NOR-gate and a XOR/XNOR-gate, ensuring consistent supply and signal voltages as well as a full swing output voltage and thus demonstrating the potential of this approach to design advanced microprocessors with simplified circuits, e.g. a D-latch, full adder and more. By integrating two of this RFETs along one NS, nearly identical devices could be fabricated and interconnected. By utilizing only a pair of distinct potentials, it was possible to achieve a complementary inverter behavior that exhibits an ideal switching point, limited current flow only during switching operations, and a full level swing at the output. This serves as supporting evidence for the existence of an undoped complementary circuit. Following the reconfiguration of both RFETs, it was observed that the inverter exhibited an almost identical behavior, with a minimal shift in the switching point. This showcases the symmetrical nature of the transistors at the circuit level, as well as the ability to reconfigure each individual transistor within the circuit. Furthermore, a reconfigurable circuit employing only four RFETs was successfully implemented to perform a NAND/NOR logic polymorphic gate. In addition it has been shown that a XOR/XNOR gate can be realized and verified very efficiently at the circuit level. Overall, when compared to conventional transistors, this design allow for a reduction in the number of transistors required, which in turn result in a reduction in the cost of the device. Circuits built of reconfigurable devices possess a broad spectrum of functional combinations and exhibit a significant level of flexibility. This particular characteristic of the polymorphic gates also presents benefits for potential secure electronic systems, such as camouflage techniques or logic locking, as the function is not dependent on only their physical layout and therefore cannot be easily identified through reverse engineering.

Although there is still potential for further enhancement, but it has been shown that these devices possess the fundamental capabilities to serve as viable alternatives to conventional transistors in certain domains. Taking a look ahead, there are some additional aspects that can be investigated to optimize the presented RFETs. First, the SiO_2 layer, as in the present work used, can of course be improved in terms of thickness and, most importantly, combined or replaced with different high-k dielectrics. In order to achieve enhanced optimization, it is advisable to consider a potential transition from silicon to alternative materials such as a silicon-germanium compound (SiGe) or pure germanium (Ge) (which are group IV semiconductor). This adjustment is supported by simulations indicating a notable increase in current, so the values of the current can be amplified by a factor of

ten, resulting in a reduction of threshold voltages. This, in turn, leads to a decrease in dynamic power consumption. So the technology offers benefits in terms of power consumption, performance enhancement, and a significant increase in circuit speed. Additionally, tin (Sn) can be integrated into germanium, enabling the building of a direct bandgap transition, which opens up the possibility of utilizing optoelectronics in exactly the same system. Furter, the proposed technology enables the implementation of ferroelectric gates, allowing for non-volatile programming of modes. This capability would empower chip development, enabling individual programming of the desired functions by customers. The incorporation of neuromorphic self-learning devices is a viable option. By applying a specific voltage, the polarization of the gate can be altered, subsequently allowing for the adjustment of current injection and they then basically learn from that. Additionally, positive feedback steep slope devices exhibit a steepness that surpasses the capabilities of conventional MOSFETs, exceeding 60 mV per decade. This characteristic enables significant reduction in power consumption. Furthermore, the Negative Differential Resistance (NDR) effect can be incorporated into the RFET, enabling the programming of voltage or NDR occurrence, meaning this device can be configured as both p-type and n-type transistors, as well as NDR transistors, which introduces an additional functionality, therefore, adding more functionality and making things more intelligent. In General, with these types of structures, there are numerous applications possible for future developments to pursue. So the whole package is really to understand as a technological platform, which offers a wide range of functionalities that can be leveraged through their seamless integration and exactly that is one of the beauties of this emerging technology.

List of Figures

Bibliography

[1] J. M. Andrews and J. C. Phillips. “Chemical Bonding and Structure of Metal-Semiconductor Interfaces”. In: *Physical Review Letters* 35.1 (July 1975), pp. 56–59.

[2] J. Bardeen. “Surface States and Rectification at a Metal Semi-Conductor Contact”. In: *Physical Review* 71.10 (May 1947), pp. 717–727.

[3] F. Braun. “Ueber die Stromleitung durch Schwefelmetalle”. In: *Annalen der Physik und Chemie* 229.12 (1875), pp. 556–563.

[4] N. Breil et al. “Challenges of nickel silicidation in CMOS technologies”. In: *Microelectronic Engineering* 137.1 (Apr. 2015), pp. 79–87.

[5] A. N. Broers, A. C. Hoole Andrew, and J. M. Ryan. “Electron beam lithography-Resolution limits”. In: *Microelectronic Engineering* 32.1-4 (Sept. 1996), pp. 131–142.

[6] D. Buchanan et al. “80 nm polysilicon gated n-FETs with ultra-thin Al/sub 2/O/sub 3/ gate dielectric for ULSI applications”. In: *International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138)*. IEEE, 2000, pp. 223–226.

[7] T. Campbell et al. “Dynamics of Oxidation of Aluminum Nanoclusters using Variable Charge Molecular-Dynamics Simulations on Parallel Computers”. In: *Physical Review Letters* 82.24 (June 1999), pp. 4866–4869.

[8] J. D. Casperson, L. D. Bell, and H. A. Atwater. “Materials issues for layered tunnel barrier structures”. In: *Journal of Applied Physics* 92.1 (July 2002), pp. 261–267.

[9] J.-P. Colinge. “Silicon-on-Insulator Technology: Materials to VLSI”. Boston, MA: Springer US, 2004.

[10] A. M. Cowley and S. M. Sze. “Surface States and Barrier Height of MetalâSemiconductor Systems”. In: *Journal of Applied Physics* 36.10 (Oct. 1965), pp. 3212–3220.

[11] S. Cristoloveanu. “SOI: a metamorphosis of silicon”. In: *IEEE Circuits and Devices Magazine* 15.1 (1999), pp. 26–32.

[12] S. Das, M. Dubey, and A. Roelofs. “High gain, low noise, fully complementary logic inverter based on bi-layer WSe2 field effect transistors”. In: *Applied Physics Letters* 105.8 (Aug. 2014), p. 083511.

[13] S. Datta et al. “Impact of contact and local interconnect scaling on logic performance”. In: *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*. IEEE, June 2014, pp. 1–2.
[14] G. Fasching. Springer Wien New York, 2005.
[15] F. Flores and C. Tejedor. “On the formation of semiconductor interfaces”. In: *Journal of Physics C: Solid State Physics* 20.2 (Jan. 1987), pp. 145–175.
[16] F. Flores, A. Muñoz, and J. Durán. “Semiconductor interface formation: The role of the induced density of interface states”. In: *Applied Surface Science* 41-42 (Jan. 1990), pp. 144–150.
[17] P. E. Gaillardon. “Functionality-enhanced devices an alternative to mooreâs law”. Ed. by P.-E. Gaillardon. Institution of Engineering and Technology, Nov. 2018, pp. 1–340.
[18] W. F. Gale and T. C. Totemeier. Elsevier Butterworth-Heinemann, 2004.
[19] P. M. Gammon et al. “Interface characteristics of n-n and p-n Ge/SiC heterojunction diodes formed by molecular beam epitaxy deposition”. In: *Journal of Applied Physics* 107.12 (June 2010).
[20] R. Gonzalez, B. Gordon, and M. Horowitz. “Supply and threshold voltage scaling for low power CMOS”. In: *IEEE Journal of Solid-State Circuits* 32.8 (1997), pp. 1210–1216.
[21] J. Hauser. “Noise margin criteria for digital logic circuits”. In: *IEEE Transactions on Education* 36.4 (1993), pp. 363–368.
[22] W. M. Haynes. “CRC Handbook of Chemistry and Physics, 93rd Edition”. CRC Handbook of Chemistry and Physics. Taylor & Francis, 2012.
[23] V. Heine. “Theory of Surface States”. In: *Physical Review* 138.6A (June 1965), A1689–A1696.
[24] A. Heinzig et al. “Reconfigurable Silicon Nanowire Transistors”. In: *Nano Letters* 12.1 (Jan. 2012), pp. 119–124.
[25] A. Heinzig et al. “Reconfigurable silicon nanowire transistors”. In: *Nano Letters* 12.1 (Jan. 2012), pp. 119–124.
[26] H. K. Henisch and C. Popescu. “Contacts with semi-insulators”. In: *Nature* 257.5525 (Oct. 1975), pp. 363–367.
[27] C. Hobbs et al. “Sub-quarter micron Si-gate CMOS with ZrO/sub 2/ gate dielectric”. In: *2001 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers (Cat. No.01TH8517)*. IEEE, 2001, pp. 204–207.
[28] K. J. Hubbard and D. G. Schlom. “Thermodynamic stability of binary oxides in contact with silicon”. In: *Journal of Materials Research* 11.11 (1996), pp. 2757–2776.
[29] “International Roadmap for Devices and Systems (IRDS) 2022 Edition”. Feb. 2023.
[30] “International Roadmap for Devices and Systems (IRDSâ¢) 2020 Edition”. Aug. 2021.
[31] J. B. Kuo and S. C. Lin. 1st edition. Vol. John Wiley & Sons. 2001.
[32] J. D. Plummer, M. D. Deal, and P. B. Griffin. Prentice Hall, 2000.
[33] K. Bernstein and J. Norman. Kluwer Academic Publishers, 2000.

[34] I. Kuon, R. Tessier, and J. Rose. “FPGA Architecture: Survey and Challenges”. In: *Foundations and Trends® in Electronic Design Automation* 2.2 (2007), pp. 135–253.
[35] M. Le Roy et al. “Wave-mechanical calculations of leakage current through stacked dielectrics for nanotransistor metal-oxide-semiconductor design”. In: *Journal of Applied Physics* 93.5 (Mar. 2003), pp. 2966–2971.
[36] E. A. Lewis and E. A. Irene. “The Effect of Surface Orientation on Silicon Oxidation Kinetics”. In: *Journal of The Electrochemical Society* 134.9 (Sept. 1987), pp. 2332–2339.
[37] J. R. Ligenza. “Effect of crystal orientation on oxidation rates of silicon in high pressure steam”. In: *Journal of Physical Chemistry* 65.11 (1961), pp. 2011–2014.
[38] M. Lundstrom. In: (2000), p. 418.
[39] C. A. Mead and W. G. Spitzer. “Fermi Level Position at Metal-Semiconductor Interfaces”. In: *Physical Review* 134.3A (May 1964), A713–A716.
[40] T. Mikolajick et al. “Reconfigurable field effect transistors: A technology enablers perspective”. In: *Solid-State Electronics* 194 (Aug. 2022), p. 108381.
[41] T. Mikolajick et al. “The RFET - A reconfigurable nanowire transistor and its application to novel electronic circuits and systems”. In: *Semiconductor Science and Technology* 32.4 (Mar. 2017), p. 043001.
[42] W. Mönch. “Electronic Structure of Metal-Semiconductor Contacts”. Ed. by W. Mönch. Vol. 4. Dordrecht: Springer Netherlands, 1990.
[43] W. Mönch. “Metal-semiconductor contacts: electronic properties”. In: *Surface Science* 299-300 (Jan. 1994), pp. 928–944.
[44] G. E. Moore. “Cramming more components onto integrated circuits”. In: *Proceedings of the IEEE* 86.1 (1998), pp. 82–85.
[45] N. F. Mott. “Note on the contact between a metal and an insulator or semi-conductor”. In: *Mathematical Proceedings of the Cambridge Philosophical Society* 34.4 (Oct. 1938), pp. 568–572.
[46] N. F. Mott. “The theory of crystal rectifiers”. In: *Proceedings of the Royal Society of London. Series A. Mathematical and Physical Sciences* 171.944 (May 1939), pp. 27–38.
[47] J. L. Murray and A. J. McAlister. “The Al-Si (Aluminum-Silicon) system”. In: *Bulletin of Alloy Phase Diagrams* 5.1 (Feb. 1984), pp. 74–84.
[48] T. Nishimura, K. Kita, and A. Toriumi. “Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface”. In: *Applied Physics Letters* 91.12 (Sept. 2007), p. 123123.
[49] “NSM Archive - Physical Properties of Semiconductors”. Feb. 2022.
[50] S. D. Pable and M. Hasan. “Performance analysis of FPGA interconnect fabric for ultra-low power applications”. In: *Proceedings of the 2011 International Conference on Communication, Computing & Security - ICCCS ’11*. New York, New York, USA: ACM Press, 2011, p. 210.
[51] J. Padovese et al. “Thin Si channel Back Enhanced (BE) SOI pMOSFET Photodetector under different bias conditions”. In: *2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*. IEEE, Apr. 2019, pp. 1–4.

[52] J. Patterson and B. Bailey. “Solid-State Physics: Introduction to the Theory”. SpringerLink: Springer e-Books. Springer Berlin Heidelberg, 2007.
[53] H.-S. Philip Wong. “Beyond the conventional transistor”. In: *Solid-State Electronics* 49.5 (May 2005), pp. 755–762.
[54] Pradyot Patnaik. 1st ed. McGraw-Hill, 2002.
[55] J. M. Rabaey, A. Chandrakasan, and B. Nikolic. 2nd ed. Vol. Prentice Hall. Prentice Hall, 2004.
[56] S. Rai et al. “Designing Efficient Circuits Based on Runtime-Reconfigurable Field-Effect Transistors”. In: *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 27.3 (Mar. 2019), pp. 560–572.
[57] E. Rhoderick and R. Williams. Ed. by P. Hammond and R. Grimsdale. 2nd ed. Oxford: Oxford University Press, 1988, p. 268.
[58] S. E. Ungersboeck. “Modeling of Strained CMOS Technology”. PhD thesis. Wien: Technische Universität Wien, 2007.
[59] K. Salah. “More than moore and beyond CMOS: New interconnects schemes and new circuits architectures”. In: *2017 IEEE 19th Electronics Packaging Technology Conference (EPTC)*. IEEE, Dec. 2017, pp. 1–6.
[60] W. Schottky. “Halbleitertheorie der Sperrschicht”. In: *Die Naturwissenschaften* 26.52 (Dec. 1938), pp. 843–843.
[61] M. Sheng and J. Rose. “Mixing buffers and pass transistors in FPGA routing architectures”. In: *Proceedings of the 2001 ACM/SIGDA ninth international symposium on Field programmable gate arrays*. New York, NY, USA: ACM, Feb. 2001, pp. 75–84.
[62] S. M. Sze and M. K. Lee. “Semiconductor Devices: Physics and Technology, 3rd Edition: Physics and Technology”. John Wiley & Sons, 2012.
[63] S. M. Sze and K. K. Ng. “Physics of Semiconductor Devices”. Wiley, 2006.
[64] S. Sze and J. Irvin. “Resistivity, mobility and impurity levels in GaAs, Ge, and Si at 300°K”. In: *Solid-State Electronics* 11.6 (June 1968), pp. 599–602.
[65] e. a. Sze Simon M. “Physik der Halbleiterbauelemente”. John Wiley & Sons, Incorporated, 2021.
[66] Takayasu Sakurai, Akira Matsuzawa, and Takakuni Douseki. “Fully-Depleted SOI CMOS Circuits and Technology”. Boston, MA: Springer US, 2006.
[67] C. Tejedor, F. Flores, and E. Louis. “The metal-semiconductor interface: Si (111) and zincblende (110) junctions”. In: *Journal of Physics C: Solid State Physics* 10.12 (June 1977), pp. 2163–2177.
[68] J. Trommer et al. “Elementary aspects for circuit implementation of reconfigurable nanowire transistors”. In: *IEEE Electron Device Letters* 35.1 (Jan. 2014), pp. 141–143.
[69] J. R. Tucker, C. Wang, and P. S. Carney. “Silicon field-effect transistor based on quantum tunneling”. In: *Applied Physics Letters* 65.5 (Aug. 1994), pp. 618–620.
[70] Vaughn Betz, Jonathan Rose, and Alexander Marquardt. Vol. 497. The Springer International Series in Engineering and Computer Science, 1999.
[71] G. F. Voort and J. Asensio-Lozano. “The Al-Si Phase Diagram”. In: *Microscopy and Microanalysis* 15.SUPPL. 2 (July 2009), pp. 60–61.

[72] H. Warlimont and W. Martienssen. Springer, 2018, p. 1140.
[73] W. M. Weber et al. “Reconfigurable nanowire electronics - A review”. In: *Solid-State Electronics* 102 (Dec. 2014), pp. 12–24.
[74] W. M. Weber and T. Mikolajick. “Silicon and germanium nanowire electronics: Physics of conventional and unconventional transistors”. In: *Reports on Progress in Physics* 80.6 (June 2017), p. 066502.
[75] F. Wessely, T. Krauss, and U. Schwalke. “CMOS without doping: Multi-gate silicon-nanowire field-effect-transistors”. In: *Solid-State Electronics* 70 (Apr. 2012), pp. 33–38.
[76] F. Wessely, T. Krauss, and U. Schwalke. “Reconfigurable CMOS with undoped silicon nanowire midgap Schottky-barrier FETs”. In: *Microelectronics Journal* 44.12 (Dec. 2013), pp. 1072–1076.
[77] N. H. E. Weste and D. Harris. 4th ed. Vol. Addison-Wesley. Addison-Wesley, 2004.
[78] G. D. Wilk, R. M. Wallace, and J. M. Anthony. “High-κ gate dielectrics: Current status and materials properties considerations”. In: *Journal of Applied Physics* 89.10 (May 2001), pp. 5243–5275.
[79] L. Wind et al. “Composition Dependent Electrical Transport in Si1âxGex Nanosheets with Monolithic Single-Elementary Al Contacts”. In: *Small* (2022), p. 2204178.
[80] L. Wind et al. “Monolithic and Single-Crystalline Aluminum-Silicon Heterostructures”. In: *ACS Applied Materials and Interfaces* 14.22 (June 2022), pp. 26238–26244.
[81] L. S. Yojo et al. “Study of BE SOI MOSFET Reconfigurable Transistor for Biosensing Application”. In: *ECS Journal of Solid State Science and Technology* 10.2 (Feb. 2021), p. 027004.
[82] L. Yojo et al. “Reconfigurable back enhanced (BE) SOI MOSFET used to build a logic inverter”. In: *SBMicro 2017 - 32nd Symposium on Microelectronics Technology and Devices: Chip on the Sands, co-located Symposia: 30th SBCCI - Circuits and Systems Design, 2nd INSCIT - Electronic Instrumentation, 7th WCAS - IC Design Cases and 17th SForum - Undergraduate*. Institute of Electrical and Electronics Engineers Inc., Nov. 2017.
[83] J. Zhang et al. “Design optimization of stacked layer dielectrics for minimum gate leakage currents”. In: *Solid-State Electronics* 44.12 (Dec. 2000), pp. 2165–2170.