Master's Thesis

Fabrication and characterization of $HfxZr_{1-x}O_y$ layers for novel nanosheet devices: from high-k to ferroelectric behaviors

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Abstract

With the continuous advancement of semiconductor technology, the size of devices has been shrinking, making it increasingly challenging to improve device performance due to issues like gate leakage and quantum tunneling. To overcome these challenges, the concept of "More than Moore" emerged, focusing on increasing the functionality of devices at a given dimension instead of following Moore's law, which involves scaling down device sizes.

A significant breakthrough occurred in 2011 when a material, hafnium oxide, was rediscovered to possess superior performance. This material exhibited greater capacitance and stable ferroelectricity even at nanometer-scale thickness. In this thesis, we investigate Zirconium-doped Hafnium Oxides, specifically Hafnium Zirconium Oxide (HZO), a material with a higher dielectric constant than SiO_2. Depending on the deposition and integration processes, HZO can exhibit strong ferroelectric properties or charge trapping capabilities, two characteristics particularly suitable for memory applications. By employing a HZO as gate oxide, it is possible to benefit from a higher dielectric constant, improved capacitance, lower power consumption, and CMOS compatibility.

The thesis primarily focuses on implementing and optimizing an Atomic Layer Deposition (ALD) process to deposit sub-10 nm thick HZO films with high purity. The grown material is comprehensively characterized using a vast set of experimental techniques, to assess the deposited thin film properties. Thanks to a careful electrical characterization, the dielectric constants of the grown HfO_2 and ZrO_2 are extracted, and the ferroelectric properties of the combined HZO are confirmed through capacitance-voltage (C-V) and polarization-voltage (P-V) analyses.

Furthermore, we investigate the possibility of realizing memory devices based on the integration of an HZO layer into monolithic and single-crystalline Aluminum-Silicon heterostructures. The fabricated devices are electrically characterized, showing the potential of Al-Si-Al heterostructure memory devices using ferroelectric materials as charge trapping memories, ensuring stable data retention and proposing their suitability for memory applications.

In conclusion, this work successfully implemented the controlled ALD growth of HZO thin films and verified the ferroelectric behavior of the grown material . Additionally, it reveals the potential of stable memory devices, providing valuable insights into the electrical properties of HZO and its promise as a high-k material for advanced semiconductor devices. The research sets a foundation for improved memory technologies and advances in semiconductor materials and devices.

Kurzfassung

Mit dem kontinuierlichen Fortschritt der Halbleitertechnologie hat die Größe der Geräte abgenommen, was es zunehmend schwieriger macht, die Leistung der Geräte zu verbessern, aufgrund von Problemen wie Gate-Leckage und Quantentunnelung. Um diese Herausforderungen zu überwinden, entstand das Konzept von "More than Moore", das sich darauf konzentriert, die Funktionalität von Geräten bei einer gegebenen Dimension zu erhöhen, anstatt dem Moore'schen Gesetz zu folgen, das das Skalieren der Gerätegrößen umfasst.

Ein bedeutender Durchbruch erfolgte im Jahr 2011, als ein Material namens Hafniumoxid wiederentdeckt wurde, das eine überlegene Leistung aufwies. Dieses Material zeigte eine größere Kapazität und eine stabile Ferroelektrizität auch bei nanometerdicken Schichten. In dieser Arbeit untersuchen wir zirconiumdotiertes Hafniumoxid, insbesondere Hafnium-Zirconium-Oxid (HZO), ein Material mit einer höheren Dielektrizitätskonstante als SiO$_2$. Abhängig von den Abscheidungs- und Integrationsprozessen kann HZO starke ferroelektrische Eigenschaften oder Ladungseinfangfähigkeiten aufweisen, zwei Eigenschaften, die besonders für Speicheranwendungen geeignet sind. Durch den Einsatz von HZO als Gateoxid ist es möglich, von einer höheren Dielektrizitätskonstante, verbesserter Kapazität, geringerem Stromverbrauch und CMOS-Kompatibilität zu profitieren.

Die Arbeit konzentriert sich hauptsächlich auf die Implementierung und Optimierung eines Atomic Layer Deposition (ALD)-Verfahrens zur Abscheidung von HZO-Schichten mit einer Dicke von weniger als 10 nm und hoher Reinheit. Das gewachsene Material wird umfassend mit einer Vielzahl von experimentellen Techniken charakterisiert, um die Eigenschaften der abgeschiedenen dünnen Schicht zu bewerten. Dank einer sorgfältigen elektrischen Charakterisierung werden die Dielektrizitätskonstanten des gewachsenen HfO$_2$ und ZrO$_2$ extrahiert, und die ferroelektrischen Eigenschaften des kombinierten HZO werden mittels Kapazitäts-Spannungs (C-V)- und Polarisations-Spannungs (P-V)-Analysen bestätigt.

Des Weiteren untersuchen wir die Möglichkeit, Speichergeräte zu realisieren, die auf der Integration einer HZO-Schicht in monolithische und einkristalline Aluminium-Silizium-Heterostrukturen basieren. Die hergestellten Geräte werden elektrisch charakterisiert und zeigen das Potenzial von Al-Si-Al-Heterostruktur-Speichergeräten unter Verwendung von ferroelektrischen Materialien als Ladungseinfang-Speicher, die eine stabile Datenspeicherung gewährleisten und sich für Speicheranwendungen eignen. Zusammenfassend wurde in dieser Arbeit erfolgreich das kontrollierte ALD-Wachstum von HZO-Dünnschichten umgesetzt und das ferroelektrische Verhalten des gewachsenen Materials verifiziert. Zusätzlich zeigt sie das Potenzial stabiler Speichergeräte auf und liefert wertvolle Erkenntnisse über die elektrischen Eigenschaften von HZO und dessen Versprechen als Hoch-k-Material für fortschrittliche Halbleitergeräte. Die Forschung legt somit den Grundstein für verbesserte Speichertechnologien und Fortschritte in Halbleitermaterialien und -geräten.

Inhaltsverzeichnis

Kapitel 1

Introduction

The invention of the transistor in 1947 by John Bardeen, William Shockley, and Walter Brattain at Bell Laboratories denoted a remarkable advancement in the field of electronics. This groundbreaking discovery utilized germanium (Ge), a semiconductor material with intermediate electrical conductivity between insulators and conductors. The transistor invention led to their recognition with the Nobel Prize in Physics in 1956. Subsequently, in 1956, Daewon Kahng and Dr. Martin Mohammed John Atalla, working at the same research institute, developed the first Metal Oxide-Semiconductor Field Effect Transistor (MOSFET). Despite its potential as a semiconductor device for digital switching, the MOSFET initially received little attention. However, continuous advancements in fabrication techniques enabled the miniaturization of MOSFET devices, allowing for the integration of multiple devices in a small area and reducing the cost per transistor. Furthermore, the introduction of the Complementary Metal-Oxide-Semiconductor (CMOS) fabrication process significantly enhanced the power efficiency of MOSFET-based circuits. Consequently, MOSFETs have become the most widely manufactured devices in history.

In 1965, Gordon Moore, co-founder of Intel, postulated "Moore's Law,ßtating that the number of components in an integrated circuit would double every 18-24 months. This law set a standard for the semiconductor industry, driving the relentless decrease in transistor size for over two decades. This downsizing facilitated higher transistor packing density, faster circuit speeds, and lower power dissipation. However, further scaling of MOSFETs into the sub-100 nm regime poses significant challenges.[1] The pursuit of miniaturization is approaching physical limits as reducing insulator thickness results in an unacceptable increase in gate leakage current through direct quantum tunneling.[2] To address the scaling issues faced by traditional Moore's Law, researchers have embraced the "More than Moore"concept, exploring alternative solutions. One promising approach involves the integration of new materials to enhance device functionality. Notably, high dielectric constant (high-k) materials have been introduced as the oxide layer in MOSFETs due to

their high permittivity.

Traditionally, MOSFETs have utilized SiO_2 as the oxide layer, which possesses a dielectric constant of 3.9. However, for very thin thicknesses, SiO_2 leads to leakage current issues. By substituting or combining SiO_2 with high-k materials, the oxide layer can avoid current leakage even at thin layers (below 10 nm) while improving device functionalities while maintaining the original structure. This paradigm shift in the "More than Mooreäpproach holds tremendous potential for future advancements in the semiconductor industry. In this thesis, we focus on a high-k material obtained from a 1:1 mixture of HfO_2 and ZrO_2, mainly known as HZO.

Under the right conditions, HZO can show strong ferroelectric properties, providing it with high permittivity and capacitance, making it an excellent material for insulation and enhancing device performance. In 2011, Qimonda announced the discovery of ferroelectricity in Si-doped hafnium oxide, reigniting interest in ferroelectric materials. HfO_2-based ferroelectric materials have demonstrated their effectiveness in producing chips below 10 nm and have emerged as promising materials to overcome limitations associated with device miniaturization. HfO_2-based materials are highly interesting for innovative memory applications, either relying on their capacity to store charges or exploiting the recently discovered ferroelectricity. In particular, ferroelectric-based device consume low power for data processing and can retain data even when power is turned off, providing significant advantages for memory devices. As a result, Intel adopted a gate oxide based on Hf. In this study, we have implemented a process for the growth of ferroelectric HZO layers through Atomic Layer Deposition (ALD) for a MOS capacitor. Our focus lies in characterizing the obtained material and analyzing its properties using a wide range of experimental techniques, including spectroscopic analysis and electrical characterization.

This thesis is structured as follows:

In Chapter 2, we delve into the basic theories of ferroelectricity, Hf-based ferroelectric materials, and Hf-based memory devices.

Chapter 3 provides an overview of the equipment and devices employed in the cleanroom, along with a detailed description of the experimental process. We discuss the modifications made to the semiconductor process to optimize the ferroelectric capacitor, which took place over several months. Furthermore, we introduce the various machines utilized in the laboratory.

In Chapter 4, we present the experimental results and conduct a comprehensive analysis of the physical, chemical, and electrical characteristics of the obtained data.

Kapitel 2

Theory

This chapter provides background information and up-to-date technological knowledge on key topics to better understand my thesis. The first part deals mainly with high-k and ferroelectricity, including an explanation of its definition and properties, as well as an introduction to a representative material and its structure and related characteristics. The second part focuses on HZO, which is widely studied for its interesting properties. A brief overview of these studies is provided. Finally, Ferroelectric RAM (FeRAM) and Ferroelectric field effect transistor (FeFET) are introduced.

2.1 Dielectricity

To provide a foundation for discussing ferroelectricity, it is important to first describe the behavior of an atom in an external electric field and the properties of dielectrics. Dielectrics can be divided into subclasses based on their crystal structure, and ferroelectrics are one such subclass. The hierarchical relationship between dielectrics and ferroelectrics is depicted in Figure 1.2.1.

Every atom is composed of electrons and an atomic nucleus and is affected by an electric field. When an external electric field is applied to an atom, the position of the electron cloud changes. The negatively charged atomic shell shifts in the opposite direction of the applied field, while the positively charged nucleus moves in the same direction as the field. This differential movement leads to the separation of electrical charges within the atom, resulting in the creation of an electric-field-induced dipole moment. This electronic polarization phenomenon can be observed in all dielectric materials.[3]

Dielectric materials are not electrically conductive, as depicted in Figure 2.2a in the absence of an electric field. Under these circumstances, only a minimal shift or displacement of charge within the material is observed. However, when an external electric field is app-

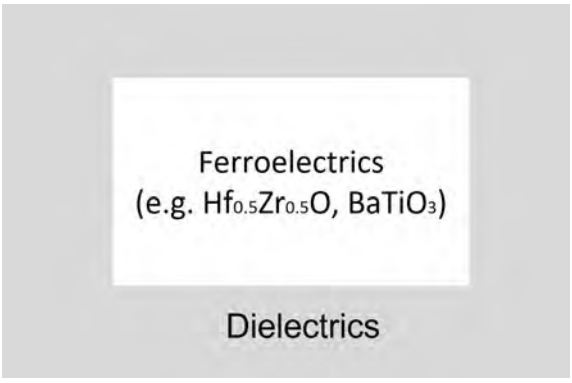
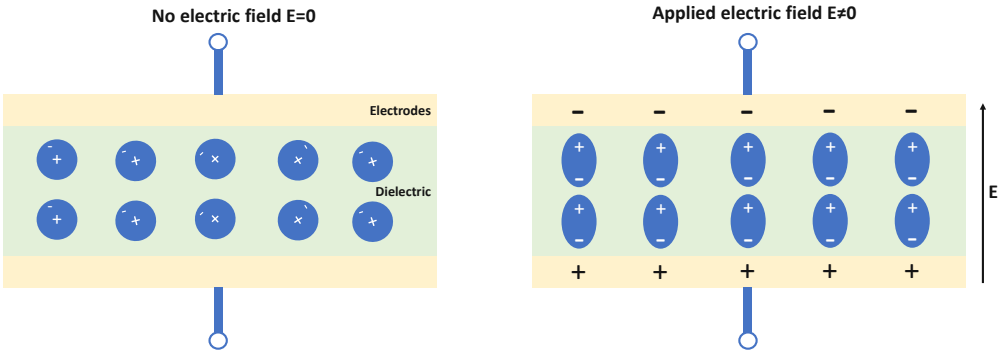


Abbildung 2.1: *Hierarchy of Dielectrics*



(a) **(b)**

Abbildung 2.2: *Atom behaviour in the presence of an external electric field*

lied, as illustrated in Figure 2.2b, dielectric materials undergo a process known as electric polarization.

The extent of shift or displacement in response to an external electric field is quantified by the dielectric constant, which represents the ability of a material to store electrical energy. When the external field is removed, the electric polarization cease to exist. This dielectric behavior can be expressed by the relation between the polarisation vector P_i, the electric field vector E_j, and the electric displacement field D_i.

$$P_i = \epsilon_0 \chi_{ij} E_j \tag{2.1}$$

$$D_i = \epsilon_{ij} E_j + P_i \tag{2.2}$$

Here, the electric susceptibility χ_{ij} is defined as $\chi_{ij} = \frac{\epsilon_{ij}}{\epsilon_0} - 1$, where ϵ_{ij} represents the dielectric permittivity. The ratio ϵ_{ij}/ϵ_0 is commonly referred to as the dielectric constant, denoted as $\epsilon_{r,ij}$. [3]

In the case of dielectric materials, a linear relationship between displacement and permittivity with respect to the electric field is commonly observed. This linear behavior is depicted in Figure 2.3a. The displacement is directly proportional to the applied electric field, and the permittivity remains constant throughout this linear range.

However, there are materials known as ferroelectric materials that exhibit non-linear behavior. These materials deviate from the linear relationship between displacement and permittivity. Figure 2.3b illustrates the non-linear behavior observed in ferroelectric materials. They demonstrate characteristics such as hysteresis loop and polarization switching, which make them distinct from linear dielectric materials. The non-linear behavior of ferroelectric materials is attributed to the presence of spontaneous polarization and domain structure within the material.

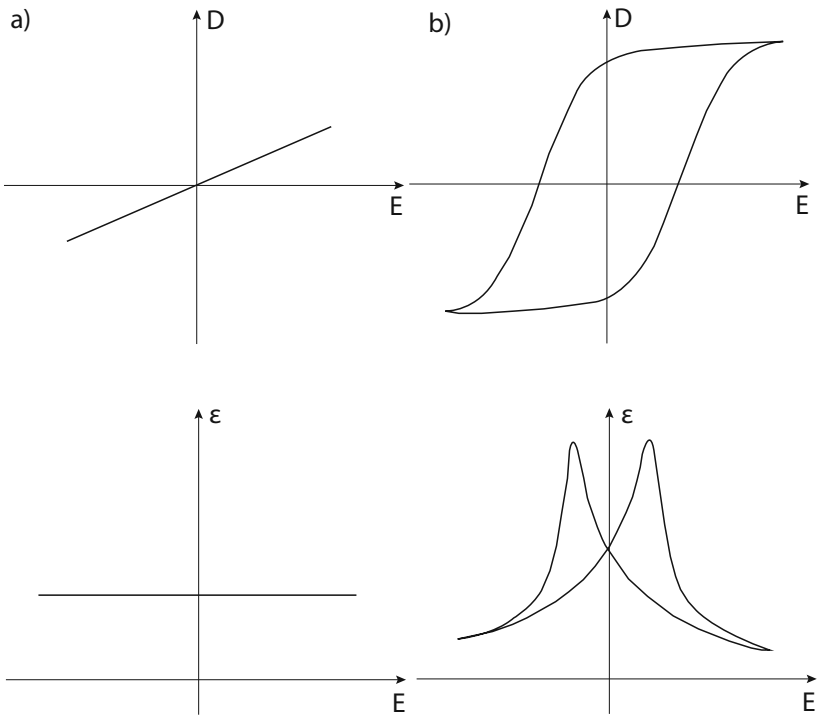


Abbildung 2.3: *a) Displacement and permittivity of linear dielectric material, b) Displacement and permittivity of non-linear material*

2.1.1 High-k material

The gate oxide plays a crucial role in the performance of transistors as it serves as an insulator, controlling the flow of charge and enabling precise modulation of transistor behavior. When a voltage is applied to the gate of a MOSFET, it modifies the distribution of charges within the underlying semiconductor. The insulator, commonly known as the

gate oxide, acts as a barrier, preventing the transfer of charges through the gate while the voltage is applied. To achieve this, the gate oxide needs to have an appropriate thickness to store charge effectively and increase insulation durability. However, as transistor sizes decrease, power consumption reduces, and operating speeds increase, there is a need for thinner gate oxides.

In conventional silicon devices, SiO_2 has been used as the gate oxide. To improve the operational characteristics of transistors and enhance integration by incorporating more transistors in smaller devices, the thickness of SiO_2 should be less than 1 nm when the transistor size is reduced to below 45 nm [4]. However, this requirement poses challenges due to physical limitations, leading to phenomena such as charge tunneling and increased leakage currents. Consequently, the performance of transistors is degraded, and the durability and reliability of the gate oxide are compromised.

Therefore, extensive research has been conducted to explore new materials that can replace SiO_2, leading to the development of high-k dielectrics. High-k materials have higher dielectric constants, which enable the formation of thicker oxide layers with the same capacitance, while simultaneously suppressing charge tunneling and reducing leakage currents. Among the most commonly used high-k dielectrics are metal-based oxides such as hafnium (Hf) and zirconium (Zr) compounds. These materials exhibit excellent interface characteristics with silicon and possess remarkable thermal stability, ensuring compatibility with Si devices. While the dielectric constant of SiO_2 is 3.9, hafnium oxide (HfO_2) exhibits a dielectric constant of 25[5]. HfO_2 has approximately five times higher dielectric constant than SiO_2. This implies that when subjected to the same voltage on equal areas and thicknesses, hafnium oxide can accommodate five times greater charge density than SiO_2. This relationship can also be observed in the equation for capacitance. Therefore, to maintain the same charge density, the thickness of HfO_2 can be increased fivefold, which helps address the leakage current issues associated with SiO_2.

The capacity of a parallel plate capacitor can be calculated using the following formula:

$$C = \frac{\epsilon_0 \epsilon_r A}{d_{ox}} \tag{2.3}$$

In this equation, C represents capacitance, ϵ_0 is the permittivity of vacuum, ϵ_r is the relative permittivity (dielectric constant) the material, A is the area, and d_{ox} is the thickness of the oxide layer.

It should be noted that having a higher dielectric constant does not automatically make a material a suitable replacement for SiO_2. The successful application of high-k dielectrics requires satisfying certain conditions. Firstly, they need to exhibit sufficiently large band offsets with Si to form a dynamically stable interface. Additionally, their properties should remain stable during the fabrication process and under operational conditions [4]. To meet these criteria, various high-k candidate materials are available, as shown in the referenced graph. From the graph, it can be observed that the dielectric constants of these oxides tend

to inversely correlate with the bandgap. Materials with sufficiently high dielectric constants and band offsets with Si are considered suitable candidates for high-k dielectrics. While oxides with extremely high dielectric constants like $BaTiO_3$ can also be candidates, their bandgaps are too low. They require a conduction band offset of at least 1 eV to avoid tunneling phenomena induced by short-circuiting electrons or holes.[4]

Moreover, research is ongoing to gain a deeper understanding of the physical properties of high-k materials and their integration with CMOS technology.

These investigations are recognized as core technologies for enhancing the performance of electronic devices and increasing integration density. Consequently, there is considerable interest in the future prospects of high-k dielectrics for CMOS applications, considering their potential for further development.

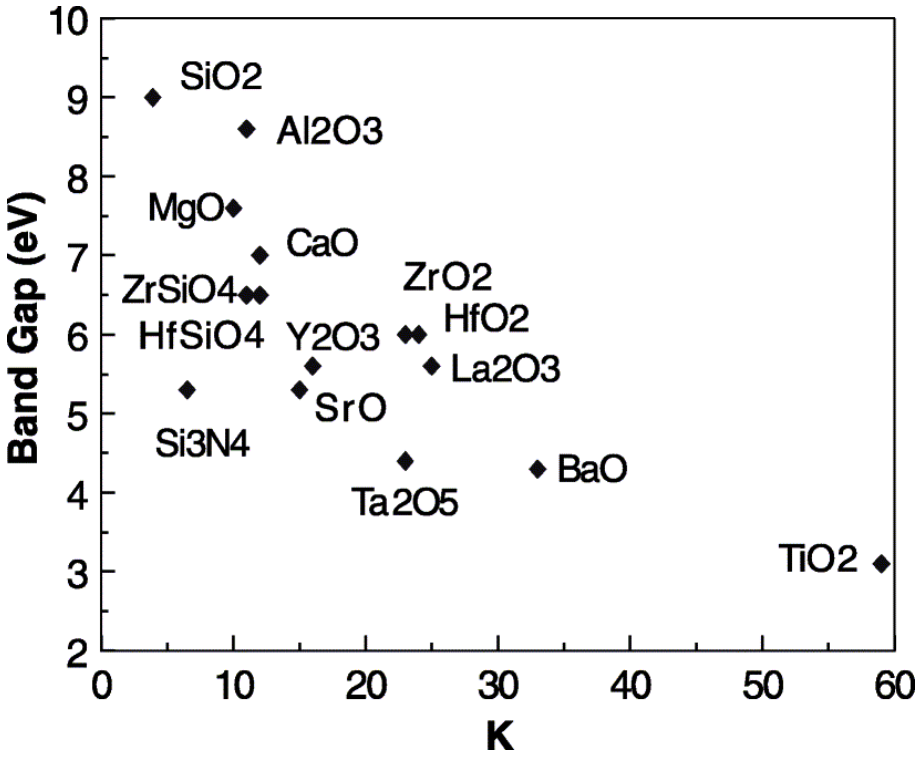


Abbildung 2.4: *Optical bandgap energies versus dielectric constant[6]*

2.1.2 Ferroelectricity

The ferroelectric behavior is a specific property observed in certain dielectric materials, characterized by the presence of spontaneous electric polarization. The polarization of ferroelectric materials can be expressed as the sum of induced polarization (P_i) and spontaneous polarization (P_s), given by the equation:

$$P = P_i + P_s \tag{2.4}$$

The induced polarisation (P_i) is produced by dielectrics material as long as external electric field exist. It is given by $P_i = \epsilon_0(\epsilon_r - 1)E$, where ϵ_0 represents the vacuum permittivity and ϵ_r is the relative permittivity (dielectric constant) of the material. This induced polarization disappears when the external electric field is removed.

On the other hand, the spontaneous polarisation (P_s) is an inherent property of ferroelectric materials and remains even in the absence of an external electric field. This is due to the separation of charges within the material, resulting in a remnant polarization (P_r). The ferroelectric displacement (D) can be expressed as:

$$D = \epsilon_0 E + P = \epsilon_0 E + (P_i + P_s) = \epsilon E + P_s \tag{2.5}$$

Here, ϵ represents the total permittivity, which includes the contribution from both induced polarization and the dielectric constant of the material.

The remnant polarisation is given by

$$D(E = 0) = P(E = 0) = P_s(E = 0) = \pm P_r \tag{2.6}$$

However, it should be pointed out that the spontaneous polarization (P_s) has a possibility to change its orientation of polarisation if a sufficiently large external field is applied. Ferroelectric materials exhibit two stable states, namely $+P_r$ and $-P_r$, as shown in equation 2.6.

The electric field-polarization graph of a ferroelectric is shown in Figure 2.5. As mentioned earlier, unlike dielectrics materials, ferroelectrics retain their polarization even when the external electric field is removed, leading to the characteristic hysteresis loop. In other words, the response of the material to an external stimulus, such as an external electric field, is affected not only by the extent of the external stimulus, but also by the materials previous history and its state at that time. Consequently, the same external stimulus can be lead to different outcomes depending on the condition under which it is applied. Ferroelectric materials typically exhibit hysteresis loops, and their characteristics repeat this loop behavior.

At the origin (point 'O') in Figure 2.5, the material's polarization is zero, assuming it starts from a state of zero polarization. As the external electric field (E) is gradually increased, the polarization (P) is generated and increased in the direction of the electric field, along the line from 'O' to point 'a'. When the electric field reaches a certain value, called saturation polarization (P_s), the polarization no longer increases. If the electric

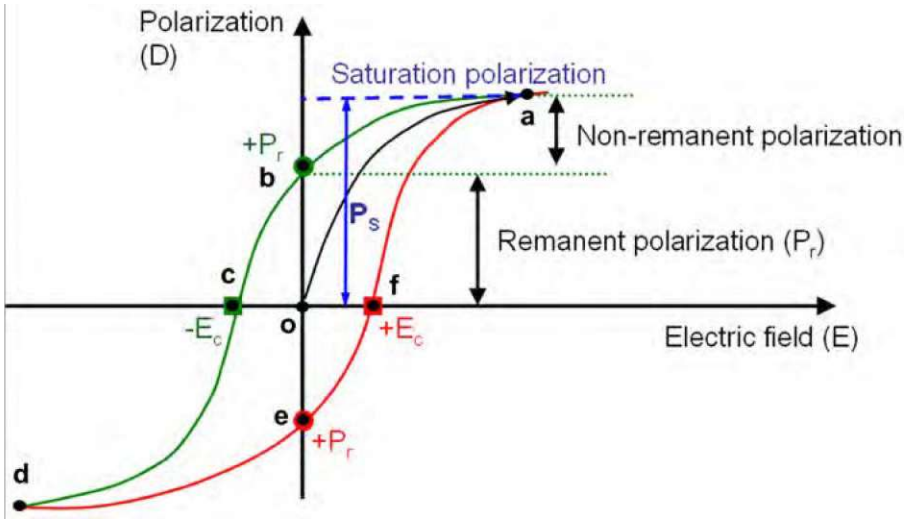


Abbildung 2.5: *Electric field-polarization hysteresis loop of a ferroelectric material[7]*

field is then reduced from the saturated polarization state, the polarization decreases slowly along the path from 'a' to 'b', which does not follow the original path from 'a' to 'o'. If an electric field is applied in the opposite direction starting from point 'b', the total polarization effectively becomes zero at point 'c'. The electric field at this point is referred to as the "coercive field"($-E_c$), which is the value required to cancel out the total polarization.

The saturation state occurs at the point 'd', but the direction of polarization is completely reversed compared to the state at point 'a'. After the applied electric field is removed, the residual polarization $-P_r$ remains at the point 'e'. If the electric field is then increased in the original direction from this state, it passes through point 'f', where the total polarization is zero at the coercive field ($+E_c$), and eventually reaches the saturation state at point 'a'. This curve exhibiting the loop-like behavior is known as the hysteresis curve.

Barium titanate ($BaTiO_3$) and Lead zirconate titanate $Pb(Zr_{1-x}Ti_x)O_3$ are two significant conventional ferroelectric materials that exhibit the perovskite or layered perovskite structure. Their general chemical formula is ABO_3, where A and B represent cations. The perovskite structure undergoes a phase transition at a specific temperature known as the Curie temperature(T_c). Above the Curie temperature (T > T_c), the perovskite structure adopts a cubic structure. In this structure, A ions occupy the cube corners, B ions occupy the body center, and the oxygen ions occupy the face center. Due to the presence of a center of symmertry, the cubic perovskite structure cannot exhibit ferroelectric properties. However when the temperature is below the Curie temperature (T < T_c), the B ion does not occupy the body center site and develop a dipole moment. This distortion leads to a lower-symmetry structure, such as tetragonal or orthorhombic, which exhibits a spontaneous dipole moment irrespective of an external electric field. This property characterises ferroelectric materials. [8]

The fig 2.6 illustrates the unit cell of cubic $BaTiO_3$, representing the perovskite structure. When the temperature drops below the Curie temperature, the position of B cation (Ti^{4+}) shifts (as shown in Figure fig2.6b), creating a geometrically unbalanced electrical charge and resulting in the formation of a dipole moment.[9] For $BaTiO_3$, this transition occurs at 120C°. Below 120C°, $BaTiO_3$ exhibits ferroelectric properties, while above this temperature, its crystal structure reverts to a cubic form, leading to the loss of its spontaneous dipole moment.

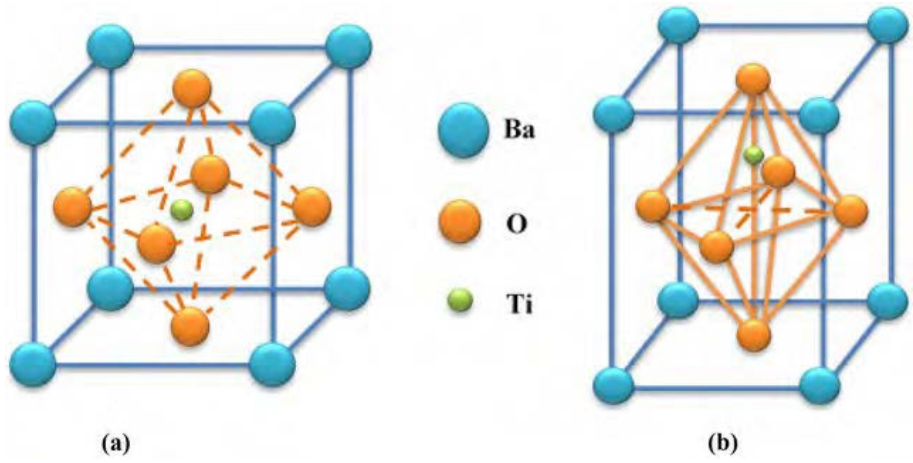


Abbildung 2.6: *Perovskite structure of ferroelectric BaTiO3 [10] [11]*

$Pb(Zr_{1-x}Ti_x)O_3$ (PZT) is also another important ferroelectric material. Another important ferroelectric material is lead zirconate titanate ($Pb(Zr_{1-x}Ti_x)O_3$)(PZT), which exhibits different phases such as rhombohedral, tetragonal and cubic phase, depending on the composition of Zr and Ti. A composition rich in $PbTiO_3$ displays a significant spontaneuos polarizatioin, allowing it to have ferroelectricity.

Ferroelectric materials, such as $BaTiO_3$ and $Pb(Zr_{1-x}Ti_x)O_3$, are widely used in applications in capacitors and memory devices due to their high dielectric constant.

2.2 Hf based ferroelectric materials

In the previous chapter, we discussed well-known ferroelectric materials such as PZT, $BaTiO_3$. However, PZT faces limitations due to its small bandgap size of 3-4 eV [12], [13]. Additionally, the thickness of PZT cannot be thinned beyond approximately 70 nm[13], posing challenges for sizes and increasing the risk of leakage current. In 2011, the discovery of ferroelectricity in HfO_2 materials[14] opened new era for the exploration of ferroelectric materials based on HfO_2. The ferroelectric properties of hafnium oxide were found to be associated with its unique structure. Experimental evidence supporting this claim was presented in a paper published in 2015, using the PACBED (Precession-Assisted Convergent Beam Electron Diffraction) technique to observe the presence of orthorhombic $Pca2_1$ phases [15]. Subsequent studies have focused on investigating the mechanisms behind the

formation of this orthorhombic structure, which exhibits ferroelectric properties.

2.2.1 HfO_2

The behavior of hafnium-based materials is influenced by various factors including thickness, temperature, and external pressure, leading to different states and phase transitions. At room temperature, hafnium oxide exists in a centrosymmetric monoclinic phase. As the temperature increases to 2050 K, it undergoes a transition to a tetragonal transitions to a cubic phase [14]. Each phase exhibits a distinct dielectric constant. The monoclinic phase of HfO_2 has a dielectric constant of 17-20, whereas the tetragonal phase has a higher dielectric constant of approximately 35-40.[8] Due to its centrosymmetric structure, the monoclinic phase does not exhibit spontaneous polarization. To induce ferroelectric behavior in hafnium-based materials, conditions that suppress the monoclinic of a certain level of tensile strain. Under these conditions, a transition to the noncentrosymmetric orthorhombic phase occurs, which exhibits spontaneous polarization and demonstrates ferroelectric properties. [8]

However, achieving the formation of the thermodynamically stable orthorhombic phase, which is naturally suppressed in pure hafnium oxide alone, is challenging. Therefore, in practical applications, doping with other elements such as silicon (Si), yttrium (Y), aluminum (Al), and zirconium (Zr) has been employed. This doping introduces structural changes to the hafnium oxide and facilitates the formation of the noncentrosymmetric orthorhombic phase. As a result, hafnium-based materials doped with these elements exhibit desirable ferroelectric properties. In the subsquent sections, ferroelectric materials generated by doping with each of these elements will be introduced.

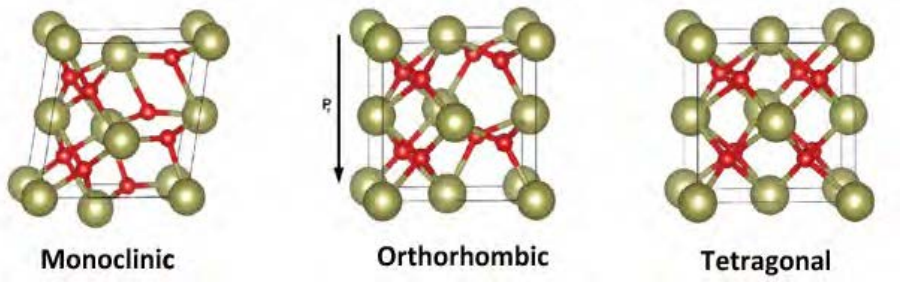


Abbildung 2.7: *Crystalline structures of HfO_2 adapted from [16]*

2.2.2 SiO_2 doped HfO_2

Boeske's findings provided valuable insights into the behavior of SiO_2-doped HfO_2 films. It was observed that SiO_2-doped HfO_2 films with a thickness of 10 nm and SiO_2 concentration below 4 mol% were examined, they exhibited a combination of monoclinic and tetragonal phases. Interestingly, when these films were mechanically encapsulated, the formation of the monoclinic phase was suppressed, resulting into the presence of an orthorhombic phase only. This observation suggests the manifestation of ferroelectric properties in the orthorhombic phase.[14]

Furthermore, the experimental results demonstrated that SiO_2 doping in HfO_2 has a significant impact on the material's ferroelectric behavior. Notably, the highest remanent polarization value, reaching approximately 10 $\mu C/cm^2$, was achieved at a coercive field of 1 MV/cm when the SiO_2 doping concentration was around 4 mol%. This remarkable finding is depicted in Figure 2.8. Additionally, the permittivity constant of SiO_2-doped HfO_2 was found to range between 3 and 40. Although smaller compared to conventional PZT, this range remains desirable for the development of ferroelectric field effect transistors. This discovery holds crucial promise, particularly considering that SiO_2-doped HfO_2 films can be fabricated with thicknesses below 10 nm, enabling further miniaturization of devices.

An interesting observation from Figure 2.8 is the transition from ferroelectricity to antiferroelectricity as the SiO_2 doping concentration exceeds 4.3 mol%. This indicates the intricate relationship between SiO_2 doping and the ferroelectric properties of HfO_2, emphasizing the importance of optimizing the doping level for achieving desired device performance.

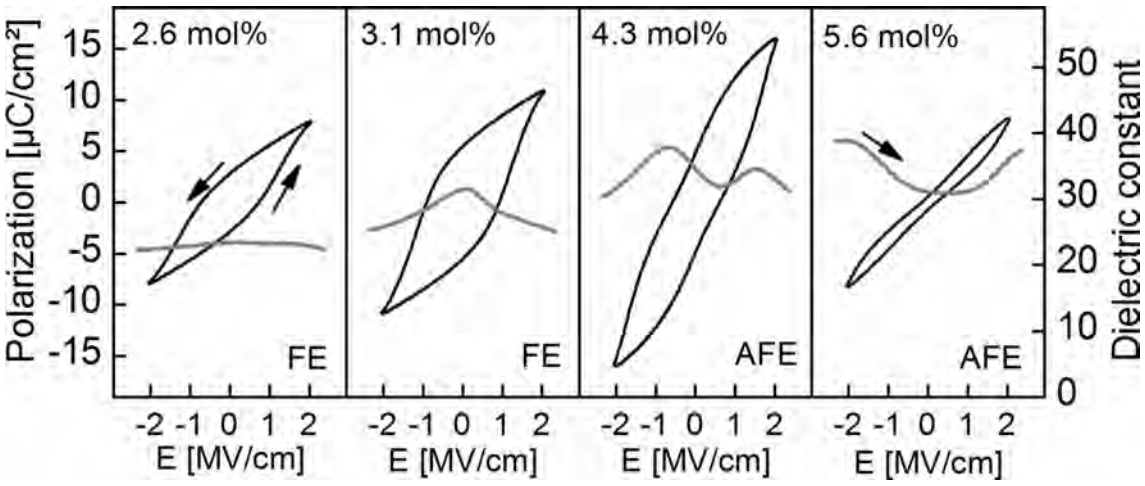


Abbildung 2.8: *Polarization hysteresis (black) and AC C-V characteristics (grey) of a set of "capped"MIM capacitors with 8.5 nm insulator thickness. The shape of the polarization loops changes from ferroelectric to antiferroelectric with increased SiO_2 admixture. This is reflected in one or two peaks in the AC C-V sweeps, respectively. [14]*

2.2.3 Al doped HfO_2

Ferroelectricity in Al-doped HfO_2 was discovered by Mueller in the paper titled Ïncipient Ferroelectricity in Al-Doped HfO_2 Thin Films"[17]. Figure 2.9 presents the polarization hysteresis curves obtained for different Al doping concentrations: 3.1, 4.8, 7.1, 8.5 and 11.4 mol %. The annealing process was performed either after metalization (referred to as PMA: Post metallization Annealing) or after the deposition of Al-doped HfO_2 (referred to as PDA: Post Deposition Annealing) for each concentration and the results are displayed in the figure.

The highest remanent polarization, approximately 6 $\mu C/cm^2$, was achieved at an Al doping concentration of 4.8 % under PDA conditions and 7.1 % under PMA conditions. The

structural analysis using X-ray diffraction (XRD) revealed an orthorhombic phase for the Al-doped HfO_2 samples. It is worth noting that at higher doping concentrations and elevated annealing temperatures, antiferroelectric behavior was observed.[17]

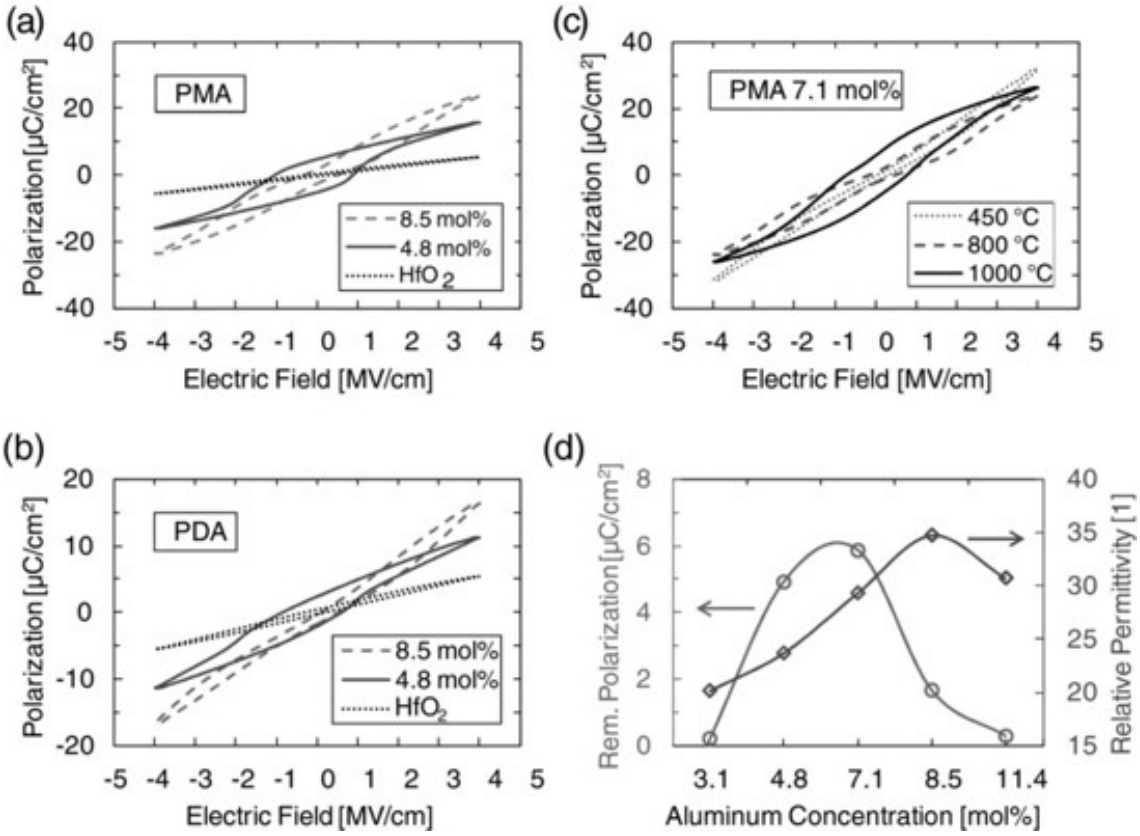


Abbildung 2.9: *Polarization hysteresis (black) and AC C-V characteristics (grey) of a set of "capped"MIM capacitors with 8.5 nm insulator thickness. The shape of the polarization loops changes from ferroelectric to antiferroelectric with increased Al admixture. This is reflected in one or two peaks in the AC C-V sweeps,respectively.[17]*

2.2.4 Y doped HfO_2

Olsen et al. reported the discovery of ferroelectricity in HfO_2 doped with low concentrations of yttrium (Y) in the range of 0.9 - 1.9 mol%. The structure studied consisted of TiN-Y doped HfO_2 stacks on a silicon substrate. In the corresponding figure 2.10, it can be observed that the remanent polarization obtained was approximately 15 $\mu C/cm^2$. However, when a higher concentration of yttrium was applied, the material exhibit paraelectric behavior. This transition occured because a larger amount of yttrium led to the formation of a tetragonal or cubic phase, which possesses a centrosymmetric structure. It is worth noting that the method used in this study was not atomic layer deposition (ALD) but RF magnetron sputtering. Additionally, the yttrium dopant was incorporated into the material through sputtering. The findings demonstrate that ferroelectric materials can be obtained even when employing physical methods other than ALD for doping.[18]

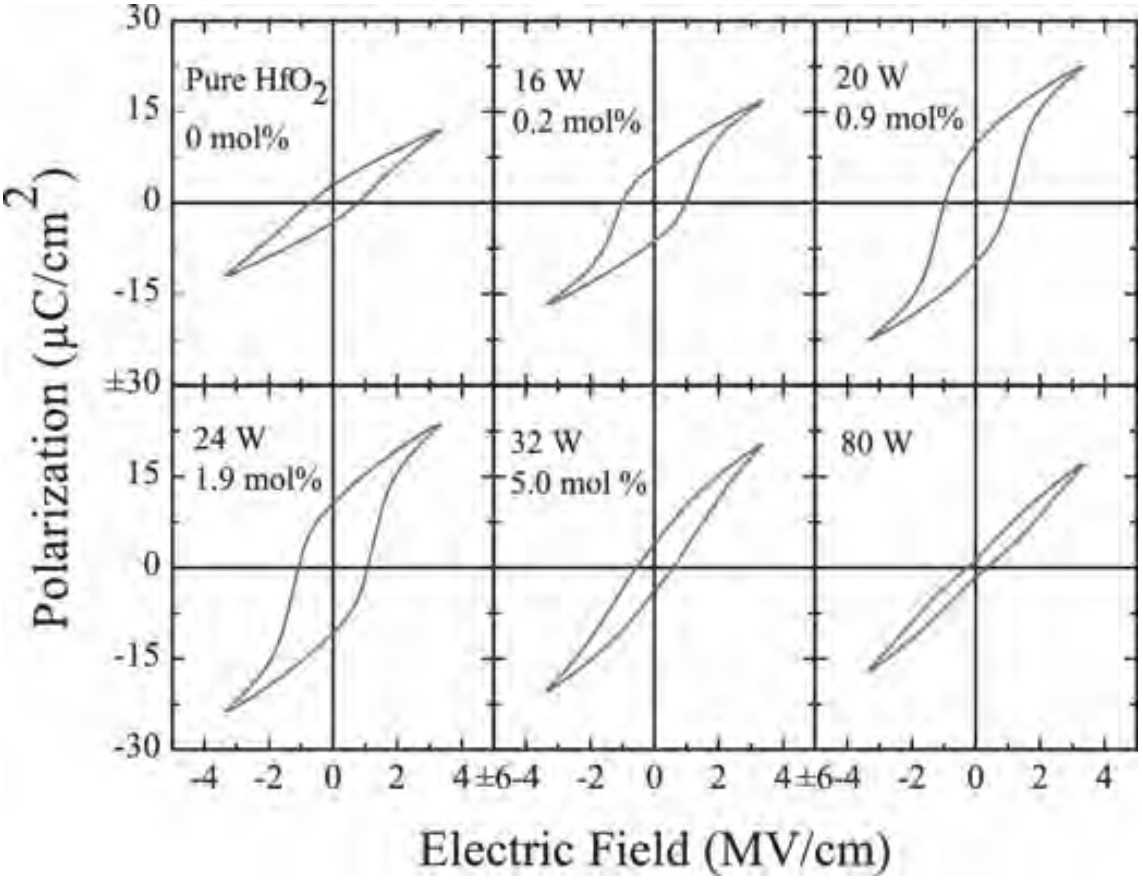


Abbildung 2.10: *Dependence of ferroelectric hysteresis properties on the concentration of yttrium dopant. For sputtering powers in the range of 20W, clear ferroelectric hysteresis is visible. For lower and higher doping concentrations a transisiton to paraelectric behaviour occurs. [18]*

2.2.5 HZO

Thin films of Hf-based materials doped with Zr offer significant advantages compared to previous materials. One notable advantage is that these films exhibit ferroelectricity even at high doping ratios of Zr, whereas previous materials showed antiferroelectricity at doping ratios above 10 %. The similarity in chemical and physical properties between Zr and Hf explain why Zr can be doped in similar ratios without losing its advantageous properties. Additionally, Zr has a relatively high dielectric constant (25) and a wide bandgap (5.1-7.8 eV), along with excellent thermal and chemical stability.[19],[20] These properties make it suitable for application as a high-k material, with the added benefit of higher permittivity compared to Hf, which is advantageous for memory storage devices.

In the case of HZO, which has a monoclinic phase at room temperature, the application of an external force has the potential to induce an orthorhombic phase, which exhibits ferroelectricity. However, it is generally challenging to form the orthorhombic phase in thin HZO films. This is primarily because the formation of the orthorhombic phase typically

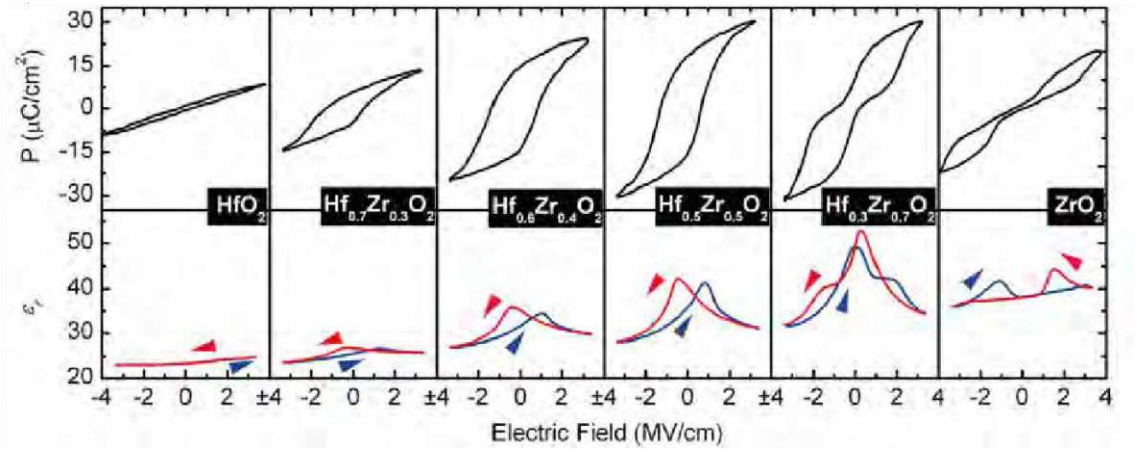


Abbildung 2.11: *PV hysteresis at 1 kHz and small signal CV hysteresis at 10 kHz (50 mV level) of 9 nm thin HfO_2-ZrO_2 based metal-insulator-metal capacitors at room temperature. An evolution from paraelectric HfO_2 to ferroelectric HfO_2-ZrO_2 to an antiferroelectric-like behavior in ZrO_2 can be observed in PV as well as in CV characteristics. [21]*

requires high pressure, which is not easily achieved in thin film due to their 2D nature and the inability to apply hydrostatic pressure.[22]

Alternatively, compressive or tensile stress can be applied to induce the desired phase transition. When amorphous or polycrystalline HfO_2 and ZrO_2 films are grown using the ALD method, the materials exhibit different degrees of thermal expansion, resulting in tensile stress.[23], [24] By applying compressive stress to the a-b plane and tensile stress to the c-axis, the tetragonal phase of HZO can be transformed into the orthorhombic phase. The specific forces required for this are apporoximately 760 MPa for tensile stress and 50 MPa for compressive stresss, which can easily induce the formation of the orthorhombic structure.[25]

In terms of the Hf:Zr ratio, as dipicted in Fig 2.11 pure HfO_2 films exhibit a nearly linear relationship between the displacement current and the applied electric field, as well as a relatively constant capacitance in this field range.[21] However, as the ZrO_2 content increases, the P-E and C-E curves exhibit hysteresis. When HfO_2 and ZrO_2 are present in a 1:1 ratio, the largest remanent polarization (P_r) value obtained is 17 $\mu C/cm^2$. As ZrO_2 occupies a larger proportion than HfO_2, the hysteresis becomes thinner and exhibits antiferroelectric properties. The graph for pure HfO_2 is close to linear, while the graph for pure ZrO_2 is close to antiferroelectric behavior.[21]

2.2.6 Comparison of material

PZT and Hf-based materials are renowned for their ferroelectric properties and widespread use in memory devices. However, in recent years, Hf-based materials have gained attention in research as an alternative to PZT. In order to provide a comprehensive analysis, this chapter aims to compare the distinctive characteristics of PZT and HZO, emphasizing

Characteristics	**Pb(Zr,Ti)O_3**	**Ferroelectric HfO_2 (HZO)**
Film thickness	$>$ 50 nm	5–40 nm
Annealing temp.	$>$ 600°C	400–1000°C (400–600°C)
Doping	N/A	$<$ 20% ($\sim$50%)
P_r	20–40 μC/cm^2	1–40 μC/cm^2 ($<$ 30 μC/cm^2)
E_c	$\sim$ 50 kV/cm	1–2 MV/cm
E_BD	0.5–2 MV/cm	4–8 MV/cm
$E_c/E_BD \times 100$	2.5–10%	12.5–50%
Dielectric constant	$\sim$ 1300	$\sim$ 30
ALD capability	Limited	Mature
CMOS compatibility	Pb and O_2 diffusion	Stable
BEOL compatibility	H_2 damage	Stable

Tabelle 2.1: *Comparison of material properties and scalability FE-HfO_2(HZO) and conventional PZT [12]*

their potential advantages in memory device applications. The comparative analysis is summarized in Table 2.1.

Film Thickness is a key aspect of modern technology, which plays a critical role in device miniaturizations. PZT films with thicknesses below 50 nm pose significant fabrication challenges, as maintaining desirable properties and stability becomes increasingly difficult in thin films. Additionally, the control of thin film deposition itself poses challenges, making it impractical to use PZT in miniaturized memory devices. In contrast, HZO can be deposited with thicknesses below 10 nm using atomic deposition techniques, thereby facilitating the fabrication of compact memory devices.

The compatibility of ferroelectric materials with complementary metal-oxide-semiconductor (CMOS) processes is a crucial consideration. PZT necessitates deposition and crystallization at temperatures exceeding 600 °C, which does not align with the lower temperature requirements of CMOS processes. This mismatch can lead to material degradation and performance deterioration. In contrast, HZO exhibit good CMOS compatibility. HfO_2 complies with the thermal budget restrictions of CMOS, which is a significant advantage of Hf-based ferroelectric materials as a promising choice for memory device applications.

Polarization Properties represent another distinguishing factor betwwen PZT and HZO. HZO requires a significantly higher electric field to alter its polarization direction compared to PZT. HZO has an ideal electric field value (E_c) ranging from 1 to 2 MV/cm, while PZT has a value of 50 kV/cm. Furthermore, there is a substantial difference in their dielectric constants. PZT can reach a maximum dielectric constant of 1300, whereas HZO has a value of approximately 30.

In light of these findings, the selection of the appropriate material depends on the intended application of the devices. Hf-based ferroelectric materials, especially HZO offer numerous

advantages as a foundation for memory devices. These advantages include the capability for thin film deposition, CMOS compatibility, feasibility of low-temperature deposition, as well as enhanced stability and durability. Consequently, the research in the field of HZO ferroelectrics are expected to thrive, particularly in memory device applications.

2.3 Applications

2.3.1 High-K Metal Gate (HKMG)

As MOSFETs have been scaled down in size, the gate length and thickness have also decreased. The thickness of the SiO_2 oxide layer has been reduced to approximately 1.2 nm, and further reduction can lead to increased leakage current, exceeding 1 A/cm^2, and tunneling, which can cause increased energy consumption and lower energy efficiency.[26]

To prevent leakage current, high-k dielectric materials with a dielectric constant greater than 3.9, such as HfO_2, ZrO_2, and Al_2O_3, have been investigated. High-k materials has several advantages over the traditional SiO_2. They have higher dielectric constant, which allows for a thicker dielectric layer with the same capacitance, while reducing leakage current.

The use of highly doped poly Si as the gate material can result in a depletion layer, which limits current flow and requires the use of thinner gate dielectrics to compensate. This issue can be addressed by replacing poly Si with a normal metal, which reduces the depletion layer and can improve device performance. [27][28]

High-k metal gate technology involved depositing a high-k dielectric layer on top of the Si substrate and then depositing a metal gate on top of the high-k layer.

2.3.2 High-K for charge trapping memories

Charge trapping memory is a prominent example of non-volatile memory, known for its ability to retain data even when the power is turned off. In the current semiconductor market, it holds significant importance and offers various advantages.

One of the key advantages of charge trapping memory is its non-volatile nature, which ensures data preservation for extended periods, even in the absence of power. This feature plays a vital role in maintaining data integrity and persistence over time.

In addition to its non-volatility, charge trapping memory enables fast data retrieval and storage. It achieves this by trapping and releasing charges within the insulating layer. By applying positive or negative charges at specific locations, charges are captured within the memory cell. The resulting electrical signals vary with the amount of trapped charges, allowing for the representation and storage of specific cell states.

To address the challenges associated with device scaling, the utilization of high-k materials in conjunction with charge trapping memory is crucial. As the device size decreases, the thickness of the oxide layer also decreases, increasing the potential for current leakage and posing a threat to data integrity. To mitigate these risks, high-k materials with high dielectric constants are employed. This unique characteristic enables the utilization of smaller electric fields to store the same charge quantity and therefore reducing the voltage needed for operation.

Moreover, by incorporating stacked high-k films as the charge-trapping layer, charge trapping memory can achieve improved operation and and energy consumption reduction. These enhancements are achieved through modifications in the trap density and the energy level of traps, alterations in the mechanism of electron/hole transmission, and the establishment of a suitable band offset. This integration of high-k materials in charge trapping memory technology has shown promising results in advancing its performance and overall functionality. [29]

2.3.3 Ferroelectric memories

Ferroelectric memories, such as FeRAM, FeFET and FTJ, are innovative devices that utilize the properties of ferroelectric materials. Understanding the development of ferroelectric memory technology is crucial for following these devices and recognizing their potential for data storage and processing. In the previous section, examples of high-k materials, such as High-k Metal Gate and High-k for charge trapping memory were discussed. Now, we will go through the operating principles of FeRAM and FeFET, as well as explore contemporary applications of ferroelectric memory.

In the 1990s, commercial ferroelectric memories using PZT were introduced. Major memory semiconductor manufacturers, including Samsung Electronics, SK Hynix, Toshiba, and Panasonic, extensively researched and commercialized FeRAM technology. However, in the 2010s, ferroelectric memory received less attention due to the emergence of other resistive switching and phase-change memories. The compatibility between CMOS processes, the basis of conventional semiconductor devices, and the existing ferroelectric material at that time, PZT, presented limitations to its further advancement. Additionally, for achieving high information storage density, device miniaturization was essential, but it was challenging to reduce the size of PZT below the 130nm node. The excellent properties of the material were observed in bulk or relatively thick film forms, making it difficult to maintain these properties in ultrathin films with thicknesses of several tens of nanometers.[30]

However, in 2011, ferroelectricity was discovered in HfO_2-based materials, leading to the revival of ferroelectric memory. Recent research has provided experimental and theoretical evidence supporting the possibility of downsizing devices using ferroelectric hafnium oxide. Based on this, research on ferroelectric memory using HfO_2 devices is currently progressing actively. Such ferroelectric memory is considered as an efficient non-volatile RAM that consumes low power and retains data even when the power is turned off. Representative

examples of ferroelectric memory include FeRAM, FeFET, and FTJ.[30][31]

2.3.3.1 Ferroelectric random-access-memory(FeRAM)

FeRAM (Ferroelectric Random-Access Memory) is a memory technology that utilizes a single cell composed of one transistor (T) and one capacitor (C), which is depicted in Figure 2.12. The capacitor incorporates a ferroelectric material as its dielectric layer to enable non-volatile information storage. The data is stored in the form of remanent polarization within the capacitor. Although FeFAM offers non-volatile characteristices, it has certain limitations in terms of integration density. Each cell requires two components, along with additional plate lines, which can hinder the scalability of the memory technology. To read information from the capacitor, a voltage higher than E_c (the switching voltage of the capacitor) needs to be applied in order to determine the switching status of the capacitor. However, during the read processed, there is a possibility of the existing information being destrcutively lost. Therefore, a refresh process is necessary after each read operation to restore the original data. This additional step can impact the overall efficiency of the FeRAM technology.

2.3.3.2 Ferroelectric field-effect-transistor (FeFET)

FeFET (Ferroelectric Field-Effect Transistor) is the most actively researched component among ferroelectric memory devices, featuring a structure similar to a MOSFET(Metal-Oxide-Semiconductor Field-Effect-Transistor). FeFET possesses both switching and threshold voltage adjustment functions, allowing it to store data.

The switching function of FeFET involves allowing or blocking the flow of electric charges in the semiconductor channel by manipulating the voltage applied to the gate. By applying positive or negative voltages above E_c, the FeFET gate can adjust the threshold voltage. The threshold volatage respresnt the minimum voltage required for the transistor to switch ON. Through this functionality, the direction of current flow can be reversed, serving as a means to store information withing the FeFET.

FeFET offers advantages such as high scalability and compatibility with existing CMOS-compatible processes, making it a promising candidate for future memory technologies. Its ability to integrate memory functionality within the transistor structure makes it particularly suitable for high-density memory applications.

2.3.3.3 Ferroelectric Tunnel Junction(FTJ)

FTJ (Ferroelectric Tunnel Junction) is a two-terminal device that adopts a capacitor structure, enabling high integration in crossbar arrays. However, the implementation of FTJ faces significant challenges in achieving uniformity and reliability over a large area, primarily due to the utilization of extremely thin sub-nanometer films. Non-uniform thickness, defects and variations that occurr during the manufacturing process can pose difficulties in ensuring consistent device performance.

In addition to the uniformity and reliability concerns, when employing a crossbar array configuration with FTJ, it becomes necessary to incorporate selection devices. These selection devices are specifically designed to activate only the desired cell while preventing interference with neighboring cells. The inclusion of selection devices aims to alleviate issues such as leakage currents, which can arise due to external factors and adversely impact the overall functionality of the array.

Despite the challenges associated with FTJ, ongoing research and development efforts are dedicated to improving its performance, reliability, and scalability. FTJ-based devices hold promise for high-density memory applications, and advancements in manufacturing techniques and device engineering are expected to enhance their viability in practical implementations.

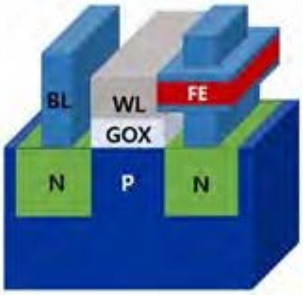
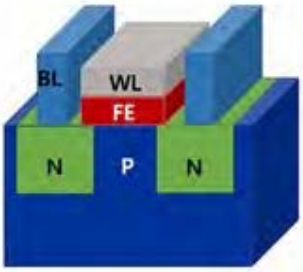
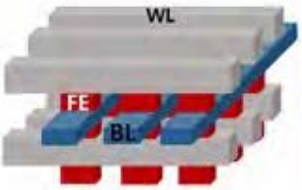
Type	1T - 1C type (FeRAM)	1T type (FeFET)	1R type (FTJ)
Structure			
Cell size	15 - 34 F^2	4 - 8 F^2	4 - 8 F^2
Read	Destructive	Non - destructive	Non - destructive
Endurance	- more than 10^{12} - Hf based Materials up to 10^{11}	- more than 10^{12} - Hf based Materials up to 10^5	- Hf based Materials up to 10^7
Retention	- 10 years - relatively good retention	- 10 years (extrapolation) - retention issue with depolarization field	- 10 years (extrapolation) - retention issue due to very thin thickness

Abbildung 2.12: *Comparison of device properties of ferroelectric random-access-memory(FeRAM), ferroelectric field-effect-transistor (FeFET), and ferroelectric tunnel junction (FTJ). adapted [30]*

Kapitel 3

Experimental Techniques

This chapter explains all the experimental processes that were utilized for this thesis. Several machines are used for the experiments. The working principle and operation of each of these tools are hereafter explained.

1. Fabrication
    - RCA cleaning
    - Sputter
    - Atomic Layer Deposition
    - Photolithography
    - Rapid Thermal Annealing
2. Chracterisation
    - Ellipsometery
    - X-ray Photoelectron Spectroscopy
    - Atom Force Microscopy
    - Capacitanve-Voltage measurement
    - Polarization measurement

3.1 Fabrication

3.1.1 RCA cleaning

The first step in the fabrication process of the experiment involves the cleaning of the silicon (Si) wafer. Si wafers obtained from the factory often contain chemical and physical residues, as well as particles such as dust that accumulate on the surface due to exposure to the surrounding environment. The presence of impurities at the micrometer or nanometer scale can lead to performance degradation and have detrimental effects on the overall yield, productivity and reliability of the fabrication process, resulting in economic losses. Therefore, a thorough cleaning process is crucial to remove these contaminants. The cleaning process consists of both wet and dry methods. Wet cleaning involves the use of chemical solutions to eliminate impurities, while the dry method employs non-solution-based techniques for impurity removal.

In this experiment, the RCA process[32], a wet cleaning method, is employed to clean the Si wafer surface. RCA 1 solution, composed of a mixture of H_2O_2 (hydrogen peroxide), NH_4OH (ammonium hydroxide), and deionized (DI) water, is utilized to remove particles and organic residues. Subsequently, RCA 2 solution, comprising H_2O_2, HCl (hydrochloric acid), and DI water, is employed to eliminate metal ions. In the subsequent part of this chapter, the RCA 1 and RCA 2 processes will be detailed, providing a step-by-step explanation of each process to achieve effective wafer cleaning.

3.1.1.1 RCA-1

The RCA-1 cleaning solution is prepared by mixing DI water, ammonium hydroxide(NH_4OH) (27% concentration), and hydrogen peroxide(H_2O_2) (30% concentration) in a ratio of 5:1:1. The following steps are followed:

1. A beaker is filled with DI water, and NH_4OH is added.

2. Both solutions are heated on a hot plate. Once the temperature reaches 70 °, H_2O_2 is added, resulting in a vigorous reaction.

3. After the solution has reacted for approximately 1-2 minutes, the Si wafer is carefully placed in the beaker and left in the solution for 15 minutes.

4. Subsequently, the wafer is rinsed several times with running DI water to remove any residual cleaning solution.

3.1.1.2 RCA-2

The RCA-2 cleaning solution is prepared by mixing DI water, hydrochloric acid(HCl) (27% concentration), and H_2O_2 (30% concentration) in a ratio of 6:1:1. The following steps are performed:

1. A beaker is filled with DI water, and HCl is added.

2. Both solutions are heated on a hot plate. Once the temperature reaches 70 °, H_2O_2 is added, resulting in a vigorous reaction.

3. After the solution has reacted for approximately 1-2 minutes, the Si wafer is carefully placed in the beaker and left in the solution for 10 minutes.

4. The wafer is then rinsed several times with running DI water to ensure complete removal of the cleaning solution.

3.1.2 Atomic Layer Deposition

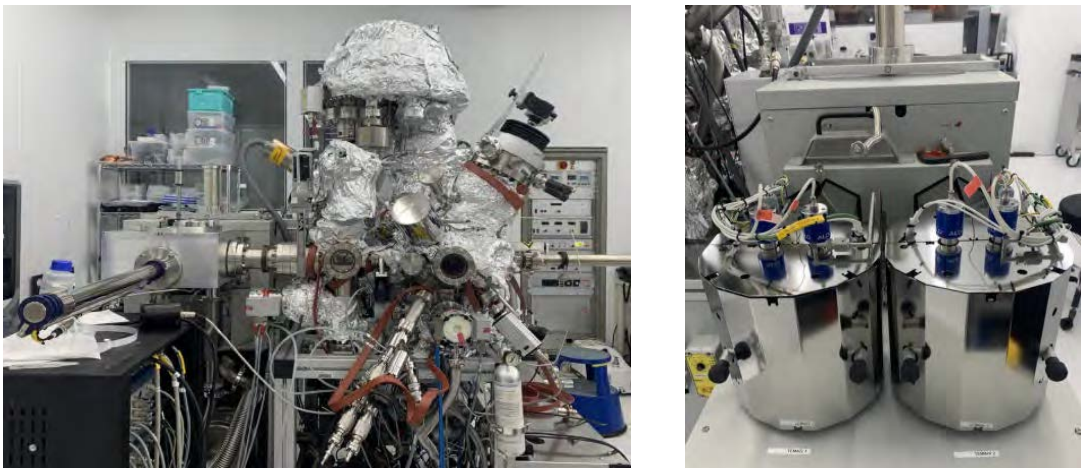


Abbildung 3.1: *a) Overview of UHV b)Precursor*

Atomic Layer Deposition (ALD) is a highly attractive technique for depositing thin layers of high-k dielectric materials onto substrates. In comparison to other deposition methods such as Physical Vapor Deposition (PVD) or Chemical Vapor Deposition (CVD), ALD offers several advantages. It enables deposition at low temperatures, exhibits self-limiting growth behavior, allowing the deposition of only one layer per cycle, and provides exceptional control over the thickness of nano-scale films. The ALD process is conducted under moderate vacuum conditions, ensuring protection against external impurities. Moreover, it yields films with excellent thickness uniformity and high density, enabling the precise fabrication of thin films.

As mentioned earlier, in this thesis we focus on the fabrication of high-k oxides. To fabricate the desired material (C), a sequential process involves introducing a precursor for an oxidizing agent (A) followed by the precursor for a metallic element (B). The precursors plays a crucial role as a necessary element to achieve the desired substance C, and refers to a substance in the step immediately before C. These precursors possess non-sticking properties and exhibit self-limiting behavior, which means that once a sufficient amount is

supplied, they saturate the surface, preventing further adsorption. Subsquently, the excess precursor is removed through purging, leaving behind only the desired atomic layer on the substrate. Following this step, a highly reactive material B is introduced, leading to a chemical reaction between the precursor (A) and material (B). This reaction results in the formation of the desired molecule (C) accompanied by the generation of by-product gases. Once again, purging is employed to eliminate the unreacted species and by-products, leaving behind the desired material C and completing the deposition process.

There are several Atomic Layer Deposition (ALD) configurations. In this thesis, we utilized two different ALD configurations: Thermal-ALD and Plasma-Enhanced ALD (PE-ALD).

Thermal-ALD involves the growth of thin films on a heated substrate, where precursor gases react with the surface. In this process, water is used as one of the reactants. The chemical reactions occur solely through the supply of thermal energy, which necessitates high deposition temperatures.[33]

On the other hand, PE-ALD involves a plasma to enhance the deposition process. A plasma is composed of radicals, ions, and electrons. The radicals exhibit high reactivity, contributing to chemical reactions easily during film growth. The deposition process in PE-ALD is similar to Thermal-ALD, but with the additional advantage of introducing plasma during the reactant pulsing step. This allows the creation of radicals and ions, even at lower temperatures, promoting film growth at reduced temperature.[34]

In this thesis, In this thesis, we always utilize a recipe based on the Thermal-ALD process. However, we discuss and compare the differences between the films obtained using the two chamber configurations, in order to verify that the obtained HZO shares the same properties. A Plasma configuration is needed to enable the direct integration of the obtained HZO with, e.g. TiN, where a Plasma-assisted process is necessary.

For this experiment, an ALD instrument, namely the Beneq TFS 200 (Figure 3.1), was utilized. The precursors used were tetrakis(ethylmethy-lamino)zirconium(IV) (TEMA-Zr) and tetrakis (ethylmethylamino)hafnium (TEMA-Hf) (Figure 3.3), while H_2O served as the reactant. Following the pulsing of each precursor, excess impurities were purged using N_2 gas.

Figure 3.2 provides a schematic representation of the Beneq TFS 200 ALD instrument, showing the gas lines and valves involved in the ALD process. The diagram displays the pressure of the chamber and reactor, the flow rate of N_2 and the temperature setpoints of the reactor and heated precursor containers. Notably, the ALD system consists of various components interconnected by gas line, including the Reactor, Hot1, Hot2, Liquid1, and Liquid2. The reactor is where the reaction happens, covering the substrate, Hot1 and Hot2 are heated precursor containers, able to be heated up to 200°C. The first one is filled with TEMA-Zr, while the second carries TEMA-Hf. (Figure 3.3), which are the precursors to

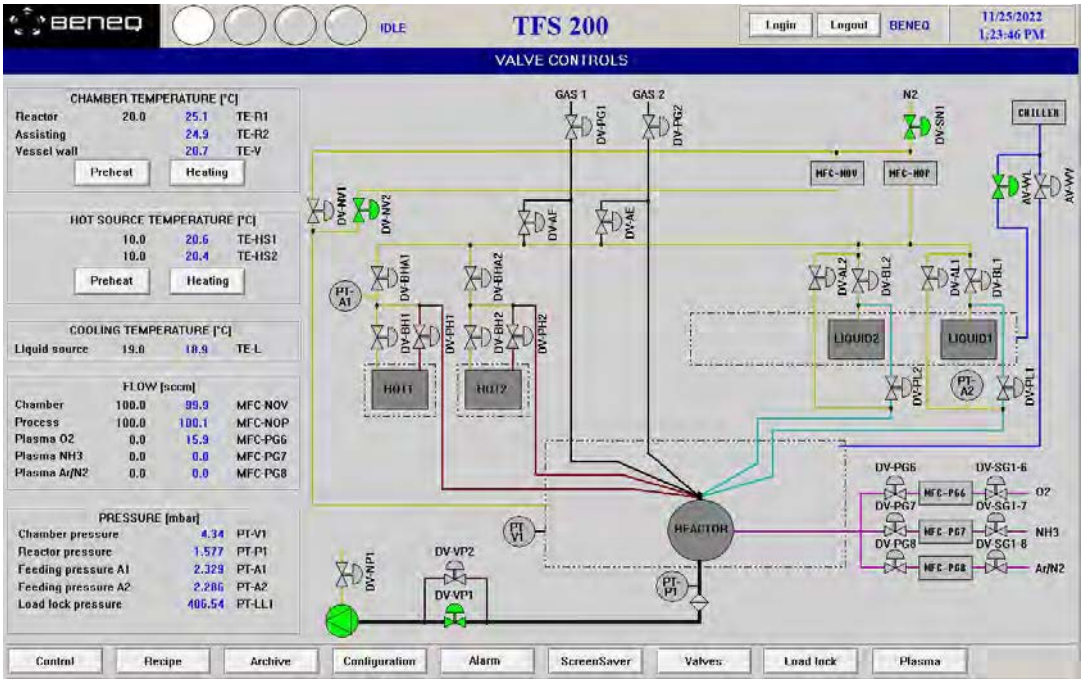


Abbildung 3.2: *ALD valves window*

be deposited. During the experiment, the valves corresponding to the desired precursors are opened for a certain period of time, allowing the precursors, carried by N_2, to flow through the tubes and reach the reactor, where the deposition process takes place. The deposition mechanism will be explained with aid of accompanying illustrations in chapter 4. The Liquid 1 precursor container is filled with ultrapure water and kept at a constant temperature of 20°C, which serves as a precursor forming an oxide film through chemical bonding with Hf and Zr. In this thesis, Liquid 2 was not used.

N_2 gas is connected to MFC-NOV and MFC-NOP mass flow controllers. MFC-NOP is connected to Hot1 and Hot2, acting as a carrier gas to facilitate the transport of precursors into the reactor. By injecting N_2 into the precursor containers, the MFC-NOP assists in transferring the Hf and Zr precursors from the chamber to the reactor because, even if heated, their vapor pressure alone is insufficient to achieve the desired precursor quantity However, the vapor pressure alone is insufficient to obtain the desired precursor quantity in the reactor. Subsequently, the valve is opened, and the precursor mixture is pulsed into the reactor.

Furthermore, N_2 gas plays an another important role in the ALD process by ensuring that the pressure inside the reactor remains higher than that of the chamber, preventing precursors from leaking outside the reactor. Additionally, N_2 gas facilitates to removal of unwanted impurity particles by continuously circulating within the equipment.

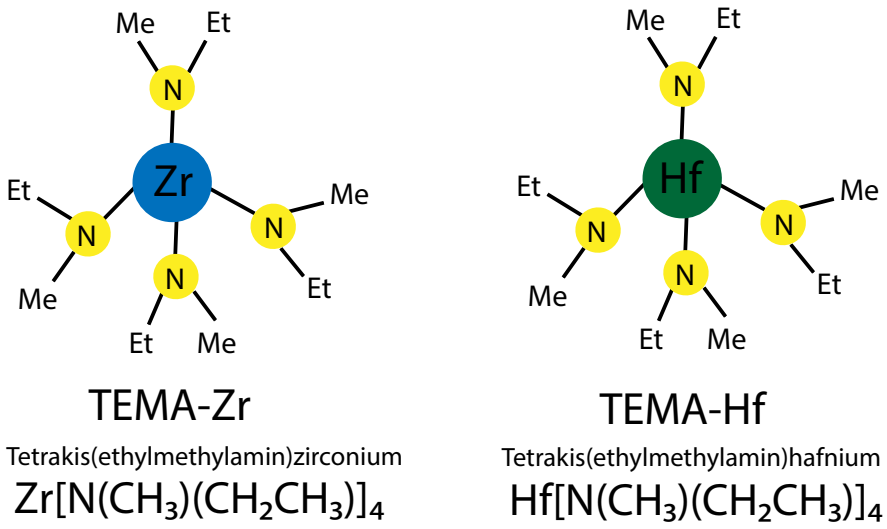


Abbildung 3.3: *Molecules of Zr precursor and Hf precursor*

3.1.3 Photolithography

Photolithography is a crucial process for patterning structures by exposing a photoresist to UV-light. The primary objective of this process is to accurately create the desired mask at the intended location on the wafer, with precise shape and size.

The photolithography process consists of three essential steps: coating, exposure, and development. Initially, a photoresist (PR) is uniformly applied onto the prepared wafer during the coating step. To achieve even and thin coverage, the wafer is subjected to spinning at 6000 rpm for 35 seconds. Subsequently, any residual solvent is removed by heating the wafer on a hot plate at 100°C. Following the coating step, the wafer is placed on the Maskless Aligner MLA 150, a precision instrument manufactured by Heidelberg Instruments. The alignment process ensures the accurate engraving of the desired pattern onto the photoresist at the intended location. Subsequently, in the exposure step, the photoresist on the wafer chemically reacts upon exposure to UV-laser.

Three types of photoresists are commonly used: positive photoresist, negative photoresist, and image reversal photoresist. Positive photoresist exhibits increased solubility upon UV-light exposure, and it is subsequently removed during the development process. Therefore, the unexposed portion of the photoresist remains on the sample. Conversely, negative photoresist hardens upon exposure to UV-light and remains after development, resulting in the removal of the mask's non-exposed regions. Image reversal resist can be processed in both positive and negative modes, allowing for the removal or retention of the illuminated areas, depending on the desired outcome.

The developer used in this experiment is AZ 5214E, a mixture of 2.8% TMAH (tetramethylammonium hydroxide) and H_2O. The wafer is immersed in the developer for approxi-

mately 17-18 seconds, followed by two rinses with deionized (DI) water.

Abbildung 3.4: *Photolithography MLA150 in cleanroom*

3.1.4 Sputtering

Sputtering is utilized as a method to create thin films of TiN on a substrate surface. Sputtering involves eroding a target material, in this case, TiN, through a gaseous plasma. Inside the vacuum chamber, the environment is evacuated to prevent the deposition of impurities and to facilitate the formation of plasma. Argon gas is then introduced into the chamber as the source gas. When a high DC voltage is applied, the argon gas undergoes ionization, forming electro ns, positive ions, and a plasma state. The positively charged argon ions are accelerated towards the cathode target, which is the TiN material. As a result of these collisions, TiN particles are detached from the cathode target and deposited onto the substrate, which is a silicon wafer.

The selection of TiN as the target material is based on its ability to promote the highest ferroelectric phase density. By sputtering TiN onto the substrate, we aim to create a thin film with the desired properties.

3.1.5 Rapid Thermal Annealing (RTA)

Rapid Thermal Annealing (RTA) is a process employed to quickly increase the sample temperature by hundreds degree per second. In this technique, infrared radiation emitted by a tungsten halogen lamp is directly supplied towards the wafer, effectively raising its thermal energy. RTA is commonly utilized for annealing purposes, which involve heat treatment to modify material properties.

In semiconductor device manufacturing, annealing plays a role in the activation of ion-implanted impurities within a silicon wafer. It facilitates the realignment of displaced silicon atoms caused by the implantation process. However, in the context of this experiment, as explained in the theoretical section, annealing is employed to crystallize the HZO layer under an inert atmosphere. Both HfO_2 and HZO have different phases depending on the temperature. Above a certain temperature, the amorphous material undergoes a phase transition, transforming into a crystalline structure. This crystallization process is essential for achieving ferroelectric behavior.

In the conducted experiment, annealing was performed using a UniTem Model UTP1100

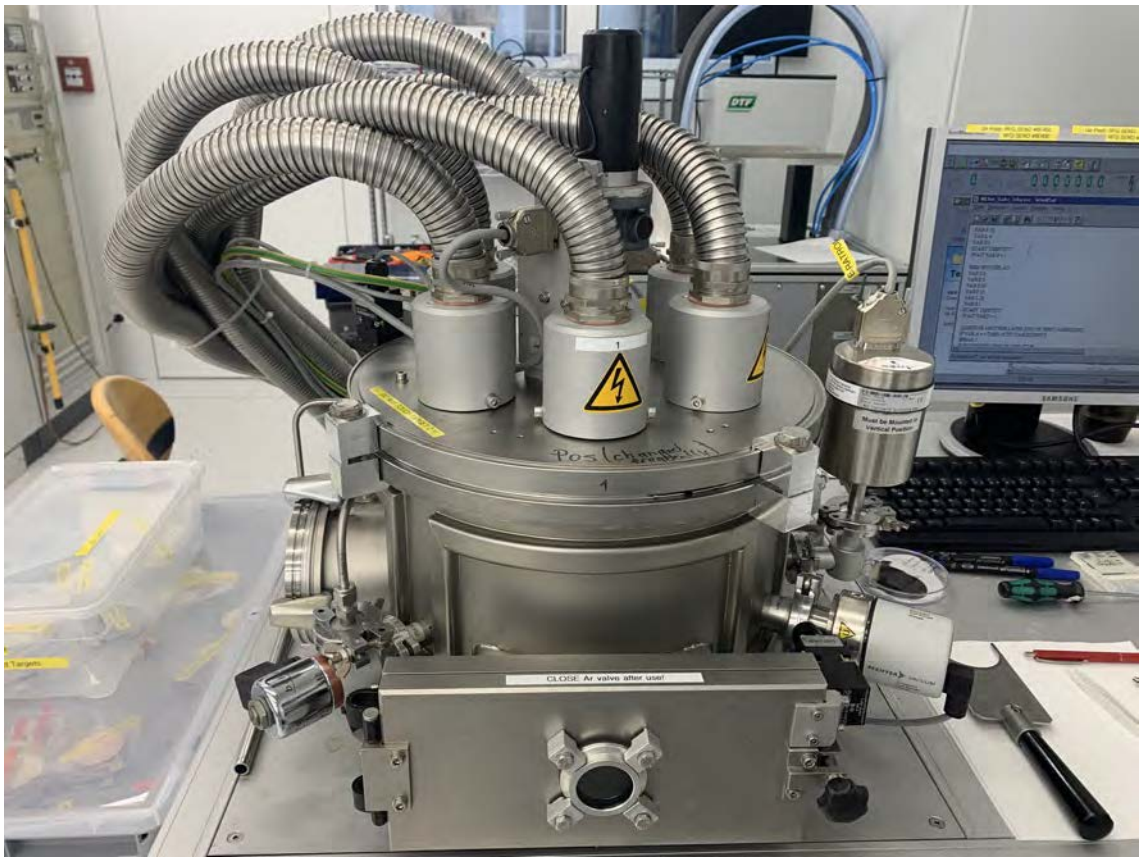


Abbildung 3.5: *Sputter in cleanroom*

oven. This oven is capable of rapidly raising the temperature from room temperature to 1000°C at a heating rate of 75 °C/s. The annealing process begins by evacuating the oven to create a vacuum, followed by the injection of pure N_2 gas. This vacuum and gas injection sequence is repeated three times to ensure the oven is filled with pure N_2 atmosphere. Subsequently, the sample is rapidly heated up to the desired temperature, in this case, 500°C, and annealed for a duration of 3-5 minutes.

3.2 Characterization

3.2.1 X-ray Photoelectron Spectroscopy

X-ray Photoelectron Spectroscopy(XPS) is a surface-sensitive spectroscopic technique analysis technique used to obtain quantitative atomic composition and chemical bonding information. It operates based on the principles of the photoelectric effect originally described by Einstein. When the sample under analysis is irradiated with photons of energy $h\nu$, electrons from the core levels are ejected, referred to as photoelectrons. During this process, both the binding energy (BE) holding the electron in the chemical bond, and the work function (Φ) of the material are surpassed, resulting in the emission of the photoelectron with a kinetic energy (KE) given by the following formula 3.1. The kinetic energy (KE) of the emitted photoelectron is measured using XPS.

The relationship between these quantities can be expressed by the equation:

$$KE = h\nu - BE - \Phi \tag{3.1}$$

By inverting this equation, the binding energy of the electron can be determined. The work function of the sample does not need to be known, since the sample and the analyzer share the same grounding potential. Since the binding energy has an each element, the elemental composition of the sample can be determined using XPS. In addition, as the binding energy varies depending on the chemical bonding state, XPS can also provide information about the chemical bonding configurations.

Due to the strong energy absorption of photoelectrons by air and other molecules, XPS measurements require an high vacuum environment (approximately $1.0\text{x}10^{-7}$ mbar or better) to ensure accurate measurement. The instrument used for XPS analysis includes a PHOIBOS 100/150 analyzer, as shown in Figure 3.6, which allows for precise detection and analysis of photoelectrons emitted from the sample surface. The X-ray photons are generated using a SPECS X-ray source XR50.

X-ray photoelectron spectroscopy (XPS) apparatus was integrated to the atomic layer deposition (ALD) loadlock system seamlessly as dipicted in Fig. 3.7 . This sophisticated configuration thoroughly designed to ensure the efficient and contamination-free transfer of samples from ALD chamber to the ultra-high-vacuum (UHV) side of the XPS instrument.

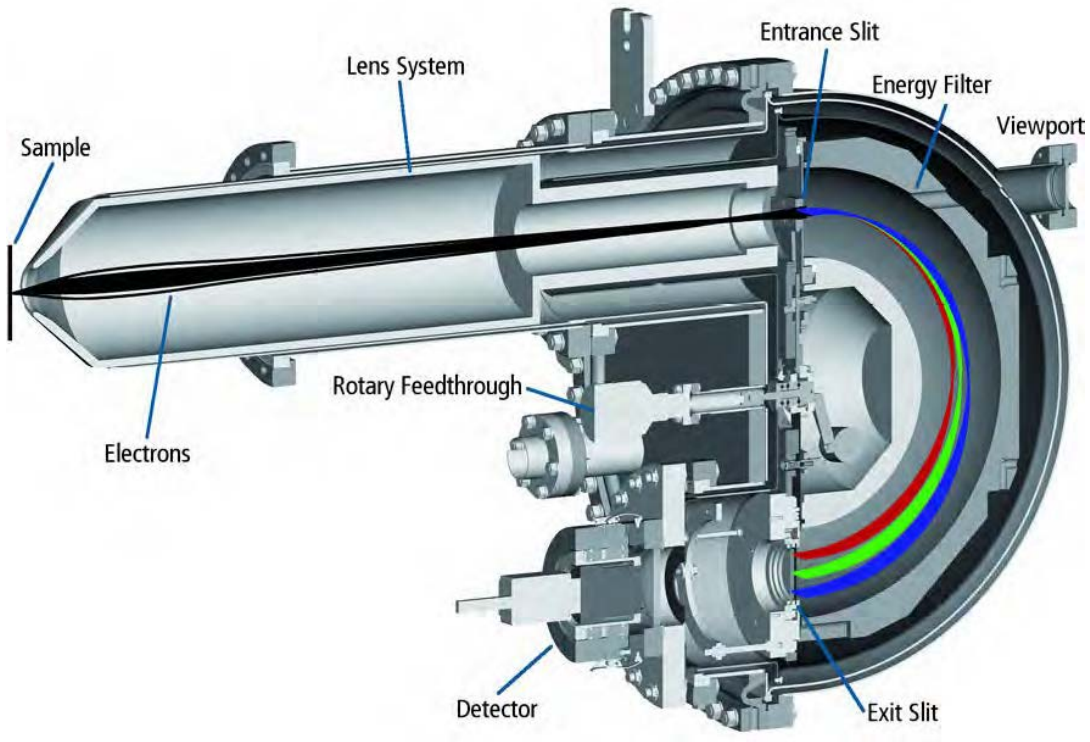


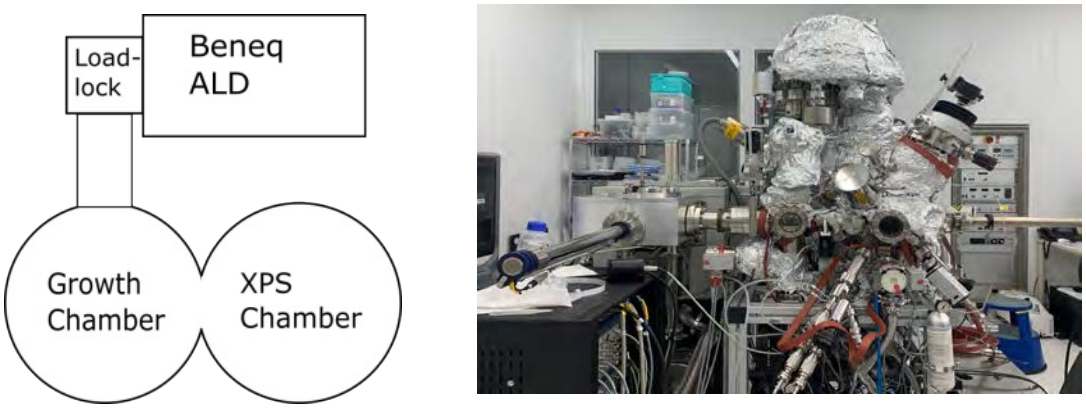
Abbildung 3.6: *Cut-out view of PHOIBOS 100/150 analyzer [35]*

By establishing a direct connection between two systems, we significantly reduced the risk of sample exposure to atmospheric contamination, preserving the pristine surface conditions necessary for accurate and reliable XPS analysis.

3.2.2 Ellipsometry

Ellipsometry provides information about optical properties, such as thickness and refractive index of thin films. It operates by measuring changes in the polarization state of light. When light with a known degree of polarization is irradiated onto the sample, its polarization state is altered upon reflection or transmission. These changes are quantified by the ellipsometer detector and expressed as the parameters Psi (Ψ) and Delta (Δ). Ψ represents the amplitude ratio, and Δ corresponds to the phase difference.

However, directly obtaining the thickness and refractive index from these measured values is not possible. Instead, a model is employed to fit the acquired data.The model takes into account the physical properties of the sample, such as the substrate, thin film optical properties and film thickness. Through a fitting process, the model parameters are adjusted to best match the acquired data to the theoretical model. The fitting procedure aims to minimize the difference between model and the actual measured values. Once a good fit is achieved, the resulting model parameters provide information about the refractive index, extinction coefficient and thickness of the thin film.



(a) (b)

Abbildung 3.7: *(a) shows a pictograph to better show the different components and their location. The system is made out of 2 UHV chambers interlocked together (Growth Chamber and XPS chamber), which are connected to a Beneq plasma enhanced ALD through a loadlock. [36] (b) shows actual system of apparatus.*

In our analysis, the thin film of HZO deposited using atomic layer deposition (ALD) was characterized using a visible range spectroscopic ellipsometry manufactured by Woollam (ALPHA-SE ELLIPSOMETER). The acquired Psi and Delta values were fitted using a Cauchy model, allowing us to extract the refractive index (n) and thickness of the film.

3.2.3 Atom Force Microscopy

Atomic Force Microscopy (AFM) is a surface characterization technique that utilizes a probe to observe and analyze the surface at the atomic level. It provides a non-destructive method for examining the local properties of a desired material with high precision and generates detailed surface topographic images at the nanoscale.

The operational principle of AFM involves bringing a sharp probe tip into proximity with the surface material. As the tip scans across the surface, it interacts with the material, detecting changes in surface properties and metrology, down to the atomic level. The precise control of the probe's movement enables the creation of high-resolution images and the measurement of surface characteristics.[37]

AFM finds application in various areas, including the measurement of width and height in etched patterns of semiconductor circuits, the reconstruction of three-dimensional surface topography, and other post-processing steps following photolithography. As the size of patterns on silicon wafers continues to decrease, accurate measurements of the actual size, depth, width, and shape of these patterns become essential. AFM allows for precise three-dimensional measurements of complex wafer surfaces, facilitating the replication of fine structures without damaging the surface. Furthermore, AFM plays a crucial role in the identification of surface defects and the analysis of semiconductor defects. Even small defects can significantly impact the yield of semiconductor circuits, making defect analysis

Abbildung 3.8: *Ellipsometery in cleanroom*

and characterization using AFM indispensable.

In this experiment, AFM was utilized to investigate the crystal morphology of the HZO thin film deposited and subjected to heat treatment. By imaging the surface of the HZO thin film using AFM, the crystal structure of the material could be examined and evaluated.

3.2.4 Current-Voltage Cascade, Keithley 4200

We have used the Cascade AttoGuard Summit 11000 AP which is for the capacitance-voltage measurement connected to the Keithley 4200 analyzer.The capacitors were analyzed using this setup.

Once the capacitor is fabricated through the previous processes, it undergoes electrical characterization. The sample is positioned on the probe station, which includes a cascade needle holder. The cascade needle holder consists of four needle holders for Source-Measure-Units (SMUs). One of these needles are fixed on the pads corresponding to the top electrode, while the other is fixed on the material corresponding to the back gate. A microscope is positioned on top of the cascade to aid in the precise positioning of the needles onto the micrometer-scale pads. Under microscopic observation, the sample's position is adjusted to ensure accurate placement of the needles on the pads.

For the C-V measurements, the analyzer is configured to sweep the voltage applied onto the top gate while applying a AC modulation, with a between 20 kHz and 100 kHz frequency (f_signal) and amplitude.

3.2.5 Polarization-Sawyer tower circuit

The Polarization-Sawyer Tower circuit, proposed by Sawyer and Tower in 1930, is a widely used method for measuring Polarization-Voltage (P-V) hysteresis loops in ferroelectric materials, which is depicted in Figure 3.9.[3][38][39] The circuit consists of connecting the ferroelectric capacitance (sample capacitor, C_S) in series with a reference capacitor (C_{ref}), which has a much larger capacitance. This configuration allows us to ignore the voltage drop across the reference capacitor, making the voltage across the sample nearly equal to the voltage from the function generator.

To calculate the electric field (E) applied to the sample, we use the input voltage and the thickness of sample(t) as follows:

$$E = \frac{V_{input}}{t} \tag{3.2}$$

To create the P-E hysteresis loop, we measure the voltage across the reference capacitor (V_{output}) and calculate the electric charge (Q) and the surface area (A) of the sample. Using these values, we determine the electric polarization (P) of the material:

$$Q = \frac{V_{output}}{C_{ref}} \tag{3.3}$$

$$P = \frac{Q}{A} \tag{3.4}$$

For accurate measurements, the capacitance of the reference capacitor (C_{ref}) must be much larger than that of the sample capacitor (C_s). The typical ratio used is $C_{ref} = 1000C_s$. The sample capacitance (C_s) can be calculated based on material properties like relative permittivity (ϵ_r), sample radius (r), and sample thickness (t):

$$C_s = \frac{\epsilon_r \epsilon_0 \pi^2}{t} \tag{3.5}$$

This setup and calculations allow us to characterize the P-V hysteresis behavior of ferroelectric materials.

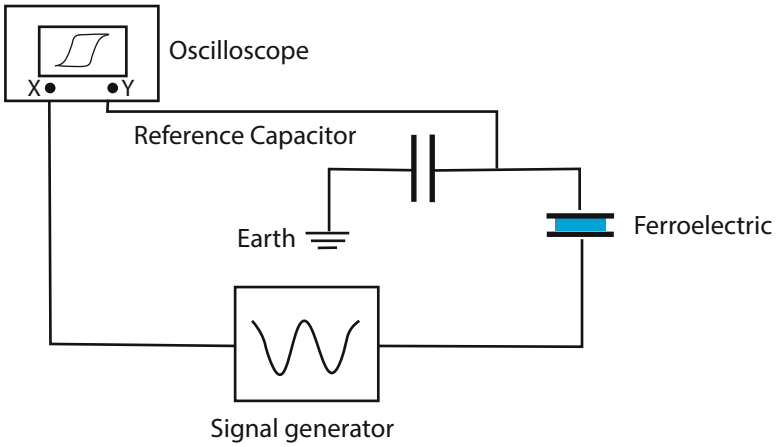


Abbildung 3.9: *The Sawyer Tower Circuit [39]*

Kapitel 4

Results and Discussion

In this chapter, the structure and characteristics of the samples produced and the results of physical and electrical analysis are presented.

4.1 HZO integration into Metal-Oxide-Metal (MIM) Capacitor

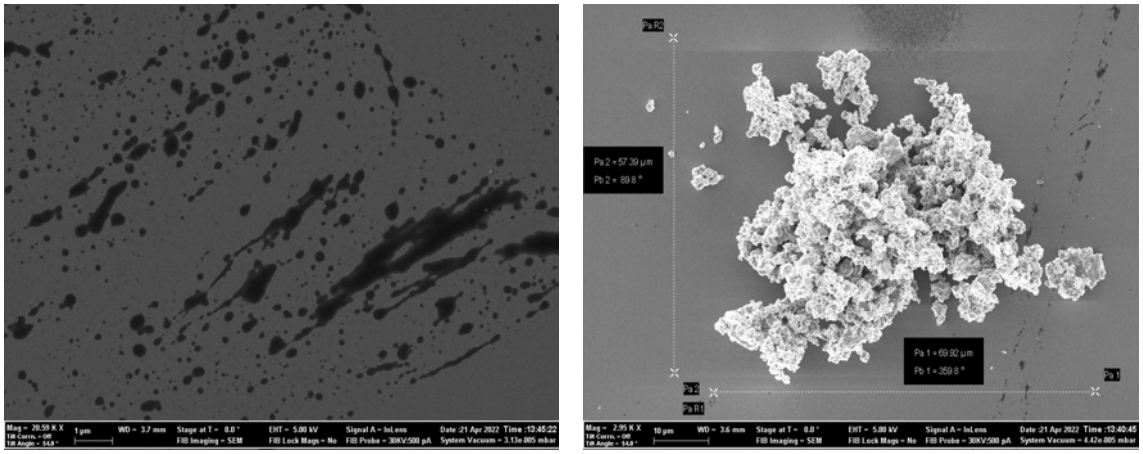
4.1.1 RCA cleaning

The experiment showed that the application of the RCA cleaning process had a significant impact on the obtained results. Initially, the experiment was conducted without the RCA cleaning process and the surface of the samples was analyzed under a microscope. The analysis revealed the presence of numerous impurities on the surface, which had a detrimental effect on the performance of the samples, which are depicted in Figure 4.1. Specifically, it resulted in low capacitance and an unconformable butterfly-shaped curve in the capacitance-voltage (C-V) measurements. To confirm this observation, Scanning Electron Microscopy (SEM) was employed. The impurities, including organic matter, on the metal surface hindered the deposition of HZO, leading to an uneven and rough surface. This, in turn, caused durability issues and prevented the observation of a clear butterfly-shaped C-V curve.

To address this issue, the RCA cleaning process was implemented. The RCA-1 process was utilized to remove chemical and physical residues such as dust, impurities, and organic matter from the surface of the Si wafer. Subsequently, the RCA-2 process was employed to eliminate metal ions.

The RCA cleaning process proved to be crucial in achieving a clean and suitable surface for subsequent processes. It played a vital role in increasing the yield and resulted in improved

surface quality and reliable measurements of the C-V curve.



(a) (b)

Abbildung 4.1: *These SEM images were captured after depositing a thin HZO film on an Si substrate without RCA cleaning. (a) This image reveals numerous unidentified particles with black spots. (b) A magnified section of the images in (a) highlights the morphology of these black spots, which hinders the production of a uniform and flat thin HZO film.*

4.1.2 Thickness series

In order to understand the electrical properties of HZO films, the dielectric constants of Hafnium Oxide (HfO_2) and Zirconium (ZrO_2) were experimentally measured. This was done to directly evaluate the quality of the Hf and Zr materials used in the laboratory and confirm their dielectric characteristics.

Dielectric samples were prepared by depositing HfO_2 or ZrO_2 thin films on Si substrates to form capacitors. This films were deposited at thicknesses of 5 nm, 10 nm, 15 nm, and 30 nm, respectively and the thickness of the native SiO_2 layer on the highly-doped Si substrate was approximately 2 nm, as measured by spectroscopic ellipsometry. The deposition of HfO_2 or ZrO_2 was carried out using Atomic Layer Deposition (ALD) techniques, as described in section 3.1.2. After defining the pattern for the top electrode using photolithography, a metal gate of TiN was deposited on top of the oxide layer.

The capacitance of the samples was measured using a Keithley 4200 instrument, which allowed for the measurement of capacitance from oxides. The capacitance provides information about the dielectric constants of the HfO_2 or ZrO_2 films.

To determine the dielectric constants, capacitance measurements of the samples were performed. The measured capacitance is called equivalent capacitance, which is composed of three capacitors in series: one for the highly-doped Si substrate, one for the native SiO_2 layer (referred to as C_{int}), and one for the HfO_2 or ZrO_2 layer (referred to as C_{ox}). Since the capacitance of the highly-doped Si substrate is significantly larger than the other two

capacitance values, it can be considered as a "conductoränd thus ignored in the calculations. Consequently, the equivalent capacitance C_{eq} can be calculated as follows:

$$\frac{1}{C_{eq}} = \frac{1}{C_{int}} + \frac{1}{C_{ox}} + \frac{1}{C_{Si}} \tag{4.1}$$

However, since the capacitance of the highly-doped Si substrate (C_{Si}) is infinite, it results in $\frac{1}{C_{Si}} = 0$, simplifying the equation to:

$$\frac{1}{C_{eq}} = \frac{1}{C_{int}} + \frac{1}{C_{ox}} \tag{4.2}$$

The equivalent capacitance (C_{eq}) was calculated using this formula 4.1 :

$$C_{eq} = \frac{C_{ox} \cdot C_{int}}{C_{ox} + C_{int}} \tag{4.3}$$

Furthermore, the capacity of a parallel plate capacitor can be calculated using the equation 2.3.

$$d_{ox} = (\epsilon_0 A \epsilon_{ox}) \frac{1}{C_{eq}} - d_{int} \frac{\epsilon_{ox}}{\epsilon_{int}} \tag{4.4}$$

By combining these two equations (4.3 and 2.3), the thickness of the oxide layer (d_{ox}) can be determined as a function of reciprocal of the equivalent capacitance ($1/C_{eq}$) (4.4). A linear fit is performed on the resulting equation, and the slope of the fitted line provides the product $\epsilon_0 A \epsilon_{ox}$. The slope obtained from the fit allows for the determination of the dielectric constant (ϵ_{ox}) of HfO_2 or ZrO_2, taking into account the associated error range.

The fitting results revealed that the dielectric constant of ZrO_2 was determined to be 27 ± 2, while that of HfO_2 was found to be 20 ± 1. The reference values for ZrO_2 and HfO_2 dielectric constant were reported as 32 [40] and 23[41], respectively. The samples I analyzed are predominantly amorphous because no post-deposition annealing was carried out. As a result, the reference data, which is based on a crystalline structure, exhibits a higher dielectric constant.

Based on the fitting results, we have calculated the dielectric constants of SiO_2. For HfO_2, the value obtained was approximately 2.56, and for ZrO_2, it was around 3.56. As a well-known reference, the dielectric constant of SiO_2 is 3.9. Interestingly, ZrO_2 exhibits a reasonably similar dielectric constant to SiO_2.

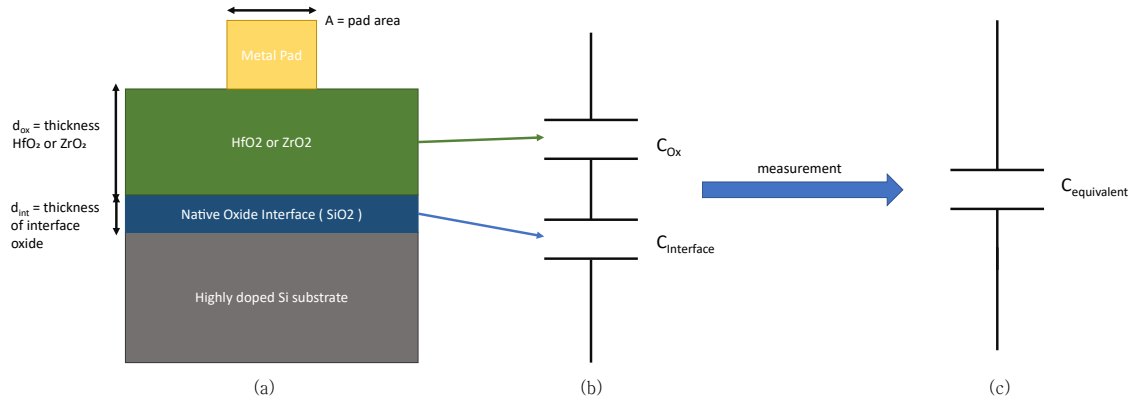


Abbildung 4.2: *Simple diagram of capacitor and capacitance equivalent*

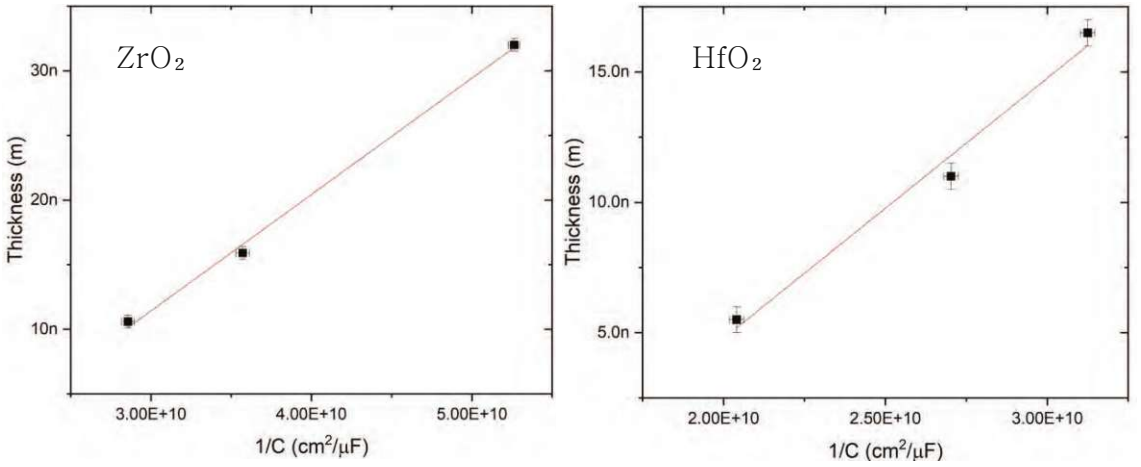


Abbildung 4.3: *Fitting graph of HfO_2 and ZrO_2 with the x-axis as 1/capacitance and the y-axis as thickness*

4.1.3 HZO deposition

The deposition of the HZO layer is performed using the atomic layer deposition (ALD) process, combining the processes for HfO_2 and ZrO_2 studied earlier. This technique allows for precise control of the film thickness and uniformity by alternating the pulses of chemical precursors and purging steps. Two precursors, TEMA-Hf and TEMA-Zr, are used for the deposition of HfO_2 and ZrO_2, respectively, and H_2O is used as the reactant.

Figure 4.4 illustrates the ALD cycle for the Zr-oxide process. The substrate surface, terminated with OH groups, undergoes the following steps:

1. Pulsing of TEMA-Zr precursor onto the surface

2. Purging with N_2 gas to remove unreacted precursors and by-products

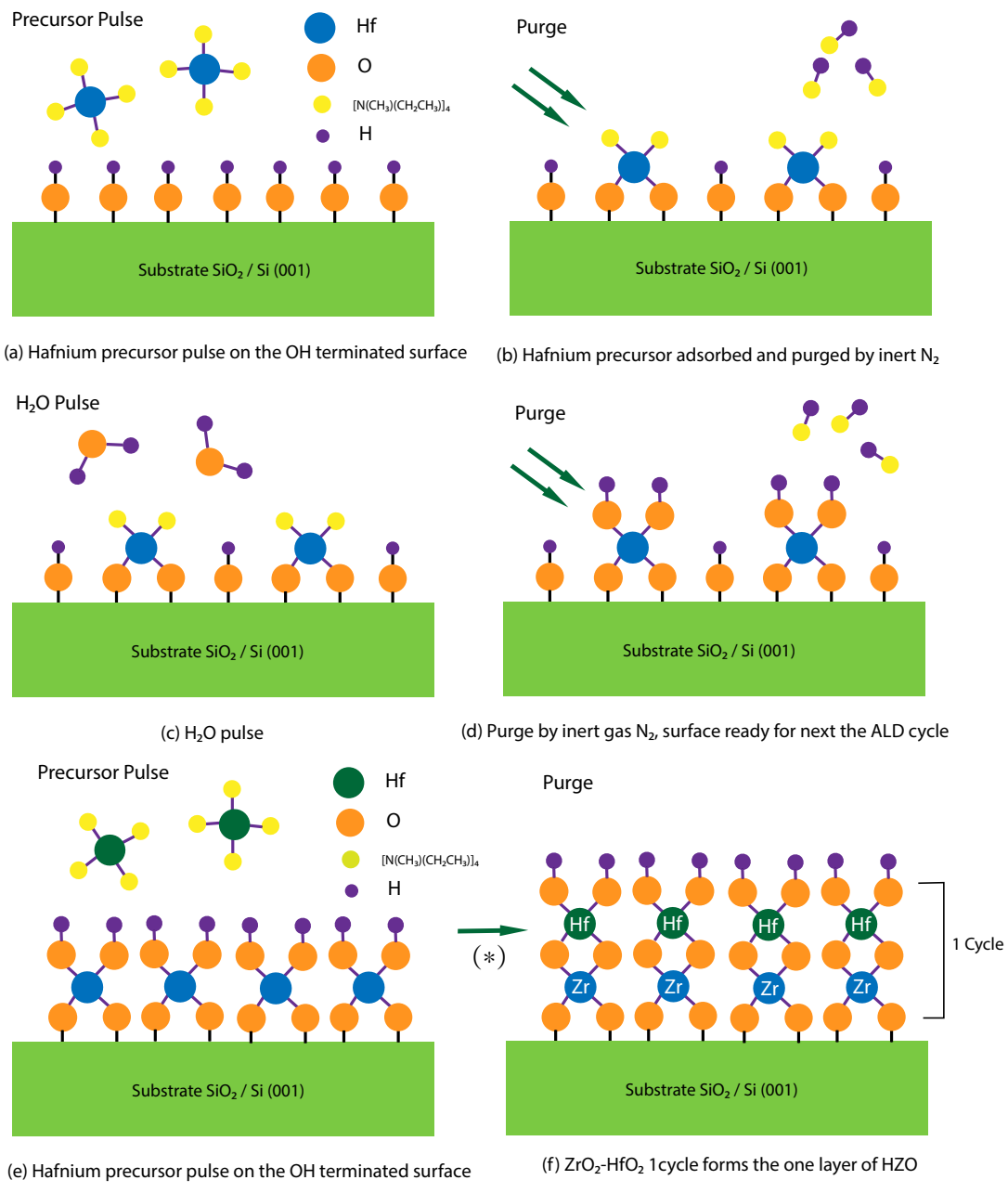


Abbildung 4.4: *(a)-(d) Schematic illustration of an ALD cycle of a Zr-oxide process where Zirconium precursors and H_2O are alternately pulsed and separated by inert N2 gas pulsing. (e), (f) Schematic illustration of an ALD cycle of a Zr-Hf-Oxide process. Image adapted from [42]*

3. Pulsing of H_2O precursor onto the surface

4. Purging with N_2 gas

This cycle results in the deposition of one layer of ZrO_2. The self-limiting behavior of the precursor ensures that only a monolayer of material is deposited per cycle.

Similarly, the Hafnium precursor, TEMA-Hf, is pulsed onto the OH-terminated substrate surface, followed by purging with N_2 gas. Then, H_2O is pulsed to react with the Hf precursor, forming HfO_2, and the chamber is purged with N_2 gas to remove by-products and residual precursor.

Figure 4.4 shows the ALD cycle for the Zr-Hf-Oxide process, where both ZrO_2 and HfO_2 layers are sequentially deposited to form the HZO film. The optimized parameters, obtained within this work, for the growth of a dense and uniform HZO layer are reported in table 4.1, including temperature and other parameters.

Parameter	**Value**
Process Temperature	250 °C
TEMA-Hf Pulse Time	0.5 s + N_2 Preloading (1.5 s)
TEMA-Zr Pulse Time	0.5 s + N_2 Preloading (1.5 s)
H_2O Pulse Time for HfO_2, Zr_2O	0.175 s
N_2 Purge Time for HfO_2, Zr_2O	2 s
TEMA-Zr Temperature	80 °C
TEMA-Hf Temperature	90 °C
Thermalization time	3-5 min

Tabelle 4.1: *ALD Parameters and Experimental Conditions*

4.1.4 Ellipsometry

After depositing HZO using the ALD process, the film was characterized using visible spectroscopic ellipsometry. The HZO film was grown on a Si substrate, which can be accurately modelled. Initially, the deposition of HZO with alternating layers of HfO_2 and ZrO_2 on a Si wafer was measured. The thickness was found to be 11.76 nm with 78 cycles, and the refractive index at 632 nm was 1.96, in line with the expected results for HfO_2 and ZrO_2.[43] This measurement served as a reference for comparing the later deposited HZO films.

After several HZO deposition, HZO deposition was measured, and the refractive index was compared to the reference model to assess the stability and reproducibility of the process. The newly measured sample showed perfect overlap with the reference model in terms of Psi (Ψ) and Delta (Δ) values, indicating that the HZO deposition using a thermal head is reproducible.

In the ALD process, HfO_2 and ZrO_2 were deposited alternately layer by layer. Each cycle consisted of depositing one layer of HfO_2 and one layer of ZrO_2, resulting in a deposition thickness of 1.7 Å per cycle. The number of cycles was determined based on the desired film thickness. The refractive index at 632 nm was measured to be 1.963, as shown in the Figure (4.6) confirming the uniformity of the ALD deposition.

The ellipsometry data was fitted using an effective medium approximation (EMA) model. To compare the density of the materials obtained from different processes, the HZO material from the first measurement was labeled as "Material 1,änd a "Void"material was selected as "Material 2."The second sample obtained using the thermal head showed a void level of 0%, indicating that the density of the layer is comparable to the first sample. This suggests that there is no density degradation over time with the same machine configuration.

On the other hand, when HZO was deposited using ALD with a plasma head, it did not match the reference model perfectly. Voids were measured at 5%, and the refractive index, measured using a Cauchy model, was 1.916 at 632 nm, which is lower than when using ALD with a thermal head. The refractive index of an ALD-grown film is directly correlated with its density as shown in the Figure 4.6, obtained from "Low-Temperature Al_2O_3 Atomic Layer Deposition"[44], indicating that the density was lower when using the plasma head, which could indicate that for realizing a low-leakage layer the thermal configuration of the available tool is preferable.

There are several possible reasons for the decrease in density when the plasma head was used. The relatively larger reactor space of the plasma head allows the precursor to disperse more, as shown in Figure (4.5), leading to a decrease in precursor concentration on the sample surface and the formation of voids. Additionally, the longer purging time needed in the plasma head configuration may favor the desorption of the precursor, contributing

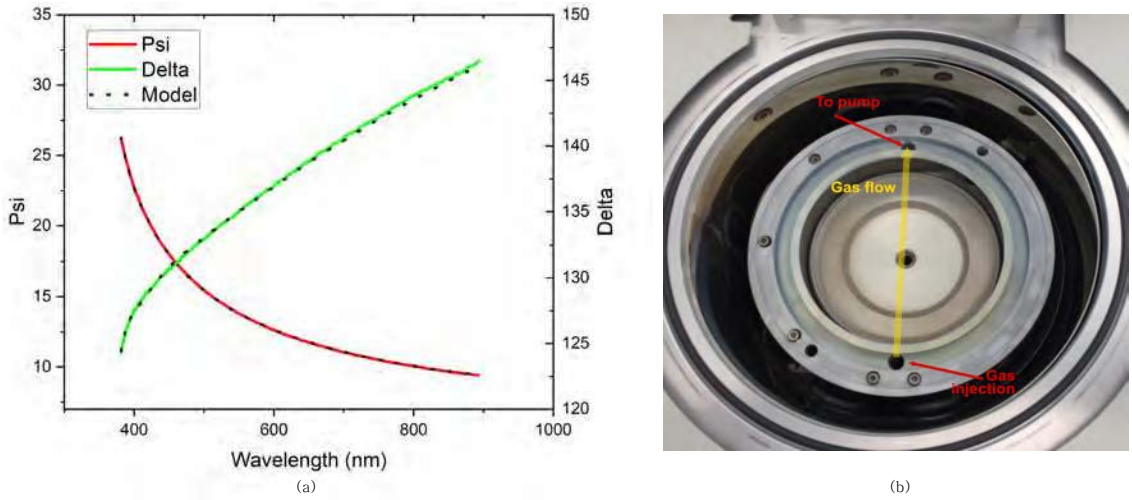


Abbildung 4.5: *(a) Dependence of Δ and ψ on wavelength at plasma head ALD configuration (b) Inside of ALD reactor*

to the decrease in density.

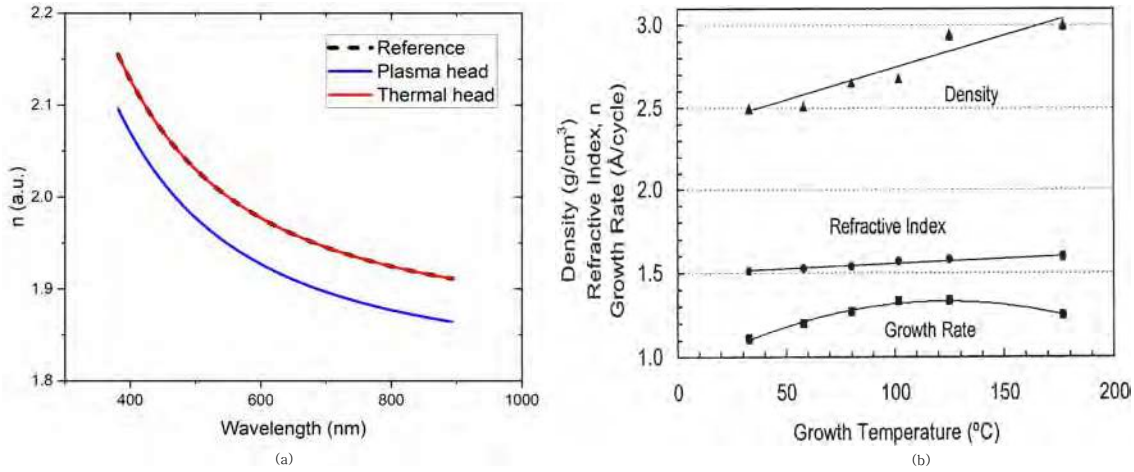


Abbildung 4.6: *(a) Refractive index dependent on wavelenght at each ALD configuration (b) Ellipsometry data for Al2O3 ALD films grown using 300 reaction cycles on Si(100) substrates. The refractive index, growth rate, and density (calculated using ellipsometry and QCM data) are plotted versus growth temperatures from 33 to 177 °C. [44]*

The decrease in density due to voids can result in defects, which can negatively impact yield and reliability, especially in microscopic semiconductor structures. Therefore, efforts should be made to improve the density and minimize void formation. The ellipsometry results confirmed that the thermal head produced a higher-density film compared to the plasma head.

4.1.5 X-Ray Photoelectron Spectroscopy (XPS)

XPS analysis was performed to characterize the chemical composition of the thin oxide film, which is formed by alternating layers of HfO_2 and ZrO_2. The XPS setup was directly connected to the ALD loadloack, ensuring the transfer to the ultra-high vacuum side without exposure to atmospheric contamination.

From the XPS data, information about the chemical state of the elements and their relative quantities in the film can be extracted. The elements Hf, Zr, O, and C were detected through XPS analysis, and the peaks associated with electrons extracted from the Hf4f, Hf4d, Zr3p, Zr3d, O1s and C1s orbitals were characterized. The XPS spectra are shown in Figure **??**, and the corresponding results, including peak positions, areas, and FWHMs, are summarized are summarized in the table 4.6

To identify the elements and bonding states, each result value obtained by XPS was compared to the database of the National Institute of Standards and Technology (NIST) data. The XPS data were calibrated using the signal from the sample manipulator structure, with the Mo3p orbital serving as a reference. The detected position of the Zr 3p3/2 orbital was 333.13 $\pm$ 0.02 eV, close to the NIST value of 332.5 eV for ZrO_2. The Zr 3d orbital peak was measured at 182.4 $\pm$ 0.1 eV, while the NIST value was 182.3 eV. The peak positions are compatible with fully oxidized Hf and Zr, demonstrating that the ALD process is executed correctly.

One advantage of XPS analysis is the ability to perform quantitative analysis of the elements present in the layer. If an element is present on the surface, it will contribute to more than one peak in the XPS spectrum. However, in this case, no peak was detected for the C1s orbital, indicating a low concentration of carbon in the film. The sensitivity of the instrument for carbon in an Hf matrix is approximately 3 at.%, meaning that the measured carbon content is lower than the sensitivity of the instrument. This suggests that the HZO film has high purity, with very low carbon concentration. The presence of high carbon impurities can adversely affect the insulating properties of the film, but the low carbon content confirms the high quality of our film. Monitoring carbon content is crucial for ensuring film quality, as adventitious carbon can result of an insufficient purging step during the ALD process.

In contrast, only one peak was observed for the O1s orbital, which can be entirely attributed to the oxide films. This observation indicates the absence of spurious oxygen on the sample, thanks to the vacuum transfer method used during the analysis process. The absence of spurious oxygen further supports the high purity and quality of the HZO film.

To estimate the relative concentration of each analysed element, the Relative Sensitivity Factor (RSF) is needed. The RSF is an empirically derived factor based on compounds of known composition, and it normalizes the peak intensity to provide atomic concentration. [45] The calibrated area is obtained by dividing the XPS-measured area by the sensitivity

factor, and this value is used to calculate the quantitative ratio of each element on the surface.[46] Since Hf, Zr, and O were detected in the sample, the calibrated area of each element is determined, and the percentage of each element is calculated, as shown in the table 4.2, 4.3, 4.4, 4.5

It was confirmed that the ratio of Zr to Hf in the film was 1:1 as shown in the table. The Zr content was slightly higher, likely because the last layer deposited was Zr.

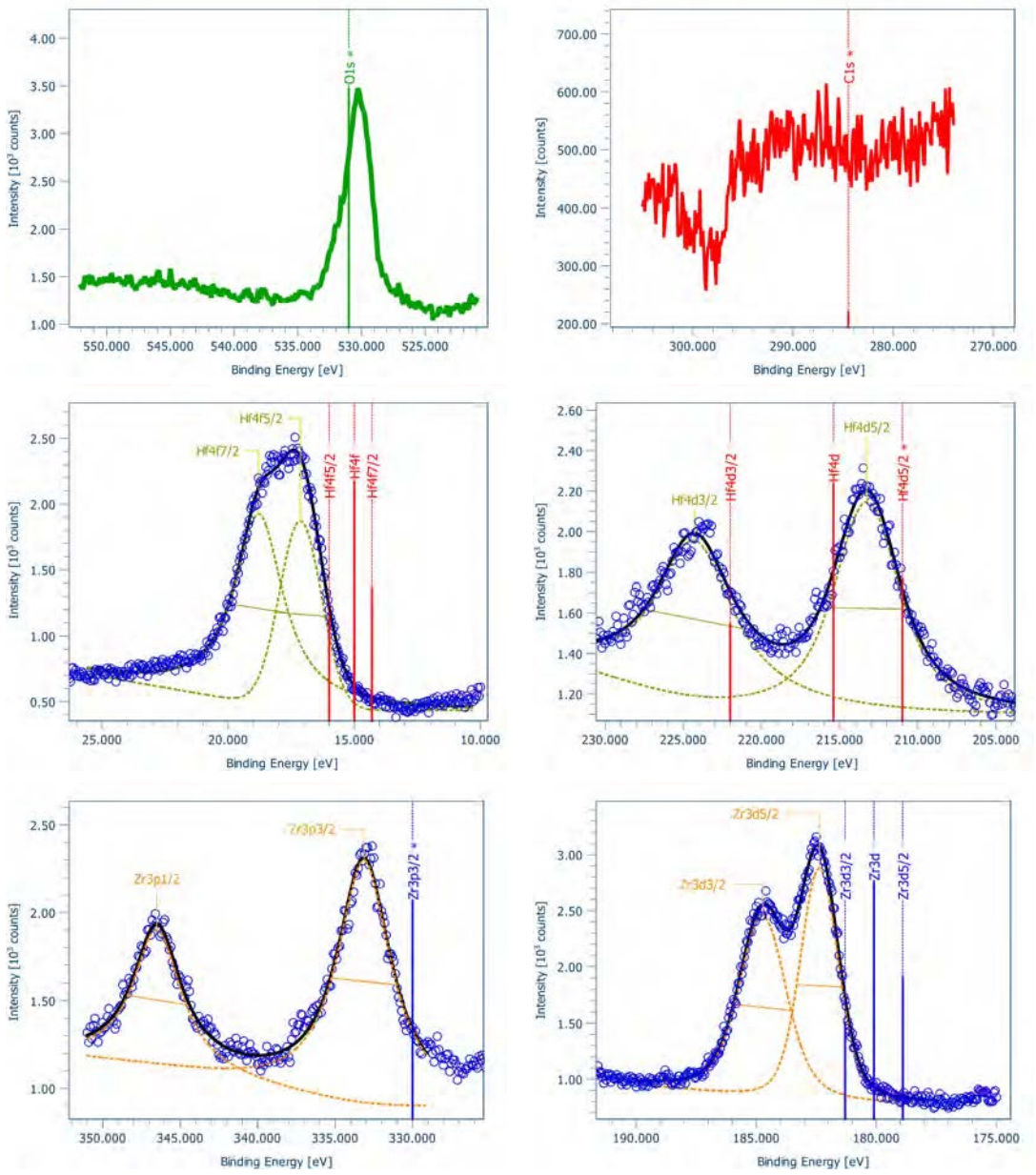


Abbildung 4.7: *XPS Binding Energy Analysis for each orbitals*

Tabelle 4.2: *Zr3p Orbitals*

Transition	Zr3p3/2	Zr3p1/2
Center (eV)	333.13 ± 0.02	346.50 ± 0.03
Area (counts)	9429.005	4674.638
FWHM (eV)	4.228	3.752

Tabelle 4.3: *Zr3d Orbitals*

Transition	Zr3d5/2	Zr3d3/2
Center (eV)	182.4 ± 0.1	184.73 ± 0.01
Area (counts)	4736.13	4895.068
FWHM (eV)	1.892	2.356

Tabelle 4.4: *Hf4f Orbitals*

Transition	Hf4f5/2	Hf4f7/2
Center (eV)	17.13 ± 0.02	18.79 ± 0.03
Area (counts)	2992.701	5343.059
FWHM (eV)	1.969	2.361

Tabelle 4.5: *Hf4d Orbitals*

Transition	Hf4d5/2	Hf4d3/2
Center (eV)	213.27 ± 0.02	224.28 ± 0.04
Area (counts)	7534.772	7760.086
FWHM (eV)	5.002	6.159

	Zr3p	Hf4f	O1s
Total Area	7912	7445	6308
Sensitivity	7.78	7.52	2.93
Quantity	24%	24%	52%

Tabelle 4.6: *Quantitative Analysis of Zr, Hf, and O atom*

4.1.6 Atom Force Microscopy (AFM)

After depositing HZO film, Atomic Force Microscopy (AFM) was used to observe the surface at the nanometer scale. In order to achieve high precision, a flat substrate is required. Normally, TiN is used as a bottom electrode on a Si wafer to make a capacitor before depositing HZO. However, TiN can introduce surface roughness to the substrate, which can result in uneven HZO deposition. To evaluate the surface condition of the HZO film deposited solely through the Atomic Layer Deposition (ALD) process, HZO was directly deposited on a silicon wafer without TiN.

Two AFM measurements were conducted. The first measurement was performed prior to heat treatment (Figure (a) in Figure 4.8), and the second measurement was done after annealing the HZO film by in a N_2 atmosphere at 500°C for approximately 3 minutes (in Figure 4.8 (b)).

The results revealed a significant difference in the surface characteristics. The first measurement showed a generally distributed amorphous surface with particles measuring 1.0 nm or smaller. In contrast, the second measurement exhibited scattered particles ranging from 1 nm to 3 nm in size, which appeared in a crystalline form. The surface roughness of the two measurements was compared using the 'Gwyddion' program. The roughness

before annealing was approximately 200 pm, while after annealing, it increased to 405.6 pm, indicating a twofold increase in roughness due to the heat treatment.

These findings emphasize the importance of heat treatment in the electrical characterization of HZO films, as it promotes molecular rearrangement and crystallization. Crystallization is particularly critical for inducing ferroelectric behavior in the material.

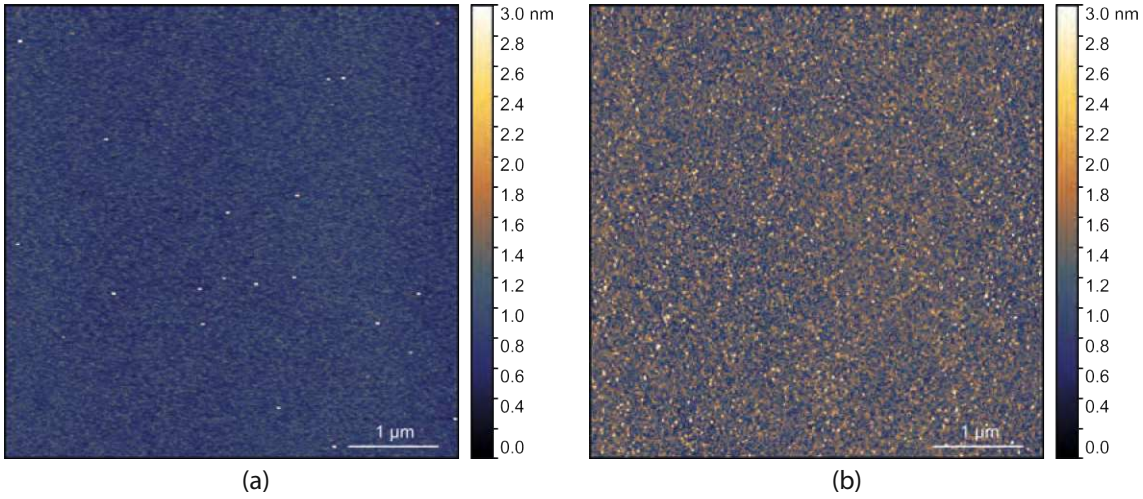


Abbildung 4.8: *(a) AFM Images of surfaces before annealing (b) AFM Images of surfaces after annealing*

4.1.7 Transmission Electron Microscopy (TEM)

The TEM image 4.9 provides crucial insights into the homogeneous distribution of the HZO compound, which is a mixture of Hf and Zr. In the image, Hf is represented by the color red, while Zr is depicted in green. Both the first and second TEM images clearly exhibit a uniform dispersion of the HZO layer, visualized as a yellow color resulting from the combination of red and green. This observation validates the successful execution of the atomic layer deposition process. Furthermore, the TEM image allows for an additional verification of the deposited thickness. Each layer appears to have a similar thickness, approximately 10 ± 1 nm, which aligns with the expected thickness for HZO deposition.

Through TEM analysis, we confirmed the absence of defects and observed a uniform distribution of Hf, Zr, and oxygen across the surfaces. This uniform coverage is critical for ensuring the quality and reliability of the fabricated device. Detecting any defects at this stage would have significant implications for the overall device performance.

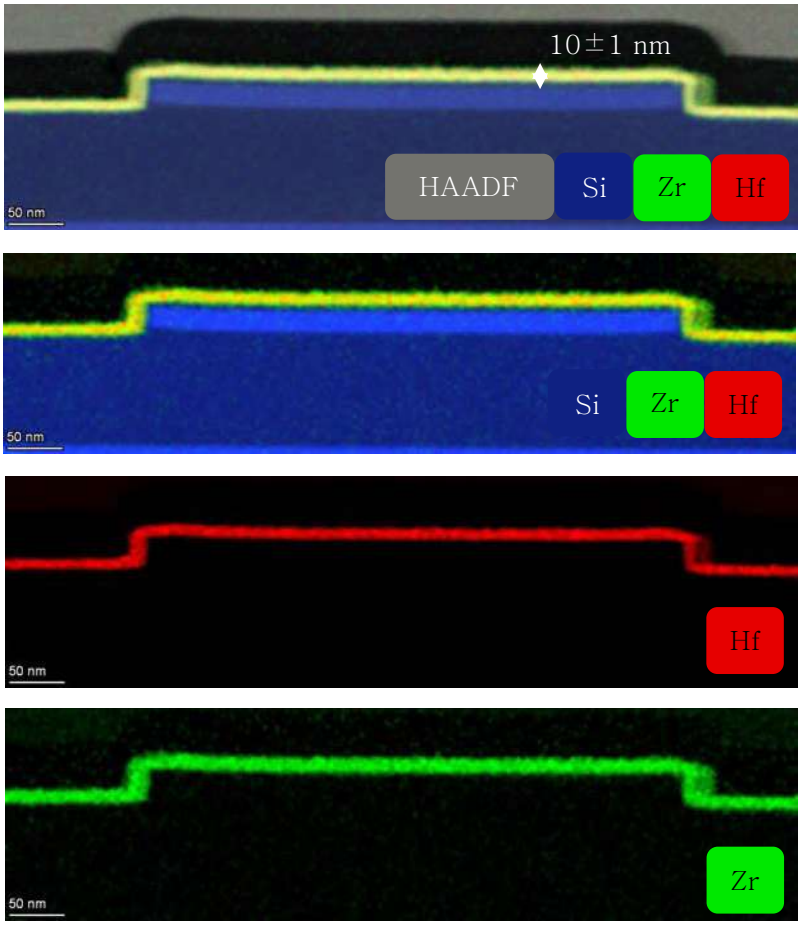


Abbildung 4.9: *Cross-sectional TEM Images of the Capacitor*

4.1.8 HZO C-V and P-V characteristics

In order to measure the capacitance and polarization behaviors, we fabricated metal-insulator-metal (MIM) capacitor involved following steps. After cleaning the substrates and removing the native oxide layer through a buffered HF wet-etching process, TiN was deposited by sputtering as the bottom electrode. Subsequently, HZO was deposited using atomic layer deposition (ALD) to form the insulating layer. The top electrodes were defined through photolithography and realized via TiN sputtering. The stack was then annealed with N_2 gas at 500°C for 3-5 minutes to promote the crystallization of the HZO layer.

After the fabrication process, electrical measurements were conducted to characterize the device. Capacitance-Voltage (C-V) measurements were performed via Keithley 4200 analyzer by applying a voltage ranging from -3.5 V to 3.5 V with a superimposed AC signal with a frequency of 100 kHz and an amplitude of 30 mV. The applied electric field is calculated by dividing the voltage applied by the sample thickness and the capacity values are divided by capacitor area to remove the area dependency. This is plotted as

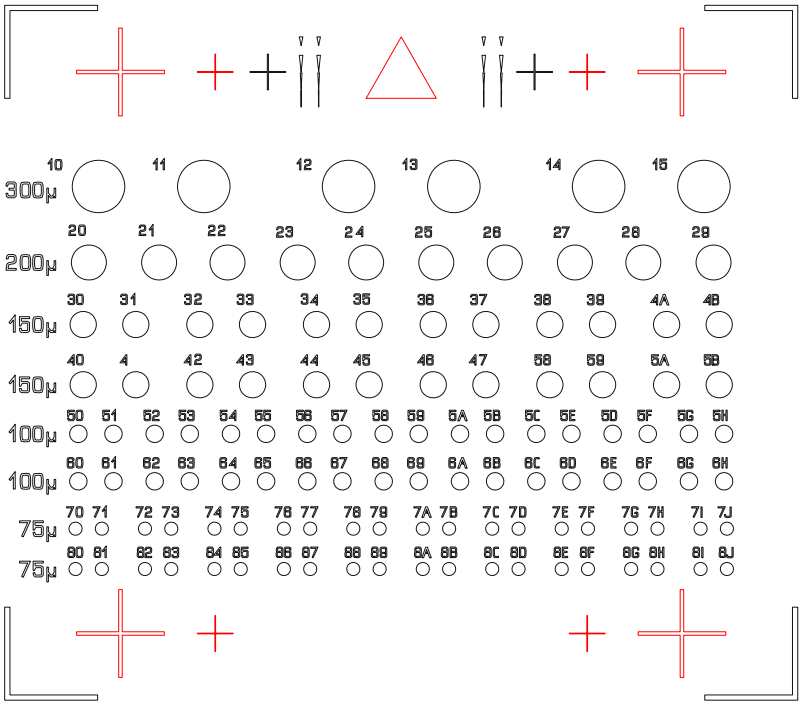


Abbildung 4.10: *Patterned pad image by photolithography for C-V measurement*

a Capacitance-Electric field (C-E) graph. The polarization was also measured using the Sawyer-Tower circuit, which is described in chapter 3.2.5, and the results were presented as a Polarization-Electric field (P-E) graph.

Figure 4.11 shows the most optimal result obtained from the C-E measurement for a top electrode diameter of 75 μm. Two different HZO thicknesses were tested: 8 nm and 15 nm. Both C-E graphs exhibit a symmetrical butterfly shape with a slight shift to the left. When the HZO thickness was 8 nm, the maximum capacitance value of 4.8 μF/cm^2 was achieved at electric fields of 0.8 MV/cm and -0.75 MV/cm. For the 15 nm thickness, the maximum capacitance value was 2.25 μF/cm^2 at electric fields of 0.8 MV/cm and -1 MV/cm. The electric field value at which the maximum capacitance is reached is similar for both thicknesses, but the capacitance is approximately twice as high for the 8 nm thickness compared to the 15 nm thickness. This is consistent with the inverse relationship between capacitance and thickness, as described by the capacitor equation **??**.

The P-E graph in Figure 4.11 shows a typical ferroelectric hysteresis loop as explained in theory part 2.1.2. However it does not start from zero because the material is already preferentially polarized. An coercive field of 1 MV/cm is required to change the orientation of the domains. For the 8 nm thickness, the remanent polarization (P_r) is measured to be 21.3 μC/cm^2, which is similar to or slightly higher than the values reported in the paper[12]. For the 15 nm thickness, the remanent polarization is 19.8 μC/cm^2, indicating that a stronger effect is expected from a thinner ferroelectric layer. Comparing these results

with the C-E graph, it is observed that the peak in capacitance corresponds to the steepest points in the P-E plot. This relationship can be explained by the fact that the capacity of a ferroelectric material is dependent on its polarization value. As the electric field is applied, the initially randomly oriented domains begin to polarize in the direction of the field, and the rate of polarization change affects the capacitance.

From this equation 2.3 where ϵ_r is the dielectric constant of HZO, ϵ_0 is the dielectric constant of vacuum, A represents the area of the pad, and d denotes the thickness of the HZO layer. The dielectric constant ϵ_r of HZO is a function that depends on the electric field, given by the equation

$$\epsilon_r = 1 + \frac{P}{\epsilon_0 E}, \tag{4.5}$$

where P represents the polarization induced in the HZO material and E represents the electric field.

Combining these equations, the expression for capacitance becomes

$$C = \frac{\epsilon_0 A}{d}(1 + \frac{P}{\epsilon_0 E}) \tag{4.6}$$

In the C-V measurements, the capacitance of the MIM device is recorded as a function of the applied electric field (E) within a specific voltage range. This data is typically represented graphically as a capacitance-electric field (C-E) curve. The maximum capacitance is achieved when the polarization P divided by the electric field E (P/E) is at its maximum value, which is depicted in Figure 4.12. This point corresponds to the maximum slope of the tangent line to the polarization-electric field (P-E) curve.

After reaching the maximum P/E value, the increase in capacitance slows down, and the capacitance increases linearly with the electric field. Consequently, the slope of the P-E tangent line decreases, leading to a decrease in the overall capacitance (C).

4.2 HZO integration into Al-Si-Al heterostructures for memory applications

This chapter outlines the fabrication of memory devices obtained integrating a HZO layer into monolithic Al-Si-Al heterostructures. The fabrication process starts from a SOI (silicon-on-insulator). The sequential fabrication steps are summarized in Figure 4.14, highlighting the additional steps compared to the MIM fabrication process.

The SOI substrate consists of a Si handling layer, a 100 nm thick buried SiO2 oxide (BOX) and an unstrained Si device layer, with a thickness of 20 nm (Figure 4.14a). Before starting the fabrication process, the wafer is cleaned following the RCA-1 recipe to remove any particles or impurities. The desired structures, which look like bones as depicted in 4.14o-1, are defined using lithography techniques. This process involves coating the sample with photoresist material(AZ5215), which is an image-reversal resist. The spin-coating process ensures an even distribution of the photoresist on the sample. The laser writer HIMT MLA 150 is then used to pattern the resist layer. In the Figure. 4.14b the unexposed resist appears in red, while the exposed resist is shown in orange. The photoresist is then developed, leading to the removal of the exposed areas (AZ726MIF), leaving the unexposed resist on the sample (Figure 4.14c). Reactive-ion etching (RIE) with a SF_6/O_2 etching gas mixture is employed to etch the Si layer (Figure 4.14d), resulting in the formation of the initial bone-like structures (Figure 4.14 (o) -1).

The next step involves the formation of the high-k dielectric. The gate dielectric layer consists of two sub-layers: SiO_2 and HZO. The SiO_2 layer has the rule of forming a nice, low trap, interface towards the Si channel. The SiO_2 layer with a thickness of 2 nm is formed through thermal oxidation at 900°C, while the HZO layer with a thickness of 9.5 nm is deposited using atomic layer deposition (ALD), as discussed in the 3.1.2 (Figure 4.14d).

Subsequently, the source and drain (S/D) pads are fabricated. A second lithography process is employed, to define the patterns for the S/D pads (Figure 4.14e). The exposed parts of the photoresist are removed, and an RIE process with SF_6/Ar etching gas is performed to etch both the SiO_2 and HZO layers, ideally stopping at the Si channel. This procedure is of difficult calibration, as the etching process is effective also for Si. (Figure 4.14h). To be completely sure that all the SiO_2 is removed, without affecting the Si layer, a final wet etching step is performed, using a buffered HF (BHF, 7:1 ratio) is carried out.(Figure 4.14h). Subsequently, aluminum (Al) is sputtered onto the sample surface, resulting in the deposition of Al on top of the desired S/D pad structures. The photoresist in a lift-off process is below the metal, leaving behind the desired Al layer for the S/D pads (Figure 4.14j and subfigure (o)-2).

The next step involves the structuring of the top gates. Similar to previous steps, a third lithography process is employed. The laser writer defines the desired top gate structures,

depicted as green structures in Figure 4.14(o)-3. The top gate is realized by sputtering a titanium nitride (TiN) layer (Figure 4.14l). After the lift-off process, the TiN layer remains as the top gate structure positioned between the S/D pads (Figure 4.14(o)-3).

To complete the formation of the Al-Si-Al heterostructure, an annealing process is conducted. The sample is annealed for a total of 6-8 minutes using a rapid thermal annealer (RTA) at a temperature of 500°C in N_2 atmosphere. During the HZO crystallized and, at the same time, the Al diffuses into the Si layer. It is crucial to monitor the diffusion process under a microscope every 60 seconds to ensure that the Si is not fully exchanged in the process. The Al-Si interfaces are intentionally positioned beneath the top gate, for optimal control of the barrier height.

4.2.1 Electrical characterization

In this section, we present the electrical characterization of the fabricated device. The experiments were conducted using a Lakeshore PS-100 probe station, connected to a Keysight B 1500a analyzer.

The measurement being performed involves probing the transfer characteristics of the device. First, a voltage pulse is applied to the top gate of the device, ranging from +5 to +7.5 V and then -5 to -7.5 V. This has the function of programming the memory device. After applying the each pulse, the transfer characteristics of the device are analyzed.

During the pulsing of the top gate, the source and drain contacts are kept fixed at 0 volts. This means that the voltage applied to the top gate controls the flow of current between the source and drain channel. By analyzing the transfer characteristics before and after the pulse, the electrical behavior and performance of the device under different operating conditions could be gained, which are plotted in Figure 4.16 (a). The first thing that can be observed is that the transfer characteristics show no hysteresis, clearly indicating that the Si-oxide interface is of extremely high quality, with a low concentration of traps.

It is important to visualize what happens when a voltage is pulsed on the top gate terminal, as plotted in Figure 4.15. Upon applying positive pulsing, the threshold voltage graph of the MOS structure shifted to the right, while negative pulsing caused it to shift to the left, as can be seen in Figure 4.16 (a), (b). Two mechanisms have to be considered, in order to explain the electrical behavior of the MOS structure: the ferroelectric property of HZO and the influence of charge trapping.

Firstly, let's examine the operating mechanism of the ferroelectric. When a positive voltage is applied, polarization occurs within the HZO layer, leading to a negatively charged upper part and a positively charged lower part. This creates a positive charge environment between the SiO_2 layer and the heterostructure Al-Si-Al.

Secondly, the mechanism involving charge trapping is analyzed. There are two interfaces

that are controlled by the applied voltage. One interface is the the Schottky junction between Al and Si in the heterostructure Al-Si-Al, which is depicted in Figure 4.15 (a). Applying a positive voltage, result in a lowering of the Si bands, which lead to a thinning of the junction barrier. As a consequence, electrons move from Al to Si, causing Si to acquire a negative charge.

Another interface is one between the gate oxide and the Si channel, which is depicted in Figure 4.15 (b), assuming a flat band condition at VG = 0 V. The top gate covers the entire device, and when a positive voltage is applied, TiN moves downward due to the band bending, electrons can tunnel through the SiO_2 interface layer into the high-k material, where are trapped.

To further analyze the changes occurring within the device after pulsing, we measured the transfer characteristic of the MOS structure, which are plotted in Figure 4.16 (a). We observed that the threshold voltage shifts to the right, following a positive pulse. This indicates that the presence of electron traps resulted in a higher number of negative charges within the channel compared to the positive charges induced by the ferroelectric property.

When a negative pulse is applied, the opposite behavior can be observed. Based on these experimental findings, we conclude that our fabricated devices operate as a charge trapping memory. The observed increase in threshold voltage with higher applied voltages indicates the presence of electron traps and their impact on the device's electrical behavior.

The following graph in Figure 4.16 (c) presents separate plots for positive and negative pulsing cases. The x-axis represents the absolute value of the applied pulsing voltage, while the y-axis shows the difference between the threshold voltage after the applied pulse, and the threshold voltage of the discharged device.

Upon observing the graph, it exhibits the almost symmetrical shape with respect to y=0V. In the case of positive pulsing, the threshold voltage increases until it reaches approximately 7.0V, beyond which the increase becomes negligible.

To assess the performance of the devices, retention tests were conducted in two different devices. Initially, transfer characteristics were measured for each device before applying negative pulsing. Subsequently, negative pulsing (-7V) was applied, and transfer characteristics were measured at various time intervals, such as 1 minute, 3 minutes, 10 minutes, 20 minutes, 30 minutes, 1 hour, and 24 hours, to monitor the performance of device over an extended duration. The results are presented for two different devices in Figures 4.16 (d) and (e).

From the Figure 4.16 (d), (e), the y-axis labeled as V_{shift} represents the difference between the minimum voltage of the transfer characteristics after pulsing and the minimum voltage

before pulsing. As time progresses in the retention test, this difference gradually converges to zero. This observation indicates that over time, the threshold voltage of device returns to its original value, this signifies that the information is lost.

In the Figure 4.16 (d) which is the one of the devices, the data indicates that after approximately $10^{4.8}$ seconds (about 6.31 hours), the threshold voltage returns to its initial value before pulsing. This implies that the device maintains stable data retention over a relatively short time frame. In contrast, the other device, as plotted in the Figure 4.16 (e) demonstrates that even after approximately $10^{12.2}$ seconds (about 1,811 years), the threshold voltage is measurably different from its pre-pulsing value. The extracted retention is clearly unfeasible, indicating that for a correct extimation, a longer measurement is needed. Nevertheless, this indicates a good stability of the analyzed device.

Based on the collected data, the realized devices are operating as charge trapping devices. The measured transfer characteristics clearly show the excellent quality of the realized Si-oxide interface, a fundamental requirement for a stable and reproducible device operation. The extracted retention times show a huge variation between different devices, although representing a good starting point. Future experiments must be focused on further evolving the interface between the semiconductor and the oxide, to tune the impact of the ferroelectric polarization with respect to the trapping mechanism, allowing us to realize both type of memories starting from the same SOI platform.

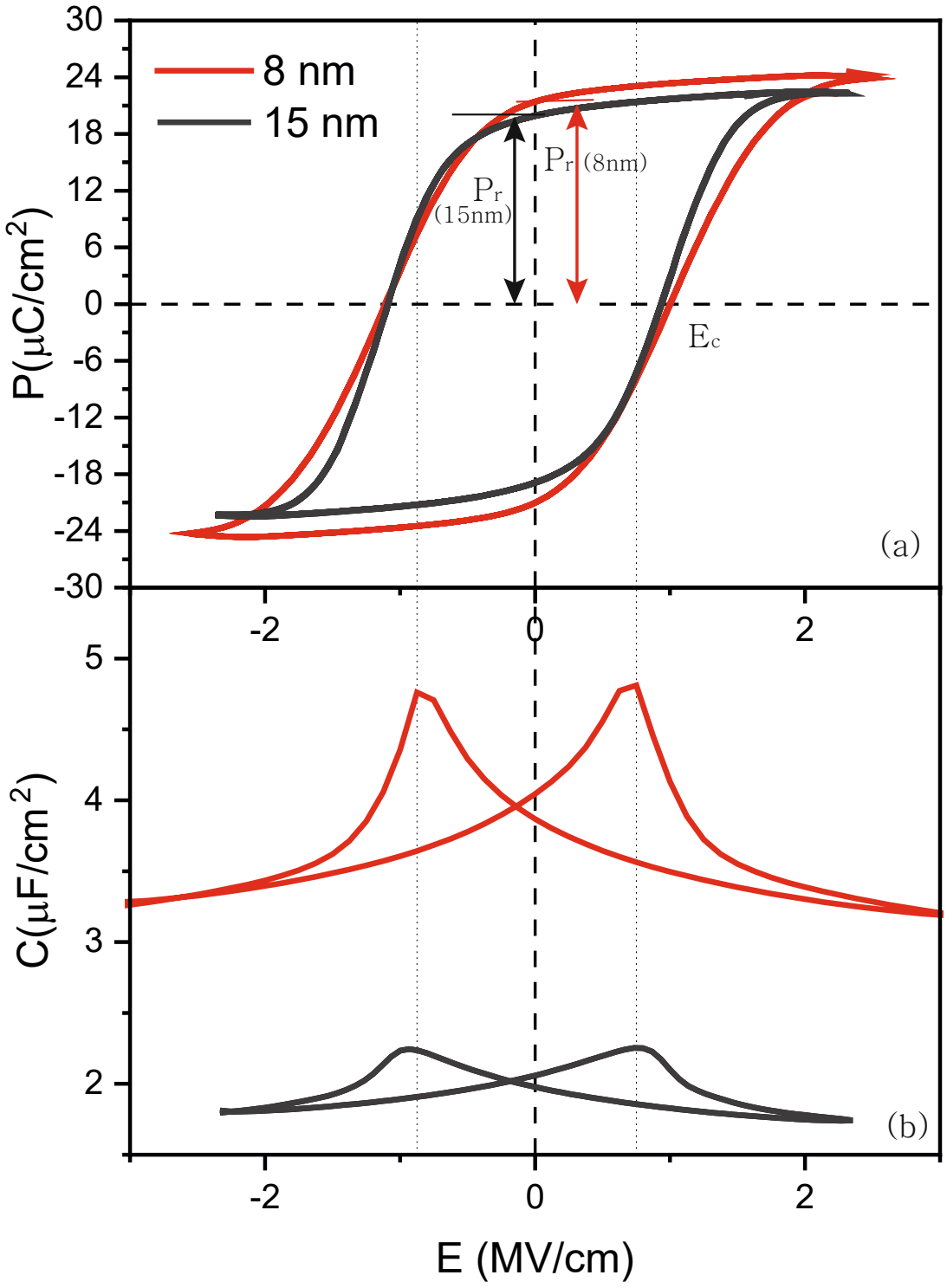


Abbildung 4.11: *Polarization-Voltage and Capacitance-Voltage curve at the thickness of 8nm and 15nm of HZO*

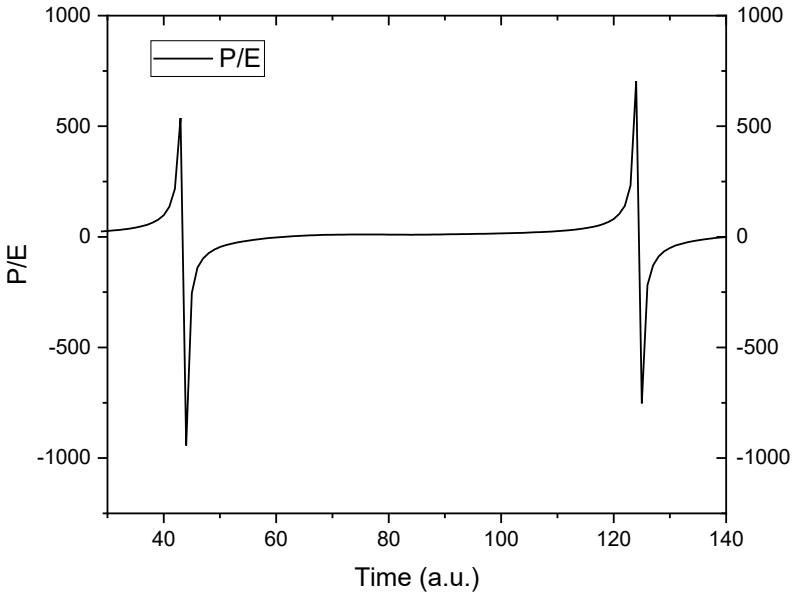
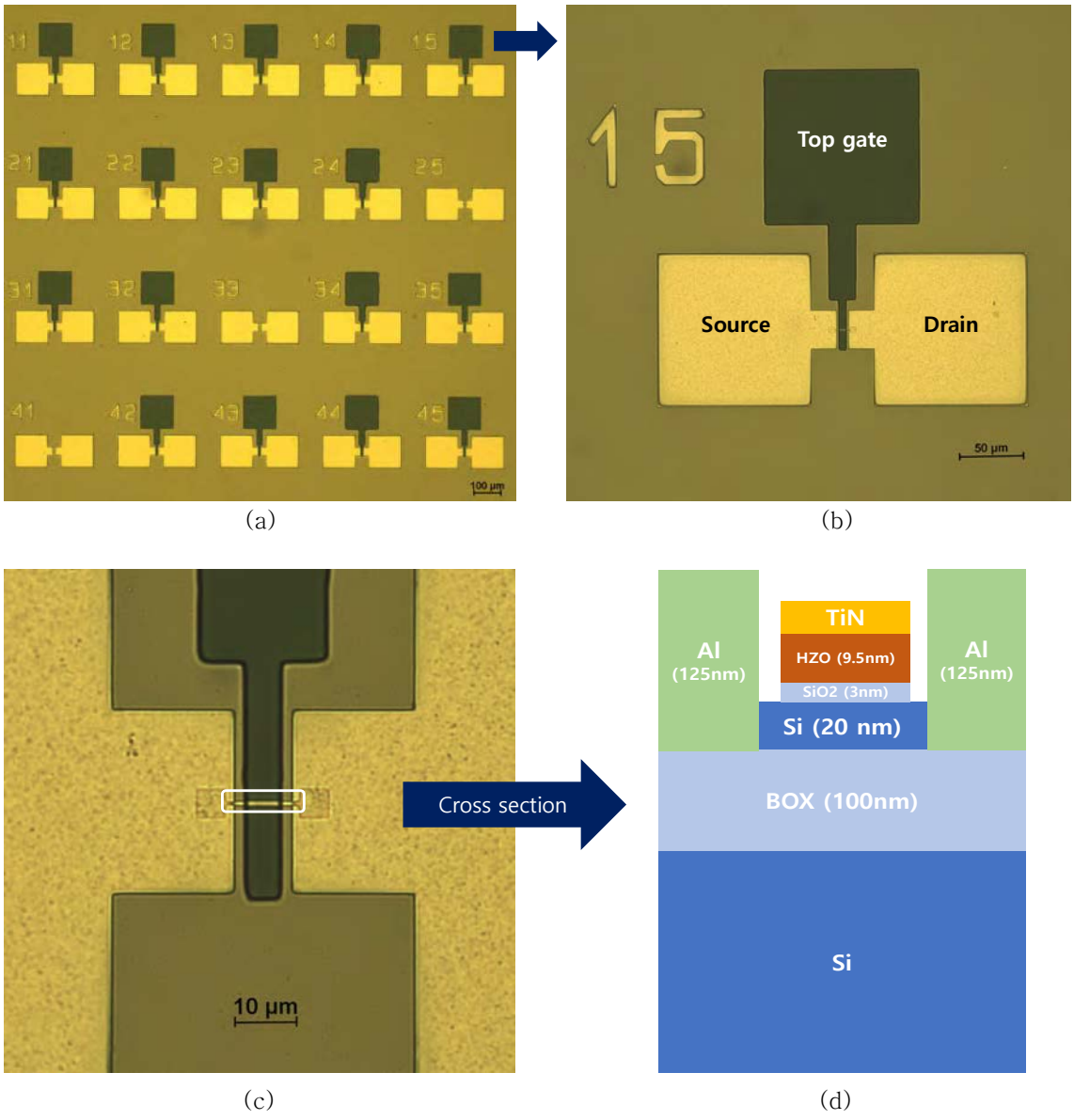


Abbildung 4.12: *P/E at the certain point of Polarization - Voltage graph*



(a) (b)

(c) (d)

Abbildung 4.13: *FeFET device structure (a) Microscopic image of overall pads at 5X magnification which were produced on the SOI-wafer (b) 20X magnification image of one pad (c) 20X magnification image of Source - Gate - Drain (S/D) part. (d) Cross section of the S/D part*

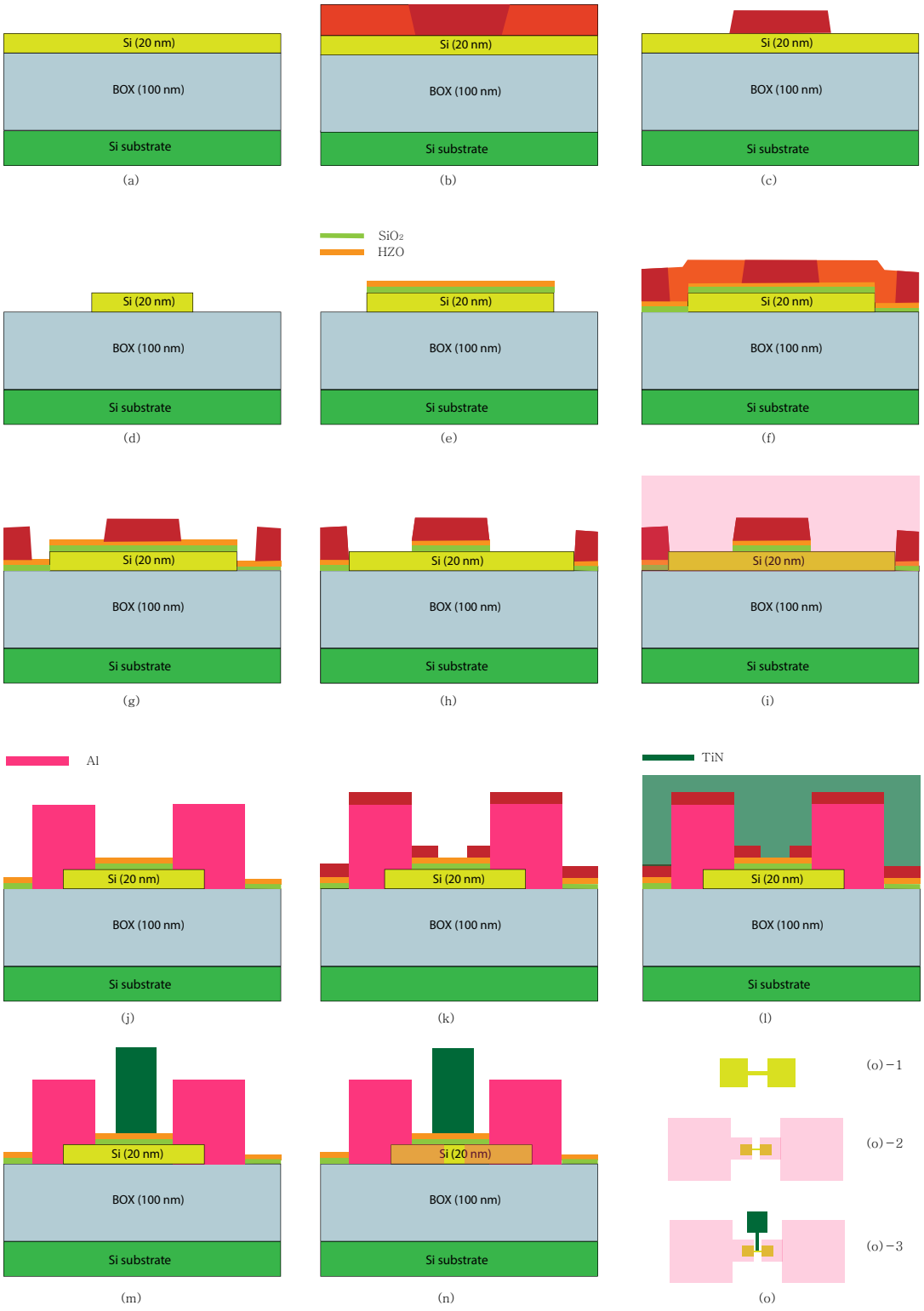


Abbildung 4.14: *Fabrication*

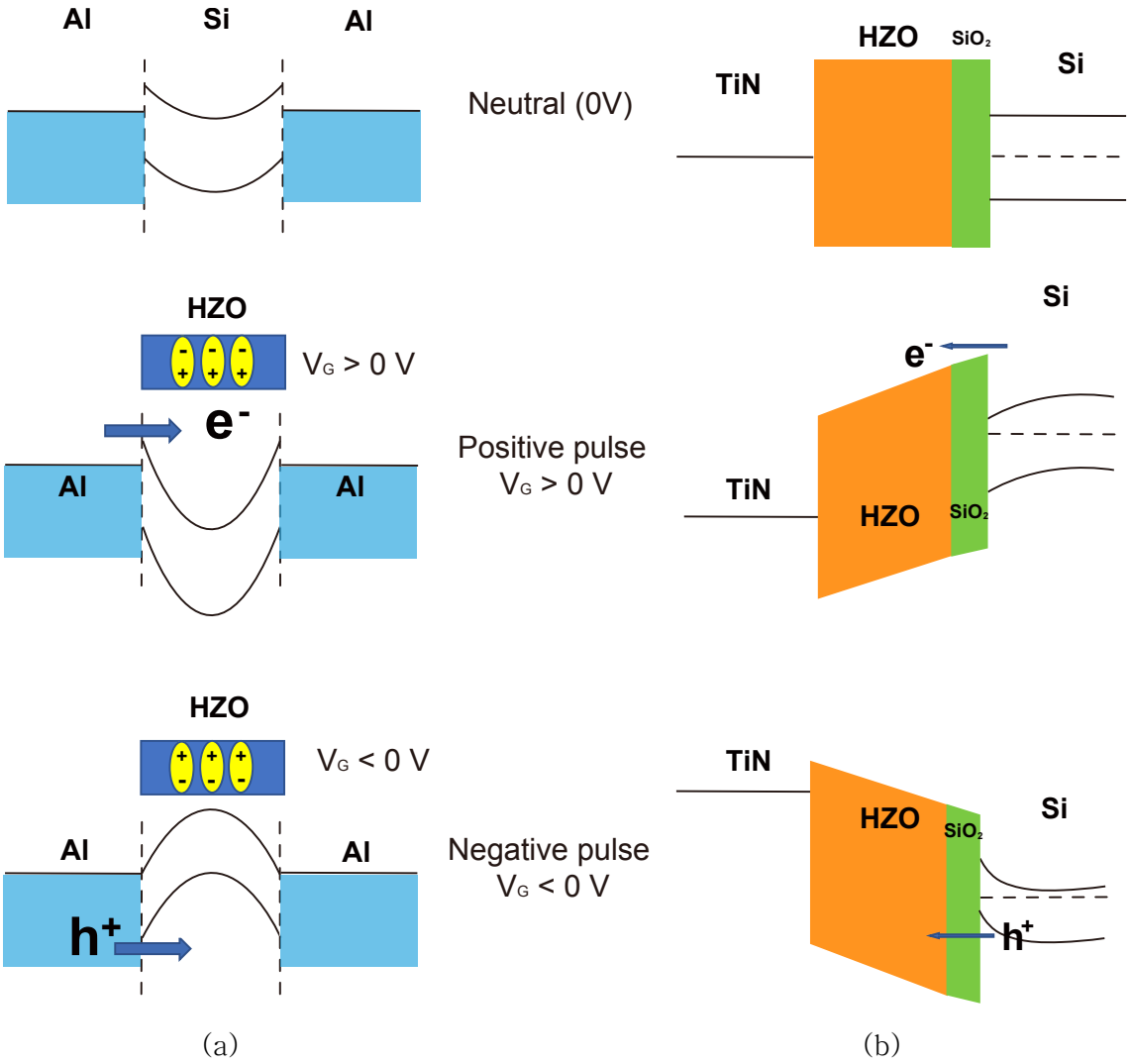


Abbildung 4.15: *Schematic representation illustrating the two interfaces. (a) Behavior of electrons and holes in response to applied voltages in Al-Si-Al heterostructure interfaces (b) Behavior of electrons and holes in response to applied voltages to the MOS structure at Top gate and the insulator interfaces where electron traps occur*

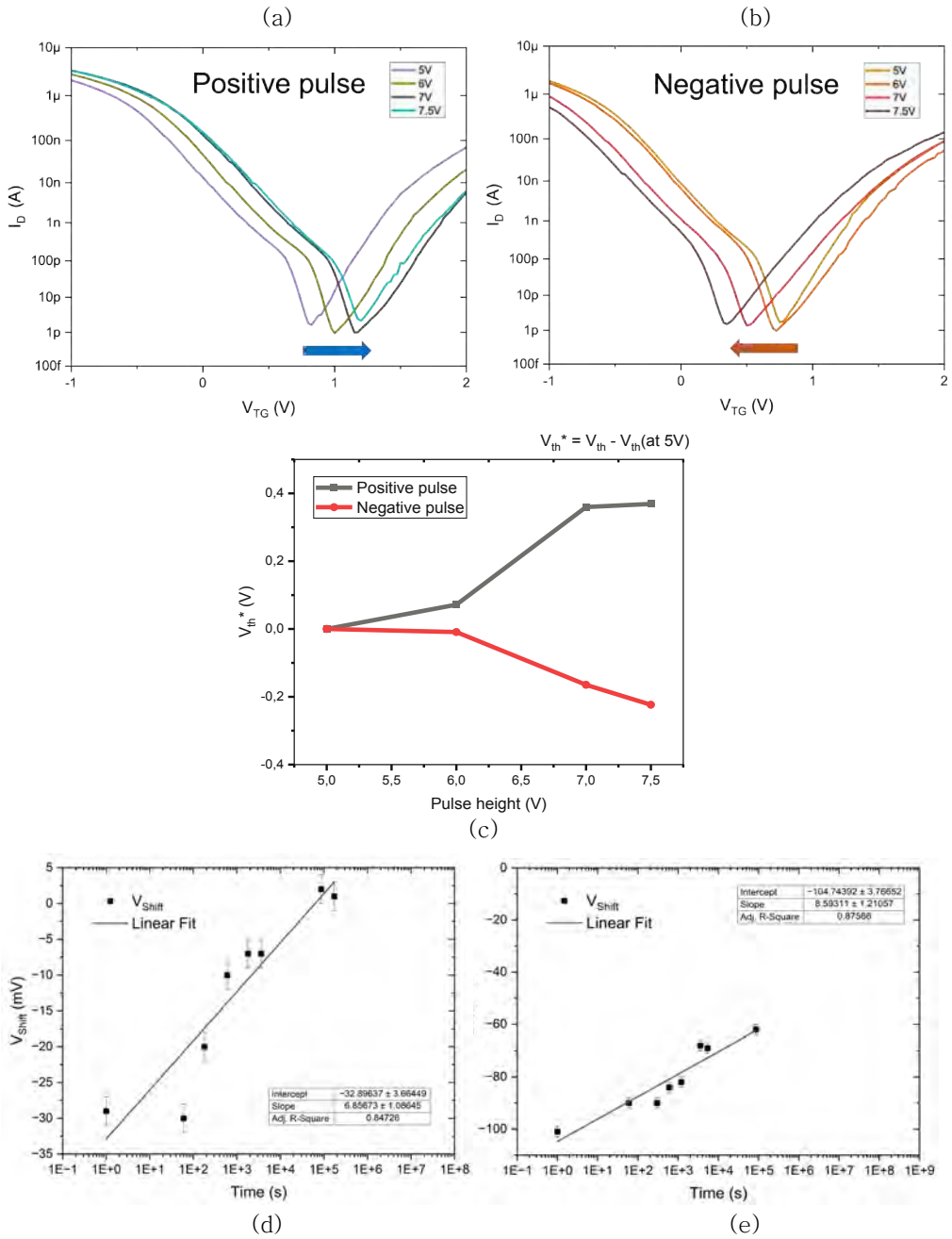


Abbildung 4.16: *(a), (b) Schematic representation of $V_{TG} - I_D$ electrical characterization when a positive and negative pulse is applied to the top gate. (a) The graph shows a shift to the right direction, compensating for the negative net charge in the device. (b) The graph shows a shift to the left direction, compensating for the positive net charge in the device. (c) Separate plots of threshold voltage for positive and negative pulsing cases. The y-axis V_{th}^* represents the difference between the threshold voltage at each voltage and the threshold voltage at +5V for positive pulsing or -5V for negative pulsing. (d), (e) Result of retention test from different Devices.*

Kapitel 5

Summary and Outlook

In this thesis, we have presented a comprehensive study involving the deposition and characterization of CMOS-compatible HZO thin films with thicknesses below 10 nm using Atomic Layer Deposition (ALD). The films were utilized to fabricate Metal-Insulator-Metal (MIM) capacitors, and the resulting devices were subjected to various characterization experiments and characterized. The key experimental findings can be summarized as follows:

- We have implemented and optimized an ALD process for the deposition of high purity $Hf_{0.5}Zr_{0.5}O_2$ (HZO) films, with thicknesses below 10 nm. Analysis through ellipsometry indicated that films deposited using a thermal-ALD exhibited higher density compared to those deposited using a Plasma-enhanced ALD.

- The chemical composition of the deposited HZO layers was analyzed using X-ray Photoelectron Spectroscopy (XPS), confirming a 1:1 ratio of Hf to Zr. TEM images further confirmed the uniform distribution of Hf, Zr, and oxygen in the HZO film.

- To succesfully integrate the high-k material into devices, we have carefully optimized all the necessary experimental steps, from substrate cleaning, to the formation of a semiconductor-oxide interface with a low density of traps, to the etching of the high-k layer. The dielectric constants of ZrO_2 and HfO_2 were directly measured using a thickness series, resulting in values of 27 ± 2 and 20 ± 1, respectively.

- MIM capacitors were fabricated, and their electrical properties were characterized through Capacitance-Voltage (C-V) and Polarization-Voltage (P-V) measurements. Annealing the 8 nm HZO film in an N_2 environment at 500°C for 3 to 5 minutes resulted in the HZO exhibiting ferroelectric behavior with an orthorhombic structure. This behavior was evidenced by the butterfly-shaped C-V curve and the hysteresis

loop in the P-V curve, with a remanent polarization of (21.3 $\mu C/cm^2$) .

- Additionally, Al-Si-Al heterostructure devices with HZO as the gate dielectric were fabricated. Electrical characterization using Transfer characteristics demonstrated that the devices as charge trapping memories with stable performances and displaying excellent properties of the semiconductor-oxide interface..

In this study, our primary focus was to implement a stable and reproducible process for the deposition of sub-10 nm thick $Hf_{0.5}Zr_{0.5}O_2$ layers using a ALD process. Therefore, we have fully characterized the obtained films using a large set of experimental techniques. This allowed us to explore and establish specific conditions under which HZO exhibits reliable and reproducible ferroelectric behavior. With these conditions successfully identified and stabilized, the next crucial step in our research is to integrate the obtained material into devices based on monolithic and single-crystalline Al-Si-Al heterostructures for memory applications, either through the exploitation of the ferroelectric behavior of HZO or benefitting from the charge trapping capabilities of the Hf-based layer.

The realized devices show stable charge trapping memory operation and an excellent quality of the realized oxide-semiconductor interface. Further studies on the fabrication process are needed to be able to tune the interface to also allow for a stable ferroelectric operation, allowing us to obtain the two type of memories from the same Al-Si-Al platform. This research direction holds significant promise for advancing the field of ferroelectric memory technologies, paving the way for more efficient and reliable memory devices in the future.

Abbildungsverzeichnis

List of Abbreviations

AFM	Atomic Force Microscopy
Al	Aluminum
Al_2O_3	Aluminum Oxide
ALD	Atomic Layer Deposition
Ar	Argon
$BaTiO_3$	Barium titanate
BG	Back-Gate
BHF	Buffered Hydrofluoric Acid
CB	Conduction Band
C-E	Capacitance-Electric field
CMOS	Complementary Metal-Oxide-Semiconductor
C-V	Capacitance-Voltage
CVD	Chemical Vapor Deposition
DRAM	Dynamic Random Access Memory
FeFET	Ferroelectric field-effect-transistor
FeRAM	Ferroelectric random-access-memory
FET	Field-Effect Transistor
FTJ	Ferroelectric Tunnel Junctionr
FWHM	Full Width at Half Maximum
HAADF	High-Angle Annular Dark Field
H_2O	Water
HF	Hydrofluoric Acid
HfO_2	Hafnium Oxide
HKMG	High-K Metal Gate
HZO	Hafnium Zirconium Oxide

HRTEM	High-resolution Transmission Electron Microscopy
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
N_2	Nitrogen
O	Oxygen
P-E	Polarization-Electric field
PMA	Post metallization Annealing
P-V	Polarization-Voltage
PVD	Physical Vapor Deposition
RTA	Rapid Thermal Annealing
SEM	Scanning Electron Microscopy
Si	Silicon
SiO_2	Silicon Dioxide
SOI	silicon-on-insulator
SMUs	Source Measure Units
STG	Single Top-Gate
T_c	Curie temperature
TEM	Transmission Electron Microscopy
Ti	Titanium
TG	Top-Gate
VB	Valence Band
XPS	X-ray Photoelectron Spectroscopy
ZrO_2	Zirconium oxide

List of Symbols

A	Area
E	Electric field
E_c	Coercive field
ϵ_0	Dielectric constant of vacuum
ϵ_r	Dielectric constant of material
d	thickness of the layer
P	Polarization
P_r	remanent polarization
q	Elementary Charge
V	Voltage
V_{th}	Threshold Voltage

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