Master Thesis

GeSn on SOI based Schottky Barrier Field-Effect Transistors with Crystalline Al Contacts

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Abstract

Countless inventions and discoveries of modern civilization have shaped our everyday lives but none to such an extent as the field effect transistor in recent years and the accompanying consequences of technological progress. Modern applications show us the great demand for transistors: more transistors are needed in smaller areas with increased performance. For a long time, Moore's Law, which states that the complexity of integrated circuits doubles every 12-24 months, could be taken as a forecast. However, the latest developments show that this rapid acceleration in complexity will no longer be achievable in the future using conventional methods.

Although the first transistor was developed more than 70 years ago, the achievements of semiconductor technology are mainly responsible for the technological progress of the last decades. Today's society as we know it with countless sensors around us, household electronics and industry would not be possible without transistors. With the constant further development of transistors and the accompanying ever smaller production, research is slowly reaching the limits of physics. One approach to overcome this limit is to make the transistor more powerful by using a metal-semiconductor junction that influences electrical properties, so-called Schottky-Barrier Field Effect Transistors. A clear advantage of such a device is that there is no need for channel doping and expensive technological steps like ion implantation and high temperature annealings can be avoided.

Such a representative of semiconductor-metal compounds can be realized with Germanium and Tin. This material composition brings numerous advantages. Among other things, the conductivity as well as the controllability can be drastically improved with a certain Germanium-Tin ratio, especially the direct band gap and thus the potential use in opto-electronics increases the interest in these electronic devices. This master thesis explores the possible implications of a germanium-tin junction for field-effect transistors and examines potential applications and development opportunities. A major part of the thesis is the fabrication of the devices and the underlying process steps. The electrical characterization of the fabricated transistors are highlighted and representative conclusions are drawn and a final comparison between different GeSn ratios is made.

Kurzfassung

Unzählige Erfindungen und Entdeckungen der modernen Zivilisation prägen unseren Alltag aber keiner in solch einem Ausmaß wie der Feldeffekttransitor in den letzten Jahren und den damit einhergehenden Folgen des technologischen Fortschritts. Moderne Anwendungen zeigen uns den großen Bedarf an Transistoren: es werden mehr Transistoren auf kleineren Flächen benötigt mit steigender Leistungsfähigkeit. Lange Zeit konnte man Moores Gesetz, welches besagt, dass sich die Komplexität integrierter Schaltkreise alle 12-24 Monate verdoppelt, als Prognose zur Hand nehmen. Die jüngsten Entwicklungen zeigen allerdings, dass diese rasante Beschleunigung der Komplexität mit herkömmlichen Methoden künftig nicht mehr erreichbar sein wird.

Obwohl der erste Transistor vor mittlerweile mehr als 70 Jahren entwickelt wurde, sind die Errungenschaften der Halbleitertechnologie hauptsächlich für den technologischen Fortschritt der letzten Jahrzehnte verantwortlich. Unsere heutige Gesellschaft so wie wir sie kennen mit unzähligen Sensoren um uns herum, Haushaltselektronik und die Industrie wäre ohne Transistoren gar nicht mehr vorzustellen. Mit der stetigen Weiterentwicklung von Transistoren und damit einhergehend die immer kleiner werdende Fabrikation stößt die Forschung langsam an die Grenzen der Physik. Eine Herangehensweise dieses Limit zu umgehen, ist die Transistoren leistungsfähiger zu machen indem ein Metall-Halbleiter-Übergang zum Einsatz kommt, welche die elektrischen Eigenschaften beeinflusst, sogenannte Schottkybarrieren-Feldeffekttransistoren. Ein klarer Vorteil eines solchen Bauelements ist, dass keine Kanaldotierung erforderlich ist und teure technologische Schritte wie Ionenimplantation und Hochtemperaturglühen vermieden werden können.

Ein solcher Vertreter von Halbleiter-Metall-Verbindungen kann mit Germanium und Zinn verwirklicht werden. Diese Materialzusammensetzung bringt zahlreiche Vorteile mit sich. Unter anderem kann die Leitfähigkeit und Steuerbarkeit mit einem gewissen Germanium-Zinn-Verhältnis drastisch verbessert werden. Insbesondere die direkte Bandlücke und damit die potentielle Anwendungen in der Optoelektronik machen dieses Bauteil besonders spannend. Diese Masterarbeit geht den möglichen Auswirkungen einer Germanium-Zinn-Verbindung für Feldeffekttransistoren nach und prüft mögliche Anwendungszwecke und Entwicklungsmöglichkeiten. Ein wesentlicher Bestandteil der Arbeit besteht in der Fabrikation der Bauteile weshalb die ausgeführten Schritte genau erklärt und eine Beschreibung der Prozessschritte dargelegt wird. Es wird die elektrische Charakterisierung der hergestellten Transistoren beleuchtet und repräsentative Schlüsse daraus gezogen sowie ein finaler Vergleich zwischen verschiedenen GeSn-Verhältnissen angestellt.

Acknowledgement

There is a saying: "The journey of a thousand miles begins with one step". In retrospect, when I think about my master's degree, I have to say that this is completely true for me. Besides some setbacks, it was all the more liberating to know that there are people whose support you have and on whom you can rely. The list would be too long to thank everyone but I would like to mention a few supporters by name:

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Last but not least, I would like to express my gratitude towards my family and friends. Thanks to their help, I was able to complete my studies as free of complications as possible. Without their encouraging words and active support, I would not be where I am now.

Contents

Chapter 1

Introduction

Transistors have been around for several decades and for good reason. Their versatile application, be it in the simplest case as a switch, as a switching half-bridge or in various amplifier circuits, make the transistor an appealing electronic component in research. It is no coincidence that the inventors of the transistor have all been honored with a Nobel Prize for their novel research. [1] However, one must not forget that today's transistor as we know it has come a long way. While the first transistor was just a few centimeters in size, today it is possible to achieve remarkable structure widths of 2-3 nanometers, which further illustrates how much has happened in this sector. This effect of miniaturising transistors and doubling the transistor count every 12-18 months is also called Moore's Law. [2] The earlier limitations of electronic circuits were often due to the enormous size of vacuum tubes. With the progressive development of the transistor, this hurdle could be overcome and more complex devices with increasing numbers of integrated transistors on smaller areas were created. Today we know: a pathfinder for advanced technologies. Newer generations of transistors are already gaining ground and demonstrate their full range of functions even at low voltages. [3]

While it was common to use Germanium to build a transistor until 1958, the use of Silicon slowly became more popular. This can be justified by the different temperatures at which the device breaks down, which is 80°C for Germanium and 180°C for Silicon. Another reason why Silicon dominated is that it is far more abundant and thus a lot cheaper. Compared to Germanium, Silicon has a wider bandgap making it less likely for current leaks across the device and it also comes with better thermal conductivity. [4] In recent years, however, more and more Germanium transistors found their way into publications. The reason is that Germanium offers the highest hole mobility among all semiconductors. [5] In addition, the electron mobility is nearly three times better than in Silicon. Looking at the mobility values of Germanium, one quickly realizes that this material is well suited for use in CMOS (complementary metal-oxide-semiconductor), since this technology uses

a combination of p-channel and n-channel field-effect transistors. p-channel FETs have a surplus of free-moving holes, while n-channel FETs have a surplus of electrons. In order to be able to realize fast circuits, a fast electron and hole movement must be the basis. Another benefit is that charge carriers are already transported with only a small applied voltage, which in turn results in low energy consumption.

Now you can ask yourself: what makes a good transistor in the first place? There are several aspects to evaluate the performance of a transistor. First and foremost, the conductivity and the ability to control the device. The interaction of these two main factors determines the rating of this component. To give an example, the higher the conductivity of a device, the lower the losses that result and higher currents can flow through the channel. This in turn means that there is a lower heat generation and this contributes to miniaturization. Summarized, increased device performance and reduced power consumption, while maintaining a good manufacturability and performance without penalizing the cost/function, are driving microelectronic research towards 3-nm technologies. [6]

The fact that Germanium is a very interesting semiconductor is already beyond question, but it is much more important to know whether the performance can be further enhanced by alloying it with another element. Why Tin is special, one might ask, and this question can be answered by considering how to create a direct band gap. By alloying a IV group semiconductor such as Germanium or Silicon with a IV group metal such as Lead or Tin, similar to the process used in a III-V compound, Germanium can be tuned in a way that a direct bandgap can be achieved. This is done by lowering the separation between indirect and direct valleys in the conduction band of Germanium. This direct bandgap is advantageous, for example, when one wants to fabricate efficient band-to-band tunneling devices such as a tunneling field effect transistor (TFET). Furthermore, the alloys' larger lattice constant relative to Germanium makes it appealing to use them to boost the carrier mobility of Germanium channel transistors.

Therefore, in this master thesis a transistor based on a Germanium-Tin-alloy was developed. The fabrication was done according to the top-down principle. Measurements were performed to electrically characterize the device and further analyze the effects of this novel material composition. The stack was grown at JKU Linz and kindly provided to the Nanocentre at TU Wien where the device fabrication including the lithography, sputtering, vapor deposition, reactive ion etching (RIE) or rapid thermal annealing (RTA) could be carried out in the clean room. Rapid thermal annealing should be treated with particular caution in this case, since Tin has a relatively low melting point of 231.9°C compared to the melting point of Germanium of 938.2°C. [7]

It is also of particular interest how high the Tin content must be in connection with Germanium in order to achieve the positive properties mentioned above. This point of view will be of enormous relevance in the practical measurements and will have to be taken into account especially when comparing single top gates, dual top gates, triple top gates

and middle gates. Samples with a tin content of 4%, 2%, 1% and 0.5% are compared. In the later course of the work it will become apparent that the temperature sweeps deliver exciting results, especially at low temperatures, where the analysis and interpretation allows a lot of leeway for further developments.

Chapter 2

Theory

This chapter is intended to give a basic overview of physical effects that occur in common devices using semiconductors. The aim is to show the development and to be able to understand why today's transistors are built the way they are. Furthermore, we will discuss the respective properties of the materials that are important in the fabrication of a transistor and explain why they are used. A special focus is set on the transport mechanisms occurring inside the transistor and the description of the emerging Schottky barrier at the Al-GeSn interface. Finally, the concept of SBFETs is discussed in more detail and why they are potentially suitable to offer a boost in performance and how the transistor design has to be adapted for this purpose.

2.1 Materials

2.1.1 Germanium

Future transistors aim at low power consumption and thus high conductivity, which is already partially achieved with materials such as strained silicon. An exciting material to push the limits of carrier mobility is Germanium. Germanium has the highest hole mobility compared to other common semiconductors and can also exhibit twice the electron mobility of Silicon. [5] These properties make Germanium particularly interesting as a material for future transistor development and in the field of research, whether as SBFETs (Schottky Barrier FET), RFETs or CMOS.

Germanium was first discovered by a German chemist named Clemens Winkler in 1886. [8] As it is easy to recognize, the name of the element originates from the home country of the discoverer, Germany. Germanium is basically widespread and was the most widely used element in the origins of semiconductor technology before silicon became widely accepted thereafter. [9] With a Clark value of 1.5 g/t, it is found in very low concentrations in the earth's crust compared to other elements. The melting point of germanium is 938.2° and the boiling point is 2833°. The atomic mass is 72.64u.

Germanium is in the semimetal series in the periodic table, but is classified as a semiconductor by more recent definition. Elemental germanium is very brittle and very stable when in contact with air at room temperature. Only when strongly annealed in an oxygen atmosphere does it oxidize to germanium(IV) oxide (GeO_2). Germanium is divalent and tetravalent, with germanium(IV) compounds being the most stable. Germanium, abbreviated as Ge, has the atomic number 32 in the periodic table and is found in the fourth period and in the fourth main group. [10]

Most elements from the fourth main group crystallize in the so-called diamond structure. Besides Silicon, Germanium-Silicon alloys and α-Tin also Germanium in pure form. The structure of the diamond structure consists of a face-centered cubic lattice and the base (0,0,0), (1/4,1/4,1/4). Each atom is covalently bonded with four neighboring atoms. The strong covalent bonds lead at temperatures around absolute zero to the fact that no free electrons exist and thus one gets into a state of fully occupied valence bands in contrast to the conduction band which is unoccupied. [11] [12] [13]

Typically, the band structure of elements crystallizing in diamond structure exhibits an indirect band gap, although the values of the band gap vary with the element. For example, Germanium has a band gap of $0.75eV$ at $0K$ and $0.67eV$ at $300K$ while Silicon has $1.17eV$ at $0K$ and $1.12eV$ at $300K$. With the low values of the energy band gap in Silicon and Germanium the thermal energy at room temperature is already sufficient to lift electrons from the valence band into the conduction band.

In an indirect band gap, the minimum of the conduction band is shifted with respect to

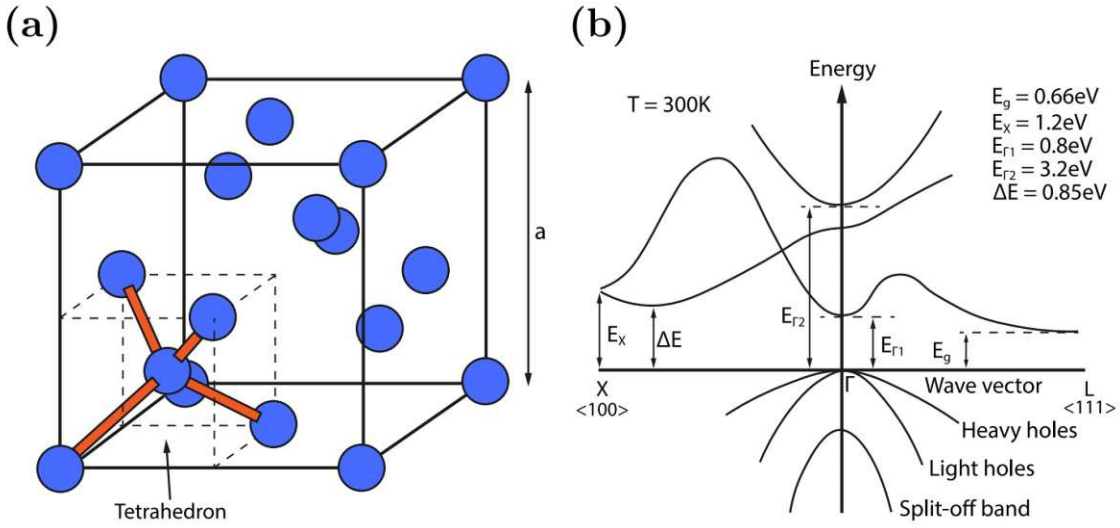


Figure 2.1: *a) Lattice Structure of Germanium b) Band gap of Germanium*

the maximum of the valence band on the $\vec{k}$ axis, hence the smallest distance between the bands is shifted. Absorption of a photon is effectively possible only in the case of a direct band gap; in the case of an indirect band gap, an additional quasi-pulse ($\vec{k}$) must be involved.

2.1.2 Tin

The discovery, around 3500 BC, that copper, easily smelted but rather soft, could be made harder and stronger by alloying with Tin, can be considered to be one of the great milestones in man's technological development, and heralded the advent of the Bronze Age. Because of its relative scarcity, Tin has always been a strategic metal and remains so to the present day. Isolation of the pure metal probably only dates from about 800 BC.

Tin is found with atomic number 50 in the periodic table under the fifth period and in the 14th group, the so-called carbon group, and is abbreviated Sn. The melting point of Tin is $231.93°C$ and the boiling point is $2602°C$. Compared to Germanium, the melting point is much lower, which had to be taken into account for Rapid Thermal Annealing, abbreviated RTA. Tin shows a chemical similarity to both of its neighbors in group 14, Germanium and Lead, and has two main oxidation states, +2 and the slightly more stable +4. The atomic mass of Tin is 11871u. [14] [15]

2.1.3 Ge-Sn-Alloy

The alloy between Germanium and Tin is of particular interest as this compound has useful properties for the band gap and thus indirectly for semiconductor devices. The alloy between the two elements provides remarkably high carrier mobility compared to pure silicon or pure Germanium. Therefore, it has been proposed that they can be used

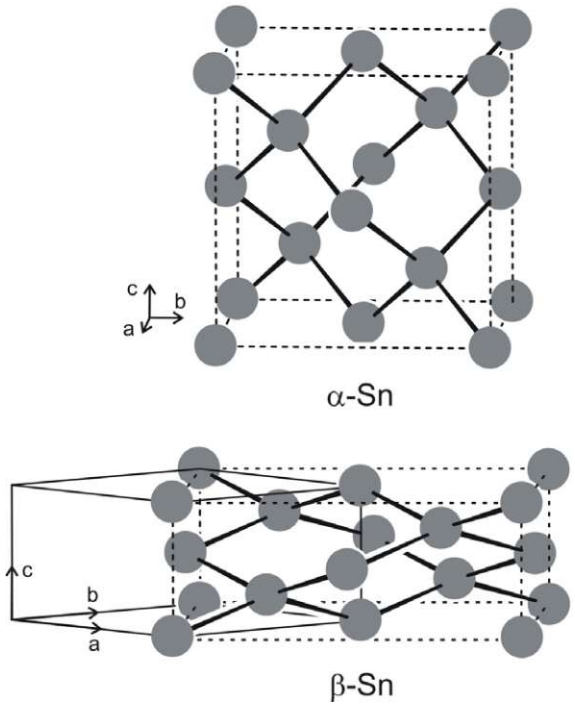


Figure 2.2: *The structures of α-and β-Sn. The tetragonal unit cell of β-Sn is drawn with a solid line. The compressed cubic cell is drawn with dotted lines for comparison.*

as a channel material in high speed metal-oxide-semiconductor field effect transistors. In addition, the alloys' larger lattice constant relative to Germanium makes it possible to use them as stressors to enhance the carrier mobility of Germanium channel transistors. Germanium-Tin alloys must be kinetically stabilized in order to prevent decomposition and are only thermodynamically stable under a small composition range. [16] [17] [18]

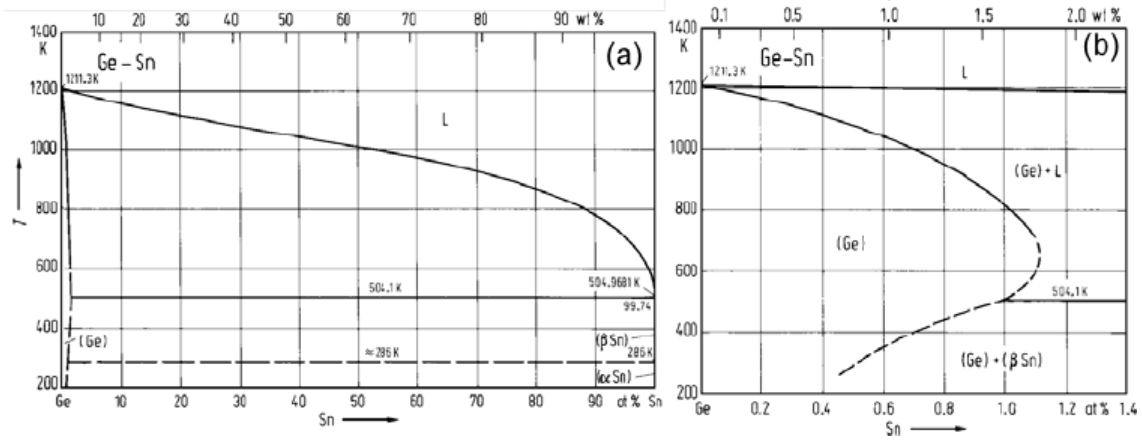


Figure 2.3: *GeSn equilibrium phase diagram and zoomed in view. a) A Ge-Sn-equilibrium phase diagram. b) a zoomed in diagram of lower Sn percentages*

As can be seen in the state diagram 2.3, the alloy already liquefies between $504K$ and $1202K$ depending on the Tin content, marked L in the diagram, and of course at temperatures higher than this. Since the transistors fabricated for this thesis use only very small amounts of Tin between 0.5% and 4%, the zoomed-in picture b) is a bit of more relevance.

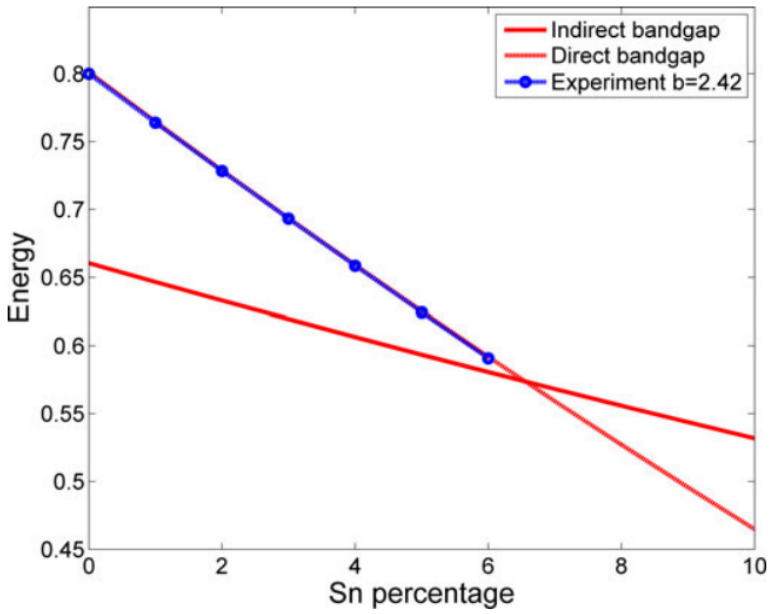


Figure 2.4: *Calculated direct and indirect bandgap energies of GeSn alloys as a function of Sn fraction.*

As can be read from figure 2.4, a direct band gap appears at about 6.55% Sn. A direct band gap is required for the construction of lasers and is therefore of interest in the field of optoelectronics. However, this master thesis deals with the effects of the integration of GeSn alloys in transistors and the associated effects on the electrical properties. Therefore, a Sn content of 4% Sn was chosen as the entry point for the samples. [19]

2.2 Field Effect Transistor

The theory of the field-effect transistor and its physical operation had been known for several years before the first prototype was even built. The Austro-Hungarian physicist Julius Edgar Lilienfeld had already filed patents for the operation of this electronic component in 1925 and Oskar Heil in 1934. It was not until about twenty years later that the three scientists John Bardeen, Walter Houser Brattain and William Shockley succeeded in building a field-effect transistor (FET) at Bell Labs in 1947.

The first working transistor was from the junction field-effect transistor (JFET) family. After the JFET proved difficult to manufacture and thus to mass produce, work began on

the development of an IGFET, insulated-gate field-effect transistor, which was seen as a potential alternative to the JFET. However, this attempt also failed due to the surface state barrier of the IGFETs, which prevented an electric field from penetrating the surface. In 1948, the foundation for MOSFET technology was laid. Basically, an IGFET was provided with an inversion layer. With the help of John Bardeen's invention of the inversion layer, one can limit the flow of minority charges and increase the conductivity, which strongly depends on the gate insulator. Based on this development, CMOS technology is still being advanced today.

The concept around field effect transistors is based on the idea that charges within a semiconductor are attracted by charges on an object nearby. Hence, the name field effect transistor since it operates using electric fields. In a FET, current flows along a semiconductor path called the channel. At one end of the channel, there is an electrode called the source. At the other end of the channel, there is an electrode called the drain. The physical diameter of the channel is fixed, but its effective electrical diameter can be varied by the application of a voltage to a control electrode called the gate. Whether the charge carriers are attracted or repelled depends on the polarity of the voltage. The conductivity of a FET is changed by the electrical diameter of the channel. A small change in gate voltage can cause a large variation in the current from the source to the drain. This is how the FET amplifies signals.

FETs are unipolar devices, which means they use only one type of charge carrier (electrons or holes) to control the current flow. The alternative to a unipolar device is a bipolar device. Unlike a unipolar device like an FET, a bipolar device such as a Bipolar Junction Transistor (BJT) uses both electrons and holes to control the current flow. Bipolar devices have a high current gain and can handle higher power levels, which makes them suitable for power amplification applications.

Depending on how the semiconductor material is doped, a distinction can be made between p-channel FETs and n-channel FETs, analogous to the BJT. In contrast to the BJT, the FET has a high input impedance usually in the range of megohms, which is often mentioned as the main advantage of the FET over the BJT, and is not current controlled like the BJT but voltage controlled instead.

The main application of FETs can be found in the field of integrated circuits, called IC. In this sector, FETs are preferred to BJTs because they have a much lower power consumption. Especially when you consider how many millions or billions of transistors can fit on a small chip area today, a power saving of several orders of magnitude can result.

The FET has lower noise, better thermal stability performance and is more immune to radiation compared to a BJT. In addition, the FET has a high gate-to-drain current resistance in the range of 100 megaohms. Since low-power switching is possible with the field-effect transistor, miniaturizability is also easier because heat generation is low

compared to other switching devices. Looking at the disadvantages of FETs in general, one comes across the low gain bandwith. Furthermore, it must be noted that a FET that can withstand high voltages also has a high on-resistance. Therefore you have to find a compromise between voltage rating and on-resistance.

Generally one would use FETs rather in the low voltage range as in the wireless transmission sectors. They are preferred in circuits or designs that require high input impedances. Less recommended is the FET for high power amplification.

2.2.1 Junctionless Field Effect Transistor

Due to MOSFET's vital position in the semiconductor industry, its technology has advanced significantly. Scalability of the device is a key benefit of MOSFETs. In order to reduce latency, power, and boost packing density, semiconductor industry trends are moving toward shrinking transistor size. Transistor scaling provides many benefits, but when a device's size approaches the submicron range, several undesired side effects like decreased mobility, short channel effects, and a gradual change in doping concentration at junctions become apparent. Due to the need for ultrasteep doping profiles, the scaling of channel length to extreme dimensions imposes strict requirements for doping in sub-10-nm devices. Additionally, because junctions are the source of leakage current, electronics with junctions experience greater power dissipation. Due to the elimination of the ultrasteep doping profile constraint, devices with uniform doping, such as junctionless transistors, have highly bright futures in semiconductor technology. The complexity of manufacturing these devices rises due to the concentration gradient that occurs at source/drain junctions. A device known as a junctionless FET (JLFET) can be fabricated to address this problem. A JLFET has uniformly high doping levels across the entire structure. It might be viewed as a high-doping gated resistor. [20] [21]

The structure of a JLFET can be seen in figure 2.5. It consists of a highly doped semiconductor film with a gate electrode that changes the channel carrier concentration and thus the resistivity of the channel. To achieve ohmic contacts at drain and source a high doping is required. Since the doping type remains the same along the channel and thus also the concentration of impurities, no metallurgic junction occurs in this electrical component, which makes it significantly different from other common semiconductor devices such as MOSFETs. The absence of a junction between drain and source in a JLFET therefore leads to different current conduction mechanisms compared to a MOSFET.

As shown in figure 2.5 b), the JLFET can be viewed as an n-MOS capacitor with n-type source/drain regions that are appended on both sides of the channel. By applying voltage to the gate electrode, the transistor or gated resistor can operate in volume depletion (or full depletion), partial depletion and accumulation modes. In order to achieve volume depletion a gate electrode with a high work function is neccessary in n-JLFETs whereas a low work function is needed for p-JLFETs. When the JLFET operates in the OFF-state, the majority carriers' depletion causes a very low conductivity and thus high resistance. In

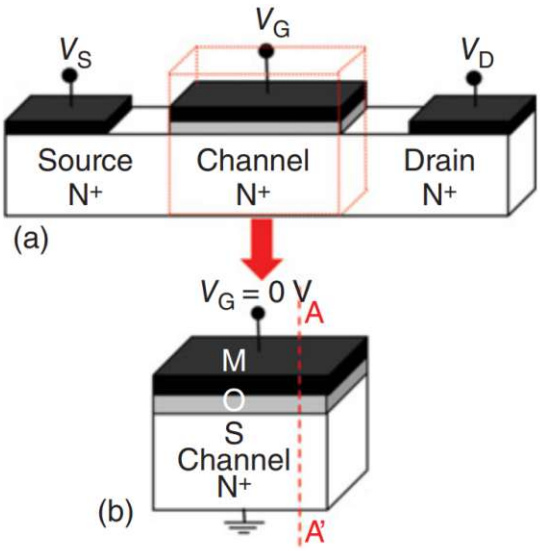


Figure 2.5: *(a) The three-dimensional view of a JLFET and (b) the MOS capacitor which forms the heart of a JLFET.*

JLFETs, the gate-induced depletion of the channel region controls the OFF-state leakage current rather than the reverse biased p-n junction leakage current as in the case of a MOSFET. The partial depletion mode is reached by applying a positive voltage to the gate electrode. This leads to a reduction in the width of the depletion layer and an undepleted region emerges in the center of the channel. Part of the channel region is still depleted in this mode of operation, which is known as partial depletion, while the remaining neutral zone, which is heavily doped, makes it easy for current to flow from the source to the drain region. The neutral region contributes to the current flow and is sandwiched between the depleted regions fairly centered in the channel due to the gate.

The depletion region width caused by the gate would decrease as the voltage on the gate electrode was raised, revealing a bigger neutral region. The gate-induced depletion areas would vanish and the entire semiconductor film would be undepleted and neutral at a specific gate voltage. For JLFETs, the flat band voltage is the gate voltage, which corresponds to a net zero depletion area width in the channel region. The entire channel turns neutral and actively contributes majority carriers for current conduction under flat band conditions. If the gate voltage is raised even further, an accumulation layer of electrons will occur because the electrons will be drawn to the channel's surface. The electric field at the surface of the channel region increases from its minimum value at flat band, and an accumulation layer of electrons is formed.

Junctionless trasnsistors have electrical characteristics very similar to those of standard multigate FETs. Both output characteristic and subthreshold characteristics resemble those of inversion-mode devices. The JLFET is a close cousin of the accumulation-mode FET. [22] [23]

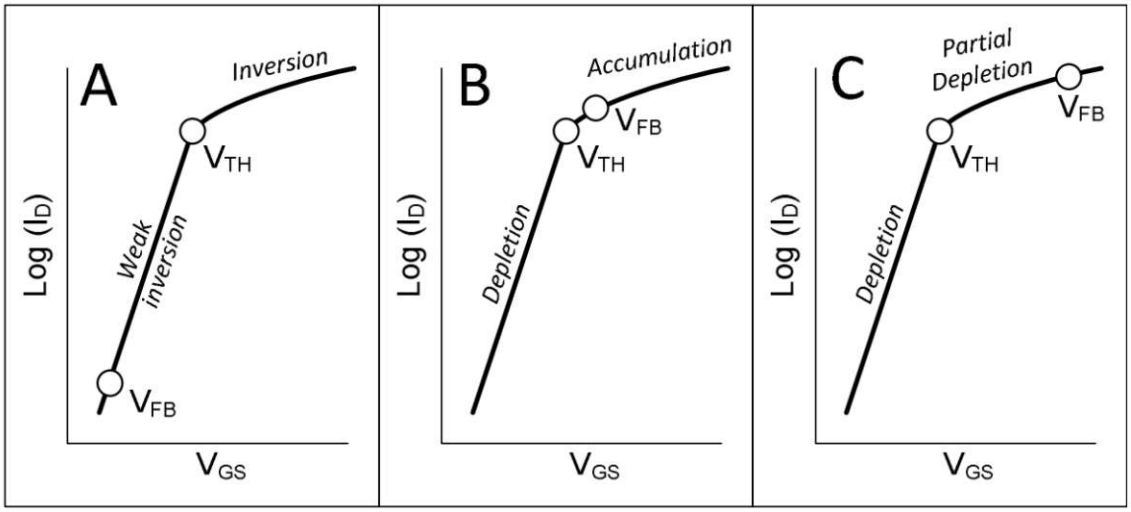


Figure 2.6: *Conduction mechanisms in A: inversion-mode; B: accumulation-mode and C: junctionless FETs.*

One important factor controlling the current flowing through FETs is the mobility of the carriers. As was previously mentioned, the JLFETs are expected to have a different mobility dependence from the MOSFETs because of their unique conduction mechanisms (bulk conduction as opposed to surface conduction in MOSFETs). The current in a MOSFET flows via the inversion layer at the surface, where the electrons are subjected to strong fields as well as scattering events caused by surface roughness. The mobility is hindered by these two variables. However, with a JLFET, the majority of the carriers flow away from the interface. In JLFETs, the electric field along the channel thickness is minimal when the device is operated in flat band conditions and increases when the device is operated in both the depletion and accumulation regions, as illustrated in Figure 2.7.

2.2.2 Metal-Oxide-Semiconductor Field Effect Transistor

Another milestone in transistor development was achieved by Mohamed Atalla and Dawon Kahng in the 1960s, again at Bell Labs. For the first time, the two scientists were able to produce a device that resembles today's structure of a MOS transistor. The basic idea of this new transistor was the same one that Bardeen, Shockley and Brattain had already used unsuccessfully in their surface field effect transistor. In its early stages, the metal-oxide-semiconductor field effect transistor, or MOSFET for short, was not really taken seriously because its response was about a factor of 100 slower than that of commercially available bipolar transistors at the time. However, the inventors already pointed out the advantages of the advancing MOSFET development, especially with regard to simpler fabrication and the use in integrated circuits.

As usual for field effect transistors, the MOSFET also has three electrical connections called drain, source and gate and it is available in two versions the n-channel MOS (NMOS)

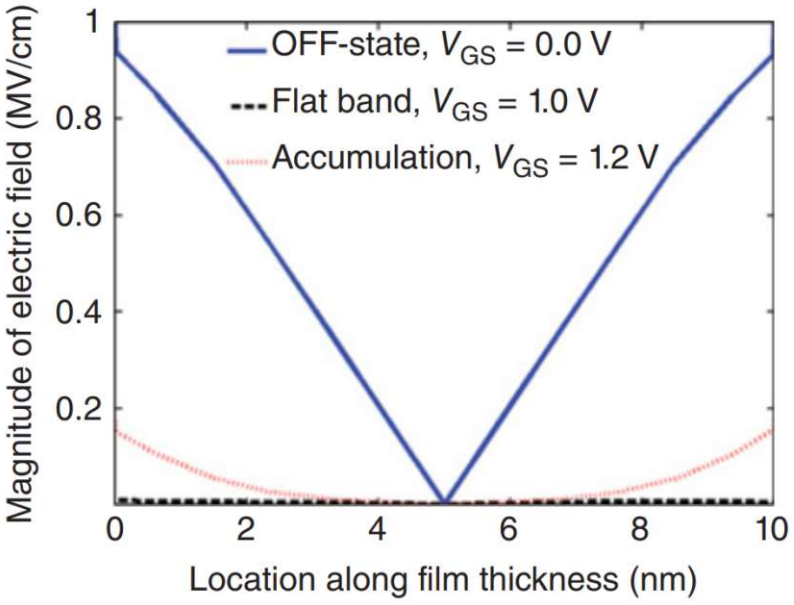


Figure 2.7: *Vertical electric field along the silicon film thickness of a JLFET in different operating regimes.*

and the p-channel MOS (PMOS), as can be seen in 2.8. The special feature of this type of transistor is that the gate terminal is electrically isolated from the channel. For this very reason, MOSFET transistors are sometimes called Insulated Gate FETs (IGFET). MOSFETs have a high input resistance due to the isolation between gate and source terminals. [24]

A MOSFET can be operated in a depletion mode as well as in an enhancement mode. If the conductivity of the transistor is increased in enhancement mode when the gate voltage is applied, the opposite happens in depletion mode. Thus, in depletion mode, the conductivity decreases when the gate voltage is applied.

Depletion Mode:
In depletion mode the MOSFET is known as "switched on" device, since the transistors are closed when there is no bias voltage applied to the gate. In this mode, as the voltage increases, the effective width of the channel is increased and thus a higher drain current I_D can flow through the channel. If a negative voltage is applied this leads to the opposite effect because the channel becomes narrower and the transistor can enter the cutoff region.

Enhancement mode:
Enhancement mode is the more commonly used mode for transistors. With this type of transistor, the device behaves like a normally open switch, since there is no conductivity when the applied gate voltage is 0. If the bias voltage is increased further, the effective channel width is increased and more drain current can flow. However, if the bias voltage

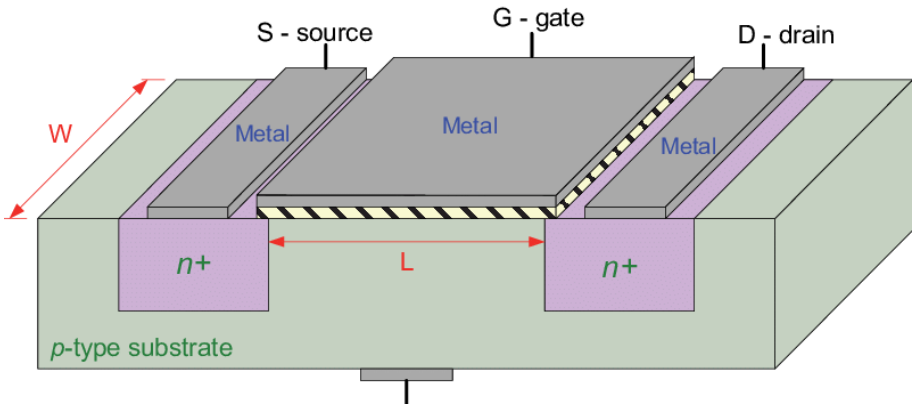


Figure 2.8: *Physical structure of an nMOS transistor.*

becomes 0 or negative, the transistor is set to a non-conducting state and turns off. Enhancement mode MOSFET transistors are mostly used as switches in electronic circuits because of their low ON resistance and high OFF resistance and also because of their high gate resistance. These transistors are used to make logic gates and in power switching circuits, such as CMOS gates, which have both NMOS and PMOS Transistors. In summary, the gate voltage leads to an enhancement of the channel, hence the name enhancement mode.

The three operating modes in which the MOSFET operates are called cut-off region, ohmic region and saturation region. [25]

- Cut-off region:

  $V_{GS} < V_{TH}$
  $I_{DS} = 0$

  When the gain source voltage falls below the threshold voltage, the transitor is set to the cut-off region and switches off completely. The drain current drops to 0A and the MOSFET behaves like an open circuit.

- Ohmic region:

  $V_{GS} > V_{TH}$ *and* $V_{TH} < V_{DS} < (V_{GS} - V_{TH})$
  MOSFET acts as a Variable Resistor

  For the transistor to operate in this linear region, two conditions must be met. First, the gate-source voltage must be greater than the threshold voltage and second, the drain-source voltage must be greater than the threshold voltage and less than the difference between the gate-source voltage and the threshold voltage. In

this range the MOSFET behaves like a variable resistor.

- Saturation region:

  $V_{GS} >> V_{TH}$ *and* $(V_{GS} - V_{TH}) < V_{DS} < 2(V_{GS} - V_{TH})$
  $I_{DS} \rightarrow max.$

  Again, two conditions must be met to operate in the saturation region. The gate-source voltage must be much larger than the threshold voltage and the drain-source voltage must be in a range between the single difference between the gate-source voltage and the threshold voltage and twice the difference between these two voltages.

The so-called threshold voltage V_{TH} describes the voltage threshold that must be exceeded for the transistor to be in the on state and for current to start flowing in the channel. Depending on the material and doping used, this varies between $0.5V$ and $0.7V$ for an n-channel device and between $-0.5V$ and $-0.8V$ for a p-channel device.

The behavior of a MOSFET transistor in depletion and enhancement modes depending on the gate voltage is summarized as follows:

MOSFET TYPE	VGS = +V	VGS = 0	VGS = -V
N-Channel Depletion	ON	ON	OFF
N-Channel Enhancement	ON	OFF	OFF
P-Channel Depletion	OFF	ON	ON
P-Channel Enhancement	OFF	OFF	ON

Table 2.1: *Comparison between OFF and ON states of MOSFET transistors in dependence of voltages*

If you now take a look at the possible semiconductor materials that can be used, you will of course most often find Silicon. There are also variations where, for example, an alloy between Silicon and Germanium is used (SiGe). The otherwise very exciting alloy Gallium Arsenide (GaAs) is less important for MOSFETs, because it turns out to be difficult to create a good interface between semiconductor and insulator. [26]

As mentioned before, the gate connection is electrically isolated from the channel. This is usually done by a layer of silicon dioxide. If one wants to keep the consumed power low or avoid leaks of the gate current, a high-κ dielectric is used like hafnium silicate or zirconium dioxide to name examples.

The range of applications for MOSFETs is broad, and the most important applications are listed below:

- use in digital integrated circuits, e.g. microprocessors
- use in memories and in logic CMOS gates
- as analog switches
- as amplifiers
- as oscillators, e.g. in radio systems

2.2.3 Schottky-barrier Field Effect Transistor

The source-drain region of the Schottky barrier MOSFET is made of silicide or metal rather than greatly doped semiconductor, despite having a device structure that is similar to that of an ordinary MOSFET. The system offers numerous potential advantages over a standard MOSFET at nanometer scale. As a result, it is being investigated for scaling beyond the standard MOSFETs capabilities. From a construction standpoint, SBFETs do not need ultrahigh doping in the source-drain regions, and the metal-semiconductor junctions between them are designed to be sharp. These characteristics eliminate the need for exceptionally high doping in the source-drain region and extremely steep pn-junctions, which are significant obstacles to the creation of traditional nanoscale MOSFETs. From the perspective of system performance, the parasitic resistance of regular MOSFETs is expected to significantly degrade the on-current at nanometer channel lengths. By using silicide source-drain, SBFETs would essentially eliminate the parasitic resistance and thus could deliver more on-current than the conventional MOSFET. [27]

An ideal Schottky barrier unfolds its rectification properties at room temperature due to emission over the barrier into the metal. The charge carrier transport can be the result of either thermionic emission or a drift/diffusion process into the depletion region. The bias will be decreased at the interface and the limiting resistance is caused by electrons having sufficient thermal energy to cross the barrier if the transport takes place at the barrier, as is the case for thermionic emission. If, however, drift/diffusion restricts the transport, the bias will be dropped over the depletion region, and the dominating resistance will result from electrons passing through the depletion region. The likelihood that thermionic emission will predominate increases with the size of the Schottky barrier and band bending. [28]

2.2.3.1 Schottky Barrier

The Schottky barrier is named after the scientist Walter H. Schottky and can be observed at a junction between semiconductor and metal. It describes a barrier of potential energy for electrons. Already in 1874, Ferdinand Braun found out that this barrier has rectifying properties, which can be suitable for use in diodes. The key figure of the Schottky barrier is the so-called Schottky barrier height Φ_B which depends on the combination of metal

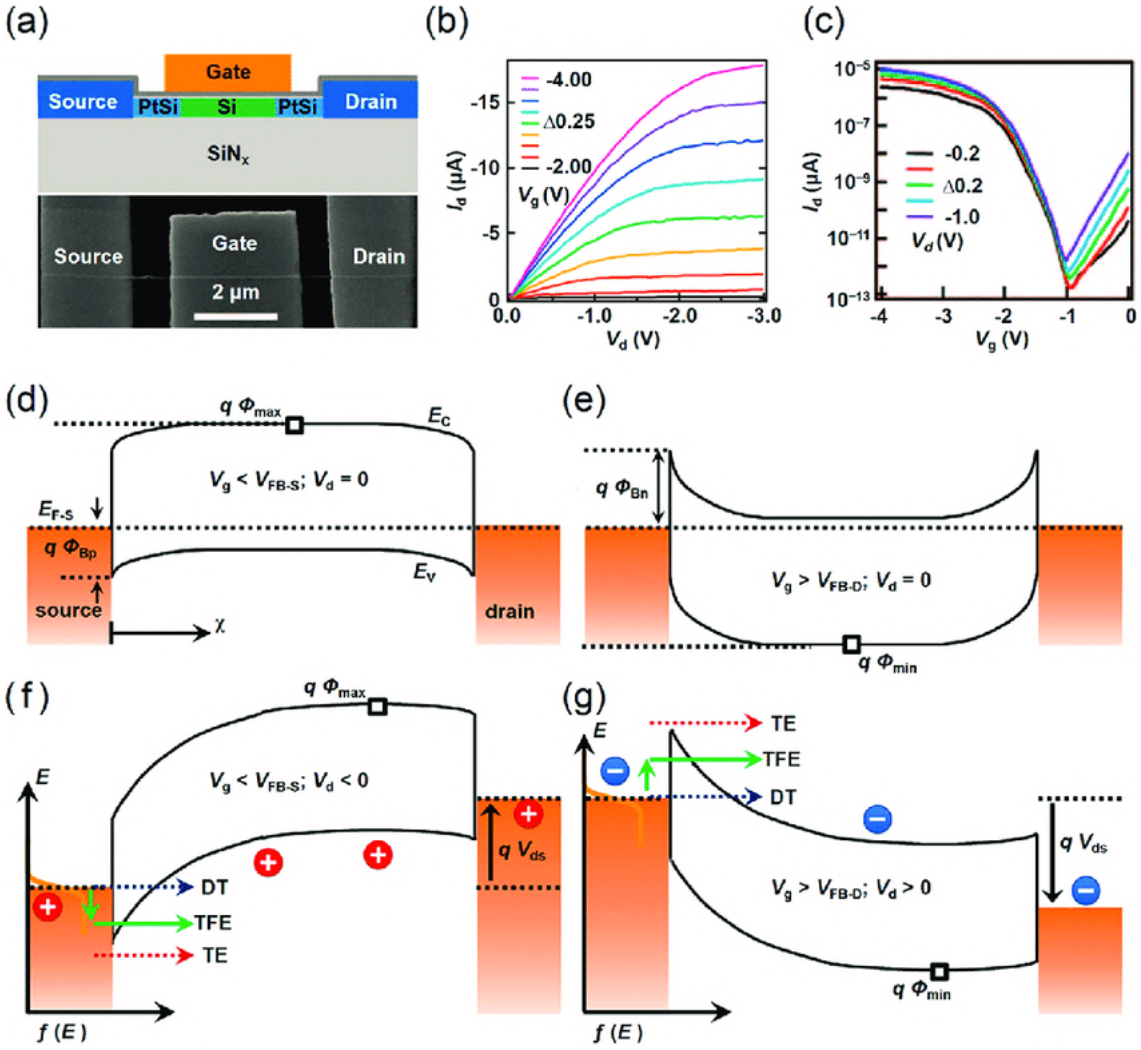


Figure 2.9: *Schottky-barrier nanowire FET. (a) Schematic illustration and SEM image of a Schottky-barrier silicon nanowire FET with metallic PtSi contacts and a top-gate electrode. (b) Output characteristics of the Schottky FET with a p-channel. (c) Transfer characteristics of the FET, which show ambipolar behavior. (d-g) Schematic band diagrams of gated charge transport in a Schottky FET. The gated upward band bending with hole transports at $V_g < V_{FB-S}$ are shown in parts d and f. Corresponding gated downward band bending with electron transports at $V_g > V_{FB-D}$ are shown in parts e and g. For the injection processes, direct tunneling, thermal field emission, and field emission are considered.*

and semiconductor. At this point, it should be mentioned that not every material combination described above is suitable to create a rectifying Schottky barrier. If a material combination is used that creates a Schottky barrier height that is too low, current can flow in both directions and rectification will not occur. In this case, the contact is referred to as an ohmic contact. [29] [30]

A Schottky barrier can be created when an n-type semiconductor and its work function is smaller than the work function of the metal, or when the work function of a p-type semiconductor is larger than the work function of the metal. Three assumptions are made when describing a Schottky barrier:

1. the contact between metal and semiconductor must be so tight that no other material layer, such as an oxide, can be found

2. inter-diffusion is neglected

3. there are no impurities present at the interface of the two materials

Generally speaking, the Schottky barrier is the energy difference between the valence (or conduction) band edge of the semiconductor and the Fermi energy of the metal, while the band offset is the energy difference of valence (or conduction) bands of two materials that construct the interface. A first approximation to the actual height of the Schottky barrier is given by the approximation model of Walter Schottky and Nevill Mott which will be discussed and elaborated in the next section.[31] [29]

After considering the materials in isolation, one can consider what happens when they are brought together and an interface is formed. Due to a phenomenon called Fermi level pinning, the center of the bandgap is pinned to the Fermi level and metal-induced gap states occur. Since the Fermi levels of the two materials must match at the interface, there exists gap states that decay deeper into the semiconductor. More details will be given in the next section.

Depending on the semiconductor used, the strength of the Fermi level pinning effect varies. One consequence of this effect is that it is relatively difficult to make ohmic contacts, especially with Silicon or Gallium Arsenide (GaAs). Non-ohmic contacts, on the other hand, impede current flow and are seen as parasitic resistance. They unintentionally consume more power and thus reduce the performance of the device.

The transport mechanism for an occurring Schotty contact depends on the height of the Schottky barrier and is described by the following equation:

$$q\Phi_B = q(\Phi_m - \chi) \tag{2.1}$$

Where $q\chi$ describes the electron affinity, $q\Phi_B$ the Schottky barrier and $q\Phi_M$ the work

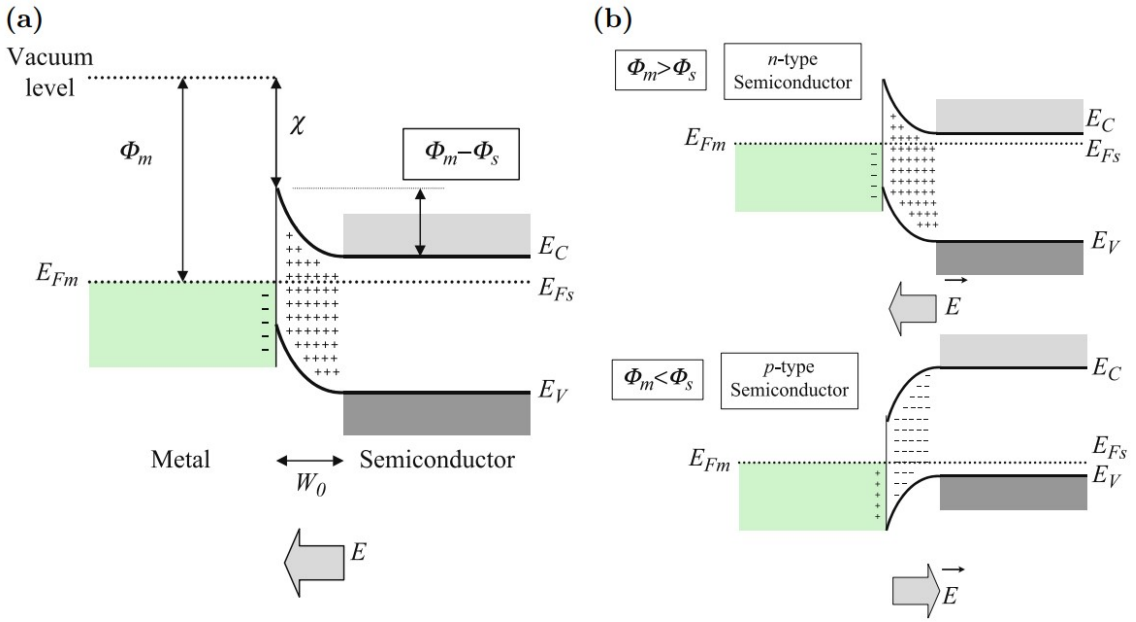


Figure 2.10: *a) Energy band and accumulated charge carriers at a junction between metal and semiconductor with work functions indicated. b) Creation of a Schottky contact and separation between two scenarios depending on Φ_M and Φ_S where the top image shows an n-type and the bottom image shows a p-type semiconductor. Movement across the junction of majority carriers is prevented by barrier height $|\Phi_M - \Phi_S|$.*

function of the metal. The resulting reverse saturation current is given by the formula:

$$I_0 = AB_eT^2e^{-\frac{\Phi_B}{k_BT}} \tag{2.2}$$

The relation between current and voltage can be described using the following equation:

$$I = I_0(e^{-\frac{qV}{k_BT}} - 1) \tag{2.3}$$

B_e represents the Richardson constant, A the area of the effective junction surface, T the temperature, V the voltage difference in the two regions, and k_B the Boltzmann constant.

If the height of the energy barrier $q\Phi_B$ is several times higher than k_BT, an equilibrium is reached and the connection surface remains free of current. Otherwise, an effect called thermionic emission (TE) occurs. This effect can be described by means of two current densities, one in the direction of semiconductor to metal $J_{S\to M}$ and the other way around from metal to semiconductor $J_{M\to S}$.

$$J_{S\to M} = A^*T^2e^{-\frac{q\Phi_B}{k_BT}}e^{\frac{qV}{k_BT}} \tag{2.4}$$

$$J_{M\to S} = -A^*T^2e^{-\frac{q\Phi_B}{k_BT}} \tag{2.5}$$

$$A^* = \frac{4\pi qm^*k_B^2}{h^3} \tag{2.6}$$

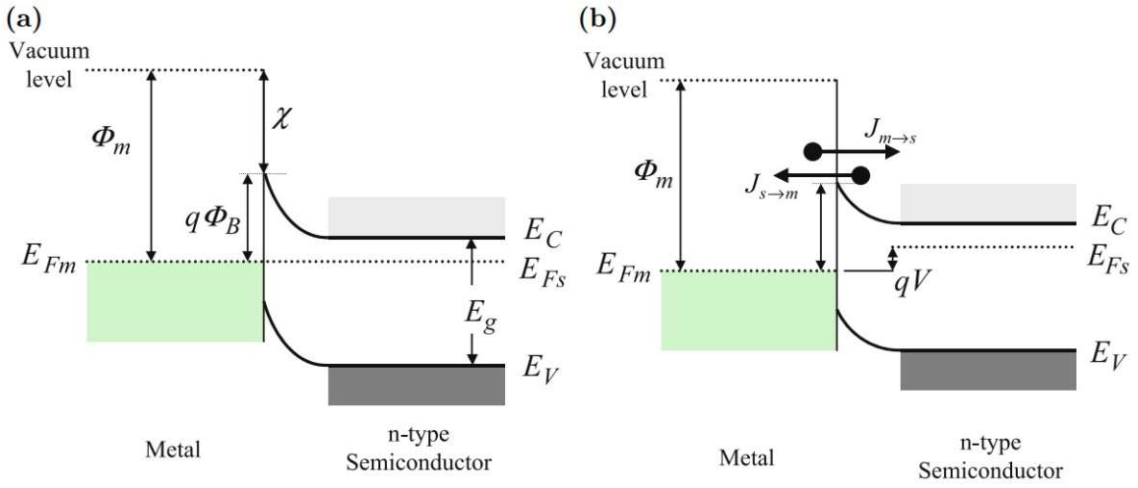


Figure 2.11: *Energy band diagram of a junction between a metal and a n-type semiconductor. a) Energy band diagram at equilibrium. b) Energy band diagram when the bias voltage V is lowered and therefore the barrier height $q\Phi_B$ is lowered too. As a consequence $J_{S\to M}$ is increased while $J_{M\to S}$ is unaffected by changes of V.*

$$J = J_{S\to M} + J_{M\to S} = A^* T^2 e^{-\frac{q\Phi_B}{k_B T}} (e^{\frac{qV}{k_B T}} - 1) \tag{2.7}$$

Where A^* is the effective Richardson constant, m^* is the effective mass, and h is Planck's constant.

The current density $J_{S\to M}$ results from the accumulated electrons in the semiconductor region that have a higher energy than the barrier and can therefore overcome it and move towards the metal. At the current density $J_{M\to S}$ the barrier height $q\Phi_B$ is constant independent of the existing bias voltage V. Due to the fact that no current flows in equilibrium, the two current densities cancel each other out and the result is:

$$J_{M\to S} = J_{S\to M} \quad at\ V{=}0 \tag{2.8}$$

In addition to thermionic emission (TE), there is a second transport mechanism that occurs in a Schottky barrier called thermal field emission (TFE). In TFE, electrons that do not have enough energy to overcome the Schottky barrier tunnel through thinner areas of the Schottky barrier. In addition to the mechanisms already mentioned, direct tunneling (DF) from the energy level E_{F_m} through the Schottky barrier also occurs.[32]

2.2.3.2 Schottky-Mott rule and Fermi level pinning

A first approximation to calculate the Schottky barrier is done by the Schottky-Mott rule. The approximation is based on the difference between the vacuum work function of the metal Φ_{metal} relative to the vacuum electron affinity of the semiconductor χ_{semi}:

$$\Phi_B^{(n)} \approx \Phi_{metal} - \chi_{semi} \tag{2.9}$$

$\Phi_B^{(n)}$ ... Schottky barrier height for electrons

$$\Phi_B^{(p)} \approx E_{bandgap} - \Phi_B^{(n)} \tag{2.10}$$

$\Phi_B^{(p)}$ ... Schottky barrier height for holes
$E_{bandgap}$ ... band gap in the semiconductor

This model originates from a thought experiment in which two different materials are brought together in a vacuum. With the help of the Schottky-Mott rule, the existence of band bending in semiconductors could already be clarified. Band bending refers to an upward or downward bending of the electronic band structure at a junction or interface. However, the Schottky-Mott model has a major weakness since it has been shown experimentally that there are large deviations between the calculated approximation of the Schottky barrier and the actual Schottky barrier. The reason for this is the so-called Fermi level pinning, which causes that some points on the band gap, where there is a finite density of states (DOS), are pinned to the Fermi level or in other words locked. Due to this fact, the height of the Schottky barrier is almost no longer dependent on the work function of the metal, resulting in the following relationship:

$$\Phi_B \approx \frac{1}{2} E_{bandgap} \tag{2.11}$$

In fact, it has been found empirically that neither the first nor the second approximation is absolutely correct. The choice of element in the metal does have an effect on the barrier and there is a weak correlation between the work function of the metal and the barrier height. It should be noted that the actual effect of the work function of the metal is only a fraction and therefore not 100% consistent with the Schottky-Mott rule.

The Fermi level pinning effect is strong in several popular semiconductors such as Silicone, Germanium or Gallium Arsenide. Nearly all metals form a significant Schottky barrier to n-type Germanium and an ohmic contact to p-type Germanium, since the valence band edge is strongly pinned to the metal's Fermi level. Fortunately, there are ways in the form of additional fabrication steps to loosen up this pinning. Adding an intermediate insulating layer to unpin the bands could be one of these solutions.[33] [34] [35]

Chapter 3

Experimental Techniques

In chapter 3 we look at the journey from the wafer to the finished transistor. We start by discussing the characteristics of the wafers supplied and the criteria used to manufacture them, as well as a description of the stack and their layer thicknesses. We then move on to the process steps used in the fabrication and the equipment that is required. Then we inspect possible top gate structures that we can apply to the transistor and how the fabrication changes when the top gate structure is changed. Finally, we will talk about the electrical characterization, the measurement equipment used and what measurements were used to finally characterize the devices and what conclusions can be drawn from them. At the end of the chapter, it should be clear where the results in chapter 4 come from and which steps had to be taken for this.

3.1 Fabrication of GeSn Samples

3.1.1 Sample Properties

The transistors are fabricated in a top-down process. In this process, a grown stack is patterned to fabricate structures. Thanks to a collaboration with the Johannes Kepler University (JKU) in Linz, the stacks were provided by our partners and a documentation with possible dislocations or deviations or a more detailed description of the actual samples was included. The scientists from JKU Linz who contributed to the timely delivery are Johannes Aberl, Enrique Prado Navarrete and Moritz Brehm.

3.1.1.1 GeSn on s-SOI

1. First Batch
The first delivery contained four different samples. The samples differ in terms of the temperature in which they were grown and whether they are capped or not. These variations were chosen because it is difficult to commission stacks without prior experience and only subsequent fabrication or measurements will determine the direction of further research.

A common feature of all samples of the first delivery is the $8nm$ thick Germanium-Tin layer and the 4% Tin content in the Germanium. In addition, strained SOI was chosen as growth substrate. The concept of strained Silicon (s-Si) relies on an alteration of the equilibrium lattice constant of Si through externally applied stress. Due to the modified lattice constant, the electronic band structure of Si is changed resulting in enhanced electronic properties. More specifically, the carrier mobilities are enhanced with the mobility enhancement being a strong function of the magnitude and the direction in which the crystal is stressed. SOI in general stands for silicon on insulator and due to the isolation provided by the oxide layer, the junction capacitances are reduced while strained Si results in higher mobilities, thereby increasing the overall performance.

The first stack consists of a total of six layers whose exact composition is described in more detail in figure 3.1.

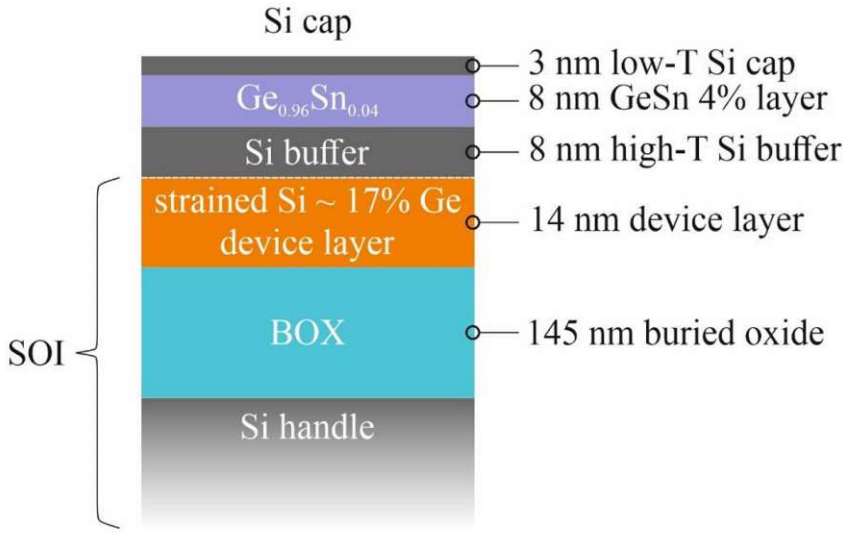


Figure 3.1: *Structure of the first four samples received with 4% Sn content in Ge and s-SOI*

The term BOX stands for buried oxide and is used to separate the strained silicon layer from the silicon substrate. This structure enables shorter switching times and lower power consumption, especially with regard to leakage currents.

Inital Name	Given Name	Thickness & Material	Grown at	Si cap	Roughness
5319 BAP-SGT	GeSn04_02	8nm $Ge_{0.96}Sn_{0.04}$	250°C	3nm	1.29nm
5328 BAP-SGT	GeSn04_03	8nm $Ge_{0.96}Sn_{0.04}$	175°C	3nm	367pm
5325 BAP-SGT	GeSn04_01	8nm $Ge_{0.96}Sn_{0.04}$	175°C	w/o cap	394pm
5326 BAP-SGT	GeSn04_04	8nm $Ge_{0.96}Sn_{0.04}$	100°C	3nm	186pm

Table 3.1: *Listing of the properties of the 4% GeSn samples and their working names*

As far as the naming of the individual samples is concerned, the material composition (in our case GeSn) is followed by the percentage of Tin and then a consecutive number in order to better distinguish the samples from each other during measurements and fabrication. As can be seen from the table 3.1, three of four samples are very smooth and thus have low surface roughness while sample GeSn04_02 is an outlier with 1.29nm. A higher surface roughness can show up with a local maximum of the electric field strength at peaks. After microscopic examination by JKU Linz, dislocations and Tin segregations were observed on samples GeSn04_02 and GeSn04_04.

3.1.1.2 GeSn on SOI

2. Second Batch
Two different samples were supplied for the second delivery from JKU Linz. One sample with 4% Tin content and the other with 2% Tin content. Some changes were made

compared to the first delivery. Firstly, the device layer was changed from strained Si to Si with alignment (001) and additionally the layer thickness was increased from 14nm to 20nm. Another change of the layer thickness was made for the BOX from 145nm to 100nm and for the GeSn layer which was reduced from 8nm to 4nm, to be seen in figure 3.2.

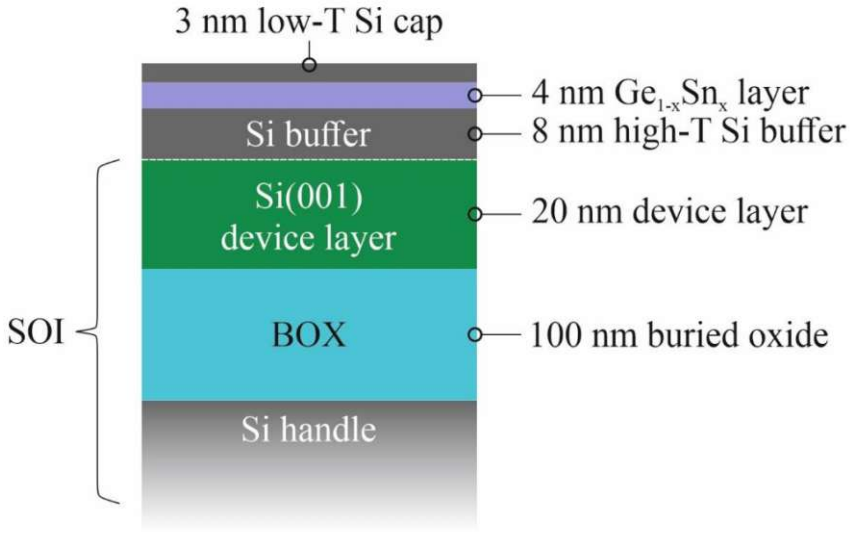


Figure 3.2: *Structure of the fifth and sixth samples received with 4% and 2% Sn content in Ge and SOI*

No dislocations were observed in the two samples delivered compared to the first delivery. Based on the experience and the results from the previous measurements, it was decided to order the samples at a growth temperature of $175°C$ with a 3nm thick Silicon cap.

Inital Name	Given Name	Thickness & Material	Grown at	Si cap	Roughness
5352 BAP-SGT	GeSn04_05	4nm $Ge_{0.96}Sn_{0.04}$	$175°C$	3nm	275pm
5353 BAP-SGT	GeSn02_01/02	4nm $Ge_{0.98}Sn_{0.02}$	$175°C$	3nm	194.3pm

Table 3.2: *Listing of the properties of the 4% and 2% GeSn samples and their working names*

As shown in the table 3.2, a total of three devices were made from the two stacks. The reason for a new 4% Tin sample is to have a comparison between s-SOI and SOI and to learn about the effects of changing film thicknesses. Since the controllability of the transistors on the GeSn04 chips did not perform impressively well and this is probably due to the high Tin content, the 2% Tin sample was ordered.

3. Third Batch

The third and last delivery was associated with two major changes. Since the reduced Tin content led to interesting results, samples with even lower Tin content were ordered, in this case with 1% and 0.05% Tin in Germanium. As for the stack, it remained largely

unchanged with the exception of the material composition just discussed and is constructed according to figure 3.3.

Since the XRD machines at JKU Linz were not operational at the time the samples were produced, there could be a slight deviation in the substrate with lower Tin content in the order of ±0.1%.

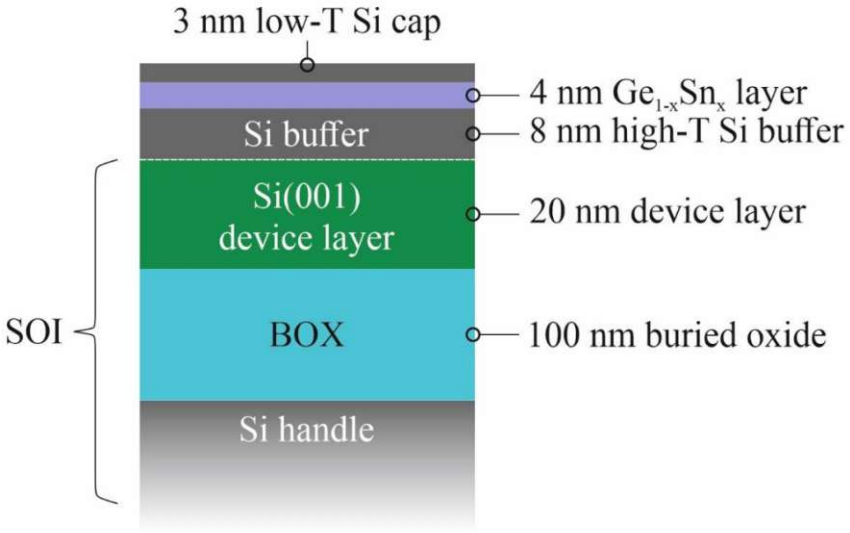


Figure 3.3: *Structure of the seventh and eighth samples received with* 1% *and* 0.5% *Sn content in Ge and SOI*

Inital Name	Given Name	Thickness & Material	Grown at	Si cap	Roughness
5417 BAP-SGT	GeSn01_01/02	4nm $Ge_{0.99}Sn_{0.01}$	175°C	3nm	162.8pm
5418 BAP-SGT	GeSn005_01/02	4nm $Ge_{0.995}Sn_{0.005}$	175°C	3nm	168.5pm

Table 3.3: *Listing of the properties of the* 1% *and* 0.5% *GeSn samples and their working names*

In addition to the information given in the table 3.3, it can be said that no dislocations occurred in either sample and a rather low hole density was observed in the epilayer.

Looking at the deliveries collectively, the following changes can be seen over the course of the total of eleven devices:

- s-SOI → SOI
- various grow temperatures → 175°C
- no cap → 3nm Si cap

- 8nm device layer → 4nm device layer
- 145 nm BOX layer → 100nm BOX layer
- tin content 4% → 2% → 1% → 0.5%

3.1.2 Fabrication Processes

At the beginning of the transistor fabrication process, the sample is cleaved to the desired dimensions. The sample is cleaved with a metal needle that creates a predetermined breaking line. By applying force to this line, the sample should break according to the pre-scored line. The target dimensions are approximately 10x10mm.

After this step, there are potential contaminations on the device, which is why additional cleaning steps are necessary. For this purpose, the sample is put into an acetone bath and placed into an ultrasonic bath at low intensity for about 20 seconds. The sample is then transferred to an isopropanol bath to remove the last acetone residues. Drying takes place using a nitrogen gun. Besides the cleaning effect, this step also serves to prepare the sample for lithography.

The next fabrication process is lithography. In this step, the transistor channel i.e. the GeSn nanosheets are patterned. First of all, a photoresist called AZ5214 has to be applied. The sample is placed in a spinner, the vacuum pump is activated to keep the sample in the center of the spinner and then the photoresist is applied in such a way that the whole sample is covered with resist but not too much that the layer thickness becomes too thick or the resist gets on the bottom surface of the sample. The applied photoresist is exposed to a hot plate at $100°C$ for 60 seconds to dry.

In the next step, the masks pre-drawn in the CAD software AutoDesk are transferred to a LaserWriter. The samples were exposed with a dose of 140 J/cm^2. After exposure, the samples are developed. The samples are immersed for 17 seconds in the developer liquid AZ726MIF, then moved for 5 seconds in coarse bubbling water and 5 seconds in fine bubbling water. Again, drying takes place using a nitrogen gun. After this fabrication step, one can observe under the microscope how well the developing has worked. For example, it may be that underdevelopment has occurred and the samples need to be redeveloped or that the alignment of the mask does not match well with the device at hand. Therefore, microscopic observation is used to check how sharp the desired wires, pads or gates are.

The final process to reveal the wires is done by Reactive Ion Etching, abbreviated RIE. This method of dry etching is performed for 50 seconds and is followed by plasma ashing. This etches all regions on which there is no photoresist after development down to the BOX, leaving only the wires.

What remains to proceed to the fabrication of the source and drain pads is the surface passivation. This step is necessary to separate the created channel from the later applied top gates. Atomic Layer Deposition, abbreviated ALD, was performed for 110 cycles at $200°C$, depositing 11.7nm aluminum oxide (Al_2O_3). Atomic layer deposition is a technique for growing thin films for a wide range of applications. ALD is a special variant of the chemical vapor deposition (CVD) technique where gaseous reactants (precursors) are introduced into the reaction chamber for forming the desired material via chemical surface reactions.

Now that the wires have been successfully manufactured, the S/D pads are fabricated. Analogous to the processes described above, cleaning is again carried out using acetone and an isopropanol bath. Photoresist is again applied in the spinner and the photoresist is dried on the hot plate, and lithography takes place repeatedly using the LaserWriter. In this case, however, a mask is used in which the previously produced wires are hidden and the structures of the source and drain pads are faded in. Special care is required at this point when configuring the LaserWriter, as the mask for the wires must be aligned with the mask of the pads by means of optical inspection. Therefore, as an optical aid for the alignment, markers in cross form were drawn in the masks. The parameters for exposure and development were retained due to the flawlessly produced wires.

After development, a new process is introduced. This involves immersing the samples in buffered hydrofluoric acid (BHF) for 18 seconds and finally washing them off for 7 seconds with hydrogen iodide (HI) which was diluted with water in a 1:3 ratio. This step removes silicon oxide (SiO_2) in the areas of the S/D pads.

After all necessary steps for the preparation of the S/D pads have been completed, the actual application of the pads takes place. Sputtering is the method of choice. Sputtering is a physical process in which the vaporization occurs of a solid material by bombarding it with ion energy. This is a process widely used in the formation of thin films on materials, engraving techniques, erosion of white material and analytical techniques.

The sputtering process used on the vonArdenne machine can be divided into four steps:

- Cleaning of the sample holder
- Reverse Sputtering
- Cleaning of the target holder
- Deposition of Aluminium (Al)

The cleaning process for the sample holder and the target holder are performed for two one-minute cycles at 100W. To remove unwanted remnants, reverse sputtering is started

for five one-minute cycles at 100W. Last but not least, the desired element, in this case Al, is applied for five one-minute cycles at 50W. This process results in an Al layer thickness of 125nm.

By sputtering, the Al for the pads is not only applied to the desired regions, but the entire sample is covered by it. To remove the excess material from the unwanted areas, a process called lift-off is performed. This involves placing the sample in an acetone bath on a hot plate at approximately $60°C$. As a guideline for the dwell time on the hot plate, experience has shown that a period of between two and five minutes can be assumed. One characteristic that becomes apparent with a successful lift-off is that the thin aluminum layer begins to contract. If this characteristic is observed, a syringe full of acetone can then be used to flush away the already slightly detached Aluminum by ejecting liquid. A container full of acetone placed in an ultrasonic bath and final cleaning with isopropanol ensures that no unwanted Aluminum remains on the sample. The efficiency of this operation can be checked by looking into the microscope and, if necessary, the steps from the ultrasonic bath can be repeated.

There is now one step missing to complete the fabrication of the S/D pads. The effective channel length can be adjusted by annealing, more precisely Rapid Thermal Annealing (RTA), in which an exchange takes place between the metal and the semiconductor. The desired channel length is about $2 - 3\mu m$ and the resulting segment should be centered between the two pads. For annealing, the sample is heated for 60 seconds at $500°C$ in an atmosphere of hydrogen (H_2) and nitrogen (N_2).

After this step, the resulting channel length should be observed under a microscope and measured if necessary. If the resulting channel length does not correspond to the expected result, the annealing process can be repeated as often as necessary until the desired channel length is reached. However, annealing should not be carried out too carelessly, as too long annealing can lead to the segment becoming too short or, even worse, to there being no segment at all since it has been completely replaced.

For the finished transistor, after making the wires and the S/D pads, only the gate is missing. For the samples with GeSn on strained-SOI it was decided to use single top gates, STGs for short. This decision can be justified with the fact that in the first phase of the thesis it should be tested how the structures behave generally and in which direction it is advisable to continue research. Since STGs are simple in fabrication and do not behave very complex in terms of measurement, this gate form was used to exclude other interfering factors for the time being.

Single top gates are characterized by the fact that they cover the channel beyond the actual segment length and thus lie above the left and right interfaces. By default, a gate width of $5\mu m$ is used at the Institute, but this is adjusted if the segment has become longer than said width. Since the position or the width of the top gates may have to be

changed when creating the mask for lithography, it is recommended to take photos of the structures in advance in order to incorporate them into the mask design.

As already described for the production of the S/D pads, the following steps must be carried out again for the application of the top gates:

- Cleaning of the sample in acetone and isopropanol
- Drawing and converting masks
- Evenly applying a photoresist and drying it
- Lithography by LaserWriter
- Development for 18 seconds and rinsing it with water

Instead of the sputtering method normally used for the drain and source contacts, a new process is now presented for the gate contact. Unlike sputtering, where the target is basically bombarded with the preselected elements, a gentler way of applying the materials is by vapor deposition, in our case Chemical Vapor Deposition or CVD for short. CVD is a technique where a solid material is deposited from a vapor by some chemical reaction occurring on or in the vicinity of a normally heated substrate surface.

Another change compared to sputtering is the selection of elements. Instead of Aluminum, in CVD a $10nm$ thick layer of Titanium is deposited first, followed by a $100nm$ thick layer of Gold. During the actual deposition, low evaporation rates in the range between $0.05nm/s$ and $0.1nm/s$ are chosen to avoid an unwanted breakout of the molten material onto the sample in the device. The electron beam used to heat the material is slightly changed in position from time to time to avoid crater-like formation.

The lift-off is performed analogously to the process described after sputtering or, in this case, evaporation. In this part of the fabrication process, the lift-off can be repeated several times to remove unwanted particles and the progress can be checked with the microscope.

Compared to the previous process steps, the final step to finish the transistors is relatively simple. A hot plate is preheated to $90°C$ and the prepared sample with the 60 transistors is placed on it for 30 minutes. Thereby one gets rid of trapped charges. Traps are filled in processes such as EBL or by exposure in the LaserWriter. To discharge these charges a temperature treatment is performed. Another advantage is that adsorbates such as oxygen or nitrogen are dissolved.

As for storage, the devices are stored in an airless container between periods of several hours or longer. In this device, the samples can be placed in an almost airless space

without fear that the metals will start to oxidize after a short time and distort the electrical properties or worse make them unusable.

In summary, the following steps must be followed in order to make a transistor:

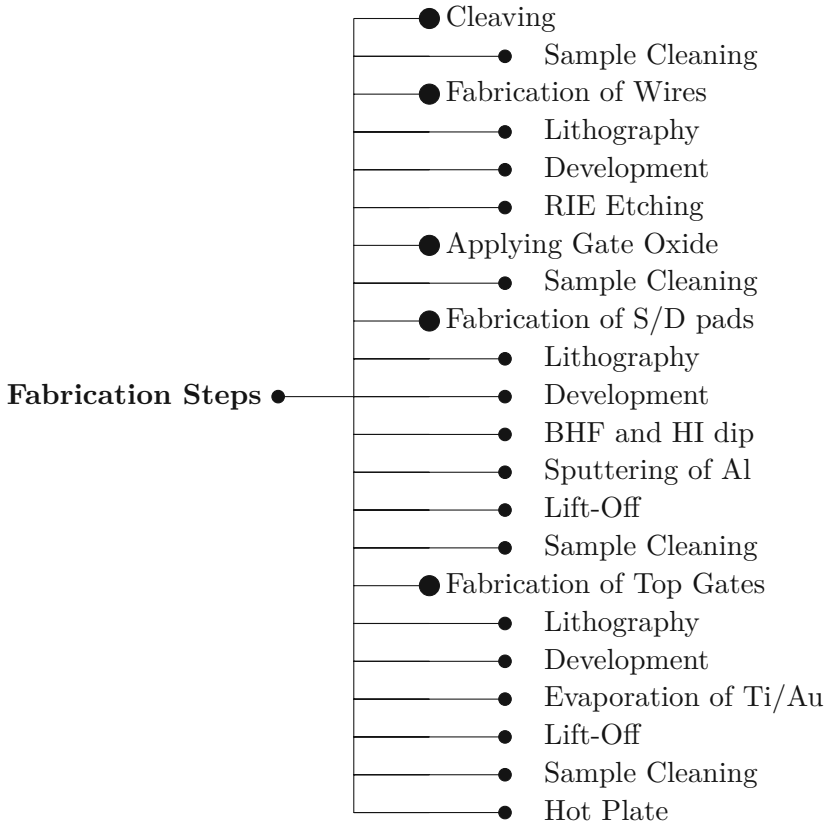


Figure 3.4: *List of the necessary process steps for the fabrication of a transistor in the clean room.*

Devices that were made according to the process steps mentioned above: **GeSn04_01/02/03/04/05**, **GeSn01_01/02** and **GeSn005_01/02**

For the samples with 2% tin content, after the measurements showed promising results, another fabrication step was added after the application of the STG. Since only 30 of 60 available structures were fabricated with STGs, there were enough free places for dual top gates (DTGs), triple top gates (TTGs), splitted triple top gates (sTTGs) and middle gates (MGs). The layout of these structures can be seen in Figure 3.5.

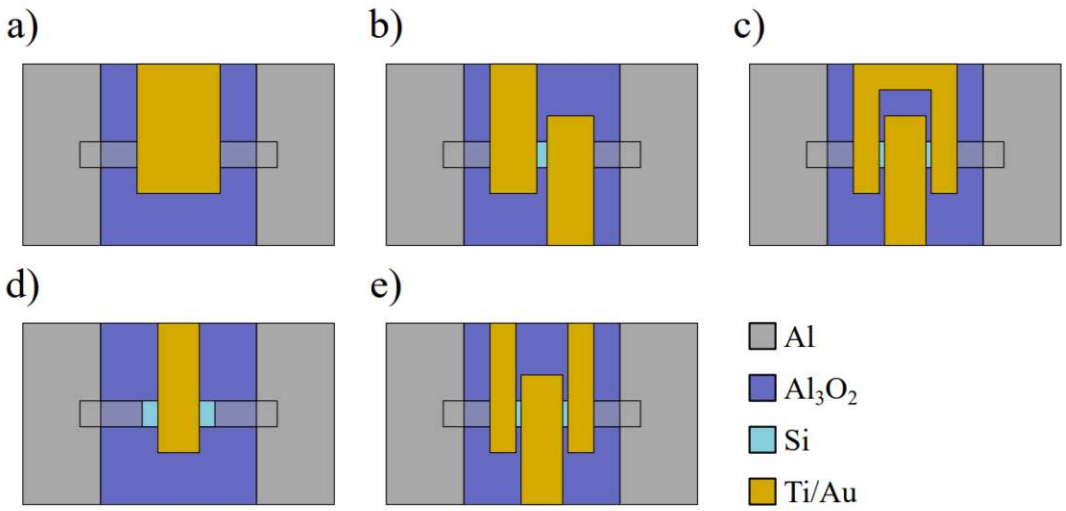


Figure 3.5: *Structures of various top gates in use*
Upper row: a) Single Top Gate b) Dual Top Gate c) Triple Top Gate
Lower row: d) Middle Gate e) splitted Top Gate.

STGs, along with Middle Gates, are the easiest gate structures to produce. Single Top Gates are wide enough to cover both interfaces and the whole segment. In contrast, Middle Gates are much thinner and are placed in the middle of the segment without covering the interfaces. [36]

As the name Triple Top Gate suggests, three gate electrodes are used here. Two polarity gates are placed over the interfaces as usual while the control gate is placed in the center of the segment. Another variant of the TTGs are the so-called splitted Triple Top Gates (sTTGs). The main difference between sTTGs and TTGs is that sTTGs electrically separate the polarity gates so that separate voltages can be applied. TTGs, on the other hand, have two polarity gates, but these are connected to each other and only one voltage can be applied. sTTGs are also more difficult to measure, since 5 measuring tips are required at the drain, source, CG and the two PGs for electrical characterization.

DTGs, TTGs and sTTGs and thin MGs need very precise techniques to place the individual gates due to the placement requirements. Since the LaserWriter is only globally aligned and therefore chip-wide, but such a high level of accuracy is required to align the top gates per structure, a new process step is introduced, the so-called electron beam lithography or short (EBL). Here the exposure is done by an electron beam. For segments that have become very short it would be unthinkable to use the LaserWriter because the necessary resolution is too low. A common feature, however, is that a resist must be applied at the beginning. This is not a light-sensitive photoresist but a liquid called polymethyl methacrylate (PMMA) resist (AR-P 679.04) which reacts to the electron beam. The PMMA is applied dropwise to the sample and spread at 4000 rpm in the spinner

for 30 seconds. Drying of this resist is again performed on a hot plate at approximately $170°C$ for a duration of ten minutes. The sample is then introduced into the e-Line and calibrations are performed. Afterwards, the drawn mask is converted and the placement of the gate electrodes is adjusted to the structures and their segments. When drawing the mask, care was taken to draw the top gates with three different layers. One layer was for regions that are very close to the wire, the second layer as a connector to large areas and the third layer for large areas that are not critical in terms of positioning.

Lithography via the e-Line is a rather time-consuming process. The preparations alone, without the actual electron beam performing, can be estimated at about two hours. About three hours must be calculated for the lithography of the three layers, whereby the first layer is finished more quickly due to the small areas, whereas the third layer takes a correspondingly long time. This information is of course machine- and device-specific. Newer EBL machines can do the actual lithography of the three layers in probably less than an hour.

After the ejection of the samples from the e-Line, development follows, just as after the LaserWriter. The developer used is AR-P 600-56 and the sample is immersed in it for 35 seconds in circular movements. This completes the development step and a 10nm Ti and a 100nm Au layer can be evaporated as with the STGs and a lift-off can be carried out to bring the manufacturing process of the top gates to an end.

Devices with Top Gates that were made using EBL: **GeSn02_01/02**.

3.2 Electrical Characterization

Now that the samples supplied and the individual production steps have been largely clarified, the electrical characterization of the transistors can take place. The characterization procedure changes with the selected top gates on the chip surface. In the case of promising measurement results or in the case of a newly fabricated GeSn-ratio, additional temperature measurements were carried out in order to specify the behavior at low and high temperatures more closely in addition to the measurements at room temperature.

3.2.1 Measurement Setup

For most of the measurements, the measuring equipment used was a prober with four measuring tips from the Lakeshore company with the model designation PS-100. With this device, very fine measuring tips can be placed on the inserted samples and air can also be pumped out. The prober is connected to an analyzer from the company Keysight named B1500A and with it voltage can be applied to the measuring tips and current can be measured.

Low temperatures can be achieved by connecting a liquid nitrogen dewar via a transfer line to the PS-100. To further test the temperature dependence at higher temperatures

of different samples, the LakeShore PS-100 offers the possibility to connect a temperature controller to heat up the transistors. The device under test (DUT) or the radiation shield can be heated separately. The temperature measurements were started at 77K with the heat controller deactivated and only used to display the temperature. To gradually increase the temperatures, the supply of nitrogen was reduced in small increments and the temperature controller was set to a defined target value and began to heat up the sample. At room temperature, the nitrogen supply was completely turned off and the controller alone gradually heated the DUT up to 400K.

Since the LakeShore prober is equipped with only four measuring tips, a different measuring instrument must be used for measuring sTTGs that require five measuring tips. For this purpose, a measuring device from Karl Zuss was used, which is connected to an analyzer from HP with the model number 4156B. This probing station has a total of six measuring tips and the sample can be darkened. However, this measuring station does not offer the possibility to pump out air or to perform temperature measurements.

3.2.2 Transfer Characteristics

A very basic and fast way to better understand the behavior of a transistor is to measure transfer curves and thus determine the transfer characteristics. To do this, the sample is placed in one of the probing stations mentioned above and, depending on the top gate structure and the required measuring tips, these are placed on the drain, source and gate electrodes. Usually the voltage values at the drain and source terminals are taken as symmetrical values ($VD = -VS$). The voltage at the gate electrode is continuously changed and the absolute drain current I_D is measured. If a DTG, TTG or sTTG is used for the gate structure then this 1-D sweep can be extended to a second dimension where the polarity gate can be switched between two values in addition to the control gate (CG). This switching of the voltage values at the polarity gate is responsible for the changing p- respectively n-mode of the transistor. Typically, the sweep of the gate voltage V_{TG} or V_{CG} starts at negative values and ends at positive values and immediately afterwards the reverse direction, i.e. from positive to negative values, is also measured. This type of sweep is called a double sweep. A sweep in one direction only is called a single sweep. In addition to the sweep measurement, a pulse measurement can also be performed. The approach differs in that with the pulse measurement the applied voltage values are held for a set period, while this is not the case with a sweep and the next value is targeted when a target voltage is reached. By holding the voltage, charging effects of the device can be better controlled and their effects can be minimized.

In order to better compare the devices with each other, the drain voltages V_D were usually set to values of $1mV$, $10mV$, $50mV$ and $100mV$. Depending on the DUT and its SOA (safe operating area), lower voltages were selected if necessary. A similar approach was taken for the selected top gate voltages. There, the range was usually $-5V$ to $+5V$. For samples with thinner oxide layers, a smaller voltage range had to be used. In the case of more robust samples, voltages of up to $\pm 7V$ were applied. During the first measurements

the leakage current I_{TG} is measured to find out the limits of the transistor. Since the drain current I_D also increases with rising temperatures when temperature measurements are carried out, the applied voltages are adjusted in such a way that the DUT can withstand the complete temperature run.

As mentioned above, this type of measurement provides a quick overview of the essential transistor properties. In addition to the conductivity, the on-off-ratio of the drain current but also if the on-off-plateaus establish can be read off and thus a first conclusion about the controllability of the sample can be made.

3.2.3 Output Characteristics

In the output characteristics measurement of a transistor, the absolute drain current is measured at different top gate voltages, similar to a transfer measurement. A difference to the transfer measurement is that the top gate voltage is changed stepwise and the applied drain voltage is swept. The transistor was measured symmetrically, which means that the voltage value on the drain electrode corresponds to the negative voltage value of the source electrode. The output characteristics measurement is used to determine how linear the measured transistor behaves. The transfer curves are superimposed on the corresponding top gate voltages and conclusions about the linearity can be drawn from the shape of the curves. The straighter the curves are, the more linear the DUT.

Depending on which gate structure is selected for the DUT, the output measurement varies. For conventional STG, the voltage V_{TG} is changed stepwise. For an RFET style transistor, the voltage at the control gate V_{CG} is changed. As with a transfer measurement, the temperature dependence can also be characterized in more detail with an output measurement. Usually the measurement starts at low temperatures at about 77.5K and is increased to 400K by the heat controller. The temperature intervals were set to 77.5K, 150K, 225K, 295K, 325K, 350K, 375K and 400K. Due to the increased nitrogen consumption at low temperatures and the effect that in the past some samples started to vibrate, we try to keep the measurement time in the colder regions rather short. It should also be mentioned that due to the Tin content and its melting point at about 230°C too high temperatures should be avoided.

There are several ways to visualize the output characteristics. One of them is to color-code the drain voltage sweeps at different top gate voltages and superimpose them and display the measured drain current I_D on a linear or alternatively on a logarithmic y-axis. In order to create a color map of the output measurement, the voltage on the top gate electrode V_{TG} or V_{CG} is plotted on the x-axis, the voltage of the drain pad V_D on the y-axis and the drain current I_D in the z-direction. This form of visualization can be used to quickly identify regions with particularly high or particularly low drain currents I_D and is called bias spectroscopy.

3.2.4 PG Sweep Characteristics

With the transfer and output characteristics, conventional transistors with STG can already be described well. If the characterization of RFETs is to be advanced further, a PG sweep is performed. As the name suggests, a sweep is performed over the voltage V_{CG} and the absolute drain current $|I_D|$ is measured. The main difference between this measurement and a conventional transfer measurement is that the measurement curves are recorded at different voltages at the polarity gate V_{PG}. Thus, the behavior of different operating modes can be shown and the n- and p-mode can be illustrated in more detail. Since the PG sweep depends on two measured variables, this is referred to as a 2-parameter measurement. As already known from the transfer measurements, the PG sweep can also be measured as a single or double sweep and at different temperature levels. Of course, the PG sweep cannot be performed for devices with an STG or MG since these do not have a polarity gate.

What makes this type of measurement particularly interesting is the fact that the mobility and controllability of holes and electrons can be characterized separately. While the n-mode primarily provides information about the electron transport, the p-mode can be used to inspect the hole transport. With this characteristic it is also exciting to observe at which values V_{PG} a switching between n- and p-mode is to be expected.

As far as visualization is concerned, two different paths can be taken, similar to the output measurement. Either the measured curves are overlaid and a distinction is made between the operating modes by means of color marking or distinguishing between solid and skip lines of the measured curves, or a 2D color map is created. If the latter is the case, the CG voltage V_{CG} is usually plotted on the x-axis, the PG voltage V_{PG} on the y-axis and the measured drain current I_D on the z-axis. As for the voltage values of the source and drain contacts, again a symmetrical distribution $V_D = -V_S$ was chosen and the usual voltage intervals of $1mV$, $10mV$, $50mV$ and for some devices $100mV$ were selected.

3.2.5 Effective Schottky Barrier Height Measurement - eSBH

As described in more detail in the theory section, a Schottky barrier occurs at a transition between a metal and a semiconductor, in the case of this master thesis between Al and Ge(Sn). The effective Schottky barrier height (eSBH) depends on the applied voltage and material parameters. To measure the eSBH the measurement method according to Schroder [37] was applied, which involves an I/V(T) thus a temperature dependent measurement approach. The Richardson constant is determined by multiple output measurements at different temperatures. However, this measurement method involves two assumptions. The first assumption is that the barrier height must be greater than k_BT and the second assumption is the existence of a small bias voltage to avoid the associated barrier-lowering effects.

In the master thesis of Fuchsberger [38] a Python script could already be successfully

written and used, which takes as input symmetric output measurements at different temperatures and delivers as output a projection of the resulting eSBH. This scheme was also used for this master thesis and the Schottky barrier heights for different top gate voltages V_{TG} were determined by means of the script.

If one now wants to determine the activation energy, it turns out that this results from the effective Schottky barrier height when this is evaluated at the zero-bias point, i.e. at $V_{DS} = 0$. Again, the symmetric output measurements at different temperatures are used to determine the activation energy. A Python script is needed to convert the measured data into a data format that can be used to create a contour plot in Origin.

The activation energy is usually visualized by means of a 2D color map. V_{TG} or V_{CG} are plotted on the x-axis, V_D on the y-axis and the activation energy E_a in eV on the z-axis. The color coding of the activation energy in the 2D map makes it particularly easy to identify regions with maxima and minima. For RFET devices, usually two color maps are provided. One color map for each operating mode to better distinguish between p- and n-mode.

Chapter 4

Results and Discussion

This chapter of the master thesis deals with the interpretation and discussion of results. In the course of the experimental part, a total of 11 different samples were fabricated and four different ratios between Ge and Sn were tested. Because such a large number of samples were produced and eight wafers were ordered from the Johannes Kepler University in Linz, the requirements per delivery could be made more and more precise. In addition to the GeSn ratio, for example, the bottom layers were changed from sSOI to SOI and the device layer from 8nm to 4nm thickness. Based on measurements, it could also be determined that a silicon cap on the wafers makes sense and helps against oxidation, and good measurement results could be achieved when a grow temperature of 175°C was used in the manufacturing process. We do not focus the following pages on the approach as we already did in chapter 3 but on the final results. In addition to that, we look at a comparison of the samples and determine in which scenarios which GeSn ratios could be useful and in which categories the samples scored particularly well.

4.1 Evolution of the Project

During the experimental part of this master thesis, a total of 11 samples were fabricated. Since the literature [39] shows that already from 6.5% Sn in Ge a direct band gap results, we started with a Sn content of 4%. The first delivery included a total of four samples with 4% Sn where each sample was grown at a different temperature and some of them had a Si cap. From each of these samples a chip with 60 transistors was fabricated and electrically measured. For growth of the GeSn 4% samples a s-SOI 17% substrate was used. After the resulting transistors had slight deficits in the area of controllability, it was decided to switch from a sSOI substrate to SOI and to reduce the GeSn layer from 8nm to 4nm in order to counteract the problem. It was also found that the best on/off ratio could be achieved at a growth temperature of 175°C where the sample had a Si cap, so these two parameters were kept for subsequent orders. The samples **GeSn04_01, GeSn04_02, GeSn04_03** and **GeSn04_04** resulted from the first delivery.

The second order of samples had two functions. First, we wanted to see if there was better controllability at 4% Sn content and change from sSOI to SOI. Secondly, we wanted to find out what happens at lower Sn levels. The choice of GeSn ratio was halved and thus samples with 2% Sn were examined. The samples **GeSn04_05, GeSn02_01** and **GeSn02_02** result from this supply. During the fabrication steps at GeSn04_05, however, problems may have occurred with the application of the gate oxide and it may have become too thin. Only a few transistors could be used for measurements, and since this small number of available measured values does not allow a truly representative comparison with the other samples, the focus was subsequently placed on the 2% Sn samples. On GeSn02_01 and GeSn02_02 DTG, TTG as well as sTTG were placed by means of the eBL differently than on the previous transistors.

The last delivery with 1% Sn and 0.5% Sn forms a good possibility to draw conclusions between electrical behavior and GeSn ratio. Regarding the stack, no changes were made between the second and third delivery. Furthermore, as with the 4% samples, only STGs were placed. The resulting devices from this delivery are **GeSn01_01, GeSn01_02, GeSn005_01** and **GeSn005_02**.

4.2 Fabricated Devices

The journey to the finished transistor begins, of course, at the fabrication stage. In total, we were provided with eight different wafers in three deliveries. First, 4% Sn and 96% Ge were examined on sSOI. Then again 4% Sn but this time on SOI. This was followed by 2% Sn and 1% and 0.5% on SOI. Imaging techniques such as TEM (Transmission Electron Microscopy) and EDX (Electron Diffraction X-Ray Spectroscopy) were used to further validate the fabrication results and provide detailed insight into the Al-GeSn transition. The TEM and EDX results were provided by a partner university in Switzerland and cleaved samples were sent there. The GeSn device layer is embedded by two silicon layers.

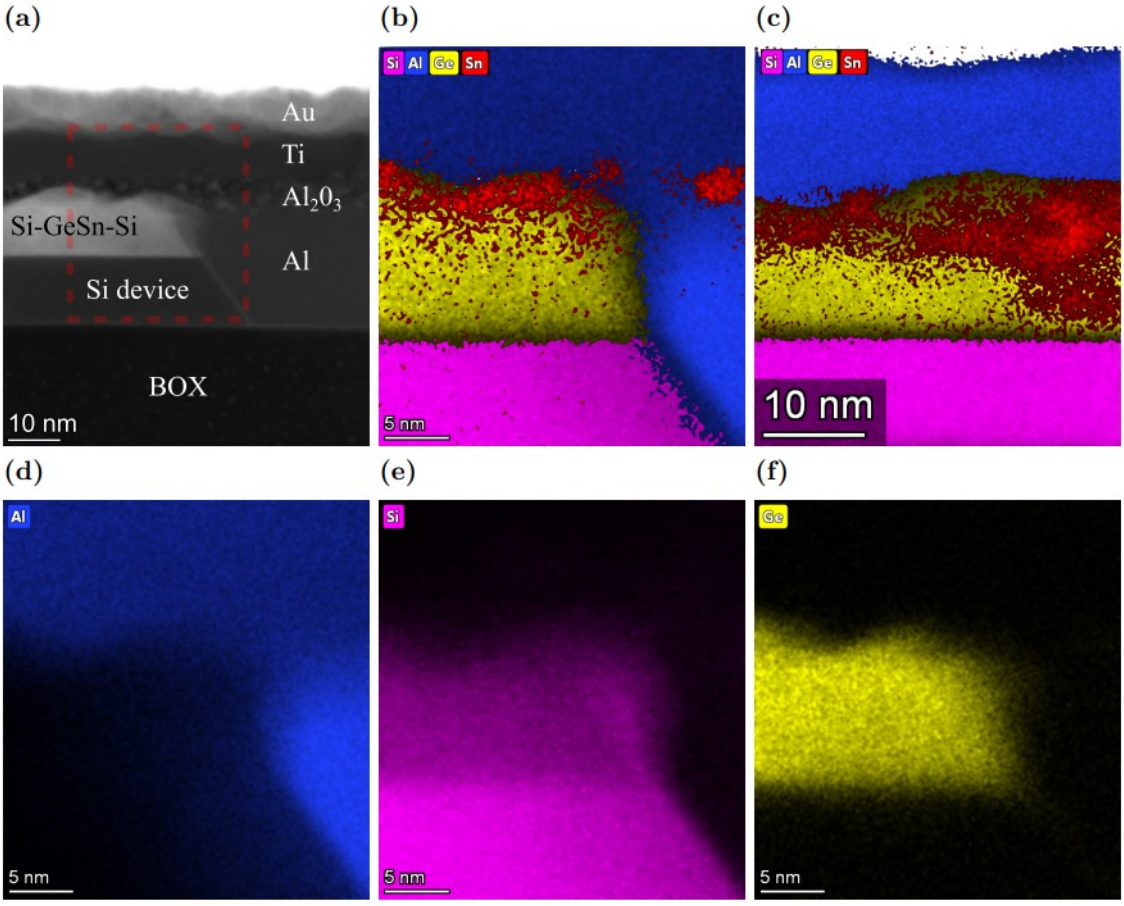


Figure 4.1: *TEM and EDX picture of the transistor (GeSn04_02) channel revealing the material composition. a) Al-GeSn interface b) Interface view and EDX analysis of Si, Al, Ge and Sn concentrations. c) Channel stack view and EDX analysis. d)-f) Detailed analysis of Al, Si, and Ge concentrations in the interface region.*

Above the GeSn layer is a Si layer grown at low temperatures and below is a Si layer grown at higher temperatures. Above this Si-GeSn-Si layer is the gate oxide layer Al_2O_3 in subpicture a) with a slightly grainy texture and on top of it the top gates made of Ti with a layer thickness of 10nm and Au with a layer thickness of 100nm.

Looking closer at image 4.1, especially sub image a), b) and c) we can see a sharp edge between Al and GeSn and thus a clear interface. Especially from images b) and c), where the Tin components in the Germanium are clearly visible in color, it is clear that Sn has mixed with Ge and formed an alloy, but the distribution of Sn deviates strongly from a homogeneous distribution within the Ge. This impression is reinforced by picture c) where a longer channel cross-section is given. This partial separation of Sn from Ge is probably related to the low melting point of Sn and the strong heating during annealing. It is assumed that Sn dissolves from Ge due to the heat and settles upwards until it reaches a barrier namely the gate oxide layer.

The bottom row of image 4.1 also brings some insights. If we look at the concentration of Al, we see that there is a high concentration in the area of the channel where annealing took place and near the gate oxide. In subgraph e) it can be seen that the Si concentration gradually decreases from the Si device layer to the Si-GeSn-Si layer and is almost imperceptible near and above the gate oxide layer. The last picture shows the Ge fractions in the channel cross section. As expected, Ge is located almost exclusively in the Si-GeSn-Si layer and forms sharp edges at the interfaces to Al. Further TEM and EDX images could not be provided in time because, according to the partner university in Switzerland that performs these imaging procedures, a lamella in the measuring device is broken and must first be replaced.

During the fabrication of the first sample GeSn04_01, black dots could be seen under the microscope in the area of the wire, as shown in Figure 4.2. We assume that the sample was probably heated too much for too long and these black spots could be Tin agglomerations or pile ups. However, we could not observe this occurrence on any other sample even though the fabrication parameters remained the same.

For samples $GeSn$02_01 and $GeSn$02_02, each top gate structure described previously was used. However, there were manufacturing problems with the DTG. The gap between PG and CG probably became too small and both electrodes were shorted. This may have resulted from a too small gap in the mask design or if the lift-off process did not work properly. Sometimes it works in this case to let a high current flow between both electrodes in the hope that this will melt small metal particles and both gates can be operated separately again. Unfortunately, this approach did not work for the samples, which is why these top gates are not discussed in the chapter 4.

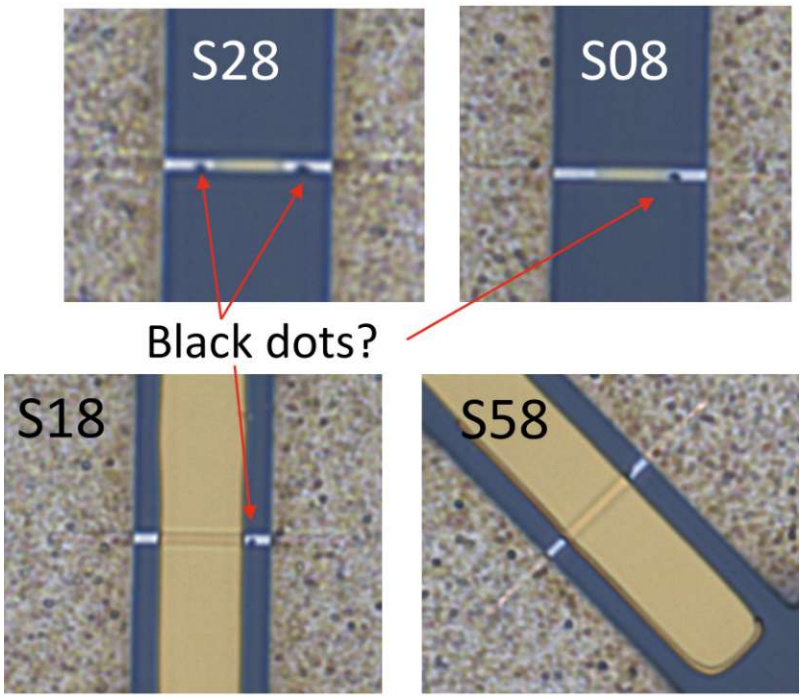


Figure 4.2: *Picture of structures of the first sample where black dots could be spotted and structure S58 without black dots as reference.*

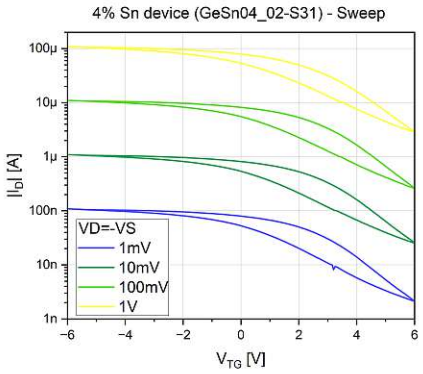
4.3 Transfer Characteristics

For the different GeSn ratios, the sample that showed the best results and where the measurement was reproducible was always chosen. This means that we will take a closer look at the samples **GeSn04_02, GeSn04_03, GeSn02_01, GeSn02_02, GeSn01_02** and **GeSn005_02** in detail as they performed best compared to other DUT. At the beginning of this section we will look at the transfer measurements and try to draw conclusions about the conductivity and controllability based on the figures and then the output characteristics of STG and TTG devices will be shown.

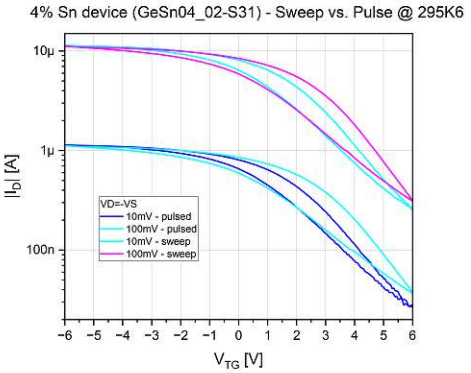
Since the distances between the polarity gate and the control gate have become too small during the fabrication process and the electrodes have probably been short-circuited to each other, no measurement data on dual top gates (DTG) can be shown. Transistors with TTG were produced for the samples with 2% Sn. Thus, in the triple top gates section, there is no comparison to other GeSn ratios but between samples **GeSn02_01** and **GeSn02_02**.

4.3.1 Single Top Gates

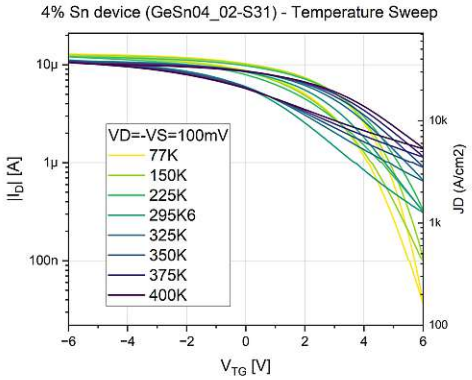
At the beginning of the transfer measurements we look at transistors with a single top gate, i.e. conventional Schottky barrier field effect transistors (SBFETs). We start with devices with a high Tin content and present devices with decreasing Sn in sequence. For



(a) *Transfer sweep measurement with various drain voltages V_D*



(b) *Sweep measurement vs. pulsed measurement*



(c) *A transfer sweep measurement with a fixed drain voltage V_D over various temperatures*

Figure 4.3: *Transfer Characteristics of a 4% Sn device with a STG*

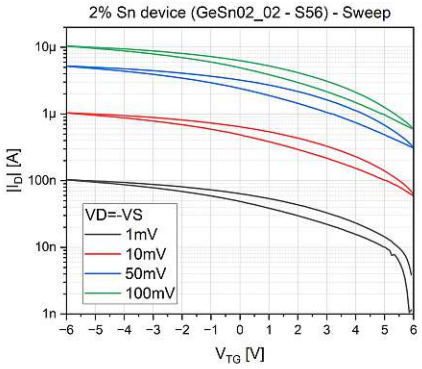
each transfer measurement, the evaluations for a sweep transfer, a comparison between a pulse and sweep measurement and finally a transfer characteristic curve over different temperatures are included. With the first figure, conclusions can be drawn about on-state and off-state, and the slope of the curve can be used to determine how well the transistor can be controlled. Since we expect a high conductivity due to the addition of Sn in Ge, we can also read off the maximum drain current I_D that flows through the wire. The next figure in the upper right corner shows a sweep and a pulsed transfer measurement superimposed. This comparison can be used to determine whether the sample is being charged and if so, how strong this effect is. With the last figure showing a sweep over several temperature steps we see the temperature dependence of the transistor on the left y-axis and on the right y-axis the current density J_D with the unit A/cm^2. Here the question arises whether a metallic or non-metallic behavior occurs and at which temperatures large deviations occur in comparison to room temperature.

4% Sn device - GeSn04_02: Figure 4.3a shows that for a tenfold increase in drain voltage V_D, a tenfold increase in drain current I_D can be achieved, which suggests a linear output characteristic. The curves are very similar in shape and appear as shifted with respect to the y-axis. Comparing a sweep with a pulsed measurement as in figure 4.3b one notices that the pulse measurement is not as smooth as the sweep measurement and lower drain currents are reached. If you look at the resulting hysteresis, you can see that it is wider for a sweep. In both figures described above, it can be seen that an on-plateau is created, which can be recognized by the significant flattening of the measurement curve. This is less obvious in the area of the off-plateau. The last figure 4.3c shows that much lower drain currents I_D are reached at low temperatures and thus the transistor is better controllable in those regions. While there are large differences in behavior at temperature jumps below room temperature, these differences are much smaller above room temperature.

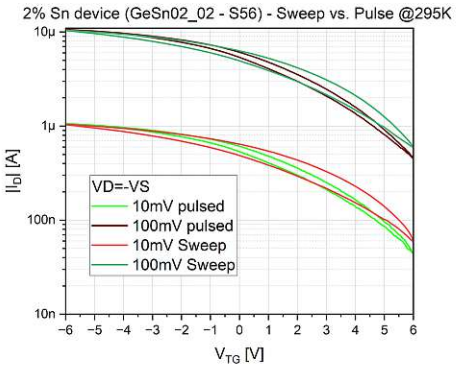
2% Sn device - GeSn02_02: As can be seen in Figure 4.4a, the sweeps are somewhat flatter for the selected structure of the 2% Sn sample compared to the 4% sample. The $GeSn02\_02$ sample had some transistors that behaved like outliers in terms of electrical behavior and had much better controllability. However, since the majority of the transistors showed a behavior like in 4.4a, this structure was chosen as a representative example. In terms of the on/off ratio, the 4% and 2% Sn devices shown behave very similarly in contrast to the shape of the trace which shows less agreement. As steps for the sweep $V_D = 1V$ was not chosen, because this voltage brought some transistors to the edge of the safe operating area. Instead a measurement with $V_D = 50mV$ was carried out instead. 4.4b allows similar conclusions as for the 4% devices. Again, the pulsed measurements achieve a lower drain current with narrower hysteresis. Likewise, the conclusio remains the same regarding the temperature measurements in 4.4c compared to 4.3c. The current density J_D shows similar ranges of values in both cases.

1% Sn device - GeSn01_02: To ensure that the devices survive the temperature measurements undamaged, 1mV, 10mV and 50mV were selected as new drain voltage steps. Compared to the previous samples, it is noticeable that the conductivity is already strongly reduced at a Sn content of 1%, as can be seen in 4.5a. However, at this GeSn ratio, the measurement curve again reaches a steeper slope, which indicates that the DUT is better controllable. In the comparison between the sweep and a pulsed measurement, several V_D steps were omitted this time, since as in 4.5b, no great differences between the two measurement methods can be determined. It can also be observed in this sample that the drain current takes on lower values with decreasing temperature. However, it is also evident in 4.5c that compared to the 4% and 2% Sn sample, a significant difference of drain current values can still be identified but not to the same extent compared to higher Sn content.

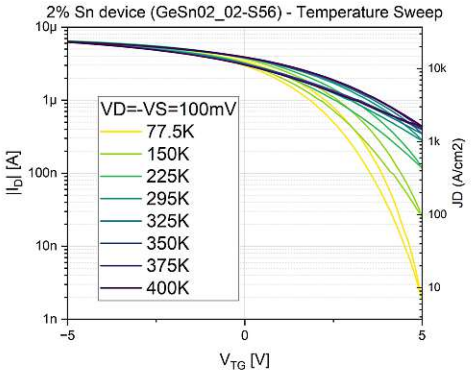
0.5% Sn device - GeSn005_02: Last but not least, we take a look at a DUT with 0.5% Sn. As far as the measuring range is concerned, the same limits were selected as for the 1% Sn device. The conductivity decreases with decreasing Sn in Ge, but the controllability is better as shown in 4.6a. The curves in 4.6b differ minimally in the width of the hysteresis. An interesting observation was made in 4.6c. At 77K, a slight increase in drain



(a) *Transfer sweep measurement with various drain voltages V_D*

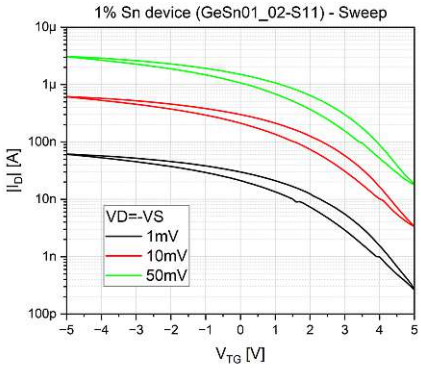


(b) *Sweep measurement vs. pulsed measurement*

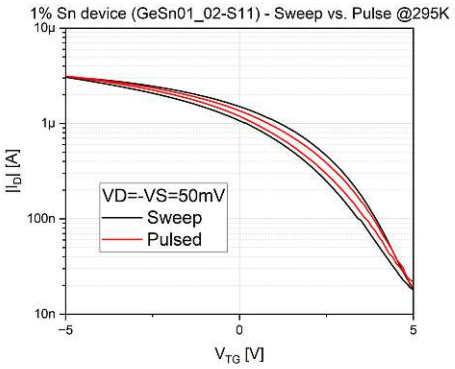


(c) *A transfer sweep measurement with a fixed drain voltage V_D over various temperatures*

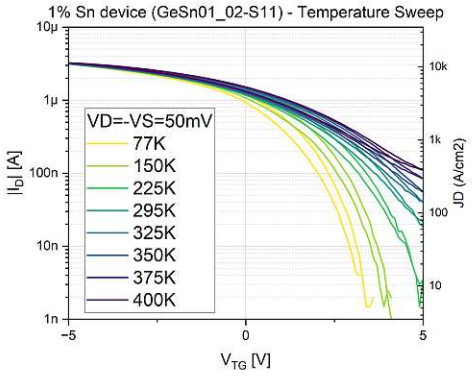
Figure 4.4: *Transfer Characteristics of a 2% Sn device with a STG*



(a) *Transfer sweep measurement with various drain voltages V_D*

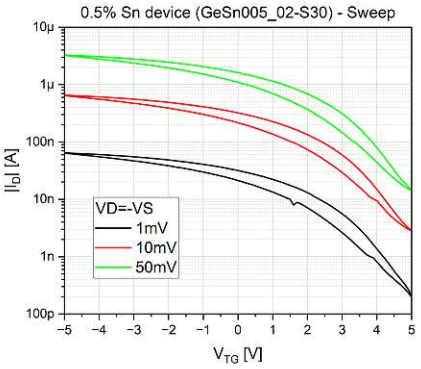


(b) *Sweep measurement vs. pulsed measurement*

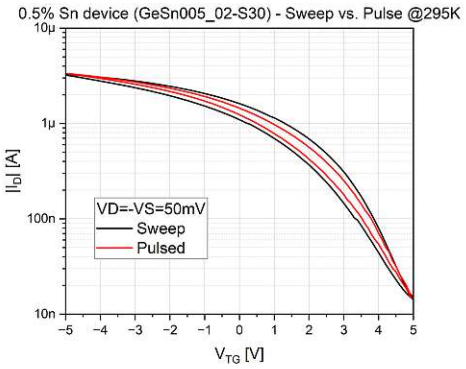


(c) *A transfer sweep measurement with a fixed drain voltage V_D over various temperatures*

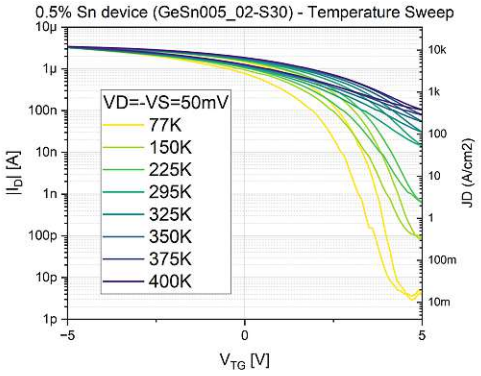
Figure 4.5: *Transfer Characteristics of a 1% Sn device with a STG*



(a) *Transfer sweep measurement with various drain voltages V_D*



(b) *Sweep measurement vs. pulsed measurement*



(c) *A transfer sweep measurement with a fixed drain voltage V_D over various temperatures*

Figure 4.6: *Transfer Characteristics of a 0.5% Sn device with a STG*

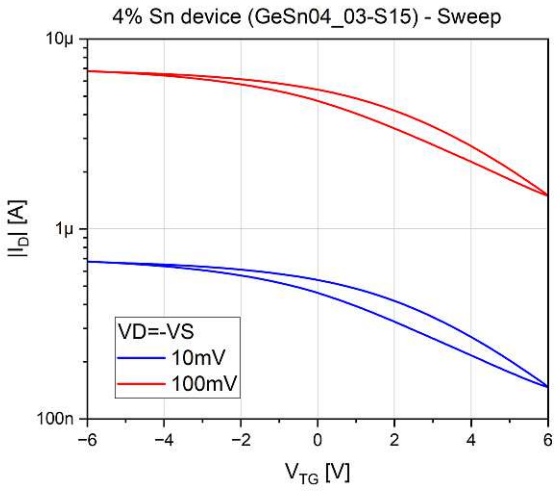


Figure 4.7: *Transfer Characteristics of a 4% Sn device with a MG*

current I_D can be observed at a top gate voltage around $4.8V$.

If one looks at the temperature sweeps again, one will notice that they show particularly good controllability at low temperatures. The reason for this is that the valence and conduction band can be controlled relative to the Fermi level by applying a voltage to the top gate electrode V_{TG} and thus changing the overlap with the Fermi-Dirac distribution in such a way that the carrier concentration is changed. As a result, the same carrier concentration is present at lower temperatures and lower V_{TG} with otherwise unchanged voltage range, since the Fermi-Dirac distribution sharpens.

4.3.2 Middle Gates

For a transistor with a middle gate (MG), the top gate electrode is placed so that it overlaps only the GeSn segment but not the junctions between Al and GeSn. This type of top gate was used in devices with 4% and 2% Sn. With a MG it can be tested how well a transistor can be controlled if the barriers at the junctions are not gated.

4% Sn device - GeSn04_03: Comparing the transfer sweep between a structure with an STG and a structure with an MG, it can be seen that the controllability and thus the slope of the measurement curve decreases only slightly with a transistor with MG. The conductivity varies of course between different structures so a direct comparison is only possible to a limited extent. However, it can also be determined that a smaller current flows through the channel compared to an STG transistor.

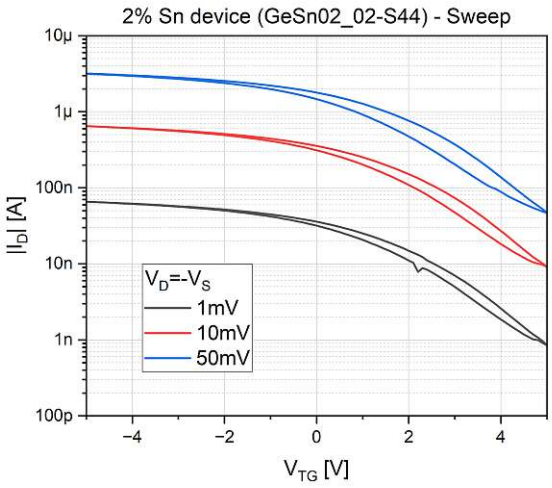


Figure 4.8: *Transfer Characteristics of a 2% Sn device with a MG*

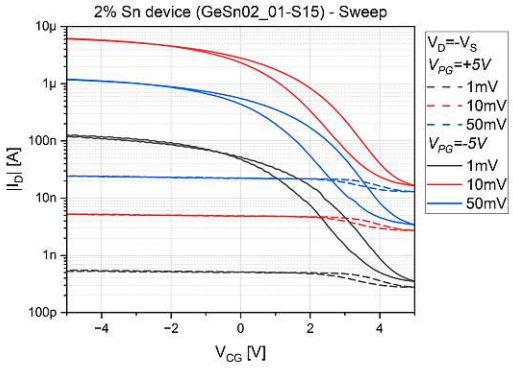
2% Sn device - GeSn02_02: Similarly, the maximum drain currents are almost halved for the 2% Sn MG device compared to a 2% Sn transitor with an STG. The extremely narrow hysteresis observed for all drain voltages V_D is also striking.

By using middle gates as top gate structure it could be shown that the transistors can already be controlled even if no gate electrode overlaps with a junction. Generally speaking, the GeSn devices are not very sensitive to STGs that have become too narrow or have not been well aligned with the junctions. Nevertheless, performance losses must be expected when using MGs compared to other top gate structures that actively stimulate the barriers. This indicates that the charge carrier modulation in the channel is of higher importance than the control of the barriers, as these act very transparently.

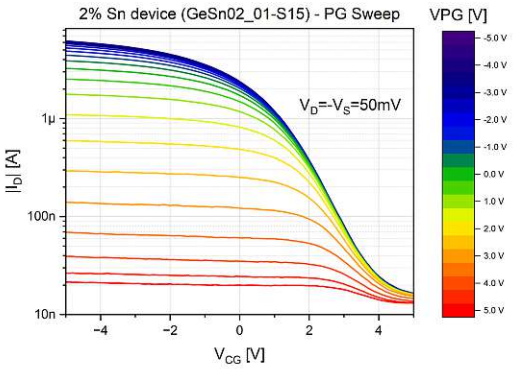
4.3.3 Triple Top Gates

With STGs and MGs we have swept over the voltage V_{TG} now a second parameter comes into play with TTGs, the voltage at the polarity gate V_{PG}. By applying a fixed voltage of $\pm 5V$ it is possible to switch between n- and p-mode and to illustrate the behavior during both operating modes by superimposing the curves. In the second figure, we fix the voltage value at the drain pad and sweep across different voltage values of V_{PG}. As before, the temperature sensitivity of the transistor is shown in the last figure.

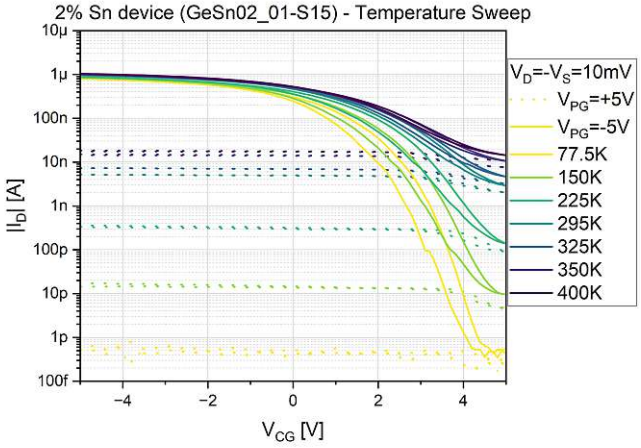
2% Sn device - GeSn02_01: 4.9a shows a transfer sweep with three different voltage levels V_D. The dashed line represents n-mode operation and the solid line represents p-mode. Here it is clear that the controllability is almost exclusively possible in p-mode, whereas there is almost no difference between on- and off-state in n-mode. What can also be observed is that a tenfold increase in V_D results in an approximate tenfold increase in I_D. 4.12b illustrates the transition from p-mode ($V_{PG} = -5V$) to n-mode ($V_{PG} = +5V$). A



(a) *Transfer sweep measurements with various drain voltages V_D and switch between n- and p-mode*



(b) *PG Sweep measurement over various V_{PG} and fixed V_D*



(c) *A transfer sweep measurement with a fixed drain voltage V_D over various temperatures and switch between n- and p-mode*

Figure 4.9: *Transfer Characteristics of a 2% Sn device with a TTG*

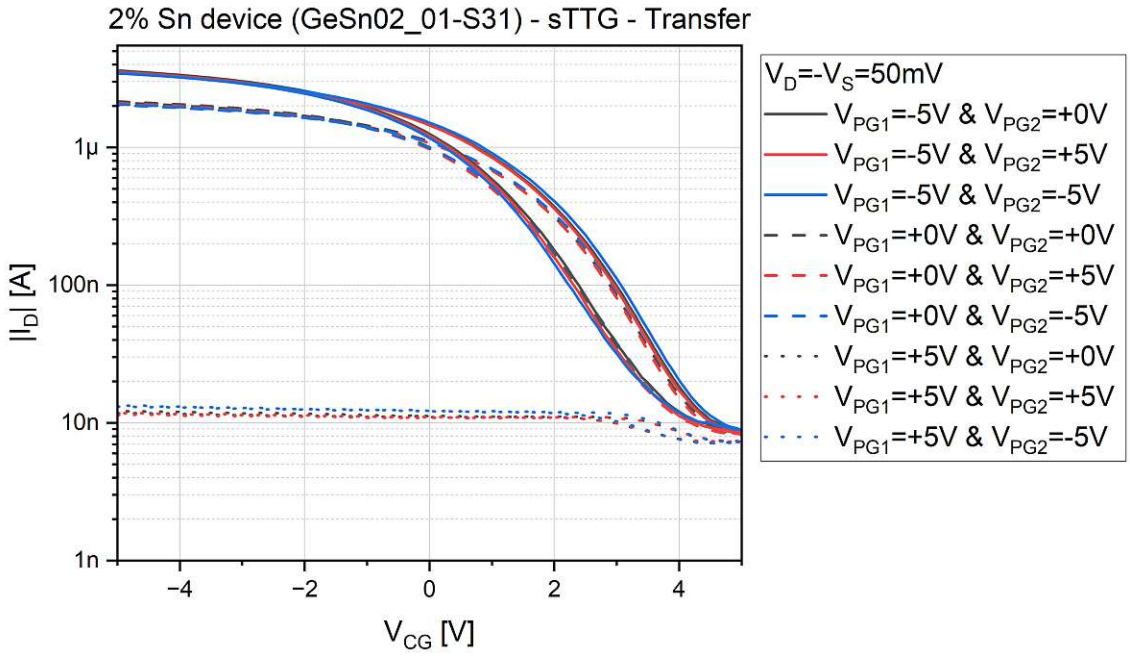


Figure 4.10: *Transfer sweep measurement over V_{CG} with various V_{PG1} and V_{PG2} of a 2% Sn device with a sTTG*

fixed voltage V_D of 50mV was applied for this measurement called PG Sweep. A flattening of the measuring curve and thus a worsening of the controllability can be recorded with a gradual increase in V_{PG}. The last figure 4.12c illustrates a sweep during different operating modes at different temperature levels. The increased on/off ratio at low temperatures also remains with TTGs. As with the PG Sweep, the dashed line stands for operation in n-mode and the solid line for operation in p-mode.

In addition to the normal TTGs, sTTGs were also applied to sample $GeSn02\_01$. By splitting the polarity gate electrode into two electrically separated electrodes, the barrier heights can be changed more specifically. As can be seen from the transfer measurement in 4.10, the device is very sensitive to changes in the first barrier and thus to the voltage V_{PG1}. In comparison, a change in the voltage value V_{PG2} seems to have little to no effect on the behavior of the transistor. This conclusion is further emphasized in 4.11 where a polarity gate sweep is performed. As with a TTG, the PG sweep can also be used to read out how the transistor behaves when the operating mode is changed. The different line types stand for the respective voltage values V_{PG2}. With this insensitive behavior to V_{PG2} the PG sweep only makes sense over V_{PG1} and therefore no further PG sweep is shown.

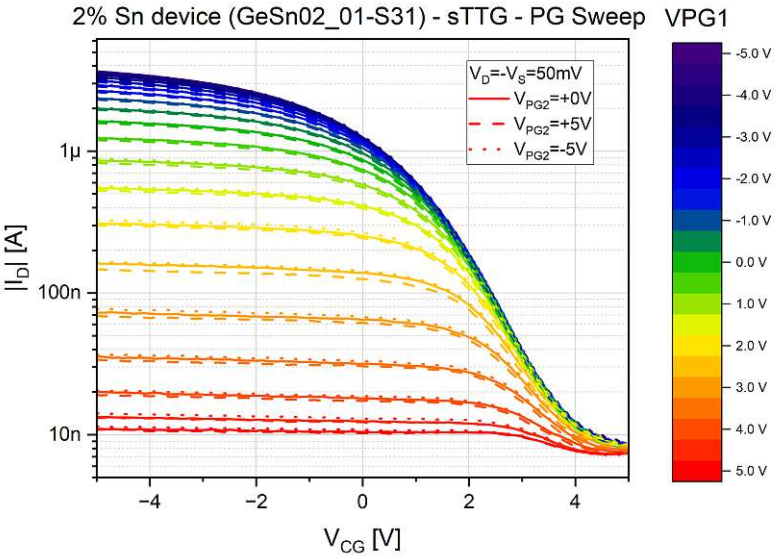
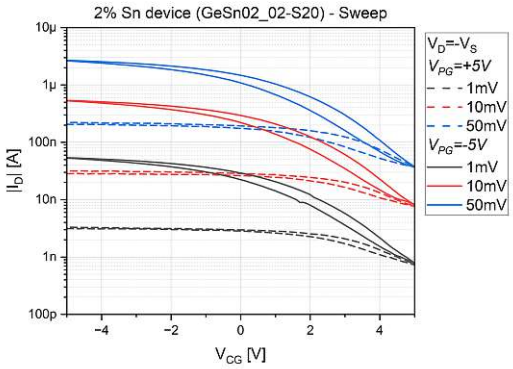
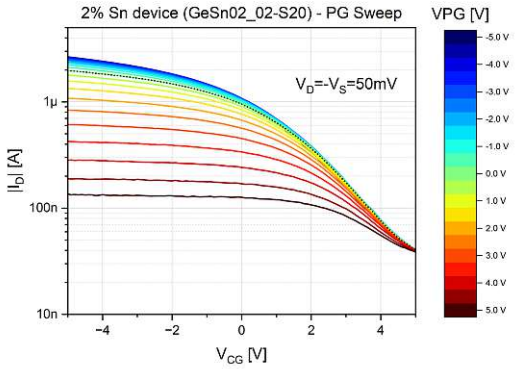


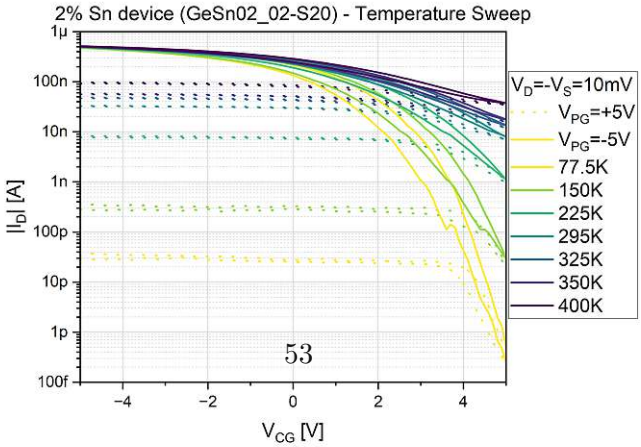
Figure 4.11: *Transfer sweep measurement over V_{CG} with various V_{PG1} and V_{PG2} of a 2% Sn device with a sTTG*



(a) *Transfer sweep measurement with various drain voltages V_D and switch between n- and p-mode*

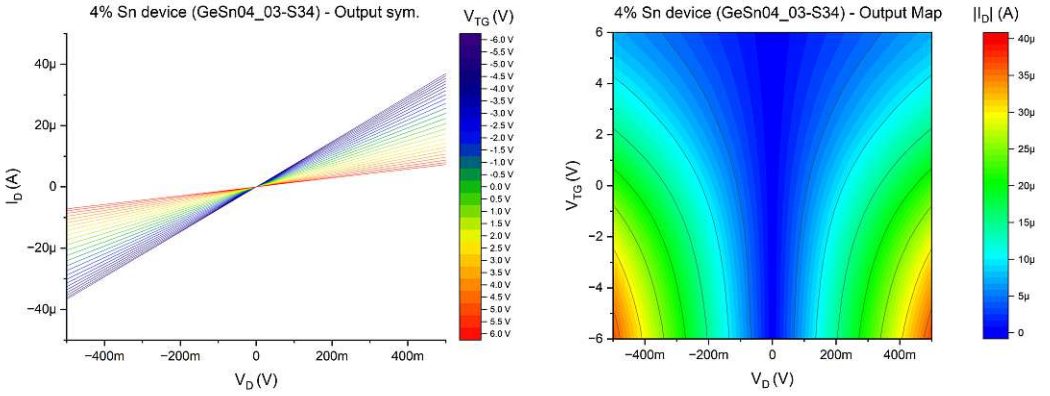


(b) *PG Sweep measurement over various V_{PG} and fixed V_D*



(c) *A transfer sweep measurement with a fixed drain voltage V_D over various temperatures and switch between n- and p-mode*

Figure 4.12: *Transfer Characteristics of a 2% Sn device with a TTG*



(a) *Output Characteristics - linear* **(b)** *Output Characteristics - 2D color map*

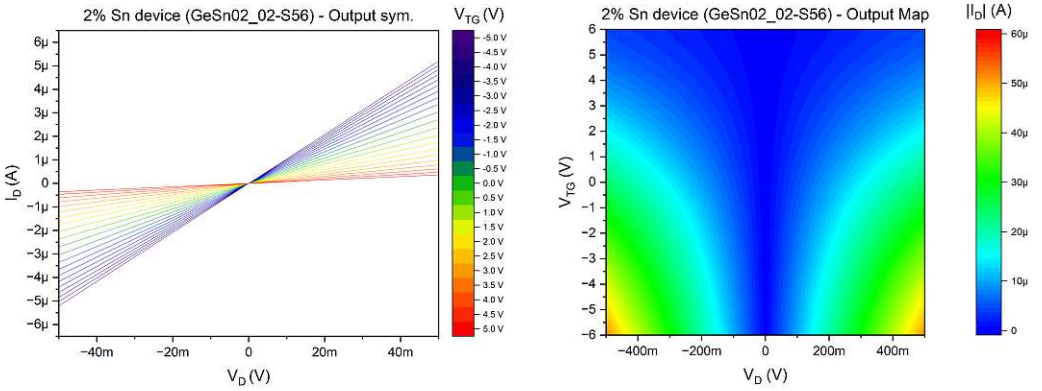
Figure 4.13: *Output Characteristics of a 4% Sn device with a STG*

2% Sn device - GeSn02_02: If you compare figure 4.12a with 4.9a, it is noticeable that the on currents are about the same, but the off currents are much higher in the second sample $GeSn02\_02$. The range of I_D in 4.12b seems to be a bit smaller than in the previously discussed DUT and thus it turns out that this transistor is a bit harder to control. The temperature measurement in 4.12c outlines that the off plateaus are less distinct compared to 4.9c.

4.4 Output Characteristics

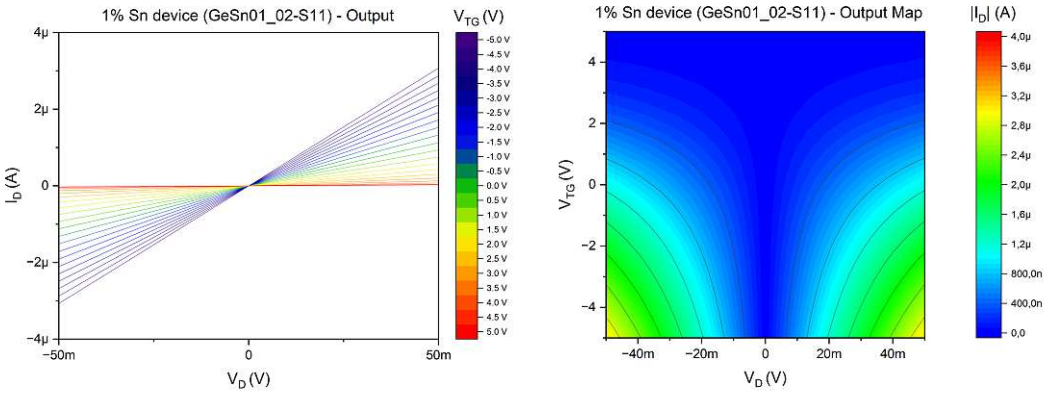
The output measurement can be used to draw conclusions about the linearity of a transistor. For this purpose, the voltage V_D is plotted on the x-axis, the current I_D on the y-axis and the applied voltage V_{TG} on the z-axis. If you want to get a better overview in which voltage range which currents occur in the channel, the display of the output color map is recommended. Here V_{TG} and I_D change the axes compared to the conventional output measurement. The color map gives information about the value ranges of the current at different voltage values. As with the description of the transfer characteristics, a comparison between the GeSn ratios also takes place here. The samples **GeSn04_03, GeSn02_02, GeSn01_02** and **GeSn005_02** were used for this purpose.

For all samples shown, it can be seen that they behave very linearly. A non-linear behavior would be present if the measurement curves shown in the graph with the linear y-axis had a curved shape. Since the transistors with 1% and 0.5% Sn are somewhat less resilient compared to the other samples and significant leakage currents could already be measured above $V_D = 50mV$, the measurement range was limited from the original $V_D = 500mV$ to $50mV$. As far as the range of V_{TG} is concerned, a range of $\pm 5V$ was chosen with exception of the 4% sample which was characterized with $\pm 6V$. Furthermore, the resulting asymmetry with respect to the x-axis is striking. If one fixes a measuring point of a color map and follows the current values along the value range of V_{TG}, one finds that



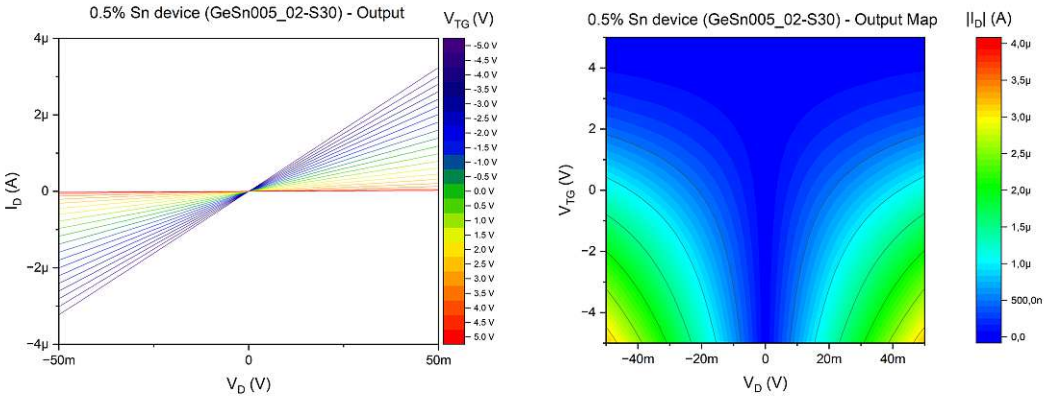
(a) *Output Characteristics - linear* **(b)** *Output Characteristics - 2D color map*

Figure 4.14: *Output Characteristics of a 2% Sn device with a STG*



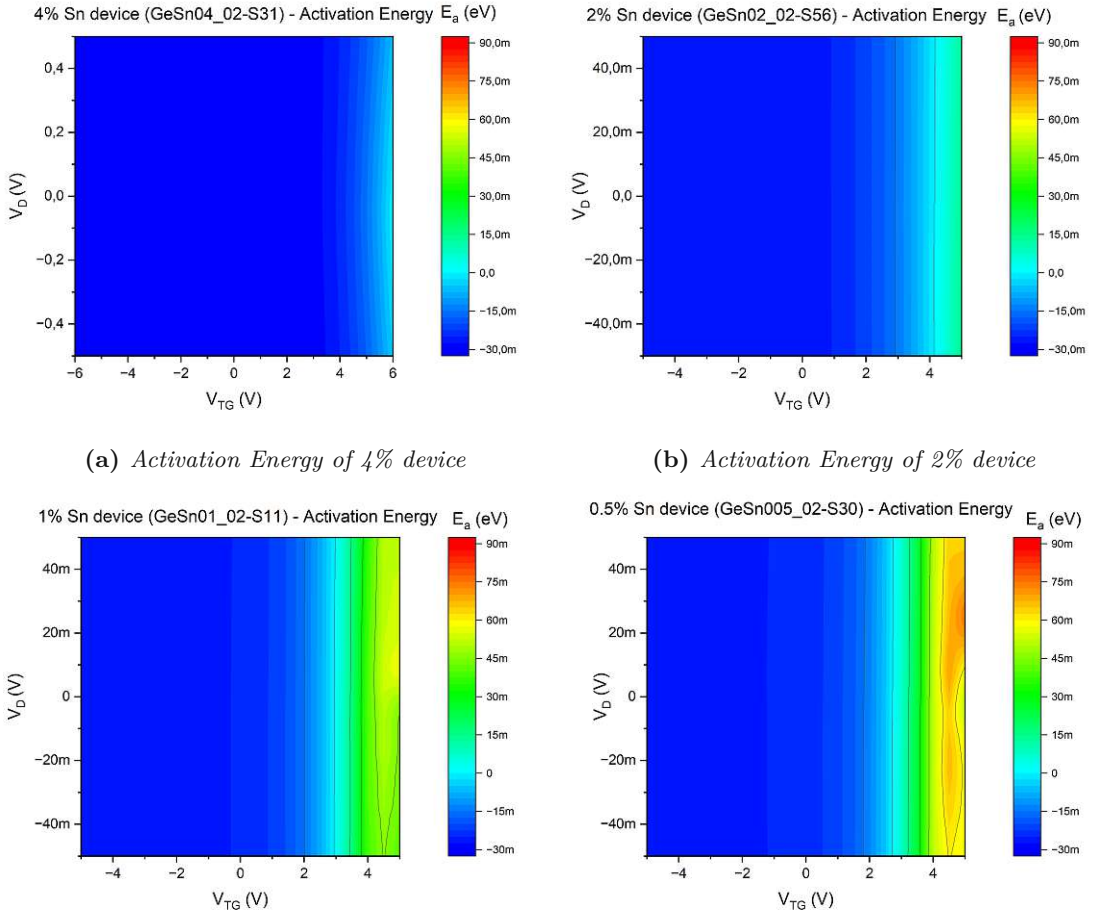
(a) *Output Characteristics - linear* **(b)** *Output Characteristics - 2D color map*

Figure 4.15: *Output Characteristics of a 1% Sn device with a STG*



(a) *Output Characteristics - linear* **(b)** *Output Characteristics - 2D color map*

Figure 4.16: *Output Characteristics of a 0.5% Sn device with a STG*



(a) *Activation Energy of 4% device*

(b) *Activation Energy of 2% device*

(c) *Activation Energy of 1% device*

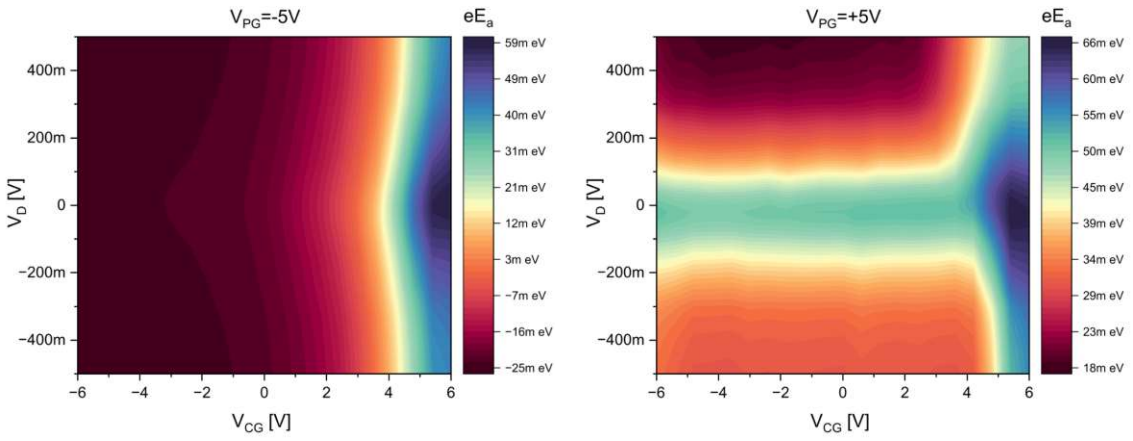
(d) *Activation Energy of 0.5% device*

Figure 4.17: *Activation Energy of a) 4% Sn b) 2% Sn c) 1% Sn d) 0.5% Sn with unified min./max. levels*

considerably larger currents I_D are reached in the range of negative values of V_{TG}. This again underlines that transistors based on GeSn show an increased hole transport while the conductivity of electrons as also indicated by the TTG investigations of the transfer characteristic is not present. Hence, the device operates like a p-type device, which is expected for hyperdoping with Sn. The eSBH measurements show a highly transparent contact for holes, which might be of high interest for p-type SBFETs with enhanced on-currents.

4.5 Activation Energy

In figure 4.17 a conclusive comparison is made with respect to the activation energy. A uniform scale in z-direction is used in the range from $-30meV$ to $90meV$ to better highlight the changing barrier with changing Sn amount. It is immediately obvious that



(a) *Activation energy of a 2% Sn TTG device with* $V_{PG} = -5V$

(b) *Activation energy of a 2% Sn TTG device with* $V_{PG} = +5V$

Figure 4.18: *Activation energy comparison of a 2% Sn device with a TTG*

the activation energy increases with decreasing Sn content. While a maximum of $-10meV$ could be achieved with the 4% Sn content. Depending on the device, an activation energy E_a of $0eV$ is reached at a voltage value V_{TG} between $3 - 4V$, indicating that a barrier is present to block the holes. Due to the symmetry with respect to the y-axis it becomes clear that E_a is almost independent of the applied voltage V_D. As a conclusion we can say the lower the Sn content, the higher the Schottky barrier that appears at the Al-GeSn interface for equilibrium. Figure 4.18 shows the activation energy of a 2% Sn device with TTG operated once in n-mode and once in p-mode. Here, a very different behavior of the operating modes clearly emerges. The barriers are much higher in n-mode, i.e. at a voltage of $V_{PG} = +5V$. From a voltage higher than $V_D = 200mV$ the activation energy decreases again in the range between $V_{CG} = -6...4V$. In p-mode, very low energy levels occur in the same range of values $V_{CG} = -6...4V$. Only from a voltage of $V_{CG} = 4V$ and upwards larger values of the activation energy can be reached. This direct comparison of the same transistor alternating in n- and p-mode clearly shows that transport via holes is preferred.

4.6 Comparison

The last section gives an overview of how the samples perform in direct comparison. Therefore, meaningful key figures like the on/off ratio, the conductivity or the maximum drain current are taken into account. In addition, a direct comparison is made between a transfer measurement, or more precisely a transfer sweep. For this purpose, all curves are plotted together for the sweep measurement in a single figure. The section is concluded with assumptions why the devices behave as shown and how this is presumably related to the introduced Sn content. The aim is to draw a clear picture of the trends caused by the decreasing Sn in the Ge in the fabricated samples.

If we take a look at the figure 4.19, it appears that the four DUT can be roughly divided

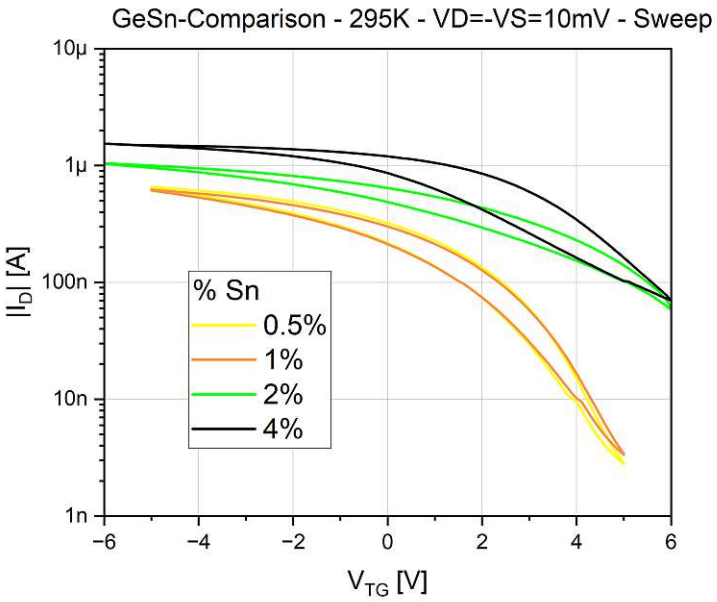


Figure 4.19: *Sweep of each representative sample in a single figure*

into two groups. The 4% and 2% Sn samples behave similarly as well as the 1% and 0.5% Sn samples. The 4% Sn sample has a maximum drain current I_D around $1.5\mu A$ while the 2% Sn device reaches a peak current around $1\mu A$. When it comes to the off-current, the 2% sample has a slightly lower off-current of $62nA$ and the 4% sample comes with an off-current of $78nA$. Comparing the 1% and 0.5% devices, both curves are almost congruent, but the 0.5% Sn sample has a slightly higher on-current around $700nA$ and a slightly lower off-current around $3nA$. The direct comparison between the DUT clearly shows that the conductivity also decreases with decreasing Sn and on the other hand that the controllability of the devices increases. Overall, it seems that the measured devices do not go into an off-state, implying that the channel is never fully depleted and no pinch-off occurs.

$$\sigma = \frac{I \cdot l}{U \cdot A} \tag{4.1}$$

Dividing the absolute value of the drain current $|I_D|$ by the cross-sectional area of a transistor results in the electrical conductivity σ, as shown in 4.20 and 4.1. Where I is the current flow through the channel, l is the length of the channel, U is the applied voltage at the drain pad, and A is the cross-sectional area through which the current flows. It is important to mention here that the GeSn04_02 sample has a larger cross-sectional area due to the 8nm thick GeSn layer, but this is negligible compared to the cross-sectional areas of other samples. The 4% Sn device has a cross-sectional area of $4.08 \cdot 10^{-11} cm^2$ and the 2% Sn device has an area of $3.76 \cdot 10^{-11} cm^2$ just to give an example of the order of magnitude of the cross-sectional areas. The conductivity is particularly high in the

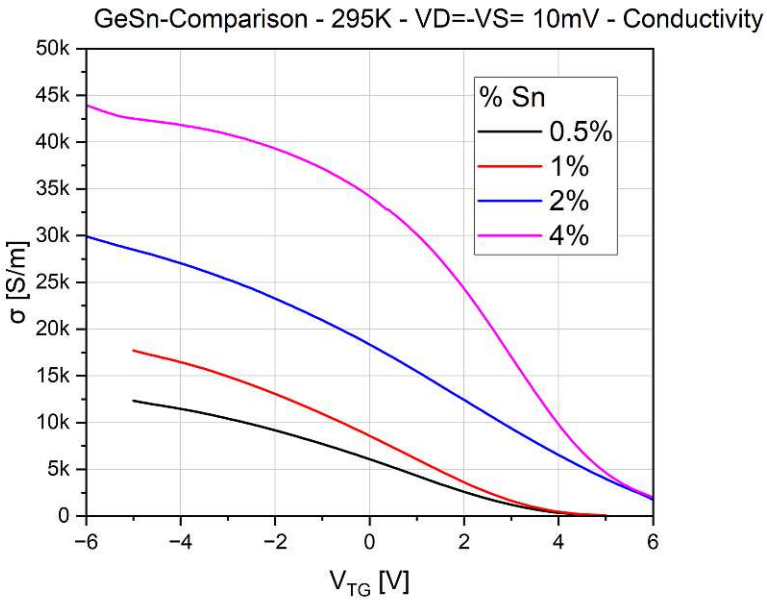
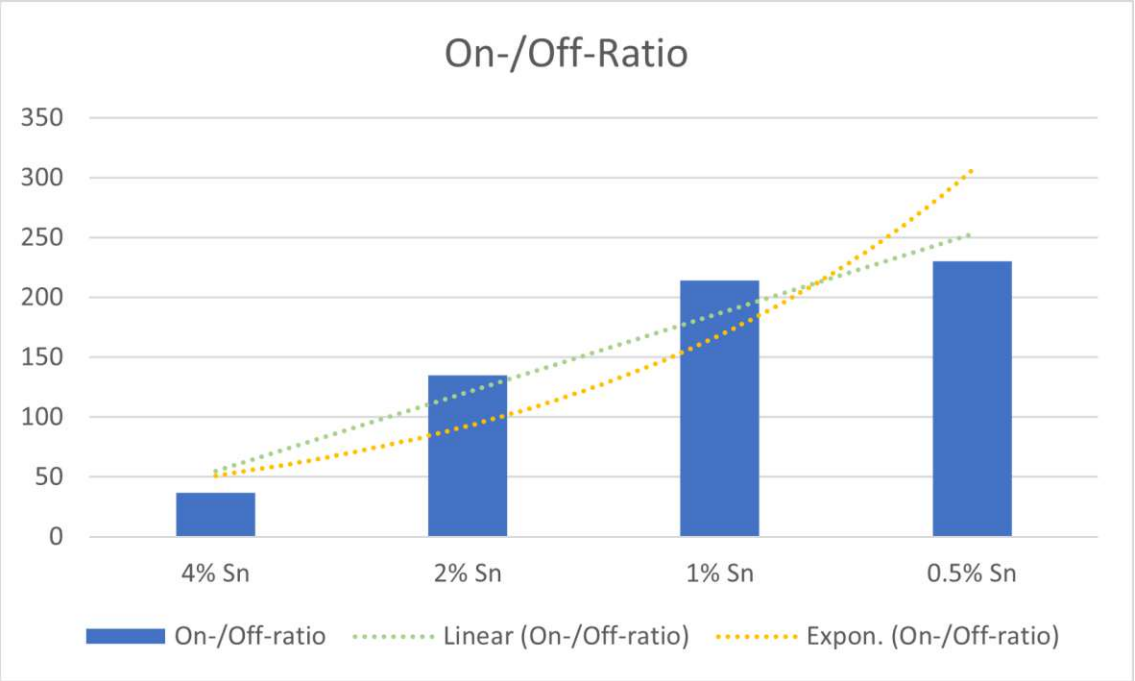


Figure 4.20: *Calculated conductivity for each representative sample in a single figure*

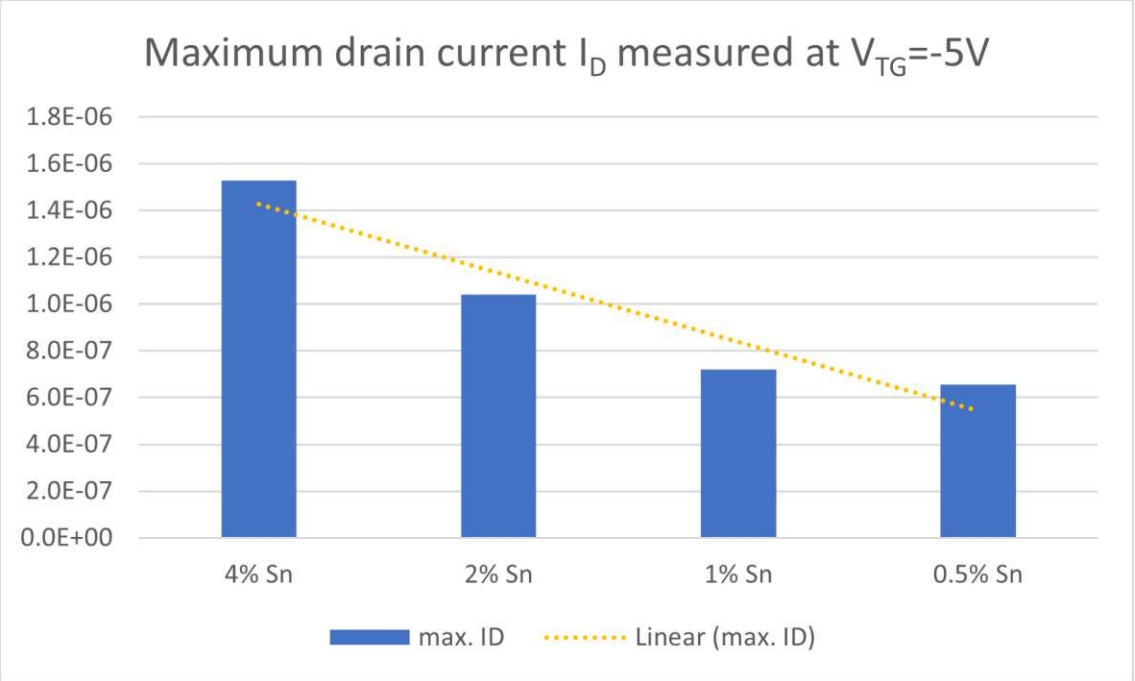
range $V_{TG} = -5V$ and levels off very quickly with positive V_{TG}. Comparing the different GeSn ratios, we can see that high conductivity can be achieved with high Sn content and conductivity decreases with low Sn content. Similar to the sweep diagram, it seems that the 1% and 0.5% Sn samples behave very similar. Pure germanium with an impurity content smaller than 10^{-9} has a conductivity of $2S/m$ at room temperature as reference.

The next bar graph 4.21a shows the on/off ratio and thus how well or how fast the transistor can change from on to off state. As the name suggests the on/off ratio is calculated by dividing the on current by the off current. In this case the values I_D at $V_{TG} = \pm 5V$ were read and evaluated. In addition, to show the trend even more clearly, linear and exponential trend lines were drawn in light green and yellow, respectively, in the bar graph. From the figure it is very clear that the samples with lower Sn content have better controllability. By adding Sn to Ge, the band gap can be effectively shifted. As the Sn content increases, the band gap is further reduced. This results in the valence and conduction band being closer to the flatter part of the Fermi-Dirac distribution in equilibrium at lower Sn and better controllability.

Bar graph 4.21b maps the maximum achievable currents flowing through the channel at a voltage $V_{TG} = -5V$. Maximum currents of around $1.5\mu A$ can still be achieved with the 4% and around $1\mu A$ for the 2% Sn devices, but only around $60 - 65\mu A$ with the 1% and 0.5% samples. This again emphasizes the original motivation for the master's thesis, namely the increased current flow inside the transistors through the addition of Sn. An



(a) *Calculated ratio between maximum and minimum drain current I_D for each representative sample*



(b) *Comparison of the highest achievable drain current I_D of each sample*

Figure 4.21: *Comparison between different GeSn ratios regarding the achieved On-/Off-ratio and the maximum drain current I_D*

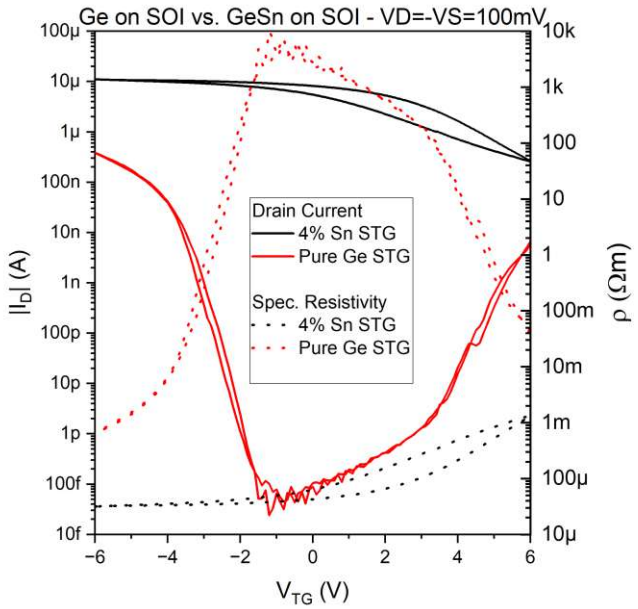


Figure 4.22: *Comparison between Ge on SOI and GeSn on SOI with 4% Sn with respect to the drain current and the specific resistivity*

initial linear prediction is indicated by the yellow dashed line. An exponential trend line was omitted because it intersected almost congruently with the linear trend line.

Finally, we should take a look at how GeSn transistors on SOI behave in relation to pure Ge on SOI. The measurement data of the sample with pure Ge was available at the institute and neither pure Ge samples nor their measurements were part of this master thesis, but since the data can be compared and at a glance one can guess what influence the introduction of Sn in Ge has, a comparison is shown in figure 4.22. The comparison is only partly representative because the current flows through cross-sectional areas of different sizes and the sample with pure Ge is only fully switched on at higher voltage ranges of V_{TG}. Therefore, as a further orientation, the specific resistivity was calculated and plotted on the right y-axis to compensate for this difference in area. The on/off plateaus of pure Ge are only clearly visible at higher and lower voltage values than shown in the figure. However, if one compares the two samples, one immediately notices the higher conductivity of the sample with GeSn at the same applied voltage $V_D = 100mV$. As far as controllability is concerned, the sample with pure Ge is unsurprisingly the winner. While with Ge on SOI the transport is possible in n- as well as in p-mode, with a GeSn transistor the transport via holes is clearly to be favored. The 4% Sn sample was chosen to compare with pure Ge because it was measured at wider voltage values of V_{TG} and higher V_D, and thus came closest to the values used in the characterization of pure Ge.

Chapter 5

Summary and Outlook

In this master thesis, the emerging Schottky barrier at the Al-GeSn junction was investigated and based on this, transistors with various top gate structures were fabricated and electrically measured. Samples with different Sn percentages like 4%, 2%, 1% and 0.5% were compared with each other and their advantages were highlighted and trends with increasing or decreasing Sn content were described. Of course, it should be mentioned that the addition of Sn in Ge changes the band gap and consequently the conductivity. Thus, the focus of the thesis is on these mentioned effects.

The basis of all devices is a SOI wafer or, in the case of the first samples, a sSOI wafer on which a layer of Si was applied, followed by the device layer with GeSn and finally another Si layer. Structures designed as SBFETs and multi-gate FET were taken as representative examples to demonstrate the effects of the Schottky barrier and the transport of holes and electrons. The resulting channel width for most devices was $700nm$ and the channel length was approximately $3\mu m$. TEM and EDX imaging of a 4% sample allowed closer inspection of the individual layers and analysis of processes after annealing. It was found that the Sn was not homogeneously distributed within Ge and that there was a tendency for the tin to settle to the top and be confined there by the aluminum oxide. However, further cuts or measurements that have already been commissioned are required for a well-founded statement.

As it turns out when comparing the results of samples with different GeSn ratios, there seems to be a compromise that has to be made when using an alloy between Ge and Sn. With increasing Sn content, the conductivity increases drastically, on the other hand, the controllability that was still present with devices with a lower Sn content decreases. The lower the Sn content, the more one approaches the original behavior of a semiconductor, which results in a lower conductivity. However, if you increase the tin, you increase the metallic properties of the alloy and higher currents can flow through the channel. What

could also be shown is that the transport of holes works well in a GeSn transistor and thus it is well suited for operation in p-mode. However, electrons have to overcome higher barriers and the resulting transistors are only conditionally n-mode capable. Depending on the area of application, this must be taken into account in the further development and investigation of other GeSn ratios.

From a Sn percentage of 6% upwards and typically at 6.55% Sn, a direct band gap occurs, which means that the GeSn alloy could also be used in the field of optoelectronics, for example in the form of lasers. In order to further improve the devices produced, development with a gate all-around approach could be carried out or, depending on the possibilities in fabrication, thinner wires and thinner oxides could be used. In addition to the improvements already mentioned, the effects of a different gate oxide material could also be investigated.

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