Three-Phase Motor-Voltage-Level Pulse Generator

MASTER THESIS

Performed for the purpose of obtaining the academic degree
Graduate Engineer (German: Diplom-Ingenieur - Abbr: Dipl.Ing.)

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Vienna, in .....   _____

Abstract

This master thesis is focused on the design and the implementation of a three-phase motor-voltage-level pulse generator used for analyzing the isolation aging status of motor windings. The thesis includes circuit development, schematic creation, PCB design as well as control software engineering. Initially, dimensioning calculations and digital simulation of the circuit are performed including the design of the power electronics circuitry and the driver and control devices. Subsequently, the software for the micro-controller is designed which includes not only the pulse pattern generation oft the motor test pulses but also the implementation of the communication protocol to a superimposed system controller (PC) via USB link. After pcb design and implementing/assembling the total hardware and software system, measurements have been performed and discussed. Key feature of the designed and implemented testing pulse generator is the generation of output testing voltages of about 750V amplitude at current pulses up to 100A per phase. The currents can be measured by an external oscilloscope based on the internal isolated current sensors or, alternatively, also by the ADCs of the internal micro controller (STM32). The pulse generator can be operated in stand-alone mode using the LCD/keyboard human interface. Alternatively, a fully control of the system can also be achieved via USB link using an external PC/laptop via python script.

Kurzfassung

Die vorliegende Arbeit befasst sich mit dem Entwurf und der Realisierung eines dreiphasigen Pulsgenerators zur Analyse des Alterungszustandes der Wicklungsisolation von elektrischen Maschinen (Elektromotoren). Die Arbeit umfasst die Schaltungsentwicklung, die Schaltplan-erstellung, das Leiterplattendesign sowie die Entwicklung der Steuerungssoftware. Zunächst werden Dimensionierungsberechnungen und digitale Simulationen der Schaltung durchgeführt, einschließlich des Entwurfs der Leistungselektronik sowie der zugehörigen Treiber- und Steuereinrichtungen. Anschließend wird die Software für den Mikrocontroller entworfen, die neben der Pulsmustergenerierung der Motortestpulse auch die Implemen-tierung des Kommunikationsprotokolls zu einer übergeordneten Systemsteuerung (PC) via USB-Anbindung beinhaltet. Nach dem Entwurf der Leiterplatte und der Implementierung/ Assemblierung des gesamten Hardware- und Softwaresystems wurden zudem Messungen durchgeführt und diskutiert. Hauptmerkmal des entworfenen und implementierten Prüfimpulsgenerators ist die Erzeugung von Ausgangsprüfspannungen mit einer Amplitude von etwa 750 V bei Stromimpulsen von bis zu 100 A pro Phase. Die Ströme können mit einem externen Oszilloskop auf Basis der internen isolierten Stromsensoren oder alternativ auch mit den ADCs des internen Mikro-controllers (STM32) gemessen werden. Das Pulsgenerator-System kann im Stand-alone-Modus händisch über die LCD/Tastatur-Bedienoberfläche betrieben werden. Alternativ kann eine vollständige Steuerung des Systems auch über eine USB-Verbindung mit einem externen PC/Laptop mittels Python-Skript erreicht werden.

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Chapter 1

Introduction

In electric vehicles, one of the main components is the inverter, which task is to control the motor. This is done by controlling the currents of the motor which have a magnitude of a few hundred amperes. Besides the high currents, the inverter also has to withstand the high voltages of the battery, which is about 400 to 800 volts. The key components of the inverter are the transistors, which have to be designed for mentioned currents and voltages. In the past IGBTs (insulated-gate bipolar transistor) were the best option for power transistors due to their price to performance ratio.

Since the past few years, a new MOSFET (Metal-Oxide-Semiconductor-Fieldeffect Transistor) technology has made its way into power electronics: The SiC (Silicium-Carbid) MOSFET. Its main advantage is its ability to switch much faster. Due to this property, however the design of the inverter circuit has to be more careful to reduce parasitic inductance. Futhermore, the greater du/dt causes a greater stress on the isolation of the motor windings. It is assumed that this increased voltage stress causes the isolation to age more quickly. This topic is going to be investigated presently by TU Wien. In order to investigate this topic, a testing unit is needed which can generate high voltage pulses onto the motors windings. Furthermore, it has to provide an interface for measuring the current during the pulse. This device is topic of this master thesis. [2] [3] [4] [5]

The pulse generator uses common 230 volts rms ac voltage as power source. Internally a high DC voltage of about 800 volts will be generated, with which large film capacitors will be charged. Three IGBT half bridges are used to discharge these capacitors into a connected motor. The motor currents are transformed into measurable voltages by a closed-loop hall sensor, which is able to handle currents of up to 100A and 200kHz. These transformed voltages can be measured either by an internal 12 bit ADC or by connected an external oscilloscope via BNC. In figure 1.1 the finished pulse generator is depicted.

Figure 1.1: Completely assembled pulse generator

Chapter 2

Schematic

In this chapter, the requirements of the system are discussed and the development of the schematics is explained.

2.1 Requirements

The pulse generators purpose is to measure the current response to a voltage pulse of predefined length on the motors windings. According to equation 2.1 the current through the motor will increase exponentially assuming the voltage is constant.

$$I_{motor}(t) = \frac{U}{R} \cdot (1 - e^{\frac{-t}{L/R}}) \tag{2.1}$$

Since the resistance of the motors is assumed to be much smaller than the inductance, an increase of the current can be approximated with a linear equation. This approximation is calculated by terminating the taylor series of equation 2.1 after the linear term, as seen in equation 2.2.

$$I_{motor,lin}(t) = I_{motor}(0) + \frac{dI_{motor}(0)}{dt} \cdot (t - 0) = \frac{U}{L} \cdot t \tag{2.2}$$

The requirements for the maximum motor current, the suggested maximum pulse time and the maximum voltage are given in equations 2.3, 2.4 and 2.5. With these equations, the suggested maximum inductance of the motor can be calculated, see equation 2.6.

$$I_{motor,max} = 100A \tag{2.3}$$

$$t_{pulse,s-max} = 1ms \tag{2.4}$$

$$U_{max} = 1kV \tag{2.5}$$

$$L_{motor,s-max} = \frac{U_{max}}{I_{motor,max}} \cdot t_{pulse,max} = 10mH \tag{2.6}$$

All requirements are summarized in table 2.1. Requirements which are suggested are just values to be guided by. The other requirements are values which are not allowed to be exceeded.

Table 2.1: Summary of requirements

Maximum high voltage	1kV
Maximum motor current	100A
Minimal current measurement bandwidth	200kHz
Suggested maximum pulse time	1ms
Suggested maximum motor inductance	10mH

2.2 High Voltage Path

This section covers the development of the high voltage path, which includes generating a high voltage as well as creating a pulse. The schematic can be find in the appendix.

2.2.1 General Description
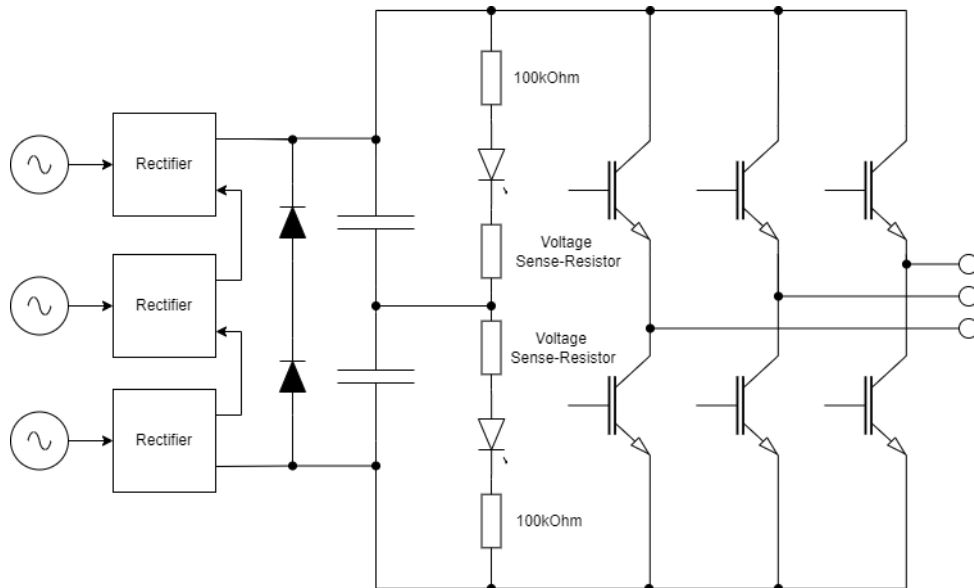
Figure 2.1: Block diagram of high voltage path circuit.

The high voltage path consists of transformers which generate the high voltage by being connected in parallel on the primary side and in series behind the rectifier on the secondary side. This voltage is used to charge intermediate circuit capacitors which act as buffer for pulse generation. A B6 bridge with IGBTs then is used to generate a voltage pulse on the motor phases.

2.2.2 Transformer

In order to generate a high DC voltage fed by mains voltage of 230 volts, transformers are required. The basic principle would be to use three standard 1:1 transformers connecting them in parallel on the primary side. On the secondary side, each transformer has its own rectifier, after which they are connected in series. This results in a peak voltage of $3 \cdot 230V \cdot \sqrt{2} = 976V$. Since the maximum voltage is required to be less than 1000 volts, using 1:1 transformers leave little margin for error. Therefore, another configuration will be used. This new configuration consists of three pairs of transformers, where each pair is connected in series on their secondary side, as depicted in figure 2.2. Transformer T1, T2 and T3 are connected in parallel over the connectors J7, J10 and J8. These transformers have a greater turns ratio compared to the other three transformers, which results in the mains voltage to be slightly decreased. Connector J1, J11 and J12 are each connected to a rectifier after which they are connected in series. This results in a peak voltage of 813V, as calculated in equation 2.7.

$$U_{HV} = 3 \cdot 230V \cdot \sqrt{2} \cdot 15V/230V \cdot 230V/18V \approx 813V \qquad (2.7)$$
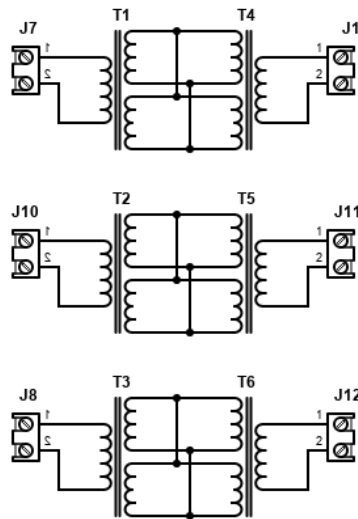
Figure 2.2: Schematic of transformers connection. The connectors names match those in the schematic attached.

Details about the selected transformers are listed in table 2.2.

According to equation 2.2, if the voltage is decreasing, the time has to increase in order to be able to supply the same current through an inductor. Since the voltage generated by the transformers configuration is smaller than the assumed 1000 volts in the requirement, see table 2.1, the pulse time has to increase. The new pulse time has to be at least $1000V/813V = 1.23$ higher. To be on the safe side the new pulse time requirement will be set according to equation 2.8.

$$t_{pulse,max} = 2ms \tag{2.8}$$

Table 2.2: Details of the selected transformers

	T1/T2/T3	T4/T5/T6
Manufacturer	RS Pro	RS Pro
Part Number	81522-P1S2	81537-P1S2
Type	Toroidal Transformer	Toroidal Transformer
Primary Voltage Rating	230Vac	230Vac
Secondary Voltage Rating	2x 15Vac	2x 18Vac
Power Rating	50VA	50VA
Operating Frequency	50Hz - 60Hz	50Hz - 60Hz
Primary Winding DC Resistance	50 Ω	50 Ω
Secondary Winding DC Resistance	2x 0.6079 Ω	2x 0.8205 Ω

2.2.3 Rectifier

One of the main properties of the rectifier diode is their current rating. In order to calculate the needed rms current, a pulse period has to be defined. This pulse period will be chosen as in equation 2.9.

$$T_{pulse} = 1s \tag{2.9}$$

Due to the assumption, that the current increases linear, when applying a voltage to the inductor, the rms current can be calculated as in equation 2.10. The corresponding values of the maximum motor current and the maximum pulse time were taken from table 2.1 considering the updated pulse time in equation 2.8.

$$I_{rect,rms} = \sqrt{\frac{1}{T_{pulse}} \cdot \int_{0s}^{t_{pulse,max}} \left(\frac{I_{motor,max}}{t_{pulse,max}} \cdot t\right)^2} = \sqrt{\frac{1}{1s} \cdot \int_{0s}^{2ms} \left(\frac{100A}{2ms} \cdot t\right)^2} \approx 2.58A \tag{2.10}$$

Details about the chosen rectifier diode can be seen in table 2.3.

Table 2.3: Details of the selected rectifier diodes

Manufacturer	On Semiconductor
Part Number	1N5408
DC Blocking Voltage	1000V
Average Rectified Forward Current	3A
Forward Voltage	1V

2.2.4 Capacitor

In previous calculations it was assumed, that the voltage is constant. This would result in a high voltage power supply with a power of $1kV \cdot 100A = 100kW$. Due to the price of such power supply and the fact, that this power only has to be available for the duration of the pulse, capacitors will be used which will store the needed energy. The charge needed for a pulse is given in equation 2.11. With this, the minimum capacitance can be derived in equation 2.12.

$$Q_{max} = \int_{0s}^{t_{pulse,max}} \frac{I_{motor,max}}{t_{pulse,max}} \cdot t = \int_{0s}^{2ms} \frac{100A}{2ms} \cdot t = 0.1As \tag{2.11}$$

$$C_{min} = \frac{Q_{max}}{U_{HV} - 6 \cdot U_{fwd,rect}} = \frac{0.1As}{813V - 6 \cdot 1V} \approx 124uF \tag{2.12}$$

Basic details about the selected capacitor are listed in table 2.4. At least four capacitors are needed (3 in parallel and 2 in series) in order to achieve the desired capacity and voltage rating.

In order to verify this results, a basic simulation of the working principle is depicted in figure 2.3a with its results in figure 2.3b. The basic principle is as follows: the capacitor is being charged up at the beginning by a constant voltage source. Subsequently the voltage source is disconnected and the inductor connects to the capacitor. After the maximum pulse time, the inductor is disconnected. The diodes represent the body diodes of the IGBT transistors. As in figure 2.3b depicted, the current through the inductor does not reach 100A within the pulse time. This can be explained due to the decreasing voltage of the capacitor. If two more capacitors are place in parallel to the existing one, the inductor does reach 100A, therefore six capacitors will be placed in the high voltage path.
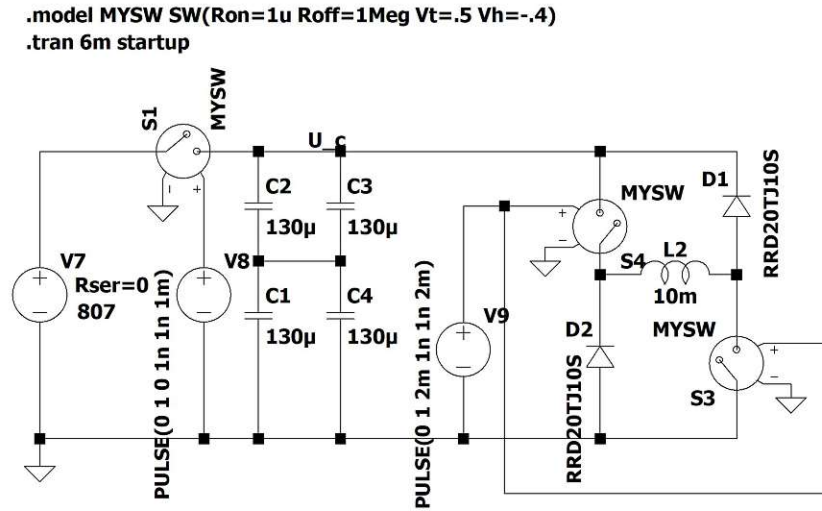
(a) Schematic the basic working principle.
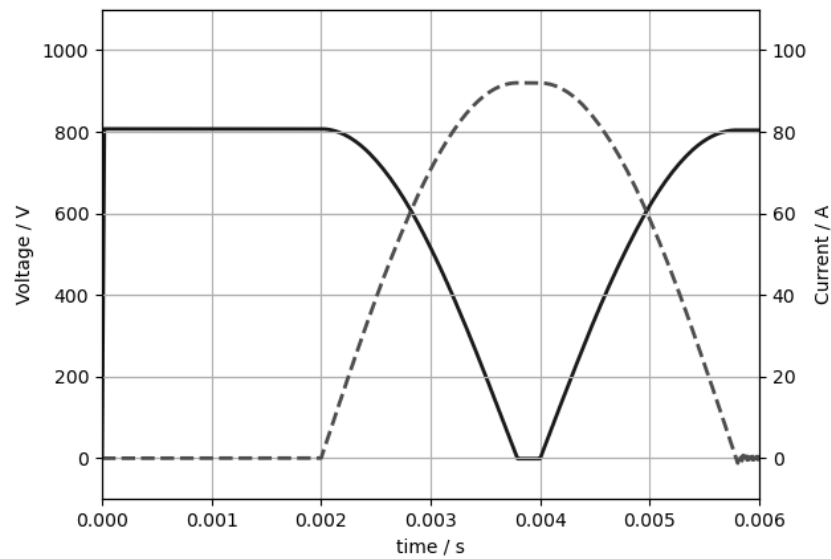
(b) Results of the basic working principle simulation.
Solid line: voltage across the capacitor
Dashed line: current through the inductor

Figure 2.3: Simulation of the basic working principle of the pulse generator.

Table 2.4: Details of the selected high voltage capacitance

Manufacturer	Kemet
Part Number	C4AQLBW6130A3NK
Capacitance	130uF
Rated DC Voltage	500V
ESL	35nH
ESR	2.4mΩ
Irms	23A

Balancing Circuit

Since capacitors are connected in series, a deviation of the capacitance can lead to an unequal voltage across upper and lower capacitors. This capacity deviation can be caused by tolerances of the production process and is dealt by balancing-resistors. These balancing-resistors are basically a voltage divider which ensures that the potential in between the capacitors is half of the total voltage across the capacitors. In order to avoid draining the capacitors more than they can be charged, the maximum current through the balancing-resistors has been set to be at most 10% of the maximum possible current from the transformers. Equations 2.13 and 2.14 calculates the minimum total resistance and power of the balancing-resistors. The value for the high voltage and the corresponding component values were taken from equation 2.7, table 2.2 and 2.3. In the schematic, 100kΩ resistors were used, realised as five 20kΩ resistors to reduce voltage stress across the resistors. Furthermore, using multiple resistors also reduces the necessary power rating for each resistor. In total a power rating for a 100kΩ resistors needs to be about 1.6 watt, according to equation 2.14. To signal a charged capacitor LEDs have been connected in series. Also a small resistor of 300Ω is added to each balancing-resistors in order to be able to sense the voltage across the capacitors. This will be explained later in detail.

$$R_{bal,min} = \frac{U_{HV} - 6 \cdot U_{D,fwd}}{\frac{S_T}{U_{ac,rms} \cdot n_{T4}/n_{T1}} \cdot 10\%} = \frac{813V - 6V}{\frac{50W}{230V \cdot 15/18} \cdot 10\%} \approx 31k\Omega \tag{2.13}$$

$$P_{bal,min} = \frac{(U_{HV} - 6 \cdot U_{D,fwd})^2}{100k\Omega} = \frac{(813V - 6V)^2}{100k\Omega} \approx 1.6W \tag{2.14}$$

Charge-Resistor

The charge-resistor limits the initial current when charging the intermediate circuit capacitors. If there is no charge-resistor the current is mostly limited by the dc resistance of the transformers and rectifier diodes. To calculate this resistance, the schematic of the transformers with their dc resistance, seen in figure 2.4a, is simplified, seen in figure 2.4b. By transforming all dc resistance to the right most side, a total dc resistance can

be calculated as in equation 2.15

$$
\begin{aligned}
R_{T,total} &= 3 \cdot \left(\left(R_{T1,p} \cdot \left(\frac{1}{n_{T1}} \right)^2 + R_{T1,s}/2 + R_{T4,s}/2 \right) \cdot n_{T4}^2 + R_{T4,p} \right) \\
&= 3 \cdot \left(\left(50\Omega \cdot \left(\frac{1}{230/15} \right)^2 + 0.679\Omega/2 + 0.8205\Omega/2 \right) \cdot (230/18)^2 + 50\Omega \right) \\
&\approx 604\Omega
\end{aligned}
\tag{2.15}
$$

A simulation of the charging and balancing behaviour of the intermediate circuit capacitors can be seen in figure 2.5 and 2.6. When dividing the steady state capacitor voltage of about 780 volts and the initial current of about 1.3 amperes, the dc resistance can be calculated, which is about 600 Ω. Therefore, the previous calculation is proved correct. However, looking at the time constant, which is 225 milliseconds according to the simulation, this does not add up. In order to have such a time constant a resistance of about $1.15k\Omega$, see equation 2.16 is necessary, which is far from the 600 Ω. In this case both is true. The real dc resistance is 600 Ω, but due to the non-continuous[1] current, the effective resistance is $1.15k\Omega$.

$$
R_{dc,eff} = \frac{\tau}{C} = \frac{225ms}{130uF \cdot 2/3} = 1.15k\Omega
\tag{2.16}
$$

The RMS charging current, according to the simulation, is about 200mA for a 2 second time frame. Since this implies a power consumption of $200mA \cdot (813V - 6V)) \approx 161W$, the power rating of the transformers is slightly exceeded. To limit the power consumption, either a charge-resistor is needed or the pulse period has to increase.

Primarily, the pulse period will be increased to 3 seconds. In order to be flexible during testing a $10k\Omega$ resistor is placed in the schematic. This resistor will only be fitted when necessary, otherwise it will be replaced by a short circuit.

$$
T_{pulse} = 3s
\tag{2.17}
$$

Balancing behaviour of the capacitors can be also seen in figure 2.5. In the worst case, it takes about 90 seconds to equalize the voltage between the upper and the lower case.

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[1]The current is not continuous due to the rectified sinus voltage
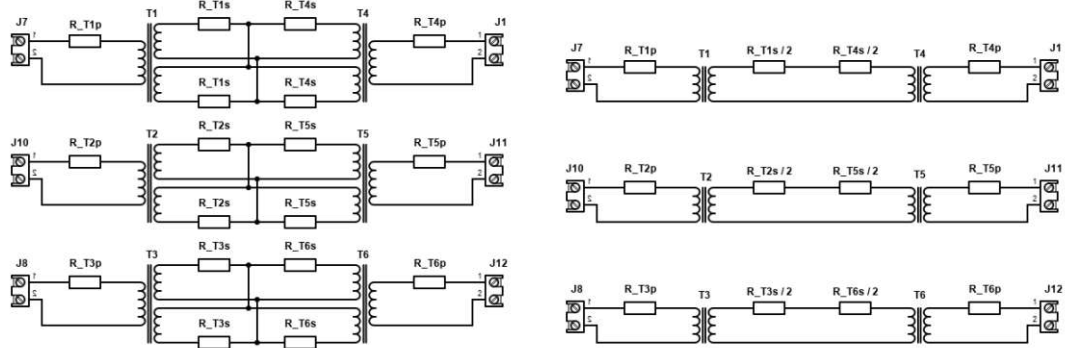
(a) DC resistance of each coil depicted as separate resistor.

(b) Simplified schematic of transformers connection with its dc resistance.

Figure 2.4: Schematic of transformers connection with its dc resistance.
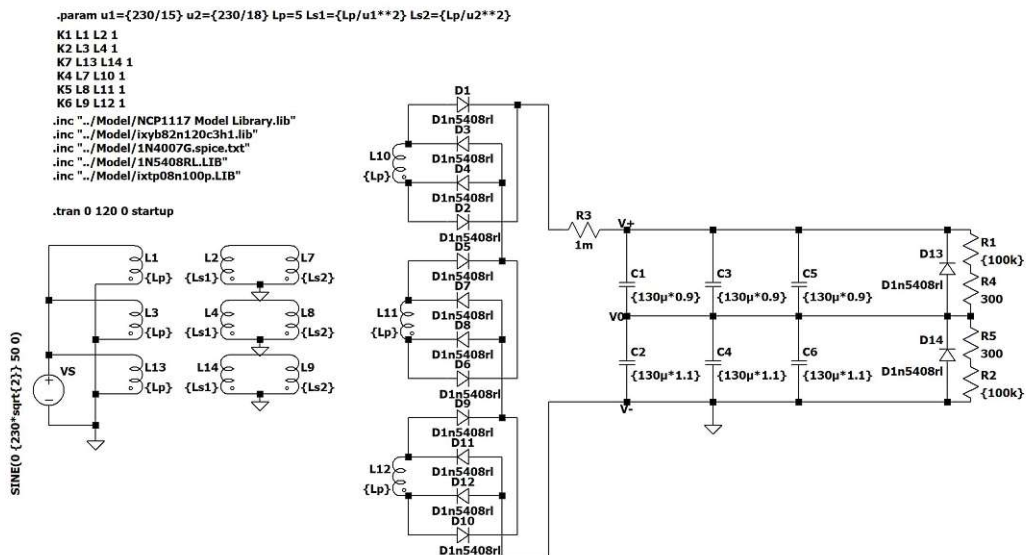
Figure 2.5: Schematic of the balancing and charging behaviour of the capacitors.
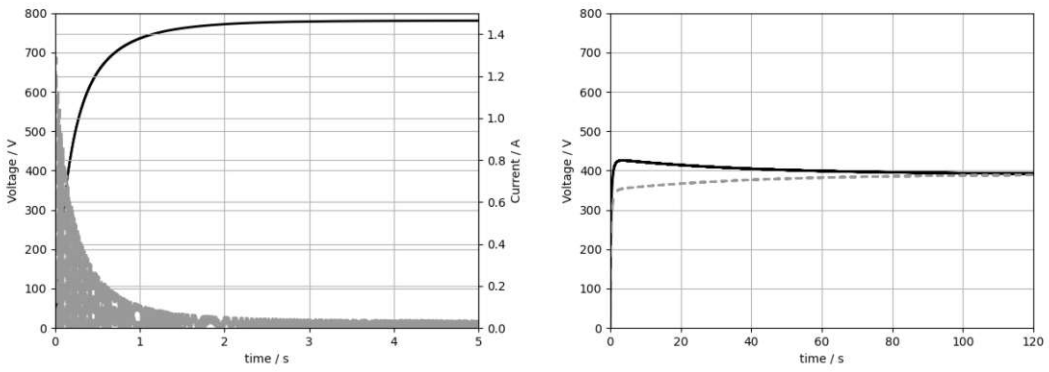
(a) Charging behaviour of the capacitance without a additional charging resistor.
Solid black line: Voltage across the capacitors over time.
Dashed grey line: current through the small charge resistor.

(b) Charging behaviour of the capacitance without a additional charging resistor.
Solid black line: voltage across the lower capacitors.
Dashed grey line: voltage across the upper capacitors.

Figure 2.6: Simulation results of the balancing and charging behaviour of the capacitors.

2.2.5 Transistor

For switching the high voltage, IGBTs [2] were selected due to their low conduction resistance compared to MOSFETs [3]. Some details of the chosen transistor are listed in table 2.5.

The six transistors, which form three half brides, have pull-down resistors connected between their gates and sources, to ensure a safe operating condition even if the gate drivers connections loosens.

Table 2.5: Details of the selected IGBT

Manufacturer	IXYS
Part Number	XYB82N120C3H1
V_{GE}	$\pm$ 20V
V_{CE}	1200V
$V_{CE,sat}$	< 3.5V
I_{C110}	82A

2.2.6 Gate Driver

Each of the transistors has its own isolated gate driver, details of which are listed in table 2.6. In the schematic "High Voltage Path" the gate driver pcbs display as a components. The main advantage of having a dedicated gate driver pcb instead of implementing everything on a single pcb is, that it can be mounted vertically. This allows to reduce the space between capacitors and transistors and therefore the parasitic inductance between them. The circuit of the gate driver pcb is displayed in the schematic "Gate Driver".

The gate driver pcb is powered by 12V. A isolated DC-DC converter generates +15V and -5V from the 12V input voltage. In order to reduce noise coupling between the different DC-DC converters, each gate driver has to filter the input voltage. Otherwise, noise coupling could lead to anomalous operation. To protect the input of any overshoot voltages, a zener-diode is placed according to the manufacturers application note.[6] Since the output voltage of the DC-DC converter increases when the current is less than 10% of its maximum current, zener-diodes are used to limit the voltage.

Table 2.6: Details of the selected Gate Driver

Manufacturer	SkyWorks
Part Number	Si8261BCC-C-IS
Insulation Rating	3.75kVrms
Output Configuration	4.0A Driver

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[2]Insulated Gate Bipolar Transistor
[3]Metal-Oxide-Semiconductor Field-Effect Transistor

2.3 Current Sensing

This section covers the development of the current sensing. The schematic can be find in the appendix.

2.3.1 General Description
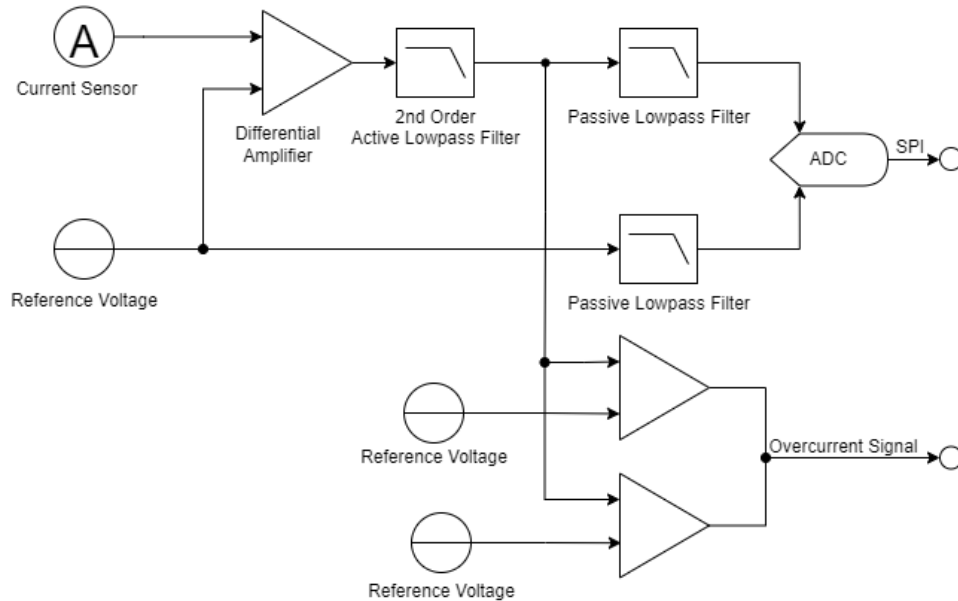
Figure 2.7: Block diagram of current sensing circuit of one phase

One of the most important features of the pulse generator is sensing the motor currents. The obtained current data is the basis of further isolation aging analysis. In order to measure a current of up to 100 amperes the LA55P-P/SP1 from LEM is selected (Table 2.7 for more information). The basic working principle is based on a closed-loop hall sensor and outputs a scaled down current. By connecting a resistor at the sensors output, a measurable bipolar voltage can be generated. This voltage can then be measured in two ways: either by directly measuring it with an oscilloscope via the BNC connectors or by reading out the corresponding ADCs. In order to be able to use ADCs, the generated bipolar voltage has to be converted into a unipolar voltage. This is due to the ADCs only being able to measure positive voltages. The conversion is done by an differential amplifier, after which a low-pass filter of second order follows. In addition to sensing, an over-current protection is implemented by comparing the output of the low-pass filter against fixed voltage thresholds via comparators. The outputs of the comparators are then combined and used to disable the gate drivers (See Chapter 2.6 for more information). The block diargam of said circuit can be seen in figure 2.7.

2.3.2 ADC Signal Chain

The resistor at the output of the current sensor, is designed in a way, that the full scale range of the ADC is ±120 amperes. This range is selected to protect the ADC

Table 2.7: Details of the selected Gate Driver

Manufacturer	LEM
Part Number	LA55P-P/SP1
Insulation Rating	2.5kVrms
Bandwidth	200kHz
Measuring Range	± 100A
Turns Ratio	1:2000

from any over-voltage created by an over-current, which may occur. Since the ADC has a reference voltage of 3 volts, the corresponding voltage at 100 amperes would be $3V/(2 \cdot 120A) \cdot 100A = 1.25V$. The necessary resistance at the output of the current sensor results in $1.25V/100A/2000 = 25\Omega$, where 2000 is the turns ratio of the current sensor.

In order to add a positive offset voltage to the sensors output voltage, a differential amplifier is used. The resistor values for this amplifier are calculated with the requirements, that the zero-current voltage shell be at 1.5V, the gain shell be -1 and the resistors value preferably be 10kΩ. A small capacitance is added in the feedback path to generate a slight low-pass filter characteristic in order to reduce anti-aliasing as well as maintaining the phase margin.

Since the selected op-amp component consists of two op-amps per package, an active low-pass filter of second order is added after the differential amplifier to further decrease anti-aliasing. A passive low-pass filter is added after the differential amplifier for the same reasons. Since the selected ADC has a maximum samplerate of 1 MSPS the maximum cut off frequency has to be at most half of that. Due to the fact, that the current sensor is only rated for currents up to 200kHz, the cut of frequency of the whole signal chain is set to be around 300kHz. To reduce noise coupling a differential ADC is selected, which measures the difference between the output of the active low-pass filter and the voltage reference of the differential amplifier. It has to be noted that this differential measurement does not result in zero-voltage when no current is flowing. The bodediagram of the ADC signal chain after the differential amplifier, the second order low-pass filter and the passive low-pass filter is depicted in figure 2.8.

2.3.3 Over-current detection

The output voltage of the second order low-pass filter is used for over-current detection. This voltage is compared against fixed voltage thresholds by two open-drain comparators. The output signals of these comparators is combined and used as active-low over-current signal. This signals turns off the gate drivers directly and is also available at a pin of the micro-controller. The voltage dividers are designed that any current greater than 96 amperes or lower than -96 amperes triggers the comparators. A simulation of the over-current detection circuit can be seen in figure 2.10 with its behaviour in figure 2.9. Every time the current exceeds about 96 amperes, the combined output of the comparators is driven low. It has to be noted, that no hysteresis is needed for the comparators, as they disable the gate drivers permanently. This is done by permanently disabling the line-driver, via a D-Flip-Flop. The D-Flip-Flop latches the low signal of the comparators until the micro-controller clears it. This is explained in chapter 2.6.
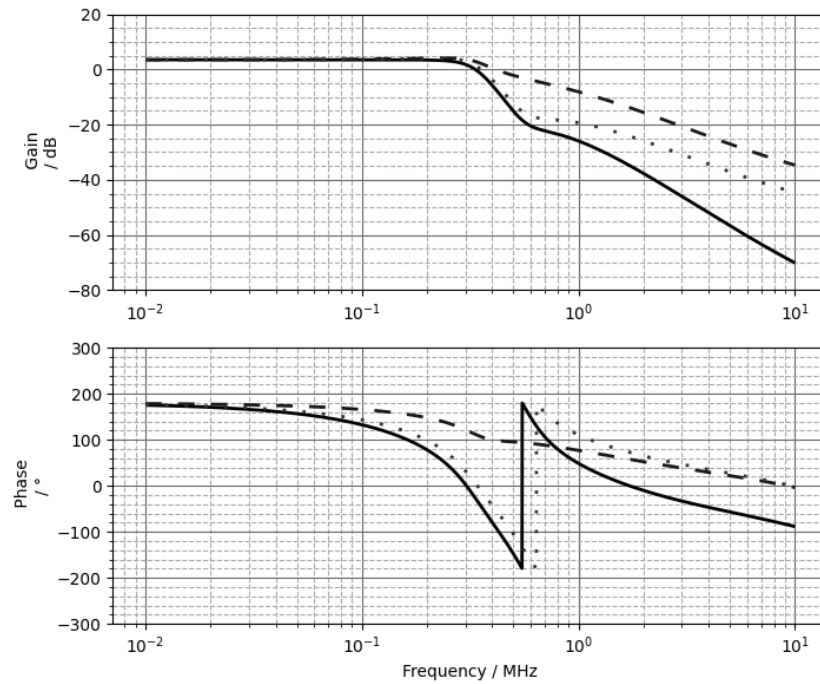
Figure 2.8: Simlulated bodediagram of the current sensing signal chain.
Dashed line: Bodediagram of output of the differential amplifier with respect to its positive input voltage
Dotted line: Bodediagram of the output of the second order low-pass filter with respect to the positive input voltage of the differential amplifier
Solid line: Bodediagram of the differential voltage after the passive low-pass filters
Maximum gain of solid line: 3.5dB
Cut-off frequency (0.5dB) of solid line: 325kHz
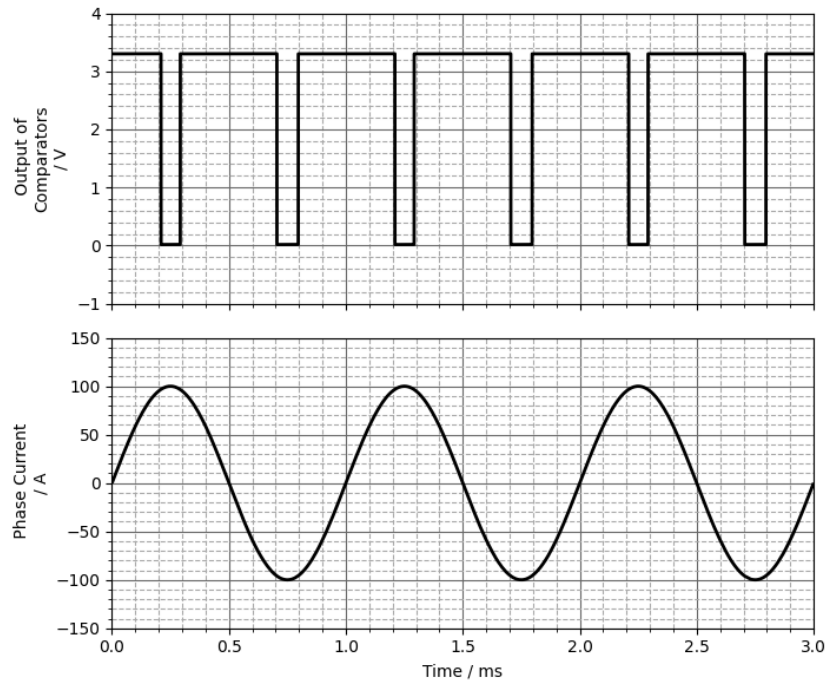
Figure 2.9: Simulated comparison between phase current and output out comparators. The low voltage levels of the comparators outputs are approximately during a phase current over 96 amperes and under -96 amperes.
Upper plot: Output voltage of the comparators
Lower plot: Phase current
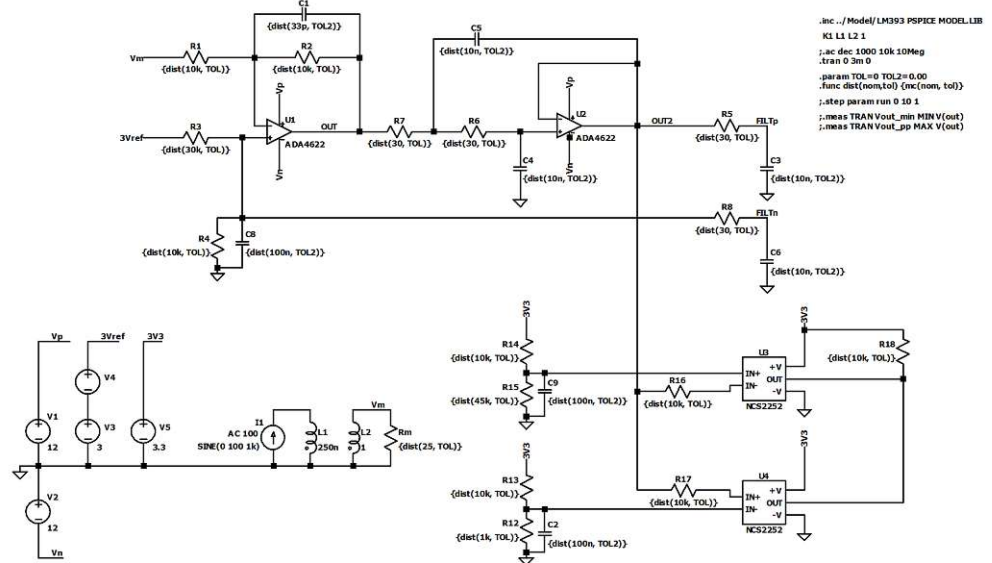
Figure 2.10: Simulation circuit created in LT Spice

2.4 Voltage Sensing

This section covers the development of the voltage sensing. The schematic can be find in the appendix.

2.4.1 General Description
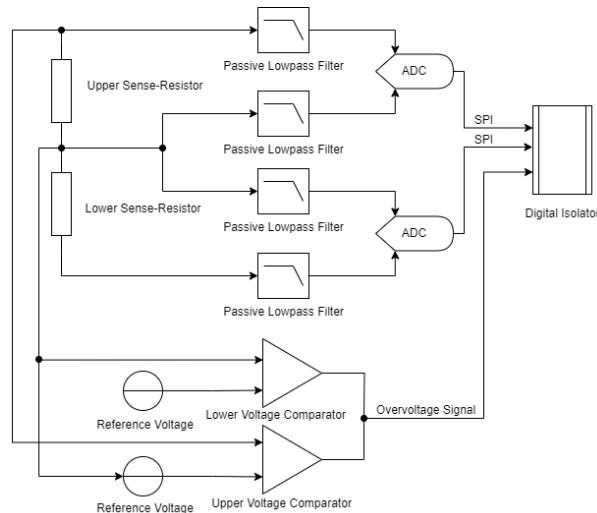
Figure 2.11: Block diagram of voltage sensing circuit

The intermediate circuit capacitors are balanced passively over parallel resistor networks. Each of these parallel resistor networks consists of five 20kΩ resistors which are connected in series. In addition to these five resistors, the networks also consists of an LED and a 300Ω sense-resistor. These sense-resistors are used to generate a voltage which can be measured by differential ADCs. These ADCs can then be read out over an SPI Bus. Additionally, a over-voltage protection is implemented by comparing the voltages across the sense-resistors against voltage thresholds via comparators. SPI signals as well as over-voltage signals connect to the micro-controller over an digital isolation chip in order to convert the voltages to the correct ground potential.

Measuring the voltage of the intermediate circuit capacitors is neither a requirement nor necessary, but is added in order to be have more information of the pulse generator state. Measuring the voltage can only be done by reading the appropriate ADCs. This measurements are currently not used, but are made available over the USB port, as all other measurements.

2.4.2 ADC Signal Chain

Due to the fact that the selected differential ADCs can only measure positive voltages, the ground potential of the voltage sensing circuit is set to the lower potential of the lower sense-resistor. The sense-resistors are designed that at the maximum allowed capacitor voltage of 500V, a voltage of 1.5V is generated on each of them (See equation 2.18). In total the sense-resistors generate a maximum voltage of 3V which is almost the reference voltage fo 3.3V of the ADCs.

$$R_{sense,v} = \frac{500V}{5 \cdot 20k\Omega} \cdot 1.5V = 300\Omega \tag{2.18}$$

In order to reduce circuit complexity, only positive voltages are designed to be measured. The main downside of being able to also sense negative voltage is the necessity of two differential amplifiers, as seen in current sensing. Since negative voltages can be avoided by placing diodes anti-parallel to the intermediate circuit capacitors, this implementation is chosen.

Between the ADCs and the sense-resistors is a passive low-pass filter with a cut-off frequency of about 350kHz. Since the maximum sampling rate of the ADCs is 1 MSPS, the cut-off frequency has to be at most half of that, 500kHz. Since the voltage measurements are not essential, the ADCs are connected in parallel over the SPI Bus. Therefore only one ADC can be read out at a time which results in lower sampling rates, when sampled alternately. To avoid short circuits on the SPI Bus, a resistor is connected in series of ADCs SPI output pins. These short circuits are a result of both chip select pins being low and should not occur under normal conditions. Someone could argue, that the cut-off frequency is still too high, since the ADCs are connected parallel on the SPI Bus and therefore the maximum sampling rate would be cut in half, if they are sampled alternately. This is correct, but the option should be kept open to sample only one ADC and still get the a bandwidth comparable to the one in current sensing. This could be used to measure the voltage of one sense-resistor during a pulse but repeating the same measurement and switching the ADC.

2.4.3 Over-voltage detection

Detection of over-voltage on the lower intermediate circuit capacitors is straight forward by comparing the voltage across the lower sense-resistor with a fixed threshold via a comparator. However, detection of the upper intermediate circuit capacitors is more complicated due to the dependence of the voltage of the lower intermediate circuit capacitors. This effect is due to the design choice of setting the ground potential to the lower potential of the lower sense-resistor. A voltage threshold is needed which changes depending on the lower sense-voltage. This is realized with an LDO whose ground pin is connected to the mid point of the sense-resistors. With a voltage divider at the output of the LDO, a over-voltage detection of the upper capacitors can also be realized with a comparator. The combined output signals of the comparators is used to disable the gate-driver during a over-voltage as well as being available to the micro-controller. It has to be noted, that no hysteresis is needed for the comparators, as they disable the gate drivers permanently. This is done by permanently disabling the line-driver, via a D-Flip-Flop. The D-Flip-Flop latches the low signal of the comparators until the micro-controller clears it. This is explained in chapter 2.6.

2.5 Power Supply

This section covers the development of the axiliary power supply. The schematic can be find in the appendix.

2.5.1 General Description
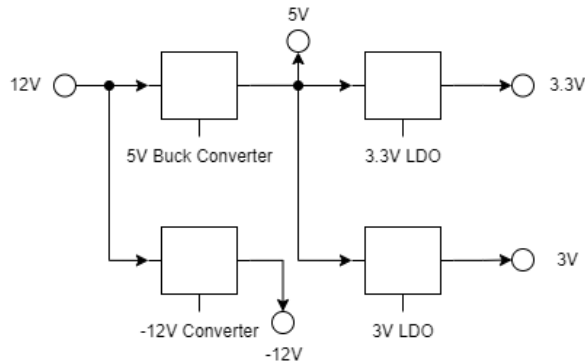
Figure 2.12: Block diagram of the power supply circuit

In order to operate the circuits, four different voltages are needed. For the current sensor a positive and negative 12V rail is necessary. The positive rail is generated by an external 12V power supply which is connected to the main grid. From this 12V input voltage all other voltages are generated. To create a negative 12V rail the MC33063AD from Texas Instruments is used. The same component is used to create the 5V rail by altering its circuit configuration. Other voltages, such as 3.3V and 3V source are generated by Low-Dropout Regulators (LDOs). In figure 2.12 the explained topology of the power supplies can be seen.

2.5.2 -12V Power Supply
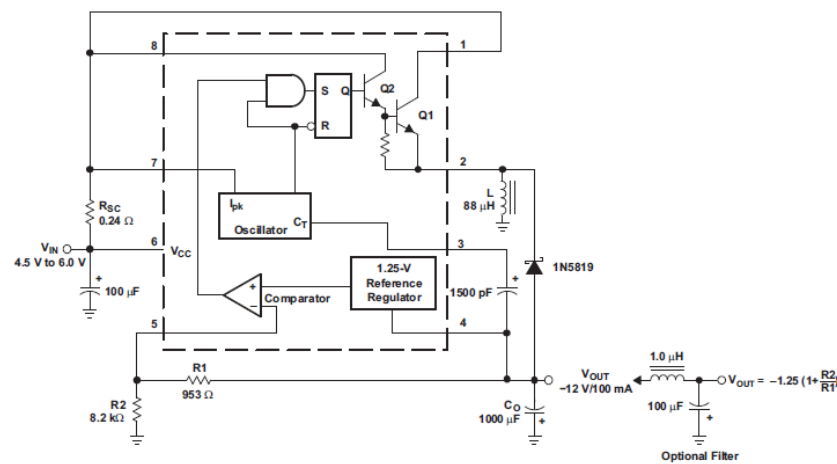
Figure 2.13: Inverting circuit topology of the MC33063AD [1]

The negative 12 Volt rail is mainly used by the current sensing circuit. This includes 3 phase current sensors, which draw a maximum of 180mA altogether according to the

datasheet and 3 operation amplifiers. The current consumption of the operation amplifiers will be neglected since they only drive high impedance loads, such as the input of the ADCs. To add safety margin, the maximum needed current will assumed to be 300mA.

Table 2.8: -12V power supply parameters

Name	Value	Comment
V_sat	1 V	Saturation voltage of Darlington Transistor Q1 & Q2
V_F	1 V	Forward voltage of the diode
V_in	12 V	Minimum Inputvoltage
V_out	-12 V	Desired Outputvoltage
I_out	0.3 A	Maximum Outputcurrent
f_min	100 kHz	Minimum switching frequency
V_ripple	5% of V_out = 0.6 V	Maximum Outputvoltage Ripple

With the parameters specified in table 2.8 and the formulas in the datasheet [1], the component values can be calculated. The value of the inductor is much larger than calculated, since this increased the precision of the output voltage in simulations.

2.5.3 5V Power Supply
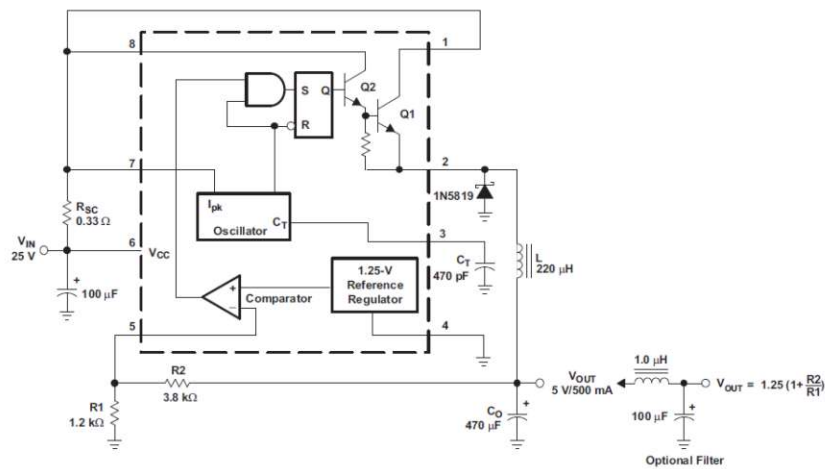
Figure 2.14: Step down circuit topology of the MC33063AD [1]

The 5V rails is only needed by a few components, such as D-flip-flop, line driver and the operation amplifiers of the temperature sensors. However, the maximum current needed was set to 500mA, although much less wil be expected to be necessary.

With the parameters specified in table 2.9 and the formulas in the datasheet [1], the component values can be calculated. The value of the inductor is much larger than calculated, since this increased the precision of the output voltage in simulations.

Table 2.9: 5V power supply parameters

Name	Value	Comment
V_sat	1 V	Saturation voltage of Darlington Transistor Q1 & Q2
V_F	1 V	Forward voltage of the diode
V_in	12 V	Minimum Inputvoltage
V_out	5 V	Desired Outputvoltage
I_out	0.5 A	Maximum Outputcurrent
f_min	100 kHz	Minimum switching frequency
V_ripple	5% of V_out = 0.25 V	Maximum Outputvoltage Ripple

2.6 Digital Peripherals

This section covers the development of the digital peripherals. The schematic can be find in the appendix.

2.6.1 General Description
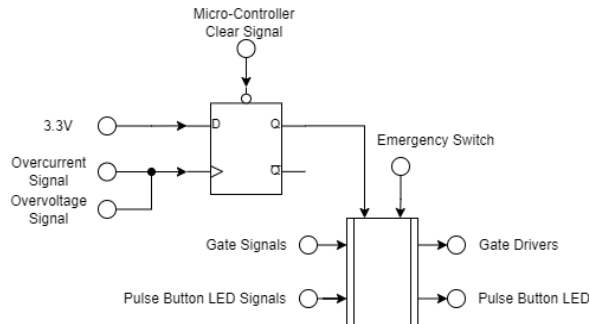
Figure 2.15: Block diagram of the gate shutdown circuit

The controller which is used to operate the circuit is a NUCLEO-F767ZI. The gate driver signals coming from the micro-controller are connected to a line driver. The purpose of the line drivers is to translate the 3.3V signal to a 5V signal. It is also necessary in order to supply enough current to the gate drivers inputs, since the microcontroller may not be able to do so. To provide a certain amount of safety features, the line driver will be disabled when the emergency switch is pressed or over-current or over-voltage faults are present. Since the over-current / over-voltage signals do not latch, a D-flip-flop is used to create a latching signal. The D-flip-flop has to be cleared by the microcontroller in order to continue operation. A block diagram of the D-flip-flop and the line driver can be seen in figure 2.15

The second safety feature is the HV shutdown circuit. It is triggered either by the micro-controller, by the HV switch or by the emergency switch. This circuit basically consists of three in series connected switches which cut off the power supply of the relais. The relais in return disconnects the transformers from the main grid.

Besides the safety features, further digital peripherals are eeproms for saving calibration data and temperature sensors. Currently only two of four temperature sensors are connected, which are used to monitor the cooling plates temperature to which the transistors are connected, as well as the temperature of the housing.

For the human interface a latching switch is used which controlls the relais of the transformers, called the HV switch. By pressing it, the transformers are connected or disconnected from the main grid which in return results in no high voltage to be generated. Furthermore, an encoder, a TFT display as well as a push-button are available. Detailed explanation of their function can be find in the appendix.

Chapter 3

Printed Circuit Board (PCB)

In this chapter, the design of the PCBs is discussed.

The total pulse generator system consists of seven PCBs. One main PCB and six gate driver PCBs. Since the gate driver has to be as close to the transistor as possible, they are mounted vertically onto the main PCB. This minimizes the distance between transistor and gate driver and the distance between transistor and capacitor. With these reduced distances a reduction of the parasitic inductance is to be expected.

3.1 Gate Driver PCB

In figure 3.1 you can see the top and bottom of the gate driver PCB is shown, which consists of four layers. During the design process, special attention has to be taken on clearances and creepage distances. The difference between the two is, that clearances relate to trough-air-distances and creepage distances relate to on-surface-distances. The low-voltage side and the high-voltage side are separated by a 5.5mm clearance. Since the pins of the gate driver component are too close to achieve a such clearance, a small cut-out is placed underneath it to at least increase creepage distance.

The resistors between the gate driver and the gate are a special resistors which are designed for pulse currents.

3.2 Main PCB

In figure 3.2 and 3.3 the main PCB is depicted. On the lower left of the top side (orange area) the input filter of the 12V input voltage as well as the 5V and 3.3V power supply are located. Directly beside them is the display connector. It should have been possible to connect the display directly onto the PCB for testing purposes, unfortunately, the pin-out of the footprint is wrong. The onboard controls, such as the encoder and the pulse button underneath the display are also there just for testing purposes. Beside the display is the micro-controller, above which are the digital peripherals, such as the temperature sensors, the EEPROM, the D-flip-flop and the line driver. The black marked area above the micro-controller, which contains the current sensing circuit, is powered the 12V rail and the -12V and 3V rail which are located in the red area.

The high-voltage path in the upper left part of figure 3.2 as well as the high voltage sensing had to be routed with a clearance of 6mm to the low-voltage part. In order
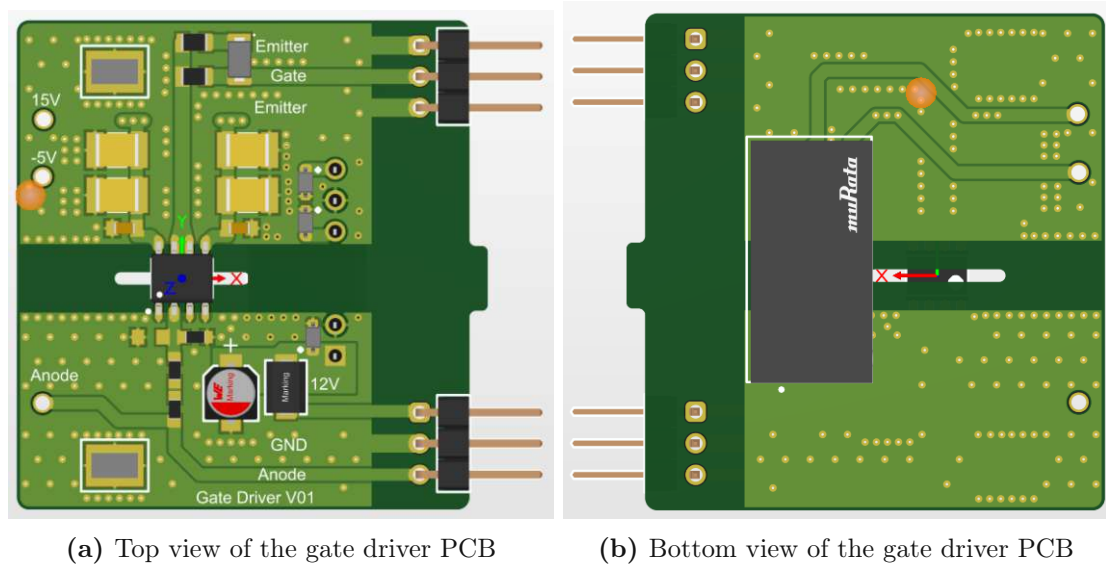
(a) Top view of the gate driver PCB   **(b)** Bottom view of the gate driver PCB

Figure 3.1: View of the gate driver PCB

to maximize the cross section of the traces carrying the load current, these traces are routed parallel on multiple layers. Capacitors and gate drivers are placed as close to the transistors as possible. Special attention is also needed for grounding. The border of the low-voltage part to the high-voltage part, is stitched with vias to reduced coupling.

Figure 3.2: Top view of the main PCB.
Orange area: Input Filter, 5V & 3.3V power supply
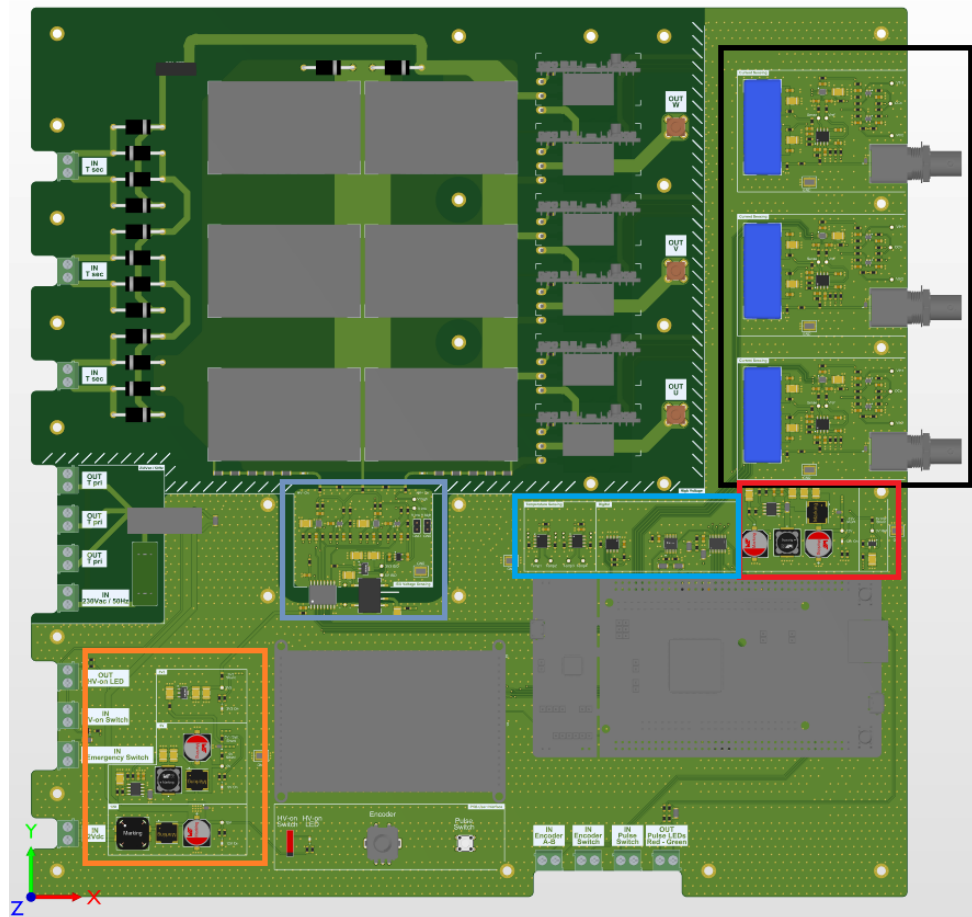Grey area: High voltage sensing
Blue area: Digital peripherals (Temperature sensors, EEPROM, line driver
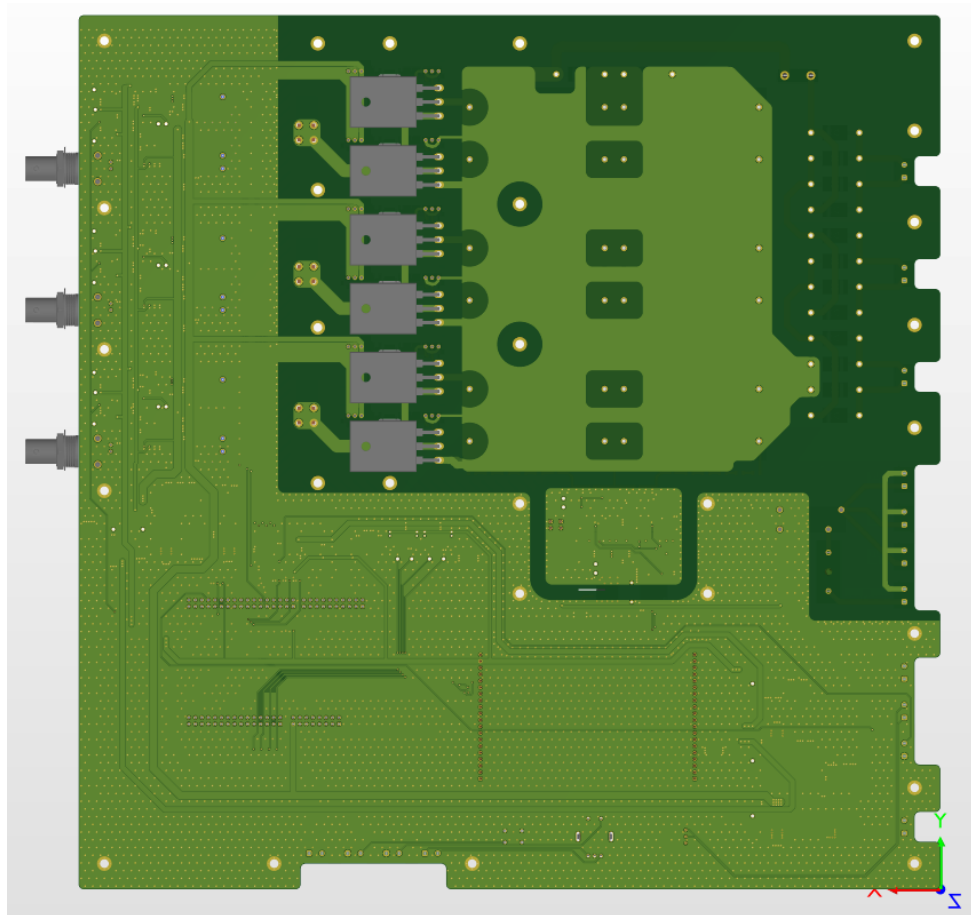Red area: -12V & 3V power supply
Black area: Current sensing

Figure 3.3: Bottom View of the main PCB.

Chapter 4

Micro-controller

In this chapter, the development of the software and peripheral configuration is discussed.

The software used for programming the Nucelo-F767ZI is Stm32CubeIDE version 1.12 from ST. With this software it is possible to easily configure the peripherals of the micro-controller as well as writing the software.

4.1   Peripheral Configuration

For each current sensing ADC a dedicated SPI interface is used. Their clock speed is configured to be 12MHz with a data length of 16 Bit, despite their maximum specified clock speed of 16MHz. The reason for that is the combination of system clock speed and available clock dividers, which do not make it possible to create a 16MHz clock speed. A possible solution is to change the system clock. Since this problem was discovered to late during the software development, a change of the system clock would have meant also adapting every other peripheral, including all buses and timers. Analysis of the performance of these ADCs will show that the lack of samples is not the major problem, but the lack of resolution. This will be explained in the next chapter. So the clock speed is chosen to stay at 12MHz.

The ADCs used for voltage sensing are of the same type as for the current sensing but share one SPI interface with a clock speed of 750kHz and a data length of 16Bit. Since voltage is not needed to be sampled at high frequency, using only one SPI interface reduces the traces to be routed. Furthermore, a reduction in clock speed compared to the current sensing ADCs can therefore be done. This reduction is necessary due to signal distortion on higher clock speeds. To increase the clock speed, more careful routing of the SPI bus traces has to be done.

The display also uses a dedicated SPI interface with 1 MHz clock speed and 8 Bit data length. To communicate with the external EEPROM an I2C interface is used with a clock speed of 100 kHz.

The signals for controlling the gate-drivers are originally intended to be software generated pulses[1] This results in us delays between the different gate-driver signals due to the sequentially executed code. Therefore the transistors would not switch synchronously, which affects the measurements. To resolve this problem, the signals have to be hardware generated. This is done by using timers, which can directly control output-pins. Since the output-pins of the timers are fixed and are not the same as the originally intended

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[1]The software controls the output-pins directly

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output-pins, the traces have to be rerouted. This is done by using an external PCB which connected onto the micro-controllers connectors. The original pins are configured as inputs, in order to not have to disconnect them from the traces. The rerouting of the signal, can be seen in figure 4.1
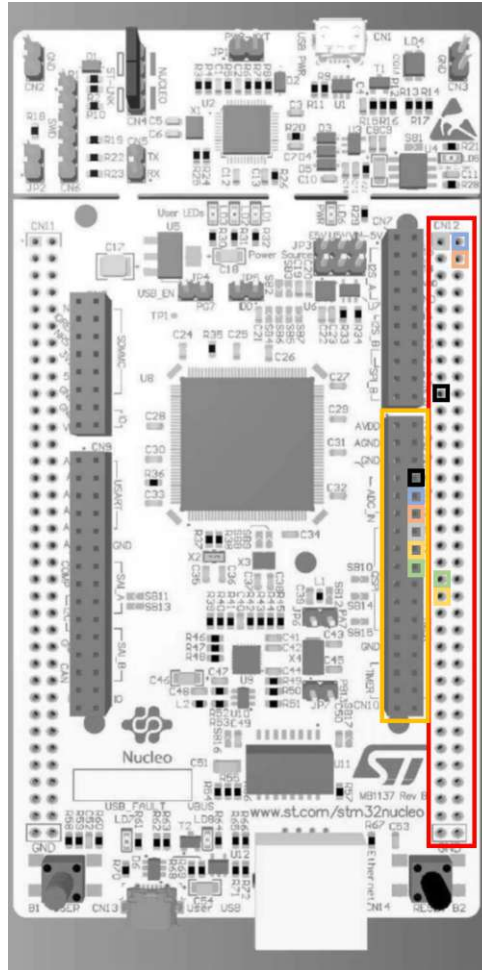
Figure 4.1: Rerouting of gate signals on the micro-controller.
CN10 is surrounded by a orange rectangle and CN12 by a red rectangle in the picture.
CN10 - 10 rerouted to CN12 - 19 (Black rectangle)
CN10 - 12 rerouted to CN12 - 2 (Light blue rectangle)
CN10 - 14 reconnected to CN12 - 4 (Light red rectangle)
CN10 - 16 reconnected to CN12 - 1 (Grey rectangle)
CN10 - 18 reconnected to CN12 - 43 (Yellow rectangle)
CN10 - 20 reconnected to CN12 - 41 (Green rectangle)

For hardware-based signal generation two timers are used in PWM One-Pulse-Mode. Timer 3 of the micro-controller controlls the signals of the phase u and v. The signals of phase w are controlled by timer 4. Timer 3 is triggered by software and timer 4 is configured to be triggered by the start of timer 3. This makes it possible at generate all PWM signals at the same time.

4.2 Software

The basic working principle can be seen in figure 4.2. On power-up, the micro-controllers first starts to initialize all internal and external peripherals, as well as initializing variables. After that, it enters a state-machine which it will never exit. This state-machine consists of three states. In Idle-State the serial communication takes place, all kind of parameters are observed and it is possible to use the human interface controls. In Pulse-Start-State the peripherals and software states are prepared to generate a pulse, after which a pulse is generated. In Pulse-Wait-State it is observed whether the pulse is already over. This is intentionally not done in Idle-State since the communication of the current-sensing ADCs should not be interrupted by any other code. However, safety features such as over-current and over-voltage detection are still working, since they are hardware based.
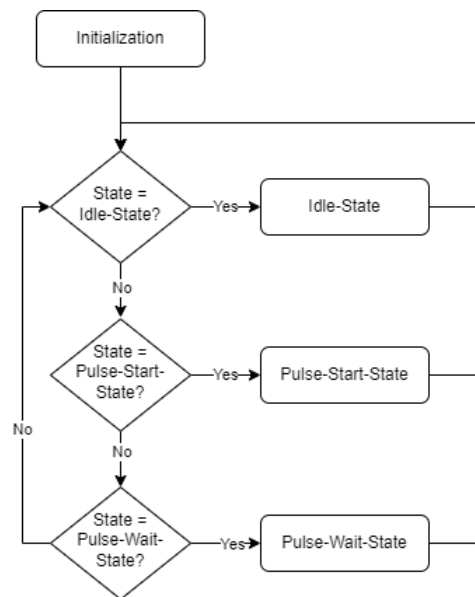
Figure 4.2: General flow diagram of the software.

A detailed view of the initialization process can be seen in figure 4.3. After initializing the micro-controllers peripherals, the pulse-button LED is set to green to indicate the start of the micro-controller. After that, variables and external peripherals are initialized as well as calibrated. The sample buffer will be filled with test data in order to be able to check the data transmission over UART before the first measurement. When the initialization process is over, the pulse-button led will be set to red.
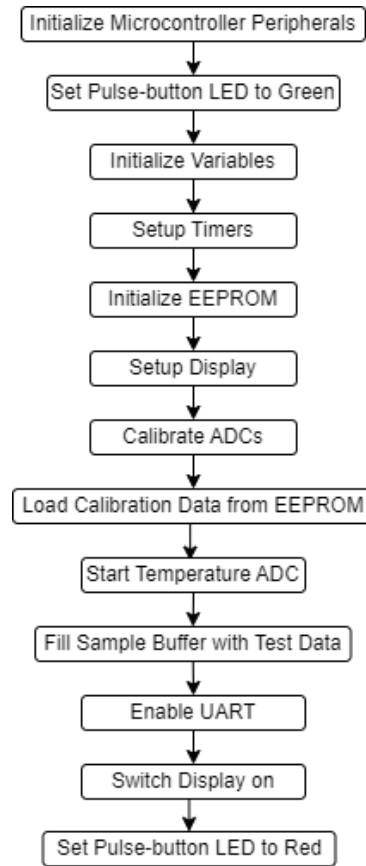
Figure 4.3: Flow diagram of the initialization process.

The first state, which will be entered after initialization is Idle-State. A detailed view of the Idle-State process can be seen in figure 4.4, 4.5 and 4.6. At the beginning of this state, seen in figure 4.4, the data received over UART will be processed. After that, the temperatures will be measured and the corresponding fault flag will be set if necessary. In order to be able to display when the high voltage threshold of 60V is exceeded, the voltages of the intermediate capacitors are continuously measured. Furthermore, this measured data is available over UART. Measuring the currents during idle state does not have a purpose, other than having a complete set of instructions over UART. After all measruements, the encoder is checked and the configuration accordingly changed. If the encoder switch is pressed for about two seconds, the local lock state is toggle. This disables or enables the usage of the human interface controls. This feature is implemented in order to avoid a change of the configuration, when it was set over UART. Pressing the encoder switch shortly twice in succession will clear all present fault flags. If faults are still present, they will be set again. Pressing the encoder switch only once will change the current parameter which can be changed by turning the encoder. It is possible to either change the pulse-time or the space-vector. A change of the configuration will then be updated on the display. A detailed explanation of how to use the inputs is in chapter A.

Before checking the pulse-button, the state of the hardware will be examined, as seen in figure 4.5. When turning the pulse-generator on for the first time, the high voltage is disabled. It needs to be turned on by pressing the pulse-button once. [2] If high voltage is not activated and no activation process is pending, the state of the hardware will be set to HV-activate. If a activation process is pending, the state will be set to CAUTION. This pending state is implemented in order to have a time to step back after pressing the pulse-button before high voltage will be activated. This timeout is three seconds. In the case that high voltage is activated, but faults are present, the state will be set to FAULT. If no faults are present, but the timeout after the pulse has been generated is still active, the state will be set to TIMEOUT, otherwise READY.

With this information about the state of the hardware the pulse-button can be checked and the corresponding action can be taken. Either starting the activation process of the high voltage or starting the pulse generation by setting the corresponding flag. It has to be mentioned, that the interrupt for the external trigger input is being disabled when generating a pulse in order to avoid re-triggering by external disturbances. As previously mentioned, a detailed explanation of how to use the inputs is in chapter A.

After checking the pulse-button, the trigger input will be checked. Despite the external trigger input being interrupt driven, as seen in figure 4.7, the interrupt only sets a flag. This flag indicates a rising flag has been detected on the trigger input. The processing of this flag takes place in the Idle-State, seen figure 4.6. If the flag is set, it will be cleared during checking. In the case that the high voltage has been activated already, the pulse flag will be set and the trigger input interrupt will be disabled.

The next step is to verify whether the high voltage activation is pending. If that is the case and the timeout is over, the HV-activation flag will be set and the relais can enabled. The high voltage will not necessarily be enabled during this step, as this depends also on the HV-switch and the emergency-switch state, which can only be actuated manually.

The last step of the Idle-State is to check whether a pulse shell be generated. If the pulsing flag is set, the state of the software will be changed to PULSE-START. When the state of the software does no change, the Idle-State will be executed all over again.

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[2] The HV-Switch has to be enabled as well
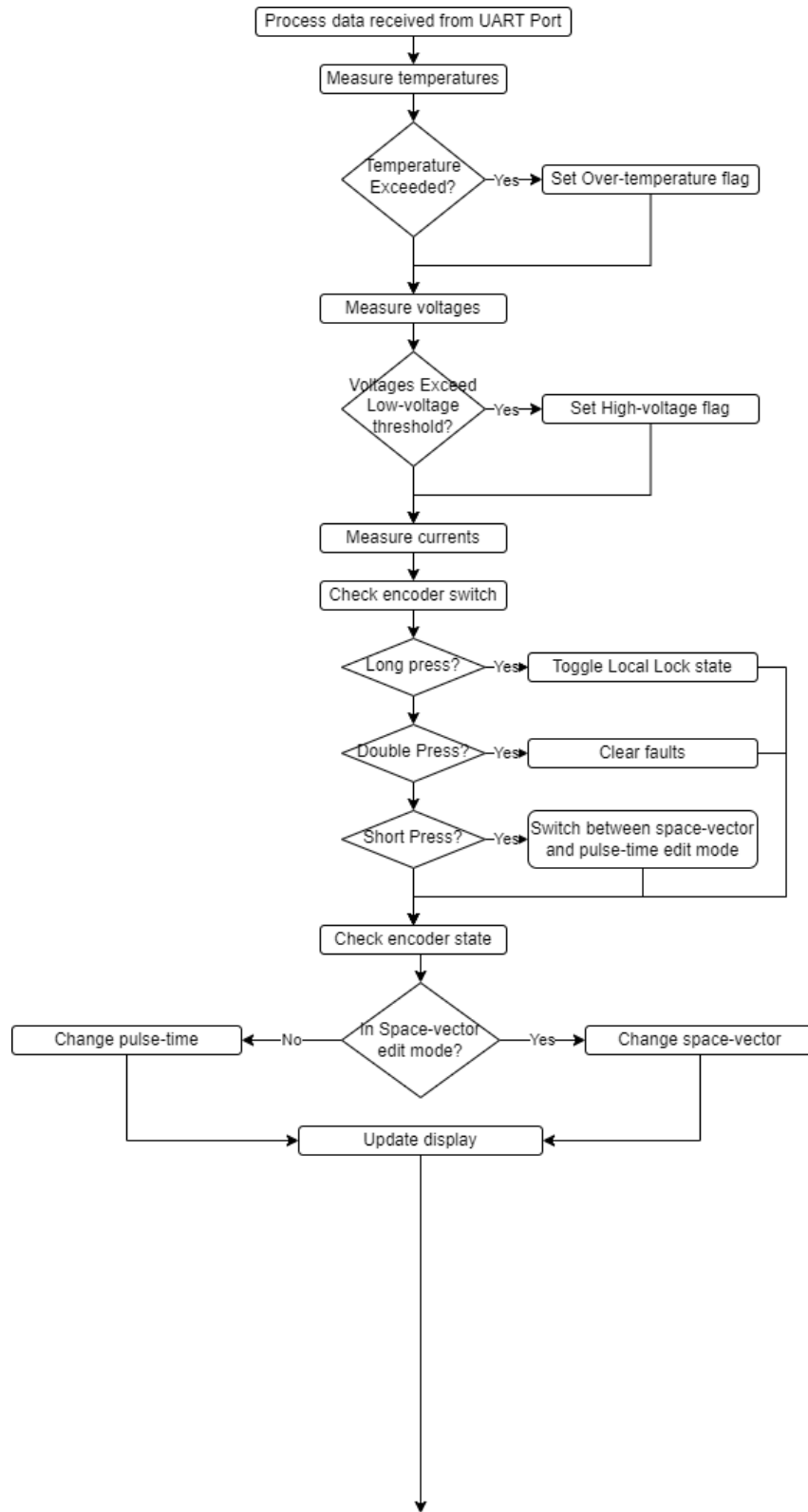
Figure 4.4: Flow diagram of the first part of the Idle State.
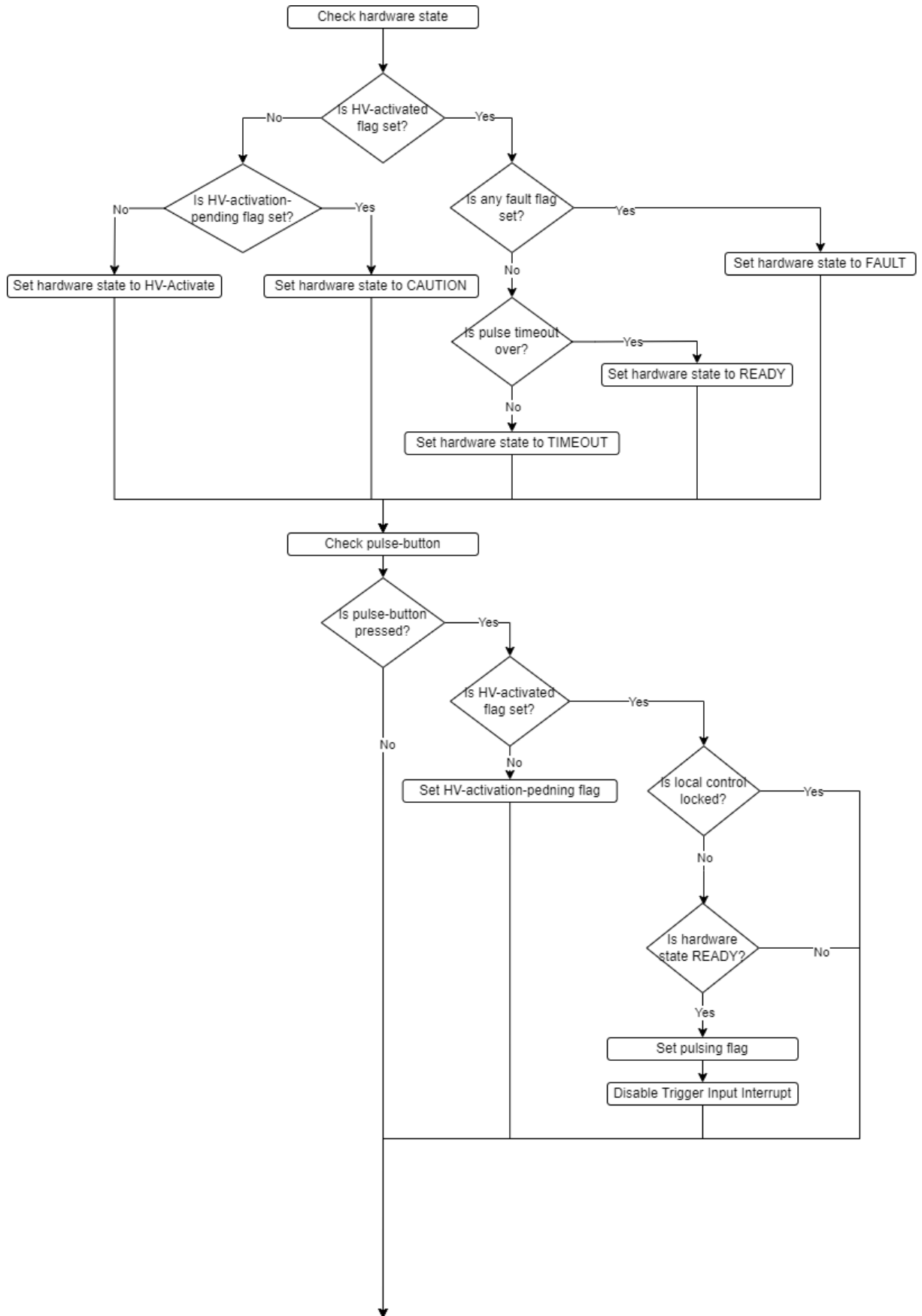
Figure 4.5: Flow diagram of the second part of the Idle State.
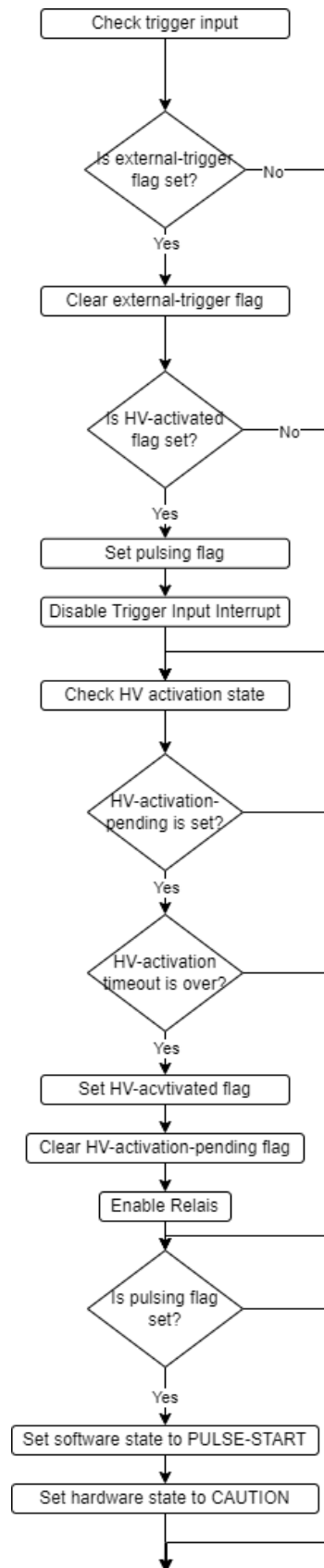
Figure 4.6: Flow diagram of the third part of the Idle State.

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One of the most important interrupts, are the GPIO interrupts, as seen in figure 4.7. These interrupts are connected to the over-voltage, over-current and trigger-input signals. Over-voltage and over-current interrupts are always active and only set the corresponding fault flags as well as stop the pulsing process by clearing the corresponding flag and stop the ADC data transfer. The trigger-input interrupt is only active during Idle-State to avoid re-triggering during pulsing.
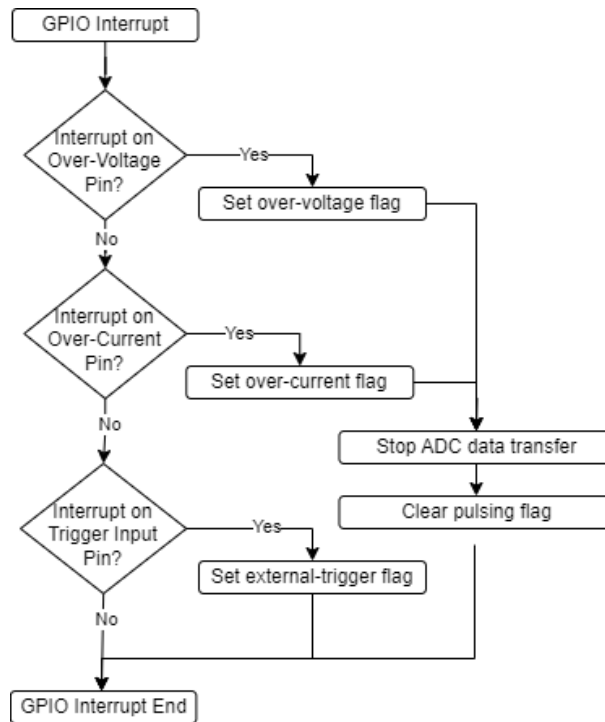
Figure 4.7: Flow diagram of the GPIO interrupt routine.

When the PULSE-START is entered, the micro-controller prepares to generate a pulse, seen in figure 4.8. Firstly, the pulse-button led is set to red to indicate to be cautious. After that the current timestamp is saved in order to calculate the correct timeout and the sample buffer is cleared. The pulse-button is set to red again and the timers are configured for the correct pulse-time and for the correct space-vector. At last, the current sensing ADC data transmission is started and the pulse generated.
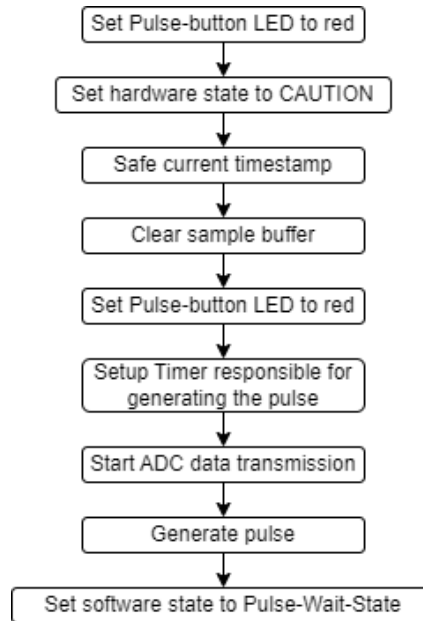
Figure 4.8: Flow diagram of the Pulse-Start state.

After the pulse has been generated, the PULSE-WAIT state is entered. In this state, it will be waited until the pulse is over, see figure 4.9. If that is the case, the trigger input interrupt will be enabled again and the IDLE-STATE will be entered. The waiting for the pulse to be over is implemented as a separate state in order to minimize interruption during data transfer of the ADCs.
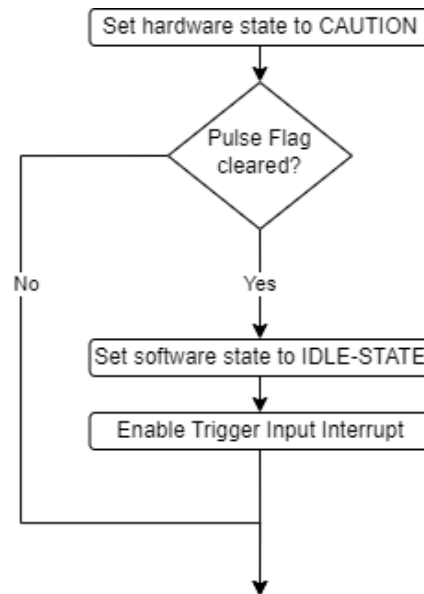
Figure 4.9: Flow diagram of the Pulse-Wait state.

Chapter 5

Measurements

The equipment used for the measurements is specified in table 5.1.

Table 5.1: Measurement equipment used

Name	Manufacturer	Type
Differential high-voltage probe	Testec	TT-SI-9110
Oscilloscope	Agilent	DSO5034A
Multi-meter	Fluke	175
Current clamp	Tectronix	TCPA300

At first, the charging speed of the intermediate circuit capacitor [1] is analyzed. This is done by closing the transformers connection to the main grid and observing the voltage change of the intermediate circuit capacitor. The voltage was measured by using the high-voltage probe and the oscilloscope. In figure 5.1 the voltage of the capacitor over time is shown. Due to some remaining charge in the capacitor, the voltage does not start at zero. This offset can be neglected for a rough estimation. The capacitor charges up to about 750 volts. 63% or 470 volts are reached after about 200 milliseconds, which is approximately the time constant τ of a RC-low-pass filter. With a capacitance of $C = 130uF \cdot 3/2 = 195uF$, this results in a parasitic resistance of $R = \tau/C = 1k\Omega$. This in return results in a maximum charge current of about $750V/1k\Omega = 750mA$. Due to the sinusoidal voltage applied to the capacitor, the effective current will be much lower.

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[1]Singular is used in order to keep the text simple. The intermediate circuit capacitor actually consists of six capacitors
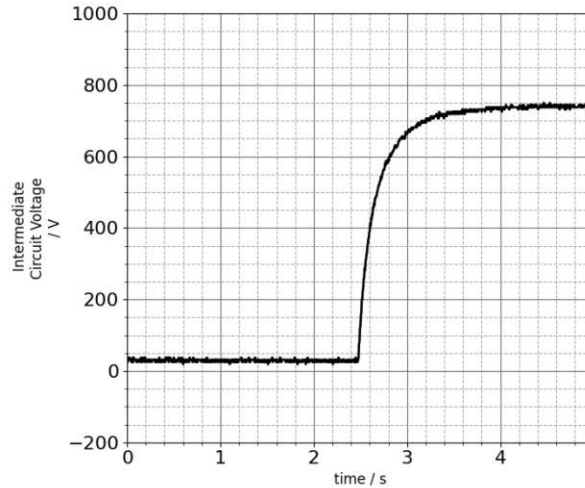
Figure 5.1: Time signal of voltage across intermediate circuit capacitors during initial charging

In order to investigate the reaction speed of the gate-driver a rectangular signal was applied to the input of the gate-driver via the function generator of the oscilloscope. The output signal was then measured with a 10:1 probe. In figure 5.2 can the signals be seen. It takes the gate-driver about 300ns to react to the input both on falling and rising edge of the input signal. Since the delay on both input signal changes is about equal, it does not influence the pulse length generated. The shortest possible pulse length has to be longer than the delay of the gate-driver. Due to the fact, that the shortest pulse is limited to 1us, see table A.1, this delay is sufficient.
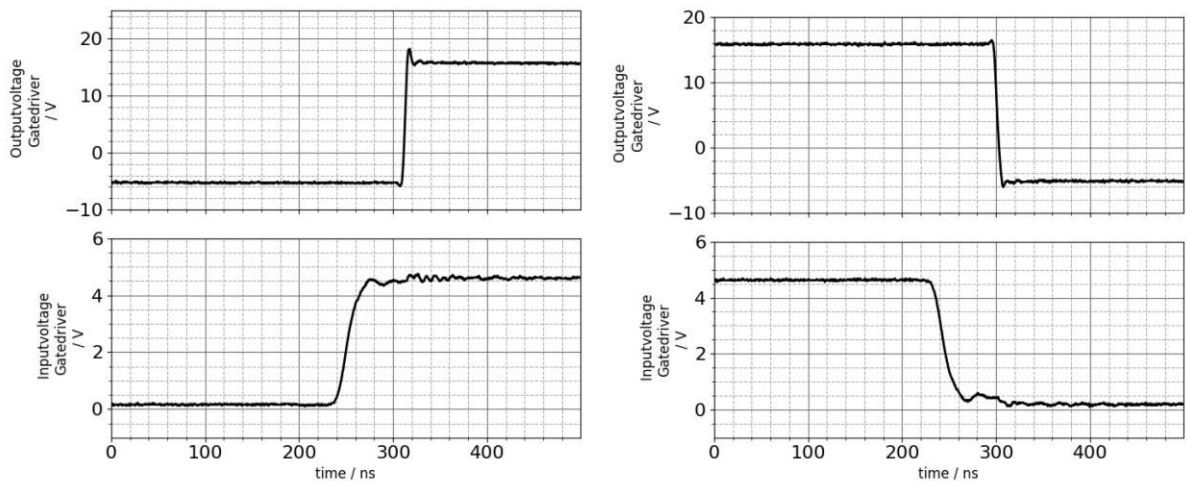
(a) Time signal of input and output signals of the gate-driver when switched on.

(b) Time signal of input and output signals of the gate-driver when switched off.

Figure 5.2: Analysis of latency of the gate-driver.
Upper curve shows the output signal of the gate-driver.
Lower curve shows the input signal of the gate-driver.

To prevent the low-side transistor from switching during high-side transistor on, the gate resistance has to be set correctly. In order to test this, an inductance was connected between the terminal of phase w and the negative high voltage potential. The gate-emitter voltage of the low-side transistor was measured by using a 10:1 probe and the oscilloscope, and the current through the inductance was measured by using the current clamp. In figure 5.3 the measured current and voltage signals can be seen. The turn-off-resistance[2] chosen is 10Ω, which results in the gate-emitter voltage not exceeding the threshold voltage of about 3 volts. Furthermore, the gate-emitter voltage does not exceed the lower limit of -20 volts, according to the datasheet of the transistor. Choosing a lower off-resistance than 10Ω results in greater voltage swings on the gate of the low-side transistor. Higher resistance slows the switching process unnecessarily more down and increases switching losses.

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[2]Off-resistance is the resistance value of the gate-driver when driven low.
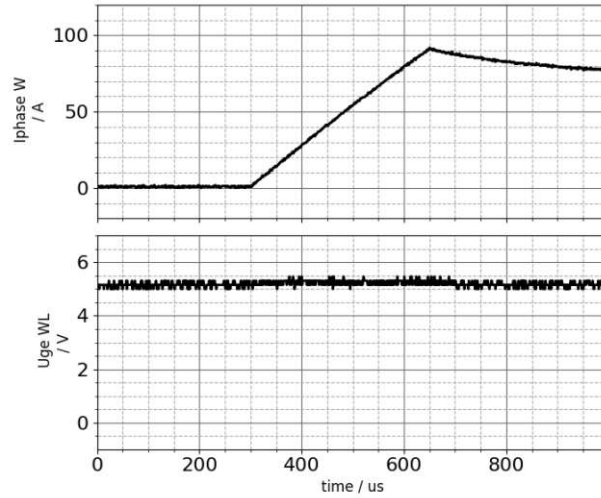
(a) Time signal of the complete pulse duration.
Upper curve shows the current through the inductance and the high-side transistor.
Lower curve shows the gate-emitter voltage of the low-side transistor.

(b) Zoomed in time signal: The high-side transistor starts to conduct.
Upper curve shows the current through the inductance and the high-side transistor.
Lower curve shows the gate-emitter voltage of the low-side transistor.

(c) Zoomed in time signal: The high-side transistor stops to conduct.
Upper curve shows the current through the inductance and the high-side transistor.
Lower curve shows the gate-emitter voltage of the low-side transistor.

Figure 5.3: Analysis of gate-emitter-voltage of low-side transistor of phase w during high-side switching. Turn-off-resistance of the gate-drivers is 10Ω. An inductance is connected between the terminal of phase w and the negative high voltage potential.
Upper diagram shows the complete signal.
Lower diagrams show the zoomed in time signal of when the high-side transistor starts to or stops to conduct.

The turn-on-resistance of the gate-driver influences the collector-emitter voltage swing of the high-side transistor. It is important, that the voltage swing does not exceed the upper limit of the transistors collector-emitter voltage rating. To test the behaviour, the collector-emitter voltage across the high-side transistor was measured by using the high-voltage probe and the current through the inductance by using the current clamp. The inductance is connected between the phase w terminal and the negative high voltage potential. The results of the measurements by using 10Ω turn-on-resistance can be seen in figure 5.4. It can be seen that significant voltage swings occur during the high-side transistor stopping to conduct. Since the voltage swing does not exceed 1200 volts, according to the datasheet of the transistor, the criteria is satisfied. Lower turn-on-resistance will lead to greater voltage swings, higher resistance to lower voltage swings but slower switching processes.

(a) Time signal of the complete pulse duration.
Upper curve shows the current through the inductance and the high-side transistor.
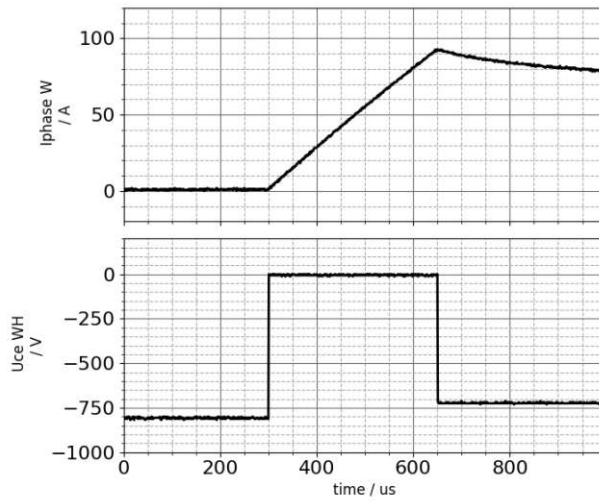Lower curve shows the collector-emitter voltage of the high-side transistor.

(b) Zoomed in time signal: The high-side transistor starts to conduct.
Upper curve shows the current through the inductance and the high-side transistor.
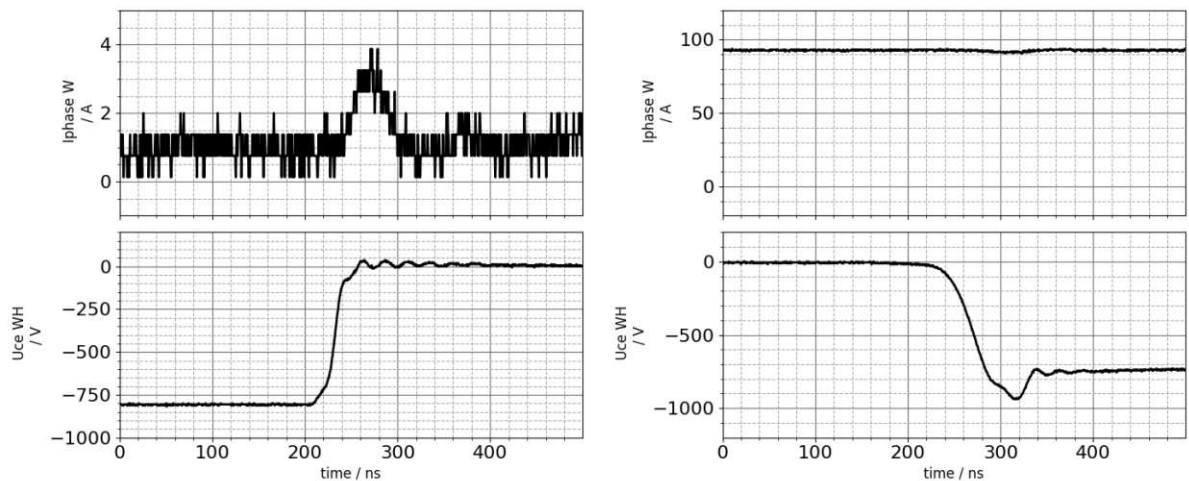Lower curve shows the collector-emitter voltage of the high-side transistor.

(c) Zoomed in time signal: The high-side transistor stops to conduct.
Upper curve shows the current through the inductance and the high-side transistor.
Lower curve shows the collector-emitter voltage of the high-side transistor.

Figure 5.4: Analysis of collector-emitter-voltage of high-side transistor of phase w during high-side switching. Turn-on-resistance of the gate-driver is 10Ω. An inductance is connected between the terminal of phase w and the negative high voltage potential.
Upper diagram shows the complete signal.
Lower diagrams show the zoomed in time signal of when the high-side transistor starts to or stops to conduct.

It is important to also verify the criteria of the gate-emitter and the collector-emitter voltages not exceeding any limits on the other phases. The measurements of phase v can be seen in figure 5.5 and those of phase u in figure 5.6. It can be seen that the gate-emitter voltage of phase u does exceed the threshold voltage and would therefore start to conduct. Fortunately, this happens while the high-side transistor stops to conduct. Would the operation of the transistors be continuous, the conduction of the low-side transistor may lead to overheating. Therefore, this problem would need to be tackled. However, due to the fact that this is a pulse application, the possible losses do not add up significantly.

(a) Time signal of the complete pulse duration.
Upper curve shows the current through the inductance and the high-side transistor.
Middle curve shows the collector-emitter voltage of the high-side transistor.
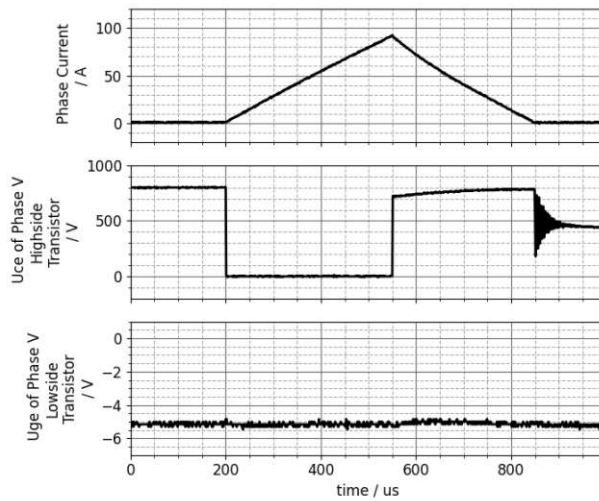Lower curve shows the gate-emitter voltage of the low-side transistor.

(b) Zoomed in time signal: The high-side transistor starts to conduct.
Upper curve shows the current through the inductance and the high-side transistor.
Middle curve shows the collector-emitter voltage of the high-side transistor.
Lower curve shows the gate-emitter voltage of the low-side transistor.

(c) Zoomed in time signal: The high-side transistor stops to conduct.
Upper curve shows the current through the inductance and the high-side transistor.
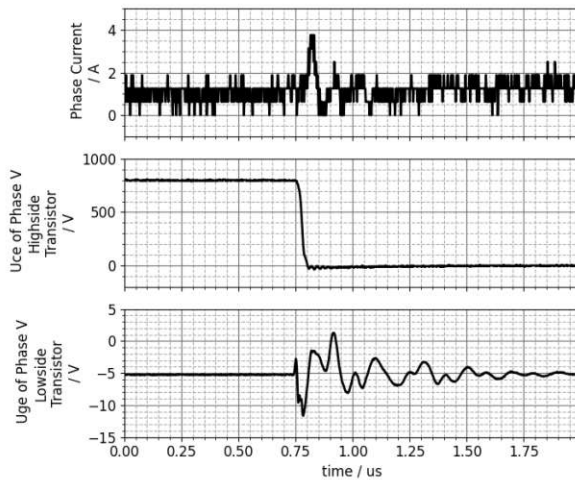Middle curve shows the collector-emitter voltage of the high-side transistor.
Lower curve shows the gate-emitter voltage of the low-side transistor.

Figure 5.5: Analysis of collector-emitter-voltage of high-side transistor and gate-emitter voltage of low-side transistor of phase V during high-side switching.
Upper diagram shows the complete signal.
Lower diagrams show the zoomed in time signal of when the high-side transistor starts to or stops to conduct.
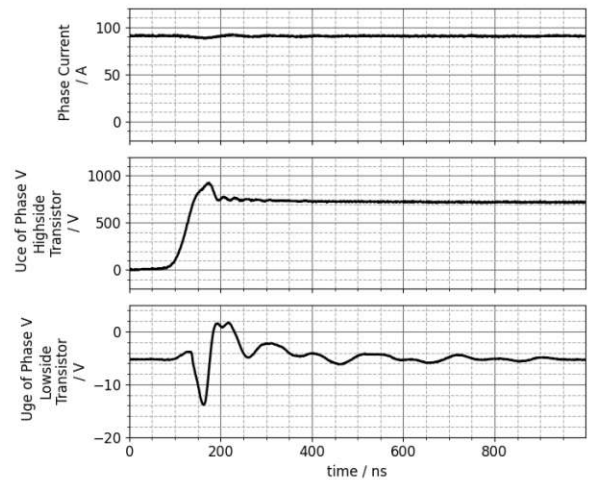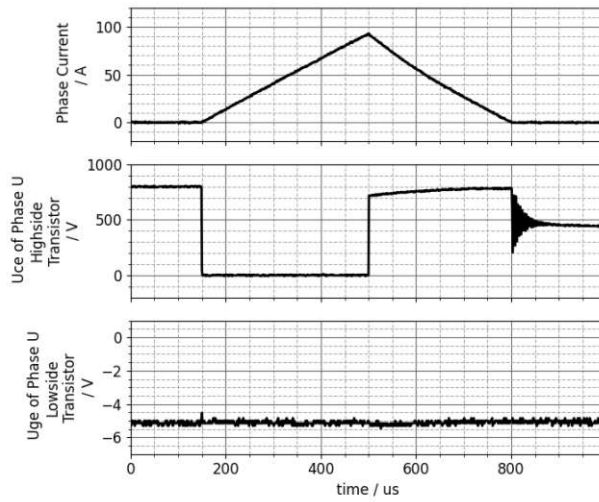
(a) Time signal of the complete pulse duration.
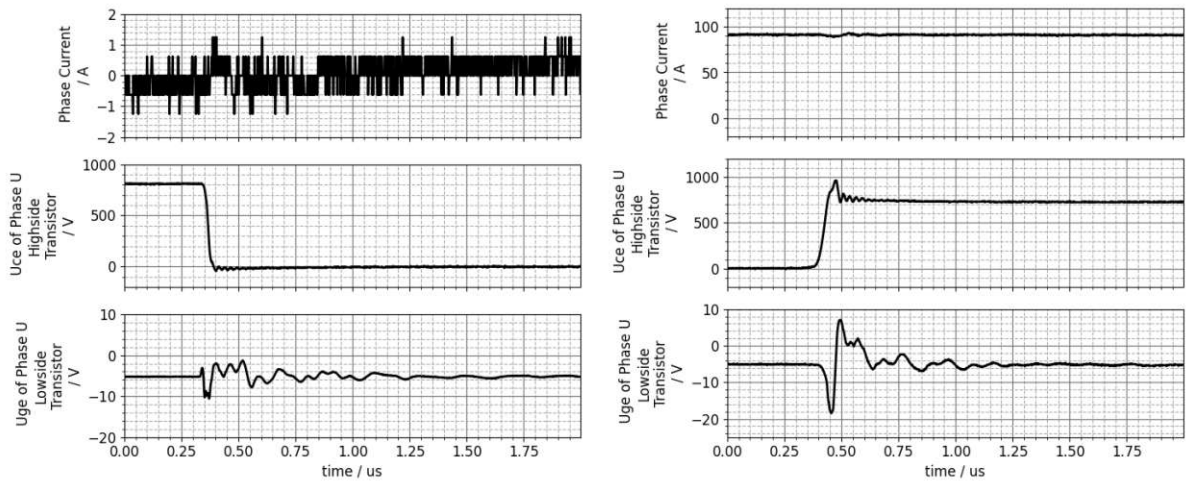
(b) Zoomed in time signal: The high-side transistor starts to conduct.

Upper curve shows the current through the inductance and the high-side transistor.

Middle curve shows the collector-emitter voltage of the high-side transistor.

Lower curve shows the gate-emitter voltage of the low-side transistor.

(c) Zoomed in time signal: The high-side transistor stops to conduct.

Upper curve shows the current through the inductance and the high-side transistor.

Middle curve shows the collector-emitter voltage of the high-side transistor.

Lower curve shows the gate-emitter voltage of the low-side transistor.

Figure 5.6: Analysis of collector-emitter-voltage of high-side transistor and gate-emitter voltage of low-side transistor of phase U during high-side switching.

Upper diagram shows the complete signal.

Lower diagrams show the zoomed in time signal of when the high-side transistor starts to or stops to conduct.

The test of the over-current shutdown mechanism can be seen in figure 5.7 for negative phase currents and in figure 5.8 for positive phase currents. In 5.7 it can be seen that the triggering of the over-current protection takes place just a little below -100 amperes of phase current. This can be explained due to components tolerances and operation amplifier offsets. Due to the fact, that the maximum current is allowed to be 120 amperes before damage occurs, this is a sufficient result. On positive phase currents, see figure 5.8, the threshold for the over-current protection is a little below 100 amperes. This suggests that there is an offset error in the system. However, since this thresholds are within the boundaries of 120 amperes, this are sufficient results.

(a) Time signal of the complete over-current test signals

Upper curve shows the current through the inductance and the low-side transistor of phase w.
Second curve shows the input voltage of the low-side transistors gate-driver.
Third curve shows the collector-emitter voltage of the low-side transistor.
Lower curve shows the over-current signal.

(b) Zoomed in time signal of the over-current test signals

Upper curve shows the current through the inductance and the low-side transistor of phase w.
Second curve shows the input voltage of the low-side transistors gate-driver.
Third curve shows the collector-emitter voltage of the low-side transistor.
Lower curve shows the over-current signal.

Figure 5.7: Analysis of over-current protection on negative phase w current.
Left diagram shows the whole time signal.
Right diagram shows the zoomed signal.

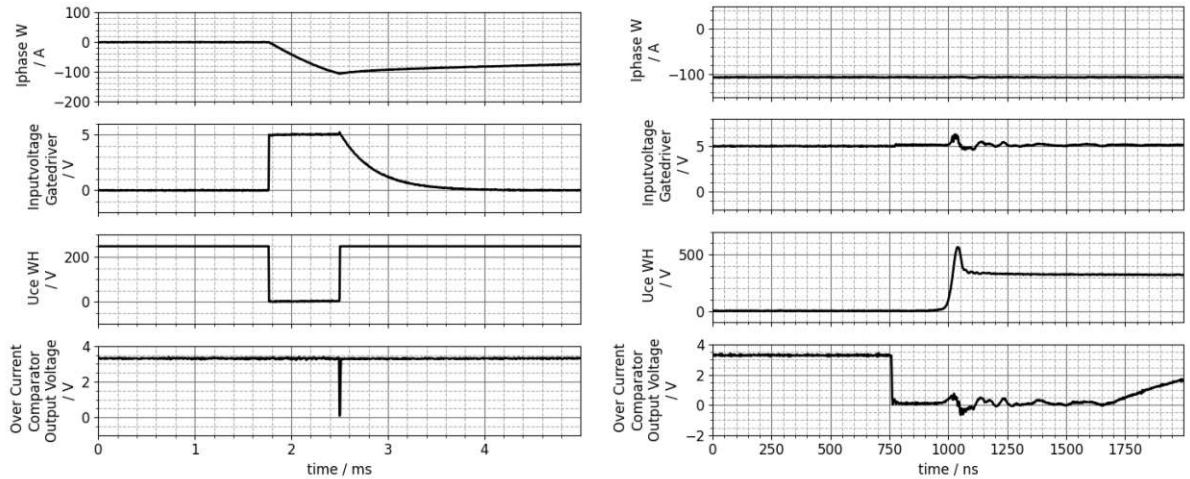**(a)** Time signal of the complete over-current test signals

Upper curve shows the current through the inductance and the high-side transistor of phase w.

Second curve shows the input voltage of the high-side transistors gate-driver.

Third curve shows the collector-emitter voltage of the high-side transistor. Lower curve shows the over-current signal.

(b) Zoomed in time signal of the over-current test signals

Upper curve shows the current through the inductance and the high-side transistor of phase w.

Second curve shows the input voltage of the high-side transistors gate-driver.

Third curve shows the collector-emitter voltage of the high-side transistor. Lower curve shows the over-current signal.

Figure 5.8: Analysis of over-current protection on positive phase w current.
Left diagram shows the whole time signal.
Right diagram shows the zoomed signal.

Over-voltage protection is tested by connecting an external high-voltage power source directly to the capacitor which is tested. This external power source is configured as current source in order to get a linear voltage rise. The voltage across the tested capacitors is measured with an high-voltage probe and the over-voltage signal with an 10:1 probe. Test results can be seen in figure 5.9. The over-voltage protection of the upper capacitors and the one of the lower capacitors are tested separately. Both results are as expected and trigger just a little below 500 volts.

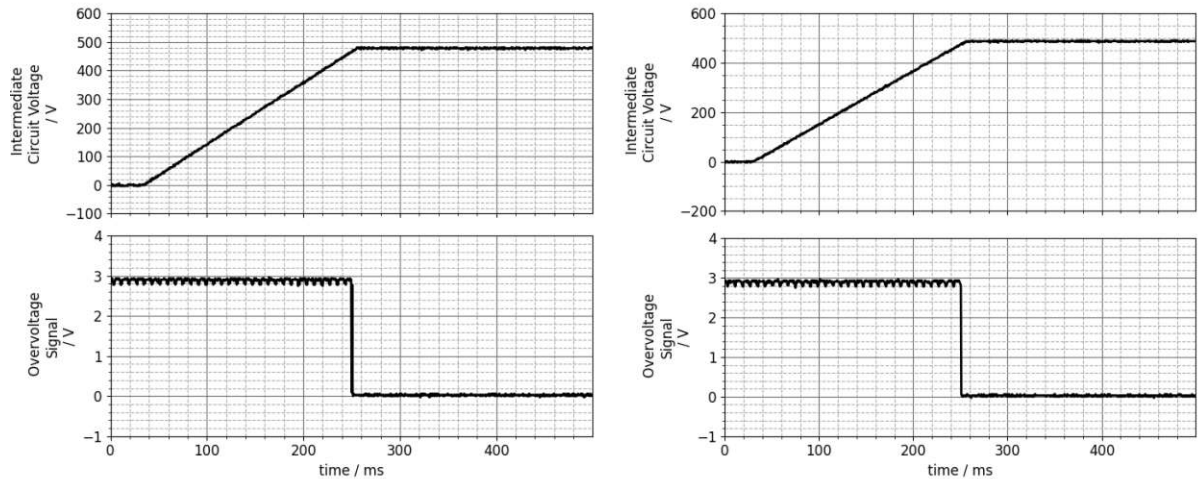**(a)** Time signal of the complete over-voltage test signals
Upper curve shows the voltage of the lower intermediate circuit capacitor.
Lower curve shows the over-voltage signal.

(b) Time signal of the complete over-voltage test signals
Upper curve shows the voltage of the upper intermediate circuit capacitor.
Lower curve shows the over-voltage signal.

Figure 5.9: Analysis of over-voltage protection.
Left diagram shows the time signals for the lower capacitor over-voltage test.
Right diagram shows the time signals for the upper capacitor over-voltage test.

Currents can be measured in three different ways. Either by using a current clamp or measuring the output voltage of the current sensors with an oscilsocope or by logging the data of the internal ADCs. All three ways are compared in figure 5.10. It can be seen that the voltage measurement of the current sensor output has the most resolution regarding bandwidth, since voltage spikes can be seen at the discontinuities. The performance of current clamp and ADCs looks the same. However, further investigation would show that current clamp has more resolution. This investigation is not shown here since the only two methods which will be used are the sensors output voltage and the ADCs.
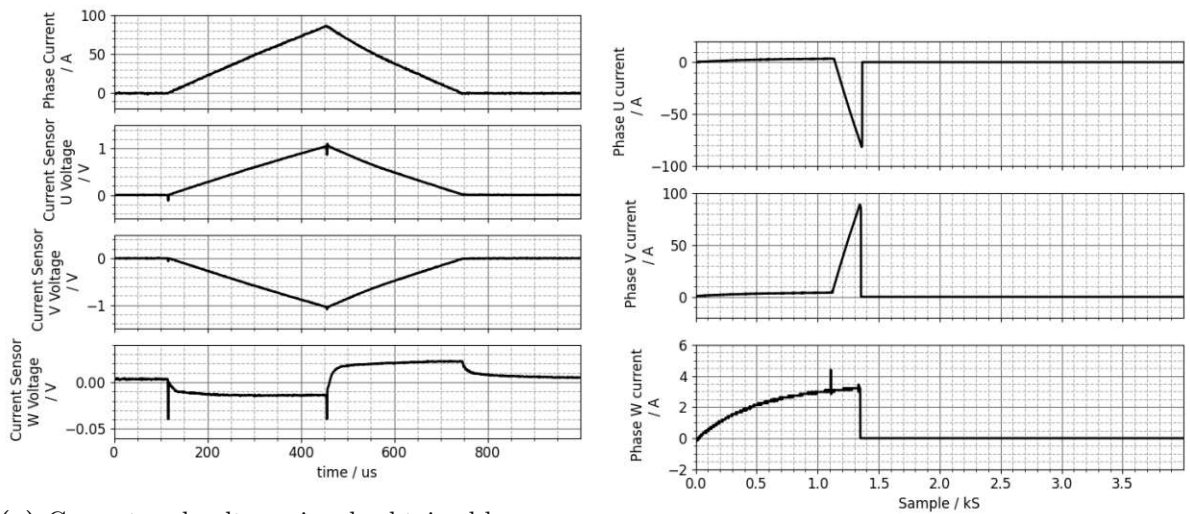
(a) Current and voltage signals obtained by an oscilloscope during a pulse.

Upper curve shows the current measured by an oscilloscope using the current clamp.

Second curve shows the output voltage of the current sensor of phase u.

Third curve shows the output voltage of the current sensor of phase v.

Fourth curve shows the output voltage of the current sensor of phase w.

(b) Current signals obtained by the internal ADCs during a pulse.

Upper curve shows the output voltage of the current sensor of phase u.

Middle curve shows the output voltage of the current sensor of phase v.

Lower curve shows the output voltage of the current sensor of phase w.

Figure 5.10: Comparison of current measurements.
Left diagram shows measurements obtained by an oscilloscope.
Right diagram shows measurements obtained by the internal ADCs.

Appendix A

Manual

Table A.1: Pulse generator specifications

Minimum pulse duration	1 us
Maximum pulse duration	2000 us
Pulse Period	5x pulse duration
Maximum current measureable	100 A
Maximum current non-measureable	120 A
Intermediate circuit voltage	$\approx 750V$
Over-current protection	$\approx \pm 95A$
Over-voltage protection	$\approx \pm 450V$

A.1   Turning On

In order to turn on the pulse-generator, following steps have to be done in the exact order

1. Make sure the power-switch is in off position

2. Connect the pulse-generator with the main grid

3. Turn on the pulse-generator by turning the power-switch in on position

After being turned on, the pulse-pushbutton led will begin to light up in green. This indicates, that the micro-controller is powered and is now initializing the peripherals. After initialization, the display will turn on and the pulse-pushbutton led will start to light up in red. In order to prevent high voltage generation on power-up, the pulse-generator demands an initial pulse-pushbutton press to enable the high voltage. [1] This is indicated by the pulse-pushbutton led flashing in red. When pressed, the led will stop flashing. There is now a three seconds delay until the high voltage is enabled. This delay is for being able to step back.

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[1]The generation of high voltage is controlled over a relais, which disconnects the transformers from the main grid. Said relais is controlled via the HV-switch, the micro-controller and the emergency switch. In order to have the high voltage enable, all three switches have to be closed. Since the HV-switch and the emergency switch are latching, high voltage could be generated on power-up. To prevent this, the micro-controller disables the high voltage, until the pulse-pushbutton is pressed once.
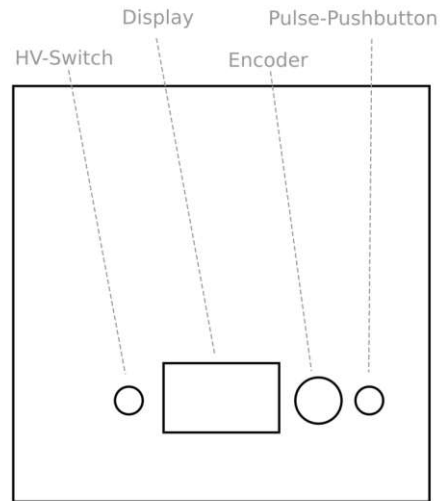
A.2 Designation of peripherals

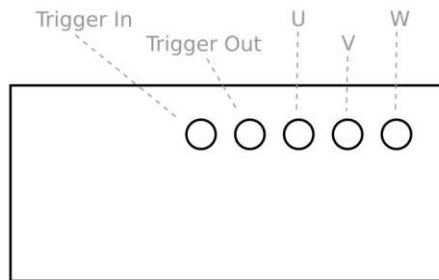**Figure A.1:** Designation of peripherals of upper side.

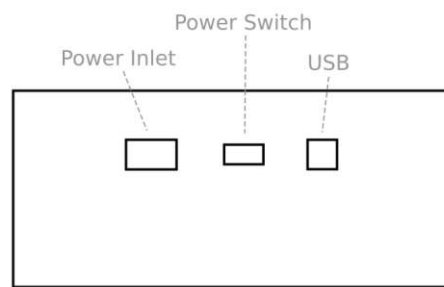**Figure A.2:** Designation of peripherals of right side.

Figure A.3: Designation of peripherals of left side.

A.3 Display

The display shows the state of the faults, the high voltage rail, the space vector and the pulse time.

(a) Display with no faults active   (b) Display with faults active
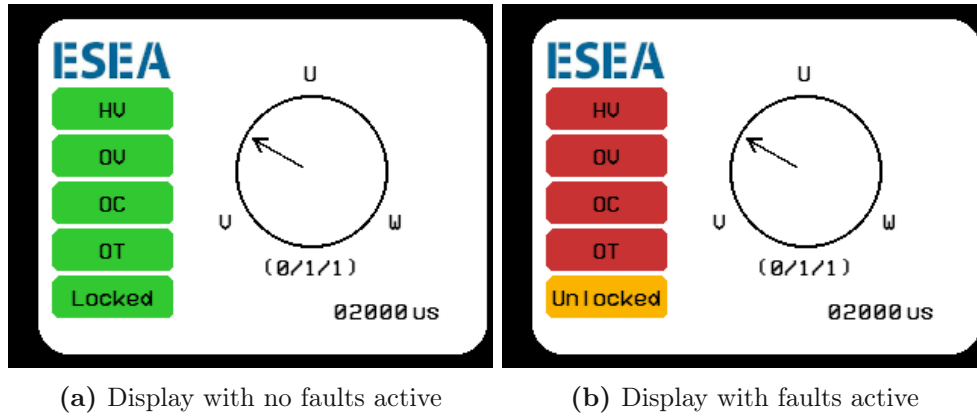
Figure A.4: Display with and without faults active.

The five **status panels** on the left side mostly represent different state.

- **HV-panel**: Represents the Voltage of intermediate capacitors.
  Green - Voltage is less than 60V
  Red - Voltage above 60V

- **OC-panel**: Represents the over-current fault state.
  Green - No over-current fault occurred
  Red - Over-current fault occurred

- **OV-panel**: Represents the over-voltage fault state.
  Green - No over-voltage fault occurred
  Red - Over-voltage fault occurred

- **OT-panel**: Represents the over-temperature fault state.
  Green - No over-temperature fault occurred
  Red - Over-temperature fault occurred

- **Unlocked/locked-panel**: Represents the local control state.
  Green - Local control is disabled. Encoder and pulse-pushbutton are disabled
  Orange - Local control is enabled. Encoder and pulse-pushbutton are enabled

The circle in the middle in combination with the arrow and the three numbers under it, represent the **space vector** state. Each number corresponds to one phase with the number one being the high state and the number zero being the low state. It is possible to configure the space vector in a way, so that all phases are pull high or low. High and low means, that the phase is being pulled to the upper or lower potential of the intermediate capacitors voltage.

The **pulse time** can be configured in 10us steps from 10us up to 2ms.

A.4 Controls and Indicators

A.4.1 HV-Switch LED

Meaning of the HV-Switch LEDs light:

- [Red continous] High voltage is enabled. Transformators are powered. Capacitors may still be discharged

- [Off] High voltage is disabled. Transformators are not powered anymore. The capacitors may however be still charged

A.4.2 HV-Switch

Effects of pressing the HV-switch:

- On-position: HV may be enabled

- Off-position: HV is disabled

A.4.3 Pulse-Pushbutton LED

Meaning of the Pulse-Pushbutton LEDs light and patterns:

- [Green continuous] Ready for pulse generation

- [Green flashing] Timeout (3 seconds) is active. Occurs after pulse has been generated

- [Red continuous] Caution. Either the high voltage is being enabled OR a pulse is currently generated.

- [Red flashing] HV Activation. High voltage has to be enabled by pressing the pulse-pushbutton once. Occurs after power-up

- [Off] Faults have been detected. Faults have to be cleared in order to continue operation

A.4.4 Pulse-Pushbutton

Effects of pressing the pulse-pushbutton:

- Activate high voltage: When the pulse-pushbutton led is flashing red

- Pulse generation: When the pulse-pushbutton led lights up green

- No effect: When faults are present, timeout is active or local control is disabled.

A.4.5 Encoder

Turning the encoder changes the configuration of either the space vector or the pulse time. If local control is disabled, turning the encoder has no effect.

Effects using encoder-pushbutton:

- Pressed once shortly: Switching between space vector and pulse time configuration

- Pressed twice shortly: Clearing present faults

- Pressed long: Toggling the local control enabling state

Appendix B

Schematics

In this chapter, the schematics of the designed pcbs are depicted. Starting with the schematic of the gate drivers and following with the schematics of the main pcb.
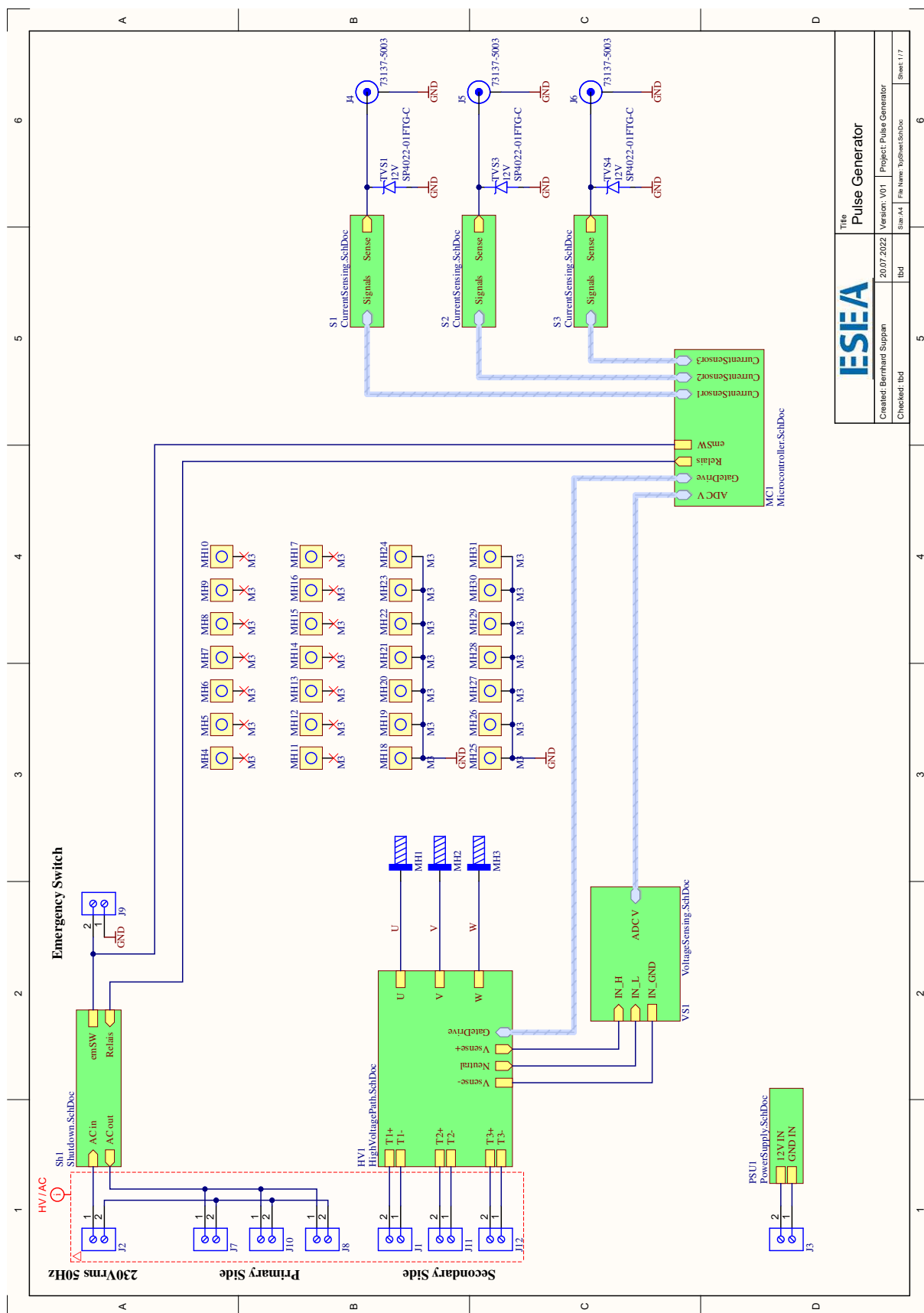
Input Filter:
According to AN
Supress Switching Frequencies
Avoid noise coupling

Zener Diode:
According to AN
Avoids overshoot due to high dV/dt

MGJ2D121505SC

The minimum load to meet datasheet specification is 10% of the full rated load across the specified input voltage range.
Lower than 10% minimum loading will result in an increase in output voltage, which may rise to typically 1.25 times the specified output voltage if the output load falls to less than 5%.

Output Current Vout -5V: 40mA
Output Current Vout +15V: 80mA

Si8261BCC

Input Forward Voltage: 1V (OFF) 1.6V - 2.8V(ON)
Input Forward Current: 3.6mA (MIN) 30mA (MAX)
Output Current: 1.8A (Source) 4A (Sink)
UVLO: 12V (Rising) 10.7V (falling)

Diode for Fast turn off
gate turn on resistance 2 Ohm -> In datasheet of
IGBT 2 Ohms are used

AN677

Decrease common-mode transient immunity by ading a pull down resistor
Decrease common-mode transient immunity by connecting NC pins to input side ground plane

L1 10µH 250mA
12V
GND
C1 10µF 16V
TVS1 SP4022-01FTG-C 12V
P1 1 2 3 Anode

IC1 MGJ2D121505SC
+Vin -Vin
+Vout -Vout 0V

15V_ISO
ZD1 BZX384-C16F 16V
ZD2 PDZ5.6B,115 5.6V
5V_ISO

C2 100nF C3 10µF 50V C4 10µF 50V
C5 100nF C6 10µF 50V C7 10µF 50V
HV

R4 100R R3 100R
C8 100pF R5 1k
LV

IC2 Si8261BBC-C-IS
NC VDD
Anode VO
Cathode VO
NC GND
GND

HV
Gate# R1 0R R2 2R
D1 SS26FL 2A
Gate
Emitter
P2 1 2 3

TP1 15V_ISO
TP2 -5V_ISO
TP4 Anode
TP3 GND 50l6
TP6 Emitter 50l6

ESE/A

Created: Bernhard Suppan	20.07.2022	Version: V01	Project: Gate Driver
Checked: tbd	tbd	Size: A4	File Name: TopSheet.SchDoc
			Sheet: 1 / 1

Title
Gate Driver

Figure B.1: Schematic of the gate driver.

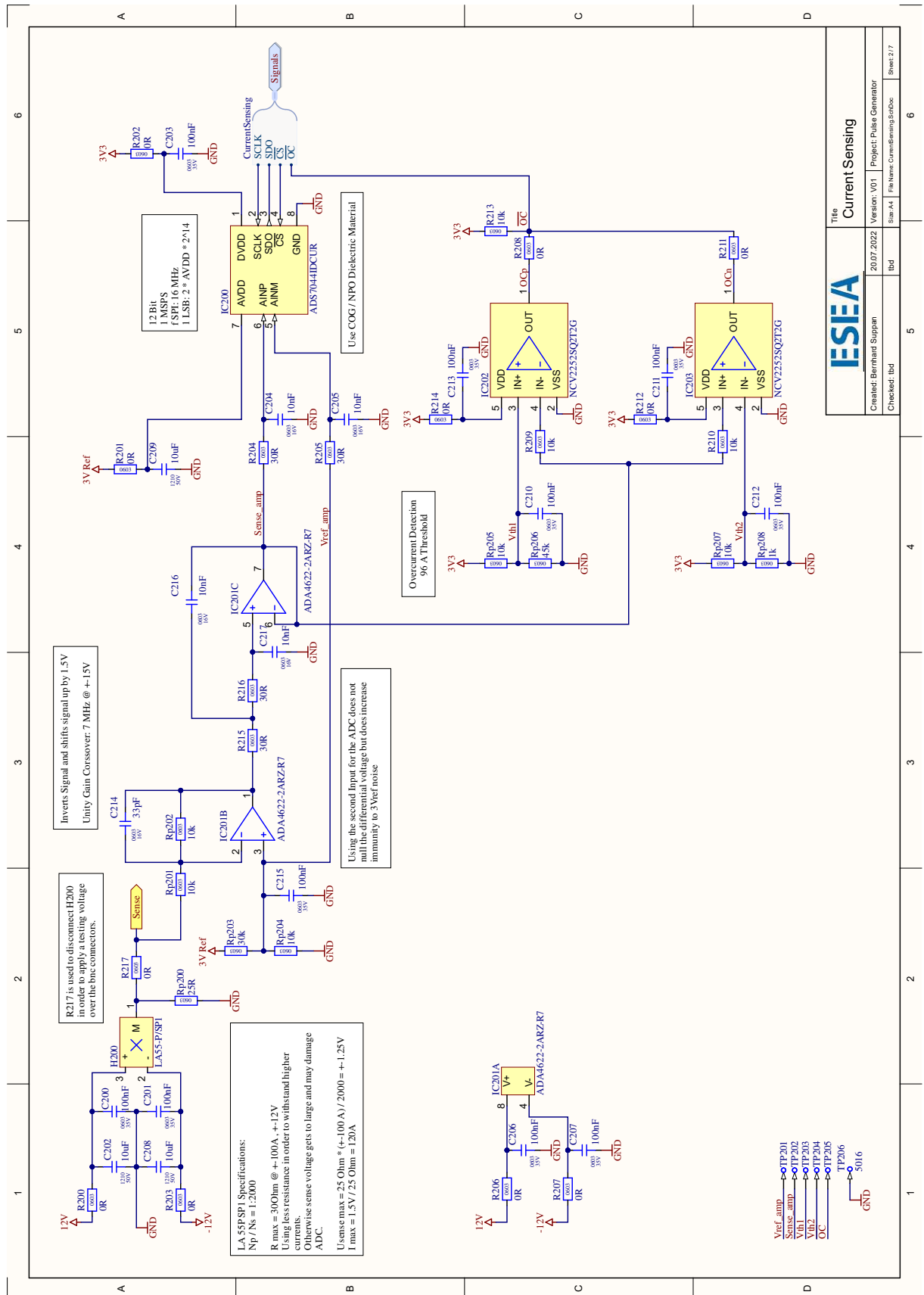**Figure B.2:** Schematic of the main pcb - Top Sheet.

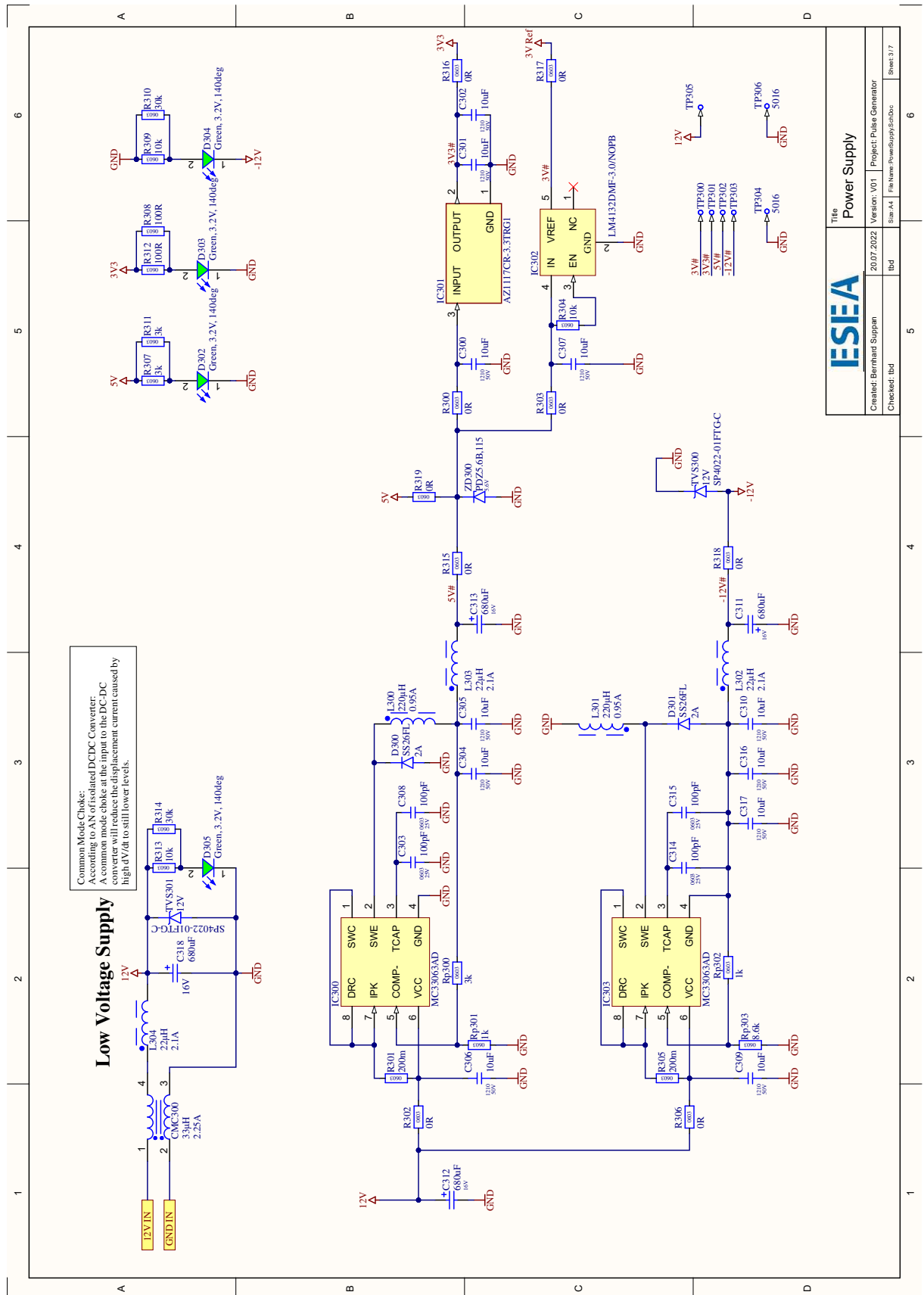**Figure B.3:** Schematic of the main pcb - Current Sensing.

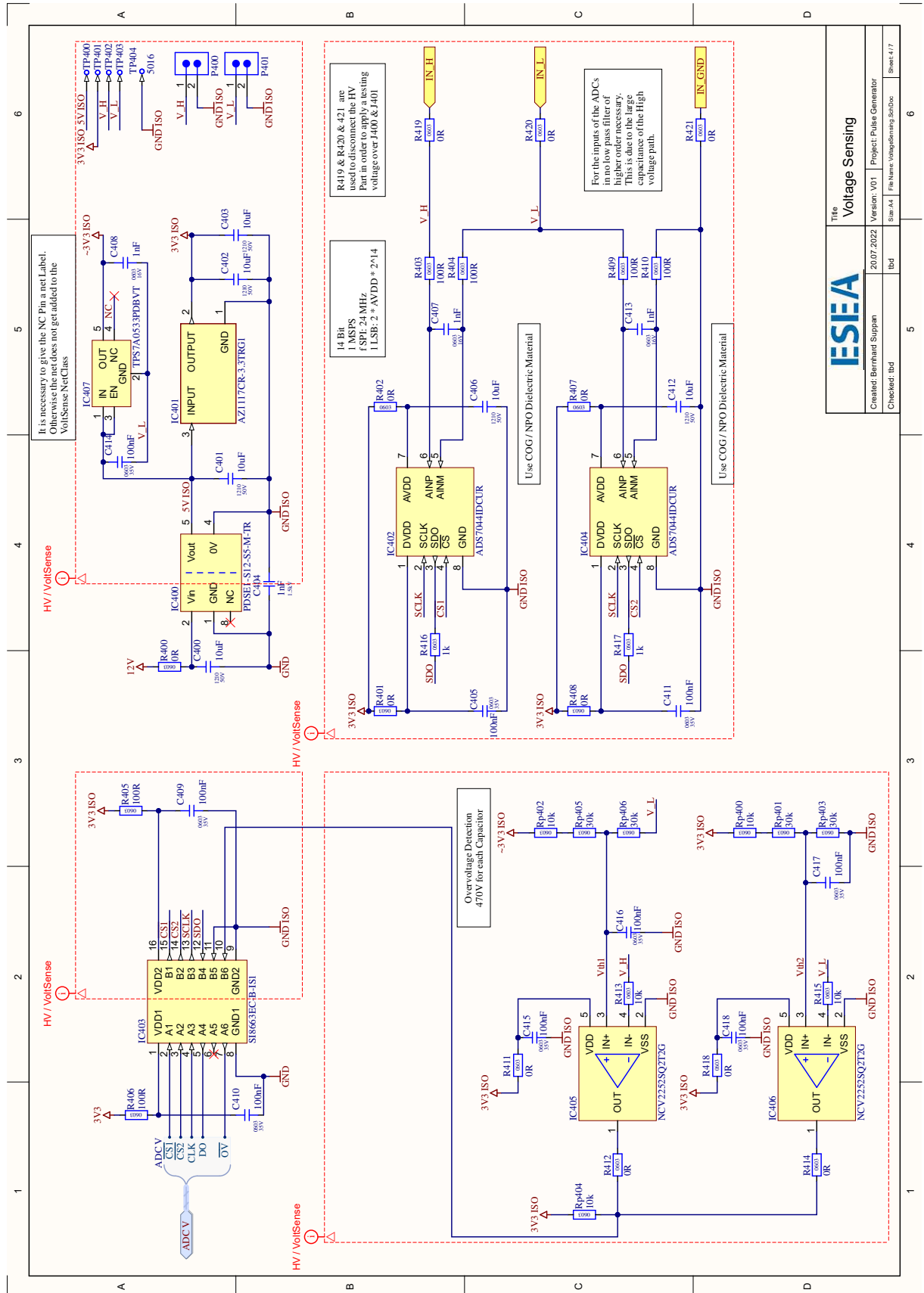**Figure B.4:** Schematic of the main pcb - Power Supply.

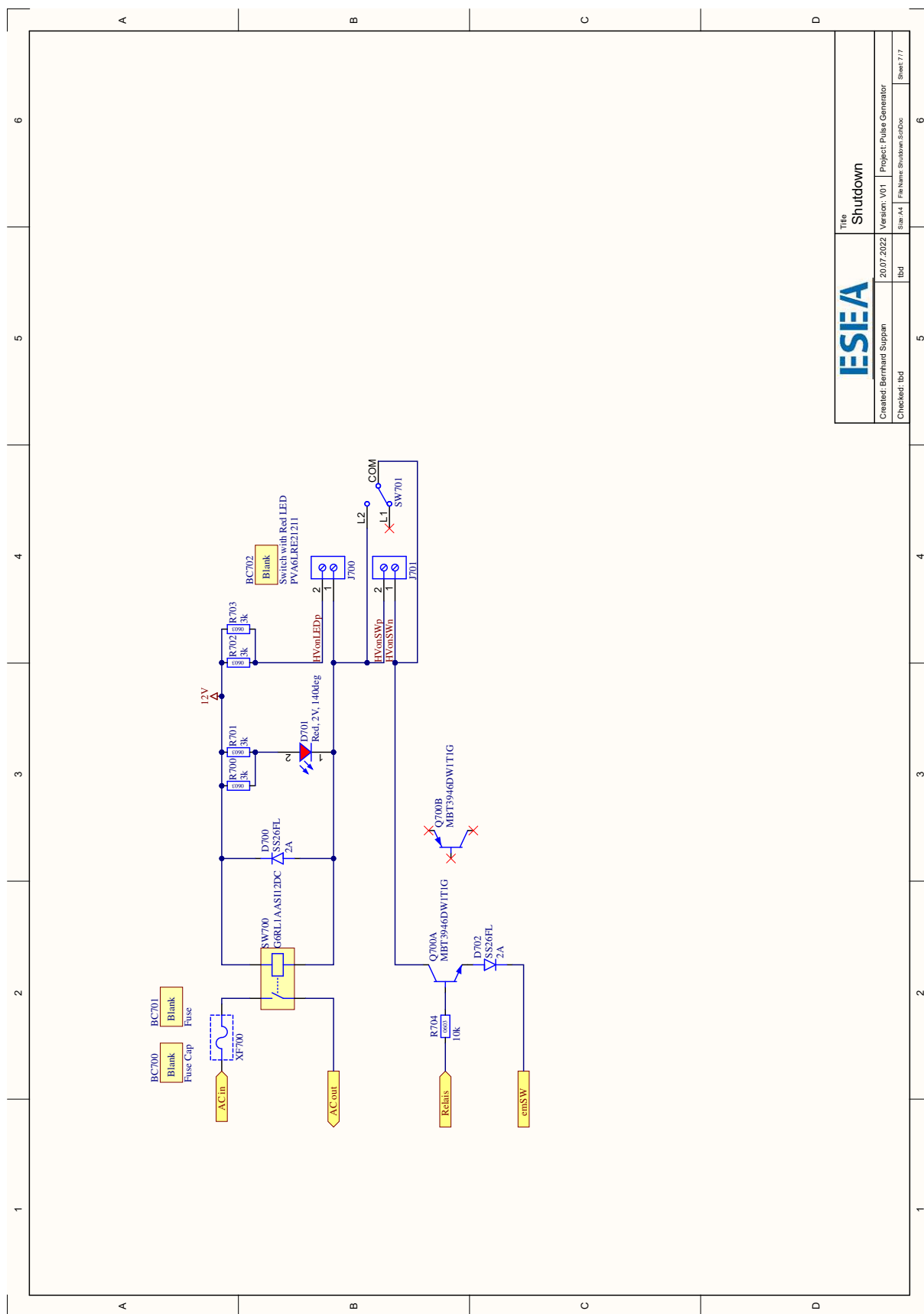**Figure B.5:** Schematic of the main pcb - Voltage Sensing.

Figure B.6: Schematic of the main pcb - Micro-Controller.

Figure B.7: Schematic of the main pcb - High Voltage Path.

Figure B.8: Schematic of the main pcb - Shutdown Circuit.

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[2] Oleg Sivkov, Martin Novak, and Jaroslav Novak. Comparison between si igbt and sic mosfet inverters for ac motor drive. In *2018 18th International Conference on Mechatronics - Mechatronika (ME)*, pages 1–5, 2018.

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[5] M. Chinthavali, P. Otaduy, and B. Ozpineci. Comparison of si and sic inverters for ipm traction drive. In *2010 IEEE Energy Conversion Congress and Exposition*, pages 3360–3365, 2010.

[6] Murata Power Solutions. Gate drive application notes, 3 2023. `https://www.murata.com/-/media/webrenewal/products/power/appnote/gdan-01.ashx?la=en-gb&cvid=20201014090811000000`.