Master Thesis

Integration of Ferroelectric Dielectrics in Reconfigurable Field-effect Transistors

submitted in partial fulfillment
of the requirements of the degree of
Master of Science

at Technische Universität Wien
Institute of Solid State Electronics

under supervision of
Univ.Prof. Dipl.Ing. Univ. Dr.-Ing. Walter Michael Weber
and
Univ.Ass. Dr.techn. Daniele Nazzari

by
Dominik Mayr, BSc
Student ID 01525865

Vienna, October 2023

Statutory Declaration

I declare, that I have authored the present work independently according to the code of conduct, that I have not used other than the declared sources and that I have explicitly marked all material quoted either literally or by content from the used sources. This work was not yet submitted to any examination procedure neither in Austria, nor in any other country.

Erklärung zur Verfassung der Arbeit

Hiermit erkläre ich, dass die vorliegende Arbeit gemäß dem Code of Conduct – Regeln zur Sicherung guter wissenschaftlicher Praxis – ohne unzulässige Hilfe Dritter und ohne Benutzung anderer als der angegebenen Hilfsmittel, angefertigt wurde. Die aus anderen Quellen direkt oder indirekt übernommenen Daten und Konzepte sind unter Angabe der Quelle gekennzeichnet. Die Arbeit wurde bisher weder im In- noch im Ausland in gleicher oder in ähnlicher Form in anderen Prüfungsverfahren vorgelegt.

Vienna, October 2023 .....

Dominik Mayr

Abstract

With the advent of Artificial Intelligence (AI) and Internet of Things (IoT), the demand for an ever-increasing computational power while simultaneously keeping a low-energy consumption has been joined by additional challenges related to memory-logic integration. Scaling in the "More-Moore" fashion was sufficient to overcome the former until the end of the 20th century, to be followed by the "More-than-Moore" approach based on functional diversification, leading to novel device concepts such as the reconfigurable field-effect transistor (RFET). This allows for switching between n-type and p-type operations during runtime. To cope with the unabated growth of required storage, ferroelectric memories based on HfO_2 are gaining importance due to their excellent scalability and already good endurance and retention properties. Therefore, a combination of both technologies is suitable, leading to concepts such as Logic-in-Memory (LiM) and new computer architectures like neuromorphic computing to overcome the von-Neumann bottleneck.

With this in consideration, the RFET concept has been extended in this thesis by integrating a ferroelectric layer of hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$, HZO) to form a Fe-RFET. To accomplish this, nanosheets were patterned on a silicon-on-insulator (SOI) substrate. Two Schottky barriers, which form a metal-semiconductor-metal heterostructure, are essential to its unique functionality and are achieved by thermally activated diffusion of aluminum (Al) into the silicon (Si) nanosheet channel. Based on extensive studies of the temperature profile for the ferroelectric orthorhombic phase, analysis of different top-gate materials and optimization of the interface layer (IL) as a suitable passivation layer to reduce leakage currents and trapping, four samples have been fabricated by iteratively adjusting the fabrication steps. This involved evaluating the intended ferroelectric effect through capacitive-voltage (C-V) and current-voltage (I-V) characterizations, confirming the desired behavior.

It has been observed that the chemically formed SiO_2, in contrast to the comparatively thick thermal oxide, is excellent for the fabrication of interfaces with low trap density, and beneficial for the ferroelectric behavior to overcome detrimental charge trapping effects. Besides, palladium (Pd) was proven to be a suitable alternative to the commonly used TiN electrodes, even resulting in a higher yield of functional devices in this work. Furthermore, the incorporation of an additional ferroelectric gate layer for already established device processes resulted in insignificant hysteresis with excellent sub-threshold slopes of up to 63 mV/dec. Nevertheless, due to the fixed charges induced by HZO, an asymmetry in the behavior (p/n ratio) occurs, which needs to be addressed by further optimization. Decent results were achieved during the measured retention and number of switches for endurance. Thus, this study provides a proof-of-concept for the realization of Fe-RFETs based on the integration of HZO onto the already versatile Al-Si-Al platform. By using the manufactured devices in applications ranging from non-volatile memory (NVM) to adaptive or self-learning circuits, it provides a preliminary way to meet the technical challenges of the present and the future.

Kurzfassung

Mit dem Aufkommen von künstlicher Intelligenz (KI) und dem Internet der Dinge (IoT) ergeben sich zusätzliche Herausforderungen im Hinblick auf die Integration von Speicher und Logik, die eine erhöhte Rechenleistung bei gleichzeitig niedrigem Energieverbrauch erfordern. Zur Bewältigung dieser Herausforderungen konnte die Skalierung nach dem "More-Moore"-Prinzip bis zum Ende des 20. Jahrhunderts herangezogen werden. Mit dem "More-than-Moore"-Ansatz - basierend auf funktionaler Diversifizierung - welcher zu neuartigen Bauelementkonzepten wie dem rekonfigurierbaren Feldeffekttransistor (RFET) führte, konnte dieser Trend fortgesetzt werden. Der RFET ermöglicht es dabei, während der Laufzeit zwischen n-Typ- und p-Typ-Betrieb zu wechseln. Um dem steigenden Bedarf an Speicherkapazität gerecht zu werden, erlangen ferroelektrische Speicher auf der Basis von HfO_2 aufgrund ihrer hervorragenden Skalierbarkeit sowie deren guten Speichereigenschaften zunehmend an Bedeutung. Daher bietet sich eine Kombination beider Technologien an, die zu Konzepten wie Logic-in-Memory (LiM) und neuen Computerarchitekturen wie dem neuromorphen Computing führen, um den von-Neumann-Bottleneck zu vermeiden.

In dieser Arbeit wurde das RFET-Konzept durch die Integration einer ferroelektrischen Schicht aus Hafnium-Zirkonium-Oxid ($Hf_{0.5}Zr_{0.5}O_2$, HZO) erweitert, um einen Fe-RFET zu bilden. Zu diesem Zweck wurden Nanosheets aus einem silicon-on-insulator (SOI)-Substrat strukturiert. Wesentlich für die besondere Funktionalität sind zwei Schottky-Barrieren, die eine Metall-Halbleiter-Metall-Heterostruktur bilden, welche durch thermisch aktivierte Diffusion von Aluminium (Al) in die Silizium (Si) Nanostruktur erzielt werden. Auf Grundlage umfangreicher Untersuchungen des Temperaturprofils für die ferroelektrische orthorhombische Phase, der Analyse unterschiedlicher Top-Gate-Materialien und der Optimierung der Grenzflächenschicht als geeignete Passivierungsschicht zur Verringerung von Leckströmen und Störstellen, wurden vier Proben, durch iterative Anpassung der Herstellungsschritte, hergestellt. Dies beinhaltete die Evaluierung des angestrebten ferroelektrischen Effekts durch Kapazität-Spannungs- (C-V) und Strom-Spannungs-Charakterisierungen (I-V).

Es konnte gezeigt werden, dass das chemisch hergestellte SiO_2 im Gegensatz zum vergleichsweise dicken thermischen Oxid hervorragend zur Realisierung von Grenzflächen mit geringer Trap-Dichte geeignet ist und sich somit positiv auf das ferroelektrische Verhalten auswirkt. Darüber hinaus hat sich Palladium (Pd) als geeignete Alternative zu den üblicherweise verwendeten TiN-Elektroden erwiesen, welches in dieser Arbeit zu einer höheren Ausbeute an funktionsfähigen Bauelementen führte. Zudem resultierte die Integration einer zusätzlichen ferroelektrischen Schicht in bereits etablierte Herstellungsprozesse zu einer vernachlässigbaren Hysterese mit exzellenten Unterschwellensteilheiten von bis zu 63 mV/dek. Nichtsdestotrotz kommt es zur Asymmetrie des p/n-Betriebs aufgrund induzierter fixer Ladungsbeiträge durch HZO, die durch weitere Optimierungen angepasst werden muss.

In Bezug auf die gemessene Retention sowie die Endurance, zeigten sich gute Ergebnisse. Die vorliegende Forschungsarbeit liefert somit einen Proof-of-Concept für die Realisierung von Fe-RFETs auf der Basis der Integration von HZO in die bereits vielseitig einsetzbare Al-Si-Al-Plattform. Durch Einsatz der hergestellten Bauelemente in Anwendungen, welche von nichtflüchtigen Speichermedien (NVM) bis hin zu adaptiven oder selbstlernenden Schaltkreisen reichen, wird ein vorläufigen Weg eröffnet, den technischen Herausforderungen der Gegenwart und der Zukunft zu begegnen.

Acknowledgement

The journey to the completion of this thesis has led me through challenges, insights and quite a few great social acquaintances, thus in this section I would like to thank the following people for everything imaginable and would like to preface this acknowledgment with a quote from Issac Newton:

If I have seen further it is by standing on the shoulders of Giants.

Walter M. Weber
With his student-orientation, he knows how to ask the right questions to get the best out of the collaboration on the one hand, and on the other hand, to successfully pass on this extensive knowledge in his field. Thank you for letting me be part of your team. This means a lot to me.

Daniele Nazzari
A brilliant physicist with passion for his field of study. I cannot thank him enough for his active support during the fabrication and characterization of the devices. I was also able to have a relaxed and enjoyable time with him at all times during this work without losing track of focus.

Lukas Wind and Masiar Sistani
Special thanks also goes to Lukas Wind for his support in the cleanroom during the fabrication of several process steps, the characterization and evaluation. Without him, this work would not have been feasible in this sense.

I would like to thank Masiar Sistani for his open personality, with which he always inspires students to have a scientific chat, visit his lectures or even do a thesis at the Institute of Solid State Electronics, as it was the case for me. I see you as a mentor and wish you much success on your further career.

Emerging Nanoelectronic Devices Group
Many thanks to the entire team of lovely people with whom inspiring discussions but also amusing conversations were held.

FKE and ZMNS
For providing the cleanrooms and other necessary facilities, without which the fabrication and measurement of this thesis would not have been feasible.

My family
With sincere gratitude for your vigorous support in all aspects of my lifelong journey, I thank you. Your encouragement has enabled me to achieve my goal of successfully completing my studies. Words cannot express how grateful I am for your kindness and affection.

My Friends
I would like to express my appreciation to all of you for the deep relationship and great friendship that has led to many wonderful memories. Cheers to many more years together! A special thanks to Hannah, Peter and Raphael for their unconditional support in all situations of life and the countless unforgettable moments.

My Partner
It means a lot to me to know that she does not have the slightest doubt in my ability to accomplish the things I want to do. Her words provided me with a lot of confidence, encouragement, patience, and the right advice for a creative break or an empowering quality-time during these sometimes challenging periods. I truly appreciate that!

Lastly, I would like to extend my thanks to all the others who have not been mentioned.

Contents

Chapter 1

Introduction

The semiconductor industry has become an integral part of the society we live in today. Beginning with the invention of the first transistor [1] in 1947 through the outstanding research of John Bardeen and Walter Brattain in the group led by William Shockley at Bell Laboratories, it has grown over the last 70 decades into a $646 million [2] industry by 2022. This achievement is mainly attributable to Gordon Moore's (Intel) economically-motivated approach of exponentially increasing density of electronic circuits by scaling down the related dimensions, manifested in the so-called "Moore's Law" [3], with which he immortalized himself in history. This scaling approach, according to Dennard [4], has been successfully applied to the complementary metal-oxide-semiconductor (CMOS) process (both n-MOS FET and p-MOS FET) as an industry standard to meet the ever-increasing demand for computational performance until about the year 2000. Nonetheless, geometric (or classical) scaling, also known as "More-Moore", led to the appearance of short-channel effects due to fundamental scaling limits, as well as to higher leakage current due to the reduction in oxide-layer thickness [5, 6]. The IEEE International Roadmap for Devices and Systems (IRDS) has gathered predictions for future solutions to these arising challenges [7]. Following this, there was also a transition to the "More-than-Moore" paradigm, which, according to Salahuddin et. al. [5], is classified as the second scaling era, under the term equivalent or effective scaling. This approach involves functional diversification enabled by the introduction of new material combinations, like silicon-germanium (Si-Ge), or by tuning the material properties through processes like strain engineering. Moreover, materials with increased dielectric constants have been employed to achieve a greater equivalent oxide thickness (EOT), such as the inclusion of hafnium oxide (HfO_2) in the Intel Penryn processor [8], which proves to be fully CMOS compatible. In this era, novel device concepts such as the non-planar fin field-effect transistor (FinFET) or the reconfigurable field-effect transistor (RFET) [9, 10] - which will be discussed in this thesis - have also been introduced.

An RFET consists of two metal-semiconductor Schottky junctions, with which, depending on the voltage condition applied to the gates, the unique property to switch between n- or p-type characteristic during run-time is enabled. This approach is particularly advantageous since it does not require any doping, making it highly favorable for nanofabrication [9, 11, 12]. To continue unabated scaling, Salahuddin et. al. [5] predict the so-called hyper-scale era for the time after 2025, in which topics such as Negative Capacitance (NC), enabling Beyond-Boltzmann switching dynamics, as well as Non-Volatile Memory (NVM) all the way to Logic-in-Memory (LiM) concepts will arise to offer a solution to the von-Neumann bottleneck (see also "memory wall" [13]) in classical computer architecture. These concepts share a common basis in the integration of an additional ferroelectric layer having two distinctive (switchable) polarization states. All of these concepts and more are essential to fulfill the demands of modern society with respect to areas such as Internet of Things (IoT), autonomous driving, big data related to the increased need for data storage [14], AI technology driven by the development of machine learning and deep learning [15] related to the Fourth Industrial Revolution (4IR or Industry 4.0).

For years, ferroelectric materials have been used in a variety of applications such as actuators and sensors. Conventional ferroelectrics with perovskite structure (e.g. $Pb(Zr, Ti)O_3$ (PZT)) are still the most common materials for most applications, but they face significant limitations in high-density integration due to the size effect of ferroelectricity and incompatibility with complementary metal-oxide-semiconductor technology [14, 16, 17]. In the early 21st century, researchers focused extensively on HfO_2- and ZrO_2-based thin films in an effort to find a suitable high-k replacement for integrated dielectrics [14, 16, 18–20]. The discovery of ferroelectricity in Si-doped HfO_2 in 2006, along with the subsequent publication by Böschke et al. [21], has changed the situation of perovskites as the leading class. Consequently, ferroelectric research has been mainly focused on HfO_2-based ferroelectric thin films. In this thesis, zirconium (Zr)-doped HfO_2 or hafnium zirconium oxide ($Hf_{1-x}Zr_xO_2$) - HZO for short - with an equal concentration of Hf and Zr (x = 0.5) is used because it exhibits the strongest ferroelectric polarization, alongside with the possibility to use the Atomic Layer Deposition (ALD) process, allowing for the creation of ultra-thin films with exceptional scalability [20].

In this context, this thesis combines the novel transistor concept of the RFET with the benefits of the ferroelectric material combination HZO in a so-called Fe-RFET. Fabrication and characterization of four different samples based on a silicon-on-insulator (SOI) substrate and the monolithic and crystalline aluminum-silicon (Al-Si) heterostructures [22], which are crucial for the functionality, are performed. In addition to methods of transistor characterization, this study utilizes capacitive-voltage (C-V) and pulse measurements to investigate the ferroelectric behavior.

The primary goal is to determine if the selected HZO layer integrated into the RFET structure is appropriate for realizing Fe-RFET devices and assess the strength of the established characteristics of these devices with respect to their switching capability.

This thesis consists of four additional chapters, namely Theory, Experimental Techniques, Results and Discussion, as well as Conclusion and Outlook. Chapter 2 (Theory) provides an overview of ferroelectric materials and their unique properties, particularly related to HZO. Additionally, a detailed explanation of the metal-semiconductor transition and its formation is given, as well as a comprehensive description of the RFET up to the integration into this concept towards the goal of achieving the Fe-RFET. In Chapter 3 of this study, various experimental approaches for the electrical and structural characterization of the ferroelectric layers are described. Moreover, the necessary fabrication steps to obtain a Fe-RFET are explained, followed by a description of the electrical characterization of its ferroelectric behavior. Chapter 4 gives the results in relation to the previously presented methods and discusses their meaning. Finally, in Chapter 5, the thesis is concluded with a summary of the results and an outlook on future extensions.

Chapter 2

Theory

Within this Chapter, the focus is on the basic theory of this thesis. It is therefore divided into four sections, the first of which classifies ferroelectric materials, followed by a brief introduction to the history of those materials and their characteristics with respect to spontaneous polarization. Based on properties, composition ratio, creation and formation of the desired crystal structure, the key material of this work, hafnium zirconium oxide ($Hf_{1-x}Zr_xO_2$), HZO for short, is discussed. In addition, the atomic layer deposition (ALD) is explained, as it was chosen as the manufacturing method for the HZO layers in this thesis.

The heterostructure between aluminum and silicon and the respective materials themselves are discussed in section two. Clarification is provided on how this transition occurs, which behavior this metal-semiconductor structure exhibits and its potential use in electrical devices.

Subsequently, in the third section, "Reconfigurable Field-Effect Transistor (RFET)", the concept is introduced by implementation of two individual Schottky barriers that occur due to the aforementioned transition from metal to semiconductor, and the operation of such a device is explained, followed by highlighting the advantages over conventional FETs.

Section four addresses the ferroelectric RFET (Fe-RFET) in general, before the benefits and advanced applications of integrating ferroelectric layers - such as HZO - into the RFET design conclude this Chapter.

2.1 Ferroelectric Materials

Materials with the ability to exhibit spontaneous electric polarization in the absence of an electric field and in addition demonstrate reversibility of the polarization state through the application of an external electric field, are called ferroelectrics [23, 24].

2.1.1 Classification and Characteristics

The structural symmetry of lattice structures - described by Bravais unit cell - provides information about its physical properties. As a result, materials exhibit, for example, dielectric, elastic, piezoelectric, pyroelectric, ferroelectric and other optical properties [25]. Therefore, as a starting point for the categorization of ferroelectric materials, the crystal classes are used, which are schematically outlined in Figure 2.1.

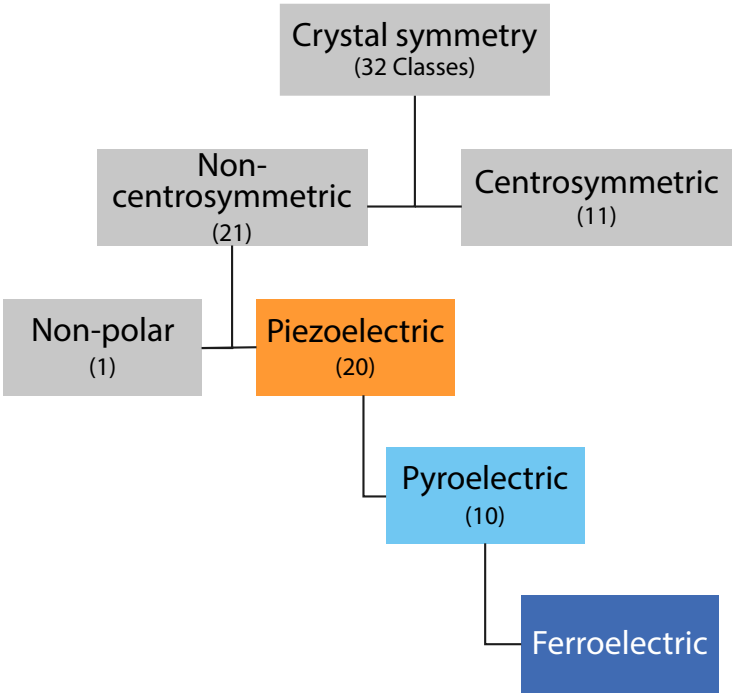

Figure 2.1: *Classification of piezoelectric, pyroelectric and ferroelectric materials within the 32 point groups. Adapted from [26]*

In general all crystal structures can be categorized into 32 crystal symmetries given by the point group theory. Eleven of them possess a center of symmetry and the remaining 21 are non-centrosymmetric (acentric) which means that they lack in inversion symmetry. Center of symmetry in a crystal structure means that for every atom in the structure there is a point in the unit cell, through which inversion will bring one to the same type of atom [24].

Of these, only one group does not exhibit piezoelectric behavior. The direct piezoelectric effect entails a change in the dipole moment, leading to a charge separation at the crystal faces because of mechanical stress. On the other hand, the reverse piezoelectric effect causes the crystal to expand when an electric field is applied [24].

Ten of these crystal structures belong to a subgroup called polar, distinguished by their unique axis of symmetry. Polar crystals exhibit both piezoelectricity, due to the mentioned asymmetry, and pyroelectricity, a charge separation caused by temperature change as suggested by its name. Their special unit cell results in intrinsic dielectric polarization through the influence of voltage or temperature change, commonly known as spontaneous polarization [24].

From these point groups, seven basic crystal systems can be further distinguished, which are listed in ascending order of symmetry as triclinic, monoclinic, orthorhombic, tetragonal, rhombohedral (trigonal), hexagonal, and cubic [23].

Ferroelectrics are related to piezoelectrics and pyroelectrics due to their unique symmetry conditions [23]. However, it is crucial to note the fundamental distinction of the spontaneous polarization in relation to the pyroelectric and ferroelectric behavior. In the ferroelectric effect, the direction and magnitude of the spontaneous polarization persist even after the field is removed. Moreover, applying an external voltage can reverse the polarization state and maintain it in the respective direction. In contrast, in the pyroelectric effect, the spontaneous polarization returns to its zero field value after the field is removed [24]. Ferroelectrics exhibit a hysteresis that results in two states of polarization. The theoretical origin of this behavior will be discussed with reference to Landau theory [27] in the Subsection 2.1.2.

Here, the properties of dielectric hysteresis as a cause of ferroelectricity are discussed for completeness. When a material is subjected to an external electric field, it results in an induced polarization (P) that is linearly proportional to the strength of the applied field (E) [23, 26]. This phenomenon is known as dielectric polarization and is expressed using the dimensionless electric susceptibility χ_e, which describes the degree of polarization of the material, and the permittivity of free space ε_0 [F/m], also known as the dielectric constant:

$$P = \epsilon_0 \chi_e E \; [C/m^2] \tag{2.1}$$

The electrical susceptibility is related to the relative permittivity, also known as the dielectric constant, through the equation:

$$\chi_e = \epsilon_r - 1 \tag{2.2}$$

The paraelectric state occurs above the Curie temperature T_C and is characterized by a nonlinear polarization in response to an external electric field [23]. If the material

is ferroelectric, spontaneous polarization also occurs alongside the non-linearity and the remanent polarization is reversible. Due to the possibility of switching the polarization with a sufficiently strong electric field, the polarization curve depends on both the currently applied electric field and the previous history, leading to a hysteresis loop as it is depicted in Figure 2.2.

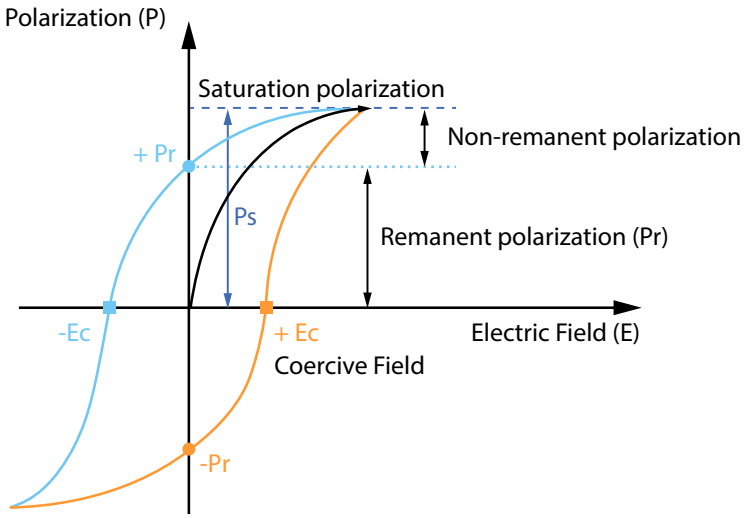

Figure 2.2: *Ferroelectric hysteresis with the highlighted saturation- P_s and remanent polarization P_r as well as the coercive field E_c. Adapted from [28]*

Starting with the increase of the electric field, the polarization also increases by aligning the different dipolar regions until the saturation point is reached, which describes the saturation value of the spontaneous polarization (P_s) by extrapolating this line to the ordinate. A continued increase of the electric field from this point will only result in an increase due to the relative dielectric constant of the material, since the slope of the P/E-curve for a linear dielectric is equal to the permittivity. The material also retains a remanent polarization (P_r) as the field is reduced to zero, which is typically slightly lower than P_s. The coercivity (E_c) is the required negative field to eliminate polarization. Since it exhibits hysteresis, a further decrease in the field leads to an inverse saturation polarization (P_s), and eventually, in the absence of any field, a negative remanent polarization (P_r) persists. The existence of ferroelectric domains rests on the premise that the polarization in distinct areas of a given crystal can be oriented in different directions [24].

The process of domain reversal under the influence of an external field is illustrated in Figure 2.3. The three phases of domain reversal consist of

1. nucleation (fast)

2. forward growth (fast) and

3. sideways growth (slow).

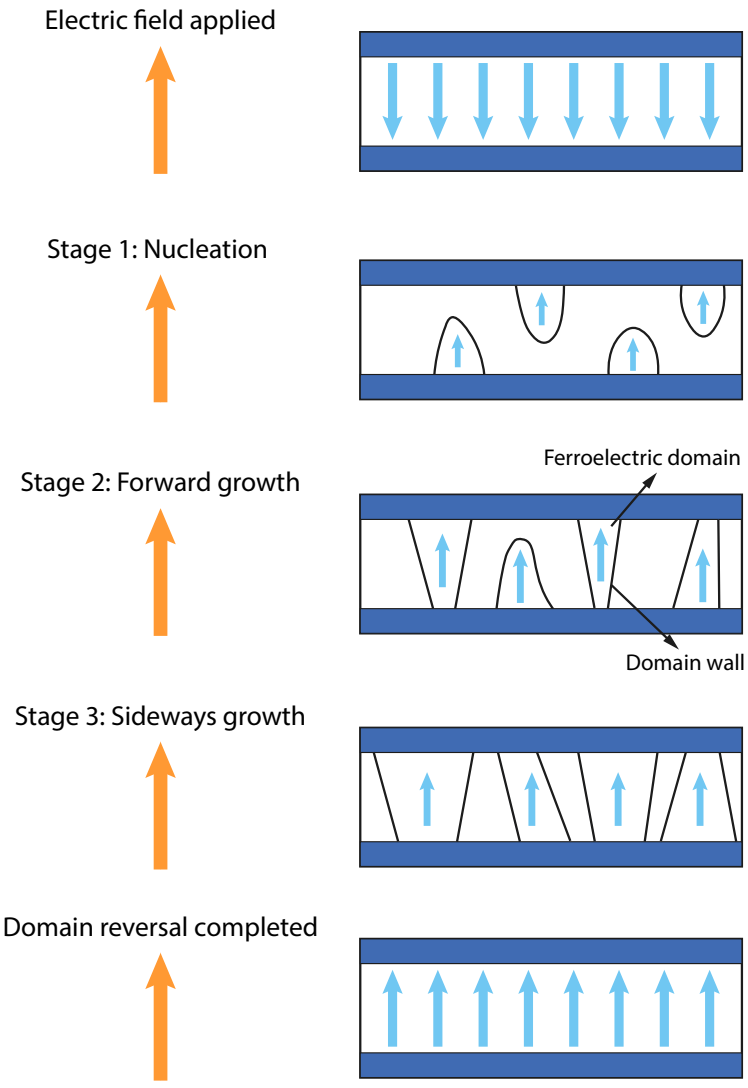

Figure 2.3: *Three phase polarization reversal sequence. Adapted from [29]*

This switchable polarization property has significant practical applications, such as in non-volatile memory. See Subsection 2.4.2 for details on applications.

As mentioned in the introduction, the need to integrate ferroelectric materials into a semiconductor manufacturing process is inevitable for at least one of the desired beyond CMOS progresses in IRDS [7]. Therefore, the history of ferroelectric materials will be briefly outlined here in order to have an understanding of how the material used in this work, namely HZO, has originated.

In analogy to ferromagnetic materials with their property of exhibiting a spontaneous magnetization and similarities such as hysteresis loops, Curie temperature (T_C), these materials are called ferroelectrics [26]. This designation was first used by Erwin Schrödinger in 1912 in german as "ferroelektrisch" when he proposed the concept of two spontaneous polarization states P_s [17, 30]. Ferro as prefix, from Latin *ferrum* commonly known as iron (Fe), comes from its similarities as mentioned above despite the fact that most ferroelectric materials do not contain iron [23].

In 1920, while studying Rochelle salt ($NaKC_4H_4O_6 \cdot 4H_2O$), Vasalek [31] discovered the first ferroelectric material. However, the ferroelectric properties of Rochelle salt were found to be significantly impacted by environmental factors, such as humidity [17].

The discovery of the second ferroelectric material, KH_2PO_4 (KDP), was made by Busch et al. [32] in 1935. This material showed improved chemical stability, and subsequently other ferroelectric crystals with similar structures were discovered. Nevertheless, these materials still have a Curie temperature below room temperature, which made them unsuitable for practical applications [17].

A decade later, in 1945, the perovskite structure $BaTiO_3$ [33] (BTO) proved to be a significant material breakthrough for practical ferroelectric applications. BTO possesses stable properties and became a popular ferroelectric material for applications with high permittivity (even higher than 1000) or piezoelectricity [17, 34].

Perovskites are determined by the general chemical formula XYO_3, in which X and Y represent different cations. The Y cations have two stable positions below the Curie temperature, which deviate from the center of the unit cell along the c-axis of the tetragonal phase. This results in two polarization states P_s [17].

Subsequently, the theory of ferroelectricity was described using a phenomenological approach developed by Landau, Ginzburg, and Devonshire. A brief discussion of Landau's approach [27] is presented in the following Subsection 2.1.2.

$Pb(Zr, Ti)O_3$ (PZT) was one of the most significant perovskite structures discovered in 1954 [35, 36]. Despite the environmental concerns related to Pb, PZT remains an essential industrial material [17]. The Zr and Ti-based oxides offer flexibility and exhibit exceptional ferroelectric properties, particularly at the morphotropic phase boundary linking the tetragonal and rhombohedral ferroelectric phases [34]. However, they are not the best choice for memory applications due to fatigue, which refers to the decline of switchable polarization with increasing read and write cycles [34].

In addition to the previously mentioned inorganic ferroelectrics, there was a detailed study of organic ferroelectric materials in the 1980s. The most frequently utilized material is poly(vinylidene fluoride trifluoroethylene) (PVDF-TrFE) [37], along with its variations

[17]. Jonas Alexander Hafner [38] is currently conducting research on ferroelectric MEMS composed of the copolymer of vinylidene fluoride and trifluoroethylene (P(VDF-TrFE)) as part of his PhD studies at TU Wien.

The 1990s marked the advent of layered perovskites, featuring oxide interlayers sandwiched between perovskite layers. Examples include strontium bismuth tantalate ($Sr_2Bi_2TaO_9$ or SBT), which proved to be a viable solution to the fatigue observed in unlayered perovskites [34]. However, the more intricate crystal structure of layered perovskites made their integration into semiconductor manufacturing processes even more difficult than for PZT.

Back in 2011, Böschke et al. were the first group to report on ferroelectricity in silicon-doped hafnium oxide [21], demonstrating on the one hand the integration into existing thin film semiconductor processes to further progress the more than Moore approach up to a thickness below 5 nm shown at that point [34]. The structure based on a fluorite crystal structure, to be precise hafnium zirconium oxide (HZO) will be discussed in more detail in Subsection 2.1.3, as it is the material chosen for this thesis.

AlScN and two-dimensional (2D) ferroelectric materials have been added as recent materials of interest in 2019 and 2023, respectively, as they have promising potential applications in memory and computing [35].

2.1.2 Thermodynamic Perspective

Here, the basic phenomenological thermodynamic theory is briefly explained to facilitate comprehension of the transition from a paraelectric to a ferroelectric phase. Extensions to the thermodynamic theory, which are based on the classic papers of Landau [27] dated 1937, as well as those by Devonshire [39] and Ginzburg [40], provide detailed treatments that would go beyond the scope of this work.

Landau theory is a symmetry-based analysis of the equilibrium behavior near a phase transition. It states that a system cannot change smoothly between two phases of different symmetry. In the transition between liquid and gaseous states, it is only possible to assume a continuous path around a critical point of first order because no symmetry change takes place [41]. In Landau theory, the ferroelectric phase transition (lower symmetric phase) is characterized by a small distortion of the structure of the paraelectric phase (higher symmetric phase) [42].

The following description is based on the description given by Jon F. Ihlefeld in the first Chapter of the book "Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices" called "Fundamentals of Ferroelectric and Piezoelectric Properties" [43]. The thermodynamic treatment used in this example refers to the simplest case of zero stress and the free energy in terms of temperature and polarization. The Gibbs energy (symbolized by F) can be expressed as a Taylor expansion using the polarization order parameter (P)

because of the minor structural change [23].

$$F = \left(\frac{\alpha}{2}\right) P^2 + \left(\frac{\beta}{4}\right) P^4 + \left(\frac{\gamma}{6}\right) P^6 - EP \tag{2.3}$$

Where F represents the Gibbs free energy, P the polarization, α the temperature dependent coefficient, β and γ the temperature independent coefficients. By finding the minimum value of the free energy with respect to the polarization, the following expression is obtained for the electric field parallel to the polarization:

$$\frac{\partial F}{\partial P} = 0 \rightarrow E = \alpha P + \beta P^3 + \gamma P^5 \tag{2.4}$$

For stability considerations, these equations can be utilized by selecting either positive or negative values for α and positive values for both β and γ. This leads to two distinct cases, as demonstrated in Figure 2.4 (a).

- $\alpha > 0$: A single minimum is observed for $P = 0$, which means that there is no spontaneous polarization.
- $\alpha < 0$: Two minima are observed corresponding to the equilibrium positions that yield the spontaneous polarizations of $P = +P_S$ and $P = -P_S$.

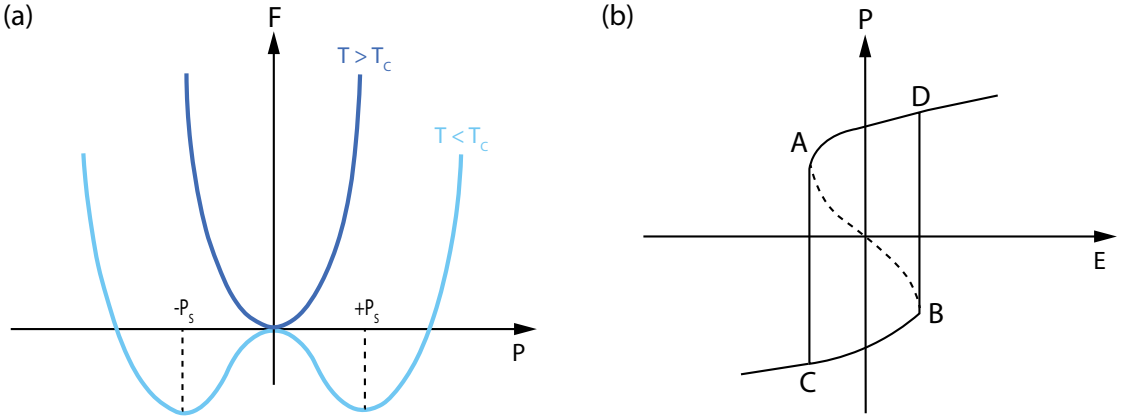

Figure 2.4: *(a) Polarization dependence of free energy is presented for a second order ferroelectric phase transition. At temperatures above T_C, α is positive, and paraelectric behavior predominates with the lowest free energy state for zero polarization. At temperatures below T_C, α is negative, and there are two non-zero lowest free energy states. Adapted from [42] (b) Polarization curve below T_C. The path C-B-D-A is observed in conventional hysteresis measurements. An unstable negative permittivity path is given by C-B-A-D. Adapted from [43]*

In order to calculate the spontaneous polarizations, it is necessary to set $E = 0$ and disregard the small fifth-order term contribution.

$$P^2 = -\frac{\alpha}{\beta} \tag{2.5}$$

Due to the temperature dependence of α, the electric field E and thus P varies uniformly with temperature for negative values of α. As a result, a second-order phase transition is described from a non-polar to a polar state.

α corresponds to the inverse dielectric susceptibility $\frac{1}{\chi}$ in the case of the non-polar phase, which has a Curie-Weiss temperature behavior:

$$\alpha = \alpha_0(T - T_0) \text{ with } \alpha_0 > 0 \tag{2.6}$$

For completeness it must be mentioned that in the case of a second-order transition the Curie-Weiss temperature T_0, which defines the maximum of the dielectric constant, is equal to the Curie temperature T_C described here. Nonetheless, in the case of a first-order transition, T_C may be 10 K higher than T_0 [44]. Therefore, in the following T_0 is to be considered equivalent to T_C.

Similarly, the temperature dependence of the spontaneous polarization of the polar phase can be determined using this approach.

$$P^2 = \frac{\alpha_0(T_0 - T)}{\beta} \tag{2.7}$$

The inverse susceptibility is derived from E with respect to P as:

$$\frac{\partial E}{\partial P} = \frac{1}{\chi} = 2\alpha_0(T_0 - T) \tag{2.8}$$

From this equation, the temperature dependence of the relative permittivity below T_0 can be determined.

$$\epsilon_r = \frac{1}{2\alpha_0(T_0 - T)} + 1 \tag{2.9}$$

In addition to the two stable polarization states at low fields, Figure 2.4 (b) indicates that another important conclusion can be made. The dashed line shows a region of negative slope given by the proportional relation ϵ_r to dP/dE, i.e. a region of negative permittivity. Although this region is unstable, it presents intriguing opportunities for application, as discussed in Subsection 2.4.2.2.

2.1.3 Ferroelectricity of Hafnium Zirconium Oxide (HZO) thin films

Both HfO_2 and ZrO_2 serve as gate oxide (high-k) layers for metal oxide semiconductor field effect transistors (MOSFETs) and as dielectric layers in dynamic random access memories (DRAMs) for commercial products [14]. Materials with a dielectric constant greater than 7 are classified by Wallace [45] as high-k dielectrics, the exact values for which can be read in the Table 2.2. One noteworthy case is the integration of HfO_2 into the Intel Penryn processor [8], which demonstrates full CMOS compatibility. Additionally, HfO_2 finds its use in academia wherein it utilizes its high relative dielectric constant of approximately 25, facilitating the reduction of leakage currents and the shifting of the transfer characteristic due to the oxide charges (to positive threshold voltage for HfO_2 and ZrO_2 (negative fixed charges) and to the negative threshold voltage for SiN_x [46] (positive fixed charges)). For instance, to achieve balanced symmetry conditions between the n- and p-branches in an RFET structure, refer to the research conducted by Andreas Fuchsberger [47] using aluminum-silicon-germanium heterostructures.

While investigating improved thin films based on HfO_2, ferroelectric behavior was first unexpectedly discovered in 2007 by Böschke et al. at Qimonda (formerly Infineon) - a manufacturer of dynamic random access memories (DRAMs). This was subsequently verified by the Waser group in Aachen. Further experimentation was conducted at NaMLab and Fraunhofer CNT, with the results being published for the first time in 2011. Böschke et al. [21] reported evidence of the formation of a ferroelectric crystalline phase in SiO_2-doped HfO_2 thin films deposited using ALD [48]. Similar ferroelectric performance could be demonstrated with HZO [20, 43, 49, 50].

The scalability of materials with sufficient ferroelectric behavior and retention are two important factors for industrial applications.

Zirconium Doped Hafnium Oxide, Hafnium Zirconium Oxide or $Hf_{0.5}Zr_{0.5}O_2$ for short HZO is a fluorite crystal structure. This structure has the advantage over conventional ferroelectrics, such as the perovskite structure, of being able to meet the aforementioned needs. A comparative overview of the most important parameters can be found in Table 2.1.

Crystal structure	Perovskite	Fluorite
Dielectric constant ϵ_r [1]	100-200	19 - 70
Band-gap E_G $[eV]$	3-4	5.0 - 5.5
Coercive field E_C $[MV/cm]$	0.09	1-2
Polarization P $[\mu C/cm^2]$	10-95	12-45

Table 2.1: *Perovskite and fluorite-structured ferroelectrics: Comparison of crystal structures and properties. Source: [51]*

According to Ma et al. the low dielectric constant of HfO_2 based ferroelectrics compared

to perovskites offers an intrinsic advantage to improve the retention properties by reducing the depolarization field due to interfacial layers with low relative permittivity [14, 52].

Thin films, which are also necessary for 3-D structures, are difficult to achieve with PZT due to their multicomponent nature and large size of Pb [48]. Since HfO_2 and ZrO_2 are CMOS compatible, the same is true for the compound HZO. Ideal for this is the possibility to use the ALD process, which allows thin films for further down-scaling with uniform integration and thus high ferroelectricity even with thin films. In addition, the fluorite structure of HZO offers band gaps in the range of 5.0 - 5.5 eV [53] - with a large band offset to Si - which has the advantage of more effectively reducing the leakage current due to thermionic emission or tunneling at the same physical thickness [51] compared to perovskite ferroelectrics with 3 - 4 eV [48].

Due to the high coercive field of about 1 $MVcm^{-1}$, a suitable storage window can be achieved even for layer thicknesses of a few nanometers [53].

To understand the origin of these significant benefits of combining HfO_2 and ZrO_2 to form HZO, the properties are briefly discussed.

As a dopant for hafnium oxide - to realize a high-dielectric-constant phase at lower temperature - numerous elements such as Si, Zr, Y, Al, Gd, Sr, and La with varying concentrations have been reported, see [48]. Some dopants such as Si or Zr have the capability to induce a transition to a crystalline phase for a ferroelectric HfO_2 behavior. Zirconium, with a concentration of 50%, provides the highest ferroelectric polarization due to its very similar physical and chemical properties to those of Hf. Zr^{4+} and Hf^{4+} have ionic radii of 0.78 and 0.76 Å, respectively for a coordination number of 7 and electro-negativities of 1.22 and 1.23, respectively [14]. This approach offers the advantage of establishing a straightforward and feasible alternating deposition (ALD) process using HfO_2 and ZrO_2, as previously described. Other dopants are only stable at much lower doping concentrations below 20%, which makes it more difficult. In addition, it has been observed that relatively low processing temperatures of about 400 °C [54] can induce ferroelectric behavior [48].

Dielectric	SiO_2	HfO_2	ZrO_2	HZO
Dielectric constant ϵ_r [1]	3.9[1]	22-25[2]	22-24[2]	t (17-20), o ($\sim$ 30), m (35-40)[5]
Bandgap E_G $[eV]$	8.9-9.0[1]	5.5-6.0[2]	5.0-7.0[2]	5.4[6]
Breakdown strength E_{BD} $[MV/cm]$	10[3]	3.9-6.7[2]	3.3-5.7[2]	$\sim$ 4[7]

Table 2.2: *Comparison of various commonly used dielectrics with HZO in terms of dielectric constants, bandgaps and electrical breakdown strength. Source: [1][45],[2][55],[3][6],[4][56],[5][57],[6][58],[7][59]*

A continuous monoclinic solid solution with a fluorite-like structure is formed due to the correspondence between atomic radii and valence in the crystal structures of HfO_2 and ZrO_2 [14].

It should be noted that the dielectric constant of HZO has a large influence on the electrical breakdown as it is phase-dependent. The value of the m-phase is much lower than that of the o-phase and this results in a higher electric field at the m-phase compared to the average electric field. Note that the values listed in the Table 2.2 may vary depending on the crystalline structure of the dielectric.

HZO films can have multiple phase structures due to polymorphism. The factors affecting transformation are dopant species and their concentrations, oxygen vacancies, surface/interface/grain boundary energy, electric field, mechanical stress and strain [43].

The interfacial stress induced by a bottom or top electrode is a crucial factor in the formation of the ferroelectric orthorhombic phase, as reported by Böschke et al. [21] using TiN surface electrodes.

Generally, doped HfO_2 films are amorphous in the deposited state [14]. Accordingly, achieving ferroelectricity requires crystallization annealing, which is typically a rapid thermal process. The phase achieved is significantly influenced by two processes: the annealing step at high temperature and the cooling step after crystallization annealing. Crystallization of amorphous films is achieved by rapidly increasing temperature to 400 - 1000 °C, depending on the dopant species [43].

Starting from the monoclinic phase (m-phase P21/c), the crystallization process progresses to a tetragonal phase (t-phase, P42/nmc) and then to a cubic phase (c-phase, Fm3m) forming small nuclei [60]. These phases are centrosymmetric and therefore nonpolar. As the grains continue to grow and the interfacial energy contribution decreases, they transition to the polar oIII-phase as shown in Figure 2.6. This phase lacks centrosymmetry which is why it is considered to be the origin of ferroelectricity. Eventually, a transition to the m-phase occurs because the bulk free energy is lower. The transformation process is illustrated in Figure 2.5.

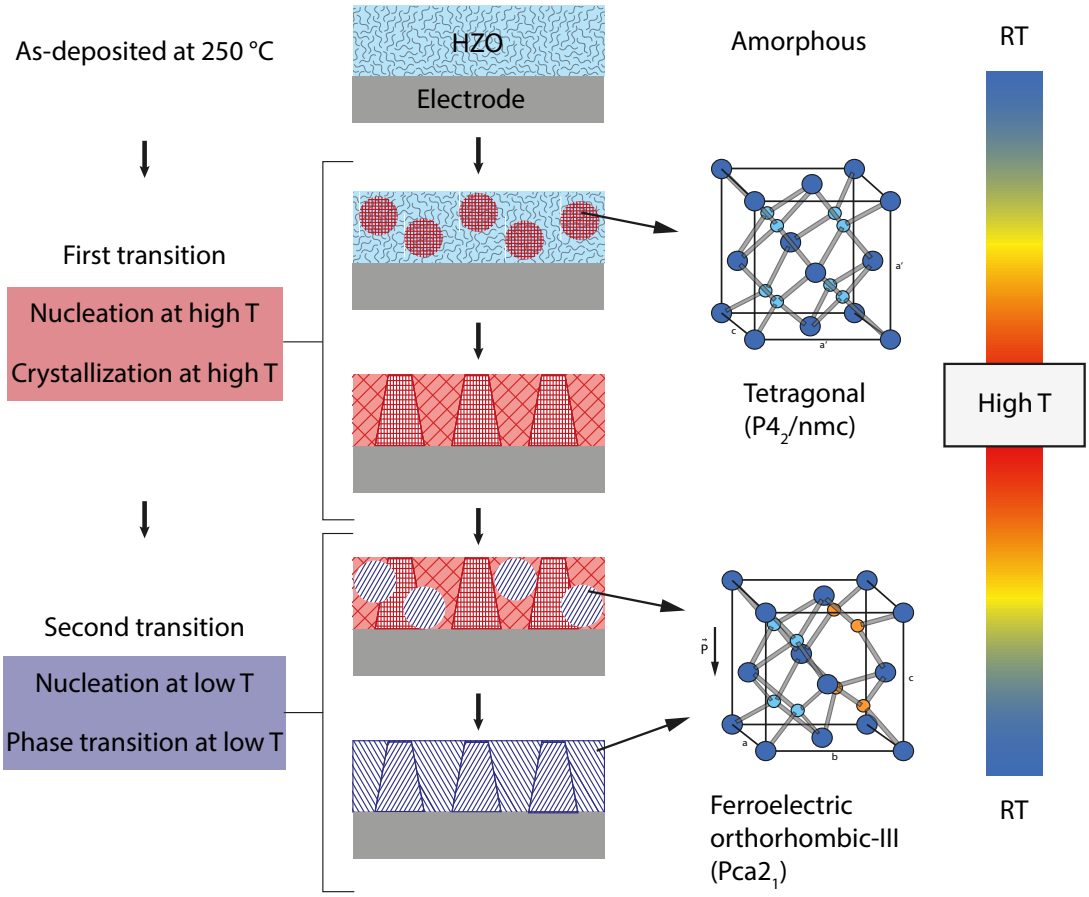

Figure 2.5: *Formation of the ferroelectric orthorhombic oIII-phase (space group: $Pca2_1$) in HZO thin films during a rapid thermal process. Adapted from [43]*

In addition, it is important to note that there are two nonpolar orthorhombic phases: the orthorhombic I phase (o-phase, Pbca), the orthorhombic II phase (oII-phase, Pnma), and the polar (ferroelectric) orthorhombic III-phase (f-phase, Pca21) mentioned at the beginning [60].

Figure 2.6 displays how the polarization direction shifts with alterations in the crystal structure.

Müller et al. [20] has shown that the characteristic behavior of the film varies tremendously depending on the ratio between HfO_2 and ZrO_2, as shown in Figure 2.7. Starting with pure HfO_2 (monoclinic phase) an almost linear relation between the polarization and the applied electric field as well as a almost constant capacitance can be observed due to its centrosymmetry. With increasing concentration of ZrO_2 a ferroelectric P-E and C-V hysteresis evolves until a ratio of equal proportions provides the best properties for use as a ferroelectric material, since it exhibits a remanent polarization of around 30 $\mu C/cm^2$ with

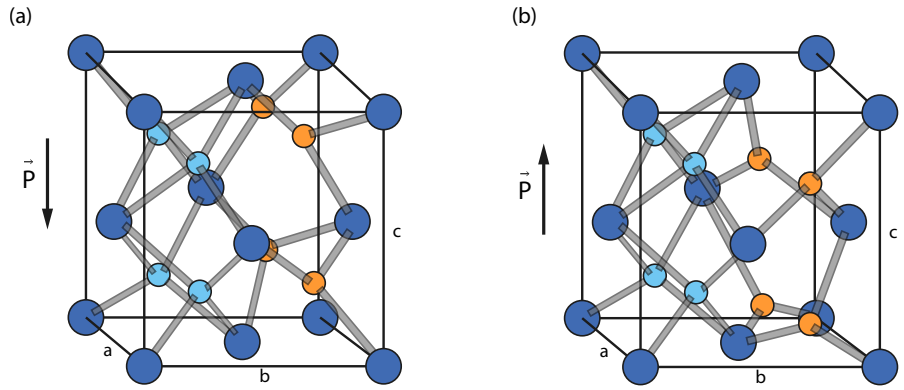

Figure 2.6: *Ferroelectric orthorhombic-III ($Pca2_1$) known as f-phase. Hf/Zr atoms are represented in dark blue, O atoms in bright blue. The O atoms mainly responsible for the polarization are highlighted orange. Adapted from [60]*

a coercive field of approximately 1 MV/cm [20]. Subsequent increase of ZrO_2 result in a thinning of the hysteresis loop at absence of electric field, which is phenomenologically best described as superimposed antiferroelectric-like characteristic [20]. While for pure ZrO_2 a distinct double-loop hysteresis can be attained.

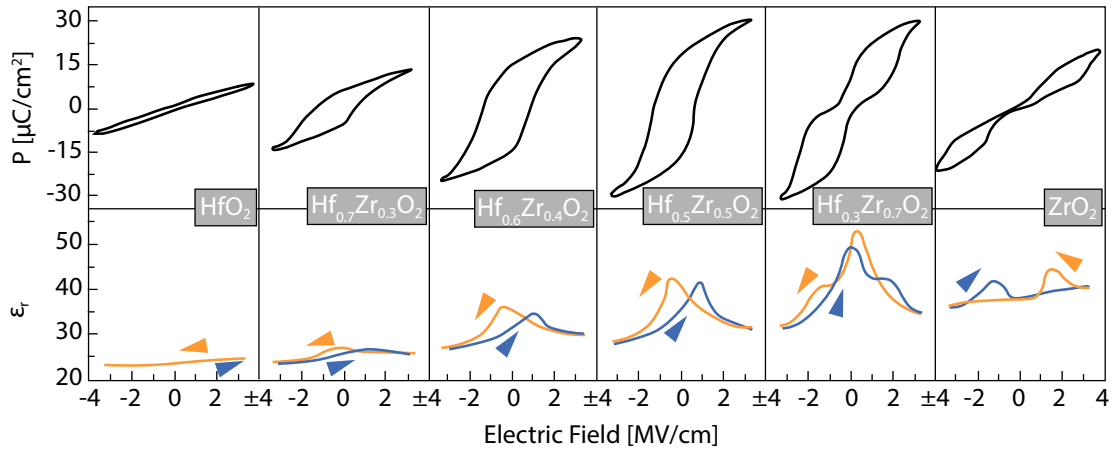

Figure 2.7: *Polarization hysteresis (1 kHz) and C-V hysteresis (10 kHz with 50 mV level) of 9 nm thin HfO_2-ZrO_2 based metal-insulator-metal capacitors at room temperature. Adapted from [20]*

Summarized, it can be stated that by varying the dopant ratio, a transition from paraelectric HfO_2 to ferroelectric HfO_2-ZrO_2 and then further to an antiferroelectric-like behavior in ZrO_2 is observed [20].

Fabrication of HZO thin films

A method for selecting the ideal concentration for these fluorite-structured HfO_2- or ZrO_2-based ferroelectrics is offered by Atomic Layer Deposition, which is already used for syn-

thesizing high-k dielectrics in the semiconductor industry and has thus gained significant importance see [61]. The ferroelectrically doped HfO_2 thin films are most commonly deposited by atomic layer deposition (ALD), according to Min Hyuk Park in [14]. Other deposition techniques include chemical vapor deposition (CVD), physical vapor deposition (PVD), chemical solution deposition, and pulsed laser deposition. However, compared to other techniques, ALD offers the significant advantage of a lower process temperature than CVD, which is important for implementation in CMOS semiconductor processing. The other two important advantages of ALD are thickness control and conformality. The combination of these two characteristics is something unique to ALD.

ALD is a commonly used vapor phase process in semiconductor technology due to its excellent ability to produce thin films of various materials. It was first introduced by Suntoka and Antson in 1977 [62].

This process is sequential and based on self-limiting reactions. Due to the remarkable quality of conformity on high-aspect ratio structures and the possibility to tune the composition concentration, it is used for the fabrication of homogeneous and reproducible HZO thin films in this thesis [63]. Due to the monolayer-by-monolayer (Angstrom level) deposition, which is determined by the number of cycles, the ALD process offers ideal thickness control of the thin films to be deposited.

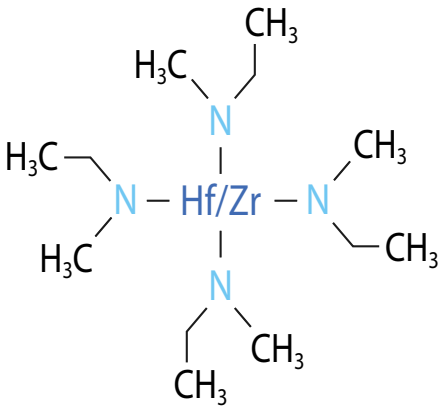

Figure 2.8: *Chemical structure of Tetrakis-(ethylmethylamido)-hafnium/zirkonium (TEMAHf/Zr). Adapted from [64]*

Two gaseous chemical precursors are necessary for a alternating layer of HfO_2 and ZrO_2. The precursors differ in their chemical structure only by the element to be deposited, in this case hafnium (Hf) and zirconium (Zr) respectively as depicted in Figure 2.8. One methyl and one ethyl group $[(CH_3)(CH_2CH_3)]$ are attached to each of the nitrogen compounds (N), which are essential for the self-limitation of this process.

The study [65] on the interaction between TEMAHf precursor and OH-terminated Si (001) surface shows two reaction mechanisms when TEMAHf reacts with the surface. In Equation 2.10, a reaction is presented in which one -OH group reacts with the Hf

atom of $3[(C_2H_5)(CH_3)N]Hf$ to form a bond with the O atom of -OH, producing one $H-N(CH_3)(C_2H_5)$ (EMA) as a by-product. The second case, indicated in Equation 2.11, is where a reaction with two -OH's produces two EMA's and the Hf atom of $2[(C_2H_5)(CH_3)N]Hf$ bonded to two O atoms.

$$\begin{aligned} &Si-OH+4[(C_2H_5)(CH_3)N]-Hf \\ &\rightarrow Si-O-Hf-3[(C_2H_5)(CH_3)N]+H-N(CH_3)(C_2H_5) \end{aligned} \tag{2.10}$$

$$\begin{aligned} &Si-OH+4[(C_2H_5)(CH_3)N]-Hf+OH-Si \\ &\rightarrow Si-O-Hf-2[(C_2H_5)(CH_3)N-O-Si+2[H-N(CH_3)(C_2H_5)] \end{aligned} \tag{2.11}$$

This reaction at the inter-dimer site is the most favorable among the five reactions and is more likely than the first one in comparison [65].

H_2O is most commonly used as a counter reactant for oxides as it is gentler to the substrate surface and can withstand higher deposition temperatures without decomposing although less reactive than, for example, O_3, O_2, H_2O_2 [65]. It is often also called oxidizer.

The recipe utilized in this thesis, as explained in Section 3.2, examines the optimal process within a specific temperature range. Kihye Kim investigated in her thesis [66] the integration of this material composition into an Schottky-Barrier FET (SBFET) structure while focusing on the HZO layer itself.

Moderate temperatures below 350 °C are normally used for ALD processes. The term "ALD temperature window" defines the temperature range in which growth is saturated. Therefore, this range should be targeted, as temperatures outside of this window usually lead to poor growth rates or insufficient film quality. At low temperatures, effects such as slow reaction kinetics or precursor condensation occur, while at high temperatures, effects such as thermal decomposition or rapid precursor desorption occur [63].

Most commonly, alkylamides - such as TEMAHf/Zr, TDMAHf/Zr - are used as ALD precursors for the deposition of HfO_2 and ZrO_2 films. They exhibit a growth rate of 0.1 nm/cycle [14]. As a result, dense films with low contamination can be produced. According to Min Hyuk Park et al. [14], these precursors have limited thermal stability, which means that the temperature is typically in the range of 200 - 280 °C, which may not be the optimal window.

An ALD cycle consists of two half-cycles, in the first of which the selected precursor is pulsed into the heated reaction chamber with a constant flow of nitrogen N_2 (highly

stable, inert) over the already (passivated) functionalized substrate (3 cycles of H_2O) to densify the amount of OH groups on the surface. The functionalization is achieved by hydroxyl groups (OH). As soon as the precursor comes in contact with the surface, the hydrogen is released and reacts with $N(CH_3)(C_2H_5)$ groups as by-product EMA ($H - N(CH_3)(C_2H_5)$). Once all potential reaction pairs have been exchanged, a so-called purge - typically with N_2 or Ar - is performed to remove the excess precursor and reaction by-products in order to initiate the second half cycle. This cycle begins with the addition of H_2O to the reaction chamber, again making the reaction self-limiting. This is followed by further purging of the chamber. The first layer is formed and the process can be continued with e.g. a zirconium oxide layer. The representation for a layer of HfO_2 or ZrO_2 is shown in the Figure 2.9.

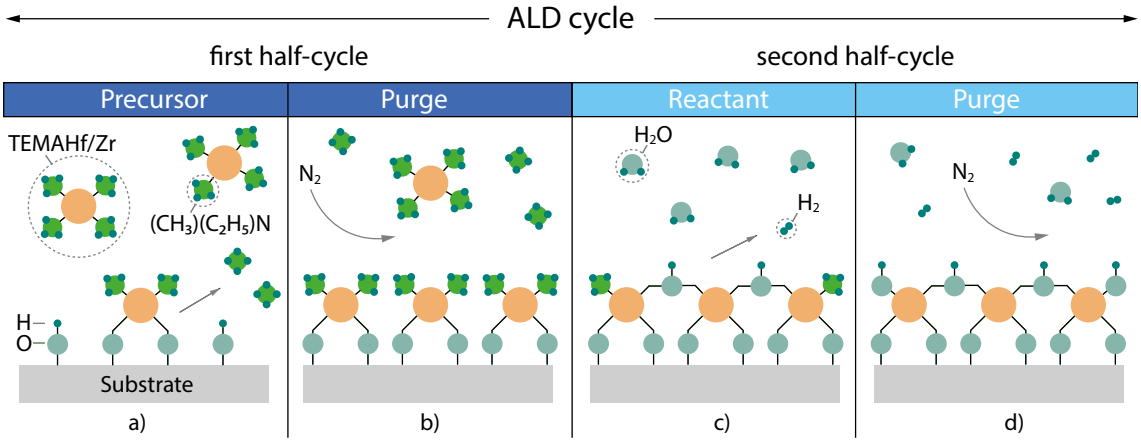

Figure 2.9: *Schematic ALD cycle of a Hf/Zr-oxide process. Adapted from [67]*

It can be concluded that the electrical properties of ALD based $Hf_{1-x}Zr_xO_2$ thin films are promising. With a demonstrated remanent polarization of more than 20 μCcm^{-2} and an endurance of more than 10^9 cycles, they are very promising for storage or energy related applications. In addition, HfO_2 and ZrO_2 have chemical and physical similarities compared to the other dopants, and therefore provide the broadest compositional range for ferroelectric properties [14].

2.2 Metal-Semiconductor Heterostructures

The quality of metal-semiconductor heterostructures is critical to the realization of reliable contacts for electronic devices. This is characterized by the absence of interface traps (pinning) and minimal contact resistance [68].

It is important to pay attention to the metal and the corresponding semiconductor contacts as they form contacts with different Schottky barrier heights, which eventually strongly influence the electrical properties of the heterostructure and thus the device functionality. In this work, aluminum and silicon have been used because the method described by Wind et al. [22], which is based on a thermally induced Al-Si exchange reaction, forms an

abrupt and void-free metal-semiconductor interface. In addition, this metal-semiconductor material combination offers the property of no intermetallic phase formation, which has a positive effect on the precision and reproducibility of the transitions [6, 68].

The binary Al-Si systems exhibit a phase diagram of a simple eutectic type with no intermetallic phase formation, as depicted in Figure 2.10.

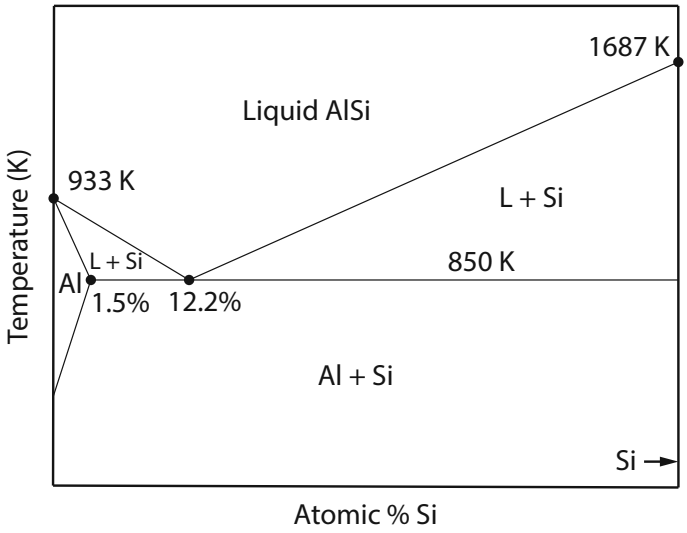

Figure 2.10: *Phase diagram of the Al-Si. Adapted from [69]*

Fick's law [70] describes the behavior of diffusion with the Equation 2.12. In this definition, the symbol J represents the diffusion flux, D refers to the diffusion coefficient, and ∇C represents the concentration gradient C. Diffusion, in general, can be defined as particle movement from a region of high to low concentrations. Thus, the outcome is to balance the concentration in the medium.

$$J = -D\nabla C \tag{2.12}$$

The temperature-dependent diffusion coefficient can be described using the Arrhenius representation, as demonstrated in Equation 2.13. In order to determine the coefficient D_0, the activation energy E_a must be obtained. k_B is the Boltzmann constant and T the corresponding temperature.

$$D = D_0 e^{-\frac{E_a}{k_B T}} \tag{2.13}$$

Furthermore, the diffusion coefficients to the respective partner materials as well as within the same material (self-diffusion) must be considered. The findings of the study carried

out by Wind et. al. [22] for the corresponding diffusion coefficients during a rapid thermal annealing (RTA) process at 774 K are presented in Table 2.3.

Al in Al (cm^2/s)	Al in Si (cm^2/s)	Si in Al (cm^2/s)	Si in Si (cm^2/s)
$6.3 \cdot 10^{-10}$	$2.0 \cdot 10^{-22}$	$4.4 \cdot 10^{-8}$	$6.5 \cdot 10^{-19}$

Table 2.3: *Diffusion coefficients of the Al-Si material system at 774 K. Values taken from [22]*

In Figure 2.11, the use of High-Resolution Transmission Electron Microscopy ((HR)TEM) and Energy Dispersive X-ray Spectroscopy (EDX) clearly illustrates the abrupt transition.

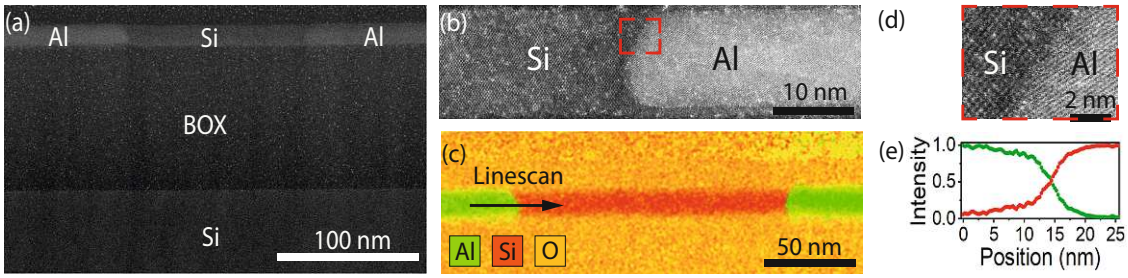

Figure 2.11: *(a) TEM image of an Al-Si-Al device fabricated by a top-down approach and the corresponding EDX map of the heterostructure (b). HRTEM image showing an Al-Si interface (c) and a close-up at the red dashed box in (b). An EDX linescan across the abrupt Al-Si junction as indicated in (d) is shown in (e). Pictures adapted under the permission of [22]*

2.2.1 Metal-Semiconductor Interface

The following section presents a detailed explanation of the diffusion process of two materials. This includes a discussion of the Schottky barrier formed by the metal-semiconductor transition.

The combination of two different materials provides interesting insights. The distinct work functions result in the emergence of rectifying Schottky barriers. Therefore, a brief overview of the theory is provided since the combination of two Schottky barriers into a single device can serve as a Schottky Barrier FET (SBET) and a reconfigurable field-effect transistor (RFET) as investigated in this study (for details see Section 2.3).

The theoretical concepts were adapted for this subsection from the book "Metal-Semiconductor Contacts" authored by E. H. Rhoderick and R.H. Williams [68], unless otherwise specified.

Utilizing the band diagram formalism for the description of Schottky barriers, is only feasible by taking three main assumptions into account [6]:

- Direct contact between the metal and semiconductor is essential, without any interfering materials i.e. oxides.

- Neglection of interdiffusion
- Impurity-free transition at the interface

The metal work function ϕ_m can be understood as the difference between the vacuum level and the Fermi level:

$$q\phi_m = E_{vac} - E_{Fm} \tag{2.14}$$

Aluminum has a work function energy of $q\phi_{m,Al} = 4.25$ eV [71]. Si has a bandgap energy of 1.12 eV and an electron affinity of 4.05 eV [6]. The work function of a semiconductor is described by Equation 2.15, as can also be seen from Figure 2.12.

$$q\phi_s = \chi + \phi_n \tag{2.15}$$

When the materials are in thermal equilibrium due to contact, their Fermi energies are brought into equilibrium. As a result, band bending occurs until charge neutrality is achieved. Charge carrier transport is responsible for this alignment [6].

A Schottky barrier $q\phi_B$ is an energy barrier that determines the direction of carrier transport based on the applied bias polarity and Schottky barrier height. The barrier height is determined by the semiconductors electron affinity χ and the metals work function ϕ_m, as shown in Equations 2.16 and 2.17 for holes and electrons, respectively.

$$q\phi_{B,n} = q(\phi_m - \chi) \tag{2.16}$$

$$q\phi_{B,p} = E_G - q(\phi_m - \chi) \tag{2.17}$$

Figure 2.12 shows the band structure for both n-type and p-type semiconductors. The initial states are shown in (a) and (c), as well as the ideal case of metal-semiconductor contact with the resulting contact potential in (b) and (d).

Depending on the magnitude of the work function of the metal and semiconductor, two cases can be distinguished, with a total of four possible scenarios determined by the carrier type of the semiconductor:

- $\phi_m > \phi_s$:

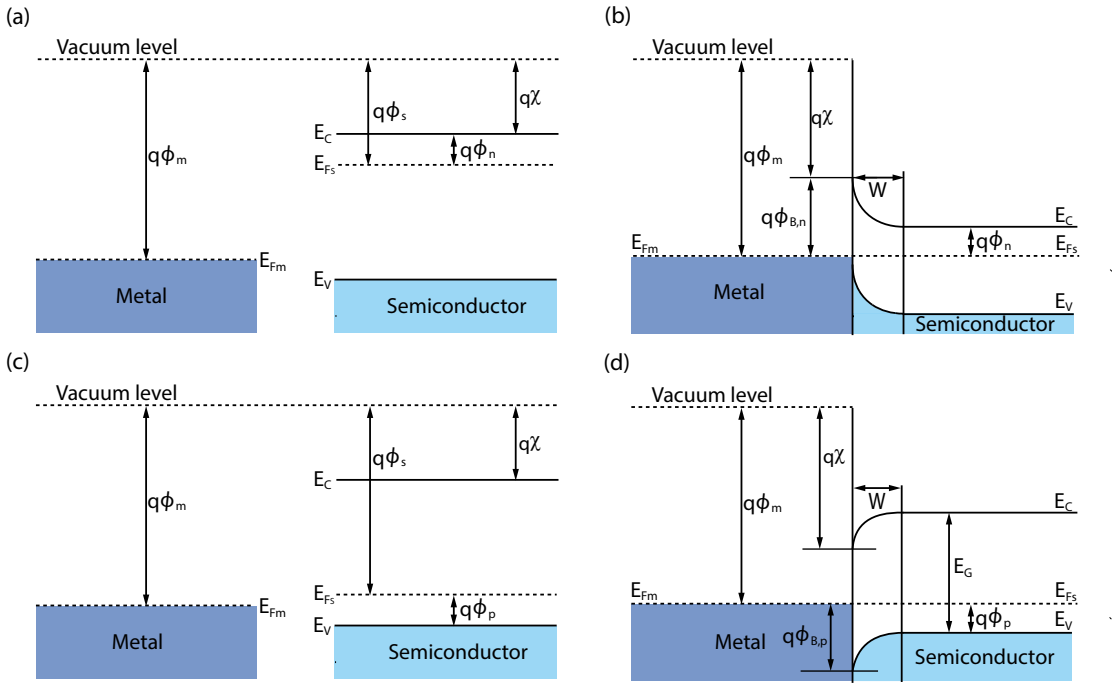

Figure 2.12: *The metal-semiconductor transition is governed by the parameters outlined in (a) for an n-type semiconductor and (c) for a p-type semiconductor. The n-type and p-type semiconductor junctions are seen in Subfigures (b) and (d), respectively. Adapted from [6, 72]*

  - n-type: The semiconductor region near the junction experiences a depletion of electrons, leading to a rectifying behavior recognized as rectifying or Schottky contact.

  - p-type: Above the Fermi-level, the region displays a bending, implying the ionization of the majority charge carriers (holes), resulting in an ohmic-like behavior of the transition, known as ohmic contact.

- $\phi_m < \phi_s$:

  - n-type: The same behavior as before is observed. In this case, electrons become ionized when bending below the Fermi-level. This results in ohmic-like behavior of the transition, known as ohmic contact.

  - p-type: In this case, the junction is depleted of holes, resulting in a Schottky contact.

For pure silicon, the aluminum-silicon pinning level is located in the middle of the band gap, as demonstrated in Figure 2.13. In most cases, metals have a Fermi level located

nearby the center of the band gap when in contact with Si. This has the advantage that the (defect-free) Schottky barrier has a symmetrical behavior for electron and hole transport, which is important for the Reconfigurable Field-Effect Transistor (RFET), see Section 2.3.

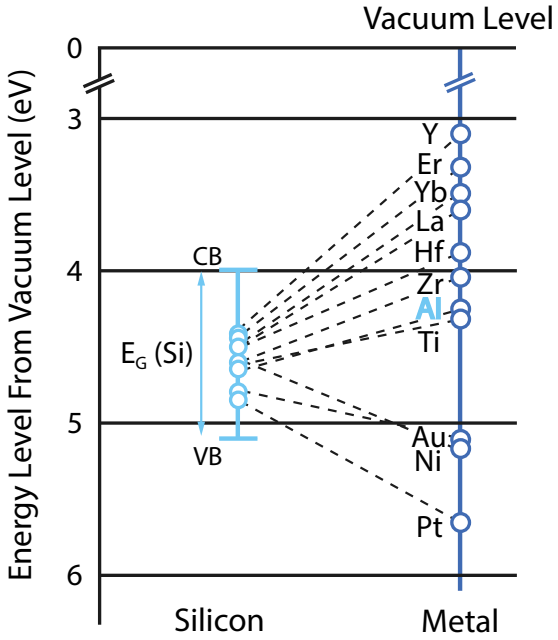

Figure 2.13:
Energy barrier heights for various metal-semiconductor transitions. Regarding silicon, the pinning occurs primarily in the middle of the bandgap. Source: [73, 74]

Figure 2.14 illustrates the five basic transport mechanisms that can be declared as [6]:

1. Thermionic electron emission from the semiconductor into the metal overcoming the Schottky barrier.

2. Quantum mechanical tunneling of electrons through the barrier.

3. Recombination within the space charge region.

4. Diffusion of charge carriers into the depletion zone.

5. Injection of holes from the metal into the semiconductor material.

According to Sze [6], the transport mechanism can be classified into three types based on their energy:

- Thermionic emission (TE), which involves high-energy charge carriers which can

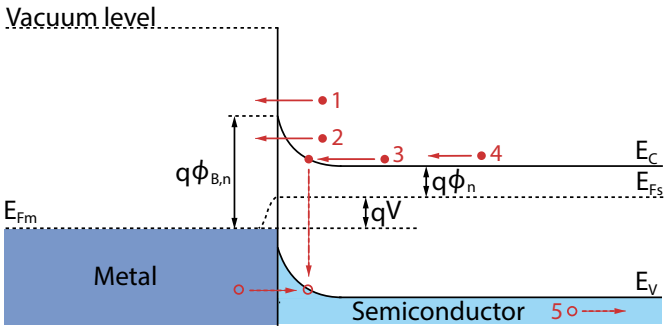

Figure 2.14: *Transport mechanisms for electron donated current: (1) thermionic emission, (2) tunneling, (3) recombination, (4) diffusion and (5) hole injection. Adapted from [6]*

surpass the barrier.

- Field emission (FE), which is the tunnel current through the barrier when energies are close to the Fermi level, which is also often referred to as Fowler-Nordheim tunneling.

- Thermionic field emission (TFE) is a combination of thermionic emission and field emission, where the carrier energy is insufficient to overcome the barrier. Due to a thinner barrier at higher energy levels, the probability of tunneling increases, leading to an increase in current.

The current due to the applied voltage V is given by:

$$I = I_0 e^{\frac{qV}{k_b T}-1} \tag{2.18}$$

With I_0 as the reverse saturation current, V the applied forward voltage, and T the temperature.

The current density can be written with the area related current as

$$J_0 = B_e T^2 e^{-\frac{q(\phi_B)}{k_b T}} \tag{2.19}$$

where B_e is the so-called Richardson constant.

As mentioned at the beginning of this subsection, the band diagram formalism assumes ideally no interface states, commonly referred to as interface traps. The presence of interface traps can significantly affect device behavior, as it can result in barrier heights that deviate from what is expected. The negatively charged interfacial charge states below the Fermi level result in a modification of the initial barrier height. This change does not only depend on the work functions, but also on the interfacial charge trap density D_{it}, illustrated in Figure 2.15 [6, 68, 72, 75].

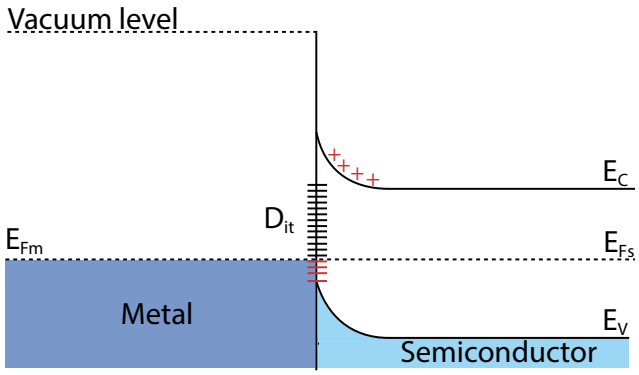

Figure 2.15: *Band bending caused by charge states at the interface. Red indicates the presence of charged interface states below the specified Fermi level. Adapted from [6]*

2.3 Reconfigurable Field-Effect Transistor (RFET)

In this section the basic principles of a reconfigurable field-effect transistor, short RFET, are explained. Furthermore advantages over a conventional field-effect transistors are given.

The RFET is obtained by having a semiconductor segment with two Schottky barriers, which occur between the metal-semiconductor junction as presented in the previous section. It is characterized mainly by the property of preventing or allowing the transport of charge carriers and switching between these two states - n- or p-type - depending on the voltage condition applied to the gates.

The development of the RFET dates back to the year 2000 at the National Chiao Tung University in Taiwan as a solution to suppress the unwanted high off-state currents in ambipolar Schottky barrier thin-film transistors (TFTs) [76]. In 2005, IBM continued to develop the RFET and published the paper "Novel carbon nanotube FET design with tunable polarity" [9].

In 2008, W. Weber and a team from Infineon improved the concept by using a $NiSi_2/Si/NiSi_2$ heterostructure with thermally intruded silicide contacts, described in detail in [11].

M. Heinzig et al. (NaMLab 2012) [10] introduced the term "Reconfigurable Field-Effect Transistor".

The Institute of Solid State Electronics at TU Wien utilized Al for the metal contacts on the semiconducting element. The works that utilize pure silicon as a channel material [22, 77], SiGe [47], and GeOI [78, 79] should be mentioned for this purpose.

Additionally, RFETs can be manufactured using both top-down defined nanosheet as well

as bottom-up grown vapor-liquid-solid (VLS) nanowires.

As shown in the Figure 2.16, different gate arrangements can be used. It should also be noted that there are applications for combinations of back- and top gate [80]. The simplest case with a top gate is shown in (a). This configuration is also known as a single top gate (STG) configuration. The top gate encloses both junctions so that the barriers are raised and lowered simultaneously. This concept belongs to the Schottky Barrier FETs (SBFET), where both barriers - at the source and drain region - are altered simultaneously. A reconfigurable FET (RFET) requires at least two independently controlled gate electrodes:

- Polarity gate (or program gate, PG): Controls the type of carrier or transport mode
- Control gate (CG): Switches the transistor between on and off state

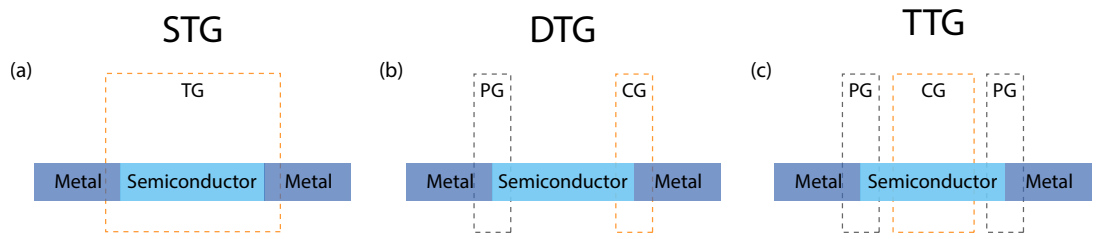

Figure 2.16: *The three different top gate arrangements of this thesis for the metal-semiconductor-metal heterostructure: (a) single top gate (STG) known as SBFET (b) and (c) RFET structure with two (dual top gate, DTG) and three (triple top gate, TTG) top gates. Adapted from [47]*

It is worth noting that the reconfiguration can be made dynamically during runtime [10, 81]. The configuration in (b) is known as the dual top gate (DTG) structure, with the electrode functionality described above. This concept can be expanded to a triple top gate (TTG) arrangement, wherein both PGs are located above the metal-semiconductor junctions and a CG is located in the center of the semiconductor segment. For this thesis, the two PGs were interconnected to shift both Schottky barriers equivalently to favor an appropriate carrier transport mode. By individually controlling them, the corresponding heterostructure can achieve greater freedom in the flow of charge carriers. The control gate serves the same purpose as in the DTG arrangement, but the controllability is considerably increased since the channel itself can be modulated.

2.3.1 Principle of Operation

The principle of operation can be explained in detail with the band diagram formalism.

To describe the electrical transport mechanism, two modes are distinguished, depending on the charge carrier type that is injected through the metal-semiconductor-metal heterostructure, as outlined in Figure 2.17. The n-mode or n-type operation is characterized by the flow of electron current whereas the p-mode or p-type operation is characterized

by hole conduction.

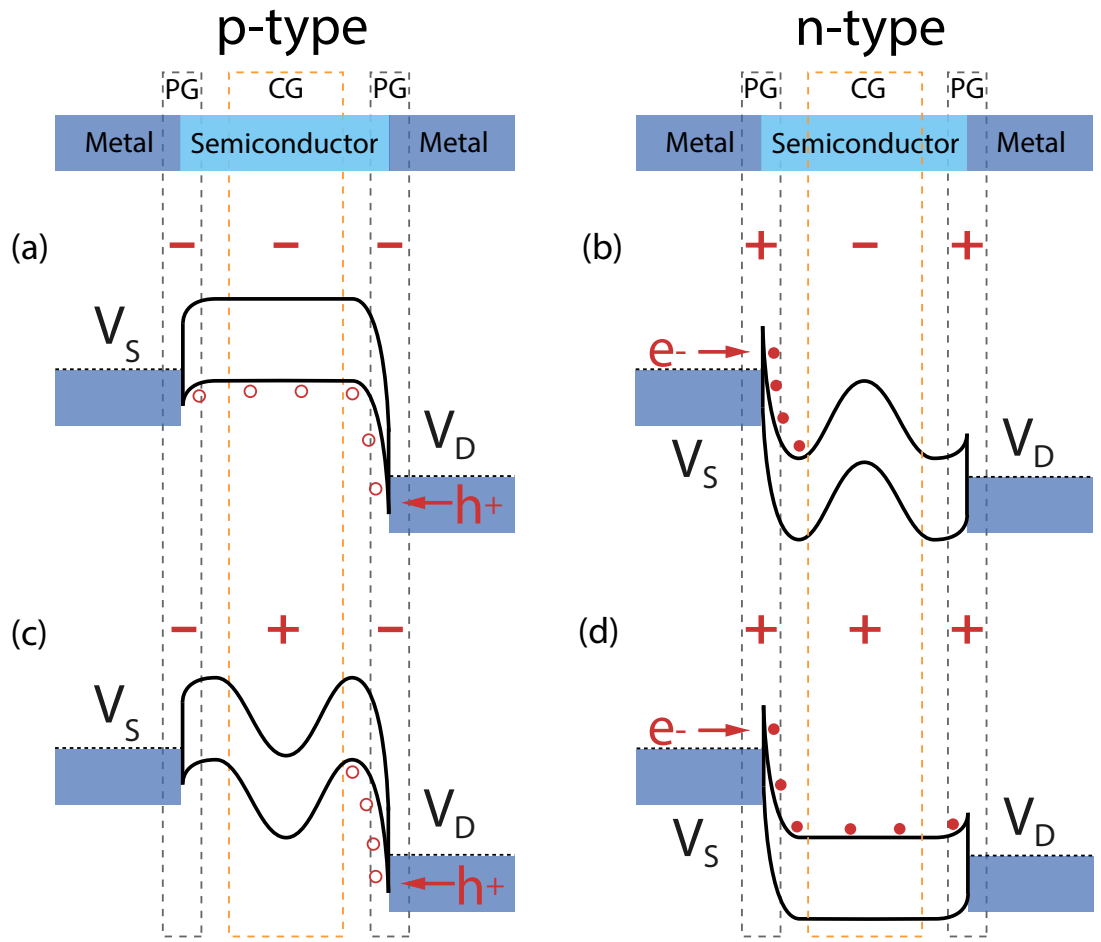

Figure 2.17: *Principle of RFET operation. Dependence of the bands with respect to the applied voltages. (a) and (c) show the p-type operation (hole line) for the on-state operation (a) and the off-state operation (c), respectively. (b) and (d) show the same behavior for n-type operation (electron line). Based on [47, 81–83]*

The source and drain contacts are set to a certain potential. In Figure 2.17, it can be noted that the source is set to a comparably higher energy level - and thus a lower voltage - than the drain.

Through the bending of barriers to a higher energy level, the holes can traverse the heterostructure in both regions as a result of the negative voltage on the PG, represented in (a) and (c). In scenario (a), the control gate is positioned at a negative voltage level, allowing for the unhindered flow of holes. In the case of (c), the current flow is interrupted in the ideal scenario due to a positive voltage at the CG resulting in a bending towards a lower energy level.

The presented procedure is based on the explanations of [81, 83, 84].

2.3.2 Advantages over Conventional Field-Effect Transistors

Firstly, as previously discussed, the use of both n- and p-type in one device reduces technological complexity. Additionally, as the name implies, the RFET approach provides the ability to dynamically program circuits at the device level. [85] Furthermore, a significant advantage of SBFET and RFET devices is their ability to eliminate the need to dope the semiconductor. Reason for this is that the band-configuration of the device depends only on the metal-semiconductor junction and the resulting altering of these Schottky barriers due to applied bias [84]. Therefore expensive doping procedures can be avoided. Furthermore, the Al-Si exchange reaction induced by thermal treatment, as explained in Section 2.2, results in metal-semiconductor interfaces that are abrupt and free of voids [22].

Moreover, the RFET offers increased functional density, although the required additional gates limit scaling. Additional functionality can be added because the transistor type (n/p) can be selected during run-time. In contrast, the functionality of a conventional MOSFET is determined during the manufacturing process. The RFET offers a wide range of flexibility, as several can be combined to form NAND/NOR or even XOR circuits with far fewer FETs compared to the CMOS counterpart, see the thesis by Özgür Demirkiran entitled "Reconfigurable Si Field-Effect Transistors with Crystalline Al Contacts Enabling Adaptive Complementary and Combinational Logic". Due to the additional gate structures, a larger footprint is created, but for certain designs a small chip area and reduced power consumption are possible [77, 81, 86, 87]. Additionally, classical short channel effects such as the gate-induced leakage current (GIDL) [87] are suppressed.

Furthermore, there are advantages in the area of hardware security, especially with respect to physically unclonable functions (PUFs) and side-channel attacks [80]. As will be explained in the following section, RFETs can be used in the field of neural networks and artificial intelligence through the implementation of ferroelectric materials [80, 88, 89].

2.4 Ferroelectric-RFET (Fe-RFET)

The idea of ferroelectric random access memory (FeRAM) was initially suggested by Buck [90] in 1952. The concept was later commercially implemented in the 1990s [17]. In 1963, Moll and Tauri [91] reported the first proof-of-concept demonstration of a memory device based on FeFET. The storage of binary additions was initially unstable due to the materials and structure. In 1974, Wu developed a device consisting of a metal ferroelectric semiconductor stack (MFS) with a perovskite ferroelectric to address these issues. Additionally, Sugibuchi demonstrated the concept of the metal-ferroelectric-insulator-semiconductor-stack (MFIS) with an additional SiO_2 insulator layer. Subsequently, high-k insulators made of HfO_2 were employed to decrease the internal fields in both the ferroelectric and dielectric layers [51].

As discussed in the Subsection 2.1.3, HZO has a comparatively large bandgap compared to perovskite ferroelectrics, a large band offset to Si, a large coercive field, and a comparatively low dielectric constant, resulting in stable data retention and a reasonable memory window even at film thicknesses of a few nanometers. To achieve the necessary miniaturization of devices and overcome issues like the short-channel effect, novel structures like ferroelectric fin field-effect transistors (FinFETs) [92] and gate-all-around (GAA) FeFETs [93] have been demonstrated. [51]

Consequently, with the discovery of ferroelectricity in Si-doped HfO_2 in 2006 and the subsequent publication by Böschke et al. [21] in 2011, the rapid progression of technology continued to be demonstrated by the fabrication of ferroelectric field-effect transistors (FeFET) using 22 nm and 28 nm technology nodes [14].

Furthermore, Sessi et al. 2018 [94] and 2020 [95] published two ferroelectric SBFET approaches, the first of which has an STG arrangement that creates a memory window (MW) that can be used as an additional non-volatile option. The second method explores tuning of charge carrier transport in a non-volatile approach by manipulating the polarization in the ferroelectric layer near the source Schottky junction.

In this thesis the metal-ferroelectric-insulator-semiconductor (MFIS) stack is utilized, hence a short explanation follows. The ferroelectric layer and the interfacial layer will be described according to the description of Mulaosmanovic et al. [53].

- Ferroelectric (FE) layer: Utilized for information storage and exhibits characteristic polarization hysteresis, representing two distinct but equivalent polarization states: $+P_R$ and $-P_R$, which remain stable even in the absence of the applied electric field E. The polarizations are commonly referred to as "up" and "down".

- Interfacial layer (IL): Utilized to separate the channel from the FE layer. Despite its thickness being in the range of just 0.5 - 2 nm, it significantly impacts critical memory metrics such as data retention and endurance, and performs multiple functions:

  - Prevention of interdiffusion of elements between the FE and the substrate (This point is not relevant for the base used in this work, which is an SOI substrate and thus carries a thick burying oxide layer).

  - Enabling a clean deposition and growth of the FE.

  - Ensuring high quality of the channel interface, which is essential for large carrier mobility and thus high transistor performance.

An applied gate voltage of an MFIS device is determined by the capacitive voltage divider between the capacitance of the ferroelectric layer, the capacitance of the interface layer

and the semiconductor capacitance [14].

$$\frac{1}{C_{Ges}} = \frac{1}{C_{FE}} + \frac{1}{C_{IL}} + \frac{1}{C_S} \tag{2.20}$$

To switch the ferroelectric polarization of an FeFET, exceeding the coercive voltage across the ferroelectric layer is necessary. This voltage divider can be manipulated to achieve this goal. Johannes Mueller et al. explain that modifying the capacitance division by only scaling the layer thicknesses is inadequate for reducing the field stress at the interface. Despite lowering the voltage applied to the gate, the electric field across the interface remains constant [14].

To achieve a lower interfacial field voltage, the capacitive divider must be adjusted by selecting an appropriate material and modifying ϵ_{IL}. High-k materials with a dielectric constant above 7 as HfO_2 can be utilized for this purpose. This material is compatible with CMOS technology, has a sufficiently large band offset, and thermal stability for direct contact with silicon [14]. It is well known that SiO_2, the native oxide of silicon, forms an ideal interface with low trap density. For this reason, SiO_2 was chosen as the primary material over high-k alternatives such as HfO_2 or ZrO_2 in this study.

The two states, low threshold voltage (LVT) and high threshold voltage (HVT), can be defined as a memory window defined as MW = HVT - LVT. Whereas the memory window can be approximated by the following simplified expression:

$$MW = 2 \cdot E_C \cdot \alpha \cdot t_F \tag{2.21}$$

Where t_F represents the thickness of the ferroelectric layer, α denotes a parameter that depends on several material properties, and is considered a measure of the ideality of a given FeFET. For typical values of HfO_2 layers such as $E_C = 1$ MVcm^{-1} and $t_F = 10$ nm, a maximum MW of 2 V obtained. [53]

In the case of the Fe-RFET, the properties of the Fe-FET are combined with those of an RFET. Considering the influence of the ferroelectric polarization on the RFET structures we can distinguish two main mechanisms which can i.e in the case of STG arrangements happen also superimposed. The first can be determined as a shift of the transfer characteristic due to these net charge on the channel and the second effect is altering the barriers at the transitions and therefore the on-current in regard to this net charges.

By applying a voltage resulting in a ferroelectric polarization, the transfer characteristic is shifted to positive threshold voltage for negative net charges and vice versa, a negative threshold voltage shift for a positive net charge, as can be seen in Figure 2.18.

Figure 2.19 depicts the different cases of barrier modification for both branches. In the case of a positive voltage at the polarity-gate (PG) the energy-level of the barriers is reduced

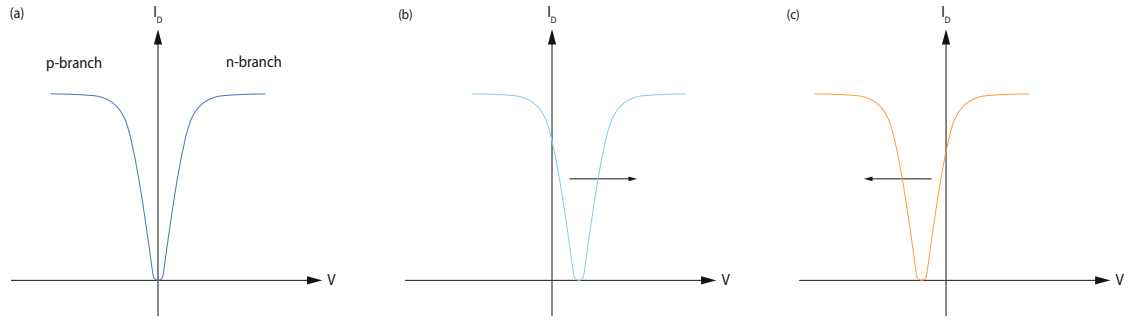

Figure 2.18: *Threshold voltage shift as a function of channel net charge. (a) neutral case, (b) negative net charge, (c) positive net charge*

which favors the electron flow and prevents hole conduction thus the on-current of the n-branch increases and decreased for the p-branch. Same behavior can be taken in analogy for a negative voltage at the PG, with increasing p-branch and decreasing n-branch.

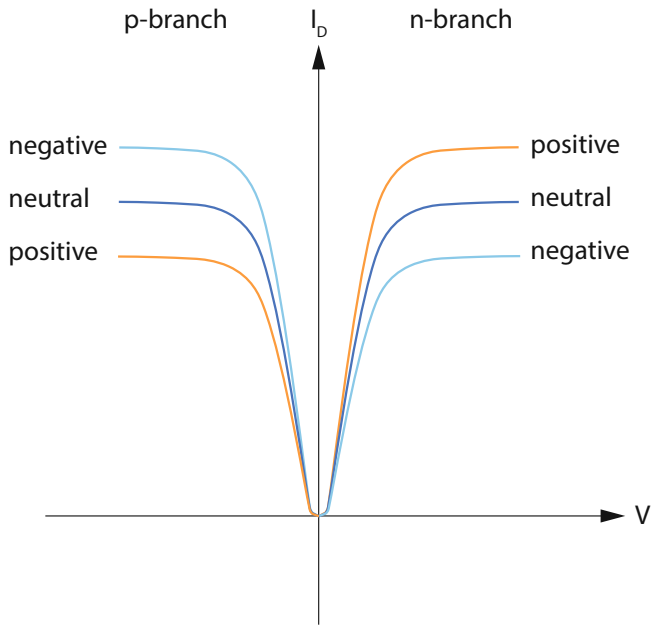

Figure 2.19: *On-current dependency due to net charge over barrier*

It needs to be remarked that in both Figures 2.18 and 2.19 it is assumed that the flat-band voltage V_{FB} is zero and an ideal fermi-level pinning (no trapping) is present for symmetrical p- and n-type behavior.

2.4.1 Non-ideality Behavior

There are two main types of traps called oxide traps and interface traps. Oxide traps have a constant impact on the device behavior (even when no bias is applied) because they do not exchange charge with the semiconductor channel and therefore shift the threshold voltage of the transfer characteristic. Oxide traps exhibit a positive threshold voltage shift for net negative charges, and a negative threshold voltage shift for a net positive charge. This impacts the symmetry of the p-n current in the RFET, as the threshold is not centered as it is in the ideal situation.

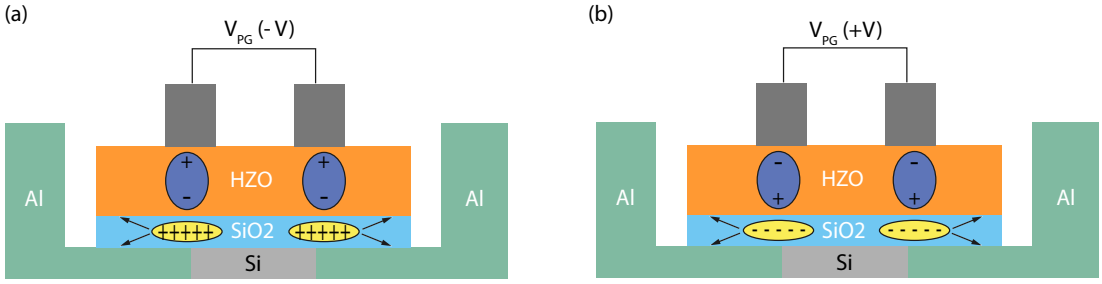

Figure 2.20: *Schematic of FeFET with different charges. Dipoles from ferroelectric material are depicted in dark blue while interface traps (Si/SiO_2 and SiO_2/HZO) of the oxide are indicated yellow. Note that these are not directly in the oxide as indicated with the arrows.*

The second trapping type is a result of the interface and can be separated into trapping regions between the Si/SiO_2 and SiO_2/HZO layers, since there are two interfaces in the device fabricated in this thesis. The first type of trapping causes a hysteresis in the transfer characteristic. However, this phenomenon is not observed so pronounced in our devices due to the well established passivation layer with reduced trap density and is therefore negligible compared to the second phenomenon. Interface traps differ by the oxide traps in their behavior that they can be filled and emptied (trapped/detrapped). In order to fill or empty these traps, the charges have to tunnel through the SiO_2. This is a dynamic process depending on the applied bias in respect to the Fermi-level. These traps typically feature high trap density. This effect shields the ferroelectric effect because the trapped charges are counteractive in this region. In summary, the behavior of the transfer characteristic is dependent on the charges present at the channel/transition. The dominating effect determines which scenario in Figure 2.20 occurs. When the ferroelectric effect dominates, scenario (a) results in a negative shift and scenario (b) results in a positive shift. On the other hand, when the trap-dominated scenario prevails, scenario (a) leads to a positive shift and scenario (b) to a negative one. This behavior is always opposite to each other. Therefore, separating the individual components of this effect proves challenging due to their co-occurrence and impact on behavior.

Depolarization is described as a field that opposes polarization and thus weakens it due to incomplete shielding of polarization charges and is one of the main causes of ferroelectric degradation when the thickness of the ferroelectric film is reduced [42].

The formation of interfacial layers is considered to be the main part responsible for this effect and is subject to the fabrication process and materials used. Using ab initio calculations, Stengel and Spaldin [96] showed in 2006 that even at an ideal metal-insulator interface, a dead interface layer with low permittivity is formed. This finding suggests that it is an intrinsic property and not just a consequence of processing problems such as defects and deformation. [42]

2.4.2 Benefits through Integration of Ferroelectric Materials

This thesis offers a method towards the following applications, which are not yet fully realizable with the current approach, but can be seen as a perspective, since there are several use cases which should not remain unmentioned.

The integration of ferroelectric materials promises a number of different applications, such as

- Non-volatile Logic-in-Memory (LiM)
- Negative Capacitance FET (NC-FET)
- Self-adaptive/learning circuit (Neuromorphic Computing).

This topics will be briefly discussed in the following subsections.

2.4.2.1 Non-volatile Logic-in-Memory (LiM)

All information in this subtopic that is not specifically cited is taken from Chapter 10.6 "Ferroelectric Devices for Logic in Memory" of the book "Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices" [43].

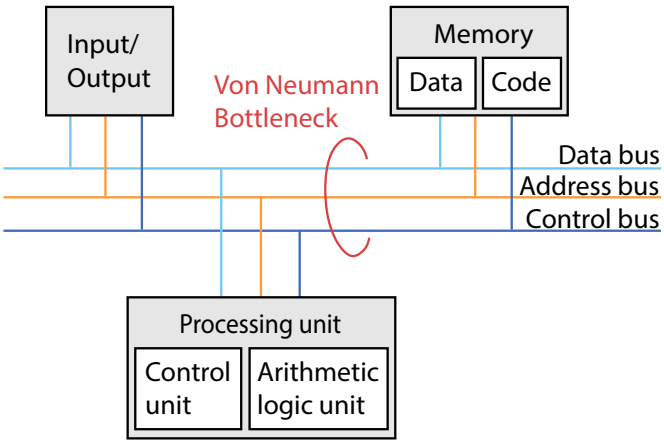

Figure 2.21: *Von-Neumann architecture with the resulting bottleneck. Adapted from [43]*

Memory and logic units are essential components in numerous electronic devices, responsible for storing and retrieving information and processing it accordingly. The von-Neumann architecture is the prevalent model modern computers use, whereby the processing unit conducts information processing, and data and program code are enclosed in a separate memory unit. These sections connect via shared buses (address bus, control bus, and data bus). Due to the sequential processing of data and instructions, buses limit information throughput, creating the von-Neumann bottleneck as depicted in Figure 2.21.

Addressing this issue requires new approaches to manage ever-increasing amounts of data. One potential solution is logic-in-memory (LiM), which bridges the gap between logic and memory units through *fine-grained* implementation. LiMs integrate both logic circuits and memory elements within one processor unit. Non-volatility offers several advantages for LiM units:

- As soon as the supply voltage is switched on, the circuit has a defined state
  $\rightarrow$ registers can be loaded in the same clock cycles.

- State of the circuit is maintained in the event of a supply voltage failure.

One potential solution is the use of non-volatile transistors, such as ferroelectric field-effect transistors (FeFET), which can store data and function as logic elements simultaneously.

Embedding a non-volatile option in an RFET is an intriguing concept. It eliminates the need for continuously applied programming voltage and offers multivalent memory operation and a tight logic-memory interface, enabling new computing paradigms like a LiM device [80].

2.4.2.2 Negative Capacitance (NC)

As mentioned in Subsection 2.1.2 the P/E-curve shows a path of negative slope for dP/dE. Salahuddin and Datta [97] described this effect in 2008. The concept is to use a ferroelectric layer as a gate insulator in a FET, which can be stabilized below a specific critical layer thickness in a NC state [14].

One important factor that limits the operating voltage is the sub-threshold swing (STHS) also known as inverse sub-threshold slope, defined as:

$$STHS = \frac{\partial V_G}{\partial(log_{10} I)} = \frac{\partial V_G}{\partial \varphi_s} \frac{\partial \varphi_s}{\partial(log_{10} I)} \tag{2.22}$$

The second term, which relates the changes in the current to the changes in the surface potential in the channel, cannot be less than 60 mV/decade at room temperature due to the fundamental Boltzmann limit, which in conventional FET structures is defined by the equation $\ln(10) k_B T/e$, where k_B is the Boltzmann constant, T is the temperature, and

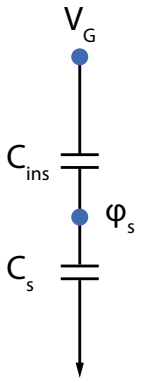

Figure 2.22: *Equivalent circuit for the division of the gate voltage between the insulator capacitance and the semiconductor capacitance for a conventional FET structure. Adapted from [97]*

e is the elementary charge. The first expression - called the body factor "m" - shows the relationship between V_G and φ_s by a capacitive voltage divider. This ratio must be greater than one

$$m = \frac{\partial V_G}{\partial \varphi_s} = 1 + \frac{C_s}{C_{ins}} < 1 \tag{2.23}$$

for achieving a lower limit of 60 mV/decade (corresponding to m = 1) on the inverse sub-threshold slope (STHS) [97].

Among the key benefits are the potential for further decreasing the supply voltage owing to the NC effect and enabling low-power electronic devices with a steep inverse sub-threshold slope.

The work of Wong and Salahuddin [98] shows a stabilization of a negative capacitor through a depolarization field caused by reduced charge screening by adding a positive capacitance in series [99]. To further deepen the knowledge, the reader is referred to [14, 97–100].

2.4.2.3 Neuromorphic Computing

Note that the theoretic basis comes from Chapter 10.7 called "Ferroelectric Field Effect Transistor for Neuromorphic Applications" of the book "Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices" [43] and the review paper "Reconfigurable field effect transistors: A technology enablers perspective" by Mikolajick et al. [80].

Another approach to von Neumann architectures is neuromorphic computing. Based on the operation of the human brain, which is characterized by its asynchronous, energy-

efficient, massively parallel, and fault-tolerant design, it is aimed to imitate the basic building blocks of the biological brain such as neurons and synapses. Furthermore, synaptic learning rules like spike timing-dependent plasticity (STDP) have already been demonstrated in ferroelectric tunnel junctions, showing the potential of ferroelectric circuitry. [43]

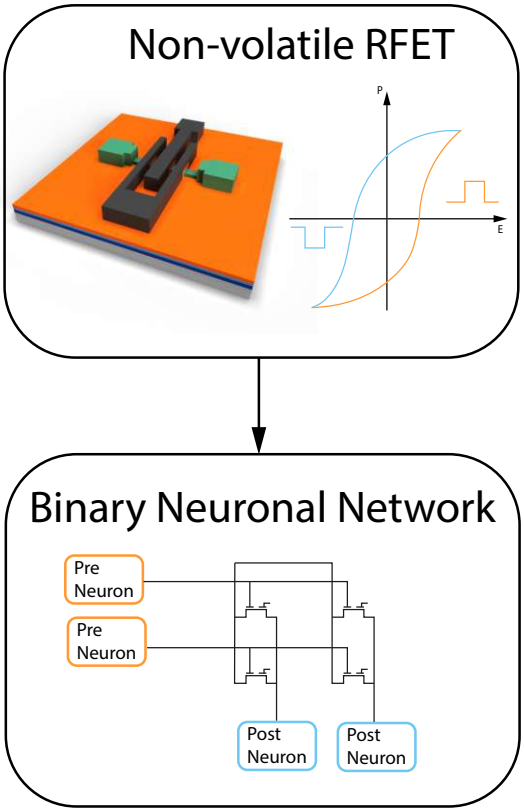

Figure 2.23: *Neuromorphic Computing with RFETs. Top: Schematic of a three-gated RFET with added ferroelectric non-volatile storage option for neuromorphic circuits. Bottom: Circuit diagram of a Binary Neuronal Network (BNN) based on RFETs. Adapted from [80]*

Artificial neural networks (ANNs) outperform standard computer hardware in mimicking cognitive processes such as pattern recognition, speech analysis, and prediction of system behavior. Due to their ability to change their function in response to electrical signals, RFETs have the potential to adapt their functionality. It is possible to imitate the adaptability found in biological neurons and synapses at the device level. Additionally, improved functionality of certain gates can result in a more compact and efficient design. For instance, the XNOR operation, can be implemented very efficiently in RFET technology, representing the matrix-vector multiplication of binary neural networks (BNN) [80].

Chapter 3

Experimental Techniques

This section discusses the experimental techniques used to characterize the fabricated HZO thin films and the targeted Fe-RFETs. It also provides a detailed description of the Fe-RFET fabrication process, enabling a comprehensive understanding of the challenges and improvements throughout the thesis.

3.1 Characterization of Hafnium Zirconium Oxide (HZO)

The HZO thin films were characterized for application in following devices together with a metal-insulator-ferroelectric-metal (MFM) or metal-insulator-ferroelectric-semiconductor (MFS) structure to ensure functionality by using the simplest case. For this purpose, C-V and P-E measurements were carried out, the operating principle of which is explained below. For the further analysis of the crystallinity and the phases of the HZO layers, the X-Ray Center (XRC) of the Vienna University of Technology [101], headed by Dipl.-Min.in Dr.in rer.nat. Klaudia Hradil, kindly assisted with interesting results.

3.1.1 C-V and P-E Measurement

For the C-V and P-E measurements, the probe station "Cascade microtech summit 11000 AP" was used with the semiconductor characterization system "Keithley 4200-SCS". This setup allows capacitance measurements from femtofarad (fF) to nanofarad (nF) at frequencies from 1 kHz to 10 MHz.

In general, capacitance is determined by the change in charge Q with changing voltage V. Here, the common method is used to evaluate the capacitance by applying a DC voltage - large signal analysis - with a superimposed small AC signal - small signal analysis - in the millivolt range to the device under test (DUT).

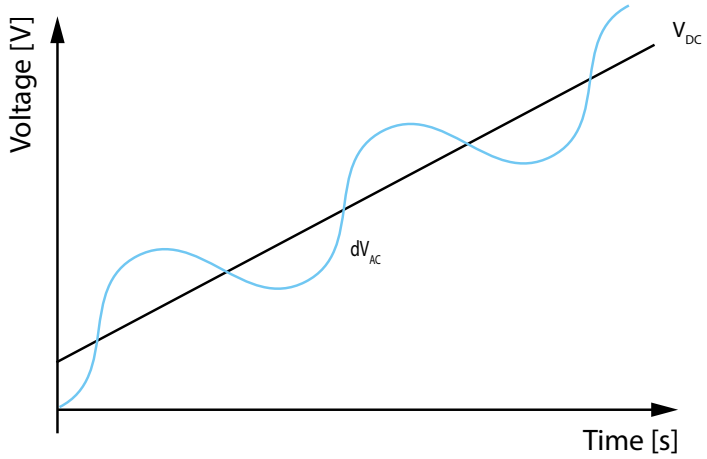

Figure 3.1: *AC and DC voltage of C-V Sweep Measurement. Adapted from [102]*

The resulting current is then used to determine the charge Q by time integration, eventually leading to the determination of the capacitance C. As shown in Figure 3.1, the DC voltage is continuously varied over a specified range while the AC voltage remains fixed in magnitude and frequency. This produces the output of the capacitance value and the conductance. This gives important information about the device behaviors. If the C-V curve for metal-insulator-metal (MFM) structures has a counter-clockwise butterfly shape this speaks for a ferroelectric effect, as can be seen in the Figure 3.4 at the bottom. This result comes from the fact that the capacity C is proportional to the dielectric constant as

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \tag{3.1}$$

with ϵ_0 as the vacuum permittivity, A the surface and d the thickness of the layer.

The dielectric constant can be written as [103]:

$$\epsilon_r = \frac{\epsilon_0 E + P}{\epsilon_0 E} = 1 + \frac{1}{\epsilon_0} \cdot \frac{P}{E} \tag{3.2}$$

The polarization P is a function of the electric field E, hence the dielectric constant is also proportional to the change of P with respect to E. As the polarization of a ferroelectric is changing depending on the applied bias before it reaches a fixed polarization state, also the capacity is affected by this behavior. Furthermore, it is important to note that polarization does not change in a linear fashion, but rather "flips," accelerating and decelerating as it changes. This produces a peak function due to the capacitance being proportional to the rate of change.

The behavior described applies to metal-insulator-ferroelectric-metal (MIFM or simply MIM) structures, since it is essentially a capacitor with a polarization-dependent dielectric

constant. However, since the real case scenario as it exists in the final device is important, the P-E curve has also been validated once for MIM, but then our efforts were focused on the C-V measurement of Metal-Insulator-Ferroelectric-Semiconductor (MIFS or MIS) structures. This semiconductor structure exhibits an accumulation property, where the semiconductor acts as a metal and the resulting curve behaves as a serial capacitance of the insulator (oxide) C_{OX} with C_{FE}, which is true for fixed polarization when already switched, as mentioned above. On the other hand, in the case of depletion, the semiconducting region serves as an insulator, resulting in a series capacitance of C_{FE} C_{OX} and C_S. Due to the considerable thickness of the semiconducting layer in comparison to the others, the capacitance value results in a rather small value. As the one with the lowest capacitance dominates in a series connection of capacitors, the impact of the remaining ones can be disregarded, leading to a primarily Si capacitor with its distinct S-shape.

Here, a distinction can also be made between the ferroelectric effect and trapping effects. In the case of a ferroelectric effect C-V curve is shifted to the opposite direction, meaning if a sweep from negative to positive direction is applied this results in a left shift, resulting in a counter-clockwise behavior, whereas for trapping the curve shifts in the same way as the given sweep direction (clockwise), because the resulting fixed charges (polarization or trapping) exert a bias on the semiconductor layer, effectively shifting the threshold voltage.

For the P-E measurement, an additional circuit is required. This circuit was developed by C.B. Sawyer and C.H. Tower [104] in 1930 and is therefore known as the Sawyer-Tower circuit.

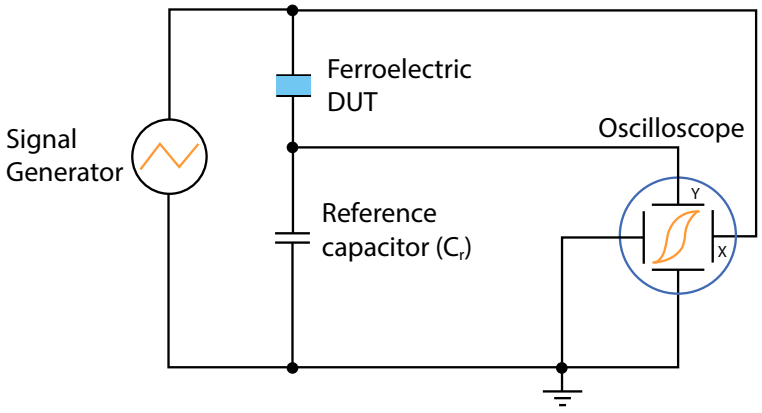

Figure 3.2: *Sawyer-Tower circuit. The polarization of the ferroelectric device under test (DUT) is determined by the charge measurement method with respect to a reference capacitor. Adapted from [105]*

The polarization is determined using a charge measurement technique. A reference capacitor is connected in series with the ferroelectric device under test (DUT). Since both

capacitor structures have the same charge, the proportionality V = Q/C results in two different voltages on the capacitors. The reference capacitor is selected to be significantly larger than the capacitor being measured (DUT) to minimize voltage drop across the reference. High-speed measurements, which are mostly limited by cable reflections, can be performed using the Sawyer-Tower method. However, slow measurements may not be appropriate due to the parallel input resistance of the voltage measurement device (oscilloscope) with the reference capacitor that discharges it with an approximate time constant of $\tau = R \cdot C$. [106] A capacitor with a value of 10 nF was used for the performed measurements.

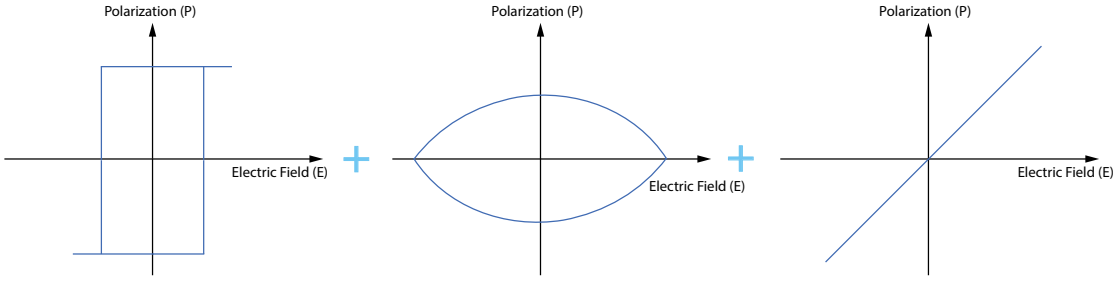

Figure 3.3: *The real polarization curve is composed additively of the ideal ferroelectric hysteresis, the resistive-leakage components, and the linear capacitor or dielectric component. Adapted from [107]*

The real polarization curve is composed of different contributions from various artifacts. This is shown schematically in Figure 3.3. These contributions include the ideal ferroelectric hysteresis, resistive-leakage components, and the linear capacitor or dielectric component. The Sawyer-Tower method is incapable of distinguishing between these components, resulting in the impracticality of being able to determine the usable remanent polarization. To attain the usable remanent polarization value, which is crucial in memory device applications, the PUND analysis technique can be utilized for distinguishing between remanent and non-remanent components. Notably, it is a single point analysis and cannot be used to derive the complete hysteresis [107]. However, the method requires current pulses that must be acquired, so it cannot be used with the existing measurement setup.

3.1.2 Grazing Incidence X-ray Diffraction Analysis (GIXRD)

As mentioned in the introduction of this section, the X-Ray Center (XRC) [101] conducted this analysis. The significance of the results lies in the ability to identify phases that determine respective proportions concerning ferroelectric impact.

In order to understand the structural correlation of the HZO thin film and its ferroelectric behavior, a detailed structural characterization is crucial. In the structural analysis of hafnium- and zirconium-based films, the coexistence of multiple phases and the similar spacing between lattice planes (d-spacing) in the metastable phases that may be present

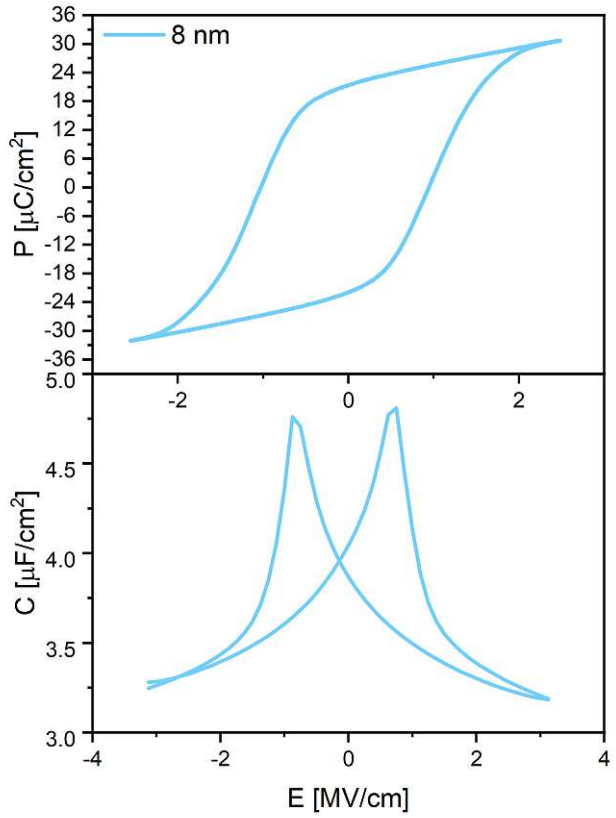

Figure 3.4: *Characteristics of a 8 nm HZO MIM structure. Top: P-E curve. Bottom: C-E curve with distinct butterfly shape. The peaks of the C-E curve correspond to the greatest slope of the P-E curve, which determines the polarization switching. Adapted from [66]*

in these poly-crystalline films in the sub-10 nm range presents a major technical challenge [108].

Among various surface characterization techniques, X-ray diffraction (XRD) is the best known and most widely used technique for thin film characterization. Advantages include the non-destructive nature of the measurement and the wide temperature and pressure range over which it can be performed. The penetration depth itself is controlled by adjusting the angle of incidence of the X-ray beam [109].

The interaction of X-rays and electrons in a solid is used to obtain structural information of thin films. Each crystalline material has its own X-ray diffraction pattern, allowing

diffraction effects to be observed with XRD [110].

This method typically produces a weak signal for thin films and a stronger signal from the main substrate as the X-rays penetrate the material. Grazing incidence X-ray diffraction (GIXRD) is the method of choice for thin film analysis because the X-rays do not penetrate as far, but are diffracted more in the top layer.

Figure 3.5 shows the XRD pattern of a 10 nm HZO test sample with a TiN bottom electrode annealed at 550 °C for 2 minutes. The peaks in the pattern imply that the layer is crystalline after annealing. However, identifying the orthorhombic phase in isolation poses a challenge due to its combination of orthorhombic (o) and tetragonal (t) phases, which share structural similarities, as well as influences from the monoclinic (m) phases. Nevertheless, in agreement with publications, it can be stated that the study of the peaks to their position is consistent with the literature - see selection [20, 111] - which are necessary for the formation of ferroelectric behavior.

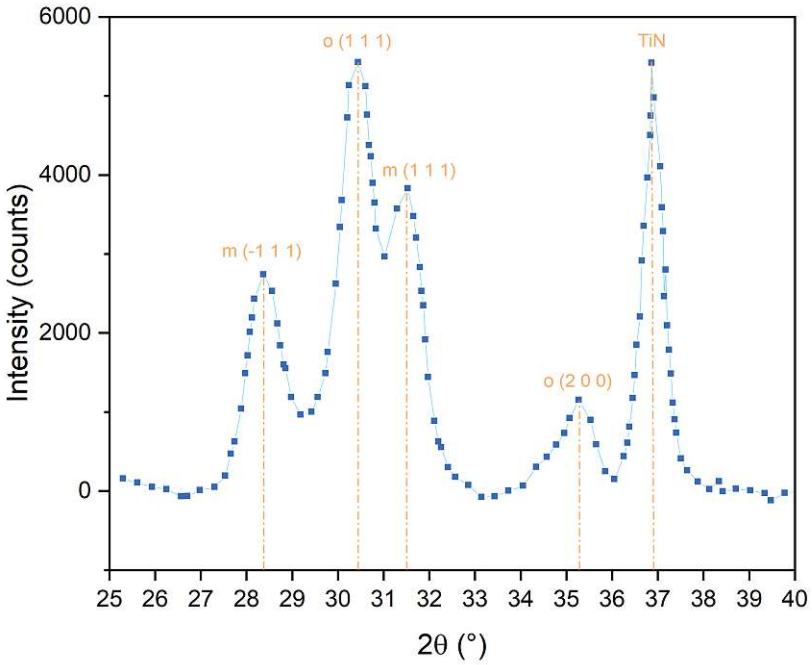

Figure 3.5: *XRD pattern of 10 nm HZO with TiN bottom electrode annealed at 550 °C for 2 minutes*

According to Kim [111], the peaks at 30.5° and 35.5° can be assigned to the o(1 1 1) and o(2 0 0) phases, respectively. Moreover, the m-phases (-1 1 1) and (1 1 1) appear at 28.5° and 31.5°, accordingly. Furthermore, the influence of the TiN bottom electrode is evident from this measurement, which shows a peak at 36.7°.

3.2 Fabrication of Fe-RFETs

The fabrication method used is a top-down device approach. The starting point for the fabrication is a silicon-on-insulator substrate consisting of a 20 nm thick unstrained (100)-oriented Si device layer on a 100 nm thick buried SiO_2 oxide (BOX) and a 500 μm thick lightly doped Si handling layer (substrate). It noteworthy that the lightly doped layer is also after the structuring of the nanosheets a distinct characteristic of the device layer. In Figure 3.6 (a) is an illustration of the corresponding SOI wafer, whereas (b) is the corresponding cross-section.

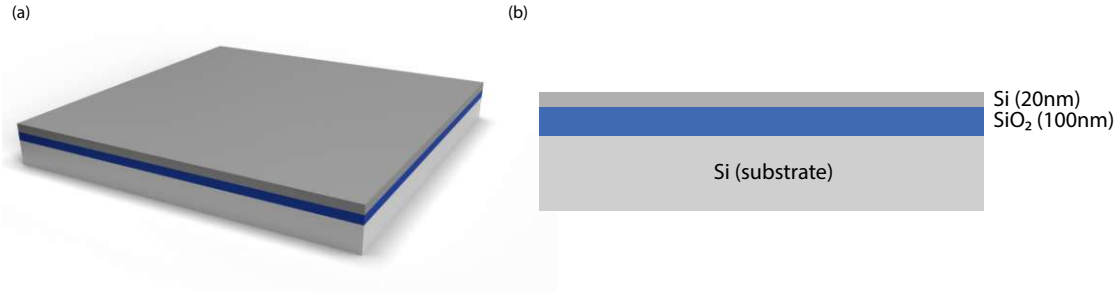

Figure 3.6: *SOI wafer stack. (a) 3-D illustration (b) Cross-section with thicknesses of the stack*

Several steps are necessary for fabricating the ferroelectric RFET (Fe-RFET) nanosheet structures, which are generally categorized as lithography, sputtering, deposition and etching. It should be noted that Fe-RFET structures can also be created with a bottom-up approach using nanowires. The process steps of this thesis are listed below and can be referred to the graphical representation in Figure 3.7.

1. Structuring of the silicon nanosheets
   (a) Lithography (laser writer)
   (b) Reactive-ion etching (RIE)
2. Surface passivation: Formation of the interfacial gate-dielectric
3. Atomic layer deposition (ALD): Formation of the ferroelectric gate-dielectric
4. Structuring of the top-gates
   (a) Lithography (laser writer (STG/DTG)/E-Beam (TTG))
   (b) Sputtering/Evaporation deposition of top-gate stack
   (c) Lift-off

5. Post Metal Annealing (PMA)/Crystallization annealing

6. Structuring of the source/drain (S/D)-pads

   (a) Lithography (laser writer)

   (b) Removal of the dielectric stack at the S/D contact area

   (c) Sputtering of Aluminum

   (d) Lift-off

7. Formation of the metal-semiconductor-metal heterostructure through an annealing step

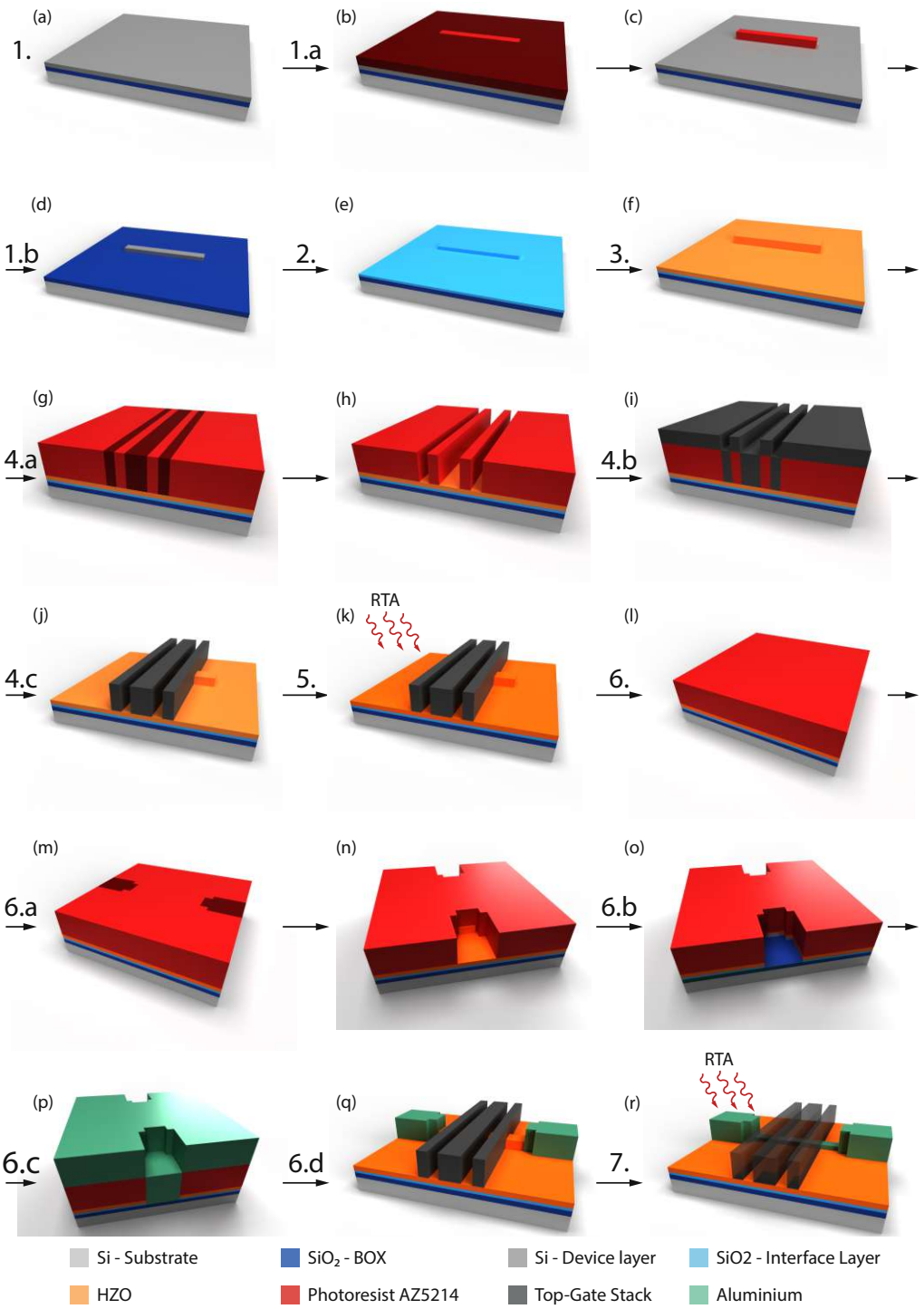

Figure 3.7: *Fabrication steps for the Fe-RFET with the indication following the listing above it. Adapted from [47]*

Silicon Nanosheet Structuring

Laser lithography is employed to define the Si nanosheet structures. This process step is divided into exposure and etching, 1.a and 1.b respectively, depicted in Figure 3.7 (b) to (d). In order to achieve this, the image-reversal photoresist (AZ5214) is evenly applied through spin coating and baked at 100 °C for 60 seconds. The structures were exposed with a laser writer "MLA150" from Heidelberg Instruments, the result is shown in Figure 3.7 (b). The photoresist that was exposed is removed using the developer AZ726MIF and rinsed with water. The actual patterning of the SOI substrate is addressed in process step 1.b, which employs the reactive ion etcher "PlasmaPro100 Cobra" manufactured by Oxford Instruments. The etching procedure uses SF_6/O_2 mixture for 50 seconds. The remaining photoresist is stripped with plasma cleaning and an acetone bath. The final nanosheet structures have a width of approximately 500 μm, depending on the quality of the laser writers exposure.

Interlayer Gate-Dielectric Formation

In the second step, a SiO_2 passivation layer is deposited, shown in light blue in Figure 3.7 (e). First, the native SiO_x is eliminated by a 3-4 second immersion in HF, known as Buffered Oxide Etch (BOE). This process leaves the surface hydrophobic, indicating that the process has been successful.

The subsequent step differs for the first sample from the others. For the first sample, a 5 nm thick thermal SiO_2 was deposited via dry thermal oxidation at a temperature of 900 °C for three minutes in O_2 and N_2 atmosphere. Whereas the other samples are based on a chemical SiO_2 oxide layer and its necessary process steps are explained in more detail.

RCA-2 cleaning, also known as Standard Clean-2 (SC-2), was developed by Werner Kern [112] in the RCA laboratories in the 1960s and is commonly used as a process to remove metal ions from silicon wafers. Decontamination relies on a process of sequential oxidative desorption and complexation with H_2O_2-HCl-H_2O, in accordance with the explanation given in [113]. This process results in a thin oxide layer - which offers a very low interface trap density [114] - covering the surface of the silicon wafer through oxidation. The thickness of this oxide layer, determined using an ellipsometer, is approximately 1 nm for the work in this thesis.

The procedure requires 6 parts water (H_2O), 1 part 27% hydrogen chloride (HCl) and 1 part 30% hydrogen peroxide (H_2O_2). To begin, DI water is poured into a Pyrex glass (borosilicate glass with low thermal expansion), followed by careful addition of HCl. The mixture is heated on a hotplate to 70± 5 °C. Once the solution reaches this temperature, the vessel is removed from the hotplate and H_2O_2 (30%) is added. After waiting for 1-2 minutes, the solution is then ready for use. The sample is left in the solution for 10 minutes. Finally, the sample is rinsed with clean deionised water. [113, 115, 116]

Ferroelectric Gate-Dielectric Formation

The third step concerns the growth of the ferroelectric layer by atomic layer deposition, as shown in light orange in Figure 3.7 (f). Note that at the point of deposition, HZO is amorphous, meaning that it lacks ferroelectric characteristics.

The technique for creating thin HZO layers is discussed in the Subsection 2.1.3. The ALD system at hand is the Beneq TFS200 model that incorporates a thermal head.

It should be noted that in this selection of literature [117–119] the enhanced remanent polarization due to ZrO_2 seed layers is pointed out. For this study, a thin (2 cycles) bottom seed layer was used. A framework of optimization resulted in thinner layers from one sample to the next in order to enhance the ferroelectric effect. Comprehensive results are outlined in Chapter 4. The process parameters are given in the Table 3.1.

Parameter	Value
Process temperature	250 °C
TEMAHf temperature	90 °C
TEMAZr temperature	80 °C
TEMAHf pulse time	0.5 s + N2 Preloading (1.5 s)
TEMAZr pulse time	0.5 s + N2 Preloading (1.5 s)
H_2O pulse time	0.175 s
N_2 purge time	2 s
Thermalization time	3-5 min

Table 3.1: *Processparameter for the HZO thin film*

Top-Gate Structuring

Different metals were used for the top gate (TG) stack depending on the sample. In general, titanium nitride (TiN) or tantal nitride (TaN) electrodes are mostly used, see [120–125] only to mention some of them. Park et al. state that the oxidation of nitride electrodes such as TiN and TaN is another critical extrinsic factor that can affect the ferroelectric properties of the doped HfO2 thin films [14]. A comparison between the TiN target and palladium (Pd) revealed that palladium had a higher yield of test samples with ferroelectric behavior, which is discussed further in Chapter 4. Consequently, the first and second samples were fabricated with palladium top-gates. Additionally, the top-gate for the third sample was fabricated with Ti(N) deposited from a titanium target in an N_2 plasma. Finally, based on the theory of scavenging effects - see [126] - the fourth sample, a Ti(N)/Ti/Pd stack, was designed. The "Plassys MEB550S" e-beam evaporator was used to deposit titanium (Ti) and Pd, while the "Creavac CREAMET 750" sputter was used for Ti(N). Note that in Figure 3.7 for simplicity, only one color was used for the respective gate stacks.

In addition, depending on the width of the TG structure, a different lithographic exposure

method has to be used. For single and dual top-gates (STG/DTG), laser writing was used, while for triple top-gates (TTG), electron beam lithography (EBL) was used. The photoresist used for EBL is a polymethylmethacrylate (PMMA) resist (AR-P 679.04). The sequence of process steps 4.a for the lithography, 4.b for the deposition of the respective TG material stack and 4.c for the lift-off step is shown in figures (g), (h), (i) and (j).

It is important to note that the selection of top-gate material has an impact on the dominant carrier characteristics due to the different work functions. Titanium nitride (TiN) is a suitable material with a workfunction range of 4.2 eV - 4.5 eV [127]. Different work functions can induce a band bending in the semiconductor, resulting in a prominent p-type characteristic at 0 V instead of a totally symmetric behavior, as it is desired for a RFET. In contrast, palladium (Pd) exhibits a predominately p-type property due to its high work function, which is measured at 4.95 eV[128] and calculated at 5 eV [129]. Consequently, its Fermi level pinning is located near the center of the Si valence band.

For sample 2, which has chemically grown SiO_2 and Pd top gates, additional gate structures were fabricated by electron beam lithography (EBL) after completion of the fabrication steps presented here, in order to investigate the influence of ferroelectricity without the process of crystallization annealing, which will be explained in the next step. Due to the smaller feature size of EBL, the common material combination of titanium (Ti) - as adhesion layer - with gold (Au) was used, since this process is well known and reliable and the lift-off is straightforward. The results of this experiment are presented in Chapter 4.

Crystallization Annealing

It should be noted here that for the first sample, the process of thermal Al-Si exchange and HZO crystallization was performed concurrently, but since it led to the expansion of the nanosheet and its destruction in the subsequent sample, these steps were separated, which also brings the advantage of having two different temperature profiles adapted to the respective requirements.

This annealing step is necessary for the crystallization of the HZO layer in order to obtain its ferroelectric phase, as shown in Figure 2.5 in the Subsection 2.1.3. For this purpose, the UniTemp UTP 1100 rapid thermal annealing (RTA) oven was used. In this process, the sample is heated in the quartz chamber of this RTA furnace with 18 kW infrared lamps within 60 seconds to 530 °C for the first sample with thermal oxide and Pd TG, the second with the chemical oxide TG within 120 seconds also to 530 °C and the last two samples for the same duration but at 550 °C and then cooled to room temperature. This process is indicated as 5. and shown in the Figure 3.7 (k), where it should be noted that also here the HZO performs the change from amorphous to crystalline with marked light orange to dark orange color. To avoid oxidation and other residual reactions, the process is performed in a nitrogen N_2 atmosphere. As stated in [14], it must be additionally mentioned that especially for ferroelectric thin films, annealing in an atmosphere containing H_2 significantly degrades their ferroelectric properties due to H-incorporation. Furthermore, annealing in

an oxidizing atmosphere can affect both ferroelectric and metallic films. As mentioned above, for ferroelectric $Hf_{1-x}Zr_xO_2$ thin films, TiN is the most commonly used electrode material, which can be (partially) oxidized to TiO_xN_y or even TiO_2. Therefore, it is crucial to comprehend the impact of annealing atmosphere to enhance the ferroelectric properties of HZO thin films.

Aluminum-Source/Drain-Contact Structuring

To pattern the source (S) and drain (D) pads that define the aluminum (Al) of the metal-semiconductor heterostructure used in this work, the following steps must be carried out. Starting with step 6 of the process, the photoresist is spin-coated for lithography. Following this step, the structure are defined with the laserwriter as shown in Figure 3.7 (m), with the pads marked in dark red. The following step is the crucial etching of the HZO and SiO_2 layer to expose the underlying nanosheet. This step is critical as under-etching or insufficient etching can result in longer-than-expected annealing for the formation (diffusion) of the Al-Si transitions or the process may not take place at all. Test etchings were performed to determine etch rates by interpolating multiple etchings. This yielded an etch rate of 1.5 nm/s for SiO_2 and 0.06 nm/s for HZO. Therefore, the etch rate of SiO_2 is 25 times greater than that of HZO. This indicates the complexity and difficulty of designing an etch with appropriate depth with this given selectivity. For etching, a physical method was employed utilizing an SF_6/Ar mixture with the reactive ion etcher "PlasmaPro100 Cobra". Next a 120 nm thick aluminum layer (green) is deposited using sputtering (Creavac CREAMET) following process step 6.c as illustrated in Figure 3.7 (p). Further, the excess aluminum must be removed through a lift-off process by subjecting the photoresist (red) to an acetone bath at a temperature of 60 °C, and additional sonication if required, see Figure 3.7 (q) for the resulting process step 6.d.

Monolithic Metal-Semiconductor-Metal Heterostructure Formation

The final step is to create the two semiconductor junctions by employing a thermally-induced diffusion process using a rapid thermal annealer (RTA) to form a monolithic metal-semiconductor-metal heterostructure. The RTA process was previously explained in a similar manner in process step 5 for the crystallization of the ferroelectric layer. The annealing is performed at a temperature of 500 °C in a nitrogen atmosphere N_2 and continued at successive time intervals until the desired result is achieved. After each annealing process, the samples undergo inspection via optical microscope. The objective is to move the Al-Si interfaces underneath the previously fabricated top-gates by estimating the diffusion mechanism. However, this approach is disadvantageous because for optimal formation of ferroelectric phases in the crystal structure, the material must also be subjected to strain via a Top-Gate (TG). This prohibits the subsequent adjustment of uncontrollable process events, such as non-uniform diffusion, by positioning the top gates accordingly. Experiments were conducted on the second sample (chemical oxide and palladium TG) to examine the impact of a subsequently added gate. Chapter 4 and the final structures in the corresponding results are referred to in this context. The process

of diffusion is illustrated in Figure 3.7 (r). Note that the oxide layers have been excluded for visibility in the figure, but are present in the real case, as can be seen in the previous Figure 3.7 (r).

The 3-D illustration of the final structure of the triple-top-gate (TTG) RFET shown in (a) and the corresponding cross-section shown in (b) and also in the top view in (c) of the Figure 3.8. It should also be noted that the SiO_2 and HZO layers in the channel area are not shown in the 3-D figure for clarity, while they are shown in the 2-D structure, except for their scale.

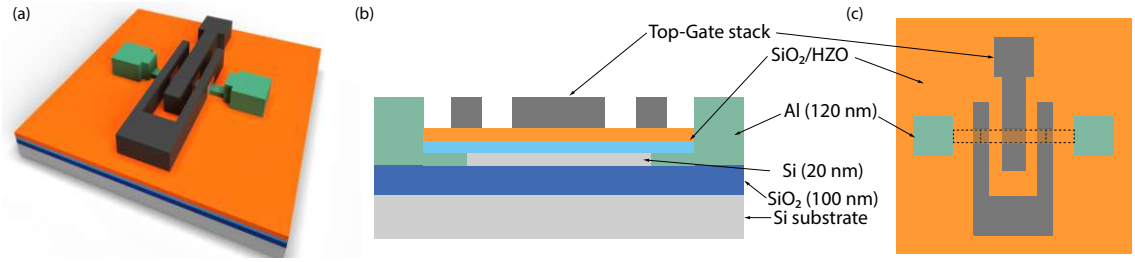

Figure 3.8: *Fabrication steps for the ferroelectric RFET structure according to the listed process steps.*

3.3 Characterization of Fe-RFETs

To adequately characterize the Fe-RFET, it is necessary to measure the transfer characteristic, output characteristic, and PG sweep characteristic, including their temperature-dependent effects. In addition, pulse measurements are performed to analyze the ferroelectric behavior associated with polarization switching. A detailed explanation of these measurements is provided subsequently.

The measurement setup used was a Lakeshore PS-100 probing station with a Keysight B1500A analyzer. To eliminate external influences such as light irradiation or particle contamination for electrical characterization, the samples to be measured are placed in a dark box that can be vacuumed, cooled, and heated, which is a necessity for temperature-dependent measurements. The setup has four source-measure units (SMUs) with which a specific voltage can be applied and the resulting current can be measured. The measuring resolution of the model is in the femto-ampere range. The needles can be precisely placed on the contact pads using an optical microscope. This ensures proper contact. The measurement configuration for STG, DTG and TTG is shown in Figure 3.9 with the equivalent circuit diagrams of the SMUs.

Due to the symmetry of the device, there is no fixed choice between the drain and source pads. The source and drain voltage levels can be independently set, depending on the investigation. V_{DS} refers to the voltage drop relative to V_D and V_S for drain and source, respectively. A symmetrical voltage assignment thus implies V_D = - V_S. The current through the channel is represented by I_D. This is due to the fact that in ideal structures

lacking leakage currents, the source current equals the drain current. It is important for the current at the gate to be negligible in order to prevent oxide leakage and reduce the likelihood of breakdown, ultimately resulting in device failure.

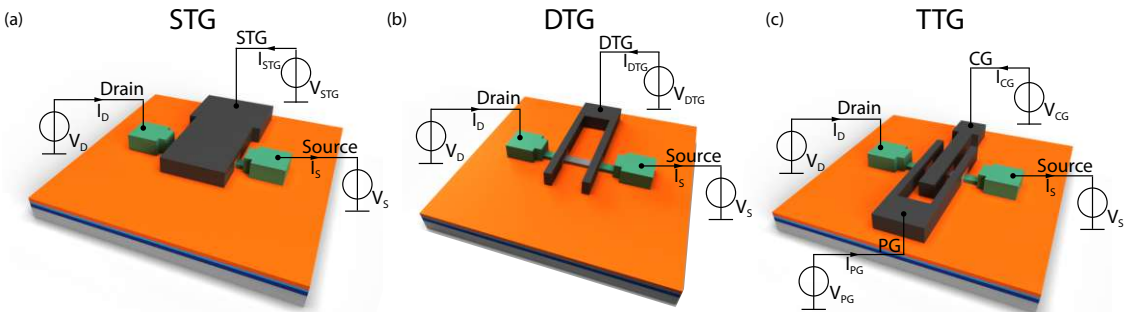

Figure 3.9: *Measurement setup for STG (a), DTG (b) and TTG (c).*

3.3.1 Transfer Characteristics

The transfer characteristic ($I_D V_G$) is a measurement in which the gate voltage V_G is continuously varied and the resulting absolute drain current I_D is determined, while fixing the bias for the source and drain. This current is typically represented in a logarithmic scale because of its wide range of values. From the measured curve, key parameters such as the on/off-current ratio, the threshold voltage V_{th} and the inverse sub-threshold slope (STHS) for both charge carrier types can be determined and used for qualitative comparison. It also represents the ability of the gate-stack to control the current flow.

In case of a STG structure this results in a ambipolar current behavior, meaning both p- and n-type configuration depending on the applied voltage, like it is the case for a Schottky Barrier FET (SBFET). In the DTG approach, selective voltage switching of the PG can mainly prevent this ambipolarity. However, it should be noted that using the back gate (silicon handling layer) as CG, as implemented in this thesis, has the disadvantages that adsorbates can form on the surface between the PGs, since this area is not covered, that the energy landscape cannot be tuned as effectively, since the interfaces of the metal-semiconductor junction are also influenced by the electric field, and that a large capacitance results due to the large area of the back gate. Whereas a TTG approach eliminates these problems by a separate CG directly above the channel and thus between the two PGs. For the respective p-mode operation and n-mode operation a negative and a positive voltage must be set.

A single-sweep measurement involves sweeping the gate voltage from the off to the on-state of the transistor once. In contrast, a double-sweep measurement records the curve in both directions. This method effectively shows the charging effects during the measurement, enabling the assessment of the quality of the oxide and ferroelectric layers with respect to their interface traps.

In addition, transfer characteristics were conducted at various temperatures, beginning at

22 °C and increasing once by 25 °C to reach 47 °C, followed by increments of 20 °C up to 127 °C. From the I/V(T) approach of Schroder [130], which is based on the theory of thermionic emission and on the theoretical assumptions for the experimental extraction of the activation energy from "Metal-Semiconductor Contacts" by E.H. Rhoderick and R.H. Williams, a script for the evaluation of the effective Schottky barrier eSBH and the effective activation energy eE_A was developed in the master thesis of Andreas Fuchsberger [47]. Using this script, the plots for the effective activation energy were created, which are discussed in detail in Chapter 4. These plots are in the form of 2-D maps with a color scheme that highlights the values of the effective activation energy. The axes represent the bias voltage V_{DS} and the control gate voltage V_{CG}.

Pulsed Operation

In contrast to sweep measurement, where the voltage value is measured continuously, pulse measurement applies successive pulses at predetermined time intervals and measures the current within these intervals. This has the advantage of better counteracting the charging effects of the device.

3.3.2 Output Characteristics

The output characteristics (I_DV_D) are determined by analyzing the drain current I_D as a function of the bias voltage V_{DS} for different values of the control gate voltages V_{CG} and V_{TG} in general. This yields a distinctive array that can be presented as a 2-D map corresponding to the drain current values matching the color scheme.

Note that the slope provides information about the contact resistance. As for the transfer characteristic, the bias voltage V_{DS} is presented as either symmetric with V_D = - V_S or asymmetric, depending on the analysis. In addition, the temperature dependency is shown using the same temperature steps as for the transfer characteristic.

3.3.3 PG Sweep Characteristics

In the case of the PG sweep characteristic, the control gate voltage V_{CG} is swept in each case for a fixed PG voltage level V_{PG} and the influence on the drain current I_D is measured. From this, the behavior for both modes (n-type and p-type) can be obtained. This array of drain curves can again be interpreted as a 2-D map with the corresponding color scheme in which the two types of operation as well as the off and on regions can be determined. In addition, the bias voltage V_{DS} can again be used to induce symmetrical or asymmetrical behavior.

3.3.4 Pulse Measurements

The purpose of the pulse measurements is to investigate the influence of positive and negative pulses on the transfer characteristics. By identifying any shift in the curve and

alteration of the on-currents due to barrier tuning, as outlined in Section 2.4, it is possible to determine whether there is a ferroelectric or charge trapping behavior dominant.

To achieve this, four methods were utilized: set-pulse, pulse cycles, retention and endurance, each of which is detailed below.

Set-Pulse

Set pulses are constant successive pulses with respect to their sign, as shown graphically in Figure 3.10. According to Xi et al. [88] who have investigated a Fe-SBFET based on $NiSi_2$/Si Schottky barriers and integrated HZO as artificial synapses for neuromorphic applications, a partial polarization switching takes place by repeated pulses of the same type, which leads to a pronounced ferroelectric behavior due to the increasing domain polarization, which affects not only the channel but also the Schottky barriers.

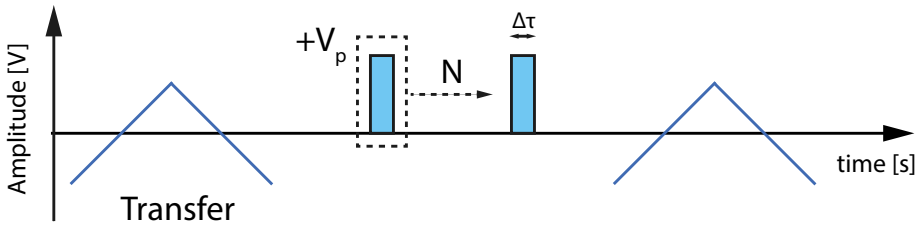

Figure 3.10: *Schematic of the set-pulse measurement with constant successive pulses of same sign, pulse height $|V_P|$ and pulse width $\Delta\tau$. Note that the pulse is illustrated with positive polarity, but negative polarity is also an equivalent condition.*

Pulse cycles

Unlike the set pulses, this method involves successive alternating pulse cycles. The polarity of the first pulse is the same as the polarity of the last pulse, and N represents the number of pulse pairs. Figure 3.11 schematically illustrates this fact.

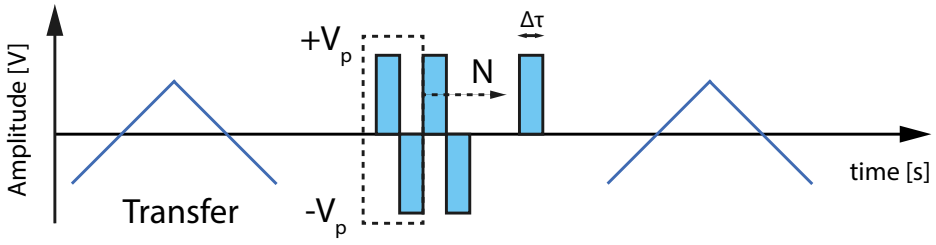

Figure 3.11: *Schematic of the pulse cycle measurement with the same pulse height $|V_P|$ and pulse width $\Delta\tau$*

Retention

Retention is a significant parameter in determining the quality of the HZO layer and thus its ferroelectric properties. After an initial measurement for the transfer characteristic

the pulse cycle measurement is applied, followed by repeated monitoring of the transfer characteristic over a specified time interval is used to measure this parameter. The drain current at $V_{CG} = 0$ V can then be determined from these collected measurement data.

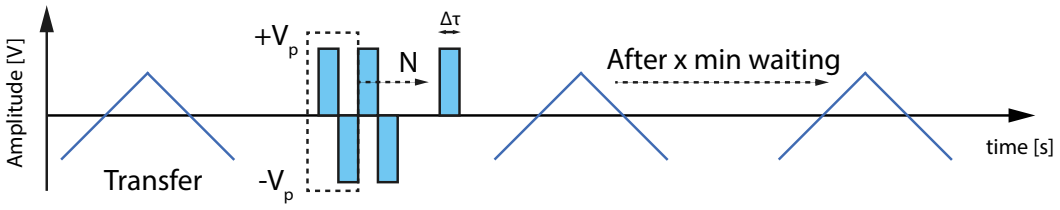

Figure 3.12: *Schematic of the retention measurement. With x as a increasing variable.*

This procedure for obtaining the current is called the constant voltage criterion, where a voltage value is selected and the corresponding current value is determined from it to compare the first determined value with the subsequent measurements, resulting in the retention plot.

Endurance

Endurance testing is the repetition of pulse cycle measurements and the subsequent comparison of the influence of the current characteristic of the respective polarization state. This is also a significant quantity for the determination of the deviation of the result after a certain number of state changes.

Chapter 4

Results and Discussion

Within this chapter, the final results and achievements are presented and discussed in detail based on the methods presented in Chapter 3. For the purpose of this thesis, the obtained findings of the four fabricated Fe-RFET devices are discussed and the ongoing optimization process is clearly outlined with various test samples based on metal-ferroelectric-metal (MFM) and metal-ferroelectric-insulator-semiconductor (MFIS) structures.

4.1 Fe-RFET Devices

To attain Fe-RFET, several iterations are required to determine which influences have a positive or negative effect on the achievement of the desired goal. An SOI wafer serves as the foundation for each sample. However, there are differences in the passivation layer, the HZO layer thickness and the top gate material. Therefore, the devices produced and analyzed are

- Sample 1 - Thermally grown SiO_2 with Pd top-gates
- Sample 2 - Chemically grown SiO_2 with Pd top-gates
- Sample 3 - Chemically grown SiO_2 with Ti(N) top-gates
- Sample 4 - Chemically grown SiO_2 with Ti(N)/Ti/Pd-stack top-gates

in the following. The specifications and the corresponding measurement results are given in the individual subsections. In order to provide a comprehensive overview of the approach taken in this project, the different investigations with MFM and MFIS structures are presented within each iteration step. Prior to the fabrication of the first device structures,

the top-gate material as well as the temperature dependency is analyzed based on those test samples. As stated in the Subsection 3.2, titanium nitride (TiN) is a commonly used material as an electrode for the formation of ferroelectric phases in e.g. HZO due to mechanical stress and strain. An MFM structure with both a TiN bottom and top electrodes was investigated for its temperature behavior to form these particular phases and analyzed using C-V measurements as shown in Figure 4.1.

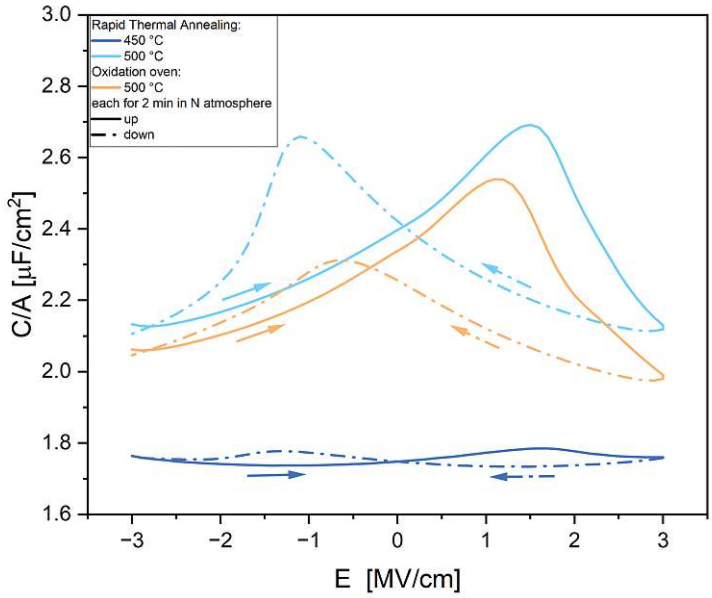

Figure 4.1: *Comparison of the thermal activation depending on the temperature and heating/cooling-rate. C-V curve with its distinct butterfly-shape representing a ferroelectric behavior*

The importance of the temperature profile lies in both its magnitude and the rate of transition from the initial to the final value of the temperature profile. During rapid thermal annealing (RTA), the temperature quickly transitions from room temperature to the designated maximum and back. This steep slope allows for crystallization within a specific temperature range where orthorhombic phase formation is more likely. Conversely, with a slow heating or cooling rate in the oxidation furnace, an extended intermediate temperature can produce incorrect phase formation.

As palladium (Pd) is known to induce crystallization in a ferroelectric phase [131, 132], it was investigated as a top gate material. A detailed comparison between the TiN target and palladium (Pd) showed that the latter produced a higher yield of test samples with the desired ferroelectric behavior. Therefore, it was decided to use this material for the initial device. For illustrative purposes, a representative example of the two electrode materials was chosen in Figure 4.2. As explained in Subsection 3.1.1 the counter-clockwise hysteresis is to be expected for a ferroelectric layer, while a clockwise hysteresis is expected in other

cases such as trapping. It can be observed that palladium exhibits a counter-clockwise behavior leading to the crossover point at approximately 1.8 $MVcm^{-1}$.

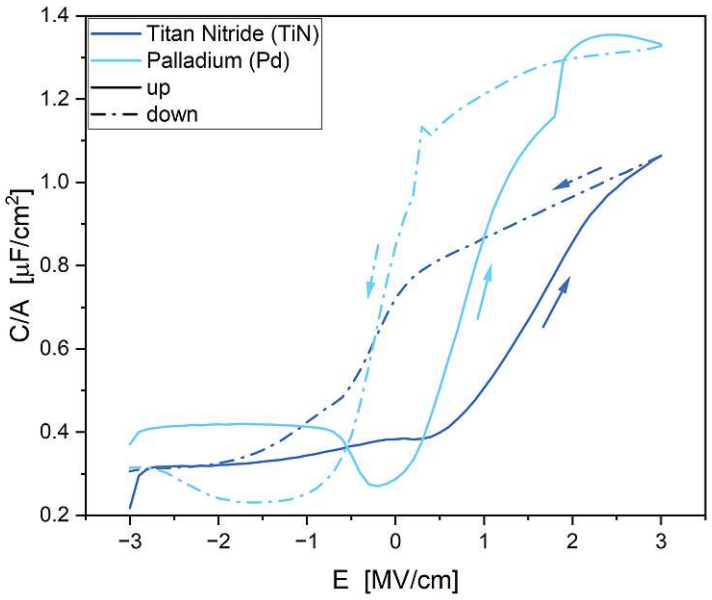

Figure 4.2: *C-V comparison between the titanium nitride (TiN) target and palladium (Pd) as potential top-gate materials.*

Based on this investigations temperature-dependent measurements were taken for an MFIS structure, which are shown in Figure 4.3. The MFIS structures have been used to model the final device stack. Subfigure (a) depicts the three temperatures in the initial C-V cycle, while (b) shows the evolution at the fiftieth cycle. The coercivity experienced an increase, indicating a "wake-up" effect.

4.1.1 Sample 1 - Thermally grown SiO_2 with Pd top-gates

The stack of the first sample consists of a 5 nm thermally grown SiO_2 followed by a 10 nm thin HZO layer applied on the SOI wafer discussed in the Section 3.2. Aluminum (120 nm) is utilized as the material of choice for the source and drain pads, additionally forming the metal-semiconductor (MS) heterostructure through a thermally induced Al-Si exchange reaction. As previously noted, the top-gate electrode consists of Palladium (70 nm). Annealing was conducted at 530 °C for 60 seconds for the formation of MS transitions and crystallization of HZO. The devices fabricated are arranged in single top-gate (STG) and double top-gate (DTG) fashion as shown in Figure 4.4.

The first sample was fabricated based on an already established, reproducible and reliable RFET process using a comparatively SiO_2 oxide thickness as gate dielectric. For reference, see the work of Lukas Wind [22] and Raphael Behrle (formerly Böckle) [87]. The aim of

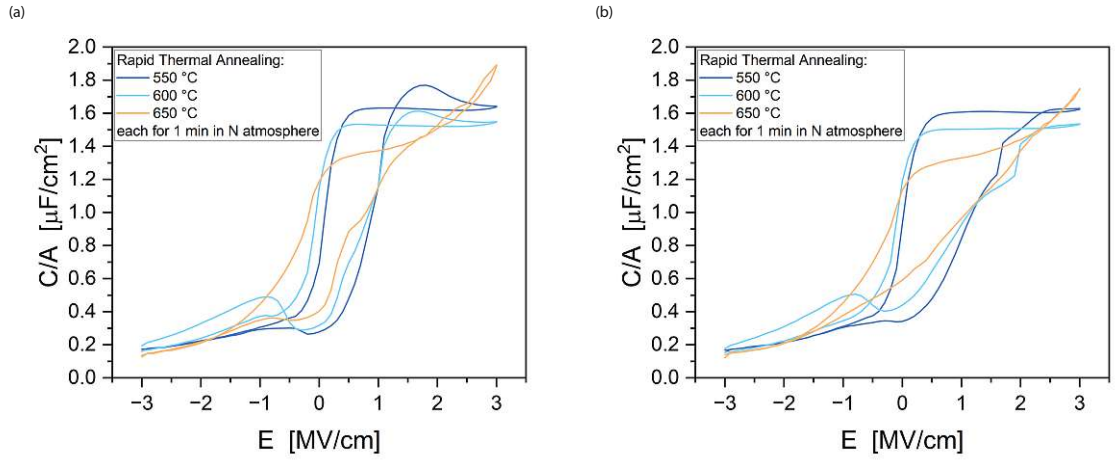

Figure 4.3: *Thermal activation comparison with a Pd MFIS structure. (a) depicts the three temperatures in the initial C-V cycle, while (b) shows the evolution at the fiftieth cycle.*

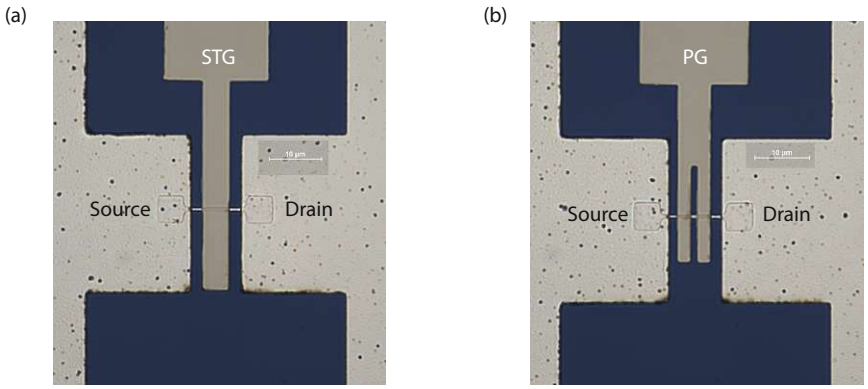

Figure 4.4: *Optical microscope picture of fabricated sample with thermally grown SiO_2 and Pd top-gates. (a) STG structure with one gate covering both MS transitions, (b) DTG configuration with the top-gate as polarity-gate (PG) and the back-gate as control gate (CG).*

this sample was to incorporate an additional layer (HZO) while preserving the remarkable reconfigurable behavior.

Several measurements were conducted to determine the impact of the additional HZO layer, including transfer, output, and PG sweep characteristics, as well as pulse measurements on both the STG and DTG devices, as shown below. Furthermore, the effective activation energies, calculated using the temperature measurements, as described in Subsection 3.3.1 are shown.

Transfer Characteristic

The transfer characteristics provide a good first estimate of the device behavior and an understanding of the degree of controllability by the gate. Specifically, it highlights the

switch-on and switch-off currents, as well as the symmetry of the two operating modes (p- and n-type). The outcomes of the characteristic for both STG and DTG setups will be discussed individually. It is important to emphasize that all measurements were conducted at room temperature and under atmospheric ambient conditions, unless otherwise stated.

STG

The STG devices are anticipated to exhibit an ambipolar SBFET characteristic because the gate influences both metal-semiconductor junctions at the same time, leading to no preference for suppression of a particular carrier type when driven at the same voltage level. The top-gate voltage V_{STG} is swept at 4 V in a "double" measurement, yet the hysteresis of this sample is practically absent, as can be seen in Figure 4.5. This is a general indication for a low interfacial trap density. This figure additionally illustrates that the p-branch is enhanced by almost four decades compared to the n-branch. The constant positive shift of the threshold voltage, caused by fixed negative charges due to the integrated HZO, may be attributed to the additional integrated HZO. Furthermore, the use of palladium which has a higher work function than Ti/Au in the top gate stack results in another pinning of the barriers. Nevertheless, the best results for the inverse sub-threshold slope (STHS) of 63 mV per decade for the p-branch is nearing the conventional Boltzmann limit of 60 mV/dec at room temperature, indicating excellent controllability and thus lower power consumption, making it ideal for use as low-power devices. Compared to that, the n-branch only delivers a value of about 290 mV/dec.

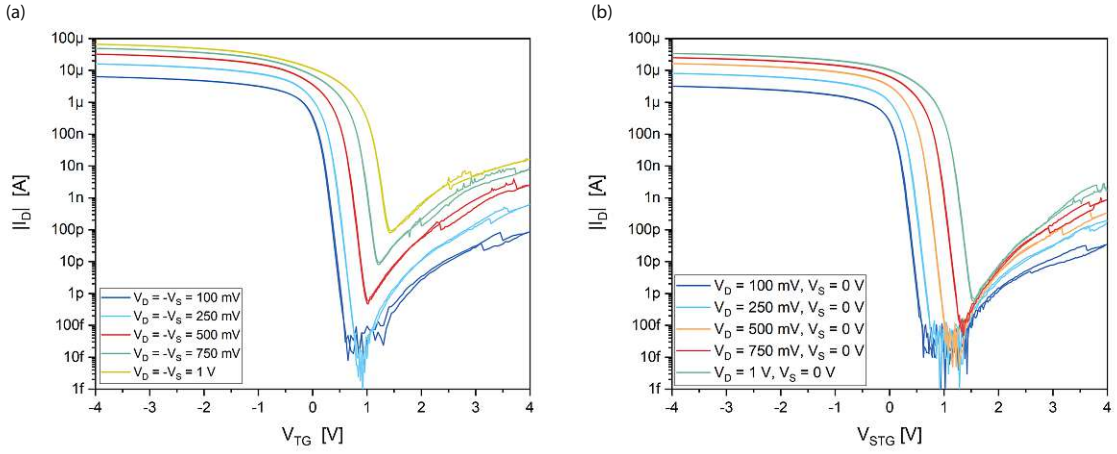

Figure 4.5: *STG transfer characteristic of sample 1 with different symmetric and asymmetric bias-voltages V_{DS}. (a) depicts the symmetric scenario with V_D = -V_S, while for (b) the asymmetric case with V_S fixed to zero can be seen.*

A bias-voltage sweep ranging from -2 V to 2 V was conducted with a gate-voltage range of 4 V in order to cover a wider spectrum, as shown in the Figures 4.6 (a) and (c) as conventional transfer characteristics and (b) and (d) as colormaps, respectively. These graphs unambiguously display the offset, the magnitude of the on- and off-currents, as well as the asymmetric behavior with a fixed drain or source voltage.

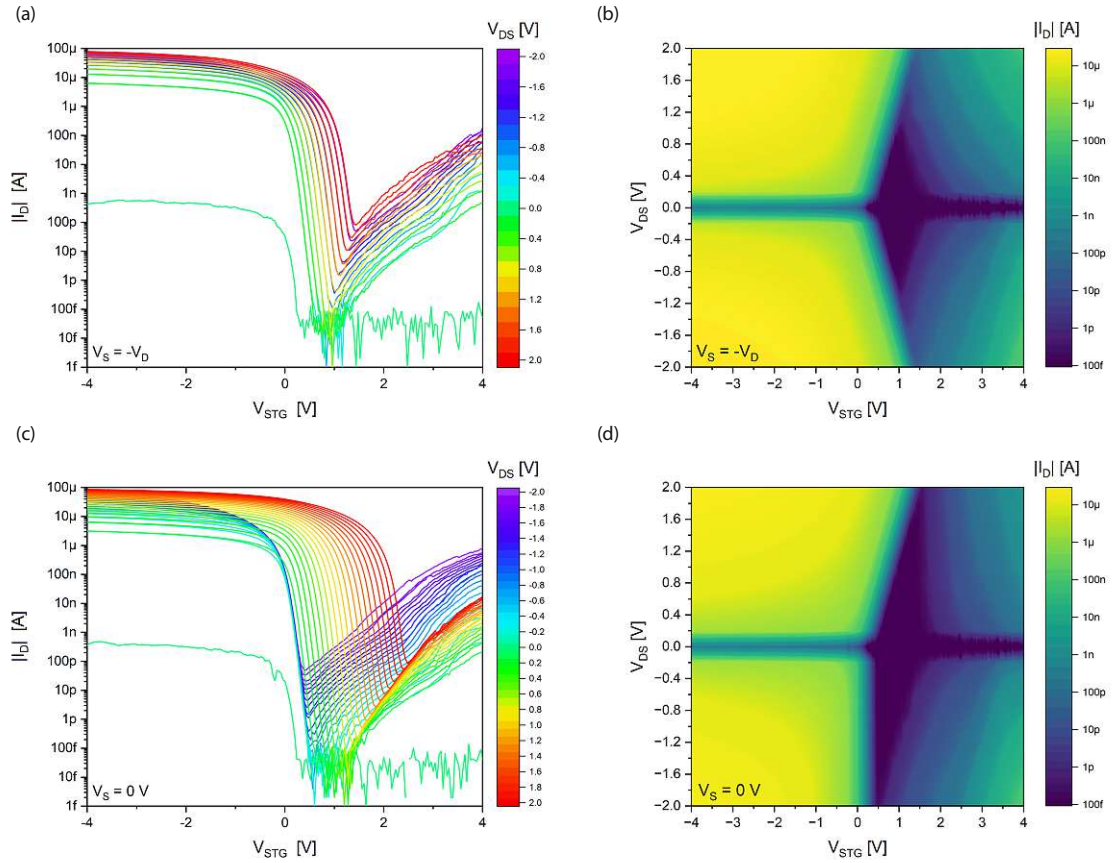

Figure 4.6: *V_{DS} sweep of STG transfer characteristic and corresponding colormaps. (a) and (b) depicts the symmetrical bias as (c) and (d) the asymmetrical behavior.*

The temperature dependence of the transfer characteristic is given in Figure 4.7 (a). The measurement started from room temperature up to 127 °C (400 K) with a symmetric bias of $V_{DS} = 1$ V. The top-gate voltage was set at 5 V, while the back-gate voltage remained at a fixed ground potential of $V_{BG} = 0$ V. The p-branch was observed to have a negligible effect on the temperature, while the n-branch displayed a consistent change over the logarithmic range. Furthermore, the off-state currents increase as the temperature rises, while the minimum point remains unaffected. For Schottky contacts and the n-branch, a rise in temperature leads to an increase in the on-current. This phenomenon is referred to as thermally activated transport. On the other hand, transparent contacts exhibit in general a decrease in on-currents at higher temperatures, which can be attributed to scattering as the primary cause of resistance. From Subfigure (b), the behavior can be visualized through the effective activation energy as a color map according to a temperature-dependent V_{DS}-sweep. The transparent region is colored dark red and shifts to dark blue when the effective barrier is greater. The blue box indicates the representative region for $V_{DS} = 1$ V. For values of V_{STG} greater than 0.5 V, energies deviating from zero can be seen and thus a temperature dependence takes place. Clearly, this behavior can also be

observed in the following colormap of the output characteristic. An inverse sub-threshold slope (STHS) of 115 mV/dec has been evaluated for V_{PG} = -6 V.

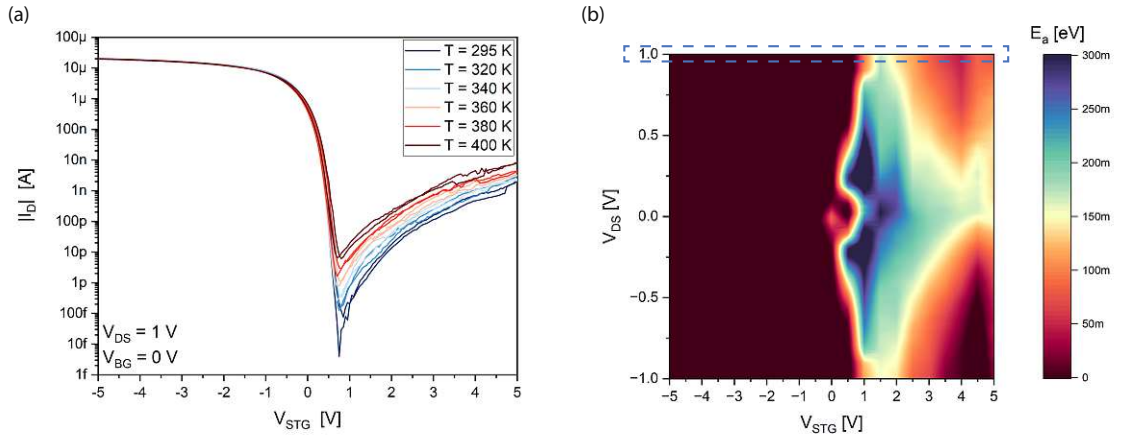

Figure 4.7: *(a) Temperature dependent investigation of the corresponding STG transfer characteristics starting from room temperature up to 127 °C (400 K). (b) Colormap for the effective activation energy based on a temperature-dependent V_DS-sweep. The blue box marks the representative area for V_{DS} = 1 V.*

DTG

Next, a look at the DTG structures is taken. The top-gate serves as the polarity gate (PG) and is used to determine the dominant charge carrier. For this particular sample, the back-gate functioned as the control gate (CG). Figure 4.8 once more demonstrates a good ratio of on-current to off-current and a symmetry of the threshold voltages is also evident. Increasing V_{PG} has a greater impact on the n-branch than on the p-branch. It appears that there is no further increase in the on-current at V_{PG} = -2.5 V . Furthermore, it is noteworthy that the n-branch saturates relatively early and corresponds to a constant current source from this voltage value on. Subfigure (b) illustrates the behavior of positive and negative V_{PG} at different biasing conditions. When the bias voltage is increased, the threshold voltage shifts to the right at first from V_{DS} = 200 mV to V_{DS} = 1 V, indicating that negative charges are present, and then shifts in the opposite direction (left) from V_{DS} = 1 V to V_{DS} = 2 V.

Furthermore, a PG sweep was performed to create a colormap. The color-coded representation in Figure 4.9 visualizes the varying magnitudes of the two regions.

As with the STG structures, the temperature dependence was investigated for the DTG. At first glance, in Figure 4.10, it appears as if the on-currents for V_{PG} = -5 V decrease with increasing temperature and increase for V_{PG} = 5 V. Nevertheless, it is important to note that the transfer curves shift, which may be attributed to charging effects. The respective effective activation energetic plots in Figure 4.11 demonstrate the observed behavior. Transparent barriers, signalized by an activation energy of 0 eV, enable carriers

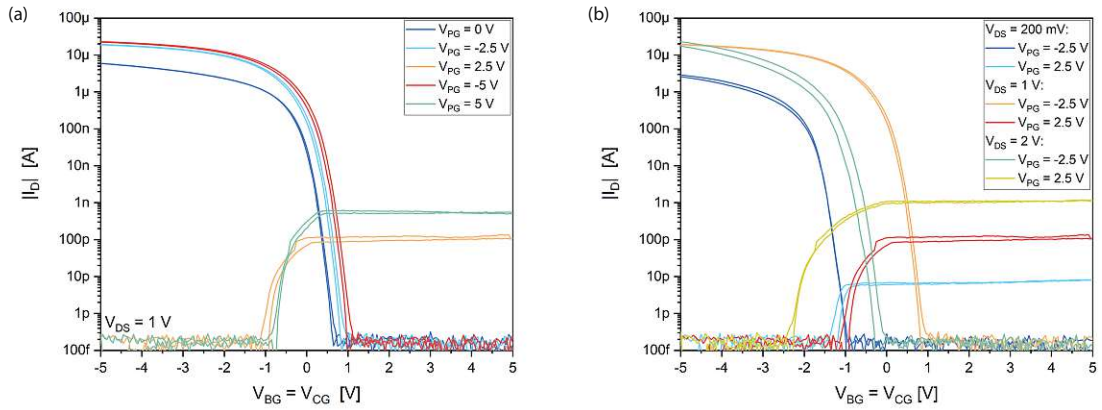

Figure 4.8: *DTG transfer characteristic of sample 1 with different polarity gate voltages V_{PG} (a) as well as with certain V_{DS} variations in (b).*

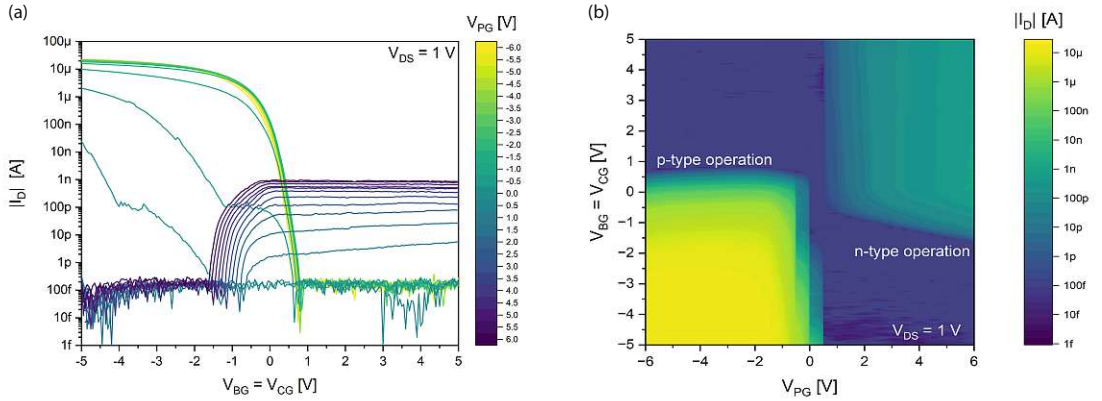

Figure 4.9: *PG-sweep of sample 1 for $V_{PG} = \pm 6$ V and $V_{CG} = \pm 5$ V (a) with the corresponding colormap (b) at $V_{DS} = 1$ V.*

to flow unhindered, while positive values of eE_a represent Schottky barrier characteristics and negative values can be regarded as ohmic behavior. Same as for the STG, this phenomenon is apparently noticeable in the temperature-dependent output measurement, as shown in the following output characteristics.

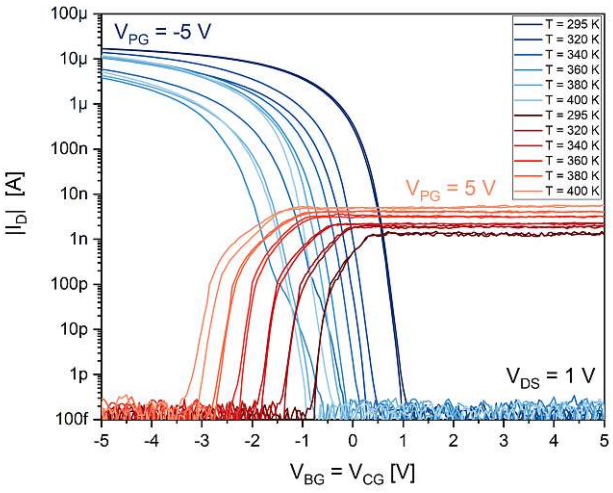

Figure 4.10: *Temperature dependent investigation of the corresponding DTG transfer characteristics starting from room temperature up to 127 °C (400 K) for $V_{PG} = \pm 5$ V.*

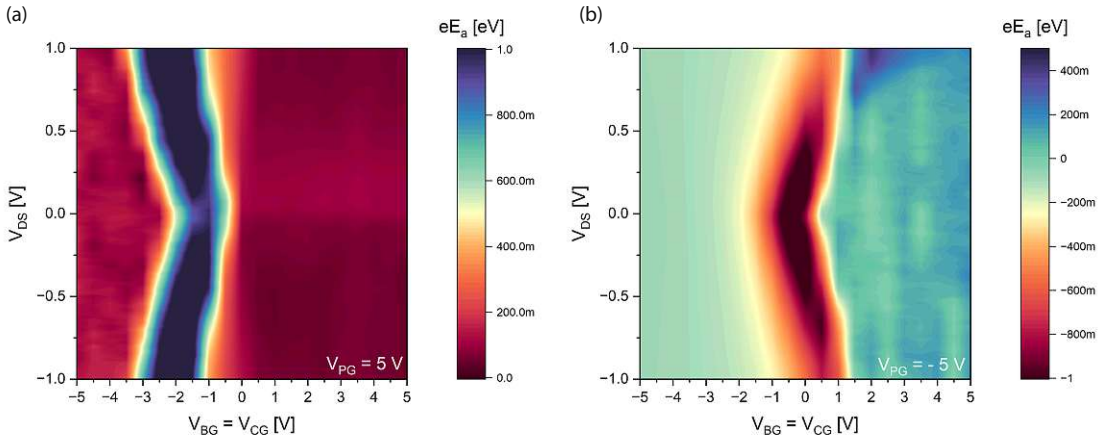

Figure 4.11: *Effective activation energy colormap for $V_{PG} = 5$ V (a) and $V_{PG} = -5$ V (b).*

Output Characteristic

STG

Figure 4.12 shows the output characteristic for symmetric V_D = - V_S and asymmetric bias-voltage with V_S = 0 V both linear (a) and (c) and logarithmic (b) and (d). V_{TG} = ±4 V was varied in 250 mV steps. As mentioned for the transfer characteristic, the ambipolarity of the STG devices can also be seen here. It can be seen that the n-type current, which occurs at positive TG voltages, is much lower than the p-type current, at negative TG voltages. Furthermore, the ohmic behavior is signaled by a linear trend of the output curves, while a Schottky contact is related to an exponential increase.

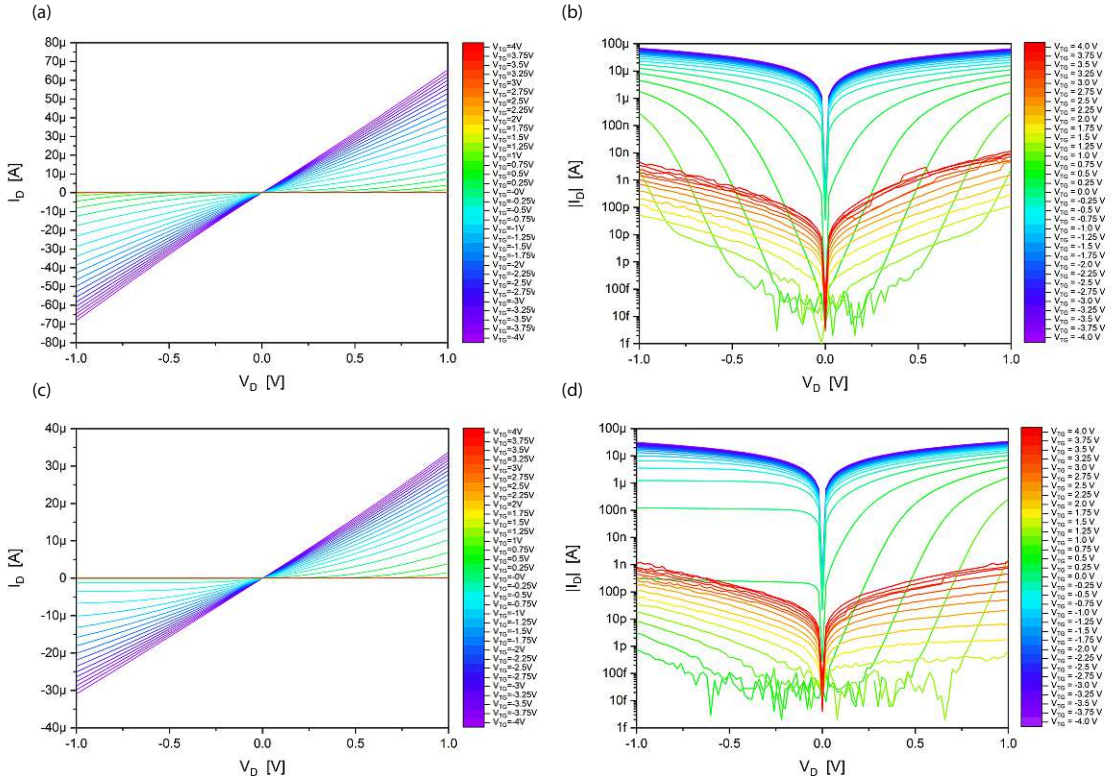

Figure 4.12: *STG output characteristic of sample 1. Subfigures (a) and (c) depict the linear representation for a symmetric V_D = - V_S and asymmetric bias-voltage with V_S = 0 V, whereas in (b) and (d) the logarithmic representation is shown.*

From temperature-dependent output characteristics, it is possible to extract specific colormaps that give a clear picture of how the devices behave. In Figure 4.13, these six representations have been combined. The p-branch, which has negative values of V_{STG}, exhibits hardly any changes, while the n-branch, with positive values of V_{STG}, shows an increase in current with rising temperature. This aligns with the behavior already discussed in the case of the transfer characteristic.

DTG

The identical approach of using colormaps for the respective temperature was also applied to the DTG structures. It is worth focusing on the plot of the effective activation energies again - see Figure 4.11 - whereby the shift can also be clearly seen.

Pulse Measurements

Pulse measurements were conducted to ascertain the ferroelectric characteristics of the sample. The theoretical foundation for the anticipated impact in both the STG and DTG

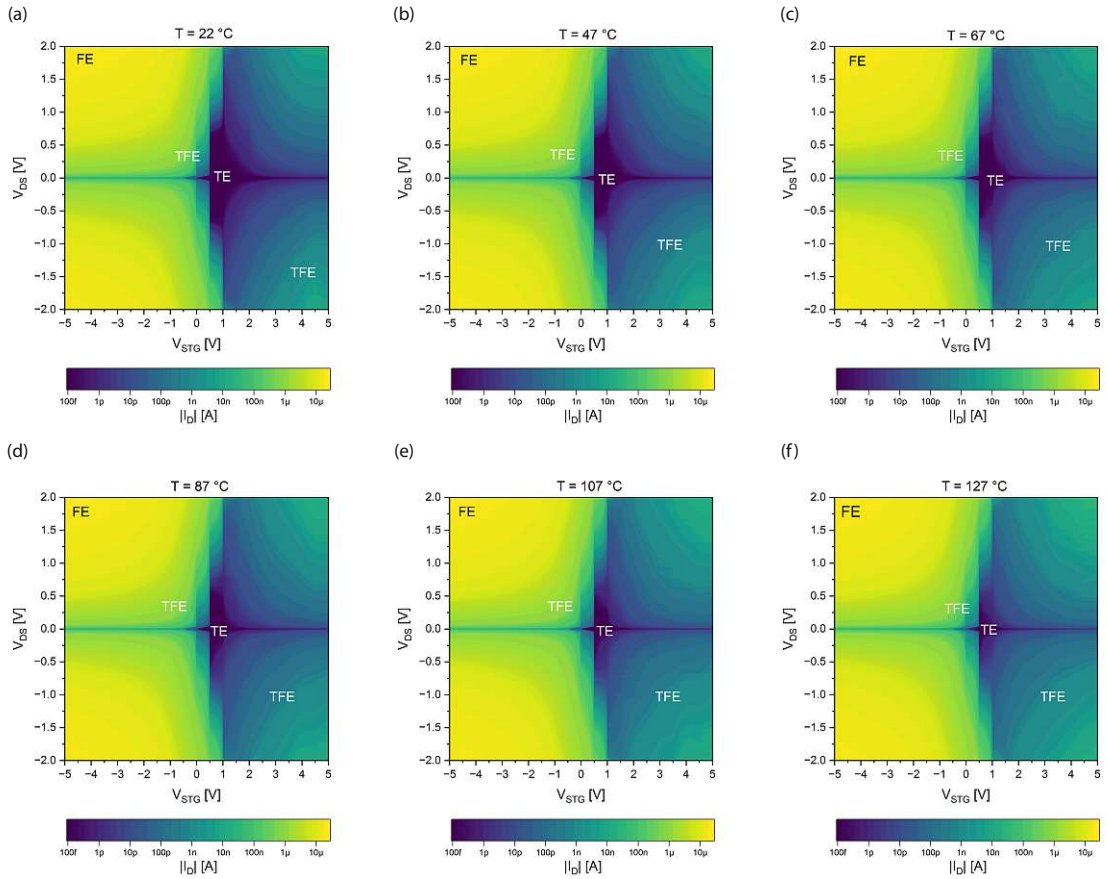

Figure 4.13: *Output characteristic as colormap from (a) to (f) with rising temperatures with the indication of the field emission (FE), thermal field emission (TFE) and thermal emission (TE).*

arrangements can be found in Section 2.4, but will be briefly mentioned again at the appropriate passages for explanation.

STG

For the results shown in Figure 4.15, a positive and a negative pulse of 8.5 V for τ = 10 ms are applied for Subfigure (a), resulting in trapping behavior as the transfer curves shift in the same direction as the sign of the applied pulse. Similar results were observed for shorter pulse-widths with a pulse-height of ±9.5 V, in Subfigure (b).

In conclusion, the devices are subject to limitations resulting from the integration of hafnium zirconium oxide (HZO) and palladium (Pd) as an additional layer and a new gate material, respectively. These limitations include the unequal symmetry of the on-currents of the p- and n-characteristic. Nonetheless, the devices retain their desired functionality and exhibit very steep transfer curves, indicative of their good controllability. However, the

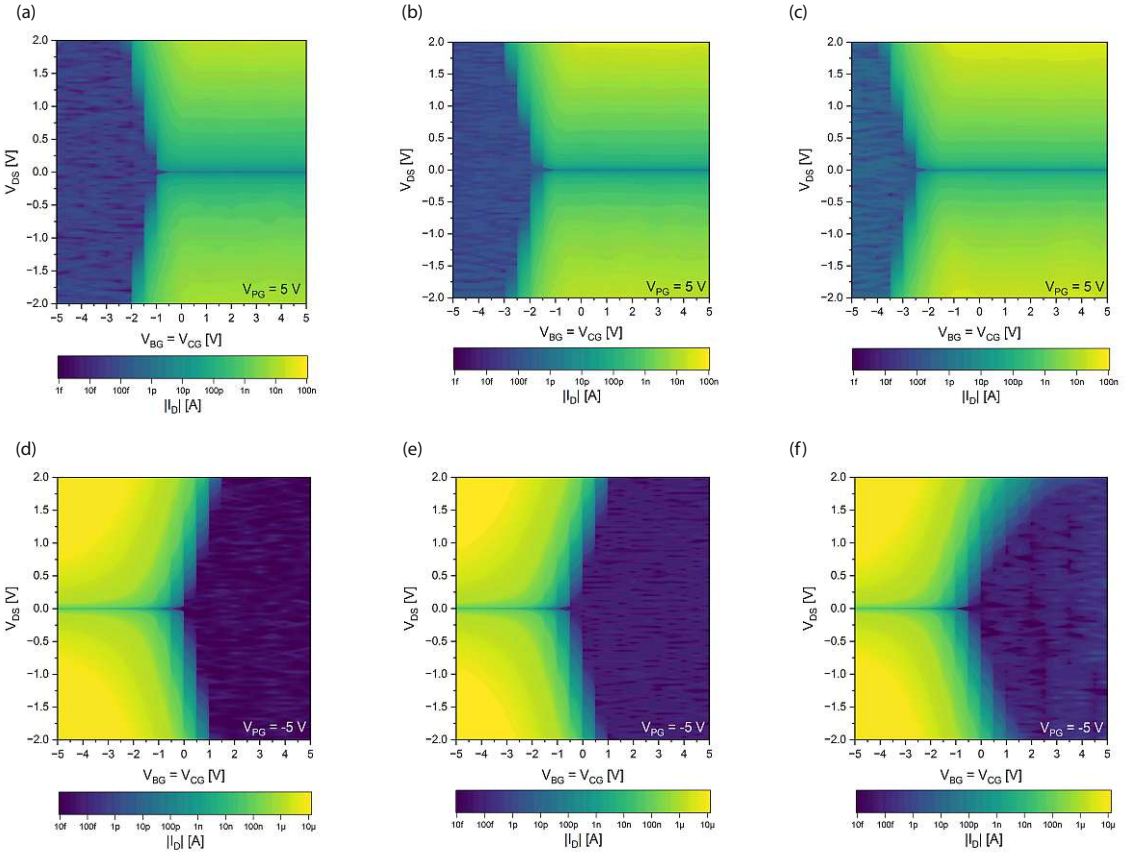

Figure 4.14: *Output characteristic as colormap from (a) to (f) with rising temperatures. (a) and (d): 47 °C, (b) and (e): 87 °C, (c) and (f): 127 °C. (a)-(c) represent a positive polarity gate voltage of V_{PG} = 5 V, whereas (d)-(f) are for negative V_{PG} = -5 V.*

first sample did not exhibit any ferroelectric behavior. We expect this effect to be caused by charge trapping at the Si/SiO2 and/or at the SiO2/HZO interface. Consequently, additional research was conducted on the interface layer, leading to the creation of a second sample.

4.1.2 Sample 2 - Chemically grown SiO_2 (Ch-SiO_2) with Pd top-gates

Based on the results of the first sample, it was concluded that the primary influence is dominated by trapping effects, although the device basically shows great behavior even with an additional layer. By analyzing the capacitive voltage divider of the semiconductor, the interfacial layer (IL), and the ferroelectric component, it was concluded that the IL would benefit from being thinned. Investigations on the IL were conducted realizing and analyzing three different MIS stacks, as illustrated in Figure 4.16 and can be compared with literature [133]. For this purpose, three different interfacial layers were used, namely the already used thermally prepared SiO_2, a SiO_2 prepared by a chemically based process (RCA) and hafnium oxide (HfO_2) deposited directly ALD. From capacitance-voltage mea-

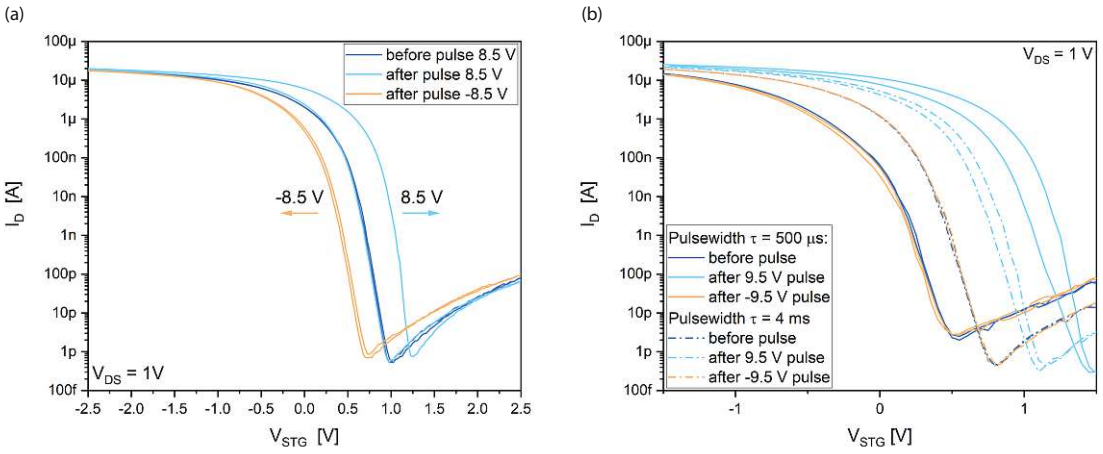

Figure 4.15: *Pulse cycle measurement for sample 1. (a) A positive and negative pulse of 8.5 V is applied for τ = 10 ms, leading to trapping behavior. (b) Different pulse-width with the same pulse-height of $\pm$9.5 V*

surements, the thermal oxide stack exhibits a clockwise orientation and thus a trapping behavior, while the chemical and hafnium oxide exhibit a ferroelectric behavior. Since the formation of an additional SiO_2 interfacial layer cannot be excluded in the case of HfO_2 and the RCA process for the chemical oxide is fairly simple as well as a good method for achieving a sufficiently thin oxide layer of about 1 nm, this approach was chosen for the following sample. The eventual presence of an additional SiO_2 interfacial layer under the HfO_2 ALD passivation will be investigated through TEM analysis in the near future.

From the literature [14, 134] it is known that a thinner layer of HZO exhibits higher polarization, which led to the decision to reduce the thickness to 9 nm for this sample. Consequently, the MFIS test structure was built, comprising a 1 nm thick chemical SiO_2 layer and a 9 nm thick HZO layer, within a highly n-doped silicon layer and a palladium top-electrode. The C-V measurement resulted in the Figure 4.17. Once again, the coercivity increases, resulting in a larger memory window. Additionally, there is only a slight change from 50 to 100 cycles, indicating a saturation of the value.

The second sample shares the same gate stack as the MFIS sample. Like the first sample, 120 nm aluminum was deposited for the pads and 70 nm palladium for the top gate material. The distinction lies in the fact that the rapid thermal annealing process was divided to facilitate separate temperature profiles for the crystallization of the HZO and the diffusion process. For the crystallization process, the sample was subjected to 530 °C for a duration of 120 seconds. The Al-Si exchange was performed several times - up to the desired channel width - at 500 °C for a total of 315 seconds. Structuring the top gates for the HZO crystallization poses difficulty in accurately determining whether the metal-semiconductor transitions form at the optimal central position of the two top-gate-arms of the DTG structure. For this purpose, some structures are left free of a top gate in order to get an overview of how the diffusion process has progressed so that it can be better

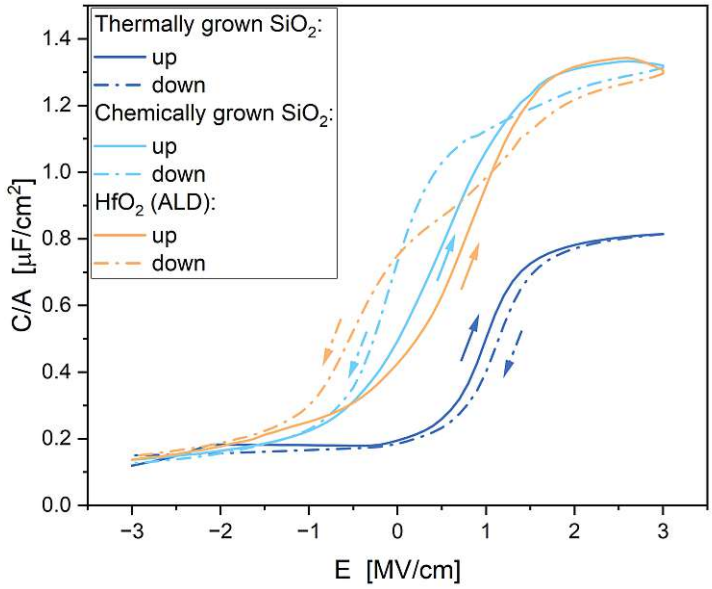

Figure 4.16: *Comparison of different interface layers within a MFIS structure. While the chemically grown SiO_2 and the HfO_2 layer are showing an ferroelectric behavior, the thermally grown SiO_2 is dominated by charge trapping effects.*

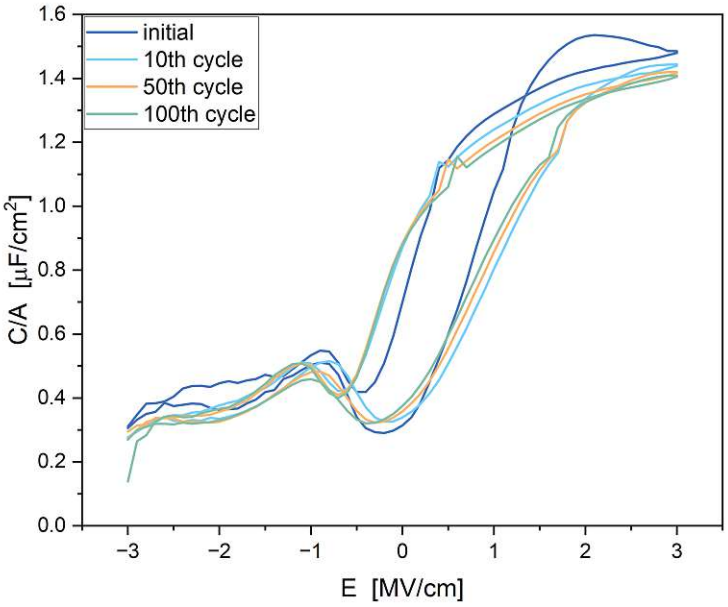

Figure 4.17: *MFIS structure with the same stack as the devices from sample 2. Numerous cycles demonstrate an increasing coercivity, and the peaks in the graph even represent the switching points.*

estimated. This aspect could be considered as a drawback given by the addition of the ferroelectric layer in the fabrication process. Figure 4.18 depicts the final device without a top-gate in (a), with the STG in (b) and the DTG arrangement in (c).

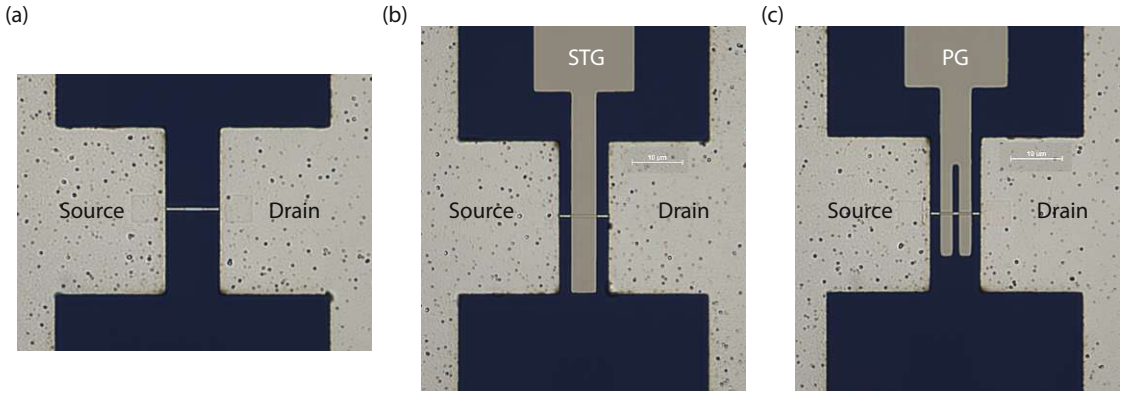

Figure 4.18: *Optical microscope picture of fabricated sample with chemically grown SiO_2 and Pd top-gates. (a) STG structure with one gate covering both MS transitions, (b) DTG configuration with the top-gate as polarity-gate (PG) and the back-gate as control gate (CG).*

To examine the impact of supplementary top-gate arrangements following the previous manufacturing process, either an additional control gate (CG) for the DTG structures or both a CG and a polarity gate (PG) for structures without a prior top-gate were realized using E-Beam lithography (EBL), as described in the Chapter "Experimental Techniques" (3) in Subsection 3.2. Such configurations can be found in Figure 4.19. The stack consist of a 10 nm titanium (Ti) adhesion layer and 100 nm gold (Au) layer as contact material.

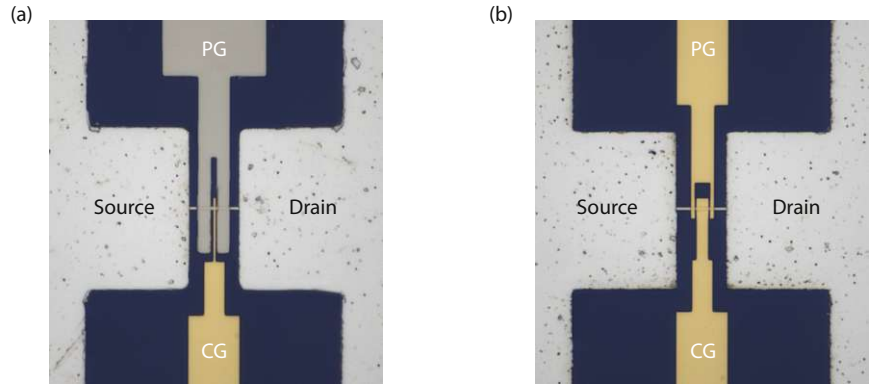

Figure 4.19: *Optical microscope picture of additional top-gate arrangements. (a) TTG structure with added control gate (CG). (b) Both polarity-gate (PG) and control gate (CG) are added afterwards to form a TTG structure.*

Transfer Characteristic

STG

In comparison to the STG device of sample 1, there was a significant increase in on-currents, particularly in the ratio of p- and n-type characteristics, as demonstrated in Figure 4.20 (a). Figure (b) shows the shift of the transfer characteristic by applying different back-gate voltages V_{BG}. This analysis aims to increase the p/n-type ratio. However, with increasing V_{BG}, the off-current decreases progressively, meaning that the device cannot be turned off properly, which is disadvantageous. The STHS is derived for the transfer curve with $V_{TG} = \pm 3$ V (orange) to 95 mV/dec and 159 mV/dec, for the p-branch and the n-branch, respectively.

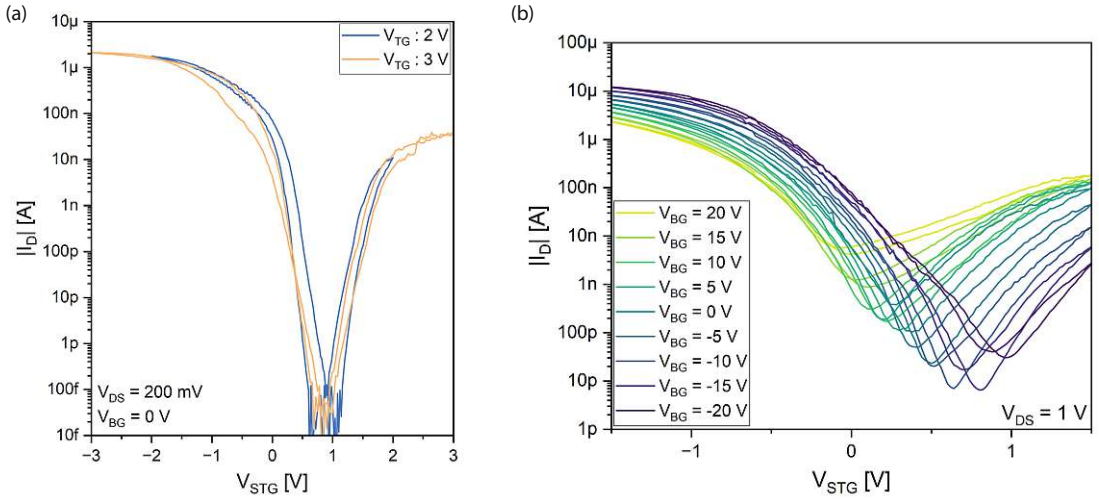

Figure 4.20: *STG transfer characteristic of sample 2 with symmetric V_{DS} of two different top-gate ranges in (a) and a back-gate voltage V_{BG} variation for enhancement of the p/n-type ration in (b).*

TTG

For the TTG devices with an additional control gate (CG), as seen in Figure 4.19 (a), a polarity-gate voltage V_{PG} sweep was examined starting from -2 V to 2 V within 250 mV steps while varying the control-gate voltage $V_{CG} = V_{BG}$ from -1.5 V to 1.5 V with a fixed bias of $V_{DS} = 1$ V. This and the corresponding colormap can be seen in Figure 4.21. Two distinct regions can be identified that describe the p-type and n-type operation, respectively. The colorcoding highlights their varying degrees of magnitude.

Pulse Measurements

In Chapter 3 two different pulse measurement methods have been described, namely "Set-Pulse" with consecutive identical pulses and "Pulse Cycle" with subsequent alternating pulses. These techniques were investigated for the STG, DTG, and TTG arrangements,

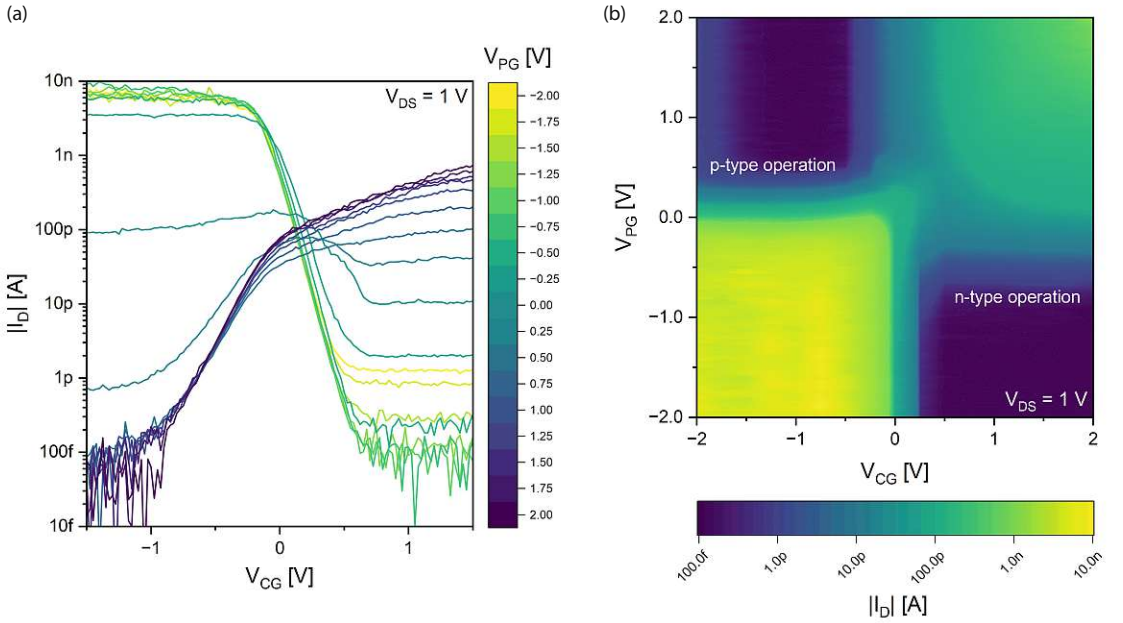

Figure 4.21: *PG-sweep of sample 2 for $V_{PG} = \pm 2$ V and $V_{CG} = \pm 1.5$ V (a) with the corresponding colormap (b) both at fixed $V_{DS} = 1$ V.*

respectively.

STG

With the Subfigures (a) and (b) in Figure 4.22 these two measurements are compared. The bias voltage used was $V_{DS} = 200$ mV, while the pulse width and number of pulses remained constant. The boxes in these figures give the configuration during and for the pulses themselves, while the values above apply to the transfer characteristic. Both scenarios exhibit a ferroelectric behavior, albeit only slightly. Positive applied pulses lead to a shift towards negative voltages and vice versa, returning to the initial state. The pulse cycle measurement causes a smaller hysteresis and has a greater impact, particularly on the on-current. The threshold-voltage shift is not the only impact of the STG configuration, since the barriers of the metal-semiconductor junction are also affected, since both the channel and the junctions are covered by the top gate. This superposition is consistent with the expectations and explanations in Section 2.4.

DTG

The DTG devices exhibit a clear ferroelectric effect, visible in Figure 4.23 (a) for set pulses and (b) for pulse cycles. The deviation between these two measurements is negligible. It is evident that the device can transition between two distinguishable states, which could serve as the basis for a memory device. Unfortunately, the remarkable reconfigurability of these devices has not yet achieved sufficient switching, although it is evident that a section

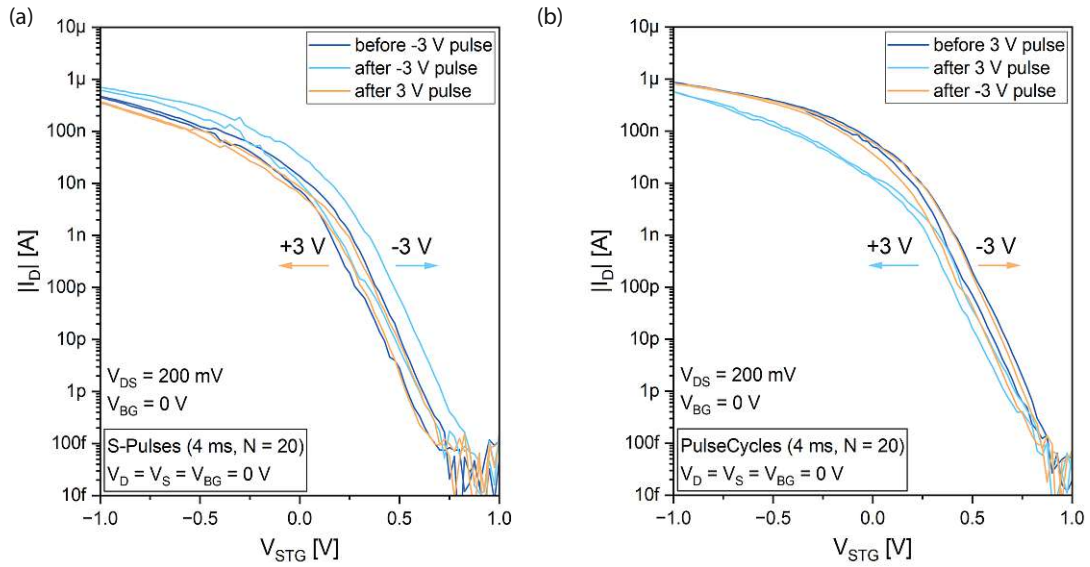

Figure 4.22: *STG pulse measurement results for sample 2. (a) shows the influence of Set-Pulses while in (b) the Pulse Cycle measurement can be compared.*

of the n-branch is emerging. Furthermore, it should be noted that the control gate has been designed with the back-gate configuration, which also impacts the Schottky barriers during the sweep of the transfer curve and thereby impacts the effect of the ferroelectric polarization. In (b), a 10-minute retention measurement reveals positive outcomes as the memory window expands even further within this time-frame. Further detailed retention measurements will be covered later.

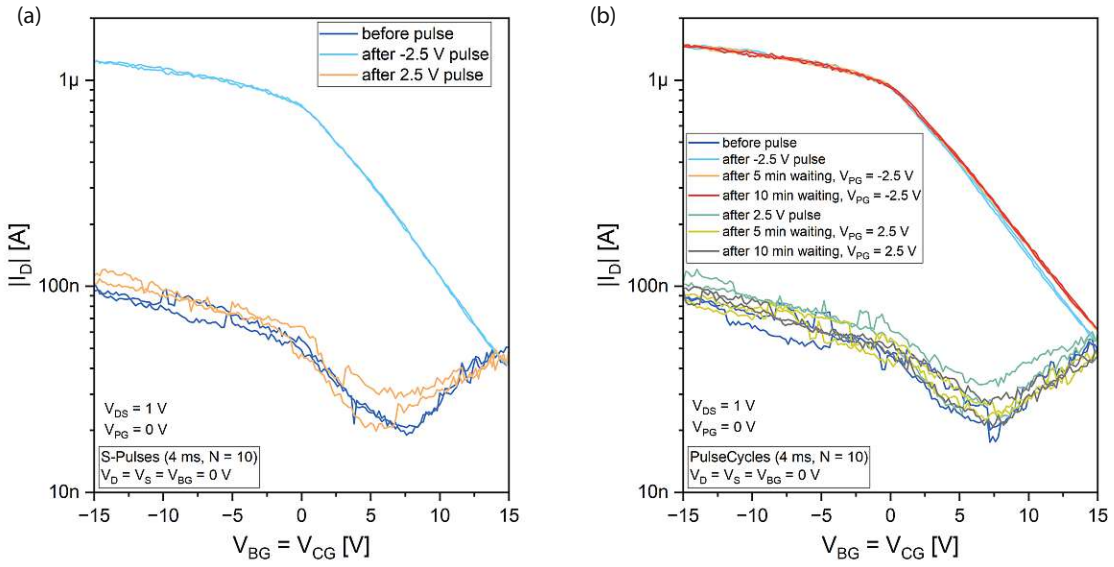

Figure 4.23: *DTG pulse measurement results for sample 2. (a) for Set-Pulse and (b) for Pulse cycle measurements and an additional 10 min retention analysis.*

TTG

As illustrated in the introduction of this section, see Figure 4.19, two different configurations of the triple-top-gates (TTG) were fabricated. The first part of this study presents two pulse measurements for the setup with an additional extended CG, showcased in Figure 4.24. Pulses with an amplitude V_{PG} of 2.5 V were used, and the polarity-gate voltage was fixed at $V_{PG} = 0$ V during the transfer characteristic measurement. In Subfigure (a), the Boltzmann limit is added to better estimate the slope. The method of pulse cycles (b) produces consistent polarization, as illustrated by the matching curves before and after the pulse in these exemplar devices. Based on the fact that the Schottky barriers and therefore the proportion of the magnitude of the currents for the p- and n- operation, it is evident that in the figures present a ferroelectric behavior. Thus, when a positive pulse is applied to the polarity gate (PG), the bands at the junctions are raised, allowing electrons to preferentially tunnel through this barrier and blocking holes, corresponding to an increase in the n-branch current and a decrease in the p-branch current. Conversely, the behavior is analogous for negative pulses.

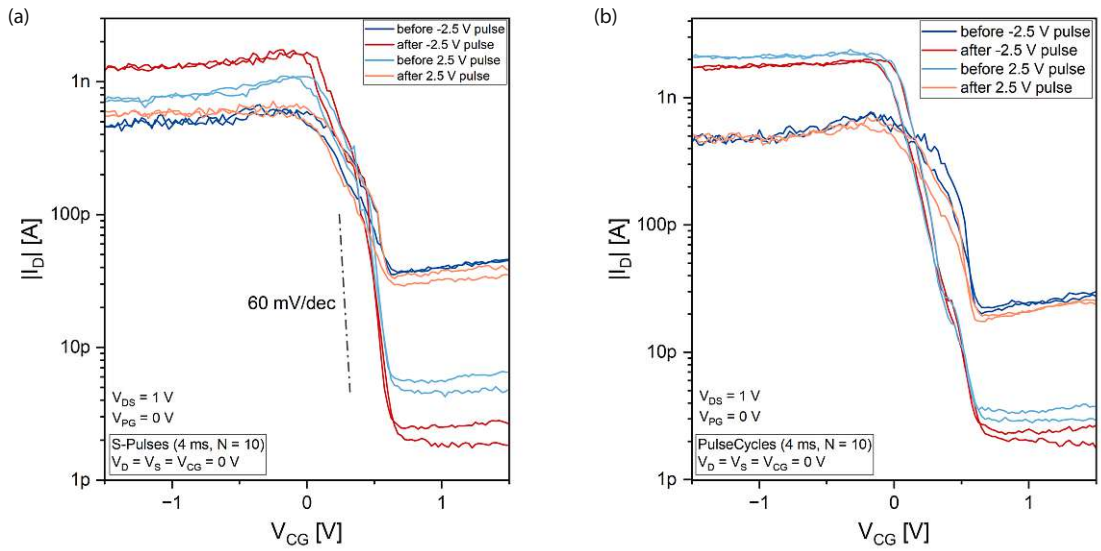

Figure 4.24: *TTG V_{PG} pulse measurement with additional CG for $V_{PG} = 0$ V while transfer characteristic is conducted. (a) For Set-Pulse measurements and (b) for Pulse Cycle measurements. For both a ferroelectric behavior can be observed. Explanation is given in the corresponding text.*

The subsequent Figure 4.25 uses the identical pulse settings as previously for the pulse cycle measurements to analyze the influence of set p- and n-dominant device behavior for V_{PG} = -1.5 V and V_{PG} = 1.5 V, respectively. It is evident that when choosing V_{PG} = 1.5 V (see Subfigure (a)), there is no noticeable effect. This may be attributed to the fact that the amount of fixed charges is dominant, which makes it more difficult for the n-type operation to experience an ferroelectric effect. While the behavior at V_{PG} = -1.5 V is comparable to that at $V_{PG} = 0$ V, but reduced, which could be due to a weakening of the polarization by the additional voltage acting during the transfer measurement.

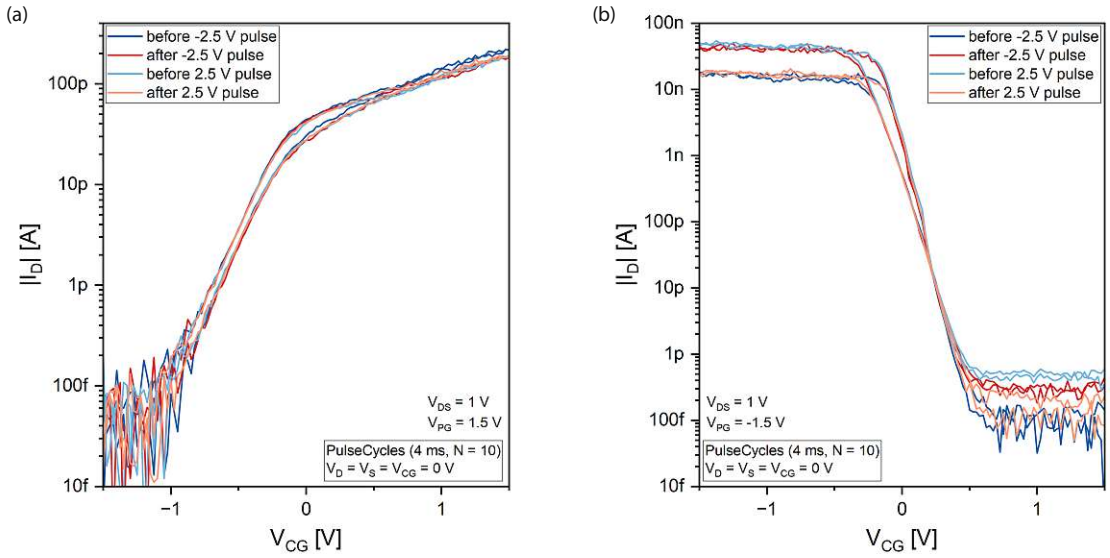

Figure 4.25: *TTG V_{PG}-Pulse Cycle measurement with additional CG for $V_{PG} = \pm 1.5$ V while transfer characteristic is conducted. (a) For $V_{PG} = 1.5$ V and (b) for $V_{PG} = -1.5$ V. Explanation is given in the corresponding text.*

To examine the impact of the control gate (CG) during pulsing, both measurement types were carried out, and the outcomes are presented in Figure 4.26. It was anticipated that the transfer behavior would remain unaffected because the CG region had not yet been covered with a suitable material during crystallization annealing, and thus the transformation to the desired ferroelectric orthorhombic phase should not have occurred. Furthermore, the CG located in the center of the channel does not affect the barriers. In addition, there is no charge trapping effect, which would be noticeable by a shift of the curves in the direction of the pulse sign.

Finally, the structures with both polarity-gate (PG) and control-gate (CG) added afterwards, as shown in Figure 4.19 (b), were investigated. As illustrated in Figure 4.27, when V_{PG} is pulsed with ± 5 V, significant charge trapping occurs, resulting in the switch from the p-type to the n-type characteristic and vice versa. Furthermore, the currents for the n-branch although still about two decades smaller, are outstandingly good compared to the other ferroelectric appearances. However, this approach as a charge trapping device was not pursued further as it was not the aim of this thesis.

Retention Measurements

A retention measurement was performed to assess the quality of the ferroelectric layer. To this purpose, the transfer characteristic was recorded for negative V_{PG} up to 270 minutes and for positive V_{PG} up to 120 minutes, as explained in Subsection 3.3.4. The graph in Figure 4.28 (a) demonstrates this fact, as well as the absolute value of the drain current $|I_D|$ determined at $V_{BG} = V_{CG} = 0$ V presented in (b). An almost constant value is kept

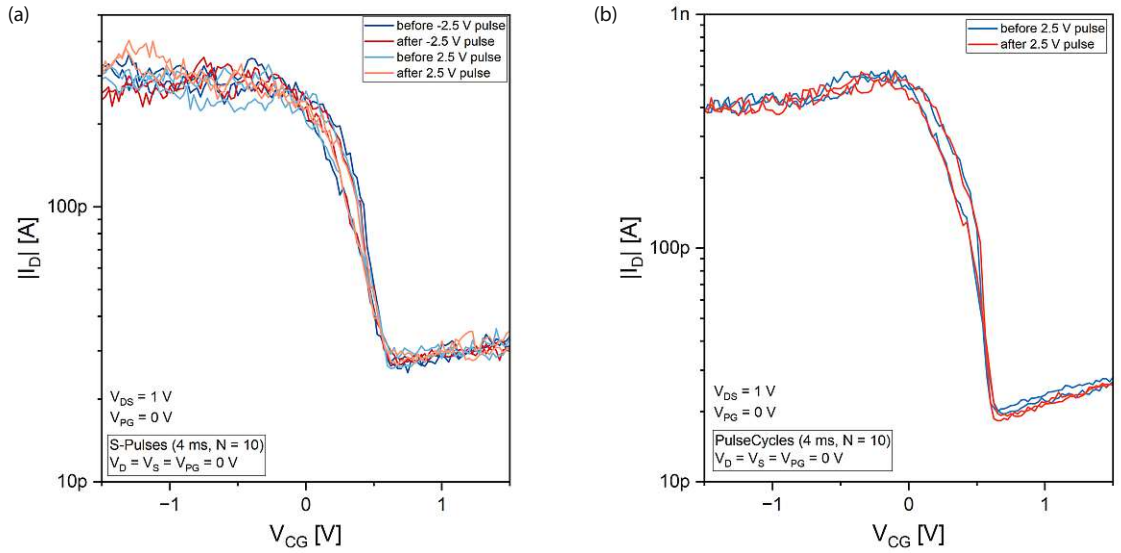

Figure 4.26: *TTG V_{CG} pulse measurement with V_{PG} set to zero. For (a) the Set-Pulse and (b) the pulse cycle measurement.*

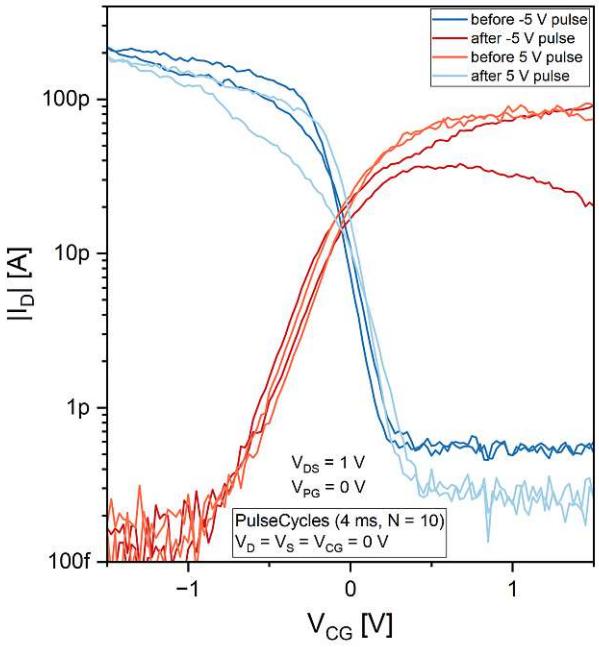

Figure 4.27: *TTG V_{CG} pulse measurement for a device with subsequent PG and CG. A clear charge trapping behavior can be observed.*

for the whole time period, therefore longer measurements will need to be made in the future for a first estimation of the duration until the effect falls below a certain threshold.

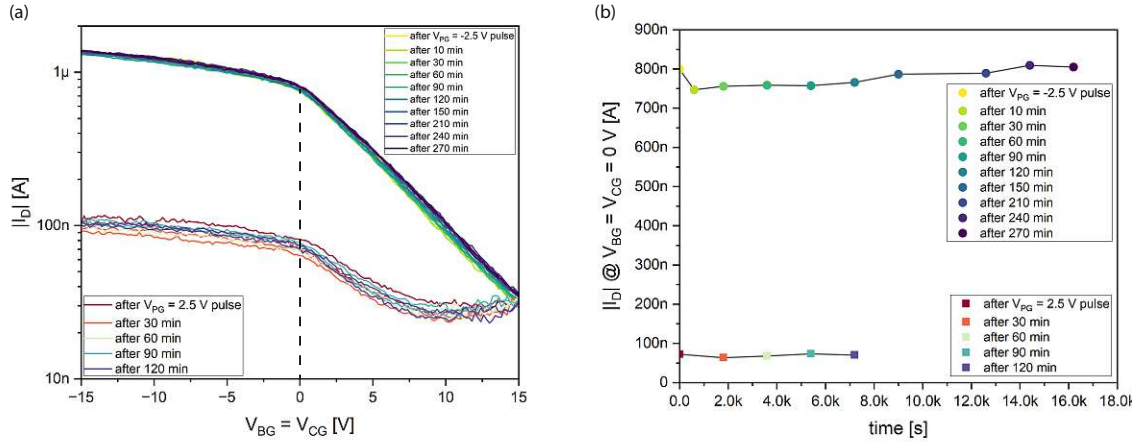

Figure 4.28: *Retention measurement for $V_{PG} = \pm 2.5$ V of DTG device. (a) Switchable transfer characteristic. (b) Absolute value of the drain current $|I_D|$ evaluated at $V_{BG} = V_{CG} = 0$ V.*

Furthermore, a error plot was created from the measurements to graphically show the deviation for both V_{PG} voltages, see Figure 4.29. It indicates a greater deviation in the case of V_{PG} = -2.5 V.

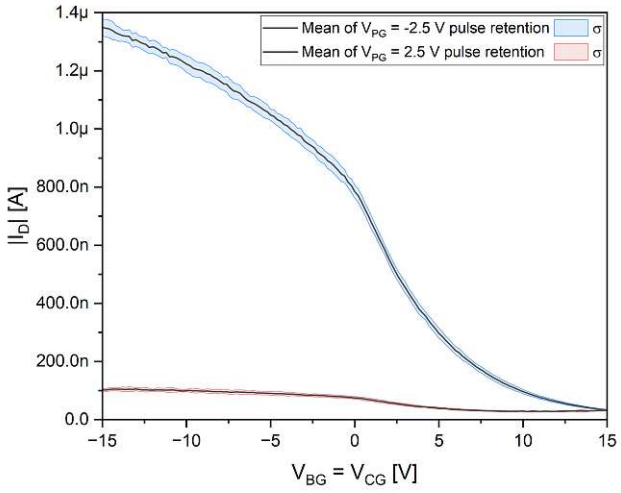

Figure 4.29: *Errorplot of the retention measurement for $V_{PG} = \pm 2.5$ V.*

Endurance Measurements

An error plot was generated using forty-four pulse cycle switches (from a different device than before). The outcome, depicted in Figure 4.30, illustrates the strong endurance of the produced devices. Nevertheless, for a more meaningful analysis, a much greater number of switches must be monitored. This can be done only resorting to automated measurement techniques, which will be implemented in the near future.

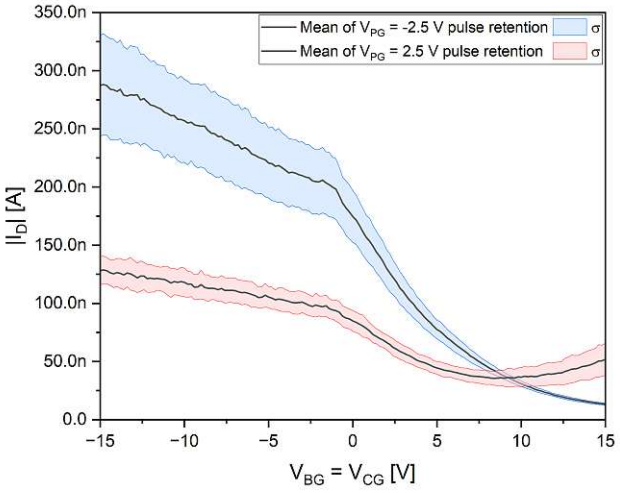

Figure 4.30: *Errorplot of the endurance measurement for $V_{PG} = \pm 2.5$ V for a sum of 44 pulse cycle switches.*

4.1.3 Sample 3/4 - Ch-SiO_2 with Ti(N) and Ti(N)/Ti/Pd-stack top-gates

The third and fourth sample share similarities with the second sample, as the SiO_2 layer with a thickness of around 1 nm is produced through the same process. Additionally, the HZO layer is further thinned to a thickness of 8 nm. The third sample features a top gate made of titanium nitride (Ti(N)) that is 100 nm thick and obtained by sputtering titanium (Ti) in a nitrogen (N) rich environment. Based on the theory of remote scavenging, which reduces oxygen vacancies in the HZO layer [126], the fourth sample consisted of a 30/20/50 nm thick Ti(N)/Ti/Pd stack.

Figure 4.31 illustrates the comparison of the TiN target discussed earlier with the Ti(N) from the titanium target. It is evident that the Ti(N) electrode exhibits a higher value, even at identical temperatures, leading to a more distinct butterfly curve. Consequently, both samples are annealed and crystallized at 550 °C for 120 seconds based on the slightly increased capacitance at higher temperatures. The exchange between Al and Si is maintained at 500 °C, but only for a duration of 150 seconds.

This duration was sufficient, since the exchange in these samples was so fast that some structures already formed a complete exchange, which meant that their function could no longer be maintained. The cause for this could be that the etching process was optimally chosen so that the overlap of the silicon nanosheet with the aluminum pad is at approximately the same level and therefore the exchange can start immediately and not with a delay, as would have been the case with under-etching or, in the worst case, with no exchange at all, as would have been the case with a too shallow etch depth. In contrast to palladium, a smaller number of devices were functional due to the detrimental impact

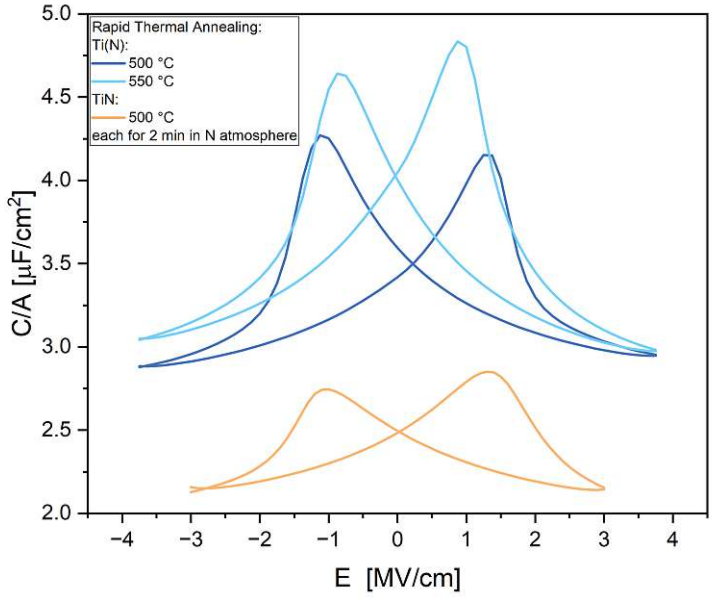

Figure 4.31: *Comparison of the thermal activation depending on the temperature for the pure TiN target and the Ti target within a nitrogen flow.*

of their leakage currents. This is demonstrated in the subsequent Subsection 4.1.4, utilizing a C-V measurement. As a consequence, the results of these last two samples are summarized in one subsection, of course also due to their similarities.

Figure 4.32 depicts the fabricated structure of the third sample again as an STG and DTG arrangement. Furthermore, it is evident that the lift-off is not so effortless compared to Pd or the Ti/Au stack and that residues remain, which are visible at the edges.

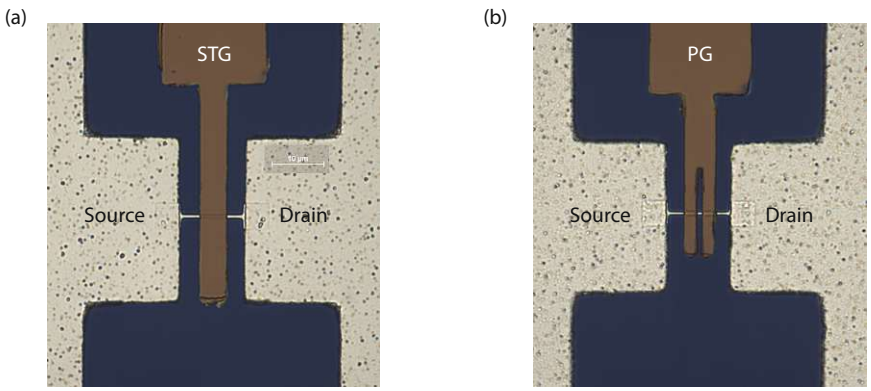

Figure 4.32: *Optical microscope picture of fabricated sample with chemically grown SiO_2 and Ti(N) top-gates. (a) STG structure with one gate covering both MS transitions, (b) DTG configuration with the top-gate as polarity-gate (PG) and the back-gate as control gate (CG).*

Within a cooperation with Empa (Swiss Federal Laboratories for Materials Science and Technology) [135] Transmission Electron Microscopy (TEM) images were acquired by Dr. Lilian Vogl from previous samples based on the same fabrication process as can be seen in Figure 4.33 with an Energy-dispersive X-ray spectroscopy (EDX) overlay for the respective layer material composition. Conformal growth of the layers and a uniform mixture of HfO_2 and ZrO_2 can be seen in this image.

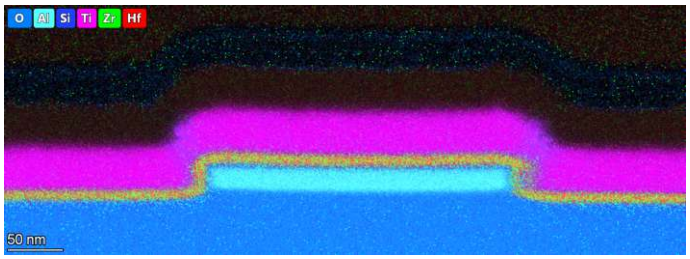

Figure 4.33: *Cross-section of the Fe-RFET with a transverse TEM cut with an Energy-dispersive X-ray spectroscopy (EDX) overlay for the respective layer material composition. Provided by Empa [135].*

Sample four is once again designed as STG and DTG as shown in Figure 4.34. In this case, also a increased effort was necessary for the lift-off process, but the result is notably better due to the Ti(N) layer thickness of one-third compared to the third sample.

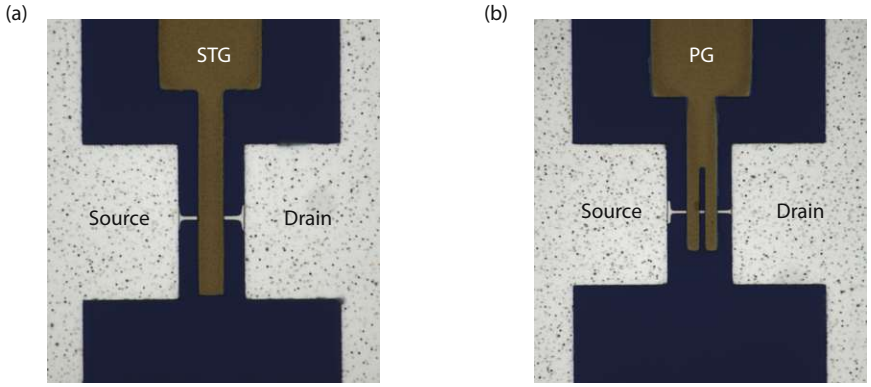

Figure 4.34: *Optical microscope picture of fabricated sample with chemically grown SiO_2 and Ti(N)/Ti/Pd-stack top-gates. (a) STG structure with one gate covering both MS transitions, (b) DTG configuration with the top-gate as polarity-gate (PG) and the back-gate as control gate (CG).*

Pulse Measurements

In this Subsection, the results of both samples are discussed, beginning with Sample 3 in the following.

Sample 3

The pulse measurements for sample 3 in the STG arrangement are shown in Figure 4.35 for the set pulse in (a) and the pulse cycle measurements in (b). Both transfer measurements were taken in pulsed mode to prevent possible charge trapping of the devices. The set-pulse measurement is characterized by a greater influence on the barrier.

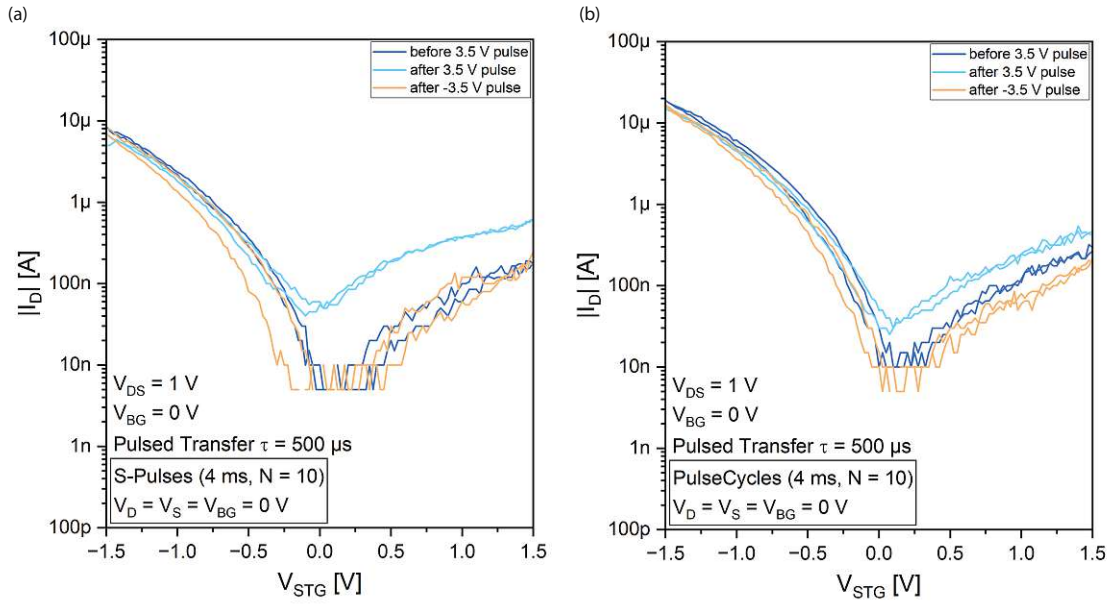

Figure 4.35: *STG pulse measurement results for sample 3. (a) for Set-Pulse and (b) for Pulse cycle measurements.*

Additionally, another result of a different device from the same sample is given in Figure 4.36, which exhibits a clearer distinction in Schottky barrier alteration mainly in the n-branch region. For this device the STHS results in 856 mV/dec (p-branch) and 485 mV/dec (n-branch) before the positive pulse of $V_{STG} = 3$ V is applied as well as 697 mV/dec (p-branch) and 460 mV/dec (n-branch) after the pulse.

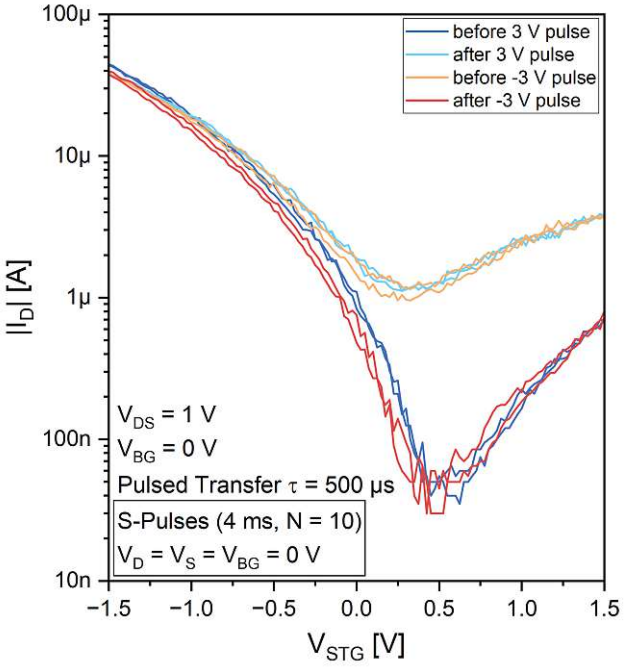

Figure 4.36: *STG pulse measurement for a different device from sample 3. It exhibits a more significant modification of the barrier.*

Sample 4

For sample four, only DTG devices could be used for the reasons mentioned at the beginning of this subsection, so a comparison of samples three and four is not feasible. Figure 4.37 illustrates both the set-pulse method (a) and the pulse cycle method (b). The observations indicate that the set pulse of the exemplary device exhibits more consistent switching compared to the pulse cycle scheme. Furthermore, a considerably larger hysteresis is noticeable for the n-operation mode, as opposed to the p-mode counterpart. Compared to sample 2, the on-currents for both states are high, resulting in a smaller memory window. Additionally the STHS results in 3.56 V/dec for the p-branch before the positive pulse of $V_{PG} = V_{TG} = 3$ V is applied as well as 2.89 V/dec (p-branch) and 3.51 V/dec (n-branch) after the pulse.

4.1.4 Comparison of the top-gate materials

To conclude this chapter, a brief comparison of top-gate materials based on MFIS structures is given. Three samples have been fabricated, all based on a highly n-doped silicon wafer, with a 1 nm thick chemical SiO_2 layer formed via the RCA process. An 8 nm thick HZO layer is deposited on top. As electrode material, the first sample has a 70 nm thick palladium layer, the second has a 75 nm thick Ti(N) layer, and the third consists of a Ti(N)/Ti/Pd stack with thicknesses of 25/10/35 nm. It can be observed in the Figure

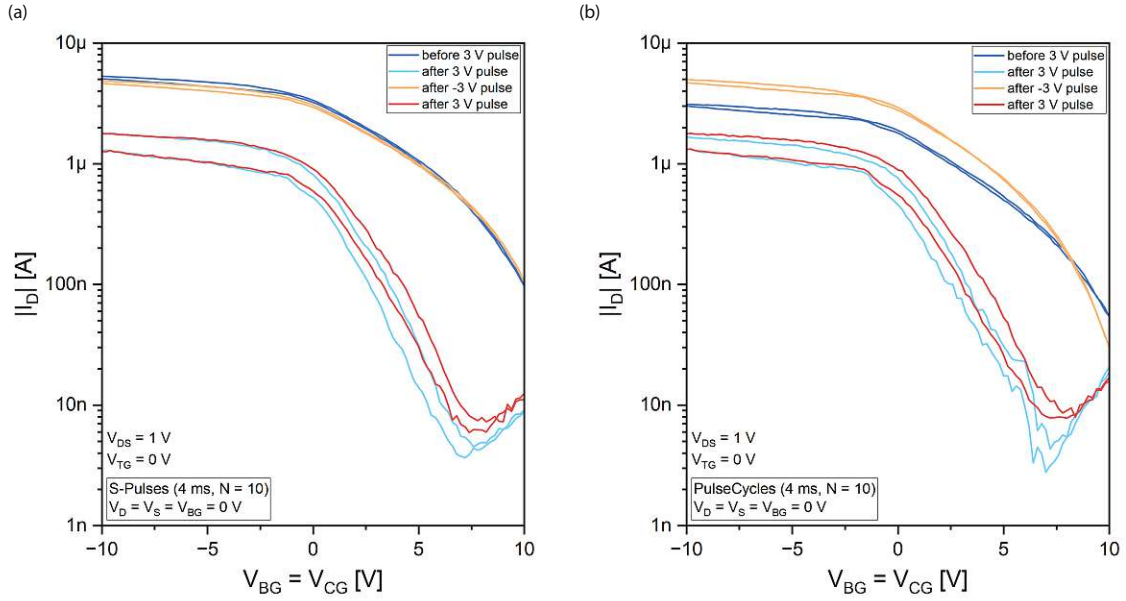

Figure 4.37: *DTG pulse measurement results for sample 4. (a) for Set-Pulse and (b) for Pulse cycle measurements.*

4.38 (a) that the palladium electrodes have the highest coercivity and that the pure Ti(N) equivalent to the values of the stack. Subfigure (b) compares the conductance. Ti(N) leads, followed by the Ti(N)/Ti/Pd stack, and Pd is the lowest. Further investigation is needed to determine the exact difference between Ti(N) and the Ti(N)/Ti/Pd stack with respect to the influence of the scavenging effect. Nevertheless, it is suspected that sputtering degrades the oxide due to the higher kinetic energy of the sputtered target compared to evaporated palladium (Pd) as discussed in Subsection 4.1.2.

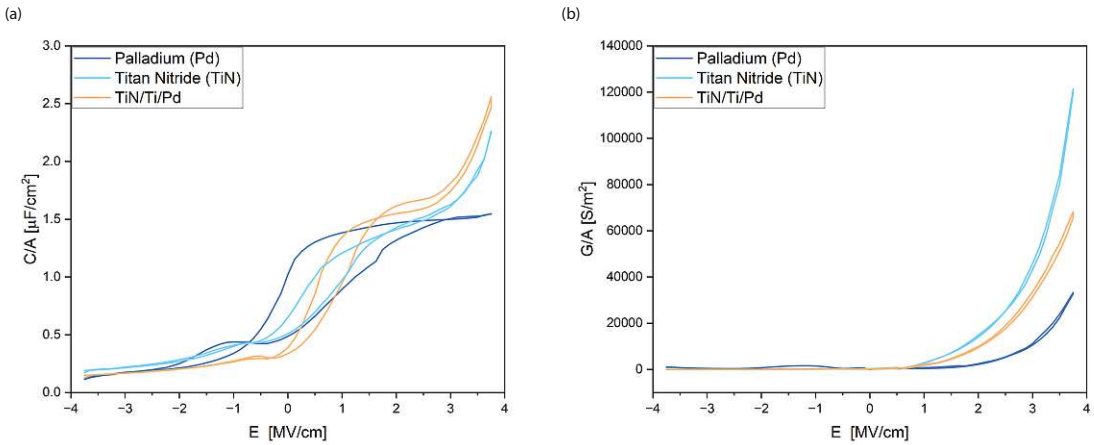

Figure 4.38: *Comparison of used electrode materials. (a) C-E measurement of Pd, Ti(N) and Ti(N)/Ti/Pd-stack. (b) Corresponding conductance values.*

Chapter 5

Conclusion and Outlook

In this thesis, Hafnium Zirconium Oxide (HZO), a ferroelectric gate dielectric, was integrated into the reconfigurable field-effect transistor. Detailed characterizations, measurements, and adapted fabrication steps were undertaken in order to obtain a so-called ferroelectric RFET (Fe-RFET). To achieve this goal, four samples were fabricated, which clearly describe the optimization and adaptation process and highlight the obstacles that need to be considered in order to make the appropriate decisions for further processes. Therefore, investigations of the thermal activation for the ferroelectric orthorhombic phase, interface engineering and the influence of the electrode material for both metal-ferroelectric-metal (MFM) and metal-ferroelectric-insulator-metal (MFIS) were performed between the iteration steps, as these allow a first estimation of the final behavior for each sample.

A comprehensive variety of measurements were performed, such as capacitance measurements (C-V), polarization measurements (P-E), conventional measurements for the transistor characterization including transfer characteristic, output characteristic, their temperature influence, as well as extended measurements with voltage pulses for the study of the ferroelectric properties.

The Fe-RFETs are based on a silicon-on-insulator (SOI) wafer that is patterned with Si nanosheets to serve as the device layer and subsequently as the channel. The RCA process was utilized to provide a high quality SiO_2 gate dielectric with low trap density. In addition, the Atomic Layer Deposition (ALD) technique was employed to deposit the ferroelectric layer. Consequently, omega-shaped top-gates were fabricated either for single top-gate (STG) or, employing a splitted gate design, for dual top-gate (DTG). The material of the top-gate was chosen according to the specific sample. Afterward, the orthorhombic phase transition was induced by means of rapid thermal annealing (RTA). Finally, two distinct metal-semiconductor (MS) transitions were formed by creating aluminum (Al) source and drain pads, leading to a thermally induced aluminum-silicon (Al-Si) heterostructure with

consistent, reproducible, and single-elementary crystalline Al contacts.

With respect to the formation of HZO crystallization, as mentioned in the theory, see Chapter 2, on the one hand the heating/cooling rate and on the other hand the magnitude of the temperature itself were demonstrated to be decisive for the optimal formation of crystallinity in the desired orthorhombic phase.

It has been shown that the implementation of HZO in the already established device process gives remarkable results, except for the asymmetry of the p- and n-characteristic, which can be attributed to negative charges in the oxide layer. Still, charge trapping and depolarization seem to dominate the fields counteracting the ferroelectric effect.

Based on this, the interface between the channel and the HZO was investigated. This involved a comparison of three layers: a thermal SiO_2 layer with a thickness of 2.5 nm, a 2 nm thick HfO_2 layer, and a chemically produced SiO_2 layer of 1 nm fabricated using the RCA process. The C-V analysis of the MFIS structure indicates that ferroelectric behavior cannot be achieved for thermal SiO_2. In contrast, the HfO_2 layer enables such behavior, although the possibility of the appearance of a thin SiO_2 layer during the ALD fabrication process cannot be ruled out. This makes the stack unfavorable for design considerations to achieve ferroelectric storage or the negative-capacitance (NC) approach. This disadvantageous aspect will be confirmed by future transmission electron microscopy (TEM) analysis of the fabricated structures. In turn, chemically-formed SiO_2 has demonstrated its potential as a viable method for producing an ultra-thin oxide layer with a low trap density, analogous to the performance of SiO_2 in general. This makes it an effective solution for the interface between Si and HZO. This interface optimization has led to a ferroelectric behavior which can overcome the charge trapping effects.

As discussed earlier, different top-gate materials were investigated including palladium (Pd) and titanium nitride (TiN), due to their known ability to induce crystallization of HZO. The utilization of palladium as a top-gate material resulted in a higher yield than TiN. This may be attributed to TiN forming multiple types of oxynitrides, as evidenced by higher concentrations of TiO_xN_y in preliminary XPS results (not included in this thesis). The leakage currents using Pd, with the largest deviation, were lower by a factor of 4 compared to Ti(N). This is believed to be related to the manufacturing process, as palladium is deposited by evaporating the target material with an electron beam, whereas TiN is applied through sputtering with higher kinetic energy particles.

In summary, the devices featuring SiO_2 prepared through chemical methods and Pd top-gates (Sample 2) exhibited the most favorable outcomes. Evidence of this can be seen in the ferroelectric shift of the threshold voltage and change in on-currents due to the influence of the Schottky barriers at the metal-semiconductor (MS) junctions. Moreover, good results were obtained for retention and endurance measurements, which can serve as a baseline for future benchmark studies. However, additional optimizations are necessary

to achieve symmetric p- and n-modes for optimal RFET functionality, considering the HZO layer and the work function of the top gate.

Further research topics and potential investigations include the integration of HZO with a different channel materials such as silicon-germanium alloy (SiGe) or even germanium-on-insulator (GeOI) based on the work of Andreas Fuchsberger [47] and Larissa Kühberger [79]. Beyond this, other top gate materials such as platinum (Pt), tantal nitride (TaN) and tungsten (W) or different concentration compositions of Ti(N) using a Ti target in a nitrogen atmosphere can be used. Moreover, incorporating supplementary dielectric stacks could compensate the effect caused by the fixed charges induced by HZO. Since the devices have only been studied at room temperature and elevated temperatures up to 127 °C, cooling would be a interesting consideration with respect to the inverse sub-threshold slope (STHS) considering its temperature dependency. Finally, measurements of longer retention times are essential for an extrapolative estimate as well as a much greater number of switches for the analysis of the endurance.

Combining ferroelectric materials with the remarkable functionality of the reconfigurable field-effect transistor (RFET) provides a foundation for paving the way to non-volatile logic-in-memory (LiM), negative-capacitance FET (NC-FET), and neuromorphic applications, to mention just a few.

List of Figures

Bibliography

[1] J. Bardeen and W. H. Brattain. The Transistor, A Semi-Conductor Triode. *Phys. Rev.*, 74:230–231, Jul 1948. doi: 10.1103/PhysRev.74.230. URL https://link.aps.org/doi/10.1103/PhysRev.74.230.

[2] European Semiconductor Industry Association. Forecast from World Semiconductor Trade Statistics (wsts). URL https://www.eusemiconductors.eu/sites/default/files/ESIA_WSTS_SpringForecast2022.pdf.

[3] Gordon E. Moore. Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, april 19, 1965, pp.114 ff. *IEEE Solid-State Circuits Society Newsletter*, 11(5):33–35, Sept 2006. ISSN 1098-4232. doi: 10.1109/N-SSC.2006.4785860.

[4] R.H. Dennard, F.H. Gaensslen, Hwa-Nien Yu, V.L. Rideout, E. Bassous, and A.R. LeBlanc. Design of ion-implanted MOSFET's with very small physical dimensions. *IEEE Journal of Solid-State Circuits*, 9(5):256–268, 1974. doi: 10.1109/JSSC.1974.1050511.

[5] Sayeef Salahuddin, Kai Ni, and Suman Datta. The era of hyper-scaling in electronics. *Nature Electronics*, 1:442–450, 2018. ISSN 2520-1131. doi: 10.1038/s41928-018-0117-x. URL https://doi.org/10.1038/s41928-018-0117-x.

[6] S.M. Sze and K.K. Ng. *Physics of Semiconductor Devices*. Wiley, 2006. ISBN 9780470068304. URL https://books.google.at/books?id=o4unkmHBHb8C.

[7] Mart Graef et al. International Roadmap for Devices and Systems™ 2022 Update - More than Moore. *IEEE*. URL https://irds.ieee.org/images/files/pdf/2022/2022IRDS_WP-MtM.pdf.

[8] Mark T. Bohr, Robert S. Chau, Tahir Ghani, and Kaizad Mistry. The High-k Solution. *IEEE Spectrum*, 44(10):29–35, 2007. doi: 10.1109/MSPEC.2007.4337663.

[9] Yu-Ming Lin, J. Appenzeller, and Phaedon Avouris. Novel carbon nanotube FET design with tunable polarity. pages 687 – 690, 01 2005. doi: 10.1109/IEDM.2004.1419262.

[10] André Heinzig, Stefan Slesazeck, Franz Kreupl, Thomas Mikolajick, and Walter M. Weber. Reconfigurable Silicon Nanowire Transistors. *Nano Letters*, 12(1):119–124, 2012. doi: 10.1021/nl203094h. URL https://doi.org/10.1021/nl203094h. PMID: 22111808.

[11] Walter M. Weber, Lutz Geelhaar, Andrew P. Graham, Eugen Unger, Georg S. Duesberg, Maik Liebau, Werner Pamler, Caroline Chèze, Henning Riechert, Paolo Lugli, and Franz Kreupl. Silicon-Nanowire Transistors with Intruded Nickel-Silicide Contacts. *Nano Letters*, 6(12):2660–2666, 2006. doi: 10.1021/nl0613858. URL https://doi.org/10.1021/nl0613858. PMID: 17163684.

[12] André Heinzig, Stefan Slesazeck, Franz Kreupl, Thomas Mikolajick, and Walter M. Weber. Reconfigurable Silicon Nanowire Transistors. *Nano Letters*, 12(1):119–124, Jan 2012. ISSN 1530-6984. doi: 10.1021/nl203094h. URL https://pubs.acs.org/doi/10.1021/nl203094h.

[13] Sally A. McKee and Robert W. Wisniewski. *Memory Wall*, pages 1110–1116. Springer US, Boston, MA, 2011. ISBN 978-0-387-09766-4. doi: 10.1007/978-0-387-09766-4_234. URL https://doi.org/10.1007/978-0-387-09766-4_234.

[14] Hiroshi Funakubo Uwe Schröder, Cheol Seong Hwang. *Ferroelectricity in Doped Hafnium Oxide: Materials, Properties and Devices*. Woodhead Publishing, 2019. ISBN 9780081024300. doi: https://doi.org/10.1016/C2017-0-01145-X. URL https://shop.elsevier.com/books/ferroelectricity-in-doped-hafnium-oxide/Schr{ö}der/978-0-08-102430-0.

[15] Ali Keshavarzi, Kai Ni, Wilbert Van Den Hoek, Suman Datta, and Arijit Raychowdhury. FerroElectronics for Edge Intelligence. *IEEE Micro*, 40(6):33–48, 2020. doi: 10.1109/MM.2020.3026667.

[16] Jiajia Liao, Siwei Dai, Ren-Ci Peng, Jiangheng Yang, Binjian Zeng, Min Liao, and Yichun Zhou. HfO_2-based ferroelectric thin film and memory device applications in the post-Moore era: A review. *Fundamental Research*, 3(3):332–345, 2023. ISSN 2667-3258. doi: https://doi.org/10.1016/j.fmre.2023.02.010. URL https://www.sciencedirect.com/science/article/pii/S2667325823000419.

[17] Thomas Mikolajick, Min Hyuk Park, Laura Begon-Lours, and Stefan Slesazeck. From Ferroelectric Material Optimization to Neuromorphic Devices. page 2206042, . ISSN 0935-9648, 1521-4095. doi: 10.1002/adma.202206042. URL https://onlinelibrary.wiley.com/doi/10.1002/adma.202206042.

[18] Ju Choi, Yuanbing Mao, and J.P. Chang. Development of Hafnium Based High-k Materials A Review. *Materials Science and Engineering: R: Reports*, 72:97–136, 07 2011. doi: 10.1016/j.mser.2010.12.001.

[19] J.A. Kittl, K. Opsomer, M. Popovici, N. Menou, B. Kaczer, X.P. Wang, C. Adelmann, M.A. Pawlak, K. Tomida, A. Rothschild, B. Govoreanu, R. Degraeve,

M. Schaekers, M. Zahid, A. Delabie, J. Meersschaut, W. Polspoel, S. Clima, G. Pourtois, W. Knaepen, C. Detavernier, V.V. Afanas'ev, T. Blomberg, D. Pierreux, J. Swerts, P. Fischer, J.W. Maes, D. Manger, W. Vandervorst, T. Conard, A. Franquet, P. Favia, H. Bender, B. Brijs, S. Van Elshocht, M. Jurczak, J. Van Houdt, and D.J. Wouters. High-k dielectrics for future generation memory devices (Invited Paper). *Microelectronic Engineering*, 86(7):1789–1795, 2009. ISSN 0167-9317. doi: https://doi.org/10.1016/j.mee.2009.03.045. URL `https://www.sciencedirect.com/science/article/pii/S0167931709002044`. INFOS 2009.

[20] Johannes Müller, Tim S. Böscke, Uwe Schröder, Stefan Müller, Dennis Bräuhaus, Ulrich Böttger, Lothar Frey, and Thomas Mikolajick. Ferroelectricity in Simple Binary ZrO_2 and HfO_2. 12(8):4318–4323. ISSN 1530-6984. doi: 10.1021/nl302049k. URL `https://doi.org/10.1021/nl302049k`. Publisher: American Chemical Society.

[21] T. S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, and U. Böttger. Ferroelectricity in hafnium oxide thin films. 99(10):102903. ISSN 0003-6951, 1077-3118. doi: 10.1063/1.3634052. URL `http://aip.scitation.org/doi/10.1063/1.3634052`.

[22] Lukas Wind, Raphael Böckle, Masiar Sistani, Peter Schweizer, Xavier Maeder, Johann Michler, Corban G.E. Murphey, James Cahoon, and Walter M. Weber. Monolithic and Single-Crystalline Aluminum-Silicon Heterostructures. *ACS Applied Materials & Interfaces*, 14(22):26238–26244, 2022. doi: 10.1021/acsami.2c04599. URL `https://doi.org/10.1021/acsami.2c04599`. PMID: 35621308.

[23] Ling B. Kong, Haitao Huang, and Sean Li. *Fundamentals of Ferroelectric Materials*, chapter 1, pages 1–31. John Wiley & Sons, Ltd, 2018. ISBN 9783527807505. doi: https://doi.org/10.1002/9783527807505.ch1. URL `https://onlinelibrary.wiley.com/doi/abs/10.1002/9783527807505.ch1`.

[24] Safa Kasap and Peter Capper, editors. *Springer Handbook of Electronic and Photonic Materials*. Springer International Publishing, 2017. ISBN 978-3-319-48931-5. doi: 10.1007/978-3-319-48933-9.

[25] Yuhuan Xu. *Ferroelectric materials and their applications*. Elsevier, Amsterdam [u.a.], 1991. ISBN 0444883541.

[26] Zouhair Hanani. *Design of flexible lead-free ceramic/biopolymer composite for energy storage and energy harvesting applications*. PhD thesis, 12 2020.

[27] L. D. Landau. On the theory of phase transitions. *Zh. Eksp. Teor. Fiz.*, 7:19–32, 1937. doi: 10.1016/B978-0-08-010586-4.50034-1.

[28] Yougui Liao. Practical Electron Microscopy and Database. 2006. URL `https://www.globalsino.com/EM/page2380.html`.

[29] M. Dawber, K. M. Rabe, and J. F. Scott. Physics of thin-film ferroelectric oxides. *Rev. Mod. Phys.*, 77:1083–1130, Oct 2005. doi: 10.1103/RevModPhys.77.1083. URL `https://link.aps.org/doi/10.1103/RevModPhys.77.1083`.

[30] Erwin Schrödinger. Studien über Kinetik der Dielektrika, den Schmelzpunkt, Pyro- und Piezoelektrizität. *Sitzungsberichten der kaiserl. Akademie der Wissenschaften in Wien*, 1912.

[31] J. Valasek. Piezo-Electric and Allied Phenomena in Rochelle Salt. *Phys. Rev.*, 17: 475–481, Apr 1921. doi: 10.1103/PhysRev.17.475. URL https://link.aps.org/doi/10.1103/PhysRev.17.475.

[32] Scherrer P. Busch, G. Eine neue seignette-elektrische Substanz. *Naturwissenschaften 23*, 1935. URL https://doi.org/10.1007/BF01498152.

[33] B. Wul and J. M. Goldman. Ferroelectric switching in batio3 ceramics. *Acad. Sci. URSS 51*, 1946.

[34] T. Mikolajick, S. Slesazeck, H. Mulaosmanovic, M. H. Park, S. Fichtner, P. D. Lomenzo, M. Hoffmann, and U. Schröder. Next generation ferroelectric materials for semiconductor process integration and their applications. 129(10):100901, . ISSN 0021-8979, 1089-7550. doi: 10.1063/5.0037617. URL https://pubs.aip.org/jap/article/129/10/100901/157224/Next-generation-ferroelectric-materials-for.

[35] Dong Wang, Shenglan Hao, Brahim Dkhil, Bobo Tian, and Chungang Duan. Ferroelectric materials for neuroinspired computing applications. *Fundamental Research*, 2023. ISSN 2667-3258. doi: https://doi.org/10.1016/j.fmre.2023.04.013. URL https://www.sciencedirect.com/science/article/pii/S2667325823001310.

[36] G. Shirane, E. Sawaguchi, and Y. Takagi. Dielectric Properties of Lead Zirconate. *Phys. Rev.*, 84:476–481, Nov 1951. doi: 10.1103/PhysRev.84.476. URL https://link.aps.org/doi/10.1103/PhysRev.84.476.

[37] Takeo Furukawa, Munehiro Date, Eiichi Fukada, Yoshiro Tajitsu, and Akio Chiba. Ferroelectric Behavior in the Copolymer of Vinylidenefluoride and Trifluoroethylene. *Japanese Journal of Applied Physics*, 19(2):L109, feb 1980. doi: 10.1143/JJAP.19.L109. URL https://dx.doi.org/10.1143/JJAP.19.L109.

[38] Jonas Alexander Hafner. *Ferroelectric polymer thin films for MEMS applications : towards soft and high-speed AFM probes*. PhD thesis, TU Wien, 2021. URL https://repositum.tuwien.at/handle/20.500.12708/16943.

[39] A.F. Devonshire. XCVI. Theory of barium titanate. *The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science*, 40(309):1040–1063, 1949. doi: 10.1080/14786444908561372. URL https://doi.org/10.1080/14786444908561372.

[40] Vitaly L. Ginzburg. *On Superconductivity and Superfluidity (What I Have and Have Not Managed to Do), As Well As on the 'Physical Minimum' at the Beginning of the 21st Century*, pages 1–34. Springer Berlin Heidelberg, Berlin, Heidelberg, 2009. ISBN 978-3-540-68008-6. doi: 10.1007/978-3-540-68008-6_1. URL https://doi.org/10.1007/978-3-540-68008-6_1.

[41] P. Chandra and P. B. Littlewood. A Landau Primer for Ferroelectrics. URL http://arxiv.org/abs/cond-mat/0609347.

[42] Writam Banerjee, Alireza Kashir, and Stanislav Kamba. Hafnium Oxide (HfO_2) - A Multifunctional Oxide: A Review on the Prospect and Challenges of Hafnium Oxide in Resistive Switching and Ferroelectric Memories. *Small*, 18(23):2107575, 2022. doi: https://doi.org/10.1002/smll.202107575. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/smll.202107575.

[43] Uwe Schröder, Min Hyuk Park, Thomas Mikolajick, and Cheol Seong Hwang. The fundamentals and applications of ferroelectric HfO_2. 7(8):653–669. ISSN 2058-8437. doi: 10.1038/s41578-022-00431-2. URL https://www.nature.com/articles/s41578-022-00431-2.

[44] J.G. Webster. *The Measurement, Instrumentation and Sensors Handbook (1st ed.)*. CRC Press, 1999. URL https://doi.org/10.1201/9781003040019.

[45] Safa Kasap and Peter Capper, editors. *Springer Handbook of Electronic and Photonic Materials*. Springer International Publishing, 2017. ISBN 978-3-319-48931-5. doi: 10.1007/978-3-319-48933-9.

[46] S. Dauwe, J. Schmidt, A. Metz, and R. Hezel. Fixed charge density in silicon nitride films on crystalline silicon surfaces under illumination. In *Conference Record of the Twenty-Ninth IEEE Photovoltaic Specialists Conference, 2002.*, pages 162–165, 2002. doi: 10.1109/PVSC.2002.1190481.

[47] Andreas Fuchsberger. Reconfigurable Field-Effect Transistors Based on Aluminium-Silicon-Germanium Heterostructures. 2022. URL https://doi.org/10.34726/hss.2022.102562.

[48] Si Joon Kim, Jaidah Mohan, Scott R. Summerfelt, and Jiyoung Kim. Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Thin Films: A Review of Recent Advances. 71(1):246–255, . ISSN 1047-4838, 1543-1851. doi: 10.1007/s11837-018-3140-5. URL http://link.springer.com/10.1007/s11837-018-3140-5.

[49] Min Hyuk Park, Han Joon Kim, Yu Jin Kim, Woongkyu Lee, Taehwan Moon, and Cheol Seong Hwang. Evolution of phases and ferroelectric properties of thin $Hf_{0.5}Zr_{0.5}O_2$ films according to the thickness and annealing temperature. 102(24): 242905. ISSN 0003-6951. doi: 10.1063/1.4811483. URL https://aip.scitation.org/doi/full/10.1063/1.4811483. Publisher: American Institute of Physics.

[50] Min Hyuk Park, Han Joon Kim, Yu Jin Kim, Taehwan Moon, Keum Do Kim, and Cheol Seong Hwang. Thin $Hf_xZr_{1-x}O_2$ Films: A New Lead-Free System for Electrostatic Supercapacitors with Large Energy Storage Density and Robust Thermal Stability. 4(16):1400610. doi: https://doi.org/10.1002/aenm.201400610. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/aenm.201400610. _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/aenm.201400610.

[51] Ju Yong Park, Duk-Hyun Choe, Dong Hyun Lee, Geun Taek Yu, Kun Yang, Se Hyun Kim, Geun Hyeong Park, Seung-Geol Nam, Hyun Jae Lee, Sanghyun Jo, Bong Jin Kuh, Daewon Ha, Yongsung Kim, Jinseong Heo, and Min Hyuk Park. Revival of Ferroelectric Memories Based on Emerging Fluorite-Structured Ferroelectrics. *Advanced Materials*, n/a(n/a):2204904, August 2022. doi: https://doi.org/10.1002/adma.202204904. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.202204904.

[52] Nanbo Gong and T. P. Ma. Why Is FE-HfO_2 More Suitable Than PZT or SBT for Scaled Nonvolatile 1-T Memory Cell? A Retention Perspective. *IEEE Electron Device Letters*, 37:1123–1126, 2016. URL https://api.semanticscholar.org/CorpusID:25723231.

[53] Halid Mulaosmanovic, Evelyn T Breyer, Stefan Dünkel, Sven Beyer, Thomas Mikolajick, and Stefan Slesazeck. Ferroelectric field-effect transistors based on HfO_2 : a review. 32(50):502002. ISSN 0957-4484, 1361-6528. doi: 10.1088/1361-6528/ac189f. URL https://iopscience.iop.org/article/10.1088/1361-6528/ac189f.

[54] Sergei Zarubin, Elena Suvorova, Maksim Spiridonov, Dmitrii Negrov, Anna Chernikova, Andrey Markeev, and Andrei Zenkevich. Erratum: "Fully ALD-grown TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN stacks: Ferroelectric and structural properties" [Appl. Phys. Lett. 109, 192903 (2016)]. *Applied Physics Letters*, 109(25):259901, 12 2016. ISSN 0003-6951. doi: 10.1063/1.4972787. URL https://doi.org/10.1063/1.4972787.

[55] J H Choi, Y Mao, and J P Chang. Development of hafnium based high-k materials - A review. *Materials Science and Engineering: R: Reports*, 72:97–136, 2011. ISSN 0927-796X. doi: https://doi.org/10.1016/j.mser.2010.12.001. URL https://www.sciencedirect.com/science/article/pii/S0927796X10001683.

[56] W. Martienssen and H. Warlimont. *Springer Handbook of Condensed Matter and Materials Data*. Springer Handbook of Condensed Matter and Materials Data. Springer Berlin Heidelberg, 2006. ISBN 9783540304371. URL https://books.google.at/books?id=TnHJX79b3RwC.

[57] Taeho Kim, Minho An, and Sanghun Jeon. Evolution of crystallographic structure and ferroelectricity of $Hf_{0.5}Zr_{0.5}O_2$ films with different deposition rate. 10(1):015104, . ISSN 2158-3226. doi: 10.1063/1.5121454. URL https://pubs.aip.org/aip/adv/article/1076539.

[58] Timofey V. Perevalov, Igor P. Prosvirin, Evgenii A. Suprun, Furqan Mehmood, Thomas Mikolajick, Uwe Schröder, and Vladimir A. Gritsenko. The atomic and electronic structure of $Hf_{0.5}Zr_{0.5}O_2$ and $Hf_{0.5}Zr_{0.5}O_2$:La films. *Journal of Science: Advanced Materials and Devices*, 6(4):595–600, 2021. ISSN 2468-2179. doi: https://doi.org/10.1016/j.jsamd.2021.08.001. URL https://www.sciencedirect.com/science/article/pii/S2468217921000642.

[59] Chin-I Wang, Hsin-Yang Chen, Chun-Yuan Wang, Teng-Jan Chang, Yu-Sen Jiang, Chih-Sheng Chang, and Miin-Jang Chen. Evolution of pronounced ferroelectricity

in $Hf_{0.5}Zr_{0.5}O_2$ thin films scaled down to 3 nm. *J. Mater. Chem. C*, 9:12759–12767, 2021. doi: 10.1039/D1TC01778K. URL http://dx.doi.org/10.1039/D1TC01778K.

[60] R. Materlik, C. Künneth, and A. Kersch. The origin of ferroelectricity in $Hf_{1-x}Zr_xO_2$: A computational investigation and a surface energy model. 117(13):134109. ISSN 0021-8979, 1089-7550. doi: 10.1063/1.4916707. URL http://aip.scitation.org/doi/10.1063/1.4916707.

[61] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki. A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging. In *2007 IEEE International Electron Devices Meeting*, pages 247–250, Dec 2007. doi: 10.1109/IEDM.2007.4418914.

[62] inventors T. Suntola, J. Antson. Method for producing compound thin films, 11 1977.

[63] Richard W. Johnson, Adam Hultqvist, and Stacey F. Bent. A brief review of atomic layer deposition: from fundamentals to applications. 17(5):236–246. ISSN 13697021. doi: 10.1016/j.mattod.2014.04.026. URL https://linkinghub.elsevier.com/retrieve/pii/S1369702114001436.

[64] MultiMedia LLC. Structure of Tetrakis(ethylmethylamino)hafnium. URL https://ereztech.com/product/tetrakisethylmethylaminohafnium-352535-01-4/.

[65] Dae-Hyun Kim, Dae-Hee Kim, Hwa-Ii Seo, and Yeong-Cheol Kim. Interaction of TEMAHf Precursor with OH-Terminated Si (001) Surface: A First Principles Study. *Journal of nanoscience and nanotechnology*, 11:4324–7, 05 2011. doi: 10.1166/jnn.2011.3623.

[66] Kihye Kim. Fabrication and characterization of ferroelectric $Hf_xZr_{(1-x)}O_y$ layers for novel nanosheet devices: from high-k to ferroelectric behaviors. 2023. URL https://doi.org/10.34726/hss.2023.96548.

[67] E Langereis, S B S Heil, H C M Knoops, W Keuning, M C M van de Sanden, and W M M Kessels. In situ spectroscopic ellipsometry as a versatile tool for studying atomic layer deposition. *Journal of Physics D: Applied Physics*, 42(7):073001, mar 2009. doi: 10.1088/0022-3727/42/7/073001. URL https://dx.doi.org/10.1088/0022-3727/42/7/073001.

[68] E.H. Rhoderick and R.H. Williams. *Metal-semiconductor Contacts*. Monographs in

electrical and electronic engineering. Clarendon Press, 1988. ISBN 9780198593355. URL https://books.google.at/books?id=0zcoAQAAMAAJ.

[69] A.J. McAlister and J.L. Murray. The Al-Ge (Aluminum-Germanium) system. *Bulletin of Alloy Phase Diagrams*, 5(4):341–347, 1984. ISSN 0197-0216. doi: 10.1007/BF02872948. URL http://dx.doi.org/10.1007/BF02872948.

[70] Adolf Fick. Ueber diffusion. *Annalen der Physik*, 170(1):59–86, 1855. doi: https://doi.org/10.1002/andp.18551700105. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/andp.18551700105.

[71] Edgar William John Mitchell, John Wesley Mitchell, and Nevill Francis Mott. The work functions of copper, silver and aluminium. *Proceedings of the Royal Society of London. Series A. Mathematical and Physical Sciences*, 210(1100):70–84, 1951. doi: 10.1098/rspa.1951.0231. URL https://royalsocietypublishing.org/doi/abs/10.1098/rspa.1951.0231.

[72] Manijeh Razeghi. *Fundamentals of Solid State Engineering*. Springer International Publishing, 2019. ISBN 978-3-319-75707-0. doi: 10.1007/978-3-319-75708-7.

[73] K.-W. Ang, K. Majumdar, K. Matthews, C. D. Young, C. Kenney, C. Hobbs, P. D. Kirsch, R. Jammy, R. D. Clark, S. Consiglio, K. Tapily, Y. Trickett, G. Nakamura, C. S. Wajda, G. J. Leusink, M. Rodgers, and S. C. Gausepohl. Effective Schottky Barrier Height modulation using dielectric dipoles for source/drain specific contact resistivity improvement. In *2012 International Electron Devices Meeting*, pages 18.6.1–18.6.4, 2012. doi: 10.1109/IEDM.2012.6479068.

[74] Tomonori Nishimura, Koji Kita, and Akira Toriumi. Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface. *Applied Physics Letters*, 91:123123, Sep 2007. ISSN 0003-6951. doi: 10.1063/1.2789701. URL https://doi.org/10.1063/1.2789701.

[75] Harald Ibach and Hans Lüth. *Solid-State Physics*. Springer Berlin Heidelberg, 2009. ISBN 978-3-540-93803-3. doi: 10.1007/978-3-540-93804-0.

[76] Horng-Chih Lin, C. Y. Lin, K. L. Yeh, R. G. Huang, M. F. Wang, C. M. Yu, T. Y. Huang, and S. M. Sze. A novel implantless MOS thin-film transistor with simple processing, excellent performance and ambipolar operation capability. *Technical Digest - International Electron Devices Meeting*, pages 857–859, January 2000. ISSN 0163-1918. doi: 10.1109/IEDM.2000.904452.

[77] Ö. Demirkiran. Reconfigurable Si Field-Effect Transistors with Crystalline Al Contacts Enabling Adaptive Complementary and Combinational Logic. 2023. URL https://doi.org/10.34726/hss.2023.102523.

[78] Raphael Böckle, Masiar Sistani, Boris Lipovec, Darius Pohl, Bernd Rellinghaus, Alois Lugstein, and Walter M. Weber. A Top-Down Platform Enabling Ge Based Reconfigurable Transistors. *Advanced Materials Technologies*, 7(1):2100647, 2022.

doi: https://doi.org/10.1002/admt.202100647. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/admt.202100647.

[79] L. Kühberger. A Germanium on Silicon on Insulator Based Reconfigurable Transistor Platform. 2023. URL https://doi.org/10.34726/hss.2023.109260.

[80] T. Mikolajick, G. Galderisi, S. Rai, M. Simon, R. Böckle, M. Sistani, C. Cakirlar, N. Bhattacharjee, T. Mauersberger, A. Heinzig, A. Kumar, W.M. Weber, and J. Trommer. Reconfigurable field effect transistors: A technology enablers perspective. *Solid-State Electronics*, 194:108381, 2022. ISSN 0038-1101. doi: https://doi.org/10.1016/j.sse.2022.108381. URL https://www.sciencedirect.com/science/article/pii/S0038110122001538.

[81] T Mikolajick, A Heinzig, J Trommer, T Baldauf, and W M Weber. The RFET - a reconfigurable nanowire transistor and its application to novel electronic circuits and systems. *Semiconductor Science and Technology*, 32(4):043001, Mar 2017. doi: 10.1088/1361-6641/aa5581. URL https://dx.doi.org/10.1088/1361-6641/aa5581.

[82] Raphael Böckle, Masiar Sistani, Martina Bažíková, Lukas Wind, Zahra Sadre-Momtaz, Martien I. den Hertog, Corban G. E. Murphey, James F. Cahoon, and Walter M. Weber. Reconfigurable Complementary and Combinational Logic Based on Monolithic and Single-Crystalline Al-Si Heterostructures. *Advanced Electronic Materials*, n/a(n/a):2200567, 2022. doi: https://doi.org/10.1002/aelm.202200567. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/aelm.202200567.

[83] W.M. Weber, A. Heinzig, J. Trommer, D. Martin, M. Grube, and T. Mikolajick. Reconfigurable nanowire electronics - A review. *Solid-State Electronics*, 102:12–24, 2014. ISSN 0038-1101. doi: https://doi.org/10.1016/j.sse.2014.06.010. URL https://www.sciencedirect.com/science/article/pii/S0038110114001439. Selected papers from ESSDERC 2013.

[84] W.M. Weber and T. Mikolajick. Silicon and germanium nanowire electronics: physics of conventional and unconventional transistors. *Reports on Progress in Physics*, 80(6):066502, Apr 2017. doi: 10.1088/1361-6633/aa56f0. URL https://doi.org/10.1088/1361-6633/aa56f0.

[85] T. Mikolajick, G. Galderisi, M. Simon, S. Rai, A. Kumar, A. Heinzig, W.M. Weber, and J. Trommer. 20 years of reconfigurable field-effect transistors: From concepts to future applications. *Solid-State Electronics*, 186:108036, 2021. ISSN 0038-1101. doi: https://doi.org/10.1016/j.sse.2021.108036. URL https://www.sciencedirect.com/science/article/pii/S0038110121000812.

[86] J Trommer, A Heinzig, T Baldauf, T Mikolajick, W M Weber, M Raitza, and M Völp. Reconfigurable nanowire transistors with multiple independent gates for efficient and programmable combinational circuits. In *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 169–174, 2016. ISBN 1558-1101.

[87] Raphael Böckle, Masiar Sistani, Martina Bažìková, Lukas Wind, Zahra Sadre-Momtaz, Martien I. den Hertog, Corban G. E. Murphey, James F. Cahoon, and Walter M. Weber. Reconfigurable Complementary and Combinational Logic Based on Monolithic and Single-Crystalline Al-Si Heterostructures. *Advanced Electronic Materials*, 9(1):2200567, 2023. doi: https://doi.org/10.1002/aelm.202200567. URL `https://onlinelibrary.wiley.com/doi/abs/10.1002/aelm.202200567`.

[88] Fengben Xi, Yi Han, Mingshan Liu, Jin Hee Bae, Andreas Tiedemann, Detlev Grützmacher, and Qing-Tai Zhao. Artificial Synapses Based on Ferroelectric Schottky Barrier Field-Effect Transistors for Neuromorphic Applications. *ACS Applied Materials & Interfaces*, 13(27):32005–32012, 2021. doi: 10.1021/acsami.1c07505. URL `https://doi.org/10.1021/acsami.1c07505`. PMID: 34171195.

[89] J H. Bae, H Kim, D Kwon, S Lim, S T. Lee, B G. Park, and J H. Lee. Reconfigurable Field-Effect Transistor as a Synaptic Device for XNOR Binary Neural Network. *IEEE Electron Device Letters*, 40:624–627, 2019. ISSN 1558-0563. doi: 10.1109/LED.2019.2898448.

[90] D. A. Buck. Ferroelectrics for Digital Information Storage and Switching. 1952. URL `https://api.semanticscholar.org/CorpusID:58236202`.

[91] J.L. Moll and Y. Tarui. A new solid state memory resistor. *IEEE Transactions on Electron Devices*, 10(5):338–338, 1963. doi: 10.1109/T-ED.1963.15245.

[92] C.-J. Su, T.-C. Hong, Y.-C. Tsou, F.-J. Hou, P.-J. Sung, M.-S. Yeh, C.-C. Wan, K.-H. Kao, Y.-T. Tang, C.-H. Chiu, C.-J. Wang, S.-T. Chung, T.-Y. You, Y.-C. Huang, C.-T. Wu, K.-L. Lin, G.-L. Luo, K.-P. Huang, Y.-J. Lee, T.-S. Chao, W.-F. Wu, G.-W. Huang, J.-M. Shieh, W.-K. Yeh, and Y.-H. Wang. Ge nanowire FETs with HfZrOx ferroelectric gate stack exhibiting SS of sub-60 mV/dec and biasing effects on ferroelectric reliability. In *2017 IEEE International Electron Devices Meeting (IEDM)*, pages 15.4.1–15.4.4. IEEE. ISBN 978-1-5386-3559-9. doi: 10.1109/IEDM.2017.8268396. URL `http://ieeexplore.ieee.org/document/8268396/`.

[93] C.-Y. Liao, K.-Y. Hsiang, Z. F. Lou, H.-C. Tseng, C.-Y. Lin, Z.-X. Li, F.-C. Hsieh, C.-C. Wang, F.-S. Chang, W.-C. Ray, Y.-Y. Tseng, S. T. Chang, T.-C. Chen, and M. H. Lee. Endurance $> 10^{11}$ Cycling of 3D GAA Nanosheet Ferroelectric FET with Stacked $HfZrO_2$ to Homogenize Corner Field Toward Mitigate Dead Zone for High-Density eNVM. In *2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)*, pages 1–2, 2022. doi: 10.1109/VLSITechnologyandCir46769.2022.9830345.

[94] V. Sessi, H. Mulaosmanovic, R. Hentschel, S. Pregl, T. Mikolajick, and W. M. Weber. Junction Tuning by Ferroelectric Switching in Silicon Nanowire Schottky-Barrier Field Effect Transistors. In *2018 IEEE 18th International Conference on Nanotechnology (IEEE-NANO)*, pages 1–4. IEEE, . ISBN 978-1-5386-5336-4. doi: 10.1109/NANO.2018.8626257. URL `https://ieeexplore.ieee.org/document/8626257/`.

[95] Violetta Sessi, Maik Simon, Halid Mulaosmanovic, Darius Pohl, Markus Loeffler,

Tom Mauersberger, Franz P. G. Fengler, Terence Mittmann, Claudia Richter, Stefan Slesazeck, Thomas Mikolajick, and Walter M. Weber. A silicon nanowire ferroelectric field-effect transistor. 6(4):1901244, . ISSN 2199-160X, 2199-160X. doi: 10.1002/aelm.201901244. URL https://onlinelibrary.wiley.com/doi/10.1002/aelm.201901244.

[96] Spaldin N. Stengel, M. Origin of the dielectric dead layer in nanoscale capacitors. *Nature*, 2006. URL https://doi.org/10.1038/nature05148.

[97] Sayeef Salahuddin and Supriyo Datta. Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices. 8(2):405–410. ISSN 1530-6984, 1530-6992. doi: 10.1021/nl071804g. URL https://pubs.acs.org/doi/10.1021/nl071804g.

[98] Justin C. Wong and Sayeef Salahuddin. Negative Capacitance Transistors. *Proceedings of the IEEE*, 107(1):49–62, 2019. doi: 10.1109/JPROC.2018.2884518.

[99] Michael Hoffmann, Prasanna Ravindran, and Asif Khan. Why Do Ferroelectrics Exhibit Negative Capacitance? *Materials*, 12:3743, 11 2019. doi: 10.3390/ma12223743.

[100] Wei Cao and Kaustav Banerjee. Is negative capacitance FET a steep-slope logic switch? 11(1):196. ISSN 2041-1723. doi: 10.1038/s41467-019-13797-9. URL https://www.nature.com/articles/s41467-019-13797-9.

[101] Website TU Wien X-Ray Center. URL https://www.tuwien.at/en/research/facilities/xrc.

[102] Tektronix. C-V Testing for Semiconductor Components and Devices - Applications Guide. URL https://www.tek.com/en/documents/application-note/c-v-testing-semiconductor-components-and-devices-applications-guide#:~:text=Capacitance%2Devoltage%20(C%2DV)%20measurements,without%20a%20source%20and%20drain.

[103] C. Kittel. *Introduction to Solid State Physics*. Wiley, 1996. ISBN 9780471111818. URL https://books.google.at/books?id=1X8pAQAAMAAJ.

[104] C. B. Sawyer and C. H. Tower. Rochelle Salt as a Dielectric. *Phys. Rev.*, 35:269–273, Feb 1930. doi: 10.1103/PhysRev.35.269. URL https://link.aps.org/doi/10.1103/PhysRev.35.269.

[105] Huie Zhu, Tokuji Miyashita, and Masaya Mitsuishi. Energy storage behaviors in ferroelectric capacitors fabricated with sub-50 nm poly(vinylidene fluoride) Langmuir-Blodgett nanofilms. *Polymer Journal*, 51, 04 2019. doi: 10.1038/s41428-019-0194-3.

[106] Klaus Prume, Thorsten Schmitz, and Stephan Tiedke. *Electrical Characterization of Ferroelectrics*, chapter 3, pages 53–75. John Wiley & Sons, Ltd, 2004. ISBN 9783527604654. doi: https://doi.org/10.1002/3527604650.ch3. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/3527604650.ch3.

[107] Abhilash Joseph, Nidhi Sinha, Sahil Goel, Abid Hussain, Harsh Yadav, and Binay Kumar. New quaternary BNT-BT-PMN-PT ceramic: ferro-/piezo-/pyroelectric characterizations. *Journal of Materials Science: Materials in Electronics*, 30, 07 2019. doi: 10.1007/s10854-019-01637-x.

[108] Vineetha Mukundan, Steven Consiglio, Dina H. Triyoso, Kandabara Tapily, Martin E. McBriarty, Sandra Schujman, Karsten Beckmann, Jubin Hazra, Vidya Kaushik, Nathaniel Cady, Robert D. Clark, Gert J. Leusink, and Alain C. Diebold. Ferroelectric Phase content in 7 nm $Hf_{1-x}Zr_xO_2$ Thin Films Determined by X-Ray-Based Methods. *physica status solidi (a)*, 218(10):2100024, 2021. doi: https://doi.org/10.1002/pssa.202100024. URL `https://onlinelibrary.wiley.com/doi/abs/10.1002/pssa.202100024`.

[109] A. Ogi and Katsuhiko Inaba. X-ray thin-film measurement techniques VI. Small Angle X-ray Scattering. URL `https://api.semanticscholar.org/CorpusID:32396507`.

[110] Mario Birkholz, Paul Fewster, and Christoph Genzel. *Thin Film Analysis by X-ray Scattering*, volume 58. 11 2005. ISBN 3527310525978352731052 4. doi: 10.1016/j.matchar.2006.04.026.

[111] Si Joon Kim, Dushyant Narayan, Jae-Gil Lee, Jaidah Mohan, Joy S. Lee, Jaebeom Lee, Harrison S. Kim, Young-Chul Byun, Antonio T. Lucero, Chadwin D. Young, Scott R. Summerfelt, Tamer San, Luigi Colombo, and Jiyoung Kim. Large ferroelectric polarization of $TiN/Hf_{0.5}Zr_{0.5}O_2$ /TiN capacitors due to stress-induced crystallization at low thermal budget. 111(24):242901, . ISSN 0003-6951, 1077-3118. doi: 10.1063/1.4995619. URL `http://aip.scitation.org/doi/10.1063/1.4995619`.

[112] W. Kern and J. Vossen. Thin Film Processes. *Academic Press*, 1978.

[113] TU Delft. RCA-2 Silicon Wafer Cleaning. URL `https://filelist.tudelft.nl/TNW/Afdelingen/Quantum%20Nanoscience/Kavli%20Nanolab%20Delft/Equipment/RCA-2%20SOP.pdf`.

[114] Supawan Joonwichien, Yasuhiro Kida, Masaaki Moriya, Satoshi Utsunomiya, Katsuhiko Shirasawa, and Hidetaka Takato. Assisted passivation by a chemically grown sio2 layer for p-type selective emitter-passivated emitter and rear cells. *Solar Energy Materials and Solar Cells*, 186:84–91, 2018. ISSN 0927-0248. doi: https://doi.org/10.1016/j.solmat.2018.06.018. URL `https://www.sciencedirect.com/science/article/pii/S0927024818303064`.

[115] W. Kern. *Handbook of Semiconductor Cleaning Technology*. Noyes Publishing:Park Ridge, 1993.

[116] National Research Council. Prudent Practices in the laboratory. 1995.

[117] Takashi Onaya, Toshihide Nabatame, Naomi Sawamoto, Akihiko Ohi, Naoki Ikeda, Takahiro Nagata, and Atsushi Ogura. Improvement in ferroelectricity of $Hf_xZr_{1-x}O_2$

thin films using top- and bottom-ZrO_2 nucleation layers. 7(6):061107. ISSN 2166-532X. doi: 10.1063/1.5096626. URL http://aip.scitation.org/doi/10.1063/1.5096626.

[118] Ji-Na Song, Min-Jung Oh, and Chang-Bun Yoon. Effect of a ZrO_2 Seed Layer on an $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Device Fabricated via Plasma Enhanced Atomic Layer Deposition. *Materials*, 16(5), 2023. ISSN 1996-1944. doi: 10.3390/ma16051959. URL https://www.mdpi.com/1996-1944/16/5/1959.

[119] T. Onaya, T. Nabatame, N. Sawamoto, Akihiko Ohi, Naoki Ikeda, T. Nagata, and A. Ogura. Impact of Top-ZrO_2 Nucleation Layer on Ferroelectricity of $Hf_xZr_{1-x}O_2$ Thin Films for Ferroelectric Field Effect Transistor Application. 09 2018. doi: 10.7567/SSDM.2018.C-7-03.

[120] Shelby S. Fields, Truong Cai, Samantha T. Jaszewski, Alejandro Salanova, Takanori Mimura, Helge H. Heinrich, Michael David Henry, Kyle P. Kelley, Brian W. Sheldon, and Jon F. Ihlefeld. Origin of Ferroelectric Phase Stabilization via the Clamping Effect in Ferroelectric Hafnium Zirconium Oxide Thin Films. *Advanced Electronic Materials*, 8(12):2200601, 2022. doi: https://doi.org/10.1002/aelm.202200601. URL https://onlinelibrary.wiley.com/doi/abs/10.1002/aelm.202200601.

[121] Yu-Hsuan Yeh, Wen-Chung Chen, Ting-Chang Chang, Yung-Fang Tan, Chung-Wei Wu, Yong-Ci Zhang, Ya-Huan Lee, Chao Cheng Lin, Hui-Chun Huang, and Simon M Sze. Degradation mechanism differences between TiN- and TaN-electrode HZO-based FeRAMs analyzed by current mechanism fitting. *Semiconductor Science and Technology*, 38(8):085004, jun 2023. doi: 10.1088/1361-6641/acde9f. URL https://dx.doi.org/10.1088/1361-6641/acde9f.

[122] Wenwu Xiao, Chen Liu, Yue Peng, Shuaizhi Zheng, Qian Feng, Chunfu Zhang, J.F. Zhang, Yue Hao, Min Liao, and Yichun Zhou. Thermally Stable and Radiation Hard Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Thin Films on Muscovite Mica for Flexible Nonvolatile Memory Applications. 1:919–927, 05 2019. doi: 10.1021/acsaelm.9b00107.

[123] Hyungwoo Kim, Alireza Kashir, Seungyeol Oh, and Hyunsang Hwang. A new approach to achieving strong ferroelectric properties in $TiN/Hf_{0.5}Zr_{0.5}O_2/TiN$ devices. *Nanotechnology*, 32(5):055703, nov 2020. doi: 10.1088/1361-6528/abc115. URL https://dx.doi.org/10.1088/1361-6528/abc115.

[124] Guo-Liang Tian, Jin-Shun Bi, Gao-Bo Xu, Kai Xi, Yan-Nan Xu, Xue-Qin Yang, Hua-Xiang Yin, Qiu-Xia Xu, and Yong-Liang Li. $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric bionic electronic synapse device with highly symmetrical and linearity weight modification. *Electronics Letters*, 56(16):840–843, 2020. doi: https://doi.org/10.1049/el.2020.0423. URL https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/el.2020.0423.

[125] Roman Khakimov, A. Chernikova, Yury Lebedinskii, Alexandra Koroleva, and Andrey Markeev. Influence of the Annealing Temperature and Applied Electric Field

on the Reliability of TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN Capacitors. *ACS Applied Electronic Materials*, 3, 09 2021. doi: 10.1021/acsaelm.1c00511.

[126] Nujhat Tasneem, Harshil Kashyap, Kisung Chae, Chinsung Park, Ping-che Lee, Sarah F Lombardo, Nashrah Afroze, Mengkun Tian, Harish Kumarasubramanian, Jae Hur, Hang Chen, Winston Chern, Shimeng Yu, Prabhakar Bandaru, Jayakanth Ravichandran, Kyeongjae Cho, Josh Kacher, Andrew C. Kummel, and Asif Islam Khan. Remote Oxygen Scavenging of the Interfacial Oxide Layer in Ferroelectric Hafnium-Zirconium Oxide-Based Metal-Oxide-Semiconductor Structures. 14(38): 43897–43906. ISSN 1944-8244, 1944-8252. doi: 10.1021/acsami.2c11736. URL https://pubs.acs.org/doi/10.1021/acsami.2c11736.

[127] L.P.B. Lima, J.A. Diniz, I. Doi, and J. Godoy Fo. Titanium nitride as electrode for MOS technology and Schottky diode: Alternative extraction method of titanium nitride work function. *Microelectronic Engineering*, 92:86–90, 2012. ISSN 0167-9317. doi: https://doi.org/10.1016/j.mee.2011.04.059. URL https://www.sciencedirect.com/science/article/pii/S0167931711004850. 27th Annual Advanced Metallization Conference 2010.

[128] R. Jaeckel and B. Wagner. Photo-electric measurement of the work function of metals and its alteration after gas adsorption. *Vacuum*, 13(12):509–511, 1963. ISSN 0042-207X. doi: https://doi.org/10.1016/0042-207X(63)90537-2. URL https://www.sciencedirect.com/science/article/pii/0042207X63905372.

[129] J. G. Gay, J. R. Smith, F. J. Arlinghaus, and T. W. Capehart. Electronic structure of palladium (100). *Phys. Rev. B*, 23:1559–1566, Feb 1981. doi: 10.1103/PhysRevB.23.1559. URL https://link.aps.org/doi/10.1103/PhysRevB.23.1559.

[130] Dieter K. Schroder. *Semiconductor Material and Device Characterization*. John Wiley & Sons, Inc., Oct 2005. ISBN 9780471749097. doi: 10.1002/0471749095.

[131] Yuh-Chen Lin, Felicia McGuire, and Aaron D. Franklin. Realizing ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ with elemental capping layers. 36(1):011204. ISSN 2166-2746, 2166-2754. doi: 10.1116/1.5002558. URL http://avs.scitation.org/doi/10.1116/1.5002558.

[132] Rongrong Cao, Yan Wang, Shengjie Zhao, Yang Yang, Xiaolong Zhao, Wei Wang, Xumeng Zhang, Hangbing Lv, Qi Liu, and Ming Liu. Effects of Capping Electrode on Ferroelectric Properties of $Hf_{0.5}Zr_{0.5}O_2$ Thin Films. 39(8):1207–1210. ISSN 0741-3106, 1558-0563. doi: 10.1109/LED.2018.2846570. URL https://ieeexplore.ieee.org/document/8382182/.

[133] Jin-Ju Kim, Seung-Eon Moon, and Sung-Min Yoon. Fabrication Strategies of Metal-Ferroelectric-Insulator-Silicon Gate Stacks Using Ferroelectric Hf-Zr-O and High-k HfO_2 Insulator Layers for Securing Robust Ferroelectric Memory Characteristics. 4 (6):2953–2963, . doi: 10.1021/acsaelm.2c00402. URL https://doi.org/10.1021/acsaelm.2c00402. Publisher: American Chemical Society.

[134] Stephen L. Weeks, Ashish Pal, Vijay K. Narasimhan, Karl A. Littau, and Tony Chiang. Engineering of Ferroelectric HfO_2-ZrO_2 Nanolaminates. *ACS Applied Materials & Interfaces*, 9(15):13440–13447, 2017. doi: 10.1021/acsami.7b00776. URL `https://doi.org/10.1021/acsami.7b00776`. PMID: 28337909.

[135] Swiss Federal Laboratories for Materials Science and Technology. URL `https://www.empa.ch/`.