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Automated Verification of Programmable Logic Controller Programs against Structured Natural Language Requirements

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Executive Summary

PLCverif is an actively developed project at CERN, enabling the formal verification of Programmable Logic Controller (PLC) programs in critical systems. In this paper, we present our work on improving the formal requirements specification experience in PLCverif through the use of natural language. To this end, we integrate NASA's FRET, a formal requirement elicitation and authoring tool, into PLCverif. FRET is used to specify formal requirements in structured natural language, which automatically translates into temporal logic formulae. FRET's output is then directly used by PLCverif for verification purposes. We discuss practical challenges that PLCverif users face when authoring requirements and the FRET features that help alleviate these problems. We present the new requirement formalization workflow and report our experience using it on two critical CERN case studies.

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Chapter 1

Introduction

Over the past few years, formal verification has become a crucial part in the process of software development for critical applications. To this end, CERN's open-source tool PLCverif [4] opened the door for the verification of Programmable Logic Controller (PLC) programs [2, 5, 6] and it has successfully been used to verify several safety-critical applications [7–9].

Given PLC code and a set of requirements formalized in either computation tree logic (CTL) or future-time linear temporal logic (LTL), PLCverif automatically transforms these to an intermediate mathematical model, i.e., control flow automata (CFA) [10]. Once the intermediate model is obtained, PLCverif supports its translation into the input language of various model checkers for verification. Finally, analysis results are presented to the user in a convenient and easy-to-understand format.

The aforementioned process relies on control and safety engineers formalizing requirements. Prior to this work, PLCverif already supported the use of natural language templates, which are a set of pre-made templates with "blanks" where expressions containing variables of the PLC program can be added (e.g., "{1} is always true at the end of the PLC cycle"). During formalization, pattern instantiations are translated to LTL or CTL based on the pre-made templates. However, the expressive power of the existing templates is limited.

In this technical report, we extend our work presented at NFM'23 [11]. We present the integration of NASA Ames' Formal Requirements Elicitation Tool (FRET [12–14]) into PLCverif, which provides a structured natural requirements language with an underlying temporal logic semantics. The integration of FRET within PLCverif helps users express and formalize a greater range of requirements and understand their semantics. The toolchain was successfully used in two critical CERN case studies: a safety program of a superconducting magnet test facility and a module of a process control library.

Zsófia Ádám and Ignacio D. Lopez-Miguel – Work performed while at CERN.

Chapter 2

Background

2.1 Temporal logic

Temporal logic is the most commonly used way to formalize a requirement for model checking. It is a form of logic specifically tailored for statements and reasoning which involves the notion of order in time [15] and it was first introduced by Amir Pnueli [16].

Linear temporal logic (LTL) is a modal logic in which modalities refer to time [16]. It allows the encoding of properties over individual paths. Usually, LTL is an abbreviation for future-time LTL, that is, it will only consider future states. Its syntax allows the use of propositional variables together with the temporal operators `X` (next) and `U` (until). Operators such as `G` (globally/always), and `F` (finally/eventually) can be derived from the former. A future-time LTL formula is valid for a program if all its execution traces starting from an initial state satisfy it.

Analogously, past-time LTL is defined with the temporal operators `Y` (previous) and `S` (since), with which other operators can be derived, such as `H` (historically) and `O` (once). A past-time LTL formula is valid for a program if all its execution traces leading to the current state satisfy it.

Future-time metric (linear) temporal logic (MTL) [17] is an extension of LTL, in which modalities are augmented with time-bounded constraints. Analogously, past-time metric LTL includes time-bounded constraints and it only refers to previous states.

Computation tree logic (CTL), in contrast to LTL, allows the encoding of properties over all possible paths starting from a state. In order to do so, it uses the universal quantifier, `A` (for all paths), and the existential quantifier, `E` (exists one path), over these paths to precede the temporal operators from future-time LTL.

FRET supports future- and past-time LTL, and their metric variants. In contrast, PLCverif supports future-time LTL and CTL.

Although many relevant properties of reactive systems can be specified in both LTL and CTL [18], the logics CTL and LTL are incomparable in their expressiveness. More precisely, there are properties that can be expressed in CTL, but cannot be expressed in LTL, and vice versa [19]. As an example, let us consider the (reachability) CTL formula `AG EF a` for which no equivalent LTL formula exists. Similarly, let us consider the (stability) LTL formula `FG a`, for which no equivalent CTL formula exists.

2.2 PLCverif

PLCverif is a customizable and extensible, plugin-based framework developed at CERN to support formal verification of PLC programs. It translates automatically PLC code and a given set of requirements to the input format of various model checkers, which are then executed. Their output is presented to the user in a convenient, easy-to-understand format. This workflow is shown in Figure 2.1, extracted from [1–3]. It consists of the following parts:

- **PLC code**. This is the code the user wants to verify. It can be written in Structured Text (ST) or Instruction List (IL).
- **Specification**. It is the property the user wants the code to satisfy. This can be given as an assertion directly writing it into the code, or in a non-intrusive way by selecting a requirement pattern from the GUI of PLCverif (Figure 5.3).
  - **Assertion**. If the user wants to verify that a given property is satisfied at a certain point of the code, an assertion can be used. This is written directly into the PLC code by using the keyword for assertions `//#ASSERT`.
  - **Requirement pattern**. There is a set of requirements that are available to the user directly in the GUI. Some of these will reflect the behavior of the system over time. The patterns that can be selected are listed below, where `PLC_END` represents the end of the PLC cycle, `PLC_START` the beginning of the PLC cycle, and `{i}` a blank that has to be filled by the user including expressions containing program variables. Their formulations are written in temporal logic (CTL or LTL).
    * *Implication*. `AG((PLC_END AND ({1})) -> ({2}))`. If {1} is true at the end of the PLC cycle, then {2} should always be true at the end of the same cycle.
    * *Invariant*. `AG(PLC_END -> ({1}))`. {1} is always true at the end of the PLC cycle.
    * *Forbidden state*. `AG(PLC_END -> NOT ({1}))`. {1} is impossible at the end of the PLC cycle.
    * *State change during a cycle*. `AG((PLC_START AND ({1})) -> A[ NOT PLC_END U PLC_END AND ({2}) ])` If {1} is true at the beginning of the PLC cycle, then {2} is always true at the end of the same cycle.
    * *State change between cycles*. `G((PLC_END AND ({1}) AND X( [ NOT PLC_END U (PLC_END AND ({2})) ] )) -> X( [ NOT PLC_END U (PLC_END AND ({3})) ] ))`. If {1} is true at the end of cycle N and {2} is true at the end of cycle N+1, then {3} is always true at the end of cycle N+1.
    * *Reachability*. `EF(PLC_END AND ({1}))`. It is possible to have {1} at the end of a cycle.
    * *Repeatability*. `AG(EF(PLC_END AND ({1})))`. Any time it is possible to have eventually {1} at the end of a cycle.
    * *Leads to*. `NOT (E[(PLC_END -> NOT ({2})) U (PLC_END AND {1})])`. If {1} is true at the end of a cycle, {2} was true at the end of an earlier cycle.
- **Intermediate model**. This is the strategy to model the given code and it is based on a network of automata representing the control flow graph of the PLC program.

Each of these automata is a Control Flow Automaton (CFA) [10]. Figure 2.2 shows a PLC cycle represented as a CFA, which calls its main function in every cycle (Figure 2.3). This main function expresses as a CFA the code shown in listing 2.1.

Input variables are modeled as non-deterministic since the external system to which the PLC is connected is not modeled, and, hence, these inputs could have any possible value.

- **Formalized requirement**. The property needs to be translated into an LTL or CTL formula if it is needed by the model checker.

- **Reductions**. Once the intermediate model is built and the requirements are formalized, it is possible to search for possible reductions of the intermediate model in order to improve the performance. As an example, please refer to in [20] to see the cone of influence (COI) reduction.

- **Backends**. When all the reductions are done, PLCverif will translate the resulting model into the specific language supported by the model checker, which is selected by the user. Then, the model checker will be executed and will produce an output, which can be a proof that the property holds or a counterexample indicating that there was a violation of the property. The three symbolic model checkers that are used are NuSMV/nuXmv [21], CBMC [22], and Theta [23].

  These general-purpose model checkers are considered to be state-of-the-art due to their performance. For these reasons and for the possibility to translate the intermediate model into their languages, they were selected as the backends for PLCverif [4].

- **Verification report**. The output produced by the model checker is processed and shown to the user in a human-readable reporting the verification result. If there is a violation of the property, it will include a counterexample demonstrating it.

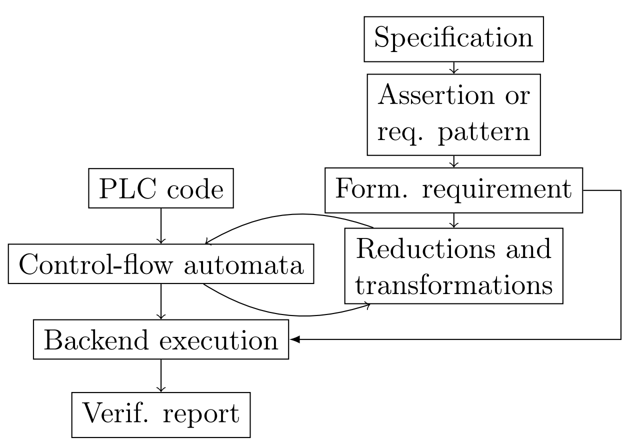


Figure 2.1: Verification process workflow using PLCverif. Given a specification and PLC code, after various intermediate steps, it generates a report specifying if the specification is satisfied or violated. More information can be found in [1–3].

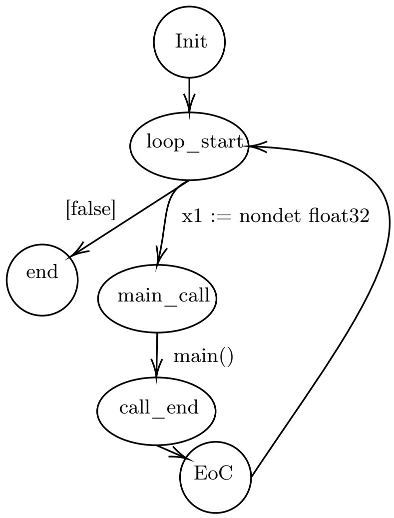


Figure 2.2: CFA–Main PLC cycle.

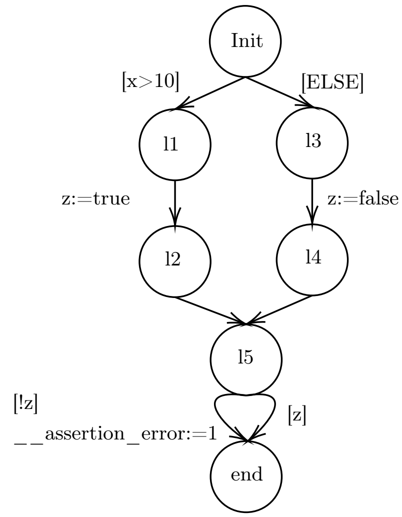


Figure 2.3: CFA–Example.

```
FUNCTION_BLOCK main
	VAR_INPUT
		x : REAL;
	END_VAR
	VAR_OUTPUT
		z : BOOL;
	END_VAR

BEGIN
	IF x>10 THEN
		z := TRUE;
	ELSE
		z := FALSE;
	END_IF;

//#ASSERT z : zTrueAssertion;
END_FUNCTION_BLOCK
```

Listing 2.1: Example of a PLC program in ST.

2.3 FRET

The NASA Formal Requirements Elicitation Tool (FRET) is an open-source framework for creating and understanding formal requirements [12,24]. The core of FRET is defined by its input language, namely FRETish, a structured natural language with strict formal semantics [25]. The core engine is surrounded by features that enable users to efficiently create, manage, understand, and analyze FRETish requirements [14,26]. Example features are the pre-defined FRETish templates, the Glossary component, the requirements simulator LTLSIM and the FRET Analysis Portal. Throughout the years, FRET has been experimentally used to formalize and analyze requirements in several NASA projects [27–31].

A FRETish requirement is described using up to six distinct fields (the * symbol designates mandatory fields): 1) `scope` specifies the time intervals where the requirement is enforced, 2) `condition` is a Boolean expression that triggers the `response` to occur at the time the expression's value becomes true, or is true at the beginning of the scope interval,

3) `component*` is the system component that the requirement is levied upon, 4) `shall*` is used to express that the component's behavior must conform to the requirement, 5) `timing` specifies when the response shall happen, subject to the constraints defined in `scope` and `condition` and 6) `response*` is the Boolean expression that the component's behavior must satisfy.

FRETish provides 8 scopes: *global*, *in*, *before*, *after*, *notin*, *only in*, *only before*, and *only after*. The scope *global* means *always*; the others are with respect to when the system is in a mode or satisfies a Boolean expression. For example, *In mode M* means the requirement is enforced when the system is in mode M, as determined by the Boolean variable M. Also allowed for scope in place of a single Boolean variable is a Boolean expression, except for *in* which in the expression case is written with *while*; e.g., *While vehicle_mode = hover*. In FRETish, the optional condition field is introduced by the words *upon*, *when*, or *if*, which are synonymous in FRETish, or the word *unless*, which is the same as *when !*. FRETish provides 10 timings: *immediately*, *at the next timepoint*, *always*, *eventually*, *never*, *for* N time steps, *within* N time steps, *after* N time steps, *until* *bool_ expr*, and *before* *bool_ expr*. When the scope is omitted it is taken as *global*; when the condition is omitted, it is taken as `true`; when the timing is omitted, it is taken as *eventually*. If we consider the condition being omitted as a separate case, there are $8 \times 2 \times 10 = 160$ possible combinations of $\langle$*scope*, *condition*, *timing*$\rangle$, each formalized as a distinct LTL formula template. The templates are generated by an algorithm that has been formally proven to generate formalizations with the intended semantics [32].

Boolean expressions can use the standard logical connectives (!, &, |) and can involve arithmetic relations (=,!=,<,<=,>,>=) and operators ($+,-,*,/$) over integer and real variables. There are two predefined predicates *preInt* and *preReal* that refer to previous values: the expression $preInt(init, n)$, for integer expression n, returns the value of n at the previous timepoint; if at the beginning of the trace where there is no previous value, then the value of *init* is returned. Currently, FRETish does not allow arbitrary nesting of temporal operators, e.g. "*In mode m, before q the system shall ...*". Timed operators with intermediate bounds are also not currently expressible; e.g., the equivalent of `H[i,j] p`, where `i` $\neq$ `0`.

For each FRETish requirement, FRET generates formulae in a variety of formalisms, including pure future-time LTL and pure past-time LTL, as well as their metric (MTL) variants.

Chapter 3

Integrating FRET into PLCverif

FRET's user interface was designed with usability in mind; engineers with varying levels of experience in formal methods can express requirements using FRETish, a restricted natural language plus standard Boolean/arithmetic expressions with precise, unambiguous meaning. For a FRETish requirement, FRET produces textual and diagrammatic explanations of its exact meaning and temporal logic formalizations in Metric LTL. FRET also supports interactive simulation of the generated logical formulae to increase confidence that they capture the intended semantics.

3.1 Limitations of Requirement Formulation in PLCverif

As already anticipated in the introduction, PLCverif *patterns* have significant limitations:

1. they offer a *limited set of 8 pre-made templates* only,
2. they do not offer any tool for *validation* of complex requirements; i.e., methods for checking if the created requirement is the same as the intended one.

FRET is able to improve on the current limitations the following ways:

Expressive Power. Users are able to formulate requirements in FRETish as constrained and unambiguous sentences, which are then automatically transformed to LTL expressions.

Validation. FRET has a built-in simulator, allowing the user to check different temporal variable valuations. Furthermore, FRET generates a textual and diagrammatic description of the requirement to further help precise understanding.

3.2 Realization of the New Workflow with FRET

The bold parts of Figure 3.1 show how FRET fits into the workflow of PLCverif. If "Edit in FRET" is chosen, FRET is opened and the user can work in the requirement editor. Once the requirement is written in FRETish and formalized, it is then sent back to PLCverif.

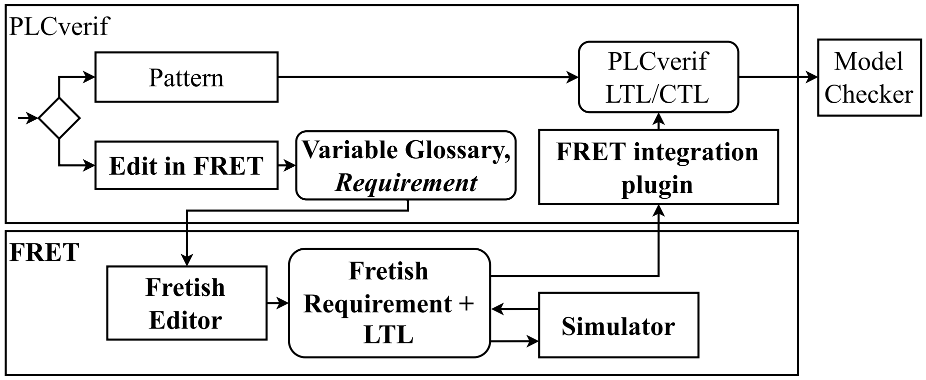


Figure 3.1: Requirement formalization workflow in PLCverif. Features integrated into PLCverif in this work are shown in bold.

The External Mode of FRET. The feature set of FRET covers much more than what PLCverif could currently utilize (e.g., requirement hierarchies). PLCverif handles each requirement in a separate verification case, thus only the following features are utilized: the requirement editor, the formalization component and the requirements simulator. To facilitate integration with external tools including PLCverif, we developed a Node.js script for running the aforementioned features as a standalone tool. This new mode also implements the ability to import a variable glossary into the requirement editor of FRET.

Variable Glossary. PLCverif extracts the list of variable names and types by parsing the PLC code. Now the resulting *variable glossary* can also be exported to a JSON file for FRET to use. This enables features such as *autocompletion* of variable names in the FRET requirement editor. It also facilitates the process of creating formalized properties that can be directly used by PLCverif for verification as these requirement variables directly match PLC code variables.

Since variable names used in PLC code may include other characters besides alphanumeric, we extended the FRET editor to support identifiers with periods, percents, or double-quoted identifiers that can contain any special character.

The supported data types differ between the two tools (e.g., PLC programs might use arrays, while FRET only has scalar types). Assigning a data type to a variable is not mandatory in FRET and in this work it is only utilized by the simulator to show what possible values a variable can be assigned. Thus implementing a best-effort mapping proved to be adequate (e.g., sending each array element as a separate variable).

Preparing FRET for PLCs. The working principle of a PLC is described by the so-called *PLC Scan Cycle*, consisting of three main steps: (1) read sensor values, (2) execute the PLC program and (3) write the actuator values. PLC requirements must be able to express cycles, e.g. "next cycle" or "at the end of the cycle".

To enable this, FRET's formalization algorithm was extended to express new built-in predicates `nextOcc(p,q)` and `prevOcc(p,q)`, and FRETish was extended with the phrases *"at the next/previous occurrence of `p`, `q`"* meaning: at the next (previous) time point where `p` holds (if there is such), `q` also holds. These are expanded into the following LTL formulae, where L (R) is the formula that specifies the left (right) endpoint of the scope interval:

- Future for nextOcc

```
($R$ | (X (((!p & !$R$) U p) => ((!p & !$R$) U (p & q)))))
```

- Past for prevOcc

```
($L$ | (Y (((!$L$ & !p) S p) => ((!$L$ & !p) S (p & q)))))
```

Based on our experience, many PLC program requirements are checked at the end of PLC cycles. This is the most critical moment since the calculated values are sent to the actuators of the system. In the FRET PLC requirements, a variable called `PLC_END` can be used to express this exact moment.

In addition, FRET allows the creation of templates to help users write common requirements. For this work, we have created new FRET templates for PLCverif (e.g., *In PLC_END* *[COMPONENT]* shall *always* *satisfy* *[RESPONSE]*).

Chapter 4

Case studies

The integration has been used in two CERN critical systems. We introduce these projects and some selected properties here. The first case study utilizes the validation capabilities, while the second employs the improved expressiveness.

4.1 Safety PLC program

The safety PLC program of the *SM18 Cluster F*, a superconducting magnet test facility at CERN, is meant to protect the personnel and the equipment of this installation.

This PLC program, written in Ladder Diagram (LD) [33], contains 31 Function_Blocks, the corresponding 31 instance Data_Blocks and 2 Functions. Regarding the number of variables, it contains 13 INT variables and 157 BOOL variables. The exported code from SIMATIC Step7 [1] (former version of Siemens TIA Portal) contains around 2800 lines of code. Figure 4.1a shows a small part of this safety program and figure 4.1b the exported code that is imported in PLCverif.

The *SM18 cluster F* is dedicated to test the new superconducting magnet technology for the High Luminosity Large Hadron Collider (HL-LHC) [34], an upgrade of the existing LHC particle accelerator. Its main risks are related to the cryogenic system and the powerful power converters up to 20.000 Amps.

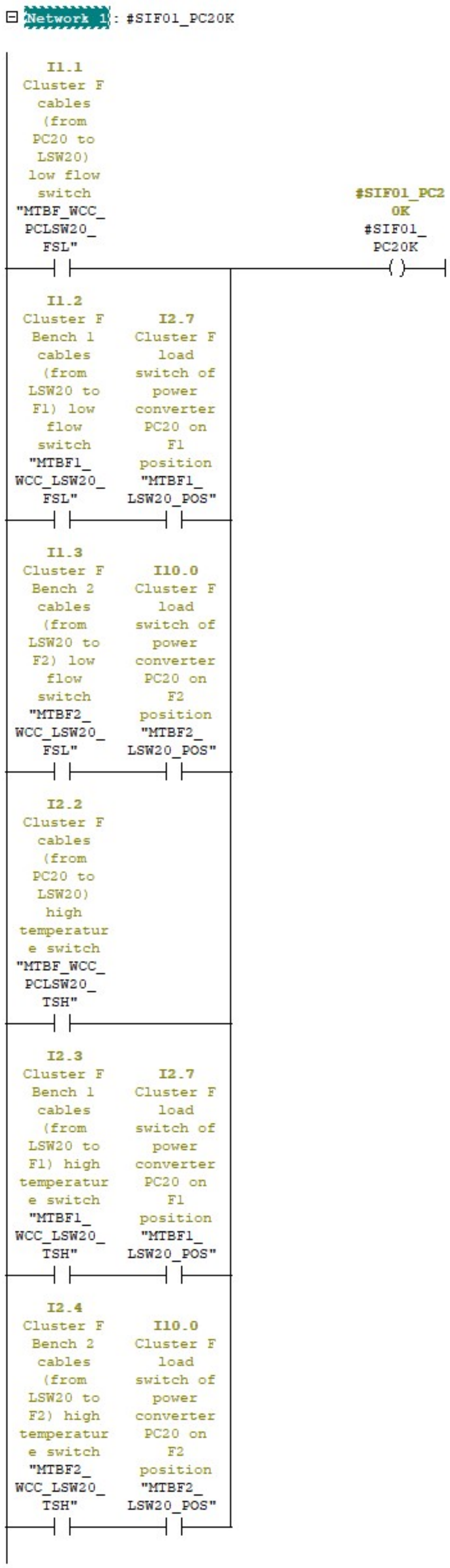
Error Property. The property of this case study corresponds to the expected logic of one of the safety functions (*SIF01_PC20K*):

if at the end of the PLC cycle (PLC_END) the flow (*_FSL) or thermo (*_TSH) switches monitoring the cooling system detect a low flow or a high temperature, and the power converter (PC20k) is connected to the magnet (*_LSW20_POS), then the safety function should shut down the power converter (SIF01_PC20K).

Figure 4.2 shows how the property is expressed in FRETish and in LTL.

Validation. Before verifying this property with PLCverif, the user should make sure that the formalized property behaves as expected. The main challenge is the number of operators and parentheses, making manual validation difficult. FRET's simulator aids by allowing the user to check any temporal valuation and whether it satisfies the property or not as shown in Figure 4.2c.

[1] https://www.siemens.com/global/en/products/automation/industry-software/automation-software/tia-portal/software/step7-tia-portal.html



(a) Part of the LD safety program.

```
FUNCTION_BLOCK "SIF01"
TITLE=
VERSION : 0.1


VAR_OUTPUT
  SIF01_PC20K : BOOL ;
  SIF01_PC15K : BOOL ;
END_VAR
BEGIN
NETWORK
TITLE =#SIF01_PC20K

      ON    "MTBF_WCC_PCLSW20_FSL";
      O     ;
      AN    "MTBF1_WCC_LSW20_FSL";
      A     "MTBF1_LSW20_POS";
      O     ;
      AN    "MTBF2_WCC_LSW20_FSL";
      A     "MTBF2_LSW20_POS";
      ON    "MTBF_WCC_PCLSW20_TSH";
      O     ;
      AN    "MTBF1_WCC_LSW20_TSH";
      A     "MTBF1_LSW20_POS";
      O     ;
      AN    "MTBF2_WCC_LSW20_TSH";
      A     "MTBF2_LSW20_POS";
      =     #SIF01_PC20K;
NETWORK
TITLE =#SIF01_PC15K

      ON    "MTBF_WCC_PCINV15_FSL";
      O     ;
      AN    "MTBF2_WCC_LSW15_FSL";
      A     "MTBF_PC15F_RELAY_ST";
      ON    "MTBF_WCC_PCINV15_TSH";
      O     ;
      AN    "MTBF2_WCC_LSW15_TSH";
      A     "MTBF_PC15F_RELAY_ST";
      O     ;
      A     "MTBF_LSW15_POS_E2";
      A     "MTBF_PC15F_RELAY_ST";
      =     #SIF01_PC15K;
END_FUNCTION_BLOCK
```

(b) Exported safety program in STL language.

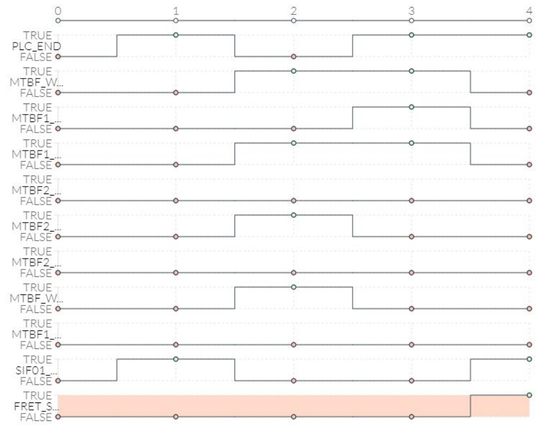
Figure 4.1: Safety program from the case study 1.

```
F_MAIN shall always satisfy if (PLC_END & (!MTBF_WCC_PCLSW20_FSL | !MTBF_WCC_PCLSW20_TSH |
     (MTBF1_LSW20_POS & (!MTBF1_WCC_LSW20_FSL | !MTBF1_WCC_LSW20_TSH)) | (MTBF2_LSW20_POS &
     (!MTBF2_WCC_LSW20_FSL | !MTBF2_WCC_LSW20_TSH)))) then SIF01_DB.SIF01_PC20K
```

(a) Property of SIF01_PC20K in FRETISH.

```
G ((PLC_END and ((((!
  MTBF_WCC_PCLSW20_FSL) or
  (! MTBF_WCC_PCLSW20_TSH))
  or (MTBF1_LSW20_POS and
  ((! MTBF1_WCC_LSW20_FSL)
  or (! MTBF1_WCC_LSW20_TSH)
  ))) or (MTBF2_LSW20_POS and
  ((!MTBF2_WCC_LSW20_FSL) or (!
  MTBF2_WCC_LSW20_TSH)))))
  -> SIF01_DB.SIF01_PC20K)
```

(b) Generated LTL property by FRET.



(c) Future LTL simulation

Figure 4.2: Property of the SIF01_PC20K safety function.

4.2 Standard PLC program

This case study is concerned with UNICOS [35], a CERN framework for the development of hundreds of industrial control systems. The selected program library is called the *OnOff* object. Its purpose is to control physical equipment driven by digital signals, which can be composed of different types of devices. This makes its PLC program highly configurable and its associated logic complex.

This PLC program is written in SCL (Structured Control Language), the Siemens PLC language equivalent to ST (Structured Text) from the IEC 61131 standard [33]. This program contains 1 main Function_Block, its corresponding instance Data_Block, 4 Functions, and 1 global Data_Block. It also contains 1 TON (Timer On Delay) and 2 TP (Pulse Timer) instances. Regarding the number of variables, it contains 9 WORD variables, 11 INT variables, 36 REAL variables, 8 TIME variables, 1 DINT variable, 6 BYTE variables, and 141 BOOL variables. The program has been written using the Siemens TIA Portal programming environment [2] and it contains around 1080 lines of code. Fig 4.3 shows a small part of this standard program.

[2]https://www.siemens.com/global/en/products/automation/industry-software/automation-software/tia-portal.html

```
(* MODE MANAGER *)

IF NOT (#HLD AND #PHLD) THEN

(* Forced Mode *)
    IF (#AuMoSt_aux OR #MMoSt_aux OR #SoftLDSt_aux) AND
        #E_MFoMoR AND NOT(#AuIhFoMo) THEN

        #AuMoSt_aux   := FALSE;
        #MMoSt_aux    := FALSE;
        #FoMoSt_aux   := TRUE;
        #SoftLDSt_aux := FALSE;

(* Software Local Mode *)
    ELSIF (#AuMoSt_aux OR #MMoSt_aux) AND #E_MSoftLDR AND NOT #AuIhFoMo THEN

        #AuMoSt_aux  := FALSE;
        #MMoSt_aux   := FALSE;
        #FoMoSt_aux  := FALSE;
        #SoftLDSt_aux:= TRUE;

(* Manual Mode *)
    ELSIF (#AuMoSt_aux OR #FoMoSt_aux OR #SoftLDSt_aux) AND
           #E_MMMoR AND NOT(#AuIhMMo) THEN

        #AuMoSt_aux   := FALSE;
        #MMoSt_aux    := TRUE;
        #FoMoSt_aux   := FALSE;
        #SoftLDSt_aux := FALSE;

(* Auto Mode *)
    ELSIF (#MMoSt_aux AND (#E_MAuMoR OR #E_AuAuMoR )) OR
          (#FoMoSt_aux AND #E_MAuMoR) OR
          (#SoftLDSt_aux AND #E_MAuMoR) OR
          (#MMoSt_aux AND #AuIhMMo) OR
          (#FoMoSt_aux AND #AuIhFoMo)OR
          (#SoftLDSt_aux AND #AuIhFoMo) OR
           NOT(#AuMoSt_aux OR #MMoSt_aux OR #FoMoSt_aux OR #SoftLDSt_aux) THEN

        #AuMoSt_aux   := TRUE;
        #MMoSt_aux    := FALSE;
        #FoMoSt_aux   := FALSE;
        #SoftLDSt_aux := FALSE;
    END_IF;

    (* Status setting *)
    #LDSt     := FALSE;
    #AuMoSt   := #AuMoSt_aux;
    #MMoSt    := #MMoSt_aux;
    #FoMoSt   := #FoMoSt_aux;
    #SoftLDSt := #SoftLDSt_aux;
 ELSE
    (* Local Drive Mode *)
    #AuMoSt  := FALSE;
    #MMoSt   := FALSE;
    #FoMoSt  := FALSE;
    #LDSt    := TRUE;
        #SoftLDSt:= FALSE;
 END_IF;
```

Figure 4.3: Small piece of the SCL program of case study 2.

Error Property. The property presented here is related to the transitions between two operation modes shown in Figure 4.4: (1) *Auto mode*, where the *OnOff* object is driven by the control logic of a higher object of the hierarchy of the program, and (2) *Manual mode*, where the operator drives the object.

The property extracted from the specification is: When the OnOff object is in Manual mode (MMoSt) and the control logic requests to move to Auto mode (AuAuMoR) at any point in the PLC cycle, the OnOff object should move to the Auto mode (AuMoSt). Figure 4.5 shows the property in FRETISH and the LTL formula.

Thanks to the new *"at the next occurrence of"* phrase, we can verify that this property is satisfied at the end of the current cycle (which is more precise and strict), as shown in

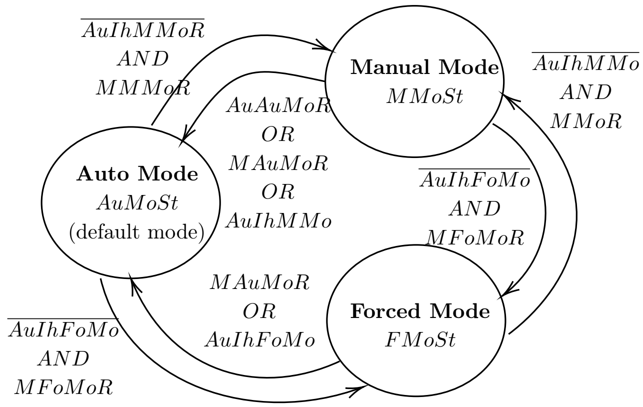


Figure 4.4: OnOff operation modes specification.

```
When (MMoSt & AuAuMoR) the
   CPC_FB_OnOff shall eventually
   satisfy AuMoSt & PLC_END
```

(a) Property expressed in FRETish.

```
(G (((!(MMoSt and AuAuMoR)) and (X (MMoSt
  and AuAuMoR))) -> (X(F(AuMoSt and
  PLC_END))))) and ((MMoSt and
  AuAuMoR) -> (F(AuMoSt and PLC_END)))
```

(b) Generated LTL property by FRET

Figure 4.5: PLCverif property for the *OnOff* object.

```
the CPC_FB_OnOff shall always satisfy
   if (MMoSt & AuAuMoR & !PLC_END)
   then at the next occurrence of
   PLC_END, AuMoSt
```

(a) Property expressed in FRETish.

```
G (((MMoSt and AuAuMoR) and (! PLC_END)) ->
  (X ((((! PLC_END) ) U PLC_END) ->
  (((! PLC_END)) U (PLC_END and AuMoSt)))))
```

(b) Generated LTL property by FRET

Figure 4.6: PLCverif property for the *OnOff* object using the `nextOcc` predicate

Figure 4.6.

These properties can not be expressed with the current PLCverif patterns, but they are expressible with the restricted natural language of FRET. Now PLCverif users can express a large variety of requirements in a natural language and validate these in the simulator.

Chapter 5

A Closer Look at FRET and PLCverif

In this chapter, we show the workflow of our tool chain in practice. Figure 5.1 represents the high-level workflow of the tools: PLCverif lets the user freely edit the PLC code and the configuration. The configuration includes the requirement, which now can be formulated in FRET. The user can open up FRET from PLCverif and edit the requirement there as many times as they want, utilizing all the earlier described functionalities of FRET. When the user is satisfied with the configurations, the verification can be executed with a click of a button.

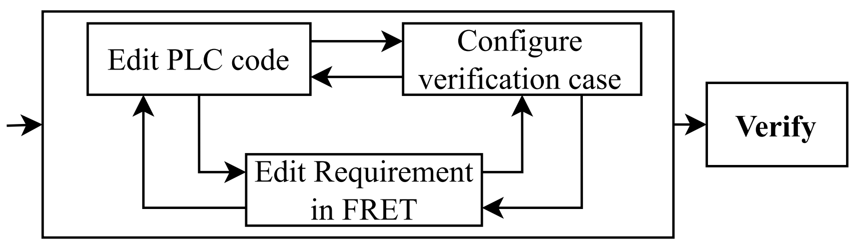


Figure 5.1: PLCverif lets the user freely edit the PLC code and the verification configuration, including the requirement.

5.1 Starting out in PLCverif

The screenshots shown in this section are taken from the OnOff case study and show the functionality of the graphical user interface of PLCverif.

The main window includes the PLC code editor, which is shown in Figure 5.2. In this example, the relevant code of the OnOff project for the first property (see Figure 4.2) of the case study is shown in this editor. The project structure is displayed on the side, in which all the necessary files for this project appear.

The verification cases, such as the one shown in Figure 5.3, also appear in the project structure with the extension *.vc3*. The configuration options of the verification case file include for example the verification backend, metadata and also the requirement.

With the presented integration with FRET the user is now able to select the option *Edit in FRET* while formalizing a new requirement. Once this option is selected, FRET pops up and the window from Figure 5.5 appears. After the user is done editing the requirement, they save it, FRET closes and the requirement written in FRETISH and its corresponding temporal logic (TL) formula appear in PLCverif.

At this point, the user is able to click on *Verify!* in order to launch the verification case. They can also still modify any of the so far mentioned options or open up FRET again if they would like to modify the requirement.

Once PLCverif is done running the verification case, it reports the result of it as shown in Figure 5.4. In this case, since the property is not satisfied, PLCverif returns a counterexample. This means that if the input variables of the OnOff object are set to the values from this counterexample, the property is violated.

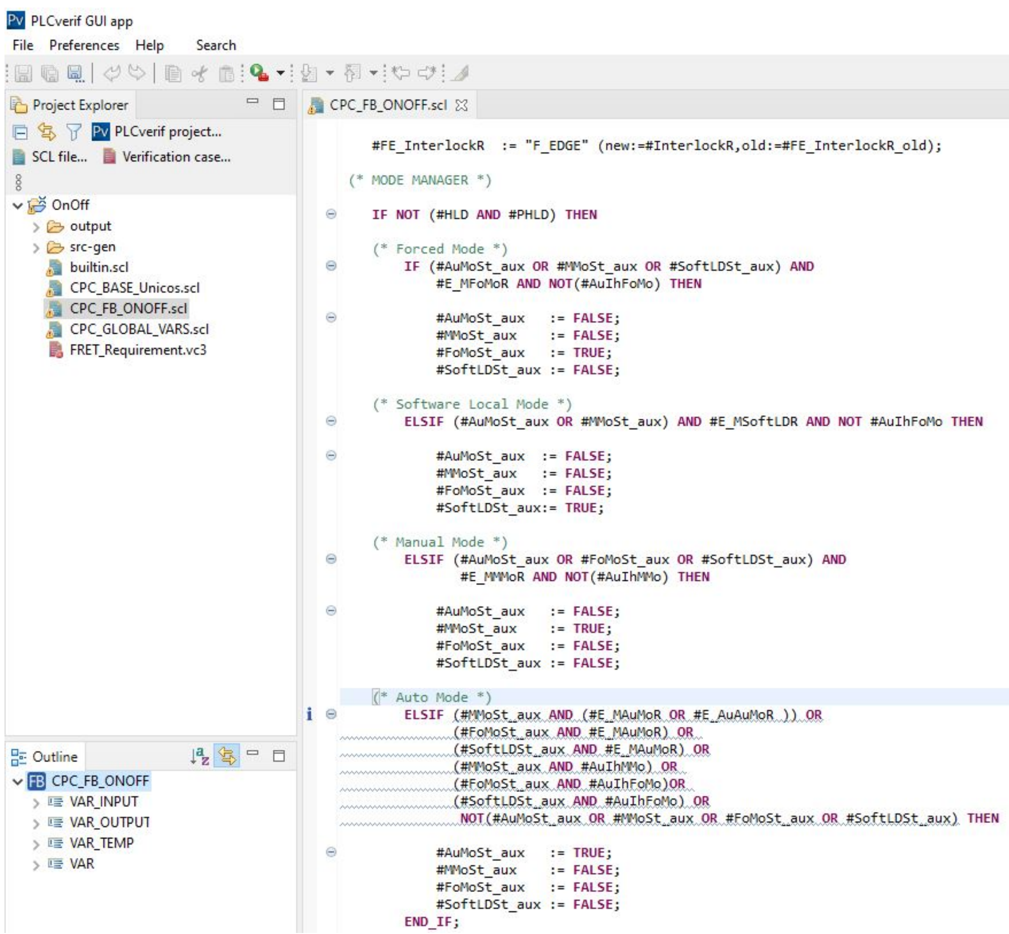


Figure 5.2: PLCverif *GUI*. It shows the relevant PLC code from the OnOff case study. The project structure details the different files that composes this project, as well as the verification cases (*.vc3*).

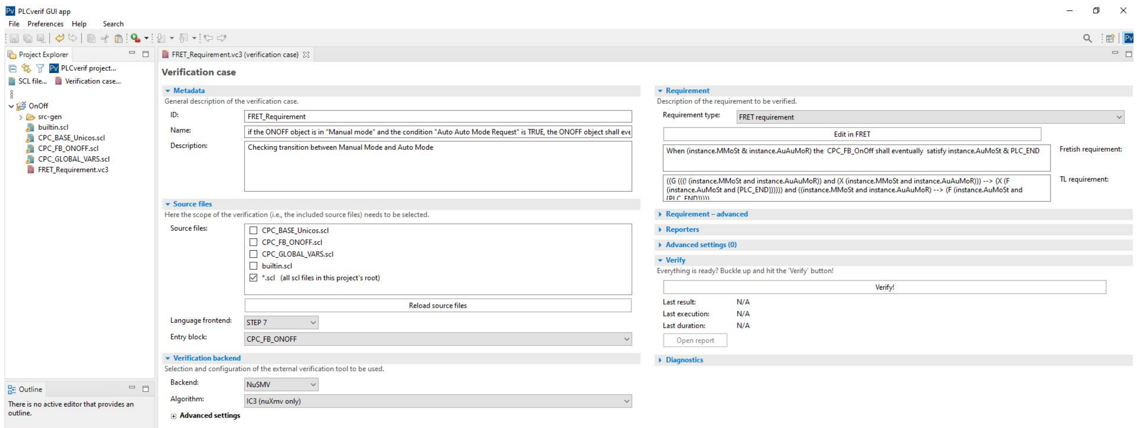


Figure 5.3: PLCverif *verification case* editor. The user can now select *Edit in FRET* in order to formalize the requirement. In this case, FRET is launched and the window from 5.5 appears. Once this new window is closed, the generated specification in FRETish and in temporal logic (TL) appears in PLCverif. The user can then verify the property.

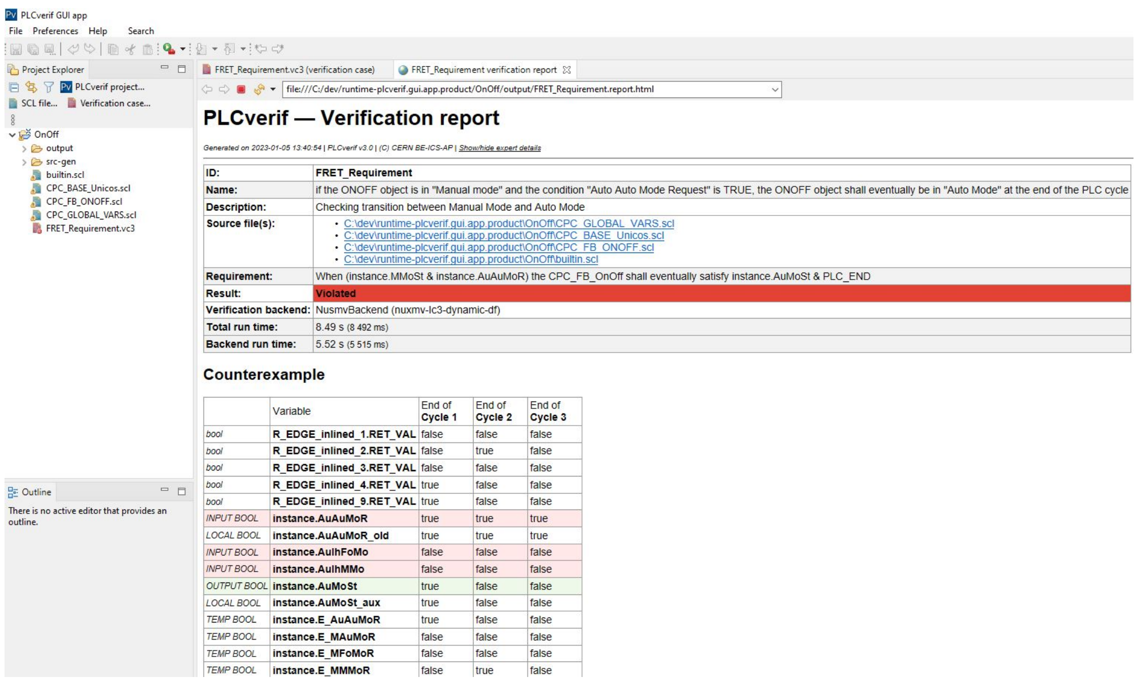


Figure 5.4: PLCverif *verification report*. Since the property is violated, i.e., the PLC code from the OnOff object does not satisfy the property, PLCverif returns a counterexample. If the input variables of the OnOff object are set to the values from this counterexample, the property is violated.

5.2 Editing the Requirement in FRET

Similarly to the last section, the following screenshots represent different steps of creating the requirement with FRET for the first property of the OnOff case study. Formulating, editing and validating a requirement in FRET has its own workflow by itself, which is introduced in this section.

Frst, Figure 5.5 shows the FRET *Update Requirement* dialog in which the user writes in FRETISH the property to be verified. The dialog is split into two parts - the editor on the left and the *Assistant*, *Templates*, *Glossary* tabs on the right.

On the left part, free text can be optionally entered in Rationale and Comments. Next, a FRETISH requirement can be written using the six sequential fields: scope, condition, component, shall, timing, and response. As the requirement is typed in, the FRET editor dynamically colors the text corresponding to the fields. Parser feedback appears in red at the bottom.

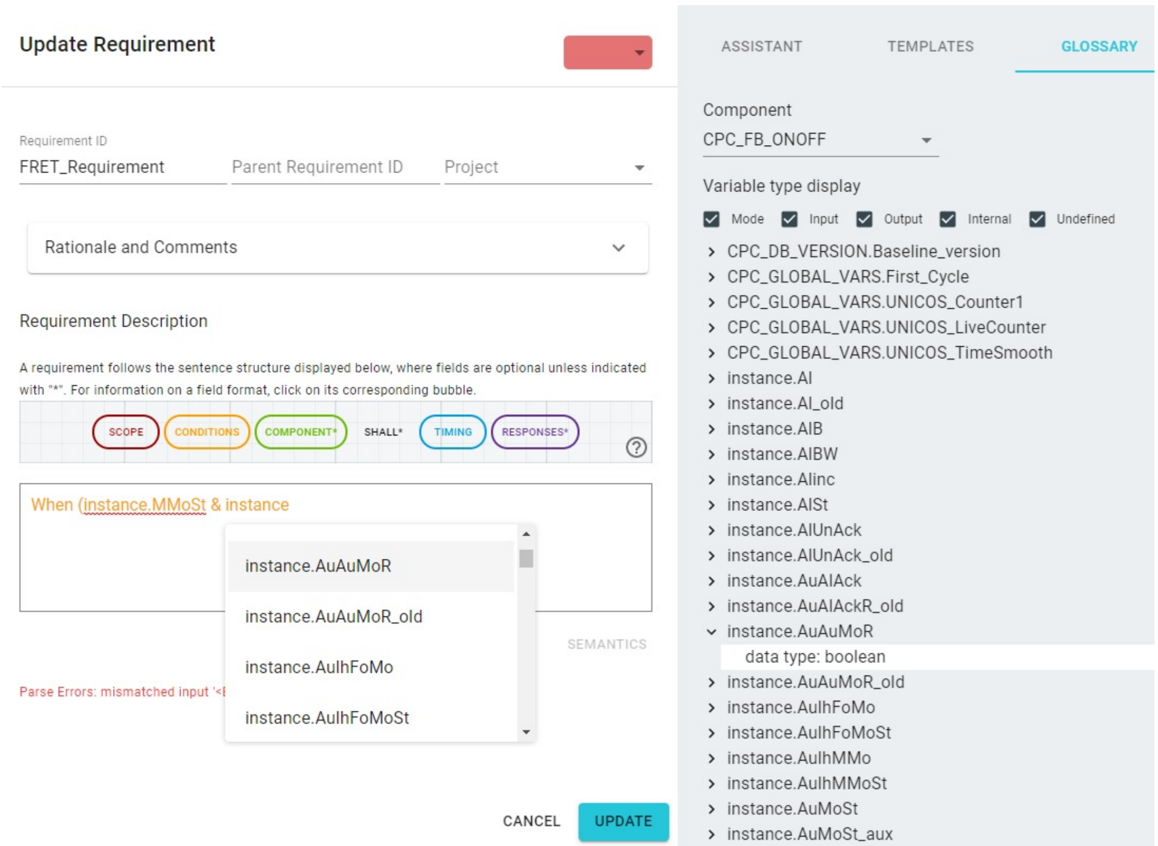


Figure 5.5: FRET *Update Requirement* editor after launching it from PLCverif. All the variables from the PLC program are available in FRET. The user can easily write the requirements by making use of the autocomplete functionality.

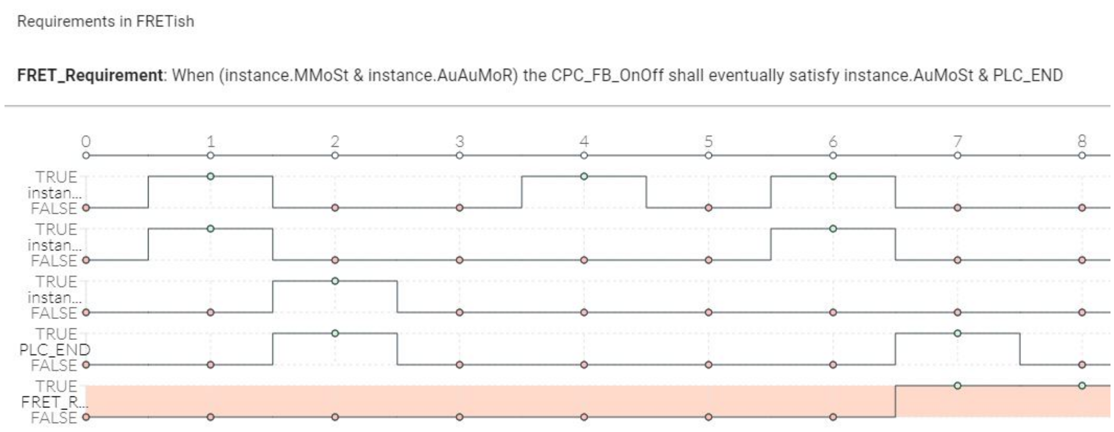


Figure 5.6: FRET simulator. After writing the requirement, the user can test its right behavior by simulating different cases.

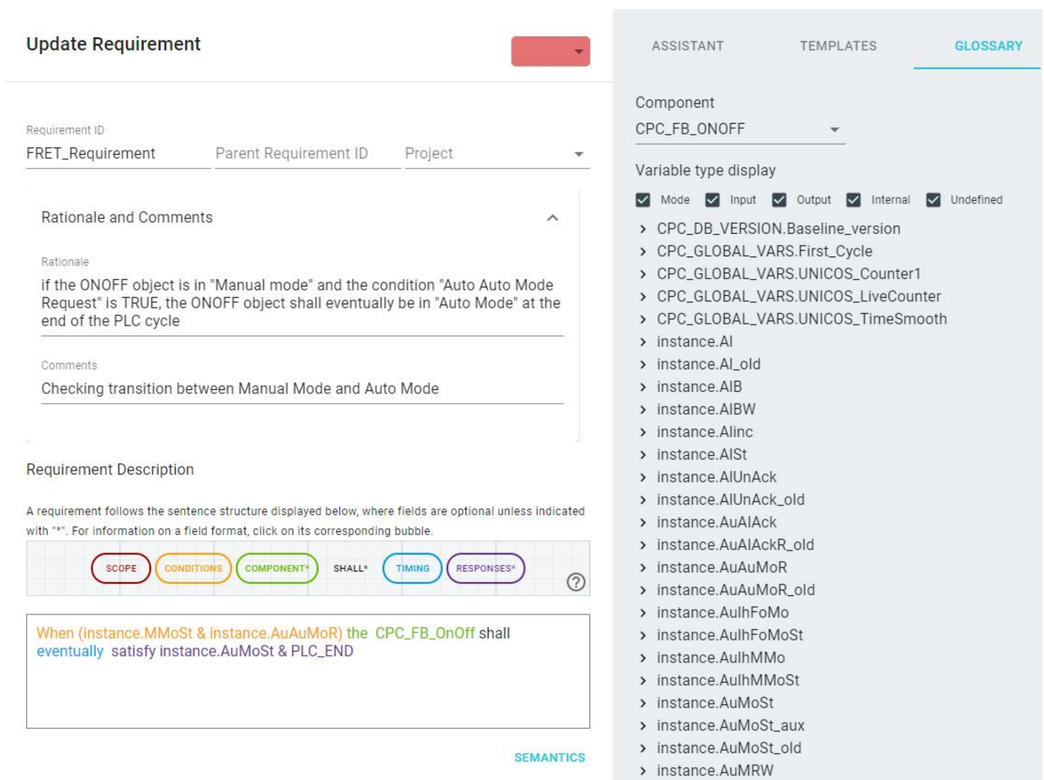


Figure 5.7: FRET *Update Requirement* editor when modifying an existing requirement. The user can modify an existing requirement. Everything that was created is now also available.

On the right side, in the *Glossary* tab, we can see the variable glossary imported from PLCverif. These variables can be autocompleted in the requirement editor (as shown in Figure 5.5). Once the user is done writing the requirement, they can test different cases using the FRET simulator (Figure 5.6). Given a FRETish requirement, the visualizer shows temporal traces of each of the variables involved, as well as the valuation of the requirement for each point in time. The user is able to change the values of signals and observe the consequences on the resulting valuation, i.e., the requirement is satisfied or violated.

After closing FRET, the property is exported to PLCverif. Afterwards, if the user wants to modify an existing FRET requirement, they can open FRET from PLCverif again and this time the *Update Requirement* editor will open as shown in Figure 5.7.

Chapter 6

Conclusion

The creation of requirements in FRET fits well into the verification workflow and improves both usability and expressiveness, as shown by the case studies. PLCverif [4] and FRET [12] are both open source and available in their respective repositories.

Plans for improvements include the support of verification of time properties in PLCverif and the support for different type widths in the FRET simulator (*e.g. 16/32 bit integers*).

To the best of our knowledge, this is the first attempt to specify formal requirements using a structured natural language for PLC program verification.

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14. ABSTRACT
PLCverif is an actively developed project at CERN, enabling the formal verification of Programmable Logic Controller (PLC) programs in critical systems. In this paper, we present our work on improving the formal requirements specification experience in PLCverif through the use of natural language. To this end, we integrate NASA's FRET, a formal requirement elicitation and authoring tool, into PLCverif. FRET is used to specify formal requirements in structured natural language, which automatically translates into temporal logic formulae. FRET's output is then directly used by PLCverif for verification purposes. We discuss practical challenges that PLCverif users face when authoring requirements and the FRET features that help alleviate these problems. We present the new requirement formalization workflow and report our experience using it on two critical CERN case studies.

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