Bias Spectroscopy of Negative Differential Resistance in Ge Nanowire Cascode Circuits

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***Abstract*—In this paper, we exploit the nanometer scale properties of Ge based Schottky barrier field-effect transistors (SBFETs) with monocrystalline Al contacts, fusing the concept of reconfiguration and negative differential resistance (NDR) in a single device. Temperature dependent bias spectroscopy is used to investigate the electronic transport in the NDR regime leading to profound understanding of the involved physical transport mechanisms. Importantly, the obtained SBFETs are capable of shifting the NDR-peak by electrostatic gating. Thus, a cascode of such devices results in overlapping NDR regions, which allows the realization of new circuit topologies beyond the capabilities of conventional CMOS.**

***Index Terms*—Germanium, Metal-Semiconductor Heterostructure, Reconfigurable Transistor, Negative Differential Resistance**

I. Introduction

Modern computing is demanding ever more complex integrated circuits. Two emerging concepts that integrate a higher expressiveness per elementary unit, thereby reducing overall transistor count and power consumption versus conventional technology, are reconfigurable field-effect transistors (RFETs) and multi-valued logic (MVL) devices. RFETs are capable of dynamically altering the device operation between n- and p-type even during run-time, while MVL devices are able to calculate with higher bases than two. In this respect, complex logic functions can be designed, such as adders with a significantly lower circuit propagation delay and reduced number of transistors [1]. Importantly, constructing overlapping negative differential resistance (NDR) regions by a series circuit of NDR devices, monostable-bistable transition logic elements (MOBILE), enabling both NAND and NOR operations can be realized [2]. Different to prior art NDR devices, which have been restricted to either being not CMOS compatible, as in MBE grown resonant tunneling diodes, or limited to cryogenic operation temperatures, as in Ge Gunn devices [3], the properties of nanowire (NW) heterostructures featuring abrupt, flat and single-crystal Al-Ge junctions [4] allow room temperature NDR operation. Towards the realization of beyond CMOS electronics with functional diversification, the NDR effect is fused with RFETs in a single Ge NW multi-gated transistor.

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II. Device architecture

In this work, we have integrated vapor liquid solid (VLS) grown and nominally undoped Ge NWs with a predominant crystal orientation of $\langle 111 \rangle$ in Schottky barrier field-effect transistors (SBFETs) and RFETs with three top-gate electrodes allowing n- and p-type polarity control with NDR accessibility via the electron transfer effect at room-temperature [5]. The key enabler for this concept is the electronic structure of quasi-1D monolithic Al-Ge-Al NW heterostructures, obtained from a thermally induced longitudinal Al-Ge exchange reaction [6]. Thereof, it is possible to monolithically embed Ge NW channels with crystalline and single-elementary Al contacts, enabling reliable and reproducible metal-semiconductor junctions with well defined properties. SBFET fabrication was done by integrating ALD-grown Al_2O_3 with a thickness of $22\,\mathrm{nm}$ as gate oxide and patterning a source-drain overlapping Ω-shaped top-gate electrode, as shown in Fig.1. The same fabrication method has been applied for the three-gate architecture (cf. Fig.5). The abrupt Al-Ge junction is shown in the high angle annular dark field (HAADF) scanning TEM provided in the inset.

III. Negative Differential Resistance

Operating a SBFET in predominant electron injection, i.e. at top-gate voltages $V_{TG} > 0\,\mathrm{V}$ an unambiguous gate-tunable NDR and the onset of impact ionization (II) is observed in

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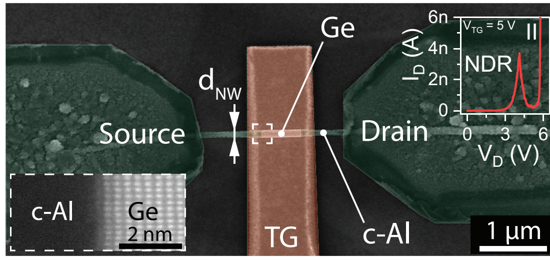

Fig. 1. False color SEM image of a Ge NDR SBFET with a diameter of d_{NW} = 75 nm. The inset shows a high-resolution HAADF TEM image revealing the atomically abrupt Al-Ge junction. A typical output characteristic showing NDR and the onset of II is shown in the right inset.

the output characteristics (cf. right inset of Fig.1). To map and analyze the SBFET NDR region, bias spectroscopy based on a series of I/V measurements at different V_{TG} in 0.5 V steps has been applied in Fig.2a, which shows a graphic representation of the NDR peak and valley region dependent on V_D and V_{TG}. Remarkably, these two regions spread over V_{TG} = 4.75 V to 7 V with a progressive enhancement increasing V_{TG} due to internal field modulation. The inset shows a sketch of the conduction band structure and the hot-electron induced transferred electron effect from the L- to the X-valley initiating the NDR effect at high electric fields [6]. Above a specific threshold electric field (V_D), the NDR region is followed by a steep current increase indicating the onset of II. An important figure of merit of NDR devices is the peak-to-valley ratio (PVR), which is defined by $I(V_{Peak})/I(V_{Valley})$. In the presented device architecture a mean PVR of 10 was extracted with peak current densities of 13.2×10^3 A/cm^2 at V_{TG} = 6 V. Importantly, a large and stable PVR is highly relevant for logic applications. To accurately map the region of negative differential conductance (NDC), the derivative dI_D/dV_D was calculated and displayed as a color map in Fig.2b. Results show NDR peak modulation with a linear I_D peak shift with a slope of $2V_{TG}/V_D$, retaining a fairly constant peak width. As V_{TG} increases, the NDR valley is broadened and the II region is shifted out because the gate drain potential difference is lowered.

Temperature dependent bias spectroscopy in the regime between T = 225 K to 400 K was used to investigate the key parameters of the NDR effect (cf. Fig.3). Prominently, a stable and reproducible NDR up to a temperature of T = 350 K with a PVR of 2.1 was observed, which is an important prerequisite for the realization of logic applications and further proves the capabilities of the proposed device concept. At room-temperature, the PVR of the Ge based SBFET device is a factor of 6.5 larger than state of the art Si/SiGe resonant tunneling diodes and a factor of 3.5 larger in comparison to AlAs/GaAs based NDR devices [7]. Based on the actual log_{10}I/V at T = 225 K (cf. right y-axis in Fig.3a), three different slopes can be identified: L-valley transport is attributed to S1, which can be related to thermionic field emission at the source junction contrasting a MOSFET. Slope S2 shows the NDR due to the electron transfer from the L- to

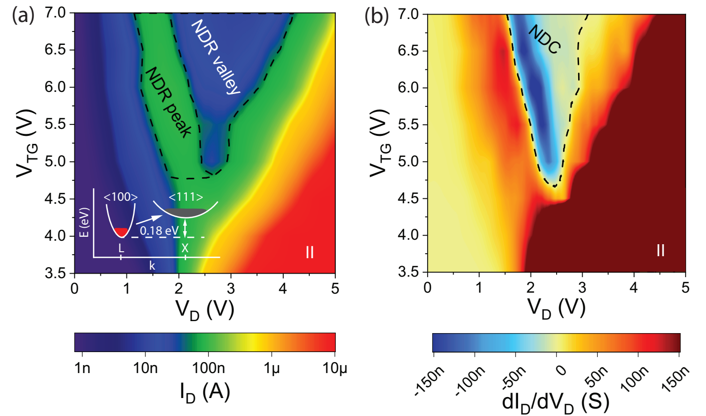

Fig. 2. (a) Bias spectroscopy showing the gate-tunable NDR characteristic of a Ge SBFET. The inset shows a schematic of the Ge band structure and the mechanism leading to NDR. (b) NDC color map derived from the bias spectroscopy data shown in (a).

the X-valley of the conduction band constituting a significant effective mobility decrease resulting in NDR. The steeper slope S3 marks the onset of II by an avalanche-like increase of electrons at high electric fields. Further, Fig.3b shows a map of the NDC region. Thereof, a thermally induced shift, caused by thermal activation, of the NDR/NDC region to lower V_D values was observed.

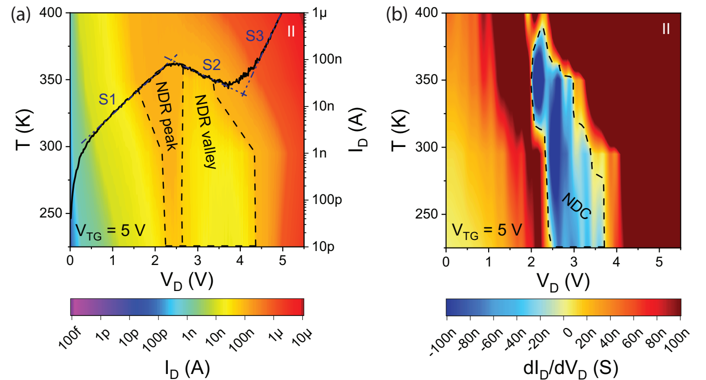

Fig. 3. (a) Bias spectroscopy of the NDR characteristic over temperature of a Ge SBFET. For reference, the right y-axis shows the log_{10}I/V at T = 225 K. (b) Thereof calculated NDC temperature dependent color map.

Demonstrating the modulation of the NDR peak, a cascode circuit of SBFET NDR devices was analyzed as shown in the inset of Fig.4a. In this configuration the low-side SBFET (T2; V_{TGL}) is always in electron-conduction mode (V_{TGL} = 5 V) enabling NDR, whereas the high-side SBFET (T1; V_{TGH}) is used as a resistive element, allowing to shift the NDR. As seen in Fig.4a, for V_{TGH} voltages from -2 V to 1.25 V, a stable NDR region with respect to V_D is obtained. This is related to the fact that T1 does not exhibit NDR, but acts like a low resistive load due to the transistor being in hole conduction mode (cf. Fig.6). Thus, V_D mostly drops over T2. However, as V_{TGH} becomes more positive, T1 is progressively steered into electron mode and the voltage over T1 is becoming

more equally distributed among T1 and T2. This enables a modulation of the NDR peak for applying V_{TGH} from 1.25 V to 2.5 V. The respective NDC color map of the measured data is shown in Fig.4b.

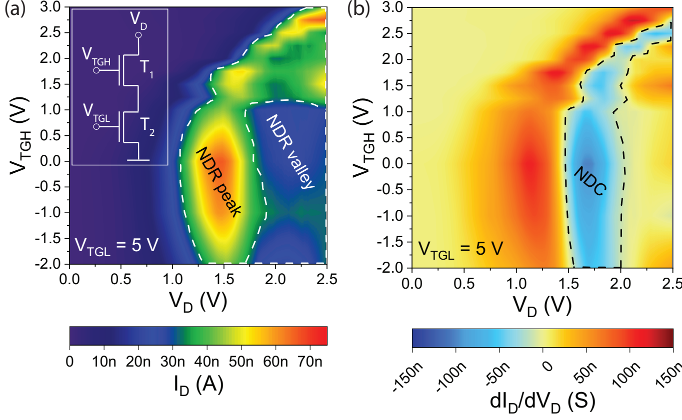

Fig. 4. (a) Bias spectroscopy of a cascode circuit of SBFET NDR devices providing an electrostatically tunable NDR region. For presentation clarity (b) shows the respective NDC color map.

IV. Polarity Control

To enable effective polarity control of the proposed SBFET NDR devices, a RFET design with three-gated regions was chosen, as shown in Fig.5. Thereto, two independent gates, the program gates (PGs) and the control gate (CG) are placed on both Al-Ge junctions and the Ge channel respectively.

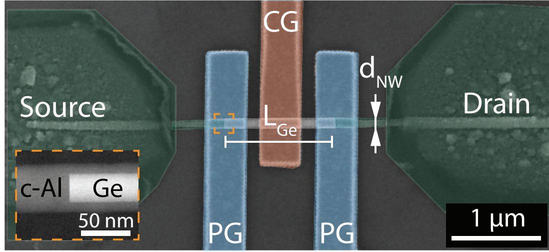

Fig. 5. False color SEM image of a Ge NDR-mode RFET with a diameter of d_{NW} = 30 nm. The inset shows a HAADF TEM image of the monolithic and single-crystalline Al-Ge junction below the PGs.

As shown in Fig.6, the proposed RFET architecture allows to switch between a n- and p-type characteristic by charge carrier polarity control provided by the PGs, while the CG is modulating the charge carrier concentration in the channel. Consequently, the ambipolar nature of Ge based SBFETs can be transposed into an unipolar n- and p-type operation and allows for efficient suppression of source-drain leakage through a blocking barrier at the drain junction limiting static power consumption despite the low bandgap of Ge. For didactic purposes, the insets of Fig.6 schematically depict the band diagrams of the gating mechanism. Despite of being able to achieve unipolar operation modes, the low effective Schottky barrier height of holes compared to electrons in Al-Ge junction based devices [8] results in strongly asymmetric on-currents for the two operation modes. This constitutes a common problem of Ge based RFETs [9], as all technologically relevant metal-Ge junctions show strong Fermi level pinning close to the valence band, resulting in predominant hole conduction [10].

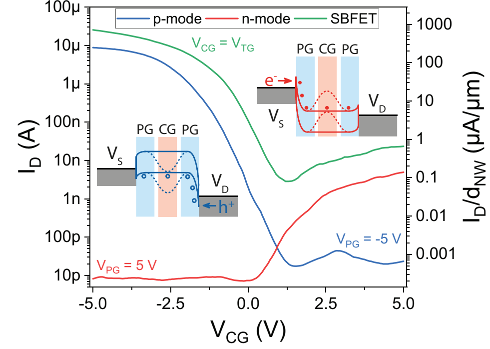

Fig. 6. Transfer characteristic of the Ge NDR-mode RFET in n- and p-type program mode for applying a bias voltage of V_D = 1 V. For comparison the transfer characteristic of a top-gated SBFET with L_{Ge} = 1.1 µm is shown (cf. Fig.1). The insets depict schematic band diagrams of the gating mechanism, resulting in unipolar electron and hole transport.

V. NDR-mode RFET

To investigate the influence of electrostatic gating on the NDR in RFET configuration, V_{CG} is kept at 5 V to inject electrons into the Ge channel and a V_{PG} sweep is executed (see Fig.7a). Since NDR in Ge is enabled by the energetic conduction band landscape, it is only observed for a positive V_{PG}. There, efficient electron injection takes place through tunneling as the barrier thickness is reduced through band bending. Starting with $V_{PG} \approx 3.5$ V injected electrons are accelerated across the channel providing L- to X-valley scattering, yielding stable and reproducible NDR, which is also visible in the derivation plot (cf. Fig.7b).

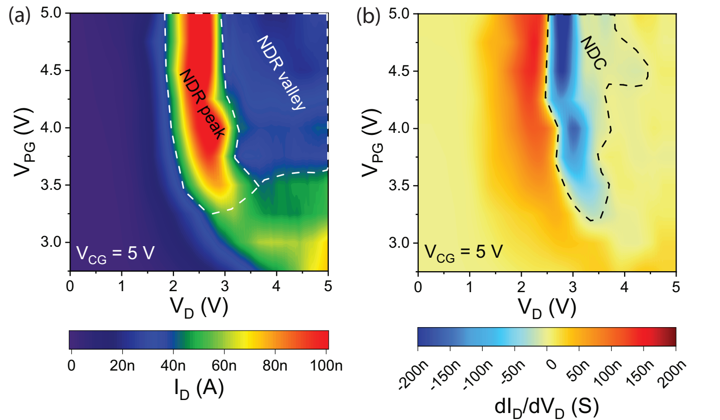

Fig. 7. (a) PG dependent bias spectroscopy of the Ge NDR-mode RFET showing a distinct NDR region between $V_{PG} \approx 3.5$ V to 5 V. The respective NDC color map is shown in (b).

Next, V_{PG} is kept at 5 V and V_{CG} is swept. In this case a sufficient injection of electrons through the Al-Ge junction is

provided, while the electron concentration in the Ge channel is modulated. The respective CG-dependent color map and the thereof calculated NDC map is shown in Fig.8. In this configuration, independent gating enables a room-temperature gate-tunable NDR, providing distinct programmable NDR even during run-time, where the NDR peak can be effectively shifted by $\approx 2\,\mathrm{V}$ applying V_{CG} between $3\,\mathrm{V}$ to $5\,\mathrm{V}$ with a room-temperature PVR of 10. Importantly, the three-gate NDR-mode RFET architecture constitutes an integrated version of the cascode circuit of SBFET NDR devices showing an even better capability to modulate the NDR region.

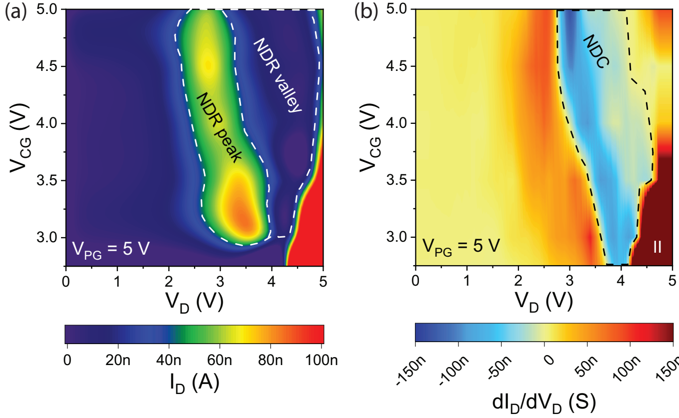

Fig. 8. (a) CG dependent bias spectroscopy of the Ge NDR-mode RFET showing the capability to modulate the position of the NDR peak with the voltage applied to the CG. (b) Thereof calculated NDC color map.

The ability to modulate the NDR peak with the CG potential can be exploited in a cascode circuit (cf. Fig.9a) of NDR-mode RFETs, where the CGs act as inputs resulting in an I/V characteristic with several overlapping NDR regions, potentially interesting for MOBILE devices, enabling reconfigurable NAND/NOR operations [11]. Importantly, the CG of T1 can be set accordingly, using the transistor either as a resistive load or as NDR device, T2 is hardwired to operate in NDR mode ($V_{PG} = V_{CG} = 5\,\mathrm{V}$). Consequently, for CG-voltages up to $1\,\mathrm{V}$, due to an increased resistive load, the NDR peak can be shifted with respect to V_D, while higher V_{CG} voltages result in two overlapping NDR regions, due to both T1 and T2 working in the NDR mode. To highlight the second NDR region, Fig.9b shows the NDC of the respective I/V data. Finally it can be stated, that we expect operation voltages to be reduced, by scaling down the channel length and effective gate oxide thickness. In this context, NDR was demonstrated in devices with channel lengths down to $150\,\mathrm{nm}$ and an applied bias of $V_D = 2\,\mathrm{V}$ [6].

VI. Conclusion

In conclusion, we have investigated the electrostatic gating capability of NDR in Ge based SBFETs by means of temperature dependent bias spectroscopy. Embedded into a RFET architecture, Ge based reconfigurable electronics can be fused with an electrostatic tunable NDR. Gate-dependent NDR measurements revealed the capability of modulating the

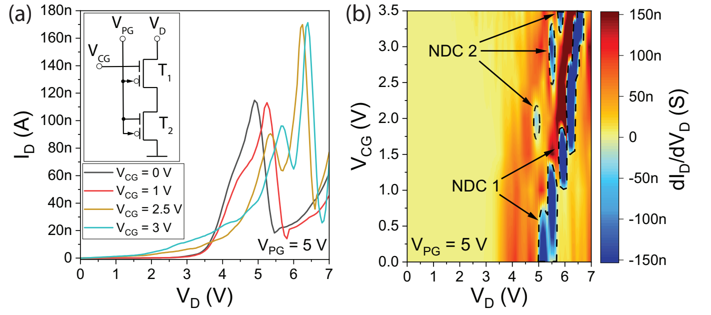

Fig. 9. (a) Cascode circuit of two Ge NDR-mode RFETs to shift the NDR region and construct a double NDR. While the NDR of T1 is being tuned by V_{CG} to switch between quasi-ohmic and NDR behavior, T2 due to its PGs and CG being hardwired to $5\,\mathrm{V}$, it constantly operates in NDR-mode. (b) Respective color map showing two distinct NDC regions.

PVR with the PG voltage, while the CG voltage can be used to effectively shift the NDR peak. Thus, arranged in a cascode circuit, an I/V characteristic comprising overlapping NDR regions is obtained. Although scalability still needs to be explored and VLS grown NWs are used as demonstration vehicle, compared to state of the art NDR devices, the NDR-mode RFET concept constitutes a small footprint and CMOS-compatible platform for potentially implementing logic functions combining CMOS with NDR.

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