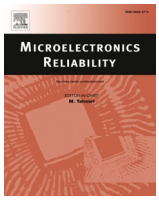
Microelectronics Reliability 150 (2023) 115098

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel



In-situ delamination detection in multi-layered semiconductor packages

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ARTICLE INFO

Keywords:
Non-destructive testing
Solder fatigue
Delamination
Accelerated reliability testing

ABSTRACT

Accurately determining the material properties of large-area solder joints is crucial for developing precise lifetime models in modern power electronic devices, as these joints play a vital role in providing both electrical and mechanical connections between components. This study presents a novel, non-destructive, and in-situ technique based on laser Doppler vibrometry for detecting crack initiation and monitoring crack growth in semiconductor structures. This method was successfully applied to determine various stages of die attach degradation during accelerated mechanical cyclic tests of large area solder joints, and was verified by scanning acoustic microscopy (SAM) measurements as well as optical methods. Furthermore, analysis of the acoustic emission (AE) signal was conducted as an alternative method for monitoring crack propagation. Optical and electron microscopy were employed to analyse crack initiation, crack paths, and crack surface morphologies. The in-situ delamination detection technique can provide essential information for robust lifetime prediction modelling of material systems in advanced semiconductor components.

1. Introduction

The increasing demand for high-power semiconductor devices, particularly the recent focus on the renewable energy sector and e-mobility, has led to the development of modules with higher power density, operating frequency, and integration [1]. During manufacturing and especially in later operation, stresses occur in such multi-layer electronic components that can be attributed to the different coefficients of thermal expansion of the materials used. Prolonged thermomechanically induced cyclic stresses can lead to the formation and propagation of cracks and eventually to fatigue and failure at the weak points of the electronic components. It is well known, that large area solder joints, which along with bonding wires are the most important electrical, mechanical and thermal connections between chips, substrate and baseplate, play the most critical role in this process. This has been further exacerbated in recent years by the increased emergence of SiC-based technologies and the need to introduce lead-free alternatives as soldering materials [2].

In order to ensure the long-term performance of these joints and to meet the growing demand for virtualized qualification methods, it is essential to have detailed information about their behaviour under cyclic loads. Knowledge of crack initiation, propagation, and degradation is crucial for understanding the fatigue mechanisms of materials. While ex-situ techniques such as ultrasonic microscopy (SAM), computed tomography (CT), thermal resistance measurements [3] or pulse-phase thermography [4] are available for detection of hidden defects of electronic components, the development of more efficient and reliable methods for the non-destructive in-situ detection and monitoring of delamination and cracking before final failure is an important area of current research. Such methods can provide necessary information for precise lifetime prediction models and estimation of the remaining useful life of the components. In particular, it is important to identify the different failure modes caused by interaction of different technologies and material combinations at an early stage of a product development.

Vibrational and modal analysis, employing laser Doppler vibrometry (LDV), has been utilized for the detection of failures, defects, and in-situ monitoring of degradation processes [5]. In the case of electronic packaging, promising attempts have been made to develop non-destructive inspection and systems based on vibration analysis for evaluation of solder joints and wire bonds [6,7]. Acoustic emission (AE) methods are well-established inspection techniques that are applied in advanced structural health monitoring [8], process control, and crack monitoring during fatigue experiments [9]. More recently, AE has been suggested for in-situ quality control during the bonding process [10] and for monitoring the health of IGBT modules during power cycling [11,12]. While the application of the acoustic emission (AE) technique for conventional low-frequency cyclic loading is a well-established topic in AE research [13], its utilization in ultrasonic fatigue testing has been

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https://doi.org/10.1016/j.microrel.2023.115098
Received 2 June 2023; Received in revised form 23 June 2023; Accepted 3 July 2023
Available online 1 October 2023

scarce.

Isothermal mechanical fatigue testing has been proven to be a reliable method for material development and has been proposed as an alternative to thermal cycling for accelerated lifetime assessment of solder joints. In previous studies [14–16] we investigated the high cycle fatigue performance of large-area solder joints using an ultrasonic (20 kHz) mechanical fatigue test based on a cyclic three-point bending (3 PB) method.

In this study, we introduce a novel application, which enables reliable and accurate non-destructive, real-time measurement of delamination crack growth in a variety of multilayered structures found in electronic devices. By utilizing these techniques based on LDV and AE measurements we successfully conducted in-situ detection of crack initiation and monitoring of the interfacial delamination propagation process during isothermal fatigue testing on chip/substrate solder joints before end of life. These investigations were carried out at 175 °C on a series of specially designed chip/solder/direct bonded copper (DCB) model test structures. Optical inspection for detection of the crack initiation and measurement of the delamination using SAM were performed to correlate the change of the vibration behaviour of Si-chip to the delaminated area. Finally, destructive shear testing with a subsequent fracture surface analysis and examination of the metallographic cross-sections of the fatigued samples revealed the extent of damage in the solder joints.

2. Experimental

2.1. Sample design

For the fatigue experiments, model test structures were designed that correspond to the layer structure used in power modules (Fig. 1a). Metallized Si chips (5 × 5 mm) were soldered onto a commercially available DCB substrate (20 × 10 mm) with Cu/Al_2O_3/Cu (300/630/300 µm thickness) using SnAg and SnSb based solder alloys commonly used as lead-free alternatives in such devices. The average thickness of the solder layer was about 100 µm. In previous studies it was found that the sample geometry has a considerable effect on the output of the cyclic bending fatigue tests at 20 kHz. In order to promote crack propagation of the solder layer without inducing fractures in the ceramic substrate or chip, a 45° rotation of the chip relative to the substrate was employed (refer to Fig. 1b). This generates stress concentration sites at the corners of the chip during the 3 PB tests with an increase of the plastic strain compared to conventional design, as was determined by FEM analysis (Fig. 2).

2.2. Finite element method (FEM)

The vibration behaviour of the specimen under time-dependent loading conditions was simulated using FEM analysis with ANSYS software. The loading conditions, were simulated in a fully transient analysis, with each vibration period divided into 38 time steps. Material models were chosen according to one of our earlier studies on the fatigue crack growth of solder joints during cyclic bending fatigue [16]. The mesh of the solder material was created using SOLID 186 tetrahedral elements with the element size adapted to the layer thickness (Fig. 3a, b). To simulate the presence of a delaminated area, a gap of defined length was introduced between the solder and substrate layer (Fig. 3b). Steady state oscillation was ensured by simulating several vibration periods. This simulation allowed us to examine the vibration characteristics at different stages of delamination. Specifically, we recorded the relative increase in the maximum displacement observed at the corners of the chip compared to the DCB substrate (Fig. 3c).

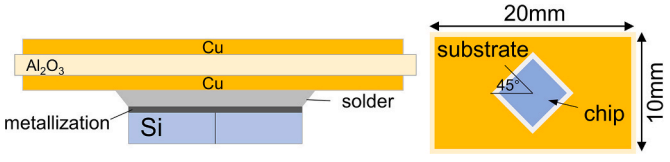

Fig. 1. Schematic (a) cross section and (b) top view of the Si/solder/DCB model samples.

2.3. Resonance fatigue setup

The accelerated fatigue tests were carried out using an ultrasonic resonance testing system consisting of a power supply, a piezoelectric transducer, an acoustic horn with a tip and the specimen which is placed on a 3 PB jig, as schematically shown in Fig. 4. The excitation of a longitudinal vibration at 20 kHz originates from the piezoelectric transducer and is amplified by the horn and suitable coupling pieces. At the point of maximum displacement, the system is coupled to the sample via the 3 PB tip of the horn. The geometry of the specimen must be designed in such a way that a standing transverse vibration is formed at 20 kHz.

The static and cyclic loads were measured with a piezoelectric load washer mounted beneath the supports of the 3 PB device. A static preload, which was about 10 N in our measurements, is necessary to ensure constant contact of the 3 PB tip with the sample during the cyclic excitation. The vibration modes and the displacement amplitude (maximum ca. 7 µm) of the sample during excitation were determined with a laser Doppler vibrometer. The fatigue tests were carried out under isothermal conditions at 175 °C in order to replicate the damage to the solder joints under harsh conditions to which power modules can be exposed during operation. A hot air blower system was used to heat the samples during the test. The temperature was regulated using a closed loop control system.

2.4. In-situ delamination detection

The setup of the non-destructive vibrometer and AE measurement during cyclic 3 PB experiments is shown in Fig. 5. The setup consists of laser Doppler vibrometers to determine the displacement amplitude of the sample, oscillating in a transversal resonant mode at 20 kHz. Two separate measurement points are directed to the corners of the chip by 90° deflecting mirrors while the acoustic emission is recorded by a so-called optical microphone (Xarion ETA100) placed at a distance of 20 mm centrally under the specimen. The microphone works on the principle of a laser Fabry-Pérot interferometer and allows contact-free ultrasound measurement in a frequency range between 10 Hz and 2 MHz. The system allows in-situ monitoring by feeding the analogue signal to a data acquisition software (QUASS Optimizer 4D). The AE signal was passed through a 10 Hz high-pass filter and recorded by the 24-bit A/D card at a sampling rate of 1 MHz. All signal processing algorithms were implemented in Python.

As soon as a crack starts to grow, due to the stress maximum at the corner of the Si chip, the displacement amplitude of the vibrometer signal at the corresponding corner increases relative to the deflection of the substrate. This increase is growing until the test is stopped or the chip is fully separated. The current non- destructive method for in situ fatigue detection was applied to the US-fatigue testing system to determine the time to the initiation of the first crack as well as the delamination rate.

In addition to the LDV measurements the AE signal was analysed to retrieve information on the delamination response. Several effects of the crack growth and delamination process can theoretically be identified in the acoustic emission spectrum [17,18].

To this end, spectrograms, taking a series of FFTs (with a segment length of 1024 readings, using Hanning window) and overlapping them, were calculated from the continuous raw waveform. The obtained spectrogram, in which the amplitude of each frequency is represented by the colour intensity as a function of time, shows the periodic horizontal

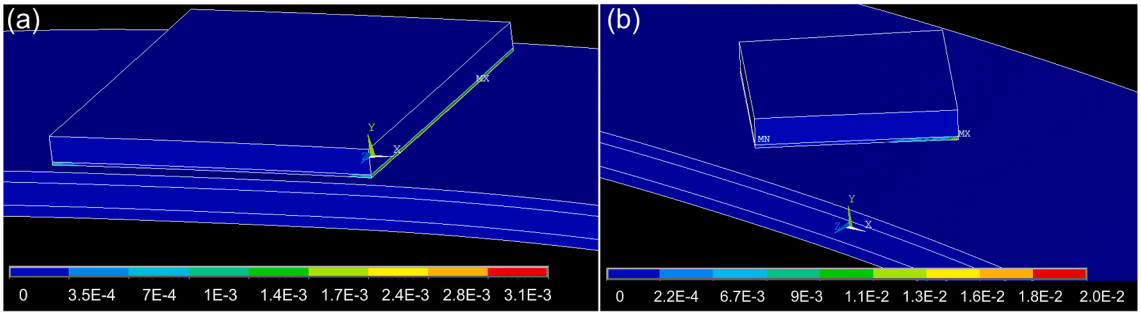

Fig. 2. Plots of v. Mises plastic strain in the solder layer for parallel (a) and 45° rotated (b) chip on DCB substrate.

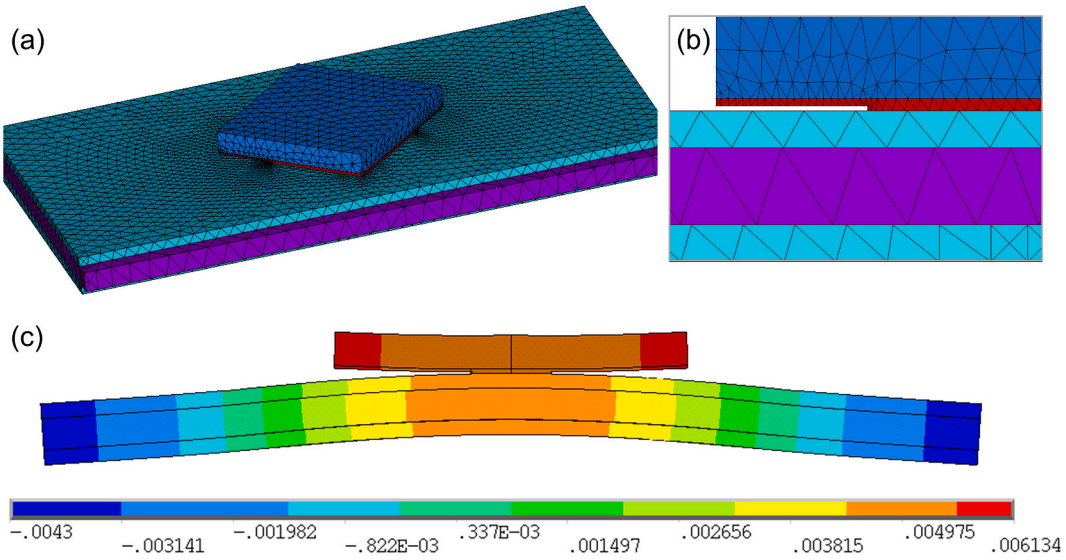

Fig. 3. (a) FEM model with (b) cross sectional detail showing the mesh in the vicinity of the gap, representing the delaminated area. (c) Plot of the displacement amplitude (in μm) during 20 kHz oscillation of the sample highlighting a maximum at the Si-chip corners (delaminated area 40 %).

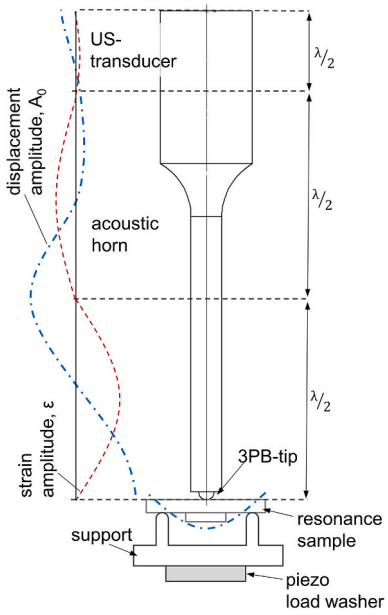

Fig. 4. Schematic and principle of the ultrasonic fatigue testing system.

lines corresponding to the maxima of the FFT function representing the harmonics of the resonance mode (Fig. 6a, b).

In order to identify AE events associated with crack initiation and propagation a processing algorithm which is describe in [19] in more detail was applied. First it is necessary to calculate the cumulative power envelope of the AE, which represents the acoustic energy, from the spectrogram. By utilizing a minimum peak prominence method, individual acoustic events can be detected within the power envelope. The cumulative power of these events can then be calculated by summing up the power of each individual event over time (Fig. 6d–f).

Before applying this processing algorithm, it was necessary to enhance the signal-to-noise ratio of the spectrograms. In the case of the US-fatigue testing system, particular attention was given to filtering out the high amplitude resonance peaks at 20 kHz excitation and its higher harmonics. By calculating the power spectral density (PSD) and filtering out these resonance peaks, a filtered spectrogram was obtained, effectively eliminating the sharp resonance peaks from the analysis (Fig. 6c).

2.5. Failure analysis

Prior and subsequent to testing all samples series were examined by means of scanning acoustic microscopy (SAM) in order to detect possible pores or unsoldered areas in the original sample and to determine the delaminated area due to the fatigue crack growth.

Subsequent to SAM investigations, a number of samples were also subjected to die shear tests, which allows fracture surface analysis and provides information on the fracture mode and crack propagation path.

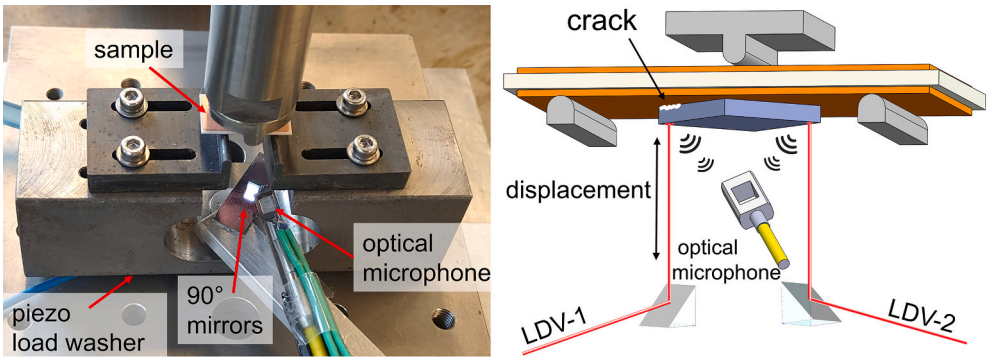

Fig. 5. Setup and schematic of the non-invasive vibrometer and AE measurement during cyclic 3 PB experiments.

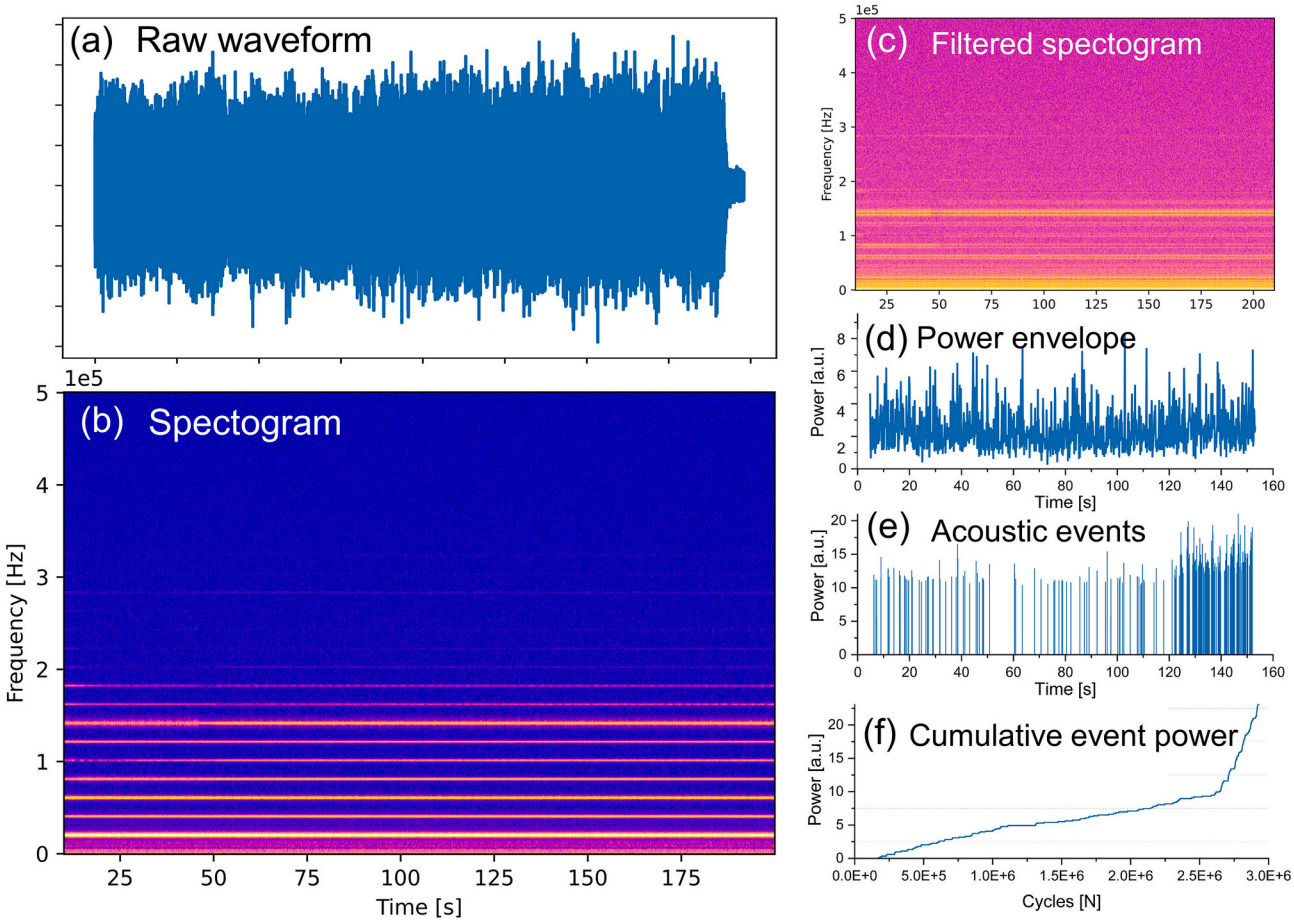

Fig. 6. Processing algorithm for filtering and AE analysis: From the (a) raw waveform a (b) spectrogram is calculated and (c) filtered for the resonance peaks. From the (d) power envelope (e) acoustic events are determined and (f) summed up for a cumulative event power.

Though shear tests are relatively easy to carry out in principle, the brittleness of the silicon and the comparatively large surface area and the associated high loads cause some difficulties in practical implementation. To reduce the stress on the Si, the tests were therefore carried out at an elevated temperature (T = 150 °C). However, partial breakage of the Si chip could not be prevented in all cases.

3. Results and discussion

3.1. Delamination detection

In Fig. 7 the displacement amplitudes vs. number of cycles are exemplary plotted for two measurements and matched with SAM images of the delaminated area after fatigue testing. In the first case the increase in displacement amplitude on both sides is accompanied by symmetrical crack growth originating from both corners of the Si chip. The second example shows one sided delamination in the SAM image with a strong increase in displacement amplitude of the corresponding vibrometer measurements while the amplitude at the other side remains constant. Asymmetrical delamination behaviour can be attributed to process-related quality differences of the solder joints (pores, layer thickness, etc.) or small deviations from the central positioning of the Si chip.

Several samples of both types of solder joints were tested for different numbers of cycles (N = $5\bullet10^6$–$1\bullet10^8$) with a maximum delaminated

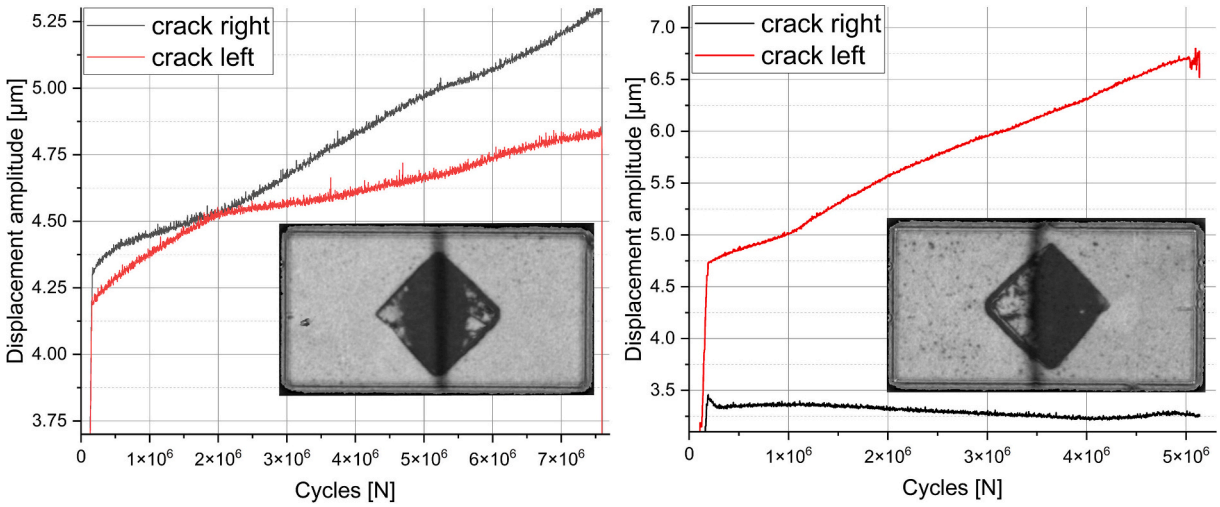

Fig. 7. Examples of two- and one-sided crack growth, SAM images (bright areas indicating delamination) and the corresponding LDV plots.

area of about 30 % at each side. An area of 50 % corresponds to complete delamination of the respective half of the chip. The delaminated area of the samples was determined by using SAM images and was plotted against the relative displacement amplitude increase which was obtained by the vibrometer measurements (Fig. 8). The correlation between the vibrometer signal and the delaminated area can be clearly identified. After establishing such a calibration curve for the respective test structure and loading conditions, this method thus allows in-situ investigations of crack initiation and determination of the delamination rate for a given sample geometry.

Additionally, the progressive delamination-induced change in the vibration characteristics of the specimen was determined using FEM. The displacement amplitude at the corners of the Si-chips of the undamaged sample as well as at several stages of delamination were determined and the relative increase in displacement amplitude relative to the undamaged sample was calculated for different delaminated areas. In a first approximation, symmetrical crack growth was assumed for simulation purposes. These results, along with a fitted curve, presented in Fig. 8, show very good agreement of experimental and simulated results.

Using the signal processing algorithm [19], a correlation between the power and frequency of the acoustic emission events and the progressive damage of the material can be established and can be used to clearly identify the crack initiation. A comparison of the calculated cumulative event power of the AE signal with the increase in displacement amplitude due to delamination at both corners of the chip as obtained by LDV measurements for two different sample are presented in Fig. 9.

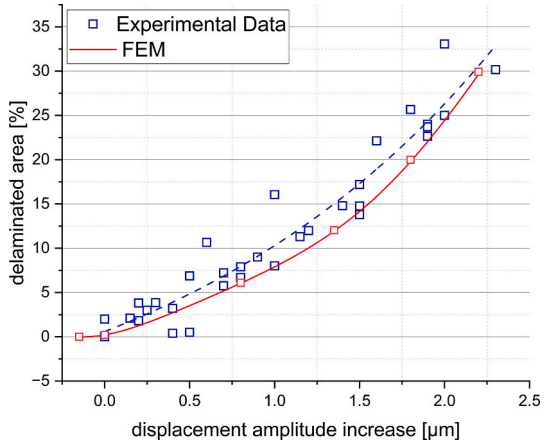

Fig. 8. Relationship between the delaminated area and the relative displacement increase.

In general, the AE analysis agrees well with the vibrometer measurements of the delamination increase. However, it is important to note that depending on the testing conditions, there may be other sources of acoustic emissions such as background noise or structural vibrations that can superimpose the signals caused by the crack propagation. In addition to the complex filtering and processing of the signals already described, a further issue is localisation of a growing crack in this setup which probably requires additional AE sensors. Consequently, while the AE method seems to be a very suitable method for early detection of crack initiation, obtaining a quantifiable result for the progression of delamination, similar to the correlation curve established by LDV measurements, appears challenging using AE analysis alone.

On the other hand, the AE method has proven to be effective in identifying events associated with brittle fractures characterized by short discrete bursts across the entire frequency range, as seen in the spectrograms. In the context of this study, these brittle fractures often indicate unwanted cracks within the Si chips, resulting from uneven load distribution due to slight asymmetries in the sample geometries after soldering. They can also suggest cyclic crack growth within the chip. When a chip fracture occurs, it causes partial relaxation of the specimen and relieves stresses in the solder layer, thereby halting further growth of solder cracks. These chip breaks are visually evident in the AE signals and are accompanied by a flattening or, in more pronounced cases, a slight drop in the delamination amplitude curves recorded by the vibrometer (Fig. 10).

3.2. *Fracture surface analysis*

To investigate the stages of the fatigue crack initiation and propagation in the solder die attach, intermittent SEM investigations of the lateral surfaces of selected samples were performed. It was found that, the fatigue cracks always initiated at the locations of highest stress concentration beneath the corners of the chip independent of the solder alloy. These sites correspond very well to the LDV measurement points during the fatigue testing. The exemplary SEM image presented in Fig. 11a shows a considerable surface roughening, formation of extrusions and micro-cracks in the SnAg solder due to local accumulation of plastic strain. An overview of a delaminated sample, with the fatigue crack growing in the SnSb solder layer along the both sides of chip is presented in Fig. 12b. By using such SEM images, the length of the fatigue cracks along the solder layer was measured to roughly estimate the delaminated area for several samples. Even though the exact crack front in the solder layer was not known, this alternative method was in most

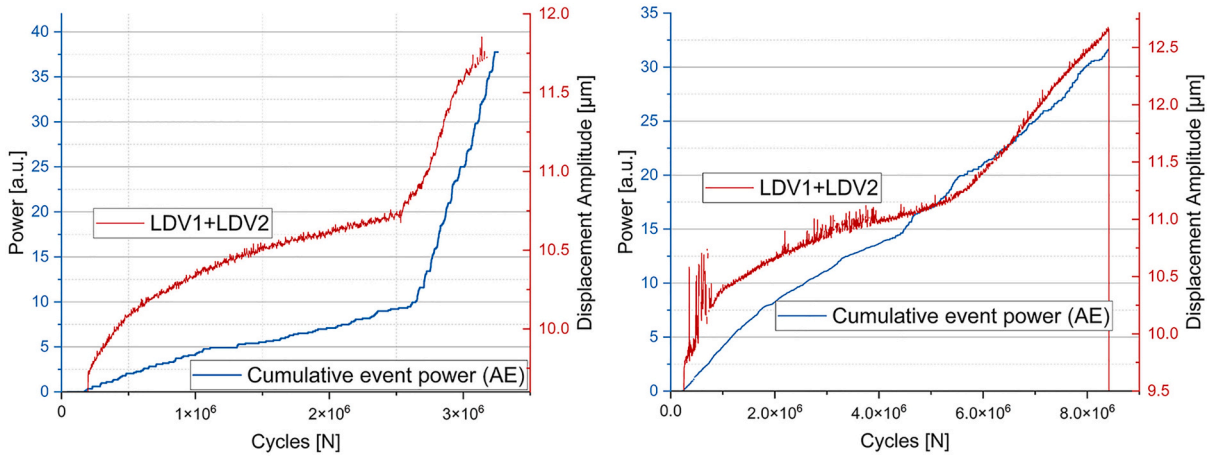

Fig. 9. Exemplary plots of LDV measurements (total displacement increase of both vibrometer signals) and AE analysis (cumulative event power) illustrates similar behaviour.

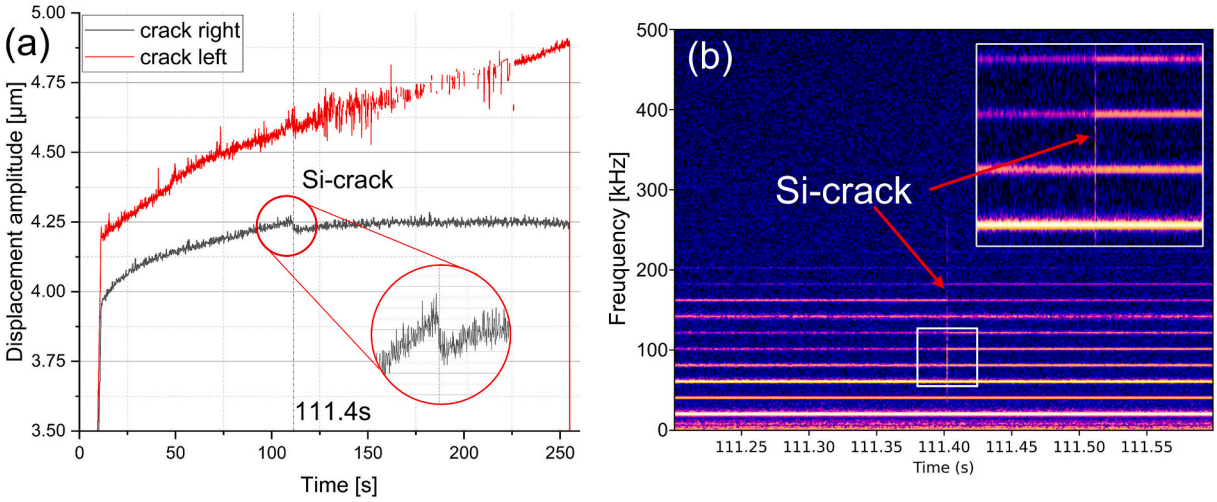

Fig. 10. (a) Displacement amplitude vs. time curves as measured by LDV. The red curve shows increasing delamination while the drop, followed by a flattening in the black curve indicates chip cracking. (b) Corresponding AE signal (spectogram) of the same cracking event shows a discrete burst.

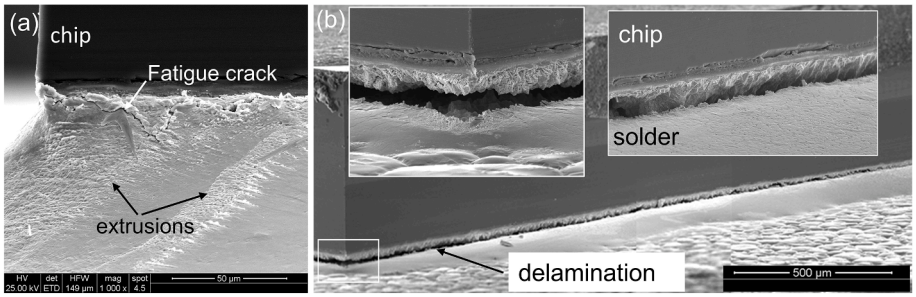

Fig. 11. (a) Strong plastic deformation and fatigue cracking in the solder layer in SnAg (b) Fatigue cracks at the corner of the chip and along the interface in SnSb.

cases in good agreement with SAM measurements.

Investigation of the crack growth path and delamination behaviour within the solder layer was conducted on cross-sectional micrographs of the fatigued samples (Fig. 12). Again, it was confirmed that the crack path always originates near the periphery of the chip/solder interface and propagates into the solder layer. In most cases it was observed, that the cracks further grow towards the DCB substrate and follow the interface near the solder and the Cu_6Sn_5 intermetallic compounds (IMC) above the Cu metallization. Examples of the fatigue fracture surface and morphology of the solder joints subsequent to shear tests which are presented in Fig. 13, also indicate a mixed fatigue crack path within the solder and close to the IMC layer at the back side of the chip. The fractured surfaces at the chip and substrate side distinctly show the fatigued area (dark grey) and the sheared area (light grey) of the solder in Fig. 14a. A comparison of the delaminated area as determined by SAM measurements (Fig. 14b) and the fracture surfaces of the sample after the die shear test (Fig. 14a) reveals a very good correlation.

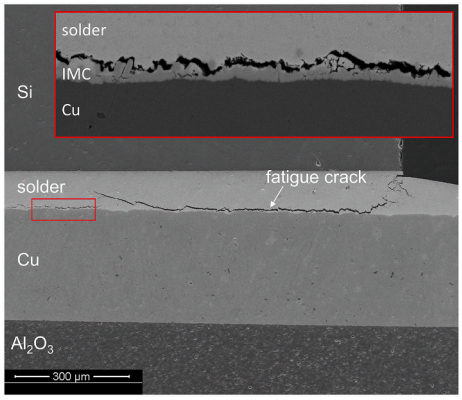

Fig. 12. SEM micrograph of the SnSb solder after fatigue testing showing crack growth along the solder/IMC interface.

4. Summary and conclusions

In this study, we have successfully developed a non-destructive in-situ method based on laser Doppler vibrometry and acoustic emission measurements, that can be applied to accelerated mechanical fatigue testing to detect crack initiation and monitor crack growth in semiconductor structures.

We applied this method to isothermal mechanical fatigue tests of large area SnSb and SnAg based solder joints, commonly used in power semiconductors. Our findings confirm that this technique is suitable for assessing the degree of damage and can serve as a reliable screening method for detecting crack initiation. In combination with FE simulations or complementary measurements of the delaminated area, our method can quantitatively determine the degree of delamination for a defined structure in-situ.

The LDV measurements allowed us to follow the progression of the cracks and to assess the degree of delamination in real time. The correlation between the increase in displacement amplitude and the delaminated area was clearly established. Additionally, AE analysis proved to be a valuable tool for early detection of crack initiation.

By combining the results from both AE analysis and LDV measurements, one can gain a more comprehensive understanding of the delamination-induced phenomena. While the AE analysis captures the presence of acoustic events associated with crack propagation, the vibrometer measurements provide a direct measurement of the displacement amplitudes at the chip corners, allowing for a more detailed analysis of the structural response. Although the AE method offers valuable insights into crack initiation and brittle fracture detection, it is essential to consider the limitations of the technique, such as the inability to localize growing cracks. Moreover, the presence of background noise and structural vibrations can sometimes interfere with the AE signals, demanding sophisticated signal processing algorithm.

Future research should focus on further refining the signal processing algorithms for AE analysis to improve the detection and localization of growing cracks.

The in-situ vibrometer measurement technique combined with

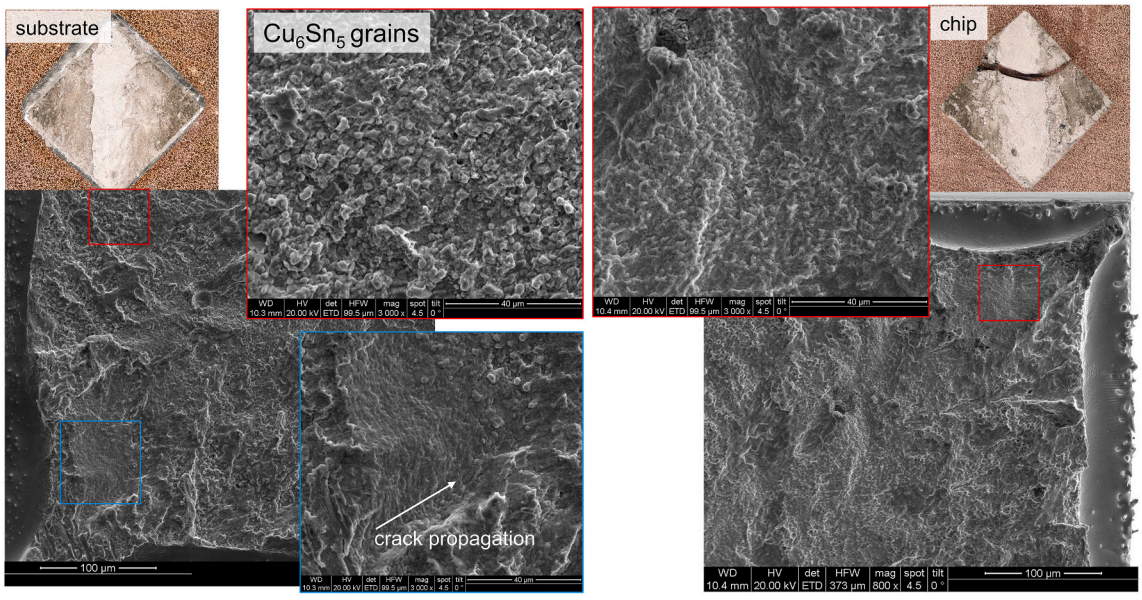

Fig. 13. SEM images of the fatigue fracture surfaces of the chip side and DCB side of a SnSb joint revealed after static shear test. The fatigue crack shows a mixed mode of failure.

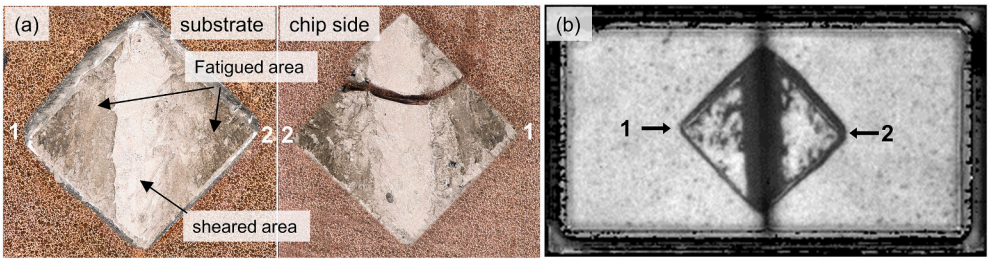

Fig. 14. (a) Fracture surfaces of the fatigued SnSb solder of substrate and chip side after shear test with (b) the corresponding SAM image.

acoustic emission has been demonstrated to be a reliable and accurate method for obtaining essential material properties needed for developing robust lifetime prediction models.

The method demonstrated in this study can be applied to a wide range of multilayer structures.

CRediT authorship contribution statement

T. Walter: Methodology, Formal analysis, Investigation, Data curation, Visualization, Writing - original draft, Writing - review & editing. **G. Khatibi:** Conceptualization, Methodology, Investigation, Writing - original draft, Writing - review & editing. **A. Betzwar Kotas:** Investigation. **N. Kretschy:** Investigation, Formal analysis, Writing - review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

The financial support by the Austrian Federal Ministry for Digital and Economic Affairs, the National Foundation for Research, Technology and Development is acknowledged. The study was partially performed within the frame of the Christian Doppler Labor RELAB at CTA, TU Wien.

The authors acknowledge TU Wien Bibliothek for financial support through its Open Access Funding Programme.

We thank Martin Lederer for his support in FEM simulations.

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