Master Thesis

Electrical Transport in Reconfigurable Transistors Based on the Heterogeneous Integration of Germanium on a Silicon on Insulator Platform

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Abstract

Driven by Moore's Law, the demand for ever more transistors on integrated circuits has surged to power our digital age. This principle predicts the doubling of transistors approximately every two years, propelling technological advancements. As we approach the physical limits of traditional scaling, *beyond CMOS* technologies and innovative material systems emerge as essential pathways. Their adoption ensures sustained growth, meeting the insatiable computational needs of the future. One approach based on functional diversification is the novel device concept of a doping free reconfigurable field-effect transistor (RFET). These stand out by their ability to dynamically switch between n-type and p-type operation during runtime, hence increasing the functional density of the circuit. Since both operation types are united in one single RFET device, typical channel width variations for p- and n-type in order to achieve similar on-state currents are not possible. The desired symmetry and other crucial device characteristics need to be engineered by the underlying material-system. Considering this, the influence on the electrical behavior of an RFET fabricated out of a pure germanium (Ge) layer on top of either a strained or unstrained silicon wafer stack, exerting different amounts of stress on the channel, are investigated in this thesis. Furthermore, the effect of different gate dielectrics, consisting of pure silicon dioxide (SiO_2) or a combination of SiO_2 and zirconium dioxide (ZrO_2), are considered. The respective transistors are fabricated in a top-down fashion out of a Ge on a silicon on insulator (SOI) or Ge on strained silicon on insulator (sSOI) initial wafer, which takes advantage of the electrical properties of Ge like the high charge carrier mobility and small band-gap, while bypassing the difficult and expensive Ge on insulator technology. The required metal-semiconductor-metal heterostructures, in the case of this thesis, the aluminum-Ge-aluminum heterostructure, are formed by thermally activated aluminum (Al) diffusion into the Ge nanosheet, resulting in reproducible, reliable and abrupt transitions. In order to form the SiO_2 passivation, a pure silicon (Si) capping layer atop of the Ge layer is dry thermally oxidized, while the ZrO_2 high-k dielectric is fabricated by atomic layer deposition (ALD). In this thesis four different types of transistors with an increasing number of top-gates are fabricated. The realized RFETs with either two or three independent top-gates, or Schottky barrier field-effect transistor (SBFET) with one single top-gate are electrically characterized. By extensive temperature dependent bias spectroscopy, important properties of the transistors and underlying material system are determined and compared to other RFETs found in literature. Moreover, the performance of single transistor wired logic consisting of RFETs with four top-gates are analyzed. The goal of this thesis was the realization of Ge based RFETs, which offer enhanced electrical properties considering the Si counterparts. Thereby relatively higher on-state currents of the respective modi and sufficient on-state symmetries were achieved. With the addition of ZrO_2 to the gate stack, improvements regarding the On/Off ratio and subthreshold slope were obtained. The material system and RFET structures presented in this thesis highlight the potential for energy-efficient and adaptive circuits in application areas such as hardware security and artificial intelligence.

Kurzfassung

Angetrieben durch die stetig ansteigende Nachfrage nach immer mehr Rechenleistung in integrierten Schaltkreisen, sagt das Mooresche Gesetz die Verdopplung der Transistordichte alle zwei Jahre voraus. Da wir uns jedoch den physikalischen Grenzen der traditionellen Skalierung nähern, gewinnen neuartige Technologien und innovative Materialsysteme immer mehr an Bedeutung. Ein auf funktionaler Diversifizierung basierender Ansatz ist das neuartige Transistorkonzept eines dopingfreien, rekonfigurierbaren Feldeffekttransistors (RFET). Diese zeichnen sich dadurch aus, dass sie während der Laufzeit dynamisch zwischen n- und p-Typ umschalten können, wodurch die Funktionsdichte der Schaltung erhöht wird. Da beide Betriebsarten in einem einzigen RFET-Bauelement vereint sind, müssen gewünschte Stromsymmetrien und andere Transistoreigenschaften durch das zugrundeliegende Materialsystem realisiert werden. Angesichts dessen wird in dieser Arbeit der Einfluss auf das elektrische Verhalten eines RFET untersucht, der aus einer reinen Germanium (Ge)-Schicht auf einer zugverspannten oder unverspannten Silizium-Schicht hergestellt wurde. Darüber hinaus werden die Auswirkungen verschiedener Gate-Dielektrika, bestehend aus reinem Siliziumdioxid (SiO_2) oder einer Kombination aus SiO_2 und Zirkondioxid (ZrO_2), betrachtet. Die entsprechenden Transistoren werden in einem Top-Down Prozess entweder aus einem Ge auf *silicon on insulator* (SOI)- oder Ge auf *strained silicon on insulator* (sSOI)-Ausgangswafer hergestellt, wodurch die elektrischen Eigenschaften von Ge, wie die hohe Ladungsträgerbeweglichkeit und die kleine Bandlücke genutzt werden, während die schwierige und kostspielige *Ge on insulator* Technologie umgangen wird. Die erforderlichen Metall-Halbleiter-Metall-Heterostrukturen, in diesem Fall die Aluminium-Ge-Aluminium-Heterostrukturen, werden durch thermisch aktivierte Aluminiumdiffusion gebildet, was zu reproduzierbaren, zuverlässigen und abrupten Übergängen führt. Zur Bildung der SiO_2-Passivierung wird eine Opferschicht aus reinem Silizium (Si) über der Ge-Schicht thermisch oxidiert, während das high-k Dielektrikum ZrO_2 durch Atomlagenabscheidung hergestellt wird. In dieser Arbeit werden vier verschiedene Typen von Transistoren mit einer zunehmenden Anzahl an Top-Gates hergestellt. Die hergestellten RFETs, mit entweder zwei oder drei unabhängigen Top-Gates oder Schottky-Barriere-Feldeffekttransistoren (SBFET) mit einem einzigen Top-Gate, werden durch umfangreiche temperaturabhängige elektrische Charakterisierung wichtige Eigenschaften der Transistoren und des zugrundeliegenden Materialsystems bestimmt sowie mit anderen RFETs aus der Literatur verglichen. Darüberhinaus werden die Schalteigenschaften von Logikschaltungen, bestehend aus einem einzelnen RFET mit vier Top-Gates, analysiert. Ziel dieser Arbeit war die Realisierung von Ge-RFETs, welche verbesserte elektrische Eigenschaften zu Si-RFETs aufweisen. Dabei wurden verhältnismäßig höhere Ströme und verbesserte Ein-Zustands-Symmetrien erreicht. Durch das Hinzufügen von ZrO_2 zum Gate-Stapel konnten Verbesserungen hinsichtlich des Ein- zu Aus-Zustands Verhältnisses und der Unterschwellenstrom-Steigung erzielt werden. Das in dieser Arbeit vorgestellte Materialsystem und die RFET-Strukturen zeigen das Potenzial für energieeffiziente und adaptive Schaltungen in Bereichen wie Hardwaresicherheit und künstliche Intelligenz auf.

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I would like to devote this thesis to my grandmother, Brigitta, who sadly passed away during the writing of this work. *Farewell Oma!*

Contents

Chapter 1

Introduction

The experimental invention of the transistor by J. Bardeen, W. Brattain, and W. Shockley in 1947 marked a pivotal moment in technological history, laying the foundation for the digital revolution that has transformed our daily lives and reshaped society [1, 2]. From the pocket-sized smartphones we depend on to the global networks that connect us, the profound impact of transistors is felt in every corner of our interconnected world. The increasing role of semiconductors in global technology has elevated their strategic importance in geopolitical affairs, not only leading to competition but also tensions between nations [3–5]. Moore's Law, which predicts the doubling of transistors on a chip approximately every 24 months, has motivated this influence by driving rapid technological advancements and intensifying the global race for semiconductor dominance [6, 7]. Even though the first transistors were made out of germanium (Ge), silicon (Si) transistors quickly established afterwards, mainly due to its high quality native oxide, silicon dioxide (SiO_2), in metal-oxide-semiconductor field-effect transistors (MOSFET) [8]. Furthermore, Si has a higher band-gap than Ge, enabling lower off-state currents and higher operating temperatures. A further reduction in power consumption was achieved by the introduction of complimentary metal-oxide-semiconductor (CMOS), consisting of, as the name suggests, complimentary n- and p- metal-oxide-semiconductors (n/p-MOS) [9]. However, different charge carrier mobilities lead to disparate on-state currents of the complimentary devices. In order to overcome this flaw, the two counterparts are geometrically asymmetric, resulting in symmetric on-state currents. Following Moore's law by continuous down scaling of the related transistor dimensions inevitability leads to fundamental scaling limits, noticeable by higher leakage currents due to increasing tunneling charge carriers through the thinner oxide layers [10–12].

In order to overcome these scaling limits, novel device concepts comprising new material combinations, like the integration of high-k dielectrics in combination with SiO_2, and high charge carrier mobility semiconductors like Ge, need to be considered. So-called "Beyond

CMOS" concepts focus on the functional diversification of devices, thereby leading to the desired increase in functional density. Reconfigurable field-effect transistors (RFETs) are one emerging device concept, enabling dynamic switching between p- and n-mode during runtime, thus making it an interesting candidate for future applications in the field of adaptive or neuromorphic computing and hardware security [13–17]. Based on Schottky barrier field-effect transistors (SBFETs), tunnel field-effect transistors (TFETs) and junction-less transistors, the RFET offers a channel doping free alternative to the aforementioned device concepts [13, 18, 19]. Additionally, since both operation types are combined in one single device, the geometric symmetry is inherently given while the on-state current symmetry is determined by the material system itself. The respective operation mode is electrically determined by the applied voltage, effectively controlling the Schottky barriers and band bending.

Based on the preceding, in this thesis the aforementioned novel device concept, the RFET, is realized with Ge as semiconductor material and aluminum (Al) as contact metal, resulting in a Al-Si-Ge-Si-Al multi-heterostructure with abrupt transitions [20]. The fabricated RFET structures are electrically characterized and evaluated in terms of their device performance in both p- and n-type mode. Thereby the electric behavior of RFETs with different top-gate arrangements, possessing two, three or four individual top-gates, placed over the metal-semiconductor junction or channel region, are investigated. In addition, SBFETs with one single top-gate, overlapping both metal-semiconductor junctions and the channel area, are characterized. Furthermore, the influence on the electrical performance of two base-substrates, exerting different amounts of stress on the Ge channel layer, is analyzed. Moreover, beside SiO_2 as gate dielectric, the device behavior with an additional high-k dielectric layer, like zirconium dioxide (ZrO_2), was investigated. The used top-down fabrication approach enables wafer-scaled processing, which is favorable in today's semiconductor industry [15].
The chosen Al-Ge channel material aims to achieve RFET devices with high on-state currents with good symmetries along with low off-state currents. This design enables energy efficiency, dynamic mode switching and adaptive circuits. Furthermore, it's fabricated using established processes and without doping, making it a strong contender for modern transistor applications [21, 22].

The questions that emerge and will be explored in this thesis are whether the chosen Ge material system, composed of the underlying silicon on insulator (SOI) or strained silicon on insulator (sSOI) substrate, is suitable for RFET applications and how high-k dielectrics influence the device behavior. Moreover, the device performance in comparison to other existing RFETs based on Ge and Si is of interest.

The thesis at hand is divided into four main chapters: theory, experimental techniques, results and a summary followed by a short outlook. Thereby, Chapter 2 introduces the used materials, the metal-semiconductor junction along with the RFET concept. Chapter 3 outlines the used fabrication processes and introduces various electrical characterization

methods, enabling a detailed investigation of the obtained structures. Chapter 4 discusses the measurement results based on the techniques described earlier and puts the measured RFET parameters into perspective by a comparison to other RFETs presented in literature. Chapter 5 concludes with a summary of the findings and gives an outlook for future research on the material system and device structure.

Chapter 2

Theory

This chapter provides a piecewise introduction of the building blocks composing the physical properties of the RFET, culminating in a presentation of the RFET concept itself. Starting with the first piece comprising the materials forming the RFET channel and corresponding gate dielectric in Section 2.1. The channel is in turn fabricated out of a silicon or strained silicon on insulator stack, which is explained in Section 2.2, being the second part. The third introduced building block are the metal-semiconductor junctions in Section 2.3. Last but not least, the overall RFET concept, benefits and working principal is explained in Section 2.4.

2.1 Materials

This section is separated into two subsections and will give an introduction to the used channel material and gate dielectrics.
First, the main properties of Ge along with a short comparison to Si are presented in Section 2.1.1 and Section 2.1.1.1, respectively. The second part deals with the used gate dielectrics in Section 2.1.2 and is itself divided into two parts. The first part in Section 2.1.2.1 outlines the electrical and physical characteristics of Si and Ge oxide while the second part introduces high-k dielectrics in Section 2.1.2.2, which enable further device scaling and better electrical controllability.

2.1.1 Germanium

First discovered in 1866 by Clemens Winkler in Freiberg, Germany [23], Ge is a metalloid with the atomic number 32 and is part of the carbon group. Therefore, Ge is located in the fourth main group and fourth period in the periodic table, right beneath silicon (Si) and is showing similar characteristics. With an average Ge content in the earth's crust of 1.5 parts per million, it is a fairly rare element and does not occur as a native metal in

nature, but as a Ge mineral, where over 30 different compositions are known today [24]. Consequently, sophisticated refinement and purification techniques were needed in order to get highly pure and defect-free, electron-grade Ge for reliable devices. These requirements were faster achieved for Si, making this the first reason for the transition away from Ge and towards Si. As a fact, the first Si transistor was demonstrated by M. Tanenbaum seven years after its Ge counterpart in 1954 [25]. However, nowadays Ge is, like Si, also available in high purities, which, among others, are achieved by zone-refining methods [26]. Further details on refinement techniques for Ge and Si, like the before mentioned zone-refining methode as well as on Czochralski processes, can be found in [27].

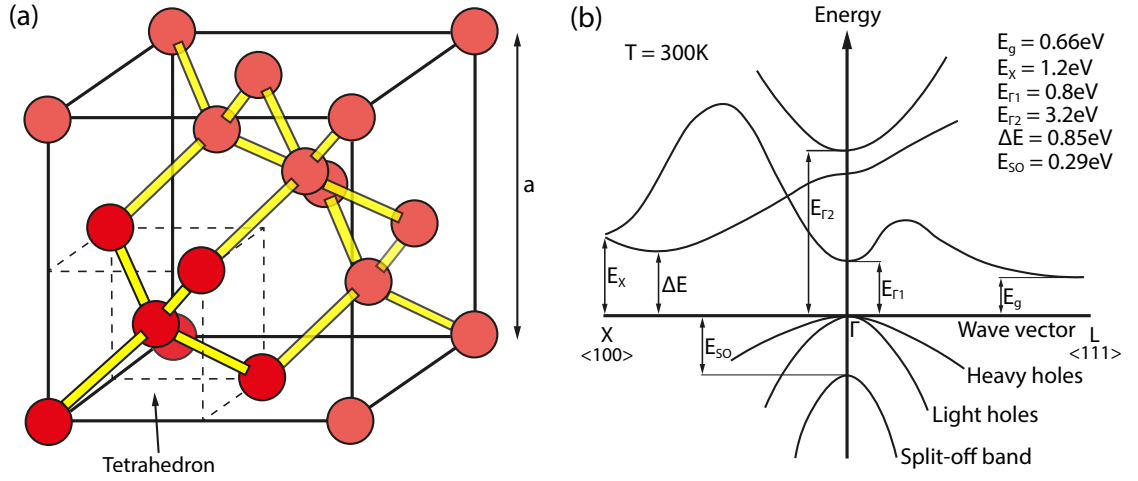

Figure 2.1: *Diamond crystal structure and band diagram of Ge. Subfigure (a) shows a diamond crystal structure along with a highlighted tetrahedron. In (b) the band structure of Ge is outlined as well as the energies of the most prominent band transitions.*
Diamond crystal structure adapted from [28, 29], Band diagram adapted from [30].

The electron configuration of Ge is as follows: $[Ar]3d^{10}4s^24p^2$ [30]. It exhibits four sp^3 hybridized valence electrons forming a tetrahedron which crystallize in a diamond crystal structure, depicted in Figure 2.1 (a). A covalent bond is formed between neighboring Ge atoms and all available electrons are shared between them in order to fill the bonding orbitals. This forms a fully occupied valence band and an empty conduction band separated by an energy gap [31]. As depicted in the band diagram in Figure 2.1 (b), Ge is an indirect semiconductor with a minimum energy gap of E_g=0.66eV at the L point. A direct band transition, without the need for an impulse change, is also possible at the Γ point with an energy difference of $E_{\Gamma 1} = 0.8$ eV. Distinct to Si, Ge possesses both a high hole and electron mobility of $\mu_h = 1900$ and $\mu_e = 4900\ cm^2V^{-1}s^{-1}$.

2.1.1.1 Comparison to Silicon

Si and Ge are quite similar regarding their physical and electrical behavior, both being semiconductors in the fourth main group. However, when comparing them side by side like in Table 2.1 the key advantages of Ge over Si become evident. The most essential advantage

Table 2.1: *Comparison between Ge and Si in terms of their physical and electrical parameters. Values taken from [30]*

Parameter	**Ge**	**Si**
Crystal structure	Diamond	Diamond
Lattice constant [Å]	5.658	5.431
Band gap, E_g $[eV]$	0.66	1.12
Electron affinity, χ $[eV]$	4.0	4.05
Electron mobility, μ_e $[cm^2V^{-1}s^{-1}]$	3900	1400
Hole mobility, μ_h $[cm^2V^{-1}s^{-1}]$	1900	450
Density, ρ $[gcm^{-3}]$ [27]	5.32	2.33
Melting point, T_m $[°C]$ [27]	937	1412

of Ge is a 2.5 and 4 times higher electron and hole mobility and a smaller band gap in comparison to Si. However, all these advantages outweigh the poor quality of germanium oxide (GeO) or germanium dioxide (GeO_2) in comparison to silicon dioxide (SiO_2). The solution is a device architecture utilizing the superior electrical characteristics of Ge as channel material in combination with a SiO_2 gate dielectric. Details about the techniques used in this work in order to overcome the challenges of Ge as a channel material can be found in Section 2.2 where the Si capping layer is introduced and Section 3.1.1 where this layer is oxidized in order to form a high quality SiO_2 interface between the Ge and the top gate metal. The electrical controllability and/or scalability can further be improved by stacking a high-κ, commonly written as high-k, dielectric on-top of the SiO_2 interface layer.

2.1.2 Dielectrics

Dielectrics are used as insulation layer between the semiconductor channel and the top-gate metal. In the following subsections a comparison between Si oxide and Ge oxide Section 2.1.2.1 is given followed by an introduction to high-k dielectrics in Section 2.1.2.2, which are used to further improve the electrical characteristics of a transistor.

2.1.2.1 Silicon Oxides Vs. Germanium Oxides

Ge forms a multitude of different oxides like GeO in amorphous form and GeO_2 which can be found in different crystallinities like hexagonal, tetragonal and also amorphous [32]. Often GeO and GeO_2 coexist making the dielectric unstable at room temperature and even water soluble in some forms [32]. Furthermore, the formed oxide strongly depends on the applied temperature and pressure during growth [33]. The preferred native oxide for electronic devices would be GeO_2, possessing the lowest defect density and leakage

current [33]. Further details about the formation or removal and electrical characteristics of GeO and GeO_2 along with the need for alternative insulators ranging from SiO_2 to high-k dielectrics can be found in [32] and the following section, Section 2.1.2.2.

SiO_2 on the other hand is very stable, has a low interface defect density along with a high breakdown field, resulting in low leakage currents and thus makes it an excellent insulator. For electronic applications, usually amorphous SiO_2 is used. It can be grown by a variety of different techniques like thermally-induced oxidation, chemical vapour deposition (CVD), evaporation, sputtering and more, all exhibiting different densities and qualities [28]. Native Si oxide is also formed if Si is exposed to ambient air. The lowest defect densities are achieved by chemically grown SiO_2 at low growth temperatures and slow growth speeds [34].

2.1.2.2 High-k Dielectrics

In 2007, the semiconductor industry witnessed its biggest change since the late 1960s and the introduction of poly-silicon gates in order to keep up with the trend of Moore's law, stating that transistors should halve in size every 24 months [6, 35]. High-k dielectrics were introduced to the gate stack, effectively minimizing leakage currents.
Due to constant field scaling, CMOS scaling not only concerned the reduction in channel length but also all other dimensions [10, 11]. This meant that, among others, the channel width, depletion layer thickness, supply voltage and, most importantly, the gate oxide thickness would have to be reduced. At some point, the insulating layer was supposed to be only a couple of atom layers thick, thus increasing gate leakage currents dramatically. The scaling limit of SiO_2 was reached [36].
This chapter will therefore introduce high-k dielectrics and highlight their advantages over conventional SiO_2. Furthermore, some potential high-k dielectrics for devices fabricated in the scope of this thesis are listed and compared in Table 2.2 and Figure 2.2. In subsection Section 4.2.1 of the results and discussion chapter, the usage of the high-k dielectric ZrO_2 for this thesis is motivated.

By the introduction of dielectric layers with higher relative permittivities ϵ_r, also referred to as high-κ or just high-k, the equivalent oxide thickness (EOT) can be reduced even further, fulfilling Moore's law. Due to the increase in ϵ_r a constant electrical capacitance, formed by the gate electrode, the high-k dielectric layer and the channel, allowed thicker oxide layers according to [35]:

$$C = \frac{\epsilon_o \epsilon_r A}{t_{ox}}$$

As a result of the increased oxide thickness t_{ox}, the gate leakage current along with the power consumption was effectively reduced [37]. The before mentioned equivalent oxide thickness, or short EOT, of the high-k oxide layer represents the corresponding thickness

Table 2.2: *Relative permittivity ϵ_r, band gap E_g and electron affinity χ of Si, Ge and SiO_2 in comparison with possible high-k dielectrics.*
Values for Si and Ge taken from [30], Values for the electron affinity and bang gap of the dielectrics taken from [38], Values for the rel. permittivity of ZrO_2 taken from [39], while the remaining are from [36].

Material	**Rel. permittivity ϵ_r**	**Band gap E_g [eV]**	**Electron affinity χ [eV]**
Si	11.9	1.1	4.0
Ge	16.2	0.66	4.0
SiO_2	3.9	9	0.9
Al_2O_3	9.5 - 12	8.8	1
HfO_2	16-30	6	2.5
ZrO_2	20-30	5.8	2.5

of a SiO_2 layer, which has the same electrical capacitance and can be calculated as follows [36]:

$$\begin{aligned} C_{SiO_2} &= C_{high\ k} \\ \frac{\epsilon_{r_{SiO_2}}}{t_{ox_{SiO_2}}} &= \frac{\epsilon_{r_{high\ k}}}{t_{ox_{high\ k}}} \\ EOT = t_{ox_{SiO_2}} &= \frac{\epsilon_{r_{SiO_2}}}{\epsilon_{r_{high\ k}}} \cdot t_{ox_{high\ k}} \end{aligned}$$

Table 2.2 compares the relative permittivity ϵ_r, band gap energy E_g and electron affinity χ of some high-k dielectrics which were considered for this thesis. The values for Si and Ge are also listed as a reference. An increased dielectric constant goes along with a decreased band gap [40]. Therefore, a trade off between ϵ_r and band gap energy, or the respective oxide thickness and barrier energy needs to be considered. Furthermore, as shown in Figure 2.2, the dielectric band alignment with respective to the semiconductor valence and conduction band edge needs to be taken into account for the case of Ge in combination with the dielectrics mentioned in Table 2.2.

A schematic band diagram highlighting the valence and conduction band edge offsets between a semiconductor and dielectric is shown in Figure 2.2 (a). The corresponding band offsets for Ge and potential high-k dielectrics stated in Table 2.2 are indicated in Figure 2.2 (b). Note the lower conduction barrier height in comparison to the valence band barrier, which applies for all depicted oxides. In the case of HfO_2 and ZrO_2 the conduction band offset is even less than half the valence band offset. Note, that the illustrated band diagrams in Figure 2.2 (a) and (b) show idealized alignments without interface defects or charges inside the dielectric.

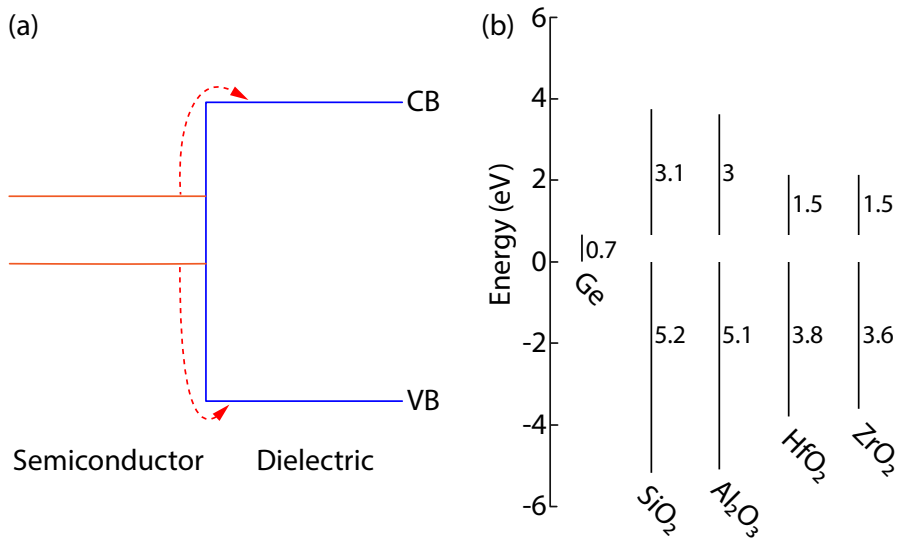

Figure 2.2: *Idealized semiconductor/dielectric band diagram. Subfigure (a) shows a schematic band diagram of an arbitrary semiconductor and dielectric in flat band condition. The red arrows indicate the required emission energies needed in order to overcome the energy barriers.*
Subfigure (b) illustrates the band offset of potential high-k dielectrics and SiO_2 to the Ge valence band edge. The calculated valence and conduction band offsets are stated for each dielectric. The energies are normalized to the Ge valence band edge.
Calculated values are rounded and taken from Table 2.2.

2.2 Germanium Rich Layers on Insulators

Isolating only the electrical properties of Ge, independent of the surround geometry, is crucial for a proof of concept work as presented in this thesis. This isolation is achieved by an insulating layer encapsulating the semiconductor. Therefore, this chapter will highlight the benefits of semiconductor on insulator technologies in comparison to their bulk counterpart. For this purpose, the advantages of Si on insulators (SOIs) are first highlighted along with the differences to germanium on insulators (GeOIs). Next, a Ge on Si insulator platform is introduced, combining both strengths of pure Ge and SiO_2.

SOIs consist of a thick Si handle wafer at the bottom, followed by a buried oxide layer (BOX) and Si device layer on top. In the case of Si the BOX usually consists of SiO_2, which is isolating the bulk handle wafer from the actual device layer. As a result, parasitic capacitance's and bulk leakage currents are reduced, consequently improving device performance and power consumption [41]. Another benefit of SOI is the transversal confinement of the channel in height enabling partial or full depleted MOSFETs, which further improves the controllability [42]. This is also interesting for RFETs, since the off current can be reduced even further by fully pinching off the channel as in conventional JFETs.
GeOI share the advantages of SOI technologies, however with major drawbacks in quality due to the poor electrical and physical characteristics of native Ge oxides, as stated

in Section 2.1.2.1. Other dielectrics like Al_2O_3 are used instead, which however further complicate the fabrication process [43]. Furthermore, high quality Ge is harder to manufacture than Si, thus bulk Ge with lower quality is often used, possessing higher dislocation densities and lower charge carrier mobilities [44].

In order to utilize the benefits of Ge as semiconductor material, as described in Section 2.1.1, a high quality BOX and Ge device layer are needed. A combination of SOI with a Ge layer is required. One approach to solve this issue, is the growth of Ge on top of a strained silicon on insulator (sSOI) or SOI base material, consisting of a SiO_2 BOX and a Si handle wafer [45, 46]. The high quality Ge device layer is thereby epitaxially grown by molecular beam epitaxy (MBE). However, due to the lattice mismatch of Si and Ge, given in Table 2.1, internal strain limits the grown layer thickness and results in increased dislocation densities and surface roughness. By adding another SiGe layer with a higher Ge content, the internal stress of the Ge device layer is reduced and thicker layers are depositable [45]. Oxidation of the Ge layer is prevented by adding a Si capping layer atop. A sketch of the resulting stack is presented in Figure 3.1 of the next chapter covering the fabrication techniques. Note, that the bottom semiconductor handle wafer and BOX can act as an additional back-gate.

2.3 Metal-Semiconductor Heterostructure

The metal-semiconductor heterojunctions and the resulting transitions are essential for the working principal of RFETs. Therefore, this chapter is devoted to this topic, starting with an introduction to metal-semiconductor transitions and what happens to the band diagram if they are brought into contact, illustrated in Figure 2.3 along with important designators. An overview of the resulting contacts is given in Figure 2.4. The emerging pinning level depending on the used semiconductor (Si or Ge) and metal is discussed in Figure 2.6. The actual contact formation between the metal and semiconductor is addressed in Section 2.3.1.

The vacuum level indicates the energy level of a free stationary electron and is a reference energy for materials with different work functions. In Figure 2.3 (a) and (c) the metal and p- and n-type semiconductor with the work-function Φ_m and Φ_s are aligned to the vacuum level. Since both materials are far apart from each other they do not influence one another. This however changes if the metal and semiconductor are brought in close contact to each other as shown in Figure 2.3 (b) and (d) where the fermi levels must align at thermal equilibrium. Depending on the metal work function Φ_m and the semiconductor fermi level the band of the semiconductor is either bent upwards, as depicted in (b) for a p-doped semiconductor, or downwards, as shown in (d) for n-type doping. The gradient of the bending and the width of the depletion zone depend on the doping intensity [28]. The resulting barrier height however, is determined by the difference from the metal work function Φ_m and the electron affinity χ_s of the respective semiconductor, as shown in the

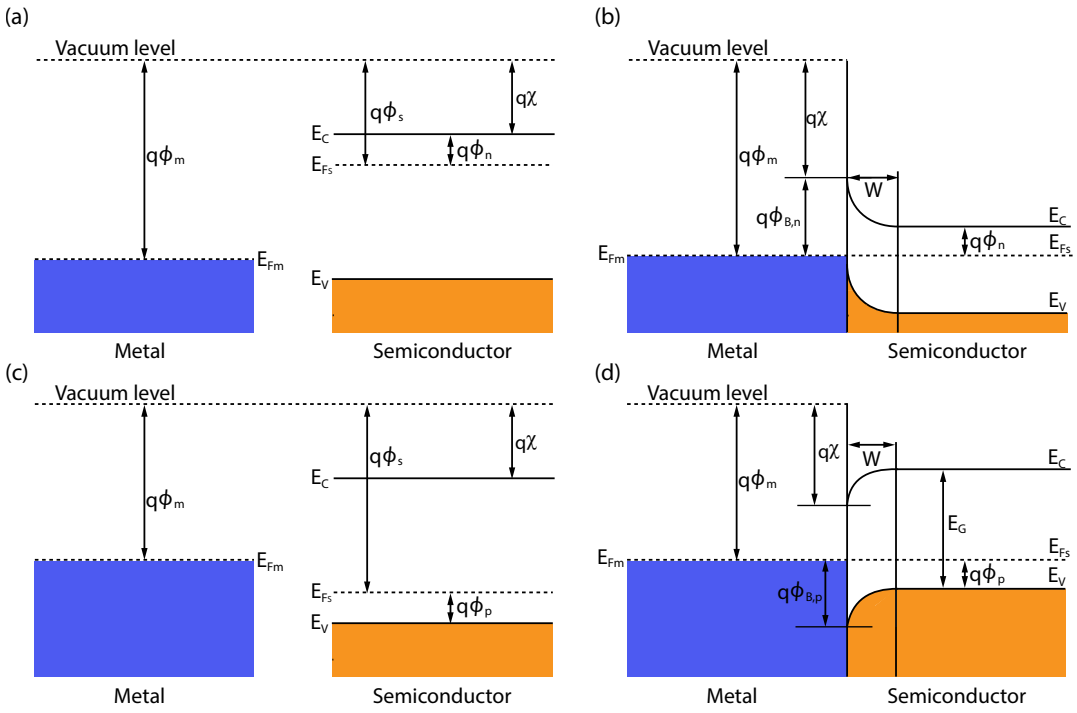

Figure 2.3: *Band diagram for a metal and p- or n-type semiconductor before and after contacting. In subfigure (a) and (c) the metal and semiconductor are align in respect to the vacuum level. When brought into close contact to each other, the fermi level of the metal and semiconductor align and a band bending occurs, illustrated in subfigure (b) and (d). The bending curvature and direction depends on the metal and semiconductor work-function Φ_m and Φ_s respectively. Subfigures (a) and (b) show a n-type semiconductor and subfigures (c) and (d) a p-type semiconductor.*
E_F represents the fermi level energy, Φ the work-function, χ the electron-affinity, q a charge, E_C and E_V the conduction and valence band energies along with E_G the band-gap energy, W the width of the depletion region, Indices M or S stand for metal and semiconductor, respectively, Φ_B for the induced barrier along with Φ_n and Φ_p for the energy difference from conduction- or valence-band to fermi level for n- and p-type semiconductor [47].
Adapted from [28, 29, 48]

following equations [28]:

$$q\Phi_{B,n} = q(\Phi_m - \chi_s)$$
$$q\Phi_{B,p} = E_G - q(\Phi_m - \chi_s)$$

This approximation assumes a defect free interface and a abrupt metal-semiconductor junction [28, 49]. Dangling bonds or interface states could shift the barrier height and curvature and would result in unreliable contacts. Therefore, a low interface state density is crucial for a reliable and reproducible device behavior [49, 50].

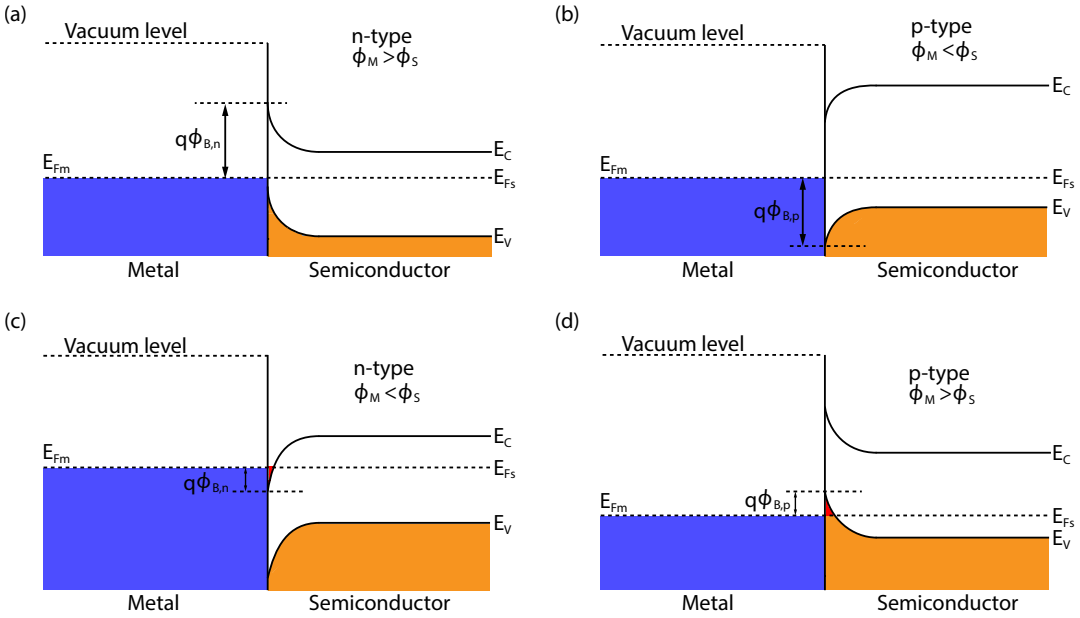

Figure 2.4: *Illustrations of metal-semiconductor transitions for p- and n-type semiconductors and metals with different work functions, resulting in Schottky or Ohmic contacts. In subfigure (a) and (b) a Schottky contact is formed, hence presenting a barrier for electrons and holes. No barrier is present for the materials presented in subfigure (c) and (d), which form a so-called Ohmic contact. (a) and (c) show the band bending for a n-type semiconductor, (b) and (d) for a p-type semiconductor along with different metal work functions Φ_m. The relation between the metal and semiconductor work function is stated in the respective subfigure.*
Adapted from [28, 29]

As mentioned above, depending on the used material composition forming the contact-interface, different band bendings and barrier heights are observed. Four distinct scenarios are depicted in Figure 2.4 for either a n- and p-type semiconductor in contact with a metal possessing a lower or higher work function as the corresponding semiconductor. Among these four cases, two specific band alignments emerge.
The first one is a so-called Ohmic contact, which is defined by have a negligible small contact resistance relative to the bulk metal or semiconductor, illustrated in Figure 2.4 (c) and (d). Therefore, the metal-semiconductor junction should not degrade the device performance significantly [51]. An Ohmic contact is formed, if the respective fermi level is above or below the conduction or valence band respectively, resulting in unoccupied states above the fermi level at the interface, highlighted in red.
The second type is a so-called Schottky contact shown in subfigure (a) and (b) in Figure 2.4. In contrast to the ohmic contact, the Schottky contact does not have unoccupied boarder states since the fermi level is inside the band-gap. This results in a rectifying behavior due to the formed barrier. Devices designed for both electron and hole currents should have a

nearly identical barrier height for both charge carrier types. This can, to some degree, be engineered by the metal and semiconductor composition, as discussed in the end of this section.

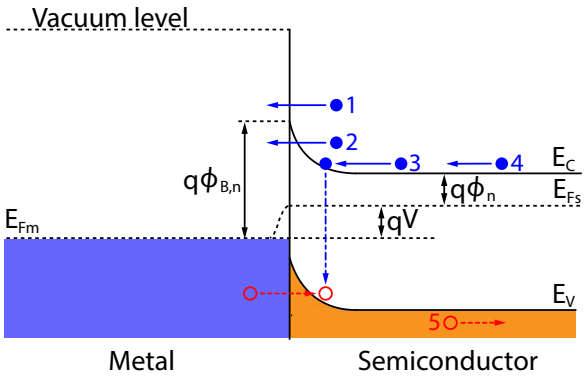

Figure 2.5: *Charge carrier transport mechanisms for electrons and holes at Schottky barrier. The total current flow consists of (1) thermionic emission, (2) tunneling, (3) hole recombination, (4) electron diffusion into depletion zone and (5) hole injection to the semiconductor. Adapted from [28, 29]*

Further band bending of the Schottky barrier is achieved by the application of a bias voltage across the metal-semiconductor junction, resulting in a lower or higher flow of charge carriers. According to Sze [28] metal-semiconductor junctions are mostly dominated by the majority carriers which can be subdivided into five different transport mechanisms illustrated for a positive bias in Figure 2.5. The thermionic emission, enumerated with (1), represents electrons which are thermally excited and surpass the barrier while quantum mechanical tunneling (2) on the other hand describes the tunneling of chargers trough the barrier itself. Moreover, the recombination of electrons and holes in the space charge region (3) also result in a charge motion. Furthermore, electrons can diffuse towards the space charge region (4) while holes are injected into the metal (5).

Depending on the applied conditions, like the bias voltage, temperature, doping and metal-semiconductor composition, distinct charge carrier transport mechanism dominated. Since the total current is a superposition of all mechanisms it is difficult to distinguish them from each other. Alternatively the different transport mechanisms can be categorized into three types, namely the field emission (FE), reflecting the tunneling current through the barrier, the thermionic emission (TE), identical to the afore introduced, and the combination of both mechanisms denoted as thermionic-field emission (TFE).

As mentioned before, by using different metals and/or semiconductors the barrier height and relative energy can be modulated. This is summarized in Figure 2.6 for Ge and Si along with a variety of contact metals. For Si a large, however equal, barrier height for electrons and holes is created by most metals and is hence located close to the band-gap center. This implies a strong fermi level pinning for an intrinsic semiconductor [53]. For Ge on the

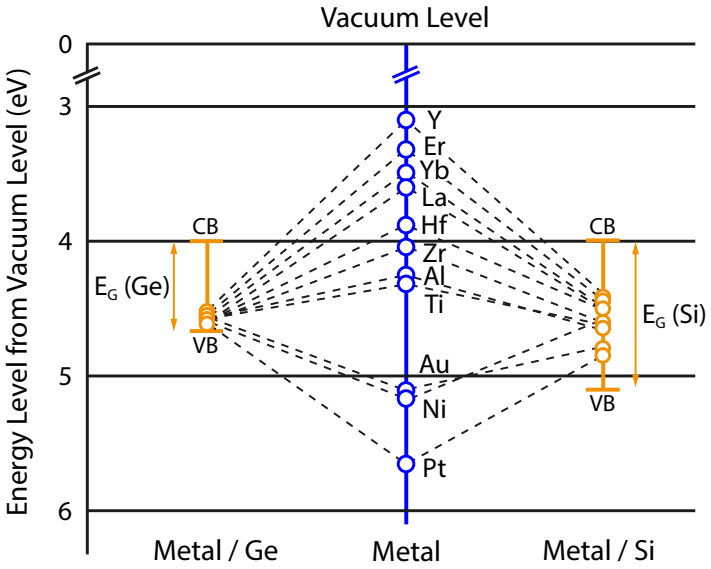

Figure 2.6: *Energy barrier heights for Si and Ge in contact with different metals. The pinning of Ge is located close to the valence band edge. For Si however, the pinning is localized around the band-gap center.*
Adapted from [29, 52, 53]

other hand, the pinning is close to the valence band, thus creating unequally high barriers for both charge carriers. In theory, Si would therefore have the more suitable interface for RFETs, where the charge carrier type is switched during runtime. More details about the interface of the devices fabricated in the scope of this thesis are presented in the Results and Discussion chapter in Section 4.1.1.

2.3.1 Metal-Semiconductor: Contact Formation

This section is highlighting the contact formation between the metal and semiconductor junction as used in the fabrication process in Section 3.1.2.4. The goal is an abrupt and reproducible metal-semiconductor junction possessing a low interface defect density. Therefore, the established Al diffusion technique presented by Wind et al. in [20, 50, 54] is used. As a bonus, the semiconductor segment length can be tailored to specific needs by adjusting the diffusion time. The presented technique only works for metals like Al, which do not form intermetallic phase at the interface [50]. Otherwise, the interfaces defect density increases resulting in a different pinning level and Schottky barrier height, as mentioned in the previous section, Section 2.3.

The metal-semiconductor transitions are formed by a thermally induced exchange process of the Al and the semiconductor, being Si or Ge. Due to the fast self-diffusion of Al, Al is efficiently supplied from the metal source to the semiconductor junction in order to compensate the out-diffusion of Si or Ge. When comparing the diffusion coefficients in

Table 2.3: *Diffusion rates for Al-Si and Al-Ge material compositions. Note the high diffusion coefficient for the semiconductors in Al. Values given for a temperature of $T = 500°C$. Adapted from [50].*

Al in Al $[cm^2s^{-1}]$	**Al in Si** $[cm^2s^{-1}]$	**Al in Ge** $[cm^2s^{-1}]$	**Si in Al** $[cm^2s^{-1}]$	**Ge in Al** $[cm^2s^{-1}]$	**Si in Si** $[cm^2s^{-1}]$	**Ge in Ge** $[cm^2s^{-1}]$
6.3 x 10^{-10}	2.0 x 10^{-22}	3.3 x 10^{-20}	4.4 x 10^{-8}	3.1 x 10^{-9}	6.5 x 10^{-19}	8.4 x 10^{-20}

Table 2.3 it becomes evident that high diffusion rates of Al, Si and Ge in Al cause this behavior. The diffusion of Al in Si and Ge or the semiconductor in itself is slower by about 10 orders of magnitude. A detailed understanding of the diffusion process is elaborated in [54] and the corresponding Al-Si and Al-Ge phase diagrams are shown in the supporting information of [50].
Furthermore, the metal diffusion process retains its elementary composition even for several subsequent annealing steps. Thus, the remaining semiconductor segment length can be decreased step by step. For narrow Al contacts single-elementary contacts are observed [54]. The abruptness of the metal-semiconductor transitions are shown by EDX measurements presented in [50] and in the Results and Discussion in Section 4.1.1.

2.4 Reconfigurable Field-Effect Transistor (RFET)

As addressed in the introduction of this thesis, conventional transistor scaling according to Moore's law [6], slowly but surely reaches physical limits and other concepts need to be taken into account. Considering the IRDS roadmap [3], different approaches are given under the name of *Beyond CMOS* for increasing device functionalities that do not follow Moore's scaling theory. One of these concepts is the reconfigurable field-effect Transistor, or short RFET, treated in this thesis.
This chapter will motivate the RFET concept itself and give an introduction into the working principle and physical requirements needed by referring to the previous chapters. Next, advantages over conventional transistor types are given in Section 2.4.1. The different RFET device architectures are covered in Section 2.4.2 along with a comparison to Schottky barrier Field-Effect Transistors (SBFETs). The electrical transport mechanism is discussed in Section 2.4.3 along with an illustration of the different work modes of RFETs in Figure 2.8.

RFETs increase the functionality of a single transistor by incorporating a unipolar p- and n-type operation mode into one single device. The desired device operation type is electrically selected and is changeable during runtime. Therefore, a semiconductor channel material capable of conducting both charge carriers and posses the capability of filter out the undesired electrons or holes by application of an electrical field to the respective gate, is required.[22].
Thus, an undoped semiconductor is used as channel material, not preferring one charge carrier type over the other due to the mid bang-gap fermi level. Schottky barriers with

similar heights for both holes and electrons are required for the mentioned filtering of the unwanted charge carrier, covered in Section 2.3 about metal-semiconductor junctions and the formed contacts and fermi level pinning. Thereto, abrupt and reliable metal-semiconductor interfaces are equally important. A fabrication technique fulfilling these requirements is treated in Section 2.3.1, describing the metal-semiconductor exchange process. The desired operation type is selected by the application of an electrical field to top-gates located above the Schottky barriers. In order to prevent an unwanted leakage current, an isolating layer between the conducting channel and top-gate electrodes is indispensable. Therefore, dielectrics as stated in Section 2.1.2 are used, featuring different interface qualities as discussed in Section 2.1.2.1 comparing Si to Ge oxide. Insulating layers with higher relative permittivity can improve the electrical control and reduce unwanted tunneling currents. A further improvement in controllability is accomplished by using semiconductor on insulators as mentioned in Section 2.2.

The first Si based RFET concept was introduced by H.C. Lin et al. [55] in 2000 as a way to suppress undesired off-states currents in TFETs and was further improved by Heinzig et al. [21] in 2011. The later device concept thereby consists of a Si nanowire with intruded $NiSi_2$ contacts [56] and two top gates, each overlapping one Schottky barrier. Since then a variety of different material systems, comprising Si and Ge as channel semiconductor, and fabrication techniques, as bottom-up grown nanowires and top-down fabricated nanosheets, have improved the reliability and reproducibility of RFETs [15, 55, 57, 58]. An additional material composition with a novel material stack is presented in the Results and Discussion chapter, Chapter 4 of this thesis, based on previous work by Fuchsberger et al. [29, 59, 60].

2.4.1 Advantages of RFETs

This section highlights the advantages of RFETs in comparison to conventional CMOS transistors. Starting with the channel material, for CMOS transistors usually a doped semiconductor, depending on the majority charge carrier type, is used, which implies the presents of foreign atoms. For RFETs (and SBFETs) however, the channel is undoped and therefore free of impurity atoms. At decreasing scales, reliable doping becomes more challenging and results in increased impurity-scattering [22].

As the name reconfigurable FET suggest, RFETs can change from p- to n-mode or vice versa during runtime, depending on the wanted operation type. The advantage becomes even more apparent when considering logic blocks or whole circuits as discussed in [15]. Not only can the total transistor count be reduced significantly, but also the responding delay [61]. RFETs with multiple control-gates can be used as wired logic devices, possessing wired AND or NOR logic functionalities as demonstrated in [62] and Section 4.3.4 of this thesis.

As a result of the runtime switching and interchanging functionality of RFET circuit designs, hardware security is increased [63]. By so-called NAND/NOR obfuscation, circuits are made physically uncloneable [63]. Thus, the listed advantages arise not only from the selected material and its metal-semiconductor junction, but also from the circuit design and desired functionality.

2.4.2 RFET Architecture

RFETs can be manufactured using a wide variety of fabrication techniques, ranging from bottom-up nanowires [64] or top-down nanosheets [58], and materials like Si [56] and Ge [65], but the basic working principle remains the same: One single device which can be dynamically configured for either p- or n-mode operation during runtime. This chapter will give an overview of the different top-gate arrangements, shown in Figure 2.7, and discuss its influence on the electrical device behavior. First however, there is a discussion of what an RFET is made of and what properties are required.

The concept of an RFET is based on two metal-semiconductor junctions and a channel region, along with top-gates enabling the electrostatic control of these regions. Since the RFET should conduct both holes and electrons, represented by a p- or n-mode, equally well, a suitable material system is required. Therefore, the channel itself must be able to allow the flow of holes and electrons. This is the case for semiconductors with a fermi level close to the middle of the band-gap, like for intrinsic, undoped Si or Ge, see Section 2.1.1. Beside the channel material, the metal-semiconductor junctions are essential for RFETs. Yet again, a good conductivity for both holes and electrons is needed. As discussed in Section 2.3 this need is fulfilled for a mid band-gap pinning. Hence, the wire, being a nanowire or nanosheet, consists of a metal-semiconductor-metal assembly, depicted in Figure 2.7 in blue and orange. By adding top-gates, one charge carrier is preferred, putting the device either in p- or n-mode. Only a suitable combination of all material properties result in proper RFETs, in respect to the evaluation requirements mentioned in Section 3.2.2.

The before mentioned different device architectures refer to various top-gate arrangements which are illustrated in Figure 2.7 for a STG (a), DTG (b), TTG (c) and 4TG (d). Note that p-mode or p-type operation refers to an upward band bending enabling the free passage of holes (h+), whereas n-mode or n-type operation indicates a downward bending allow the flow of electrons (e-). The naming is based on its FET counterparts.

A STG has, as the name single top-gate suggests, one single top-gate (TG) covering the whole channel region along with both metal-semiconductor junctions. As a result, the whole semiconductor as well as the injection barriers at source and drain are controlled by one top-gate resulting in an ambipolar behavior without distinct p- and n-modes. This behavior and top-gate geometry are an analogy to a Schottky barrier FET (SBFET), however in the context of RFETs the term STG is used [66].
By adding another top-gate over one metal-semiconductor junction, one branch of the

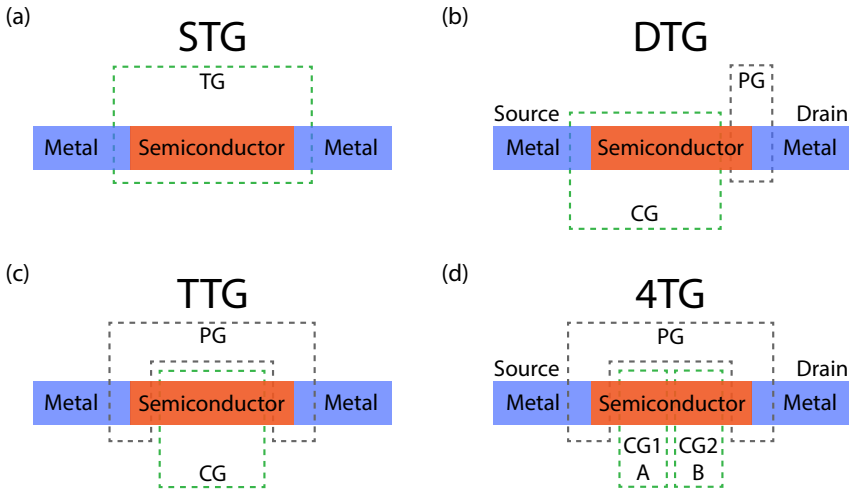

Figure 2.7: *Illustration of the top-gate arrangements of a STG, DTG, TTG and 4TG. Note the wide control-gate (CG) for the DTG and the physically connected polarity-gates for the TTG and 4TG. Source and drain are labeled for the geometrically asymmetric devices.*

originally ambipolar behavior is suppressed, hence making the device polar. A dual top-gate or DTG is created. This gate is therefore baptized polarity-gate or PG along with the control-gate (CG), covering the remaining channel region and metal-semiconductor junction. However, this makes the architecture geometrically and electrically asymmetric. For all devices presented in this thesis, the polarity-gate was placed of the drain metal-semiconductor junction, as shown on Figure 2.7 (b). This has the benefit of a positive bias for the n-mode and a negative bias for the p-mode along with same sign control-gate and polarity-gate voltages, as its MOSFET counterparts. A polarity-gate at source would result in a flipped bias direction. What happens if the bias direction is not changed, is discussed in the next section about the electrical transport mechanism, Section 2.4.3.
A second polarity-gate overlapping the other semi-conductor junction gives a triple top-gate or TTG depicted in Figure 2.7 (c). The polar behavior of the DTG is preserved and enhanced by the addition of another polarity-gate and the ability to modulate both injection barriers separately of the control-gate. By physically connecting the two polarity-gates overlapping the junctions the top-gate arrangement becomes geometrically and electrically symmetric and bias direction independent. Source and drain can thus be chosen freely. All TTG devices covered in this thesis had this physical connection of the two polarity-gates, due to the limited amount of probe needles connected to SMU at the used measurement station discussed in Section 3.2.1.
Adding a second control-gate between the polarity-gates results in a 4TG design, presented in Figure 2.7 (d). This top-gate arrangement is by design not electrically asymmetric, however by labeling the left control-gate CG1 or A the device became asymmetric in terms of its input selection. The further addition of control-gates would result in 5TG, 6TG and so forth architectures.

Although, the STG and TTG design are geometrically and electrically symmetric, source and drain were chosen in accordance to the top-gate arrangement made for the DTG and 4TG device, where source is on the left, drain on the right.

The different device architectures presented above not only differ from each other in terms of their geometry, but also in their electrical behavior. A comparison between an STG, DTG and TTG is shown in Figure 4.4, at equal bias and top-gate voltages. The transfer measurements are shown on a semi-logarithmic plot, with the absolute drain current $|I_D|$ along with the absolute top-gate leakage currents, $|I_{TG}|$, $|I_{PG}|$ and $|I_{CG}|$, on the ordinate (denoted with $|I_{TG/D}|$) and the top-gate or control-gate voltage on the abscissa (denoted with V_{CG}). The respective polarity-gate voltages for p- and n-mode are labeled in the top left and right corner. Note, that the bias is set to $V_{DS} = 2V$ and applied in a symmetric fashion for the STG and TTG. For the DTG however, the bias is applied asymmetrically and with a flipped direction for the p-mode branch, as discussed in the next section, Section 2.4.3 and in Section 3.2.1.2.

As mentioned above, the STG only has one single top-gate covering the whole channel region and overlapping both metal-semiconductor junctions at drain and source. Therefore, the entire band is moved at once (discussed in Section 2.4.3), resulting in an ambipolar behavior as shown in Figure 4.4 in blue, with no distinct p- or n-mode as its multi top-gate counterparts.
For architectures with two top-gates, as the illustrated DTG in Figure 2.7 with the polarity-gate at the drain metal-semiconductor junction, explicit p- and n-modes are observed in Figure 4.4 in red. The corresponding transport mechanism and band diagrams are discussed in Section 2.4.3 and Figure 2.8.
For a TTG architecture with two polarity-gates over each metal-semiconductor junction and one separate top-gate covering the remaining channel, the transfer characteristic also exhibit a controllable p- or n-mode, depicted in Figure 4.4 in black.

As seen in Figure 4.4 each architecture has its own benefits and drawbacks, hence making the RFET concept even more versatile by the ability to tailor the top-gate geometry to the desired application. The ambipolar character is unique for the STG design and results in no explicit off-state region however an lowest current point which will be referred to as off-state. The DTG architecture possesses distinct p- and n-mode regions, with on-state currents and threshold voltages V_{th} close to the STG. As the DTG, the TTG also possesses a distinct p- and n-mode branch, however with a typically higher on-state current at the cost of a lower threshold voltage V_{th}. This shift in the threshold voltage and increase in current is explained in the next section covering the electrical transport mechanisms, Section 2.4.3.

2.4.3 Electrical Transport Mechanism

In this section the electrical transport mechanism for different RFET architectures introduced in the previous section, Section 2.4.2, will be explained by the corresponding energy band diagrams [28].

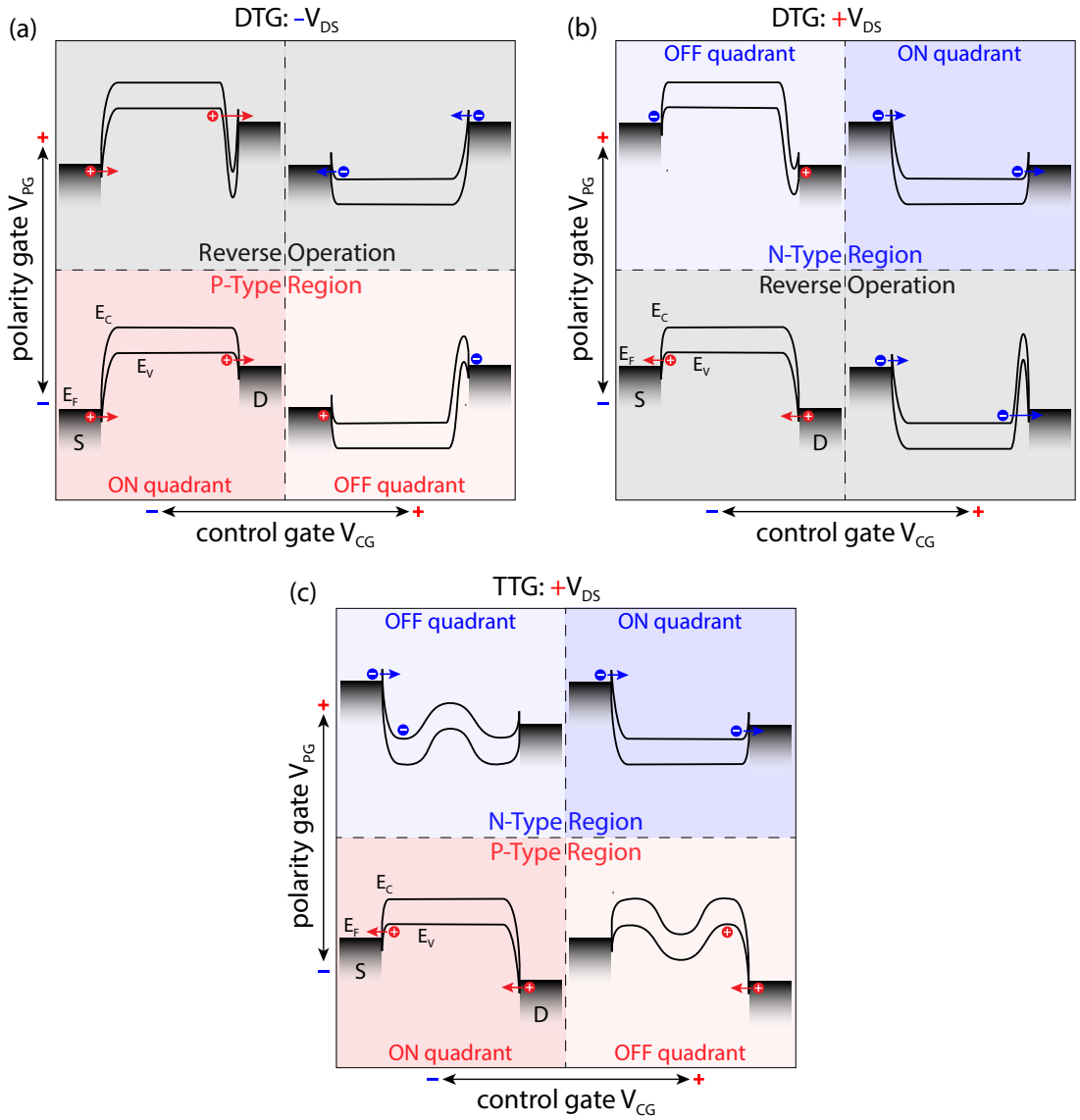

Figure 2.8: *Operating regions depending on the applied control- and polarity-gate voltage with corresponding band diagram of a DTG, in backward (a) and forward (b) bias direction, and a TTG (c). Dashed lines at V_{PG} separate the p- and n-mode regions, while dashed lines at V_{CG} mark the separation of on- and off-state quadrants. Red and blue circles represent holes and electrons respectively, along with their moving direction, indicated by arrows. Note the different bias directions for the DTG in (a) and (b) and corresponding shift of the drain and source potential. For (c), the TTG, the bias direction is set to a positive value.*

Figure 2.8 shows the different operation regions of a DTG with a neg. (a) and pos. bias (b) and a TTG in (c) at varying control- and polarity-gate voltages and bias direction. Corresponding sketches of the band diagrams are depicted in each in quadrant, illustrating the transport mechanism along with the charge carrier type. For the off-current quadrants the charger carrier transport is prevented by a control-gate controlled mid-channel barrier or a polarity-gate controlled injection barrier at the metal-semiconductor junction.

As mentioned in Section 2.4.2, introducing the different RFET architectures, a TTG has three top-gates, including two physically connected polarity-gates over the metal-semiconductor junctions along with one control-gate over the remaining channel region. This geometrical symmetry makes the TTG bias direction independent. Therefore, the transport mechanisms can be explained by the forward/positive bias direction as shown in Figure 2.8 (a). In case of a negative bias direction, the band diagrams are mirrored vertically, while the drain and source location stay the same.
Figure 2.8 (c) can be separated into two regions, a p-type region for negative polarity-gate voltages or a n-type region for positive polarity-gate voltages, in analogue to a conventional p- or n-channel FET. For RFETs however, these regions are usually termed p- or n-mode region. Depending on the applied control-gate voltage in the respective region, either an on- or off-state is reached, denoted with on- and off-quadrants in Figure 2.8. For same sign polarity- and control-gate voltages an on-state is reached. For the case of a positive polarity- and control-gate, the TTG is configured for n-mode operation and is located in the first quadrant or n-mode on-state quadrant. The overall band diagram is bent downward, resulting in transparent injection barriers and no channel barrier. Electrons, as the majority charge carrier in that configuration, can flow freely from source to drain, as indicated by the blue circles and arrows. However, if the control-gate voltage is flipped to negative voltages, a mid channel barrier is induced, effectively blocking the flow of electrons, as depicted in the second quadrant. For negative polarity-gate voltages the same holds true, however the band diagram is bent upward, allowing the flow of holes, represented by red circles.

The simplest device architecture, consisting of just one top-gate covering both the semiconductor junctions and channel region, is the STG. Due to the single gate atop the whole band is bent simultaneously, modulating the injection barriers and channel region at once. The corresponding STG band diagram can be adapted from its triple top-gate counterparts, shown in Figure 2.8 (c) at equivalent polarity- and control-gate voltages $V_{PG} = V_{CG}$, effectively resulting in an STG with narrow and negligible ungated regions in between the individual gates. Therefore, the corresponding band diagrams of an STG are shown in quadrant 1 and 3 of Figure 2.8 (c), for the flow of electrons and holes respectively. Note, that for STGs it can be assumed that an effective blocking of charge carriers is never reached, resulting in an overlapping transition from electron to hole current and vice versa. This assumption is motivated by the high off-state point current presented in Figure 4.4.

A DTG, consisting of only one polarity-gate overlaping the drain-sided metal-semiconductor junction and one control-gate stretching over the remaining channel region and the source-sided junction which results in an geometrically asymmetric top-gate arrangement, as discussed in Section 2.4.2. This asymmetry makes the DTG bias direction dependent. Therefore, band diagrams for a negative/backward and positive/forward bias direction are shown in Figure 2.8 (a) and (b) respectively. Note, that the location of source and drain is not exchanged in the sketches.

Considering the DTG band diagram shown in Figure 2.8 (b), for a device biased in forward direction, the band diagram of quadrant 1, for same and positive sign polarity- and control-gate voltages, illustrates the on-state of the n-mode. For the same polarity-gate however along with a flipped sign control-gate voltage, the device is put into off-state, effectively blocking both the injection of electrons and holes at the two Schottky barriers, as depicted in the second quadrant. The DTG band diagram in this quadrant is thereby different to the TTG counterpart, as the control-gate stretches over the source-side metal-semiconductor junction and the channel area, resulting in an overall lifted band except for the region under the polarity-gate. The third quadrant, set by both negative polarity- and control-gate voltages, indicates the same electrostatic situation as for the previously mentioned TTG, with a hole conduction from drain to source. Quadrant four on the other hand does not effectively block the flow of charge carriers as expected. In order to fully understand the involved transport mechanisms in this quadrant, further measurements and simulations need to be carried out and were not part of this thesis. However, the following paragraph is going to give possible explanations, which were also considered in the analysis made in Chapter 4, discussing the respective measurement results.

One possible explanation for the observed current flow of the presented DTG device configuration shown in Figure 2.8 (a) quadrant two or (b) quadrant four is the depicted band-to-band tunneling [67]. Thereby the respective charge carrier quantum-mechanically tunnels through a thinned barrier, consisting of the strongly bent band diagram, to the opposite band either directly or via intermediate trap states inside the band-gap [68]. However, the tunneling probability strongly depends on the barrier thickness and therefore the band bending induced by the control- and polarity-gate along with the respective spacing in between the two gates [49]. Moreover, stray charges or traps further screen the applied potential, resulting in a lower overall bending. Another possible interpretation is also based on the depicted band bending and the thereby resulting potential *pockets*, induced by the polarity-gate. This suggests a gradual filling of the pockets with charges and results in an effective lowering of the barriers and pockets. Furthermore, opposing sign charges accumulate at the left-hand side of the barrier, further reducing the relative barrier height. This process comes to hold when an equilibrium is reached and could result in a constant flow of charge carriers along with electron-hole pair recombination [49].

For TTG designs with individually controllable polarity-gates, TTGs are able to achieve a similar characteristic as the presented DTGs, by varying the drain or source polarity-gate simultaneously with the control-gate for forward of backward biased devices respectively. This could not be tested on the devices fabricated in the scope of this thesis, because of the physical connection of the polarity-gates, but is presented in literature and referred to as low/high V_{th} mode TTG in [69].

As discussed in the paragraph above, DTG devices will be measured with a positive/forward bias for the n-mode and a negative/backward bias for the p-mode. This configuration is also highligthed in Figure 2.8 (a) and (b) by the red and blue p- and n-type regions. A further discussion about the bias direction and symmetry is also given in the next chapter concerning the measurement techniques in Section 3.2.1.2.

Corresponding measurements over varying polarity- and control-gate voltages are introduced in Section 3.2.5 as polarity-gate characterization, of the next chapter and can be directly mapped to respective band diagrams illustrated in Figure 2.8.

Chapter 3

Experimental Techniques

The goal of this thesis is the fabrication and detailed electrical characterization of Ge RFETs, fabricated in a top-down approach based on molecular beam epitaxy (MBE) grown Ge on either strained or unstrained SOI substrates. The theoretical background of RFETs including the importance of the metal-semiconductor junction was given in Sections 2.3 and 2.4, respectively. The following chapter will introduce the fabrication process used to fabricate RFETs (Section 3.1) and give an overview of the different electrical characterizations techniques (Section 3.2).
The first Section 3.1.1 will start with an introduction to the base-substrate, out of which the RFETs are fabricated according to the fabrication process described in Section 3.1.2. Starting off with the plain wafer stack, the process begins with the nanosheet patterning and oxidation, followed by the Al drain and source deposition along with the Al-Ge exchange, finishing with the deposition of the top gates.
The electrical characterization methods are outlined in Section 3.2 starting with a specification of the measurement setup and procedures in Section 3.2.1. Followed by Section 3.2.2, listing a series of device characteristics extracted from the characterization techniques described in Sections 3.2.3 to 3.2.6 and 3.2.8, like the transfer measurement. In the last section the automated evaluation script is described regarding its output and capabilities. The evaluation results presented in Chapter 4 are extracted with the aforementioned script.

3.1 Fabrication of Germanium Based RFETs

This section is devoted solely to the sample fabrication and will delineate the processing steps that need to be taken from the plain base-substrate, described in Section 3.1.2.1, to a finished RFET in Section 3.1.2.5. In the first section, Section 3.1.1, the used base-substrate is introduced as well as the needed fabrication steps in order to arrive at the wafer stacks depicted in Figure 3.1. Unique for these substrates are the $10nm$ thick layers

of pure Ge, which are grown atop of a silicon on insulator (SOI) or strained silicon on insulator (sSOI) wafer. These wafer stacks are further processed in a top-down approach, in order to fabricate RFETs out of these, as described in Section 3.1.2. An overview of the process steps that have to be carried out in sequence are shown in Figure 3.3 and is described in the equally named and numbered Sections 3.1.2.1 and 3.1.2.5. The sample is furthermore visualized in Figure 3.3 (a) to (i) at different stages during the process along with a cross section of a fully processed TTG in Figure 3.4.

3.1.1 Strained and Unstrained Silicon on Insulator Base-Substrate

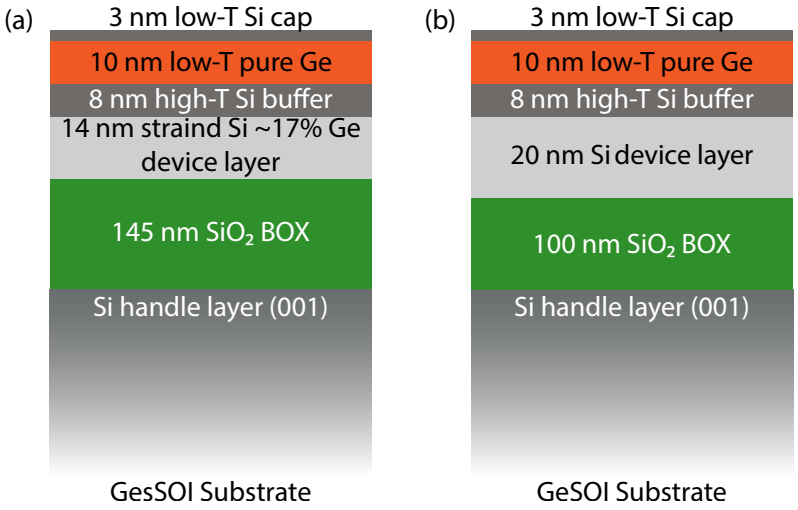

Figure 3.1: *Illustration of the used substrate stack as cross section. The main difference between the two substrates is in the composition and thickness of the respective device layer. The strained silicon on insulator (sSOI) substrate shown in subfigure (a) possesses a strained Si device layer and is hence named Ge on sSOI (GesSOI) whereas the device layer on the silicon on insulator (SOI) substrate is pure Si and not stressed given it the name Ge on SOI (GeSOI), depicted in subfigure (b).*
Layers not to scale.

The base-substrate for all fabricated RFETs covered in this work are either a sSOI or SOI stack, outlined in Figure 3.1 (a) and (b), respectively. The according wafer stack consist of a strained or unstrained SOI wafer and MBE grown Si, Ge and Si layers on top. The mentioned sSOI wafer consists of a Si handler layer with (001) orientation with a $145nm$ thick SiO_2 buried oxide (BOX) and a $14nm$ strained Si layer atop, shown in the lower three layers of Figure 3.1 (a). The strained Si layer was grown on top of a relaxed silicon-germanium layer with an Ge content of approx. 17% ($Si_{83}Ge_{17}$), resulting in a lattice mismatch, see Table 2.1 and is therefore subjected to in-plane tensile stress. After growth the strained Si layer was transferred to the depicted SOI wafer, resulting in a Ge free wafer-scale strained Si device layer [70, 71]. This lattice mismatch is consequently needed in order to grow thicker Ge layers without excessive defect formation or delamination in the worst case. However, by reducing the process temperature during MBE growth, thicker layers are depositable, despite the existing lattice mismatch [45, 72]. On top of

the strained layer a $8nm$ Si buffer, and a $10nm$ Ge along with a $3nm$ Si capping layer are grown with MBE.
The SOI based substrate depicted in Figure 3.1 (b) on the other hand, possesses an overall thinner BOX, a $20nm$ thick pure Si layer without Ge, an $8nm$ thick Si buffer and the pure Ge layer capped with a $3nm$ thick Si layer on top. Note that the layers in the illustration of the cross section of Figure 3.1 are not true to scale.

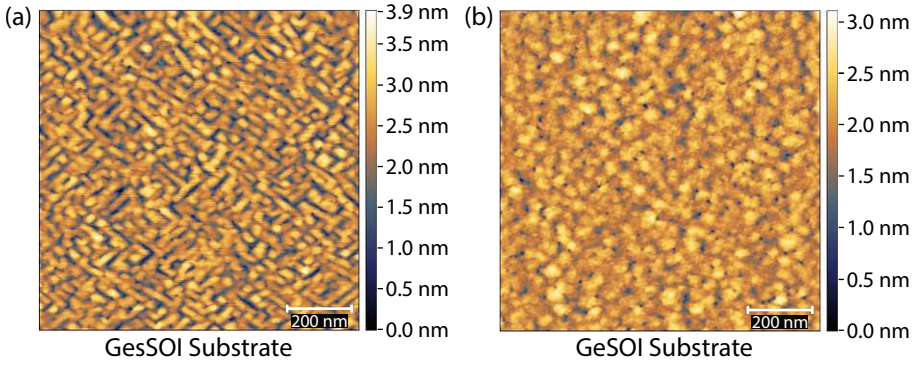

Figure 3.2: *AFM measurements of the GesSOI (a) and GeSOI (b) substrate before processing, showing the surface topography of the corresponding Si capping layer. The root-mean-square (RMS) surface roughness (row alignment with a polynomial-5 fit) is $S_q = 487pm$ for the GesSOI substrate and $S_q = 287pm$ for the GeSOI substrate. Note the different scale for each measurement.*
The AFM measurements were performed by Enrique Prado Nvarrete and Johannes Aberl at Johannes Kepler UniversitÃ¤t (JKU) in Linz.

The layers are grown in a Riber SIVA-45 MBE chamber after a cleaning procedure including a hydrofluoric acid (HF 1%) dip in order to remove the native oxide. The $10nm$ thick Ge layer along with the $3nm$ Si capping layer were deposited at $T = 250°C$, hence the supplementary *low-T* in Figure 3.1. The corresponding AFM measurements of the GesSOI and GeSOI substrate are illustrated in Figure 3.2 (a) and (b), respectively. Thereby, the different surface morphologies of the two substrates is evident along with the overall smoother surface of the GeSOI stack, despite the large lattice mismatch. Furthermore, no indication of pinholes or other dislocations are visible for both material systems, even on large scan areas. Further details about the manufacturing process are to be published by C.Wilflingseder et al., but were not available at the time of writing this thesis. Similar work considering the growth of thick SiGe layers has been published in [45].

3.1.2 Fabrication Steps: From Nanosheet to Top-Gates

Having introduced the base-substrate stacks in the previous section, Section 3.1.1, out of which the nanosheets are structured in a top down fashion, this section will cover the fabrication process, as depicted in Figure 3.3. Section 3.1.2.1 starts with the definition of the nanosheet and the removal of excess material surrounding it. Followed by Section 3.1.2.2, covering the growth or deposition of the gate dielectric, which is either SiO_2 or SiO_2/ZrO_2. Next in Section 3.1.2.3, the source and drain pads are defined along with a connection of these to the nanosheet. Subsequently, the Al-Ge exchange process is discussed in Sec-

tion 3.1.2.4. As a last step, the metal top-gates are placed over the metal-semiconductor junctions and on top of the remaining Ge channel region. The fabrication process is also visualized in Figure 3.3 (a) to (i), showing the device at different stages during the process-flow. A cross section of a resulting TTG device is shown in Figure 3.4.

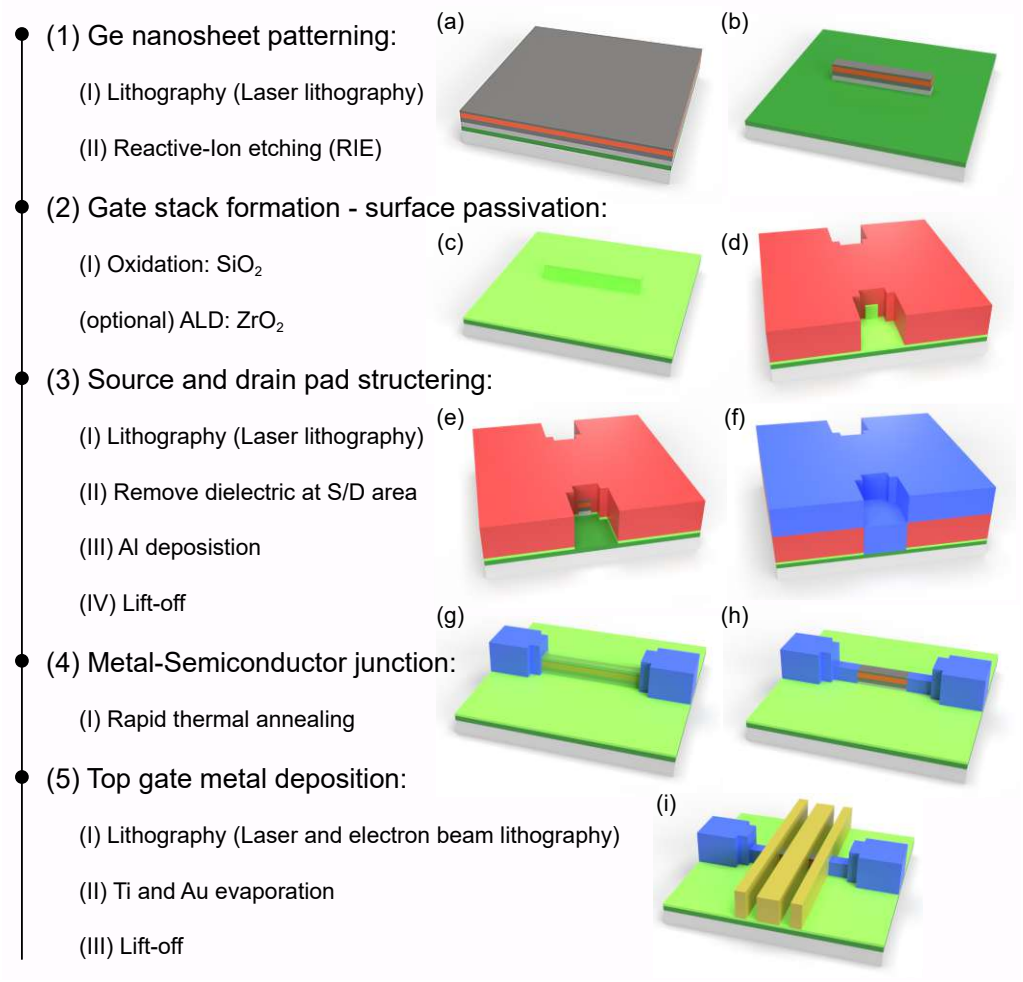

Figure 3.3: *Fabrication process steps with illustrations of the sample at different stages during fabrication.*
The illustrations in subfigure (a) to (i) were adapted from [29].

3.1.2.1 Nanosheet Patterning

The first fabrication step mentioned in Figure 3.3 is the formation of the nanosheets in a top-down approach. As the name already says, the nanosheets a defined from the top downward in order to making use of the underlying material stack of the base-substrates shown in Figure 3.1. This fabrication step can be divided into two parts, namely a lithography step and sequential reactive-ion etching (RIE), as written in Figure 3.3 (1).

The lithography step itself can further be separated into three parts which all comprise the photoresist, namely the resist application, resist exposure and resist development. The sample, which only consists of the base-substrate at this point, as illustrated in Figure 3.3 (a), is first cleaned, than an image reversal photoresist (AZ5214) is spun on and softbaked at $100°C$ for $60s$. Afterwards, the photoresist exposed, which is done by a laserwriter (HIMT MLA150) with a dose of $140J/cm^2$. The defined nanosheets are $10\mu m$ long and $700nm$ wide, however the width is decreased by optical effects and under-etching, resulting in widths between 350 to $500nm$. Furthermore, the nanosheets are not just strait lines, but have larger areas at the ends. This results in a larger interface areas of the Ge and the later fabricated Al drain and source pads, as discussed in Section 3.1.2.3, and provide a more reliable Al diffusion for the hetero-junction formation described in Section 3.1.2.4. After exposure, the photoresist is developed in developer (AZ726MIF) for $17s$ and rinsed with water afterwards.

Next, the defined nanosheet is released from the stack by RIE (Oxford Instruments PlasmarPro100 Cobra) with SF_6/O_2 for $50s$, removing the surrounding layers of Si and Ge down to the BOX. The residual resist on the sample is removed by plasma incineration (Pink V10-G) for $300s$ at $300W$, followed by rinsing with acetone and isopropanol.

The current state of the sample is illustrated in Figure 3.3 (b), showing one freestanding nanosheet with the initial stack from the base-substrate down to the BOX. This first fabrication step is the same for all samples presented in this thesis, since it is independent of the used base-substrate and the later applied dielectric.

3.1.2.2 Gate Stack Formation

The nanosheets fabricated in the previous step require a dielectric layer, in order to electrically separate the conductive channel from the top-gates, which will be fabricated in the last fabrication step in Section 3.1.2.5. The fabricated gate stack consists of either a SiO_2 layer or a SiO_2 with a ZrO_2 layer atop, making this the only fabrication step in which the samples introduced in the results and discussion chapter in Chapter 4 differ from each other. The deposited dielectric layer(s) cover the whole wafer, as depicted in Figure 3.3 (c) in light green. However, it has to be mentioned, that the exposed Ge on the sides of the nanosheet, illustrated in Figure 3.3 (b) in gray and orange, also oxidize. A homogeneous coverage of the nanosheet top and sides with high quality SiO_2 is desirable, since the top-gate metal wraps around the sheet. Nativity a Ge oxide layer will form on the exposed Ge sidewalls, which is preferably overgrown with a SiO_2 layer from the Si capping and Si buffer layer.

The SiO_2 layer is grown for each device, no matter if a high-k dielectric is grown on top, because of the superior electrical property mentioned in Section 2.1.2 along with reduced interface states if compared to a Si or Ge/ZrO_2 interface [73]. This is also the reason for

the Si capping layer, shown in dark gray in Figure 3.1, out of which the SiO_2 is formed and to prevent the formation of Ge oxide with a rather poor electric behavior as discussed in Section 2.1.2.1.

The omega-shaped SiO_2 passivation of the Ge nanosheet is formed by dry thermal oxidation at 900°C for $180s$, resulting in an approximately $5nm$ thick SiO_2 layer. The thickness may vary for each sample and was estimated with another test sample, which was oxidized at the same time. The ZrO_2 is deposited by ALD with TDMA-Zr and H_2O as precursor gases and N_2 as carrier at an reactor temperature of $250°C$. The exact amount of cycles and the estimated thickness, again measured on a test sample, are given in Section 4.2.1.

3.1.2.3 Source and Drain Deposition

The formation of the source (S) and drain (D) pads is discussed in the third fabrication step shown in Figure 3.3. This process step can be split into four parts, consisting of a lithography step, define the S/D pad regions, the removal of dielectric in the S/D pad area, the deposition of Al and finally the lift-off where the excess metal is removed.

The lithography process is similar to the one used for the nanosheets in Section 3.1.2.1, however this time the desired S/D pad regions are exposed and developed, as illustrated in Figure 3.3 (d). The nanosheet is however still covered by the dielectric layer, shown in light green, which is removed in the next step either by wet chemical or physical etching, depending on the used dielectric. Only if the dielectric is removed completely, a good interface between the Al S/D pads and the Ge channel is formed. For samples with a SiO_2 dielectric the oxide is removed by a HF-dip in buffered HF (BHF 7:1). This process can however not be used for samples with ZrO_2 layers, due to low etch rates. Therefore the ZrO_2 and underlying SiO_2 layer are etched physically by RIE with SF_6/Ar. Due to the low selectivity of physical etching in comparison to wet chemical etching a well established process is needed, in order to not etch away parts of the contacting area of the nanosheet. The desired etching result is shown in Figure 3.3 (e) with an exposed nanosheet, in comparison to (d) before the etching.

The third part is the deposition of Al. Therefore, $125nm$ of Al are sputtered (Creavac CREAMET) over the whole sample as depicted in Figure 3.3 (f) in blue. Last but not least the underlying photoresist, shown in Figure 3.3 (f) in red, is removed by a lift off process in acetone. Thereby the access Al on top of the resist is also removed, resulting in S/D pads on top of the BOX which contact the nanosheet, as illustrated in Figure 3.3 (g).

3.1.2.4 Metal-Semiconductor Junction Formation

As discusses in the theory Section 2.4 of the RFET, a reproducible and reliable, abrupt metal-semiconductor junction is needed and can be realized by Al-Ge diffusion as described in Section 2.3 and [50, 54, 74]. This brings us to the fourth step in our fabrication

process in Figure 3.3, the formation of the metal-semiconductor junction by thermally induced diffusion. Therefore, a rapid thermal annealing (RTA) system heats up the sample to $500°C$ in a forming gas (N_2-H_2) atmosphere. The duration depends on the desired Ge segment length, depicted in Figure 3.3 (h), which should remain after the annealing step or in other words, which should not be replaced by Al. If the duration is chosen too long, the entire nanosheet is exchanged with Al. To prevent this from happening, subsequent annealing steps, which do not influence each other, as discussed in Section 2.3, are performed with an intermediate optical examination of the Ge segment. The diffusion is made more reliable, due to the bigger Al/Ge interface areas mentioned in Section 3.1.2.1.

After the desired Ge length is reached, the locations of the Al-Ge interfaces are measured optically, because the top-gates fabricated in the next step, in Section 3.1.2.5, must be placed over those, to enable good electrical controllability as discussed in Section 2.4. The Ge segment width is furthermore needed for the calculation of the current density. For the samples presented in this thesis the Ge segment lengths vary between $700nm$ to $3.5\mu m$ for annealing durations between $180s$ to $250s$. Note that this process is independent of the gate dielectric and therefore the same for all presented samples.

3.1.2.5 Top-Gate Metal Deposition

The last step in the process flow illustrated in Figure 3.3 is the fabrication of the omega-shaped Ti/Au top-gates, which were fabricated atop of the Al-Ge-Al heterostructures, using a combination of laser lithography, electron beam lithography, Ti/Au evaporation and lift-off techniques.

The different device architectures, introduced in Section 2.4 of the RFET chapter, require one, two, three or four top-gates. Depending on the necessary resolution either laser lithography or electron beam lithography (EBL) is used. For devices with one top-gate (STG) the laser lithography is used with the same procedure as introduced in Section 3.1.2.1 of the nanosheet patterning. For devices with more than one top-gate (DTG, TTG and 4TG) the polarity-gate needs to be placed precisely over the Al-Ge junction, in order to manipulate the injection barrier efficiently. These requirements can no longer be met by laser lithography reliably. For that purpose, an EBL (Raith e-LiNE) is used, possessing a high resolution for smaller structures at the expensive of a longer write time. For EBL a polymethylmethacrylat (PMMA) resist (AR-P 679.04) and a suitable developer are used. The other process steps, like the spin coating of the resist and lift-off of the excess metal, are the same for both laser lithography and EBL.

After development, $10nm$ of titanium (Ti) and $100nm$ of gold (Au) are deposited via electron-beam evaporation (Plassys meb550s) over the whole sample, on top of the dielectric layer which also surrounds the nanosheet as indicated in Figure 3.3 (g). Note, that the channel work function will be set by the $10nm$ thick Ti layer, covering the channel oxide. Au on the other hand, will result in better electrical contacts, since the probing needles are also made out of Au. The lift-off process removes the underlying resist and

excess metal, resulting in a finished device as shown in Figure 3.3 (i). It has to be pointed out that in Figure 3.3 (i) and Figure 3.4 both Ti and Au are shown as one yellow layer, in both cases for a TTG architecture.

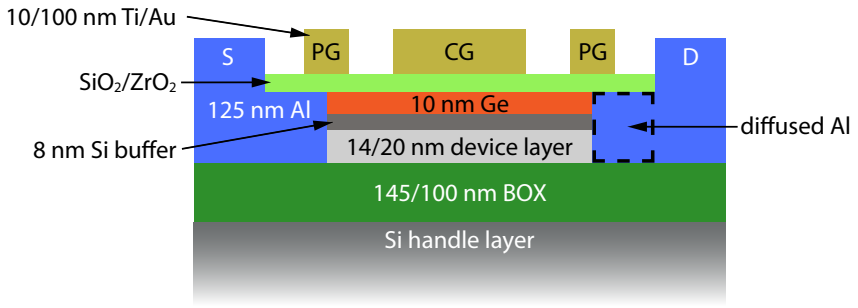

Figure 3.4: *Illustration of a fabricated RFET as cross section, with thicknesses and materials of each region. Shown for a TTG with two polarity-gates (PG) and one control-gate (CG). Layer thicknesses not to scale.*

In Figure 3.4 a sketch of a TTG cross section is illustrated, possessing two polarity-gates overlapping the Al-Ge junctions and one control-gate over the remaining Ge segment. Furthermore, the described Al-Ge diffusion, discussed in Section 2.3 of the theory chapter, is highlighted by a dashed black box, showing the exchanged area. It also has to be pointed out that, the Si capping layer is fully oxidized away, as described in the respective fabrication step in Section 3.1.2.2. This becomes evident when comparing the cross sections of the base-substrate shown in Figure 3.1 and of the fabricated RFET in Figure 3.4.

A fabricated sample, following the steps mentioned in this section, consists of 60 individually controllable RFET devices possessing different architectures. The typical number of STGs, DTGs, TTGs and 4TGs of each fabricated sample are given in Table 4.2. Thereby, the exact number and location on the chip varied from sample to sample, due to slightly different Ge segment lengths of each device. Shorter Ge segments were used for STGs, intermediate segments for DTGs and TTGs and long ones for 4TGs.

3.2 Electrical Characterization

In the previous section, Section 3.1, the used fabrication process was discussed along with the fabrication differences for each sample. The following section will cover the electrical characterization methods for RFETs and outline differences to conventional MOSFET characterization. First the used measurement setup in Section 3.2.1 is described along with typical measurement settings which were taken for the electrical measurements. Followed by a review of key aspects for RFET devices in Section 3.2.2. How these individual features are extracted and identified from the electrical measurements are described in the individual sections of each measurement technique from Section 3.2.3 to 3.2.8. Last but not least, the calculations of the automated analyses-script are covered in Section 3.2.9.

The used measurement techniques for the characterization of the nanosheet RFETs are based on the Book *Semiconductor Material And Device Characterization* by D.K. Schroder [75].

3.2.1 Measurement Setup

For all measurements presented in this thesis one and the same measurement setup was used, consisting of a Keithley 4200-SCS semiconductor characterization system in combination with four source measurement units (SMUs), a Cascade Summit 11000 AP four arm needle prober, shown in Figure 3.5 (a), an optical microscope along with a heat-/cool- and moveable stage which was regulated by a ERS Electronic SP72 300 temperature controller, crucial for the temperature investigations presented in Section 4.3 of the Results and Discussion chapter.

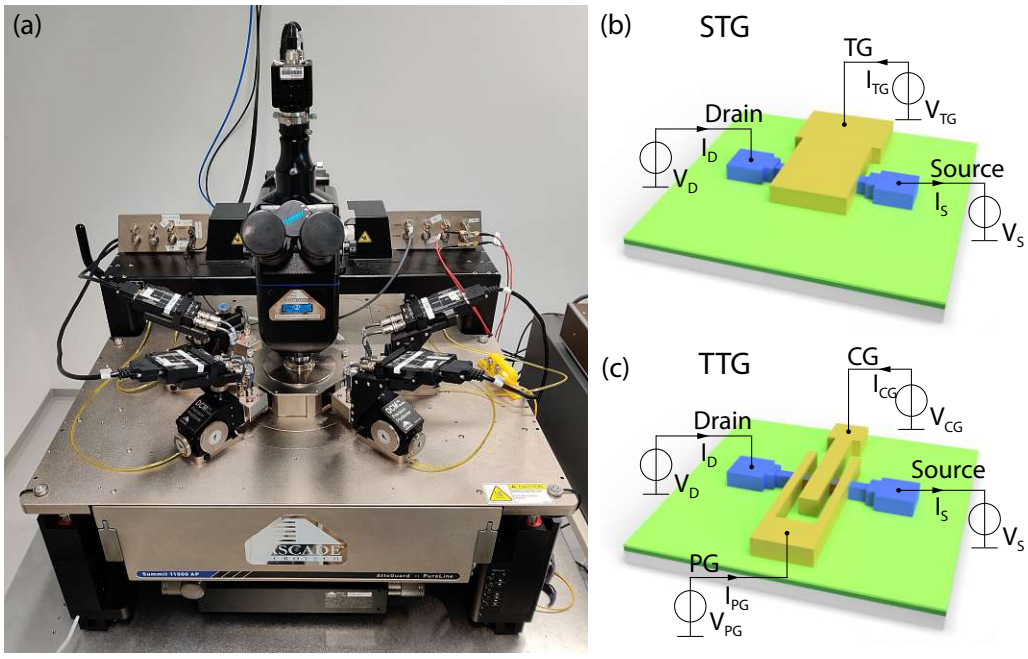

Figure 3.5: *In (a) the cascade Summit 11000 AP four arm needle proper with SMUs and microscope used to contact the devices under test is shown. Subfigure (b) and (c) demonstrate the contacting and naming convention of the SMUs for a STG and TTG measurement, respectively. The illustrations in subfigure (b) and (c) were adapted from [29].*

The needles of the probing station were placed on the device pads which were connected with the SMUs according to the sketch shown in Figure 3.5 (b) and (c) for an STG and TTG device. Fo an STG characterization only three SMUs were connected to drain, source and the top-gate, as shown in Figure 3.5 (a). While for DTG and TTG measurements an additional SMU was necessary for the added polarity-gate connection, as depicted in Figure 3.5 (c). 4TGs required yet another SMU for the added control-gate, however the probing station only has four SMUs. Therefore, a Keithley 2700 digital multimeter was

used as constant voltage source for the polarity-gate voltage, since only the voltage of input A and B (or $CG1$ and $CG2$) was varied during one measurement, as described in Section 3.2.6. The drain and source were connected to the remaining two SMUs. The left pad connection of the nanosheet was usually the drain, see Figure 3.5 (b) or (c) and Figure 2.7, if not state otherwise. For the sake of completeness it has to be mentioned that the currents and voltages of the respective connections have been indexed with the connection name, e.g. I_{CG} and V_{CG}.

3.2.1.1 Measurement Settings

This subsection will give an overview of the measurement procedure, from maiden to temperature run, and outline some conventions which where taken. After fabrication every device on one sample was characterized with at least one transfer characteristic, consisting of a p- and n-mode measurement for DTG and TTG devices, at a suitable bias and top gate voltage for this sample. The suitable voltages for each sample were ascertained by a hand full of symmetrical and asymmetrical transfer measurements along with top-gate leakage current measurements for two or more devices. Usually, one device of each sample, possessing a different oxide thickness and composition, was deliberately destroyed in order to find out the gate oxide breakdown voltage by ever increasing top-gate voltages (V_{TG} or V_{CG} and V_{PG}) and simultaneous leakage current measurements. After that a safe working voltage, $2-3V$ lower than the breakdown voltage, for TG or CG and PG was found along with a suitable bias voltage and symmetry. The remaining devices where characterized after these settings. After evaluation of all devices, the best three of one architecture were chosen for an in depth temperature behavior characterization from room temperature to $125°C$ in $20°C$ steps, see Section 4.3.

Following some conventions, which apply to all presented measurements, if not stated otherwise:

Measurement Direction: For STG's the start voltage is lower than the end voltage ($V_{TG_{start}} < V_{TG_{end}}$), thus the measurement starts with the hole and ends with the electron conduction for negative and positive top-gate voltages respectively.
For DTG's, TTG's and 4TG's the measurement direction is from on- to off-state, hence for p-mode the start voltage is lower than the end voltage ($V_{TG_{start}} < V_{TG_{end}}$) and the other way around for n-mode ($V_{TG_{start}} > V_{TG_{end}}$).

Note that $V_{TG_{end}}$ is the end voltage of one sweep direction of a double measurement.

Continuous Measurements: The sweeping parameter, being V_{TG}, V_{CG}, V_{PG}, V_D, V_S or any other parameter, is scanned thru continuously from one value to the next without an interruption. Pulsed measurements, where the sweeping parameter is set to a base voltage ,usually $0V$, in between two values are not presented in this thesis.

Single/Double Measurements: A single measurement represents the singular passing from start to end value. While a double measurement stands for forward and backward measurement from start to end and back to start again.

Back-Gate Voltage: The back-gate, consisting of the Si-handle layer and the BOX as dielectric, discussed in Figure 3.1 and Section 3.1.1, is kept floating during all measurements, if no stated otherwise. A shift towards lower or high threshold voltages can be achieved by applying a positive or negative voltage at the back-gate, hence tuning the symmetry. This however comes with the cost of decreased/increased on-state currents.

3.2.1.2 Bias Direction and Symmetry

The bias voltage is defined as the voltage which is applied along the channel. In the case of a FET/RFET this is the drain-source voltage V_{DS}. If the drain potential is set to an arbitrary value, for instance $V_D = 2V$ and the source potential to $V_S = 0V$, the overall bias is $V_{DS} = 2V$ and **asym**metrical because $V_D \neq -V_S$. For a drain voltage of $V_D = 1V$ and a source voltage of $V_S = -1V$ the overall bias is also $V_{DS} = 2V$, however the bias is **sym**metrical because $V_D = -V_S$. In the following sections, especially in Chapter 4 presenting the measurement results, the bias will be abbreviated with V_{DS} and sym/asym, for a symmetrical or asymmetrical bias respectively.

Furthermore, the bias direction is, if not stated otherwise, not flipped for p- and n-mode measurements of TTGs and 4TGs, thus V_{DS} and therefore the current direction stays the same for both modes. This makes TTG band bending directly comparable with that of an STG and would result in a same sign current independent of the mode, which can be useful for some applications. However, for FET's commonly all voltage directions, including V_{DS} or if a positive value is desired V_{SD}, are flipped for p-mode FET devices. The influence of a flipped bias $V_{SD} = -V_{DS}$ for both p- and n-mode is evident from Output characteristics presented in Figures 4.7 and 4.14 and is represented by a horizontal symmetry.

Note, that for DTG devices the bias direction is always flipped, unless stated otherwise, thus $V_{DS_N} = -V_{DS_P} = V_{SD_P}$. Otherwise an ambipolar behavior is observable for example for the p-mode if the bias is positive, as explain in Section 2.4.3. This can be observed for polarity-gate characterizations of DTG's discussed in Section 4.3.2.

3.2.2 Key Aspects of RFETs

Since RFETs are somewhat different, but on the other hand also quite similar to conventional FETs, the emphasis of the electrical measurements and the resulting conclusions maybe be different for every reader, depending on the individual background. This subsection will give an overview of the key device aspects which were considered in this work, in order to form a common ground for the upcoming measurement evaluations in Chapter 4. In order to efficiently analyze a bunch of devices a evaluation script, introduced

in Section 3.2.9, extracting most of the following key aspects, was implemented. Therein, parameters like the averaging window and the threshold voltage extraction method are discussed. A *good* device should fulfill all, or as many aspects as possible, without failing to achieve one aspect totally. Note, that the following list is not sorted by any means.

Key Aspects of RFET devices:

On/On Symmetry: Ratio between the mean on-state current in p- and n-configuration. Always given as ratio ≥ 1 - no specific order for nominator or denominator, whereby p-mode is typically higher in on-state current for Ge devices. Written as On/On. Usually extracted from Transfer characterizations, Section 3.2.3.

Off/Off Symmetry: Ratio between mean off-state current in p- and n-configuration. Always given as ratio ≥ 1. Written as Off/Off, however generally not explicitly given. Usually extracted from Transfer characterizations, Section 3.2.3.

On/Off Ratio: Ratio between mean on- and off-state current for each mode. Always given as ratio ≥ 1. Written as $On/Off\ p$ or $On/Off\ n$. Usually extracted from Transfer characterizations, Section 3.2.3.

V_{th} **Symmetry:** Offset of threshold voltage (V_{th}) for p- and n-configuration relative to the center top- or control-gate voltage, which is $V_{TG/CG} = 0V$ in this work. Written as individual threshold voltage for each mode, $V_{th}\ p$ or $V_{th}\ n$, but evaluated as absolute difference between each threshold voltage. Usually extracted from Transfer characterizations, Section 3.2.3.

Subthreshold Slope: A similar subthreshold slope for both p- and n-mode is needed in order to accomplish high On/On symmetries with a adequate V_{th} symmetry. Written as $STHS\,p$, and $STHS\,n$ for the respective mode. Usually extracted from Transfer characterizations, Section 3.2.3.

Bias Direction Symmetry: On- (and off-state) currents symmetry depending on the applied bias direction in each mode. Note, that V_{DS} can be applied symmetrically ($V_D = -V_S$) or asymmetrically ($V_S = 0$). Not explicitly written. Usually extracted from Output characterizations, Section 3.2.4.

Hysteresis: Area spanned between on- to off- and off- to on-state, other direction also possible, sweep during an Transfer measurement. For the sake of simplicity and comparability the hysteresis is calculated as the difference between V_{th} from on- to off- and V_{th} from off- to on-state. Written as individual hysteresis for each mode, $Hyst.p$ or $Hyst.n$. Usually extracted from Transfer characterizations, Section 3.2.3.

Polarity-Gate Symmetry: Offset of V_{th} for p- and n-configuration at varying V_{PG} and constant V_{CG} relative to the center polarity-gate voltage, which is $V_{PG} = 0V$ in this work. Not explicitly written. Usually extracted from Polarity-gate characterizations, Section 3.2.5.

Top-Gate Leakage Current: Leakage current of the top gate electrode(s). Not specified if from the channel to top-gates or between top gates themselves. For STG I_{TG}, DTG and TTG I_{PG} and I_{CG}, 4TG I_{PG}, I_A and I_B are written. Usually only measured at the first Transfer characterization of each device, Section 3.2.3.

3.2.3 Transfer Characteristic

A transfer measurement, or often also referred to as I_DV_G curve, displays the absolute drain current, often logarithmic absolute drain current, over the changing top-gate voltage V_{TG} (STG) or control-gate voltage V_{CG} (DTG or TTG) on the ordinate and abscissa respectively. The bias voltage V_{DS} is kept constant during one sweep, as well as the polarity-gate voltage V_{PG} for DTG, TTG and 4TG devices. A transfer measurement with top-gate leakage currents is usually the first measurement done on a maiden device, because it gives a first glance on six key aspects given in Section 3.2.2, namely the On/On-, Off/Off-symmetry and On/Off ratio along with the V_{th} symmetry, hysteresis and the top gate leakage current.

3.2.4 Output Characteristic

For an output characterization the top-gate voltage, being V_{TG} for STG or V_{CG} for DTG and TTG devices, is kept constant during one measurement while the bias voltage and direction is changed. Note that the symmetry of the bias is not changed during one measurement. Usually not one single top-gate voltage is characterized, but several resulting a multitude of curves. Output measurements can be visualized as conventional line plots or as colormaps, where the absolute drain current $|I(D)|$ is displayed as color gradient over the varying bias and top-gate voltage V_{TG}/V_{CG} on the abscissa and ordinate, respectively. From these plots the bias symmetry for contrary bias directions for STG and TTG can be extracted. In an ideal case the mirror plane is located at zero bias $V_{DS} = 0V$. This is however not possible for DTG devices, due to the explained reverse operation mode discussed in Section 2.4.3. Note that the bias is also applied symmetrically or asymmetrically as discussed in Section 3.2.1.1 and will also be abbreviated accordingly.

Broadly speaking, the output characterization is a two parameter sweep. In an inner loop the bias is varied, while the top-gate voltage is changed in an outer loop. Transfer characteristics at varying bias voltages and directions put together into one colormap could also have the same appearance as an output measurement. However, the inner and outer sweeping parameters are flipped for the two measurements.

3.2.5 Polarity-Gate Spectroscopy

As the name describes, the polarity-gate characterization illustrates the device behavior in dependence of the polarity-gate voltage for different control-gate voltages. The measurement is usually performed in a two parameter sweep, with the control-gate voltage in the inner and the polarity-gate in the outer loop. The applied symmetrical/asymmetrical bias voltage V_{DS} is constant during the measurement and is abbreviated accordingly.

3.2.6 Multi Control-Gate Measurements

Multi-control-gate characterizations address the wired logic device behavior of 4TG's, depending on the voltage applied to the control-gates $CG1$ and $CG2$, see chapter Section 2.4. Therefore, $CG1$ and $CG2$ are varied in a two parameter sweep fashion, with $CG1$ in the inner- and $CG2$ in the outer-loop. The polarity-gate voltage is kept constant during the measurement and specifies the preferred mode, being p-mode, logical NOR, or n-mode, logical AND, along with a steady bias direction and voltage. In this work $CG1$ and $CG2$ will be termed A and B respectively, since wired AND and NOR gates were investigated. For these logic gates a symmetric behavior is preferable as input A and B should be interchangeable with each other. Furthermore, symmetric and sharp defined on- and off-states, later referred to with L and H, standing for low- and high-current region, are desired.

3.2.7 Effective Schottky-Barrier Height

Since the effective Schottky barrier height (eSBH) of a metal-semiconductor heterojunction is determined by the material compositions used as discussed in Section 2.3, an estimation of the formed barrier height, especially for new material combinations, is of great interest. Therefore, an effective Schottky barrier height estimation using a current temperature approach or I/V(T)-approach presented in the book of Schroder[75] is carried out. The simplifications made in Section 2.3 for the estimation of the barrier height are also valid for the eSBH assessment, if the barrier height is greater than k_BT at room temperature ($\approx 26mV$) and if barrier-lowering effects due to excessive bias voltages are neglectable [28, 75, 76].

Since the presented devices in this thesis consist of two metal-semiconductor junctions in a Al-Ge-Al system and the afore mentioned estimation methods are applied for conventional single junctions, the required activation energy for a flow of charge carriers can be approximated by the effective SBH (eSBH). Since the current through the device consists of a combination of thermionic-emission and field-emission, as introduced in Section 2.3.1, which either go over or thru the barrier and are indistinguishable by measurement, the total current is used for the eSBH estimation. Further complications arise if the applied voltages at the different top-gates are taken into account, which effect the barrier height along with their charge carrier injection. As a result, finding a physically suitable model describing all effects is difficult. Therefore, the presented results are only a rough estimation of the actual barrier height.

The required device inputs are taken from Output characteristics which were measured over temperature, starting at room-temperature ($T = 295K$) and going up to $T = 400K$ in $20K$ steps. The eSBH estimations are calculated out for STGs, since the single top-gate arrangement results in a less complex electrostatic configuration and therefore better approximations. Furthermore, only positive bias directions are considered. Details about the underlying theory, the applied estimation methods and how the used calculation script worked, can be found in [29]. The eSBH estimations of the STG devices fabricated in the context of this thesis are presented in Figure 4.8.

3.2.8 Effective Activation Energy

An extension of the before introduced effective Schottky barrier height (eSBH) is the effective activation energy (eAE) estimation. In contrast to the eSBH, where the barrier height is estimated at the zero-bias point $V_{DS} = 0V$ extrapolation, the effective activation energy indicates the required energy of a charge carrier in order to surpass the modulated barriers over the applied bias voltage. The eAE is calculated in the same way as the eSBH presented in Section 3.2.7 and [59], however without the extrapolation towards the zero-bias point. As a result, the same output measurements over temperature are the starting point of the eAE calculations. Further details about the used methods are given in [29, 59].

The eAE plots presented in this thesis will be presented as 2D colormap, where the control-gate voltage V_{CG} and drain-source bias V_{DS} are depicted on the abscissa and ordinate, respectively. The estimated effective activation energy is represented by the overlaying color scheme. In this thesis eAE are only presented for TTG device architectures. As a result, two separate eAE plots, one for each mode, are depicted. Note that the polarity-gate voltage is constant during the underlying measurement. The resulting eAE estimations of the TTG devices fabricated in the context of this thesis are presented in eAE Figure 4.16.

3.2.9 Device Evaluation

Since the graphical representation can be optically distorted by e.g. different axis scaling, thus preventing a qualitative comparison between different structures and simply because a large number of devices at different temperatures were measured, the raw data was analyzed. For this purpose a script was written in python which outputs the following key aspects according to Section 3.2.2: maximal absolute drain current $I_{D\,max}$ normalized to the nanosheet width W and current density $J_{D\,max}$ normalized to the nanosheet cross section $W \cdot H$ in $\frac{A}{\mu m^2}$ for p- and n-mode, On/On symmetry, On/Off symmetry for p- and n-mode, threshold voltage V_{th} for p- and n-mode, hysteresis for p- and n-mode and subthreshold voltage in $\frac{mV}{dec}$ for p- and n-mode. Note that the On/On symmetry along with the On/Off symmetries are taken from average on- and off-current values with varying averaging windows depending on the device architecture. Thereby, the STG's averaging window was set to 4 data points for both on- and off-current while for DTG's 20 and 10 and TTG's 30 and 20 on- and off-state current data points were averaged. The Off/Off

symmetry was not analyzed in the script, because the off-region currents were usually limited by the measurement resolution, hence no meaning full value would be obtained except for elevated temperatures.

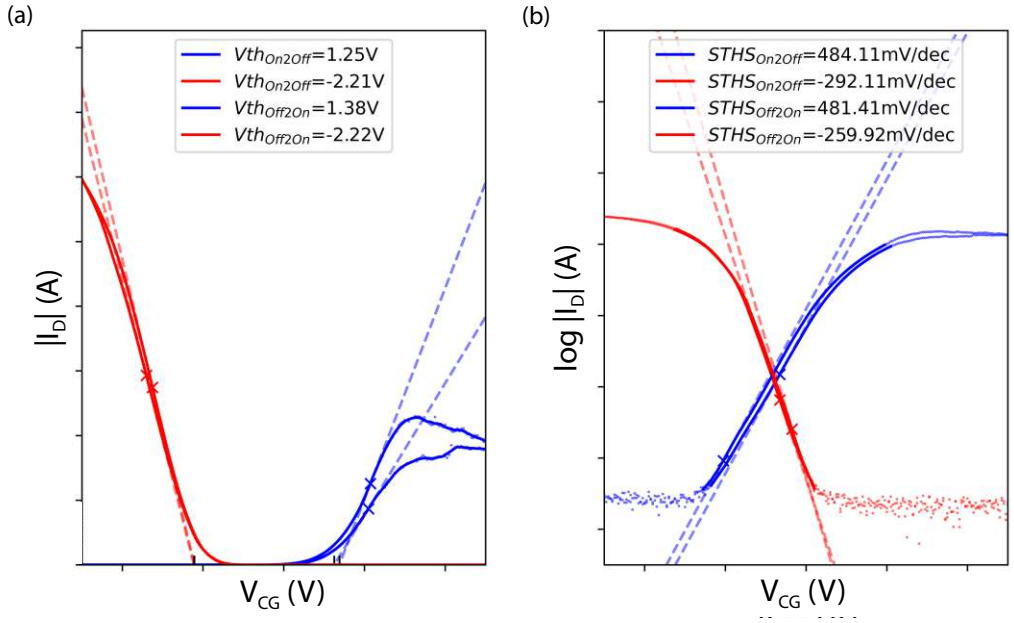

Figure 3.6: *Threshold voltage V_{th} and subthreshold slope $STHS$ evaluation of an TTG device. Both (a) and (b) show the same transfer measurement in the same control-gate voltage range, varied between $V_{CG} = \pm 5V$ with the sweeping direction depending on the respective mode, as stated in Section 3.2.1.1. For (a) the absolute drain current $|I_D|$ is plotted on a linear scale, while for (b) on a logarithmic ordinate. In (a) the linear extrapolation illustrated by the dashed lines intersect the abscissa where the respective threshold voltages are indicated by small black vertical marks. In (b) the $STHS$ is represented by the slope of the dashed lines. A symmetric bias voltage and direction of $V_{DS} = 2V$ is applied for both p- and n-mode. The illustration is generated by the evaluation script, hence the different style to all upcoming measurement results.*

The threshold voltage V_{th} of the p- and n-mode were calculated according to the linear extrapolation (LE) method [75, 77]. As the name indicates, the threshold voltage is the interception of the abscissa, representing the top-gate voltage axis for V_{TG} or V_{CG} at $I_D = 0A$, with the linear extrapolation of the I_D/V_G curve at its maximum gradient or highest transconductance g_m value. An exemplary evaluation is shown in Figure 3.6 (a), where the threshold voltages V_{th} is given for the p- and n-mode indicated in red and blue, respectively. In addition the threshold voltage of each sweep direction, being either from on to off ($on2off$) or off to on ($off2on$), of the analyzed double sweep transfer measurement is given.

For the sake of comparability the hysteresis is calculated as the difference between the on to off and off to on threshold voltage of a double measurement. Since all devices were measured from on to off and back, as stated in Section 3.2.1.1, the measurement direction

is not the same for p- and n-mode. As a result, the usual clockwise and counterclockwise hysteresis analysis and corresponding conclusions on the underlying physical effects are not applicable [78]. Therefore, a scheme introduced in [79], depending on whether the back sweep current (BSC) is lower or higher than the forward sweeping current. Lower BSC indicates a charge carrier trapping close to the channel while a higher BSC suggests mobile ions inside the dielectric layer [79]. For the given evaluations a higher BSC results in a positive sign for the hysteresis, while a negative values stand for a lower BSC hysteresis since $Hyst. = V_{th_{Off2On}} - V_{th_{On2Off}}$. Recall the mode independent sweeping direction for STGs, which are always varied from negative to positive and back top-gate voltages. For the example given in Figure 3.6 (a) the hysteresis for the p- and n-mode are both positive since the BSC is higher with values of $hyst_p = 0.01V$ and $hyst_p = 0.13V$.
For the sake of completeness, it has to be pointed out that severe diverging on to off and off to on sweep slops could lead to a large displacement of the calculated threshold voltage V_{th} resulting in a wrong value and sign for the determined hysteresis value. Therefore, a visual inspection is also indispensable.

The subthreshold slope $STHS$ puts a top-gate voltage change (in mV) and a current increase/decrease by a factor of 10 (in decades) into relation. Therefore, indicating how fast a transition from low to high current state, and vice versa, is possible. As the name states, this approximation is valid for top-gate voltages below the threshold voltage or in the region of weak inversion [28]. Therefore, only the current range between on- and off-state was analyzed by the script. Thereby, the subthreshold slope is the reciprocal subthreshold swing which is defined by [28], chapter 6.2, as:

$$S := \frac{dV_G}{d(log_{10} I_D)}$$

The maximal subthreshold slope is at the biggest gradient of the logarithmic current $|I_D|$ and is indicated by a small cross in Figure 3.6 (b), an exemplary transfer measurement of a TTG shown in a semi-logarithmic plot. The dashed line is a guidance for the eye and symbolizes the reciprocal maximum slope as the tangent in that point.

Note, that in Figure 3.6 the raw measurement data is shown by light red and blue dots, whereas the smoothed data point have a higher opacity. The data was only smoothed and therefore analyzed in the reigns of interest which excludes the noisy off currents for both analysis along with the on currents for the $STHS$ extraction. Drain currents that were below a multiple, usually a factor of three, of the average on or off currents were removed. The statistical data and calculated values presented in Tables 4.3 to 4.9, 4.11 and 4.12 of the respective transfer measurements, are extracted with the before mentioned python script.

Chapter 4

Results and Discussion

Based on the theoretical aspects discussed in Chapter 2 and the introduced fabrication process and characterization techniques in Chapter 3, this chapter presents and discusses the obtained fabrication and measurement results of individual samples.
The first section introduces the three fabricated samples based on different substrates in combination with distinct gate passivation layers. Thereby, the realized structures are analyzed in terms of scanning electron microscope (SEM) images. The next section compares the electrical behavior of STG, DTG and TTG devices fabricated on each sample, highlighting the influence and benefits of the underlying material system on the device behavior. Thereby, the performance of one sample stands out and is further characterized in the subsequent section by extensive bias spectroscopy, comprising transfer and output characterizations over temperature for the related STG, DTG and TTG devices. Furthermore, the temperature dependent mode switching behavior of DTG and TTG devices is analyzed by polarity-gate measurements along with the effective Schottky barrier height and effective activation energy for STG and TTG devices, respectively. On the same sample, the performance of 4TG devices as two input wired logic gates is studied. The respective evaluation results are presented in the last section and puts the obtained parameters into perspective to other Al-Ge and Al-Si RFETs found in literature.

4.1 Fabricated Devices

As already mentioned in the introduction of this chapter, the electrical behavior of three different RFET samples was investigated. Thereby, the influence of a sSOI and SOI base-substrate along with the inherent strain exerted on the Ge layer was of interest. An overview of the layer structure with the corresponding layer thicknesses of Sample A, B and C is given in Figure 4.1, subfigure (a), (b) and (c). Note the absence of the Si-capping

which acted as a sacrificial layer for the SiO_2 formation.
An overview of the measurement results for single, double and triple top-gate architectures fabricated on each sample is given in the next Section 4.2.1.

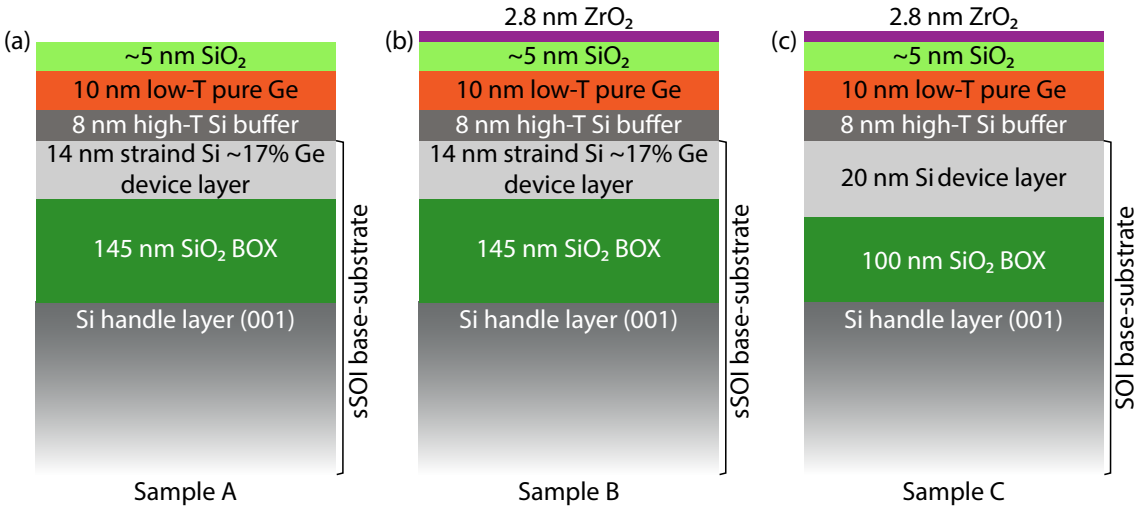

Figure 4.1: *Comparison of Sample A, B and C's layer structure. Sample A and B, shown in subfigure (a) and (b), are made out of the same base GesSOI substrate, while Sample C is fabricated from the GeSOI base-substrate. Note the added high-k dielectric layer for Sample B and C. Layer thicknesses are not to scale.*

Sample A was fabricated out of a GesSOI substrate, composed of a sSOI base-substrate, a Si buffer and pure Ge layer along with a SiO_2 gate dielectric. The strained Si layer of the sSOI base-substrate reduces the lattice mismatch to the grown Ge layer.
Sample B was fabricated out of the same substrate as sample A, however with an additional ZrO_2 dielectric layer atop of the SiO_2.

Sample C on the other hand, is based on the GeSOI substrate, consisting of a SOI base-substrate, a Si buffer and a pure Ge layer along with a SiO_2/ZrO_2 dielectric stack. The absence of a strained Si layer underneath the Si buffer, yields a bigger lattice mismatch for the grown Ge layer. Therefore, it is believed that the internal stress of the Ge layer of sample C is bigger than in sample A and B. A comparison between the samples and thus also the electrical effects of the induced strain inside the Ge channel is given in Section 4.2. Note the thinner BOX and thicker device layer for the SOI base-substrate used in Sample C.

A further comparison concerning the oxide fabrication and annealing time for the Al-Ge exchange process is given in Table 4.1. Note the same oxidation time for all three samples and the similar amount of ALD cycles for sample B and C. The total required annealing time in order to get the desired Ge segment length is slightly higher for sample C. This increase in time could result from the additional strain in the Ge layer, but also results in shorter Ge segments on average, as shown in Table 4.2.

Table 4.1: *Fabrication differences and similarities between Sample A, B and C. Note, that no high-k dielectric layer was added to Sample A.*

Sample	Substrate	SiO_2: Oxidation time	ZrO_2: ALD cycles	Total anneal time	EOT
A	GesSOI	180 sec.	x	185 sec.	5 nm
B	GesSOI	180 sec.	30	190 sec.	5.4 nm
C	GeSOI	180 sec.	29	250 sec.	5.4 nm

As mentioned in Section 3.1.2.2, the SiO_2 growth of all three samples was done by dry thermal oxidation in nitrogen at $T = 900°C$. The ALD reactor temperature of $T = 250°C$ for the ZrO_2 deposition was the same for both sample B and C.
The grown SiO_2 and ZrO_2 thicknesses were estimated by Ellipsometry measurements. Therefore an additional pure Si test-sample was added to the oven/reaction chamber and measured before and after growth/deposition. However, it has to be pointed out that the added Si test-samples had a different crystal orientation than the Si capping layer, resulting in different growth rates for the two samples [80]. Furthermore, the Si capping layer was only 3nm thick, resulting in a Si exhaustion for oxidation times of 3 min. [59].

All samples were annealed at $T = 500°C$ in forming gas, starting the Al-Ge exchange process and forming the metal-semiconductor junctions, as described in Section 3.1.2.4. The stated total anneal time in Table 4.1 consists of three subsequent anneal steps for sample B and C and four steps for sample A, each with different times and intermediate optical Ge segment measurements.

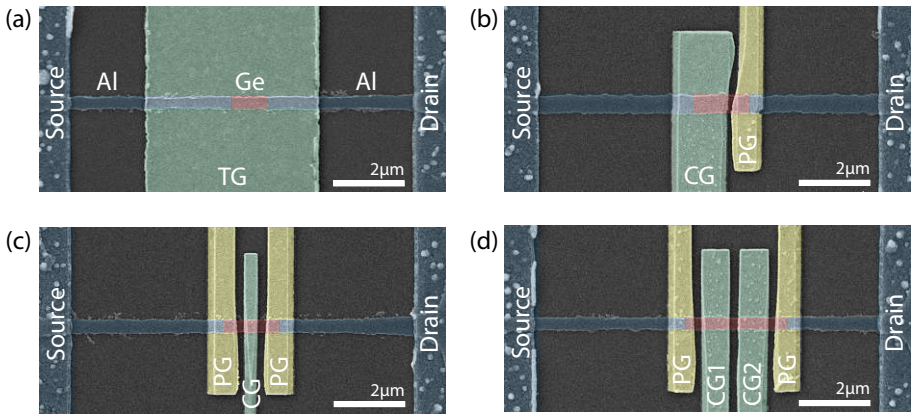

Figure 4.2: *False colored SEM images of different device architectures along with highlighted Germanium (Ge) segments in red, Aluminum (Al) source and drain contacts in blue, top-gate (TG) or control-gate (CG) in green and polarity-gate (PG) in yellow. Subfigure (a) shows the top-gate arrangement of a STG with a Ge-segment length $L \approx 1\mu m$ and a nanosheet width $W \approx 0.4\mu m$, (b) a DTG with $L \approx 1.7\mu m$ and $W \approx 0.5\mu m$, (c) a TTG with $L \approx 1.6\mu m$ and $W \approx 0.4\mu m$ and (d) a 4TG with $L \approx 3\mu m$ and $W \approx 0.4\mu m$. The distance between the source and drain pad is $\approx 10\mu m$, while the CG and PG distance varies between $150nm$ and $250nm$.*

Exemplary structures fabricated on sample B possessing different device architectures, as introduced in Section 2.4.2, are illustrated in Figure 4.2 showing false color SEM images at 20K magnification. Thereby, by taking a look at subfigure (c) and the narrow control-gate, the Ge-segment length dependent architectural choice becomes evident. The position of the Ge-segment is determined prior to the top-gate deposition, allowing a deliberate positioning of the respective gates, as discussed in Section 3.1.2.5. Note, that the physical connection of the polarity-gates of the presented DTG, TTG and 4TG devices is not shown in subfigures (b-d) and that the dark gray area surrounding the nanosheet is the underlying SiO_2 BOX of the respective base-substrate. The corresponding etching process is described in Section 3.1.2.1.

Table 4.2: *Overview of the fabricated device architectures on each sample, along with the average nanosheet width and Ge segment length.*

Sample	# STGs	# DTGs	# TTGs	# 4TGs	avg. width [μm]	avg. length [μm]
A	24	10	21	3 (+2 5TGs)	0.5	2.05
B	6	22	28	4	0.44	1.94
C	7	20	30	3	0.47	1.78

Each fabricated sample possesses 60 individually controllable RFET devices, which yet again have slightly different nanosheet widths and Ge segment lengths. Depending on the remaining Ge segment length after the Al-Ge diffusion, STG, DTG, TTG or 4TG were fabricated. Due to the required space of additional top gates, the amount of top gates decreases with decreasing segment lengths. The exact amount of each fabricated RFET device architecture for the respective sample along with the average nanosheet width and Ge segment length are given in Table 4.2.

4.1.1 Al-Si-Ge Heterostructure

Due to the off-centered fermi level pinning of the Al-Ge metal-semiconductor junction, as shown in Figure 2.6, a disparate hole and electron conduction for p- and n-mode is excepted, since the resulting Schottky-barriers are dissimilar. This is however not the case as demonstrated in the subsequent measurement, revealing p- and n-mode on/on symmetries as low as a factor of two. Therefore, it is believed that an Al-Si-Ge metal-semiconductor junction is formed from the Si sandwiched Ge layer, as presented for a similar material system with a sSOI channel layer [50]. Thereby, the added Si interlayer results in a mid band-gap fermi level pinning of the formed junction, enabling the formation of equal height Schottky-barriers for both holes and electrons. The Al-Si-Ge heterostructure is further motivated by the faster Si diffusion in Al, as stated in Table 2.3.

4.2 Project Evolution

In search of the most suitable RFET platform and gate stack composition, the electrical behavior of the afore introduced samples A, B and C was further investigated. This section will highlight the distinct differences regarding the transfer characteristics of each sample concerning the STG, DTG and TTG device architecture. The measurement results are presented in Figure 4.3 and Tables 4.3 to 4.5.

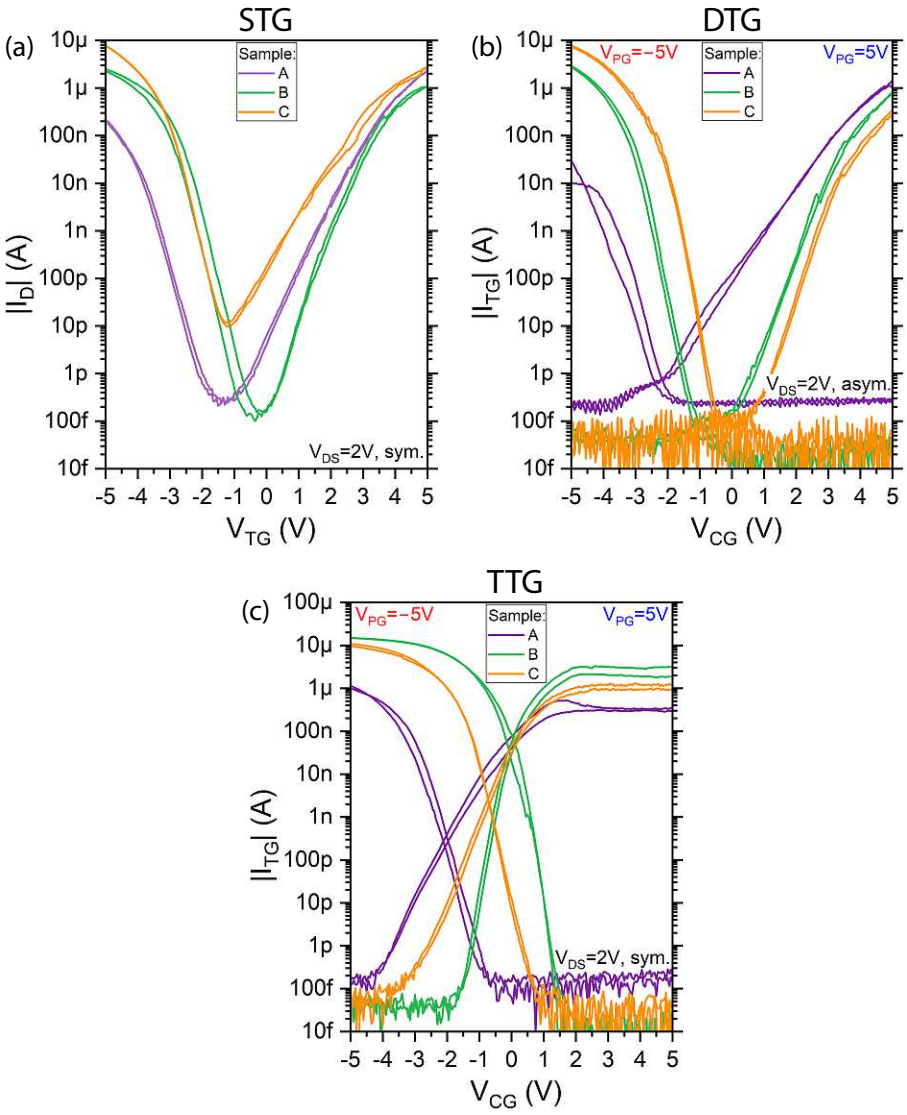

Figure 4.3: *Comparison of transfer characteristics of STGs, DTGs and TTGs fabricated on sample A, B and C. The measurements of each device architecture were conducted with the same electrical and environmental conditions, being ambient air and room temperature ($T \approx 295K$). An additional equally scaled ordinate was added on the right side, simplifing a visual symmetry analysis. Furthermore, note the adapted ordinate for subfigure (c) ranging up to $100\mu A$.*

For the comparison in Figure 4.3 the best performing device, according to the criteria discussed in Section 3.2.2, of each device architecture was compared to its counterpart on the other sample. Furthermore, the devices were operated in the same mode, thus had the same top-gate voltage range, polarity-gate voltage, bias direction and symmetry along with the same ambient temperature (room temperature, $T \approx 295K$) and environment. Hence, the measurements are directly comparable in terms of device performance. Note, that the following comparison between the three samples only focuses on the distinct differences, due to the lack of statistics. An in depth analysis of the measurement results of sample B is given in the next Section 4.3.

Subfigure (a) in Figure 4.3 shows the juxtaposition of sample A, B and C for the STG device architecture. Thereby, a shift of the off-point towards higher current values and lower top-gate voltages of sample C is the most prominent difference between the samples. This increase in off-current is somewhat compensated by increasing on-state currents, which however goes along with a reduced On/On symmetry. A shift towards lower top-gate voltages is also observed for sample A along with a low On/On symmetry. As a result, the device of sample B overall outperforms the other samples, as can also be seen in Table 4.3 by the green highlights. Solely the before mentioned on-state current of the STG on sample C outperform sample B along with the hysteresis of the other samples. Considering the hysteresis of the presented devices, sample A possesses the lowest values and overall smallest variation. Recall, that the On/On and On/Off symmetries are calculated from the mean on- or off-state currents of the respective mode.

Table 4.3: *Evaluation results of STGs fabricated on Sample A, B and C. The highlighted values indicate the best performance among the three samples.*

Sample	On/On	On/Off n	On/Off p	V_{th} n [V]	V_{th} p [V]	|Hyst. n| [V]	|Hyst. p| [V]	STHS n [mV/dec]	STHS p [mV/dec]
A	10.75	$4.29{\cdot}10^5$	$5.50{\cdot}10^4$	3.90	-4.30	0.06	0.04	643.7	-390.1
B	2.11	$5.62{\cdot}10^6$	$1.55{\cdot}10^7$	3.58	-3.55	0.15	0.36	402.7	-328.2
C	2.76	$1.69{\cdot}10^4$	$6.33{\cdot}10^4$	3.54	-3.87	0.73	0.01	722.6	-331.1

A comparison of the DTG measurements over the respective samples can be seen in Figure 4.3, subfigure (b). Thereby, a similar electric behavior of sample B and C is observed. Not only are the STHS similar but also the overall curvature of the transfer behavior. Since the slope of the p-mode is almost twice as large as that of the respective n-mode, the centered V_{CG} position of sample C results in a worse On/On symmetry. The n- and p-mode threshold voltage of sample B on the other hand, is shifted by approximately 0.2V and 0.3V respectively, resulting in an improvement in On/On ratio by a factor of more than 7. Furthermore, the p- and n-mode intersection of sample B and C is located in the off-state current, which is typical for DTG architectures or low V_{th} devices [58]. Sample A on the other hand, does not follow the trend. Not only is the overall curvature different but also the STHS along with an increased off-state current. Moreover, the V_{th} values are shifted far to the left, leading to excessively high On/On ratios of about 40. As seen in

Table 4.4, the DTG of sample B possesses the lowest On/On symmetry along with the most centered V_{th} values. Although, sample B is outperformed in various factors, as seen in Table 4.4, it overall has the best RFET performance, mainly due to its good On/On ratio and centered V_{th} symmetry.

Table 4.4: *Evaluation results of DTGs fabricated on Sample A, B and C.*

Sample	On/On	On/Off n	On/Off p	V_{th} n [V]	V_{th} p [V]	|Hyst. n| [V]	|Hyst. p| [V]	STHS n [mV/dec]	STHS p [mV/dec]
A	44.02	$6.52{\cdot}10^{6}$	$8.70{\cdot}10^{4}$	3.75	-3.66	0.34	0.82	717.5	-359.6
B	3.50	$1.58{\cdot}10^{7}$	$9.26{\cdot}10^{7}$	4.05	-3.90	0.20	0.09	461.1	-271.7
C	24.01	$5.78{\cdot}10^{6}$	$1.89{\cdot}10^{8}$	4.17	-3.46	0.04	0.04	240.9	-163.6

The TTG performance of the fabricated samples is compared in subfigure (c) of Figure 4.3. Yet again, sample B outperforms the other samples. Only the On/On current symmetry is higher for sample A. The exact evaluation results are given in Table 4.5. Optically the TTG transfer characteristic of sample B also stands out. Not only is the intersection point of the p- and n-mode centered at $V_{CG} \approxeq 0V$, it is also at the highest current value of the three devices. However, it has to be pointed out that the optical hysteresis of sample C is yet again the lowest. At this point the off-state current of sample A needs to be pointed out, which seems not to underpass $|I_D|$=100fA, independent of the device architecture. In contrast to the STG and DTG evaluation results, sample C did not show the highest on-state current, neither for p- or n-mode.

Table 4.5: *Evaluation results of TTGs fabricated on Sample A, B and C.*

Sample	On/On	On/Off n	On/Off p	V_{th} n [V]	V_{th} p [V]	|Hyst. n| [V]	|Hyst. p| [V]	STHS n [mV/dec]	STHS p [mV/dec]
A	2.28	$8.93{\cdot}10^{5}$	$5.14{\cdot}10^{6}$	0.19	-3.21	0.16	0.43	563.4	-316.9
B	4.64	$6.69{\cdot}10^{7}$	$1.23{\cdot}10^{9}$	0.77	-0.87	0.11	0.01	215.5	-163.5
C	7.07	$2.08{\cdot}10^{7}$	$2.48{\cdot}10^{8}$	0.98	-2.02	0.62	0.22	473.2	-275.0

Comparing the evaluation results in Tables 4.3 to 4.5 for all three device architectures over the individual samples, shows that the GesSOI substrate in combination with a SiO_2/ZrO_2 gate stack used in sample B is best suitable as RFET platform for various device architectures. Not only are the devices of sample B more centered but also exhibit a higher on-state and lower off-state current. Comparing sample A and B with each other, it is evident that the added high-k dielectric layer on sample B results in a better electrical controllability along with a right shift of the transfer characteristic. The improvement in controllability can be justified with a growing electrical capacitance, as described in Section 2.1.2.2. As a result, equivalent band bending requires less voltage at the respective top-gate. Furthermore, leakage currents are reduced due to the thicker oxide layer. The shift in top-gate voltage is discussed in the next Section 4.2.1 and mostly depends on formed interface states. However, one disadvantage of sample B is the comparatively larger hysteresis.

A direct comparison between sample B and C outlines the influence of the pure Si device layer of the SOI base-substrate used in sample C. The consequently increased internal stress of the Ge layer and the influence on its electrical behavior are debated in Section 4.2.2. Considering the DTG and TTG measurements displayed in Figure 4.3 (b) and (c), the results lie between sample A and B in terms of on-state currents and V_{th} symmetry. For the STG device architecture, in subfigure (a), however, the on-state currents are higher than for sample A and B. This behavior though is accompanied by an increased off-state current and a negative V_{th} shift.

As a consequence of the measurement results discussed above, the electrical behavior of RFETs fabricated on sample B are further investigated. Therefore, the electrical transport phenomena of STGs, DTGs and TTGs over temperature are studied in the following Section 4.3 along with the capabilities of 4TGs as wired logic gates.

4.2.1 Electrical Influence of a SiO_2 and ZrO_2 Gate Dielectric

As seen in Figure 4.3 the samples with a SiO_2 gate dielectric only, exhibit a transfer characteristic which is shifted towards negative top-gate or control-gate voltages. This shift can be verified numerically by considering the respective threshold voltages of the p- and n-modes. In order to counteract this offset in threshold voltages, a high-k dielectric can be added to the gate stack. Depending on the chosen dielectric layer different interface states between the SiO_2 and high-k dielectric interface are formed. These states can either favor holes, electrons or both, leading to a corresponding shift in V_{th}. Thereby, a combination of SiO_2 and ZrO_2 result in an increase of fixed negative charges, effectively shifting the I_D/V_G to the right or more positive top-gate voltages [81].
For the sake of completeness it has to be mentioned that the high-k dielectric layers were not directly deposited onto the semiconductor, but instead on top of SiO_2 forming the aforementioned SiO_2/ZrO_2 interface. This results in lower interface state densities close to the conducting channel and therefore to a reduced hysteresis [82].

Due to the obtained results of sample A, an additional high-k dielectric layer of ZrO_2 was added on top of the SiO_2 for samples B and C, resulting in a positive V_{th} shift, better electrical controllability, steeper STHS and less gate leakage.

4.2.2 Influence of Strain on the Electrical Characteristic

The influence of strain on the intrinsic carrier mobility of semiconductors has been known since the early 1950's [83, 84]. Thereby the externally applied or internal strain changes the carrier mobility. Note that this effect is depending on the crystal direction of the semiconductor and the flow direction of charger carriers [85]. In contrast to conventional FETs, where one transistor is either p- or n-type and therefore tailored for its specific charge carrier, RFETs must be optimized for both polarities.

Comparing the electrical behavior of sample B and C in Figure 4.3 the influence of the strained and unstrained base-substrate becomes evident. Thereby, sample B is fabricated out of a sSOI base-substrate possessing a strained Si device layer on top of which the Ge layer is grown with a Si buffer layer in between. Sample C on the other hand, has a SOI base-substrate with a pure Si device layer beneath the Ge layer, which was grown under the same MBE conditions. Since Ge has a larger lattice constant than Si, as stated in Table 2.1, the Ge grown atop of the pure Si device layer of Sample C is exposed to a higher lattice mismatch resulting in a higher internal stress of the grown layer in comparison to sample B with the strained Si device layer.

The observed higher p-mode on-state currents for both STGs and DTGs fabricated on sample C, can be traced back to increased hole mobilities due to the increased strain of the Ge layer [86–88]. The TTG measurements presented in Figure 4.3 (c) suggest a slight decrease of hole and electron mobility. Further investigations not only on the crystallographic orientation but also the amount of the exerted strain in dependence of the base-substrate need to be conducted in order to give a viable answer. However, the effect of the strained Ge layer is observable in the measurements at hand.

4.3 Ge on Strained Silicon on Insulator (GesSOI)

In this section the electrical behavior of a variety of RFET devices possessing different top-gate architectures fabricated on Sample B (GesSOI with SiO_2 and ZrO_2) are investigated. Therefore, several STG, DTG and TTG devices were measured under the same conditions. The corresponding statistical results highlight the stability of the presented RFET platform. Furthermore, the influence of temperature on the electrical transport mechanism of RFETs was investigated. For this reason, transfer and output characteristics for three representative STG, DTG and TTG devices were measured over temperature, starting from room temperature ($T \approx 22°C$) until $T \approx 127°C$ in $20°C$ steps. For DTGs and TTGs an additional polarity-gate characterization was added, illustrating the mode-switching behavior. The corresponding measurement results are presented in Sections 4.3.1 to 4.3.3, while the characterization techniques are explained in Section 3.2. Since the temperature was set in Kelvin on the respective temperature controller, subsequent measurement temperatures will also be given in Kelvin.

Before plunging into the individual device architecture investigation and temperature analysis, a comparison between the three main device architectures fabricated on the same sample needs to be considered. Figure 4.4 thereby not only highlights the advantages of each device architecture but also underlines the transport theory presented in Section 2.4.3.

As concluded in Section 2.4.2, discussing the RFET top-gate layouts, depending on the device architecture different features can be exploited, such as lower threshold voltages, higher on-state currents or an ambipolar I/V behavior, as shown in Figure 4.4. This is a result of the specific Schottky barrier modulation and control-gate variation, which is

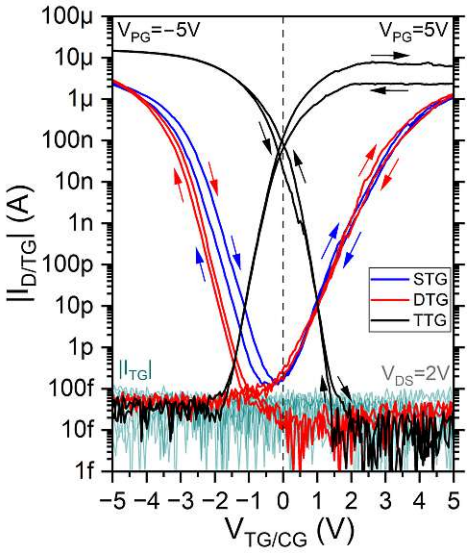

Figure 4.4: *Transfer measurements of STG, DTG and TTG devices fabricated on sample B/GesSOI with a SiO_2 & ZrO_2 gate dielectric. The STG and TTG were bias in a symmetric fashion, while the DTG was biased asymmetrically. The bias voltage however was the same for all devices with $V_{DS} = 2V$. The respective colored arrows indicate the sweeping direction of the device. Note the top-gate leakage current $|I_{TG}|$ depicted in cyan, which is perishing in the measurement resolution.*

different across the particular architectures, making the junction transparent or blocking for holes and electrons, as described in Section 2.4.3 concerning band bending and the corresponding illustration in Figure 2.8. As a result, one device architecture may be better suited for the application than the other. Nevertheless, all three presented top-gate layouts feature high On/On symmetries, On/Off ratios of six orders of magnitude, only limited by the measurement resolution, and negligible top-gate leakage currents. The evaluation results of the discussed measurements containing the afore mentioned On/On symmetries and On/Off rations along with the respective V_{th} and STHS are given in Table 4.6.

Another detail to point out in Figure 4.4 is the hysteresis of the fabricated devices on Sample B. Thereby the colored arrows indicate the sweeping direction of the respective device. The visually determined back sweep current directions (BSC) and corresponding calculated signs given in Table 4.6 are in agreement with the presented evaluation method in Section 3.2.9.

4.3.1 Electrical Transport of Ge based SBFETs

Next the device performance between six different STG devices fabricated on sample B will be compared. Therefore, the transfer measurements of all STGs are illustrated in Figure 4.5 (a). The corresponding statistical evaluation is given in Table 4.11. An overview of the fabricated devices on sample B is given in Table 4.2.

Table 4.6: *Evaluation results for a representative STG, DTG and TTG fabricated on sample B. The corresponding transfer characteristic is illustrated in Figure 4.4.*

Architecture	On/On	On/Off n	On/Off p	V_{th} n [V]	V_{th} p [V]	Hyst. n [V]	Hyst. p [V]	STHS n [mV/dec]	STHS p [mV/dec]
STG	2.11	$5.09{\cdot}10^6$	$1.31{\cdot}10^7$	3.58	-3.55	-0.15	0.36	402.7	-328.2
DTG	2.13	$2.58{\cdot}10^7$	$7.76{\cdot}10^7$	3.82	-3.90	-0.25	0.09	384.1	-271.7
TTG	2.08	$1.91{\cdot}10^8$	$1.23{\cdot}10^9$	0.65	-0.88	0.14	-0.01	219.6	-163.5

Considering the measurement results in Figure 4.5 (a), a coarse trend regarding on-state currents is observably. This also holds true for the p-mode STHS, resulting in a low standard deviation, as stated in Table 4.11. When it comes to the n-mode STHS and off-state current, the matter looks somewhat different. There the devices can be separated into two groups. Device 11, 21 and 37 stand out due to their low off-state current and therefore centered V_{th}. Thereby not only the On/On symmetry is improved, but also the STHS of the n-mode branch. The elevated off-state currents of device 27, 53 and 57 counteracts the desired device behavior, resulting in worse On/On symmetries, V_{th} values, n-mode STHS along with an overall asymmetric behavior for the p- and n-branch.

Analyzing the evaluation results in Table 4.11 for all STG devices a good On/On symmetry of around two, high On/Off ratios with more than five orders of magnitude and a low overall hysteresis of $0.15V$ and $0.38V$ are achieved. Despite the obvious shift in off-state currents, the mean threshold voltages are still relatively symmetrical with a delta of $0.2V$. The total current densities on the other hand are lower than comparable results presented in [58].

The transfer behavior over temperature is shown in Figure 4.5 (b), starting at room temperature ($T = 295K$) and going up to $T \approx 127°C$ or $T = 400K$. Note the second ordinate, representing the current density $|J_D|$ normalized to the nanosheet cross section. Thereby, a steady increase in both p- and n-mode on-state currents with higher temperatures is observed. This behavior is coupled to the increase in conductivity with temperature of semiconductors [28]. Thereby, the off-state current should also increase by an equal amount. This is however not the case, since it rises from around $|I_D| \approx 100fA$ at $T = 295K$ to $|I_D| \approx 100pA$ at $T = 400K$ in comparison to the on-state current increase of not even on order of magnitude. This can be explained by the change in Fermi-Dirac distribution at the metal-semiconductor junction and the increasing in thermionic-field emission (TFE) current, representing the combination of both thermionic emission (TE) and field emission (FE) or tunneling currents [22, 28], as discussed in Section 2.3.1. In addition to the increase in off-state current, it also shifts towards more negative top-gate voltages at elevated temperatures, with $T = 400K$ being the outlier with a slight right shift. Moreover, a gain in hysteresis is noticed with ascending temperatures, especially for the p-mode starting at almost none at room temperature. This increasing in hysteresis

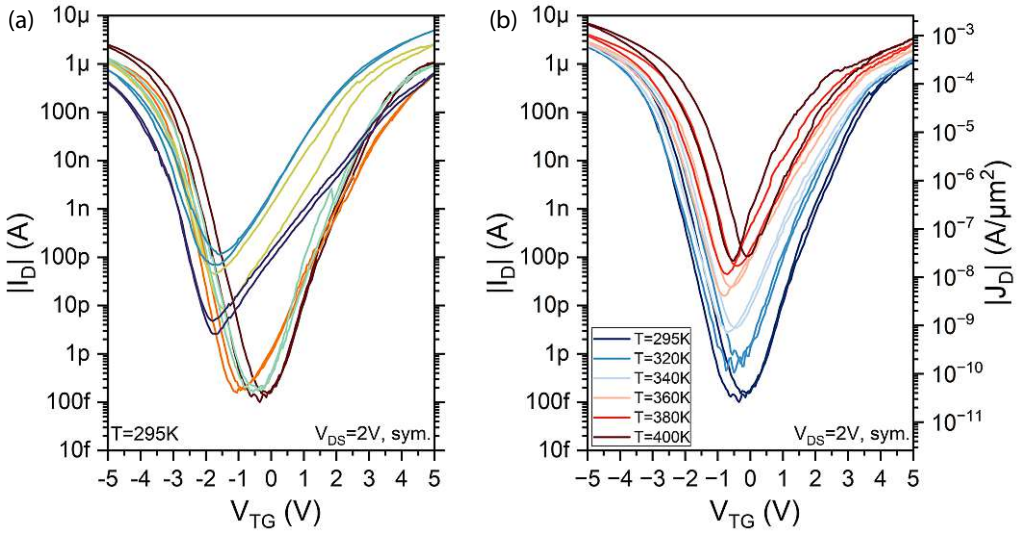

Figure 4.5: *GesSOI STG: Transfer investigation for a multitude of STG devices and temperature effects. (a) Transfer characteristics of six individual STG devices, all operated under the same electrical and environmental conditions. An additional equally scaled ordinate was added on the right side, simplifying a visual symmetry analysis. (b) Transfer behavior of device 11 at different elevated temperatures. Note the added current density $|J_D|$ axis on the right ordinate.*
Measurement details for (a) and (b): The top-gate voltage was varied in $50mV$ steps starting at $V_{TG} = -5V$ to $+5V$ and back in a double sweep measurement. The bias voltage of V_{DS} was applied symmetrically to drain and source. In (b) the temperature was gradually increased in $20K$ steps, starting at $T = 295K$ and going up to $400K$.

with temperature can be described by an enlargement of the active trap region for a lower BSC or positive hysteresis value while a higher BSC or negative value suggests an increase in mobile ions inside the oxide [89].

While analyzing the evaluation results in Table 4.7, the previous visual inspection of Figure 4.5 is verified and extended. Thereby the interesting trend of gradual improving On/On symmetries with rising temperature stands out. The afore mentioned rising on- and off-state current is also observed in increasing $|J_D|$ while On/Off ratios are decreasing with temperature. As a result, the transfer slops are getting flatter leading to higher STHS values for both n- and p-branch. Furthermore, rising temperatures contribute to a reduction in threshold voltage, while the V_{th} symmetry is not improved either. Interestingly, no clear trend for the p- and n-branch hysteresis is notable from the evaluation data, while the visual analysis showed a clear increase. At this point it is worth pointing out that the calculated value for the hysteresis is only considered at the respective threshold voltage. Further details are given in Section 3.2.9, discussing the evaluation script.

As described in Section 3.2.4, the output characterization puts the top-gate voltage V_{TG}, associated as input voltage, in perspective to the resulting drain current I_D in dependency of the applied drain-source bias V_{DS}. Therefore, the drain current I_D is measured at a

Table 4.7: *GesSOI STG: Statistical temperature evaluation of an STG device possessing a nanosheet width $W \approx 390nm$ and a Ge segment length of $L \approx 0.95\mu m$.*

Temp. [K]	On/On	On/Off n	On/Off p	V_{th} n [V]	V_{th} p [V]	Hyst. n [V]	Hyst. p [V]	STHS n [mV/dec]	STHS p [mV/dec]
295	2.20	$5.36{\cdot}10^6$	$1.43{\cdot}10^7$	3.66	-3.37	-0.15	0.36	407.5	-330.4
320	2.05	$6.65{\cdot}10^5$	$1.99{\cdot}10^6$	3.51	-3.39	0.02	0.33	470.1	-357.0
340	1.86	$1.04{\cdot}10^5$	$2.77{\cdot}10^5$	3.71	-3.34	-0.13	0.40	572.1	-376.1
360	1.47	$1.61{\cdot}10^4$	$3.14{\cdot}10^4$	3.47	-3.27	-0.19	0.36	687.1	-376.1
380	1.49	$1.02{\cdot}10^4$	$2.09{\cdot}10^4$	3.82	-3.26	0.36	0.45	598.5	-404.3
400	2.00	$1.45{\cdot}10^4$	$3.55{\cdot}10^4$	3.59	-3.09	0.14	0.42	528.6	-398.0

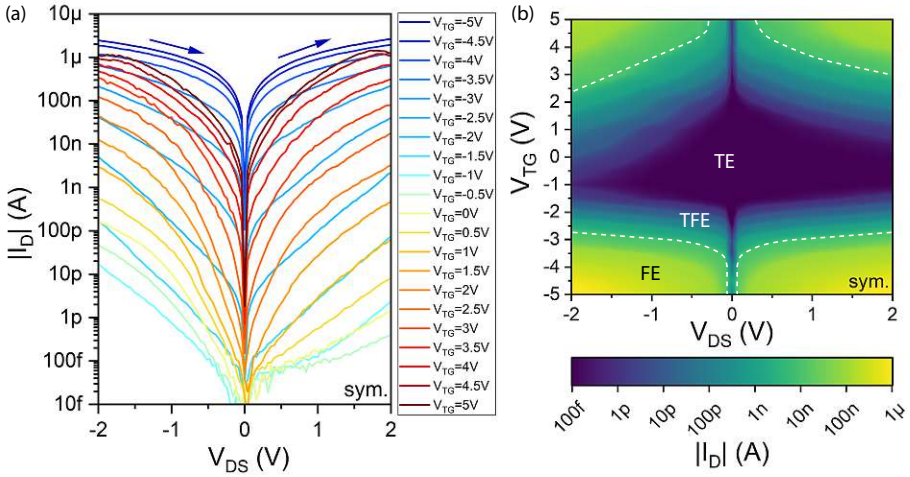

Figure 4.6: *GesSOI STG Output characterization displayed as line plot (a) and colormap (b). The white dashed line along with the dark blue region mark the respective dominant charge carrier transport regime in subfigure (b).*
TE ... Thermionic emission, TFE ... Thermionic-field emission, FE ... Field emission

variety of bias voltages V_{DS} and different top-gate voltages V_{TG}. The resulting measurement can either be displayed as line plot for each top-gate voltage over a varying bias voltage on the abscissa and the resulting absolute drain current on the ordinate, as shown in Figure 4.6 (a), or as colormap with the bias and top-gate voltages represented on the abscissa and ordinate respectively, whereas the absolute drain current is shown as color gradient, as depicted in Figure 4.6 (b).

Comparing the two illustrations methods in Figure 4.6 of one and the same measurement, different properties are highlighted in each plot. In the line plot representation the different gradients of the p- and n-branch are evident, however each measurement is overlapped by a multitude of others. This is not the case for the colormap representation, since every measurement for each top-gate voltage is vertical staked. The aforementioned difference in p- and n-branch slops can be distinguished by the pitch between two adjacent equipotential

surfaces, represented by the same color. Furthermore, the dominate transport regimes, as discussed in Section 2.3.1, are indicated. Thereby, thermionic-emission (TE) has the highest influence in the low-current region, while field-emission (FE) dominates the high-currents, whereas thermionic-field emission is located in the transition region in between. Note that further output characterizations will be shown as colormap.

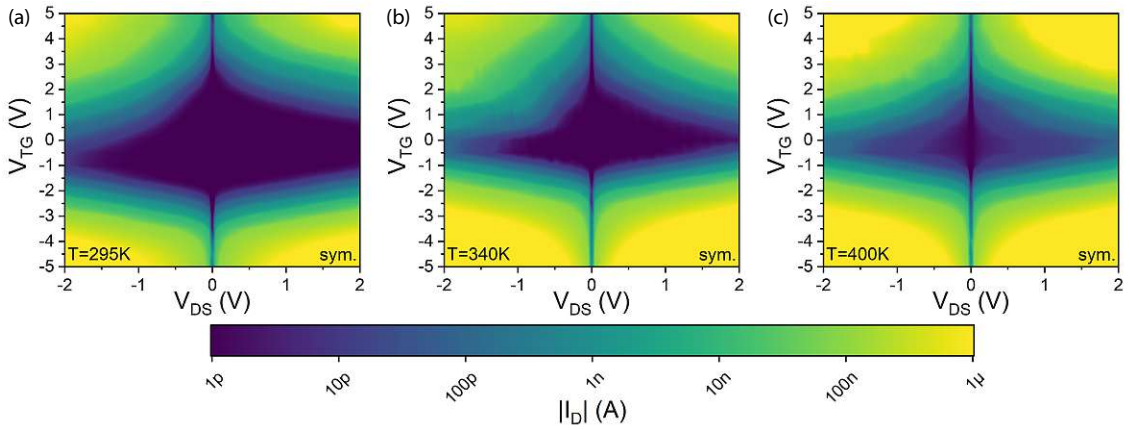

Figure 4.7: *GesSOI STG: Output investigation over temperature under same bias conditions. Note the backward bias direction for negative V_{DS} values.*
Measurement details for (a), (b) and (c): Various top-gate voltages from $V_{TG} = -5V$ to $+5V$ in $0.5V$ steps over a varying bias voltage starting from $V_{DS} = -2V$ to $+2V$ in $0.02V$ steps applied in a symmetric fashion. Increasing temperature $T = 295K$ for (a), $T = 340K$ for (b) and $T = 400K$ for (c).

The output characterizations for three distinct temperatures, $T = 295K$, $340K$ and $400K$, are depicted in Figure 4.7 (a-c). Note that positive V_{DS} values indicate a forward bias direction while negative V_{DS} voltages stand for a backward direction, as discussed in Section 3.2.4. Since an STG device is analyzed, there is no distinction between p- and n-mode due to its ambipolar behavior.

Considering the three output measurements shown, both on- and off-state currents increase with rising temperature, which is in agreement with the previous findings of the transfer measurements. Worth pointing out is the visual pronunciation of this behavior, with an ever shrinking dark blue center and growing yellow sections at the border. Furthermore, the forward and backward bias symmetry, horizontal symmetry, is improving with temperature, especially for the n-branch being less symmetric in reverse bias at lower temperatures. The vertical symmetry in V_{TG} is improved with elevated temperatures likewise. Generally, an increase in $|I_D|$ with rising bias voltages, independent of its direction, is observed, which is in good accordance with the band model presented in Section 2.4.3. Furthermore, it is worth pointing out the obviously low $|I_D|$ current at $V_{DS} \approx 0V$.

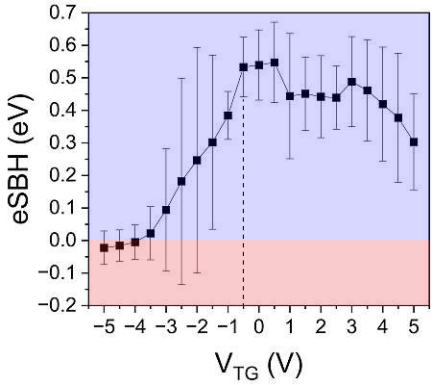

Figure 4.8: *GesSOI STG: Averaged effective Schottky barrier height estimation calculated from the output measurements from three devices. Note that the backward bias direction was not taken into account for the calculations.*

As mentioned in Section 3.2.7 the effective Schottky barrier heights (eSBH), estimated from the output measurements over temperature of three STG devices, are presented in Figure 4.8. Thereby, the two Schottky barriers of the horizontal Al-Ge-Al cross section of the STG are abstracted into one. Remember, that the effective Schottky barrier height approximation is the extrapolation of the eAE estimation towards the zero-bias point. The blue or red background colors highlight the areas of positive and negative energy, respectively. Thereby, a negative energy stands for a transparent or ohmic like contact, as mentioned in Section 2.3.1 and [48, 50, 90].

The lowest current point in an STG transfer characteristic resembles the intrinsic state and is located at $V_{TG} \approx 0.5V$ for the three used devices, as shown in Figure 4.5 (a), and correlates with the maximum value of the estimated barrier height in Figure 4.8, marked by a dashed line. Lower effective barriers are obtained for negative or positive V_{TG}, showing the controllability of the single top. The observed temperature behavior of device 11 in Figure 4.5 (b) is also in good agreement with the calculated barriers. Thereby, the rise in off current can be explained by thermally excited charge carriers surpassing the barrier with an increase in temperature. On-state currents are however dominated by field-emission which are not as temperature dependent as the before mentioned thermionic-emission, resulting in lower increases of the on-state currents over temperature [28, 91]. As discussed in Section 2.4.3 the charge carrier type depends on the respective mode of the RFET. As a result, not only electrons but also holes need to be considered when evaluating the estimated barrier. The *switch* from hole to electron barrier and vice versa takes place at the lowest current point of the transfer measurement, also highlighted by the black dashed line. This circumstance further complicates the estimation of the barrier height. Nevertheless, the obtained results are in good agreement with the data presented in literature [13, 91, 92].

4.3.2 Electrical Characteristics of Dual-Top-Gate RFETs

Similar to Section 4.3.1, this section will focus on the measurement results obtained for DTGs fabricated on sample B or the GesSOI platform with SiO_2 and ZrO_2 as dielectric. Therefore, eight DTGs were compared to each other and characterized over temperature.

Figure 4.9 (a) illustrates the transfer measurements of eight individual DTG devices. At first glance, all devices seem to have a fairly similar characteristic, which is also confirmed by low standard deviations in Table 4.11. At closer inspection however, slight variations, especially for the n-mode, are noticeable.

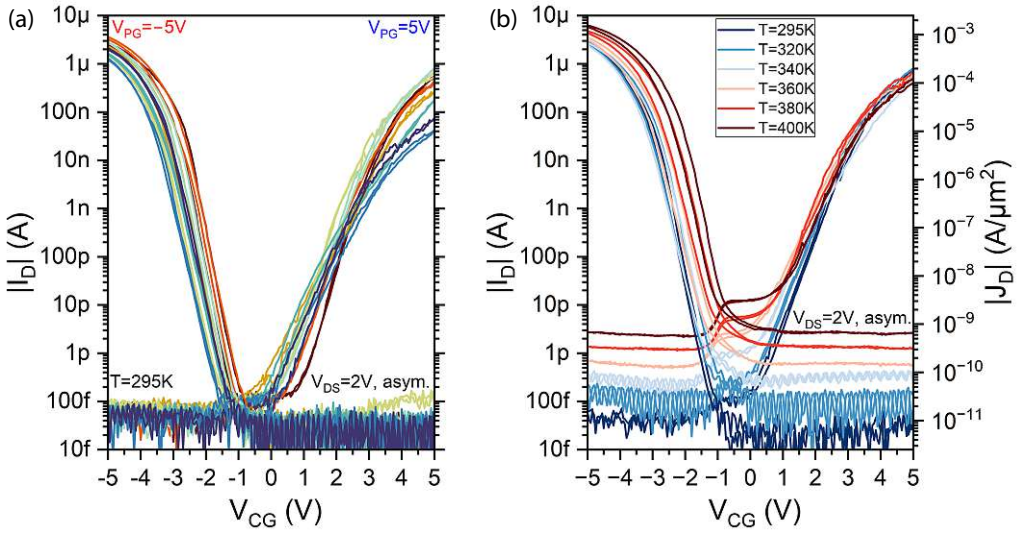

Figure 4.9: *GesSOI DTG: Transfer investigation for a multitude of DTG devices and temperature effects. (a) Transfer characteristics of eight individual DTG devices, all operated under the same electrical and environmental conditions. (b) Transfer behavior at different elevated temperatures. Note the added current density $|J_D|$ axis on the right ordinate.*
Measurement details for (a) and (b): Control-gate voltage applied from on- to off-state, $V_{CG} = \pm 5V$ to $\mp 5V$ in $50mV$ steps, in a double measurement. The polarity-gate and bias voltages were set to positive or negative voltages of $|V_{PG}| = 5V$ and $|V_{DS}| = 2V$. The bias was applied in an asymmetric fashion. For (b) the temperature of the sample was continuously increased from room-temperature to $T = 400K$.

All illustrated devices possess a low p-/n-mode intersection point which is additionally also close the center control-gate voltage V_{CG}. Furthermore, the V_{th} is also symmetric and only differs by about 0.2V for p- and n-mode. However, due to the steeper p-mode of around $300mV/dec$, compared to approximately $450mV/dec$ for n-mode, lower n-mode on-state currents are reached. This unbalance is further enlarged by varying n-mode on-sets voltages, resulting in On/On ratios as large as 30 for device 52 and 54. Nevertheless, both modes retain a low mean hysteresis of $0.24V$ and $0.07V$ for the respective n- and p-mode. Additionally, high current densities J_D of $10^4 A/\mu m^2$ are reached. The low off-

state currents result in overall high On/Off ratios of six to seven orders of magnitude. However, it has to be pointed out that the off currents for p-mode are lower than its n-mode counterpart.

The temperature characterization consist of transfer and output measurements at elevated temperatures shown in Figure 4.9 (b) and Figure 4.10, along with polarity-gate evaluations, identifying the distinct operating regions in Figure 4.12. Furthermore, the results of the transfer measurements over rising temperatures are given in Table 4.8

Table 4.8: *GesSOI DTG: Statistical temperature evaluation of a DTG device possessing a nanosheet width of $W \approx 400nm$ and a Ge segment length $L \approx 1.9\mu m$.*

Temp. [K]	On/On	On/Off n	On/Off p	V_{th} n [V]	V_{th} p [V]	Hyst. n [V]	Hyst. p [V]	STHS n [mV/dec]	STHS p [mV/dec]
295	3.67	$1.53{\cdot}10^7$	$7.97{\cdot}10^7$	4.15	-3.86	-0.20	0.05	487.5	-284.5
320	4.38	$4.16{\cdot}10^6$	$2.56{\cdot}10^7$	4.02	-3.82	0.04	0.19	525.8	-311.9
340	5.63	$1.41{\cdot}10^6$	$6.80{\cdot}10^6$	3.98	-3.77	-0.25	0.25	527.6	-333.8
360	5.52	$8.93{\cdot}10^5$	$5.42{\cdot}10^6$	4.06	-3.69	-0.25	0.22	599.0	-338.2
380	8.14	$4.16{\cdot}10^5$	$3.46{\cdot}10^6$	3.84	-3.33	0.56	0.28	487.9	-331.1
400	14.06	$1.59{\cdot}10^5$	$2.28{\cdot}10^6$	4.05	-3.15	-0.01	0.34	592.5	-299.9

Taking a look at the transfer measurements over temperature in Figure 4.9 (b) and the corresponding evaluation results in Table 4.8, an overall similar curvature and STHS is evident. Comparing the characteristics of p- and n-mode, an almost steady on-state is observed for n-mode, while p-mode seems to unfold with rising temperature. Thus, p-mode on-state currents are increased, resulting in a decrease in On/On state symmetry with rising temperatures, starting at ratios of 3.7 and going up to 14. This is exactly the opposite behavior as for the STG in Section 4.3.1. Albeit, the increasing off-state currents with rising temperature are similar to the STG measurements and seem almost identical for both p- and n-mode. This could be justified with similar metal-semiconductor barriers for both holes and electrons. As for the STGs, the increase in off current is higher than the on-state current, leading to shrinking On/Off ratios. Similar to the STGs, this rise in off current is followed by flatter slopes, or higher STHS values for both p- and n-mode. Analogous to the STG, the sign of the n-mode hysteresis changes with temperature, while staying positive for the p-mode. Last but not least, the reason behind the emerging kink around $V_{CG} = 0V$ for the n-mode at elevated temperatures, resulting in higher p-/n-mode intersections is believed to depend on the corresponding band bending and possible thermionic-field emission currents at certain control gate voltages, as depicted in Figure 2.8, since it its only observed for DTGs.

The output characteristic of a DTG will be displayed differently in comparison to its STGs and also TTGs counterparts, as discussed in detail in Section 2.4.3. First, there is a distinction between p- and n-mode, which is set by the polarity-gate voltage. Second,

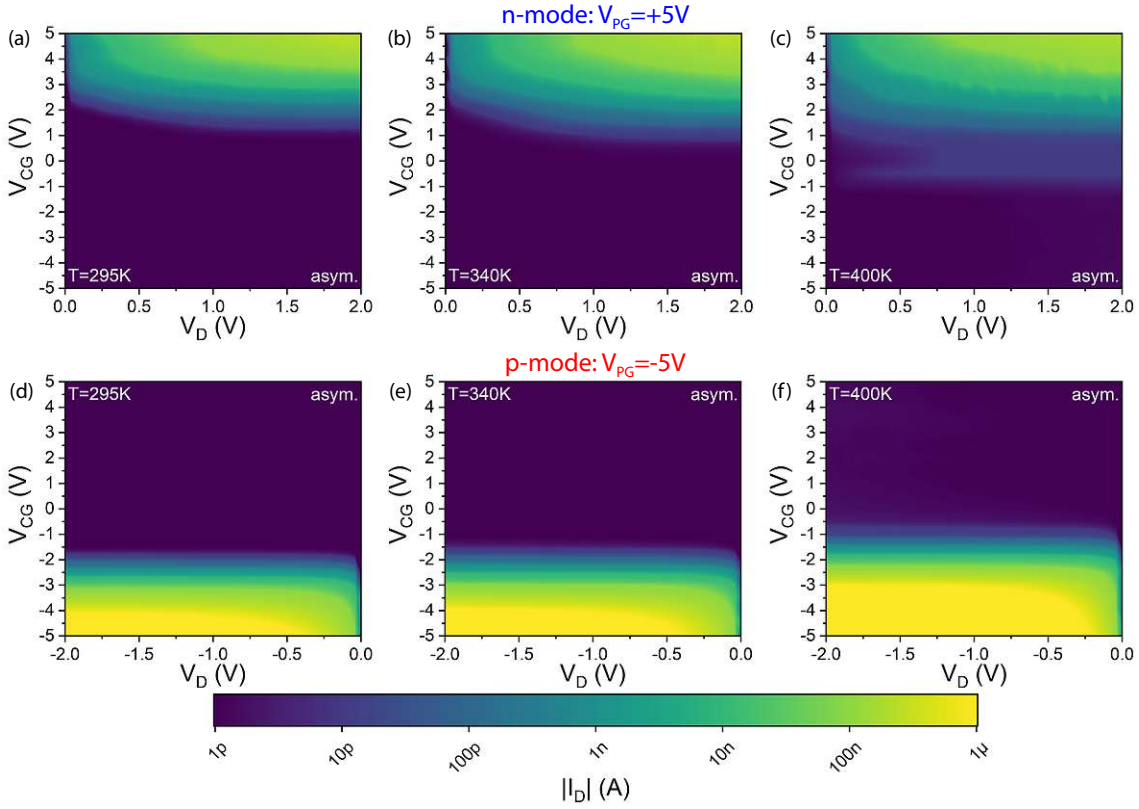

Figure 4.10: *GesSOI DTG: Output investigation over temperature under same bias conditions. The reverse operating region is not displayed, as discussed in Section 2.4.3. Therefore, only positive or negative V_D values are shown for n- and p-mode, respectively.*
Measurement details for (a-f): Asymmetric bias voltage decreased from $V_D = \pm 2V$ to $0V$ in $40mV$ steps for various control-gate voltages starting from $V_{CG} = \pm 5V$ to $\mp 5V$ in $0.5V$ steps, applied from on- to off-state. In (a-c) the DTG was put into n-mode operation with a polarity-gate voltage of $V_{PG} = +5V$, while in (d-f) it was configured for p-mode with $V_{PG} = -5V$. The temperature was increased from room temperature to $T = 400K$ in $20K$ steps, while only three temperatures of each mode are depicted.

the reverse operation region is not shown. Therefore, n-mode will only feature positive bias voltages, whereas for p-mode only negative biases are depicted. Note, that the source potential V_S is zero for both modes.

In Figure 4.10 (a-c) the n-mode ($V_{PG} = +5V$) output measurements are shown for room temperature, $T = 340K$ and $T = 400K$. Comparing the on-state currents, there is a clear increase with temperature, as expected from the previous analysis and Section 2.4.3. As a result, the off-state region, shown in dark blue, shrinks and suggests a threshold voltage shift towards lower control-gate voltages. Furthermore, the on-state current seems to be bias independent for $V_{DS} > 1V$. This can be a result of a saturating electron current or an artifact of the colormap.

Figure 4.10 (d-f) on the other hand show the same measurements however for p-mode, set by a negative polarity-gate voltage of $V_{PG} = -5V$ and a negative bias direction. The evident increase in on-state current with rising temperature is also visible here along with a shift towards lower control-gate and bias values, further expanding the on-region displayed in yellow. Thereby, the on-state current seems to bias independent from bias voltage as low as $|V_{DS}| > 0.5V$. This is however for sure caused by the colormap, since the p-mode on-state current exceeds $1\mu A$, as previously discussed.

Comparing n- to p-mode, a higher on current for p is noticeable. Furthermore, a stronger shift in n-mode V_{th} is implied, which is however not ratified by the evaluation of the transfer measurement in Table 4.8.

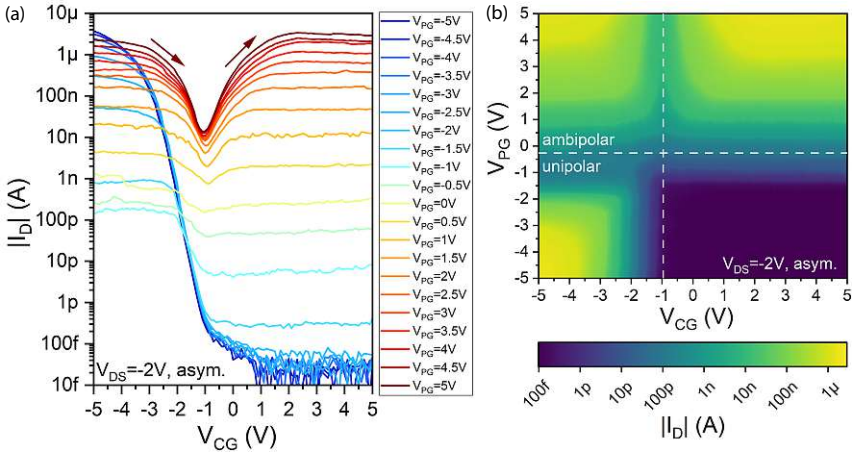

Figure 4.11: *GesSOI DTG Polarity-gate characterization displayed as line plot (a) and colormap (b) with a negative bias voltage of $V_{DS} = -2V$. The vertical white dashed line divide the on- and off-state regions, while the horizontal line marks the separation between the polar DTG-like behavior and the ambipolar STG-like characteristic.*

Depending on the applied polarity-gate voltage V_{PG}, the RFET is either set to p- and n-mode operation. The device behavior subjected to polarity-gate voltages in between the respective maxima is determined by polarity-gate characterizations, as described in Section 3.2.5. Therefore, transfer characterizations at various polarity-gate voltages are measured. The resulting measurements can either be displayed like a multitude of overlapping transfer measurements with various polarity-gate voltages V_{PG}, as depicted in Figure 4.11 (a), or as colormap with the control- and polarity-gate voltages represented on the abscissa and ordinate respectively, while the absolute drain current $|I_D|$ is shown as color gradient, as illustrated in Figure 4.11 (b). Note that the enabled mode of a DTG not only depends on polarity- and control-gate voltages but also on the corresponding bias voltage. Furthermore, the bias is applied in an asymmetric fashion.

The horizontal white dashed line in (b) marks the transition from *DTG*-like behavior, with a distinct p-mode set by a negative bias of $V_{DS} = -2V$, to an ambipolar *STG*-like characteristic in reverse-operation mode, as discussed in Section 2.4.3 and the corresponding band-diagram in Figure 2.8 (a). The vertical white dashed line highlights the on-state region of the illustrated p-mode and is set to a fixed control-gate voltage V_{CG}. Furthermore, variations in the drain-current at decreased polarity-gate voltages V_{PG} become more evident. The forthcoming polarity-gate characterizations will be illustrated as colormap with the white dashed lines mentioned before.

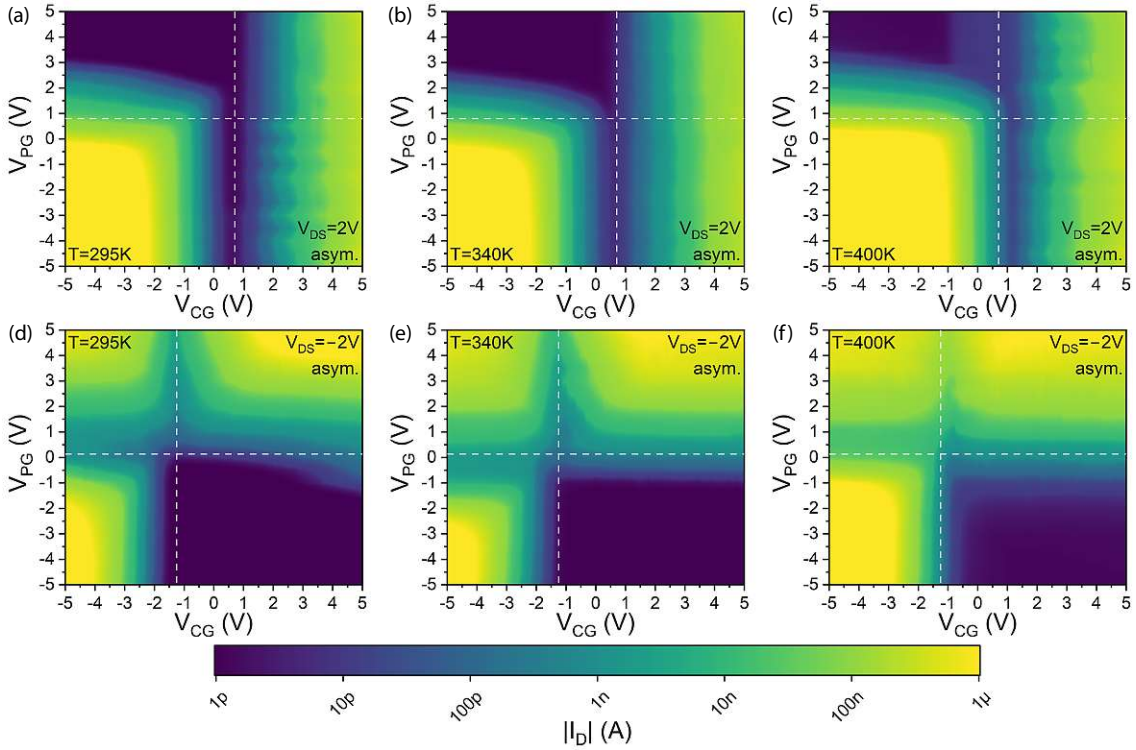

Figure 4.12: *GesSOI DTG: Polarity-gate characterization over temperature for different bias conditions. Note the ambipolar behavior in reverse operation.*
Measurement details for (a-f): The control-gate voltage was varied from $V_{CG} = \pm 5V$ *to* $\mp 5V$ *in* $0.1V$ *steps while the polarity-gate voltage was swept from* $V_{PG} = \pm 5V$ *to* $\mp 5V$ *in* 0.5 *steps. The source-drain potential was set to* $V_D = \pm 2V$ *while source was set to* $V_S = 0V$*, resulting in an asymmetric bias. Note that every mode was measured from on- to off-state.*

Figure 4.12 depicts the polarity-gate characterization under forward, subfigure (a-c), and backward, subfigure (d-f), bias direction. Different sign bias and polarity-gate voltages result in reverse operation regions, showing an ambipolar behavior as discussed in Section 2.4.3. The white dashed lines highlight the off regions at room temperature and are a guidance for the eye at higher temperatures and the corresponding shift in off-state regions. Furthermore, the horizontal line separates the preferable DTG behavior from the

undesired ambipolar *STG*-like behavior in reverse operation, as described in Section 2.4.3. Note that these are not set to the center control- nor polarity-gate voltage. The corresponding band diagrams for both positive and negative biases are shown in Figure 2.8.

In Figure 4.12 (a-c), the DTG is operated under a positive bias, highlighting the n-mode for same sign polarity-gate voltages. Thereby, a clear on-state region for both positive control- and polarity-gate voltages is observed. However, there is no clear distinction between on-stats for high control-gate voltages in combination with decreasing polarity-gate voltages. Furthermore, a rise in absolute drain current for negative control-gate voltages and low, but still positive, polarity-gate voltages is noticed. Polarity-gate voltages of $V_{PG} < 3V$ thereby mark the start of the ambipolar character in reverse operation.
With increasing temperature, the ubiquitous rise in current is identified. In addition, a slight shift of the vertical off-state line, dashed white line, towards higher control-gate voltages is observed along with an increase in off-state currents.

Subfigure (d-f) on the other hand emphasizes the p-mode, through, the simultaneous application of a negative bias and same sign control- and polarity-gate voltages. Thereby, a clear on-state island, with an increase in current for increasing polarity- and control-gate voltages is apparent. On the other hand, no such clear distinction in off-state current is seen for an ambipolar curve in reverse operation, as compared to its flipped bias direction. For increasing temperature the p-mode island is broadened and expanded towards lower control- and polarity-gate voltages.

4.3.3 Electrical Transport in Three-Gated Ge RFETs

As in the previous sections, concerning the STG in Section 4.3.1 and DTG in Section 4.3.2, this section deals with the statistical and temperature behavior of TTG devices fabricated on sample B, the GesSOI substrate in combination with a SiO_2/ZrO_2 gate dielectric stack. Therefore, the transfer measurements of nine individual TTGs were measured along with the temperature behavior of three devices.

Figure 4.13 (a) depicts the transfer measurements of nine individual TTGs. Overall a similar electrical behavior of all devices is observed in terms of their slops, on- and off-state currents and threshold voltage. This observation is verified by low standard deviations in Table 4.11 and implies a reliable and stable manufacturing process.

Generally, high on-state currents of almost $|I_D| = 10\mu A$ and low off-state with sub $100fA$ are reached, resulting in On/Off ratios of almost eight orders of magnitude. The overlapping p-mode has only one outlier, while the n-mode is rather unfolding at higher control-gate voltages, leading to increased On/On ratios. The fairly large and not self contained hysteresis for the n-mode on-state transfer curves are probably generated by fixed charges or traps with long relaxation times [89]. Measurements in vacuum could improve this behavior. Moreover, both p- and n-mode slopes are step over a wide control-gate range, with mean STHS of $270mV/dec$ and $430mV/dev$, respectively. However, the threshold

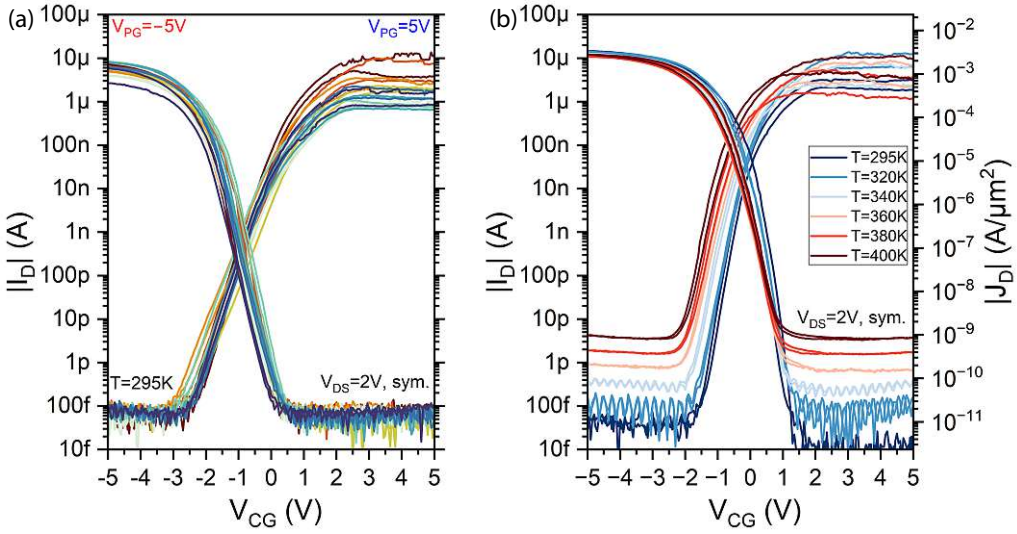

Figure 4.13: *GesSOI TTG: Transfer investigation for a multitude of TTG devices and behavioral change with increasing temperature. (a) Transfer characteristics of nine individual TTG devices, all operated under the same electrical and environmental conditions. (b) Transfer behavior at different elevated temperatures. Note the added current density $|J_D|$ axis on the right ordinate. Measurement details for (a) and (b): Control-gate voltage applied from on- to off-state, $V_{CG} = \pm 5V$ to $\mp 5V$ in $50mV$ steps, in a double measurement. The polarity-gate voltage was set to either $|V_{PG}| = +5V$ or $|V_{PG}| = -5V$ for n- or p-mode, respectively. The bias was set to $V_{DS} = +2V$ and applied symmetrically. For (b) the temperature of the sample was increased in $20K$ steps, starting from room-temperature to $T = 400K$.*

voltage is shifted towards more positive control-gate voltages, leading to an off-centered p- and n-mode intersection which is furthermore located somewhat in the center of the On/Off ratio.

Figure 4.13 (b) illustrates the temperature behavior of the transfer measurements. Thereby, the almost perfectly overlapping p-mode over temperature is most noticeable and does not follow the trend of the previous device architectures. This furthermore results in steady on-state currents along with slightly shifted threshold voltages towards more negative control-gate voltages, as stated in Table 4.9. Due to ever increasing off-state currents, On/Off state ratios deteriorate along with flatter subthreshold slopes, starting at $180mV/dec$ and going up to $280mV/dec$.
The n-mode on the other hand shows the typical unfolding behavior with rising temperatures. However, the threshold voltage and on-state currents vary due to the afore mentioned charging effect in Section 2.3.1 and Section 2.4.3. The STHS is only marginally increased with temperature from $220mV/dec$ at room temperature to $270mV/dec$ at $T = 380K$. The off currents gradually increase with temperature and cause a lowering in the On/Off ratio. The p- and n-mode intersection is close to the on-state currents and centered to the control-gate voltage V_{CG}. Furthermore, same sign hysteresis are observed, expect for the room temperature measurement. Lastly, the On/On ratio improvement is not convincing

due the charging effect leading to large n-mode on-state variations.
Worth pointing out is the steepest STHS out of all presented transfer measurements with $180mV/dec$ for the TTG p-mode at room-temperature.

Table 4.9: *GesSOI TTG: Statistical temperature evaluation of one TTG device possessing a nanosheet width $W \approx 430nm$ and a Ge segment length of $L \approx 1.7\mu m$.*

Temp. [K]	On/On	On/Off n	On/Off p	V_{th} n [V]	V_{th} p [V]	Hyst. n [V]	Hyst. p [V]	STHS n [mV/dec]	STHS p [mV/dec]
295	6.23	$5.42{\cdot}10^7$	$1.41{\cdot}10^9$	0.72	-0.96	0.11	-0.10	220.2	-182.7
320	1.66	$8.19{\cdot}10^7$	$1.33{\cdot}10^8$	1.10	-0.93	-0.89	0.15	254.4	-214.1
340	3.66	$1.16{\cdot}10^7$	$3.97{\cdot}10^7$	1.00	-1.06	-0.59	0.20	248.5	-238.5
360	3.20	$5.27{\cdot}10^6$	$1.68{\cdot}10^7$	0.49	-1.19	-0.74	0.30	272.2	-261.4
380	6.14	$1.30{\cdot}10^6$	$6.57{\cdot}10^6$	-0.02	-1.18	-0.61	0.28	270.8	-259.6
400	2.43	$1.65{\cdot}10^6$	$3.32{\cdot}10^6$	0.08	-1.17	-0.59	0.27	254.6	-280.0

The attentive reader may have noticed some differences between the room temperature transfer measurements in Figure 4.13 (a) and the transfer characterization over temperature in (b), regarding the overall curvature and most notable the n- and p-mode intersection. The exact reason behind the change in device character is not fully known, but it is believed to be caused by the gold top-gate metal diffusion with time and especially temperature. For instance, the measurements in subfigure (a) were taken two weeks prior to the temperature run presented in (b). However, the previously presented STG and DTG measurements at elevated temperatures were conducted during these two weeks, exposing the sample to $T_{max} \approx 127°C$ for some hours. A solution to this instability in device behavior is presented in the Summary and Outlook chapter, Chapter 5.

The output characteristics are shown in Figure 4.14, where the set polarity-gate voltage V_{PG} determines the mode. Subfigure (a-c) in Figure 4.14 depict the n-mode output over temperature. Thereby, distinct on- and off-regions are recognizable, which depend on the applied bias. The on- and off-state transitions are located around $V_{CG} = 0V$. These are shifted towards lower and slightly negative control-gate voltages for a rising temperature. Furthermore, the drain current is lowered for negative bias voltages, resulting in a forward/backward, or horizontal, asymmetry which is however improved with temperature.

The p-mode output measurements, set by a negative polarity-gate voltage of $V_{PG} = -5V$, are displayed in subfigure (d-f) of Figure 4.14. As for the n-mode, the p-mode also possesses distinct on- and off-state regions highlighted in yellow and dark blue, respectively. In contrast to the n-mode, the threshold voltage is shifted to more negative voltages, as also stated in Table 4.9. This results in a visual reduction of the on-state area. The afore mentioned horizontal asymmetry is not visual for p-mode, since the current is higher than $1\mu A$.

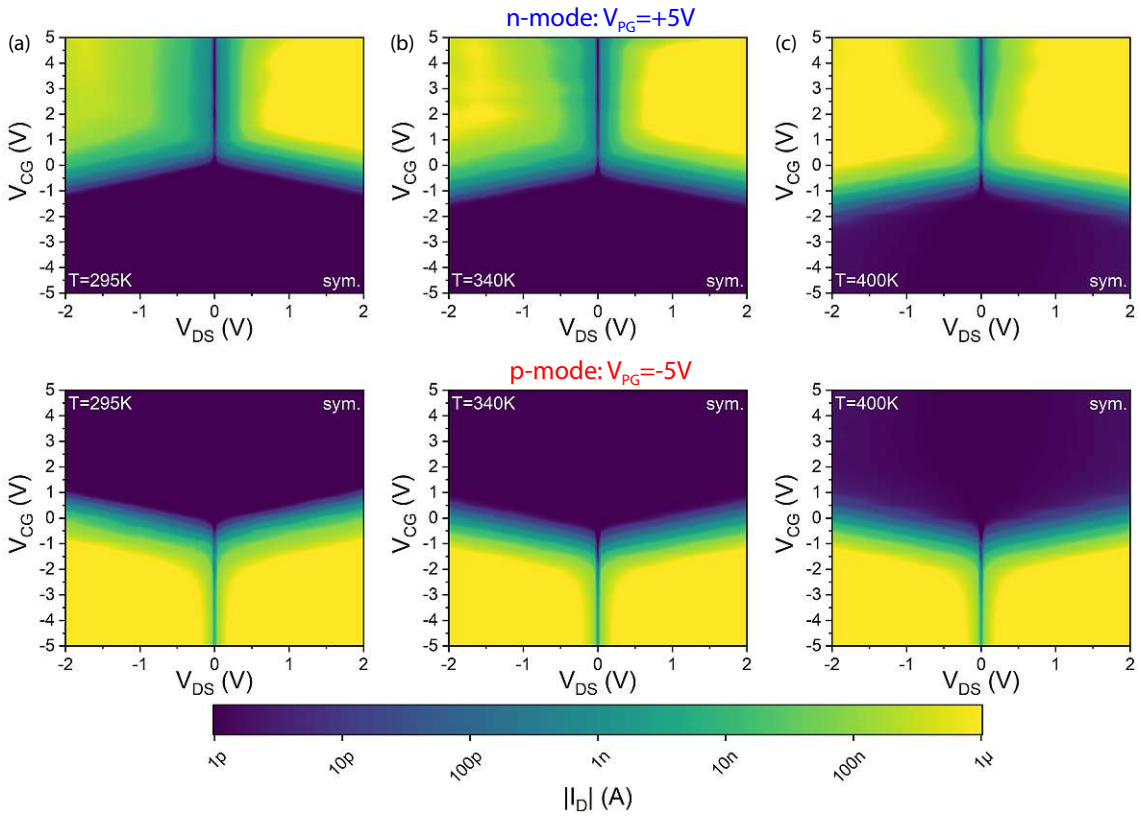

Figure 4.14: *GesSOI TTG: Output investigation over temperature under same bias conditions. Backward bias directions are indicated with negative V_{DS} values.*
Measurement details for (a-f): Symmetric bias voltage decreased from $V_{DS} = \pm 2V$ to $0V$ in $20mV$ steps for various control-gate voltages starting from $V_{CG} = \pm 5V$ to $\mp 5V$ in $0.5V$ steps (from on- to off-state). For (a-c) the polarity-gate was set to $V_{PG} = +5V$, while in (d-f) it was set to $V_{PG} = -5V$. The temperature was increased from room temperature to $T = 400K$.

Considering both p- and n-mode no bias independent range as for the DTG is evident. Furthermore, no distinct rise in off-current is noticeable. However, as expected, there is no current around the zero-bias condition, $V_{DS} = 0V$.

Figure 4.15 shows the polarity-gate sweep at elevated temperatures, where the mode-switching behavior with varying control- and polarity-gate voltages is investigated. The added white dashed lines are set to $V_{PG} = V_{CG} = 0V$, dividing the graph into four quadrants which should ideally separate the p- and n-mode from each other. Furthermore, the lines serve as guidance for the eye, easing the identification of shifts at elevated temperatures. The corresponding band diagram of each mode is shown in Figure 2.8, using the same separation into four quadrants.

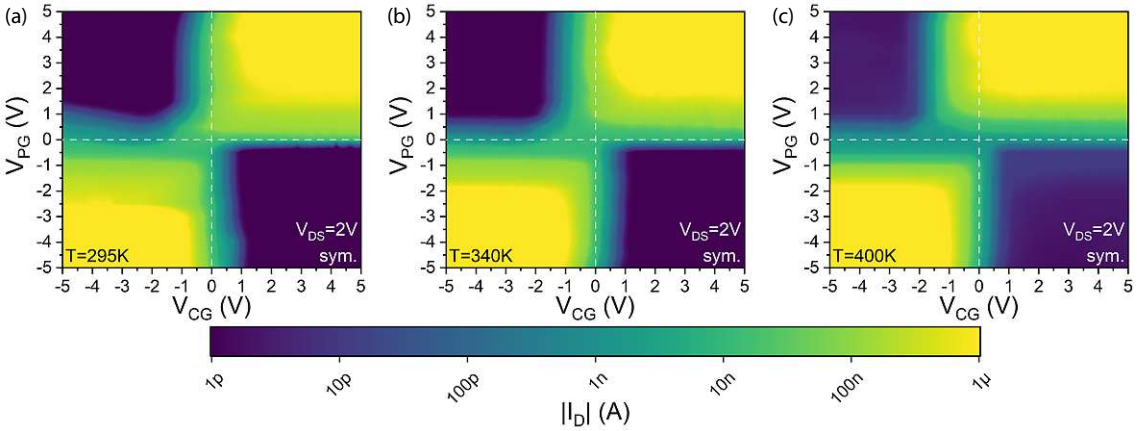

Figure 4.15: *GesSOI TTG: Polarity-gate characterization over temperature under same bias conditions.*
Measurement details for (a), (b) and (c): The control-gate voltage was varied from $V_{CG} = \pm 5V$ to $\mp 5V$ in $0.1V$ steps while the polarity-gate voltage was swept from $V_{PG} = \pm 5V$ to $\mp 5V$ in 0.5 steps. The bias voltage was set to $V_D = +2V$ and applied symmetrically to drain and source. The temperature of the sample was step-wise increased from room temperature to $T = 400K$.

Almost independent of the set temperature, on-state islands in quadrant one and three separated by off-regions in quadrant two and four are identified in subfigure (a-c) of Figure 4.15. Diagonally, for same control- and polarity-gate voltages, the on-regions are however connected by a narrow path of high drain currents.

At room temperature quadrant one is almost fully filled by high on-state currents, representing the n-mode for both positive polarity- and control-gate voltages. The p-mode on the other hand, located in quadrant three does not fill up the square defined by negative polarity- and control-gate voltages. For elevated temperatures, this however is changed and the n-mode outgrows quadrant one and extends to negative control-gate voltages in quadrant two. The p-mode however stays inside its quadrant even at $T = 400K$. The initially narrow diagonal connection of p- and n-mode further extends to negative control-gate voltages for $V_{PG} \approx 0V$. Furthermore, the overall off-state current increases with temperature.

Polarity-gate characterizations for same bias directional devices, as the TTG or any geometrically symmetric device with more than one top-gate, are especially helpful to identify operation regions in regard to control- and polarity-gate voltages. Note, that the polarity-gate sweeps shown in Figure 4.15 are merged together at $V_{PG} = -V_{CG}$, showing the respective on to off sweep in control-gate voltage, horizontal sweep, for each mode.

Rounding up the temperature investigation of the presented TTG devices fabricated on sample B is the effective activation energy (eAE) estimation, depicted in Figure 4.16. Therefore, the previously presented output measurements at varying bias voltages over a

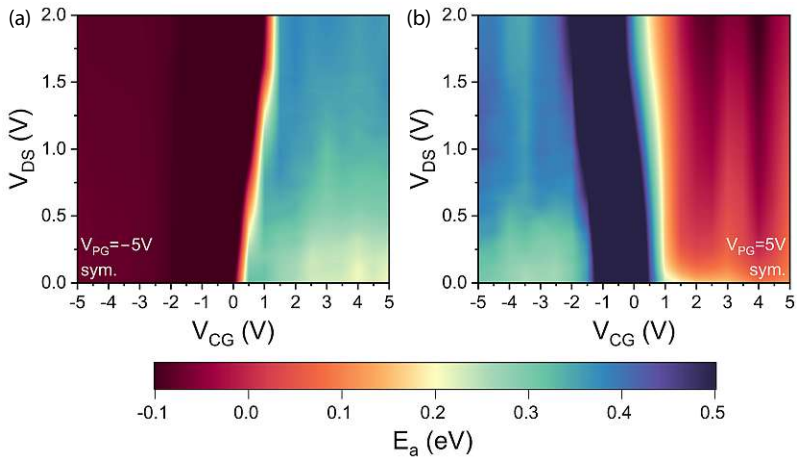

Figure 4.16: *GesSOI TTG: Effective activation energy plot for p- and n-mode.*

changing control-gate voltage were analyzed as discussed in Section 3.2.8. Resulting negative activation energies stand for a transparent injection barrier, also referred to as ohmic contact, while positive barriers resemble Schottky barriers, as illustrated in Figure 2.4. Depending on the presented barrier at the metal-semiconductor junctions, a lower or higher current flow is achieved.

Figure 4.16 shows the eAE evaluation of a TTG device on sample B, where subfigure (a) is configured for p-mode operation with a negative polarity-gate voltage of $V_{PG} = -5V$ and (b) for n-mode with $V_{PG} = +5V$. The expected low activation energy regions correlate with the high current regions of Figure 4.13 (b). Thereby, the transition regions from high to low energies are shifted with increased bias, endorsing the barrier thinning and the resulting increase in tunneling currents. These transition lines do not overlap with the respective threshold voltages, but rather with the initial increase of current flow. Interestingly, the high effective activation energy band around $V_{CG} = 0V$ for the n-mode in subfigure (b) is not observed for the corresponding p-mode in (a).

4.3.4 Electrical Characteristics of Multi-Gate RFETs

By adding another top-gate the functionality of the previously discussed TTG, in Section 4.3.3, can further be extended. The 4TG thereby has two individual control-gates, $CG1$ and $CG2$, as illustrated in Figure 2.7, overlaying the channel region, along with two polarity-gates over both metal-semiconductor junctions. The second control-gate enables an additional manipulation of the underlying Ge band structure and targeted control of charge carrier flow. As a result, standalone wired logics with only one transistor are feasible. Theoretically, even more top-gates can be added, further diversifying RFETs with N top-gates, allowing multiple input logic blocks. Note, that a comparatively longer Ge segment length is needed in order to fit the excess control-gates.

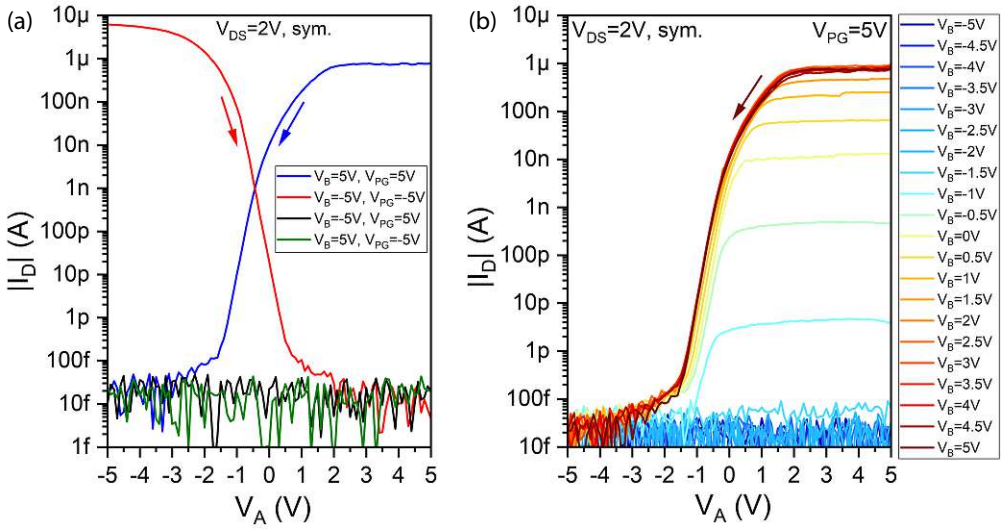

Figure 4.17: *GesSOI 4TG: Transfer characterization for various polarity-gate and input A and B voltages. (a): Transfer measurements for same and different sign polarity-gate and input B voltages over input A V_A. (b): Various input B voltages V_B at a fixed polarity-gate voltage of $V_{PG} = +5V$ over input A V_A.*
Measurement details for (a): V_A was varied from on- to off-state, $\pm 5V$ to $\mp 5V$, indicated by the arrows, in $0.1V$ steps. For (b) V_A was only varied from $+5V$ to $-5V$ and while the polarity-gate voltage was fixed at $V_{PG} = +5V$. The bias voltage for both measurements was set to $V_{DS} = 2V$ in symmetric fashion.

The presented 4TGs in this thesis have a top-gate arranged as presented in Figure 2.7, possessing two top-gates, $CG1$ and $CG2$ which are denoted with A and B, along with two physically connected polarity-gates. As mentioned in Section 3.2.6, concerning the measurement setup and procedure of the 4TG device characterization, the absolute drain current in dependence of the two input voltages A and B at constant polarity-gate and bias voltage is investigated.

Transfer measurements conducted on 4TG devices are illustrated in Figure 4.17 (a) for various V_A and V_B input- and V_{PG} polarity-gate voltages. Thereby, TTG-like curves for same sign input voltages V_A, V_B and polarity-gate voltages V_{PG} are observed. No distinct on-state current is obtained for disparate signs. Subfigure (b) on the other hand, depicts the electrical behavior of the 4TG set to n-mode operation, by $V_{PG} = +5V$, for various V_B input voltages over input A V_A. A gradual decrease in drain current I_D with decreasing V_B voltages is observed, resembling the functionality of a wired AND logic. Alternatively, the same measurement can also be plotted as colormap, as shown in Figure 4.18 (b). Thereby, the distinct high and low current regions are highlighted. Subfigure (a) of Figure 4.18 sketches the same variation of input B V_B over A V_A however for a fixed polarity-gate voltage of $V_{PG} = -5V$, resulting in a NOR type behavior.

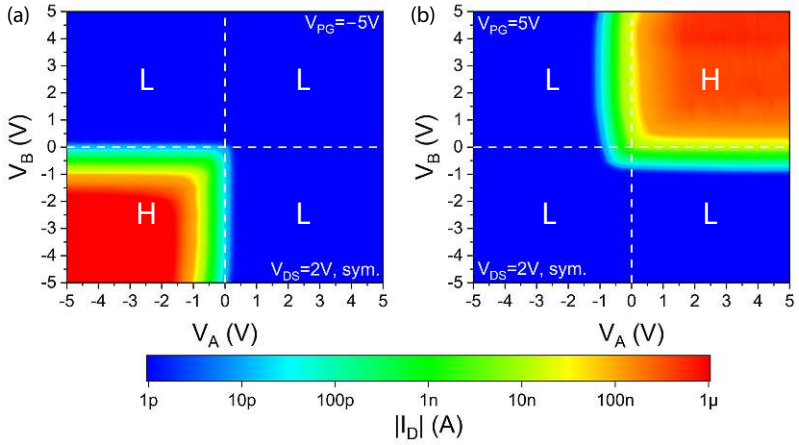

Figure 4.18: *GesSOI 4TG: Wired NOR (a) and AND (b) of a 4TG, configured in p- and n-mode, respectively. The white dashed lines at the center voltages of V_A and V_B separate the high and low current regions, indicated by H and L, which are representing logic 0 and 1 of the respective logic gate.*
Measurement details for (a) and (b): V_A and V_B were varied from on- to off-state, $\pm 5V$ to $\mp 5V$ in $0.1V$ and $0.5V$ steps, respectively. The bias was set to $V_{DS} = 2V$ and applied symmetrically to source and drain. The polarity-gate voltage was set to $V_{PG} = -5V$ for (a) and $V_{PG} = +5V$ for (b).

Logic truth tables for the presented logic gates in Figure 4.18 (a) and (b) are given in Table 4.10. Furthermore, a wired XNOR gate is also realizable with a TTG and its correspond polarity-gate and control-gate as input A and B, equivalent to the polarity-gate characterization presented in Figure 4.15. Moreover, the top-gate count is even less for the XNOR since it is a triple top-gate. With the addition of an RFET inverter, created out of two subsequent TTG (or DTG) devices, wired in analogue to its MOSFET counterpart [93], all basic logic blocks can be recreated with one 4TG and two TTGs or three TTGs [14, 94, 95].

Table 4.10: *Two-input truth table for a logic NOR, AND and XNOR gate, which can be reproduced by a 4TG RFET in p- or n-mode or a TTG RFET.*

Input A CG1/PG	Input B CG2/CG	NOR 4TG p-mode	AND 4TG n-mode	XNOR TTG w. PG and CG
0	0	1	0	1
0	1	0	0	0
1	0	0	0	0
1	1	0	1	1

4.3.5 Comparison of Transfer Characteristics

This section puts the obtained STG, DTG and TTG measurement results of Sections 4.3.1 to 4.3.3 into perspective by comparing the evaluation results side by side. Therefore, the transfer characterizations presented in Figures 4.5, 4.9 and 4.13 (a) are evaluated as discussed in Section 3.2.9. The obtained currents are either normalized to their respective nanosheet width W, stated as $I_{on/off}/W$, or cross section $W \cdot H$, where H is the height of the Ge layer which is $10nm$ for all samples, stated as J_{on}. Due to varying signs of the hysteresis between devices of one architecture, the absolute values are calculated.

In general a better electrical controllability, resulting in higher on-state and lower off-state currents along with steeper slops, is observed in Table 4.11 with increasing top-gates. Note the relatively high normalized off-state currents I_{off}/W of the presented STGs, which can be traced back to three devices Figure 4.5 (a), possessing high and left shifted off-state points.

Moreover, the obtained measurement results presented in Section 4.3.3 and Table 4.11 of nine TTG devices fabricated on sample B (GesSOI with SiO_2 & ZrO_2) are compared to other Al-Ge RFETs found in literature. Thereby, the effects of a 4nm, 10nm and 20nm thick Ge layer are put into perspective. However, these sample do not just differ in their respective Ge layer thickness but also in their base-substrate, gate oxide material and thickness, applied top-gate voltage and drain-source bias. As a result, a direct comparison between the samples is not fair and reasonable. However, Table 4.12 indicates a trend and puts the used material compositions into relation. Additionally, a comparison to Al-Si based TTGs is made, highlighting the characteristics of each semiconductor material for RFET applications.

Taking a closer look at the different Ge samples presented in [29, 60] revels that all were measured with a polarity-gate voltage of $V_{PG} = \pm 5V$ and a control-gate voltage range of $V_{CG_{range}} = \pm 5V$. The Al-Si sample on the other hand, possessing a higher EOT, was measured until $\pm 7V$ for PG and CG. However, all samples were measured with the same symmetric bias voltage of $V_{DS} = 2V$. The Al-Ge sample possessing a 20nm thick Ge layer also stands out by not using a SiO_2 dielectric layer along with its Ge on insulator GeOI platform. This however results in a virtually none existing n-mode with an On/Off ratio of $\approx$70.

However, venturing a wage comparison outlines the benefits of the presented GesSOI based RFETs of this thesis in terms of overall current density, On/On ratio, V_{th} symmetry and STHS. Thereby, the introduced platform is a valuable alternative to conventional Si based RFETs.

Table 4.11: *Transfer evaluation of STG, DTG and TTG devices operated under the identical conditions and fabricated on the same GesSOI platform with a SiO_2/ZrO_2 gate dielectric stack. Therefore, the mean value and standard deviation of six STG, eight DTG and nine TTG devices were calculated. Varying signs of the calculated hysteresis lead to false statistical results, therefore the absolute values are given.*

Sample B GesSOI	**STG (6)**		**DTG (8)**		**TTG (9)**	
	Mean	**Std.**	**Mean**	**Std.**	**Mean**	**Std.**
I_{on}/W n [$\mu A/\mu m$]	4,31	4,02	0,85	0,66	7,27	9,27
I_{on}/W p [$\mu A/\mu m$]	2,78	1,70	4,72	2,72	13,51	3,28
J_{on} n [$A/\mu m^2$]	$4{,}31{\cdot}10^{-4}$	$4{,}02{\cdot}10^{-4}$	$8{,}50{\cdot}10^{-5}$	$6{,}65{\cdot}10^{-5}$	$7{,}27{\cdot}10^{-4}$	$9{,}27{\cdot}10^{-4}$
J_{on} p [$A/\mu m^2$]	$2{,}78{\cdot}10^{-4}$	$1{,}70{\cdot}10^{-4}$	$4{,}72{\cdot}10^{-4}$	$2{,}72{\cdot}10^{-4}$	$1{,}35{\cdot}10^{-3}$	$3{,}28{\cdot}10^{-4}$
I_{off}/W n [$\mu A/\mu m$]	$1{,}35{\cdot}10^{-3}$	$2{,}34{\cdot}10^{-3}$	$1{,}31{\cdot}10^{-7}$	$6{,}07{\cdot}10^{-8}$	$1{,}58{\cdot}10^{-7}$	$2{,}19{\cdot}10^{-8}$
I_{off}/W p [$\mu A/\mu m$]	$1{,}04{\cdot}10^{-3}$	$1{,}78{\cdot}10^{-3}$	$8{,}47{\cdot}10^{-8}$	$7{,}78{\cdot}10^{-8}$	$1{,}56{\cdot}10^{-7}$	$4{,}06{\cdot}10^{-8}$
On/On	2,69	1,95	12,26	10,78	4,23	3,05
On/Off n	$1{,}30{\cdot}10^{6}$	$2{,}03{\cdot}10^{6}$	$5{,}52{\cdot}10^{6}$	$4{,}66{\cdot}10^{6}$	$3{,}69{\cdot}10^{7}$	$4{,}61{\cdot}10^{7}$
On/Off p	$3{,}19{\cdot}10^{6}$	$5{,}39{\cdot}10^{6}$	$7{,}07{\cdot}10^{7}$	$3{,}39{\cdot}10^{7}$	$8{,}31{\cdot}10^{7}$	$2{,}76{\cdot}10^{7}$
V_{th} n [V]	3,58	0,47	4,03	0,19	1,23	0,52
V_{th} p [V]	-3,69	0,30	-3,85	0,18	-2,23	0,15
|Hyst. n| [V]	0,25	0,32	0,22	0,11	0,50	0,60
|Hyst. p| [V]	0,18	0,12	0,07	0,05	0,10	0,08
STHS n [mV/dec]	677,9	255,0	468,2	69,4	429,1	40,8
STHS p [mV/dec]	-386,6	96,7	-294,4	21,0	-268,9	25,8

Table 4.12: *Comparison of the evaluated TTG RFETs of Sample B (GesSOI with SiO_2 & ZrO_2) to other Al-Ge TTG RFETs in literature. Furthermore, a comparison to Al-Si TTG RFETs based on a SOI wafer is made, highlighting the benefit of the used GesSOI substrate. Note, that the presented values are average values of nine or ten representative TTG devices on each platform.*

Material System: **Channel height:** **Source:**	**Al-Ge** **10nm Ge** **Sample B**	**Al-Ge** **4nm Ge** **[60]**	**Al-Ge** **20nm Ge** **[60]**	**Al-Si** **15.4 nm Si** **[59]**
Platform	GesSOI	Ge on SOI	GeOI	SOI
Oxide	SiO_2 | ZrO_2	SiO_2 | ZrO_2	GeO_x | Al_2O_3	SiO_2
Thickness [nm]	5 | 2.8	9 | 3.2	11	12.4
Relative permittivity ϵ_r	3.9 | 27	3.9 | 27	9.31	3.9
EOT [nm]	5.40	9.46	4.60	12.40
I_{on}/W n [μA/μm]	7.27	3.74	0.04	6.20
I_{on}/W p [μA/μm]	13.51	6.47	10.66	11.80
J_{on} n [A/μm^2]	$7.27{\cdot}10^{-4}$	$9{,}36{\cdot}10^{-4}$	$2{,}00{\cdot}10^{-6}$	$4{,}16{\cdot}10^{-4}$
J_{on} p [A/μm^2]	$1.35{\cdot}10^{-3}$	$1{,}62{\cdot}10^{-3}$	$5{,}33{\cdot}10^{-4}$	$7{,}87{\cdot}10^{-4}$
I_{off}/W n [μA/μm]	$1.58{\cdot}10^{-7}$	$1.32{\cdot}10^{-5}$	$6.85{\cdot}10^{-4}$	$3.00{\cdot}10^{-7}$
I_{off}/W p [μA/μm]	$1.56{\cdot}10^{-7}$	$1.98{\cdot}10^{-7}$	$9.08{\cdot}10^{-4}$	$2.80{\cdot}10^{-7}$
On/On	4.23	1.96	120.30	1.90
On/Off n	$3.69{\cdot}10^{7}$	$2.00{\cdot}10^{7}$	$6.98{\cdot}10^{1}$	$2.10{\cdot}10^{7}$
On/Off p	$8.31{\cdot}10^{7}$	$3.00{\cdot}10^{7}$	$2.10{\cdot}10^{4}$	$4.20{\cdot}10^{7}$
V_{th} n [V]	1.23	0.32	1.34	1.80
V_{th} p [V]	-2.23	-1.24	-0.01	-2.80
STHS n [mV/dec]	429.1	557.7	752.6	480.0
STHS p [mV/dec]	-268.9	-275.6	-407.1	-336.0

Chapter 5

Summary and Outlook

In the thesis at hand, a comparison of Ge on SOI and sSOI based reconfigurable FET structures is given. Depending on the fabricated sample, the wafer stack had a 10 nm thick Ge layer grown on top of a SOI or a sSOI substrate, which were fabricated by our project partner. The MBE grown Ge layer was covered with a 3nm thick Si capping layer, acting as a sacrificial layer allowing the formation of a low trap density Ge-SiO_2 dielectric interface. In order to form the underlying metal-semiconductor-metal heterostructure, or in the case of this thesis the Al-Ge-Al heterostructure, thermally activated solid-state diffusion of Al into the Ge nanosheet was used, resulting in two abrupt, reliable and reproducible Al-Ge transitions at each end of the nanosheet. The nanostructure is either passivated with dry thermally grown SiO_2 only or with SiO_2 in combination with the high-k dielectric ZrO_2, deposited by ALD. As stated in the project evolution section, Section 4.2, three different samples were fabricated, two out of the sSOI wafer stack, one with a SiO_2 only and the other with an added ZrO_2 dielectric layer atop, and one out of the SOI base-substrate with SiO_2 and ZrO_2. The electrical behavior of all three samples was analyzed and discussed while sample B was thoroughly investigated and characterized over temperature, since it had the best performance in terms of on-state current densities, on to off ratios and threshold voltage. Depending on the Ge segment length, either single top-gated SBFETs or RFETs with two, three or four top-gates were realized.

The three distinct samples, which differ in their respective base-substrate and gate dielectric, were compared in terms of their STG, DTG and TTG transfer behavior and evaluation results. The temperature dependent electrical characterization of the RFET structures fabricated on sample B included transfer curves and output measurements for STG, DTG and TTG device architectures along with polarity-gate characterizations, highlighting the mode switching behavior of DTGs and TTGs in dependence of the applied top-gate voltages. Furthermore, the associated effective Schottky barrier heights (eSBH) and effective activation energies (eAE) were extracted from the STG and TTG Output meas-

urements conducted at temperatures ranging from $T = 295K$ to $400K$. The related RFET parameters were extracted within a $5V$ top-gate voltage range and for a bias voltage of $V_{DS} = 2V$. Thereby, the bias voltage of STGs, TTGs 4TGs was applied symmetrically to drain and source, while the bias of DTG devices was applied asymmetrically to drain while the source potential was grounded.
Since the presented samples either differ in their underlying base-substrate or used gate dielectric while the remaining fabrication process and electrical characterization were the same, a direct comparison between the three samples highlights the influence of each material combination. In general, the sample fabricated out of the sSOI wafer stack in combination with the SiO_2/ZrO_2 gate dielectric outperformed the other samples in terms of on- and off-state currents for both p- and n-mode resulting in higher on to off ratios along with symmetric threshold-voltages and improved subthreshold slopes. However, the sample based on the SOI substrate possessing the same SiO_2/ZrO_2 gate stack, had the lowest hysteresis of all investigated device architectures. This is unexpected, because the main source of defect states was believed to be at the SiO_2 - ZrO_2 interface, which is however present for both samples. Thus, the Ge - SiO_2 interface seems to be effected by the underlying Si layer of the base-substrate and the resulting stress. Furthermore, the DTG devices fabricated from the SOI substrate had the comparably lowest STHS for both p- and n-mode among this device architecture. The considered 4TG devices revealed sharp and steep on- and off-state transitions, preferable for wired logic applications.
Considering the extensive bias spectroscopy over temperature analysis for STG, DTG and TTG devices fabricated on the sSOI base-substrate with a SiO_2/ZrO_2 passivation, a general increase in on- and off-state currents with rising temperatures is noticed, while the threshold voltage of both modes is shifted towards $V_{TG/CG} = 0V$. Since the off-state currents increase by several orders of magnitude from room-temperature to $T = 400K$ while the on-currents just double, the on to off ratios decrease and the subthreshold slope flattens at elevated temperatures. Interestingly, the sign of the n-mode hysteresis of STG, DTG and TTG devices arbitrary flip over temperature, indicating lower and higher back sweeping currents (BSC) in contrast to the constant positive sign, resembling a higher BSC, of the p-modes.
In order to set the obtain TTG RFET characteristics into perspective, a comparison to other Al-Ge based RFETs comprising either thinner or thicker Ge layers and Al-Si RFETs is conducted. Thereby, the sSOI based Al-Ge RFET sample, fabricated in the scope of this thesis, stands out by the highest p- and n-mode on-state current normalized to the nanosheet width I_{on}/W along with the lowest normalized off-state currents. This results in on/off state ratios of more than seven order of magnitude. Despite a slightly lower current density in comparison to the Al-Ge RFET sample possessing a similar wafer stack however only a 4 nm Ge layer, the subthreshold slope of the presented material system is the lowest among the comparison. Generally, the fabricated RFET sample indicates improvements in every aspect, except the on to on symmetry, in comparison to its Al-Si counterpart. This slight increase in asymmetry is probably caused by a none centered pinning level of the underlying Al-Si-Ge interface, as discussed in Section 2.3.1.

From the perspective of the semiconductor industry, there's a clear advantage in fabricating transistor devices at wafer-scale using a top-down approach as the Ge RFETs presented in this thesis. The importance of on-state symmetry is highlighted when considering reconfigurable circuits and the noted size discrepancies between n- and p-MOS transistors in CMOS technology. Since both p- and n-mode of an RFET are combined in one single device, the resulting transistors are of equal dimensions. Furthermore, a reliable and stable fabrication process, particularly for the formation of the metal-semiconductor junctions, like the introduced thermally activated Al diffusion, is crucial. Additionally, the capability to dynamically switch the operational mode during runtime enables efficient logic circuits with fewer transistors. The symmetry observed for the Ge RFETs presented in this thesis are primarily caused by the underlying material system of the base-substrate, eliminating the need to additional strain engineering [13, 14, 21].

Providing an outlook, there are still certain aspects of the presented material system that can be investigated, in order to obtain an extensive understanding of the underlying properties. For instance, the influence of the exerted stress on the Ge channel layer, effecting the electrical device behavior, can be determined by various Ge contents in the SiGe seed layer of the strained Si layer. Furthermore, the fabrication process can be made CMOS compatible by replacing Au with Al as top-gate metal, which would probably improve the device degradation over time and temperature. Given the possibility of single transistor RFET logic's, like the presented two input AND, NOR and XNOR gates, the next step is to establish complex logic circuits comprising Al-Ge based RFETs overcoming the possibilities of traditional CMOS technology.

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