Reconfigurable Si Field-Effect Transistors With Symmetric On-States Enabling Adaptive Complementary and Combinational Logic

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***Abstract*— Reconfigurable field-effect transistors (RFETs), combining n- and p-type operation in a single device, have already shown promising simulation results for enhancing performance and functionality in conventional devices and further enabling novel adaptive computing concepts. With recent advances in the formation of high-quality monolithic and single-crystalline Al-Si Schottky contacts providing a reproducible way to fabricate RFETs with highly symmetric n- and p-type operation, we are now able to demonstrate their integration in fundamental complementary and combinational logic circuits. In this regard, we show an inverter, as well as NAND/NOR and XOR/XNOR gates, capable of dynamically run-time switching their operation mode, while simultaneously reducing transistor count compared to conventional circuits with static transistors. Importantly, we could demonstrate their reliable operation using only fully symmetric supply voltages while providing a full output swing. Their robust operation is verified by analyzing their noise margins, stability to input voltage variations, and transient behavior. Most notably, the presented device concept and the Al–Si material system are potentially compatible with the state-of-the-art complementary metal–oxide–semiconductor (CMOS) processing technology, paving the way for future hybrid reconfigurable-CMOS circuits with improved functional density and energy efficiency.**

***Index Terms*— Combinational logic, reconfigurable field-effect transistors (RFETs), reconfigurable transistor, Schottky barrier field-effect transistor (SBFET), silicon-on-insulator (SOI).**

I. Introduction

PERFORMANCE enhancement and improved energy efficiency are important aspects for the further development of the existing high-end integrated circuits. Therefore, driven by Moore's law, transistor scaling and geometry optimization have been the main approaches to increase functional density in the last decades, but these are slowly approaching physical limits [1]. In this regard, transistor concepts capable of increasing functionality by run-time alteration of their device characteristics have recently emerged as alternative concepts. Thereto, polarity-controlled transistors implemented in efficient designs are capable of reducing physical resources within the integrated circuit, boosting its functional space while reducing its power consumption [2], [3], [4]. Such reconfigurable field-effect transistors (RFETs) combine unipolar n- and p-type transistor characteristics in a single electrically run-time programmable device [5], [6], [7], [8], [9]. As a result, a vast functionality increase is gained compared to conventional complementary metal–oxide–semiconductor (CMOS) technology, where the characteristic of each transistor, and therefore each logic cell, is static and predefined by its physical properties and interconnect layout during fabrication. This enables the efficient implementation of highly flexible logic circuits that can be dynamically reprogrammed at run-time in a recursive learning routine to change their function and be optimized for the desired application, highly promising for convolutional neural networks [10], [11]. In addition, RFETs allow intrinsic and therefore efficient implementation of XOR and majority (MAJ) gates, even with a large number of inputs, which are advantageous for the computation of many arithmetic operations but are very complex and inefficient to implement in conventional CMOS. Moreover, the integration of RFETs and intelligent circuit design can significantly reduce the number of transistors required for the same functionality, which not only has a positive effect on energy efficiency but also reduces the required chip area and the circuit delay [12]. Using an optimized design automation framework for RFETs, area and delay savings of 22%–42%, respectively, have been predicted for digital circuits [3]. Furthermore, RFETs show high potential in a broad field of applications concerning emerging hardware security solutions [13], [14], [15], as it is possible to design complex generic building blocks that can host numerous functions, which are merely defined by electrical program signals. Additionally, RFETs are gaining interest in analog circuitry [16], [17], [18].

Manuscript received 7 August 2023; revised 20 October 2023; accepted 19 December 2023. Date of publication 4 January 2024; date of current version 24 January 2024. This work was supported by the Austrian Science Fund (FWF) under Project I5383-N. The review of this article was arranged by Editor L. Ge. *(Corresponding author: Masiar Sistani.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2023.3346361.

Digital Object Identifier 10.1109/TED.2023.3346361

However, most previous studies on RFET-based logic circuits have focused on simulations rather than their physical implementation, since their proper integration requires high symmetry of both operating modes, as well as a reasonable yield in lab-scale device fabrication [4], [12], [19]. So far, most realized reconfigurable circuits are based on complex material compositions or concepts that are difficult to scale and implement in a modern CMOS design flow [20], [21], [22]. In this regard, recent advances in the formation of abrupt and high-quality Schottky junctions based on a thermally induced exchange reaction between Al and Si have proven to provide reproducible Schottky barrier field-effect transistors (SBFETs) [23]. Although in modern CMOS technology bulk Al has been abandoned and replaced by other metals due to problems with electromigration and contact spiking [24], [25], in our nanosheet devices, we observe flat and void free interfaces even after extended measurements [23]. Utilizing these single elementary Al–Si–Al heterostructures, RFETs with highly symmetrical transistor current–voltage subthreshold transfer characteristics for both n- and p-type operation in terms of on/off currents, threshold voltages, and subthreshold slopes have been observed [26]. This high degree of symmetry is achieved without additional measures, such as doping or strain engineering [27], [28], [29], as the Al–Si material system inherently has relatively symmetrical effective Schottky barrier heights for both electrons and holes [23], [26]. Importantly, a low device-to-device variability has been demonstrated, suitable for the larger scale integration into logic circuits.

II. Device Description

In this article, we report on the potentially CMOS compatible integration of top–down fabricated RFETs in reconfigurable logic gates that are already showing their key advantages to conventional complementary logic in terms of flexibility and simplicity. Therefore, fundamental RFET-based logic gates, such as complementary inverters, reconfigurable NAND/NOR gates, and intrinsic XOR/XNOR gates, are presented together with their static operation voltage stability ranges. A single RFET is shown in the false-color scanning electron microscopy (SEM) image in Fig. 1(a), with its three independent metal top gates (here made of Ti/Au for simplicity in our lab, but transferable to TiN since Ti and TiN have similar metal work functions), Al source and drain contacts, and the indicated lowly p-doped Si channel (ρ = 9–15 Ω cm). The key process steps are summarized in Fig. 1(b). The devices are based on top–down fabricated Si nanosheets, patterned from silicon-on-insulator (SOI) substrate with a 20-nm device layer. These Si nanosheets with an average structure width of $W = 420$ nm are then passivated by a 10.5-nm-thick thermally grown SiO_2 shell with a remaining Si layer thickness of 17 nm. For the fabrication of the source and drain contacts, the oxide on the contact area of the nanosheet is first removed using BHF etching, followed by 125-nm-thick Al sputter deposition. To form the high-quality metal–semiconductor junctions, rapid thermal annealing (RTA) at 774 K in forming-gas atmosphere is performed to induce the Al–Si solid-state exchange reaction. Thereby, Si is diffusing into the Al and is replaced by Al, resulting in a shortened Si channel, contacted by

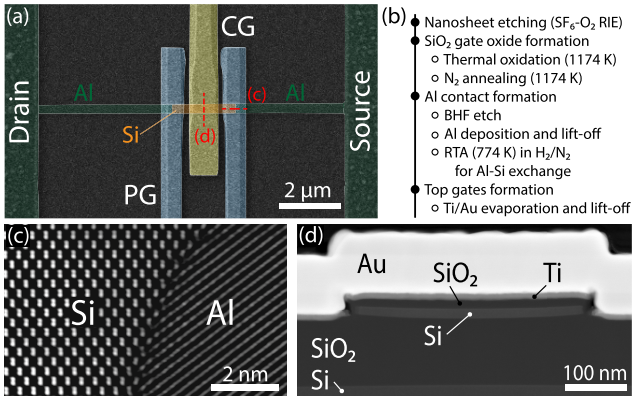

Fig. 1. (a) Colored SEM image of a three top-gate RFETs based on an Al–Si–Al heterostructure. (b) Process scheme for the fabrication of the proposed devices. (c) FFT-filtered HRSTEM image of the Al–Si interface. (d) Cross-sectional HRSTEM image showing the gate-stack of the RFET.

crystalline, single-elementary Al leads [23]. A cross section of the atomically sharp Al–Si junction is shown in the fast Fourier transform (FFT) filtered high-resolution scanning transmission electron microscopy (HRSTEM) image in Fig. 1(c). Importantly, no intermetallic phases are formed, overcoming the difficulty of complex growth kinetics of the state-of-the-art metal silicides and reducing process variability and yield issues. Therefore, several subsequent annealing steps can be performed to control the length of the remaining Si channel without complex phase transitions [23], [30], in contrast to Ni silicides [31], [32]. Furthermore, due to the absence of grain boundaries in the single-crystalline Al leads, we believe that electromigration of grain boundaries in Al should be sufficiently suppressed [24]. On top of the Al contacts in the S/D region, other metals, such as W or Cu with TiN or TaN diffusion barriers [33], can be deposited for the interconnects to the individual devices. To electrostatically control the RFET, two electrically independent omega-shaped top gates are fabricated atop the Al–Si–Al heterostructure. The complete gate-stack, showing the Si channel on top of the BOX of the SOI substrate, the SiO_2 gate oxide, and the Ti/Au top gate, is shown in the cross-sectional HRSTEM image in Fig. 1(d). The polarity gate (PG) is placed directly atop both Al–Si interfaces, allowing a precise tuning of the injection barrier. This allows the selection of the desired carrier type to be effectively injected into the semiconductor channel while blocking the other carrier type. Importantly, a small overlap of the PGs over the interface is necessary for a sufficient control of the barrier and to ensure low off currents and parasitic capacitances [34]. With the control gate (CG) atop the Si channel, the channel barrier can be electrostatically tuned to control the current flow through the device as in a regular MOSFET. This three top-gate design allows the Schottky and channel barriers to be controlled independently, resulting in superior polarity control and therefore improved RFET characteristics compared to a two top-gate architecture [35]. The electrical characteristic of a single RFET is shown in Fig. 2(a). At positive voltages at the PG (V_{PG} = 4 V), indicated by the red curves, the RFET operates as an n-type FET with an electron-induced current flowing at positive voltages at the CG. The holes are efficiently blocked by the emerging barriers, resulting in very low off

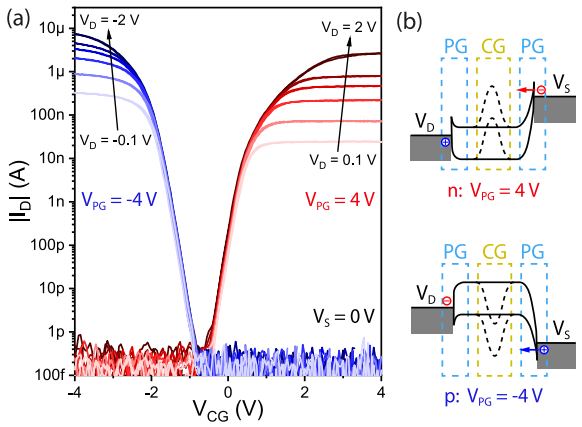

Fig. 2. (a) Transfer characteristic of the RFET in p (V_{PG} −4 V) and *n* configuration (V_{PG} = 4 V), for V_D between ±100 mV and ±2 V. The curves are swept in both directions, showing almost no hysteresis. (b) Schematic illustration of the energy band diagrams for both operation modes.

currents at negative V_{CG} by an effective reduction of reverse junction leakage. The p-mode is enabled at $V_{PG} = -4$ V and negative bias voltages, resulting in efficient hole conduction and blocking of electrons. Note that the inverted bias for the p-mode results in a comparable modulation of the barriers to allow a better comparison between the two modes. The energy band landscape for both modes is illustrated in Fig. 2(b). By increasing the bias voltage between $V_D = \pm$ 100 mV and ± 2 V, the on currents can be further tuned to optimize the symmetry for both operation modes, reaching an on-current ratio I^p_{on}/I^n_{on} of 5.7 and 2.8 for $V_D = 1$ and 2 V, respectively. Remarkably, the device characteristics show no hysteresis due to the high quality of the Si–SiO_2 gate dielectric and the Al–Si interfaces.

III. Circuit Operation

A. Complementary Inverter

By connecting two of the proposed RFETs in series, a complementary inverter can be realized. Exploiting the thermal Al–Si exchange reaction, the RFET-based inverter can even be fabricated from a single Si nanosheet, in which the Si below the Al output contact has been completely exchanged, as shown in the colored SEM image in Fig. 3(a). In contrast to conventional CMOS, where the interconnection of two transistors with different doping schemes and channel dimensions is mandatory, the inverter is realized with RFETs that are nominally identical in dimension and composition and are programmed to operate in an n-type (pull-down) or p-type (pull-up) configuration by the choice of a positive or a negative voltage V_{PG} on the PGs, respectively. Note that the chosen convention of $V_{SS} = -V_{DD}$ is used for presentation purposes, making the p- and n-type operation clearer. Realization with $V_{SS} = 0$ V = GND is feasible by shifting the entire operation region, meaning that operation with the supply signals V_{DD} and GND is possible. This is a crucial aspect for circuit designers, as only the two logic high- and low-voltage levels can be used to ensure a proper operation, simplifying the circuit layout and obviating the need to generate additional supply voltages. The input voltage V_{IN} is applied to the connected CGs of the two RFETs and the output signal V_{OUT} is read at the common

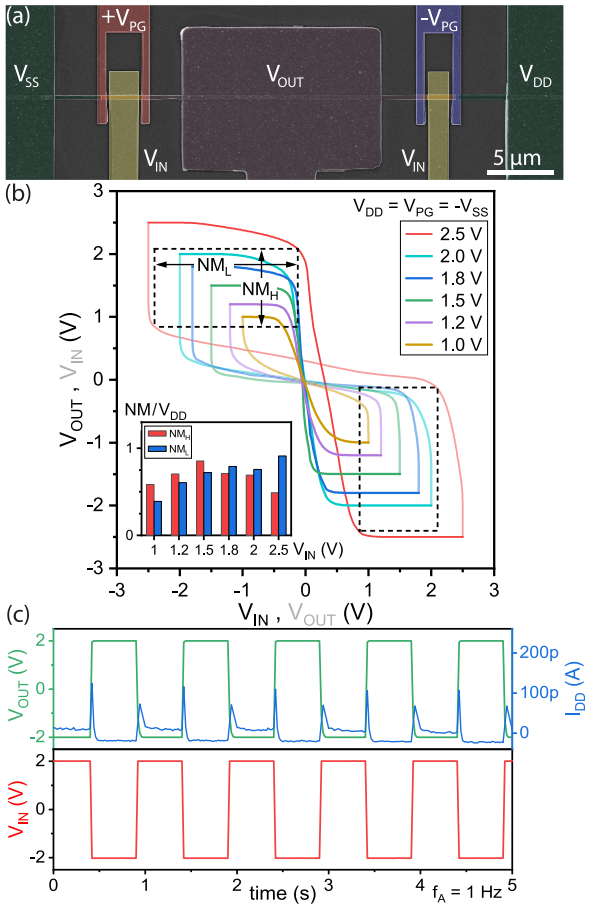

Fig. 3. (a) Colored SEM image of a complementary inverter based on two RFETs. (b) Inverter voltage transfer characteristic for various voltage levels ranging from 2.5 V down to 1 V. V_{IN} and V_{OUT} are plotted interchangeably to evaluate noise margins (NM_L and NM_H), which are shown in the inset, normalized to the different operation voltages. (c) Transient operation of the proposed inverter at a symmetric logic level of ±2 V showing the inverted output signal V_{OUT} and the current I_{DD}.

node connecting both RFET drain regions. The related inverter voltage transfer characteristic, with the output voltage V_{OUT} over the input voltage V_{IN}, is given in Fig. 3(b) for various symmetrically applied voltage levels. Remarkably, the voltage levels ($V_{DD} = V_{PG} = -V_{SS}$) can be varied from ±2.5 V down to ±1 V, while still retaining a symmetric full-swing output with a sharp transition between the two logic states. Adding the output characteristic with interchanged axes into the same plot allows to determine the noise margins for both the logical low (NM_L) and logical high state (NM_H) [36]. The captured noise margins normalized to the operation voltage for various symmetrically applied voltage levels are presented in the inset of Fig. 3(b). High and symmetric noise margins are achieved, especially for operation voltages between ±2 V and ±1.5 V with $NM_{H,L}/V_{DD}$ from 0.7 to 0.85, allowing a more robust and reliable operation. Accordingly, Fig. 3(c) shows the transient behavior of the inverter operated at ±2 V, with the input voltage V_{IN} and the inverted output voltage V_{OUT}. A negative input–output voltage level (−2 V) is thereby considered a logic "0," and positive voltages (2 V) are considered a logic "1." Therefore, the RFET-based inverter provides a full swing of the output voltage, while retaining a low rail to rail cross-current flow, with low peaks in the range of 100 pA only

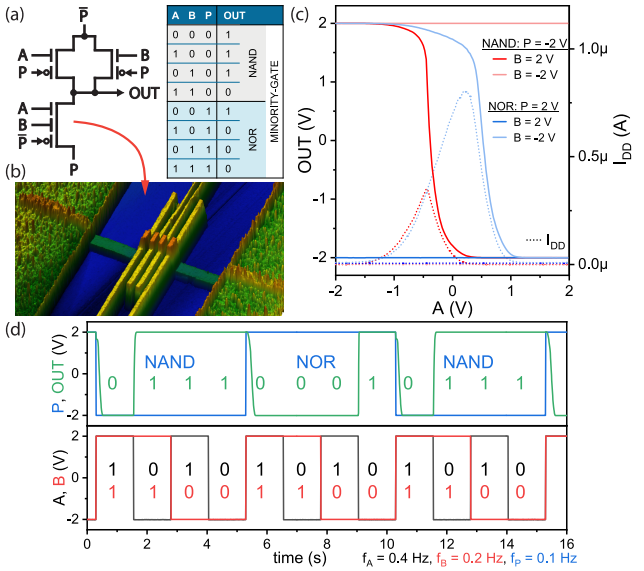

Fig. 4. (a) Schematic of the reconfigurable NAND/NOR gate, including the logic table for NAND, NOR, and minority gate operation. (b) Lower transistor features an additional CG, realizing a wired-AND, shown in the AFM-scan. (c) Transfer characteristic of the logic cell for NAND ($P = -2$ V) and NOR operation ($P = 2$ V). (d) Time-resolved circuit response depending on the input signals A and B and the polarity P at a symmetric logic level of ± 2 V.

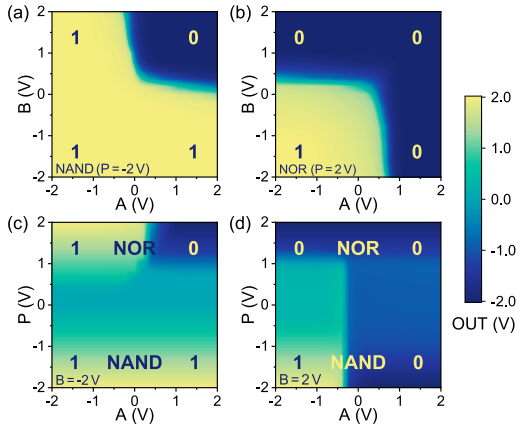

Fig. 5. Color maps showing the switching operation of the reconfigurable NAND/NOR gate. (a) NAND and (b) NOR operation; the inputs A and B are varied to change the output voltage. (c) and (d) Input B is fixed to -2 and 2 V, respectively, and P is varied to continuously switch between NAND and NOR mode.

when switching the output stage, which is typical for a complementary circuit design. Note that the slow switching frequency of 1 Hz was used since our lab-based technology forces us to use large and planar interconnect lines within the same layer as the devices, exhibiting the disadvantages of having extremely high parasitic capacitances. Nevertheless, mixed mode TCAD simulations of Si RFETs in logic circuits have already proven that the operation of RFET-based ring oscillators in the gigahertz region having a proper interconnect technology is feasible [34].

B. Reconfigurable NAND/NOR Gate

To take further advantage of the flexibility of the RFET, a reconfigurable logic gate capable of run-time switching between NAND/NOR operation can be built with only three RFETs. In Fig. 4(a), the schematic and its corresponding truth table are shown. The polarity of the circuit and therefore its operation mode can be set using the signal P and its inverted signal $\bar{P} = -P$ that are connected to the PGs of the RFETs and the supply voltages V_{DD} or V_{SS}. The input signals A and B are applied on the CGs. Again, only a single, symmetric voltage level is used for its operation, retaining its functionality in the range of ± 1.2–± 2.5 V. Note that the bottom transistor features an additional CG between the PGs, realizing a wired-AND gate with two input signals. This structure therefore merges two RFETs in series into one device, with a current only flowing when all gates are on the same logic level [26]. An atomic force microscopy (AFM) scan of this four top-gate structure is depicted in Fig. 4(b). The ability to replace multiple transistors with these multigate structures is another feature of this RFET architecture and also contributes to further reducing the transistor count in the circuit. Using P and $\bar{P}$ as a logic input, this circuit can be operated as a three-input minority (3MIN) transmission gate, further demonstrating its flexibility. Compared to a NAND or NOR gate implemented with four conventional static transistors, the proposed RFET-based gate uses fewer transistors while significantly increasing its functionality. The measured transfer characteristic of this reconfigurable circuit in Fig. 4(c) for operation voltages of ± 2 V exhibits a full swing operation with very sharp transitions between the output states, both for NAND ($P = -2$ V) and NOR operation (2 V). Furthermore, the currents I_{DD} are properly suppressed at the defined output states, with values as low as 0.2 and 6 nA for NAND and NOR mode, respectively, while small current peaks of up to 0.35 μA and 0.8 μA occur at the state transitions. Fig. 4(d) shows the transient behavior of this reconfigurable circuit. A sequence of input signals is applied to the inputs A and B, as well as the polarity P and $\bar{P}$, demonstrating not only the reliable switching operation within a single logic configuration but also its capability of dynamic reconfiguration when switching between NAND/NOR operation and thus the operation of a 3MIN transmission gate.

To further demonstrate the stability and operation window of the proposed RFET-based circuit, color maps based on a wide range of current voltage measurements are plotted in Fig. 5, showing the output voltage in relation to the voltages at the inputs A and B and the polarity P. Remarkably, the output remains very stable at ± 2 V over a wide range of input voltages, providing a very robust operation against voltage fluctuations at the inputs as well as large noise immunity. The transitions between NAND and NOR operation in Fig. 5(c) and (d) are not as sharp and distinct as for switching between the individual states within the NAND/NOR gate, since P not only controls the voltage on the PGs but also flips the supply rail voltages of the circuit. Therefore, the output level is directly affected by small changes in the voltage level at P.

C. Reconfigurable XOR/XNOR Gate

Similar to the inverter and the NAND/NOR circuit, RFETs offer the potential to realize even more sophisticated logical circuits, such as the XOR/XNOR, which are notably more complex to implement in common CMOS [3]. According to the given circuit for the two-input XOR logical gate in

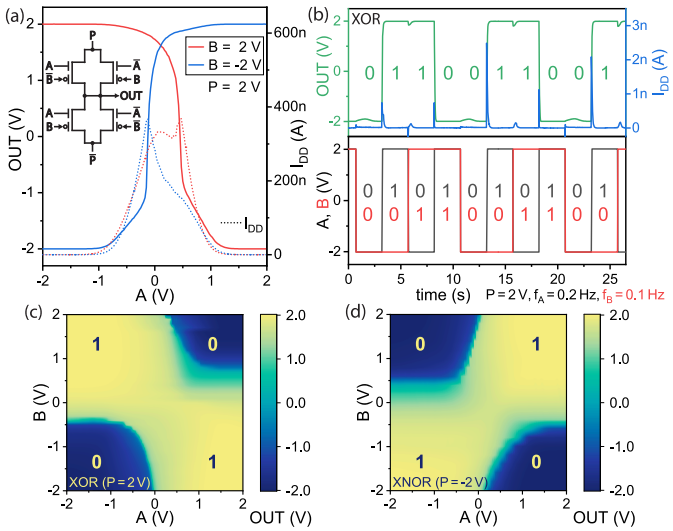

Fig. 6. (a) Output characteristic of the XOR gate for B = 2 V and −2 V. The current flow I_{DD} through the device is indicated by the dotted line. The schematic of the XOR/XNOR gate is shown in the inset. (b) Transient operation of the XOR gate. (c) and (d) Output maps for varied input levels A and B, in XOR ($P = 2$ V) and XNOR ($P = -2$ V) configuration.

the inset of Fig. 6(a), the PGs and CGs are connected to the input signals A and B or their inverted signals $\bar{A}$ and $\bar{B}$. Additionally, the drain and source pads are associated with P and $\bar{P}$ and the output OUT. Compared to XOR gates in conventional CMOS topologies, the implementation with RFETs can already reduce the number of transistors by half, resulting in reduced path delays and power consumption. As the number of inputs increases, these benefits become even more significant [12]. In addition, due to the flexible nature of RFETs, the entire circuit can be inverted via the polarity input P, further increasing functionality over static CMOS. Thus, this circuit can be switched between an XOR and XNOR mode during run-time by setting P to positive or negative voltages, respectively. With P used as an additional logic input, a three-input XOR transmission gate is obtained [3]. For the electrical characterization of the proposed logic gate, fully symmetric operation voltages of ±2 V were chosen, with 2 V as logical high and −2 V as logical low. Accordingly, Fig. 6(a) shows the output voltage level as a function of the applied input A at fixed input levels B in the XOR configuration ($P = 2$ V). Again, a full swing of the output voltage is provided, with sharp and well-centered transitions between the logic states, crossing OUT = 0 V at $A = -0.12$ and 0.45 V for $B = -2$ and 2 V, respectively, despite the need of adjusting the rail polarity by dedicated RFETs. Peak switching currents in the range of 380 nA arise, while at the distinct output states, the current flow through the circuit is well suppressed, with $I_{DD} < 30$ pA. Fig. 6(b) demonstrates the stable transient operation of this XOR gate, with the output voltage OUT switching to a logic "1" when only one of the two inputs A or B is set to "1" and with only small current peaks during the state transitions. As carried out above for the NAND/NOR circuits, sweeping both input voltages and plotting the recorded values in color maps allows to make more general assessments regarding the stability of the device operation and functionality, particularly with respect to voltage variations within the circuit. Therefore, Fig. 6(c) and (d) shows the output voltage levels resulting from varying the applied input voltage levels of an XOR and XNOR operation, with P set to 2 and −2 V, respectively. With respect to the four distinct high or low areas in both color maps depending on the logic operation and the applied input voltage levels, it is quite remarkable that the same circuit can exhibit both very stable XOR and XNOR functionality due to the reconfigurability of the RFET structures. The analyzed NAND/NOR and XOR/XNOR gates can be viewed as building blocks for generic hardware security circuits [13], [14], [15].

IV. Prospects Toward Performance Enhancements

Various works have analyzed the scaling and enhancement behavior of the RFET devices by device TCAD simulations. Gore et al. [37] have used a 10-nm Si nanowire technology and developed a respective process development kit (PDK) showing enhanced performance. Baldauf et al. [34] have systematically analyzed the scalability of Si and Ge nanowire RFETs by considering the different tunneling and thermionic electronic injection regimes and benchmarking their ring-oscillator frequency versus power consumption. More recently, Quijada et al. [38] analyzed the performance of Ge nanowire RFET circuits considering a 14-nm FinFET PDK, showing improved latencies versus Si RFETs. Certainly, in our Al–Si–Al nanosheet RFETs, the inverse subthreshold slope, threshold voltages, and operation voltages can be reduced to lower the dynamic power consumption without compromising static power consumption by improving the device gating electrostatics. Appropriate measures are a reduction of the Si channel thickness, the introduction of gate-all-around (GAA) gating, and the decrease of the effective oxide thickness of the gate-stack, e.g., by the use of high-κ dielectrics [39]. Also, the replacement of the Si channel with lower bandgap materials, such as SiGe [39] and Ge [40], [41], helps in reducing dynamic power consumption while maintaining a manageable static power consumption due to the inherent blocking barrier behavior imposed by the RFET's program gate.

V. Conclusion

We have reported a potentially CMOS compatible integration of RFETs based on Al–Si–Al heterostructure sheets exhibiting inherently high $I - V$ symmetry between n- and p-type operation, thereby enabling reconfigurable complementary and combinational logic. Fundamental logic gates, such as inverters and reconfigurable NAND/NOR as well as switchable XOR/XNOR gates, are demonstrated that can be operated with a single symmetrical voltage level over a wide voltage range from 2.5 V down to 1.2 V, simplifying the circuit layout. Thereby, a full output swing with sharp state transitions is provided, while the current flow at the defined states is well suppressed due to the complementary circuit design. Furthermore, their reliable operation is demonstrated, showing large noise margins and highly stable output characteristics with respect to input voltage variations. In particular, the intrinsic XOR gate, which is based on only four RFETs

and can be inverted to XNOR operation at run-time, offers significant advantages over conventional CMOS technology, such as reduced circuit complexity and transistor count. The presented circuit demonstrators are primitives that allow for the design of generic run-time reconfigurable circuits for improving hardware security in circuitry. In this respect, the proposed device architecture has high potential to complement conventional CMOS technology and can lead to novel circuit concepts with increased functional density.

ACKNOWLEDGMENT

The authors would like to thank the Center for Micro- and Nanostructures for providing the cleanroom facilities.

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