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A Run-Time Reconfigurable Ge Field-Effect Transistor With Symmetric On-States

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ABSTRACT Here, we present a Ge based reconfigurable transistor, capable of dynamic run-time switching between n- and p-type operation with enhanced performance compared to state-of-the- art Si devices. Thereto, we have monolithically integrated an ultra-thin epitaxial and defect-free Ge layer on a Si on insulator platform. To evade the commonly observed process variability of Ni-germanides, Al-Si-Ge multi-heterojunction contacts have been employed, providing process stability and the required equal injection capabilities for electrons and holes. Integration into a three top-gate transistor enables effective polarity control and efficient leakage current suppression to limit static power dissipation. Exploiting the advantages of multi-gate transistors, combinational wired-AND gates are shown to be capable of extending a single transistor to a logic gate. Notably, the obtained Al-Si-Ge multi-heterojunction reconfigurable transistors constitute the first CMOS compatible platform to combine efficient polarity control enabling the envisioned performance enhancements of Ge based reconfigurable transistors.

INDEX TERMS Germanium, reconfigurable field-effect transistor, symmetric on-state, wired-logic.

I. INTRODUCTION

Modern computing is built upon effectively increasing the transistor count by down-scaling of metal-oxide- semiconductor field-effect transistor (MOSFET) dimensions to achieve ever more compact integrated circuitry within fixed physical layouts and functionality [1]. To enable functional diversification and adaptive computing, advanced device concepts such as reconfigurable field-effect transistors (RFETs) are envisioned [2]. RFETs allow switching the corresponding charge carrier operation type for a single device at run-time by applying a dedicated program voltage and corresponding modulation of the band bending across the device channel and junctions. The RFET concept thus provides the potential to overcome the rigid circuit function definition by design and doping in conventional CMOS circuits, as the operation type is flexibly adjusted with the applied voltage. Thus, making RFETs an interesting candidate for future applications in the field of neuromorphic computing and hardware security [3], [4]. Accordingly, a CMOS circuit can be realized by RFETs so that a single "universal" transistor can be used as both a n-type and p-type FET without any further necessary n-/p-type scaling. Moreover, RFETs provide wired-AND capabilities beyond conventional CMOS technology, [5] permitting the suppression of parasitic charge sharing effects in dynamic logic gates [6]. Consequently, a tangible circuit example is the realization of a run-time reconfigurable NAND/NOR logic gate consisting of only three RFETs instead of four as necessary in static CMOS applications [7]. Further, highly compact XOR/XNOR gates can be realized with four RFETs, [8] enabling majority (MAJ) logic for highly efficient arithmetics. In the quest of achieving energy-efficient and faster switching RFETs, Ge with half the band gap and significantly lower effective masses of electrons and holes compared to Si has been

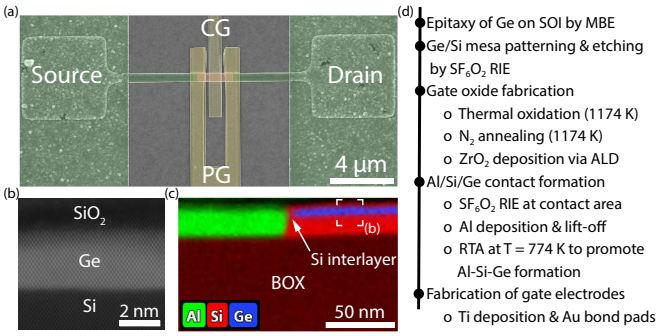

FIGURE 1. **(a) False-color SEM image of the Ge on SOI RFET device. (b) HRSTEM image showing an axial cut across the transistor channel. (c) EDX scan of the corresponding metal-semiconductor multi-heterostructure. (d) Process flow of the device fabrication.**

TABLE 1. **Comparison of key performance parameters of the proposed Ge on SOI RFETs with SOI RFETs and GeOI RFETs, both with 20nm device layer. Moreover, the related EOT for each platform is given. The green highlighting indicates the best performance for each parameter**

	SOI	GeOI	Ge on SOI
Oxide	SiO_2	Al_2O_3	SiO_2 | ZrO_2
Thickness (nm)	13	11	9 | 3.2
Rel. dielectric constant ϵ	3.9	9.31	3.9 | 27
EOT (nm)	13	4.6	9.46
J^n_{on} (kA/cm^2)	41.6± 16.1	0.2±0.15	93.6±22.8
J^p_{on} (kA/cm^2)	78.7± 22.9	53.3±35.4	162.0±13.1
J^p_{on} / J^n_{on}	1.9± 0.9	120.3±63.8	1.96±1.78
J^n_{on}/J^n_{off}	$\approx 10^7$	$\approx 10^1$	$\approx 10^7$
J^p_{on}/J^p_{off}	$\approx 10^7$	$\approx 10^3$	$\approx 10^7$
V^n_{th} (V)	1.8±0.22	1.34±0.24	0.32±0.26
V^p_{th} (V)	-2.8±0.3	-0.01±0.2	-1.24±0.35

identified as an improved channel material [9]. Despite the forecasted advantages, processing issues and the high fabrication costs of Ge on insulator (GeOI) platforms [10] have so far hindered harnessing these. In this regard, low-temperature molecular beam epitaxy (MBE) of thin, flat and defect-free Ge layers on a SOI platform proved to be a viable alternative leveraging the advantages of Ge, bypassing GeOI processing issues and providing a low-cost alternative to GeOI platforms [11].

II. DEVICE FABRICATION

In this work, we report on Ge based RFETs implemented on a SOI platform with high and symmetric on-state conductance for both, n- and p-type operation (see **Figure 1**a). Under conventional epitaxial growth conditions, only approx. 0.5 nm of Ge can be grown on Si(001) without significant elastic and plastic relaxation [12], i.e., too thin for the here proposed device applications. Thereto, ultra-low temperature MBE [13] was employed to grow a (100) surface oriented Ge layer with a thickness of $d_{Ge} = 4$ nm onto the device layer of a commercially available SOI wafer with a device layer of $d_{Si} = 20$ nm. Importantly, for the growth of strained and defect free Ge, growth temperatures slightly below 574 K are required. The Ge growth rates for typical chemical vapor deposition (CVD) processes used for CMOS fabrication tend to be low at that temperatures due to restricted precursor decomposition [14]. However, low growth rates in this case should enable epitaxial Ge growth due to the anyway limited adatom surface diffusion at low growth temperatures. Thus, the growth of the here presented structures, while performed with MBE, can be considered as CMOS compatible [13]. Moreover, a high-resolution transmission microscopy (HRSTEM) image of the channel stack is shown in Figure 1b. To exclude the formation of instable Ge oxide throughout device fabrication, a Si capping layer with a thickness of $d_{cap} = 3$ nm was gown and thermally oxidized to obtain a 5 nm to 9 nm thick SiO_2 interface dielectric layer. This further allows adding a high-κ gate-dielectric enabling a threshold voltage shift due to fixed charges [15] without substantial drive current degradation and Ge diffusion into the gate-dielectric [16]. In this regard, the gate-insulator stack is completed by a 3.2 nm thick ZrO_2 gate- oxide grown by atomic layer deposition (ALD). To ensure high reproducible, temperature stable and reliable Schottky barrier (SB) contacts, Al-Si-Ge multi-heterojunctions have been employed, providing a CMOS compatible platform for significantly enhanced Ge based RFETs [17]. Thereto, the nanoscale dimensionality of the grown Ge layers allows an epitaxial exchange reaction between Al and Si/Ge, delivering abrupt and flat junctions of high structural and electrical stability. This is in strong contrast to the known deficiencies of bulk Al/Si and Ge systems [18]. Figure 1c shows an electron diffraction X-ray spectroscopy (EDX) map of the respective metal-semiconductor junction, revealing an approximately 5 nm long Si segment in between the Ge layer and the Al contacts. This Si interlayer has already been observed for various SiGe compositions, see [17], [24], but, interestingly, as evident, it is also formed for the introduced Ge on SOI wafer substrate. It is expectable, that the Si atoms are fed from the surrounding buffer layer into the Al pads, eventually reaching a saturating point close to the interface forming the visible multi-heterojunction. The interface layer allows overcoming the common Fermi level pinning to the valence band of metal-Ge junctions and diminishes the predominant p-type conduction of Al-Ge junctions [19], [20]. Further, placing program gates (PGs) atop the Al-Si-Ge junctions allows to use these as a filter for the desired charge carrier type, while the control gate (CG) in between the PGs modulates the charge carrier concentration in the channel, thus turning the transistor on- or off. The process flow of the Ge on SOI RFETs is given in Figure 1d. The obtained structures exhibit a channel length between 1.5 μm and 1.8 μm and a width from approximately 500 nm up to 600 nm.

III. DEVICE CHARACTERISTICS

As shown in **Figure 2**, setting a positive (negative) program voltage V_{PG} enables electron (hole) injection and blocking of holes (electrons), allowing a run-time reconfiguration between n- and p-type mode. **Figure 3** shows the respective

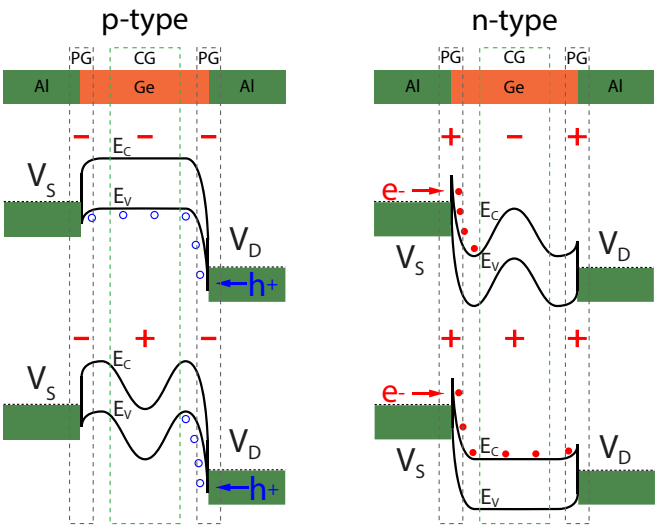

FIGURE 2. Schematic band diagrams for n- and p-type operation of the proposed Ge on SOI RFET device demonstrating the electrostatic mode-switching ability. Electrons / holes are depicted as full / open circles.

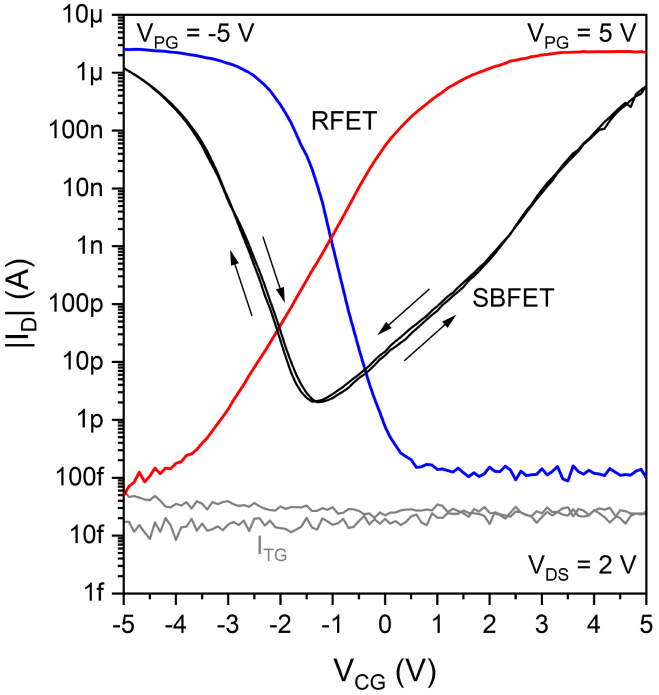

FIGURE 3. Transfer characteristics for both RFET operation types from the same device, shown in red (n-mode) and blue (p-mode), respectively. For comparison, the transfer curve of a single top-gate SBFET reference device including the related gate leakage-current (grey curve) is shown in black. The arrows indicate the sweep direction.

unipolar transfer characteristic for both operation modi The achieved I_{On}/I_{Off} ratios of the proposed Ge RFETs is on par with mature Si RFET technology, despite the smaller band gap, and is three to four orders of magnitude higher compared to state-of-the-art Ge REFT [9], [21]. To set the transistor metrics of proposed Ge on SOI RFET into perspective, **Table 1** provides relevant RFET properties of control structures based on a conventional SOI and a GeOI wafer. The geometric dimensions of the devices are comparable for all three wafer platforms. The related thicknesses are determined by SEM or TEM investigations and via ellipsometry and the relative dielectric constant via CV-measurements. Despite the use of a GeOI substrate with a thin Ge device layer and monolithic Al contacts of the same structural quality as the proposed Ge on SOI platform, [21] the thereof fabricated Ge RFETs are falling short in reaching both the promised performance as well as reaching the required on-current symmetry necessary for complementary circuits. In this regard, the proposed Ge on SOI technology provides a roughly twice as high on-currents normalized to the cross-section as the SOI control sample without Ge layer. Importantly, the proposed three-gate RFET architecture not only allows reconfiguration by charge carrier polarity control, but also enables low off-currents, due to efficient reverse junction leakage suppression. This is related to the potential barrier formed by the CG compensating the low band gap of Ge. Further, this is backed by control structures with a single source/drain overlapping gate-electrode. Such ambipolar SBFETs show significantly higher off-currents and shallower subthreshold swing due to a coupling to the SB [22] (Figure 3). Lastly, the comparison table, Table 1, impressively shows that the proposed Ge on SOI technology can maintain the low off-current, hysteresis and on-current symmetry of SOI RFETs and additionally enables considerably lower threshold voltages.

IV. ACTIVATION ENERGY

The activation energy over/through a barrier is an important parameter to investigate the injection capabilities of a junction, especially as different injection mechanisms are encountered in Schottky junction devices. In this respect, the here presented activation energy map reflects the barrier, which charge carriers (electrons for n-type and holes for p-type operation) face in dependency of the applied voltages. Therefore, mapping the temperature dependent I_D over a wide range of V_{DS} and V_{CG} (bias spectroscopy) and applying the thermionic emission theory, the gate- and bias-voltage dependent activation energy as a more general abstraction of the effective SB height comprising thermionic emission (TE) and field emission (FE) over the metal-semiconductor-metal multi-heterojunction can be extracted. The determined energy levels rely on an I/V(T) approach [23], where the resulting I_D for various symmetrically applied V_{DS} from –2 V to 2 V is captured at T from RT to 398 K in 25 K steps. A detailed description of the methodology can be found in [17], [24]. Note, that the applied thermionic theory exhibits validity limitations, especially concerning low bias voltages and the prevailing major FE/TFE current contribution of the Ge RFET. However, in the light of the experimental perspective of the fabricated structures, the used method offers a carefully estimation of the related band

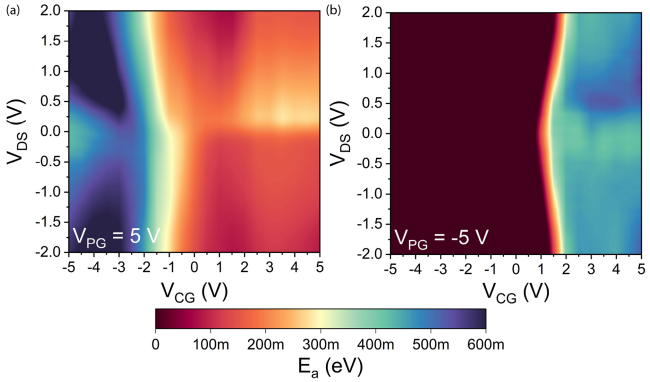

FIGURE 4. Activation energy maps retrieved from temperature dependent I/V characteristics for temperatures between 297 K and 398 K for n-type operation (a) and p-type operation (b).

bending situation. Further, from a physical point of view, the flat-band situation is more accurate to extract the SB height, however, the focus was set on actual bias/gate voltage levels for operating the device. Alternatively, Pacheco-Sanchez and Claus [25] introduced a quantitative model to determine the SB heights of SBFETs with higher precision. Moreover, there are also different experimental extraction models for the effective SB height [26]. The determined gate- and bias-voltage-dependent activation energies for both operation modi are presented in the energy maps in Figure 4, where the n-type operation (Figure 4a), is set with a PG voltage V_{PG} of 5 V and the p-type operation (Figure 4b), with the corresponding negative PG voltage V_{PG} of –5 V. The CG voltage V_{CG} is swept from –5 V to 5 V for both cases. As evident, there are distinct areas with a high activation energy in the range of 600 meV and above and areas with a low or even negative activation energy, indicating a highly-transparent contact despite the Si interlayer. Considering n-type operation, electrons face a blocking energy barrier for control gate-voltages V_{CG} from –5 V to –1 V, whereas for more positive voltages the charge carriers can more easily pass the multi-heterojunction, as the corresponding abstracted activation energy exhibits lower values resulting in efficient electron injection dominated by tunneling. The related band structure in respect to the applied voltage situation is schematically depicted in Figure 2. Moreover, there is no strong V_{CG}-dependent gradient of the activation energy for various bias voltages, revealing a very symmetric and stable device. The complementary situation for p-type operation, presented in Figure 4b, exhibits a similar behaviour but for negative voltages.

V. WIRED-LOGIC

Moreover, devices with multiple CGs have been investigated regarding their capabilities of transforming a single transistor into a reconfigurable logic gate. **Figure 5**a shows the corresponding SEM image of the proposed device with a symmetrically applied bias-voltage V_{DS} of 5 V. The operation mode is set with the V_{PG}. Considering the applied

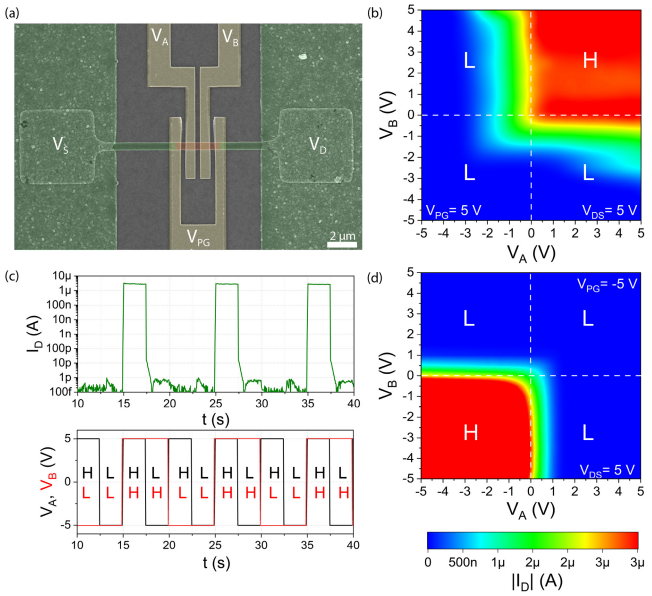

FIGURE 5. (a) False-color SEM image of the respective 2-input wired AND. Input spectroscopy for both, n-type operation (V_{PG} = 5 V) (b) and p-type operation (V_{PG} = −5 V) (d) at a bias-voltage of 5 V. (c) Transient analysis for input voltages, V_A and V_B, between −5V and 5V and the resulting drain current I_D.

CG voltages at the inputs A and B as voltage input, consequently 5 V as logical high (H) and –5 V as logical low (L), and the arising drain current as output, a logical high (H) i.e., a high current, is obtained for applying the logical high (H) level to both terminals A and B. Contrary, any other logical input combination at A and B results in a seven orders of magnitude lower drain current, which can be interpreted as logical low (L). The relating transient analysis, see Figure 5c, reveals the corresponding drain current in dependency of the applied input voltages V_A and V_B, with a polarity gate-voltage set to n-type operation, so to 5 V. Investigations of the resulting drain current in respect to variations of the input voltages for both operation modi, as it can be seen in Figure 5b and d, exhibits a very distinct high current area when applying positive input voltages for n-type operation and negative input voltages for p-type operation, respectively. Taking logical circuit systems into account, it is evident that the presented Ge RFET can withstand potentially unwanted occurring (input) voltage changes to guarantee functionality. Concerning the introduced logical interpretation of the input voltages and output drain current, the multi-CG structure depicts a so- called 2-input wired-AND [5] for the n-type operation (V_{PG} = 5 V) and the logical equivalent of the complementary logical function for the p-type operation (V_{PG} = –5 V), as indicated in Figure 5b and d.

VI. CONCLUSION

In conclusion, a RFET based on an ultra-thin MBE-grown Ge layer integrated on a standard SOI platform is presented. Monolithic and single-crystalline Al-Si-Ge multi-

heterojunctions have been formed to bypass the commonly observed process variability of Ni-germanide contacts, at the same time facilitating the advantages of Ge based devices such as boosting the drive currents while reducing the threshold and operation voltages. The ultra-thin Si interlayer contacting the Ge channel is providing process stability and equal injection capabilities for electrons and holes resulting in a highly symmetric on-state ratio. Importantly, the ultra-thin epitaxial Ge layer enhances the on-state currents compared to SOI- and GeOI-based RFETs. However, there are still remaining challenges to overcome in respect to achieve full CMOS compatibility, especially adaptation to modern W based on-chip interconnect technology [27]. Therefore, an additional protective layer, such as TiN or TaN [28], may need to be added to hinder the Al outdiffusion. Notably, the Ge on SOI REFT platform supports a multi-gate design to obtain single-transistor combinational wired-AND gates important for reconfigurable NAND/NOR logic gates as well as XOR/XNOR gates.

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L.W., D.N. and M.S. performed the device fabrication. A.F., M.S., L.K. and D.P. conducted the electrical measurements. D.N. developed and deposited the ZrO_2 gate dielectric. L.V., S.L., P.S. and X. M. carried out the HRSTEM measurements and analysis. J.A., E.P.N. and M.B. designed and grew the Ge on SOI. M.S and W.M.W. conceived the project and contributed essentially to the experimental design and data evaluation. The authors further thank the Center for Micro- and Nanostructures (ZMNS) of TU Wien for providing the cleanroom facilities.

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