TECHNISCHE UNIVERSITÄT WIEN

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The large-scale production of silicon sensors for the Phase-2 upgrade of the CMS Outer Tracker

ausgeführt zum Zwecke der Erlangung des akademischen Grades eines Doktors der technischen Wissenschaften unter der Leitung von

PRIV.-DOZ. DIPL.-ING. DR. CHRISTOPH SCHWANDA,
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am Institut für Hochenergiephysik
der Österreichische Akademie der Wissenschaften
und Atominstitut der Technischen Universität Wien

eingereicht an der Technischen Universität Wien,
Fakultät für Physik

von

DIPL-ING. KONSTANTINOS DAMANAKIS

Matrikel Nummer.: [redacted]

Unterschrift Betreuer

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Kurzfassung

Die Hochluminositätsaufrüstung des Large Hadron Collider (LHC) am CERN wird eine neue Phase der Herausforderungen für die Hochenergiephysik-Community einleiten. Die Erhöhung der Instantanluminosität der Maschine auf das 5×10^{34} cm^{-2}s^{-1} (oder 7×10^{34} cm^{-2}s^{-1} im besten Fall) wird mit mehr Statistiken zu den Zerfällen des Higgs-Bosons versorgen und das Entdeckungspotenzial insbesondere für seltene Prozesse des Standardmodells oder der Physik über das Standardmodell hinaus erweitern. Der HL-LHC soll bis zum Ende seiner Lebensdauer eine integrierte Luminosität von 3000 - 4000 fb^{-1} liefern. Der Detektor CMS (Compact Muon Solenoid) muss mehrere Upgrades durchlaufen, um die Erhöhung der Luminosität durch den HL-LHC vollständig nutzen zu können. Dieses Upgrade-Programm ist als das CMS *Phase-2* upgrade bekannt. Der innerste Subdetektor des CMS, das Spurensystem (CMS Tracker), wird durch einen fortschrittlicheren Detektor vollständig ersetzt, der mit den höheren Teilchenraten und den hohen Strahlungspegeln des HL-LHC umgehen kann.

Der Phase-2 Tracker besteht aus einem Inner Tracker (IT) basierend auf Pixelsensoren und einem Outer Tracker (OT) basierend auf Streifen und Makro Pixelsensoren. Der Outer Tracker benötigt etwa 26400 neue Siliziumsensoren. Die Produktion der Outer Tracker Sensoren hat im Sommer 2020 begonnen.

Diese Doktorabeit beschreibt die grundlegenden Eigenschaften der neuen Siliziumsensoren für den Outer Tracker und fasst den CMS Plan zur Überwachung der Stabilität und Qualität der groß angelegten Produktion zusammen. Dieser Plan umfasst die elektrische Charakterisierung der Produktionssensoren und der Teststrukturen auf stichprobenweiser Basis. Die Teststrukturen werden auf denselben Wafern wie die Hauptensoren entwickelt, und sie teilen dieselben Eigenschaften. Sie bieten einen schnellen Zugang zu mehreren Sensormerkmalen, von denen viele nicht direkt am Hauptsensor gemessen werden können, wie beispielsweise die Flachbandspannung (flat-band voltage), oder die möglicherweise destruktive Tests erfordern, wie die Durchbruchspannung des Kopplungsoxids (coupling oxide).

Bis heute hat die Massenproduktion der Siliziumsensoren des Phase-2 Outer Trackers mehr als 70% des Gesamtziels erreicht. Daher wurden ausreichend Daten gesammelt, um den Produktionsprozess zu charakterisieren. Diese Arbeit bietet eine Zusammenfassung der Entwicklung aller gemessenen Sensor und Waferparameter über die Produktionszeit. Ein Vergleich und eine Korrelation aller Parameter im Zusammenhang mit denselben Sensoreigenschaften werden durchgeführt. Ein Schwerpunkt liegt auf jenen Parametern, die Trends und Inkonsistenzen über die Produktionszeit aufzeigen. Neben Schlussfolgerungen zur Qualität der Produktionssensoren versucht diese Arbeit, die Bedeutung der Prozessqualitätskontrolle (Process Quality Control) als Werkzeug zur rechtzeitigen Erkennung von Fertigungsprozessvariationen zu festigen und einen umfassenden Einblick in die Wafer-Eigenschaften zu geben.

Darüber hinaus werden Studien zur Robustheit der Produktionssensoren des Outer Trackers gegenüber externen Faktoren wie elektrostatischer Aufladung und Feuchtigkeit durchgeführt. Die elektrostatische Aufladung ist ein Effekt, der einen großen Teil der Outer Tracker Sensorproduktion betrifft. Die Quelle dieses Effekts, ihre Auswirkungen auf das elektrische Verhalten der Produktionssensoren sowie eine vom CMS definierte Minderungsstrategie werden in dieser Arbeit präsentiert. Auch die Auswirkungen hoher relativer Feuchtigkeit auf die Produktionssensoren werden untersucht. Die Rolle hoher relativer Feuchtigkeit wird während des Modulmontages-

tadiums aufgrund der langen Exposition der Sensoren gegenüber der feuchten Umgebung der ESD-sicheren Reinräume immer wichtiger. Die Reaktion der Sensoren nach langer Exposition gegenüber Feuchtigkeit wird untersucht, und eine Erholungsstrategie wird für diejenigen Sensoren definiert, die aufgrund von Feuchtigkeit eine Verschlechterung ihres elektrischen Verhaltens zeigen.

Abstract

The high-luminosity upgrade of the Large Hadron Collider (LHC) at CERN will introduce a new period of challenges for the high-energy physics community. The increase of the peak instantaneous luminosity of the machine up to 5×10^{34} cm^{-2}s^{-1} (or 7×10^{34} cm^{-2}s^{-1} in the ultimate case) will provide with more statistics of the Higgs boson decays and expand the discovery potential especially for rare processes of the standard model or beyond standard model physics. The HL-LHC is expected to deliver an integrated luminosity of 3000 - 4000 fb^{-1} by the end of its lifetime.

The CMS (Compact Muon Solenoid) detector needs to undergo several upgrades in order to fully exploit the increase in luminosity delivered by HL-LHC. This upgrade program is known as the CMS *Phase-2* upgrade. The innermost sub-detector of CMS, the tracking system (CMS Tracker), will be fully replaced with a more advanced detector which is designed to cope with the larger particle rates and the high radiation levels of HL-LHC.

The Phase-2 Tracker consists of an Inner Tracker (IT) based on pixel sensors and an Outer Tracker (OT) based on strip and macro pixel sensors. The Outer Tracker requires about 26400 new silicon sensors. The production of the Outer Tracker sensors has started since the summer of 2020.

This thesis describes the basic features of the new Outer Tracker silicon sensors and summarizes the CMS plan to monitor the stability and quality of large-scale production. This plan comprises the electrical characterization of the production sensors and the test structures on a sampled basis. The test structures are developed on the same wafers as the main sensors and they share the same properties. They provide quick access to several sensor parameters, many of which can not be directly measured on the main sensor, such as the flat-band voltage or they require potentially destructive tests, such as the breakdown voltage of coupling oxide.

To date, the mass production of the Phase-2 Outer Tracker silicon sensors has exceeded 70% of the total. Hence, a sufficient number of data has been collected in order to characterize the production process. This thesis provides a summary of the evolution of all the measured sensor and wafer parameters over production time. A comparison and a correlation of all the parameters related to the same sensor properties is performed. An emphasis is given on those parameters which reveal trends and inconsistencies over production time. Apart from providing conclusions for the quality of the production sensors, this thesis attempts to prove the importance of process quality control as a tool to spot in-time fabrication process variations and to give a full insight into the wafer properties.

Moreover, studies are conducted on the robustness of the Outer Tracker production sensors against external factors such as electrostatic charge-up and humidity. The electrostatic charge-up is an effect which concerns a large fraction of the Outer Tracker sensor production. The source of this effect, its impact on the electrical behavior of the production sensors as well as a mitigation strategy as defined by CMS, are presented in this thesis. Also, the impact of high relative humidity on the production sensors is investigated. The role of high relative humidity becomes more crucial during the module assembly stage due to the long exposure of the sensors to the humid environment of the ESD-safe clean rooms. The response of the sensors after a long exposure to humidity is examined and a recovery strategy is defined for those sensors which show a deterioration of their electrical behaviors due to humidity.

Acknowledgments

I would like to express my deepest gratitude to my supervisors, Prof. Christoph Schwanda and Dr. Marko Dragicevic. I would like to thank Christoph for being supportive and always willing to advise me on the progress of my research work and my doctoral studies. I am very grateful to Marko for supervising my daily work at HEPHY, teaching me a lot about the CMS detector and the principles of sensor design as well as for giving me his feedback and fruitful comments on the content of this thesis. I would also like to thank Dr. Thomas Bergauer for sharing his constructive comments and ideas during the group meetings at HEPHY which were very helpful for my daily work.

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Last but not least, this endeavor would not have been possible without the support of my parents, my sister and my best friends who were always very encouraging, especially during the first challenging year of my doctoral studies.

Contents

Chapter 1

High energy physics at CERN

The European Organisation for Nuclear Research (CERN) is one of the largest scientific institutes in the world located at the French-Swiss borders. It is a European laboratory which aims to study the most fundamental constituents of matter and to extend the limits of human knowledge on the creation of our universe. The physics program of CERN includes detailed studies of the four fundamental interactions, direct searches for new physics, as well as the discovery of new particles and precision measurements of their properties. The investigation of new physics phenomena requires looking for them at high energy scales. Today, this possibility is given by the circular accelerators (synchrotrons) which can accelerate particle beams up to several GeV and under the action of focusing magnets, bring them into collision. High-rate interactions at high energy scales are produced from these collisions.

CERN has already announced a number of discoveries, such as the discovery of weak neutral currents in 1973 [1], [2] and the measurement of W and Z boson masses in mid of 1980 [3], [4]. A milestone was the discovery of the Higgs boson in July 2012 [5], [6]. The Higgs boson is a result of the quantum excitation of the Higgs field which gives mass to particles when interacting with them. The Higgs mechanism had already been formulated 50 years prior to this discovery. Figure 1.1 illustrates a candidate for the decay H $\rightarrow$ ZZ (ee$\mu\mu$), where the green lines coming from the interaction point are associated with two electrons and the two red lines describe two muons.

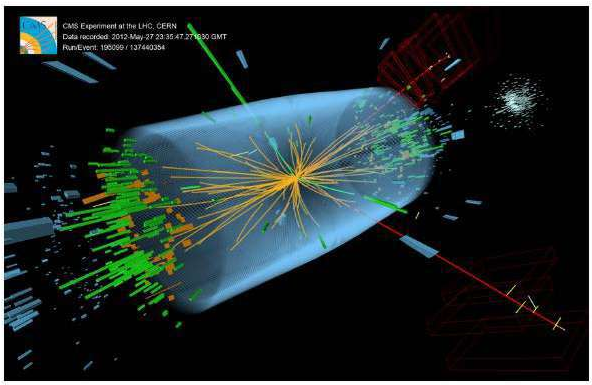

Fig. 1.1: Candidate for the decay $H \rightarrow ZZ \rightarrow ee\mu\mu$, with the green lines towards the center of the picture describing two electrons and the red lines describing two muons.

The Large Hadron Collider project at CERN is still in progress and while this thesis is written in 2023, a new run of data collection (Run-3) is taking place. The high-energy physics community aims to collect more data on the Higgs boson couplings, to study in more detail its properties, as well as to search for dark matter candidates.

1.1 The Large Hadron Collider

The Large Hadron Collider (LHC) is a storage ring in which proton beams collide at a center mass energy of $\sqrt{s} = 14$ TeV [7]. The circumference of LHC is approximately 27 km and it is located about 100 meter below the ground. Two beams consisting of 2808 bunches of a few $\times$ 10^{11} protons per bunch, circulate until they are brought into collision. The beams are restricted in a circular trajectory by 1232 superconducting dipole magnets, which produce a magnetic field of 8.33 T. To generate such a strong magnetic field, the properties of superconducting materials are exploited; below a certain critical temperature, the resistance of the superconductor vanishes and a large current can flow freely. The LHC ring operates at 1.9 K. The beams are focused by the action of 474 focusing quadrupole magnets.

The LHC together with the pre-accelerators installed at CERN is shown in Fig. 1.2. The formation of the final 7 TeV proton beams must undergo several sequential stages. In the first stage, an ion source is fed with hydrogen gas and H^- ions are produced which leave the source with an energy of 45 keV. The ions are then injected into a linear accelerator, the LINAC4, which accelerates them to an energy of 160 MeV. After this stage, the two electrons are stripped off the H^- by passing through a thin Carboin foil and the bare protons are inserted into the BOOSTER, where they are subjected to an energy boost up to 2 GeV. The protons are accelerated further at the PS (Proton Synchrotron) and the SPS (Super Proton Synchrotron), where energy up to 26 GeV and 450 GeV is reached respectively. Finally, the proton beams are injected into the LHC, where the proton bunches are accumulated and accelerated up to the nominal energy of 7 TeV. At peak energy, the beams can circulate around the LHC for about 10 hours during which they are brought into collisions several times. The luminosity of each beam reduces with increasing number of beam crossings. When the beams are not useful anymore for collisions, they are directed to the beam dump system and new beams are inserted into the LHC.

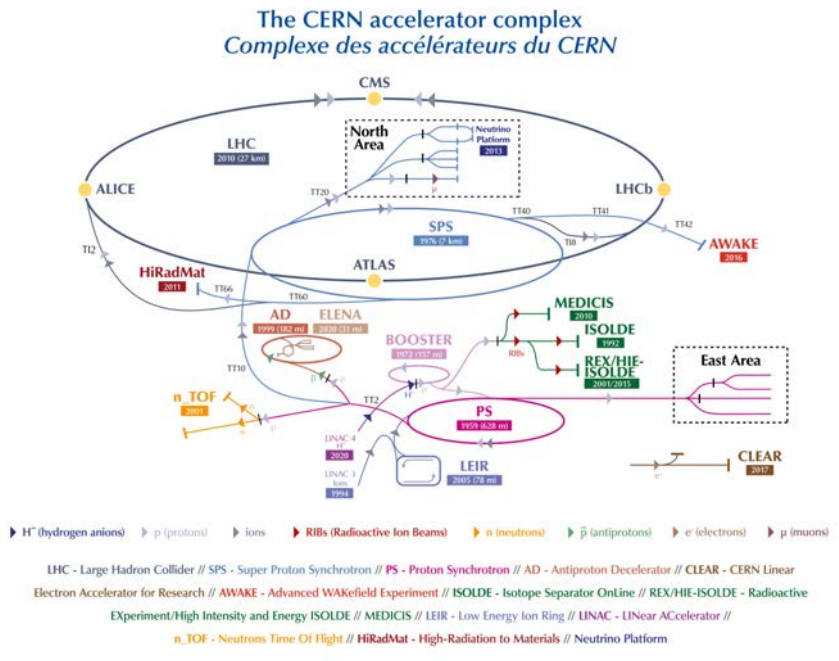

Fig. 1.2: Illustration of the Large Hadron Collider complex with its pre-accelerators and the numerous smaller experiments hosted at CERN.

Each collision of two bunches is called a bunch crossing (BX) and the collisions take place at 4 interaction points every 25 ns or at 40 MHz. In each single BX, about 50 interactions (pile-up) happen at an instantaneous luminosity of 2×10^{34} cm^{-2}s^{-1}, where most of them are "soft" collisions which produce lower energy-scale events. In other words, only a small fraction of these interactions per bunch crossing leads to "hard" collisions which produce high-energy particles.

Besides the proton-proton collisions, one month per each Run-year, heavy ion bunches of Pb-Pb (lead-lead) or p-Pb collide in order to study in more detail the QCD processes.

Each of the four interaction points of LHC hosts a detector which is responsible for recording and measuring the properties of the emerging particles. These four large experiments are ATLAS [8], CMS [9], ALICE [10] and LHCb [11]. ATLAS and CMS are general-purpose detectors aiming to discover new particles and physics. ALICE focuses on heavy-ion collisions and studies of the quark-gluon plasma (QGP). LHCb focuses on heavy-flavor physics, studies of the 2nd and 3rd generation quarks and in particular the beauty quark.

1.1.1 Luminosity

To evaluate the capabilities of an accelerator, two quantities are necessary: the energy and the luminosity of the beam. Collisions of high-energy beams are required in order to produce high-energy processes. The number of interactions per bunch crossing should be maximized to increase the statistics of occurring processes and the probability that low cross-section events can happen. The accelerator parameter which indicates the number of interactions is known as *luminosity*. For a given process, the rate of events is [12]

$$\frac{dN}{dT} = \mathcal{L} \cdot \sigma_p \tag{1.1}$$

where $\mathcal{L}$ is the instantaneous luminosity and σ_p is the cross-section of the process. The unit of instantaneous luminosity is $1/(\mathrm{cm}^2\,\mathrm{s})$.

For two colliding bunches with a Gaussian distributed density in space, the instantaneous luminosity $\mathcal{L}$ is given by:

$$\mathcal{L} = \frac{N_1 N_2 f_{\mathrm{rev}} N_b}{4\pi\sigma_x\sigma_y} \tag{1.2}$$

where $N_{1,2}$ describes the number of particles per bunch, f_{rev} is the revolution frequency, N_b the number of bunches and σ_x, σ_y the cross section of the beam in x, y directions perpendicular to the axis of interaction z.

The integration of the instantaneous luminosity over a period of time T gives the integrated luminosity L_{int}

$$L_{\mathrm{int}} = \int_0^T \mathcal{L}(T')\,dT' \tag{1.3}$$

The integrated luminosity is expressed in units of fb^{-1} (1b $= 10^{-28}$ m^2) and is a quantity which relates directly the number of occurring events over certain amount of time T

$$L_{int} \cdot \sigma_p = \text{number of events of interest} \tag{1.4}$$

For instance, in 2022 which was the first year of LHC Run-3, the machine achieved a peak luminosity up to 2×10^{34} cm^{-2}s^{-1} while CMS and ATLAS recorded for this year a total integrated luminosity of 40 fb^{-1} [13].

1.1.2 The event rates at LHC

As it is stated by the formula 1.1, the event rate of a given process is defined by the luminosity of the collider and the cross-section of the process. Figure 1.3 illustrates the cross sections of different proton-proton or proton-antiproton processes as a function of the center-of-mass energy $\sqrt{s}$ of the colliding beams. The cross-section of proton-proton inelastic collisions at center-of-mass energy $\sqrt{s} = 14$ TeV is about 80 mb $= 8 \times 10^{-26}$ cm^{-2}. Assuming an instantaneous luminosity of $\mathcal{L} = 10^{34}$ cm^{-2}s^{-1}, the number of events per second is in the order of 10^9/s. The amount of data collected for each event is around 1 MB. Therefore, about 1 PB/s of data is generated in the LHC.

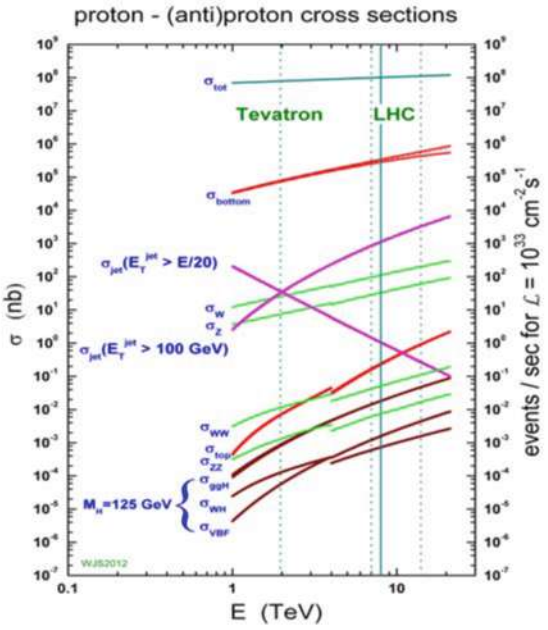

Fig. 1.3: Cross sections of selected proton-(anti)proton processes as a function of centre-of-mass energy. The vertical dashed lines indicate center-of-mass energies reached by the Tevatron and the LHC [14].

This very large amount of data can not be stored due to limitations in data storage capacity. Therefore, a selection of interesting events, such as decays of rare particles, is done by the experiments. More information on that is provided in the next section.

1.1.3 The pileup at LHC

The mean number of interactions per bunch crossing μ, for a given instantaneous luminosity $\mathcal{L}$ is defined as:

$$\mu = \frac{\sigma_{\text{inel}} \mathcal{L}}{n_{\text{b}} f_{\text{rev}}} \tag{1.5}$$

where σ_{inel} is the inelastic cross section, n_{b} the number of bunches and f_{rev} the revolution frequency. The parameter μ is known as *pile-up*.

Assuming the design instantaneous luminosity of $\mathcal{L} = 10^{34}$ cm^{-2}s^{-1} of LHC, with $n_{\text{b}} = 2808$ and $f_{\text{r}} = 11.245$ kHz, the pile-up is $\mu \simeq 25$. Figure 1.4 illustrates the distribution of pile-up for the Run-2 as recorded by CMS.

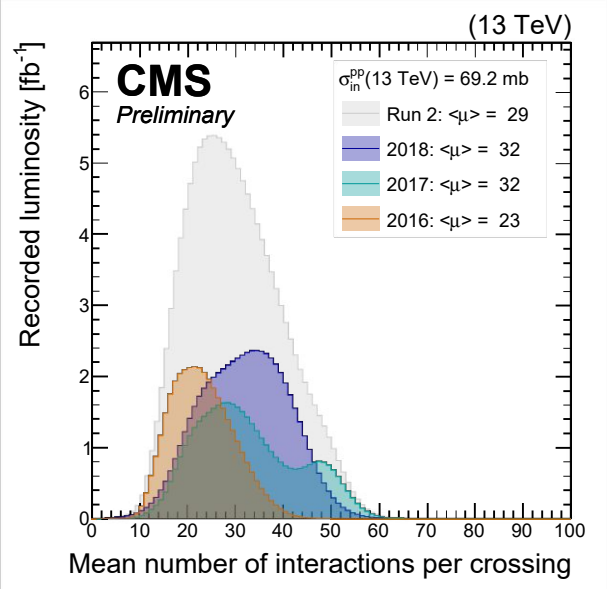

Fig. 1.4: Distribution of mean number of interaction per crossing for proton-proton collisions in 2016 (orange), in 2017 (green), in 2018 (blue) and integrated over the years 2016 - 2018 (grey). The data comes from the CMS experiment. An inelastic cross-section of 69.2 mb was chosen [15].

The target of the experiments is to reconstruct the primary and secondary vertices which occur from the proton-proton collisions. Among them, only a fraction corresponds to events which are under study by the experiments while the rest are related to well-understood processes. The additional collisions result in overlapping hits in the detectors and make more challenging the reconstruction of the events of interest. The experiments such as CMS and ATLAS have developed mitigation techniques in order to minimize the impact of pile-up in the reconstruction of the processes of interest. An example that presents the pile-up mitigation strategy of CMS for Run-2 is given in [15].

1.2 The Compact Muon Solenoid (CMS)

The Compact Muon Solenoid [9] is similar to ATLAS a multi-purpose detector located at one of the four interaction points of the LHC. CMS and ATLAS have a common target to discover new physics but their design and the technologies which instrument them vary in a significant way. The different geometry of the two detectors is mostly attributed to a different choice of magnetic system. More information regarding the comparison between the two detectors is given in [16].

CMS is a compact, hermetic detector with a very strong magnetic field of 3.8 T, generated by its superconducting magnet coils. It is located 100 m below the earth's surface and it weighs around 12500 t. The detector consists of many layers of different sub-systems, arranged in a barrel shape with end-caps at both ends. The closest to the collision point sub-detector is the tracking system which is surrounded by the superconducting solenoid, an electromagnetic calorimeter (ECAL) and a hadronic calorimeter (HCAL). The outer part of CMS comprises an iron magnet "return yoke" which confines the magnetic field and is interleaved by muon chambers. Forward sampling calorimeters extend the pseudo-rapidity coverage of CMS to large $|\eta|$. The data from

all the sub-systems is collected, analyzed and combined, resulting in detailed information of the physical properties (mass, energy, momentum) of the particles that emerge from the interaction point. An illustration of the CMS detector is given in Fig. 1.5.

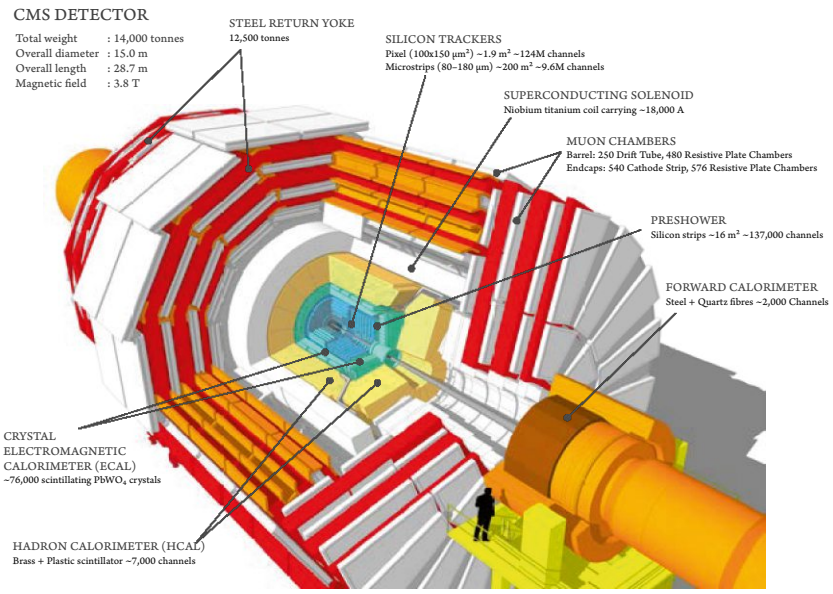

Fig. 1.5: Display of the Run-2 CMS detector. From inner to outer region: the silicon tracking system (blue), the ECAL (light blue) and the HCAL (yellow) are surrounded by the superconducting solenoid (white barrel) and the iron yoke with the muon chambers (red and white) [17].

The main requirements of the CMS detector are summarized below [9]:

- Good muon identification and momentum resolution, ability to determine without ambiguities the charge of muons with E $<$ 1 TeV.
- Good charged particle momentum resolution and reconstruction efficiency in the tracker.
- Good electromagnetic energy resolution, good diphoton and dielectron mass resolution, wide geometric coverage, π^0 rejection, and efficient photon and lepton isolation.
- Good missing transverse-energy and dijet-mass resolution, requiring hadron calorimeters with a large hermetic geometric coverage and with fine lateral segmentation.

The design of CMS is driven by its strong magnetic field which is necessary for high-precision momentum measurements of charged particles and in particular, muons. The magnetic field bends the track of the charged particles which are produced by the collisions at the interaction point. The momentum and the sign of the particle can be deduced by measuring the sagitta of the curvature of its track. This information is given by the silicon tracking system. The energy measurement is performed by the calorimeters. In particular, the ECAL measures the energy of particles which interact via the electromagnetic force with its medium, such as electrons and photons. The electromagnetic interaction of the incoming particles with the material of ECAL produces showers inside the detector until the energy of the incident particle is fully deposited. Similarly, the HCAL measures the energy of hadrons, such as protons, neutrons and pions which interact via the strong force with the material of the calorimeter. The muons can penetrate large amounts of material and lose small fraction of their energy, thus they are not stopped by the

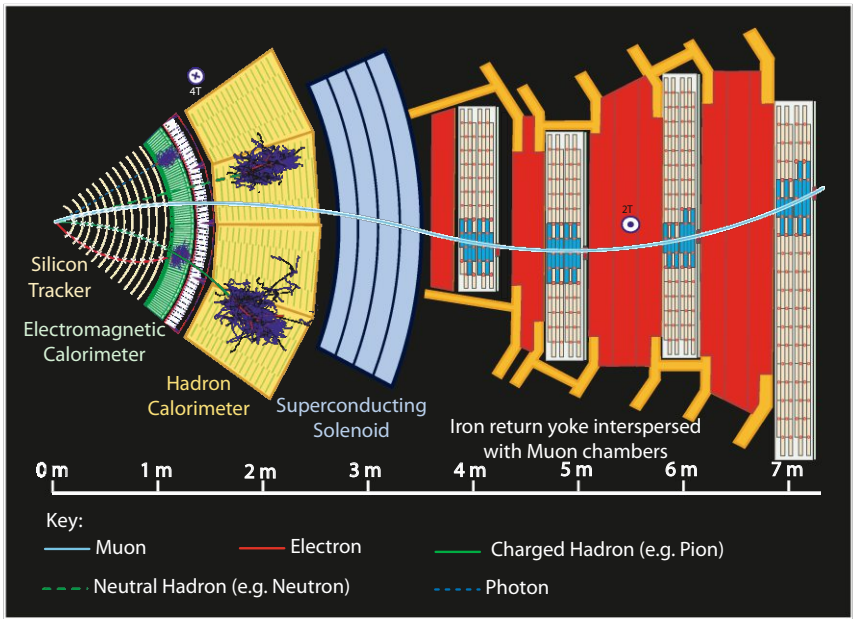

Fig. 1.6: A slice of CMS detector with examples of particle trajectories. A tracking system provides information about charged particles momentum. The energy is measured by the electromagnetic and hadronic calorimeter. Muons are identified by the muon chambers [18].

calorimeter. Muon chambers which are embedded into the iron yoke are used for the detection of muons. The muon chambers is the most massive subsystem of CMS optimized in a way to increase interactions with muon. Since muons (as well as neutrinos which barely interact with the detectors) are the only particles that escape the calorimeters, signals measured by the muon chambers are indicators of the passage of a muon. An example showing how different types of particles are detected by the different sub-systems of CMS is given in Fig. 1.6.

Tracker

The CMS tracking system is instrumented with radiation-hard silicon sensors which cover an area of $\simeq 206$ m^2. The tracker is designed to operate with a maximum occupancy of $1-3\%$ at all layers, with a position resolution up to 10 µm and excellent impact parameter resolution in Rϕ and Rz. It covers a pseudorapidity range up to $|\eta| < 2.5$.

The innermost layer of the tracking system must cope with the highest particle rates because it is installed near the interaction point, at a radius of $r = 4$ cm. Each LHC bunch crossing at design luminosity, with a pile-up of about 20 proton-proton collisions, creates an average of 1000 particles which hit the tracker layers. This leads to a hit rate density of 1 MHz/mm^2 at a radii of 4 cm, falling to 60 kHz/mm^2 at a radii of 22 cm and 3 kHz/mm^2 at a radii of 115 cm [9]. The challenge to preserve high efficiency in such an environment is the main motivation for the design and the selected technology of the system.

The Tracker is subdivided into an Inner Tracker (IT) and an Outer Tracker (OT). The Inner Tracker comprises silicon pixel sensors with 4 barrel layers while the Outer Tracker consists of silicon strip sensors with 10 barrel layers. Each side of the barrel is completed by an end-cap which consists of three pixel disks in the pixel detector and three small plus nine large disks in the outer tracker on each side (Fig. 1.7).

Pixels are an ideal choice for the innermost layers which are exposed to the highest rate of particles. The pixel detector of the inner tracker contains approximately 66 million pixels, offering high granularity, fast response and radiation tolerance. The pixel detector is essential for b and τ tagging, primary vertex reconstruction. It also determines the track seed towards the outer strip tracker [19].

The strip detector is instrumented with about 10 million strips. Among the sensors, different sizes, thicknesses and shapes are realized. Strips with smaller lengths and pitch are installed in the inner layers of the strip detector, where the occupancy is higher, while sensors with longer strips populate the rest of the area. The position resolution offered by the outer tracker varies between 23 µm to 53 µm according to the layer and the features of the installed sensors.

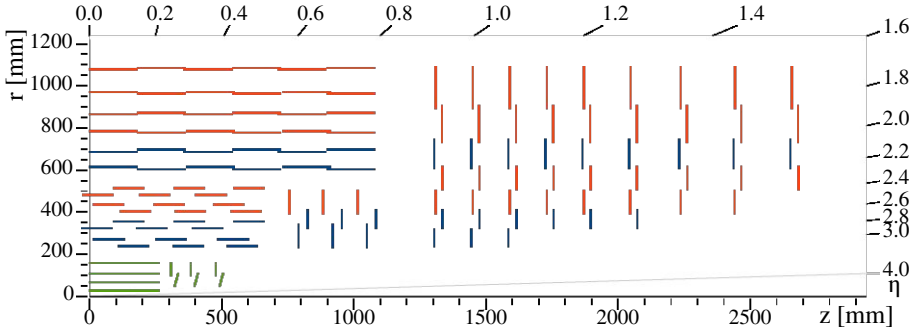

Fig. 1.7: Illustration of a quarter of the current CMS Tracker ir r-z. The Inner Tracker layers are shown in green while the Outer Tracker is shown with blue and red segments. The red lines correspond to the single-sided strip modules while the blue lines correspond to the double-sided strip modules [20].

Electromagnetic calorimeter (ECAL)

The electromagnetic calorimeter surrounds the tracker and covers a pseudo-rapidity range of about $|\eta| < 3.0$. It consists of a central barrel and two end-caps. It is a homogeneous calorimeter which offers excellent energy resolution, granularity and radiation hardness. Key to that is the use of high-density crystals. The design of ECAL is optimized for the detection of the Higgs channel decay $H \to \gamma\gamma$. Besides the γ, electron identification and reconstruction, ECAL contributes also to the reconstruction of tau leptons, jets and missing transverse momentum measurements.

ECAL uses 68524 lead tungstate crystals ($PbWO_4$). They feature high density (8.28 g/cm^3), short radiation length (0.89 cm) and small Molière radius (2.2 cm) which results in a fine granularity. The scintillating $PbWO_4$ crystals are read out by avalanche photodiodes (APD) at the barrel and vacuum phototriodes (VPT) at the endcaps. The scintillators produce light proportional to the deposited energy of the incoming particle and the photodiodes amplify and measure the emerging light. The scintillation decay time of the used crystals is comparable to the LHC bunch crossing time: about 80% of the light is emitted in 25 ns.

An additional pre-shower detector is installed in front of the endcaps of ECAL. That is 2 layers of silicon-strip sensors with a pitch of 1.9 mm. The aim of the preshower system is to identify neutral pions in the endcaps within a fiducial region $1.65 < |\eta| < 2.6$, while it also contributes to the identification of electrons against other minimum ionizing particles.

Hadronic calorimeter (HCAL)

The hadronic calorimeter of CMS is designed to measure hadron jets, neutrinos and exotic particles which are identified through the missing transverse energy. Therefore, the hermeticity and the ability to measure E^{T}_{miss} is driving its design. The HCAL is located between the ECAL and the superconducting magnet. It features a barrel and endcap geometry. Its barrel is radially restricted between 1.77 m $<$ R $<$ 2.96 m where the outer part of ECAL and the inner part of magnet coils are installed. Apparently, this sets a constraint on the total amount of material which can be used.

HCAL is a sampling calorimeter with alternating layers of absorbers and plastic scintillators. The absorbers are 5 cm thick brass, while the plastic scintillators are 4 mm thick. HCAL scintillators contain 70000 tiles which are read out by multi-channel hybrid photodiodes. The tiles are connected to the photodiodes through wavelength-shifting fibers.

Outside of the magnet coils is installed an additional layer of 10 mm thick scintillators which serves as the last absorption layer and completes the barrel region. The detector is extended beyond $|\eta| = 3$ and up to $|\eta| = 5.2$ by the Hadron Forward Calorimeter (HF). The HF is installed at a distance of 11.2 m from the interaction point. The HF has to cope with large particle fluences and it was foreseen to receive a total dose of about 10 MGy after 10 years of LHC operation [21]. The active material is quartz fibres which is more radiation hard while the absorber material is steel. The quartz fibers generate Cherenkov light when charged shower particles above the Cherenkov threshold enter its medium. The produced light is read out by Photomultiplier Tubes (PMT) [22]. An illustration of the layout of the CMS calorimeters is shown in Fig. 1.8.

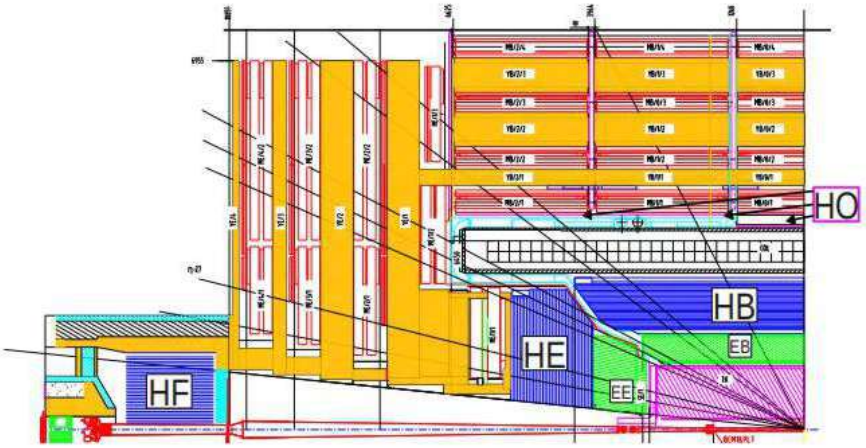

Fig. 1.8: A schematic drawing of a quarter of the CMS detector showing the location of the ECAL and HCAL. EB and EE correspond to the ECAL barrel and endcap respectively. HB and HE are the abbreviations for the HCAL barrel and endcap, while HO is the outer calorimeter and HF is the forward HCAL [23].

Muon Chambers

The CMS muon system is designed for identifying muons, triggering upon the arrival of a muon and reconstructing their momentum. Good muon momentum resolution is a key parameter which is provided by the very good spatial resolution of the detectors. The muons are the only charged particles which can penetrate the calorimeters without being absorbed. The installation of the muon chambers behind the calorimeters ensures that the signals generated in their detectors

come from muons, although hits from the neutron-induced background play also a significant role in the endcap regions [24].

Three types of gas detectors are used for muon identification in the CMS detector. The barrel region is instrumented with drift tube chambers which match the cylindrical geometry of the solenoid, and the 2 endcap regions with cathode strip chambers. Resistive plate chambers are interleaved in between the barrel and the endcap.

The drift chambers (DT) populate the barrel region of the muon system and are a good choice for this region due to the low muon rate and the small neutron-induced background and magnetic field. The barrel drift tube chambers provide coverage of $|\eta| < 1.2$. In the endcap region, the muon flux and the background are large, while the magnetic field is stronger and non-uniform. A good selection for this area is the cathode strip chambers (CSC) because they have a fast response time, they are finely segmented and can tolerate the non-uniformity of the magnetic field. The CSC together with the DT covers a range of $|\eta| < 2.4$. The Resistive plate chambers (RPC) are installed both in the barrel and the endcaps and are dedicated detectors for triggering. Their excellent time resolution is exploited for this purpose. A quarter of the CMS muon system is shown in Fig. 1.9.

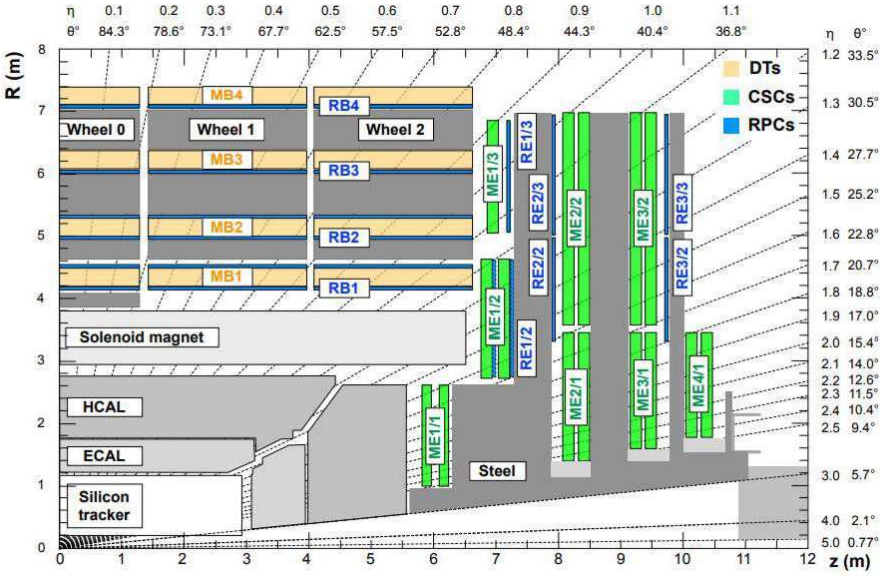

Fig. 1.9: A r-z cross-section of CMS detector with emphasis on the muon system. The 4 drift tube stations (light orange) are labeled as MB (muon barrel) and the cathode strip chambers (green) are labeled as ME (muon endcap). Resistive plate chambers (blue) are installed in the barrel and the endcaps of CMS and are labeled as RB and as RE, respectively [25].

Trigger

At LHC, bunches of protons collide every 25 ns (40 MHz) while at the nominal luminosity of 10^{34} cm^{-2}s^{-1}, about 20 actual collisions happen. At nominal luminosity, the interaction rate exceeds 1 GHz. It is not possible to store and process all of the generated data without discrimination and selection of the events which correspond to interesting physics processes. This is the target of the CMS trigger system. The rate is reduced in two steps; the first selection is made by the Level-1 (L1) Trigger and a second, final selection by the High-Level Trigger (HLT). A detailed description of the CMS trigger system is given in [26].

The Level-1 Trigger consists of custom-made, programmable electronics and has a latency of 3.2 µs, which means that all data needs to be stored in the front-end electronics of each sub-detector for that time until a decision from the trigger logic is sent out. The L1 receives and combines information from the calorimeter and the muon system and searches for events with high transverse energy or momentum or high missing energy. The L1 output data rate is 100 kHz.

The High-Level Trigger is software running in a large farm of thousands of commercial computers, including over 13000 CPU cores. HLT receives the data which is forwarded from the front-end electronics after an L1 accept and performs fast physics selections in order to achieve a further reduction to 100 Hz.

1.3 The High-Luminosity LHC (HL-LHC)

By the end of Run-3, LHC is expected to have delivered a total integrated luminosity of 500 fb^{-1} to the experiments. In order to extend the discovery potential, to observe new rare events with small cross-sections and to perform more precise measurements on known physics processes, the number of collected statistics must be increased. To accomplish this goal, the LHC machine should offer a higher collision rate and therefore deliver higher integrated luminosity to the experiments. This is the main motivation for the high-luminosity upgrade of the accelerator which is scheduled for the years following 2025 (Fig. 1.10). The upgraded accelerator is known as the *High-Luminosity LHC* (HL-LHC).

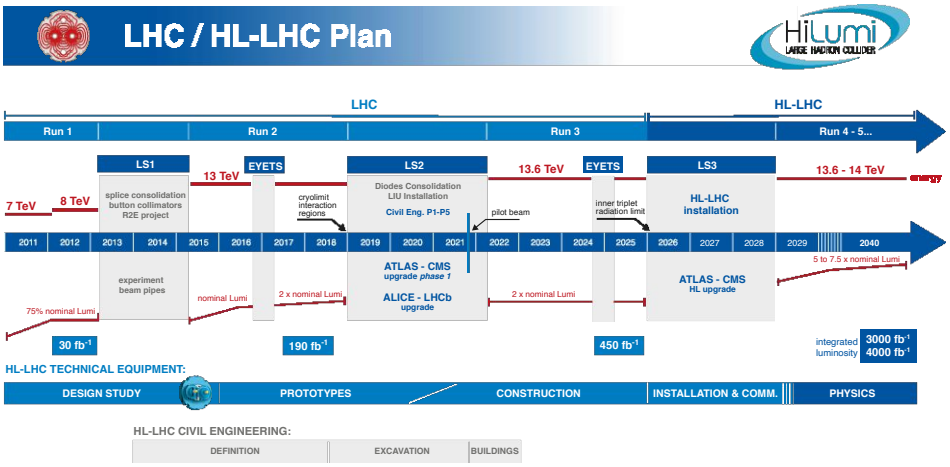

Fig. 1.10: CERN project schedule from LHC to high luminosity upgrade. Figure taken from [27].

The HL-LHC will provide a peak luminosity of 5×10^{34} $\text{cm}^{-2}\text{s}^{-1}$ or up to 7×10^{34} $\text{cm}^{-2}\text{s}^{-1}$ in the ultimate case. The center-of-mass energy will remain at 14 TeV as well as the bunch crossing frequency at 25 ns. The increase of the peak luminosity will result in an increased number of collisions per bunch crossing and a pile-up of 140 (or 200 in the ultimate scenario) events. HL-LHC is foreseen to operate for about 10 to 12 years which means that in the course of this time, the total integrated luminosity will reach 3000 - 4000 fb^{-1}.

The key to the increase in luminosity of the LHC is the further squeezing of the beams near the interaction point. New quadrupole magnets will be used in HL-LHC capable of producing a magnetic field up to 12 T. The magnets will be installed near the interaction points located at the CMS and ATLAS detectors. The properties of the superconducting material Nb_3Sn will be exploited.

In addition, crab cavities will be installed near the interaction points in order to reduce the crossing angle of the colliding beams. The beams are brought into collision at an angle of a few hundred microradians. This happens to prevent undesired collisions of bunches at either side of the interaction point since the two beams share the same vacuum chamber. However, a large crossing angle decreases the luminosity, as it reduces the overlap area of the bunches. In HL-LHC the crossing angle of the beams will be larger because the beam size will be reduced by a factor of two [28]. A larger crossing angle is a limiting factor for the increase in instantaneous luminosity. With the use of crab cavities, the head and the tail of each bunch will receive a kick in the opposite directions while the centroid of the bunch will receive no kick. Due to this deflection, the bunch overlap will be improved which increases the luminosity. A comprehensive overview of the physics plan and the technical upgrades for the transition to HL-LHC is given in [29]

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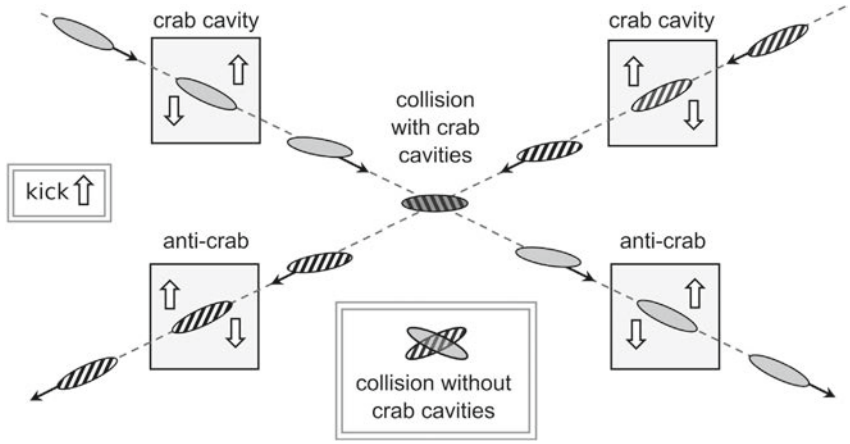


Fig. 1. Simplified diagram of the collisions at the IP with and without crab cavities. There is a π phase advance between crab and anti-crab cavities.

Fig. 1.11: Collisions at the interaction point with and without the use of crab cavities. Crab and anti-crab cavities feature a π phase difference [28].

Table 1
List of parameters for the baseline optics (HL-LHCV1.3).

Machine circumference	26 659 m
Proton energy at collision	7 TeV
Beam intensity N	2.2×10^{11} ppb
Number of bunch n_b	2748
r.m.s bunch length (σ_z)	9.0 cm
Bunch spacing	25 ns
Longitudinal emittance	3.03 eVs
Harmonic number	35 640
Transition gamma	55.76
Transverse normalized emittance $\epsilon_{(x,y)}$ (r.m.s)	2.5 μm
Revolution frequency	11.3455 kHz
Synchrotron frequency	23.8 Hz
RF frequency of main cavity	400.79 MHz
Total RF voltage of main cavity	16 MV
Full crossing angle	490 μrad
Crab cavity voltage	3.4 MV/cavity
Crab cavity RF frequency	400.79 MHz

1.4 CMS Phase-2 upgrade

In order to fully exploit the increased instantaneous luminosity provided by the HL-LHC, the CMS detector needs to be upgraded. This upgrade is known as the CMS *Phase-2 Upgrade*. The higher radiation levels require a more radiation-hard detector, more granularity to reduce the occupancy, while a larger bandwidth is necessary to accommodate the higher event rates.

In particular, the muon system will enhance its performance in tracking and triggering with the addition of new gas detector technologies: the Gas Electron Multiplier (GEM) detectors which have a superior high rate capability than the technologies used in the current system and the Resistive Plate Chamber (RPC) which has a very good timing resolution [30].

cavities in total are required). The total crabbing voltage required for full compensation at the IP[1] [11] is given as

$$V_1 = \frac{cE_s \tan\theta/2}{e\omega\sqrt{\beta^*\beta_{c.c}}\sin\mu}, \quad (2)$$

where c is the speed of light, E_s is the energy of the synchronous particle, e is the charge of the proton, ω is the angular frequency of the crab cavity RF, μ is the betatron phase advance between the upstream crab cavity and the IP, β^* and $\beta_{c.c}$ are the β functions at the IP and crab cavity locations respectively. The crab cavities are to be installed at locations where $\beta_{c.c}$ is large to reduce the required cavity voltages as determined by Eq. (2). The phase advance from the crab cavity to the IP and the IP to the anti-crab cavity are set as $\mu = \pi/2$. The required total anti-crab

representative bunch structure of the LHC bunch train is shown in Fig. 2. Consequently there is strong transient beam loading in the accelerating RF cavities (as opposed to the crab cavities) as there is full beam loading during a PS batch of 72 bunches (shown in blue) and zero beam loading during the gaps (shown in white).

To keep the accelerating cavity amplitude and phase constant over a full train of bunches making a whole turn of the LHC in the presence of transient beam loading, the klystron forward power takes an amplitude and phase modulation as dictated by the Low Level RF controls (LLRF) that responds to the gaps. Charged bunches passing through a cavity change its amplitude and phase. Acceleration cavities are detuned in the presence of high beam currents acting in quadrature to the RF current in order to reduce the power demanded from the klystrons at the LHC in the accelerating cavities). Because the cavities are detuned, the power demanded then peaks during each gap in the bunch train. The LHC's detuning scheme was optimized at the outset so that the demand for klystron power during gaps does not exceed 300 kW. This is achieved by detuning the cavity for half the peak beam current, hence the name "half detuning" [12,13]. The half-detuning scheme requires 200 kW average klystron power for the nominal LHC beam current (2808 bunches, 1.15×10^{11} particles per bunch). After optimization of the coupling between klystron and the cavity, the power requirement scales linearly with the beam current. The beam current for HL-LHC is almost double the nominal LHC current (2748 bunches, 2.2×10^{11} particles per bunch [1]), hence using the half detuning scheme, the required klystron average power will be near 400 kW and the peak power will be near to 600 kW. This level exceeds the klystron saturation power of 300 kW installed prior to 2008. All the accelerating RF systems installed at this time were designed for a maximum of 300 kW continuous wave (CW) operation. Increasing the RF power available for acceleration would require a significant modification of the RF power chain, including high voltage power supplies, klystrons, circulators,

The electron and hadron barrel calorimeters will undergo minor changes, unlike the endcap calorimeters which will be totally replaced. This replacement is motivated by the fact that the calorimeter endcaps are not foreseen to tolerate radiation levels higher than those which correspond to an integrated luminosity of about 500 fb^{-1} [31]. A new sampling calorimeter will be installed, namely the *High Granularity Calorimeter* (HGCAL). The electromagnetic section of HGCAL will comprise 28 sampling layers with silicon as the active material interspersed between Cu, CuW and Pb absorbers. The hadronic section will have 22 sampling layers and it will use two different technologies. The part which is closer to the interaction point, where the radiation levels are higher, will use silicon as the active medium. The part which corresponds to larger radii will use scintillators as an active medium. Steel will be used as the absorbing material.

The tracking system will see a full replacement of its inner and outer parts. Both sub-systems will be equipped with more radiation hard sensors and electronics which are specified to withstand the increased particle fluence and to offer high tracking efficiency under higher particle rates. More information regarding the upgrade is given in Chapter 2.

The trigger system will have to cope with the much higher data rates due to the increased pile-up. In order to maintain its discrimination capability and its sensitivity to interesting physics events, a number of improvements are scheduled. The addition of information from the Tracker in the Level-1 decision is one major modification [32]. The inclusion of tracking objects together with the information from the calorimeter and muon system in the L1 decision is a strategy which can satisfy a reduction in the L1 rate without deteriorating the physics performance of the detector [20]. The L1 trigger rate will be about 750 kHz (compared to the current 100 kHz) to exploit the full potential of the increase in peak instantaneous luminosity. The processing time for a trigger decision will be also longer with a latency of 12.5 µs due to the use of data from the Tracker. The use of modern FPGAs and processors, high-speed optical links for data aggregation and sophisticated reconstruction algorithms are some of the additional features of the upgraded Trigger system.

The Phase-2 CMS detector will feature a Minimum Ionising Particle Timing Detector (MTD) which aims to measure the precise timing of each track in order to associate it to interactions within a bunch crossing. The MTD will have a time resolution of 30-40 ps. This resolution is expected to degrade to 50-60 ps by the end of HL-LHC lifetime due to radiation damage [33]. The MTD exploits the fact that the occurring interactions within a bunch crossing are distributed over time with an RMS of 180 ps. The role of this subsystem is to collect timing information of the charged particles which will be combined with the tracking information to reconstruct vertices and tracks. With the use of this information, the pileup events which occur at overlapping times will be disentangled. The MTD consists of the Barrel Timing Layer (BTL) equipped with LYSO crystals and SiPMS and of the Endcap Timing Layer (ETL) which is instrumented with Low-Gain-Avalance-Diodes (LGADs). The selection of different technologies in the two regions is attributed to the different radiation levels that each of these detector regions will experience.

Chapter 2

Phase-2 upgrade of CMS tracker

The new CMS tracking system must maintain the performance of the current tracker in terms of track separation, efficiency and background rejection [34] but in the more severe environment of HL-LHC. Radiation tolerance and low occupancy at high pile-up are two conditions which should be fulfilled by the new system. In addition, the Phase-2 Outer Tracker will provide tracking information to the Level-1 (L1) Trigger of CMS. This will allow for a reduction of the data rates without sacrificing the physics performance of the detector. Although feasibility studies about the use of pixel information from the pixel detector in the Level-1 decision were conducted [35], the bandwidth and latency constraints at the L1 were a limiting factor. Therefore, the information from the Inner Tracker will be used only in the High-Level Trigger similar to the current CMS detector.

The following sections provide an overview of the most significant attributes characterizing the Phase-2 upgrade of the Outer Tracker. A brief discussion about the driving force of the upgrade will be followed by a description of the Phase-2 system layout, the new module concept as well as the building blocks which instrument each module. Since the new silicon sensors of the Outer Tracker are the main topic of this thesis, a comprehensive presentation of their features is given in Chapter 4.

2.1 Requirements for the tracker upgrade

This section summarizes the most critical requirements which should be satisfied by the CMS Tracker in the HL-LHC era. The reasons which make necessary the full replacement of the current Tracker with a more advanced system are also presented in the following paragraphs.

2.1.1 Radiation tolerance

The current CMS Tracker was designed to cope with an integrated luminosity of 500 fb^{-1}. Each run of HL-LHC is expected to deliver an integrated luminosity comparable to the total luminosity collected by CMS after the full life circle of LHC. After the end of its lifetime, HL-LHC will have delivered an integrated luminosity of 3000 - 4000 fb^{-1} to CMS. Figure 2.1 shows a FLUKA simulation of the anticipated particle fluence reaching all locations of the current tracking system after 300 fb^{-1} and after 3000 fb^{-1}. Each location of the current Tracker will see about one order of magnitude increase in particle fluence in the HL-LHC era. The innermost layer of the Tracker will have to cope with a total fluence up to a few 10^{16} n_{eq}/cm^2.

The current tracking system is not expected to withstand the high radiation levels of HL-LHC. Figure 2.2 shows a simulation of the number of failed modules of the current Tracker only after 1000 fb^{-1} of collected integrated luminosity. The simulation considers as a temperature the minimum sensor operation temperature of -20°C. A very large number of modules in the barrel as well as in the endcaps are not operational anymore after 1000 fb^{-1}. This failure will lead

to a deterioration of the tracking efficiency of the system and an increase in the fake rates, as illustrated in Fig. 2.3.

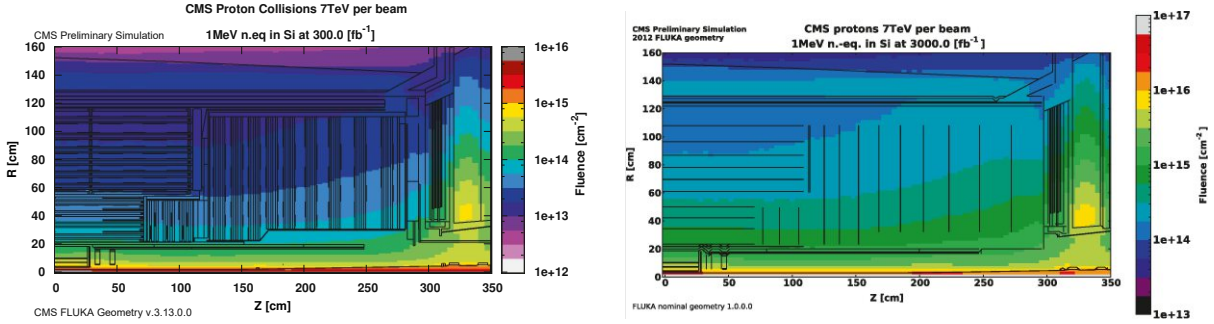


Fig. 2.1: FLUKA simulation of the total particle fluence in 1 MeV/cm^2 in silicon delivered to the current CMS Tracker after 300 fb^{-1} (left) and 3000 fb^{-1} (right).

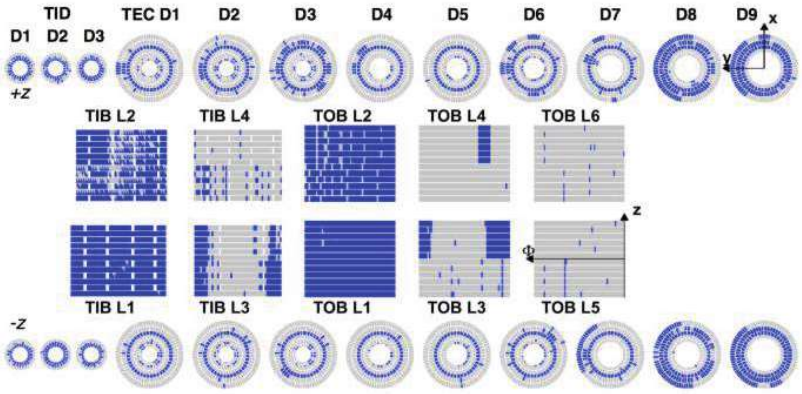


Fig. 2.2: Map of non-functional modules (blue) of the current CMS Outer Tracker after receiving 1000 fb^{-1} [36].

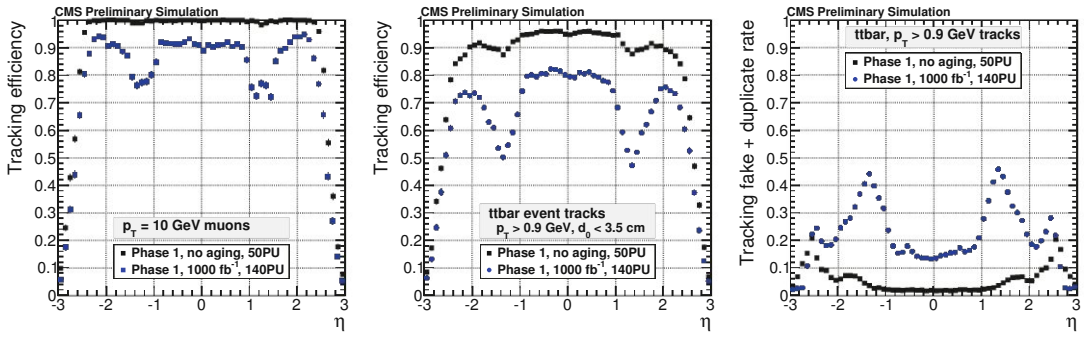


Fig. 2.3: Left: tracking efficiency for $p_T = 10$ GeV muons as a function of η for the current CMS Tracker before and after the Outer Tracker has received an integrated luminosity of 1000 fb^{-1}. Center: same plot for charged particles with a $p_T > 0.9$ GeV from tt^- events, produced in the transverse region at 3.5 cm from the interaction point. Right: the fraction of reconstructed tracks that are not matched to a simulated charged particle (fake rate) for the same particles in tt^- events. [36].

The development of a new, more radiation-hard tracking system is necessary. The new system will be instrumented with more advanced and radiation-tolerant silicon sensors and readout ASICs. The Inner Tracker will use pixel sensors of 100 × 25 µm^2 pixel size in all of its layers, except the innermost barrel layer which will be instrumented with 3-D pixel sensors of the same size [37]. The Inner Tracker is easily accessible and offers the possibility, if needed, to replace the modules of its innermost layers which are more susceptible to radiation damage due to their smaller distance from the interaction point. On the contrary, the Outer Tracker will not be replaced over the whole lifetime of HL-LHC.

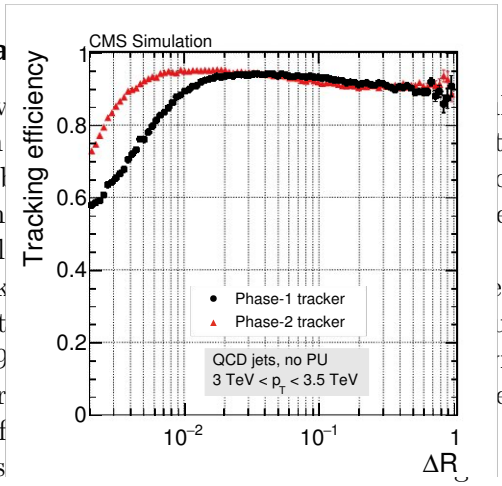


Figure 6.11: Tracking efficiency in cores of jets with $3 < p_T < 3.5$ TeV as a function of the distance between a simulated track and its nearest neighbour, ΔR, for the Phase-1 (black) and the Phase-2 (red) tracker, without pileup.

2.1.2 Tracking performa

The CMS Tracker will hav ltimate scenario) in HL-LHC. The challenge is to maintain t system under higher pile-up and to keep the occupancy l or the IT in all regions. This can be accomplished by an e Tracker. A more granular Tracker is required to handl

The Phase-2 Inner Track ls in total from 124 million channels which comprises t uter Tracker, the number of channels will increase from 9 ith the addition of about 170 million macro pixels. Figur e momentum resolution and the impact parameter as a f the current Tracker and the Phase-2 Tracker. The Phas η. Single muons of $p_T = 10$ GeV/c is used for the simulation. An improvement in both parameters is clearly seen due to the more granular Tracker as well as due to the reduction of the material budget, as discussed in the next paragraph.

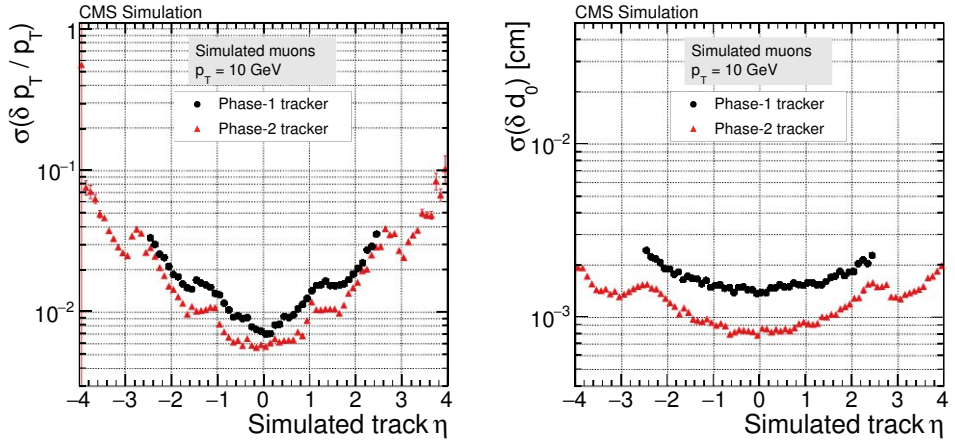


Figure 6.12: Relative resolution of the transverse momentum (left) and resolution of the transverse impact parameter (right) as a function of the pseudorapidity for the Phase-1 (black dots) and the Phase-2 Tracker (red triangles), using single isolated muons with a p_T of 10 GeV [20].

Fig. 2.4: Relative resolution of the transverse momentum (left) and resolution of the transverse impact parameter (right) as a function of the pseudorapidity for the Phase-1 (black dots) and the upgraded tracker (right) using single isolated muons with a transverse momentum of 10 GeV.

In Fig. 6.11 the tracking efficiency in jet cores is shown as a function of the distance between a simulated track and its nearest neighbour, $\Delta R = \sqrt{\Delta\eta^2 + \Delta\varphi^2}$, for the Phase-1 and the Phase-2 trackers. In the current Phase-1 reconstruction a special algorithm to split clusters has been implemented as well as a special iteration to perform robust tracking in jet cores. Although this has not yet been ported to the Phase-2 reconstruction, a significant improvement can already be seen for small values of ΔR thanks to the higher granularity of the new detector. Further improvement is expected for large values of ΔR as well after applying a similar tuning.

2.1.3 Material Budget

The reconstruction performance of the current tracking system is limited by the amount of material used. The effect of multiple scattering, Bremsstrahlung and photon conversion can be

decreased if a lighter Tracker is realized. This becomes feasible through the combined impact of several modifications, such as the decrease of layers in the barrel and in the endcap regions, the use of thinner pipes where the cooling CO_2 circulates, the utilization of lightweight mechanical structures made of carbon fiber, optimization of module and layout design. An illustration of the material budget expressed in terms of radiation length, in comparison to the current Tracker, is given in Fig. 2.5.

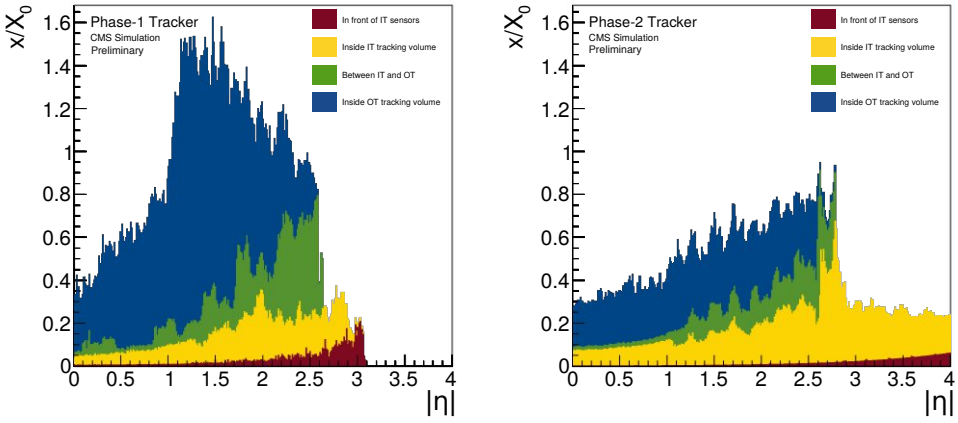


Fig. 2.5: Material budget inside the tracking volume expressed in radiation length, comparing the Phase-1 (left) and the Phase-2 (right) detectors.

2.2 The Phase-2 Tracker layout

A sketch of the Phase-2 Tracker design is shown in Fig. 2.6. Similar to the current system, the detector features a barrel and endcap region and is divided into an inner part (Inner Tracker) which is located at radii below $r < 20$ cm from the interaction point and an outer part (Outer Tracker) at distance 20 cm $< r <$ 120 cm. Each line represents a module that incorporates silicon sensors, read-out chips and mechanical and electrical support. The coverage of the tracking system is extended to $\eta = |4|$ which concerns the inner part. This extension will have a beneficial influence on the physics performance of the detector as well as on the pileup mitigation [20].

The Inner Tracker is instrumented with pixel sensors and covers an area of 4.9 m^2. It is comprised of 4 barrel layers and 12 disks at each end. As mentioned in the previous section, all Inner Tracker modules will feature pixel sensors of 100 $\times$ 25 μm^2 size, except the innermost layer, where 3-D pixel sensors will be installed. The 3-D pixel technology is chosen for the first layer of the IT due to the higher radiation tolerance and smaller power dissipation.

The Outer Tracker contains 6 barrel layers and 5 disks at each end. It is instrumented with strip and macro pixel sensors. It covers an area of roughly 200 m^2. Each module comprises two sensors and there are two module flavors: the 2S module with two strip sensors and the PS module with one strip and one macro pixel sensor. A singular feature of the Outer Tracker is that the PS modules in the first 3 layers of the barrel will be tilted so that they will be facing toward the interaction point. A tilted geometry offers better tracking and triggering efficiency than the flat barrel case since it maximizes the probability in these regions that a track crosses both sensors. This case is explained in [20]. In addition, the tilted geometry leads to a reduction in the number of modules populating the first three layers of the Outer Tracker barrel.

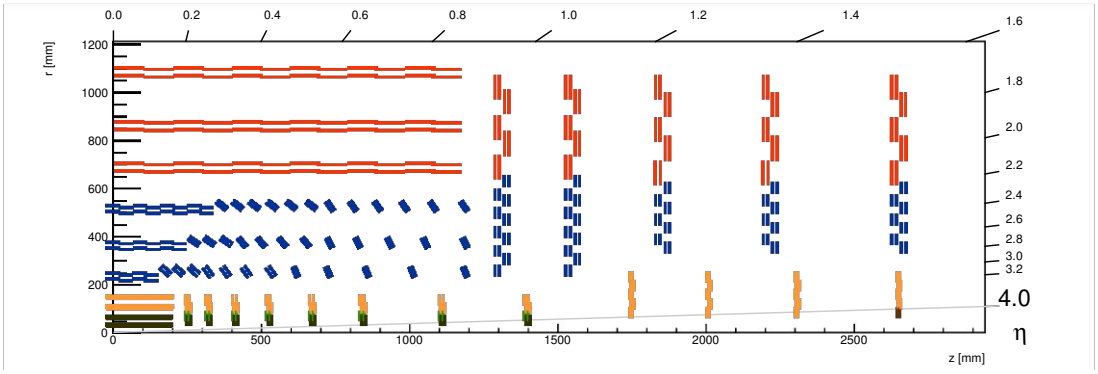


Fig. 2.6: Illustration of one quarter of the Phase-2 Tracker layout in r-z. In the Inner Tracker, the green and yellow lines correspond to pixel modules with two (green) and four (yellow) readout chips respectively. In the Outer Tracker, the blue lines represent the PS modules and the red lines the 2S modules. Each OT module is represented as a double line since it consists of two sensors [20].

2.3 The p_T selection concept

The addition of track information in the L1 trigger event selection is the driving force of the design of the Outer Tracker modules. The Outer Tracker modules will perform a filtering of events associated with low transverse momentum p_T tracks. Due to this novel functionality, the modules are known as p_T-modules.

Each p_T-module consists of two parallel, narrowly stacked sensors. The way p_T-modules perform the discrimination relies on the strong magnetic field of CMS which bends the charged particles emerging from the interaction point. The bending angle of the charged particle is inversely proportional to its transverse momentum. The passage of a particle from a module creates hit patterns on both sensors which are read out and correlated by the readout ASICs. The first silicon sensor acts as a seed while a search window is defined on the second sensor. If the occurring cluster of hits falls within this acceptance window, the track is associated with a high p_T particle which is known as a *stub*. The acceptance window is programmable and corresponds to p_T threshold above 2 GeV/c^2. An illustration of the p_T selection logic is shown in Fig. 2.7.

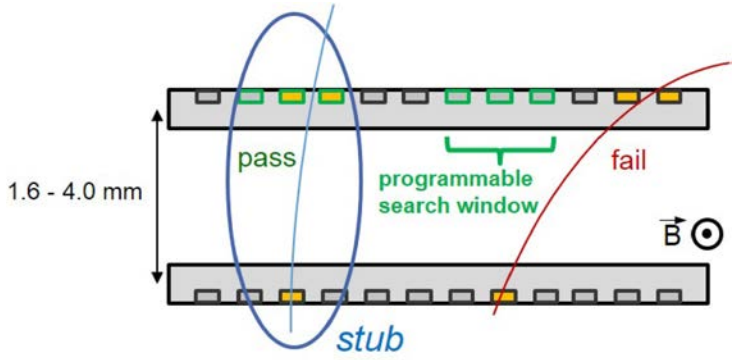


Fig. 2.7: Illustration of the p_T module concept. Each box represents a channel (strip or pixel). A passage of a charged particle creates signals on both sensors which are correlated. If they fall within an acceptance window they correspond to high p_T tracks and they are denoted as stubs [38].

The spacing between the two sensors of a module varies from 1.6 mm to 4 mm and depends on their location in the Tracker volume. The incident angle at which a charged particle crosses the module increases with the distance from the interaction point. To ensure high discriminating performance of high p_T tracks, the sensor spacing increases towards lower radii where the incident angle becomes smaller.

2.4 The Outer Tracker modules

The two type of Outer Tracker modules, the 2S and the PS module, are illustrated in Fig. 2.8. The main difference between the two modules is the granularity, as the PS modules feature a larger number of channels due to the use of macro pixel sensors.

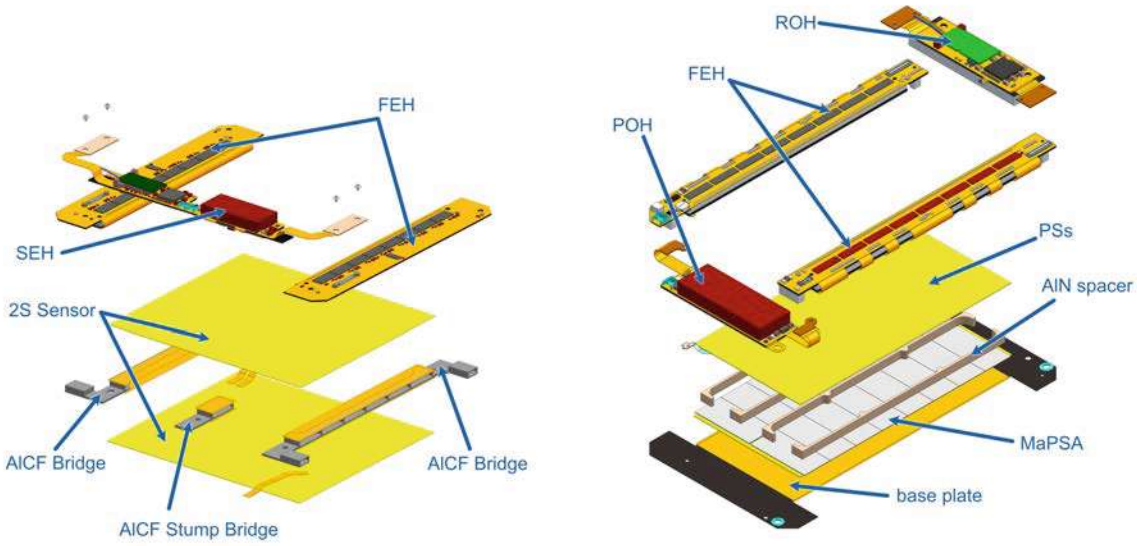
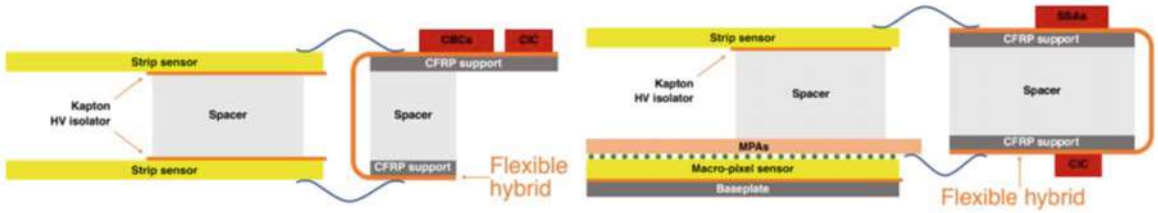


Fig. 2.8: The 2S (left) and the PS module (right). All abbreviations are explained in the main text.



(a) 2S module **(b)** PS module

Fig. 2.9: Sketches of the front-end hybrids and the connectivity of the Phase-2 Outer Tracker modules [20].

The PS module comprises a strip sensor with two banks of 960 strips. Each strip has a length of about 2.5 cm and a pitch of 100 µm. The macro pixel sensor features $2 \times 8 \times 16 \times 120$ (30720) pixels. Each pixel has a length of 1.5 mm and pitch of 100 µm. The macro pixel pitch is designed to match exactly the pitch of the PS strip sensor. The strips are wire-bonded to the binary *Short Strip ASIC* (SSA) [39]. A Front-End Hybrid (FEH) on each side houses 8 SSAs, therefore

120 strips are connected via wire-bonding to each readout ASIC. The macro pixel sensor is bump-bonded to 16 *Macro-Pixel-ASICs* (MPA) with 16 × 120 cells each [40]. The macro pixel sensor bump-bonded to its MPA chips is known as *macro pixel sub-assembly* (MAPSA). Each half of the strip sensor is read out separately by its respective SSAs. The signals from the SSAs are routed via the bent flex hybrid to the MPAs. Each MPA processes and sparsifies the hits from 1920 macro pixels. It correlates this information with the data received from the SSA and performs the stub-finding logic. The Power Hybrid (POH) is responsible for delivering the power to the ASICs for the PS module. The power consumption of a PS module is roughly 8 W. The Readout Hybrid (ROH) is responsible for data exchange (optoelectrical conversion) and module control.

The 2S module is instrumented with 2 identical sensors of 10 × 10 cm^2 size. A 2S sensor consists of 2 banks of 1016 strips. Each strip is 5 cm long with a pitch of 90 µm. The 2S module contains two Front-end Hybrids (FEH), one on each side. Each FEH hosts 8 ASICS which perform the readout of the sensors. The ASIC is called the *CMS Binary Chip* (CBC) [41], [42]. Each CBC is wire bonded to 254 strips with the odd channels connected to one sensor and the even channels connected to the other. The CBC performs the correlation logic for the stubs. The two FEHs are connected to the Service Hybrid (SEH), which is responsible for the data transmission and powering of the module. The power consumption of a 2S module is 5 W.

The on-module electronics

The CMS Binary Chip (CBC) is a binary readout ASIC developed in 130 nm CMOS technology and features 254 channels. It is connected to 127 channels of each sensor of the 2S module. The signal of each strip is amplified, shaped and fed into a comparator which returns a digital 1 if the signal exceeds a certain threshold. The ASIC includes all the logic to perform correlation between the signals of the two sensors and identify stubs which are transmitted at 40 MHz. Full hit information is stored in static random-access memory (SRAM) for 12.5 µs (L1 Trigger latency) and is read out upon arrival of a trigger signal from the Level-1 Trigger [42].

The Short Strip ASIC (SSA) is a binary readout ASIC developed in 65 nm CMOS technology and features 120 channels which are wire-bonded to 120 strips of the strip sensor of the PS module. The collected signals are amplified, shaped and then discriminated. The outcoming pulses are digitized and sampled at 40 MHz. In sequence, the digitalized hits are separated into two data paths: the stub data path and the L1 data path. The former are transmitted to the MPA where the correlation is performed while the latter are stored and are readout upon an L1 accept signal [39].

The Macro-Pixel ASIC (MPA) is a pixel readout ASIC developed in 65 nm CMOS technology and it features 16 × 120 channels. The signals coming from the pixels are processed by the analog front-end which consists of a pre-amplified, a shaper and a two-stage discriminator. The stub-finding logic of the MPA combines the front-end data coming from the pixel hits with the external data coming from SSAs and searches for stubs. The stub information is transmitted at 40 MHz. In parallel, a static RAM (SRAM) stores the full zero-suppressed hit information for a 12.5 µs until a L1 accept is received [40].

The Concentrator Integrated Circuit (CIC) is common for PS and 2S modules [43]. It is connected to all the ASICs of a service hybrid (CBCs or SSAs), and it collects and aggregates the data from the CBC (2S module) or MPA (PS module) and transmits it to the Low Power Gigabit Transceiver. Each module houses two CICs. The CIC aggregates the data coming from 48 input lines at the rate of 320 MHz. The output is transmitted at 320 MHz over 7 lines, among which, one is used for the full readout data and the rest are dedicated for the stub data transmission.

The Low Power Gigabit Transceiver (LpGBT) is hosted on the ROH for the PS modules and on the SEH for the 2S module. It receives, serializes and deserializes the data from the 2 CICs and performs an optical transmission with a Versatile Link Transceiver Plus (VTRx+) at 5.12 GB/s. The VTRx+ converts the data from electrical to optical signals and vice-versa and transmits them to the back-end electronics.

The DC-DC converter is responsible for the powering of the module ASICs. The 2S module houses the DC-DC converter on the FEH and the PS module hosts it on the POH. A two-stage DC-DC converter scheme provides low voltage to the electronics of the module. An input voltage of 10 – 12 V provided by the power supply system is converted into 2.55 V by the bPOL12V for the biasing of the optical electronics and as a second stage into 1.0 - 1.25 V by the bPOL5V for powering the ASICs. More information is provided in [44].

The module mechanics

As discussed in Section 2.1, the Tracker mass should be kept as low as possible in order to decrease the impact of multiple scattering on the track reconstruction. Therefore, the use of lightweight materials is desirable. In addition, the used materials should exhibit high thermal conductivity to allow for efficient dissipation of the heat generated by the electronics.

The 2S modules use spacers made of carbon fiber-reinforced aluminum (Al-CF). The Al-CF bridges serve as the main support element of the module and also play an important role in thermal management. In each 2S module, there are two long Al-CF bridges which span across the full width of the sensors and a smaller one which is placed between the sensors (Fig. 2.8(left)). The Al-CF is characterized by low density, high thermal conductivity and a low coefficient of thermal expansion (CTE) [20]. The CTE is indicative of the extent to which a material expands upon heating. Since silicon has low CTE, the mechanical support should feature a similar value to avoid mechanical stress induced during cooling the detector from room temperature to -30°C. The heat flow from the sensors and the hybrids is guided through the Al-CF bridges to the cooling system. The Al-CF bridges are electrically isolated from the backplane of the sensors through Polyimide films. The films or Kapton strips are glued in between the aluminum backside of the sensor and the Al-CF spacers. The bias voltage of the sensors is provided through flex cables (pigtails) from the SEH. The HV tails are wire-bonded to the sensor backplane and encapsulated to reduce any damage during handling.

The PS module is assembled onto a carbon fiber reinforced polymer (CFRP) base plate of 200 µm thickness, which in turn is glued to a larger area cooling joint to provide a thermal path for the heat dissipated in the sensors and MPA chips. This method differs from the 2S module due to the higher heat load generated by the MPAs. Therefore, the whole area of the bottom sensor is used in order to transfer the heat load of the module to the cooling system. The two sensors are separated by aluminum nitride (AlN) spacers. Due to the isolating properties of the AlN material, Polyimide films are not needed for HV isolation, unlike the 2S module. All hybrids (FEH, POH, ROH) are glued onto the CFRP baseplate at the two ends.

The heat load produced by the modules of the Outer Tracker must be removed efficiently by the cooling system and the sensors should remain always at $-20°C$ or lower. Cooling pipes will be responsible for the cooling of the modules. The Phase-2 cooling system is designed for a nominal coolant operating temperature of $-35°C$ and uses two-phase CO_2. The CO_2 is an ideal coolant because it is radiation-hard, cheap and environmentally friendly. The main advantage is that it allows for the utilization of lower diameter tubes due to its low density and its very good thermodynamic properties [45].

2.5 The L1 track finder

The L1 trigger system will receive about 15000 stubs at each bunch crossing, for a pile-up of 200. It must reconstruct L1 tracks within 5 µs in order to comply with the L1 trigger latency of 12.5 µs.

The stub data are sent out by the p_T modules at 40 MHz to the off-detector, backend readout electronics which are responsible for the track finding. An illustration of the data transmission path is given in Fig. 2.10. The modules interface through fiber optic links to the Data, Trigger and Control system (DTC) which consists of a custom-developed ATCA (Advanced Telecom Computer Architecture) blade based on commercial FPGAs. Each board can interface with many modules. The DTC extracts, pre-processes and transmits the stub data to the Track Finder Processor (TFP). In addition, it forwards the full event data to the DAQ system upon an L1 accept. The Outer Tracker is divided into 9 detector sectors in ϕ of equal size (Fig. 2.11). The modules of each detector sector interface to 24 DTCs. Each Track Finder Processor board receives input data from two neighboring detector sectors. In total, 162 TFP boards are employed. Each processing board receives an event every 450 ns (or every 18th bunch crossing), therefore a time-multiplexing factor of 18 is used.

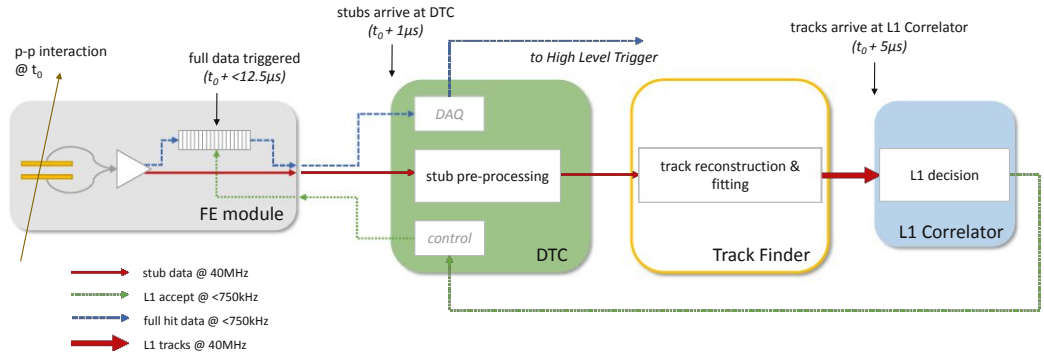


Fig. 2.10: The data transmission path and latency requirements for the L1 trigger decision [46].

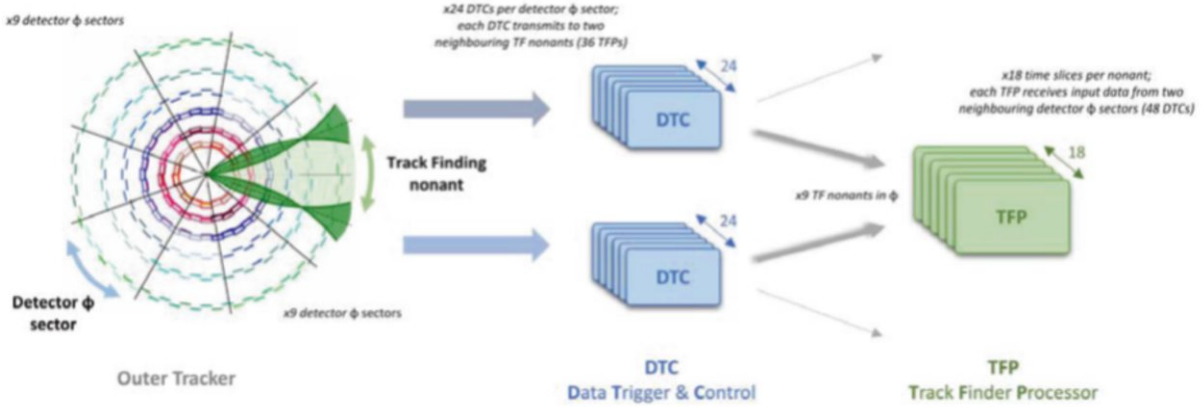


Fig. 2.11: Tracker geometry in the x - y plane. The L1 track finding system is divided into nine ϕ sectors (nonants), each processed by one track finding board for each of the 18 time-multiplexing (TM) slices showing the data flow through the data trigger and control boards (DTCs) to the track finding processor boards (TFPs) [20].

Figure 2.12 illustrates the logic which is used for the determination of a track from the module stubs. The algorithm forms seeds or tracklets from pairs of stubs in consecutive layers considering the primary interaction point as a constraint. The tracklets are extrapolated to the other layers and discs while the algorithm searches for matching stubs in small windows around the projection. An L1 track is formed by a minimum of 4 stubs. The track candidates are fitted with a Kalman filter algorithm to identify the best stub candidates and estimate the track parameters [47]. More information is given in [20].

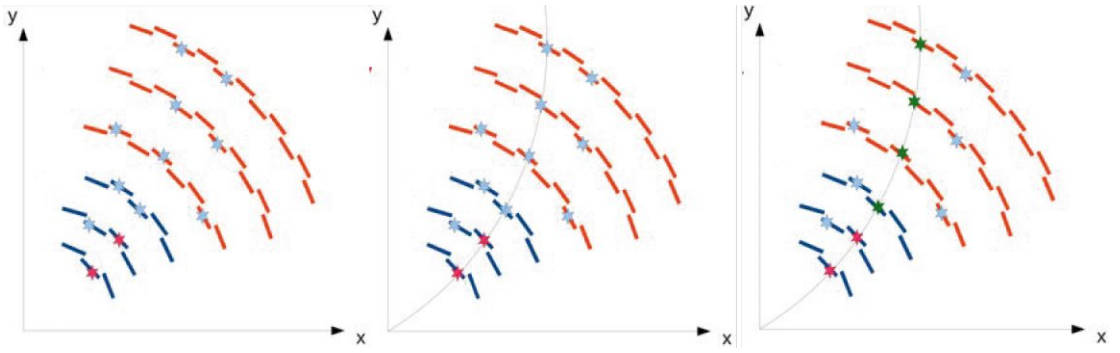


Fig. 5. An illustration of the track-finding algorithm concept [8]. First, stubs are paired up to create seeds (left). Using the seed and the origin, a rough helical track is calculated and projected to the other layers (middle). Then, stubs that are close enough to the track estimation in the other layers are matched to the track (right).

Fig. 2.12: An illustration of the track-finding algorithm logic. Pairs of stubs create seeds (left). Considering the seed and the interaction point, a helical track is calculated and extrapolated to the other layers (middle). The stubs of the other layers which are close enough to the track estimation are assigned to the track (right) [20].

The majority of the processing modules are implemented in firmware using High-Level Synthesis (HLS) [11]. It takes code similar to C++ and compiles it into firmware. A few modules, such as the Kalman Filter and the Track Quality module, as well as the intermediate memories, were implemented using the hardware description language VHDL. This grants more control over resource usage. The connections of each module and memory are made by using a VHDL top-level script. However, due to the great number of modules and memories involved, a script instantiates and compiles all module copies. A C++ software emulation writes out a map of all module and memory connections, and a Python script uses that map to write the top-level VHDL. This Python script also allows for top-level functions that only contain a fraction of the full track-finding chain for small-scale testing.

4.1 Stub Organisation

The first two steps organise the stubs into bins to reduce the processing time and number of combinations in future steps. The first module, the Input Router, sorts the stubs depending on which layer they come from. The data is streamed directly into the Input Router and the output is then saved to intermediate memories that are being read one-by-one by the VMRouter. The VMRouter organises the stubs into so-called Virtual Modules (VMs) that in each layer represent small regions in φ. The track-finding algorithm can then minimise the number of combinations simply by trying to create tracks using VMs that are compatible with a track $p_{\mathrm{T}} > 2$ GeV. Each VM corresponds to one intermediate memory in the upcoming processing.

4.2 Track Seeding

In the following step, the Tracklet Engine, the stubs in each layer are paired with stubs in the neighbouring layer to form track seeds. Only a few VMs need to be checked to find compatible matches. All stub pairs are then saved in a memory that is read by the Tracklet Calculator. It is worth noting that the same stub can be used in multiple pairs and that the seeding is performed in multiple layers. This creates redundancy to increase robustness against inefficient sensor modules. In the Tracklet Calculator, the seeds along with the interaction point are used to form track estimations, called tracklets. Thanks to the uniform magnetic field in CMS, the particles will travel according to a helix, thus the track parameters are evaluated by simple calculations. The tracklets are then projected

Chapter 3

Silicon detectors in high energy physics experiments

Semiconductor detectors have a long history in particle and nuclear physics starting from the 1960s with their use in experiments for gamma-ray energy measurements. Semiconductor detectors as position-sensitive devices were introduced in particle physics experiments around 1980. With their segmentation into electrodes of 50 to 100 µm range, they could provide high precision tracking measurements with excellent resolution [48].

Semiconductor materials are solids with an electrical conductivity which lies between that of conductors and insulators. Typically, the semiconductors feature a resistivity which is between 10^{-3} to 10^{8} Ωcm. The most common semiconductors belong to group IV (e.g Carbon, Silicon, Germanium) of the periodic table or they are compounds, which means that they are formed as a combination of elements from group III (e.g Boron, Gallium, Indium) and group V (e.g Phosphorus, Arsenic, Antimony) or group II and group VII.

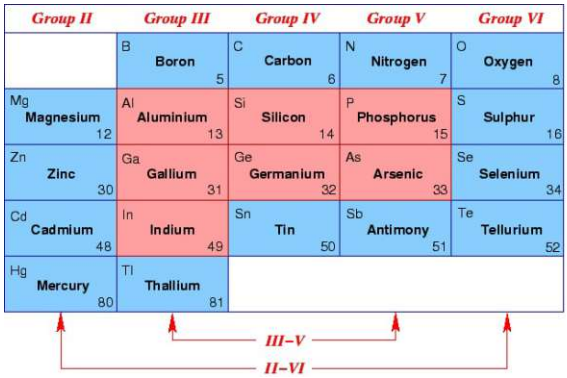


Fig. 3.1: Part of the periodic table displaying the elements involved in the formation of semiconductors.

The most commonly used material in semiconductor detectors is silicon due to its large abundance in nature. It is only present in compounds, mostly as silicon dioxide (SiO_2). The semiconductor industry has a lot of experience in exploiting silicon for microelectronics. High-energy physics experiments benefit a lot from the modern developments in the silicon industry. The following sections present the basic properties of silicon as a material used in detectors for high-energy physics experiments. In addition, the basic principles of a silicon sensor as a position-sensitive device are discussed.

3.1 Silicon properties

Silicon has a diamond lattice structure and belongs to the IV group of the periodic table. As a tetravalent material, it features four valence electrons in its outer shell, each of which

forms a covalent bond with one valence electron of a neighboring Si atom (Fig 3.2). The atoms of the lattice are arranged in close relative distances, the electrons of the neighboring atoms interact with each other and as a consequence, the discrete energy levels of electrons in individual atoms degenerate into bands of allowed energies. This effect is dictated by the Pauli's exclusion principle. The bands of allowed energies that electrons can occupy are separated by bands of forbidden energies.

An example considering an isolated silicon atom is displayed in Fig 3.3. Silicon has an atomic number of 14. The first ten electrons of the silicon atom occupy the first two levels. The remaining 4 are less tightly bound and occupy the n = 3 level. The 3s state (n = 3, l = 0) contains two quantum states while the 3p (n = 3, l = 1) state contains 6 states. As the neighboring atoms come closer and the interatomic distance decreases, the 3s and 3p states interact and degenerate. At the equilibrium interatomic distance (a_0) the bands split again forming four quantum states in the lower band and four quantum states in the upper band. At T = 0K, the lower band (valence band) is fully occupied and all states in the upper band (conduction band) are empty. The energy difference between the top of the valence and the bottom of the conduction band is described by the *bandgap energy* E_g. The bandgap energy of silicon is $E_g = 1.12$ eV.

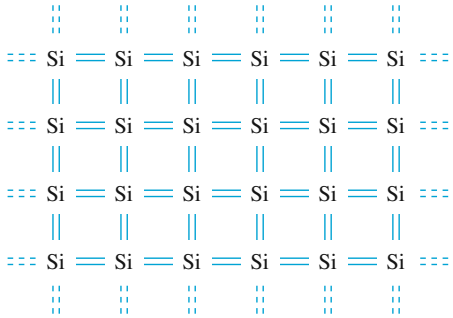


Fig. 3.2: Intrinsic silicon crystal lattice [49].

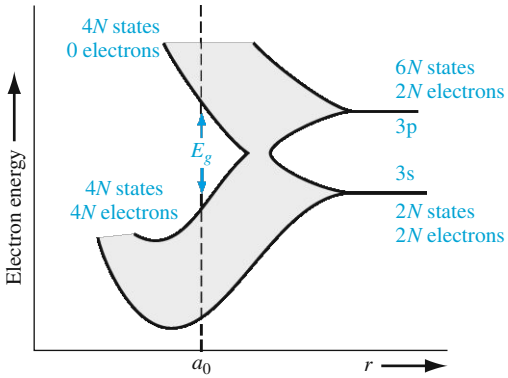


Fig. 3.3: Illustration of splitting of three energy states into allowed energy bands [49].

3.1.1 Intrinsic silicon

Intrinsic is called the semiconductor when no dopants are added to its crystal lattice. An intrinsic silicon at 0K is an insulator, which means that all the energy states of the conduction band are empty. At T > 0K, electrons from the valence band can acquire enough energy due to

thermal excitation in order to jump into the conduction band. The required energy should exceed the energy of the bandgap. Whenever an electron moves from the valence to the conduction band, it leaves an empty state behind which corresponds to a hole and acts like a positive charge. The relatively small bandgap of intrinsic silicon allows electrons to populate its conduction band at room temperature.

The probability that an electron occupies a quantum state with an energy E is given by the Fermi-Dirac formula:

$$F(E) = \frac{1}{1 + \exp\left(\frac{E - E_\mathrm{F}}{k\mathrm{T}}\right)} \tag{3.1}$$

where k is the Boltzmann constant, T is the temperature and E_F is the Fermi level, the energy at which the probability of occupation is 1/2. At T = 0K, the Fermi energy describes the limit below which all states are filled with electrons ($F(E < E_\mathrm{F}) = 1$) and above which all states are empty ($F(E > E_\mathrm{F}) = 0$).

For an intrinsic silicon in thermal equilibrium, the concentration of electrons in the conduction band is described by the formula:

$$n_\mathrm{i} = N_\mathrm{c} \exp\left(\frac{-(E_\mathrm{c} - E_\mathrm{Fi})}{k\mathrm{T}}\right) \tag{3.2}$$

where N_c is the effective density of states function in the conduction band, E_c is the bottom energy of the conduction band and E_Fi is the intrinsic Fermi energy ($E_\mathrm{Fi} = E_\mathrm{F}$).

Similarly, the concentration of holes in the valence band is given as:

$$p_\mathrm{i} = N_\mathrm{v} \exp\left(\frac{-(E_\mathrm{Fi} - E_\mathrm{v})}{k\mathrm{T}}\right) \tag{3.3}$$

where N_v is the effective density of states function in the valence band and E_v is the top energy of the valence band.

Since in thermal equilibrium the concentration of electrons and holes in an intrinsic silicon is equal, one can define the intrinsic carrier density by using (3.2), (3.3) as:

$$n_\mathrm{i} p_\mathrm{i} = n_\mathrm{i}^2 = N_\mathrm{c} N_\mathrm{v} \exp\left(\frac{-(E_\mathrm{c} - E_\mathrm{v})}{k\mathrm{T}}\right) = N_\mathrm{c} N_\mathrm{v} \exp\left(\frac{-E_\mathrm{g}}{k\mathrm{T}}\right) \tag{3.4}$$

where E_g is the bandgap energy.

The intrinsic carrier concentration is temperature dependent as it is obvious by equation (3.4). For silicon in room temperature, it is $n_\mathrm{i} = 1.5 \times 10^{10}$ cm^{-3}.

The Fermi energy can be derived from equations (3.2), (3.3):

$$E_\mathrm{Fi} = \frac{E_\mathrm{c} + E_\mathrm{v}}{2} + \frac{k\mathrm{T}}{2} \ln\left(\frac{N_\mathrm{v}}{N_\mathrm{c}}\right) = E_\mathrm{midgap} + \frac{k\mathrm{T}}{2} \ln\left(\frac{N_\mathrm{v}}{N_\mathrm{c}}\right) \tag{3.5}$$

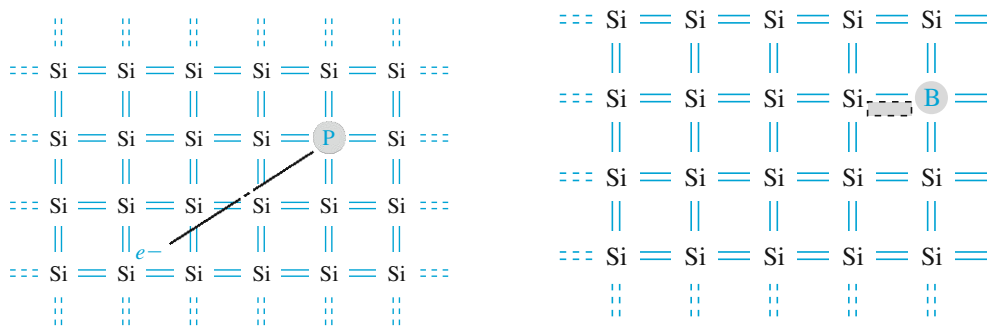
This is a very important equation describing how the intrinsic Fermi level shifts with respect to the density of states. If $N_\mathrm{c} > N_\mathrm{v}$, the intrinsic Fermi level is below the center of the bandgap, if $N_\mathrm{v} > N_\mathrm{c}$ the intrinsic Fermi level is above the center and if $N_\mathrm{v} = N_\mathrm{c}$ it is located exactly at the midgap. In other words, the intrinsic Fermi level shifts away from the band which features a larger density of states in order to maintain equilibrium.

3.1.2 Extrinsic silicon - Doping

Extrinsic is called the silicon with a controlled amount of dopants or impurity atoms added to its crystal lattice. The process of adding impurities in the crystal lattice is called *doping*.

When atoms of the VI group of the periodic table are added, for instance, arsenic (As) or phosphorus (P), then this is known as a n-type doping (Fig. 3.4a). The dopant atoms are known as donors because they have an excess of a valence electron with respect to silicon. This electron does not form covalent bonds, is weakly bound and can easily jump into the conduction band. The presence of a donor creates an additional energy state in the bandgap which is located near the conduction band.

When atoms of the III group are added, for example, boron (B), this is known as a p-type doping (Fig. 3.4b). The dopant atoms are known as acceptors and they feature one fewer valence electron than the silicon. An electron from a neighboring silicon atom jumps in to fill this vacant state and forms a covalent bond. This transition creates a new vacant state which is equivalent to the presence of a hole. The presence of an acceptor creates an additional energy state in the bandgap which is located near the valence band.



(a) n-type silicon lattice doped with phosphorus (P) atom.

(b) p-type silicon lattice doped with boron (B) atom.

Fig. 3.4: Extrinsic silicon crystal lattice [49].

Since doping changes the distribution of electrons and holes in the silicon crystal, the Fermi level shifts according to the type of doping. When $E_F > E_{Fi}$ the concentration of electrons is larger than the concentration of holes (n-type). On the other hand, when $E_F < E_{Fi}$ the concentration of holes is larger than the concentration of electrons (p-type). Both cases are illustrated in Fig. 3.5.

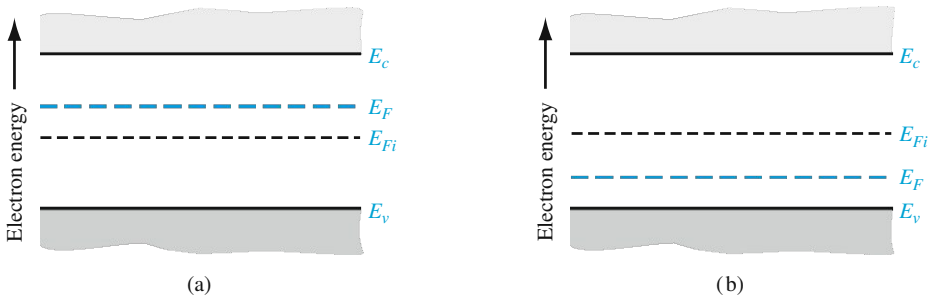


Fig. 3.5: Position of Fermi level in the band gap for (a) a n-type silicon and (b) for a p-type silicon.

3.1.3 Charge carrier transport mechanisms

The movement of charge carriers inside the silicon bulk is called transport and depends on two main mechanisms: drift and diffusion. These mechanisms are responsible for the net flow of electrons and holes which generates electric currents. They determine the current-voltage characteristics of silicon devices.

Drift

When an external electric field is applied to silicon, the electrons and holes will undergo an acceleration and consequently a net movement. This movement under the influence of an electric field is called *drift*. The current generated by the drift is called drift current.

The electron (or hole) which gets accelerated by an electric field E is also subjected to scattering processes with atoms of the lattice which decelerate it. Hence, the drift velocity is replaced by an average drift velocity which is defined as:

$$u_{\mathrm{d}}^{\mathrm{n}} = -\mu_{\mathrm{n}} E \quad \text{electrons} \tag{3.6}$$

$$u_{\mathrm{d}}^{\mathrm{p}} = \mu_{\mathrm{p}} E \quad \text{holes} \tag{3.7}$$

where μ_{n} and μ_{p} is the electron and hole mobility. The mobility is a function of temperature, doping concentration and effective mass of the particle. Since electrons have smaller effective mass than holes, their mobility is larger. For silicon at T = 300K, it is $\mu_{\mathrm{n}} = 1350\ \mathrm{cm}^2/(\mathrm{Vs})$ and $\mu_{\mathrm{p}} = 450\ \mathrm{cm}^2/(\mathrm{Vs})$.

The drift current density due to electrons/holes can be expressed as:

$$J_{\mathrm{d}}^{\mathrm{n}} = -enu_{\mathrm{d}}^{\mathrm{n}} = en\mu_{\mathrm{n}} E \quad \text{electrons} \tag{3.8}$$

$$J_{\mathrm{d}}^{\mathrm{p}} = epu_{\mathrm{d}}^{\mathrm{n}} = ep\mu_{\mathrm{p}} E \quad \text{holes} \tag{3.9}$$

where n and p are the volume charge density of electrons and holes respectively. Both charge carriers contribute to the total current, thus one can combine equations (3.8) and (3.9) in order to get the total drift current density as:

$$J_{\mathrm{d}} = en\mu_{\mathrm{n}} E + ep\mu_{\mathrm{p}} E = e(n\mu_{\mathrm{n}} + p\mu_{\mathrm{p}})E \tag{3.10}$$

From equation (3.10) one can define the conductivity σ as:

$$\sigma = e(n\mu_{\mathrm{n}} + p\mu_{\mathrm{p}}) \tag{3.11}$$

The conductivity is given in units $(\Omega\mathrm{cm})^{-1}$. Similarly the resistivity ρ can be defined as:

$$\rho = \frac{1}{\sigma} = \frac{1}{e(n\mu_{\mathrm{n}} + p\mu_{\mathrm{p}})} \tag{3.12}$$

The resistivity is given in units Ωcm.

Diffusion

Diffusion is the process in which particles flow from a region of high concentration to a region of low concentration. This flux creates a diffusion current. The diffusion current density is described by Flick's law according to the equation:

$$J_{\text{diff}}^{\text{n}} = eD_{\text{n}}\frac{dn}{dx} \quad \text{electrons} \tag{3.13}$$

$$J_{\text{diff}}^{\text{p}} = -eD_{\text{p}}\frac{dp}{dx} \quad \text{holes} \tag{3.14}$$

where D_{n} and D_{p} is the electron and hole diffusion coefficient, n, p the electron and hole concentration.

Combining equations (3.10), (3.13), (3.14) one can define the total current density as:

$$J = e(n\mu_{\text{n}} + p\mu_{\text{p}})E + eD_{\text{n}}\frac{dn}{dx} - eD_{\text{p}}\frac{dp}{dx} \tag{3.15}$$

3.1.4 The p-n junction

The p-n junction or diode is one of the most fundamental and interesting semiconductor devices. It is formed when n-type and a p-type silicon are brought into contact. The electrons which are the majority carriers of the n-type semiconductor, begin to diffuse into the p-type region where they have a lower concentration. Similarly, the holes, as the excess carriers of the p-type semiconductor diffuse into the n-type region. The diffusion of electrons to the p-side leaves positive donor atoms behind, while the diffusion of holes to the n-side leaves negative acceptor atoms in the p-type region. As an outcome of this process, a region depleted of free charges is formed at the border of the p-n contact. This region is known as the *depletion region* or the *space charge region*. The net charges of the n and p regions induce an electric field with direction from the n side (positive charge) to the p side (negative charge). This electric field opposes the diffusion of charge carriers and as a result, limits the expansion of the depletion region. This process is displayed in Fig. 3.6.

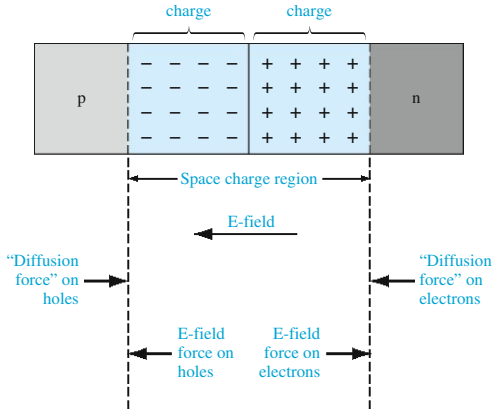


Fig. 3.6: Illustration of a p-n junction with the space charge region [49].

Figure 3.7 shows a sketch of the energy band diagram of a p-n junction. The junction is at thermal equilibrium, thus a constant Fermi level across the whole p-n junction can be assumed.

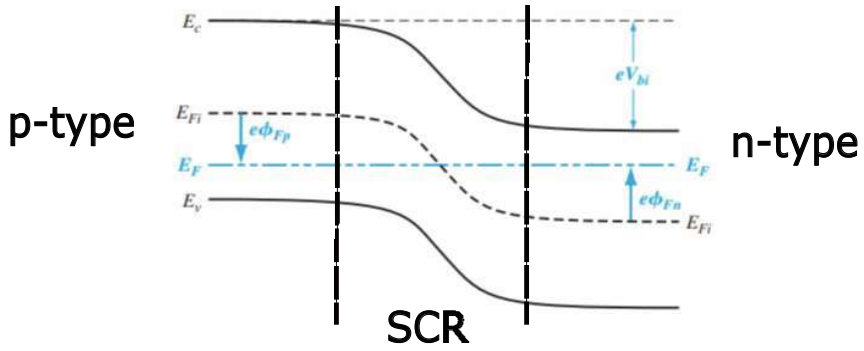


Fig. 3.7: The energy band diagram showing the formation of the space charge region (SCR) when n-type and a p-type silicon are brought into contact. The figure is taken and modified from [49].

No external potential is applied in this case. The relative position of the conduction and valence bands with respect to the Fermi level is different in p and n type regions. Therefore, when brought into contact, the valence and the conduction bands of the two semiconductors must bend towards the space charge region. The electrons in the conduction band of the n-type region must overcome a potential barrier when they move into the conduction band of the p-type side. This is the so-called *built-in potential* V_{bi}. This built-in potential maintains equilibrium between majority carriers of one side (for instance electrons for n-type silicon) and minority carriers of the other side (for instance electrons for p-type silicon), hence no current is produced by this voltage. One can define as ϕ_{Fn} and ϕ_{Fp} the potentials which describe the difference between the Fermi level of the p-n junction and the intrinsic Fermi level of each of the n, p-type semiconductors.

The built-in potential can be calculated by the formula:

$$V_{\mathrm{bi}} = |\phi_{\mathrm{Fp}}| + |\phi_{\mathrm{Fn}}| = \frac{E_{\mathrm{F}} - E_{\mathrm{Fi}}^{\mathrm{p}}}{q} + \frac{E_{\mathrm{Fi}}^{\mathrm{n}} - E_{\mathrm{F}}}{q} = \frac{k\mathrm{T}}{q} \ln\left(\frac{N_{\mathrm{A}} N_{\mathrm{D}}}{n_{\mathrm{i}}^2}\right) \tag{3.16}$$

The width of the depletion region d depends on the doping concentration of the two materials which form the junction. In the case of asymmetric doping, the depletion region extends more into the less doped region. The total width of the space charge region is the sum of the widths of the depletion region of the n and p type sides [50]:

$$\begin{aligned} d = d_{\mathrm{n}} + d_{\mathrm{p}} &= \sqrt{\frac{2\epsilon_0\epsilon_r V_{\mathrm{bi}}}{q} \frac{N_{\mathrm{D}}}{N_{\mathrm{A}}(N_{\mathrm{A}} + N_{\mathrm{D}})}} + \sqrt{\frac{2\epsilon_0\epsilon_r V_{\mathrm{bi}}}{q} \frac{N_{\mathrm{A}}}{N_{\mathrm{D}}(N_{\mathrm{A}} + N_{\mathrm{D}})}} \\ &= \sqrt{\frac{2\epsilon_0\epsilon_r V_{\mathrm{bi}}}{q(N_{\mathrm{A}} + N_{\mathrm{D}})}} \left(\sqrt{\frac{N_{\mathrm{D}}}{N_{\mathrm{A}}}} + \sqrt{\frac{N_{\mathrm{A}}}{N_{\mathrm{D}}}}\right) \\ &= \sqrt{\frac{2\epsilon_0\epsilon_r V_{\mathrm{bi}}(N_{\mathrm{A}} + N_{\mathrm{D}})}{q N_{\mathrm{A}} N_{\mathrm{D}}}} \end{aligned} \tag{3.17}$$

Reverse bias

The equilibrium is violated when an external voltage is applied between the n and p-type region. The diode is reverse biased when a positive voltage is applied to the n-type and a negative to the p-type region. Electrons from the n-type and holes from the p-type regions start to move

toward the electrodes while the width of the space charge region increases. The total potential barrier is $V_{\text{tot}} = V_{\text{bi}} + V_{\text{bias}}$. From equation (3.17) it is:

$$d = \sqrt{\frac{2\epsilon_0\epsilon_r(V_{\text{bi}} + V_{\text{bias}})(N_{\text{A}} + N_{\text{D}})}{qN_{\text{A}}N_{\text{D}}}} \tag{3.18}$$

For asymmetric doping where $N_{\text{D}} >> N_{\text{A}}$, equation (3.18) can be written as:

$$d = \sqrt{\frac{2\epsilon_0\epsilon_r(V_{\text{bi}} + V_{\text{bias}})}{qN_{\text{A}}}} \tag{3.19}$$

In reverse bias mode, the diode conducts essentially no current due to its large depletion region. The width of the space charge region increases with increasing bias voltage as can be clearly seen from equation (3.18). In reality, a very small current flows through the diode. This current, the so-called *leakage current* (or dark current), has two components: a current generated by the charge carriers which diffuse into the depletion region and a current generated by the electron-hole pairs which are created inside the depletion region due to the temperature.

Forward bias

When a positive voltage is applied to the p-type side and a negative voltage is applied to the n-type side, the diode is in forward bias mode. Due to the external electric field, electrons and holes move towards the space charge region and the depletion zone shrinks. The equation 3.17 is written as:

$$d = \sqrt{\frac{2\epsilon_0\epsilon_r(V_{\text{bi}} - V_{\text{bias}})(N_{\text{A}} + N_{\text{D}})}{qN_{\text{A}}N_{\text{D}}}} \tag{3.20}$$

When $V_{\text{bias}} > V_{\text{bi}}$, the depletion region width is negligible and a current starts flowing through the diode in one direction.

Current - Voltage characteristics

The current-voltage characteristics of a diode are described by the Shockley equation [51] as follows:

$$I = I_{\text{s}}\left(\exp\left(\frac{qV_{\text{bias}}}{k\text{T}}\right) - 1\right) \tag{3.21}$$

where I_{s} is the reverse bias saturation current. This equation implies that for forward biasing ($V_{\text{bias}} > 0$) the diode current increases exponentially. For reverse biasing ($V_{\text{bias}} < 0$) the current saturates at $I = -I_{\text{s}}$. This is the leakage current. In an ideal case where the leakage current comes only from the diffusion process, I_{s} can be expressed as:

$$I_{\text{s}} = eA\left(\frac{D_{\text{n}}n_{\text{po}}}{L_{\text{n}}} + \frac{D_{\text{p}}n_{\text{no}}}{L_{\text{p}}}\right) \simeq eA\left(\frac{D_{\text{n}}n_{\text{i}}^2}{L_{\text{n}}N_{\text{A}}} + \frac{D_{\text{p}}n_{\text{i}}^2}{L_{\text{p}}N_{\text{D}}}\right) \tag{3.22}$$

where $D_{\text{n,p}}$ is the diffusion coefficient for electrons and holes, A is the cross sectional area and $L_{\text{n,p}}$ the diffusion length of electrons-holes.

The second mechanism is related to the current generated inside the depletion region due to thermal generation at the generation-recombination centers. These centers in the bandgap are attributed to defects or impurities inside the silicon bulk. This mechanism dominates the leakage current and is proportional to the depleted volume as:

$$J_{\text{vol}} \simeq -e\frac{n_{\text{i}}}{\tau_{\text{g}}}d \tag{3.23}$$

where J_{vol} is the volume generated leakage current per unit area A, τ_{g} is the carrier generation lifetime, n_{i} is the intrinsic carrier concentration and d is the depletion width. Since n_{i} is temperature dependent, as deduced from equation (3.2), the temperature dependence is inserted in the volume generated current as:

$$J_{\text{vol}} \propto \text{T}^2 \exp\left(\frac{-E_{\text{g}}(\text{T})}{2k\text{T}}\right) \tag{3.24}$$

A standard rule of thumb is that the J_{vol} doubles every 7K.

At very high negative voltages the diode can exhibit a rapid increase of its current, as shown in Fig. 3.8. The voltage at which this effect occurs is called the *breakdown voltage*.

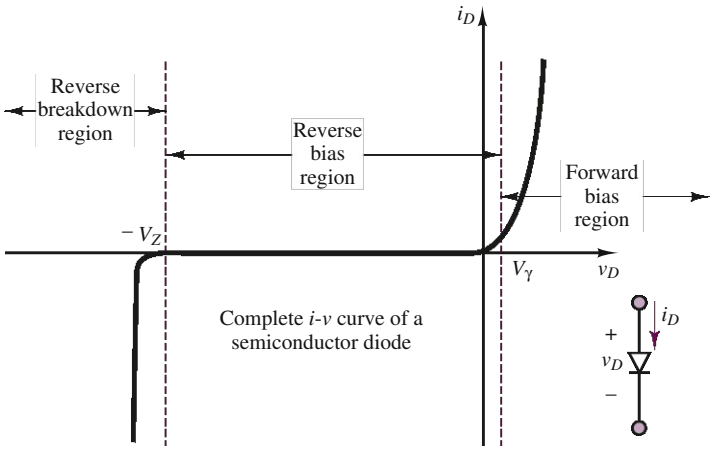


Fig. 3.8: I-V characteristics of a typical diode. The different operation modes are shown. The offset voltage V_γ is the voltage beyond which a noticeable current is conducted through the diode. V_{Z} is the Zener or breakdown voltage [52].

The breakdown effect is a result of a very strong electric field applied to the reverse biased diode and has two main mechanisms [50]. The first one is the *Zener effect* which typically happens in heavily doped p-n regions. Such p-n junctions have narrow depletion widths which results in a very high electric field. A high electric field can give enough energy to the covalent electrons of the atoms in the depletion region to break their bonds. The free electrons are accelerated by the electric field and drift towards the n-type side. The second mechanism is the *Avalanche effect*. As the bias voltage increases, the free charge carriers inside the depletion region are accelerated by the strong electric field and if they gain sufficient kinetic energy, they can transfer enough energy to the electrons of the Si atoms to break their covalent bonds. This phenomenon (impact ionization) can create an avalanche inside the depletion region. This avalanche of charge carriers across the junction leads to a dramatic increase in the diode current.

3.3 CIRCUIT MODELS FOR THE SEMICONDUCTOR DIODE

From the viewpoint of a *user* of electronic circuits (as opposed to a *designer*), it is often sufficient to characterize a device in terms of its i-v characteristic, using either load-line analysis or appropriate circuit models to determine the operating currents and voltages. This section shows how it is possible to use the i-v characteristics of the semiconductor diode to construct simple yet useful *circuit models*. Depending on the desired level of detail, it is possible to construct *large-signal models* of the diode, which describe the gross behavior of the device in the presence of relatively large voltages and currents; or *small-signal models*, which are capable of describing the behavior of the diode in finer detail and, in particular, the response of the diode to small changes in the average diode voltage and current. From the user's standpoint, these circuit models greatly simplify the analysis of diode circuits and make it possible to effectively analyze relatively "difficult" circuits simply by

Capacitance-Voltage characteristics

In a simplified case, the diode can be considered as a parallel plate capacitor in which the depletion region acts as the dielectric between the n and p-type electrodes. In such a scenario, the capacitance of the diode can be expressed as:

$$C = \epsilon_0 \epsilon_r \frac{A}{d}$$

where d is the width of the depletion region, given by the equation (3.18). Inserting equation 3.19 ($N_D >> N_A$), the capacitance can be written as:

$$C = A\sqrt{\frac{\epsilon_0 \epsilon_r q N_\mathrm{A}}{2(V_\mathrm{bi} + V_\mathrm{bias})}} \tag{3.25}$$

The required voltage to deplete the full active volume of the diode is known as the *full depletion voltage* ($\mathrm{V_{FD}}$). This is a crucial parameter for the silicon sensors since it defines the minimum operation voltage. Assuming a fully depleted diode of thickness D and $\mathrm{V_{FD}} >> \mathrm{V_{bi}}$, then the full depletion voltage can be expressed as:

$$V_\mathrm{FD} = \frac{q N_\mathrm{A} D^2}{2\epsilon_0 \epsilon_r} \tag{3.26}$$

The resistivity can be inserted in (3.26) via (3.12) which results in the following formula:

$$V_\mathrm{FD} = \frac{D^2}{2\epsilon_0 \epsilon_r \mu_\mathrm{h} \rho} \tag{3.27}$$

As equation (3.27) states, the full depletion voltage is proportional to the square of the sensor thickness and reciprocal to the wafer resistivity.

3.2 Interaction of charged particles with silicon

The operation of a silicon sensor as a particle detector depends on the interaction of a charged particle crossing its volume with its atoms. Any charged particle which traverses a material loses part of its energy through inelastic collisions with the electrons of the surrounding atoms. The mean energy loss of a charged particle due to ionization and excitation is given by the Bethe-Bloch formula:

$$-\frac{dE}{dx} = 2\pi N_A r_e^2 m_e c^2 \rho \frac{Z}{A}\frac{z^2}{\beta^2}\left[\ln\left(\frac{2m_e\gamma^2 u^2 W_\mathrm{max}}{I^2}\right) - 2\beta^2 - \delta - 2\frac{C}{Z}\right] \tag{3.28}$$

where:

- $2\pi N_0 r_e^2 m_e c^2 = 0.1535\ \mathrm{MeV}c^2/\mathrm{g}$
- $r_e = 2.817 \times 10^{-13}$ cm is the classical electron radius

- m_e is the electron mass
- $N_A = 6.022 \times 10^{23}$ mol^{-1} is the Avogadro's number
- I is the mean excitation energy
- Z is the atomic number of the medium
- A is the atomic weight of the medium
- ρ is the medium density
- z is the charge of the particle
- $\beta = u/c$
- $\gamma = (1\text{-}\beta^2)^{-1}$
- δ is the density correction
- C is the shell correction
- $W_{\max}$ is the maximum energy transfer on a single collision

The Bethe-Bloch formula provides a description of the energy loss for all charged particles with $0.1 < \beta\gamma < 1000$ except the electron and positron. If the charged particle is an electron or a positron, equation 3.28 must be modified since in this case the collisions occur between indistinguishable particles.

Figure 3.9 illustrates an example of the mean energy loss of pions in silicon. The energy loss reaches a minimum of around $\beta\gamma = 3.5$. This minimum varies according to the Z of the material. The particles in this kinematic range are called *Minimum Ionizing Particles* (MIP).

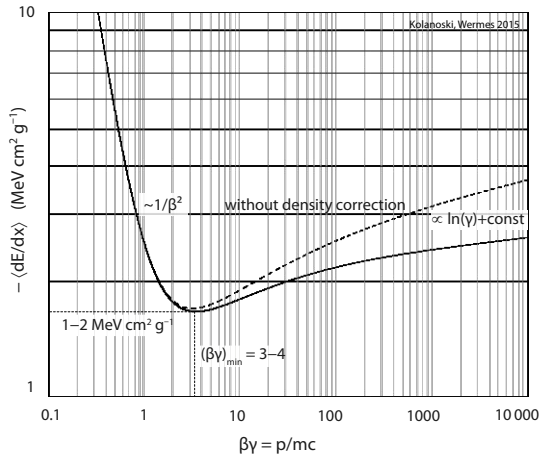


Fig. 3.9: Mean energy loss of charged pions in silicon as a function of $\beta\gamma$ [53].

After reaching a minimum, the energy loss shows an increase towards high energies (Fig. 3.9). This relativistic rise comes from the fact that the electric field of the ionizing particle in the lab frame is proportional to γ. The larger the momentum the particle has, the stronger the field becomes. Hence, the particle can ionize atoms at larger distances and as a consequence, lose more energy. The energy loss follows a logarithmic rise. In fact, the logarithmic rise saturates at high

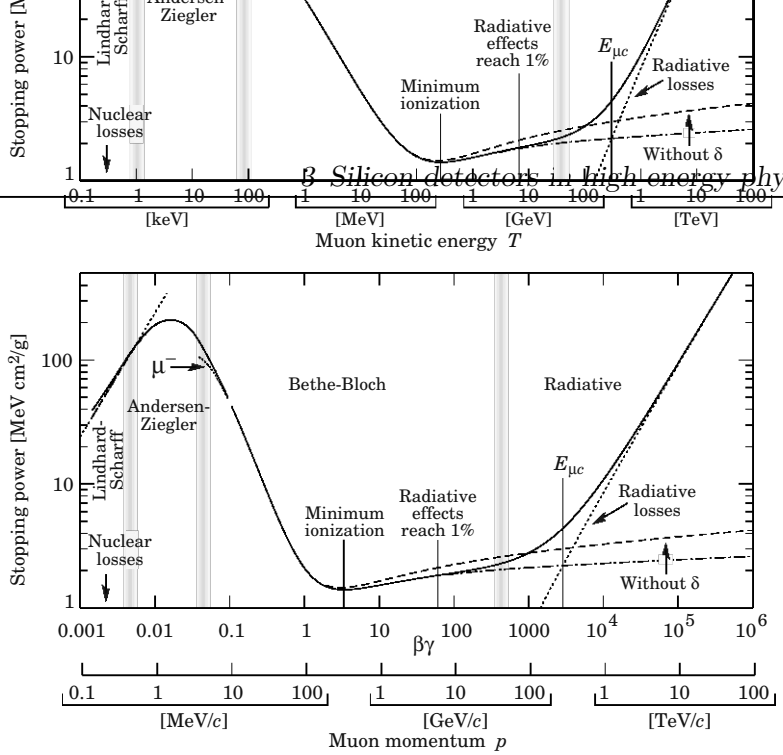


Figure 1: Stopping power ($= \langle -dE/dx \rangle$) for positive muons in copper as a function of momentum $p = M\beta c\gamma$ (bottom figure, 9 orders of magnitude). Solid curves indicate the total stopping power. Data below the break at $T \approx 0.5$ MeV are scaled by the appropriate mass ratios from the π^- and p tables in ICRU 49 [3], and data at higher energies are from the present calculations. Vertical bands indicate boundaries between different theoretical approximations or dominant physical processes. The short dotted links labeled "μ^-" illustrate the "Barkas effect" [8]. "Nuclear losses" indicates non-ionizing nuclear recoil energy losses, which are negligible here.

Fig. 3.10: Energy loss (stopping power) of positive muon in copper as a function of its momentum [54].

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energies due to the density correction δ. The density effect is associated with the polarisation of the medium which causes a screening effect of the nearby atoms influencing the electric field.

The high density of silicon ($\rho_{Si} = 2.33$ g/cm$^3_6$) leads to a mean energy loss for a MIP particle of about 390 eV per µm. To create an e-h pair inside the silicon volume a mean ionization energy of $E_{pair} = 3.6$ eV is required. For a density of 300 µm of silicon, the number of electron-hole pairs created due to the passage of a charged MIP is:

$$\frac{(dE/dx)_{\mathrm{MIP}} \cdot d}{E_{\mathrm{pair}}} = \frac{390 \cdot 300}{3.6} \frac{(\mathrm{eV/\mu m}) \cdot \mu\mathrm{m}}{\mathrm{eV}} = 32500 \quad \text{electron-hole pairs}$$

In fact, the number of collisions per unit of medium as well as the transferred energy per scattering are subjected to statistical fluctuations. The collisions with a small transferred energy are favored. However, there are also cases in which there is a large energy transferred from the so-called δ-electrons. The δ-electrons are produced in head-on collisions of the incoming particle with the electrons of the atomic shells of the medium. They are highly energetic and can cause further ionization in the material. These electrons are responsible for the formation of the tail towards the high-charge depositions in the distribution of the energy transfer. This distribution is better described by the Landau theory. The Landau distribution is described by the Most Probable Value (MPV). An example is shown in Fig. 3.11.

3.2.1 Bremsstrahlung

In addition to energy loss due to ionization, charged particles lose energy through interactions with the Coulomb field of the nuclei of the traversed medium. Due to this interaction, the charged particles are decelerated and a part of their kinetic energy is emitted as photons. This is the so-called *Bremsstrahlung effect*. The energy loss due to Bremsstrahlung can be approximated as :

$$-\frac{dE}{dx} \simeq 4\alpha N_{\mathrm{A}} \frac{Z^2}{A} z^2 \left(\frac{1}{4\pi\epsilon_0} \cdot \frac{e^2}{mc^2} \right)^2 E \ln \frac{183}{Z^{1/3}} \tag{3.29}$$

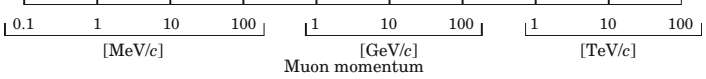

Fig. 1.14 Charged particles lose energy, when traversing material. The figure shows the stopping power $\langle dE/dX \rangle$ of copper for traversing muons [326]. Exactly this effect is the fundamental principle of all ionising detectors. The sensor design needs to make sure to detect the **M**inimum **I**onizing **P**article (MIP) with a maximum signal/noise (S/N) ratio. The plot includes the corrections to the Bethe formula at low and high energies, whose explanations are beyond the scope of this book

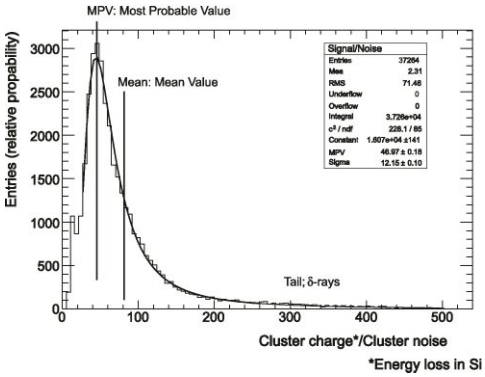

Fig. 1.15 A Landau distribution. The distribution displays the ratio of ionisation signal charge to noise in 500 µm silicon from cosmic particles (MIP) arriving at normal incidence in a 3.8 T field. The distribution shows a significant difference between Most Probable Value (MPV) and the mean, and the long-tail of the distribution from delta-rays is clearly visible [340]

Fig. 3.11: Distribution of signal detected by the passage of cosmic particles through a silicon bulk in a 3.8 T magnetic field. The difference between the mean value and the most probable value of the distribution is clearly shown [19].

where Z is the atomic number, A is the atomic weight of the medium, z is the charge number, m is the mass and E is the energy of the incident particle.

The energy loss due to Bremsstrahlung is proportional to the energy of the particle and inversely proportional to its mass. This makes clear why the Bremmstrahlung effect plays a very important role for electrons. In particular, equation 3.29 is modified as:

$$-\frac{dE}{dx} \simeq 4\alpha N_{\mathrm{A}} \frac{Z^2}{A} z^2 r_e^2 E \ln \frac{183}{Z^{1/3}} \tag{3.30}$$

One can define the radiation length X_0 as the characteristic length for the particle's energy loss through Bremsstrahlung as:

$$\left(\frac{dE}{dx}\right)_{\mathrm{rad}} = -\frac{E}{X_0} \tag{3.31}$$

which gives:

$$E = E_0 \cdot \exp(-x/X_0) \tag{3.32}$$

Formula 3.32 states that radiation length is the distance in which the energy of an incoming particle is reduced by $1/e$ due to radiation effects. The radiation length is a property of the material and can be defined as:

$$X_0 = \frac{A}{4\alpha N_{\mathrm{A}} Z^2 r_e^2 \ln \frac{183}{Z^{1/3}}} \tag{3.33}$$

The radiation length X_0 of silicon is 9.36 cm [55]. The thickness of materials used in particle detectors are typically given in units of radiation length.

3.2.2 Total energy loss

Energy loss by ionization and by radiation depends in a different way on the particle energy E, the particle mass M and the nuclear charge Z of the medium. Ionization dominates at low

energies while energy loss due to Bremsstrahlung is dominant at very high energies. The two types of energy loss become equal at some critical energy E_c, such as:

$$\left(\frac{dE}{dx}\right)_{\text{ion}} = \left(\frac{dE}{dx}\right)_{\text{rad}} \tag{3.34}$$

An approximation for the critical energy in solids and liquids is [53]:

$$E_c \simeq \frac{610 \text{ MeV}}{Z + 1.24} \tag{3.35}$$

Figure 3.10 illustrates the energy loss of muon in copper as a function of its momentum. Bethe-Bloch formula describes the energy loss in the region where ionization dominates. Beyond the critical energy E_c^{μ} energy loss due to radiation dominates.

3.2.3 Multiple scattering

The interaction of a charged particle with the Coulomb potential of the nuclei and the electrons of the medium leads to deflections with very low deviations from its original path. When the charged particles are hadrons then a contribution from the strong interaction should be considered as well. The scattering angle of the particle after multiple interactions follows approximately a Gaussian distribution with a standard deviation :

$$\theta_{\text{plane}}^{\text{rms}} = \frac{136\text{MeV}}{\beta pc} z \frac{x}{X_0} \left(1 + 0.038 \ln(x/X_0)\right) \tag{3.36}$$

where θ_{plane} is the angle projected onto a plane perpendicular to the direction of motion of the incoming particle, p is the momentum, βc is the velocity and z is the charge of the scattered particle. The parameter x/X_0 is the thickness of the scattering medium measured in units of radiation length. It is evident that the effect of multiple scattering becomes more pronounced in a thicker medium.

3.3 Working principle of silicon sensors

The silicon sensors for high energy physics experiments exploit the properties of a p-n junction operated in reverse bias mode. The formation of a region fully depleted of charge carriers is essential for the detection of a particle crossing the sensor volume. An undoped silicon could not act as a particle detector. A sensor made of intrinsic silicon would feature about 10^9 free charge carriers at room temperature while only 10^4 e-h pairs are created from the interaction of a charged particle with the silicon medium.

The good position resolution of the silicon sensors makes them ideal candidates for position-sensitive devices. However, a simple diode without any structured electrode would give no information about the position of the traversing particle. To provide track information, a segmentation of the readout electrode into fine structures is necessary. The readout electrode is typically segmented into a pattern of micro strips or pixels.

As an example a n-on-p AC-coupled silicon sensor is illustrated in Fig. 3.12. A heavily doped n-type electrode (n^+) segmented into micro strips, is implanted onto a p-type silicon bulk. Many parallel p-n junctions are created. The high voltage is applied to the backside while the strips are grounded. The depletion region starts growing from the strips to the backside until the full

volume is depleted. The electron-hole pairs which are generated by the interaction of a crossing particle with the silicon volume drift towards the electrodes due to the external electric field.

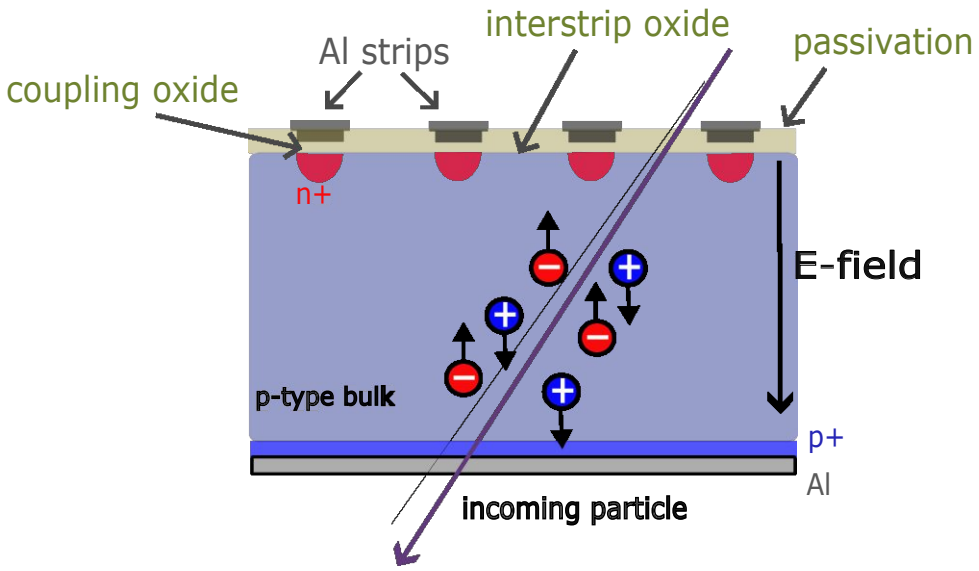

Fig. 3.12: A simplified sketch illustrating the working principle of a n-on-p silicon sensor.

Signal formation

The drift of the charge carriers inside the silicon bulk induces an electric current in each segment. This current or signal is detectable as soon as the charge starts to move and not only upon the arrival of the charge in the electrode. The induction mechanism was described and formulated by Schockley and Ramo [56], [57]. A movement of a charge q with a drift velocity $\vec{u}$ induces an instantaneous current i_i to an electrode i which is described by the formula

$$i_i(t) = q\vec{u} \cdot \vec{E}_w \tag{3.37}$$

where $\vec{E}_w$ is the weighting field. The weighting field should be distinguished from the electric field which accelerates the charge. It is a measure of the electrostatic coupling between the sensing electrode and the moving charge. To obtain the weighting field one should calculate the weighting potential ϕ_w by setting a unit potential to the electrode i, zero potential to all the rest and solve the Poisson equation. It should be highlighted that the weighting field depends on the electrode geometry and not on the charge movement. Both electrons and holes induce signals of the same sign because they drift in opposite directions.

For a strip or pixel sensor, the weighting field $\vec{E}_w$ as well as the electric field $\vec{E}$ peak in the vicinity of the segmented electrodes. Considering that the drift velocity $\vec{u}$ is proportional to the electric field ($\vec{u} = \mu\vec{E}$), the induced current becomes larger and larger as the charge approaches the considered electrode. The signal ceases to exist at the time the charge is fully collected by the electrode. The weighting potential of a segmented electrode approaches zero towards the direction of the other electrode, as shown in Fig. 3.13.

The collected charge over a time interval (t_1, t_2) can be calculated by integrating the induced current as follows:

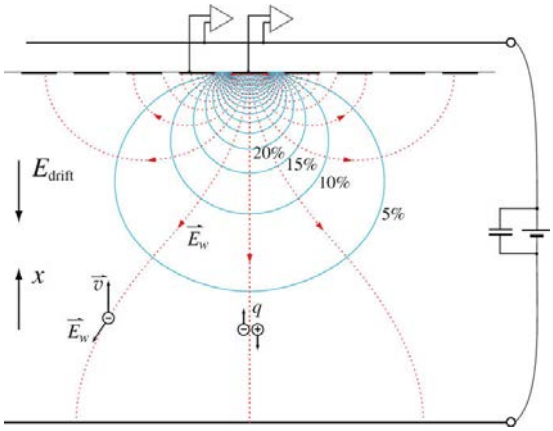

Fig. 3.13: Weighting potential (blue) and weighting field lines (dashed red) for a strip sensor. The sketch is taken from [58].

$$Q = \int_{t_1}^{t_2} i_i(t)dt = q\left[\phi_w(\vec{x}_1) - \phi_w(\vec{x}_2)\right] \tag{3.38}$$

Spatial resolution

In reality, the motion of the charge carriers inside the silicon volume is a combination of drift due to the applied electric field and thermal diffusion. The latter leads to a spreading of the charge cloud in the transverse direction. The transverse root mean square (RMS) of the charge cloud is given by:

$$\sigma = \sqrt{2Dt} \simeq \sqrt{2\frac{\kappa_B \mathrm{T}\mu_{\mathrm{e,h}}}{q}t} \tag{3.39}$$

Since σ is temperature dependent, the diffusion is suppressed for low temperatures. That is the case for the CMS silicon sensors during operation at $\mathrm{T} = -20°\mathrm{C}$, resulting in a diffusion below 1 µm [19].

The position resolution of the silicon sensor mainly depends on the strip (pixel) pitch as well as on the readout method. In the case of a binary readout, the only information is whether the collected charge in an individual electrode exceeds or not a certain threshold (hit or not hit). In a binary readout scheme, the position resolution depends exclusively on the strip (pixel) pitch. The variance of the estimated position of the particle is given as:

$$\sigma_x^2 = \frac{1}{p}\int_{-p/2}^{p/2} x^2 \cdot dx = \frac{p^2}{12} \tag{3.40}$$

where p is the electrode pitch.

An analog readout scheme allows for a hit position estimation with higher precision than the binary readout. It provides pulse height information, a signal which is proportional to the collected charge. For a cluster of hits, interpolation algorithms are used. One of these algorithms,

the so-called Center of Gravity algorithm (CoG), uses the weighted averaging of the neighboring strips or pixels. The hit position x_{CoG} can be estimated by:

$$x_{\mathrm{CoG}} = \frac{\sum_{i=0}^{n} x_i \cdot S_i}{\sum_{i=0}^{n} S_i} \tag{3.41}$$

where x_i is the position of the electrode i and S_i is the corresponding signal. A strip is assigned to a cluster of hits only if its signal exceeds a certain threshold. The threshold depends on the strip noise. The resolution of the analog readout is given by

$$\sigma_x = \frac{p}{\mathrm{SNR}} \tag{3.42}$$

where SNR is the signal-to-noise ratio.

Noise contributions

Signal-to-noise ratio (SNR) is the figure of merit for a silicon sensor operating as a tracking device. The noise should be minimized while the signal should be as large as possible. There are multiple sources of noise contribution in a silicon sensor. The noise is typically described as *Equivalent Noise Charge* (ENC) which refers to the number of electrons which contribute to the noise. It is defined as:

$$\mathrm{ENC} = \sqrt{\mathrm{ENC}_c^2 + \mathrm{ENC}_{I_\mathrm{L}}^2 + \mathrm{ENC}_{R_\mathrm{P}}^2 + \mathrm{ENC}_{R_\mathrm{S}}^2} \tag{3.43}$$

where ENC_c the noise from the load capacitance, $\mathrm{ENC}_{I_\mathrm{L}}$ is the noise from the leakage current, $\mathrm{ENC}_{R_\mathrm{P}}$ the noise from the parallel and $\mathrm{ENC}_{R_\mathrm{S}}$ the noise from the series resistance. The load capacitance is a network of capacitances, such as the interstrip, the coupling and the strip-to-backplane capacitance. The noise from the parallel resistance sources from the bias resistors and the serial noise from the metal strip resistance. More information on the definition of each noise contribution factor is given in [19].

3.4 Radiation damage

The interaction of particles with the silicon sensor medium is the key to their detection but it also induces damage in the volume of the detector. The radiation damage becomes more critical in high-energy physics experiments in which the silicon sensors are installed near the interaction point where the particle densities are large. The radiation-induced effects in the silicon bulk and in the oxide can deteriorate the behavior of the device or lead to permanent damage. Therefore, studying and understanding the main mechanisms of radiation damage in silicon is crucial. The radiation effects are divided into bulk and surface damage effects.

3.4.1 Bulk damage

Bulk damage refers to the damage created in the silicon volume by non-ionizing energy loss of incident particles, mainly hadrons. When a high-momentum particle crosses the silicon volume, it interacts with the nuclei of the crystal lattice and transfers a part of its momentum. If the transferred momentum is high enough, it can displace the atom which leaves behind a vacancy. Typically, an energy transfer of 25 eV is enough to initialize a displacement in silicon lattice [48]. The displaced atom is called *primary knock-on atom* (PKA) and will relocate to another

point of the lattice as an interstitial. The combination of an interstitial and a vacancy is called a *Frenkel pair*. Depending on the recoil energy, the displaced atom might be able to displace further atoms of the lattice, leading to a cluster of defects. All these radiation-induced defects create new energy levels in the bandgap, changing the properties of silicon.

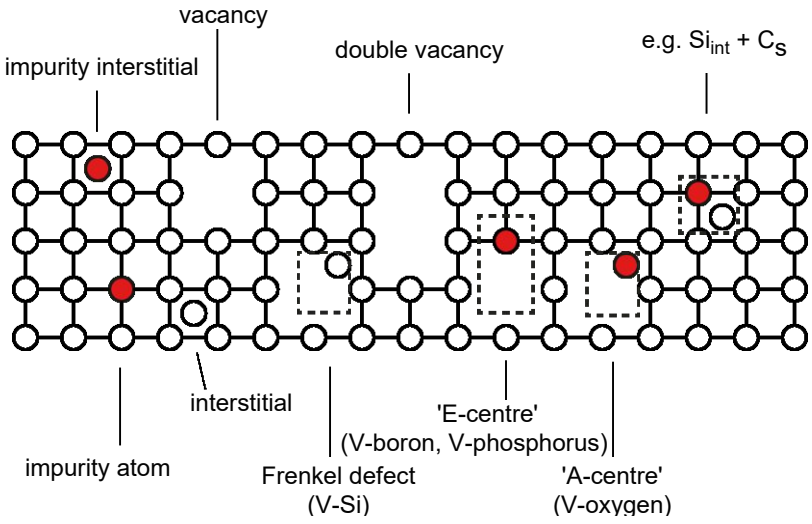

Fig. 8.79 Different defect types in a silicon lattice caused by particle radiation. The filled red circles are impurity atoms. Type complex defects are marked by the dashed rectangles. V marks a vacancy. Si_{int} is a lattice interstitial. C_S is a carbon atom substituting a lattice atom. Impurities can enter a crystal for instance during the crystal growth.

Fig. 3.14: Illustration of different types of radiation induced defects in the silicon bulk [53].

The charged hadrons, such as pions and protons interact predominantly via the Coulomb force with atomic nuclei. They create mostly point defects or clusters of defects in case of high energy transfers. On the other hand, the neutrons, since they are uncharged, interact with the nuclei only via nucleus-nucleus scattering. Thus, a great fraction of their energy is going into atomic displacement, initiating the formation of defect clusters. In fact, a neutron of 1 MeV can transfer about 60 keV to a silicon atom. Photons need larger energy than 250 keV to create displacement damage [48].

NIEL hypothesis

The Non-Ionizing Energy Loss (NIEL) hypothesis is a model that quantifies the bulk damage of different particles and energies under the assumption that the damage scales proportionally with the transferred energy. The energy-dependent damage cross section $D(E)$ of a particle traversing the silicon lattice is expressed as:

$$D(E) = \sum_i \sigma_i(E) \int_{E_d}^{E_R^{\max}} f_i(E, E_R) P(E_R) dE_R \tag{3.44}$$

where E, E_R are the energies of the impinging particle and the recoil atom, E_d is the minimum energy required to dislocate an atom, index i iterates over all occurring reactions with cross-section σ_i, $f_i(E, E_R)$ is the probability that in a reaction i a recoil atom with energy E_R is produced and $P(E_R)$ is a partition function which describes how much of the recoil energy is available for further displacement damage [53].

One can define the *Fluence* by introducing a so-called hardness factor k which scales the damage of different types of particles to the equivalent damage inflicted by a neutron of 1 MeV. The hardness factor is defined as:

$$k = \frac{\int D(E)\phi(E)dE}{D_{\text{neutron}}(1\text{ MeV})\int \phi(E)dE} \tag{3.45}$$

where $\phi(E)$ is the fluence of any kind of particle with energy E. It can be scaled to the fluence of 1 MeV by weighting the real fluence that a detector sees by the factor k, as follows:

$$\Phi_{\text{eq}} = k\Phi = k\int \phi(E)dE \tag{3.46}$$

where Φ is the irradiation fluence. The unit of Φ_{eq} is $\text{n}_{\text{eq}}/\text{cm}^2$ or $\text{n}_{1\text{ MeV}}/\text{cm}^2$.

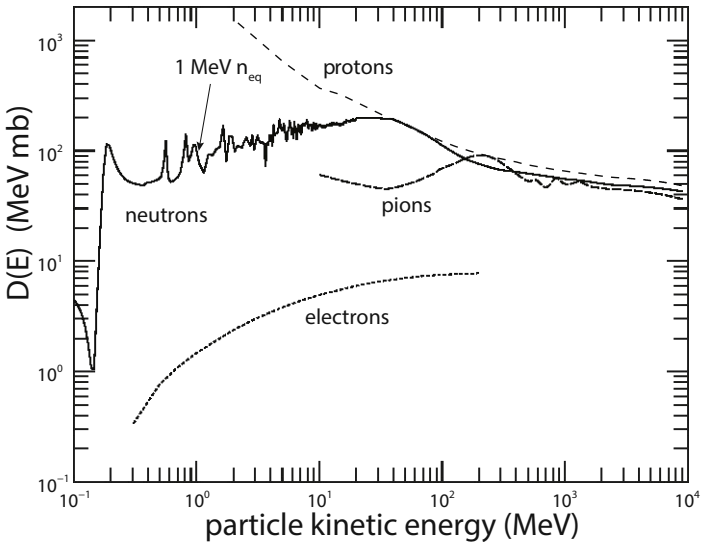

Fig. 8.82 Damage function $D(E)$ for atom dislocations in a Si-lattice for different particles: neutrons, protons, pions, electrons (after [660], with kind permission of Elsevier). The normalisation point for 1 MeV neutrons is marked by the arrow.

Fig. 3.15: Damage function $D(E)$ for atomic displacements in the silicon lattice over different particle energies for protons, neutrons, pions and electrons [33].

3.4.2 Impact of bulk damage on sensor properties

The microscopic defects generated in the silicon bulk due to displacement damage lead to macroscopic changes in the sensor behavior. Additional states in the bandgap are created due to damage in the crystal silicon lattice which can alter the properties of the sensor. The three main effects of the bulk damage are the increase in total dark current, the change in the doping concentration and the charge trapping.

Total leakage current

The defects generated near the middle of the bandgap act as generation-recombination centers. They lead to a decrease of the generation lifetime t_g which means a higher generation rate of electron-hole pairs. The transition of the generated pairs to the conduction or valence band is enhanced due to the shorter distance. This leads to an increase in the total dark current. In fact, the total leakage current increase is proportional to the applied fluence, according to the

current generation due to NIEL damage is constant (see page 349). It states that all lattice radiation damage in silicon linearly scales with the NIEL and can be traced back to the abundance of primary defects (point defects and clusters), irrespective of their initial distribution over energy and space, that is, whether they are homogeneously scattered over a large volume (typical for low-energy proton or gamma ray damage) or whether they are densely clustered in small regions (typical for neutron damage). Assuming the NIEL hypothesis, the observed differences in damage caused by neutrons, protons, pions and electrons can be scaled to each other using fig. 8.82 (*NIEL scaling*).

The damage effect of 1 MeV neutrons corresponds to $D_n(1\text{ MeV}) = 95\text{ MeV mb}$ [659] and is used as the normalisation point in fig. 8.82 for the damage caused by radiation from different particles at different energies. NIEL scaling means that the efficiency of a damage created by a different particle species at a different energy is described by the ratio κ of D_x for a radiation species x at an energy E to neutron damage D_n at 1 MeV:

$$\kappa = \frac{\int_{E_{min}}^{E_{max}} D_x(E)\phi(E)dE}{D_n(1\text{ MeV})\int_{E_{min}}^{E_{max}} \phi(E)dE}. \tag{8.100}$$

κ is often called *hardness factor* or *damage factor* [713]. As an example, for 24 GeV protons a value of $\kappa \approx 0.62$, for 25 MeV protons $\kappa \approx 2.0$ is used [352]. The *equivalent fluence* for 1 MeV neutrons then is the damage-weighted real fluence that a detector has received from a given particle species at a certain energy:

$$\phi_{eq} = \kappa\,\phi\,. \tag{8.101}$$

Typical (kinetic) energies of the particles mainly causing bulk damage at the inner zones ($r < 20$ cm) of the LHC experiments are 0.6–1 GeV for protons and 10 MeV for neutrons.

NIEL hypothesis. The increase of leakage current ΔI normalized to the sensor volume V can be written as:

$$\frac{\Delta I}{V} = \alpha \Phi_{eq} \tag{3.47}$$

where a is the current-related damage rate.

As discussed in section 3.3, the electronic noise increases with the total leakage current. Also, the temperature of the detector increases with the current which in turn creates more thermally generated current. This chain reaction can lead to the *thermal runaway* effect which can be destructive for the efficient operation of a silicon detector.

Doping concentration

The silicon bulk contains dopants such as phosphorus or boron which due to radiation damage can be captured into new defect complexes. The new complexes could contribute with a charge sign different from the original dopants. For instance, phosphorus can capture a moving single vacancy, result in a vacancy–phosphorus complex and change its charge sign from positive to neutral. Moreover, complexes with other impurities such as oxygen and carbon can be formed. The sign of the charge depends on their position with respect to the Fermi level [59]. Acceptors are mainly induced by irradiation into the bulk lattice while donors are removed. Therefore, for a p-type bulk, the effective doping concentration N_{eff} increases with irradiation and the bulk becomes more p-doped. This results in an increase of the full depletion voltage. In contrast, for a n-type bulk, the effective doping concentration decreases due to donor removal until the number of acceptors overcomes the number of donors. At this point, the n-type bulk turns into a p-type bulk. This effect is called *type inversion* and it is illustrated in Fig. 3.16.

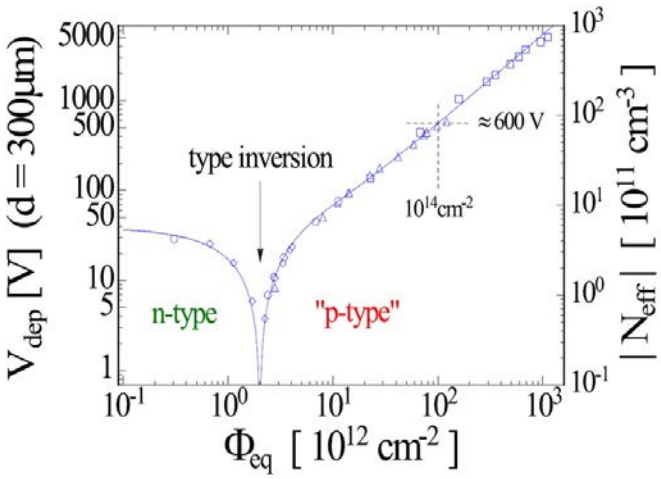

Fig. 3.16: Fluence dependence of the effective doping and of the full depletion voltage for an n-type silicon. The effect of type inversion is clearly illustrated in this plot [55].

Regarding the operation of a silicon sensor in a high radiation environment, such as the CMS detector, the type inversion can be well-exploited if n-type silicon technology is used. The full depletion voltage decreases up to a certain fluence at which the type inversion occurs. Therefore very low operation voltage is required. After type inversion, the full depletion voltage and the effective doping concentration start to increase again.

Charge trapping

The radiation-induced defects are responsible for the generation of trapping centers in the silicon bulk. These traps are unoccupied states in the depleted region and can hold or trap part of the signal charge for a time longer than the collection time. Therefore, this results in a reduction of the signal height. A parameter which refers to the effect of trapping is the trapping time τ_t which is inversely proportional to the fluence:

$$\frac{1}{\tau_t(\Phi)} = \frac{1}{\tau_t(\Phi = 0)} + \gamma\Phi \tag{3.48}$$

where γ is a coefficient related to the irradiation. The trapping effect due to radiation damage becomes more pronounced on p-on-n sensors than n-on-p sensors because the former collect holes. The mobility of holes is lower than the mobility of electrons, hence the probability of getting trapped increases. Nonetheless, the trapping effect becomes critical also for the n-on-p silicon sensors of 300 µm thickness for fluence beyond 10^{15} n_{eq}/cm^2 [55].

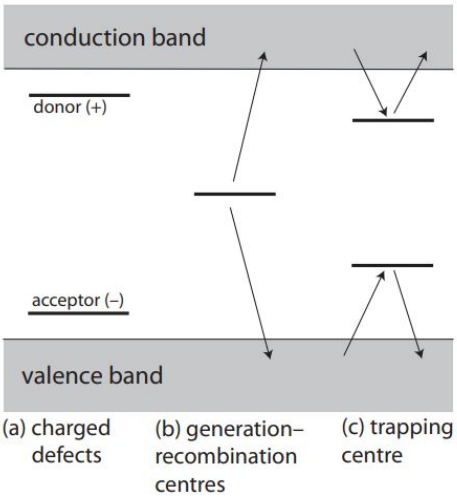

Fig. 3.17: Different location levels of radiation-induced defects in the bandgap. Donors in the upper half and acceptors in the lower half contribute to the effective doping concentration (a). Mid-gap levels are mainly contributing to the leakage current (b). Trapping centers decrease the signal and reduce the charge collection efficiency (c). Plot taken from [53].

3.4.3 Annealing

The radiation-induced defects in the crystal lattice such as the interstitials and the vacancies become mobile with temperature. During their displacement in the lattice, they can meet and recombine or form other types of combinations. The whole process is called *annealing*. Defects such as Frenkel pairs tend to recombine with time, leading to a gradual decrease of the effect of radiation damage in the silicon bulk. This effect is called *beneficial annealing*. In contrast, mobile defects can combine into more complex defects which can degrade the macroscopic properties of the sensor. This is called *reverse annealing* and requires a longer time. In principle, the annealing is suppressed below 0°C.

The total dark current and in particular the current-related damage rate α decreases with annealing time. Thus, the annealing of the total dark current is only beneficial. An example can

be found in Fig. 3.18. The damage rate can be parametrized by an exponential and a logarithmic term [59]. Therefore, the annealing behavior can be described by:

$$\alpha = \alpha_0 + \alpha_1 \exp\frac{t}{\tau_I} - \beta \cdot \ln\frac{t}{t_0} \tag{3.49}$$

with $\alpha_0 = (\text{-}8.9 \pm 1.3) \cdot 10^{-17}$ A/cm + $(4.6 \pm 0.4) \cdot 10^{-14}$ A K/cm $\cdot \frac{1}{\mathrm{T}_\alpha}$ a fitted parameter dependent on the annealing temperature T_α, $\alpha_I = 1.25 \cdot 10^{-17}$ A/cm, t_0 arbitrarily set to 1 min. The parameter τ_I can be expressed as:

$$\frac{1}{\tau_I} = k_{0I} \cdot \exp\frac{E_\mathrm{g}}{k_B \mathrm{T}_\alpha} \tag{3.50}$$

which takes into consideration the annealing temperature T_α. The fit parameter $k_{0I} = 1.2^{+5.3}_{-1.0} \cdot 10^{13}$ s^{-1}. The values of all parameters are taken from Ref. [55].

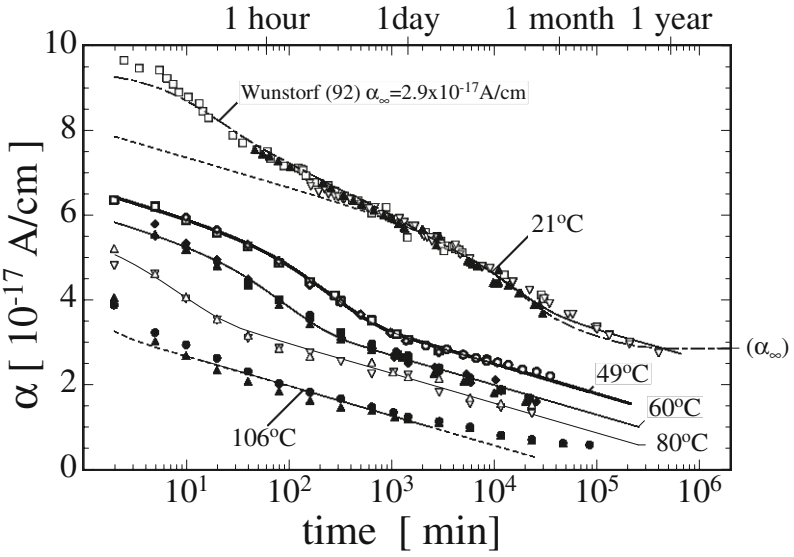

Fig. 3.18: Current-related damage rate α as a function of annealing time [55].

Annealing leads to a change in the effective doping concentration and in the full depletion voltage. The change in the effective doping concentration $\Delta\mathrm{N}_\mathrm{eff}$ can be parametrized as:

$$\Delta N_\mathrm{eff} = N_\mathrm{eff}^{\Phi=0} - [N_\mathrm{c}(\Phi) + N_\mathrm{a}(\Phi, \mathrm{T}_a, t) + N_\mathrm{Y}(\Phi, \mathrm{T}_a, t)] \tag{3.51}$$

where N_c is a term describing the stable damage which is independent of the annealing time and the temperature, N_a is a term describing the short-term or beneficial annealing and N_Y describes the reverse annealing. The term N_a describes the annealing of acceptors which leads to a decrease in the full depletion voltage in contrast to N_Y which describes the build-up of acceptors which leads to an increase of the effective doping concentration and the full depletion voltage.

3.4.4 Surface damage

Surface damage includes all the radiation-induced defects created in the SiO_2 dielectric layer as well as in the interface of the oxide with the silicon bulk. In general, the mechanism of damage

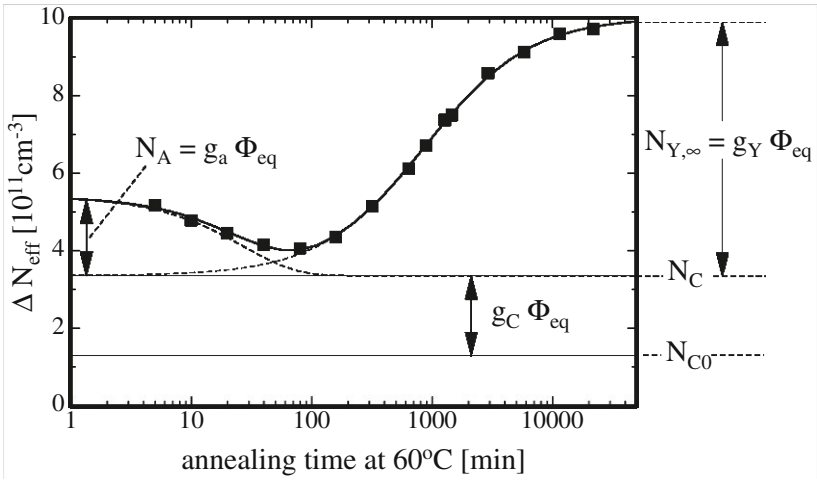

Fig. 3.19: change of effective doping concentration as a function of annealing time at T = 60°C after a fluence of $1.4 \cdot 10^{13}$ n_{eq}/cm^{-2} [55].

in the oxide is different than in the bulk due to the larger bandgap of the SiO_2 (8.8 eV) as well as due to the different lattice structure. Atomic displacements which is the major mechanism of radiation damage in the silicon bulk, have a minor effect on oxide. It is rather the damage from the ionizing radiation which plays a crucial role in the SiO_2.

Oxide damage is caused mostly by photons, X-rays and charged particles. The ionizing radiation creates electron-hole pairs in the oxide layer. The electrons have much larger mobility in the oxide than the holes ($\mu_{ox}^{n} \simeq 20$ $cm^2/V\,s$ while $\mu_{ox}^{p} \simeq 2 \times 10^{-5}$ $cm^2/V\,s$) which leads to a fast separation of electron-hole pairs. Assuming a positive voltage is applied on the metal, the electron drifts very fast toward the metal electrode while the holes move with a hopping mechanism via shallow levels to the Si-SiO_2 interface. If the holes arrive at the interface region, where many deep hole traps exist, they may be trapped there permanently. The hole traps are mainly oxygen vacancies which are created due to irregular lattice structure at the transition region between silicon and silicon dioxide [60]. The trapped charges form a *positive oxide-trap* charge at the interface. While holes hop through the interface or when they are trapped, hydrogen atoms are released in the oxide which drifts also towards the interface. These hydrogen atoms can react and form the so-called *interface traps* near the interface region. More information on the surface effects due to irradiation can be found in [61], [62].

The increase of the positive oxide charge has an influence on the electric field distribution in the silicon bulk close to the interface. It can favor the formation of an inversion layer between the strips or pixels for an n-on-p sensor and consequently deteriorate the interstrip isolation. Surface damage can be annealed at temperatures above 150°C [55]. The oxide annealing is explained by the drift and tunneling of bulk electrons into the interface region where they recombine with the trapped holes.

3.5 Manufacturing process

The production of silicon sensors for particle detectors uses the same basic processes as the production of commercial semiconductor devices. The production is based on the so-called *planar process* in which the development of a semiconductor device structure is done through a sequence of steps carried out near the surface plane of the silicon crystal. This process includes a sequence

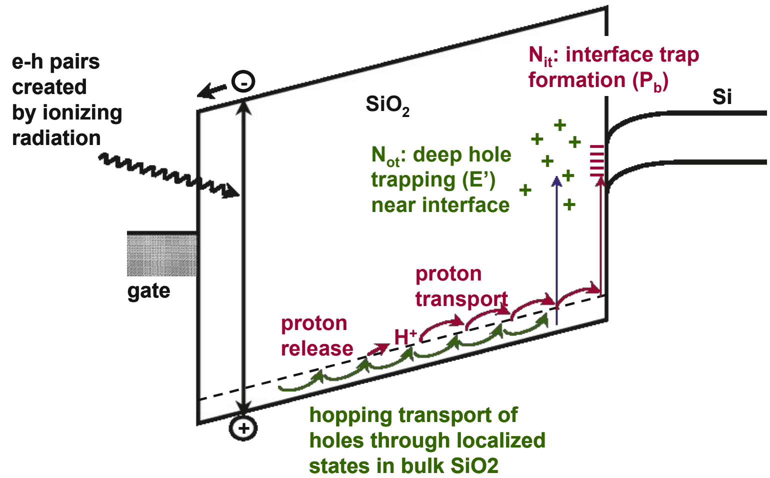

Figure 1: Band diagram of an MOS capacitor with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation.

Fig. 3.20: Band diagram of a MOS capacitor where a positive voltage is applied to the gate. The main radiation-induced defects are illustrated [60].

of oxidation, patterning and … this discussed in the following sub-sections. However, there are special requirements … processing … complexity. The size of … wafers must feature a high purity and the number of defects must be minimized.

The following paragraphs include a brief introduction to the crystal growth and manufacturing techniques for the production of a silicon sensor. A more detailed discussion … can be found in [63], [64].

3.5.1 Silicon crystal growth

Silicon exists on earth mostly as quartzite which is a form of pure sand (SiO_2). The material undergoes several purifying steps including melting in a furnace at high temperatures (above 1400 °C) and reacting at first level with carbon such as:

$$SiC\ (solid) + SiO_2\ (solid) \rightarrow Si\ (solid) + SiO\ (solid) + CO\ (gas)$$

At a second level, silicon is treated with hydrochloric acid (HCl) at 300°C:

$$Si\ (solid) + 3HCl\ (gas) \rightarrow SiHCl_3\ (gas) + H_2\ (gas)$$

The purified $SiHCl_3$ reacts then with hydrogen in order to produce a silicon of purity 99.9999999%:

$$SiHCl_3\ (gas) + H_2\ (gas) \rightarrow Si\ (solid) + 3HCl\ (gas)$$

The produced high-quality silicon is … (EGS). From this type of silicon, a single silicon crystal is … different processes … a single silicon crystal.

The Czochralski technique is the most commonly used method for crystal growth in the silicon fabrication industry. EGS is melted inside a quartz crucible at a temperature slightly higher than the melting point (1412°C). A single crystalline seed of known crystal orientation is dipped into the silicon melt. The seed is pulled slowly under rotation from the surface of the liquid. The silicon freezes out at the surface giving a single mono-crystalline ingot (Fig. 3.21). The diameter

where they may react to … interface traps. At thr… interface traps are predom… positively charged for p-c… transistors and negatively c… for n-channel transistors.

In addition to oxide-t… charge and interface-trap … buildup in gate oxides, … buildup will also occur in … oxides including field … silicon-on-insulator (SOI) … oxides, and alternate diel… The radiation-induced … buildup in these insulator… cause device degradation … circuit failure. Positive … trapping in the gate oxide can invert the channel interface causing leakage current to flow… OFF state condition (V_{GS} = 0 V). This will result in an increase in the static power supply … of an IC and may also cause IC failure. In a similar fashion, positive charge buildup in fie… SOI buried oxides can cause large increases in IC static power supply leakage current (cau… parasitic leakage paths in the transistor). In fact, for advanced ICs with very thin gate … radiation-induced charge buildup in field oxides and SOI buried oxides normally domina… radiation-induced degradation of ICs. Large concentrations of interface-trap charge can de… the mobility of carriers and increase the threshold voltage of n-channel MOS transistors. … effects will tend to decrease the drive of transistors, degrading timing parameters of an IC… this section, we present the details of oxide-trap and interface-trap charge buildup in … transistors.

B. Charge Yield

If an electric field exists across the oxide of an MOS transistor, once generated, el… in the conduction band and holes in the valence band will immediately begin to trans… opposite directions. Electrons are extremely mobile in silicon dioxide and are normally sw… of silicon dioxide in picoseconds [1,2]. However, even before the electrons can leave the… some fraction of the electrons will recombine with holes in the oxide valence band. T… referred to as initial recombination. The amount of initial recombination is highly depen… the electric field in the oxide and the energy and type of incident particle [3]. In general, st… ionizing particles form dense columns of charge where the recombination rate is relativel… On the other hand, weakly ionizing particles generate relatively isolated charge pairs, a… recombination rate is lower [3]. The dependence of initial recombination on the electri… strength in the oxide for low-energy protons, alpha particles, gamma rays (Co-60), and x… illustrated in Figure 2 [4,5]. Plotted in Figure 2 is the fraction of unrecombined holes (… yield) versus electric field in the oxide. The data for the Co-60 and 10-keV x-ray curve… taken from Ref. [5]. The other two curves were taken from Ref. [4]. For all particles, … electric field strength increases, the probability that a hole will recombine with an e… decreases, and the fraction of unrecombined holes increases. Taking into account the eff…

of the ingot can be adjusted by the ingot pull rate. The target impurity concentration is achieved by adding impurities to the melt in the form of heavily doped silicon. However, the grown silicon contains many undesired impurities, such as oxygen atoms which originate from the walls of the crucible. Therefore, this technique is not ideal for the production of high resistivity wafers of a few kΩcm [55].

An alternative method is the *Float Zone* (FZ) technique. A high-purity polysilicon rod is vertically contacted to a seed crystal which is both placed in a quartz envelope filled in with inert gas (Fig. 3.21). A small part of the crystal is melted by a radio-frequency (RF) heater which moves upwards along the rod. As the formed floating zone moves together with the RF heater, single-crystal silicon freezes to a single crystal at the orientation of the seed. The impurities are better solvable in the melt than in the crystal, therefore they are driven toward the end of the rod. Oxygen concentrations are very low because there is no crucible used in this process, unlike the Czochralski method. The Float Zone technique is preferred when the production of silicon wafers of higher resistivity is desired.

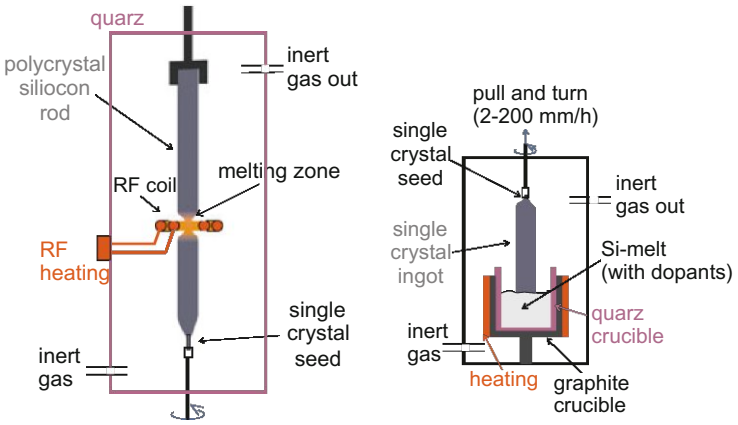

Fig. 3.21: Schematic illustration of the Czochralski technique (right) and the Float Zone technique (left) [19].

Fig. 1.50 The *left* picture shows the *F*loat-Zone method FZ, where a polycrystalline silicon cylinder from a mold with a single crystal seed on one edge is subjected to RF heating, melting the cylinder to form a single crystal or "*ingot*". The impurities have a higher solubility, therefore impurities diffuse to the boundaries further purifying the crystal. The *right* picture shows the **Cz**ochralski method CZ, where the single crystal "*ingot*" is directly drawn out of the melt using a single crystal as seed. The Czochralski method is most common globally, it additionally allows easy adding of dopants directly into the melt

The produced silicon ingot is then cut into thin discs, the so-called *wafers*. The cutting is typically performed with the use of a diamond blade. Before any further processing, the wafers are subjected to etching and polishing in order to remove any kind of imperfections, impurities or defects.

FZ ingots are doped by gas diffusion to achieve n- or p-type base materials. n-type can also be achieved by **N**eutron **T**ransmutation **D**oping NTD, where with $^{30}\mathrm{Si}+n \rightarrow {}^{31}\mathrm{Si} \rightarrow {}^{31}\mathrm{P}+\beta^-$ one achieves better uniformity.

The typical length of a single crystal ingot is 1 – 2 m. The ingots are normally not fully round and are then grinded to real cylinders, also a flat or a notch is applied to indicate the crystal orientation. Very early sensors have been produced on 2 in. diameter wafers while today 4 – 6 in. wafers are common and 8 in. wafers are candidates for some HL-LHC detectors – many examples in the next chapters. Today's electronic industry works mainly with 8 – 12 in.

For several years the FZ technique was superior to the CZ method with respect to purity (e.g. oxygen content) and was therefore the only possibility to achieve sensor grade silicon. Also high resistivity material was not available due to the lack of commercial applications. With a better purity and therefore a longer charge carrier lifetime it was also the preferred material for solar cells. Nowadays, the CZ also realizes sensor grade material and probably the high oxygen content makes it interesting for the HL-LHC project, see Sect. 7.1.1. On the other hand, since higher oxygen concentration seems to improve radiation tolerance, oxygen is often added to FZ in a later step by diffusion – DOFZ **D**iffusion **O**xygenated **FZ**.

The silicon ingot now needs to be cut into thin disks, called "wafers". The actual thickness is still not final but already below 1 mm. The cutting is achieved by a disk with a diamond blade or for multiply synchronous dicing a **M**ulti **W**ire **S**aw MWS,

3.5.2 Processing steps

The fabrication of a silicon sensor requires further processing steps which are identical to the typical manufacturing procedure of commercial micro-electronic devices. However, the sensors aimed for high-energy physics experiments should satisfy some special requirements which set extra challenges to the fabrication process.

3.5.2.1 Thermal Oxidation

A SiO_2 layer is grown at the surface of the silicon wafer through a thermal oxidation process. The wafer is inserted into a furnace at a temperature between 900 and 1200°C. The furnace is filled with oxygen, which reacts with the silicon and forms the oxide. In case dry oxygen is used, the technique is known as *dry oxidation*. In this case, the oxide grows very slowly forming uniform layers with high quality and few defects. If a H_2O steam is injected instead, then the process is

known as *wet oxidation* which is faster. However, the dry process shows better performance in terms of oxide breakdown stability, pinhole density and surface charges [55].

The formed oxide consumes around 44% of the thickness of the silicon on the surface [63]. The process slows down with increasing thickness of the oxide layer and is strongly temperature-dependent. The impurities inside the silicon become mobile at high temperatures. The dopant impurities near the silicon surface will be redistributed during the process. Special care is taken in order to validate that the properties of the device are not altered due to the introduction of impurities.

Typical thickness of the oxide is a few hundred nm. The SiO_2 layer is amorphous. This lack of internal structure leads to the formation of dangling bonds which are responsible for the presence of the fixed positive charges. These dangling bonds can be partially annealed. Heating the wafer in a hydrogen environment enables hydrogen to diffuse through the oxide towards the interface, thus leading to a bounding of the dangling bonds with the hydrogen atoms. As a consequence, the concentration of fixed positive charges decreases after this special heat treatment.

3.5.2.2 Deposition of thin films

Besides the silicon dioxide, other materials such as silicon nitride, and polysilicon can be deposited onto the wafer. A very common technique for the deposition of such thin films is *Chemical Vapor Deposition* (CVD). A gas which features the chemical compounds needed for the production of the thin film is thermally decomposed. For instance, the polysilicon can be deposited by silane (SiH_4) pyrolysis at about 600°C. There are three commonly used deposition techniques: atmospheric-pressure CVD, low-pressure CVD (LPCVD) and plasma-enhanced chemical vapor deposition (PECVD) [63].

The deposition of metals such as aluminum can be done by evaporation or sputtering. Evaporation is usually done by heating in a tungsten boat while sputtering is typically done by bombarding an aluminum target with accelerated ions, atoms or electrons. The purity of the deposited metal layer is defined by the purity of the target. During this process, the so-called aluminum spikes can be created in the silicon bulk. Silicon atoms can diffuse into the aluminum leaving empty space which can be filled in by the metal. The presence of these metal spikes can deteriorate the high-voltage stability of the device. Spiking depends strongly on the crystal orientation [50]. Countermeasures to reduce the impact of spiking can be taken. For instance, a small amount of silicon can be added to the aluminum which prevents the diffusion of silicon atoms into the metal. Also, the introduction of a thin layer of barrier metal between the aluminum and the silicon substrate is another method [63].

3.5.2.3 Photolithography

The structuring of the wafer surface is done via the photolithography technique. The wafer is mounted on a rotating chuck and a photosensitive liquid is dropped on the center of the wafer. Due to the rotation of the chuck, the photoresist is distributed homogeneously over the wafer. When the liquid is dry, the layer is exposed to UV light while a mask is either placed on top of the photoresist or at a well-defined distance from the wafer (typically around 10 - 20 µm [50]). The exposure of the photoresist to light transfers the pattern of the mask to the wafer. There are two types of photoresist: the positive and the negative. For positive photoresist, the exposed regions become more soluble and the patterns formed in the positive resist are the same as the patterns on the mask. For negative photoresists, the exposed regions become less soluble, and the patterns formed in the negative resist are the reverse of the mask patterns. The mask

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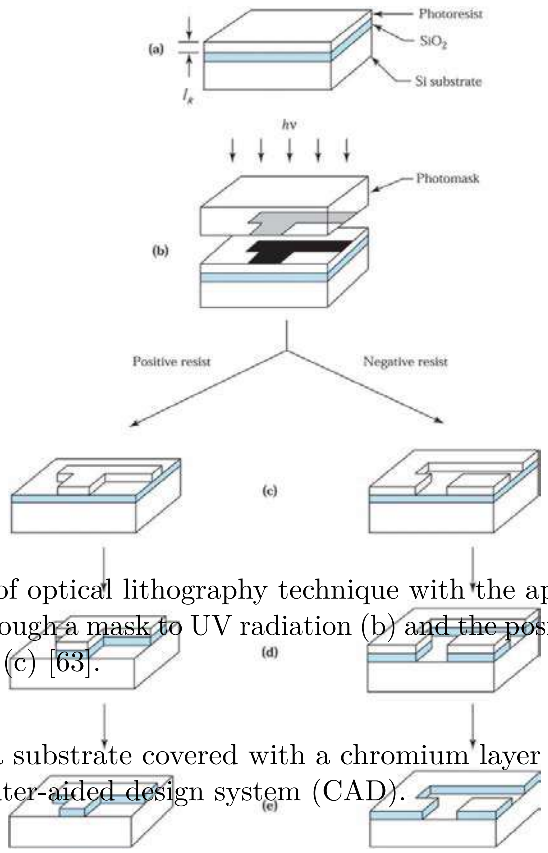


Fig. 9 Details of the optical lithographic pattern transfer process.[8] (a) Application of resist. (b) Resist exposure through the mask. (c) Development of resist. (d) Etching of SiO_2. (e) Removal of resist.

Fig. 3.22: Illustration of optical lithography technique with the application of a resist (a), the exposure through a mask to UV radiation (b) and the positive or negative development of the resist (c) [63].

consists of a fused silica substrate covered with a chromium layer and the pattern is designed with the use of a computer-aided design system (CAD).

3.5.2.4 Etching

After the illumination process, all the parts of the oxide which are not covered by the photoresist are removed by etching. This process includes the use of an etchant and is divided into two different types: wet and dry etching.

Wet etching uses liquid etchants and involves multiple chemical reactions that consume the original reactants and produce new reactants. The wet etching process is described in three steps: the diffusion of the liquid etchant to the structure that is to be removed, the reaction between the liquid etchant and the material being etched away and the products from the surface are removed by diffusion. Wet etching shows high selectivity which is a parameter describing to what extent the process removes only the material desired and stops at other materials [55]. Wet etching is typically used in wafer processing for particle detectors [50].

Dry etching uses different techniques to remove the substrate material such as plasma etching or ion beam etching. In dry etching, the surfaces are removed via bombardment of vapor or gas, chemically through a reaction between the reactive species and the surface, or the combination of both physical and chemical reactions. Dry etching is a common method in microelectronics since it provides a high degree of anisotropy and allows for small structures.

3.5.2.5 Doping

The creation of a p-n junction requires the introduction of additional dopants on the wafer. The strips/pixels, the backplane, the edge and the guard ring are heavily doped implants, exceeding by orders of magnitude the doping concentration of the bulk. Boron is typically used as a p-type dopant and Arsenic or Phosphorus as an n-type dopant. For the introduction of the dopants, two are the most common methods in the semiconductor industry: diffusion and ion implantation.

For doping by *diffusion* technique, the wafer is inserted into a furnace and exposed to a gas at a temperature of 800 - 1200°C. The dopants are either added directly as a gas or are directed to the gas through a bubbler which contains a liquid form of the dopant [55]. The doping concentration depends on the applied temperature and the time of the exposure.

In the *ion implantation* method, doping atoms are ionized, accelerated and directed into the silicon wafer. It is performed at room temperature which allows the use of a photoresist to mask the areas that are not aimed to be doped. The penetration depth of the ions can be adjusted by selecting the energy of the ions. After the implantation step, the dopants need to be activated and annealed by a thermal treatment at high temperatures. This process can also heal crystal defects which are created during the ion bombardment. The ion implantation method is nowadays most commonly used due to the fact that it allows precise control of doping levels and depth. The dopant atoms are mostly located in interstitial positions after the implantation. This method requires a thermal treatment in controlled conditions to restore the position of the dopant atoms in the regular lattice sites.

3.5.2.6 Dicing

After the fabrication, the chips or structures which are developed on the wafer must be separated. This is accomplished by the *dicing process*. The dicing is a very crucial step since the individual components or dies should be cut from the wafer with high precision without damage introduced during the cutting process. There are three common wafer dicing techniques: blade, laser and plasma dicing.

Blade dicing

Blade dicing uses a high-speed rotating diamond blade to cut through the wafer and separate the individual dies. The blade is mounted on a dicing saw which controls the position and the depth of the cut and ensures high precision. The blade dicing technique is very commonly used in the semiconductor industry, it is compatible with a wide range of materials such as silicon, and germanium and has low cost. The limitations of this technique become more evident when very small structures and thinner wafers need to be diced. Mechanical stress is generated while the blade cuts through the wafer which can lead to cracking or deformations of the delicate and small structures. In addition, the width of the kerf which is the material removed by the cutting process, can be large. This means that a significant amount of material is wasted. Nevertheless, recent developments in dicing blades with ultra-thin profiles have led to a reduction of kerf width and the mechanical stress applied during the cutting. Typically, the dicing saw is equipped with a cooling system which uses a coolant to dissipate the heat from the cutting area. This heat is produced due to the friction generated during the cutting process and can create thermal damage to the wafer.

Laser dicing

Laser dicing uses a focused laser beam to separate the structures from their wafer. One main advantage of this technique in comparison to blade dicing is that it is not a mechanical process. Thus, the problems caused by the mechanical stress and the vibrations do not concern this method. The laser dicing is subdivided into two techniques: *ablation* and *stealth dicing*.

Ablation dicing is based on the ablation process which refers to the removal or vaporization of a part of a material after focusing a laser beam on its surface for a short amount of time. Due to the intense and localized heating of the material from the laser beam, the use of cooling is required in order to mitigate any thermal effects on the die.

Stealth dicing uses a laser beam with a wavelength that is semitransparent to the wafer material [65]. The laser beam is focused inside the wafer material on specific points. This is the main difference to the ablation dicing in which the beam is focused on the surface of the material. Along the scanned line, the so-called *Stealth Dicing* (SD), layers are created. A series of cracks is formed internally as a result of the deposited … of … a tape. The next step is the expansion process … which creates a tensile stress to the internal cracks of t… beam. The cracks extend to the top and the bottom s… An illustration of the stealth dicing process is given in Fig. … ical stress applied to the wafer, essentially no kerf … no friction or debris.

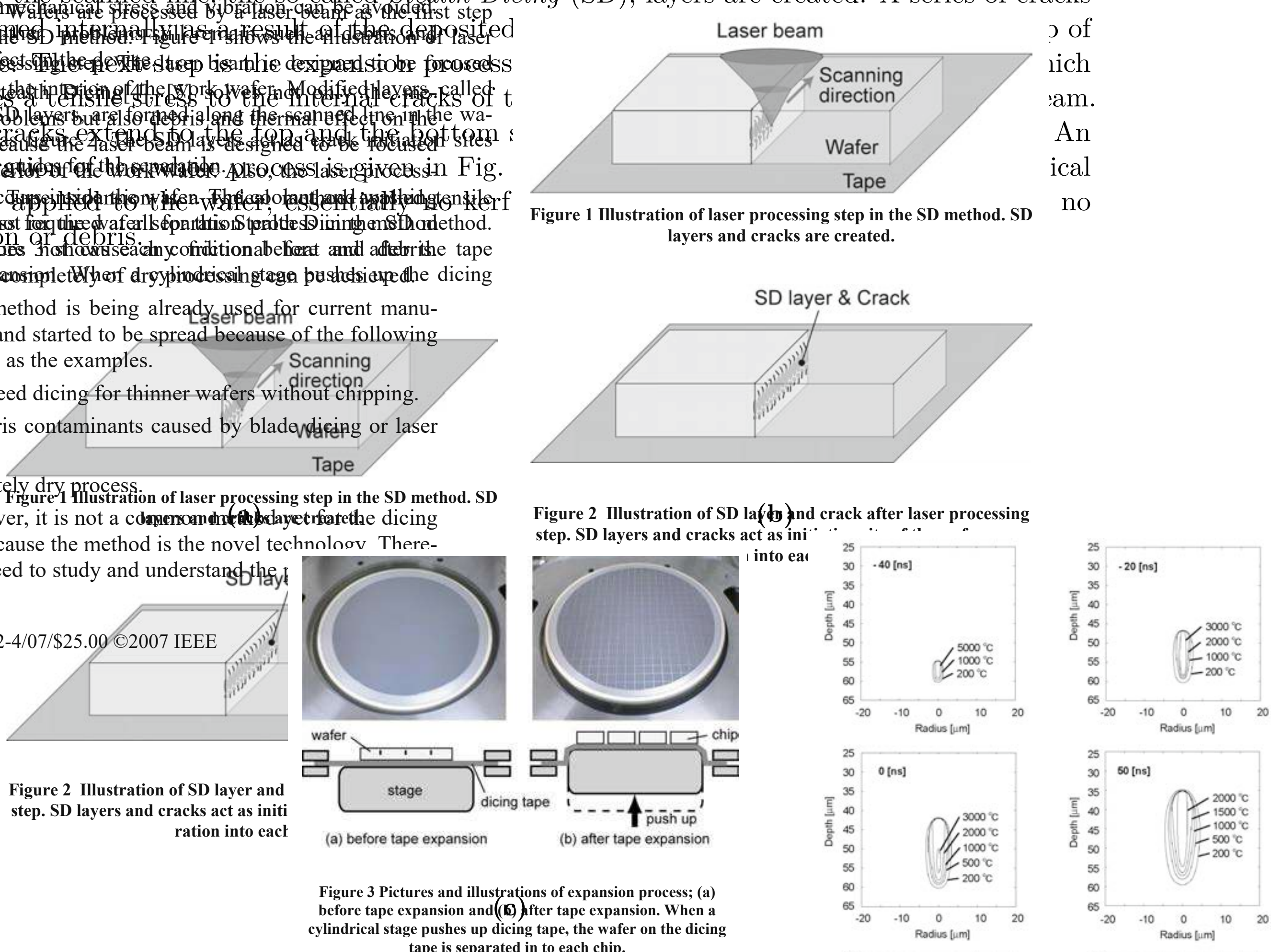


Fig. 3.23: Illustration of stealth dicing process. A laser beam is internally focused (a) and creates the Stealth Dicing layers and the cracks (b). With the tape expansion process, the wafer is separated into each die (c). Pictures are taken from [65].

Plasma dicing

Plasma dicing is also known as plasma etching or Deep Reactive Ion Etching (DRIE). This process etches narrow and deep trenches (dicing streets) into the wafer using a plasma gas such as Sulphur hexafluoride (SF_6). The etching is performed simultaneously across the whole wafer. Two standard methods are used: Dice Before Grind (DBG) and Dice Post Grind (DPG) [66].

In the DBG approach, the etching happens first on the front side where the dies are defined. After that, the wafer is inverted and attached to a dicing frame (Fig. 3.24). A grinding process thins out the wafer from the backside until the dies have been separated.

In the DPG approach, the wafer is thinned out first and then the wafer is attached to the dicing frame (Fig. 3.25). The dies are separated by etching through the full wafer thickness up to tape. Special care must be taken to prevent damage to the silicon at the interface between the wafer and the tape. The etching continues until the tape is exposed. Electrical charges can

Substrates

The major difference between conventional plasma etching and dicing is the substrate. For dicing before grinding (DBG) [2], the substrate is standard. But, for conventional dicing (or dicing post grinding, DPG), the wafers are thinned and mounted on a tape tightly suspended from a metallic or plastic frame. These approaches are described in the images below.

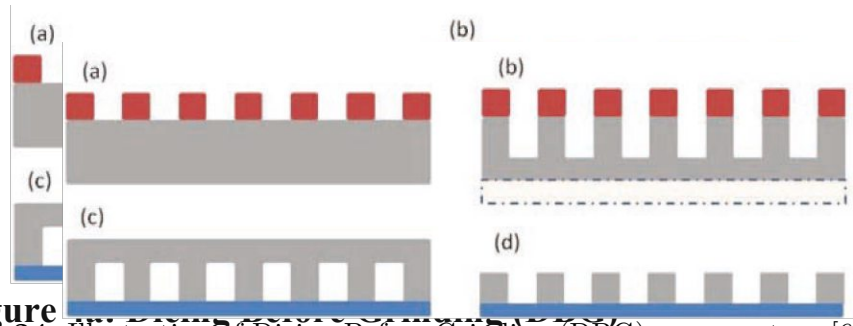


Fig. 3.24: Illustration of Dicing Before Grinding (DBG) process steps [66].

Figure 4a: Dicing Before Grinding (DBG)

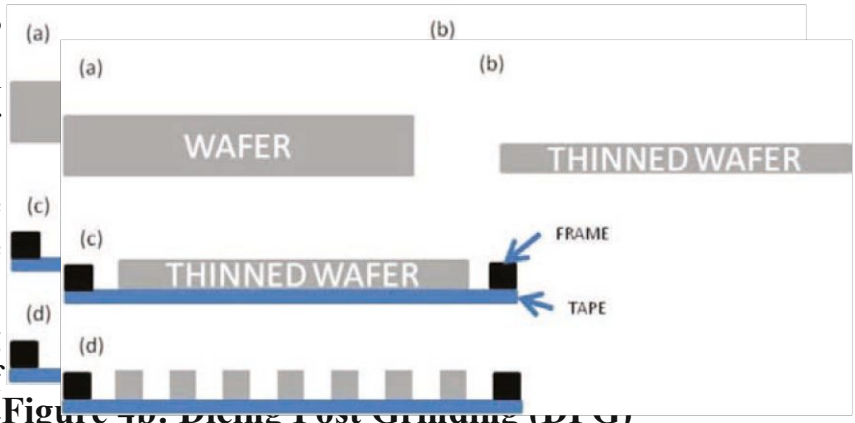


Fig. 3.25: Illustration of Dicing Post Grinding (DPG) process steps [66].

Figure 4b: Dicing Post Grinding (DPG)

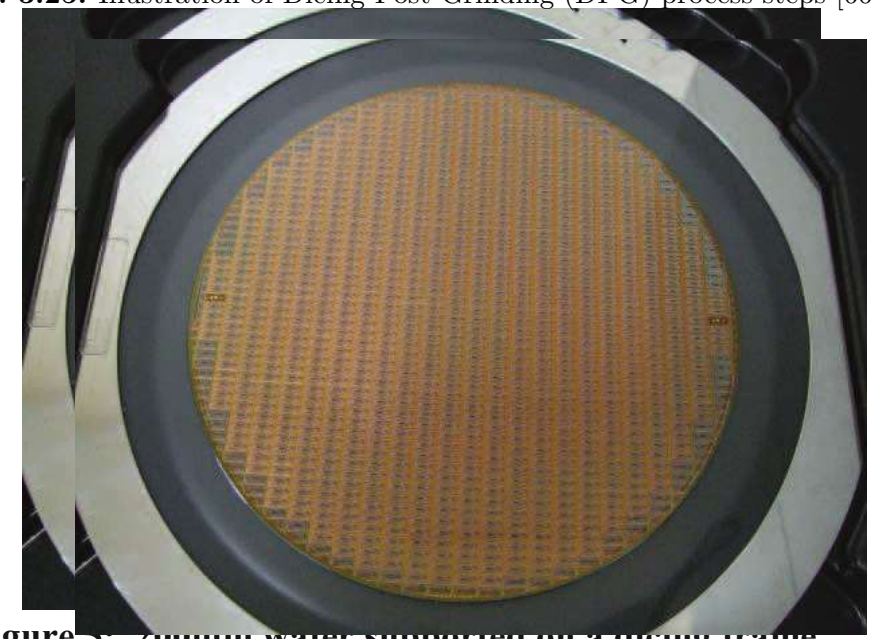


Figure 5: 200mm wafer supported on a dicing frame

The frame is one element that needs accounting for since the substrate size is no longer the diameter of the wafer, but the diameter of the frame. Typically the outer diameter of the

Chapter 4

Outer Tracker silicon sensors

The silicon sensors which will instrument the Phase-2 Outer Tracker modules must satisfy certain conditions dictated by the environment of HL-LHC and the CMS physics program. The Outer Tracker sensors will operate over a minimum of 10 years without any replacement, thus radiation hardness is a critical property they should have. CMS conducted a program that started in 2010, examining different options with regard to wafer material, substrate type, thickness, geometry and many other sensor-related properties, until the current baseline was established. Some of the most important features of the Phase-2 Outer Tracker sensor design are discussed in the following sections.

4.1 Sensor type, material and thickness

The current CMS strip detector comprises p-on-n silicon sensors (p^+ strips on n-type bulk). Sensors with n-type bulk exhibit a decrease in effective doping concentration and full depletion voltage as a function of fluence up to type inversion. In order to delay the type inversion, CMS chose material of lower resistivity which results in high initial full depletion voltage. As a consequence, the full depletion voltage of the inverted bulk is roughly the same as the initial full depletion voltage after 10 years of LHC operation [19].

Regarding the substrate type selection for the Phase-2 Outer Tracker sensors, both n-on-p and p-on-n options were examined by CMS. The studies included sensors of 200 µm and 300 µm thickness produced with the Float Zone technique which were irradiated up to the maximum expected fluence delivered by HL-LHC (Fig 4.1). The sensors were biased at 600 V during the charge collection measurements while an annealing procedure after each irradiation was performed [67]. Figure 4.2 shows the seed signal of 300 µm thick p-on-n and n-on-p sensors. The seed signal is defined as the highest strip signal within a cluster of hits and is the parameter of interest due to the binary readout of Outer Tracker modules. The seed signal of the p-on-n sensor exhibits a faster decrease than the seed signal of the n-on-p. The trapping effect becomes dominant at high fluence and since a p-on-n sensor collects holes which feature lower mobility than electrons, the probability of signal loss due to trapping increases. Comparing the two candidates with an active thickness of 200 µm (Fig. 4.3), the seed signals show a similar behavior as a function of fluence. Due to lower active thickness, the electric field strength is high enough to ensure a high collection efficiency and mitigation of the trapping effect. Here the picture changed significantly when the noise was compared [67]. As illustrated in Fig. 4.4, beyond a proton fluence of 3×10^{14} n_{eq}/cm^2, p-on-n sensors exhibit strong non-Gaussian tails adding up to the noise distribution. This can result in fake hits during detector operation and an increase in occupancy. Simulations performed by CMS collaboration verify the presence of high fields at the p^+ strips. The thermally generated charge carriers could be accelerated under the presence of these high electric fields, trigger the avalanche multiplication effect and generate random signals. This is not observed on n-on-p sensors, where the fields are more distributed due to the presence of p-stop.

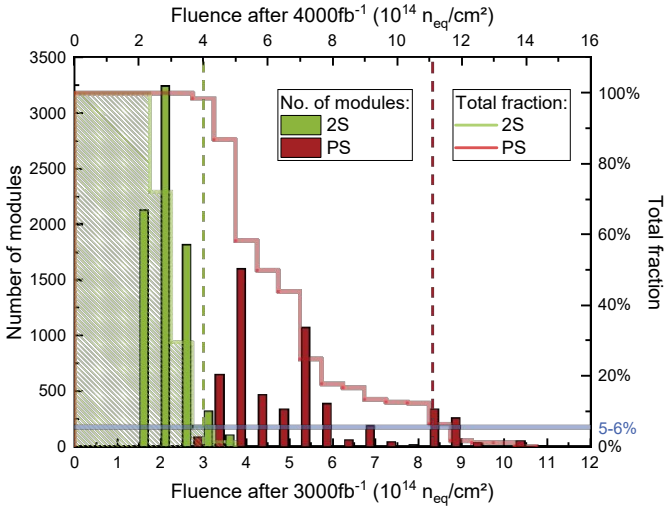


Fig. 4.1: Distribution of the total fluence the modules will have received after the end of HL-LHC lifetime considering their different locations in the Outer Tracker. The lower x-axis indicates the total fluence after 3000 fb^{-1} and the upper x-axis after 4000 fb^{-1}. A second histogram is overlaid showing the fraction of modules for each type with an accumulated fluence which exceeds the corresponding fluence of each bin. The dashed lines indicate the maximum fluences for about 95% of modules in the 2S and PS region [68].

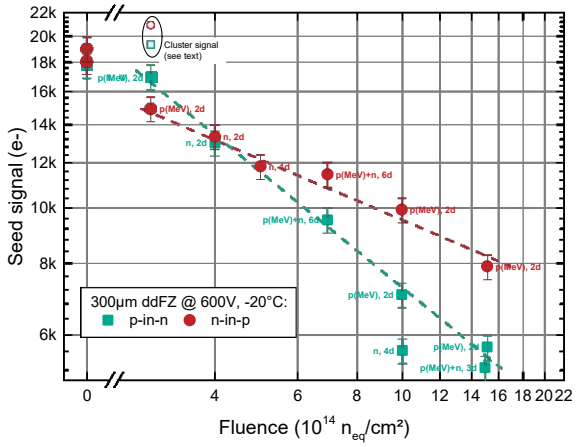


Fig. 4.2: Seed signal measurement of 300 µm thick sensors with different substrate types as a function of the fluence. The measurements were performed at T = −20°C with the sensors biased at V_{bias} = 600 V [67].

Similar to the silicon sensors of the current tracker, the Phase-2 wafers are manufactured with the Float-Zone technique. An alternative process which was considered is the magnetic Czochralski (mCz) technique which offers wafers of high radiation resistance due to the higher oxygen concentration [69]. Sensors produced by these two techniques were irradiated and their performance in terms of charge collection and electrical parameters was compared [70]. Both candidates are suitable choices. Mass production of high-resistivity wafers with the mCz technique could not be easily available in that time, hence the Float-Zone base material was the final selection.

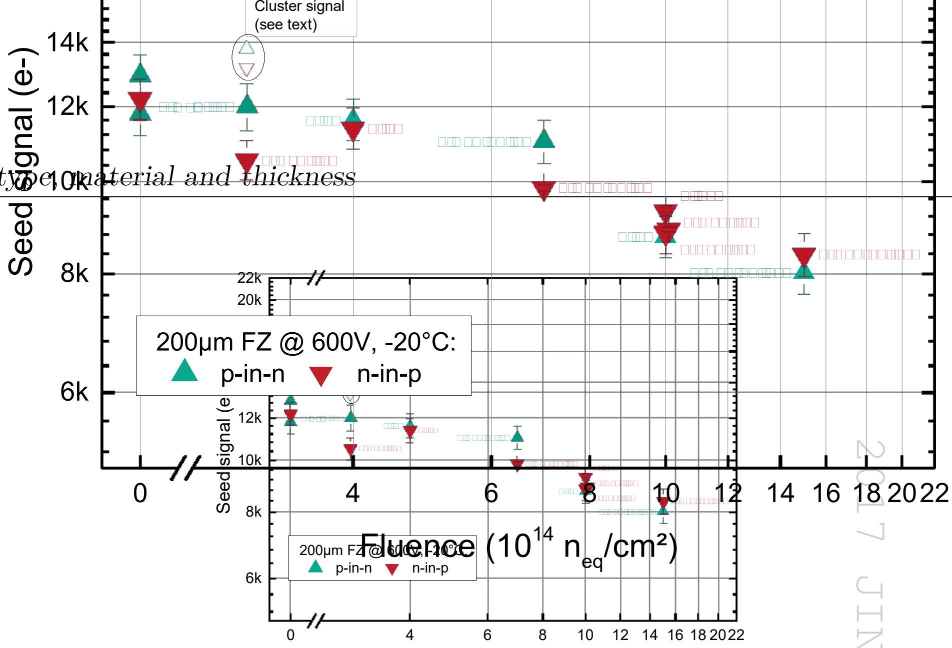


Figure 9. Charge collected on the seed strip for sensors with a nominal active thickness of 200 µm after a short annealing time of between 0 and 15 days at room temperature. The error bars reflect an estimated uncertainty of about 5% representing statistical and gain uncertainties. The text next to the symbols indicates the irradiation type (**p** stands for protons with energy range MeV/GeV and **n** for neutrons) and the equivalent annealing time at 21°C.

Fig. 4.3: Seed signal of 200 µm thick sensors with different substrate types as a function of the fluence. The measurement was performed at T = −20°C with the sensors biased at V_{bias} = 600 V [67].

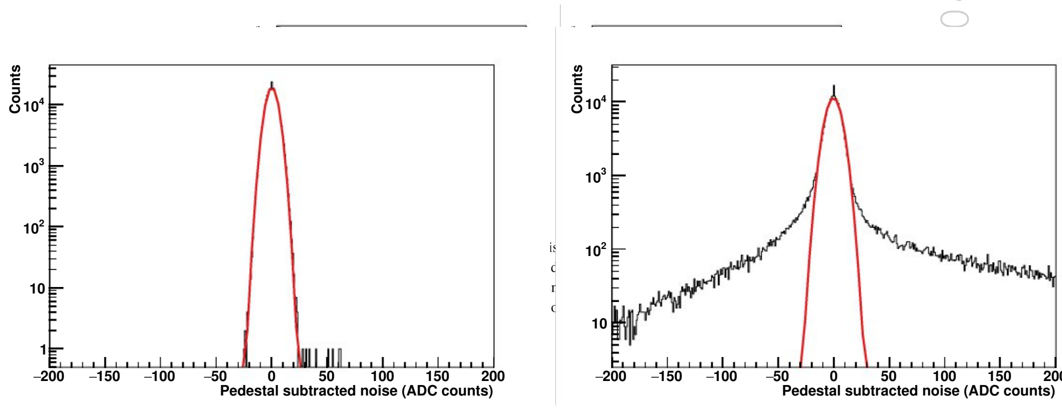


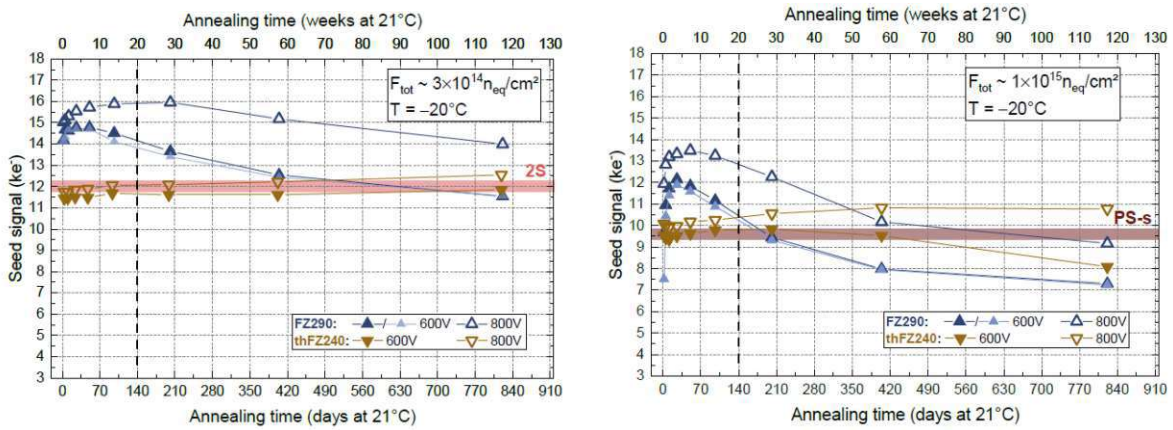
Figure 10. Two examples of pedestal-subtracted noise distributions as measured with the ALiBaVa system and fitted by a Gaussian distribution: a normal noise distribution (left) as observed on p-in-n type FZ sensors before irradiation, which looks similar for n-in-p sensors (both non-irradiated and irradiated), and a noise distribution affected by the non-Gaussian component observed for irradiated p-in-n FZ sensors with a nominal active thickness of 200 µm (right).

Fig. 4.4: Example of noise distribution of 200 µm thick p-on-n sensors before (left) and after irradiation (right). The n-on-p sensors of the same thickness show similar behavior to the plot on the left, before and also after irradiation [67].

Different options concerning the active thickness of the sensors were also investigated. A favorable candidate was thinner sensors with an active thickness below 300 µm. The advantage of thin sensors over thicker sensors is that, in principle, they should have lower bulk current, higher collection efficiency after irradiation due to the formation of high electric field strength around the electrodes and less material. The final selection was made between an active thickness of 240 µm, produced with the so-called *thinned Float-Zone* process (thFZ240) and an active thickness of 290 µm produced with the standard Float-Zone technique (FZ290). The FZ290 undergoes a special treatment during fabrication which allows the backside p^+ doping to extend up to 30 µm, resulting in a physical sensor thickness of 320 µm. The thick backside gives the sensor good robustness against scratches. The wafer is fully processed in this thickness state. The thinner sensors produced with the thFZ240 technique follow an additional process. The thinning happens after the processing of the front side. The backside heavily doped implant can extend only about 1 µm and it is constrained by the fact that the already processed front side can not be exposed to large temperature for a long time. Therefore, the active and the physical thickness of the sensor are similar.

More details on the experimental procedure and the results can be found in [68]. Both 2S and PS-s sensors were irradiated up to the maximum expected fluences. Since the PS-s sensors will be installed in the first layers of the Outer Tracker, they will have to cope with a maximum fluence of about 1×10^{15} n_{eq}/cm^2 after 3000 fb^{-1} (Fig. 4.1). The 2S sensors will experience a maximum particle fluence of 3×10^{14} n_{eq}/cm^2 after the same integrated luminosity. For charge collection studies, the annealing time to which the sensors will be subjected during the technical stops of each HL-LHC operation year must be considered. A realistic scenario of 20 weeks (2 weeks per year) of annealing time at room temperature over the 10 years of HL-LHC operation was adopted and an annealing procedure equivalent to this scenario was defined [68].

Figure 4.5, compares the collected signal over annealing time for the FZ290 and thFZ240 2S (Fig. 4.5a) and PS-s (Fig. 4.5b) sensors. The annealing time of 20 weeks is indicated by the dashed, black line. The horizontal red line shows the seed signal threshold which is defined by the noise of the readout chip. The sensors were biased at 600V which is the maximum operation voltage. A second case was considered, with a bias voltage of 800 V. This voltage is an option to be applied towards the end of the HL-LHC lifetime to those sensors which will be exposed to large particle fluence in order to give a boost to the collected signal. In the 2S region (Fig. 4.5a), the FZ290 shows a larger signal than the thFZ240 over a large range of annealing time at 600 V as well as at 800 V. A similar observation can be made for the PS-s sensors (Fig. 4.5b). The FZ290 sensor is well above the threshold up to an annealing time of 20 weeks, while a boost up to 800 V ensures a sufficiently large signal. The thFZ240 sensor biased at 600 V shows a signal around the threshold over annealing time, while it slightly exceeds the threshold with a bias voltage of 800 V. Only for an annealing time beyond 30 days, the thFZ240 sensors collect more signal than the FZ290. Even in this case, the signal of the thicker sensors can stay above the threshold with a boost up to a bias voltage of 800 V.



(a) **(b)**

Fig. 4.5: Seed signal of FZ290 (blue upward pointing triangles) and thFZ240 (golden downward pointing triangles) 2S (left) and PS-s (right) sensors as a function of equivalent annealing time. The sensors were irradiated up to the maximum expected fluence in the tracker region where the respective modules will be installed. Measurements were performed at −20°C [68].

All in all, the FZ290 sensors show a larger signal than thFZ240 over an annealing time of 20 weeks in both PS and 2S regions, after being irradiated with the maximum expected fluences of those regions. Furthermore, the FZ290 sensors feature a 30 µm thick backside which makes them more robust against scratches during handling than the thFZ240 with the 1 µm backside. In

addition, the cost of production is higher for the thFZ240 sensors due to the additional process. Therefore, CMS decided that the FZ290 sensors are the baseline for the Phase-2 Outer Tracker.

4.2 Sensor design

The design of the Outer Tracker sensors should ensure long-term and stable operation under high bias voltage. Especially after irradiation, the operation voltage of the sensors is expected to reach several hundreds of volts, therefore high voltage stability is essential. The following sections aim to give a detailed picture of the design principles of the Outer Tracker silicon sensors and to explain the motivation behind the selection of all the relevant parameters.

4.2.1 Strip/macro pixel geometry

The design of the implant geometry should be optimal in order to maximize the position resolution and minimize the noise levels. The Outer Tracker comprises two flavors of strip sensors (2S, PS-s) which differ in terms of a number of channels, pitch and physical dimensions but they are identical in every other design aspect. In contrast, the macro pixel sensors (PS-p) have a totally different segmentation which results in some adjustments to the implant parameters.

The active length of the strip implants is shorter with respect to the strip sensors of the current Outer Tracker. In particular, the strip length is 5 cm for the 2S sensors and 2.3 cm for the PS-s sensors. The choice of shorter strips allows an increase in the number of channels without increasing the area of the sensor, it increases the granularity and preserves a good spatial resolution at the high particle density of HL-LHC.

As it is discussed in [71], an implant width-to-pitch (w/p) ratio of 0.25 is a good compromise that satisfies high voltage stability and a not very large interstrip capacitance which would increase the noise (section 3.3). The design of the Phase-2 Outer Tracker strip/macro pixel implants respects this ratio. For 2S sensors, the pitch is selected to be 90 µm. The pitch of PS-s/PS-p implants is 100 µm. This value is the lowest allowed limit of the bump-bonding technology (C4 - Controlled Collapse Chip Connection) which was chosen for the macro pixel sensor integration [72]. Despite the constraints, this technology was preferred by CMS due to its lower cost for such a large-scale production. For the above pitch sizes, the width of the implants was adjusted accordingly in order to respect the w/p ratio.

A table which summarizes the geometry of strip/macro pixel implants for every sensor type, is given below:

Sensor type	active width (µm)	active length (µm)	number of channels
2-S	94183	102700	2×1016
PS-s	98140	49160	2×960
PS-p	98740	49160	30720

Tab. 4.1: Dimensions of Outer Tracker sensors. The active dimensions correspond to the distance of the inner edges of the bias ring (vertically and horizontally).

4.2.2 Signal Coupling

The movement of charged particles inside the silicon bulk induces a signal in the readout electrodes which in sequence is transfered to the readout electronics. The way this transfer is

Sensor type	implant width (µm)	implant length (µm)	Pitch (µm)	Width-to-pitch ratio
2-S	22.5	50724	90	0.25
PS-s	25	23472	100	0.25
PS-p	25	1467	100	0.25

Tab. 4.2: Dimensions of Outer Tracker strips and macro pixels.

realized differs between strip and macro pixel sensors due to their different configuration of the electrode-readout chip connection.

The macro pixel sensors are DC-coupled which means that the electrodes are directly connected to the amplifiers of the readout chips. In this configuration, the AC component of the current signal induced by the drift of the generated charge carriers is transferred together with the DC component which is a contribution of the leakage current. The pixel leakage current is very low due to the small size of the electrode, even after irradiation, therefore, the amplifier can cope with it by using a current compensator.

The strip sensors of CMS Outer Tracker are AC-coupled. This means that the AC component is capacitively coupled to the readout chips while the DC component is filtered out. Due to the large strip size, the strip leakage current of an unirradiated sensor is in the order of pA or a few nA but can increase up to µA after irradiation. The DC component of the leakage current can be eliminated either with the use of a high-pass filter in front of the amplifier or with the integration of a DC filter directly onto the sensor. This can be implemented by the incorporation of a dielectric oxide between each strip implant and the aluminum electrode. This configuration emulates a parallel-plate capacitor. Typically the dielectric is made of a thin silicon dioxide (SiO_2) layer which can be covered by a second dielectric layer of silicon nitride (Si_3N_4). Silicon dioxide with the addition of silicon nitride is used for the coupling oxide of Outer Tracker strip sensors. The thickness of the dielectric is a crucial parameter since it determines the coupling capacitance of the strip.

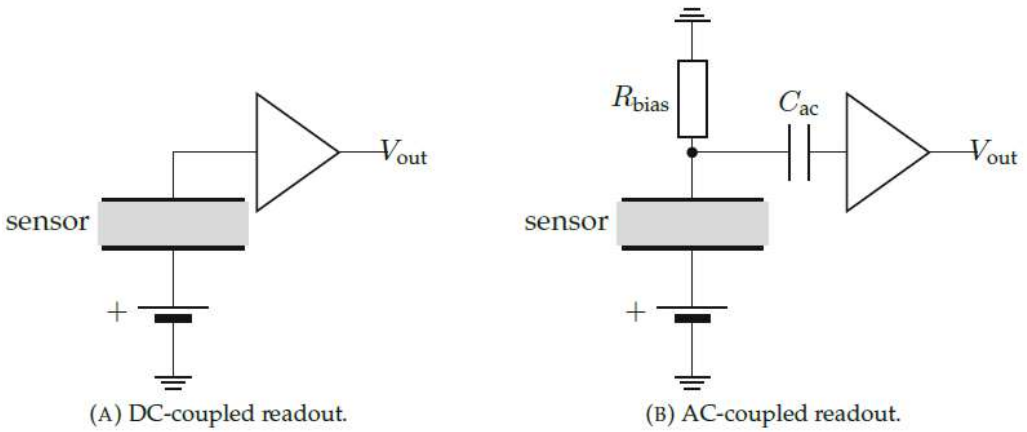


Fig. 4.6: The DC (left) and AC (right) coupling scheme. For DC-coupled sensors, all current components are transferred directly to the amplifier of the readout chip. For the AC-coupled sensors, the integrated coupling capacitor decouples the AC from the DC signal. The readout chip receives the AC component while the DC current is driven to the bias resistors.

4.2.3 Biasing

A potential between the front and backside of a sensor must be applied in order to deplete its active volume. For a n-on-p sensor, the reverse bias is established by applying a negative voltage to the p-type bulk while the n^+ implants are set to ground. The depletion zone starts to grow from the implants towards the backside electrode (the n^+ implants form a p-n junction with the silicon p-type bulk). Between the backside metal and the silicon bulk a heavily p^+ doped implant of low resistivity is introduced which provides a good ohmic contact to the 1 µm thick aluminum backside metalization. In addition, in case of over-depletion, this layer prevents the strong electric field from reaching the backside and trigger an avalanche breakdown effect.

In the strip sensors, the front side is set to ground potential through the *bias ring* which is a ring-shaped n^+ implant surrounding all strip implants and featuring a metalization on top. Each individual strip is set to ground via the bias or polysilicon resistors which are connected to the bias ring (Fig. 4.7). The bias resistors are made of doped polycrystalline silicon and feature a meander structure which ensures a high resistance value on such a small area. They are very radiation-hard structures which makes them the ideal selection for the CMS environment. The implantation dose and therefore the resistance of the polysilicon can be adjusted by the manufacturer. Furthermore, the polysilicon resistors isolate electrically the strips and offer current protection in beam-loss scenarios, where the sensor is exposed to very high particle fluxes which can induce very large currents. CMS has set a target resistance value of 1.5 ± 0.5 MΩ.

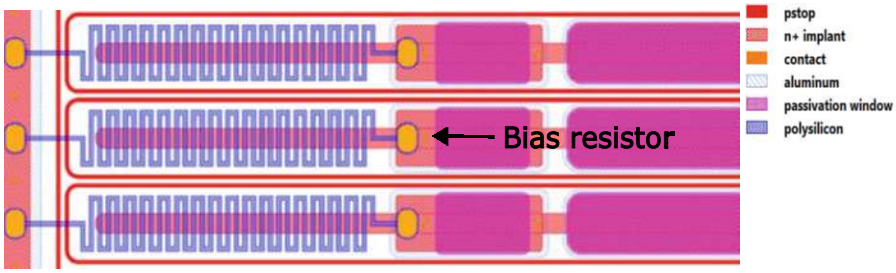


Fig. 4.7: PS-s sensor layout with polysilicon meander structures. The bias resistors are connected to the bias ring from one side and to the strip implant from the other side.

In the case of DC-coupled macro pixel sensors, the ground potential is applied to each individual pixel via the readout chip. However, to facilitate pixel testing before the bump-bonding of the pixels to their readout chips, a *bias grid* is implemented which acts as an additional biasing structure. The bias grid is connected via punch-through structures to each pixel (Fig. 4.8).

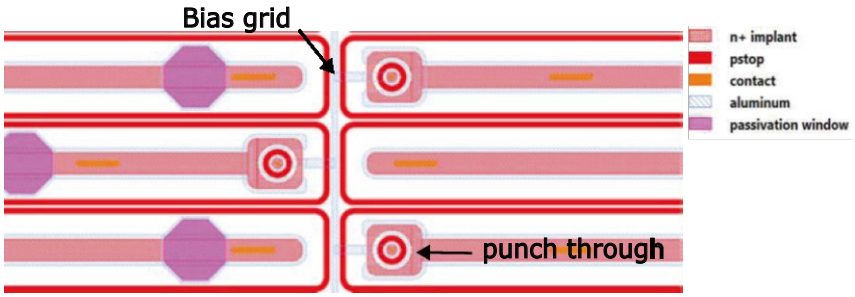


Fig. 4.8: PS-p sensor layout with bias grid and punch-through structures.

4.2.4 Stability under high voltage

The CMS sensors are typically operated in over-depletion to ensure a large drift velocity of the collected charges and to minimize their collection time. The full depletion voltage for a p-type bulk increases constantly with irradiation. The full depletion voltage for the unirradiated Outer Tracker sensors is between 200 to 300 V, therefore the operation voltage of the sensors is expected to reach several hundreds of volts by the end of the HL-LHC lifetime. The sensors are specified to operate long-term under high voltage without problems and especially without exhibiting any electrical breakdown. To guarantee high voltage stability, special elements are taken into account when it comes to the sensor design. In principle, the strong electric fields which are developed inside the silicon bulk due to the applied potential should never exceed the breakdown voltage of silicon which is 30 V/µm.

Starting from the physical edges of a sensor, the existence of local defects induced by the dicing process (when the sensor is cut from the wafer) is unavoidable. These defects are a potential threat to trigger an electrical breakdown. While biasing the sensor, if the lateral spread of the electric field reaches the edge defects, an avalanche breakdown can be induced. To restrict this spread, a p^+ implant, the so-called *edge ring*, is introduced. The edge ring encircles the whole sensor, is heavily doped and prohibits the space charge region from reaching the edges.

The p^+ edge ring is set to the same potential with the backside due to the formation of a conductive connection between the edge ring, p-type bulk and p^+ backplane implant. Considering that the bias ring is set to ground potential, there is a voltage drop in the lateral direction between the edge and the bias ring. This rapid decrease of potential in the lateral direction can produce an electric field peak which can result in a breakdown. It is necessary to establish a smooth voltage drop towards the sensor edge. This is facilitated by an additional n^+ implant between the bias and the edge ring. It is known as the *guard ring*. The guard ring is left floating. Simulations have shown that with this configuration, a more uniform lateral voltage drop is achieved [73]. Figure 4.9 shows the layout of a corner of a PS-s sensor, in which the bias, guard and edge ring are annotated.

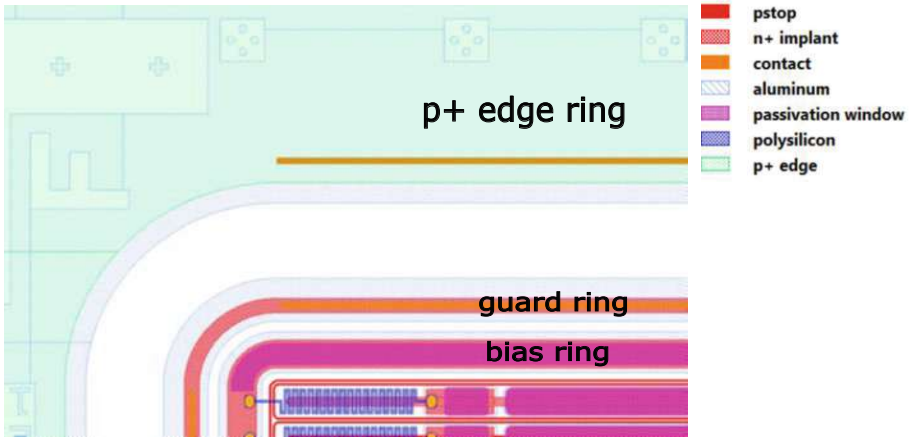


Fig. 4.9: PS-s sensor layout with edge ring, guard ring and bias ring annotated. The picture shows a corner of the PS-s sensor.

CMS uses a design feature to further improve the high voltage stability of the implants which is known as *metal overhang*. The metallization on top of each strip is designed to be 5 µm wider than the implant itself. The metal overhang is asymmetric for the bias, guard and edge ring. All Outer Tracker sensors feature identical periphery. The positive effect of using the metal overhang technique is that the maximum electric field densities do not peak at the edges of the

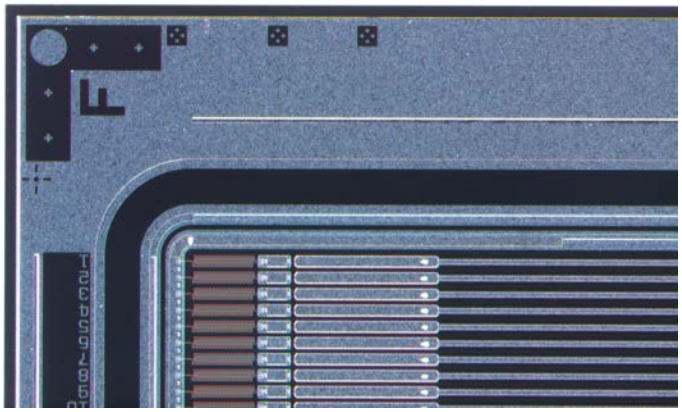


Fig. 4.10: Picture of the top left corner of a 2S production sensor.

strip implantation but rather in the oxide. This is desirable because the SiO_2 exhibits two orders of magnitude larger dielectric strength than the silicon.

In addition, structures with sharp corners (for example small corner radii) can potentially create local peaks of the electric field strength which if exceeding the critical field could cause a breakdown of the sensor. For the Outer Tracker silicon sensors, every implant corner is designed with a radius R $\geq$ 5 µm.

Parameter (in µm)	Outer Tracker Sensors
Bias ring implant width	75
Guard ring implant width	40
Minimum width of edge ring	500
Bias ring to guard ring distance	70
Guard ring to edge ring distance	300
Metal overhang strips/pixels	5
Inner metal overhang bias ring	10
Outer metal overhang bias ring	20
Inner metal overhang guard ring	20
Outer metal overhang guard ring	50
Inner metal overhang edge ring	50

Tab. 4.3: Dimensions of Outer Tracker sensors ring structures in the common periphery. All units expressed in µm.

4.2.5 Interstrip/Interpixel isolation

A good electrode isolation is essential in a position-sensitive sensor in order to prevent an ohmic connection between adjacent strips or pixels. If a cross-talk happens, the signal induced on one strip will be also seen in the neighboring strip. This effect will deteriorate the position resolution of the detector. The interstrip resistance between the neighboring implants must be

high enough in order to ensure that isolation is established and no conductive path is formed between them. The interstrip resistance should be orders of magnitude larger than the polysilicon resistance before and after irradiation, an essential condition which would not allow the charge sharing between consecutive strips.

The formation of an accumulation layer of electrons is created due to the presence of positive oxide charges in the Si-SiO_2 interface. The positive charges attract electrons from the silicon bulk which accumulate near the interface and can short-circuit the adjacent implants. This layer becomes critical for the sensors with n^+ strip or pixel implants due to electron collection while it is no issue for the sensors with p^+ electrodes (such as p-on-n sensors) which collect holes. To interrupt the formation of this conductive path, an additional p^+ implantation is introduced in the area between each consecutive strip/pixel. In principle, two different techniques can be used (Fig. 4.12).

The first method is known as *p-stop* technique using a p^+ implant which surrounds each strip/pixel at a defined distance. The p-implant forms a p-n junction with the n^+ strip. The disadvantage of this method is that it requires additional steps during the fabrication process for the formation of the p-stop. This increases the cost of production.

An alternative method is the so-called *p-spray* technique. Here, a shallow and uniform layer of p-doping covers the whole wafer. It is a cheap method since it does not require any additional photolithography step. The p-spray technique is a simpler option in case the distance between the implants is small.

CMS decided for the use of the p-stop method as a baseline for the Phase-2 Outer Tracker sensors. The p-spray was rejected due to the fact that it is more difficult to control the implantation dose over large areas and over production time. The p-stop implants fully surround each strip in an atoll configuration, they are 6 µm wide at a 4 µm relative distance to each other.

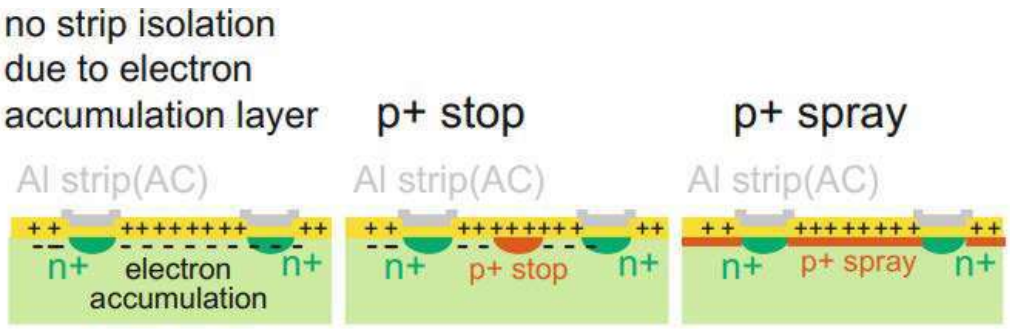


Fig. 4.11: The formation of a conductive layer of electrons in an n-on-p sensor happens due to the positive charges distributed in the silicon-silicon dioxide interface (left). The introduction of a p-stop, between the strips repels the electrons and interrupts the conductive path (middle). Similarly, a uniform distribution of p-doping on the bulk, the so-called p-spray technique, can sufficiently isolate the adjacent strips (right) [19].

4.2.6 Contact pads

For the AC-coupled strip sensors, each strip features two pads, the DC and the AC pad. The DC-pad is directly connected to the strip implant via contact holes which are etched through the dielectric layer. Its functionality is to facilitate strip characterization and measurements such as the strip leakage current and the resistance of the bias resistor. Each strip features two DC pads, one at each end. For the DC-coupled PS-p sensors, there is only one DC pad on each macro

pixel. The AC-pad, which is only present in the strip sensors, is extended over a large fraction of the strip metal. It facilitates the electrical characterization of the strip but it is primarily used for the connection of the strip to the readout chip with wire bonds. No wire bonds are used for the connection of the macro pixels to the readout chips due to the small size and large density of pixels. Each macro pixel is bump-bonded to its readout chip.

Fig. 4.12: Illustration of a single strip with the DC and AC pad annotated.

4.2.7 Passivation

The operation of a sensor can be strongly influenced by contamination, dust or humidity coming from its external environment. Furthermore, any sort of mechanical damage on the surface of the sensor during its handling can potentially degrade its behavior. In order to protect the sensor from external influences, a passivation layer on top of the sensor is introduced. The most common materials used are silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) both featuring high electrical resistivity. Typically only one material is used for the passivation layer. It is crucial that the oxide of the sensors feature no contaminants because even a small concentration of charges in it can change the electric field configuration in the silicon bulk-oxide interface and near the implants.

The CMS Outer Tracker sensors feature a passivation of SiO_2. The passivation layer features openings on the DC, and AC pads as well as on the bias ring to enable contact with the probe needles during testing and also to allow wire bonding.

Chapter 5

Quality assurance plan

The Phase-2 tracking system requires 26400 silicon sensors in total: 15216 2S, 5592 PS-s and 5592 PS-p sensors. The contract for the sensor production was awarded to *Hamamatsu Photonics K.K* (HPK) [74]. In order to monitor and characterize this large-scale production, CMS defined a quality assurance strategy. It includes the optical inspection, electrical characterization and irradiation tests of the produced sensors on a sampled basis. Several parameters are extracted from the measurements and compared with the CMS specifications. Through this process, the quality of the sensors and the wafers is evaluated.

The following sections give an overview of the CMS plan for the characterization of the mass production of Phase-2 Outer Tracker sensors and present the CMS quality assurance scheme.

5.1 The final wafer layout

The Outer Tracker sensors are produced on 6-inch wafers. Figure 5.1 shows a picture of a real 2S production wafer. A 2S wafer hosts one main sensor while the PS-s and PS-p wafers host two main sensors. The periphery of the wafers houses several sets of test structures and mini-sensors. An example of a mini sensor and a set of test structures from a PS-s wafer is shown in Fig. 5.2.

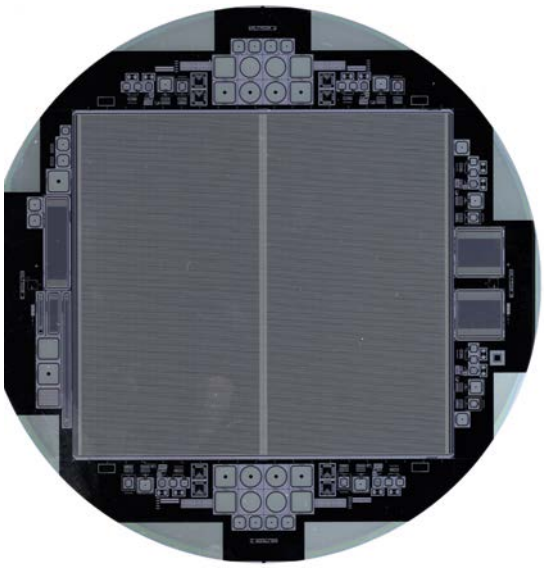


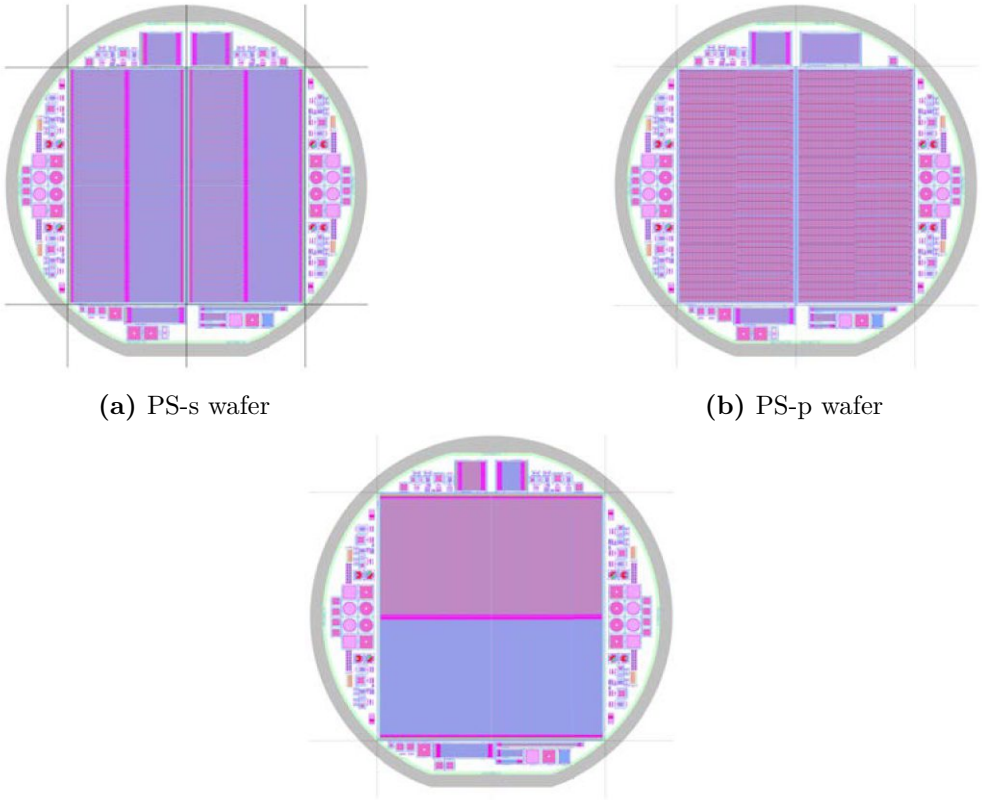
Fig. 5.1: Picture of a production 2S wafer. The test structures and mini-sensors surround the main sensor.

After the dicing of the main sensor, the remaining dies which have a semi-circular shape, include the test structures and the mini sensors. These wafer segments are known as *half-moons*. The half-moons are delivered to CMS, in addition to the main sensors, for electrical characterization.

(a) **(b)**

Fig. 5.2: Layout of a mini sensor (a) and a set of test structures (b) from a PS-s wafer.

The two main sensors of the PS-s and PS-p wafers are placed next to each other without any separation. There is no risk of damage during the dicing process because the HPK stealth dicing method has a kerf of zero. An overview of the stealth dicing is given in section 3.5.2.6. Figure 5.3 shows the layout of the three Phase-2 Outer Tracker wafers. The black vertical and horizontal lines indicate the dicing lines. A 2S wafer has four dicing lines, therefore besides the main sensor, there are 4 half-moons remaining after the dicing. The PS-s and PS-p wafers (Fig. 5.3a, 5.3b) have one additional dicing line which intersects the wafer at the center and acts as a guide for the separation of the two sensors during dicing. Four dies above and below the main sensors are the outcome of the dicing, in addition to the two dies at each side of the main sensors. Thus, the PS-s and PS-p wafers have 6 half-moons in total.



(a) PS-s wafer **(b)** PS-p wafer

(c) 2S wafer

Fig. 5.3: Layout of Outer Tracker wafers as designed with the software KLayout. The main sensor or sensors are located at the center of the wafer while mini sensors and several test structures are housed on the periphery.

5.2 Production schedule and overview

The production of the Outer Tracker silicon sensors started in 2020 and it will be completed in the first half of 2024. The new Outer Tracker needs for 26400 silicon sensors, nevertheless, CMS has placed an order of 6.5% additional strip sensors and 14% additional macro pixel sensors. These extra orders are a contingency to compensate for losses during detector assembly. A small, negligible number of sensors might be damaged during sensor qualification in CMS centers due to mishandling or accidents while testing. The number of losses is expected to be larger during module assembly which is a process requiring a sequence of high complexity steps. An example of the procedure for the assembly of a 2S module is given in [75]. The larger number of extra PS-p sensors takes into consideration that the macro pixel sensors undergo an additional procedure, the bump bonding process. Additional orders can be placed by CMS, if needed, before the final months of production.

The mass production of Outer Tracker sensors is divided into two phases: *pre-production* and *production* phase. Sensors from both phases will be used in the CMS detector. The pre-production period spanned from July to October 2020 and includes the first 5% of production. During the sensor qualification by CMS, a non-critical design weakness in the polysilicon resistors was discovered. More information is given in Appendix A. CMS requested a modification of the polysilicon resistor meander design which was implemented by HPK. Sensors from one batch showed problems with regions of low interstrip isolation and electric breakdown at low voltages, therefore this batch was rejected. More information is given in section 9.4. Apart from that, all characterized wafers from the pre-production phase conformed well with the specifications. The main production phase started in the first months of 2021. For the PS-p sensors, the timeline was different since the final wafer design had not been submitted by the time the pre-production of the strip sensors started. Therefore, the first deliveries of pre-production PS-p sensors arrived at the beginning of 2021. Their production phase started no sooner than the summer of 2022 due to the fact that the companies that would be responsible for the MaPSA assembly had not been chosen yet.

The processing of the wafers is done in groups or *batches*. This means that the wafers of a batch should share identical electrical properties since they were processed consecutively and under similar conditions. The wafers of a batch do not come necessarily from the same ingot but a batch should not comprise wafers from more than two different ingots. A typical delivered batch contains 40 to 45 wafers. The PS-s and PS-p wafers house two sensors, therefore each batch contains typically a number between 80 to 90 sensors.

The sensors and half-moons are packed individually in envelopes and are placed in a “sandwich” configuration between two plastic cards which offer protection to the structures (Fig. 5.5). The envelopes are labeled with strings which act as an identifier for the sensor or the half-moons of a wafer. A picture of an HPK envelope is shown in Fig 5.4. The string “Type” refers to the ingot number. The string “Serial No” contains the batch number, a unique wafer number between 1 to 50 which distinguishes the sensor/half-moons from the rest of their batch, the wafer type and an identifier of the type of structure (sensor or half-moon). The string “Scratch No” is the scratch pad assigned by HPK to easily identify the sensor.

The envelopes with the structures are packed into boxes and sealed with moisture-proof packaging. All sensors from a single production batch should be packed in the same box. The boxes are delivered to CERN and then are re-distributed to the CMS test centers. The opening of the boxes and breaking of the seal happens in the CMS clean rooms while the boxes are stored in a dry cupboard until all the selected sensors or half-moons from the batch are characterized. More information about quality assurance is given in the following section.

Fig. 5.4: Example of an HPK envelope in which the production sensors are placed.

Fig. 5.5: Envelope including a production 2S sensor and the plastic cards.

Figure 5.6 shows the number of sensors per delivered batch to date. The x-axis shows the batch number as assigned by HPK. The ascending order is assumed to correspond to a time evolution. The dashed lines describe the lower accepted number of sensors per batch type, which is 30 (orange dashed line) for 2S and 75 (blue dashed line) for PS-s and PS-p. A significant number of low-yield batches were delivered to CMS in the first half of 2022. The vendor attributed this issue to a low-quality wafer material that was provided by their supplier. This had an impact on the production which resulted in a decrease in the yield and the delivery rates.

Regarding the low-yield batches, HPK reported that only specific wafers were affected in each of these batches. The sensors from these wafers were not delivered to CMS since they violated the specifications. The delivered wafers were free of defects and their quality showed no problems. This was validated by CMS with an increase in the testing sampling rate for the sensors which come from the low-yield batches. Indeed, the electrical parameters of the sensors and test structures showed no deviation from the usual batches. HPK announced that since the summer of 2022 the delivered batches should contain no more wafers from the problematic material and as a matter of fact, the yield went up to the usual numbers. There was no effect on the module assembly because the start of module production was planned for 2023 while a large number of sensors had been already qualified and stored in the CMS centers.

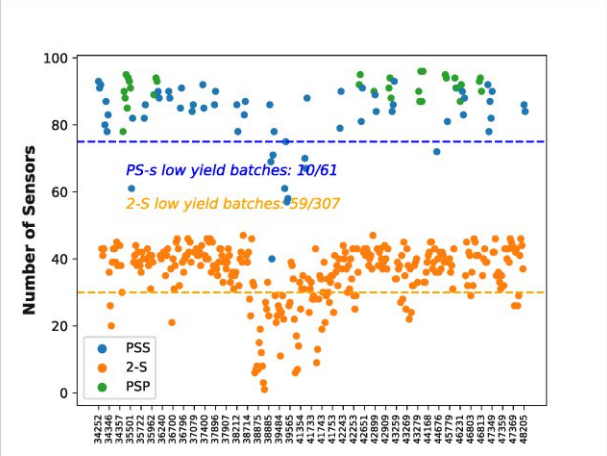


Fig. 5.6: Evolution of the delivered number of sensors per batch. The ascending batch order is assumed to correspond to a time evolution. The dashed lines indicate the minimum expected number of sensors within a batch, which is 30 for 2S (orange dashed line) and 75 for PS-s and PS-p (blue dashed line).

5.3 Quality assurance

During the mass production, it should be ensured that all the produced sensors meet the requirements and are usable for instrumenting the Phase-2 Outer Tracker. The conformity of the wafers is validated through an electrical characterization from which several parameters are extracted and compared to the CMS specifications. These specifications have been established from long R&D campaigns. CMS defined a quality assurance plan to facilitate, organize and coordinate the qualification process. The plan is divided into four parts.

At the first level, HPK performs a minimum set of electrical tests to determine the quality of the produced wafers. Only those wafers which conform to the specifications are sent to CMS. This part of the quality assurance plan is known as *Vendor Quality Control* (VQC). It includes voltage-current and voltage-capacitance measurements of each sensor as well as a minimum characterization on each strip for defect identification. HPK performs electrical measurements on the AC pads to detect pinholes and aluminum shorts between two neighboring strips and on the DC pads to detect leaky strips (strips with high leakage current) and problems with the bias resistors.

The qualified sensors are delivered to CERN and then distributed to the quality control centers (QC centers). They are institutes which belong to CMS collaboration and are equipped with all the required infrastructure to perform extensive and detailed electrical tests on the sensors and test structures. The European qualification centers are the Institute for High Energy Physics in Vienna (HEPHY), Karlsruhe Institute of Technology (Germany), INFN Perugia (Italy), and NCSR Demokritos (Greece). From the USA the Brown University, Rochester Institute of Technology, and from Asia, the University of Dehli (India) and the National Centre of Physics in Islamabad (Pakistan) are the centers which contribute to this project.

The QC centers are responsible for the remaining three parts of the quality assurance scheme: the Sensor Quality control (SQC), the Process Quality control (PQC) and the Irradiation tests (IT). The overall quality assurance flow chart is displayed in Fig. 5.7. Each part is described in more detail in the following subsections. All extracted results from these procedures are combined in order to characterize the quality of a batch. In addition, all three parts are a very useful tool to monitor the production, to observe general trends of all interesting parameters and

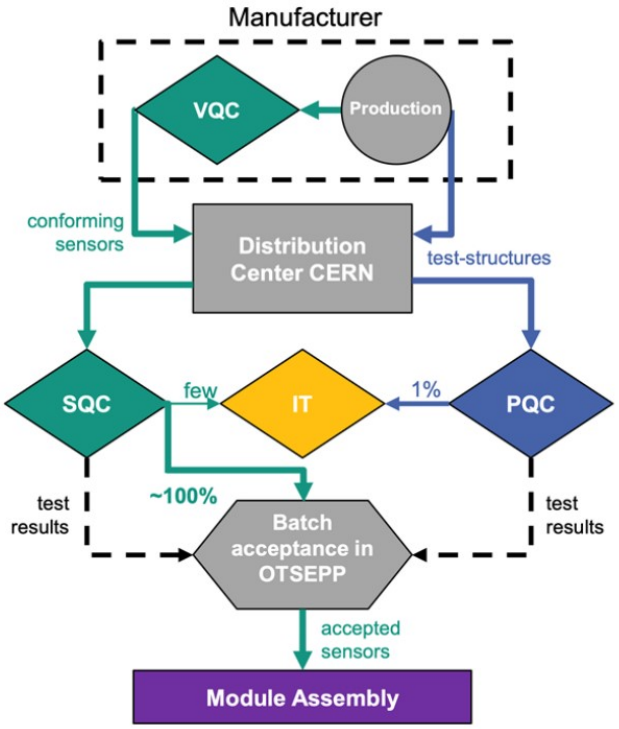


Fig. 5.7: Flow chart of Phase-2 Outer Tracker quality assurance plan.

to spot in time any deviations from their expected values. Such deviations, especially when they become frequent or start forming trends, can indicate potential issues related to the production sequence and therefore they must be communicated as soon as possible to the vendor.

5.3.1 Sensor Quality Control

Sensor quality control (SQC) is a process which includes the optical inspection and electrical characterization of individual sensors in order to ensure that they conform with the specifications. The QC centers perform measurements, on a sampled basis due to the large number of sensors and the required time of a full characterization which is about 8 hours for a single sensor. The selection of sensors for testing is based mainly on the I-V data from VQC. The sensors which show larger currents than the average currents of their batch or an electric breakdown are typically candidates for a full characterization.

The SQC part concerns only the qualification of strip sensors. The macro pixel sensors will be bump-bonded to their MPA readout chips, therefore any additional handling during sensor testing might introduce contamination on the pixels or mechanical damage. Also, the characterization of each of the about 30000 pixels would be very time-consuming. Thus, CMS relies only on VQC and PQC to qualify the macro pixel sensors.

Electrical characterization of strip sensors includes the investigation of a number of parameters which can be divided into two parts: the global parameters and the strip parameters. The global parameters describe the general behavior of the full sensor through a current-voltage (I-V) and a capacitance-voltage (C-V) measurement. With the current SQC measurement configuration, the strip parameters (such as strip current, resistance of bias resistor, current through dielectric, coupling capacitance) are measured on each 4^{th} strip while the interstrip parameters (interstrip

resistance and capacitance) are measured on every 15$^{\text{th}}$ strip. A detailed discussion of the measurement procedure follows in the next section.

Besides the investigation of single parameters, the sensors are exposed to long-term biasing with a voltage of 600 V in a temperature and humidity-controlled environment. The temperature is set to T = 21 ± 1°C and the relative humidity below 10%. The current of each sensor is monitored over a time span of 48 hours and the current is measured every 60 s.

5.3.2 Process Quality Control

Process quality control (PQC) is a method to characterize the stability and quality of the production process through measurements on test structures. The test structures are produced on the same wafer with the sensors, they undergo the same process during fabrication and as a consequence, they share the same properties with them. Therefore, performing an electrical characterization on the test structures is an alternative way to investigate the sensor properties. The test structures offer the capability of extracting sensor parameters which can not be easily measured on the main sensors. Furthermore, the same test structures are replicated across each wafer several times. This multiplicity allows for investigating the uniformity of each parameter over the full wafer. The PQC measurements are fast and time-efficient which facilitates the characterization of a larger fraction of wafers and consequently allows for an increase in statistics.

5.3.3 Irradiation tests

Irradiation tests (IT) include hadron and X-ray irradiation on mini-sensors and test structures up to the maximum expected fluence to which the sensors of the Phase-2 Outer Tracker will be exposed (Fig. 4.1). The radiation hardness of the sensors over production time is monitored and compared to the behavior established for the prototyping sensors. For the X-ray irradiation, the X-ray dose goes up to 40 kGy and allows for studying separately the surface damage on the thick oxide. Only a sample of batches which have been tested in SQC undergo irradiation tests since this process requires a lot of time. Therefore IT is not included in the final batch qualification decision.

After irradiation, the mini sensors go through an annealing procedure which is defined by the CMS irradiation centers [61]. The electrical characterization is performed at T = −20°C to prevent further annealing and at low dew point to prevent condensation. The electrical characterization of mini sensors includes also signal measurements with the use of a Sr-90 source and an analog read-out system, such as Alibava. This measurement comprises voltage scans from 300 V to 900 V with a 100 V step during which the signal is measured. The test is repeated four additional times for different annealing steps; 60 min at 60°C, 120 min at 60°C, 30 min at 80°C and 60 min at 80°C. More information about the defined IT procedure is given in [61].

Chapter 6

Sensor Quality Control

The electrical characterization of silicon sensors requires a dedicated probe station equipped with all the necessary devices and tools in order to perform all the defined measurements in a reliable and time-efficient way. The probe station should be housed in an ESD-safe clean room, where the temperature should be well-controlled to guarantee consistency over different measurements. A full characterization includes the extraction of global and strip parameters. A description of the parameters as well as the measurement procedures is given in section 6.3. Due to the large production volume, all CMS SQC centers should be able to fully characterize at least one sensor within one working day.

The Institute for High Energy Physics in Vienna (HEPHY) is one of the CMS centers which are responsible for sensor testing. It is committed to qualify 25% of the total sensor quantity. The SQC probe station at HEPHY is described in the following section.

6.1 SQC setup at HEPHY

The SQC setup at HEPHY is a custom-made development which is designed to perform semi-automatic measurements of strip sensors. It can measure a large variety of physical parameters such as current, voltage, capacitance and resistance while high bias voltage can be applied to the sensor. The measurements are performed in a temperature and humidity-controlled environment. The setup is semi-automated with all the electrical tests being done by custom-made python software.

6.1.1 The probe station

The probe station located at HEPHY clean room (Fig. 6.1) is enclosed by a light-tight metal box which, in addition, shields the setup from stray electric fields. Inside the box, there is a x-y-z stage installed which is moved by a motor along all three axes with very high precision, in the order of micrometers. A vacuum jig (chuck) is mounted on top of the stage. The sensors or devices under test are placed on the chuck for a measurement (Fig. 6.2). The jig features several vacuum holes. The vacuum is switched on during a measurement so that the sensor is fixed onto the chuck. The high voltage is provided to the backplane of the sensor through the chuck while an embedded PT100 sensor measures the temperature of the chuck surface. Two small extensions are installed on one side of the jig which host two micro-positioners. The needles of the two positioners contact the bias ring and set the sensor to ground potential (Fig. 6.2). On the other side, a platform hosts up to four micro-positioners with needles aimed for strip measurements (Fig. 6.1). An additional z stage is mounted on the platform which hosts the two positioners which contact the AC pads and are driven upwards and downwards upon a software command to the *Tango Mini 3* controller [76].

Furthermore, the probe station includes a microscope with a mounted camera which facilitates the placement of the needles on the sensor pads. The relative humidity and temperature of the air inside the box are measured by temperature and humidity sensors while a dry air supply system flushes the probe station with nitrogen in order to control the relative humidity. A light detection sensor measures the intensity of light inside the box. An ion blower device is installed at a safe distance above the jig. The motivation for integrating an ion blower in the setup is discussed in section 7.2.

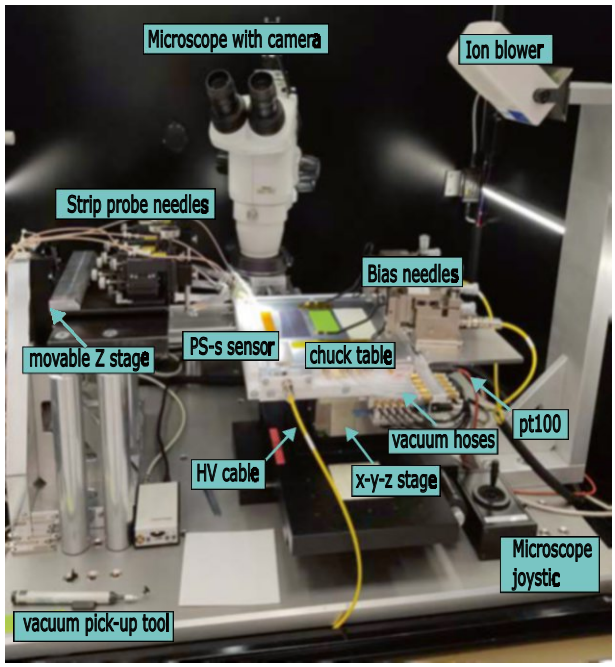


Fig. 6.1: Picture of the SQC probe station at HEPHY.

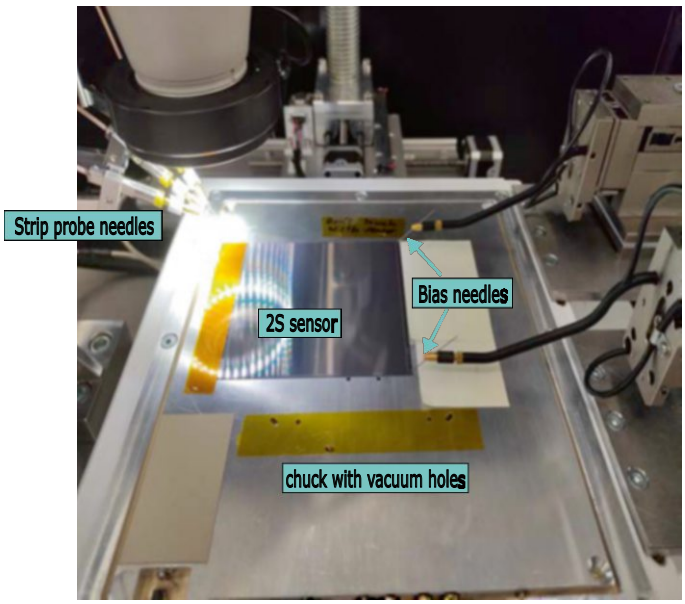


Fig. 6.2: A 2S sensor placed on the vacuum jig with the bias needles connected.

6.1.2 The measurement devices

The SQC setup comprises four measurement devices which are used for the electrical characterization. A Keithley SMU 2657 applies the bias voltage and measures the total current of the sensor, a Keithley SMU 2410 is used for low voltage and current measurements, a Keithley 6514b electrometer for precision current measurements and a Keysight E4980b LCR meter for capacitance measurements. The LCR meter is connected to a decouple box which decouples the bias voltage path from the capacitance measurement path. The devices that apply the low voltages (electrometer and 2410 SMU) are directly connected to the switching matrix. The switching matrix is responsible for the switching of all low-voltage signals between different measurements. On the other hand, the high-voltage paths are connected to a custom-made unit with high-voltage switches. The switches are controlled by a microcontroller. A rack located near the probe station hosts all the SQC instruments (Fig. 6.3). A drawing of the HEPHY SQC switching scheme is given in Fig. 6.4.

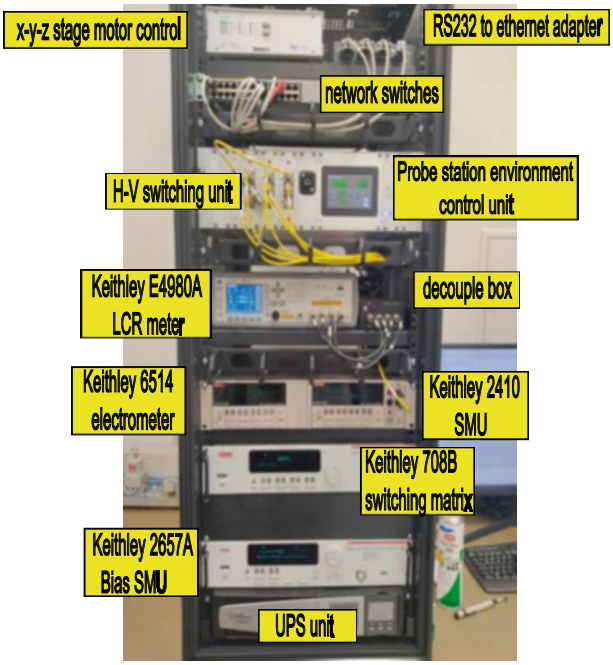


Fig. 6.3: Picture of the rack which hosts the devices used in SQC setup at HEPHY

The unit for the HV switching can handle voltages up to 3 kV. It features three inputs denoted with the letters A, B, and C and for each input there are two possible outputs (A1out, A2out, B1out, B2out, C1out, C2out). The B2out output is connected to the high potential terminal of bias SMU while the node B1out is connected to the low voltage path H of the switching card. An accidental switching from B1out to B2out could drive a high voltage of several volts to the switching matrix which could damage the device. This is why a safety diode is installed between the node B1out and the H channel of the switching matrix. As additional safety precautions, the software itself has a functionality which checks whether the switching is performed correctly.

The low voltage switching is handled by the switching matrix. The columns A to H are connected to the output nodes of the High Voltage Switching, the electrometer and the 2410 which is used for the low voltage measurements. From the 8 rows of the switching matrix, four are connected to the four positioners which contact the AC and DC pads of two adjacent strips (denoted as α and β strips in Fig. 6.4).

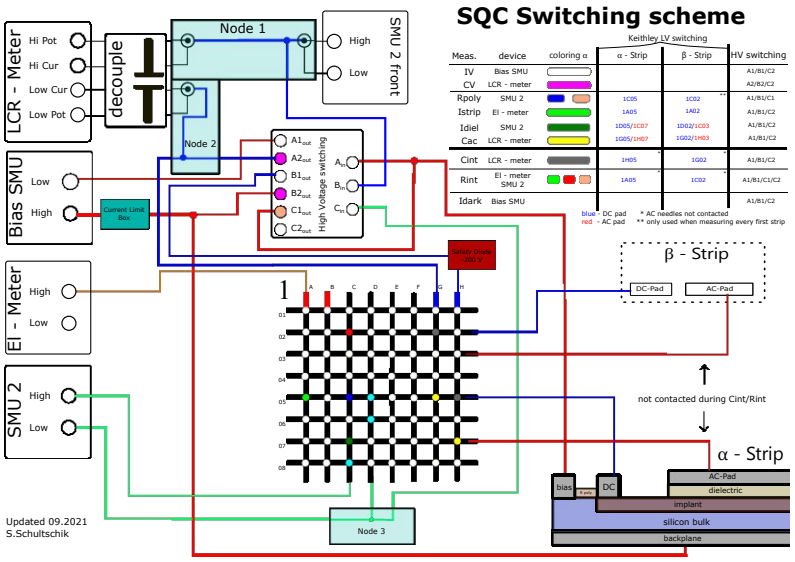


Fig. 6.4: The switching scheme of SQC setup at HEPHY.

A custom-made device developed at HEPHY is responsible for the HV switching, the reading of the temperature, humidity and light detection sensors as well as the control of the dry air supply.

6.1.3 The SQC software

A full automation of the SQC measurements is possible via the use of custom-made software, implemented in Python and developed at HEPHY. During the first 2 years of the sensor qualification process, an older software was used. However, the need for more flexible software with more functionalities which could be used beyond the needs of SQC drove the decision to implement a new software version. The new software can be found in [77]. All SQC measurements since summer 2022 are performed with the new software version.

The SQC framework consists of a set of routines, interfaces with the hardware, defines the measurement procedure, proceeds with the measurements and stores all information in JSON and ASCII files. Each measurement sequence sources information from a YAML configuration file where the user can define various parameters such as the start or end value of a voltage ramp, the waiting time until a value is fetched by a measurement device, the compliance limit or the channels of the switching matrix. A Graphical User Interface (GUI) facilitates the user-software communication. The measurement sequences are displayed in a tree configuration and can be enabled or disabled by the user according to the needs of the measurement (Fig. 6.5).

A panel of graphs with a live display of the measured parameters is located at the right side of the GUI. All data is stored temporarily in dictionaries and is written, as a final step, in ASCII and JSON files. The files are saved in the output path which can be manually selected by the user.

An additional control panel with buttons gives the option to control the x-y-z stage, the z stage with the AC needles and the microscope camera before a measurement starts (Fig. 6.6). Each button is linked to a class method and it is equipped with some functionality. The panel hosts also the buttons for the alignment of the needles with respect to the sensor position. The user can assign three alignment points, based on which the software calculates a transformation matrix which is used during the measurement in order to transform the absolute to relative

Fig. 6.5: HEPHY SQC software for automated measurements on silicon sensors.

movement. Based on that alignment, the software can perform optical inspection on the sensor by moving across the x and y coordinates of the sensor with a step defined by the user while taking snapshots at each step.

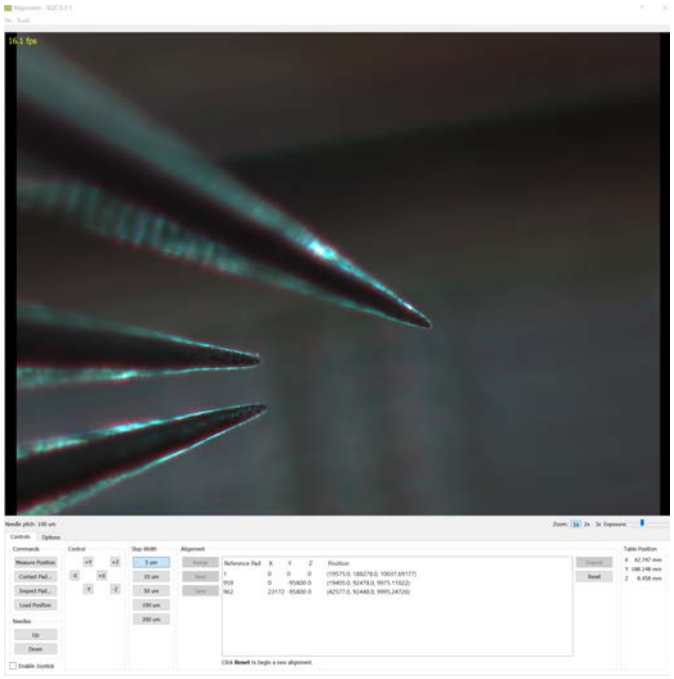


Fig. 6.6: Alignment tab of SQC software with buttons controlling the x-y-z stage and the Tango motor.

6.2 Setup for long-term sensor test

Measuring the total current of sensors biased at 600 V in an environment with well-controlled temperature and humidity, over several hours, is a part of the sensor quality control. Three sensors per batch are selected to undergo this test inside a climatic chamber for a minimum time of 48 hours. The long-term test aims to validate that the total current of the biased sensors

remains stable with time. Furthermore, the use of a climatic chamber offers more opportunities for further studies such as the dependence of the sensor electrical properties on environmental conditions (humidity, temperature).

The climatic chamber at HEPHY is a commercial product developed by *CTS GmbH* [78]. The climatic chamber can be controlled either manually via a front panel or via a software interface provided by the company. The chamber is light-shielded. The inner side of the chamber features three levels (Fig. 6.7a), each of them can host up to three plates with sensors, such as the one illustrated in Fig 6.9.

The measurement instruments used for the electrical tests are located next to the chamber (Fig. 6.7b). A Keithley SMU 2410 is responsible for providing the bias voltage to all the plates inside the chamber. Each plate is connected to a shunt resistor of a custom-made box. Each shunt resistor features a resistance of 470 kΩ. A Keithley 2700 multimeter/switch system measures the voltage drop across each shunt and through this, the total current of each sensor is extracted. A drawing of the circuit for the measurement of the total current of each sensor in the long-term setup is illustrated in Fig. 6.8. The electrical connection to the sensor plates is managed with the use of heat-resistant cables which are inserted through a cable gland into the chamber.

(a) Inner part of the CTS climatic chamber.

(b) Measurement devices used for the long term tests.

Fig. 6.7: The climatic chamber setup at HEPHY.

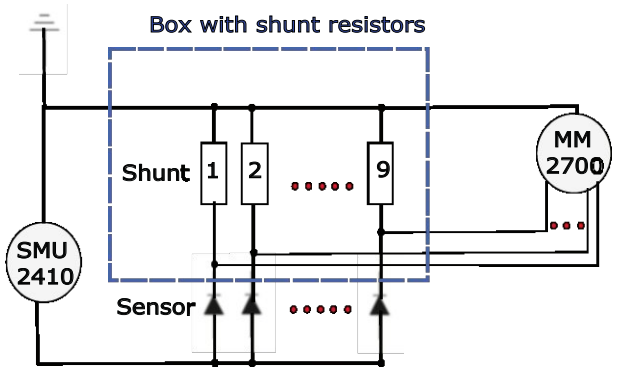


Fig. 6.8: Drawing of the circuit for the measurement of the total current of the sensors which are placed in the climatic chamber.

Each sensor is mounted on a conductive rubber plate. The position of the sensor on the plate is fixed by a Teflon bridge. The high voltage is applied from the backside while the ground is established through wire-bonding the bias ring of the sensor to the grounded pad of the plate.

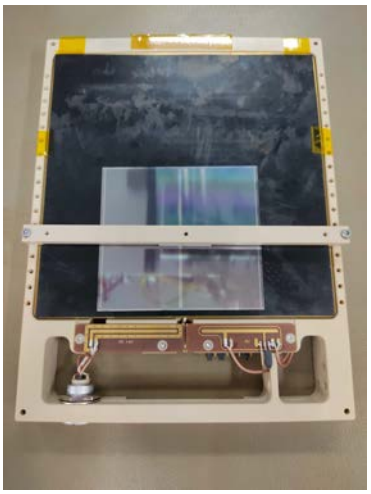


Fig. 6.9: Rubber plate on which a 2S sensor is fixed with the use of a teflon bridge.

6.3 SQC measurements

The SQC comprises electrical tests on sensors during which the global (total current, bulk capacitance), the single strip and interstrip parameters are measured. The following subsections give an outlook of each individual measurement and extracted parameter.

6.3.1 Global current measurement

The total dark current of the unirradiated Outer Tracker sensors is specified to be below 2.5 nA/mm^3 at 600 V (I_{600}). In particular, for a 2S sensor, the limit corresponds to a total current of 7.25 µA and for a PS-s/PS-p sensor to a current of 3.25 µA. In addition, the current at 800 V (I_{800}) must be lower than $2.5 \times I_{600}$. This is an indication that no electric breakdown happens up to 800 V.

The total current as a function of the reverse bias voltage is measured between the backplane and the bias ring of the sensor. The backplane is set to high potential while the bias ring is grounded (Fig. 6.10). A voltage ramp from 0 V to −1000 V with a stepsize of −5 V is performed. The minimum waiting time between applying the voltage and measuring the current is set to 0.5 s. Figure 6.11 shows an example of an I-V measurement of a 2S production sensor.

A high total current or a breakdown can be attributed to various factors such as defects inside the bulk, the presence of scratches or mechanical damage on the sensor, electrostatic charge-up or the impact of high relative humidity (chapter 7).

6.3.2 Full depletion voltage measurement

The full depletion voltage (V_{FD}) of a silicon sensor is a crucial parameter. Since the V_{FD} of a p-type bulk increases with particle fluence, this parameter should be as low as possible before

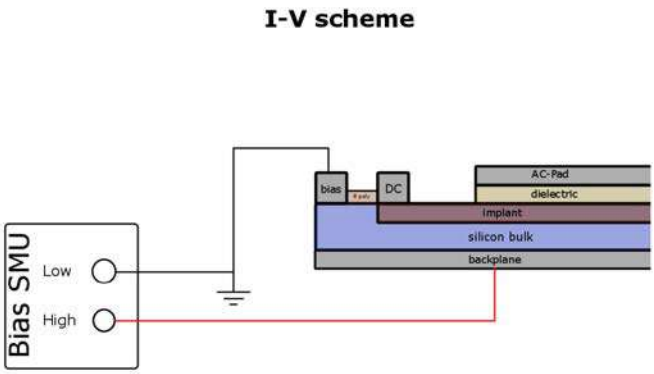


Fig. 6.10: Current - voltage measurement scheme.

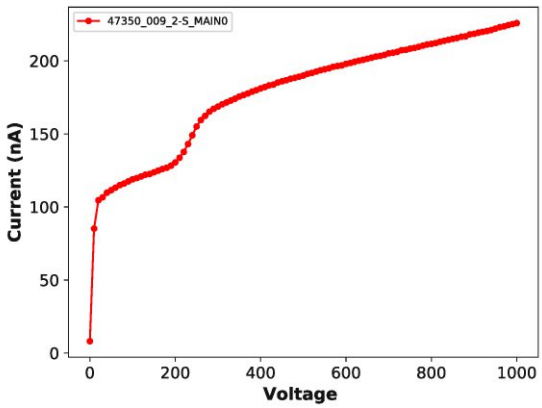


Fig. 6.11: I-V curve of 2S production sensor.

irradiation. The CMS specification is $V_{FD} < 350$ V. The full depletion voltage is extracted from a voltage-capacitance measurement of the silicon bulk.

The total capacitance as a function of the reverse bias voltage is measured between the backplane and the strips of the sensor. Similar to I-V, the backplane is set to high potential while the bias ring is grounded. The voltage ramp goes up to −600 V with a stepsize of −5 V. An LCR meter measures the bulk capacitance for each voltage (Fig. 6.12). For this measurement, the LCR is configured to a frequency $f_{CV} = 1$ kHz and a voltage amplitude $V_{CV} = 250$ mV. Figure 6.13 shows an example of a C-V ($1/C^2$-V) measurement on a 2S production sensor.

6.3.3 Strip current (I_{strip})

The strip or pixel leakage current should be as low as possible. Large strip leakage current introduces high noise levels to the readout channel which consequently deteriorates the resolution. According to CMS specifications, the strips should feature leakage current lower than 10 nA/cm. This corresponds to 50 nA for 2S, 25 nA for PS-s while for the macro pixels, the pixel current should be lower than 300 pA.

The strip leakage current can be measured with a probe needle contacting the DC pad. As described in section 4.2.6, the DC pad is directly connected to the implant. The electrometer is connected between the DC pad and the grounded bias ring (Fig. 6.14).

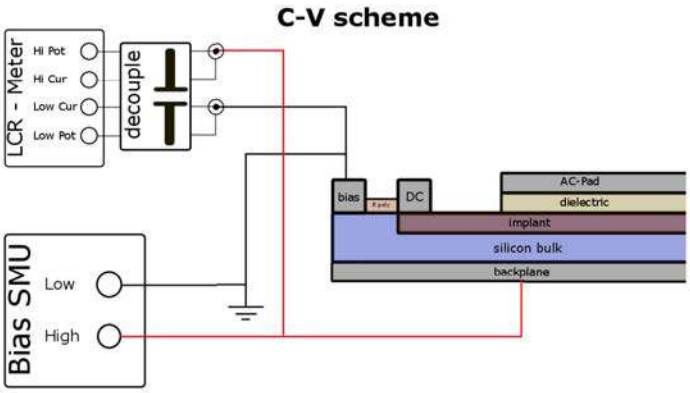


Fig. 6.12: Capacitance - voltage measurement scheme.

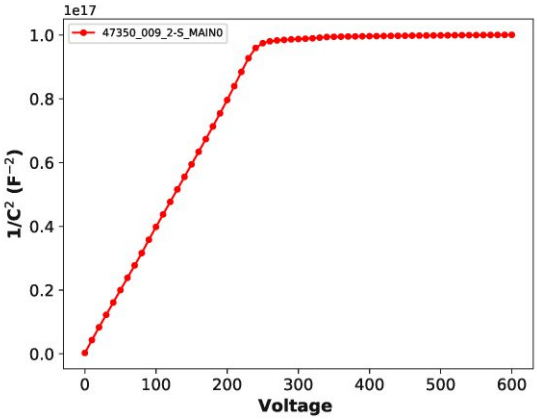


Fig. 6.13: $1/C^2$ - V curve of 2S production sensor.

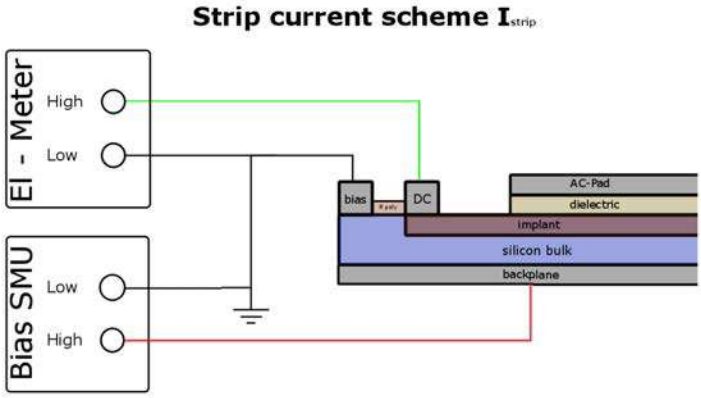


Fig. 6.14: Strip current measurement scheme.

6.3.4 Bias polysilicon resistor (R_{poly})

The resistance of the bias polysilicon resistor (R_{poly}) is specified in the range of 1.5 ± 0.5 MΩ. Also, it is important to be uniform over the whole sensor in order to guarantee uniformity of the field distribution around the implants as well as the induced signals.

To estimate the resistance of the polysilicon resistor, a low voltage difference of $V = 5$ V is applied between the DC pad and the bias ring (Fig. 6.15). The current I generated by the low voltage flows through the bias resistor to the grounded bias ring. This current must be corrected by subtracting the strip leakage current. The SMU 2410 applies the low voltage and measures the current. The resistance of the bias resistor is then extracted by Ohm's law:

$$R = \frac{V}{I - I_{\text{strip}}}$$

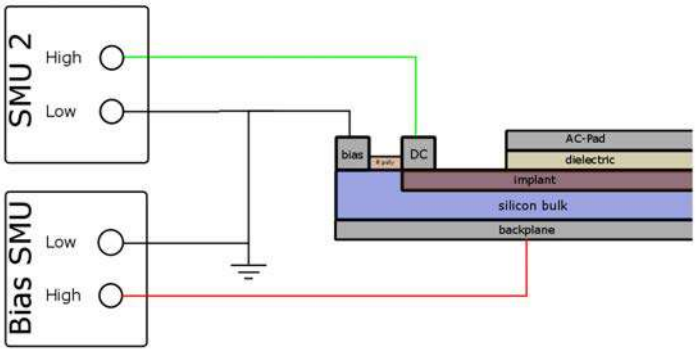


Fig. 6.15: Bias resistor resistance measurement scheme.

6.3.5 Dielectric current (I_{diel})

The dielectric current (I_{diel}) flows through the thin oxide if a potential is applied across the layer. Since the thin oxide is an insulator, I_{diel} should be negligible. Large current (in the order of nA) is an indicator of the presence of a pinhole. A pinhole is a short between the strip implant and the strip metallization on top. In the case of a pinhole, the strip current can flow into the readout electronics. The result is that the channel noise increases while the large current can potentially damage the amplifiers of the readout chip. CMS has defined the limit for a pinhole detection to a dielectric current larger than 10 nA.

A pinhole can be created when a gap or a defect in the coupling oxide is filled with aluminum. Also, a deep scratch through the aluminum and the oxide can create a conductive path between the implant and the metal.

To measure the dielectric current, a voltage difference of 10 V is applied between the AC and the DC pad of a strip and the current which flows due to this voltage difference is measured (Fig. 6.16).

6.3.6 Coupling capacitance (C_{ac})

The coupling capacitance (C_{ac}) is a parameter which is related to the AC-coupled sensors and describes the capacitance between the readout electrode and the strip implant which are separated by a coupling oxide. This value should be sufficiently high in order to couple efficiently

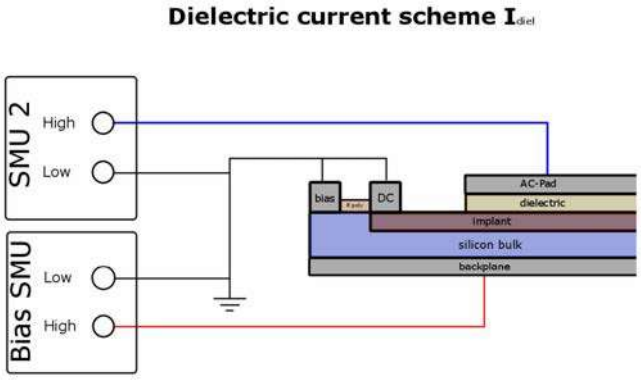


Fig. 6.16: Dielectric current measurement scheme.

the induced signal to the readout electronics. Thus, the coupling capacitance should be larger than 1.2 pF/(cm · µm) or 135 pF for a 2S and 75 pF for a PS-s strip.

The C_{cac} is measured between the AC and DC pad of an individual strip with the use of an LCR meter (Fig. 6.17). In particular, the HIGH of the LCR meter is connected to the AC pad while the LOW goes to the DC pad. The frequency of LCR is set at $f_{Cac} = 1$ kHz and the voltage amplitude at $V_{Cac} = 250$ mV. An open correction of the LCR meter should be performed before measuring a sensor and the stray capacitances of the path should be subtracted from the measured value.

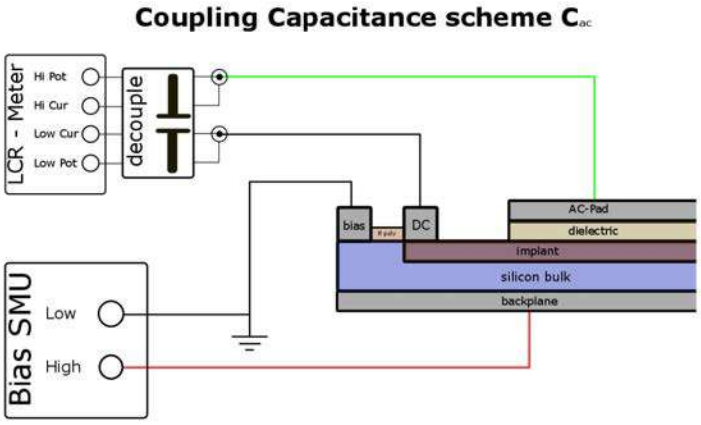


Fig. 6.17: Coupling capacitance measurement scheme.

The coupling capacitance is a parameter inversely proportional to the coupling oxide thickness (formula 3.25). Variations of the oxide thickness are directly reflected on the C_{ac}. Large strip coupling capacitance can be also an indication of a metal short. A metal short is a connection of the metal pads of two or more neighboring strips. Due to this short-circuit, the measured capacitance increases according to number of strips affected by the short. In contrast, lower coupling capacitance can hint the presence of a break in the metallization of the AC pad (open metal).

6.3.7 Interstrip capacitance (C_{int})

The interstrip capacitance C_{int} is one of the main contributors to the total load capacitance, as discussed in section 3.3. Since the load capacitance contributes to the noise of the readout

electronics, the interstrip capacitance should be low. On the other hand, C_{int} should not be too small in order to favor the charge sharing between the neighboring strips which is important for a good sensor spatial resolution. The CMS specification for this parameter is $C_{int} < 0.5$ pF/cm.

The interstrip capacitance is measured between two neighboring strips. The DC pads of two adjacent strips are contacted with two probe needles and an LCR meter measures the capacitance of the interstrip region (Fig. 6.18). The frequency of LCR is set at $f_{Cint} = 1$ MHz and the voltage amplitude at $V_{Cint} = 1$ V. Similar to coupling capacitance measurement, an open correction of the LCR meter is needed before the measurement.

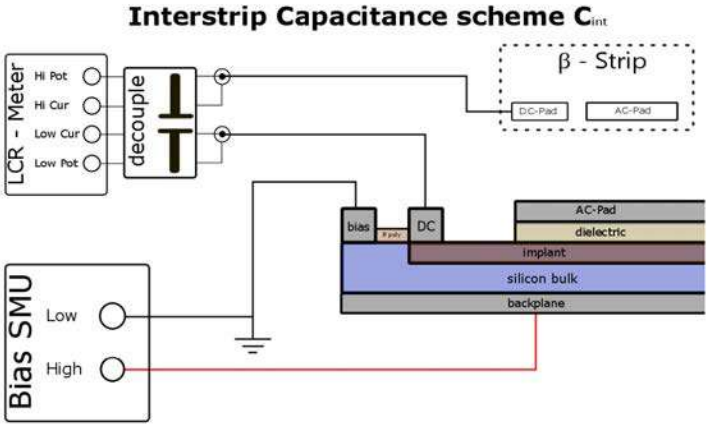


Fig. 6.18: Interstrip capacitance measurement scheme.

6.3.8 Interstrip resistance (R_{int})

Interstrip resistance (R_{int}) is the parameter which is indicative of the isolation between adjacent strips. As described in section 4.2.5, CMS uses the p-stop technique to ensure sufficient isolation of the interstrip region before and after irradiation. For strip sensors, the interstrip resistance should be much higher than the bias resistance, before and after irradiation, in order to suppress resistive charge sharing among the strips. For unirradiated strip sensors, the interstrip resistivity is specified to be larger than 10 GΩcm which results to $R_{int} > 2$ GΩ for 2S and $R_{int} > 4$ GΩ for PS-s sensors. After irradiation the interstrip resistance decreases to the MΩ scale due to radiation damage [61]. For unirradiated macro pixel sensors, it is specified that Rint > 1 GΩ.

The interstrip resistance is determined by applying a low voltage ramp on one strip and measuring the current which flows to the adjacent strip (Fig. 6.19). The measured current is the sum of the strip leakage current and the current flowing due to the applied low voltage. The voltage ramp starts from 0 V and goes up to 5 V with a stepsize of 1 V. The interstrip resistance is extracted as the inverse slope of the linear fit of the measured current over the applied voltage.

Low interstrip isolation could be attributed to a low doping of the p-stop implant or indicate the presence of defects in the p-stop. Also, the interstrip isolation is affected by the presence of a high concentration of fixed positive charges in the Si-SiO_2 interface. Furthermore, scratches on one or more strips, implant shorts or damage of the passivation can create a conductive path between the implants and therefore, reduce the R_{int}. The interstrip resistance is also affected by the presence of electrostatic charge-up on the surface of the sensor, as discussed in section 7.2.

All specifications of the Outer Tracker strip sensors parameters are summarized in Table 6.1:

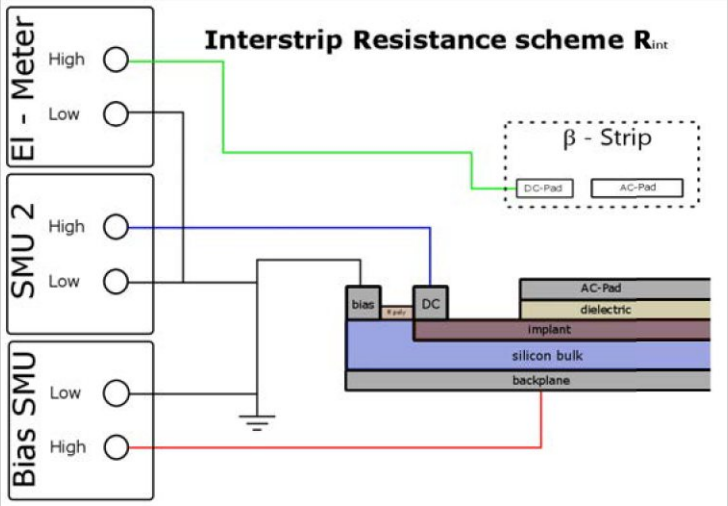


Fig. 6.19: Interstrip resistance measurement scheme.

Sensor parameter	Specification
Total current (I_{tot})	< 2.5 nA/mm^3
Full depletion voltage (V_{FD})	< 350 V
Strip current (I_{strip})	< 10 nA/cm
Polysilicon resistance (R_{poly})	1.5 ± 0.5 MΩ
Coupling capacitance (C_{cac})	> 1.2 pF/(cm·µm)
Dielectric current (I_{diel})	< 10 nA
Interstrip capacitance (C_{int})	< 0.5 pF/cm
Interstrip resistivity (R_{int})	> 10 GΩcm

Tab. 6.1: CMS specifications for Outer Tracker strip sensors.

6.4 Procedure for sensor batch acceptance

As mentioned in 5.3, every produced sensor undergoes the Vendor Quality Control which acts as a first-order qualification. HPK performs I-V and C-V measurements on every sensor and delivers to CMS only those sensors which meet the requirements. An example of an I-V and C-V measurement of a 2S batch performed by HPK is given in Fig. 6.20. HPK tests all sensors up to 1 kV for the I-V and up to 400 V for the C-V measurement.

The SQC workflow aims to characterize a minimum of 10% of a batch with an I-V and C-V measurement while a 5% of the batch sensors undergo a full characterization, including in addition to an I-V and a C-V, a measurement of the strip and interstrip parameters. Therefore, for a typical 2S batch of about 45 sensors, 5 sensors undergo an I-V and C-V measurement while 3 additional sensors are fully characterized. For a PS-s batch, the number of sensors that go through a full measurement is 5 due to the larger number of sensors included in the batch (section 5.2). The above numbers are the minimum requirement of testing for a batch qualification. If problems are spotted on at least one sensor of a batch, the sampling rate increases in order to test a larger fraction. The selection of sensors relies on the I-V results from HPK. Typical

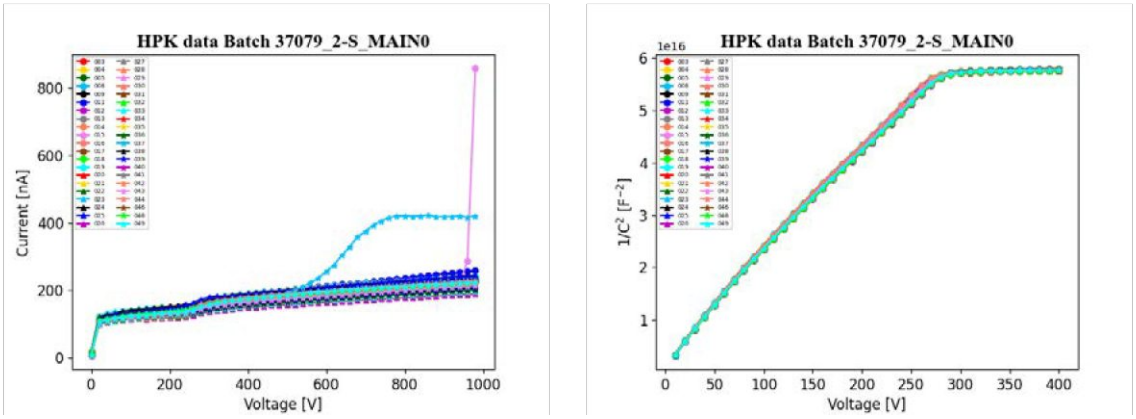


Fig. 6.20: I-V and $1/C^2$-V measurements of 2S batch with ID number 37079, performed by HPK.

candidates are sensors with larger total current that deviate from the average behavior of their batch (for instance sensor 037 in Fig. 6.20) or sensors with breakdown.

An optical inspection of the sensors is performed prior to a strip characterization. The sensor front side is inspected with the use of a microscope and during this process pictures of the sensor surface are taken with a camera. These pictures are used as a record and as a way to identify strip defects which can be visually spotted.

Figures 6.21, 6.22 are a comparison between the I-V and C-V measurements performed by HPK and HEPHY on the same sensors from batch 37079. Both sites performed the measurements at a similar temperature of 24°C, however, the relative humidity (RH) was different. The SQC measurements are conducted in an environment of RH $< 10\%$ while HPK claims to do the electrical characterization in RH $\simeq 40\%$. The I-V behavior of the 8 sensors, as tested at HEPHY, is similar or even better than the one shown at the HPK probe station. Sensor 037 exhibits a consistently elevated current on both tests while sensor 015 shows no breakdown at HEPHY. This improvement in the I-V behavior of sensor 015 might be associated with the different humidity levels since high relative humidity has an impact on the I-V, as discussed in section 7.3. The C-V measurements (illustrated as $1/C^2$ in Fig. 6.22) agree well.

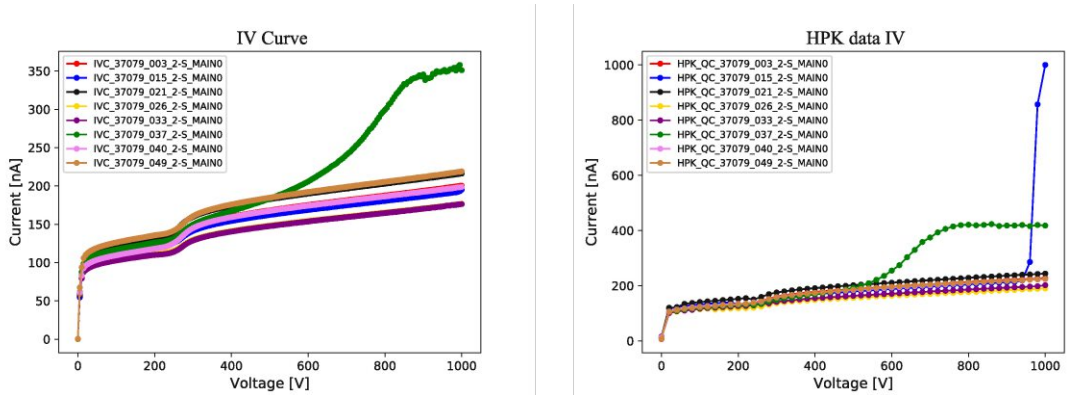


Fig. 6.21: Comparison between SQC (left) and HPK (right) I-V measurements of the same sensors.

The strip and interstrip measurements, in the way they are described in section 6.3, are performed only at CMS SQC sites. Over the first 6 months of production, the single strip

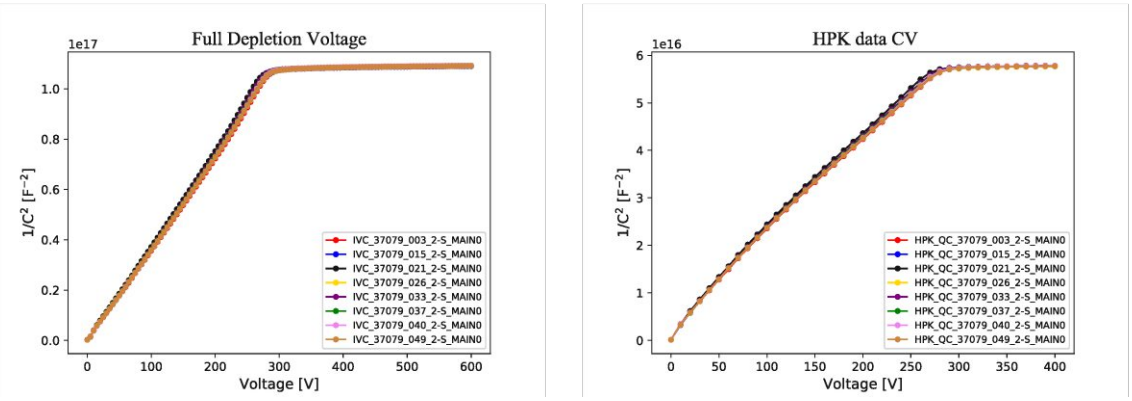


Fig. 6.22: Comparison between SQC (left) and HPK (right) C-V measurements of the same sensors.

parameters were tested on every strip while the interstrip parameters were measured on every 50^{th} strip. Since the overall quality of the sensors produced during this time was good, CMS decided to decrease the sampling rate to every 4^{th} strip for the single strip parameters since a negligible number of individual bad strips had been detected so far. In addition, the frequency for interstrip parameters increased to every 15^{th} strip because a few issues with the isolation had been observed. This testing rate is sufficient to spot clusters of bad strips which violate the CMS specifications. In case a region of problematic strips is detected, each strip of that cluster of strips is measured.

Figure 6.24 illustrates the strip and interstrip parameters as measured across the full sensor for three samples from batch 37079. At HEPHY, the one bank of strips (1-1016 for 2S and 1-960 for PS-s) is characterized at the edge pads which are near the bias resistors (Fig. 4.10) while the second bank of strips is measured at the central pads (Fig. 6.23). All parameters are well within the specifications and relatively uniform over a full sensor.

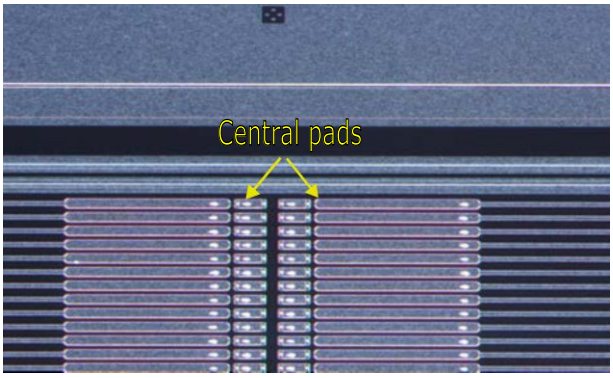


Fig. 6.23: Picture of the central pads of a 2S sensor.

The strip leakage current shows an increase over the first 100 strips for all the tested sensors in Fig. 6.24. This effect is consistent in every SQC measurement performed at HEPHY, it is not a feature of the strip sensors but rather a setup-related issue. The electrometer which measures the strip current is constantly turned on, also when no measurement is performed, therefore this should exclude a device warm-up effect. Another scenario would be that the increase in the leakage current could be correlated to an increase in the temperature inside the probe station. However, this observed gradual increase of the strip leakage current is reproducible also after a

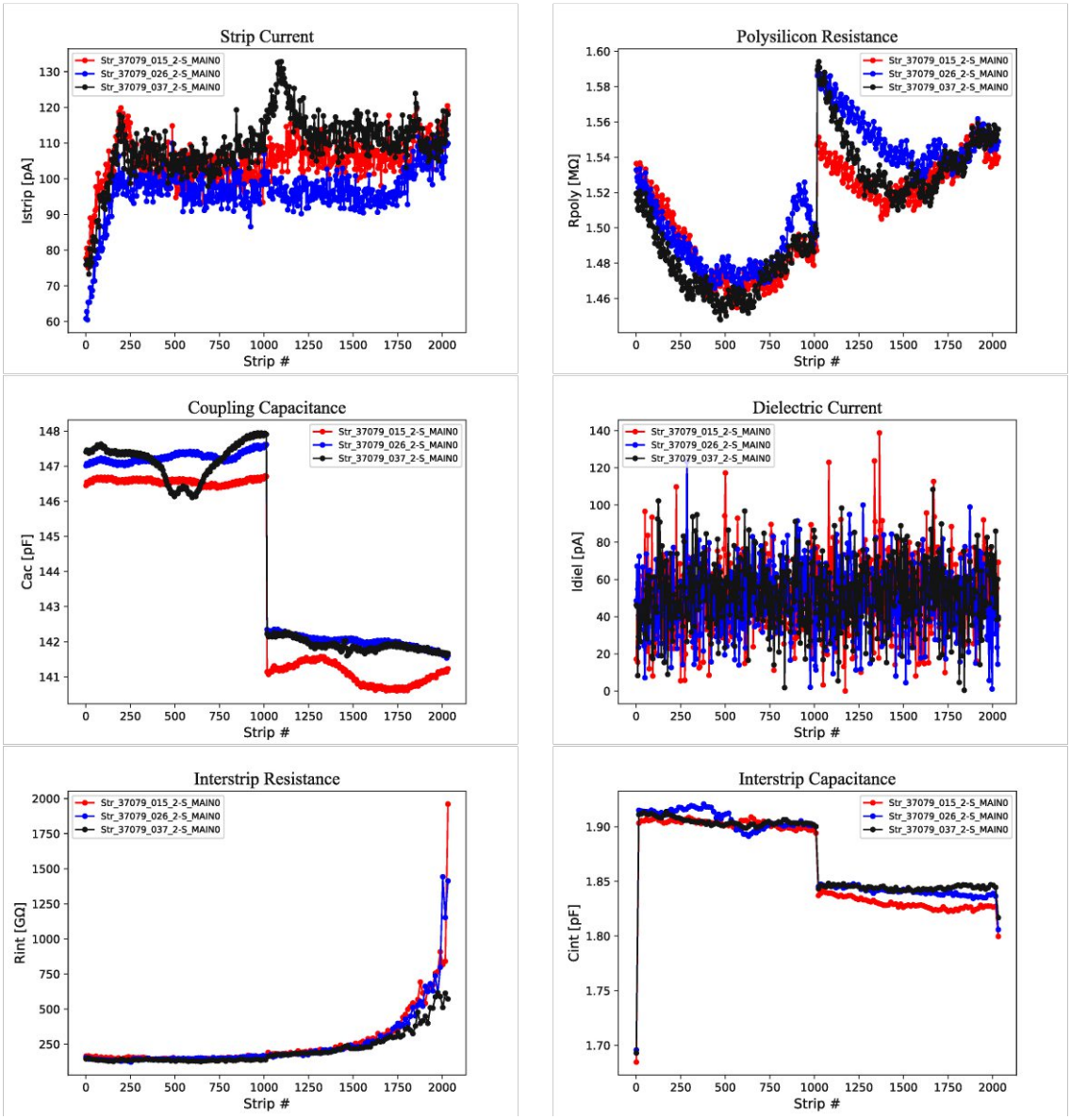


Fig. 6.24: Strip parameters across 3 production sensors from batch 37079.

full measurement (which lasts about 6 hours). After this time, the temperature of the probe station is stable. A more thorough investigation of the source of this effect (such as whether this could be a contribution of the chuck) would require a partial disassembly of the setup which was not possible during the mass production phase.

The polysilicon resistance measured at the central pads include also the resistance of the strip implant which is connected in series to the bias resistor. In section 8.2.5, it is given that the mean sheet resistance of the strip implant measured to date is $R^{n+}_{sheet} = 34.83 \pm 0.50\ \Omega$/sq. Figure 6.25 shows the R_{poly} for the measured strips of a PS-s sensor, with the strips illustrated in red to be characterized at the edge pads and the strips in blue to be measured at the central pads. The same strips were measured. Subtracting the polysilicon resistance values measured at either side of the strip gives the strip resistance. For a PS-s strip with a length of 2.3 cm and a width of 25 µm, the mean strip resistance is 32.04 kΩ, assuming the mean strip sheet resistance of $R^{n+}_{sheet} = 34.83\ \Omega$/sq. Figure 6.26 shows the distribution of the strip resistance of the tested PS-s sensor as

the difference between the two measured resistances. The mean strip resistance of the sensor is 29 kΩ.

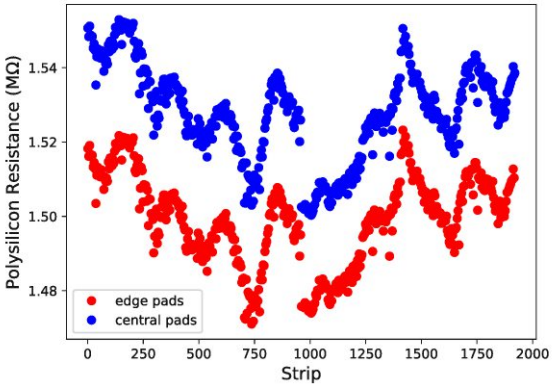


Fig. 6.25: Polysilicon resistance across a PS-s sensor as measured at the edge pads (red) and central pads (blue) of the same strips.

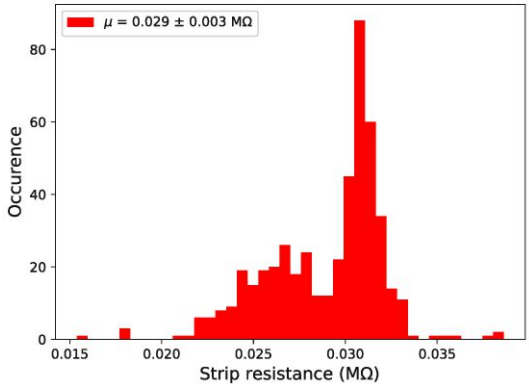


Fig. 6.26: Distribution of strip resistance extracted as the difference between the resistance measured at each end of the characterized strips.

The interstrip resistance shows a different trend and higher values when measured at the central pads than when measured at the edge pads. The reason for this different behavior is not fully clear. Figure 6.27 illustrates the R_{int} across a PS-s sensor measured at the edge pad (red) and at the central pad (blue) of the same strips. The I-V ramp of an arbitrary strip selected from each of the two curves of Fig. 6.27 is shown in Fig. 6.28. As long as the resistance is high enough and the measurement can sufficiently detect regions of low interstrip isolation (examples in section 7.2), the observed discrepancies due to different measurement configurations are not an issue.

The last part of SQC includes a long-term biasing at 600 V for a minimum of 3 sensors per batch, in an environment of controlled and fixed temperature and humidity. Figure 6.29 shows the total current behavior of three sensors from batch 37079 as evolves over more than 48 hours. The sensors were tested inside the climatic chamber, biased at 600 V in a stable temperature of 20°C and a stable relative humidity of 5%. All sensors behave well over time with the total current being constantly low and stable with a tendency to decrease.

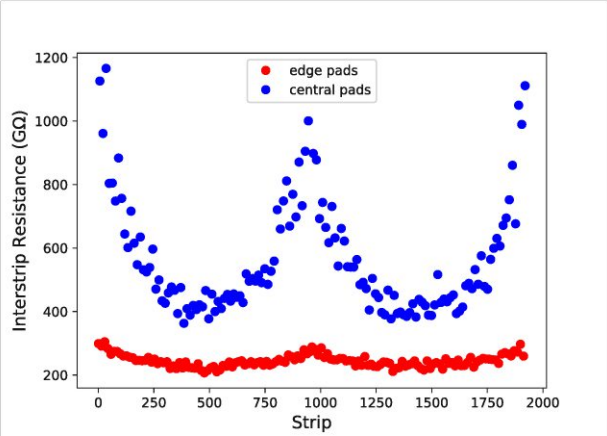


Fig. 6.27: Interstrip resistance across a PS-s sensor measured at the edge pads (red) and at the central pads (blue) of each characterized strip.

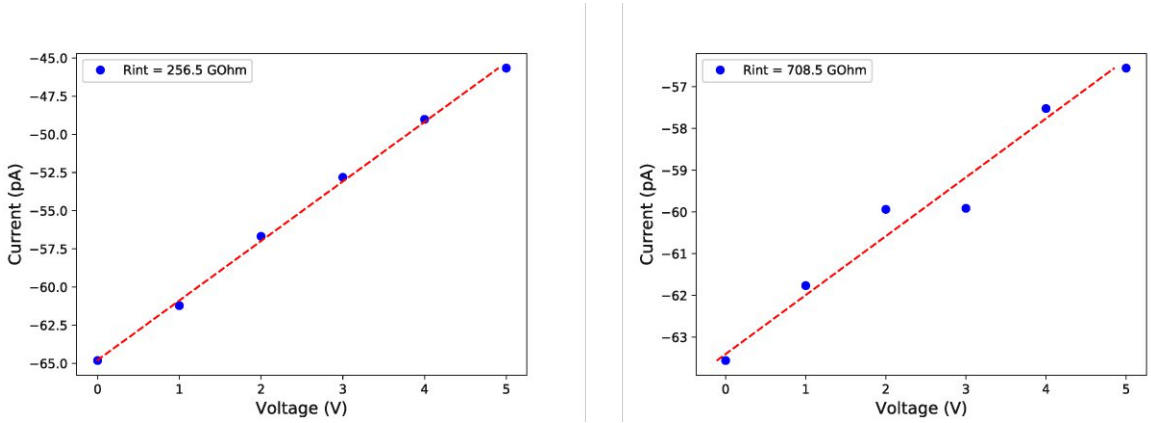


Fig. 6.28: I-V ramp for the extraction of interstrip resistance from two arbitrarily selected strips, one measured at the edge pad (left) and one measured at the central pad (right).

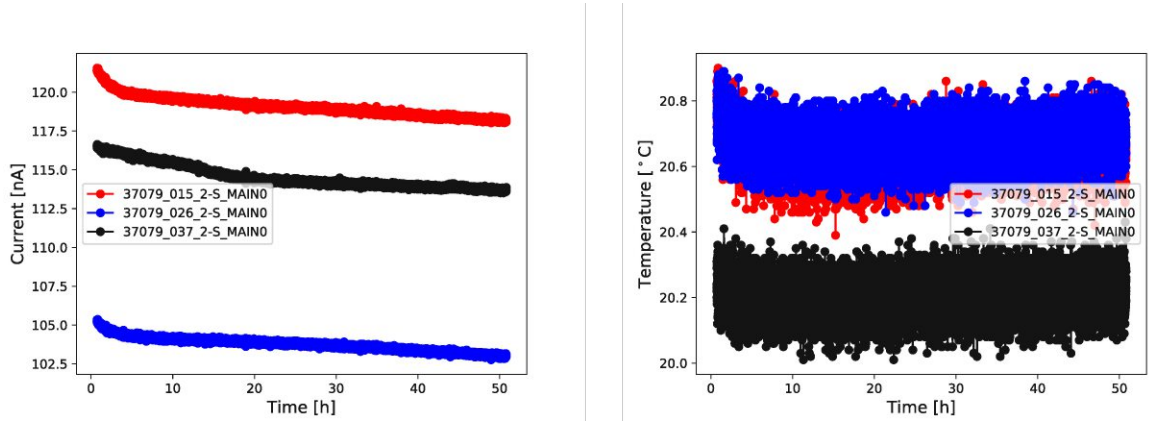


Fig. 6.29: Total current (left) and temperature (right) evolution of three tested sensors over 50 hours at 20 °C and RH = 5%.

Chapter 7

Dependence of sensor electrical behavior on external conditions

During the characterization of the sensor electrical parameters over the first three years of production, several observations were made regarding the influence of external factors on the electric behavior of the Outer Tracker sensors. Environmental conditions such as high relative humidity can potentially deteriorate the properties of the sensors, as discussed in section 7.3. The impact of long exposure to high humidity on the Outer Tracker sensors becomes more crucial during module assembly due to the duration of this procedure. Apart from humidity, other kinds of external influences, such as electrostatic charges have shown to affect the electric behavior of the production sensors, as discussed in section 7.2.

The set of studies included in this chapter investigates the response and resilience of the Outer Tracker production sensors against humidity and electrostatic charge-up. In addition, mitigation techniques are examined and based on them, a set of recommended lab procedures for the recovery of the affected sensors is provided.

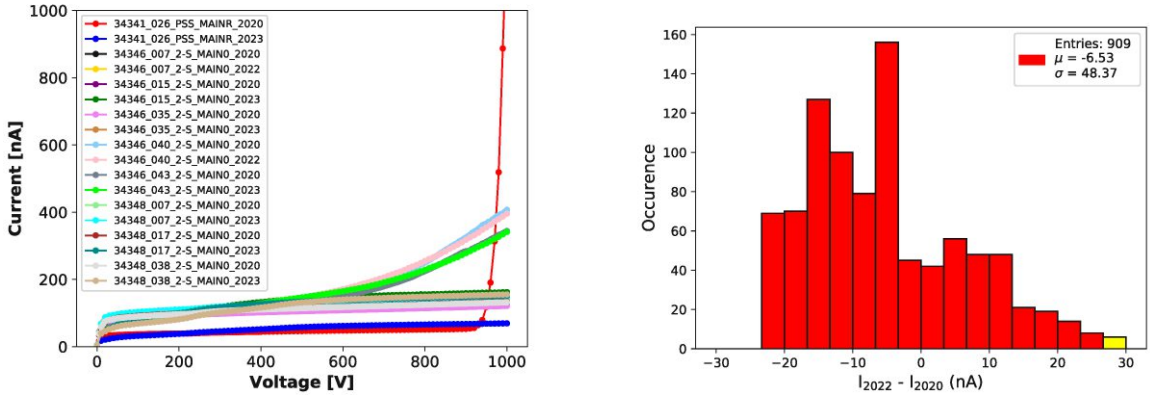
7.1 Shelf-life test

As described in section 5.2, the batches of the production sensors arrive at CMS centers in vacuum-sealed boxes. After breaking the seal, the boxes are placed inside a dry cupboard until the qualification of the batches which are included is complete. In sequence, the boxes are stored vacuum-sealed in conventional cupboards until they are dispatched to the module assembly centers. The vacuum packaging should ensure that no chemical reaction occurs between the sensors and the external environment over the time of storage. Therefore, the shelf-life of an unirradiated sensor should be indefinitely long and the sensor parameters should not alter with time.

The shelf-life test includes a remeasurement of a few samples that have been previously qualified in SQC and then stored vacuum sealed. Sample measurements on the batches that were delivered to CMS in 2020 were performed by all SQC centers. This section presents only data collected by HEPHY.

An example of the I-V data collected during the shelf-life test is shown in Fig. 7.1. All I-V measurements were performed at a similar temperature of 24°C, nonetheless, the currents are scaled to 20°C to facilitate the comparison. Figure 7.1a shows the I-V plots of each sensor measured in 2020 and in 2022 while the distribution of the ΔI (I_{2022} - I_{2020}) is shown in Fig. 7.1b. The ΔI refers to the difference of the two measured currents for each bias voltage and each different sensor. The raw data (negative currents) were used for the subtraction, thus a positive ΔI means that the total current of a sensor in 2020 was larger than the measured current in 2022. For the majority of the sensors, it is -25 nA $< \Delta I <$ 25 nA. As it can be seen in Fig. 7.1a, the sensor 34341_026_PSS_MAINR had initially a breakdown beyond 900 V in 2020 which

was not reproduced in the next I-V measurement after about 2 years. This improvement of the I-V behavior seems to be related to the presence of moisture remnants on the surface of the sensors which slowly dissipated in the moderately low relative humidity environment in which the sensors were stored between the two measurements.



(a) Comparison of I-V curves. **(b)** Histogram of I_{2022} - I_{2020}.

Fig. 7.1: I-V curves of 9 production sensors as measured before and after more than 2 years in dry storage conditions.

In the scope of this study, the behavior of the strip and interstrip parameters was also investigated. An example is shown in Fig. 7.2, in which one of the sensors from Fig. 7.1 is fully characterized and compared with its initial measurement. As discussed in section 6.1.3, HEPHY switched to new software for the SQC measurements since the summer of 2022. The initial measurements were conducted with the old software. In addition, the measurement sampling rate was different between the two runs. In the run of 2022, every 4^{th} strip was characterized (every 15^{th} for the interstrip measurements) while in the run of 2020, each single strip was measured (every 50^{th} for the interstrip measurements). All parameters except interstrip capacitance show consistency after 2 years of storage. The two strips with higher leakage current spotted in 2020, were not measured in 2022 due to the different sampling rate. The interstrip resistance remains sufficiently high, exceeding 150 GΩ. Regarding the interstrip capacitance, since this measurement was not performed correctly at HEPHY during the first 6 months of production, there is no data to compare. Nevertheless, the interstrip capacitance, as measured in 2022, follows the typical trend observed in other 2S sensors, with the values being within the typical range. All in all, no evidence of any change either in the global or in the strip parameters has been detected to date.

Based on the results from the shelf-life test, there is no evidence implying that the quality of the production sensors deteriorates with time due to improper conditions of storage. Data collected by other SQC centers is consistent with the observations at HEPHY and supports the above statement.

7.2 Electrostatic charge-up issues

Around the end of the first year of production, several delivered batches showed a degradation of their quality with many sensors failing to pass the CMS specifications. Sensors with initially good I-V behavior when tested by HPK, showed a deterioration in their current-voltage behavior when tested by CMS. No visual damage on the surface of the sensors was spotted. An example is

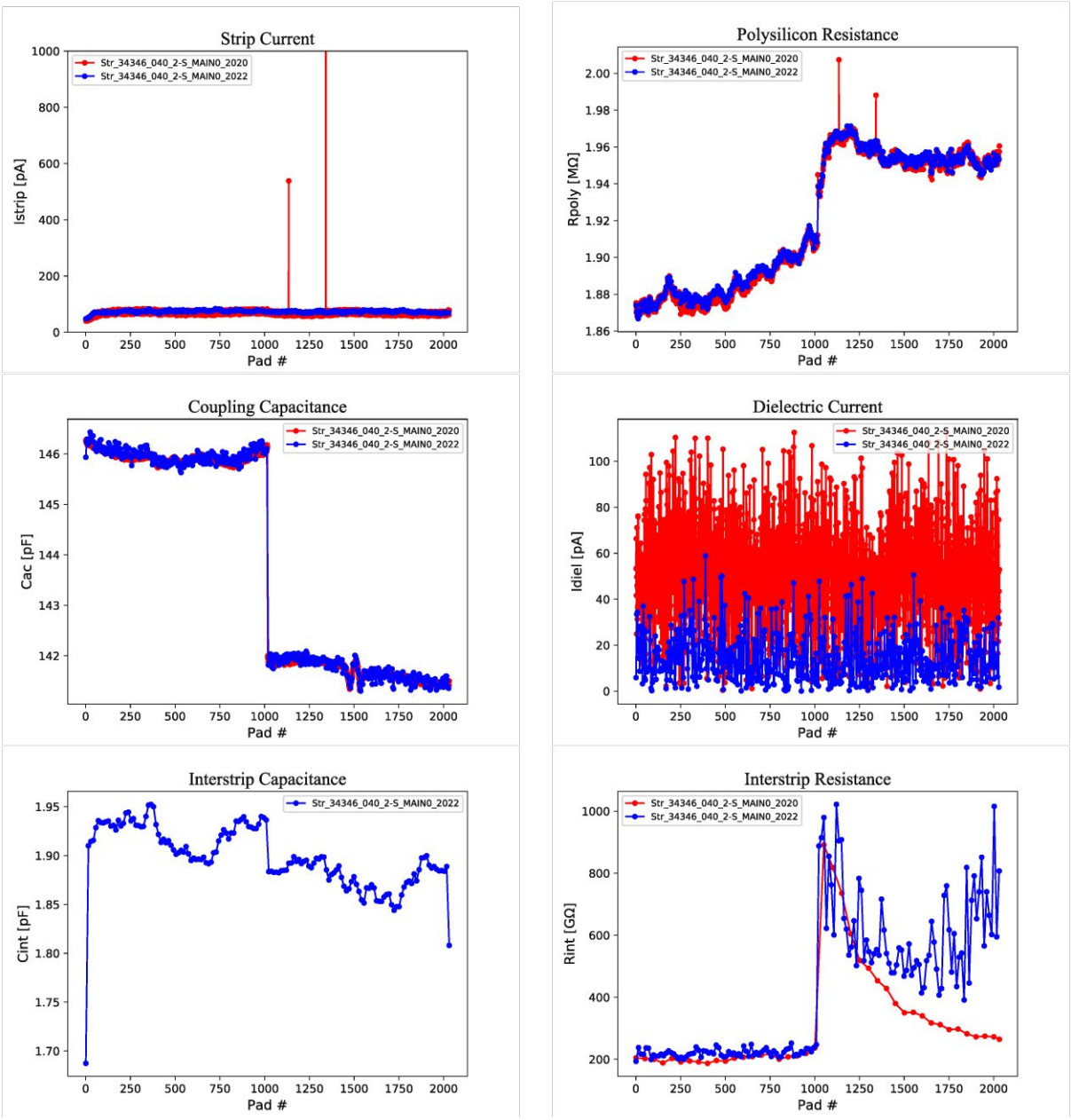


Fig. 7.2: Comparison of strip parameters as measured in 2020 and in 2022.

given in Fig. 7.3. In addition, problems were observed on specific strip and interstrip parameters, such as the low interstrip (R_{int}) and bias resistor (R_{poly}) values which were found (Fig. 7.4). The regions of strips which violated the specifications among different tested sensors were consistent with the region of the sensors contacted by the vacuum pick-up tool. The ESD-safe vacuum tool is applied to the sensor to pick it up and place it on the chuck of the probe station. Similar problems were observed by other CMS centers [79]. With the use of an electrostatic field meter [80], the potential generated by the electrostatic charges was measured. A strong concentration of charges on the surface of the passivation was detected, with a measured voltage up to 300 - 400 kV, as shown in Fig. 7.5a. The measurements with the electrostatic field meter were performed before the application of the vacuum tool. In addition, positive charges were measured on the plastic sheet which is placed atop the front side of each sensor (Fig 7.5b). Sensors from the first

months of production were also tested but negligible potential was measured by the electrostatic field meter. This indicates that a change occurred in one of the processes followed by HPK. At HEPHY, electrostatic charge-up issues were detected for the first time in batch with ID number 37906 (Fig. 5.6).

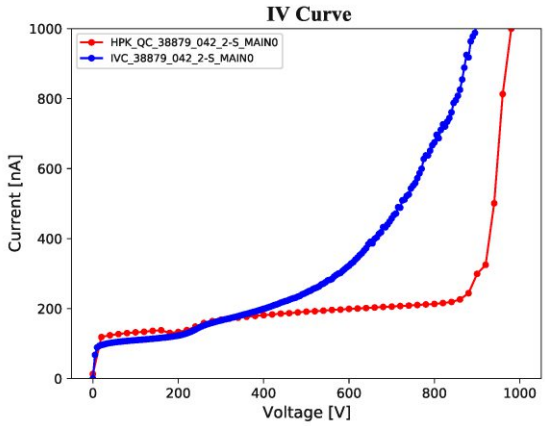
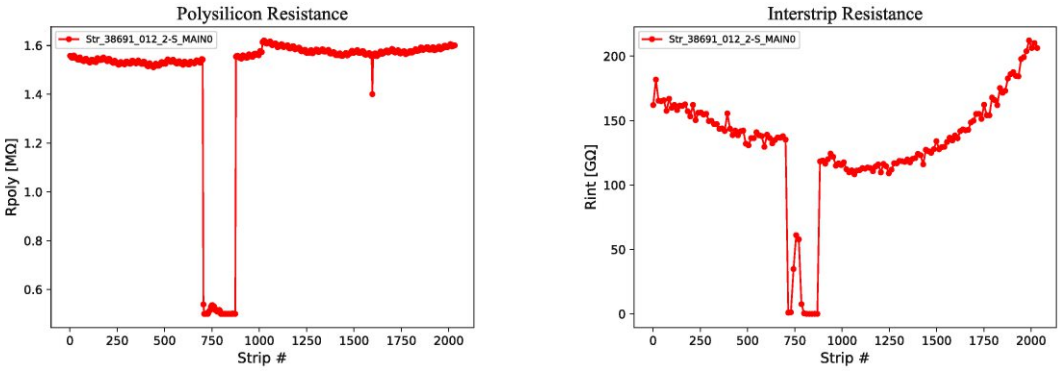


Fig. 7.3: I-V of sensor suffering from charge up. The comparison with HPK data shows a clear increase in total current after charge-up and a shift of the breakdown to lower voltage.



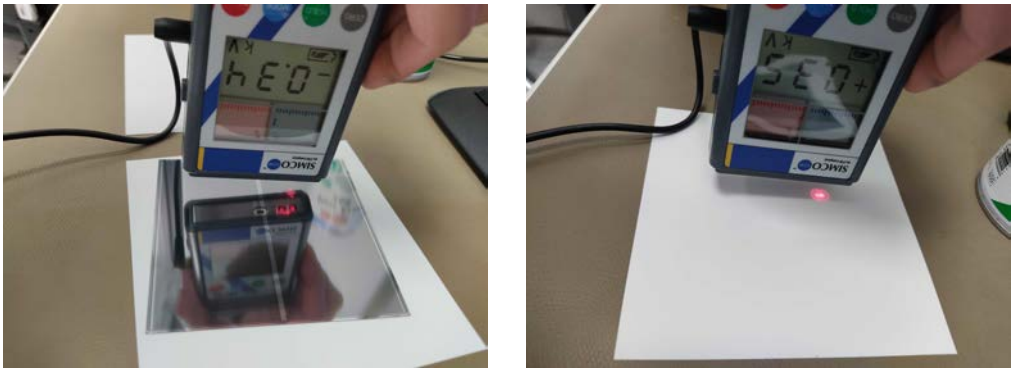
(a) R_{poly} over strip number

(b) R_{int} over strip number

Fig. 7.4: Example of sensor with strong charge-up problems. The area of strip clusters with low R_{int} and R_{poly} correlates to the region which was contacted by the vacuum pickup tool.

Similar issues were observed by ATLAS ITk as discussed in [81]. After reporting this issue to HPK, the vendor confirmed that electrostatic charges are created from the packaging material. The card material does not prevent the occurrence of the triboelectric effect which, through the friction between the sensor and the card, enables the transfer of charges from the card to the surface of the sensor. This explains the observations shown in Fig. 7.5. Since this packaging material has been used for a large fraction of the production, it is assumed that the majority of the delivered sensors should feature similar issues.

The presence of static charges on top of the sensor passivation does not inflict permanent damage but it deteriorates its properties and hinters the qualification process since cluster of strips of the affected sensors violates the specifications. Figure 7.6 shows the measured voltage



(a) Measurement on the sensor surface **(b)** Measurement on top plastic card

Fig. 7.5: Measurement of the electrostatic potential of the sensor surface (left) and of the top plastic card (right) with a SIMCO electrostatic field meter [80]. The measurement of a voltage equal to −340 V indicates the strong presence of charges.

across a PS-s sensor with charge-up issues. The voltage was measured manually with the use of the electrostatic field meter. Although the charges are distributed over the whole outer side of the passivation layer, the effect becomes more pronounced in the regions touched by the vacuum pen. This case is shown in Fig. 7.4a, 7.4b, where a 2S sensor with charge-up issues was tested. The application of this tool on the surface of the sensor seems to concentrate the charges locally on this region and maximize their impact. An impact of the pick-up tool on the sensor electrical properties was observed for the first time in tests of early produced PS-p sensors, conducted by one CMS center [79]. The effect was minor and mostly visible on the pixel leakage current heatmap. These measurements were performed a few months before the effect of charge-up was spotted for the first time by CMS. Nevertheless, this observation is indicative of the impact that the suction cup of the vacuum tool can introduce on the electrical measurements of the sensors. In principle, the tip of the vacuum tool which is applied on the sensor is made of a conductive material. When it is used by a grounded operator, it should allow for the dissipation of the charges from the vacuum tip to the ground.

Modification of the testing procedures could be done in order to mitigate the impact of the charge-up in the sensor qualification, such as refraining from using the vacuum pen or grounding the vacuum tip while applying this tool on the sensor surface. Ideally, a strategy to completely dissipate the electrostatic charges from the surface of the sensors would be required.

The mechanism which connects the presence of external negative charges on the outer surface of the passivation to the loss of interstrip isolation has not been yet well understood. Observations related to the impact of electrostatic charges on the interstrip parameters are discussed in [82], [83], [84]. Similar observations with loss of interstrip isolation due to external negative charges have been made in p-on-n sensors [84]. The interstrip region can be emulated by a MOSFET structure, as discussed in section 8.2.4. The gate voltage which controls the conductivity of the source to drain channel of the MOSFET can be compared to the potential created by the electrostatic charges on top of the passivation of the sensor. A pMOSFET (p-type drain and source on a n-type substrate) is switched on when a negative voltage larger than the threshold voltage is applied to the gate (section 8.2.2, 8.2.4). As a result, an inversion layer with a conductive channel of holes is formed between the source and the drain. In the presence of negative external charges on the outer side of the passivation of a p-on-n sensor, a similar "p-channel" inversion layer can be formed due to the potential created by these charges. This can result in an ohmic cross-talk between two adjacent strips and a loss of interstrip isolation. In the

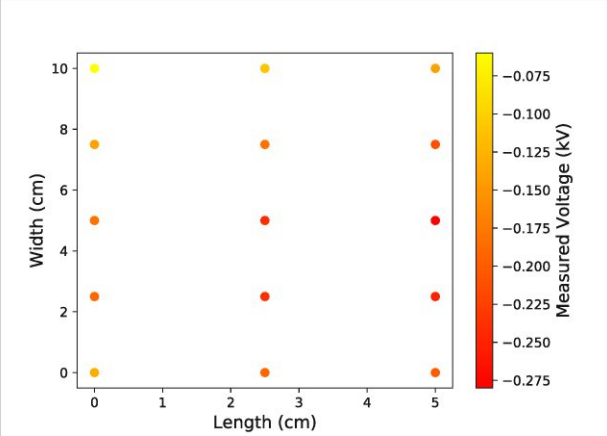


Fig. 7.6: Distribution of measured potential across a charged-up PS-s sensor. The coordinate (0,0) corresponds to strip 1.

case of a nMOSFET, the channel between the source and drain becomes conductive (n-channel) if a positive voltage larger than the threshold voltage is applied to the gate. An inversion layer of electrons is formed between the source and the drain. However, in the presence of external negative charges on the passivation, the formation of a conductive channel of electrons between the strips can not be explained by this approach in which a comparison to a MOSFET is done. The assumption that can be made is that the external negative charges create an additional electric field which changes the distribution of the field in the interstrip region and therefore impacts locally or disrupts the isolation that is provided by the presence of the p-stop. More detailed studies and simulations will be needed in order to understand the mechanism which creates this effect.

Charge dissipation techniques

The charge-up is a persistent but reversible effect. A mitigation strategy which can efficiently dissipate the charges from the surface of the sensors is needed. High levels of humidity in the environment can facilitate the dissipation of the charges through the more humid air. Exposing the sensors to the environment of the ESD-safe clean room until the sensor is fully discharged could be one solution. However, this method has two drawbacks. First of all, it can be very time-consuming since up to several hours might be needed for the dissipation of the charges [84]. An example is illustrated in Table 7.1 in which two sensors are exposed to the environment of the clean room (relative humidity about 40%) for 90 min. The sensors were put out of their envelope and an initial voltage of −200 V was measured for sensor 46801_010 and −150 V for sensor 46809_008. The measured potential decreases with time and after 90 min the largest fraction of charges dissipated. Charged-up sensors with a measured voltage below -30 V do not typically show problems with the interstrip isolation during testing, according to the experience collected at HEPHY. The required time for a full charge dissipation varies among different sensors, it depends primarily on the amount of initial charges. Several minutes are required for the discharge which makes this method not efficient in terms of time. The second disadvantage of this method becomes clear in section 7.3.2. The longer the exposure of a sensor in the humid environment of a clean room, the higher the probability of experiencing problems with its HV stability due to the impact of high relative humidity.

An alternative strategy which is widely used in industry, is the utilisation of ionization devices for the removal of static electric charges. Such an example is a commercial ion blower or ion fan

Sensor	0 min	15 min	30 min	45 min	75 min	90 min
46801_010_2-S	-0.20kV	-0.11kV	-0.09kV	-0.09kV	-0.08kV	-0.06kV
46809_008_2-S	-0.15kV	-0.06kV	-0.03kV	-0.03kV	-0.01kV	-0.01kV

Tab. 7.1: Measured electrostatic potential on the surface of the samples over time.

[85]. The ionizing air fan produces an air flow rich in ions which when directed to the surface of an object, neutralizes the static electric charges. The positive effect of the ion blower was verified with the electrostatic field meter, where an initially charged-up sensor showed negligible voltage across its surface after the application of the ion blower for about 5 minutes. Figure 7.7 shows one example of two sensors with clusters of low R_{poly} and R_{int} values due to charge-up which, after the use of ion blower for about 20 minutes, recovered fully. The duration of the process as well as the relative distance between the ionizing device and the sensor are important for maximum efficiency. The use of an ion blower has been included in the standard CMS quality control procedures and many centers, including HEPHY, have integrated the device into their SQC probe station. A relative distance about 20 - 25 cm is preferable, based on the experience at HEPHY, but this depends on the specifications of the ion blower and the space limitations that each probe station has. The typical process at HEPHY is to use the ion blower, which is placed about 25 cm above the sensor, for about 5 to 10 minutes before any measurement is conducted. It should be noted though, that the duration of this process might vary among different probe stations.

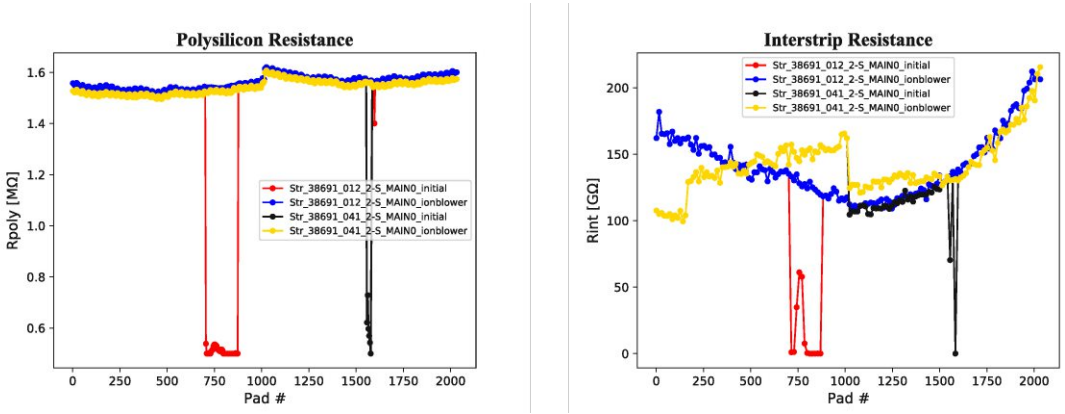


Fig. 7.7: Example of R_{int} and R_{poly} of 2 sensors before and after the use of ion blower. The regions of low values recovered fully after blowing the sensor with ionizing air for a few minutes.

The problems introduced by the electrostatic charges might become more pronounced in the quality assurance process, nevertheless it is an issue that should concern the module centers as well. It is not certain at which level the presence of electrostatic charges on the surface of the sensors can impact or even harm the modules. Since the sensors after testing are put again inside the envelopes, it is certain that they can get recharged with the same mechanism which produced the charge-up in the first place. In addition, SQC qualifies only a fraction of the delivered sensors, the rest of which will be I-V tested for the first time by CMS, at the module assembly centers. The assumption should be that almost every sensor which will be assembled into a module shows potential charged-up issues. Since ESD safety is of major importance for the module assembly

Fig. 7.8: Picture of a SIMCO-ION mini ion fan used at HEPHY [85].

procedures, precautions against this effect, such as the use of ionizing devices, should be taken also by the module centers.

7.3 Humidity studies

Previous studies [73], [86], [87] have shown that high relative humidity can impact the electrical behavior of silicon sensors and deteriorate their HV-stability. The sensors are tested in SQC in low relative humidity conditions in order to minimize any potential influence of moisture. The Outer Tracker sensors must go through several module assembly steps during which they are exposed to the humid environment of ESD-safe clean rooms for several days [75]. Although the sensors feature a SiO_2 passivation layer which protects the silicon bulk from the interaction with the external environment, any weak spots in this layer can trap moisture. In this case, the weak spots can form conducting channels in the oxide which decreases its dielectric breakdown strength and as a consequence, its high-voltage stability.

The impact of humidity on the Phase-2 Outer Tracker sensors is investigated in this section, under two different scenarios. The first part examines the dependence of the breakdown voltage on humidity. The second part focuses on the effect of long exposure to humidity on the HV-stability of the sensors. In addition, a recovery strategy is investigated for the sensors which show a persistent deterioration of their I-V behavior due to humidity.

7.3.1 Impact of humidity on electrical behavior of sensors

In the scope of this study, the electric response of 18 production sensors to different relative humidity levels was investigated. The sensors come from 6 different production batches and feature larger than the average currents of their respective batches. The assumption is that these sensors are more susceptible to the impact of humidity and therefore, this study represents a worst-case scenario. The sensors were tested inside the climatic chamber of HEPHY. The I-V curves of the 18 tested sensors are shown in Fig. 7.9 which compares the SQC to HPK results. The measurements were performed in similar temperatures, between 24 to 25°C but at different humidity levels. The relative humidity in the SQC probe station was below 10% while HPK performed the measurements in a relative humidity of 40%. None of the 18 sensors see a breakdown below 800 V. Sensor 46810_041 shows higher current than HPK data which is

attributed to a long scratch on its surface created after the HPK measurement and prior to the SQC test.

Before the test, all sensors had been biased at 600 V for 48 h in an environment with a temperature of 20°C and relative humidity of 5%. The testing procedure included a variation of relative humidity from 20% to 50% with a stepsize of 10%, at a fixed temperature of 20°C. For every humidity set point, an I-V measurement was conducted. Figure 7.10 summarizes the results. Two sensors have a breakdown already at 30% humidity while the I-V behavior of the rest is unaffected up to 40%. At 50% about half of the examined sensors feature an electric breakdown below 600 V. The I-V of the scratched sensor is affected in a minor way by humidity.

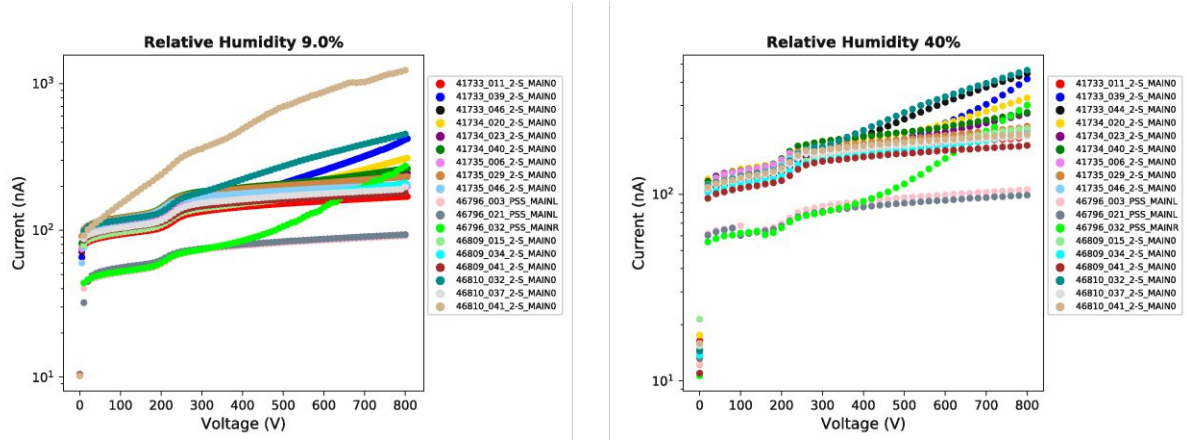


Fig. 7.9: IV curve of 18 tested production sensors at SQC (left) and at HPK lab (right). The measurements were conducted in a similar temperature of 24 - 25°C, while the relative humidity in the HEPHY probe station was below 10% and in HPK probe station about 40%.

As it can be observed in Fig. 7.10, the sensors which are included in this study (worst-case scenario), become more prone to experience HV-instabilities at relative humidity above 40%. Their response to high relative humidity varies. Some sensors show no impact even up to RH = 50%, while others are strongly affected at 50% or lower. It should be noted that the relative humidity in the ESD-safe clean rooms, where the sensors undergo all module assembly processes, is typically 40 - 50%. Therefore, any potential impact of humidity on the sensor's electrical behavior becomes more probable during the module assembly phase. The sensor testing is performed in a dry environment as explained in section 6.4 in order to minimize this effect. Also, the impact of humidity on the sensors during operation in the CMS detector is of no concern because the Tracker is constantly flushed with dry air in order to avoid condensation due to the low temperature of operation.

7.3.2 Impact of long-term exposure to humidity and recovery procedure

The second study investigates the electric response of the production sensors after long-term exposure to a humid environment. Trapping of moisture in the weak spots of the passivation layer can lead to a persisting deterioration of the HV-stability of the device until the humidity is completely evaporated from the sensor surface. The following case study is motivated by the module assembly procedures during which thousands of sensors are exposed to the ambient conditions of the clean rooms for several days. It is crucial to acquire some knowledge about the

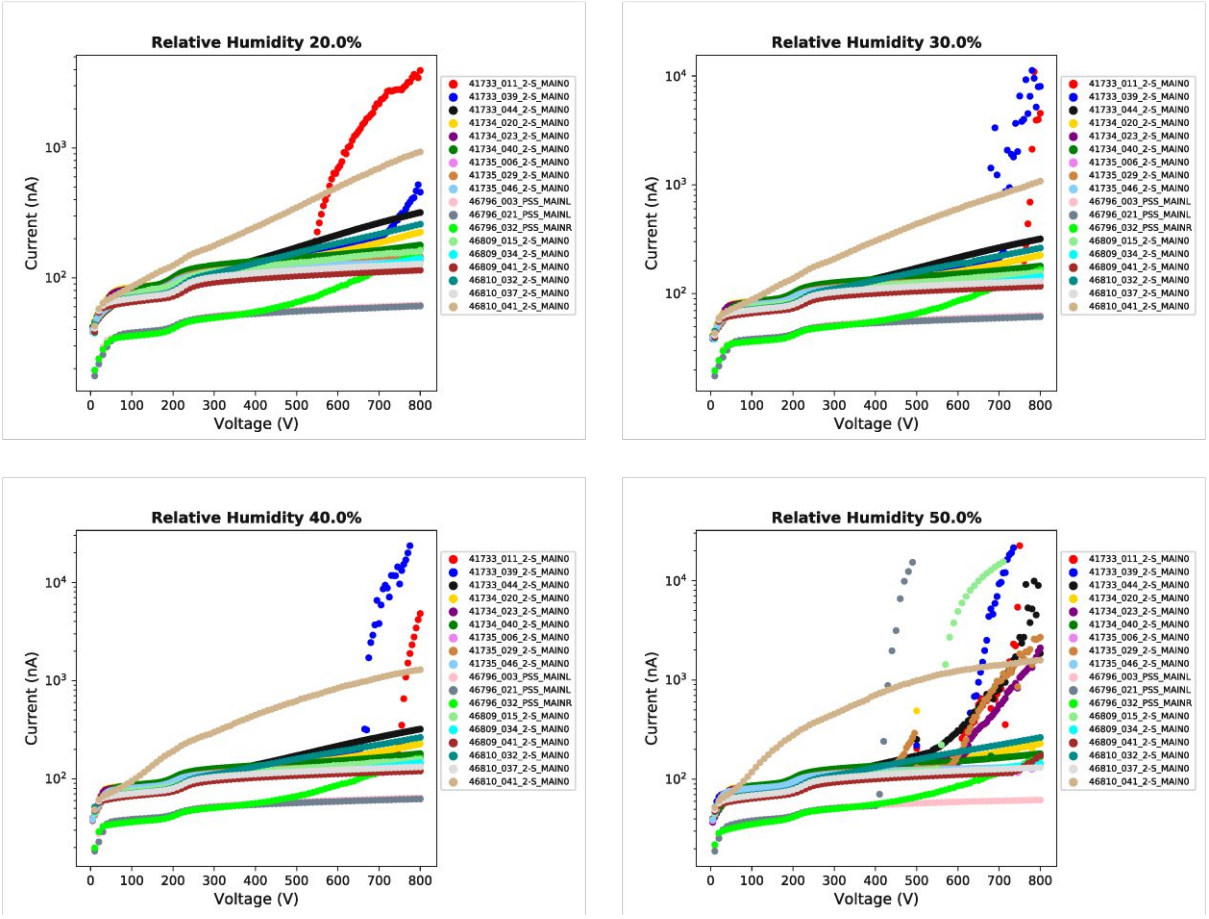


Fig. 7.10: IV curve of 18 tested production sensors at T = 20 °C, RH = 20, 30, 40 and 50%.

expected impact of environmental conditions on the electrical behavior of the sensors after long exposure to high humidity.

Sensors undergo an I-V measurement at several stages during module assembly, at a relative humidity equal to or lower than 20%. The study considers an extreme scenario, in which a sensor is exposed to RH = 50% for 60 h (equivalent to a full weekend). An I-V is conducted in this environmental condition, in sequence the humidity decreases to 20% and a new I-V measurement is performed instantly.

This study includes 45 production sensors tested under the same conditions inside a climatic chamber. The sensors belong to 15 different production batches and they show larger than the average total dark current of their batches. The selection is biased and hence, this study is an extreme scenario as these sensors represent the “worse” 5% from the production. Before the main test, all sensors were tested in an environment with a temperature of 20°C and 5% relative humidity. A reference to their initial behavior was acquired. The I-V curves are illustrated in Fig. 7.11.

The sensors were exposed to 50% relative humidity and T = 20°C for 60 h, and then a current-voltage measurement in the same environmental conditions was performed. The results are shown in Fig. 7.12. About half of the sensors see a breakdown below 800 V, for most of which the steep current increase starts below 600 V. However, the other half of the samples is unaffected and shows resilience against high humidity.

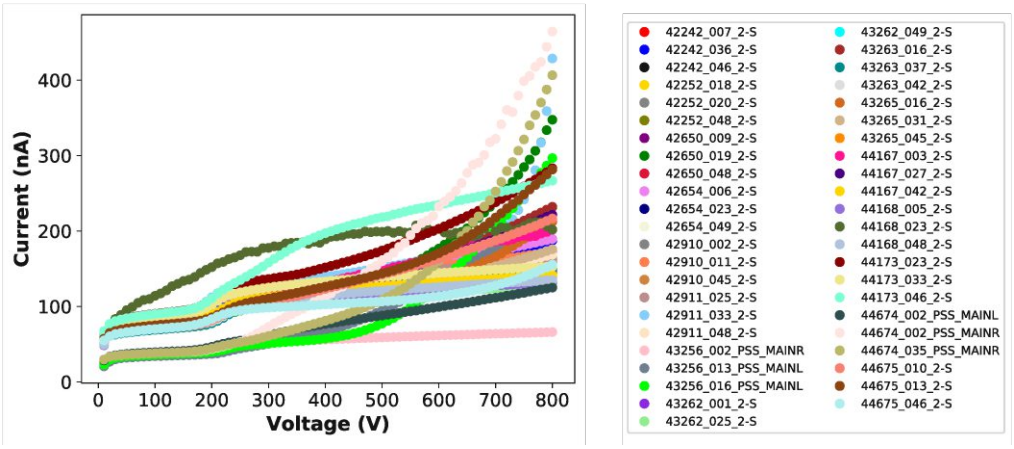


Fig. 7.11: Initial I-V curve of 45 tested production sensors at T = 20°C, RH = 5%.

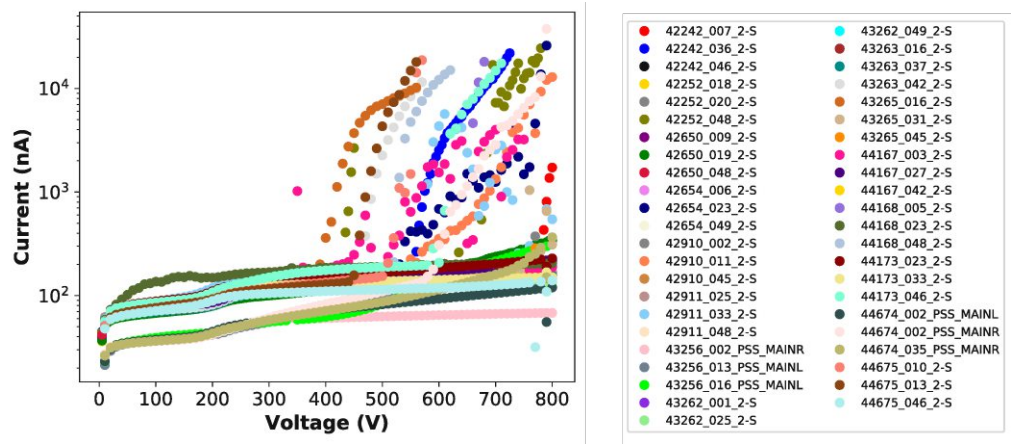


Fig. 7.12: I-V curve of 45 production sensors after an exposure to RH = 50% and T = 20°C for 60 h. The measurement was performed in the same environmental conditions.

As a next step, the relative humidity was set to 20% followed instantly by an I-V measurement. The electric behavior of the sensors is illustrated in Fig. 7.13. The majority of sensors with a breakdown at RH = 50% recover at 20%. Nonetheless, about 15% of the tested samples show a persisting breakdown below 600 V.

The first part of the test shows that a long exposure to high relative humidity can potentially deteriorate the I-V behavior of the sensors. Some of them might not recover immediately if a drier environment is established, such as a relative humidity of 20%, as shown in Fig. 7.13. It should be noted, that this is not a general statement concerning all the production sensors since this study is biased and represents an extreme case.

Recovery procedure

A recovery procedure for cases such as the sensors shown in Fig. 7.13 is required. Long-term biasing slightly above the breakdown voltage in a dry environment (this is also known as sensor training) is a method that is followed in this part of the test. After the I-V illustrated in Fig. 7.13, the sensors were biased slightly above the breakdown voltage in the same environmental conditions (T = 20°C, RH = 20%) for an hour. In sequence, an I-V measurement was conducted and the results are shown in Fig. 7.14. The combination of the training procedure with the

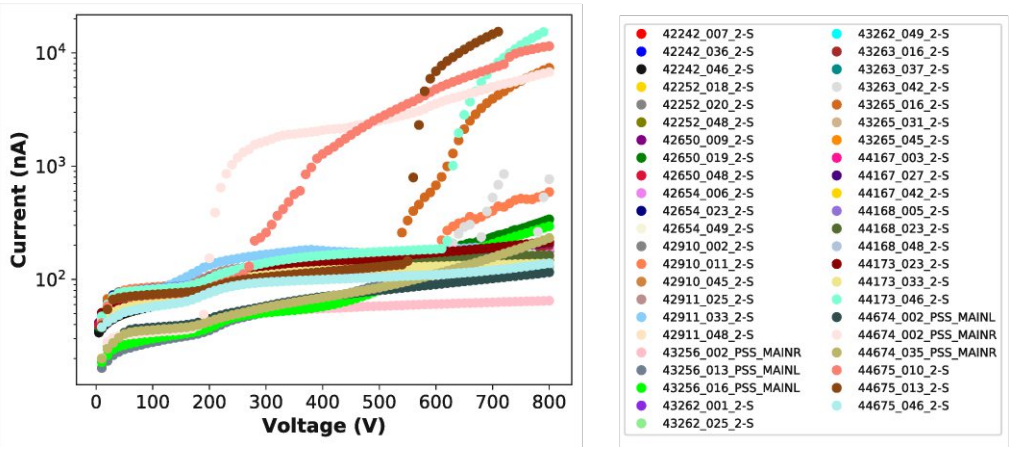


Fig. 7.13: I-V curve of 45 production sensors after an exposure to RH = 50% and T = 20°C for 60 h. The measurement was performed at the same temperature and a relative humidity of 20%.

longer exposure to the relatively dry environment of RH = 20% was beneficial for the sensors. The breakdown voltage vanished completely or shifted to higher values for most of the samples, however, it seems that more time of exposure under the same conditions was required for a few of them. A second observation is that two sensors, namely 42242_007 and 42242_046, showed a late response to humidity with a breakdown seen in the second I-V at RH = 20%, although it was absent in Fig. 7.13.

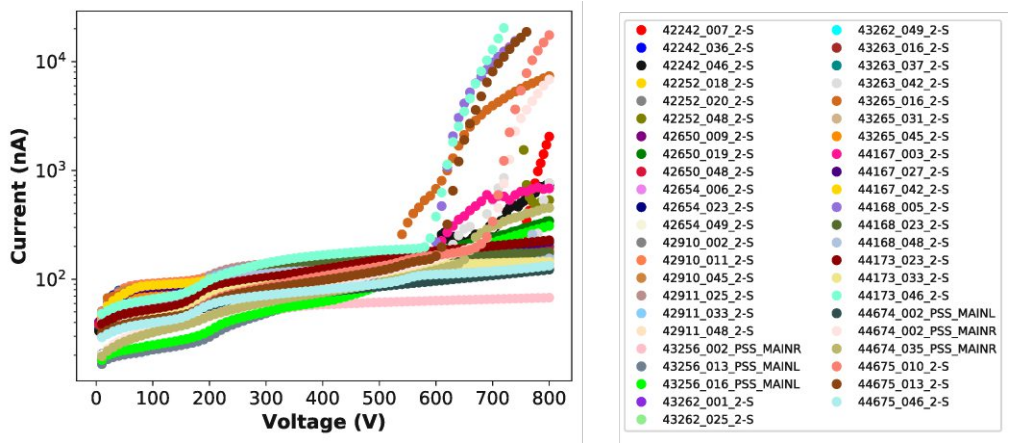


Fig. 7.14: I-V curve of 45 production sensors at RH = 20% and a temperature of T = 20°C, after an exposure to these conditions for an hour.

The recovery could be accelerated even more if the same procedure is followed in an environment of lower humidity. For the next step, the relative humidity was set to 5%, the sensors were biased slightly above the breakdown voltage for an hour and in sequence, an I-V was performed. The results are illustrated in Fig. 7.15. All sensors but 3 recovered fully. For the three sensors which did not recover fully, the breakdown shifted above 700 V. Additional time of treatment under the same conditions was needed for the three sensors which had still an erratic behavior at 5%. As it can be seen in Fig. 7.16, the recovery of sensor 44168_005_2-S needed 2 days, while sensors 44172_046_2-S and 44675_013_2-S needed a whole week.

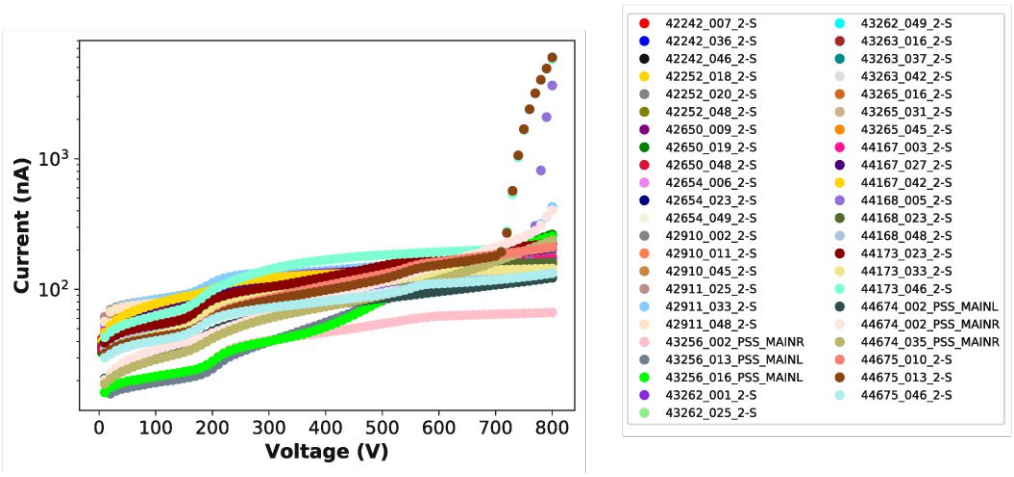


Fig. 7.15: I-V curve of 45 production sensors at RH = 5% and a temperature of T = 20°C, after an exposure to these conditions, biased at 600V for an hour.

In the study presented above, the temperature inside the climate chamber was constant at 20°C. An additional study was conducted in which the role of temperature in the recovery of sensors affected by long exposure to humidity was investigated. This study includes 9 mini sensors from 3 different batches. Mini sensors instead of the main sensors were selected for this study due to their larger availability. Their smaller size compared to the main sensors makes them potentially more resilient against humidity which means that the exposure time should be increased in order to see a deterioration of their electrical behavior. Figure 7.17 shows the current-voltage behavior of the samples at a temperature of 20°C and RH = 20%. In sequence, all miniaturized sensors were exposed to RH = 50% for 4 days and then an I-V in these conditions was performed. This is displayed in Fig. 7.18. Three mini sensors see a breakdown above 600 V.

Applying the same recovery procedure as described above, the relative humidity decreased to 5% with the temperature stable at T = 20°C. The I-V of the mini sensors in these conditions is illustrated in Fig. 7.19. One mini sensor among the three which showed a breakdown in Fig. 7.18, recovered. The other two mini sensors showed a deterioration in their behavior with a shift of the breakdown to lower voltage. This effect could be related to the observations made in Fig. 7.14. An alternative recovery procedure was followed. This process combined a longer exposure to the low relative humidity conditions while the temperature of the air inside the climatic chamber increased to 60°C. The idea behind this step is that a dry and warm environment should speed up the evaporation of humidity from the surface of the devices. The mini sensors were exposed to these conditions for about 3 hours. In sequence, the temperature was set back to 20°C and an I-V was conducted instantly. Figure 7.20 shows that all mini sensors recovered fully.

7.4 Conclusion of the studies

Robustness against environmental impact is important during storage, testing, module assembly and integration. The experience acquired from the quality assurance to date shows that high relative humidity and electrostatic charge-up are two main factors which can potentially deteriorate the electric behavior of the sensors. Nonetheless, the influence on the sensor properties is rather temporary and no permanent damage has been observed so far. Humidity during operation in the CMS detector is no issue of concern, as explained in section 7.3.1.

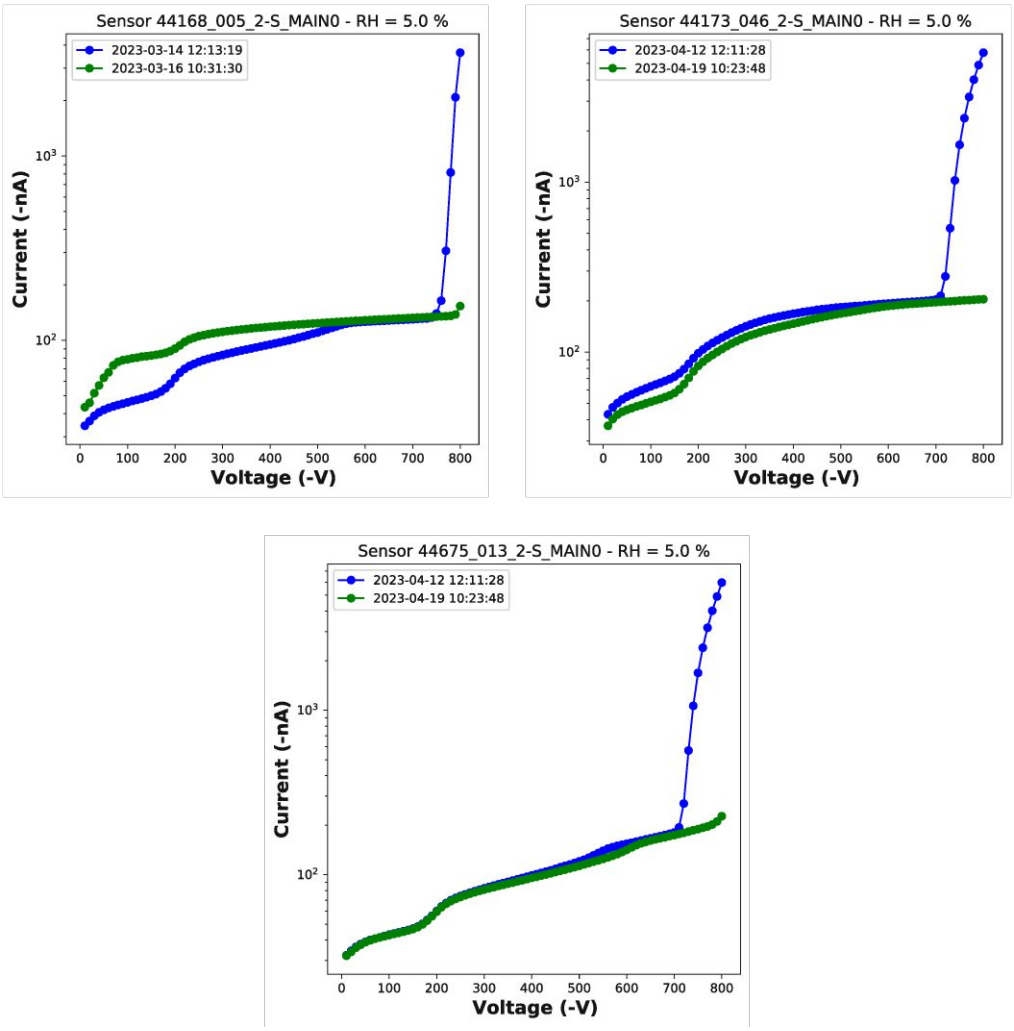


Fig. 7.16: Comparison of I-V curves of 3 sensors at T = 20°C and RH = 5%, before and after a long exposure to these environmental conditions. Sensor 44168_005_2-S (top-left) needed two days (14-16/3) to recover while sensors 44173_046_2-S (top-right) and 44675_013_2-S (bottom) needed a whole week (12-19/4) for a full recovery.

Sufficient experience has been collected about the methods for the recovery of the sensors which are affected by the aforementioned external factors. Ionizing devices prove to be a very useful tool in accelerating the discharge of the sensors. Also, for those sensors that show high sensitivity in humidity and persistent deterioration of their electric behavior due to long exposure, the defined procedure presented in section 7.3.2 could be a successful method of recovery.

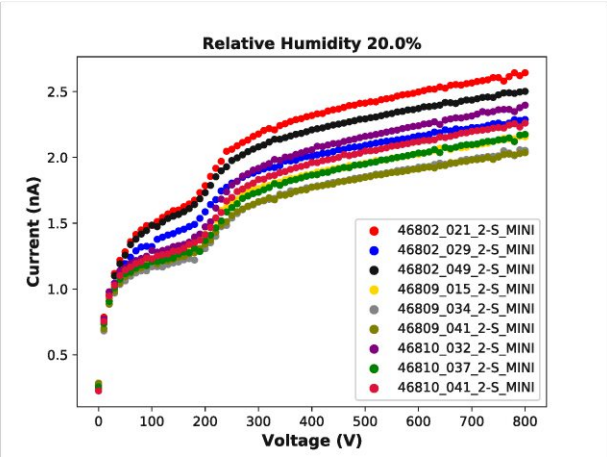


Fig. 7.17: IV curves of 9 mini sensors performed at T = 20°C and 20% relative humidity.

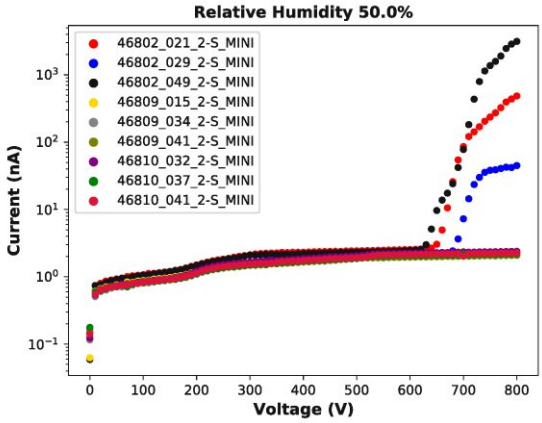


Fig. 7.18: IV curves of 9 mini sensors after a 3-day exposure to 50% relative humidity.

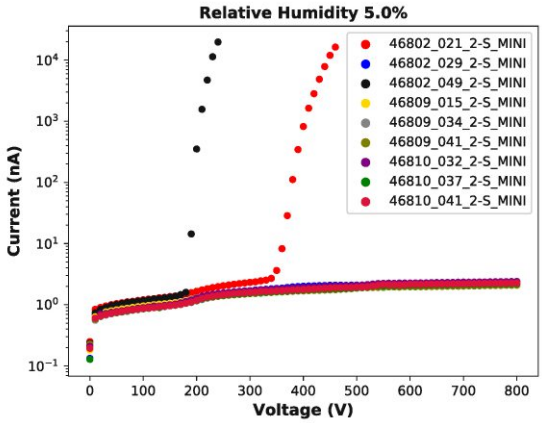


Fig. 7.19: IV curves of 9 mini sensors after a 3 days exposure to 50%, measured at RH = 5% and T = 20°C.

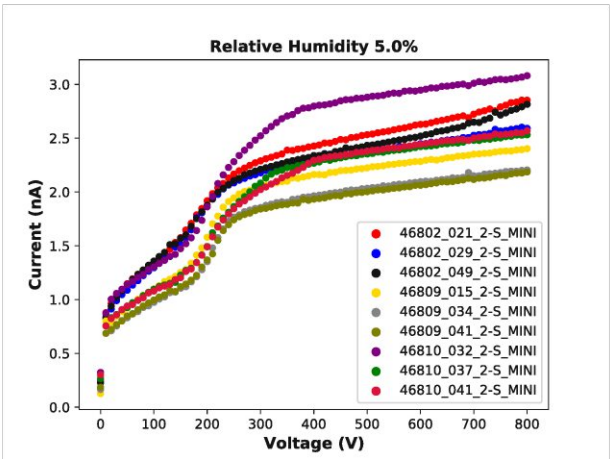


Fig. 7.20: Recovery of all mini sensors after an exposure to T = 60°C and RH = 5% for 3 hours. The I-V was conducted at T = 20°C.

Chapter 8

Process quality control

The process quality control (PQC) as a part of the CMS quality assurance plan aims to monitor the quality and stability of the wafer production through measurements on dedicated test structures. The use of test structures for wafer characterization is a well-established tool in the modern semiconductor industry, therefore CMS benefits from this acquired knowledge and experience. The test structures are incorporated in the same wafers as the sensors and share the same properties. Several parameters are extracted from these measurements which can give an overview of the wafer quality. One advantage of this method is time efficiency since the measurements are generally fast. In addition, PQC offers the opportunity to investigate parameters that are not easily measurable on the main sensors, including parameters that require potentially destructive measurements such as the extraction of the breakdown voltage of the coupling oxide.

Test structures for characterization of the sensor production were also used in the quality assurance process of the current CMS strip detector. A fraction of the Phase-2 test structures are adapted from previous designs, such as diodes, MOS capacitors, and gate-controlled diodes. A set of additional structures has been added which expands the potential of PQC to investigate further crucial parameters. Some examples of newly introduced structures are Van-der-Pauw structures which measure the sheet resistance of different implant layers or MOSFET test structures to assess the interchannel properties. More detailed information regarding the design, the parameters of interest and the measuring procedure of each structure is given in the following sections.

8.1 The PQC flutes

The test structures of CMS Outer Tracker wafers are developed around the main sensor. They are delivered as four half-circular segments which together with the main sensor are the remaining parts of the wafer after the dicing process. These segments are known as *half-moons*. Several different structures are hosted on each half-moon, developed either for automated or manual measurements. The structures for the automated measurements are arranged around an array of 20 contact pads (2×10), optimized for measurements with a 20-needle probe card. Each array of pads is called a *flute*. Each set of test structures features 15 flutes (Fig. 8.1). The flutes are spaced in equal steps in both horizontal and vertical directions. Each flute pad has a pitch equal to 200 µm and a size of 100×100 µm. An instance of a 20-pad array is given in Fig. 8.2. Among the 15 flutes per set, 4 are measured in PQC. The extracted parameters from these 4 flutes are sufficient to give an overview of the wafer quality. Flutes 1 and 2 are known as "Quick" flutes, while flutes 3 and 4 are known as "Extended". The remaining 11 flutes which are known as the "Additional" flutes, are aimed for a more detailed analysis of individual parameters with respect to different geometry and design.

The set of test structures which is illustrated in Fig. 8.1 is replicated up to 6 times on each CMS wafer. The characterization of all these structures can give a good picture of the uniformity of each individual parameter on a wafer level. A convention North-South-East-West is used in

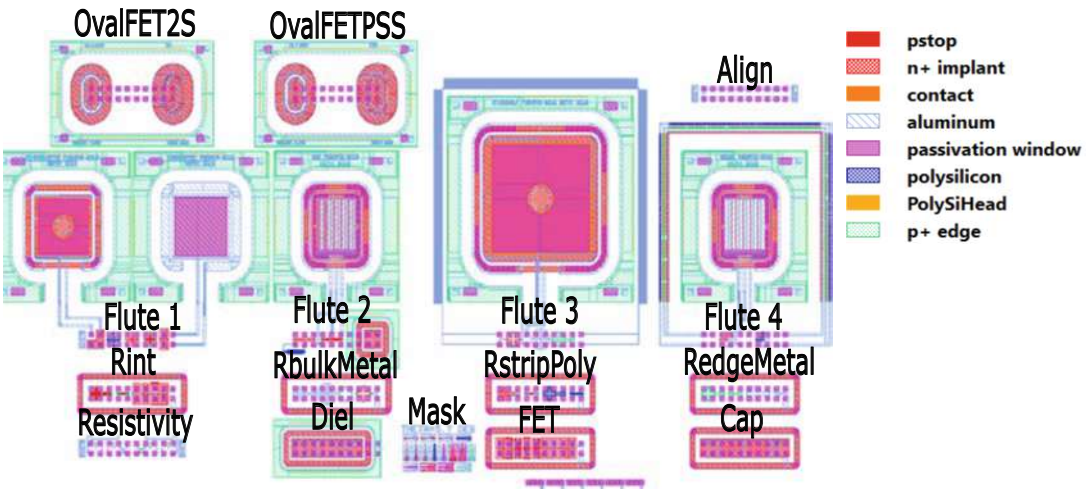


Fig. 8.1: PQC set with 15 flutes. A naming convention is assigned to each flute.

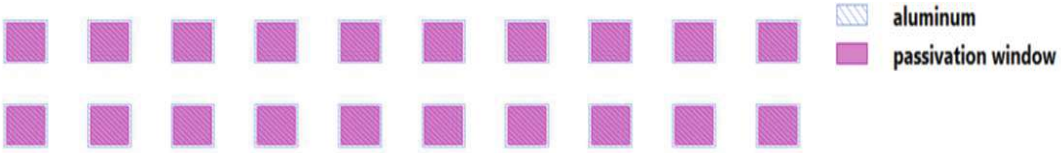


Fig. 8.2: The array of 20 pads which is connected to the structures of the flute.

order to specify the location of each half-moon (Fig. 8.3). The 6 sets of structures are located on the West, East and North half-moons. The South half-moon includes test structures for manual measurements and a mini-sensor with the same design and strip length as the main sensor. The South half-moon is used for the irradiation tests (section 5.3).

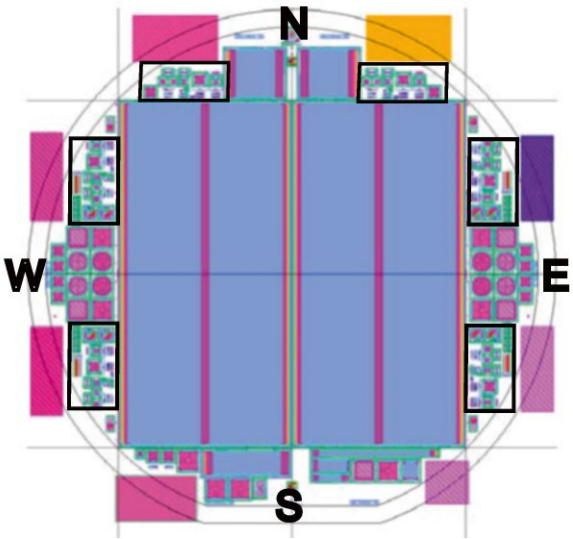
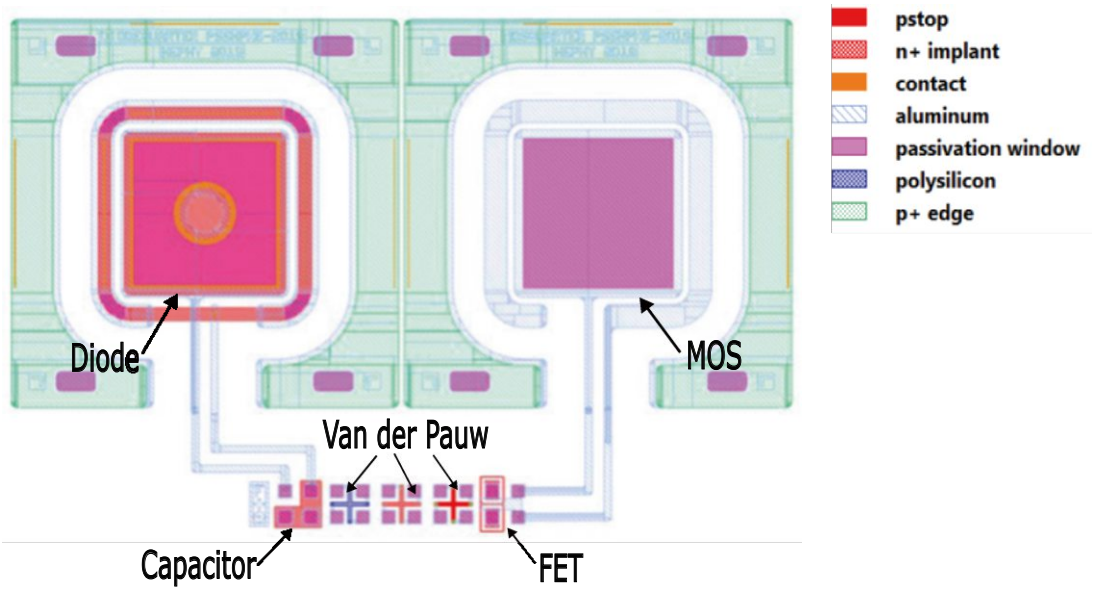


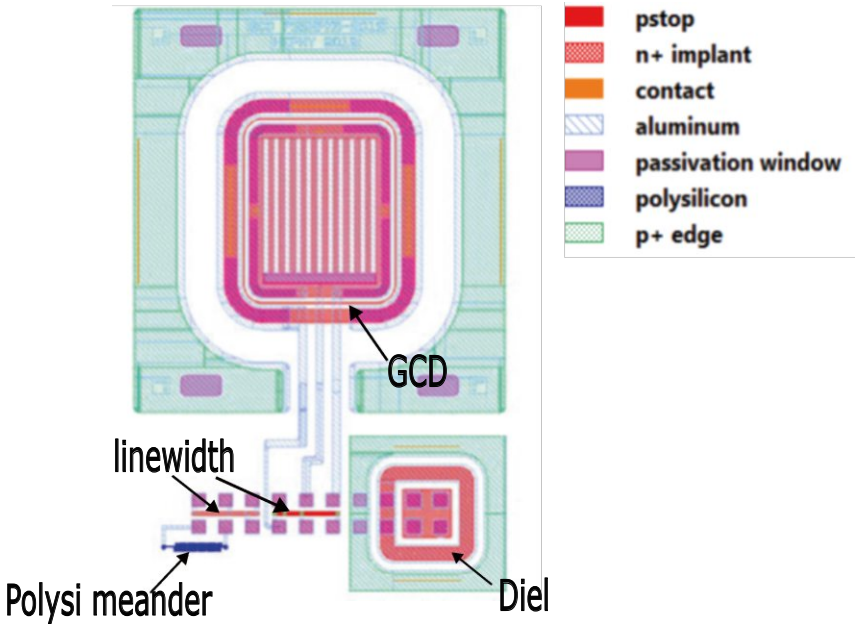
Fig. 8.3: A PS-s wafer layout. The 6 sets of test structures which are aimed for PQC measurements are enclosed by the black boxes. The orientation of each half-moon with respect to the main sensor is given.

8.1.1 Quick flutes

Flute 1 and 2 host structures with the target to perform a quick and automated measurement of the most important process parameters. In principle, testing the "Quick" flutes is sufficient to extract some general conclusions concerning the quality of the wafer. Parameters such as the full depletion voltage, the sheet resistance of the implants, the flat-band voltage of the thick oxide, the resistance of the bias resistor as well as the thickness and the breakdown voltage of the coupling oxide can be determined.

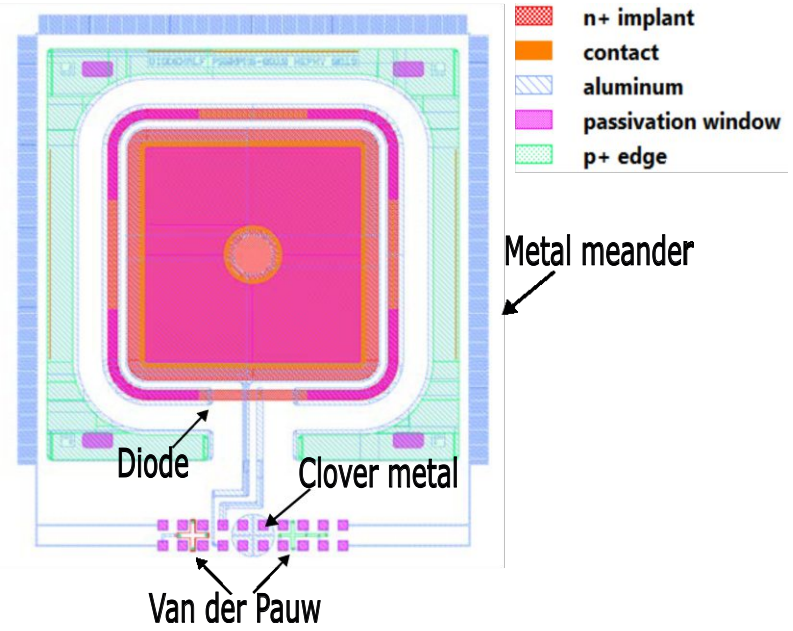


(a) Flute 1.

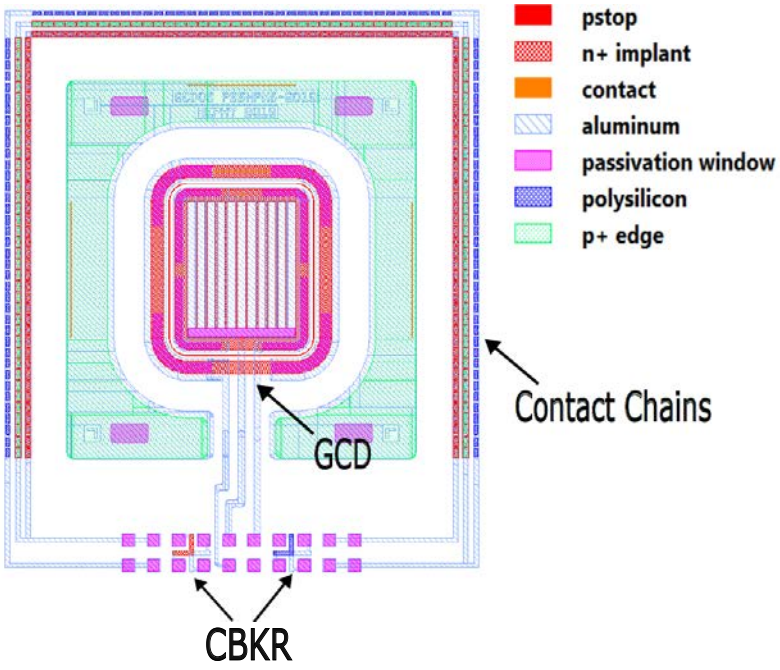


(b) Flute 2.

Fig. 8.4: Quick flutes with all individual test structures annotated.



(a) Flute 3.



(b) Flute 4.

Fig. 8.5: Extended flutes with all individual test structures annotated.

8.1.2 Extended flutes

Flutes 3 and 4 provide a more thorough investigation of all parameters of interest. Combining the information given from the structures of the "Extended" and "Quick" flute is sufficient to obtain full knowledge about the quality and characteristics of the wafer. Additional parameters which can be extracted from "Extended" flutes are the resistance of the metal to implant and metal to polysilicon contact, the sheet resistance of the p-edge implant and the metal, and the bulk resistivity measured from a Van-der-Pauw structure.

8.1.3 Additional flutes

The remaining 11 flutes are not included in the standard CMS PQC measurements. They provide the option for a more in-depth analysis in case anything abnormal is observed on one or more parameters. The additional flutes are arranged in two rows below each PQC main flute.

Two automated structures with 20-pad flutes are located below flute 1. A set of Van-der-Pauw and FET structures with a main focus on studying the properties of p-stop is hosted on the first row (Fig. 8.6). The second-row houses structures designed for 4-wire measurements on the p-bulk resistivity (Fig. 8.7). Additional Van-der-Pauw structures for measuring the metal and bulk sheet resistance are located on the first row below flute 2 (Fig. 8.8) while the second row hosts a dielectric breakdown structure with 20-pads (Fig. 8.9). The rows below Flute 3 include a flute with n^+ and polysilicon implantations for sheet resistance and linewidth measurements (Fig- 8.10) and a flute with transistors of different designs for characterization of the p-stop (Fig- 8.11). Moreover, the first row under flute 4, houses Van-der-Pauw cross-bridge structures for measurements on the metal and p^+ edge sheet resistance (Fig. 8.12) while the second row features a 20-pad flute with capacitor structures to determine the coupling oxide thickness (Fig. 8.13).

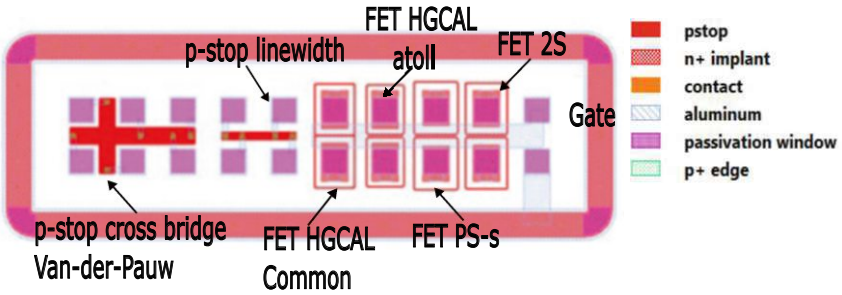


Fig. 8.6: Interstrip resistance flute. The p-stop implant is characterized through cross-bridge van-der-Pauw, linewidth and four field-effect transistor structures. The FET shares a common gate and inter-channel geometries mirroring the inter-strip layout of different tracker and HGCAL designs.

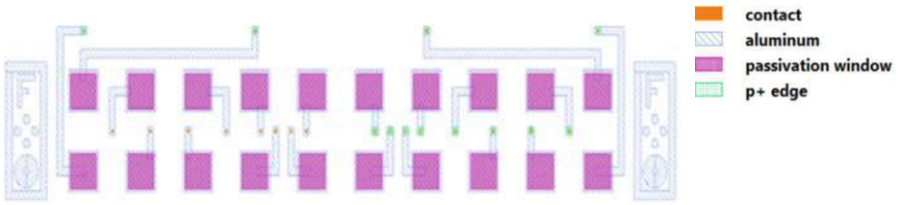


Fig. 8.7: 4-wire bulk resistivity flute. The consecutive 4-wire structures feature different contact distances (53, 133 and 600 µm). In addition, some contacts include p^+ implants with the aim of minimizing contact resistance. The flute acts as an alignment flute for the PQC sets due to the alignment marks at the sides.

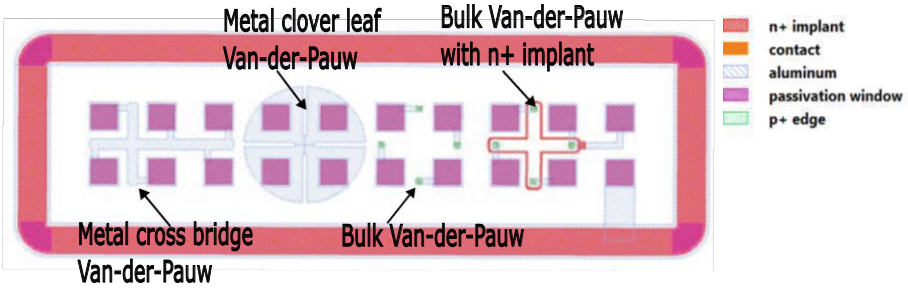


Fig. 8.8: Van-der-pauw flute for measuring the bulk and the metal sheet resistance. A metal cross-bridge and a metal clover leaf structure are accompanied by a cross van-der-Pauw which offers contact to the bulk. The two rightmost pads offer contact to the n^+ implant (top) and to the guard ring (bottom).

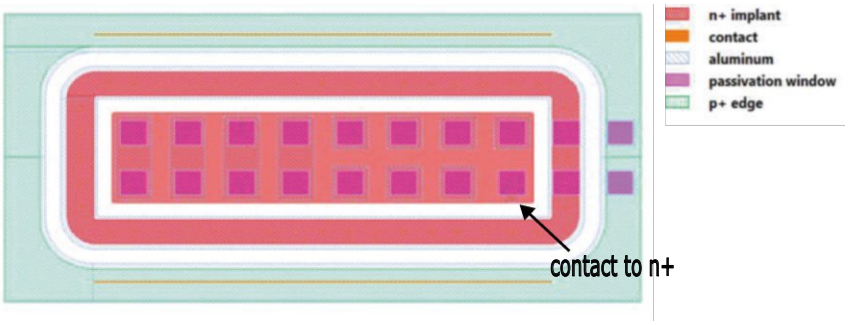


Fig. 8.9: The dielectric breakdown flute. Metal pads are developed atop of a SiO_2 coupling oxide and a n^+ implant. Dedicated pads offer the option to contact directly the n^+ implant, the guard and the edge ring.

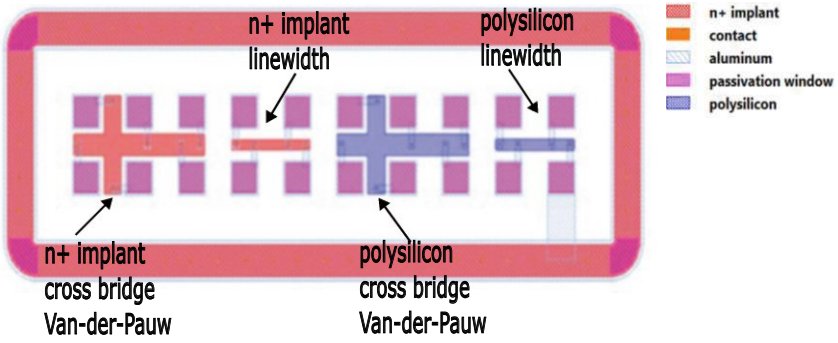


Fig. 8.10: Flute with cross-bridge Van-der-Pauw and linewidth structure for characterisation of the n^+ implant and the polysilicon.

8.2 The test structures

8.2.1 Diode

The diode is one of the most fundamental structures in the semiconductor industry and is optimal for characterizing the properties of the silicon bulk. Through a diode measurement, one can extract parameters such as the full depletion voltage, the total leakage current, the bulk resistivity, the doping concentration and the active thickness of the substrate. These parameters

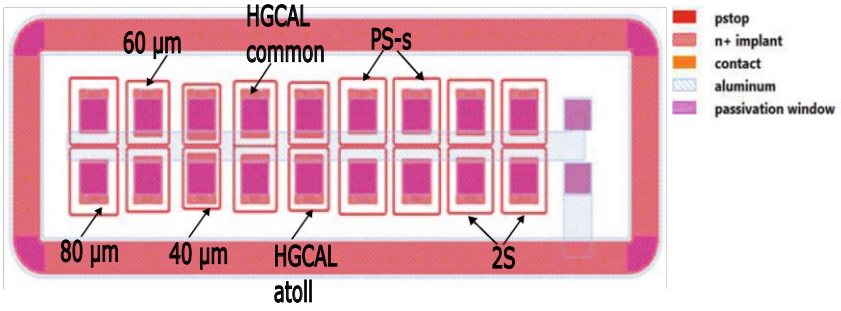


Fig. 8.11: FET flute. It contains 9 transistors which share a common gate metal. 6 out of 9 transistors are designed based on the inter-channel geometries of the tracker and HGCAL sensors. Furthermore, the flute includes three FET with channel widths 40,60 and 80 µm.

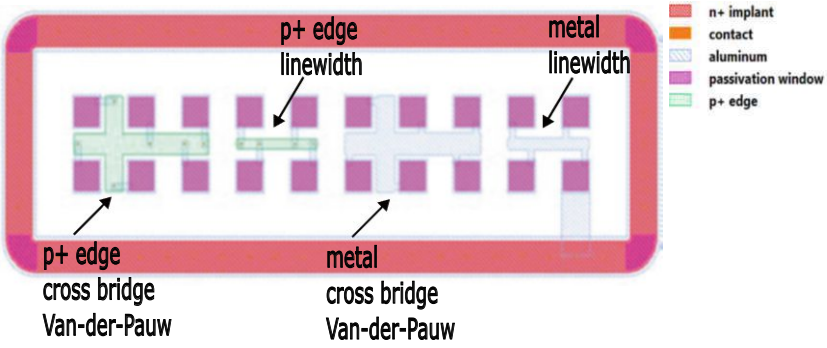


Fig. 8.12: Flute with cross-bridge Van-der-Pauw and linewidth structure for characterisation of the p^+-edge implant and the metal.

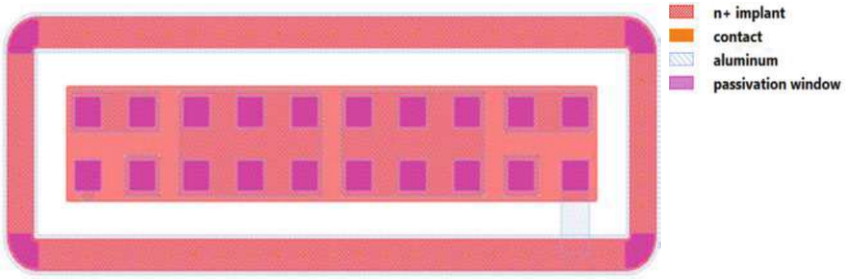


Fig. 8.13: Capacitor flute with different structures formed by a common n^+ implant, a SiO_2 coupling dielectric and metal pads atop. A direct contact to the n^+ implant is provided by the bottom left pad.

can be extracted also from direct measurements on the main sensor. However, in this case, the impact of the segmentation of the anode should be taken into consideration in the final results.

The design of the CMS diodes is based on a n^+ implant which forms a p-n junction with the p-type bulk, while a n^+ guard ring and a p^+ edge ring surround the structure. Similar to the main sensor, the aluminum on top of the implants extends beyond the implant edges on both sides to improve the high voltage stability of the diode (metal overhang). The structure features a SiO_2 passivation layer with openings at the center pad, the guard ring and the edge ring to facilitate contact with probe needles.

There are several diodes of different sizes and geometries incorporated in each wafer. A half-sized diode (2.5 mm × 2.5 mm) and a quarter sized diode (1.25 mm × 1.25 mm) are the two diode structures with flute contacts. The former is located in flute 1 (Fig. 8.4a) while the latter is located in flute 3 (Fig. 8.5a). Due to the fact that these diodes are connected to the metal pads of the flute, an opening on the edge ring is necessary to facilitate the connection to the n^+ implant and to the guard ring. However, this opening impacts the high-voltage stability of the structure, as it is shown in the following section. An illustration of a flute diode is given in Fig. 8.15.

Moreover, each wafer hosts diodes for manual measurements. In particular, there are 8 square diodes (5 mm × 5 mm), 12 square half-sized diodes (2.5 mm × 2.5 mm) with and without a p-stop implant, one square quarter-sized diode (1.25 mm × 1.25 mm) and 4 round diodes (diameter 5 mm). The round shape is an optimal geometry to reduce the impact of the edge effects. All diodes feature a circular opening in the aluminium which supports tests with laser injection. Figure 8.14 illustrates a few examples of CMS Outer Tracker diodes for manual measurements.

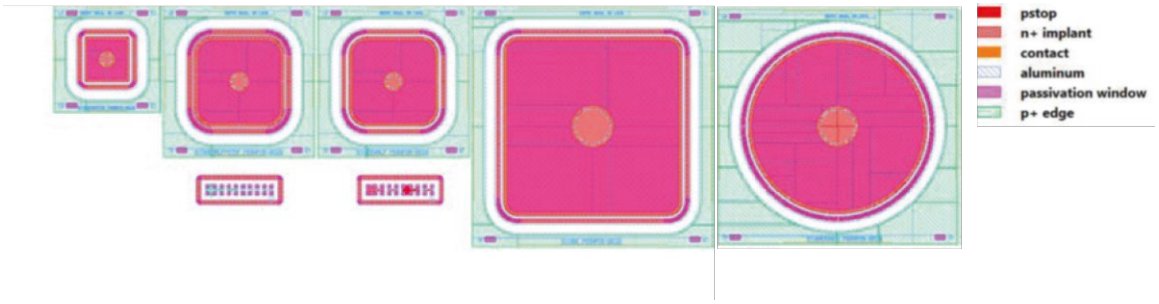


Fig. 8.14: From left to right: quarter-sized square diode (1.25 mm × 1.25 mm), half-sized square diode (2.5 mm × 2.5 mm) with and without a p-stop surrounding the n^+ implant, square diode (5 mm × 5 mm) and the round diode. All of the illustrated diodes are designed for manual measurements.

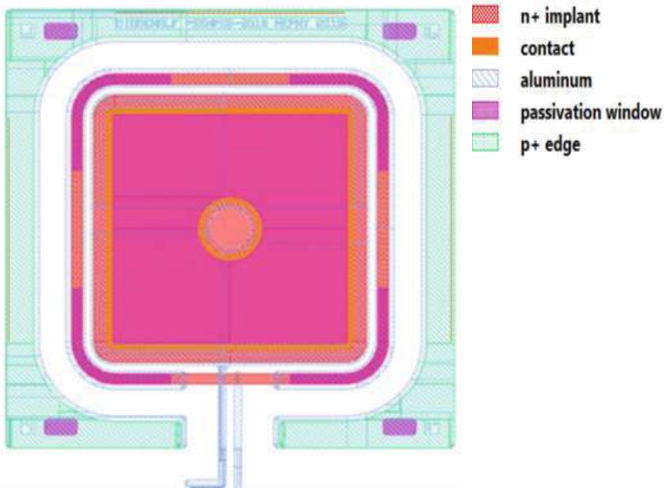


Fig. 8.15: CMS wafer diode with opened edge ring for facilitating contacts to the flute pads.

8.2.1.1 I-V Characteristics

The bulk leakage current is one of the main parameters that characterizes a diode. As discussed in section 3.1.4, when a diode is in reverse bias mode, the total bulk current is created predominantly by two mechanisms: the diffusion of charge carriers into the space charge region and the thermal generation of electron-hole pairs in the depleted region. The bulk current is a direct indication of the bulk purity since for a certain temperature, the leakage current increases with increasing concentration of impurities.

The diode current is measured through an I-V ramp from 0 V up to −1000 V with a −10 V stepsize. For the measurement, the backside is set to a high potential and the guard ring is set to the ground. The leakage current can be measured by contacting the pad which is connected to the n^+ implant, with a probe needle.

Unlike the sensor I-V measurement where the guard ring is left floating, the diode guard ring during the I-V measurement is grounded. The structure is not properly isolated from its surrounding structures due to the opened edge ring. Hence, parasitic currents, in the order of a few µA, are introduced [88]. When the guard ring is grounded, the parasitic currents are driven to the ground before they reach the n^+ pad, where an electrometer measures the diode total current. A drawing of the circuit is given in Fig. 8.16.

Figure 8.17 compares the diode current when measured by the electrometer (red curve) which is connected to the n^+ pad and by the source SMU which applies the high voltage between the backplane and the guard ring (blue curve). It is clear that the parasitic currents when driven to the guard ring, sum up to a very large measured current. The trend of the current when measured from the n^+ pad is different. Below 100 V the diode exhibits a very large current. An electrical connection is established between the guard ring and n^+ implant which is set to the same potential (ground). As the bias voltage increases, the depletion region expands laterally and eventually isolates electrically the two implants. This explains the gradual decrease of the measured total current which beyond 100 V includes only the bulk current of the diode. Introducing a p-stop implant between the guard ring and the n^+ implant could establish an isolation that disrupts the formation of the channel at low voltages. As shown in [88], the p-stop mitigates this effect. Beyond 400 V the diode shows an elevating current which is attributed to the reduced high-voltage stability of the structure due to the opened edge ring. A typical I-V behavior of PQC flute diodes is illustrated in Fig. 8.18.

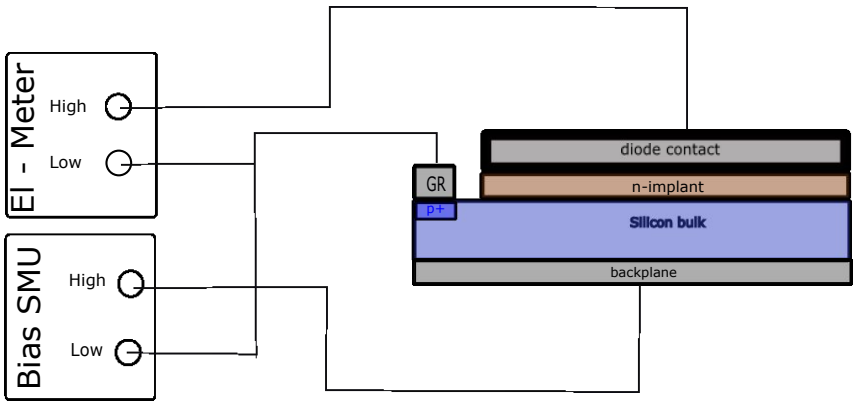


Fig. 8.16: Diode I-V measurement with grounded guard ring.

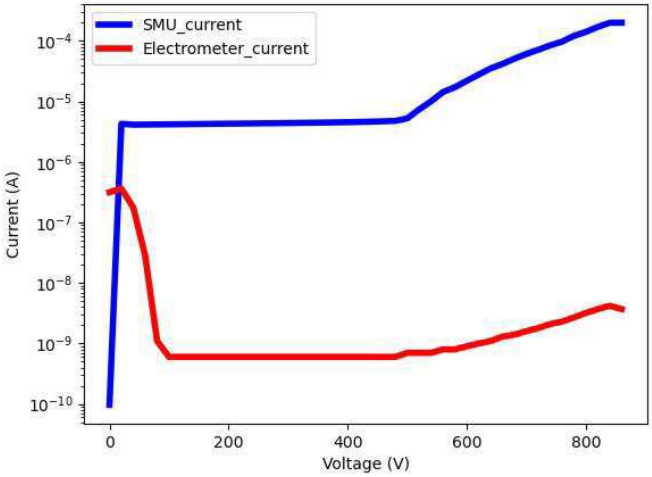


Fig. 8.17: Diode I-V curve. The blue curve shows the diode leakage current as measured by the SMU which applies the voltage. The red curve corresponds to the leakage current measured on the n^+ implant by the electrometer.

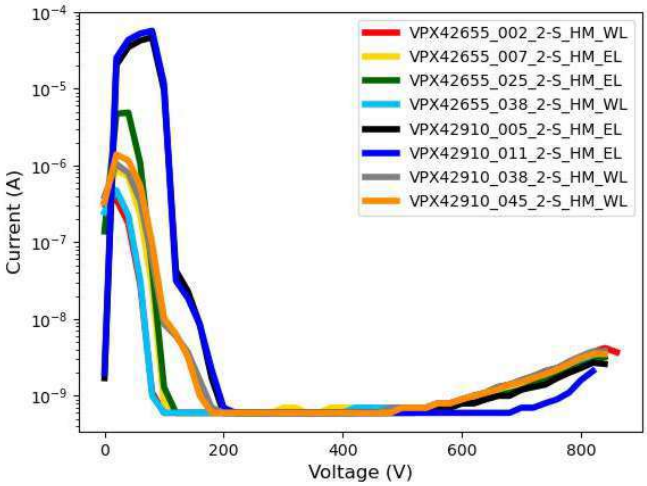


Fig. 8.18: Comparison of I-V curves of flute diode structures from different wafers.

8.2.1.2 C-V characteristics

The full depletion voltage of the diode can be extracted from a C-V measurement. This value is determined from the intersection point of two linear fits to the two characteristic regions of the $1/C^2$ - V curve (Fig. 8.19). A voltage ramp is performed from 0 V to −500 V with a −5 V stepsize while the capacitance is measured for each voltage. For the PQC diode measurements, the LCR test amplitude is set to 250 mV and the frequency to 10 kHz.

As discussed in references [89], [88], setting the guard ring to ground potential reduces the influence of the edge capacitance. With a grounded guard ring, only the capacitance of the depletion region is measured, while the edge effects are minimized. A drawing of the circuit of a diode C-V measurement is displayed in Fig. 8.20.

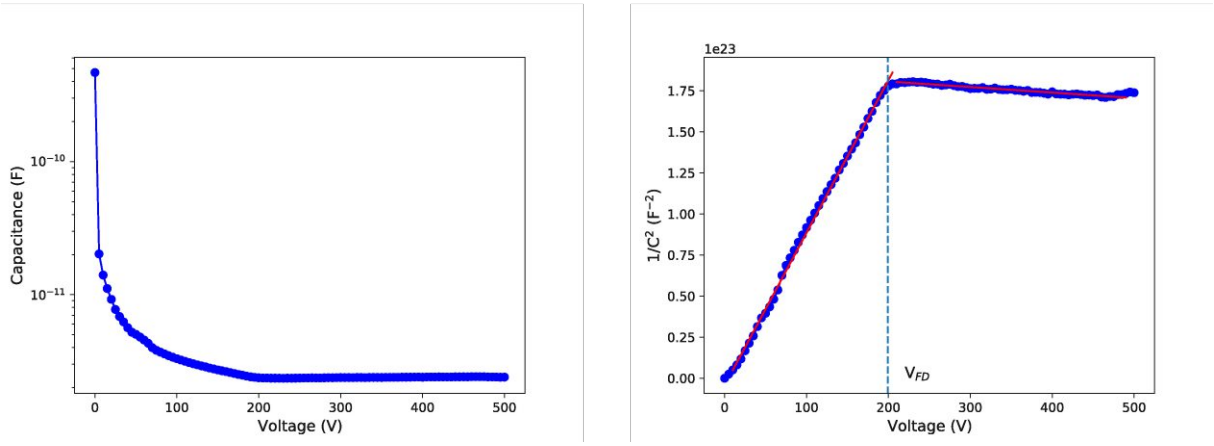


Fig. 8.19: The C-V characteristics of a diode (left) and the equivalent $1/C^2$ - V curve (right) with the extracted full depletion voltage V_{FD}.

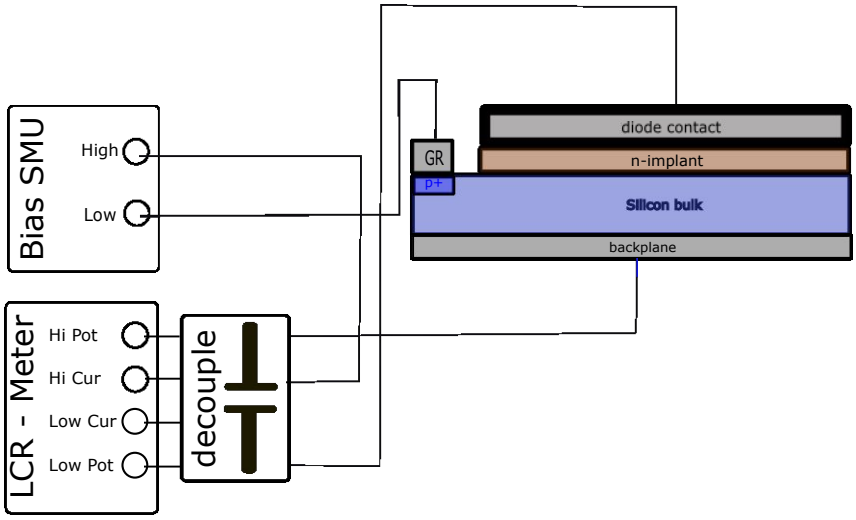


Fig. 8.20: Equivalent CV circuit of the diode. The return path of the LCR meter (LDUT) has no direct connection to the ground. To decouple the LCR from the applied bias voltage, a decoupling unit is used.

The opened edge ring of the flute diodes has a small impact on the C-V measurement. As can be seen in Fig. 8.19, the $1/C^2$-V curve deviates from a straight line for voltages below 100 V. Parasitic currents from the surrounding of the diode or coupling to the neighboring structures via the probe card needles might be the reason why the C-V shows this noisy behavior. Nonetheless, the extraction of the full depletion voltage is still feasible. This behavior is more pronounced on the smaller quarter-sized diode (1.25 × 1.25 µm) which belongs to flute 1 than on the larger half-sized diode (2.5 × 2.5 µm) of flute 3 [88]. Due to its more robust behavior, the half-sized flute diode is included in the standard PQC tests. Typical $1/C^2$ - V curves of half-sized flute diodes are given in Fig. 8.21.

Using the slope of the linear region for $V < V_{dep}$ one can extract the bulk doping concentration N_A as:

$$N_A = \frac{2}{A^2 q \epsilon_0 \epsilon_{r,Si} \frac{d(1/C^2)}{dV}} \tag{8.1}$$

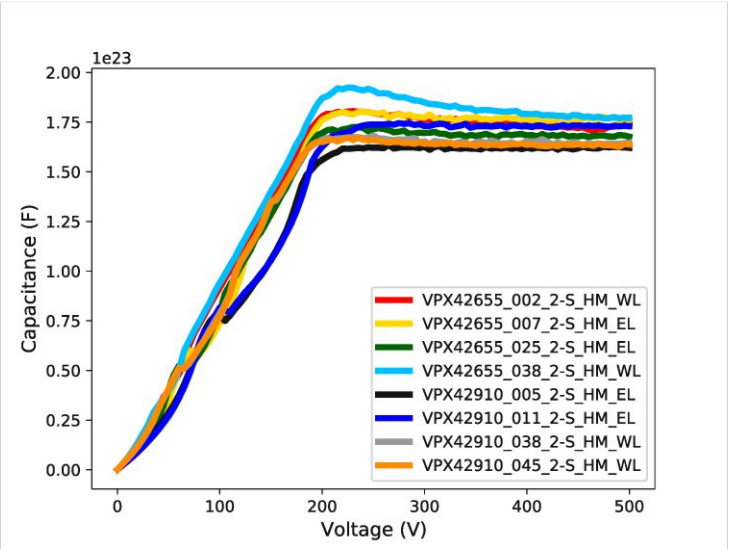


Fig. 8.21: $1/C^2$ curve of half-sized PQC flute diodes from different wafers.

where A is the plate area, $\epsilon_0 = 8.85 \times 10^{-12}$ F/m is the vacuum permittivity and $\epsilon_{r,Si} = 11.68$ is the relative permittivity of silicon.

The bulk resistivity can be calculated by the formula:

$$\rho = \frac{d^2}{2\epsilon_0 \epsilon_r \mu_\mathrm{h} \mathrm{V_{FD}}} \tag{8.2}$$

where d is the active thickness of the diode and $\mu_\mathrm{h} = 450$ cm/(Vs) is the hole mobility in silicon.

8.2.2 Metal Oxide Semiconductor capacitor (MOS)

The Metal Oxide Semiconductor (MOS) structure consists of a metal gate electrode, an insulating material that acts as a dielectric layer (typically SiO_2) and a silicon bulk. In PQC, the MOS structure is used as a tool to examine and characterize the properties of the oxide-substrate interface. It should be highlighted that the oxide of the MOS structure is not the coupling oxide which is deposited between the strip implant and the metal, but rather the thicker SiO_2 oxide layer. The properties and quality of the oxide have a direct impact on the interstrip isolation due to the presence of positive oxide charges. Hence, the evolution of its characteristic parameters over production time as well as their behavior after irradiation is crucial to be monitored by CMS.

The CMS Phase-2 MOS structures consist of a p-type bulk, a SiO_2 layer and a metal pad atop which acts as the gate. A n^+ guard ring and a p^+ edge ring surround the MOS and shield it from the influence of the surrounding structures. A squared-sized and a round-shaped MOS capacitor are incorporated in each CMS wafer intended for manual measurements (Fig. 8.22). In addition, a quarter-sized MOS with a gate area of 1.29×1.29 mm^2 is connected to flute 1. The structure is shown in Fig. 8.23. It features an opening on its edge ring in order to facilitate the connection to the flute pads.

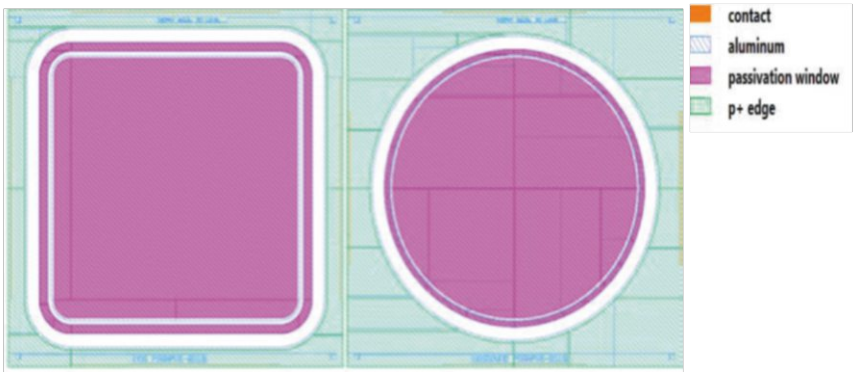


Fig. 8.22: A CMS Phase-2 quarter and a round MOS structure aimed for manual measurements.

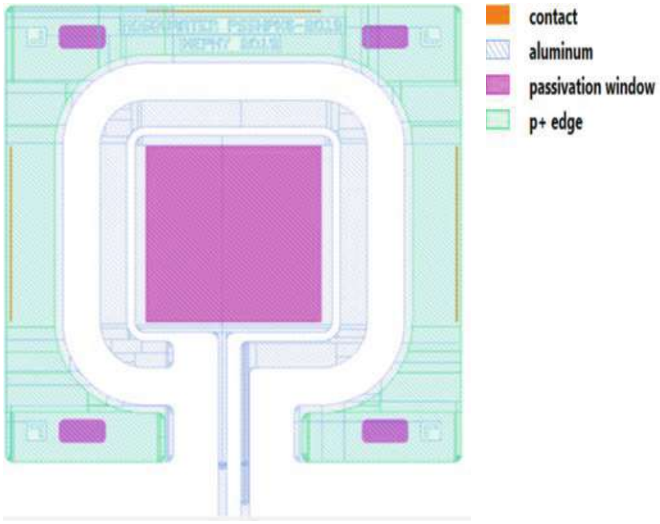


Fig. 8.23: Flute MOS with opened edge ring.

8.2.2.1 MOS operation states

The properties of the oxide-silicon interface of a MOS capacitor can be regulated by altering the gate voltage. To understand how the behavior of the interface varies with gate voltage, one should consider the energy band diagram of the metal and the silicon. This is displayed in Fig. 8.24.

Flat-band condition

Figure 8.24(a) shows the ideal case when zero bias is applied across the MOS device. The energy bands are flat which indicates that there is no net charge in silicon. This condition is known as *flat-band* condition. However, in reality, the flat-band condition occurs far from the ideal case. Two are the main mechanisms which are involved.

The first factor is the work function difference between the metal and the semiconductor. A characteristic parameter of the metal is its work function $e\phi_m$ which describes the required

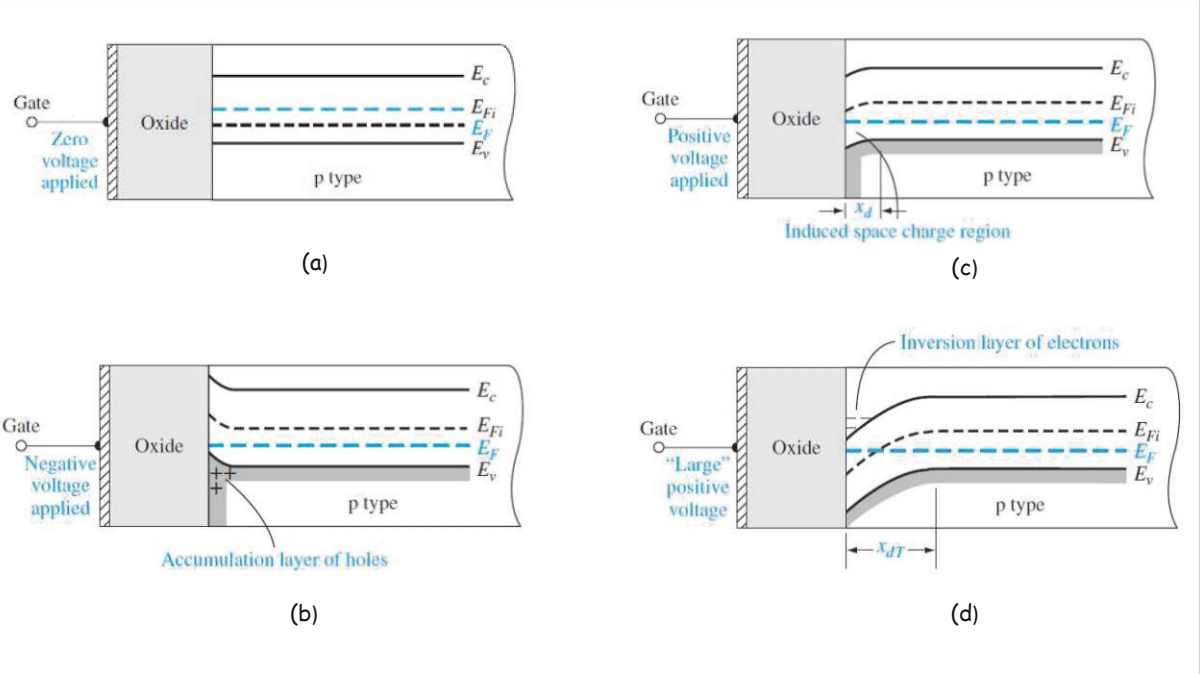


Fig. 8.24: MOS states for a p-type bulk: flat-band condition (a), accumulation (b), depletion (c) and inversion (d) [49].

energy to remove one electron from the Fermi level to the vacuum. Similar for a semiconductor, the work function is defined as $e\phi_s$ where

$$\phi_s = \chi + \frac{E_\mathrm{g}}{2} + \frac{k\mathrm{T}}{q}\ln(\frac{N_A}{n_i}) \tag{8.3}$$

where E_g is the band-gap energy, T is the temperature expressed in K, n_i is the intrinsic carrier concentration and N_A is the bulk carrier concentration. The parameter χ is called *electron affinity* and describes the necessary energy to remove an electron from the conduction band into the vacuum. Silicon has an electron affinity equal to $\chi_\mathrm{Si} = 4.05$ eV. In the ideal case, the Fermi bands of the metal and the silicon are perfectly aligned. However, for a p-type silicon bulk, it is true that $\phi_\mathrm{m} < \phi_\mathrm{s}$ [49]. This leads to a charge transfer from the bulk toward the surface and consequently to a bending of the bands. In that case, the flat-band voltage should be considered as the difference between the work function of the metal and the semiconductor, hence it should be $V_\mathrm{fb} = \phi_m - \phi_s$.

The second factor that should be considered is the presence of net fixed charges (Q_ox) near the Si-SiO_2 interface. These charges can be divided into oxide-trapped charges which are associated with defects in the oxide, interface traps which are attributed to the interruption of the periodic lattice structure in the Si-SiO_2 interface, as well as the fixed positive oxide charges near the interface. The latter is attributed to the dangling bonds that are formed close to the interface during the oxidation process of the SiO_2. The charge density can be altered to some level by annealing the oxide in an argon or nitrogen atmosphere, nevertheless, a certain amount of charge is still there (section 3.5.2.1). The net fixed charge induces an electric field in the oxide and a voltage equal to $-Q_\mathrm{ox}/C_\mathrm{ox}$. As an outcome, the bands are deflected.

The combined action of both effects leads to a deviation of the flat-band condition from the ideal case. An external voltage must be applied in order to establish flat bands (Fig. 8.25). Hence, the flat-band voltage V_{fb} is defined as:

$$V_{\mathrm{fb}} = \phi_{\mathrm{m}} - \phi_{\mathrm{s}} - \frac{Q_{\mathrm{ox}}}{C_{\mathrm{ox}}} \tag{8.4}$$

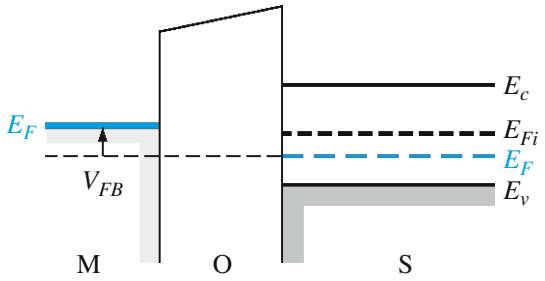


Fig. 8.25: MOS energy diagram at flat-band condition [49].

Accumulation

When a negative voltage is applied to the gate ($V < V_{\mathrm{fb}}$), holes which are the majority carriers in a p-type bulk are accumulated at the oxide-substrate interface. This is illustrated in the band diagram of 8.24(b), where the valence band edge close to the interface is nearer to the Fermi level than in the bulk. This state of the MOS capacitor is known as *accumulation*. The region of the substrate below the interface is more p-doped than the bulk. At accumulation, the gate metal is negatively charged while the region below the oxide-silicon interface is positively charged. A parallel plate capacitor is essentially formed while its capacitance is defined exclusively by the oxide capacitance C_{ox}. With known oxide capacitance, one can calculate the oxide thickness using the formula:

$$t_{\mathrm{ox}} = \epsilon_0 \epsilon_{r,\mathrm{SiO_2}} \frac{A_{\mathrm{gate}}}{C_{\mathrm{ox}}} \tag{8.5}$$

here $\epsilon_{r,\mathrm{SiO_2}} = 3.9$ is the relative permittivity of SiO_2 and A_{gate} is the area of the gate.

The total oxide charge is given by the formula:

$$Q_{\mathrm{ox}} = qN_{\mathrm{ox}}A_{\mathrm{gate}} \tag{8.6}$$

where N_{ox} is the charge concentration in the oxide. Using formula 8.4, the parameter N_{ox} is given by:

$$N_{\mathrm{ox}} = \frac{C_{\mathrm{ox}}(\phi_{\mathrm{ms}} - V_{\mathrm{fb}})}{qA_{\mathrm{gate}}} \tag{8.7}$$

Depletion

When a positive gate voltage is applied, the holes are repelled and pushed away from the interface. The energy bands start to bend downwards. A space charge region is formed near the oxide-silicon interface. This is the *depletion state* of a MOS capacitor and is displayed in

Fig. 8.24(c). Since the depletion width of the space charge region adds up to the oxide thickness, the total capacitance is smaller than the accumulation state.

Inversion

An even higher increase of positive voltage causes a stronger bending of the energy bands downwards. The point at which the intrinsic Fermi level E_{Fi} of the semiconductor is lower than the constant Fermi level E_F is when the minority carriers (electrons) have surpassed the number of holes. An inversion electron layer is created at the oxide-silicon interface. Near the surface, the energy band diagram looks like a n-type semiconductor. Thus, near the surface, the silicon bulk has inverted from p-type into n-type (Fig. 8.24(d)).

Figure 8.26 illustrates the energy band diagram of p-type silicon at the inversion point. At this point, the surface potential ϕ_s equals to $2\phi_{\mathrm{FP}}$, where ϕ_{FP} is the potential difference between the intrinsic Fermi level of the silicon bulk and the Fermi level. This equality states that the Fermi level at the surface is as far above the intrinsic Fermi level $\mathrm{E_{Fi}}$ as it is below the $\mathrm{E_{Fi}}$ in the p-type bulk. This is the so-called *threshold inversion point*. The gate voltage that creates this condition is known as *threshold voltage* V_{th}. The threshold voltage is defined as:

$$V_{\mathrm{th}} = V_{\mathrm{FB}} + 2\phi_{\mathrm{FP}} + \sqrt{4\epsilon_{\mathrm{si}} q N_{\mathrm{A}} \phi_{\mathrm{FP}}} \tag{8.8}$$

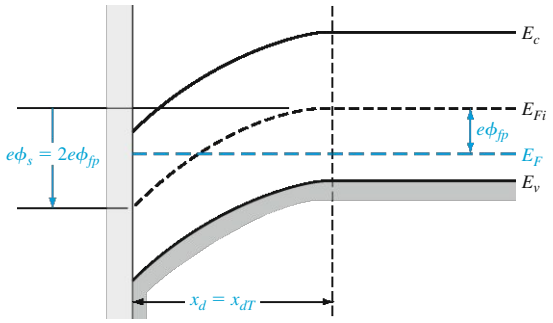


Fig. 8.26: Energy diagram of p-type silicon bulk at threshold inversion condition [49].

8.2.2.2 MOS C-V characteristics and extraction of parameters

From the aforementioned MOS parameters, the flat-band voltage and the oxide capacitance can be extracted experimentally from a C-V measurement. Figure 8.27 illustrates an example of a C-V measurement at 10 kHz test frequency for a p-type MOS capacitor with an aluminum gate. In this measurement scheme, the gate electrode is set to ground while the voltage is applied to the backside of the structure. This is the inverted case of what is displayed in Figure 8.24. For negative voltages, electrons build up at the surface creating an inversion layer while the accumulation state is achieved for sufficiently large positive voltages. Figure 8.28 is a drawing of the circuit for a PQC MOS capacitor measurement.

At the accumulation state, the measured capacitance is relatively stable and equals the oxide capacitance C_{ox} ($C_{acc} = C_{ox}$). As it can be seen in 8.27, when the applied voltage becomes smaller than the flat-band voltage, a depletion region is formed below the interface and as a consequence, the total capacitance decreases. For the extraction of the flat-band voltage, different

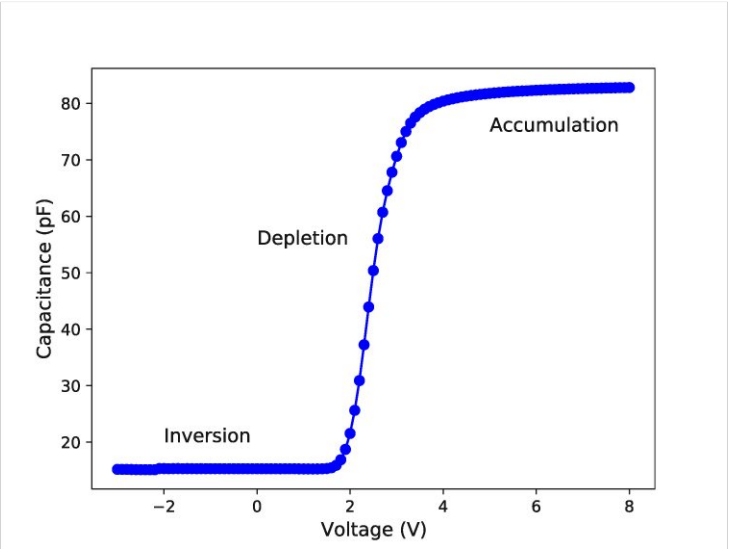


Fig. 8.27: MOS high-frequency C-V curve.

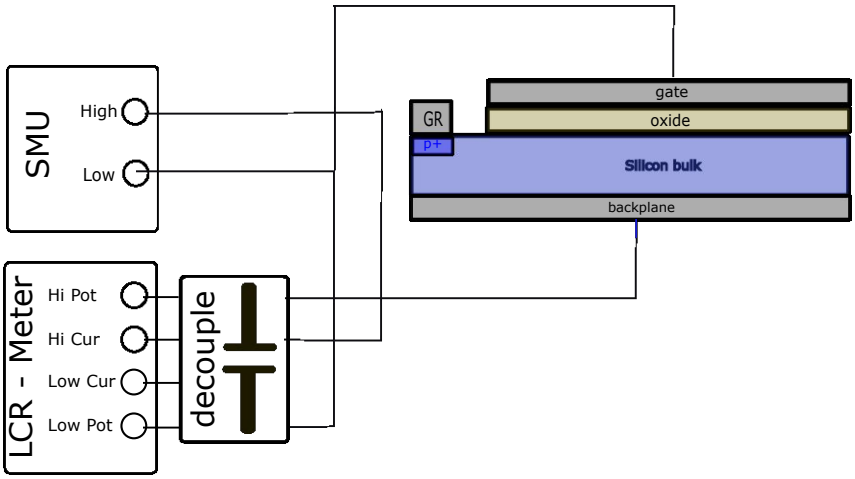


Fig. 8.28: Drawing of PQC MOS circuit as implemented at HEPHY.

methods have been developed [88]. In the scope of CMS PQC the V_{fb} is approximated as the intersection point of two linear fits in the accumulation and depletion regime (Fig. 8.29). This method is reliable for non-irradiated MOS structures, however, a different approach to extract the flat-band voltage is used for the irradiated case [61].

8.2.3 Gate Controlled Diode (GCD)

A Gate Controlled Diode (GCD) is a combination of a MOS capacitor and a diode. Similar to MOS, the main objective of measuring a GCD structure is to characterize the quality of the SiO_2 layer and particularly the Si-$Si0_2$ interface. The parameter which can experimentally measured through a GCD is the surface current I_{surf}. It is proportional to the surface generation velocity (s_0) and consequently to the density of interface trap states D_{it}. Therefore the GCD structure is used for characterizing the Si-SiO_2 interface in terms of interface trap states.

The CMS GCD design features a p-type bulk and a SiO_2 layer with a gate metal atop. Essentially, a MOS capacitor is formed while the GCD oxide thickness is the same as the one of

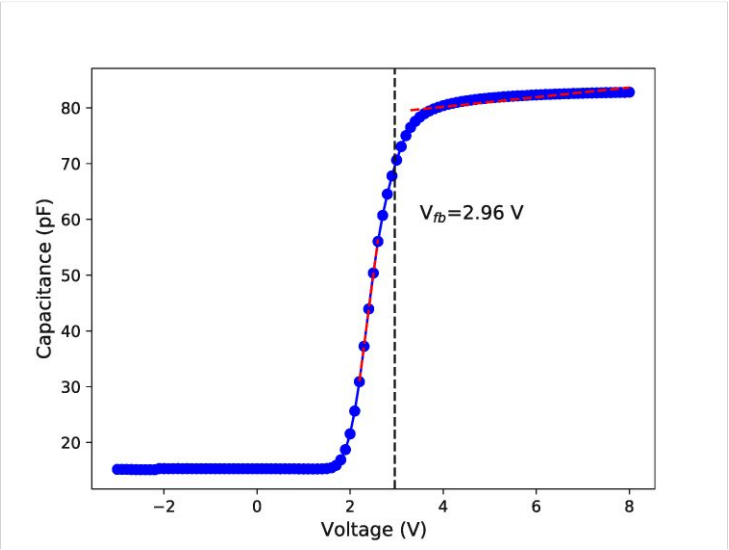


Fig. 8.29: Extracted V_{fb} from a MOS high-frequency C-V curve as the intersection of the linear fits in the accumulation and in the depletion region.

the MOS structure. The gate region is intertwined with n^+ implants which form p-n junctions with the silicon p-bulk. The properties of a MOS capacitor and a diode are combined. The main GCD structure is encircled by a n^+ guard ring and a p^+ edge ring (8.30). Each half-moon hosts two GCDs for automated measurements, one on flute 2 and one on flute 4. Both feature a p-stop implantation which surrounds the diode implant. The addition of a p-stop makes the structure more robust since it allows setting the guard ring to the same potential with the diode contact (section 8.2.1) during measurement and minimizes the impact of parasitic currents driven to the GCD by the surrounding structures. The flute 4 GCD has a wider gate than the flute 2 GCD [88]. In addition, each wafer houses a gate-controlled diode aimed for manual measurements (Fig. 8.31).

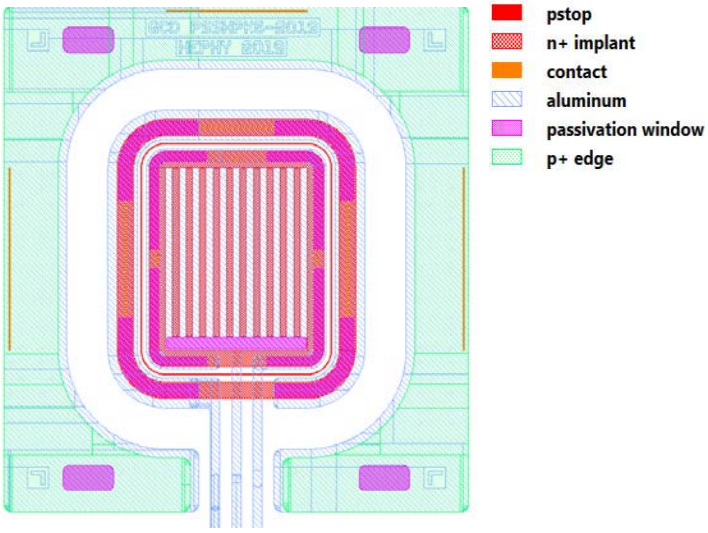


Fig. 8.30: Flute GCD structure with opened edge ring.

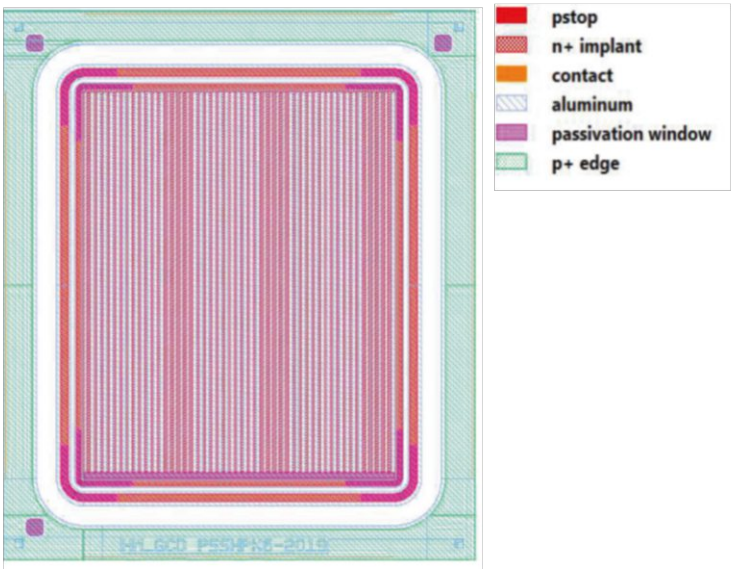


Fig. 8.31: GCD structure for manual measurements.

8.2.3.1 Surface Generation Velocity

The surface current is extracted from a gate-controlled diode through an I-V measurement. From this parameter, the surface generation velocity s_0 can be calculated. The surface generation velocity is correlated to the generation lifetime τ_0 which is the average time needed for the generation of an electron-hole pair in the oxide-silicon interface. A fixed bias voltage is applied to the backside of the GCD setting the structure in a reverse bias mode while a voltage ramp (V_{gate}) is performed on the gate electrode. A depletion region is grown below the n^+ implants as happens in a typical diode. The circuit of a PQC GCD I-V measurement is shown in Fig. 8.32.

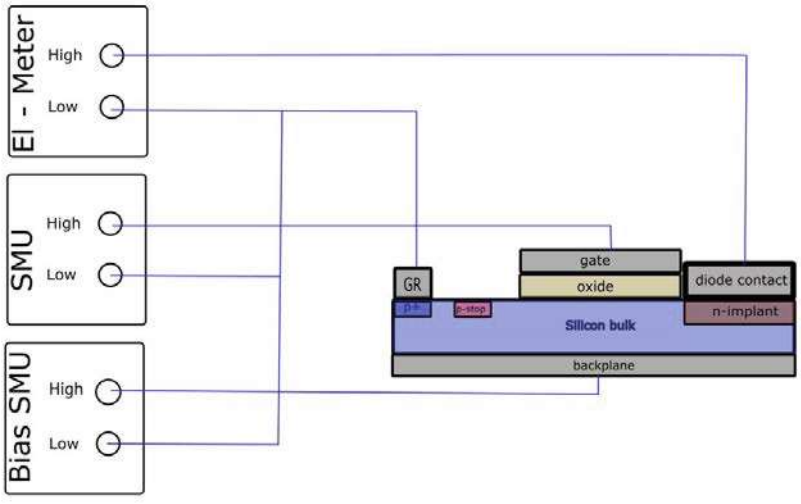


Fig. 8.32: GCD I-V circuit.

While altering the gate voltage from negative to positive values, the region at the Si-SiO_2 interface exhibits the same properties as a MOS capacitor (accumulation, depletion, inversion). An I-V measurement of a CMS Flute GCD structure is displayed in Fig. 8.34, where the three operation states are distinguished. When $V_{gate} < V_{fb}$, the device is in an accumulation state

and only the volume generated current from the diode contributes to the total GCD current. When $V_{gate} > V_{fb}$, a depletion zone is formed below the gate which connects to the depletion region of the diode. The generation-recombination centers at the Si-SiO_2 interface contribute in addition to the diode current [90]. An additional contribution to the total GCD current comes from the depletion zone which grows to the bulk region below the gate metal. Hence, an increase in the total GCD current is observed. For $V_{gate} >> V_{fb}$, the device enters the inversion state and the layer of electrons which builds up below the interface shields the contribution from the interface states. Only the current of the p-n junction plus the current from the depletion zone below the gate are considered in this case. The gate depletion region reaches its maximum width for voltages beyond the inversion voltage, which is why a stabilization in the total current of the structure is observed. To estimate the surface current one should simply subtract the measured current in the inversion layer from the current in the depletion layer such as:

$$I_{surf} = I_{depl} - I_{inv} \tag{8.9}$$

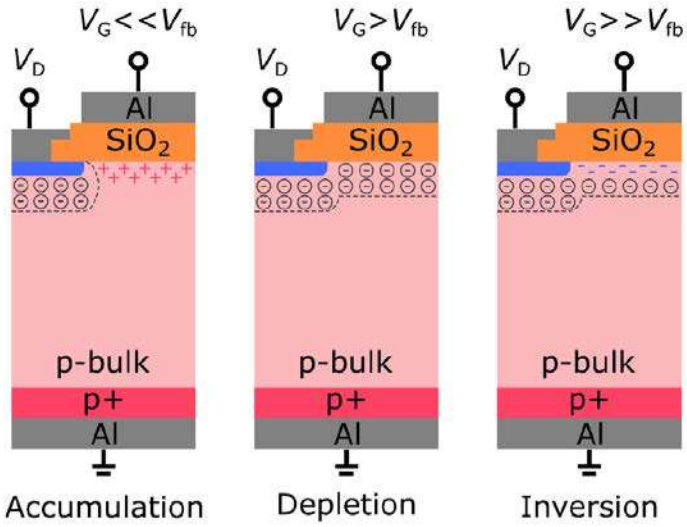


Fig. 8.33: GCD operation states.

The surface generation velocity s_0 can be extracted from the formula:

$$s_0 = \frac{I_{surf}}{qA_{gate}n_i} \tag{8.10}$$

where q is the elementary charge, n_i the intrinsic charge carrier concentration of silicon and A_{gate} the gate area.

If a uniform distribution of bulk and surface centers within the forbidden gap is considered as discussed in [91], the surface generation velocity can be related to the interface trap density D_{it}:

$$D_{it} = \frac{s_0}{\sigma_s u_{th} \pi kT} \tag{8.11}$$

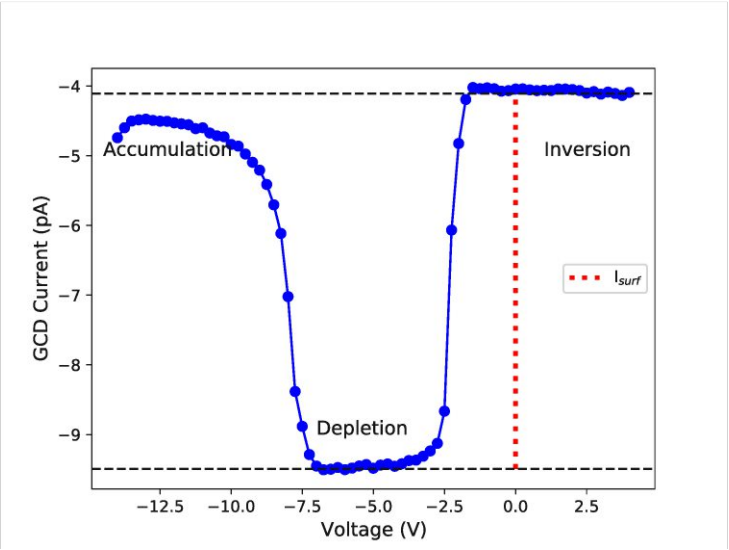


Fig. 8.34: I-V curve of an arbitrary CMS flute GCD structure. The three different states of the device with respect to the applied voltage (accumulation, depletion, inversion) can be are annotated on this plot.

where σ_s is the effective capture cross-section of the interface trapping centers for electrons and holes, u_{th} is the thermal velocity of minority carriers. From formula 8.11 the concentration of interface traps can be defined as:

$$N_{\text{it}} = D_{\text{it}} \frac{E_g}{2} \tag{8.12}$$

8.2.4 Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

The Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is a widely used device in electronics. The property of this device is that its conductivity is controlled by an applied voltage to the gate terminal. The utilization of a MOSFET test structure for quality assurance procedures of silicon sensors is a rather new development for CMS.

The CMS Flute MOSFET device is connected to flute 1. It features a p-type silicon substrate with two heavily n^+ doped rectangular implant regions, namely the source (S) and the drain (D). A SiO_2 layer is deposited on top of the substrate. The oxide features the same thickness as the thick oxide of the main sensor. The two implants share a common gate. The basic difference with a typical MOSFET device is the introduction of p-stop implants which encircle the source and the drain (Fig. 8.35). The geometry of the transistor imitates the interchannel geometry of the main sensor.

One of the main parameters of interest in a MOS field effect transistor is the threshold voltage. As discussed in section 8.2.2, this is the voltage above which an inversion layer between the source and the drain is created. The significance of this parameter for the PQC MOSFET structures is that it acts as an indicator of the quality of the p-stop implant. It has to be noted though, that the threshold voltage depends on various parameters, such as the oxide thickness, the concentration of positive oxide charges in the interface, the channel geometry and the p-stop doping concentration in the case of CMS MOSFETs. Therefore, variations in the threshold voltage should be interpreted in correlation to all the above parameters which can be extracted

from other PQC structures, such as the MOS capacitor (section 8.2.2) or the Van-der-Pauw structure with the p-stop implant (section 8.2.5).

The knowledge of the p-stop doping concentration and the implantation depth is important in order to characterize the implant. An experimental method to extract these parameters through a MOSFET measurement has not yet been implemented by CMS. Nevertheless, a qualitative analysis through the threshold voltage is possible for characterizing the p-stop since, as it is shown in [92], the threshold voltage is sensitive to p-stop doping concentration variations.

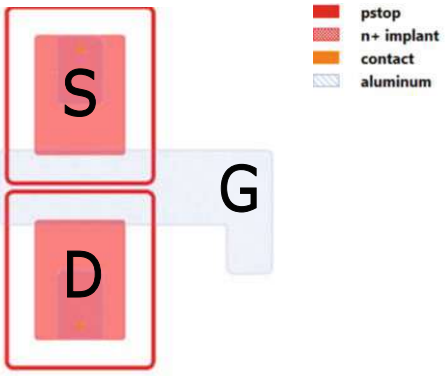


Fig. 8.35: A standard MOSFET test structure with probe contacts. The Source-Drain-Gate terminals are annotated.

The standard MOSFET structure is illustrated in Fig. 8.35. It is optimized for probe card contacts and it is not protected against edge effects. An additional MOSFET with a circular design is incorporated in CMS production wafers (Fig. 8.36). The p^+ implant which surrounds the structure as well as the circular shape of the source and drain make the round MOSFET more robust against external influences than the rectangular structure. Furthermore, structures with the same interchannel spacing but without p-stop implants are implemented to allow for studies of the influence of p-stop implants on channel isolation and threshold voltage. Oval MOSFET test structures with the 20 probe pad design which replicate the 2S and PS-s interchannel layout with and without p-stop implants are included in the set for automated PQC measurements (Fig. 8.1).

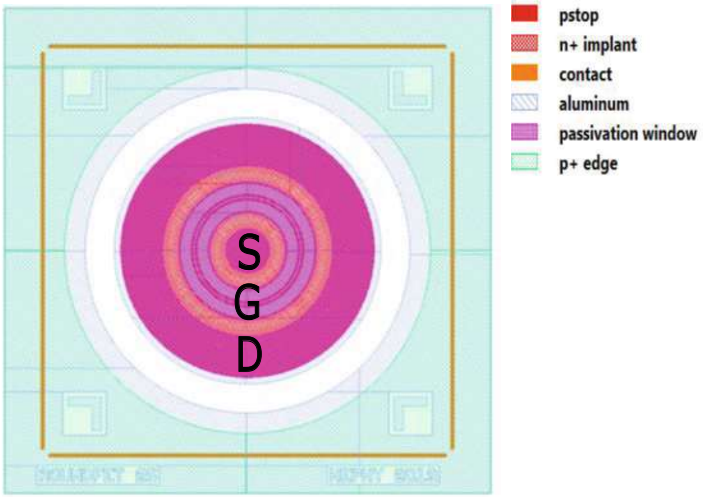


Fig. 8.36: A round MOSFET for manual measurements.

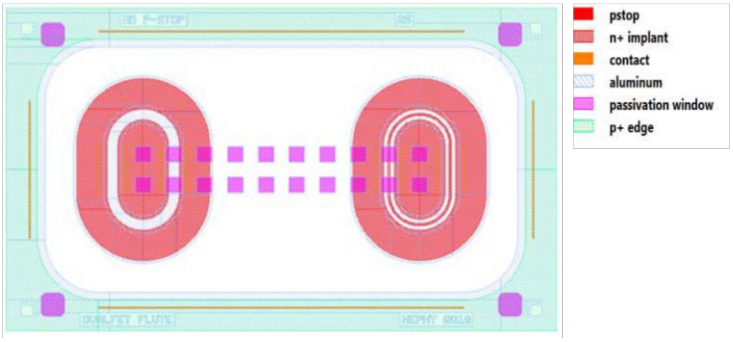
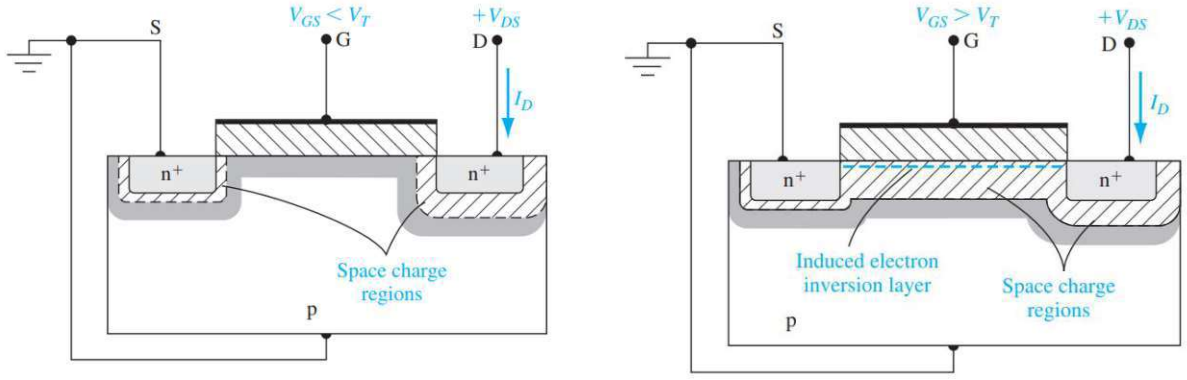


Fig. 8.37: An oval MOSFET structure optimised for flute contacts.

8.2.4.1 Operation principle of MOSFET

Figure 8.38 illustrates the operation state of a nMOSFET (n-type source and drain on a p-type bulk) at a gate voltage below and above the threshold voltage V_{th}. When $V_{\mathrm{G}} > V_{\mathrm{th}}$, the MOSFET has exceeded the threshold inversion point and an inversion layer of electrons is formed near the Si-SiO_2 interface (Fig. 8.38b). Due to the presence of the electron layer between the channels, a channel current can flow if a voltage V_{DS} is applied between the two implants.



(a) nMOSFET state for $V_{\mathrm{G}} < V_{\mathrm{th}}$. **(b)** nMOSFET state for $V_{\mathrm{G}} > V_{\mathrm{th}}$.

Fig. 8.38: nMOSFET states.

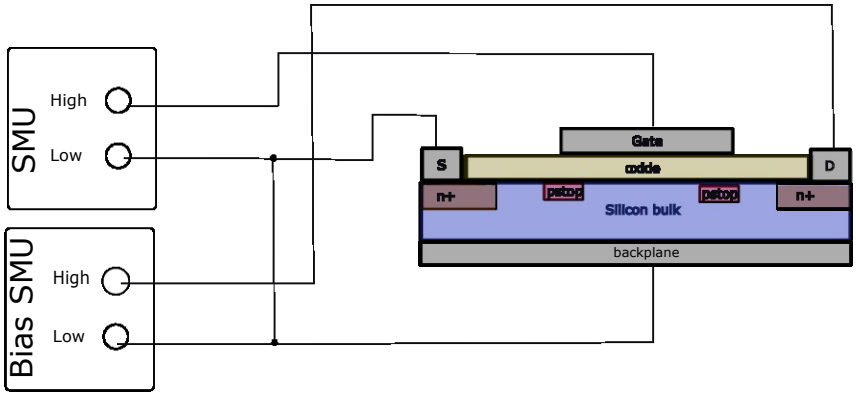


Fig. 8.39: Drawing of circuit for measuring the transfer characteristics of PQC MOSFET.

The channel current or drain-to-source current I_{DS} is defined as [49]:

$$I_{\mathrm{DS}} = \frac{\mu_n W C_{\mathrm{ox}}}{2L}\left[2(V_{\mathrm{G}} - V_{\mathrm{th}})V_{\mathrm{DS}} - V_{\mathrm{DS}}^2\right] \tag{8.13}$$

where W is the channel width, L is the channel length, C_{ox} is the oxide charge and μ_n is the electron mobility.

The change in drain-source current $\mathrm{I_{DS}}$ with respect to a change in the $\mathrm{V_G}$ is defined as transconductance g_m:

$$g_m = \frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{G}}} \overset{(8.13)}{=} \frac{\mu_n W C_{\mathrm{ox}} V_{\mathrm{DS}}}{L} \tag{8.14}$$

The transconductance is independent of the gate voltage at the non-saturation region of the I_{DS}-V_{G} curve. It is proportional to the channel width W and inversely proportional to the channel length. The transconductance is often referred as the *transistor gain*.

For CMS PQC measurements, the drain to source voltage is constant to $V_{\mathrm{DS}} = 100$ mV and the gate voltage varies from -2 V to 6 V with a stepsize of 100 mV. In order to extract the threshold voltage from the transfer characteristics of the transistor, different methods can be deployed. The most widely used method is the so-called *Extraction in the Linear Region* (ELR). The V_{th} is extracted as the intersection point of the tangent applied to the transfer characteristics and the voltage axis. The tangent is applied to the point at which the transconductance g_m maximizes. An example of the application of this method in PQC data is shown in Fig. 8.40.

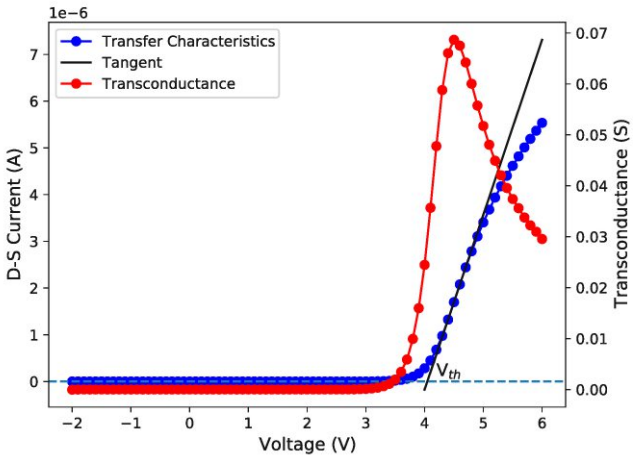


Fig. 8.40: Transfer characteristics of MOSFET with extrapolation in linear region method.

The introduction of heavily doped $\mathrm{p^+}$ implants between the drain and the source shifts the threshold voltage of a nMOSFET to larger values. An example can be seen in Fig. 8.41 which compares two identical 2S round MOSFET structures from the same half-moon, one with a p-stop and one without any p-stop between the source and drain. The round MOSFET without p-stop features a $\mathrm{V_{th}}$ = -2.01 V while the structure with the implant has a $\mathrm{V_{th}}$ = 2.59 V.

The substrate bias effect

As illustrated in Fig. 8.39, in the standard PQC measurement procedure the bulk and the source are set to the same, ground potential. Assuming that the bulk is set to a more negative

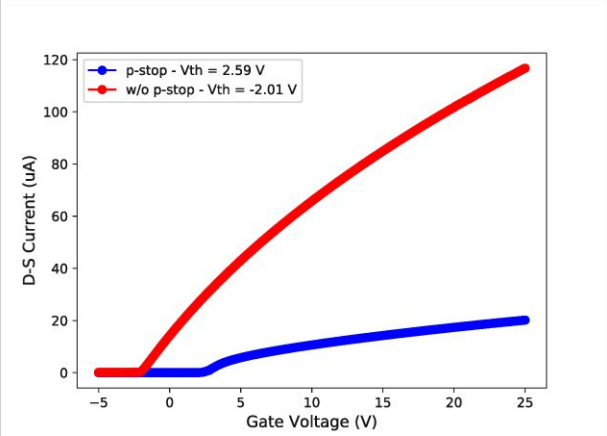


Fig. 8.41: Comparison of 2S round MOSFET transfer characteristics with p-stop (blue) and without p-stop (red).

potential with respect to the source ($V_{SB} > 0$), the depletion region becomes larger and the space charge density also increases. To reach the inversion point, the applied gate voltage must also increase in order to compensate for the change in space charge density [49].

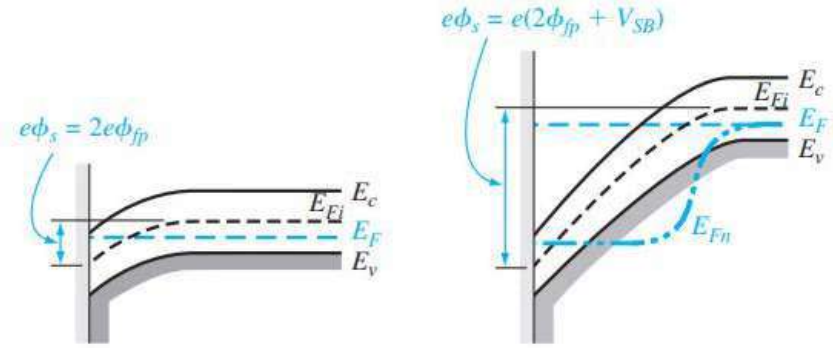


Fig. 8.42: Band bending diagram for $V_{SB} = 0$ (left) and $V_{SB} < 0$ (right).

When no substrate bias is applied ($V_{SB} = 0$), the charge density is given by:

$$Q_d = -x_d q N_A = -\sqrt{2qN_A\epsilon_{si}\phi_s} \tag{8.15}$$

where x_d is the depletion region, qN_A is the space charge density and ϕ_s is the surface potential. For $V_{SB} > 0$, the space charge density is:

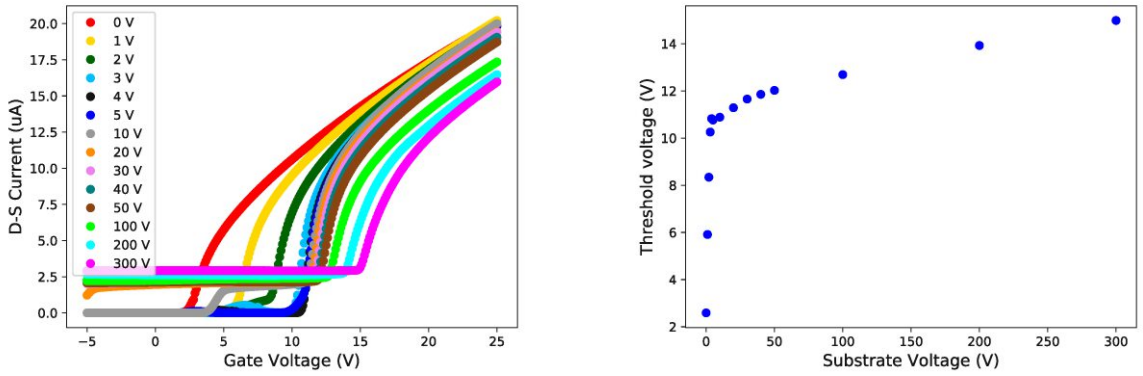
$$Q'_d = -\sqrt{2qN_A\epsilon_{si}(\phi_s + V_{SB})} \tag{8.16}$$

The threshold voltage under biased substrate is given:

$$V_{th} = V_{th}^{V_{SB}=0} - \frac{\Delta Q'_d}{C_{ox}} = V_{T0} + \frac{\sqrt{2qN_A\epsilon_{si}}}{C_{ox}}\left[\sqrt{(\phi_s + V_{SB})} - \sqrt{\phi_s}\right] \tag{8.17}$$

According to the formula 8.17, the threshold voltage increases as a function of the source to substrate voltage. For a certain MOSFET structure and varying substrate voltage, the increase of the threshold voltage should follow the square root of the V_{SB}. The behavior of a 2S MOSFET

structure with respect to different substrate voltages is investigated in Fig. 8.43. The drain to source voltage was fixed to 100 mV. The transfer characteristics of the structure for different substrate bias voltage is given in Fig. 8.43a while the extracted V_{th} over the applied bias voltage is shown in Fig. 8.43b. The depletion width increases with bias voltage and so does the measured current in depletion mode (for gate voltage below the V_{th}), as shown in Fig. 8.43a.



(a) Transfer characteristics. **(b)** Threshold voltage over bias voltage.

Fig. 8.43: Dependence of transfer characteristics of 2S MOSFET structure on V_{bias}.

8.2.5 Van-der-Pauw structures

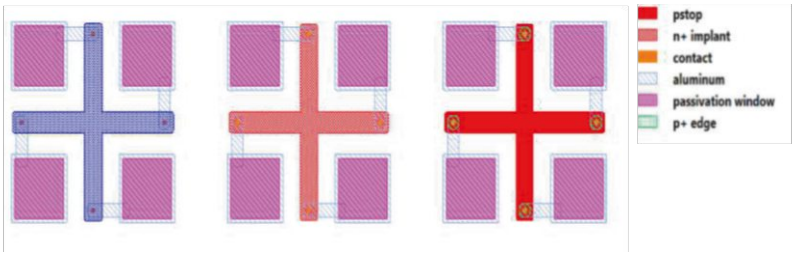
The Van-der-Pauw (VdP) structures are standard test structures in the semiconductor industry which are used to measure material parameters such as electrical conductivity, resistivity, the doping density. Through the Van-der-Pauw four-wire method, one can measure the sheet resistance of thin films. The structures should be homogeneous and uniformly thick and the contacts should be placed at the edges of the sample [93].

CMS production wafers include several Van-der-Pauw structures of different implantation types. Dedicated structures are developed for characterizing the n^+ (strip implant) layers, the p-stop implants, the p^+ edge layers, the polysilicon layers and the aluminum metalization (Fig. 8.48). The typical design of VdP structures resembles a Greek cross with four symmetrical contact pads at the edges. This structure allows a 4-point resistance measurement. Apart from the cross-like structures, CMS production wafers house clover-leaf structures of the metal layer (Fig. 8.44b). This special design is adapted in order to minimize the measurement errors that become significant in the case of aluminum layers which feature very low sheet resistance in the order of tens mΩ/sq [73].

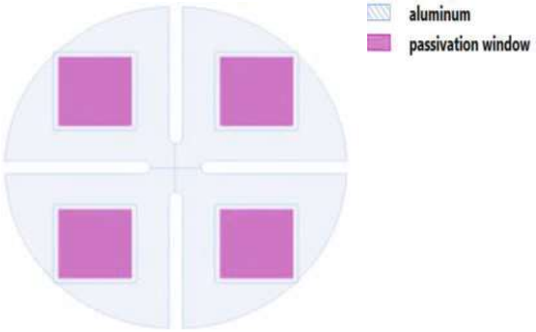
The sheet resistance of a thin film R_{sheet} is defined as the ratio of resistivity of the layer ρ over its thickness t:

$$R_{sheet} = \frac{\rho}{t} \tag{8.18}$$

where R_{sheet} is measured in units of Ω/sq. A square is the ratio of length L over width W of the layer (Fig. 8.45).



(a) Standard cross Van der Pauw structure.



(b) Clover leaf structure.

Fig. 8.44: Illustration of different Van-der-Pauw structures implemented in CMS Outer Tracker wafers.

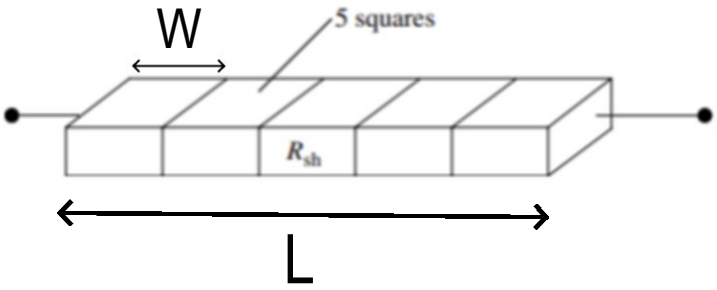


Fig. 8.45: A sketch of 5 squares of an arbitrary implant where the width W and the length L are annotated. The sketch is a modified version taken from [93].

For symmetrical structures such as the cross VdP, the sheet resistance R_{sheet} can be extracted experimentally from the formula:

$$R_{\text{sheet}} = \frac{\pi}{\ln 2} \frac{V}{I} \tag{8.19}$$

The configuration of the pads at which the voltage is applied and the current is measured can be seen in Fig. 8.46. The current ramp varies according to the respective VdP structure. The I-V curve of a n^+ implant cross VdP is illustrated in Fig. 8.47 as an example.

8.2.6 Line width

The line width structure aims to determine the smallest of the two lateral dimensions of a layer. The line width structures of CMS production wafers feature two different designs. There are two simple bridge structures which are located in flute 2 and feature a n^+ and a p-stop

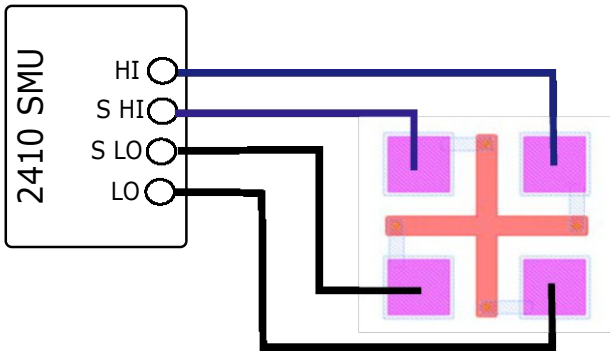


Fig. 8.46: Circuit for IV measurement of p-stop cross Van der Pauw structure.

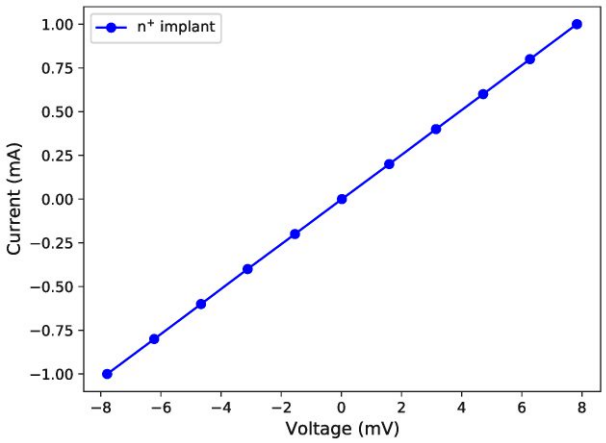


Fig. 8.47: I-V curve of a n^+ Van der Pauw cross structure.

implant (Fig. 8.48b). Additionally, there is a bridge structure in combination with a Van der Pauw cross (cross-bridge) which is located in flute 3 and features a p^+ implant (Fig. 8.48a).

For a cross-bridge, the calculation of line width depends on the extraction of R_{sheet} which is assumed to be the same across the whole structure. Based on the configuration shown in Fig. 8.48a, the line width w can be defined as:

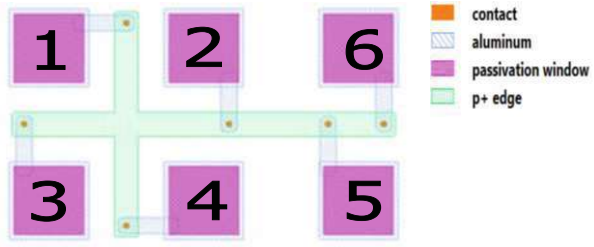
$$w = \frac{R_{\text{sheet}} d_{25} I_{36}}{V_{25}} \tag{8.20}$$

where d_{25} is the distance between contacts 2 and 5, I_{36} is the current which flows between contacts 3 and 6, and V_{25} is the voltage between contacts 2 and 5.

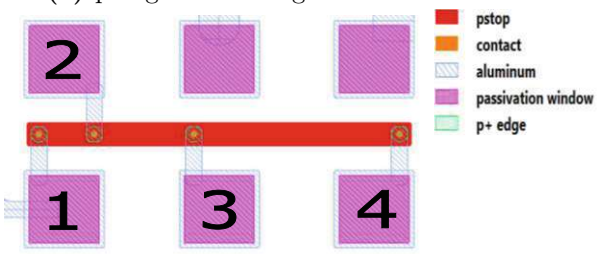
For a bridge line width (Fig. 8.48b), the determination of w is given by:

$$w = \frac{R_{\text{sheet}} d_{23} I_{14}}{V_{23}} \tag{8.21}$$

where the current I_{14} flows between pads 1 and 4 while the voltage is measured between pads 2 and 3. In this case R_{sheet} must be calculated from the respective VdP structure, under the assumption that the sheet resistance of the line width is the same.



(a) p-edge cross-bridge line width structure.



(b) Assymetric p-stop bridge line width structure.

Fig. 8.48: Types of line width test structures.

8.2.7 Four-terminal resistivity cross

The four-point measurement technique is a standard way in industry to determine the wafer resistivity. CMS production wafers host dedicated structures which allow a four-terminal resistivity measurement as an alternative method to the standard diode C-V measurements.

The 4-point structure follows the design of Van-der-Pauw structures with four contact pads to be placed symmetrically at four corners. Heavily doped p^+ implants are placed under the contact holes in order to establish good ohmic contacts with the p-type bulk. A thin n^+ cross-shaped implant surrounds the contacts in order to form a p-n junction with the bulk. An illustration of the bulk resistivity Van-der-Pauw structure which is located in flute 3 is given in Fig. 8.49.

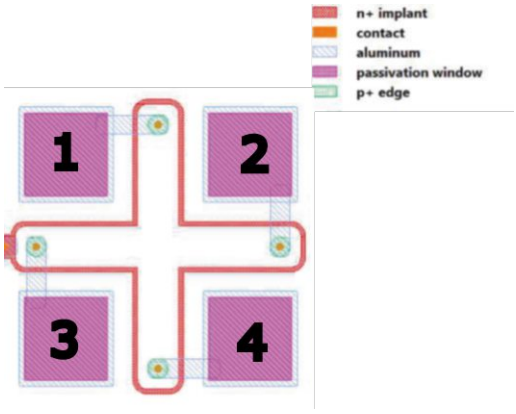


Fig. 8.49: Bulk resistivity VdP structure with a surrounding n^+ implant.

The geometry of the structure must be taken into account when extracting the resistivity. As discussed in [93], the voltage at a point P with a distance r from the probe which induces a current I is given as:

$$V = \frac{I\rho}{2\pi r} \tag{8.22}$$

Assuming the configuration shown in Fig. 8.49, 8.51, where the current flows from pad 1 to pad 2, the potential difference between pads 3 and 4 would be:

$$\begin{aligned} V_3 - V_4 &= (\phi_{31} + \phi_{32}) - (\phi_{41} + \phi_{42}) \\ &= \frac{I\rho}{2\pi}\left[\left(\frac{1}{s} - \frac{1}{\sqrt{2}s}\right) - \left(\frac{1}{\sqrt{2}s} - \frac{1}{s}\right)\right] \\ &= \frac{I\rho}{2\pi}\left(\frac{2-\sqrt{2}}{\sqrt{2}}\right) \end{aligned} \tag{8.23}$$

where s is the distance of two adjacent pads.

Combining (8.22), (8.23), the resistivity can be written as:

$$\rho = \frac{2\pi s}{2-\sqrt{2}}\frac{V_{34}}{I_{12}} \tag{8.24}$$

The equation (8.24) holds true for the case of a semi-infinite, lateral or vertical bulk dimension [93]. For the structures of CMS wafers, equation (8.24) should include a correction factor F, such as:

$$\rho = \frac{2\pi sF}{2-\sqrt{2}}\frac{V_{34}}{I_{12}} \tag{8.25}$$

where for bulk thickness of $d = 290$ µm and a pad distance of $s = 187$ µm, the correction factor is $F = 1.081$.

An alternative design of a four-point resistivity test structure is included in CMS wafers. This structure features four equally spaced contacts to the silicon bulk that are routed to the probe needle pads (Fig. 8.50). The resistivity in that case can be calculated by the formula:

$$\rho = 2\pi sF\frac{V_{23}}{I_{14}} \tag{8.26}$$

where s is the contact spacing, V_{23} is the voltage measured between contacts 2 and 3, I_{14} is the current flowing from pad 1 to 4 and F is the correction factor. The correction factor takes into consideration the probe location near the sample edges, the sample thickness, the diameter, the temperature as well as the probe placement [93].

8.2.8 Meander structures

Meander structures are developed on the CMS production wafers in order to measure the resistivity of the polysilicon implant and the aluminum. The polysilicon meander structure is located in flute 2 (Fig. 8.52). The implant has a design width of 5 µm with 476 squares. It features the same dimensions as the bias resistor of the main sensor. The aluminum meander is

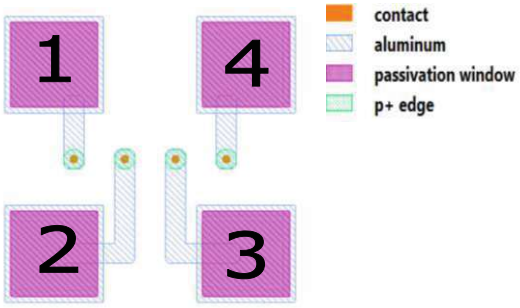


Fig. 8.50: Standard bulk resistivity four-terminal structure.

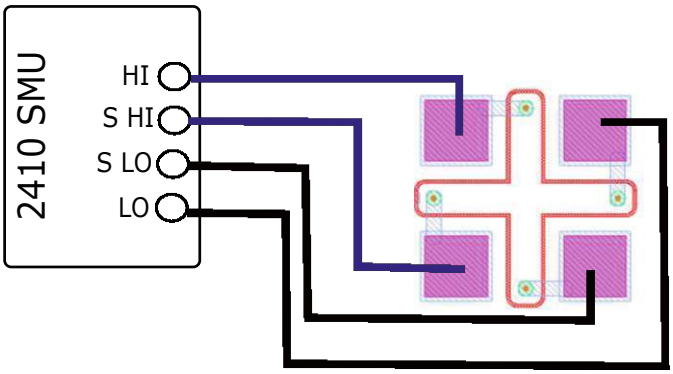


Fig. 8.51: Drawing of the circuit for a VdP resistivity measurement.

located in flute 3 (Fig. 8.53). It features a strip with a design width of 10 µm and consists of 12852 squares. The structure surrounds the flute 3 diode, as it is shown in Fig. 8.5a.

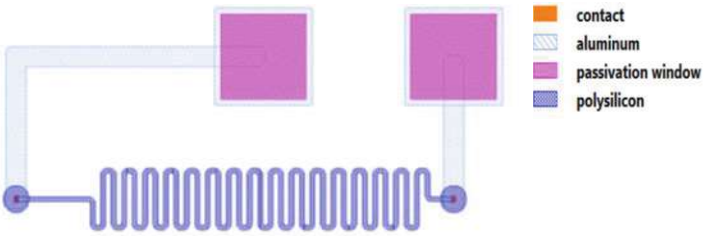


Fig. 8.52: Polysilicon meander featuring the same shape and size with the bias resistor.

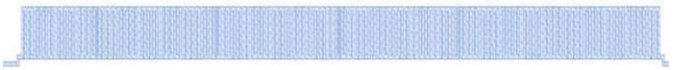


Fig. 8.53: Illustration of a segment of the aluminum meander structure.

The typical measurement on a meander structure is an I-V from the slope of which, the meander resistance R can be determined. After measuring the resistance, the specific resistivity ρ/sq can be calculated, according to the formula:

$$\frac{\rho}{\mathrm{sq}} = R\frac{w}{l}$$

where w is the width of the square and l is the length of the strip. The resistance of the polysilicon resistor is extracted from a 2-terminal current-voltage measurement with a voltage ramp from -100 mV to 100 mV with a stepsize of 25 mV. For the aluminum meander, a 4-terminal I-V measurement is performed with a ramp from -1 mA to 1 mA with a stepsize of 50 µA. An example of a metal meander I-V curve is shown in Fig. 8.54.

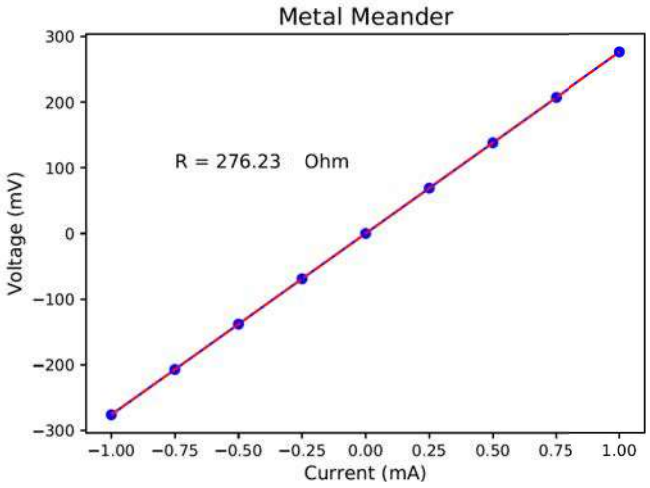


Fig. 8.54: Aluminum meander I-V curve.

8.2.9 Capacitor with n^+ implant

The coupling capacitor structure with a n^+ implant is a dedicated structure for determining the properties of the coupling, thin oxide. The structure is located in flute 1. A metal and a n^+ implant are separated by a dielectric layer which is the same oxide developed between the implant and the metal in the AC-coupled Outer Tracker sensors. By measuring the capacitance of the capacitor, the thickness of the coupling dielectric can be calculated. The coupling oxide thickness should be uniform over production time since it is a decisive factor for the strip coupling capacitance. The capacitor structure is hosted also on the PS-p wafers, although they are DC-coupled.

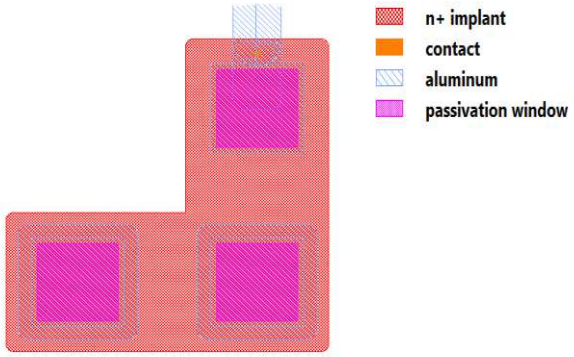


Fig. 8.55: Capacitor test structure with n^+ implant.

Regarding the design of the capacitor structure, one electrode features a contact through the oxide to the n^+ implant while the other two electrodes are placed atop the dielectric oxide. A voltage difference is set between the implant and the metal electrode with a voltage ramp from -2 V to 2 V and a stepsize of 0.5 V. At each voltage step, the capacitance is measured by the LCR meter. The LCR frequency is set to 10 kHz and the voltage amplitude to 250 mV. The coupling capacitance of the structure is extracted through averaging over all measured values. An illustration of the circuit for the capacitor measurement is given in Fig 8.56.

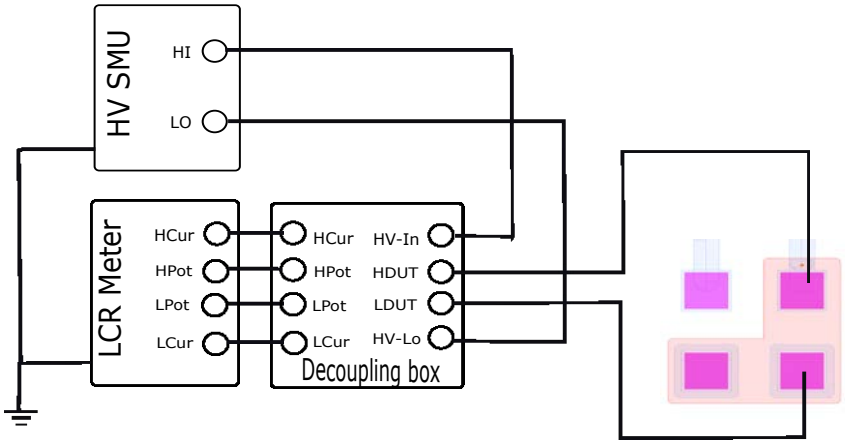


Fig. 8.56: PQC capacitor measurement at HEPHY.

The electrode size of the capacitor is 130 µm × 130 µm. The CMS specification for the coupling capacitance is $C_{Cac} > 1.2$ pFcm^{-1}µm^{-1} per implant length and width. This means that for the capacitor structure with the above dimensions, a value larger than $1.2 \times 0.13 \times 130 = 2.028$ pF is expected. Figure 8.57 shows an example of a capacitor structure C-V measurement from a production wafer. The mean capacitance is 2.4 pF which is well above the limit. This value corresponds to a coupling oxide thickness of $d_{ox} = 243$ nm.

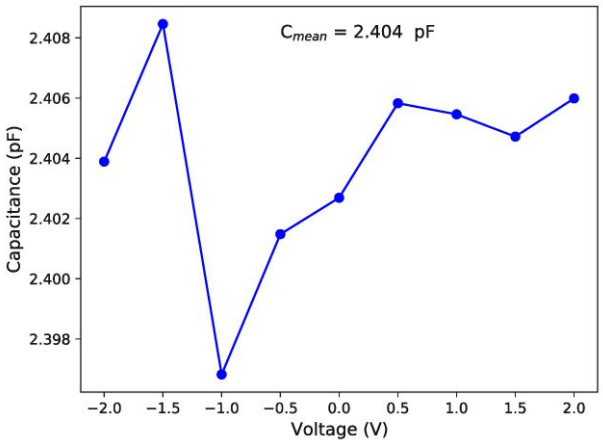


Fig. 8.57: Capacitor with n^+ implant C-V measurement as performed by CMS.

8.2.10 Dielectric breakdown structure

High voltage stability is a crucial property that should characterize the thin oxide of the AC-coupled sensors. The dielectric strength of the oxide scales with its thickness. If the applied voltage generates an electric field across the oxide which exceeds the oxide dielectric strength, then the oxide will experience an electric breakdown. The breakdown voltage corresponds to the minimum voltage that should be applied between the n^+ implant and the metal in order to create a flow of a substantial amount of current in the dielectric. In the actual conditions of the CMS experiment, a high potential across the coupling capacitor can be developed during a beam loss scenario. In such a case, large amounts of charge are deposited in the detector which can set the strip implants to a much higher voltage with respect to the readout electrode. If the voltage across the coupling capacitor exceeds the breakdown voltage of the oxide, it can have a destructive effect, such as creating a short between the implant and the metal. Therefore, the coupling oxide should be robust and exhibit a high breakdown voltage. The CMS specification for the breakdown voltage of the thin oxide is $V_{bd} > 150$ V.

Test structures are implemented on CMS wafers to examine the breakdown voltage of the thin oxide. The idea is to perform potentially destructive tests on the structure which is not possible to be done in the main sensor without creating permanent damage on the oxide crystal. The standard dielectric breakdown structure which is included in PQC measurements is illustrated in Fig. 9.45. It is located in flute 2. One pad is connected directly through the oxide to the n^+ implant. The other three contact pads form a capacitor with the oxide and the underlying implant. An I-V is performed on the structure in order to extract the breakdown voltage. For the measurement, a positive voltage ramp is applied to the pad which is directly connected to the implant while one of the metal electrodes is set to ground potential. The measurement circuit is given in Fig 8.59. The ramp goes from 0 V to 200 V with a stepsize of 5 V. As it is shown in section 9.7, no breakdown is typically observed up to 200 V.

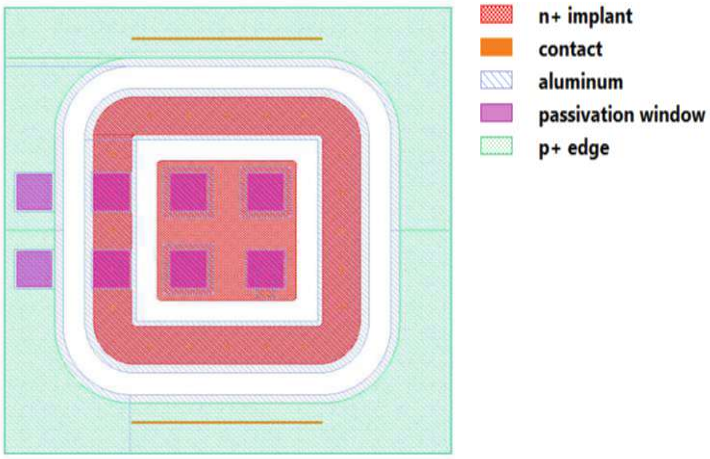


Fig. 8.58: Dielectric breakdown structure.

A high breakdown voltage of the thin oxide over production is desirable which would hint a stability in the thin oxide growth process. An example of an I-V behavior of the thin oxide with a breakdown shown beyond 175 V is illustrated in Fig. 8.60.

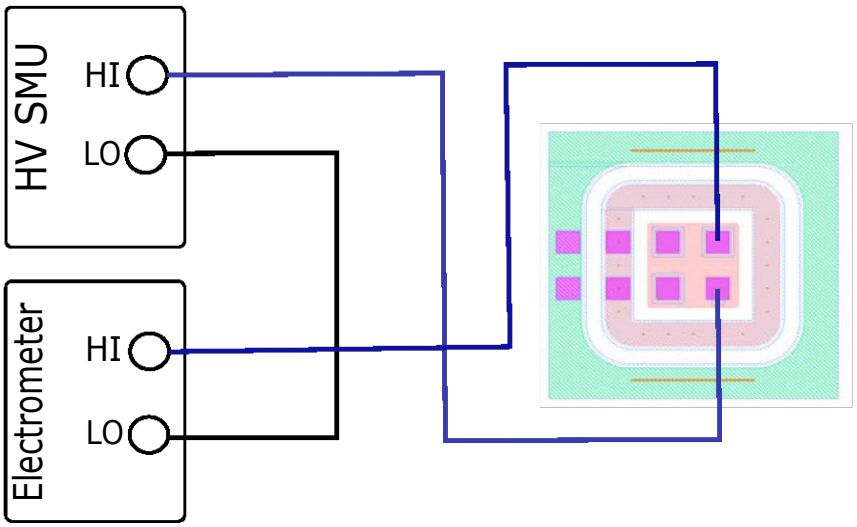


Fig. 8.59: Circuit for measuring the I-V characteristics of the dielectric breakdown structure.

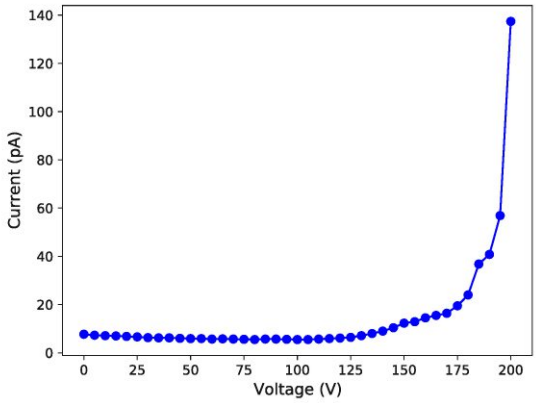


Fig. 8.60: The I-V curve of a dielectric breakdown structure from a production wafer.

8.2.11 Cross Bridge Kelvin Resistor

The Cross bridge Kelvin Resistor (CBKR) is a structure that is used in the semiconductor industry to characterize the metal-semiconductor contact and in particular its resistance. This is done through a measurement of the specific contact resistance ρ_c. Two types of CBKR structures are housed on the CMS wafers: one structure to measure the resistance of the contact between the metal and the n^+ implant and one structure that measures the resistance of the contact between the metal and the polysilicon implant (Fig. 8.61).

The measurement configuration of a n^+ implant CBKR structure is displayed in Fig. 8.62. A voltage difference is applied between a pad connected to the metal and a pad connected to the implant while the output voltage is measured between the other two pads. A voltage drop between the two measured points is expected due to the contact resistance R_c.

According to the 1-D Kelvin model the specific contact resistance can be extracted from the formula $\rho_c = R_c/A$, where A is the contact area. However, this model does not account for the current flowing in the overlap region between the contact edge and the underlying n^+ implant sidewall [94]. This contribution is non-negligible when the contact size is smaller than the

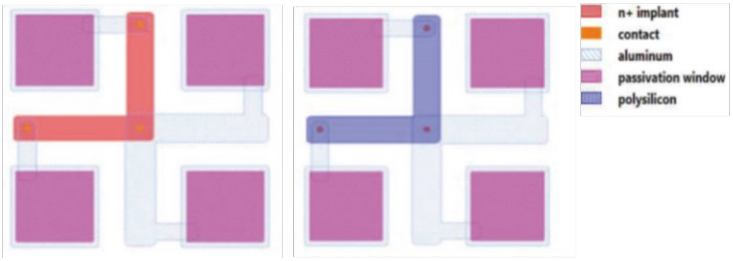


Fig. 8.61: Cross bridge Kelvin Structure with four terminals as implemented on CMS production wafers. On the left is the CBKR structure with the n^+ implant and on the right is the metal-to-polysilicon CBKR.

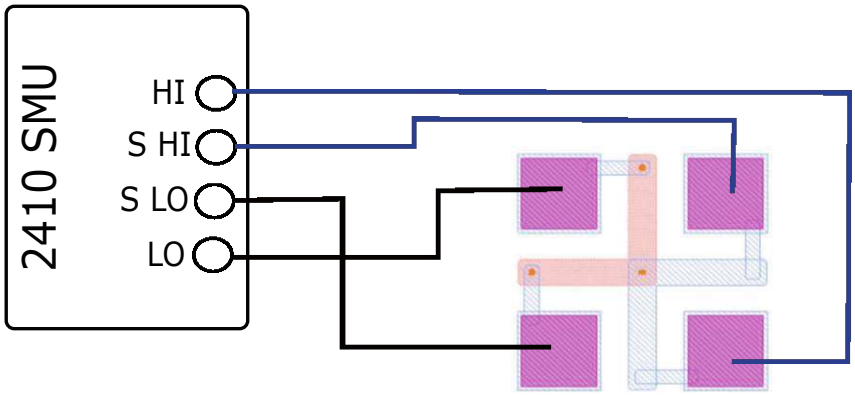


Fig. 8.62: Drawing of circuit for I-V measurement of n^+ CBKR structure.

underlying implant. In that case, a 2-D approach should be adopted as described in [95]. This model considers also the contribution of a resistance R_{geom} due to the aforementioned current around the overlap region. Therefore, the contact resistance R_c should be the difference between the measured resistance R_{meas} and R_{geom}:

$$R_c = R_{meas} - R_{geom} = \frac{V}{I} - \frac{4R_{sh}d^2}{3w^2}\left(1 + \frac{d}{2(w-d)}\right) \tag{8.27}$$

where R_{sh} is the sheet resistance of the implant or polysilicon, w is the corresponding linewidth and d is the distance between the contact edge and the overlap region (Fig. 8.63).

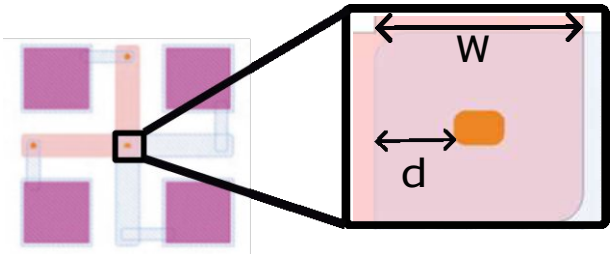


Fig. 8.63: Enlarged view of the contact between the n^+ implant and the metal.

A current-voltage measurement is performed on the n^+ CBKR structure with a current ramp from -100 µA to 100 µA and a stepsize of 20 µA. For the polysilicon CBKR, the ramp goes from -1 µA to 1 µA with a stepsize of 0.05 µA. An I-V measurement from an arbitrary n^+ CBKR is

illustrated in Figure 8.64

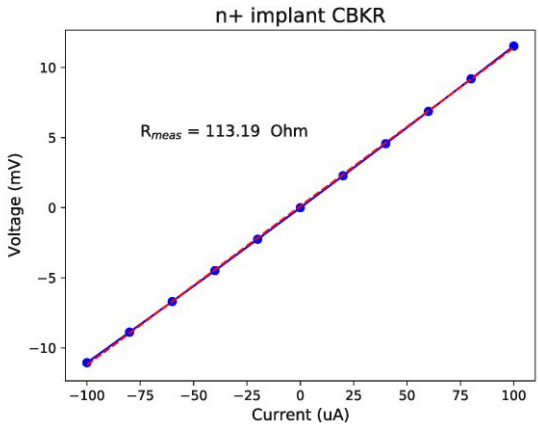


Fig. 8.64: I-V curve of a n^+ CBKR structure.

8.2.12 Contact Chain

The contact chain is a test structure that characterizes the quality of the metal to n^+ implant, p^+ edge and poly-silicon contact. A region of implant or polysilicon connected with small contact holes to an overlying metal is replicated multiple times, forming a sequence resembling a chain (Fig. 8.65). Each structure includes 228 contact holes in total. Three contact chains encircle the fourth flute, one for each of the implants mentioned above. The n^+ chain is surrounded by a p-stop implant and the p^+ edge is encircled by a n^+ implant in order to be isolated from their neighboring structures. Even a single problematic contact hole can lead to a significant increase in the total resistance of the whole contact chain. The total resistance of a contact chain for N consecutive implant or poly-silicon layers and 2N contact holes is given by the formula [93]:

$$R_{tot} = \frac{NR_{sh}d}{w} + 2NR_c \tag{8.28}$$

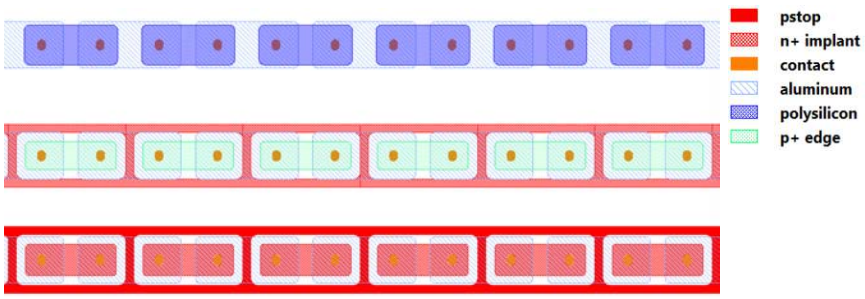


Fig. 8.65: Segment of the contact chain structure with polysilicon, p^+-edge and n^+ implants.

For the measurement of the n^+ and the p^+ implant contact chain, a current ramp from -10 µA to 10 µA with a stepsize of 0.1 µA is applied while the voltage drop across the structure is measured for each step. For the polysilicon contact chain, the current ramp goes from -10 nA to 10 nA with a stepsize of 1 nA. An example of an I-V measurement of a n^+ contact chain is given in Fig. 8.66.

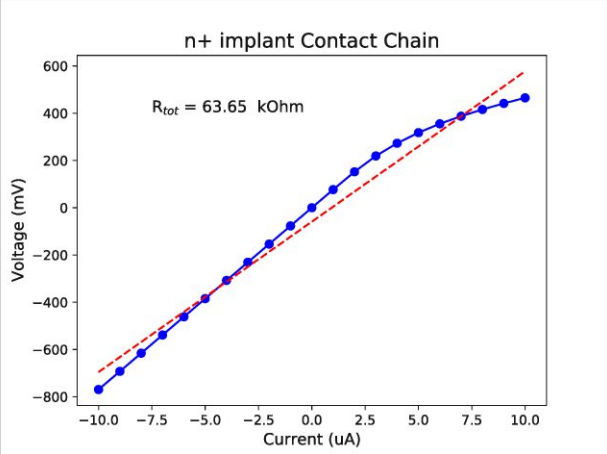


Fig. 8.66: I-V curve of a n^+ contact chain structure.

8.3 The PQC setup at HEPHY

The PQC probe station at HEPHY is designed for performing automated and manual measurements on test structures. The probe station is enclosed by a light-tight box which acts as a Faraday cage, shielding the setup from external electromagnetic fields. The devices under test (DUT) are placed on a vacuum jig which features vacuum holes with switchable vacuum. The high voltage is applied from the jig to the backside of the structures while heat pumps (Peltier elements) can heat the surface of the chuck and an external chiller can provide a cooling to the table. The temperature of the chuck can be monitored via a temperature sensor which is embedded into the jig. The system is mounted on top of a x-y-z stage which can move along all 3 directions with a micrometer precision. Up to four CMS tracker half-moons can be placed onto the table and be tested in one run (Fig. 8.67b). The humidity inside the box can be controlled through a dry air system. A probe card with 20 needles is installed at the rear side of the box while at the front side, two platforms are mounted on both sides of the chuck which host the manual micro-positioners. A camera, aligned to the probe card provides visual help during contacting the flute pads with the probe card needles. A microscope with a mounted camera is also installed inside the probe station and can facilitate manual contact with the micro-positioners. The inner side of the light-tight box is shown in Fig. 8.67c.

Outside of the probe station, a rack houses all the instruments used for the electrical measurements (Fig. 8.67a). The used devices are two Keithley 2410 voltage source meters, a Keithley 6517B electrometer, a Keysight 4980A precision LCR meter, and a Keithley 707B switching matrix with three 8×12 matrix cards. All the channels of the matrix are connected to the probe card and the manual micro-positioners. A custom-made environment control system is equipped with multiple functionalities such as monitoring the temperature and relative humidity inside the probe station, controlling the light of the microscope and probe card camera as well as a laser switch which prevents the x-y-z stage from crashing into the probe card while moving.

The whole setup is controlled by a python, custom-made software, similar to the one used in the SQC setup at HEPHY. More detailed information regarding the PQC software is given in [88] and further optimizations in the software and the automated analysis are given in [96].

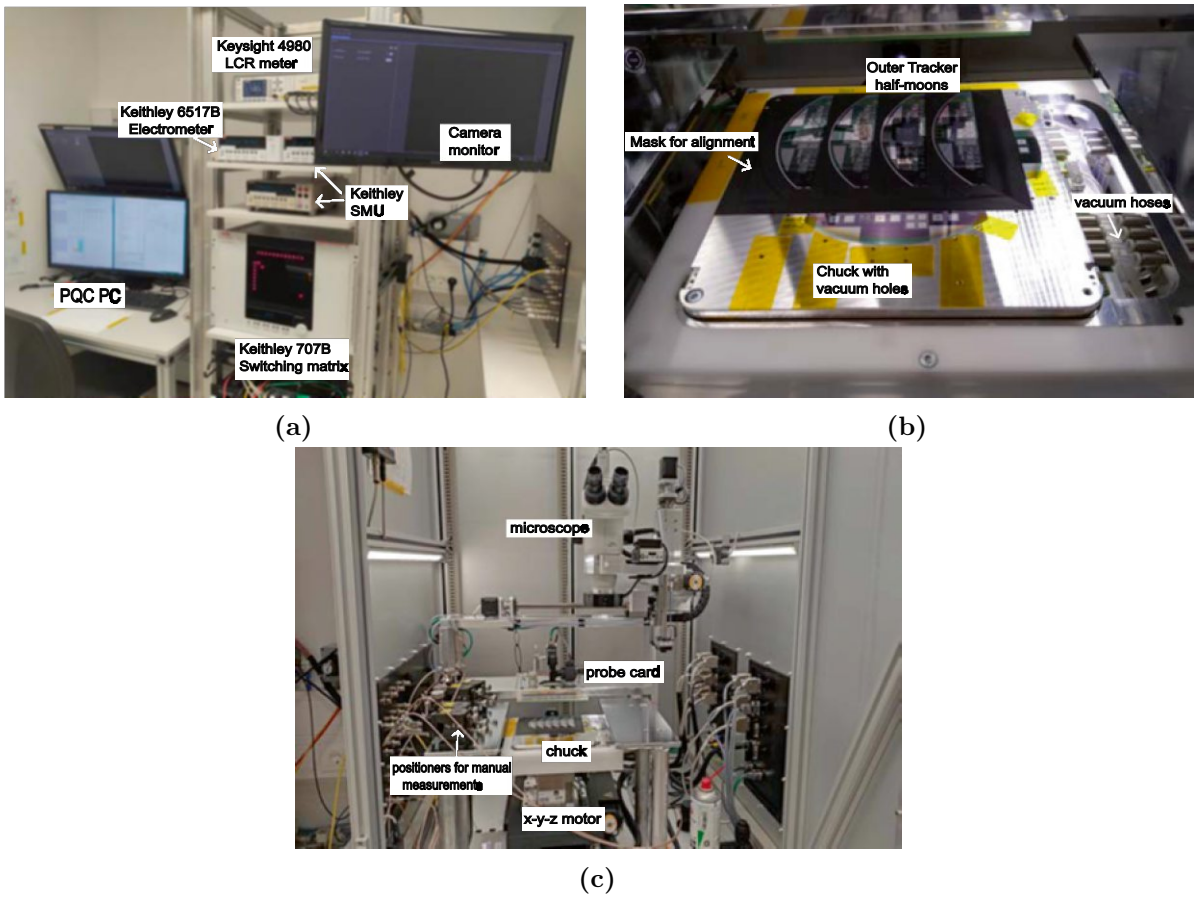


Fig. 8.67: The custom-made PQC setup at HEPHY. Pictures of the instruments and the PC with the software (a), the alignment of the four half-moons on the jig (b) and the box that encloses the probe station (c) are given.

8.4 The PQC workflow

The Process Quality Control of each production batch includes the characterization of a minimum 8 wafers. The wafers for qualification are selected based on the I-V results of the main sensors, as measured by HPK. The flutes 1 - 4 which are tested in PQC are mirrored twice in each of the North, West and East half-moons, as discussed in section 8.1. The West and East half-moons are characterized for each selected wafer. Therefore, for a number of 8 selected wafers, in total 16 half-moons are tested. Figure 8.68 shows a picture of a 2S East half-moon. The convention is that only the left side of each half-moon is measured. In addition, the right side of the half-moon is tested, only for the flute 1 structures, such as the MOSFET and the Van-der-Pauw for p-stop, polysilicon and strip implants, for which a more in-depth investigation of the uniformity across the wafer is performed. Figure 8.69 illustrates a 2S batch table with the parameters measured on the structures of flute 1.

Fig. 8.68: Picture of an East half-moon from a 2S production wafer.

Halfmoon	Vth	Vfb	C_acc	Tox	Nox	VdP_Rpoly (S)	VdP_Rpoly (R)	VdP_N+ (S)	VdP_N+ (R)	VdP_Pstop (S)	Vdp_Pstop (R)	Capacitor (L)	Capacitor (R)
	[V]	[V]	[pF]	[nm]	[cm^-2]	[kOhm/sq]	[kOhm/sq]	[kOhm/sq]	[kOhm/sq]	[kOhm/sq]	[kOhm/sq]	[pF]	[pF]
47354_005_2-S_HM_EL	3.02	2.85	81.5	704.4	10.8	1.86	1.9	35.8	35.5	18.8	18.5	2.44	2.32
47354_005_2-S_HM_ER	4.48	---	---	---	---	1.87	1.87	35.4	35.6	19.2	19.1	---	---
47354_005_2-S_HM_WL	4.44	2.83	80.7	711.9	10.7	1.89	1.89	36.3	35.5	19.5	19.3	2.43	2.33
47354_005_2-S_HM_WR	4.53	---	---	---	---	1.91	1.89	39.3	39.3	20.0	19.9	---	---
47354_013_2-S_HM_EL	4.52	2.91	81.9	701.2	11.1	1.84	1.85	35.6	35.6	18.8	18.9	2.42	2.35
47354_013_2-S_HM_ER	---	---	---	---	---	1.85	1.85	35.6	35.5	19.6	19.4	---	---
47354_013_2-S_HM_WL	5.4	2.93	80.4	714.5	10.9	1.89	1.85	35.7	35.6	19.3	19.2	2.4	2.32
47354_013_2-S_HM_WR	4.47	---	---	---	---	1.88	1.88	35.6	35.8	19.1	19.1	---	---
47354_014_2-S_HM_EL	4.62	2.91	80.9	710.0	10.9	1.85	1.86	35.3	35.3	19.2	18.9	2.4	2.3
47354_014_2-S_HM_ER	4.39	---	---	---	---	1.85	1.84	35.4	35.6	19.0	19.0	---	---
47354_014_2-S_HM_WL	4.36	2.93	80.4	714.6	10.9	1.86	1.85	36.7	36.2	19.1	19.2	2.42	2.32
47354_014_2-S_HM_WR	4.52	---	---	---	---	1.89	1.87	35.6	35.9	18.9	19.0	---	---
47354_015_2-S_HM_EL	4.54	2.92	81.8	702.3	11.1	1.84	1.85	42.4	36.9	18.9	18.4	2.47	2.37
47354_015_2-S_HM_ER	4.42	---	---	---	---	1.83	1.85	36.3	35.7	19.0	19.1	---	---
47354_015_2-S_HM_WL	4.42	2.93	80.4	714.4	10.9	1.86	1.85	36.1	35.4	19.3	19.3	2.41	2.31
47354_015_2-S_HM_WR	4.52	---	---	---	---	1.89	1.88	35.6	35.8	18.9	19.0	---	---
47354_026_2-S_HM_EL	4.65	2.73	81.5	704.7	10.5	1.98	2.0	35.4	35.5	18.8	18.8	2.4	2.32
47354_026_2-S_HM_ER	4.45	---	---	---	---	2.0	2.0	35.4	35.2	19.4	19.4	---	---
47354_026_2-S_HM_WL	3.7	2.72	81.1	708.1	10.4	2.06	2.06	35.9	35.5	19.3	19.3	2.43	2.34
47354_026_2-S_HM_WR	4.59	---	---	---	---	2.04	2.02	35.6	35.7	18.9	19.0	---	---
47354_034_2-S_HM_EL	4.62	2.77	81.9	701.5	10.6	1.95	1.96	35.4	35.5	18.9	18.9	2.46	2.23
47354_034_2-S_HM_ER	4.5	---	---	---	---	1.97	1.98	35.3	35.5	19.0	19.3	---	---
47354_034_2-S_HM_WL	4.53	2.73	81.4	705.8	10.4	2.02	2.02	35.8	35.3	19.2	19.2	2.44	2.35
47354_034_2-S_HM_WR	4.55	---	---	---	---	2.01	2.0	35.6	35.7	18.9	19.2	---	---
47354_046_2-S_HM_EL	4.5	2.87	82.1	699.6	11.0	1.87	1.89	35.4	35.5	19.2	19.2	2.39	2.32
47354_046_2-S_HM_ER	4.4	---	---	---	---	1.9	1.89	35.4	43.4	23.4	---	---	---
47354_046_2-S_HM_WL	3.92	2.84	81.6	704.1	10.8	1.93	1.93	35.8	35.6	19.1	19.1	2.41	2.32
47354_046_2-S_HM_WR	---	---	---	---	---	1.94	1.92	35.8	35.8	19.1	19.0	---	---
47354_048_2-S_HM_EL	4.5	2.85	82.2	698.4	10.9	1.87	1.89	35.4	35.5	18.9	18.9	2.4	2.32
47354_048_2-S_HM_ER	4.39	---	---	---	---	1.87	1.89	35.5	35.3	19.1	19.1	---	---
47354_048_2-S_HM_WL	4.44	2.83	81.4	706.0	10.7	1.94	1.95	35.6	35.5	19.2	19.1	2.4	2.31
47354_048_2-S_HM_WR	4.44	---	---	---	---	1.93	1.91	35.6	35.7	19.0	19.0	---	---
Median	4.49	2.85	81.45	705.25	10.85	1.89	1.89	35.6	35.6	19.1	19.1	2.42	2.32
Standard Deviation	0.37	0.08	0.61	5.38	0.22	0.06	0.06	1.37	1.53	0.8	0.27	0.02	0.03

Fig. 8.69: Example of a batch table with the extracted parameters of flute 1.

Chapter 9

Results from Quality Control

The production of the Outer Tracker wafers has exceeded 70% at the time of writing in November 2023. This fraction is sufficient to draw some solid conclusions and make some observations regarding the quality of the sensors that will instrument the outer tracking system. These conclusions combine the information from the first level of quality control performed by the vendor with the sampled and more in-depth measurements on sensors and test structures conducted by CMS. All collected data is stored in the CMS database and are available for further processing and analysis.

This chapter summarizes and presents all the results extracted from the electrical characterization of the production wafers. The results from the irradiation tests are not included in this thesis, while some early results are presented in [61]. The following analysis includes data from the global parameters of 20492 sensors produced and tested by HPK (Fig. 9.1). Among them, a fraction of about 13% are characterized by CMS in terms of global parameters and a fraction of about 5% are fully characterized (global and strip characterization). This is illustrated in Fig. 9.2. As mentioned in Chapter 5, the PS-p sensors are not tested by CMS and are delivered directly to the external companies that are responsible for the MaPSA assembly.

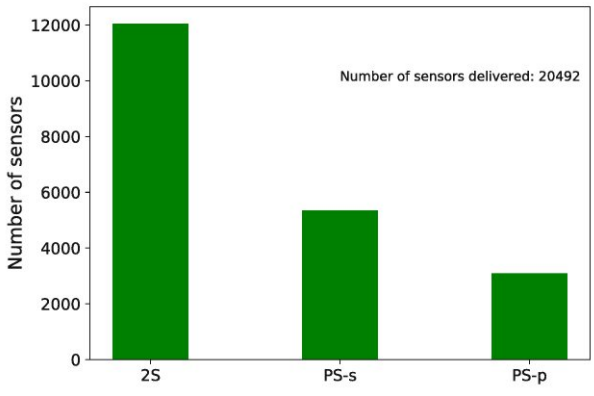


Fig. 9.1: Numbers of delivered 2S, PS-s and PS-p sensors.

About 2976 wafers have undergone the Process Quality Control with the results of the various extracted parameters given in the following sections. This number corresponds to 18% of the delivered wafers. The number of wafers is smaller than the number of sensors because the PS-s and PS-p wafers host two sensors. About 3% of the delivered wafers have been characterized by PQC with at least one sensor from the same wafer fully characterized (Fig. 9.3).

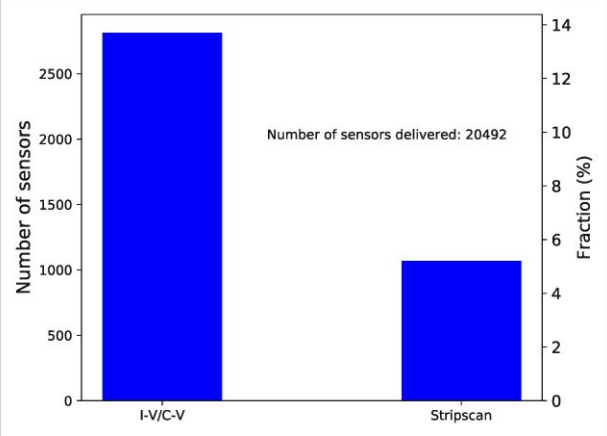


Fig. 9.2: Number of characterized sensors by CMS. The y-axis on the left side shows the number of tested sensors while on the right side shows the corresponding fraction with respect to the total number of delivered sensors.

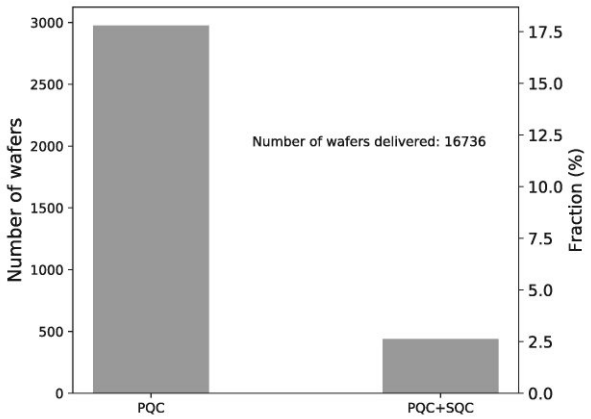
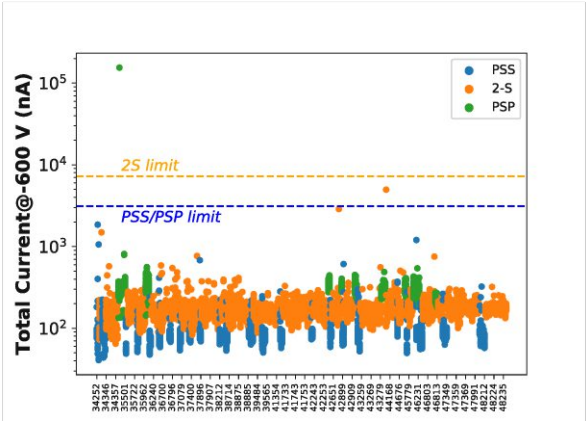


Fig. 9.3: Number of characterized PQC wafers by CMS. The y-axis on the left side shows the number of tested wafers while the right side shows the corresponding fraction with respect to the total number of delivered wafers.

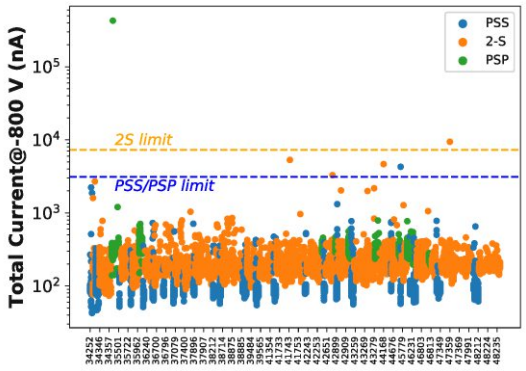
9.1 Total current

The total sensor current at 600 V is specified to be below 2.5 nA/mm^3. This results in a total current below 7.25 µA for 2S and below 3.25 µA for PS-s/PS-p sensors. In addition, the current at 800 V over the current at 600 V should be lower than 2.5 ($I_{800}/I_{600} < 2.5$) which should ensure the absence of any breakdown up to 800 V.

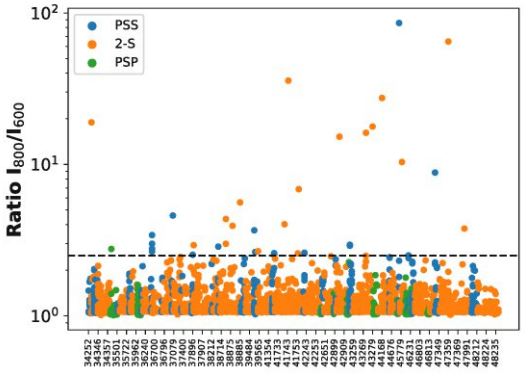
The trend of the total current at 600 V and 800 V over production time for the total amount of sensors delivered to date is illustrated in Fig. 9.4. The plot includes data from HPK and CMS. This means that the sensors tested by CMS have two entries in this plot, the HPK and the CMS measurement. Data from all CMS centers is included. The x-axis is in ascending order of the batch number, as defined by HPK which is assumed to coincide with the production date. The y-axis is given in the logarithmic scale. All currents are scaled to the same temperature of 20°C to facilitate the comparison and compensate for temperature variations among different probe stations.



(a) Total current at 600 V



(b) Total current at 800 V



(c) Ratio I_{800}/I_{600}

Fig. 9.4: Total current and I_{800}/I_{600} ratio over production time for 2S, PS-s and PS-p sensors. The plots include data from HPK and CMS. The dashed lines indicate the respective limits.

Concerning the global current at 600 V (Fig. 9.4a), almost all sensors exhibit a total current much below the respective limits which are indicated with dashed lines. The majority of the sensors show a I_{600} of a few hundreds of nA. The overall trends are stable over increasing batch number which indicates a stability of the production. The total current of a handful of sensors is near or beyond the limits. These sensors feature scratches and defects created in the SQC centers. The good behavior of the production sensors does not change in Fig. 9.4b with a I_{800} in the nA range for most of the cases. There is no specification for the total current at 800 V besides the ratio I_{800}/I_{600}. As a reference, the limits at 600 V are used in Fig. 9.4b. In both plots, three populations can be distinguished, each of which relates to a sensor flavor. The 2S has twice the size of PS-s sensor which results in about two times larger total current. The PS-p sensors feature the largest total current among the three flavors.

The evolution of I_{800} to I_{600} ratio is illustrated in Fig. 9.4c. The dashed line corresponds to a ratio of 2.5 which is the limit. Only a handful of sensors does not comply with this specification, some of which are also distinguishable in Fig. 9.4a, 9.4b as outliers. All 31 sensors which violate the ratio limit are analyzed in Fig. 9.5, which compares the measured ratio at HPK probe station (VQC) to the ratio measured at CMS centers (SQC). Five sensors violate the ratio at HPK but comply with it when remeasured by CMS. This seems to be a humidity-related effect with the most probable explanation for this improvement to be the lower relative humidity with respect

to HPK, in which CMS characterizes the sensors. The storage in dry conditions between the two measurements can also improve the behavior of sensors with humidity-related issues. Six sensors violate the limit at both testing sites. These sensors were delivered to CMS by mistake since the sensors which do not respect the ratio limit in the HPK measurement are not qualified. As consequence, these sensors were rejected. Twenty sensors included in Fig. 9.5 violate the ratio at SQC centers while they showed no issues during the measurements at HPK. This deterioration in their I-V behavior is an outcome of a damage inflicted on the sensors during handling in SQC clean rooms or scratches, contamination found on the sensors during optical inspection, the source of which is not attributed to the CMS centers.

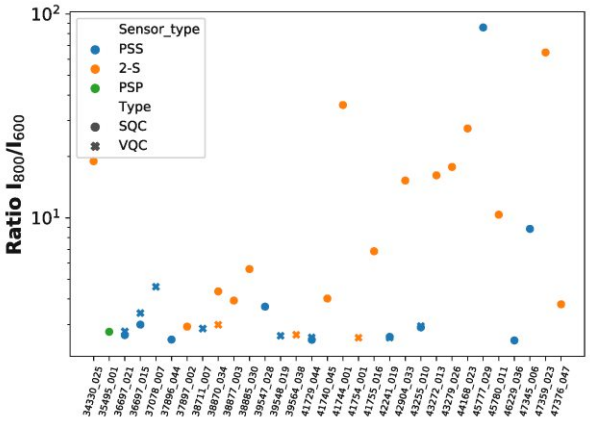


Fig. 9.5: Sensors which violate the ratio I_{800}/I_{600} in either the HPK or CMS I-V measurement. The plot includes 31 sensors.

Figure 9.6 is a histogram which includes all the sensors measured by CMS and shows the distribution of the difference between the total current at 600 V, as measured by HPK and CMS (I_{HPK} - I_{CMS}). All currents are scaled to the same temperature of 20°C. Among the 2820 characterized sensors, 169 (6% of the tested sensors) exhibits larger current at 600 V when tested by CMS with respect to the HPK results. Apart from the 20 sensors shown in Fig. 9.5 which violate the limits, the rest of them respect all specifications and they are good sensors. The majority of the sensors (94%) exhibit larger total current in HPK probe station which should be attributed to the humidity conditions in which they perform the I-V measurements (RH = 40%).

9.2 Full depletion voltage and bulk resistivity

The Outer Tracker sensors are specified to reach full depletion below a bias voltage of 350 V. The bulk resistivity of the sensors is specified to be within 3.5 to 8 kΩcm. Figure 9.7 shows the evolution of the full depletion voltage (V_{FD}) over production time. Some sensors with V_{FD} near or even above the limit were delivered over the first months. Despite that, these sensors are good enough and usable for the experiment, therefore they are qualified. Nonetheless, CMS asked HPK to deliver sensors of higher resistivity with a full depletion voltage well below the limit. Eventually, the full depletion voltage stabilized below 300 V, as it is shown in Fig. 9.7. Figure 9.8 shows the normalized histogram of full depletion voltage, including only the HPK data to avoid duplicates. The measured full depletion voltage follows a Gaussian distribution as it is shown by the Gaussian fit which is illustrated in red. The production sensors delivered to date yield a mean value of full depletion voltage V_{FD} = 239.31 V with σ = 35.29 V.

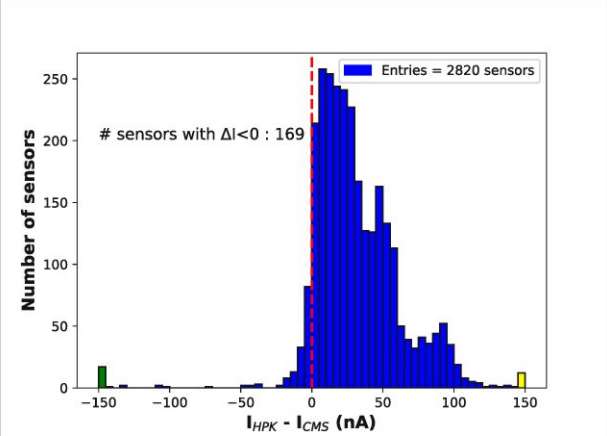


Fig. 9.6: Histogram of $\Delta I = I_{HPK}$ - I_{CMS} with the currents measured at 600 V. The bins left to the red dashed line include all the sensors for which the CMS measurement showed larger current than HPK. The overflow and underflow bin contain all ΔI above 150 nA or below -150 nA.

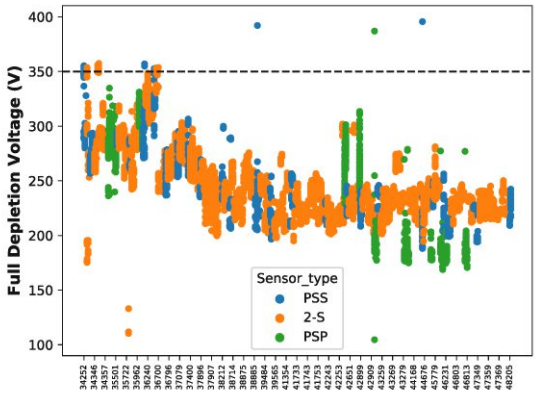


Fig. 9.7: Time evolution of full depletion voltage.

An alternative option to extract the full depletion voltage and to characterize the bulk resistivity is given by the diode structure which is hosted on the CMS production wafers (section 8.2.1). The diode full depletion voltage is measured from a C-V measurement while the bulk resistivity is extracted through the formula 8.2. The time evolution of the two diode parameters is given in Fig. 9.9. The trend of the diode full depletion voltage is in agreement with the observed trend in Fig. 9.7. Figure 9.9b shows the evolution of the bulk resistivity extracted from the diode structure.

Figure 9.11 is a comparison of the V_{FD} extracted from the main sensors with the V_{FD} extracted from the diode structures of the same wafers. The main plot shows the scatter of the compared data with blue points. The distribution of each parameter is shown at the opposite side of the axis which describes its values. The PS-p wafers are also included in the scatter plots, therefore only sensor data from HPK measurements is considered for consistency. In Fig. 9.11a, 9.11b the data is differentiated based on the location of the structures on the wafer (Fig. 9.10) in order to check for any inconsistencies of the bulk properties across the wafer due to the processing variations. The West side diodes are compared to the MAINL PS-s and PS-p sensors (Fig. 9.11a) while

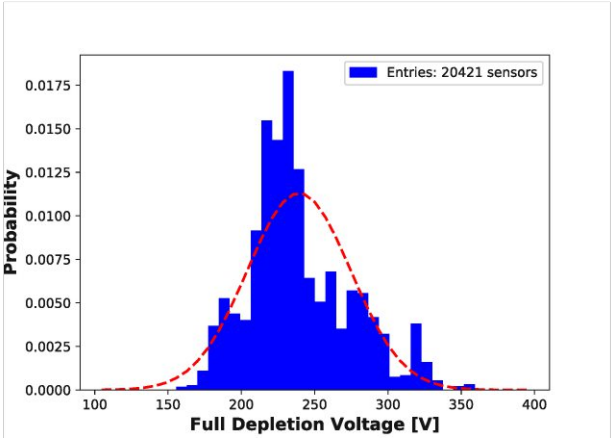
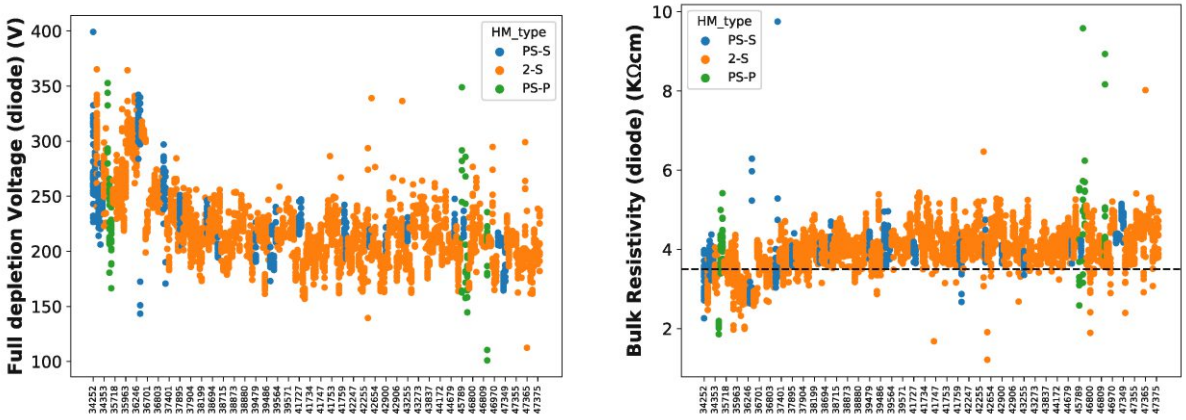


Fig. 9.8: Normalized histogram of full depletion voltage fitted with a Gauss function. The mean and standard deviation of the Gaussian distribution are displayed on the plot.



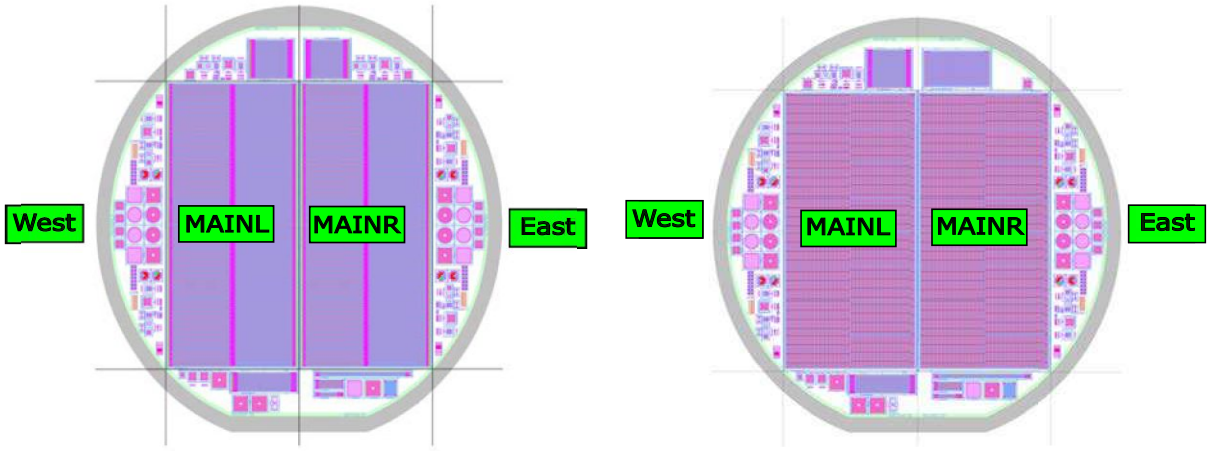
(a) Full depletion voltage. **(b)** Bulk resistivity

Fig. 9.9: Evolution of diode parameters over production time.

the diodes of the East side are compared to the MAINR sensors (Fig. 9.11b). The 2S sensors are compared to both test structures since a single sensor is hosted on the wafer. Assuming a linear correlation between the two data sets, the Pearson correlation coefficient[1]is about 0.5. Consistency is observed among the two sides of the wafer. A few outliers are observed in both Fig. 9.7, 9.9a which occur from low quality fitting due to the shape of C-V curves. Moreover, the diode V_{FD} shows a larger spread than the sensor values which is attributed to the impact of the non-optimized design of the structure on the C-V measurement (section 8.2.1)

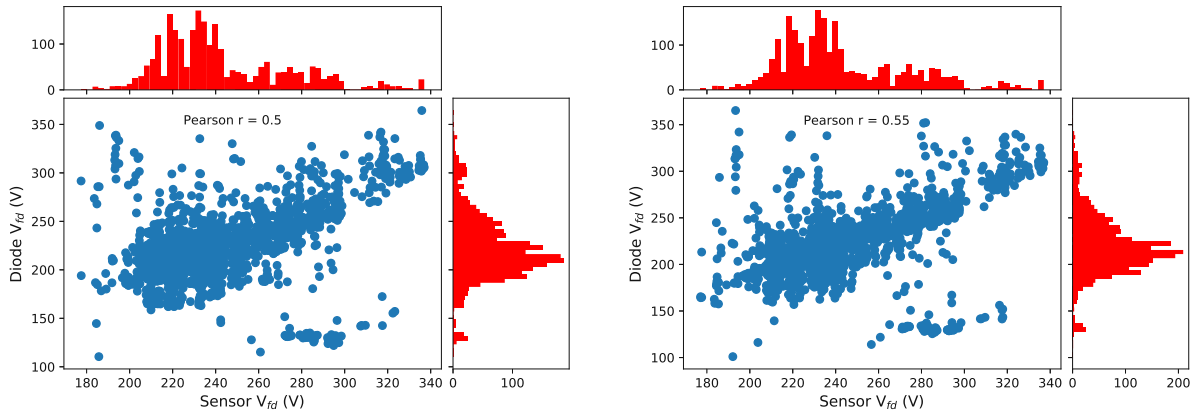
An additional PQC structure which can be used for the determination of the bulk resistivity is the cross-shaped Van-der-Pauw (VdP) structure with contacts to the p-type bulk. Following the same logic with the analysis presented in Fig. 9.11, the correlation between the resistivity calculated from the sensor full depletion voltage (formula 8.2) and the bulk resistivity extracted from the Van-der-Pauw structure is shown in Fig. 9.12. The correlation is consistent between the two sides of the wafer, as shown in Fig. 9.12a, 9.12b. The trend of the compared data shows a good agreement and a strong correlation. The Van-der-Pauw structure shows a good robustness

[1] $\rho_{X,Y} = \frac{cov(X,Y)}{\sigma_X \sigma_Y}$ where *cov* is the covariance



(a) PS-s wafer. **(b)** PS-p wafer.

Fig. 9.10: Wafer layout with orientation convention.



(a) West wafer side. **(b)** East wafer side.

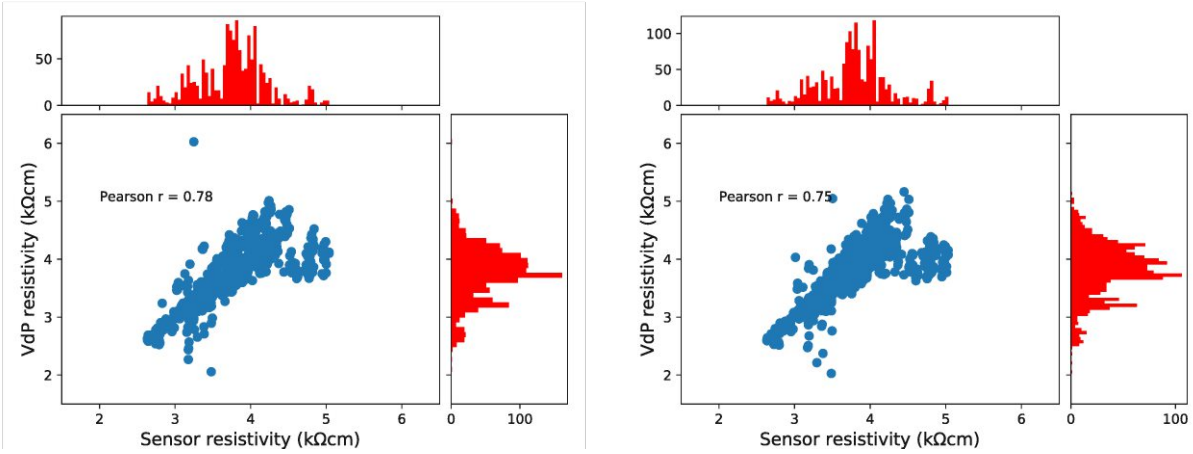
Fig. 9.11: Correlation plot of the diode ρ versus the sensor V_{FD}.

and reliability in determining the bulk resistivity through a four-wire I-V measurement (section 8.2.7).

9.3 Strip parameters

About 5% of the total amount of sensors delivered to date has undergone a strip characterization. As discussed in section 6.4, the I-V behavior of the sensors, as measured by the vendor, is the main driver for the selection of samples for full characterization. Hence, the sensors that are included in the following analysis are those that exhibit a larger total current than the average current of their batch. If faulty strips are present in a batch, the chances are higher that they will belong to those sensors with a deviating I-V behavior.

The results presented in the following sections include measurements from about 730000 characterized strips. The analysis of the strip parameters is structured in a common way. For each strip parameter, two types of plots are shown: a scatter plot which shows the evolution of the sensor median value over production time and a histogram which shows the distribution of all measured strips. The median is chosen instead of the mean because it is more robust against



(a) West wafer side. **(b)** East wafer side.

Fig. 9.12: Correlation plot of the bulk resistivity extracted from the Van-der-Pauw structure versus the resistivity extracted from the calculated sensor V_{FD}.

outliers. Outliers are those strips of a sensor with electrical parameters that deviate from the behavior of the rest, such as strips with pinholes or high leakage current. For similar reasons, the median absolute deviation[2]is used instead of the standard deviation in order to describe the spread of the data .

9.3.1 Strip leakage current

As shown in section 9.1, the majority of the unirradiated production sensors exhibit low total current. This hints that the majority of the strips are expected to feature low leakage current since the sum of a sensor strip leakage current should be approximately equal to the total sensor current. The strip leakage current is specified to be $I_{strip} < 10$ nA/cm (absolute value). The evolution of the strip current parameter over production time is displayed in Fig. 9.13. Each point corresponds to the median I_{strip} of a sensor. The y axis is given in logarithmic scale in order to include also the limit which is shown with a dashed line. The median strip leakage current of all measured sensors to date is about two orders of magnitude lower than the limit.

The distribution of all measured I_{strip} values is illustrated in Fig. 9.14. Among all measured strips, 52 of them (about 0.007%) violates the CMS I_{strip} specification. This number is negligible considering the total number of characterized strips. The evolution of the strips which violate the I_{strip} specification is shown in Fig 9.15. The strip leakage current of the tested strips yields a median of $I_{strip} \pm \delta I_{MAD}$ = -0.014 $\pm$ 0.004 nA/cm.

9.3.2 Polysilicon resistor

The strip bias resistor is specified to a resistance within the range of 1.5 $\pm$ 0.5 MΩ. Figure 9.16 shows the evolution of the sensor median bias resistor over production time. During the first production months, the delivered sensors exhibited a polysilicon resistance near or even higher than the upper limit (R_{poly}^{upper} = 2.0 MΩ). Although it is not related to the observed larger values, it should be noted that these sensors are produced with the old design of the polysilicon meander, as explained in Appendix A. It was asked from HPK to perform the necessary changes in the process so that the resistance of the bias resistors can reach the target value of 1.5 MΩ.

[2]MAD = median $(|(X_i - \text{median}(X)|)$

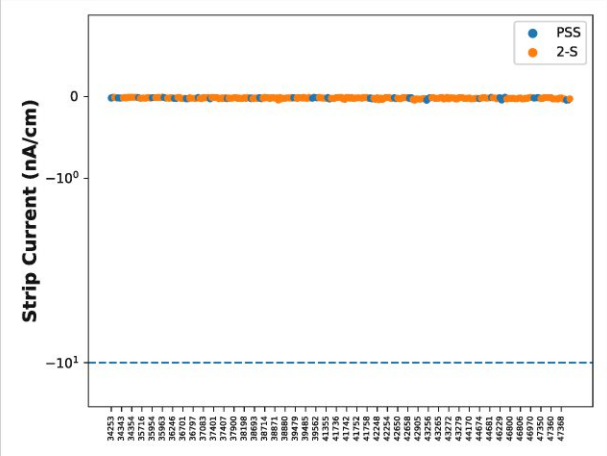


Fig. 9.13: Time evolution of sensor median I_{strip} grouped by sensor flavor. The dashed line shows the limit of 10 nA/cm.

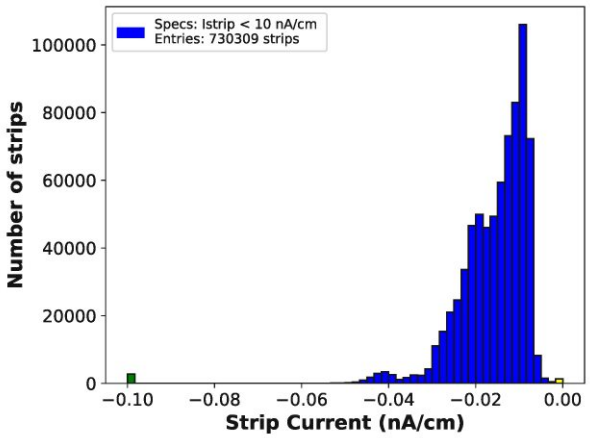


Fig. 9.14: Histogram of I_{strip} including all measured strips.

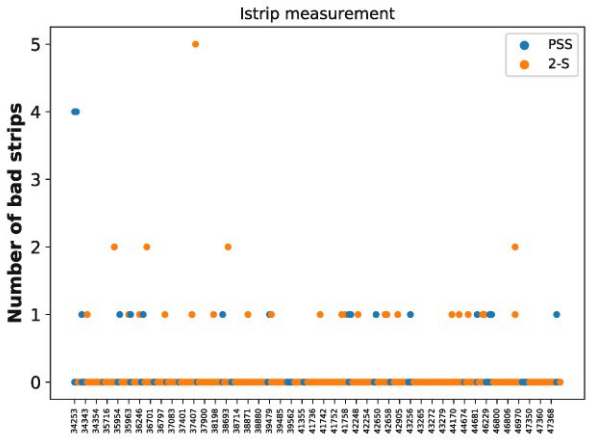


Fig. 9.15: Evolution of number of strips with $I_{strip} > 10$ nA/cm over production time.

HPK adjusted the doping of the polysilicon implant and as a result, the target value was reached. This adjustment is well reflected in the trend in Fig. 9.16 as well as in Fig 9.17, where the two

populations are distinguishable. The analysis of the polysilicon resistance of all measured strips yields a value of $R_{poly} \pm \delta R_{MAD} = 1.59 \pm 0.13$ MΩ.

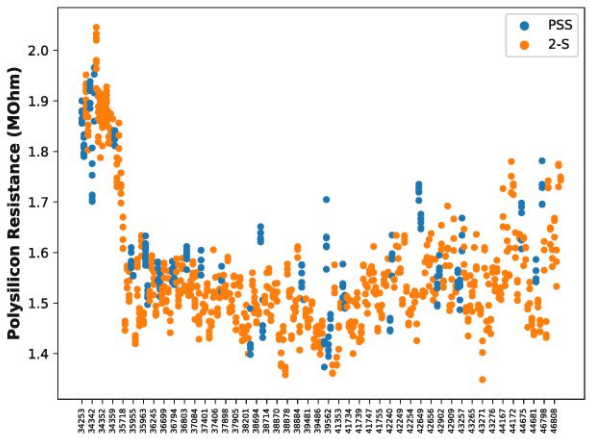


Fig. 9.16: Time evolution of sensor median R_{poly} parameter.

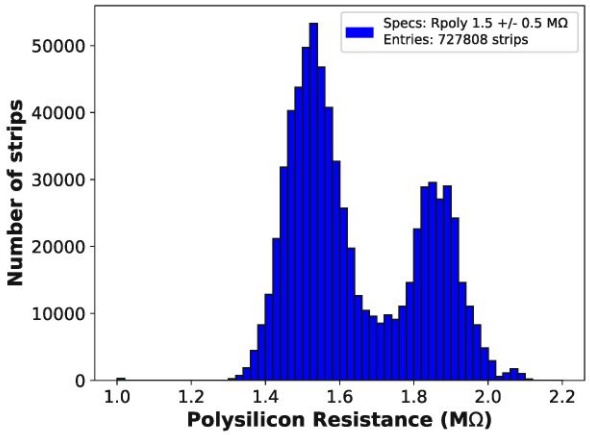


Fig. 9.17: Histogram of R_{poly}.

A Dedicated test structure is available on the CMS wafers in order to characterize the resistance of the bias resistors. The polysilicon meander on flute 3 (section 8.2.8) is a replication of the actual bias strip resistor, featuring the same design. The resistance of the meander is expected to be in accordance with the average resistance of the strip bias resistors. The time evolution of this parameter is illustrated in Fig. 9.18. The trend agrees well with the one shown in Fig. 9.16. As expected, the structure reflects the adjustment of the polysilicon doping.

Since the polysilicon meander is the same as the bias resistors of the main sensor, one could perform a correlation analysis on the two extracted parameters. This is illustrated in Fig. 9.19. The grouped structures and sensors are again differentiated according to their location on the wafer, as explained in section 9.2. The median sensor polysilicon resistance shows a strong correlation with the meander R_{poly}. A few outliers coming from the PQC measurements of the polysilicon meander do not change the generally good agreement between the compared parameters. An example of an I-V measurement giving an outlier is shown in Fig. 9.20. The measured current shows an increase in the last applied voltage which deviates from the linear behavior, as typically shown in a meander I-V curve.

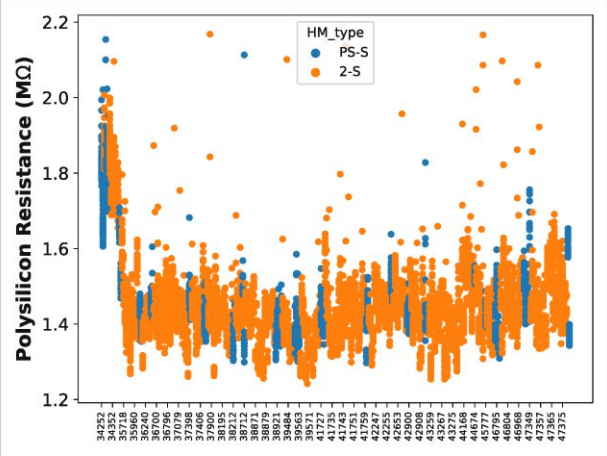
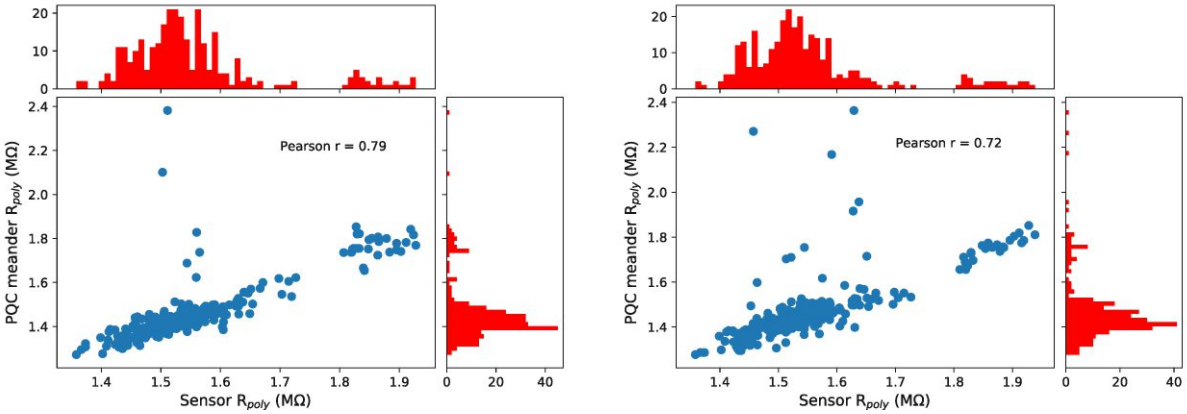


Fig. 9.18: Evolution of meander R_{poly}.



(a) West wafer side. **(b)** East wafer side.

Fig. 9.19: Correlation plot of sensor R_{poly}^{median} versus PQC meander R_{poly}.

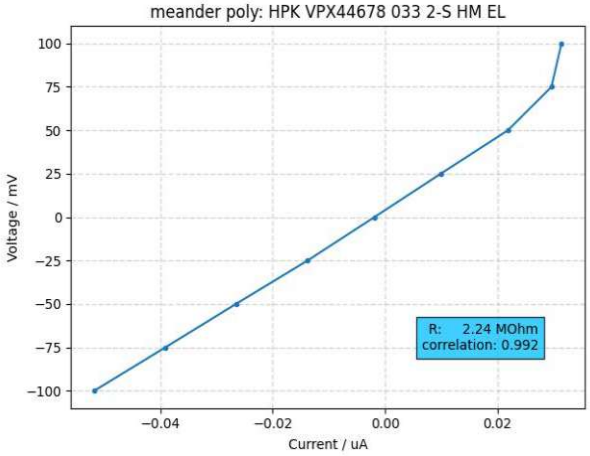
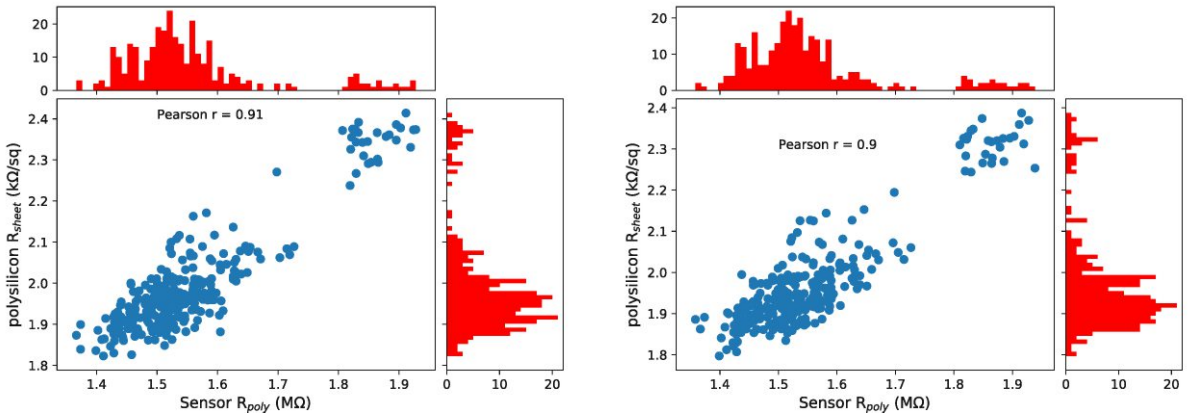


Fig. 9.20: Example of an I-V measurement of a PQC polysilicon meander which slightly deviates from the typical linear behavior.

An additional structure housed on the CMS wafers that characterizes the sheet resistance of the polysilicon resistor is the Van-der-Pauw cross-shaped structure with a polysilicon implant (section 8.2.5). More information about the behavior of this parameter over production time is given in section 9.8. Figure 9.21 illustrates the correlation of the median resistance of the sensor bias resistors versus the polysilicon sheet resistance from the structures of the same wafers. The two parameters exhibit a very strong correlation which hints the robustness of the Van-der-Pauw structure and its reliability in measuring the sheet resistance of the characterized implant.



(a) West wafer side. **(b)** East wafer side.

Fig. 9.21: Correlation plot of sensor R_{poly}^{median} versus R_{sheet} of VdP polysilicon structure.

9.3.3 Coupling capacitance

The coupling capacitance is directly related to the thickness of the coupling oxide which couples the strip implant to the read-out metal. The CMS specification for the coupling capacitance is $C_{cac} > 1.2$ pF/(cm·µm). The time evolution of the sensor median coupling capacitance is displayed in Fig. 9.22.

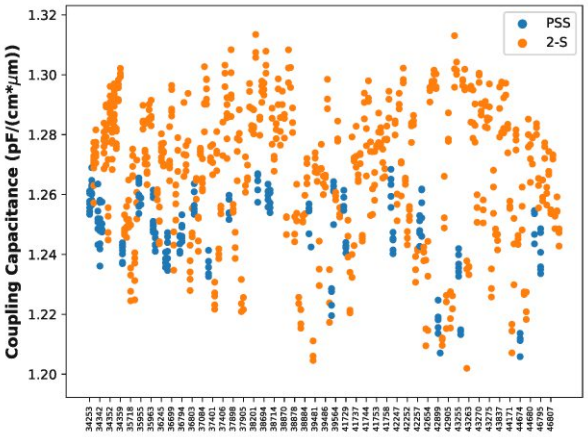


Fig. 9.22: Time evolution of sensor median C_{ac} parameter.

The histogram of the strip coupling capacitance is given in Fig. 9.23. The underflow bin contains a significant number of strips. This bin includes all strips with a measured coupling capacitance equal to or lower than the specified limit. Figure 9.24 illustrates the evolution of the

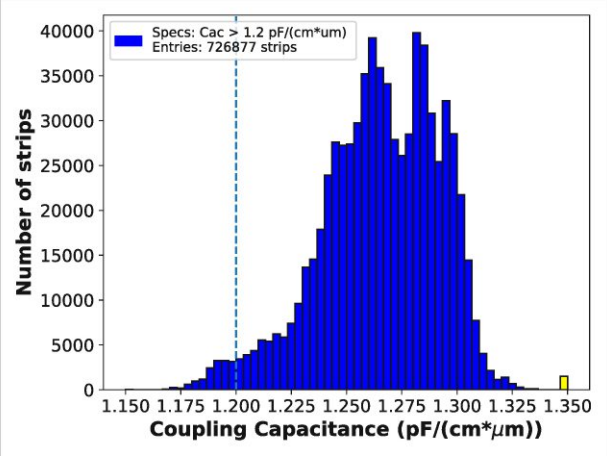


Fig. 9.23: Histogram of strip C_{ac}.

number of strips with low C_{ac}. No issues were observed up to roughly batch 38878. The first population with low values appears between batches 38878 and 41734. This indicates variations in the process which result in non-uniformity of the coupling, thin oxide. A second population with a large number of affected sensors appears above batch 42649. Lower coupling capacitance values can in the worst-case scenario, increase the chances of signal loss. Even if the low C_{ac} values concern only a subset of strips and are not extended over the whole sensor area, this can be still problematic since such an effect can result in a non-uniform signal. However, these batches were not rejected since the measured values of coupling capacitance which are slightly below the limit, are not considered to be a critical issue in the performance of these sensors during operation.

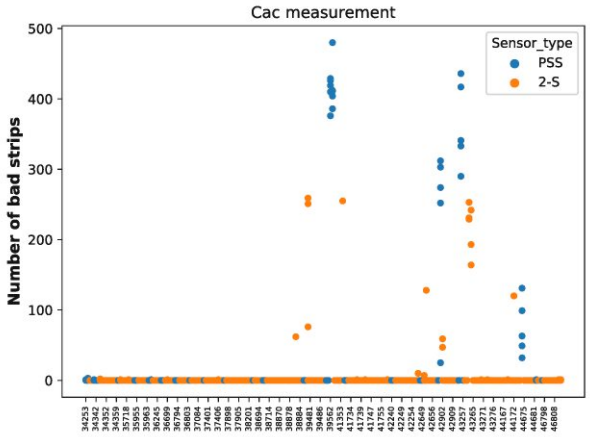


Fig. 9.24: Time evolution of sensors with lower C_{ac}.

CMS made known this issue to HPK and the vendor attributed these lower values to variations in the heat treatment process which led to variations in the coupling oxide thickness. Although further explanation was not given, according to the vendor the tuning of some process parameters could resolve this issue. In addition, it was stated that an increase of the coupling capacitance (decrease of the thin oxide) by a few percent will be achieved due to the implementation of this change. The effect of this adjustment in the thermal oxidation process started to be visible in the most recent deliveries, the data of which is not included in Fig. 9.22. However, a few of these

batches were delivered to HEPHY and there was the opportunity to validate the impact of that process variation on the sensor coupling capacitance. An example is illustrated in Fig. 9.25 with the coupling capacitance across the sensors showing values about 15% larger than the typical values seen in Fig. 9.22.

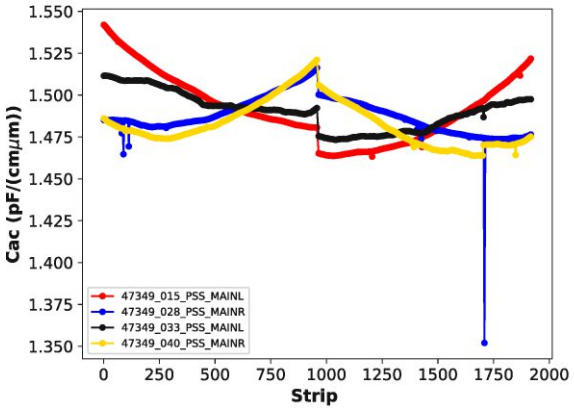


Fig. 9.25: The C_{ac} across the full sensor as measured on four PS-s sensors. This PS-s batch is produced with the new thermal treatment by HPK.

9.3.4 Pinholes

The absence of pinholes in the thin oxide is a crucial condition for its quality. As described in section 6.3, the dielectric current is the measurable parameter that indicates the presence of a pinhole. In principle, this current is negligible due to the insulating nature of the oxide. This is observed in the histogram illustrated in Fig. 9.26 with the vast majority of the measured strips exhibiting an I_{diel} in the order of a few pA. The spread of the measured currents is attributed to the use of different instruments among different SQC centers for the low current measurements. A dielectric current of 10 nA is the limit beyond which a pinhole is considered.

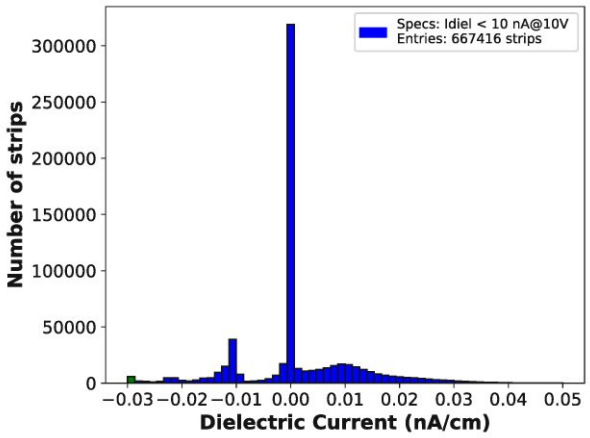


Fig. 9.26: Histogram of strip dielectric current I_{diel}.

To date, the number of pinholes detected in the tested Outer Tracker sensors equals to 20 which corresponds to 0.002% of the total characterized strips (Fig. 9.27). In most cases, these

pinholes are associated with deep scratches in the respective strips created by the probe needles during testing at CMS centers.

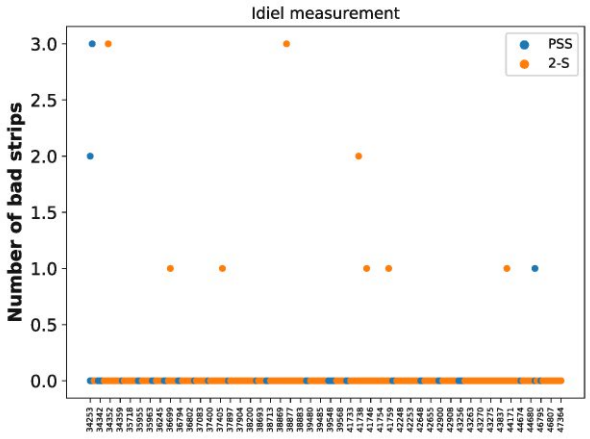


Fig. 9.27: Evolution of strips with $I_{diel} > 10$ nA (pinholes) over production time.

9.4 Interstrip parameters

The interstrip resistance and capacitance are two parameters of high significance since the former reflects the quality of interstrip isolation and the latter affects the noise level to the readout system and the charge sharing between neighboring strips. The following sections give an overview of the results from the interstrip parameters of the characterized sensors to date. The number of strips that have undergone an interstrip characterization and are included in the following results is about 142000.

9.4.1 Interstrip resistance

The interstrip resistivity of the unirradiated Outer Tracker sensors should be above 10 GΩcm. The time evolution of the median interstrip resistivity per measured sensor is shown in Fig. 9.28. The histogram of all measured interstrip resistivity values to date is displayed in Fig. 9.29. The majority of the characterized strips exhibit a resistivity beyond 200 GΩcm. The overflow bin contains all values that exceed 2500 GΩcm. Section 6.4 gives an example of a batch qualification where it is shown that these higher values depend on the DC pad of the strip (edge or central) in which the interstrip resistance is measured. A dashed line shows the limit below which all strips included in the bins violate the specifications.

One PS-s batch (34352) from the first production deliveries was rejected because regions of low interstrip isolation were spotted on more than one sensor from this batch. Therefore, this batch is not included in the analysis shown in Fig. 9.28, 9.29. The majority of the strips which have R_{int} values below the limit in Fig. 9.29 come from charged-up sensors (section 7.2), the data of which was uploaded on the database before this issue was well-understood. Therefore, these sensors are not considered as bad since their electrical behavior recovered fully after the use of ion blowers. A negligible number of low R_{int} values are attributed to scratches on the respective strips.

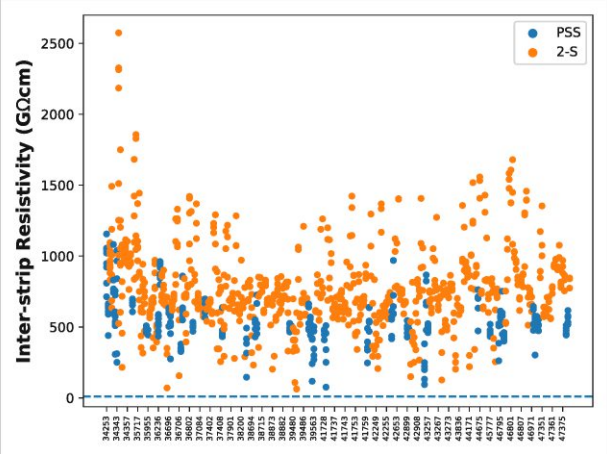


Fig. 9.28: Time evolution of interstrip resistivity.

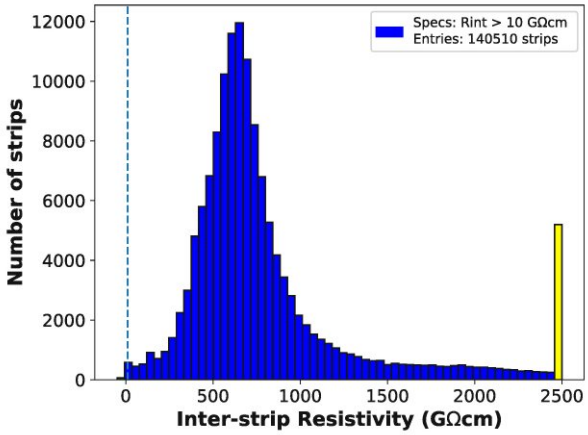


Fig. 9.29: Histogram of interstrip resistivity.

9.4.2 Interstrip capacitance

The CMS specification for the interstrip capacitance is $C_{int} < 0.5$ pF/cm. Figure 9.30 illustrates the time evolution of the interstrip capacitance. The observed spread of the C_{int} values is attributed to the different setups.

9.5 Si-SiO_2 interface quality

The evolution of the properties and quality of the Si-SiO_2 interface over production time are monitored through measurements on the MOS capacitor and the GCD test structures.

The flat-band voltage (V_{fb}) is a parameter extracted from the MOS capacitor and is an indicator of the number of positive trapped charges at the Si-SiO_2 interface. These trapped charges impact the electric field distribution at the interface, as discussed in section 8.2.2 and as a consequence, the interstrip isolation between consecutive strips. The number of positive charges increases with oxide damage. Thus, a small flat-band voltage before irradiation is desirable. The time evolution of V_{fb} is illustrated in Fig. 9.31a while the distribution of the V_{fb} values is given in Fig. 9.31b. The measured MOS structures to date yield an average value of $V_{fb} = 3.07 \pm 0.61$ V and a good uniformity for different wafer types. The PS-p wafers feature larger

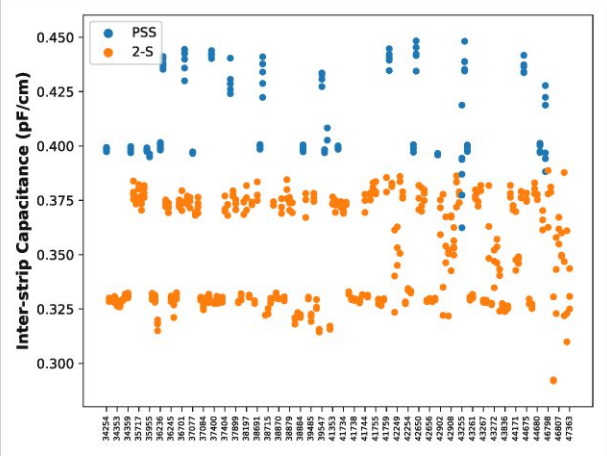
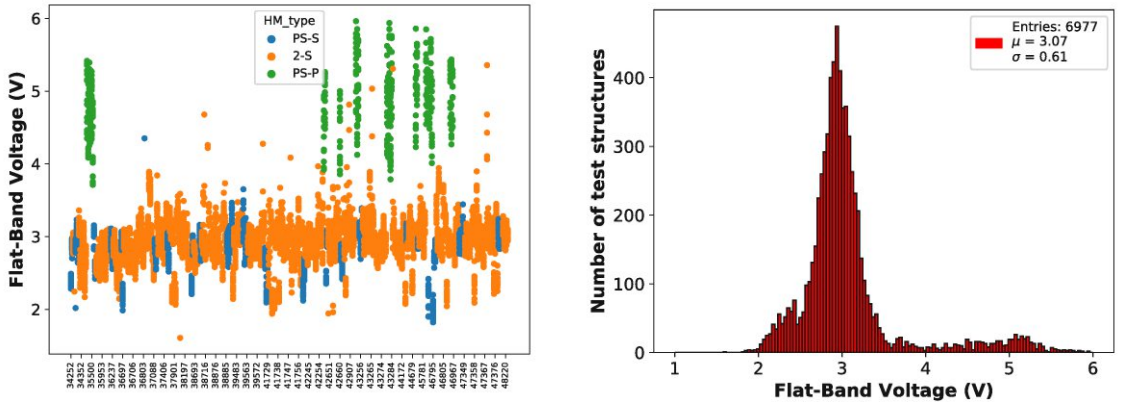


Fig. 9.30: Time evolution of interstrip capacitance.

flat-band voltage, hence a higher concentration of fixed oxide charges at the interface. The AC and DC-coupled wafers might undergo a slightly different thermal oxidation or post-thermal oxidation process, during which the annealing of the oxide charges takes place (section 3.5.2.1). The oxide charges decrease with higher oxidation temperature. After oxidation, the number of oxide charges decreases if an annealing procedure is followed, for instance with nitrogen or argon [93]. It is not known which of the processing steps varies between the fabrication of the two types of wafers, nevertheless, such a variation could explain the observed discrepancy. The larger flat-band voltage for the PS-p sensors is not critical before and after irradiation, as no problems with the interpixel isolation after oxide damage have been spotted to date by the irradiation studies.

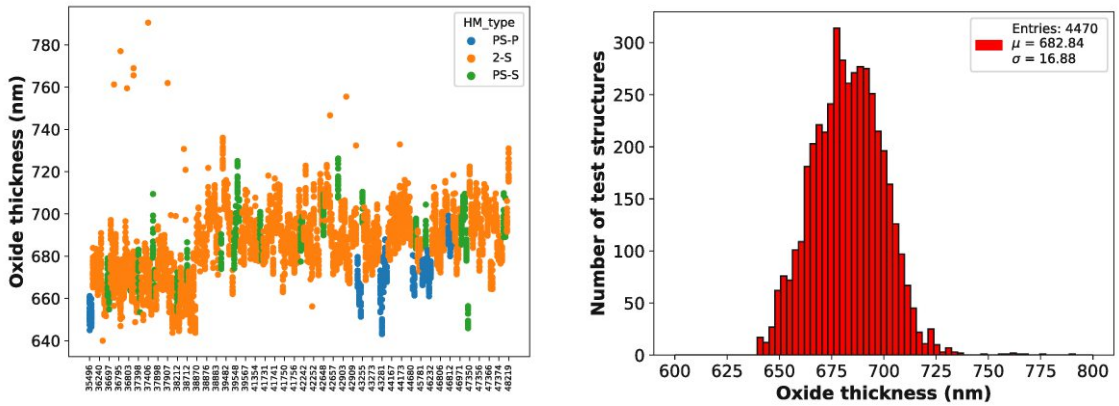


(a) Evolution of V_{fb} over production time. **(b)** Histogram of V_{fb}.

Fig. 9.31: Flat-band voltage of Outer Tracker production wafers.

The distribution of the thick oxide thickness (t_{ox}) is shown in Fig. 9.32b and the time evolution in Fig. 9.32a. It is extracted from the MOS structure using the formula 8.5. Not all extracted t_{ox} data from the characterized MOS structures have been uploaded on the CMS database which explains this discrepancy in the number of entries between the histograms 9.31b, 9.32b. A minor increase of 3 - 4% after roughly the first year of production is observed in Fig. 9.32a while

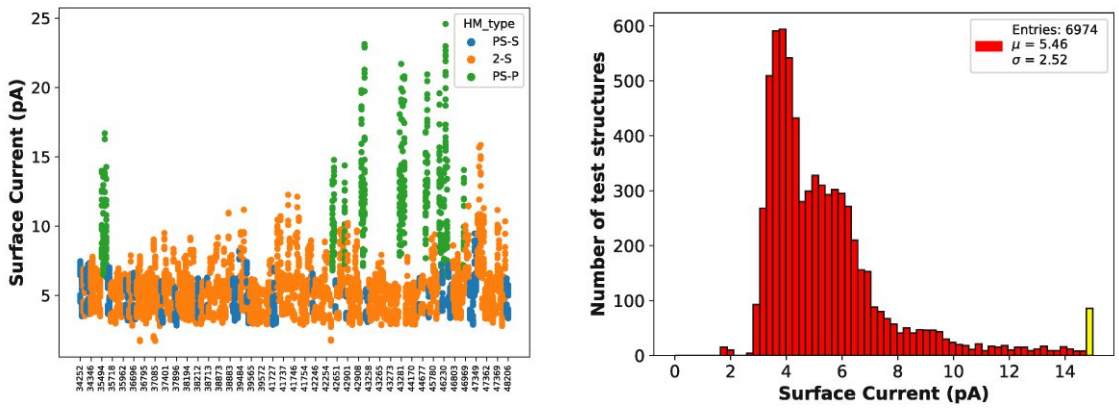
in sequence t_{ox} stabilizes again. The average oxide thickness extracted from the structures in Fig. 9.32b equals to $t_{ox} = 682.84 \pm 16.88$ nm.



(a) Time evolution of t_{ox}. **(b)** Histogram of thick oxide thickness t_{ox}.

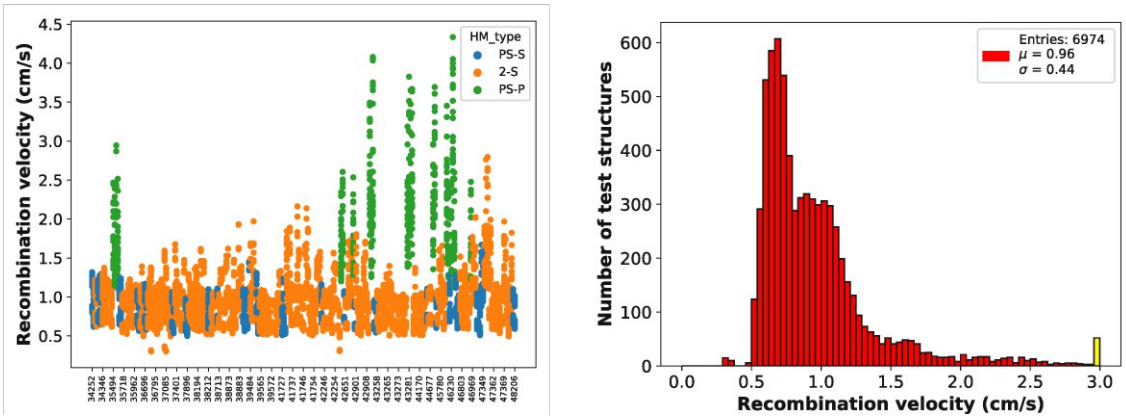
Fig. 9.32: Thick oxide thickness t_{ox} of Outer Tracker production wafers.

Besides the fixed oxide charges, the interface traps play an important role in the properties of the Si-SiO_2 interface as well as in the radiation hardness of the oxide. The interface can be characterized in terms of interface traps through the Gate Controlled Diode. The surface current is the measurable parameter that is proportional to the interface trap density (section 8.2.3). It exhibits a stable behavior over production time, as illustrated in Fig. 9.33a. The 2S and PS-s GCD structures show a surface current typically between 4 to 6 pA while for the DC-coupled wafers, I_{surf} shows a larger spread with surface currents between 8 to 20 pA. A larger concentration of interface traps in the thick oxide of DC-coupled wafers is evident. Presumably, differences in the annealing process that passivates the interface traps could be an explanation for this discrepancy. Figure 9.34a displays the evolution of the surface generation velocity which is calculated by the formula 8.10. The distributions of I_{surf} and S_0 can be seen in Fig. 9.33b, 9.34b.



(a) Time evolution of I_{surf}. **(b)** Histogram of I_{surf}.

Fig. 9.33: Surface current (I_{surf}) measured from GCD stuctures.



(a) Time evolution S_0. **(b)** Histogram of S_0.

Fig. 9.34: Recombination velocity (S_0) measured from GCD structures.

The surface current of the measured GCD structures yields $I_{surf} = 5.46 \pm 2.52$ pA while the surface recombination velocity is $S_0 = 0.96 \pm 0.44$ cm/s. The large standard deviation is expected due to the aforementioned discrepancy of the surface current between the AC-coupled and DC-coupled wafers.

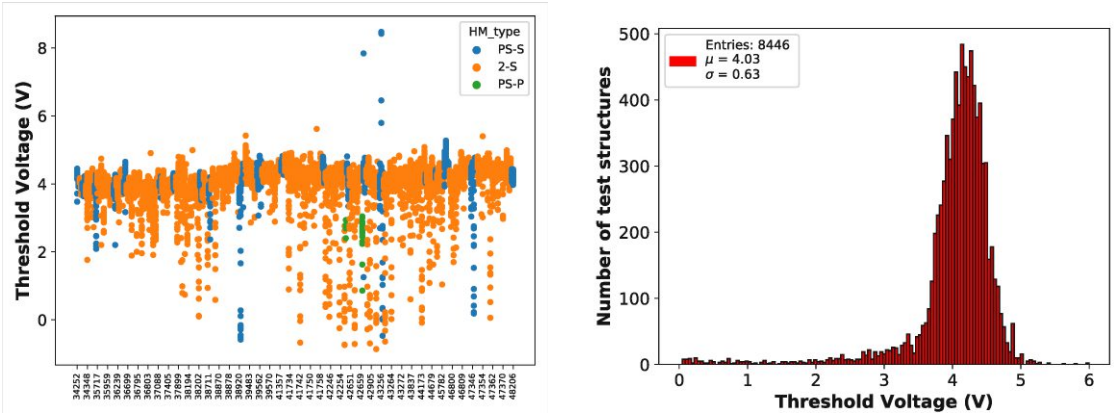
9.6 Characterisation of p-stop quality

The CMS wafers offer two alternative structures for the characterization of the p-stop quality: the PQC MOSFET structure with a p-stop implantation (section 8.2.4) and the cross-Van-der-Pauw structure with a p-stop implant (section 8.2.5). The former checks for variations in the threshold voltage (V_{th}) and the latter measures the sheet resistance of the implant which is inversely proportional to the p-stop doping concentration. Any variations in the p-stop doping concentration are reflected directly on the Van-der-Pauw structure. The geometry of the MOSFET structure mimics the interstrip region with a p-stop implant surrounding each of the n^+ implants which act as the source and the drain. Variations in the threshold voltage can reflect variations in the geometry of the structure, the p-stop doping or the oxide charge concentration.

The time evolution of the threshold voltage and the p-stop sheet resistance are displayed in Fig. 9.35a, 9.36. The mean threshold voltage extracted from the MOSFET structures to date is $V_{th} = 4.03 \pm 0.63$ V.

The correlation of the two PQC parameters is investigated in Fig. 9.37 which shows the scattering of p-stop sheet resistance data versus the threshold voltage measured on the same flutes and half-moons. The distribution of each parameter is shown, as a reference, at the sides of the plot. Excluding the PS-p wafers, the plot of Fig. 9.37a results in Fig. 9.37b. The correlation of the two parameters is stronger without the PS-p wafers. This can be understood if one considers the discussion in section 9.5, where it was shown that the flat-band voltage of the PS-p wafers is larger than the PS-s and 2S wafers. This means that for a certain p-stop sheet resistance, the threshold voltage of the PS-p MOSFETs is lower than the PS-s and 2S structures, as shown in Fig. 9.35a. As explained in sections 8.2.2, 8.2.4, the threshold voltage of a transistor decreases with increasing concentration of fixed positive charges at the Si-SiO_2 interface.

The presence of several V_{th} values below 1 V in Fig. 9.35a or R_{sheet} values above 24 kΩ/sq in Fig. 9.36 is a sign of variations in the production process related to the p-stop implantation.



(a) Time evolution of V_{th}. **(b)** Histogram of V_{th}.

Fig. 9.35: Threshold voltage measured from MOSFET structures.

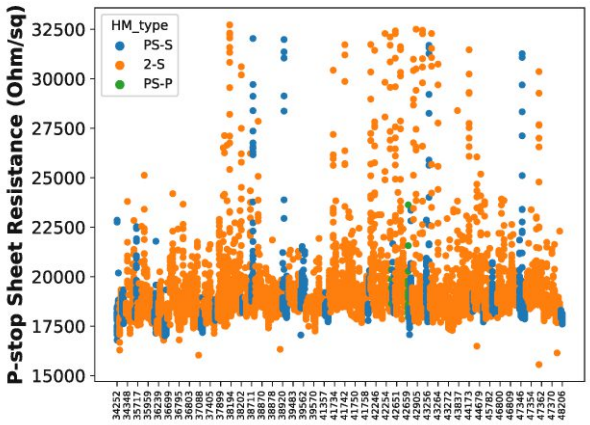
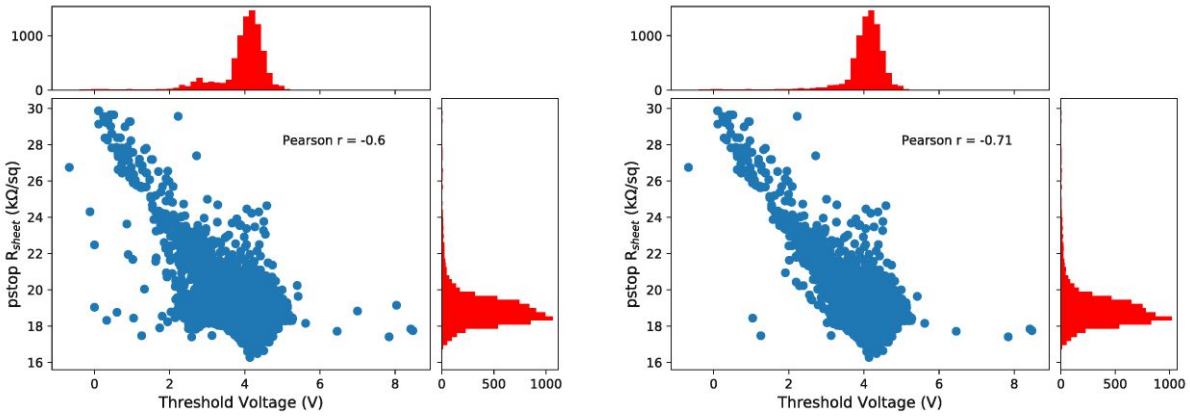


Fig. 9.36: Time evolution of p-stop R_{sheet}.

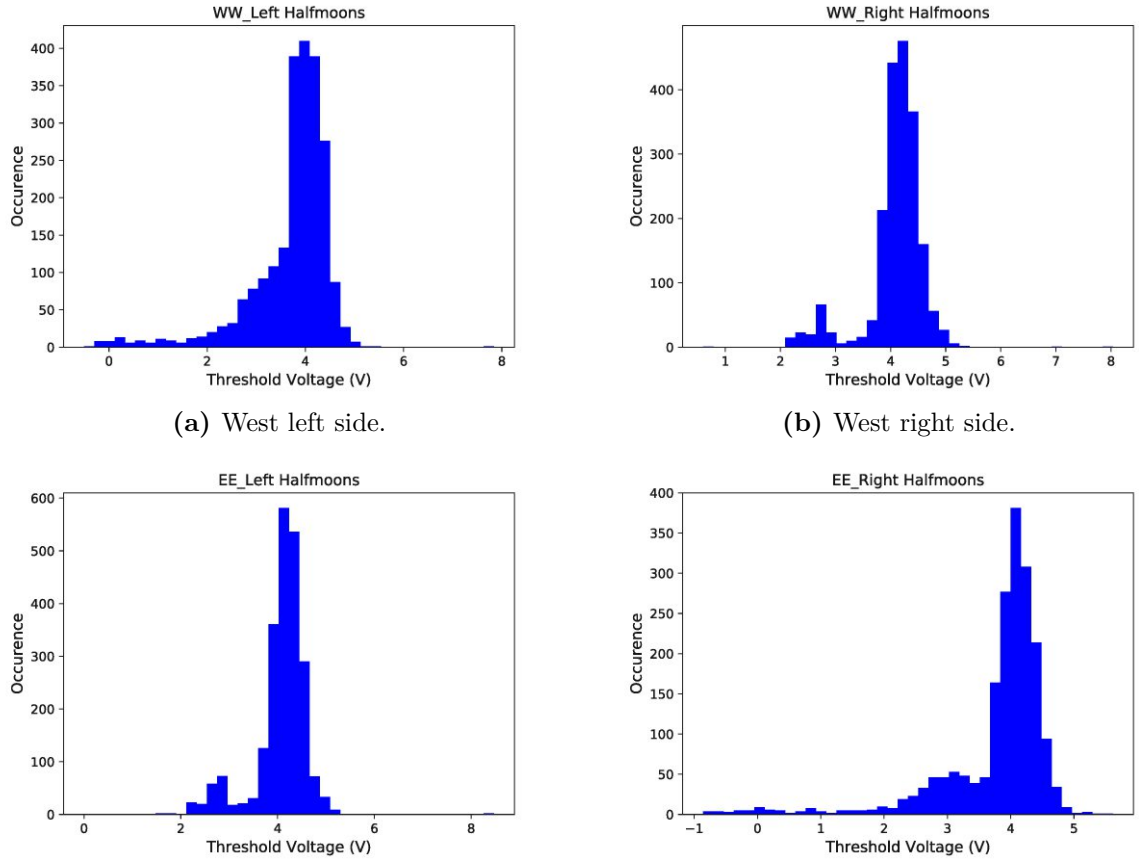


(a) All wafers included. **(b)** Without the PS-p wafers.

Fig. 9.37: Correlation of threshold voltage and p-stop sheet resistance for the Outer Tracker production wafers.

An increase in the p-stop sheet resistance means lower p-stop doping concentration. Low p-stop doping can become a problem for interstrip isolation before and especially after irradiation if the doping concentration falls below a critical limit.

Associating the structures with the low threshold voltage values to their location on the wafer, a pattern is formed. As can be seen in Fig. 9.38, values Vth < 2 V are typically observed on the two low corners of a wafer which corresponds to West-Left (WL) and East-Right (ER) orientations. Low threshold voltage values have not been observed so far in the structures located at the other two corners of the wafer. This pattern hints an inhomogeneity in the process. This could be related to variations in the thermal treatment for the activation of the dopants. The source of this variation is under investigation by the vendor.



(a) West left side. **(b)** West right side.

(c) East left side. **(d)** East right side.

Fig. 9.38: Distribution of V_{th} for different locations of the MOSFET on the wafer.

Sensors from the wafers with the low and non-uniform p-stop doping concentration were characterized but no abnormal behavior of R_{int} was spotted. An example is illustrated in Fig. 9.40. Three sensors from wafers with uniform threshold voltage across all the wafer corners are included as a reference (red points). The mean threshold voltage and the standard deviation across the wafer are shown in Fig. 9.41 with red points. In addition, three sensors from wafers of non-uniform and low mean threshold voltage (blue points in Fig. 9.41) are included in Fig. 9.40 and compared to the reference sensors. All sensors were tested by the same CMS Quality Control center which performs the characterization of both banks of strips at the edge pads. The trends of both groups of sensors are similar. The inhomogeneity of the p-stop doping concentration across the wafers included in Fig. 9.41 is not reflected on the interstrip

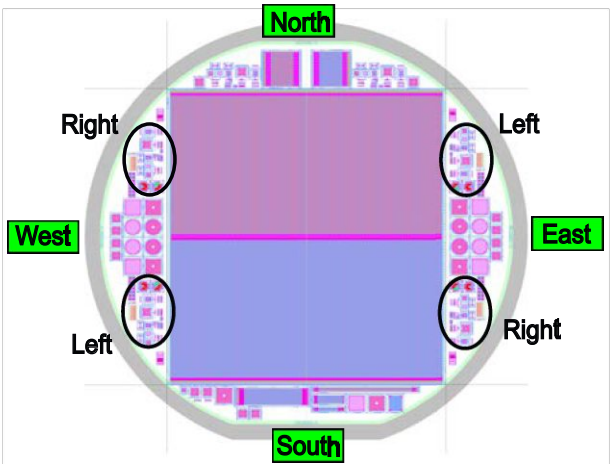


Fig. 9.39: Wafer orientation. The layout of a 2S wafer is used as a reference.

resistance of the respective sensors, showing trends and values that do not deviate from the interstrip resistance of the reference sensors. Moreover, irradiation studies focused on sensors from the wafers with the very low V_{th}, were conducted by CMS and they did not reveal any issues with the interstrip isolation after irradiation with the interstrip resistance being sufficiently high.

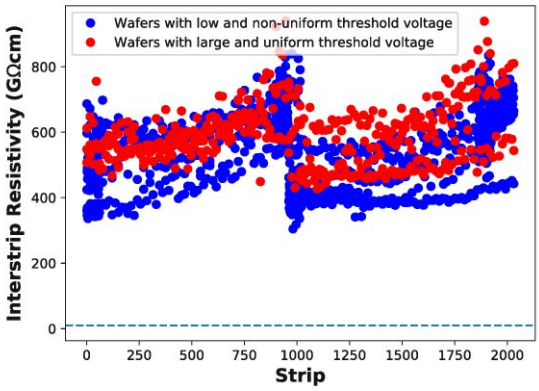


Fig. 9.40: Interstrip resistivity over strip number for three sensors (with blue) which come from wafers with low and non-uniform p-stop doping concentration. The interstip resistivity of three sensors (with red) with uniform and large threshold voltage is given as a reference. The light blue, dashed line describes the limit of 10 GΩcm.

9.7 Thin oxide quality

The thin oxide of the AC-coupled sensors can be directly characterized through the capacitor structure which is located in the CMS wafers (section 8.2.9). The oxide thickness is calculated from the measured capacitance through the parallel plate capacitor formula 3.25. The two extracted parameters from the capacitor structure are illustrated in Fig. 9.42. The plots include also the most recent batches which are produced with the adjusted thermal treatment (section 9.3.3). These are the batches with ID 47364, 47990, and 48221 in Fig. 9.42a, 9.42b. An increase

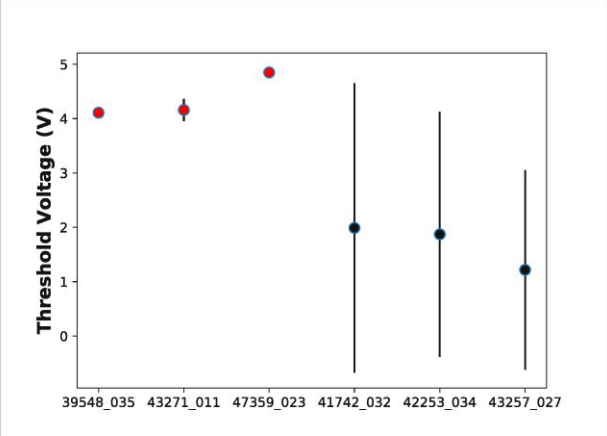
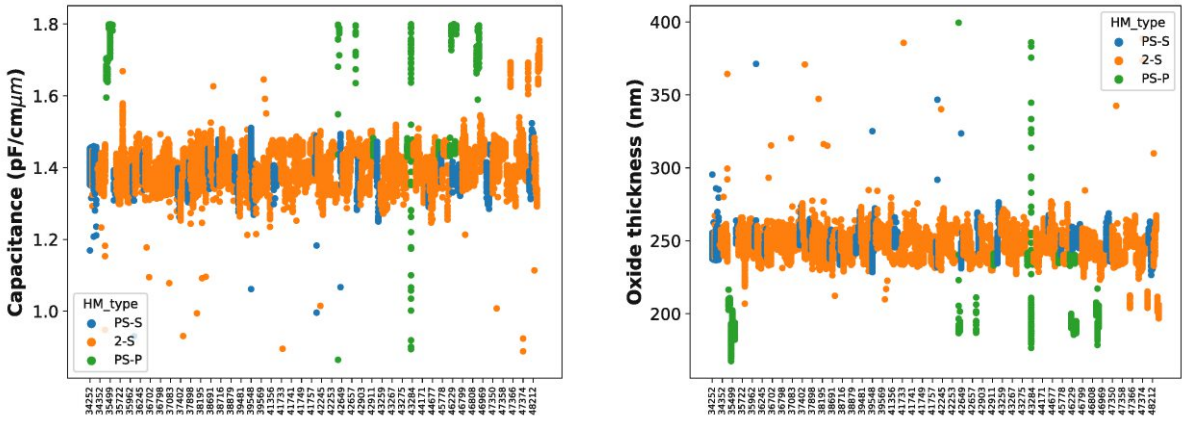


Fig. 9.41: Mean threshold voltage of compared wafers with error bars showing the standard deviation of the parameter across the wafer.

of about 15% of the oxide thickness can be observed which agrees well with the increase of the coupling capacitance of the sensors shown in Fig. 9.25. Figure 9.43 is a scatter plot of the sensor mean coupling capacitance versus the mean capacitance of the PQC capacitor structures of each compared wafer. The capacitor structures of the wafers that host main sensors showing lower coupling capacitance (below 1.2 pF/µm · cm), do not reflect the same trend. The same thin oxide is deposited on the full wafer, nevertheless, the strips which are a few cm long represent a large sample of the oxide while the test structures, due to their small size, sample only a small fraction of it.



(a) Evolution of capacitance of the capacitor structure.

(b) Evolution of coupling oxide thickness extracted from the capacitor structure.

Fig. 9.42: Time evolution of PQC capacitor parameters.

The capacitor structures from the PS-p wafers show consistently thinner oxide than the capacitors of the AC-coupled wafers, as it is evident from Fig. 9.42b. The dielectric between the readout and implant strip is made of a thicker SiO_2 layer of about 200 µm and a thin Si_3N_4 layer of about 50 µm. For the DC-coupled sensors, it is assumed that the nitride is not deposited which would explain the observed discrepancy.

The thin oxide thickness based on the collected data from the capacitor structures to date, yields a mean value of $d_{ox} = 243.48 \pm 15.09$ nm.

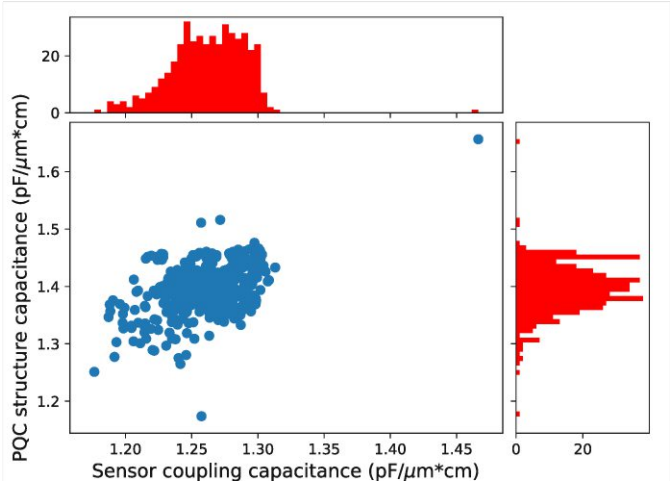


Fig. 9.43: Scatter plot of sensor coupling capacitance versus the capacitance of the PQC capacitor structure.

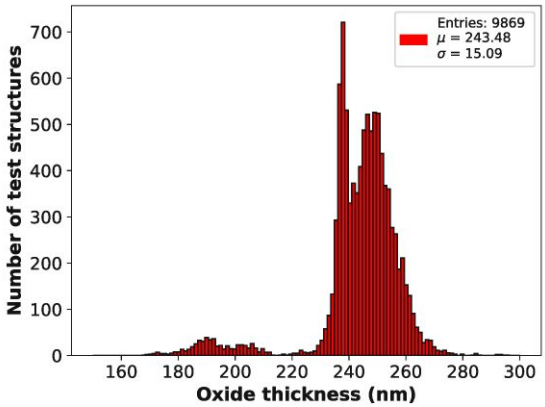


Fig. 9.44: Evolution of thin oxide thickness extracted from the capacitor structure.

H-V robustness of thin oxide

The high voltage robustness of the thin oxide is another indicator of its thickness. It is specified to exceed 150 V. High-voltage stability of the dielectric is important for resilience against high induced currents which in collider experiments can occur in beam loss scenarios, as described in section 8.2.10. The breakdown voltage (V_{bd}) of the oxide is investigated through potentially destructive tests in the PQC dielectric breakdown structure, where an I-V is performed up to a voltage of 200 V. The evolution of this parameter over production time is displayed in Fig. 9.45. A consistent behavior of the V_{bd} is evident, with the breakdown voltage of the AC-coupled wafer structures being typically beyond 200 V. The thin oxide of the DC-coupled PS-p wafers shows a smaller breakdown voltage, around 160 - 170 V which should be related to the missing nitride which ends up to a smaller thickness than the thin oxide of the AC-coupled wafers.

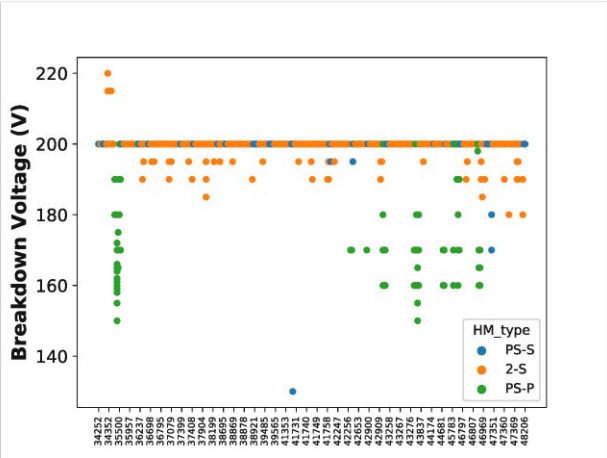


Fig. 9.45: Evolution of thin oxide breakdown voltage V_{bd}.

9.8 Implant and metal sheet resistance

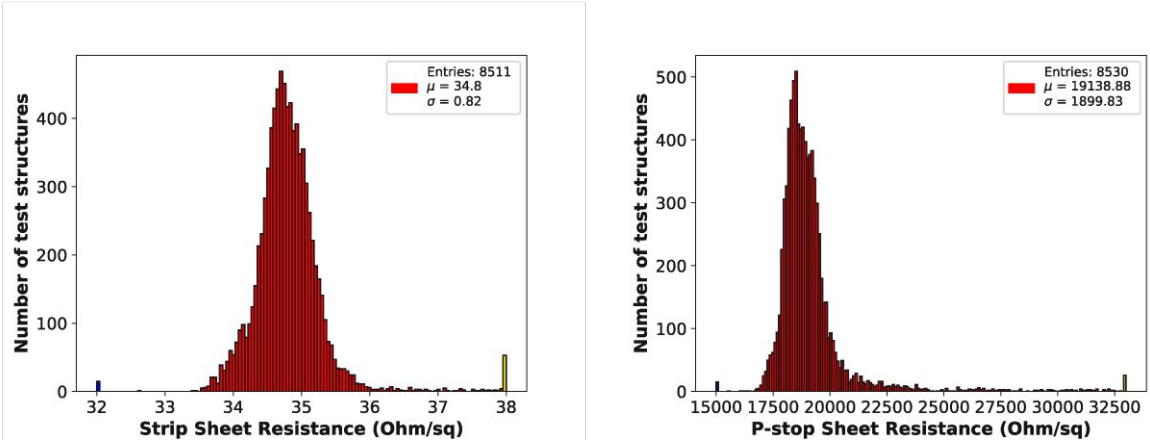
The sheet resistance (R_{sheet}) of thin films such as the n^+, the polysilicon, the p-stop and the p^+ implant of the edge ring are extracted through I-V measurements on the respective Van-der-Pauw structures. Figures 9.46 illustrate the distribution of the measured sheet resistance values for all the characterized implants in the scope of PQC. The n^+ and p^+ implants exhibit uniform sheet resistance while the observed spread of the polysilicon and p-stop sheet resistance values is discussed in sections 9.3 and 9.6. The average n^+ strip sheet resistance measured to date yields $R^{n^+}_{sheet} = 34.80 \pm 0.82\ \Omega/sq$, well-below the CMS specification of $R^{n^+}_{sheet} < 250\ \Omega/sq$. For the polysilicon implant, it is $R^{poly}_{sheet} = 1.98 \pm 0.50\ k\Omega/sq$, while a comparison with the results from the polysilicon meander follows in section 9.10. The p^+-edge implant shows an average value of $R^{p^+}_{sheet} = 1.20 \pm 0.05\ k\Omega/sq$ and for the p-stop is $R^{p\text{-stop}}_{sheet} = 19.13 \pm 1.89\ k\Omega/sq$. All averages are consistent to the early results from the Pre-Series wafers (a small number of wafers produced before the production in order to validate the sensor design and quality) shown in [88]. Only the polysilicon implant features a lower average sheet resistance related to the adjustment of the polysilicon doping performed by HPK, as discussed in section 9.3.2.

The clover metal structure is used for the extraction of the aluminum sheet resistance. The extracted sheet resistance is $R^{metal}_{sheet} = 19.16 \pm 1.27\ m\Omega/sq$ and the distribution is given in Fig. 9.47. A comparison with the results from the metal meander is done in section 9.10.

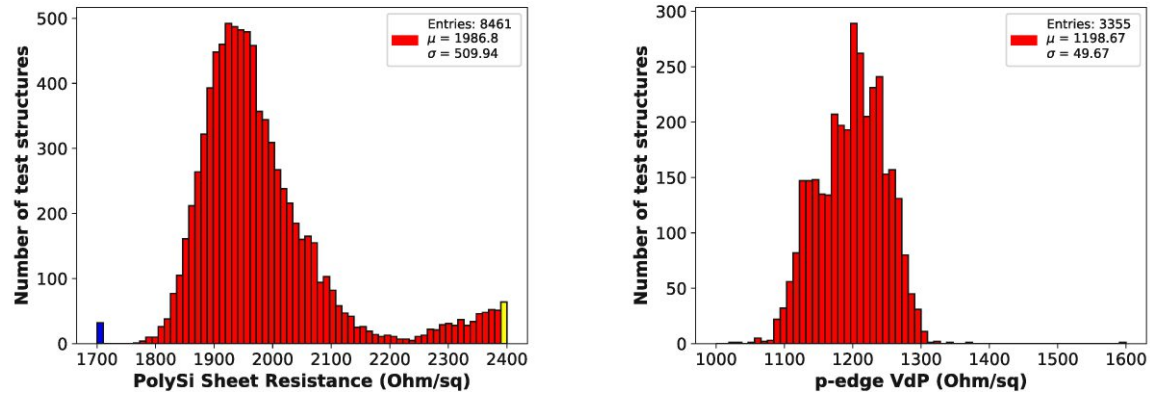
The histograms of the p-stop and n^+ implant line widths are illustrated in Fig. 9.48. For the strip implant, it is $w_{n^+} = 34.18 \pm 0.95\ \mu m$. For the 4-wire measurement, the line width of the p-stop implant yields $w_{p^+} = 49.84 \pm 13.16\ \mu m$.

9.9 Implants to metal contact resistance

The resistance of the contact between the aluminum and the n^+, p^+ and poly-silicon implants is characterized through measurements on the respective contact chain structures. As mentioned in section 8.2.12, the contact chain structure includes 228 adjacent contacts in a chain configuration, hence the measured value corresponds to the total resistance of the whole structure. Considering all the characterized contact chain structures to date, the following average values are obtained: $R^{n^+}_{cc} = 74.53 \pm 15.68\ k\Omega$, $R^{p^+}_{cc} = 81.16 \pm 9.09\ k\Omega$ and $R^{poly}_{cc} = 23.58 \pm 8.17\ M\Omega$.



(a) n^+ implant. **(b)** p-stop implant.



(c) polysilicon implant. **(d)** p^+ edge implant.

Fig. 9.46: Distribution of sheet resistance of different implants tested by PQC.

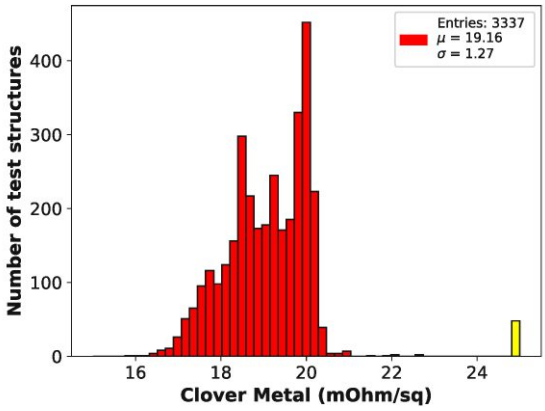
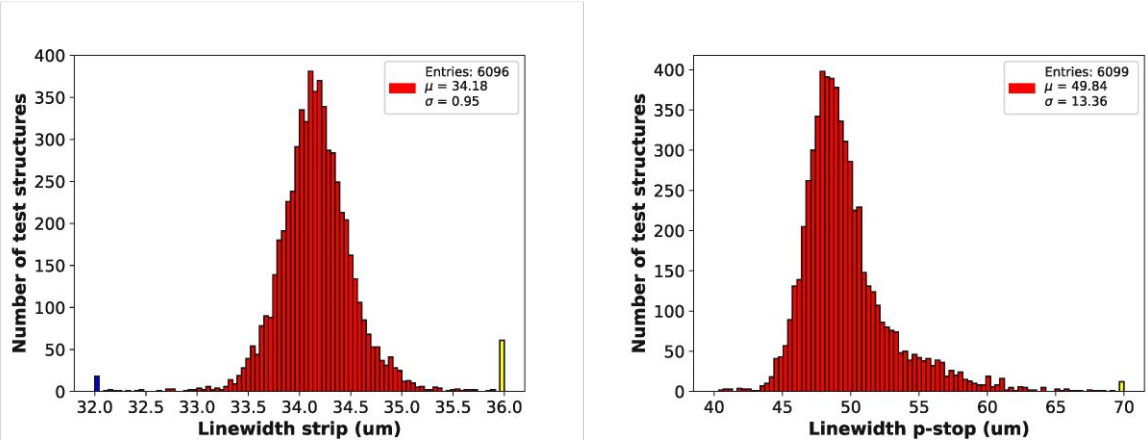


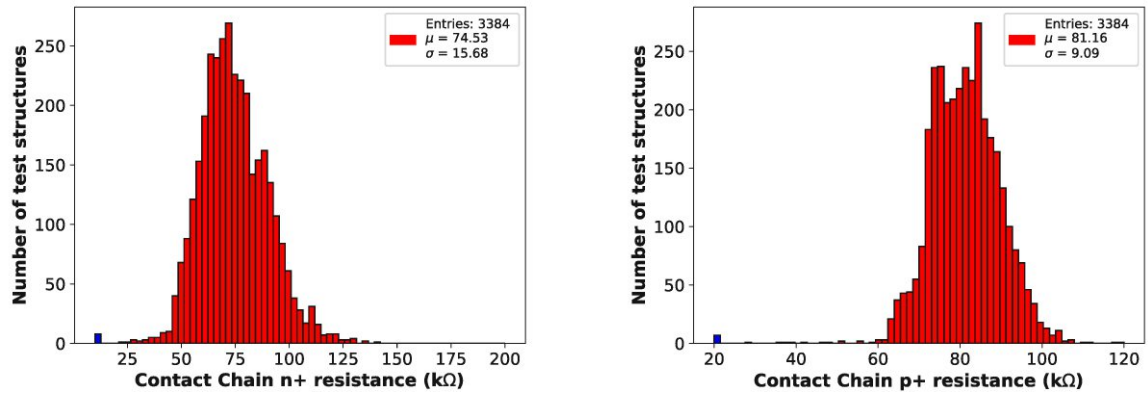
Fig. 9.47: Distribution of clover metal sheet resistance.

As discussed in section 8.2.11, the contact resistance between n^+ implant and aluminum as well as between polysilicon and aluminum can be also characterized through the Cross-Bridge-Kelvin-Resistor (CBKR). The distributions of the collected data from the two parameters are

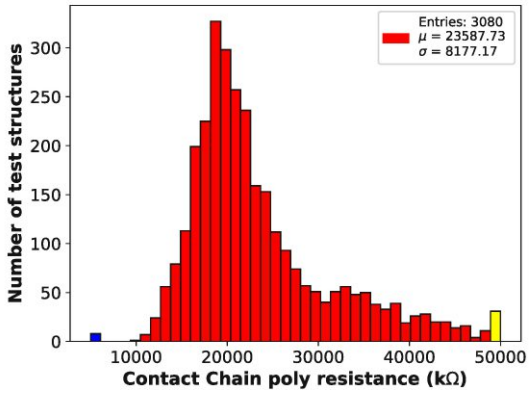


(a) n^+ implant. **(b)** p-stop implant.

Fig. 9.48: Line width of n^+ and p-stop implants.



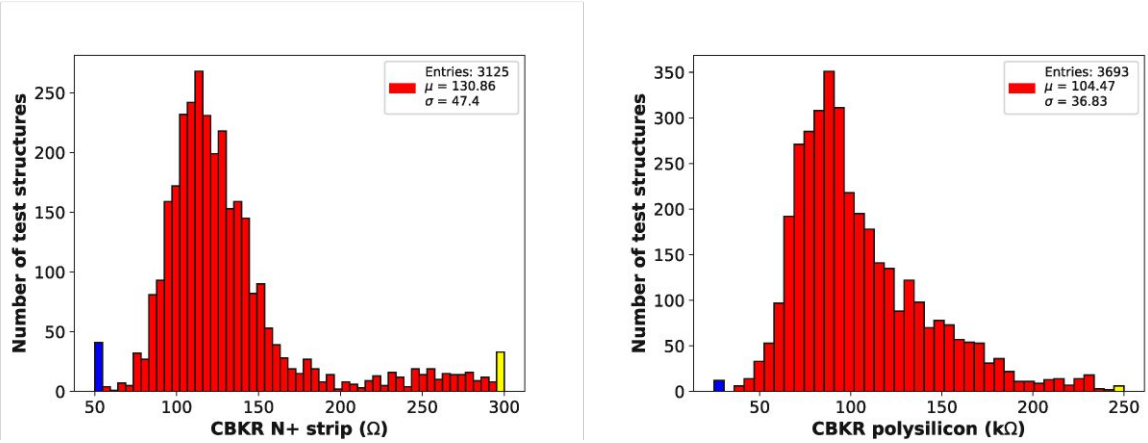
(a) n^+ implant. **(b)** p-edge implant.



(c) Polysilicon implant.

Fig. 9.49: Contact chain resistance of implants.

shown in Fig. 9.50. The extracted average values are $R_c^{n^+} = 130.86 \pm 47.40\ \Omega$ for the contact between n^+ implant and metal and $R_c^{poly} = 104.47 \pm 36.83\ k\Omega$ for the contact between the polysilicon and the metal.



(a) n^+ implant. **(b)** Polysilicon implant.

Fig. 9.50: Contact resistance of implants extracted from CBKR structure.

Since the contact chain structure consists of an arrangement of adjacent implants and overall 228 contacts between the metals and the implants, the expected total resistance of the structure can be calculated if one knows the contact resistance given by the CBKR structure, the implant sheet resistance and the aluminum resistance. Using the extracted averages for the $R_c^{n^+}$, R_c^{poly}, $R_{\text{sheet}}^{n^+}$, $R_{\text{sheet}}^{\text{poly}}$ and $R_{\text{sheet}}^{\text{al}}$, then:

$$R_{cc}^{n^+} = 228 \cdot R_c^{n^+} + \frac{228}{2} \cdot 2.5(R_{\text{sheet}}^{n^+} + R_{\text{sheet}}^{\text{al}}) \simeq 39.41 \text{ k}\Omega$$

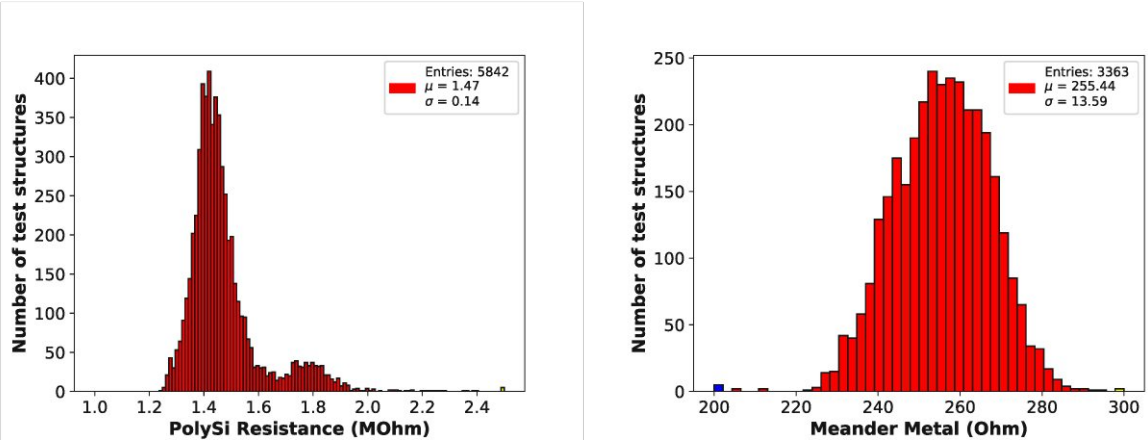
$$R_{cc}^{\text{poly}} = 228 \cdot R_c^{\text{poly}} + \frac{228}{2} \cdot 2.5(R_{\text{sheet}}^{\text{poly}} + R_{\text{sheet}}^{\text{al}}) \simeq 24.38 \text{ M}\Omega$$

The above estimation for the R_{cc} resistance agrees very well for the polysilicon contact chain. For the n^+ implant contact chain the measured R_{cc} is about two times larger than the estimated value. This discrepancy had been observed in earlier comparisons [88]. This inconsistency could be explained by some variations in the quality of the n^+ implant to metal contact, nevertheless a more in-depth investigation is required in order to understand this discrepancy.

9.10 Meander structures

The distribution of the measured values from the two types of meander structures hosted on the CMS wafers, the polysilicon and the metal meander, are illustrated in Fig. 9.51. The histogram of the polysilicon meander shows the two populations that agree with the observed distribution of the bias resistor in Fig. 9.17. The mean value is $R_{\text{poly}} = 1.47 \pm 0.14$ MΩ. For the metal meander, the structures tested to date give an average of $R_{\text{metal}} = 255.44 \pm 13.59$ Ω.

As shown in section 9.8, the sheet resistance of the aluminum is $R_{\text{sheet}}^{\text{metal}} = 19.16 \pm 1.27$ mΩ/sq. Assuming the design value of 12853 squares and considering $R_{\text{metal}} = 255.44$ as the mean meander resistance, a mean sheet resistance of about 19.87 mΩ/sq is expected to be calculated from the metal meander. There is a 4% variation between the expected and the measured metal sheet resistance. Therefore, considering the mean sheet resistance of $R_{\text{sheet}}^{\text{metal}} = 19.16$ mΩ/sq, an average



(a) Polysilicon meander. **(b)** Metal meander.

Fig. 9.51: Histogram of PQC meander structures.

number of 13332 squares is extracted. Hence, the width of the aluminum strip has an average value of 9.64 µm, smaller than the design width of 10 µm.

Regarding the polysilicon meander, a mean sheet resistance of $R_{sheet}^{poly} = 1.98 \pm 0.51$ kΩ/sq is extracted in section 9.8. Subtracting the mean value of the resistance of the contact between the polysilicon and the metal $R_c^{poly} = 104.47$ kΩ (section 9.9) from the mean polysilicon meander resistance and dividing by the mean R_{sheet}^{poly}, gives an average number of 689 squares. This value is slightly lower than the early results presented in [88] and shows a large variation from the design value of 476 squares. Therefore, the width of the polysilicon meander strip features an average value of 3.45 µm instead of the design value of 5 µm.

9.11 Conclusion from quality assurance results

The results presented in the previous sections include data from the production wafers which correspond to the first three years of mass production. This amount is sufficient to draw some solid conclusions about the quality of the Outer Tracker sensors as well as the stability of the production process. The following statements are by no means final conclusions as the production process is still ongoing.

- The production sensors exhibit very good bulk properties with low total dark current and well-controlled full depletion voltage which is well below the limit. The sensors are characterized by high-voltage robustness with about 97% of them showing no breakdown up to 1 kV. The total current at 600 V is typically in the order of some hundreds of nA. Only a few exceptions exhibit higher total current, in the order of µA, as shown in Fig. 9.4a. For these few cases, the elevated current at 600 V can be attributed to leaky strips (strips with higher leakage current due to possible defects), to scratches made during testing which deteriorate the sensor I-V behavior, or to the charge-up effect, as discussed in section 7.2. Moreover, after the first months of production, when wafers of lower resistivity were delivered to CMS (section 9.2), the full depletion voltage was stabilized, typically between 220 - 250 V.

- The good quality of the delivered sensors is indicated also by their negligible number of defective strips. Over all characterized strips, only a tiny fraction features larger strip

leakage current while a negligible number of pinholes has been detected so far. Sensors from one batch coming from the very first deliveries, showed regions of bad interstrip isolation and high-voltage instability. This batch was rejected. Non-critical issues were observed in the polysilicon resistance and the coupling capacitance with values near the limits. As discussed in sections 9.3.2. 9.3.3, these issues were resolved before they affected a larger fraction of the production.

- The uniformity which characterizes most wafer parameters measured by PQC, hints a good stability and reliability of the production process. This is a crucial requirement for any large-scale production. The results from the Sensor Quality Control are also indicative of the production stability, nevertheless, the information given by Process Quality Control provides a deeper insight. Variations across the wafers have been spotted on the p-stop doping which is indicated by the results from the MOSFET and the p-stop Van-der-Pauw structures (section 9.6).

- Deviations from the expected behavior of the measured parameters have been spotted in time due to the comprehensive quality assurance plan which combines the SQC and PQC procedures. The formation of trends is always a warning for potential inconsistencies or issues in the production sequence. All the observed trends among different parameters presented in this chapter have been discussed with the vendor in order to find solutions.

Chapter 10

Summary - Outlook

The high luminosity upgrade of the LHC will improve the capability of the accelerator which will be able to provide a peak luminosity of 5 - 7 $\times$ 10^{34} $cm^{-2}s^{-1}$ in the best case scenario. This upgrade will provide a higher potential for discoveries in the experiments which are located at CERN, one of which is the CMS experiment. The increase in luminosity will result in a larger number of interactions per bunch crossing with the number of pile-up events reaching 200 in the ultimate case. Each year of operation, the HL-LHC will deliver an integrated luminosity of about 300 fb^{-1} to the experiments.

The high pile-up and the large number of particles emerging from the interaction point at each bunch crossing create new challenges to the track reconstruction performance of the CMS Tracker. Moreover, the tracking system will be exposed to higher radiation levels. The current CMS tracking system is not expected to preserve its performance in the challenging environment of HL-LHC, hence an upgrade is required (Phase-2 upgrade). The full Tracker will be replaced. Radiation hardness, increased granularity, lower material budget, and contribution to the CMS Level-1 trigger decision are a few of the key elements that the new tracking system will feature.

In particular for the Outer Tracker, a driving force for its new design is the challenge to contribute tracking information to the Level-1 CMS Trigger. Due to bandwidth limitations, a reduction of the data sent out from the Outer Tracker to the Level-1 Trigger is required at each bunch crossing. The key for that is the discrimination of events coming from high transverse momentum (p_T) particles which will be performed by the Outer Tracker modules. Due to this functionality, they are known as p_T-modules. The p_T-modules comprise two aligned and closely spaced silicon sensors. The discrimination technique relies on the fact that the emerging particles from the interaction point are bent due to the 3.8 T CMS magnetic field and while crossing a module, they create a pattern of hits in the two sensors. The tracks that fall within an acceptance window set by the readout ASICs (typically > 2 GeV/c^2) correspond to high momentum particles and are called stubs. The stub data is transmitted to the CMS Level-1 track finder while the full information is read out upon a Level-1 trigger accept. There are two flavors of the Outer Tracker modules: the 2S and the PS module.

The Outer Tracker will be instrumented with about 26400 new silicon sensors. Both strip and macro pixel technology will be used. The macro pixel (known as PS-p) sensors together with strip sensors (known as PS-s) will populate the modules of the inner layers of the Outer Tracker. They will offer high granularity and precise measurement of the z coordinate in a region which is expected to cope with higher particle densities. The remaining layers, located at larger radii from the interaction point will be populated with strip sensors (2S) with about twice the size of the PS-s and PS-p sensors.

CMS quality assurance for mass production of silicon sensors

The production of the Outer Tracker sensors commenced in the summer of 2020 and is planned to finish by mid-2024. In order to accommodate the monitoring and characterization of this large production of sensors, CMS defined a Quality Assurance plan. This plan relies on three

main parts: Sensor Quality Control (SQC), Process Quality Control (PQC) and Irradiation Tests (IT). The SQC characterizes a sample of production sensors by measuring some of the most crucial sensor electrical parameters while the PQC characterizes, also on a sampled basis, the test structures which are developed on the same wafers with the sensors. The PQC can give a faster and more in-depth insight into some important sensor-related parameters, many of which can not be extracted directly from the sensors. In the scope of IT, samples of mini-sensors and test structures are irradiated up to the maximum fluence which the Outer Tracker will have received after the full lifetime of HL-LHC, and their electrical parameters are characterized. The Institute for High Energy Physics in Vienna (HEPHY) contributes to SQC and PQC by qualifying 25% of the total amount of delivered sensors and test structures.

Impact of external factors on electrical behavior of the Outer Tracker sensors

In the scope of Sensor Quality Control, besides the evaluation of the production quality, studies were conducted about the impact of the external environment on the behavior of the production sensors. A deterioration of the sensor electrical properties was observed due to the presence of electrostatic charges on the surface of the sensors. The charge-up effect is created by the packaging material, as it was confirmed by the vendor. A strong concentration of electrostatic charges on the surface of the passivation impacts the electric field distribution at the Si-SiO_2 interface and leads to a loss of the interstrip isolation. The impact of the charge-up was mostly pronounced on the measurements of the interstrip parameters and the resistance of the polysilicon bias resistors, while in some rare cases, it leads also to a sensor electrical breakdown. This issue can be mitigated with the use of an ionizing air device which can neutralize the negative charges and eliminate the impact of charge-up on the sensor electrical behavior.

Furthermore, studies presented in this thesis show that the long exposure of a sensor to high relative humidity levels can potentially deteriorate its electrical properties and introduce a breakdown inconsistent with its initial I-V behavior. The level of impact that exposure to a humid environment can have on the sensor I-V is important information for the module assembly, during which each sensor will be exposed to the high humidity ESD-safe clean rooms for several hours or days. For the cases of the affected sensors, a recovery process has been defined. The biasing of sensors at the breakdown voltage in a very dry environment such as 5% relative humidity can accelerate their recovery. The duration of the process could last from several minutes to several hours, depending on the response of each sensor. Establishing a warm and dry environment, with a temperature of 60°C or beyond could be also a successful strategy to evaporate the humidity from the sensor surface and restore its initial behavior.

Results from the quality assurance process

As the production of Outer Tracker sensors has exceeded 70%, the results extracted from the CMS Quality Assurance plan are sufficient to draw some general conclusions about the quality of the production process. The average total dark current of the production sensors to date is at least one order of magnitude lower than the CMS specification while the majority of them can be biased up to 1000 V without experiencing any electrical breakdown. Over the first months of production, several wafers featured lower resistivity than the specified limit (3.5 kΩcm) which resulted in a sensor full depletion voltage near the limit of 350 V. CMS discussed this issue with the vendor, and eventually, a material of higher resistivity within the target range was used. The full depletion voltage stabilized well below the limit.

The strip parameters are well within the CMS specifications and, in principle, uniform over production time. The number of strips which violate the specifications is negligible, most of which

come from strips with larger leakage currents. A negligible number of pinholes has been observed to date, most of which are related to damaged strips with scratches inflicted during testing. The resistance of the bias resistors showed larger values at the beginning of the production phase with the bias resistor of many strips approaching the upper limit of 2 MΩ. CMS requested the vendor to adjust the process in order to achieve a resistance near the target value of 1.5 MΩ which was successfully implemented. During the production period, the thickness of the strip thin oxide exhibited non-uniformity among different batches with many sensors featuring lower coupling capacitance, thus thicker strip oxide. The vendor made an adjustment in some parameters related to the thermal treatment process which resulted in a decrease of about 15% of the thin oxide thickness.

A good uniformity among subsequent batches is also shown in the electrical parameters extracted from the PQC test structures. The PQC proves to be a valuable tool in characterizing and monitoring the large-scale production of the Outer Tracker sensors and offers many opportunities to study in more detail several parameters which are related to the sensor properties. The most interesting observations extracted from PQC are summarized below:

- The flute diode structure, despite its non-optimal design with the opened edge ring, is able to characterize the bulk properties in terms of full depletion voltage and bulk resistivity. It provides an alternative way to the sensor C-V measurement in order to measure these parameters. The trend of the flute diode full depletion voltage agrees with the trend shown by the delivered sensors. The bulk resistivity can be in addition characterized by a Van-der-Pauw structure with contacts to the bulk. This structure provides a more reliable and robust way to extract this parameter, as it is shown in section 9.2.

- The implant sheet resistance of the polysilicon, the n^+ strip and the p^+ edge ring implants as extracted from the Van-der-Pauw structures, shows a good uniformity across each wafer and among subsequent wafers. However, this is not always the case for the p-stop sheet resistance. Significant inhomogeneity of the p-stop sheet resistance across some production wafers has been observed. This effect is consistently present on two specific corners of the wafer. This hints a variation of the process which impacts the p-stop doping concentration with respect to the wafer location. Apart from the p-stop Van-der-Pauw structure, the MOSFET with the p-stop implants between the source and drain confirms this observation. The threshold voltage of the MOSFET and the p-stop sheet resistance of the Van-der-Pauw structure are correlated, as expected since both parameters can reflect any p-stop variation. The interstrip resistance of the sensors which come from the affected wafers show no deviation from the typically observed values. Also, irradiation studies have shown no issues with the interstrip isolation after irradiation of the sensors from the wafers with non-uniform p-stop doping. This fact indicates that the p-stop doping concentration is sufficiently above a certain threshold which ensures a good interstrip isolation.

- The Si-SiO_2 interface properties show a quite uniform behavior to date. The flat-band voltage as extracted from the MOS capacitor is stable over production time and shows a consistent discrepancy between AC (2S, PS-s) and DC-coupled (PS-p) wafers. The PS-p wafers feature about 50% larger concentration of fixed positive oxide charges than the AC-coupled wafers. This reveals a variation in some parameters of the thermal oxide treatment process between the two wafer types. A similar effect can be seen in the surface current extracted from the Gate Controlled Diode (GCD) structure which indicates a larger presence of interface trap charges in the PS-p wafers. This higher concentration of oxide charges leads to a lower threshold voltage of the PS-p MOSFETs with respect to the 2S and PS-s MOSFETs, for a certain p-stop sheet resistance. Nevertheless, there is no impact

on the interpixel isolation of the PS-p sensors before and after irradiation. Hence, this discrepancy is not critical for the performance of the macro pixel sensors.

Conclusion

This thesis is a contribution to the Outer Tracker upgrade project with a main emphasis on the characterization of silicon sensor production. A fraction of this work focuses on the sensor quality and process quality control at HEPHY. I have contributed to the further development and improvement of the SQC setup for the electrical characterization of the production sensors, the supervision of the SQC and PQC procedures at HEPHY over the first 3 years of production and the development of a framework for the analysis of the experimental data and the extraction of the parameters of interest. Moreover, I developed tools for interacting with the CMS database, retrieving, processing and analyzing the data which are uploaded by all the SQC and PQC institutes. This makes it possible to make comparisons and check for trends and correlations by using the results from the total amount of characterized sensors and structures.

Based on the observations made at HEPHY during sensor characterization, procedures regarding sensor handling have been defined. The beneficial impact of sensor training was studied, especially on sensors which have been affected by the effect of long exposure to humidity. This process refers to the healing of sensors showing a breakdown through long-term biasing at the breakdown voltage in a low-humidity environment. In addition, a recommended procedure of recovery was defined for the sensors that are affected by the presence of electrostatic charges on their passivation layer. It must be noted that all these findings and procedures are based on the collective effort of the CMS Outer Tracker sensor group and thus, other collaborating institutes and colleagues have also a large contribution to this work.

A part of this thesis was devoted to investigations regarding the impact of humidity on the electric behavior of the Outer Tracker sensors. Studies were conducted according to the typical procedures followed by the Outer Tracker module assembly group in order to emulate the environmental conditions and the time of exposure experienced by the sensors during module assembly. The electric response of the sensors after a long exposure to the humidity levels of the ESD-safe clean rooms was examined. Furthermore, a recovery strategy was defined for those sensors which show a deterioration of their electrical behavior due to long exposure to high relative humidity.

Appendix A

Modification of the bias resistor design

The design of the bias resistor was modified in the first months of production due to a potential design weakness which was spotted in SQC. A small amount of sensors was delivered before the start of production for characterization and validation of the design. During the electrical tests, one sensor with an initially low total current showed a sudden increase in its total current and a breakdown in the subsequent I-V measurements. After a strip characterization, four subsequent strips with low resistance of the bias resistors were spotted. The investigation with an infrared camera showed that large current densities were located at these four strips at the strip implant edges, whereas in the older design, the corner of the polysilicon meander and the implant edge overlapped (Fig. A.2a). These tests took place in Kalsruhe Institute of Technology (KIT), therefore a more detailed description of the process and an illustration of the results can be found in [79].

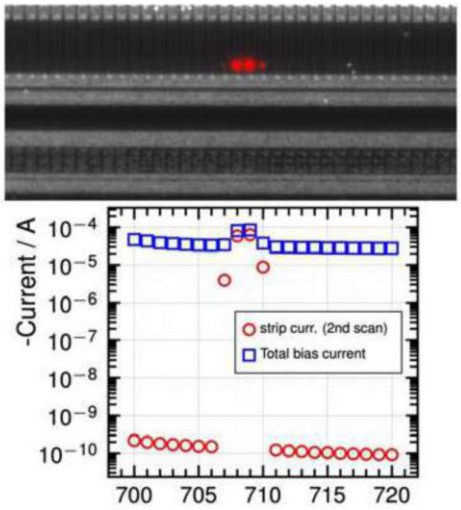
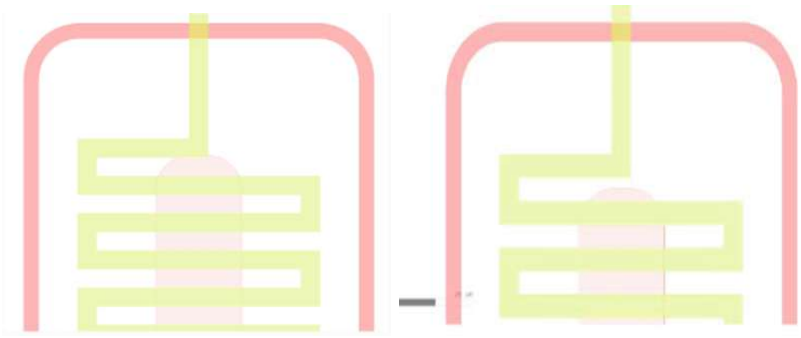


Fig. A.1: Top: Picture taken with an infrared camera at the region of bad strips. Bottom: The strip leakage current and the total current measured around this problematic region of strips. A high strip leakage current for strips 708 - 711 is evident. Courtesy of KIT and Andreas Nürnberg.

The polysilicon resistor is connected to the bias ring which is set to ground potential. When a strip features a high leakage current there is a potential between the resistor connection to the bias ring and the implant below the SiO_2 oxide. The electric field peaks near the implant edge, as discussed in section 4.2.4. Presumably, due to the overlapping with the sharp corner of the meander, the electric field could in under certain circumstances, increase beyond a critical field exceeding the dielectric strength of the oxide. This creates a short circuit between the implant and the polysilicon resistor. An oxide breakdown can lead to bulk damage which explains the increase in the total current.

CMS discussed the weakness in the R_{poly} design with HPK and requested to make a more robust design by shifting the bias resistor a few µm away from the edge implant, as shown in Fig. A.2b. The production of the first batches of production sensors was ongoing while this discussion was taking place, therefore a small fraction of the production sensors feature the old design of Fig. A.2a. It should be noted that during quality control of the production sensors with the old bias resistor design, no similar problems related to the bias resistor were observed. These sensors are qualified to instrument the Outer Tracker. In addition, this problem has not been observed during the qualification of the production sensors with the adapted bias resistor design.



(a) Design with overlapping edges **(b)** Modified design

Fig. A.2: Layout of the strip implant with the polysilicon meander (yellow). The implant (red) which encircles the strip is the p-stop.

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