Multi-Channel PWM Heater Control Chip in 0.18 μm High-Voltage CMOS for a Quantum Simulator

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Abstract—A circuit to control heating resistors with a pulse-width modulated (PWM) signal for a photonic quantum simulator is introduced. The output voltage is switched on for a changeable specified time and switched off for the rest of the period. The length of the resulting current and voltage pulse determines the mean heating power on the resistors connected to the outputs. The PWM generation is delay-line based and fully scalable. The PWM signal has a voltage swing of 9.9 V to power the heating resistors and is also synchronized with an input clock. The chip is designed for an PWM base clock in the range of 100 MHz. The chip also includes transimpedance amplifiers (TIAs) to monitor light powers inside the photonic integrated circuit (PIC) of the quantum simulator. 40 PWM channels and eight TIA channels are monolithically implemented in an application-specific integrated circuit (ASIC) using a 0.18 μm high-voltage CMOS technology. The pulse duration for each channel can be set via a serial peripheral interface (SPI).

Index Terms—Heater control, cascoding, PWM, delay line, CMOS, photonic quantum simulator, quantum simulator.

I. INTRODUCTION

SILICON photonics is utilized in increasing numbers of applications, such as flexibly controllable and scalable switches [1], [2], [3] and quantum applications [4]. While photons are difficult to use in universal quantum computers, since they are bosons and do not interact with each other, they are very promising candidates as quantum objects for quantum simulators. While these quantum simulators are not as universal as quantum computers, real problems such as optimization problems can be solved using these photonic devices. Photonic quantum simulators which are to a large part based on discrete optics have made huge progress in the last few years. In 2020, a Gaussian boson sampling quantum simulator has been published that supposedly reached quantum advantage [5]. While this result is impressive, and an even further increase of the simulator's complexity has been shown in 2021 [6], it seems evident that for significant further scaling integrated silicon photonics could be very promising. While current quantum simulators in silicon

photonics do not reach the high number of photons of [6] yet, the very nature of integration promises that this should change in the future. To keep the photonic quantum simulator flexible and to allow to map many problems to it, the quantum simulator should be flexibly programmable.

One way to add flexibility to a quantum simulator is to add programmable phase shifters in the arms of integrated interferometers built from integrated waveguides [7]. Programming the phase shift seen by the light while passing through the waveguide can be achieved by utilizing many different physical effects, such as electro-optic effects, dependence on the density of free carriers or thermo-optic effects [8], [9], [10]. The latter combines efficient integration as well as low loss.

The thermo-optic effect describes the dependency of the refractive index on the temperature. Using integrated heaters built from resistors, the temperature of the waveguide is controlled. Therefore, it is necessary to power heating resistors near the areas where the refractive index should be changed. Scaling of the photonic quantum simulator to higher numbers of photons also results in increasing numbers of programmable phase shifters, which necessitates efficient and scalable control circuitry. Goal of the chip presented in this paper, is the efficient control of heaters integrated in a silicon photonics quantum simulator developed in the EU project EPIQUS, based on silicon nitride waveguides [11].

The simplest way to control the heating power of the resistors is to apply a constant (in time) voltage to the resistor and change the voltage with a controller to adjust the generated heat. The loss in a linear regulator strongly depends on the required heating power in the heating resistor [1]. [9] shows that using digital switching of the heater resistors can reduce the power dissipation of the controller considerably. For an ideal switch and zero load capacitance there are no power losses in the controller, because either the voltage across the switch or the current through it is zero and there are no charging/discharging losses. Therefore, the PWM approach is used to control the heating power. In real MOSFET switches, the on-resistance is not zero and a small voltage drop across the MOSFET occurs in the on-state. In addition, unavoidable charging and discharging of the parasitic capacitance of heating resistors and metal traces to them cause additional power dissipation. However, a theoretical investigation and also complete circuit simulations show that the PWM approach causes a much lower power dissipation in the control circuits (depending on the load capacitance) than using a linear regulator. A theoretical comparison of the
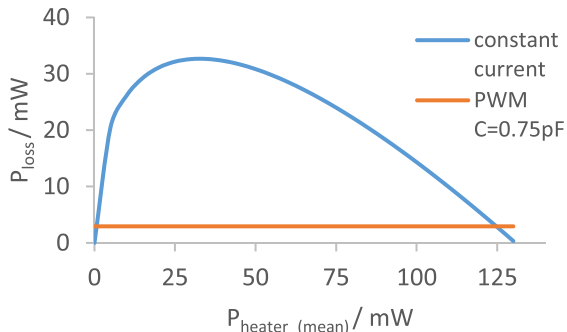
Fig. 1. Theoretical power losses in the driver compared for constant voltage/current heating and PWM heating (R_{on} of the PWM switch neglected; without any control and level shifter) for a 750 Ω heating resistor.

charging/discharging losses by using a PWM approach and of the losses of a constant current/voltage driver is shown in Fig. 1. Since the charging/discharging losses are (linear) proportional to the capacitance, it is advantageous to keep it small. The maximum capacitance of the metal line to the heater on the PIC of 0.75 pF is considered for the PWM approach. The theoretical power saving of the PWM approach is up to a factor of 11 compared to the constant current regulator. The lower power dissipation of the PWM controller chip is especially important for 3-dimensionally integrated control circuits and photonic chip (PIC), because the controller chip then heats indirectly the complete PIC.

The heater power is proportional to the duration of the voltage pulses applied to the heating resistor (Be aware that the voltage of the pulses is constant). Therefore, this control approach is called pulse-width modulation (PWM). This means that the voltage on the heater is switched on and off at a fast rate (to keep the thermal ripple at the heaters small). By switching the voltage on for a specific time every period, the resulting mean heating power is set. The duty cycle (expressed in percent) describes the proportion of the time the voltage is switched on to the total period. Lower duty cycles correspond to lower heating powers. The PWM period must be short in relation to the thermal time constant because switching on and off causes a temperature ripple. To further reduce the impact of the small ripples, the PWM signal is also synchronized to an input clock signal for synchronization of the laser pulses in the quantum simulator. This synchronization is an advantage over the free running PWM approach introduced in [9]. In addition, the individual PWM channels (on the ASIC) are delayed to each other over the whole period to reduce strong spikes on the supply voltages, which occur due to bond-wire inductance. The constant phase, as the goal of the synchronization, is thus nevertheless ensured within each channel. The circuits are designed for a period of about 12.5 ns (80 MHz) which corresponds to the specified laser clock for the quantum simulator. With an adapted bias distribution, a base clock up to 300 MHz would be possible.

Since the power is the product of the voltage and the current, the voltage must be as high as possible to keep the current as low as possible and thus reduce the ohmic losses on the metal lines. The metal lines to the resistors need to be narrow to reduce
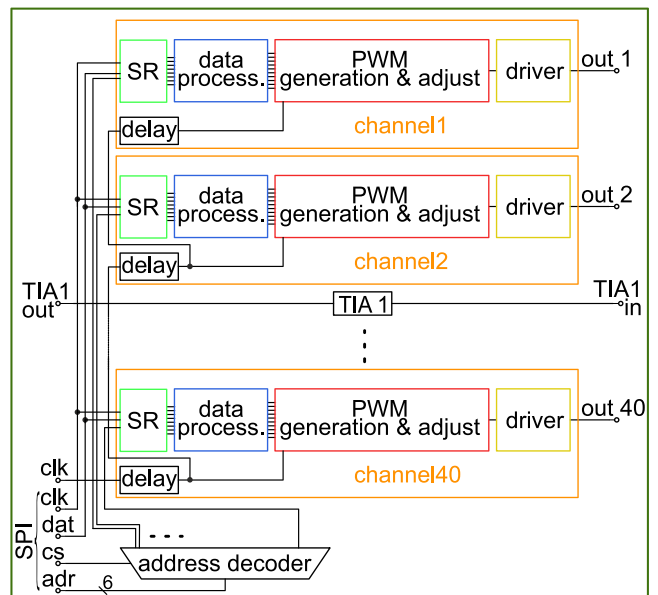

Fig. 2. Block diagram of PWM chip with 40 channels and monitor TIAs.

the parasitic capacitance to enable the high switching frequency. Nevertheless, it is necessary to switch the voltage very fast to keep the power dissipation during the voltage transient low and therefore fast MOSFETs are necessary which limits the possible voltage swing. The proposed circuit can output a voltage swing of 9.9 V and reduces therefore the current and the losses on the metal lines to the resistors. In this work, we use 0.18 μm high-voltage CMOS and double cascoding with 3.3 V transistors for the realization of the PWM chip with 40 channels. To the best of the authors' knowledge, the proposed PWM chip is the first one using double cascoding and outputting a 9.9 V 80 MHz PWM signal.

II. PWM CHIP

Fig. 2 shows the simplified block diagram of the multi-channel PWM chip. The proposed system consists of an address decoder and 40 separate PWM channels (orange), which all include a delay block, a shift register stage SR (green), a data processing unit (blue), a PWM generation and adjustment unit (red), and a double cascoded driver (yellow). The circuit is designed with 1.8 V and 3.3 V MOSFETs in 0.180 μm CMOS technology. The 3.3 V transistors are used to reach a voltage swing of 9.9 V at the heating resistors and the faster 1.8 V transistors are employed for all other parts to ensure the best possible timing performance and to reduce power consumption. The chip also includes eight transimpedance amplifier channels to monitor the light power on the PIC.

The address decoder for the SPI interface has 6 address bits (adr) to select one of the 40 channels. The SPI includes a serial data (dat), a clock (clk) and a chip select (cs) input. Every channel can be controlled via the SPI by setting a value from 0 to 511 (000000000 – 111111111) via the serial data input (dat).

The clock for every channel (PWM) is delayed after every channel to distribute the switching times as evenly as possible
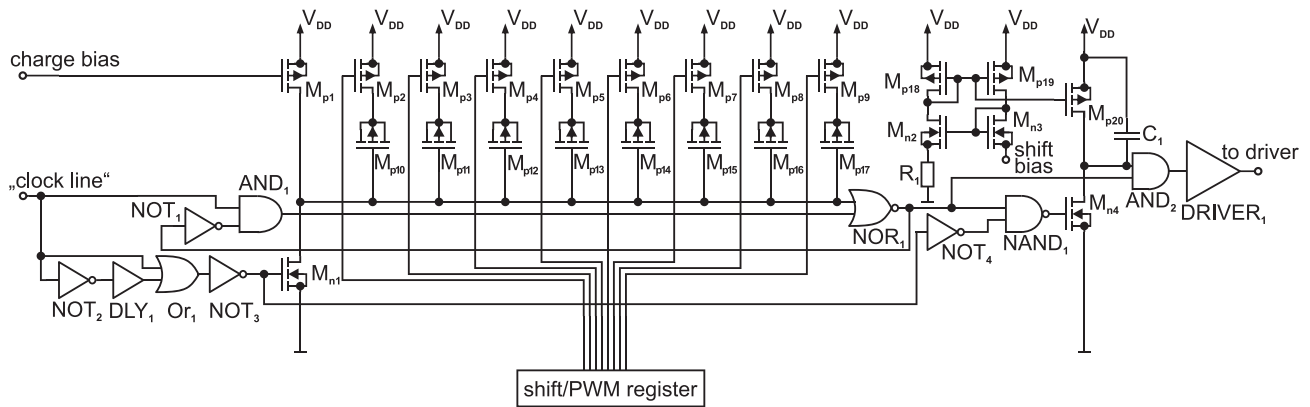
Fig. 3. Circuit diagram of the PWM generator and of the PWM adjust with MOSCAPs (8bit, a previous version).
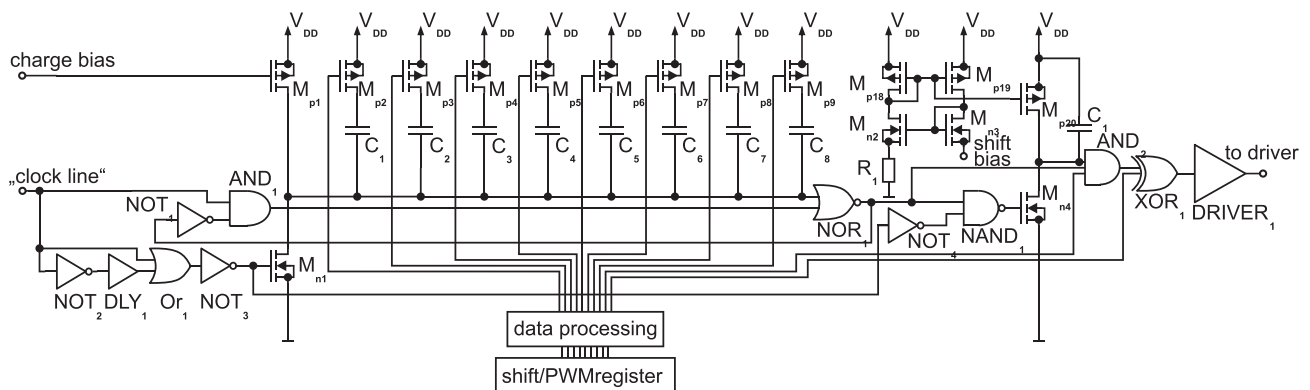

Fig. 4. Improved circuit diagram of the PWM generator and of the PWM adjust with DMIM capacitors (9bit version).

over the PWM period. There are two bias voltage inputs to adjust the generated PWM signal to cope with process and temperature variations and adapt the PWM generation to different base frequencies. One bias (charge bias V_{charge}) determines how fast the mean heating power increases with increasing digital values. The other bias voltage (shift bias V_{shift}) shifts the mean heating power for all digital values up or down.

III. PWM CIRCUIT

A. PWM Generation and Adjustment

Each PWM channel has a dedicated PWM generation unit. The PWM generator is based on a delay line principle [12], [13], [14]. Fig. 2 shows the principle adapted to the application in the quantum simulator. Switchable binary weighted capacitors which are charged with a constant current define the delay, i. e. the length of the heating pulse and therefore the mean heating power. Within the capacitor bank ($C_1 - C_8$) each of the 8 capacitors can be switched on or off with MOSFETs, which are controlled according to a register set via the SPI input. To obtain a more linear behavior, the capacitors and the corresponding MOSFET switches ($M_{p2}-M_{p9}$) are split into small unit transistors and are distributed to get a better matching. The more capacitors are active, the longer the PWM pulse and the higher the heating power. The bias input "charge bias" controls the charging current of the capacitor bank. A higher value causes the capacitors to be charged faster and therefore the shortest and the longest pulse length is shorter. To reduce the parasitic capacitance to the substrate and therefore the minimal possible capacitance Double Metal-Insulator-Metal (DMIM) capacitors are used (see Fig. 4) instead of the first investigated MOSCAPS (see Fig. 3) which had a higher area capacitance. Also, the p-wells under the DMIMs are removed to reduce the capacitance to substrate. Even if all capacitors are switched off, the capacitance on the delay line is not zero because of the parasitic capacitances. The load time and therefore the shortest possible pulse duration is therefore always significantly larger than zero. To achieve lower heating powers, the pulses are shortened. This reduces the smallest possible heating power and shifts the heating powers down, but also reduces the maximum possible heating power. The shift is done by charging C_1 with a constant current from M_{p20} and the AND_2 logic gate. The shift can be externally controlled via the "shift bias", which controls the drain-source current through M_{p20}. Depending on PVT, only a duty cycle between 0% and about 70% is possible with the tuning range of the capacitors (first 8 bits via SPI). Therefore, the 8-bit version (Fig. 3) was not fabricated.

To solve the problem with the limited duty ratio, the data processing block was added in the block diagram (see Figs. 2 and 4), the PWM control circuit was extended to a ninth bit and
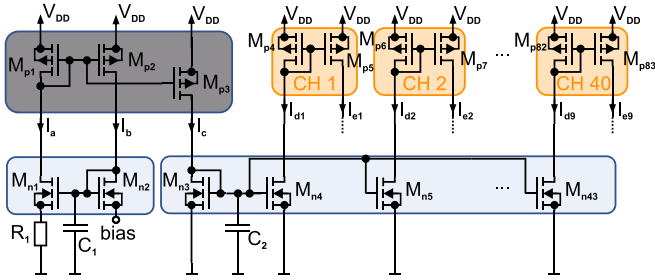
Fig. 5. Bias current distribution for 40 PWM channels.

an XOR gate was implemented. Depending on the ninth bit, all bits in the data processing unit and the output are inverted. The ninth bit adds the digital values from 256 to 511. The start and end trigger of the PWM pulse is swapped with the activation of the ninth bit, which enables the utilization of the remaining duty cycles. This is done automatically in the data processing unit and does not need to be taken into account when specifying the values 255 - 511. The phase to the input clock jumps at the transition from 255 to 256, but remains constant within these values. If the bias voltages are not adjusted, the values from 256-511 (ninth bit active) would in the case described above correspond to a duty cycle from about 30% to 100%. In the transition from 255 to 256 the power drops from 70% to 30%. If the bias voltages are adjusted, it is possible to shift the pulse width, to get a duty cycle from 0% to 50% for digital values 0 to 255 and 50% to 100% for digital values 256 to 511. The data processing also ensures that the output is constant off for the digital value 0 (000000000) and constant on for the value 511 (111111111).

B. Shift Register and Data Processing

To store and set the duty cycle and therefore the mean heating power of every channel separately each channel has a 9-bit shift register to store a digital value. A custom serial peripheral interface (SPI) with 11 input pads including a reset input is implemented to access the shift registers. To set all channels to zero (000000000) and to power off all channels a separate reset input is used. A central 6-bit address decoder is used to select one of the 40 channels if the chip select input (cs) is enabled. The shift register in the selected channel receives 9 data bits via the serial data input line (dat). Each bit is sampled at the positive edge of the SPI clock. A SPI clock frequency of up to 200 MHz is possible. The design was done with a digital VHDL workflow implemented in the mixed signal layout.

C. Bias Distribution

To reduce the number of bond pads, all 40 channels, use the same charge and shift bias, which means that it has to be distributed along the about 8.6 mm wide chip. According to [15], [16] and our own simulations, current compared to voltage distribution over long distances achieves a better matching. In the proposed circuit the distribution is done with multiple current mirrors which are locally matched, shown in Fig. 5. Matched MOSFETs are in a common-colored field in the illustration. The
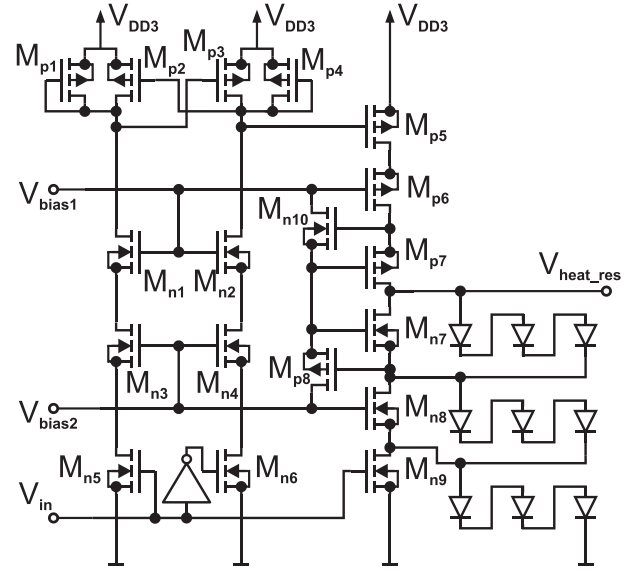

Fig. 6. High-voltage double-cascoded switch (HVCS) with adaptive bias shift and voltage level shifter (MP1-Mp4; Mn1-Mn6) and protection diodes. The switch corresponds to the driver in Fig. 1.

blue marked transistors are centrally placed and matched, the orange marked ones are placed in the 40 channels. The currents I_a and I_b are defined by the bias voltage and the internal resistor R_1. This current is mirrored via M_{p3} with a mirror ratio of 1 to I_C. This current is again mirrored with 40 NMOS transistors (M_{n4}-M_{n43}) to the current mirrors inside the channels. The metal tracks to the channels (I_{d1}, I_{d2}, …) are up to 4.5 mm long. As long as all transistors are in saturation the different resistance and therefore the voltage drop on the long tracks have only a negligible effect on the current mirrored inside the channels.

D. High-Voltage Cascode Switch (Driver)

The main advantage of using the PWM technique is that it reduces the power losses in the driver. Theoretically (for infinitely fast switching) there is no voltage drop at the output transistors of the driver, if it is switched on and there is no current through the driver when it is off. Because the power is the product of voltage and current, there would be no power loss. In reality, of course, this is not quite the case and depends especially on the switching losses during the transition time and on the voltage at the driver in the switched-on state (due to ON resistance of the MOSFETs). The switching losses are therefore strongly dependent on the transition time, which is largely determined by the capacitive load. To reach the fastest possible transition times with a voltage swing of 9.9 V in the $0.18 \mu m$ technology a high-voltage double-cascoded switch (HVCS) with adaptive bias voltages is used. The proposed driver switch for a maximum swing of 9.9 V is shown in Fig. 6 (Mp5 – Mp7 and Mn7 – Mn9; a modified version of the quenching switch of an active SPAD quencher realized in 0.35 μm CMOS presented in [17]). The output (V_{heat_res}) of the switch is connected to one side of the resistor the other side is connected to VDD = 9.9 V. Theoretically only the transistors M_{n7} - M_{n9} are needed to switch
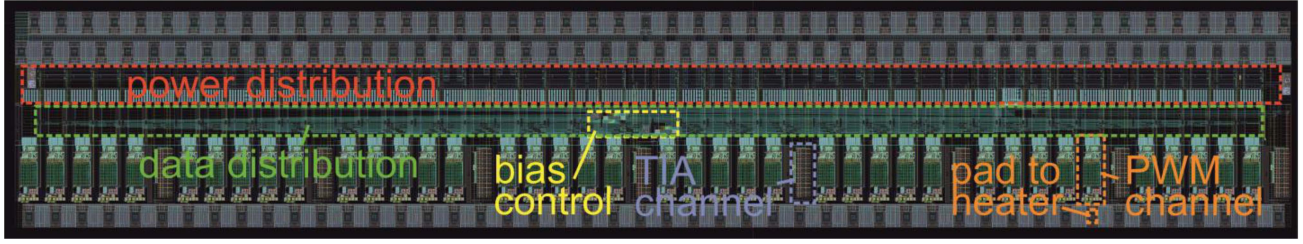
Fig. 7. Layout of the PWM chip.

"on" and "off" the heating resistors because the output would automatically charge back to 9.9 V if the transistors are switched off. To reach faster transition times also the transition to 9.9 V is done with MOSFETs (M_{p5}-M_{p7}).

The driver is built with standard 3.3 V transistors. The output is switched between 0 V (ground) and 9.9 V. Therefore, an output voltage of 0 V corresponds to the maximum heating power ("on" state) and an output voltage of 9.9 V corresponds to zero heating power ("off" state). The three stacked NMOS MOSFETs M_{n7} – M_{n9} have to withstand 9.9 V when the output is "off" because the transistors PMOS M_{p5} – M_{p7} pull the output to V_{DD3} = 9.9 V. The three stacked transistors M_{p5} – M_{p7} have to sustain 9.9 V, when the output is "on" and the MOSFETs M_{n7} – M_{n9} pull the output to ground. At least three transistors for each side are required since the nominal voltage of one single transistor is 3.3 V. The bulks of the MOSFETs M_{p5} – M_{p7} and M_{n7} – M_{n9} are connected to their corresponding sources. All transistors are isolated with medium deep n-wells. The corners of the p-wells of the transistors M_{n7} and M_{n8} are rounded to withstand the occurring higher voltages than the nominal 8 V between the p-wells and the deep n-wells. To save space, the MOSFETs M_{n7} and M_{n8} are in the same medium deep n-wells.

The driver should be either "on" or "off", therefore the upper transistors and the lower transistors are inversely controlled. Since there is a voltage difference between M_{p5} and M_{n9} a level shifter is necessary. This is done with the MOSFETs M_{n1} – M_{n6} and M_{p1} – M_{p4}, based on [18]. It ensures that the control voltage at the gate of M_{p5} is in the range of V_{DD3} = 9.9 V to V_{bias1} = 6.6V. If the switch is turned "on" (V_{in} = 1.8 V) the transistor M_{n9} switches on and the transistor M_{p5} switches off, because the level shifter applies V_{DD3} to the gate of M_{p5}. The drains of M_{n9} and M_{p5} are discharged to ground (0 V) and V_{bias1} + V_{Th}, respectively. The transistors M_{n8} and M_{p6}, respectively, switch on and off because the gate of M_{p6} is at a fixed bias voltage of V_{bias1} = 6.6 V and the gate of M_{n8} is at a fixed bias voltage of 3.3 V. The drain of M_{n8} is discharged to ground. Therefore, the transistor M_{p8} is in the on-state and shifts the voltages on the gate of M_{n7} and M_{p7} to V_{bias2} = 3.3 V. This shift at the gate of M_{n7} sets this transistor into the on-state and discharges its drain and therefore the output to ground (0 V). Because of the shift at the gate of M_{p7} the transistor is now in the off-state. The adaptive bias circuitry (M_{n10}, M_{p8}) is necessary to keep the voltages on M_{n7} and M_{p7} in the process limits. Due to the different output pulse lengths, there are conditions that would exceed the absolute maximum rating of the MOSFETs M_{n7}-M_{n9}. To reduce the voltages, protection diodes shown in
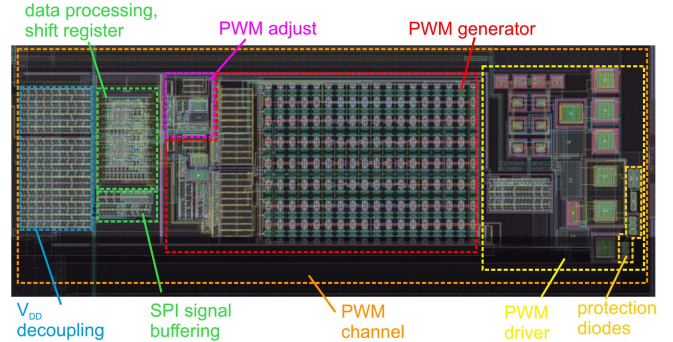

Fig. 8. Layout of one PWM channel.

Fig. 6 are used to distribute the drain-source voltage more evenly. The used diodes are polysilicon diodes with a higher forward voltage compared to crystalline-silicon diodes. The resulting current at 1.1 V (9.9 V evenly distributed) is nominally 1.93 μA according to circuit simulation.

E. Layout

The PWM ASIC with the 40 PWM and 8 monitoring channels has a size of about 1.5×8.7 mm^2. The layout of the whole chip is shown in Fig. 7. There is a double pad row which includes data, clock, bias and various power supply voltage pads. The single pad row includes the output pads to the 40 heaters and the eight transimpedance amplifiers (blue) current input pads. The power and the data distribution take a relatively large area because of the high currents needed and the high number of data lines. One PWM channel is presented in Fig. 8. The chip area of such a PWM channel is 170×440 μm^2. The layout of each channel is tuned to a pitch of 180 μm, which was chosen to meet the requirements of the integrated photonic chip. The layout of the channels could be adjusted to achieve a smaller pitch in the range of 100 μm, limited mainly by the bond pads. A smaller pitch would have no effect on the static power consumption and would only slightly increase the dynamic power consumption due to longer metal lines. Since the total area of the PWM channel will stay approximately the same, the width of the layout in Fig. 8 would increase, resulting in longer metal lines.

IV. CHARACTERIZATION OF CHIP

The measurement setup consists of two programmable power supply units, a pulse generator (Agilent 81134A), the Picoprobe
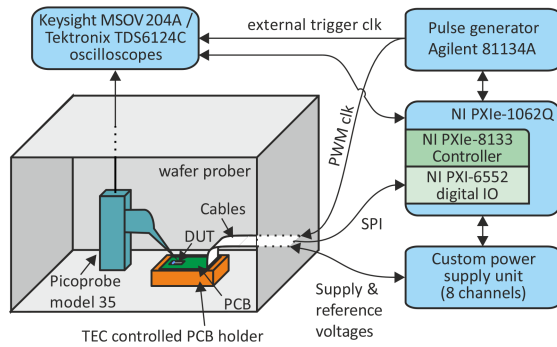
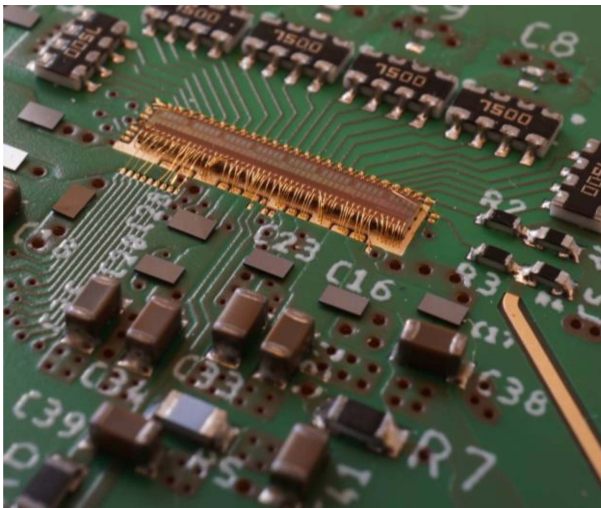Fig. 9. Measurement setup for characterizing the PWM chip.

Fig. 10. PWM chip bonded with gold bond wires to the test PCB.

Fig. 11. Measured transient voltage on heating resistor 24 on the PCB at the selected digital value using 8 bits ($V_{charge} = 0.15$ V, $V_{shift} = 0.25$ V).

model 35 and two different oscilloscopes (Keysight MSOV204A and Tektronix TDS6124C), controlled by a PXI system from National Instruments (NI), comprised from the chassis NI-PXIe-1062Q and the controller NI PXIe-8133, as depicted in Fig. 9. The digital signals for programming the SPI are generated with the NI PXI-6552 digital IO card.

The PWM chip is glued and wire bonded onto a test PCB (printed circuit board) with FR4 substrate including various decoupling capacitors close to the pads, shown in Fig. 10. The heating resistors (750 Ω) in this test setup are not bonded to a PIC, they are placed directly on the PCB. The PCB is placed on a thermoelectric cooler (TEC) set to 25°C, having in mind that the PIC has to be cooled anyway, because of the heating power of many phase shifters. The cooler, the picoprobe, and the PCB are placed inside a wafer prober PA 200 from Karl Suss. The pulse generator supplies a base clock of 80 MHz to the PWM signal input of the chip and to the external trigger of the used oscilloscope. The needle of the picoprobe is placed onto the corresponding bond pad on the PCB and the output of the picoprobe is connected to the used oscilloscope. The 20 GHz Keysight MSOV204A oscilloscope is used to measure the voltage transients for extracting the rise and fall times. The Tektronix TDS6124C oscilloscope is used for all other
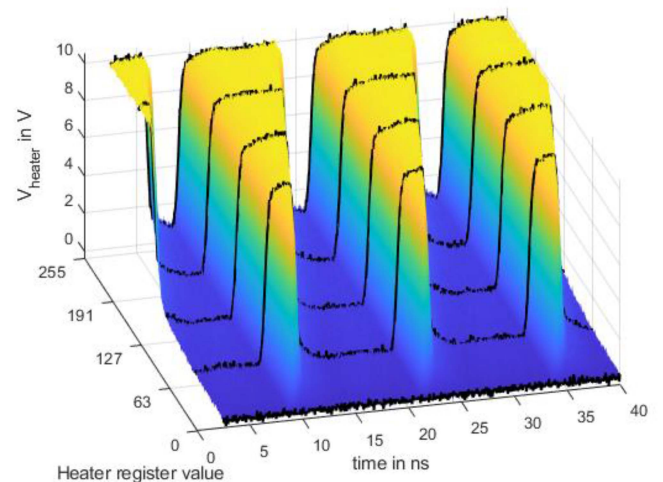
measurements due to availability of the measuring equipment. The SPI and therefore the shift register of every channel are accessed via the digital IO card of the PXI system.

In the first measurements, only the first 8 bits are used. This makes it possible to change the power at the resistor without a (possibly small) jump in power and phase. However, it limits the maximum tuning range and therefore the maximum power. Compared with the maximum possible heating power with a constant voltage (9.9 V at the resistor) only 70% of this power is achieved. The charge and the shift bias are therefore adjusted so that the charging speed is slower and longer pulses with smaller digital values are reached. The charge bias V_{charge} was set to 0.15 V and the shift bias V_{shift} was set to 0.25 V to reach the maximum possible tuning range (70%) with only 8 bits. Fig. 11 shows the transient voltage on a heating resistor over time and for different digital values. The color indicates the voltage level. The increase in pulse width with increasing digital values is shown. At a digital value of 255, a duty cycle of approximately 70% is achieved. This corresponds to approximately 90 mW at the used 750 Ohm resistor. The 20%-to-80% rise time of the output voltage is 0.46 ps and the 80%-to-20% fall time is 0.44 ns.

Fig. 12 shows the mean heating power in percent for arbitrarily chosen heaters 14, 15 and 24 with only 8 used bits. The mean heating power

$$P_{heater} = 1/(R * T) * \int_0^T u_{heater}(t)^2 \ dt. \tag{1}$$

is calculated from the transient voltage curve $u_{heater}(t)$ shown in Fig. 11 for every digital value.

Fig. 13 shows the transient voltage on a heating resistor over time and for different digital values with 9 used bits. A tuning range from 0% to 100% is now achieved with 9 bits. The charge and the shift bias are set to reach a perfect transition from 255 to 256. The phase jumps at the transmission from 255 to 256 (where the 9th bit switches from 0 to 1), but stays then constant for all larger digital values.
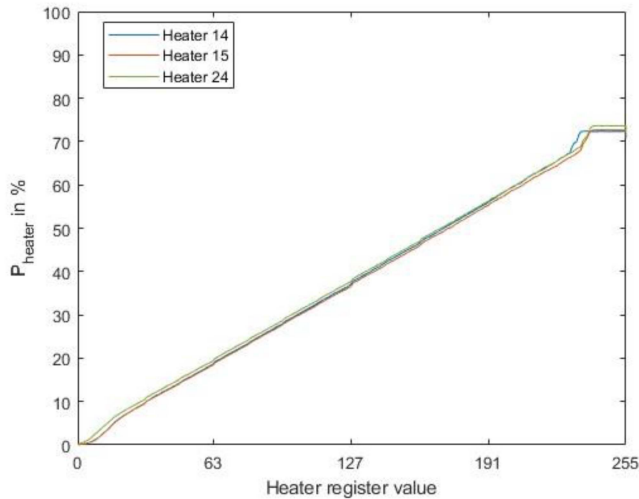
Fig. 12. Mean heating power of heaters 14, 15, and 24 at the selected heater register value using only 8 bits (V_{charge} = 0.15 V, V_{shift} = 0.25 V).
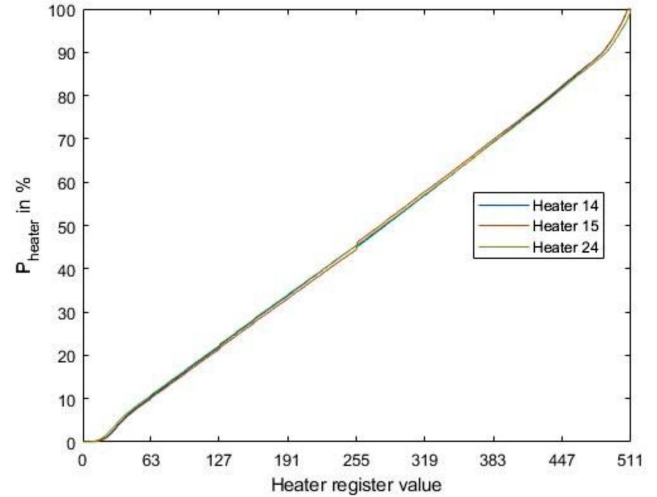

Fig. 14. Mean heating power of heaters 14, 15, and 24 at the selected digital value using 9 bits (V_{charge} = 0.25 V, V_{shift} = 0.38 V).
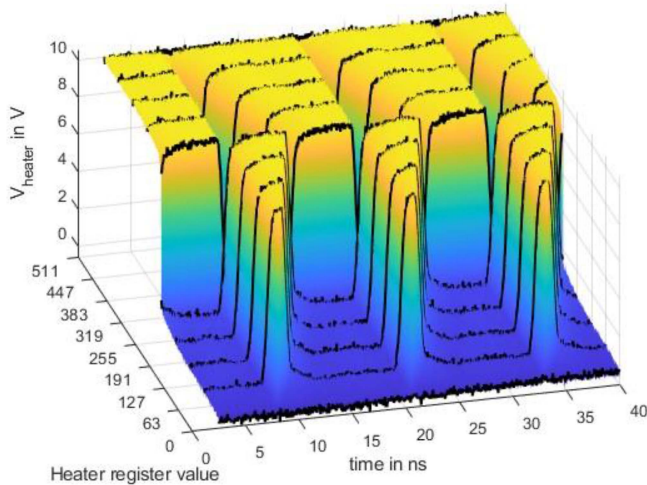

Fig. 13. Transient voltage on heating resistor 24 measured on the PCB for the heater register values using 9 bits (V_{charge} = 0.25 V, V_{shift} = 0.38 V).

TABLE I
COMPARISON OF REFERENCES WITH INTEGRATED HEATERS

Ref.	Type	Sync	Int.	PWM freq. (MHz)	Voltage (V)	Max. heater power (mW)
[19]	DC	-	N	-	<2.1	104
[20]	DC	-	N	-	<11	18
[21]	DC	-	N	-	n. r.	21
[22]	DC	-	N	-	n. r.	2.5
[23]	PWM	N	Y	78*	1.8	14
[24]	PDM	Y	Y	50 (400)	3.3	40
[25]	PWM	Y	Y	0.584	5	n. r.
[26]	PWM	Y	Y	9.4	1.8	14
[27]	PWM	n. r.	N	2	5	5
[28]	PWM	n. r.	N	4	2	25
This work	PWM	Y	Y	80	9.9	130

Y: yes; N: no; *: peak at 50% duty cycle; PDM: pulse density modulation, n. r.: not reported

Fig. 14 shows the mean heating power in percent for heater 14, 15 and 24 with 9 bits. The mean heating power is calculated in the same way as in (1) from the transient voltage.

The static mean power consumption of the hole chip is approximately 460 mW (corresponding to 11.5 mW per channel), where the largest part is caused by the level shifter. The maximum additional power dissipation of one active channel is approximately 15 mW.

Table I shows an overview of different references where integrated heating resistors are controlled. The heating power in references [19], [20], [21], [22] is controlled with a constant voltage or constant current signal (DC). As far as can be gathered from the papers, all DC solutions are controlled externally and not on-chip. This may be due to the fact that (as described in the introduction) the control with constant voltage/current can generate high losses in the controller. References [23], [24], [25], [26] also have fully integrated heater control circuits ranging

from 1.8 V to 5 V output swing and frequencies from 583.5 kHz to 50 MHz (65 nm CMOS, driver designed for 400 MHz). [27] and [28] are using an off-chip generated PWM signal to control the heating powers.

V. CONCLUSION

We designed and characterized a multi-channel PWM heater control chip in 0.18μm high-voltage CMOS for application in a quantum simulator. To ensure for each laser pulse the same temperature of the phase shifter and therefore the same phase of the photons, the PWM signal is synchronized to the laser pulses. The chip has 40 PWM channels which output a 9.9 V PWM signal with a power of up to 130 mW per channel at

a load resistor of 750 Ω. The approach is fully scalable and can be easily extended to more channels. Compared to the approach in 160 nm BCD8sP [26] with a peak output power of 14 mW the heating power is about nine times higher. The measured 20%-to-80% rise time of the output is 0.46 ns and the 80%-to-20% fall time is 0.44 ns. The measured static mean power consumption of the hole chip is approximately 460 mW at 80 MHz PWM base clock. The maximal additional power dissipation of one active channel is approximately 15 mW, compared to the maximal heating power of 130 mW. In a redesign, the used level shifter for the output driver should be replaced as it is responsible for a significant portion of the static power consumption.

For 3-dimensional integration of photonic integrated circuit and control ASIC, using PWM will decrease heat dissipation of the control ASIC to the photonic integrated circuit of the quantum simulator, which will allow to control a larger number of active photonic components in the quantum simulator for a given thermal budget, and therefore is crucial for scaling to more complex quantum simulators. Furthermore, temperature drifts within the simulator will decrease and will allow to control the photonic chip's global temperature with a smaller thermo-electric cooler. Additionally, the exceptionally high frequency of the PWM signal together with precise synchronization of the PWM signal with the laser pulses of the quantum simulator will reduce the effective thermal ripple far below critical limits required for this high precision application.

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