A PhD THESIS ON

Design and characterization of CMOS avalanche photodetectors

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Abstract

Detecting weak optical signals is crucial across diverse opto-electronic applications, from time-of-flight sensors and quantum cryptography to optical wireless communication and medical diagnostics via optical tomography. The avalanche photodiodes employ the avalanche multiplication effect, allowing for signal amplification, offering high sensitivity, thereby enabling the detection of weak optical signals across a range of applications. These photodiodes, depending on the operating voltage, can either provide moderate and linear avalanche amplification, which is called APD, or work in Geiger mode and provide a gain in the range of millions, known as SPAD. In addition, the use of a CMOS process for the production of integrated avalanche photodiodes with electronic circuitry for read-out and signal processing reduces the influence of parasitic effects, and furthermore offers a cost-effective production. Accordingly CMOS avalanche photodiodes are attractive candidates as optical detectors in many optical systems that require low-light detection.

This thesis begins by presenting a photon detection probability (PDP) model for SPAD, which is very valuable for the development and optimization of SPADs while avoiding time-consuming experimental investigations. The dependence of SPAD's PDP on the distribution of the electric field inside the structure and also the propagation behavior of the irradiated light to reach the photo-sensitive area of the photodiode are investigated and discussed based on the presented model.

Conventional design approaches towards CMOS-integrated avalanche photodiodes (APDs and SPADs) rely on planar n^+/p-well or p^+/n-well junctions. In these structures, the presence of physical guard rings to avoid a premature edge breakdown decreases the fill factor, defined as the ratio of the photo-sensitive area to the total device area. My research delves into investigating the implementation of virtual guard rings to enhance the fill factor within such structures. In addition to the low fill factor and limited scalability of these structures, they generally exhibit a trade-off between bandwidth and responsivity, notably observed in the long-wavelength range when they operate in the linear mode (APD operation mode).

To address these limitations, I implement the field-line crowding concept to design a new APD by employing a small n^+/n-well structure fabricated in a standard CMOS process without process modi-

fication. This structure provides a maximum bandwidth of 1.6 GHz with a responsivity of 32 A/W at a wavelength of 675 nm and at an operating voltage of 67 V while having a high sensitive-area to total-area ratio. Its scalability while retaining sensitivity and offering a large fill-factor makes it attractive for array sensor applications. Further characterization in the near-infrared range and investigation into design parameter effects on its performance are presented.

However, the high operational voltage of these diodes can present integration challenges with electronic circuits in some CMOS technologies. Therefore, this study introduces a novel CMOS-integrated dot avalanche photodiode, demonstrating comparable performance at significantly lower operating voltages compared to the field-line crowding APD. Additionally, my research proposes a n^+/p-well multi-dot structure, comprising an array of individual dots with a shared anode. This innovative design facilitates the expansion of the active area while upholding performance, thereby positioning the multi-dot APD as a promising solution for applications necessitating a larger light-sensitive area. Furthermore, leveraging the advantage of decoupling the P/N junction area from the light-sensitive area in such structures enables designing a high light-sensitive-area photodiode with a relatively small capacitance.

Kurzfassung

Die Erkennung schwacher optischer Signale ist in einer Vielzahl von opto-elektronischen Anwendungen von großer Bedeutung, von Time-of-Flight-Sensoren und Quantenkryptographie bis hin zur optischen drahtlosen Kommunikation und medizinischen Diagnostik über optische Tomographie. Avalanche-Photodioden nutzen den Avalanche-Multiplikationseffekt zur Signalverstärkung und bieten damit eine hohe photo-Empfindlichkeit, die die Erkennung schwacher optischer Signale über eine Vielzahl von Anwendungen ermöglicht. Je nach Betriebsspannung können diese Photodioden entweder eine moderate und lineare Avalanche-Verstärkung bieten, die als APD bezeichnet wird, oder im Geiger-Modus arbeiten und eine Verstärkung im Bereich von Millionen, bekannt als SPAD, liefern. Darüber hinaus reduziert der Einsatz eines CMOS-Prozesses bei der Herstellung integrierter Avalanche-Photodioden mit elektronischen Schaltungen zur Auslesung und Signalverarbeitung den Einfluss parasitärer Effekte und bietet eine kostengünstige Produktion. Demnach sind CMOS-Avalanche-Photodioden attraktive Kandidaten als optische Detektoren in vielen optischen Systemen, die eine Erfassung bei schwachem Licht erfordern.

Diese Arbeit beginnt mit der Vorstellung eines für die Photon-Detektions-Wahrscheinlichkeit modells SPADs, das für die Entwicklung und Optimierung von SPADs sehr wertvoll ist und zeitaufwändige experimentelle Untersuchungen vermeidet. Die Abhängigkeit der Photon-Detektions-Wahrscheinlichkeit von SPAD von der Verteilung des elektrischen Feldes innerhalb der Struktur und auch das Ausbreitungsverhalten des bestrahlten Lichts zur Erreichung des lichtempfindlichen Bereichs der Photodiode werden anhand des vorgestellten Modells untersucht und diskutiert.

Herkömmliche Designansätze für CMOS-integrierte Avalanche-Photodioden (APDs und SPADs) basieren auf planaren n^+/p-Wanne- oder p^+/n-Wanne-Übergängen. In diesen Strukturen führt das Vorhandensein physischer Schutzringe zur Vermeidung eines vorzeitigen Kantenversagens zu einer Verringerung des Füllfaktors, definiert als das Verhältnis des lichtempfindlichen Bereichs zur Gesamtfläche des Bauteils. Meine Forschung untersucht die Implementierung virtueller Schutzringe, um den Füllfaktor in solchen Strukturen zu verbessern. Diese Strukturen weisen jedoch im Allgemeinen einen Kompromiss zwischen Bandbreite und Empfindlichkeit auf, der besonders im langwelligen Bereich im

linearen Modus (APD-Betriebsmodus) zu beobachten ist.

Um diese Einschränkungen zu bewältigen, setzen ich das Konzept der Feldliniendichte ein, um eine neue APD durch Verwendung einer kleinen n^+/n-Wanne Struktur zu entwerfen, die in einem herkömmlichen CMOS-Prozess ohne Prozessänderungen hergestellt wird. Diese Struktur bietet eine maximale Bandbreite von 1,6 GHz bei einer Empfindlichkeit von R=32 A/W und einer Wellenlänge von 675 nm sowie einer Betriebsspannung von 67 V, wobei das Verhältnis von lichtempfindlichem Bereich zur Gesamtfläche hoch ist. Ihre Skalierbarkeit bei gleichzeitiger Beibehaltung der Photo-Empfindlichkeit und Bereitstellung einer größeren lichtempfindlichen Flache macht sie attraktiv für Anwendungen mit Arraysensoren. Weitere Charakterisierungen im nahen Infrarotbereich und Untersuchungen zu den Auswirkungen von Designparametern auf ihre Leistung werden vorgestellt.

Die hohe Betriebsspannung dieser Dioden kann jedoch in einigen CMOS-Technologien Integrationsherausforderungen mit elektronischen Schaltungen darstellen. Daher stellt diese Studie eine neuartige CMOS-integrierte Avalanche-Photodiode vor, die vergleichbare Leistungen bei deutlich niedrigeren Betriebsspannungen im Vergleich zur APD mit Feldlinienverdichtung erzielt. Darüber hinaus schlägt meine Forschung eine n^+/p-Wanne Multi-Dot-Struktur vor, bestehend aus einem Array einzelner Punkte mit einer gemeinsamen Anode. Dieses innovative Design ermöglicht die Erweiterung des aktiven Bereichs unter Beibehaltung der Leistung und positioniert die n^+/p-Wanne Multi-Dot-APD als vielversprechende Lösung für Anwendungen, die einen größeren lichtempfindlichen Bereich erfordern. Darüber hinaus ermöglicht die Nutzung des Vorteils der Entkopplung des P/N-Übergangsbereichs vom lichtempfindlichen Bereich in solchen Strukturen den Entwurf einer Fotodiode mit großem lichtempfindliche Bereich und einer relativ kleinen Kapazität.

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Vienna, Austria, February 2024 Saman Kohneh Poushi

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Dedication

To my beloved wife, Golan, whose patience and support have eased the challenges along my journey, and to my dear daughter, Solin, the shining light of my life.

To my parents, Latif and Nasrin, who are the source of my strength.

Contents

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Acronyms

υ Drift velocity. 3

μ Mobility of carrier. 3

$\alpha(\lambda)$ Wavelength-dependent optical absorption coefficient. 2

K_B Boltzmann constant. 3

APD Avalanche photodiode. 4

APP Afterpulsing probability. 5

ARC Anti-reflection coating. 24

ATP Avalanche-triggering probability. 12

CMOS Complementary metal-oxide-semiconductor. 8

DCR Dark count rate. 5

Dn Diffusion constant for electrons. 3

Dp Diffusion constant for holes. 3

E Electric field. 3

EFLC-APD Electric field-line crowding APD. 28

hv Photon energy. 2

Le Diffusion length for electrons. 10

Lh Diffusion length for holes. 10

MD-PIN Multi-dot PIN. 29

MD-APD Multi-dot APD. 29

PDK Process design kit. 11

PDP Photon detection probability. 5

PIN Photodiode with an intrinsic region in between the n- and p-doped regions. 29

SiPM Silicon photomultiplier. 27

SPAD Single-photon avalanche diodes. 4

T Absolute temperature. 3

TCAD Technology computer-aided design. 11

Chapter 1

Introduction

Avalanche photodiodes are critical components in numerous optical systems, providing enhanced sensitivity to detect low-level optical signals. These photodiodes use the avalanche multiplication effect, allowing for signal amplification, heightened sensitivity, and improved signal-to-noise ratios, thereby enabling the detection of weak optical signals across a range of applications. The widespread application of avalanche photodiodes spans various fields, including optical communications, light detection and ranging systems, biomedical imaging, spectroscopy, and beyond [1–11]. In each domain, the demand for higher performance, increased sensitivity, lower noise, and better efficiency necessitates continual advancements in avalanche photodiode technology.

Avalanche photodiode operation can be thought of as a simple diode with a reverse bias, designed to detect incoming photons and convert their energy into an electrical signal. This detection process involves two primary stages: Firstly, photon absorption, which leads to the generation of electron-hole pairs. Subsequently, the photo-generated carriers are transported within the diode, which induces a flow of current. The resulting photocurrent can then be detected using an external circuit.

1.1 Optical absorption and photogeneration

Photon absorption in semiconductors is a fundamental process where incident photons transfer their energy to the semiconductor material. This interaction causes the excitation of electrons from the valence band to the conduction band, generating electron-hole pairs. The energy of the absorbed photon must match or exceed the bandgap energy of the semiconductor for this process to occur efficiently. The bandgap energy of silicon is about 1.12 eV, implying that solely photons with an energy level higher than 1.12 eV are capable of being absorbed within silicon.

The transmitted optical power (P) decays exponentially as it traverses through an absorbing medium. This decay can be expressed by the following equation based on Lambert Beer's law [12]:

$$P(\lambda, x) = P_0(\lambda)e^{-\alpha(\lambda)x}, \tag{1.1}$$

which, P_0 denotes the optical power at the surface of silicon (x=0). $\alpha(\lambda)$ represents the wavelength-dependent optical absorption coefficient, where λ signifies the wavelength of the light. Here, x represents the depth within the silicon material, considering the incident light to be perpendicular to the surface. Table 1.1 outlines the optical absorption coefficient of silicon and the corresponding 1/e penetration depth across some key wavelengths [13, 14].

Table 1.1: Optical absorption coefficient of silicon and the corresponding 1/e penetration depth for some key wavelengths[13].

Wavelength (nm)	α (μm^{-1})	1/e penetration depth (μm)
850	0.06	16.67
780	0.12	8.33
680	0.24	4.16
635	0.38	2.63
565	0.73	1.37
465	03.6	0.278

The expression for the photogeneration rate per volume (G) concerning the depth (x) in silicon is derived as follows [12]:

$$G(x) = \frac{P(x) - P(x + \Delta x)}{\Delta x} \frac{1}{Ah\upsilon}, \tag{1.2}$$

where P(x) is optical power, A denotes the cross-sectional area for light incidence, and hv is the photon energy of the incident photons. When Δx approaches zero, the expression $G(x) = -\frac{dP(x)}{dx}\frac{1}{Ah\upsilon}$ is obtained. Upon differentiating equation 1.1, the photogeneration results [12]:

$$G(x) = \frac{\alpha P_0}{Ah\upsilon} e^{-\alpha x}. \tag{1.3}$$

To accurately obtain the photocurrent in photodetectors, it is necessary to incorporate photogeneration into the semiconductor equations [12, 15]. These equations encompass the Poisson equation, transport equations, and continuity equations, collectively defining the behavior of semiconductors. Various device simulators such as ATLAS [16], MEDICI [17], or SENTAURUS [18] specialize in solving these semiconductor equations to model the intricate characteristics of semiconductor devices, accounting for photogeneration and providing comprehensive insights into device performance.

1.2 Carrier transport

Carrier transport in semiconductor photodetectors involves a combination of mechanisms such as drift and diffusion. In drift transport, carriers experience acceleration due to the electric field and move with an average velocity known as drift velocity. This velocity (υ) is determined by the carrier mobility (μ) within the semiconductor material and the strength of the applied electric field (E), as represented by the following equation [12]:

$$\upsilon = \mu E. \tag{1.4}$$

In the context of silicon, the drift velocities of both electrons and holes reach saturation at approximately 10^7 cm/s under high electric field conditions. Additionally, carrier mobilities are significantly influenced by impurity concentrations, particularly doping levels within the semiconductor material. Higher doping concentrations tend to lower carrier mobilities, a critical factor to consider in photodetector development [19]. These factors, including carrier mobilities, generation/recombination rates, and other related quantities, are critical to be considered in the design and optimization of photodetectors. Device simulators offer various models to characterize carrier mobilities and other essential parameters [15–18]. Selecting appropriate models within these simulators is crucial for accurately predicting and analyzing the behavior of carriers within semiconductor photodetectors, aiding in device performance enhancement and design refinement.

The diffusion of minority carriers significantly influences the response speed of photodetectors. Carrier diffusion occurs in semiconductor regions lacking an electric field, characterized by the movement of carriers due to concentration gradients. The carrier diffusion coefficients, Dn and Dp, representing the diffusion of electrons and holes, respectively, are linked to carrier mobilities through the Einstein relation [12]:

$$D_{n/p} = \mu_{n/p}\frac{K_B T}{q} \tag{1.5}$$

Here, K_B represents the Boltzmann constant, T denotes the absolute temperature, and q signifies the elementary charge. Consequently, carrier diffusion tends to be notably slower compared to carrier drift due to the relatively low value of the thermal voltage (approximately 26 mV) around room temperature. In contrast, the electric field strength at P/N junctions and within the space-charge region (depleted region) of photodiodes typically reaches several thousand V.cm^{-1}

As a result, when light generates carriers solely within the depleted drift regions, photodiodes exhibit high bandwidth and show short rise/fall times in the photocurrent. However, if carriers are also photo-generated below the depleted space-charge region, especially in the substrate and highly doped regions, the photocurrent exhibits a slow diffusion tail [19]. Understanding and controlling carrier

diffusion is crucial for optimizing the response characteristics and speed of photodetectors in various applications.

1.3 Operation mode

In order to provide a wide depletion region, photodiodes are operating in a reverse bias voltage. By widening the space-charge region more incident photons have the opportunity to be absorbed within this zone. Therefore, incident photons generate electron-hole pairs within the depletion region of the photodiode, creating a photocurrent proportional to incident light intensity.

As the reverse bias voltage increases, the electric field at the p/n junction becomes stronger and accordingly, the generated electrons and holes under the large electric field may contribute to the generation of more electrons and holes within the device by the process of impact ionization. Impact ionization is a process that occurs when an electron, accelerated by a strong electric field, gains enough kinetic energy to collide with a bound electron within the crystal lattice, causing the bound electron to break free and create an electron-hole pair. This process leads to an avalanche multiplication of carriers, where one carrier collision generates multiple additional carriers. Photodiodes operating within the avalanche region are termed avalanche photodiodes. When avalanche photodiodes exhibit moderate and linear avalanche amplification upon incident photons, usually below 1000x, are called (APD) and provide increased sensitivity compared to the photodiodes biased in the unamplified mode.

By increasing the reverse bias to above the breakdown voltage, known as Geiger mode, the impact ionization caused by a single photon leads to a self-sustaining avalanche effect, which produces a large number of electron-hole pairs. This avalanche process results in a detectable electrical pulse for each detected single photon. The photodiodes operating in Geiger mode are called single-photon avalanche diodes (SPAD). Figure 1.1 shows these three different operating regions.

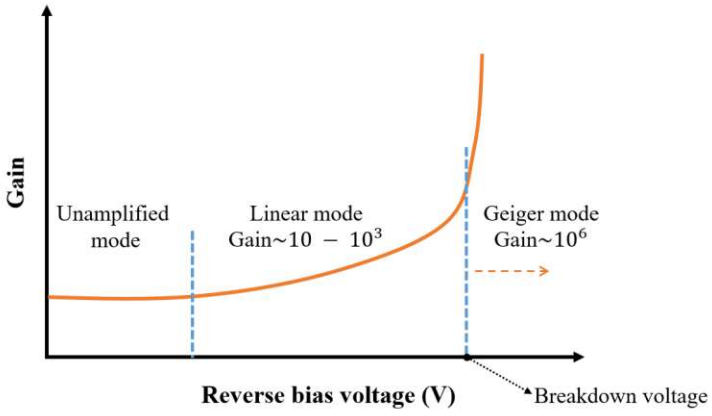

Figure 1.1: Operation regimes of photodiodes.

It's important to note that SPADs function as binary or "digital" devices. Consequently, the resulting current doesn't precisely correlate with the number of incident photons that initiated the diode's reaction; rather, it signifies the occurrence of an avalanche event. This current persists until the voltage across the SPAD decreases below or approaches the breakdown voltage. The primary distinction between SPADs and APDs lies in their operational characteristics. An APD typically operates near the breakdown voltage, albeit slightly below it. However, such operating voltage provides a high electric field to achieve an internal multiplication gain of a few hundred. Consequently, the resulting avalanche current in APDs is linearly proportional to the intensity of an optical signal.

1.4 Key performance parameters of SPAD and APD

Here, some key performance features of SPAD and APD are introduced. Understanding and optimizing these parameters is very important to adjust the performance of the photodetector for specific applications.

1.4.1 SPAD

Photon detection probability (PDP): PDP measures the SPAD's effectiveness in converting incident photons into electrical signals. It is calculated as the ratio of detected photons to the total number of incident photons. Higher PDP values indicate better photon detection capability.

Dark count rate (DCR): DCR represents the rate at which false detection events occur in the absence of incident photons. These events, known as dark counts, are caused by thermal or intrinsic noise within the SPAD. Lower DCR values are desired to minimize false detections and improve the signal-to-noise ratio of the device.

Afterpulsing probability (APP): APP refers to secondary avalanches triggered by previously detected photon events. Afterpulsing probability measures the likelihood of these subsequent avalanches occurring. Reducing afterpulsing is critical for accurate photon counting and minimizing false detection events.

Fill factor: Fill factor represents the ratio of the active sensitive area of the SPAD to its total area. Higher fill factors increase the device's photon collection efficiency by maximizing the active area available for photon detection.

Recovery Time: Recovery time denotes the duration required by the SPAD to return to its operational state after a photon detection event. Shorter recovery times enable faster response rates, allowing the SPAD to handle higher count rates.

Avalanche build-up time: The avalanche build-up time refers to the time it takes for the avalanche

multiplication process to reach its maximum amplification level after the detection of a single photon. It is a critical parameter because it influences the time resolution of the SPAD. A shorter avalanche build-up time allows the SPAD to respond more quickly to incoming photons, enabling high-speed detection of individual photons and improving the time resolution of the system.

1.4.2 APD

Gain: APDs exhibit internal gain, which is the result of the avalanche effect, where a single photon triggers a cascade of electron-hole pairs. This multiplication of carriers enhances the sensitivity of the device, amplifying the electrical signal output compared to a standard photodiode.

Responsivity: Responsivity measures the device's ability to convert incident optical power into an electrical output signal. Higher responsivity indicates better efficiency in converting photons into measurable electrical signals, contributing to increased photo-sensitivity.

Bandwidth: APDs have specific bandwidth limitations because of avalanche build-up time that defines their operational speed and frequency response. Higher bandwidth allows APDs to effectively respond to rapid changes in incident light intensity, making them suitable for high-speed applications like optical communication.

Internal noise: Internal noise in APDs comprises several components, including excess noise due to the avalanche process and thermal generation originating from the semiconductor material. Minimizing internal noise is essential to maintain a high signal-to-noise ratio, ensuring accurate detection of weak optical signals.

Capacitance: The capacitance of an APD is an important performance parameter that influences the device's high-frequency response and speed of operation. Lower capacitance values are desirable for high-speed applications as they allow for faster response times and higher bandwidth, enabling the APD to detect rapid changes in incident light intensity or high-frequency optical signals.

1.5 Scope and cohesion of this thesis

This thesis focuses on the improvement of the PDP of SPADs and the scalability (i.e. fill factor) enhancement of SPAD and APD structures without compromising other essential performance parameters. For this purpose, a physics-based modeling and simulation approach is introduced to characterize the PDP, enabling the prediction and analysis of SPAD performance under varying conditions (see Section 1.6). The model integrates both optical and electrical simulations to capture the intricate dependencies of PDP on factors such as wavelength, excess bias, and incident light angle.

The focus of this modeling effort is on commonly used planar n^+/p-well CMOS SPAD structures.

In the TCAD simulation, the structure is defined based on the SPAD layout, including information from the process design kit (PDK) and doping profiles provided by the foundry. However, for an accurate definition of the structure in the simulation environment, the lateral folding of the doping profiles requires calibration. The lateral folding of the doping profiles in planar n^+/p-well or p^+/n-well structure-based cylindrical diodes influences the radius of the active region. This parameter can be calibrated by comparing the simulation-derived lateral PDP results with the measured results. In dot structures, this parameter affects the breakdown voltage of the diode, which is adjusted by comparing the breakdown voltage obtained from the simulation with the measurement results. To ensure the simulation considers all physical effects, proper models for impact ionization, generation-recombination, and carrier mobility are carefully selected. The breakdown voltage of the diodes is significantly influenced by the impact ionization parameters, for which various models exist [20–25]. Through a thorough literature review and a comparative analysis of breakdown voltages obtained from simulations and measurements, the Selberherr's impact ionization model has been chosen for implementation in this study. However, it is important to note that there is flexibility in adjusting the model's parameters to achieve an optimal alignment with the measured breakdown voltage. Table1.2 provides the precise parameters of Selberherr's impact ionization model utilized in this thesis.

The optical simulation encloses defining the attributes of the light source, establishing boundary conditions, and incorporating known optical and structural properties of the device, including the refractive indexes of silicon, oxide, and air. Furthermore, it necessitates the calibration of optical properties specific to the isolation and passivation layers. This calibration is vital for achieving accurate results in optical simulations, given the absence of crucial technology information, such as the exact isolation thickness.

Utilizing the presented model, the dependence of the PDP on the distribution of the electric field inside the structure is studied (see Section 1.7). This investigation involves comparing PDP characterizations of two distinct reach-through SPADs with different doping profiles. Understanding the impact of electric field distribution on PDP performance is crucial for optimizing photodetection in the design of various SPAD structures. Furthermore, the model is employed to examine how the application of an anti-reflection coating over the photosensitive area can enhance the PDP in CMOS-SPADs (see Section 2.1). Consequently, the optimal ARC layer thickness that corresponds to maximal PDP enhancement across different wavelengths in the visible spectrum is extracted. This insight aids in ARC selection when various thickness options are available within the CMOS process.

The widely adopted planar n^+/p-well or p^+/n-well structure-based CMOS-integrated avalanche photodiodes (SPAD and APD) typically demonstrate low fill factors attributed to limited peripheral charge collection and the use of physical guard rings to prevent premature edge breakdown. In this

study, I explore the substitution of physical guard rings with virtual guard rings to comparatively improve the fill factor within these structures (see Section 2.2). This design approach proves more effective in miniaturized SPADs where guard ring dimensions closely match those of the photo-sensitive area. In addition to the low fill factor and limited scalability inherent in these structures, they typically exhibit a trade-off between bandwidth and responsivity. This trade-off is particularly notable in the long-wavelength range when they operate in the linear mode (APD operation mode).

To overcome these limitations, I introduce a novel CMOS-APD design based on the field-line crowding concept. This design not only offers comparable but potentially enhanced performance parameters compared to conventional design approaches for CMOS-integrated avalanche photodiodes (see Section 2.3). The new APD is fabricated using a standard CMOS process without requiring modifications, and its performance is thoroughly examined. Additionally, I provide further characterization in the near-infrared range and explore the effects of design parameters on its overall performance (see Section 2.4).

Furthermore, my research introduces a novel n^+/p-well multi-dot structure, featuring an array of individual dots with a shared anode (see Section 2.5) with lower breakdown voltage. This innovative design allows for the expansion of the active area while maintaining performance, making the multi-dot APD a promising solution for applications requiring a larger light-sensitive area. Moreover, by taking advantage of decoupling the P/N junction area from the light-sensitive region in such structures, it becomes possible to design a PIN-photodiode with a significantly increased light-sensitive area and a relatively small capacitance (see Section 2.6) with a lower operating voltage.

1.6 PDP modeling in CMOS-SPADs

Modeling photon detection probability in CMOS-SPAD is of great importance for the development and optimization of SPADs while avoiding time-consuming experimental investigations. By modeling PDP, designers can predict and analyze SPAD performance across varying conditions, offering insights into how alterations in bias voltages, wavelengths, or incident light angle impact photon detection efficiency. In addition, Understanding the limitations through PDP modeling leads to targeted improvements, thereby enhancing performance.

Recently, some physics-based modeling and simulation approaches were introduced to characterize the PDP by parameterizing the probability of avalanche triggering within silicon [26–31]. Given that the probability of avalanche triggering significantly relies on the depth of electron-hole generation within the silicon, an accurate determination of the photon absorption profile is crucial. Because when the device is illuminated, the photons on the way to reach the silicon must pass through the layer

covering it. Consequently, this layer influences the propagation of light within the structure. This effect becomes especially important in cases where an anti-reflection coating layer is absent, and an isolation and passivation stack covers the sensitive area, a common occurrence in numerous CMOS process technologies. It should be mentioned that the aforementioned models overlook this effect. In addition, due to the formation of a standing wave in the layers above the silicon, the optical transmission into the silicon and the resulting PDP spectrum of the SPAD exhibit considerable dependencies on both the incident light's wavelength and its angular deviation from the surface normal.

I expand upon the methodology introduced in [27–30] and adapt it to a standard CMOS process, aiming to develop a comprehensive PDP model [32, 33]. This enhanced model integrates optical and electrical simulations to capture the intricate dependencies of PDP concerning wavelength, excess bias, and incident light angle. To validate the effectiveness of the model, the spectral and excess bias dependencies of the PDP for a specific SPAD featuring an n^+/p-well structure (Figure. 1.2) are calculated, and subsequently, the results are compared with experimental measurements.

1.6.1 SPAD structure

Figure 1.2 depicts the cross-sectional view of the SPAD structure fabricated in a 0.35 μm OPTO-ASIC CMOS process. This structure comprises a thick low-doped absorption region (p- epi) with a multiplication zone established at the n^+/p-well junction.

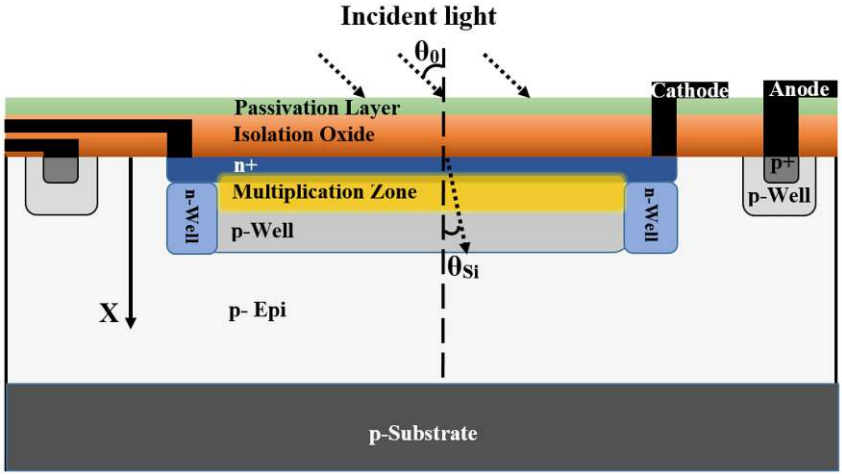

Figure 1.2: Schematic cross section of the n^+/p-well CMOS SPAD (not to scale). Here, θ_0 denotes the angular deviation of the incident light from the surface normal and x indicates the depth inside the silicon. © 2021 IEEE. Reprinted, with permission, from [33].

In this particular technology, the absence of an anti-reflection coating layer results in the active area being covered by thick inter-metal level oxide and passivation stacks. When the device is exposed to light, photons traverse through the isolation and passivation stacks before reaching the silicon surface.

The refractive index difference of these layers causes partial reflection of photons at each interface. Consequently, the interference between transmitted and reflected waves traveling in opposite directions leads to the formation of standing waves in both the isolation and passivation stacks.

Moreover, when the device operates beyond the breakdown voltage (i.e., when an excess bias is applied), the entire absorption region becomes depleted, and a strong electric field is formed over the multiplication zone. This notably increases the extent of the drift region, wherein photons should be absorbed [34]. To prevent premature edge breakdown, the p-well is deliberately made smaller than the n^+ region. Additionally, an n-well is introduced at the edge of the n^+ region.

1.6.2 Modeling approach

The experimental determination of PDP involves calculating the ratio of detected photons to the total number of incident photons, measured with a (calibrated) reference detector. It's evident that a fraction of incident photons gets reflected before reaching the silicon, and only a portion of the transmitted photons is absorbed, subsequently generating electron-hole pairs in an area that could lead to an avalanche event. Moreover, not every transmitted photon leading to electron-hole pair generation occurs within a region where the carriers can trigger a self-sustaining avalanche. In fact, the avalanche triggering probability (P_{av}), signifying the likelihood of a photo-generated electron-hole pair initiating an avalanche, is a function of the absorption depth (x) (i.e., the electric field) and the diffusion lengths of carriers (Le, Lh).

Thus, along the one-dimensional axis of x (i.e., at the device center and spanning the region encompassed by the multiplication areas where the electric field is vertical), the estimation of PDP relies on two distinct and independent factors: the photon absorption probability (P_{ab}) and the avalanche triggering probability (P_{av}). Accordingly, the PDP is expressed as [27]:

$$\mathrm{PDP}(\lambda, \theta_0, V_{\mathrm{ex}}) = \int_0^{x_{\mathrm{sub}}} P_{\mathrm{ab}}(\lambda, \theta_0, x) \times P_{\mathrm{av}}(V_{\mathrm{ex}}, x) dx, \tag{1.6}$$

Here, x_{sub} represents the deepest point within the silicon substrate, typically within the range of a few hundred micrometers (in my simulations, it's set at 350 μm). Both P_{ab} and P_{av} exhibit a strong dependence on the variable x. Furthermore, $P_{\mathrm{ab}}(\lambda, \theta_0, x)$ depends on the wavelength (λ) and the angular deviation of the incident light from the surface normal (θ_0). On the other hand, $P_{\mathrm{av}}(V_{\mathrm{ex}}, x)$ is dependent on the excess bias voltage (V_{ex}), defined as the discrepancy between the applied reverse bias and the breakdown voltage.

Given the structural symmetry depicted in Figure 1.2 and considering that the device diameter is 80 μm, which is approximately two orders of magnitude larger than the wavelengths of light, both P_{ab}

and P_{av} display dependencies on x but exhibit negligible variations in other directions. As a result, accurately determining these two probabilities (as a function of x) simplifies the calculation of PDP to a one-dimensional numerical integration issue.

Figure 1.3 illustrates the flow chart of the proposed methodology for modeling the PDP. This approach involves the extraction of $P_{\text{av}}(V_{\text{ex}}, x)$ and $P_{\text{ab}}(\lambda, \theta_0, x)$ from TCAD and optical simulations, respectively, for subsequent utilization in Eq. 1.6. Within the TCAD simulation, the structure is defined based on the layout of the SPAD, incorporating information from the process design kit (PDK) and the doping profiles provided by the foundry. To ensure a comprehensive simulation considering all physical effects, suitable models for impact ionization, generation-recombination, and carrier mobility must be carefully selected. Additionally, calibration of the impact ionization parameters is imperative to achieve an accurate alignment with the measured data.

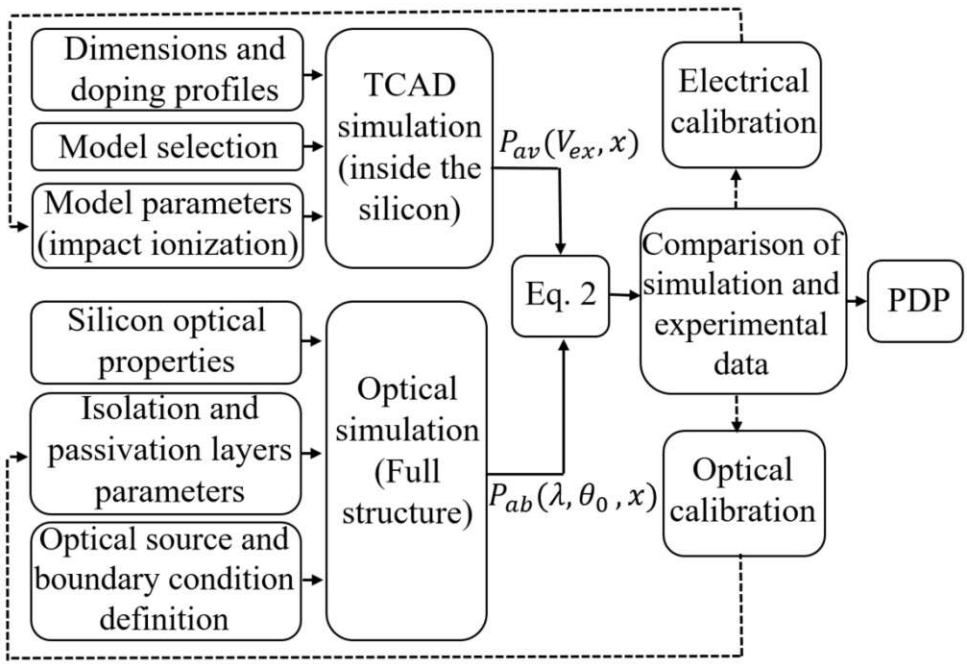

Figure 1.3: Flow chart of the PDP modeling procedure. © 2021 IEEE. Reprinted, with permission, from [33].

The optical simulation involves defining the characteristics of the light source, setting up boundary conditions, and integrating known optical and structural properties of the device—such as the refractive indexes of silicon, oxide, and air. Additionally, it requires calibration of the optical properties specific to the isolation and passivation layers. This calibration becomes crucial to attain precise results in optical simulations, due to the lack of important technology information, such as exact isolation thickness values or refractive index details concerning the isolation and passivation layers.

Optical simulations

To derive $P_{\mathrm{ab}}(\lambda, \theta_0, x)$, I propose conducting electromagnetic simulations to achieve precise calculations of photon transmission and absorption profiles, which are critical for accurate assessments. By treating light as a wave, its transmission properties can be evaluated at any wavelength to calculate the amount of light intensity penetrating the silicon. This quantity, when divided by the total incident light intensity, signifies the fraction of light penetrating the silicon and, when light is viewed as photons, represents the probability of photon transmission into the silicon. Similarly, computing the absorption profile of light within the silicon through electromagnetic simulations facilitates the derivation of the probability distribution for photon absorption as a function of x. This method allows us to establish the likelihood of photons being absorbed at various depths within the silicon.

Here, as the diameter of the active area is large enough compared to the wavelength, one can consider the light as a plane wave propagating along the x axis and having a uniform amplitude on any plane parallel to the active area (i.e. the silicon interface). This is a simplifying assumption to estimate $P_{\mathrm{ab}}(\lambda, \theta_0, x)$ as the photon absorption probability distribution multiplied by the probability that a photon is transmitted into the silicon at any λ and θ_0.

As previously outlined, the modeling approach presented includes the calibration of optical properties related to the isolation and passivation layers. These calibrated parameters act as degrees of freedom, offering a certain level of compensation for additional assumptions regarding the precise properties of the light source. This calibration mechanism enables achieving an agreement between the model and experimental data. For instance, even if the optical simulation incorporates the effect of a non-zero beam angle of the light source, adjusting the properties of the isolation and passivation layers allows for a good agreement between the model and experimental outcomes.

TCAD simulations

If a photon is absorbed within the depletion region, the resulting electron and hole swiftly separate, each carrier moving in opposite directions due to the electric field. The minority carrier, accelerated by the electric field, moves toward the multiplication region. However, if the photon is absorbed in a neutral region, the generated carriers might initiate an avalanche solely if they diffuse into the depletion region. Notably, not all carriers can diffuse into the depletion zone, necessitating consideration of the recombination probability to determine the comprehensive avalanche-triggering probability (ATP). Consequently, contingent upon the absorption depth (x), an avalanche may be triggered by either a generated electron or a hole. To determine the total ATP, it's treated as the sum of the probabilities that an electron or a hole singularly triggers an avalanche event—viewed as two independent occurrences.

Therefore, P_{av} signifies the probability of an inclusive event and is expressed by [27]:

$$P_{\text{av}}(V_{\text{ex}}, x) = [P_{\text{e}}(V_{\text{ex}}, x) + P_{\text{h}}(V_{\text{ex}}, x) - P_{\text{e}}(V_{\text{ex}}, x) \times P_{\text{h}}(V_{\text{ex}}, x)] \times P_{\text{diff}}(x). \tag{1.7}$$

In this context, $P_{\text{diff}}(x)$ signifies the probability of a photo-generated minority carrier diffusing into the depletion region from the neutral zone. When x resides in the depletion region, this term equates to 1. However, when x is within the neutral regions, $P_{\text{diff}}(x)$ is determined using the following equation. It's noteworthy that contrary to the conventional definition, which solely defines avalanche probability within the multiplication region and disregards it elsewhere, the total avalanche probability (P_{av}) here represents an effective value. It accounts for the avalanche probabilities of both the diffused and drifted carriers generated outside the multiplication region [27].

$$P_{\text{diff}}(x) = \begin{cases} e^{-(\frac{w_1 - x}{L_{\text{h}}})} & \text{neutral n-type (above),} \\ e^{-(\frac{x - w_2}{L_{\text{e}}})} & \text{neutral p-type (below),} \end{cases} \tag{1.8}$$

where, L_{h} (L_{e}) denotes the diffusion length attributed to holes (electrons), while w_1 (w_2) denotes the top (bottom) boundary from the neutral regions to the depletion zone.

Now, at a specific excess bias voltage, $P_{\text{e}}(V_{\text{ex}}, x)$ and $P_{\text{h}}(V_{\text{ex}}, x)$ are acquired by solving a coupled set of two equations, as outlined in McIntyre's work [35]. These equations are expressed as follows [27]:

$$\begin{aligned} \frac{\partial P_{\text{e}}}{\partial x} &= (1 - P_{\text{e}})\gamma_{\text{e}}(P_{\text{e}} + P_{\text{h}} - P_{\text{e}}P_{\text{h}}), \\ \frac{\partial P_{\text{h}}}{\partial x} &= (1 - P_{\text{h}})\gamma_{\text{h}}(P_{\text{e}} + P_{\text{h}} - P_{\text{e}}P_{\text{h}}). \end{aligned} \tag{1.9}$$

Here, γ_{e} and γ_{h} represent the electron and hole impact ionization coefficients, respectively. These parameters substantiate the considerable influence of avalanche probabilities concerning excess bias and are determined through TCAD simulations.

1.6.3 Results and discussion

Optical considerations

Figure 1.4 illustrates the measured PDP spectrum and the simulated transmission for the aforementioned SPAD structure. The fluctuations observed in the PDP spectrum across different wavelengths stem from the formation of standing waves within the isolation and passivation layers situated above the silicon. Remarkably, this particular phenomenon, to the best of my knowledge, has been overlooked in prior PDP modeling endeavors [27–30]. I firmly believe that this effect necessitates careful consider-

ation, especially in SPAD devices integrated into standard CMOS technologies, where the availability of an anti-reflection coating is typically absent.

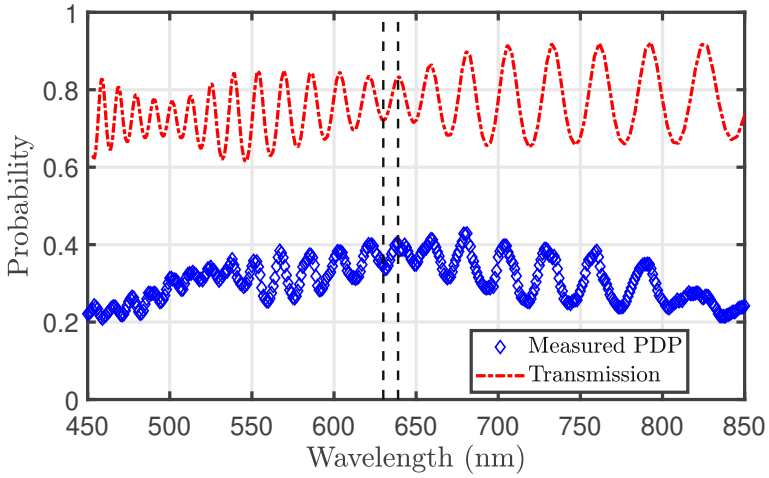

Figure 1.4: The optical transmission into the silicon (simulated at $\theta_0 = 0$) and the measured PDP spectrum (at $\theta_0 = 0$ and $V_{\text{ex}} = 6.6\ V$). © 2021 IEEE. Reprinted, with permission, from [33].

Upon closer examination of the measured spectrum, a noticeable envelope accompanies the primary, more rapid oscillations concerning λ. This envelope might be interpreted as the existence of two standing waves formed within the isolation (i.e., intermediary) and passivation layers. Specifically, the swifter fluctuation aligns with the standing wave within the thicker isolation layer, while the enveloping pattern corresponds to the standing wave occurring in the passivation layer, possessing an optical thickness of approximately one-tenth that of the isolation layer. The thicker layer causes a greater multitude of nodes and antinodes (i.e., $\lambda/2$ divisions) within a standing wave. Consequently, any alteration in λ accumulates across these fractions, yielding a higher rate of fluctuation in the spectrum. Consequently, when a layer's thickness diminishes significantly, its associated fluctuations are observed as an envelope encompassing the swifter fluctuations.

For a deeper comprehension of this phenomenon and to enhance the precision of PDP modeling outcomes, an electromagnetic simulation was conducted utilizing the CST Microwave Studio simulation tool [36]. Figure.1.4 shows the optical transmission as a function of λ for the SPAD structure (depicted in Figure.1.2). These findings validate that the oscillations witnessed in the PDP spectrum are a consequence of λ-dependent photon reflection/transmission behaviors. It underscores the necessity to account for this effect to ensure an accurate calculation of the photon absorption probability.

As previously discussed, an accurate depiction of photon transmission and the absorption profile within the silicon enables the derivation of P_{ab}. Conventionally, the photon absorption profile is estimated using a simple formula $\alpha \cdot \exp(-\alpha x)$, where α signifies the absorption coefficient and varies with λ. However, a more precise determination of the photon absorption profile involves a normalized

light intensity extracted from electromagnetic simulations, showcased in Figure. 1.5. This approach provides a more reliable and detailed assessment of the photon absorption profile within the material.

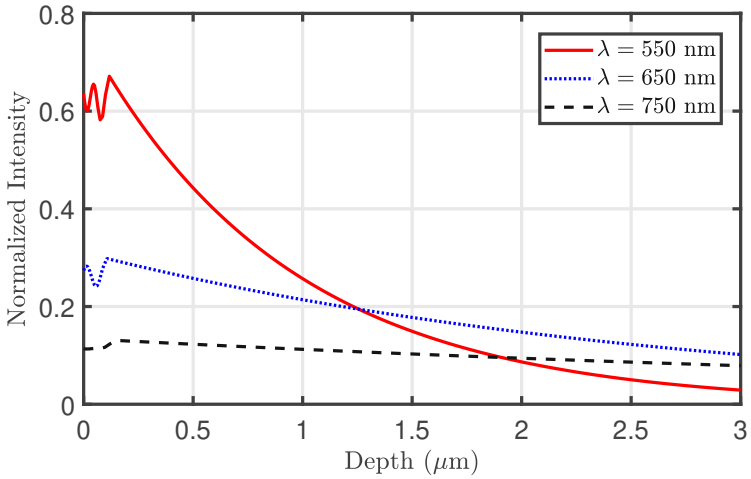

Figure 1.5: Normalized light intensity as a function of depth x for three different values of λ at $\theta_0 = 0$.

It's worth noting the deviation of the profile from an expected exponential decay typical for silicon absorption profiles [28–30]. The observed interference just below the silicon surface (near $x = 0$) might be attributed to the penetration of the standing wave, originating in the isolation layer, into the silicon substrate. The absorption profile within the silicon doesn't fit to a typical exponential decay starting precisely at the surface ($x = 0$). This discrepancy arises due to the dissimilarity between the boundary condition at the silicon surface and the interface of two materials infinitely extended from the other side. Consequently, the interference generated by waves reflecting back and forth in the isolation layer infiltrates the silicon, leading to an altered absorption profile. The exponential decay characteristic is shifted away from the silicon surface by approximately 200 nm due to this effect.

To ensure an accurate computation of the PDP, it's crucial to consider this interference effect, particularly in CMOS-based SPADs where the multiplication zone resides very near the surface. Moreover, with shorter wavelengths, a substantial proportion of incident photons are absorbed in proximity to the silicon surface. For instance, within the wavelength range of approximately 400 nm to 500 nm, nearly half of the transmitted photons are absorbed within the depth range of $x = 0$ to 200 nm. This emphasizes the significance of accounting for these proximity effects, especially when evaluating PDP characteristics in such devices.

1.6.4 Electrical considerations

To acquire the ATP necessary for Eq. 1.6, TCAD simulations are imperative. Precisely, determining the impact ionization coefficients (Eq. 1.9) as a function of x and computing the two-dimensional electric field (to derive $E(x)$ for various incidence angles) requires TCAD simulations. These simulations aid in estimating the probabilities of electron and hole avalanche triggering, crucial for implementing Eq. 1.7. Table1.2 displays the essential parameters and their corresponding values employed in these simulations.

Table 1.2: Summary of the parameters used in the TCAD simulation performed by ATLAS and the extracted boundaries of the depleted zone to be use in Eq. 1.7 at an excess bias voltage of 6.6 V [33].

Parameter	Description	Value
a_n	Impact ionization constant for electron [37]	$7.03 \times 10^5 cm^{-1}$
En_{crit}		$1.231 \times 10^6 V.cm^{-1}$
a_p	Impact ionization constants for hole [37]	$1.58 \times 10^6 cm^{-1}$
Ep_{crit}		$2.036 \times 10^6 V.cm^{-1}$
V_{br}	Breakdown voltage	25 V
τ_n	Electron lifetime	200 μ s
τ_p	Hole lifetime	200 μ s
L_e	Electron diffusion length	270 μ m
L_h	Hole diffusion length	90 μ m
W_1	Top boundary of depleted region	220 nm
W_2	Bottom boundary of depleted region	12.5 μ m

Figure 1.6a illustrates a two-dimensional representation of the electric field at an excess bias voltage of 6.6 V, simulated using the Geiger-mode device simulation feature of SILVACO Atlas [16]. The plot showcases the boundaries of the depleted region, specifying the neutral regions from the depletion zone. The dimensions of the depleted region exhibit a strong dependence on the applied reverse bias. This effect becomes more pronounced at voltages lower than the breakdown, where the device isn't fully depleted. However, when reverse biases surpass a certain threshold, the device transitions into full depletion. Consequently, any further increase in reverse bias yields a minor effect on w_1 and w_2, within the range of nanometers.

Figure 1.6b exhibits the electron, hole, and effective (total) ATP distributions as a function of x for various excess bias voltages. Despite the avalanche process primarily occurring within the multiplication region, carriers generated outside this area possess the capability to reach the multiplication zone,

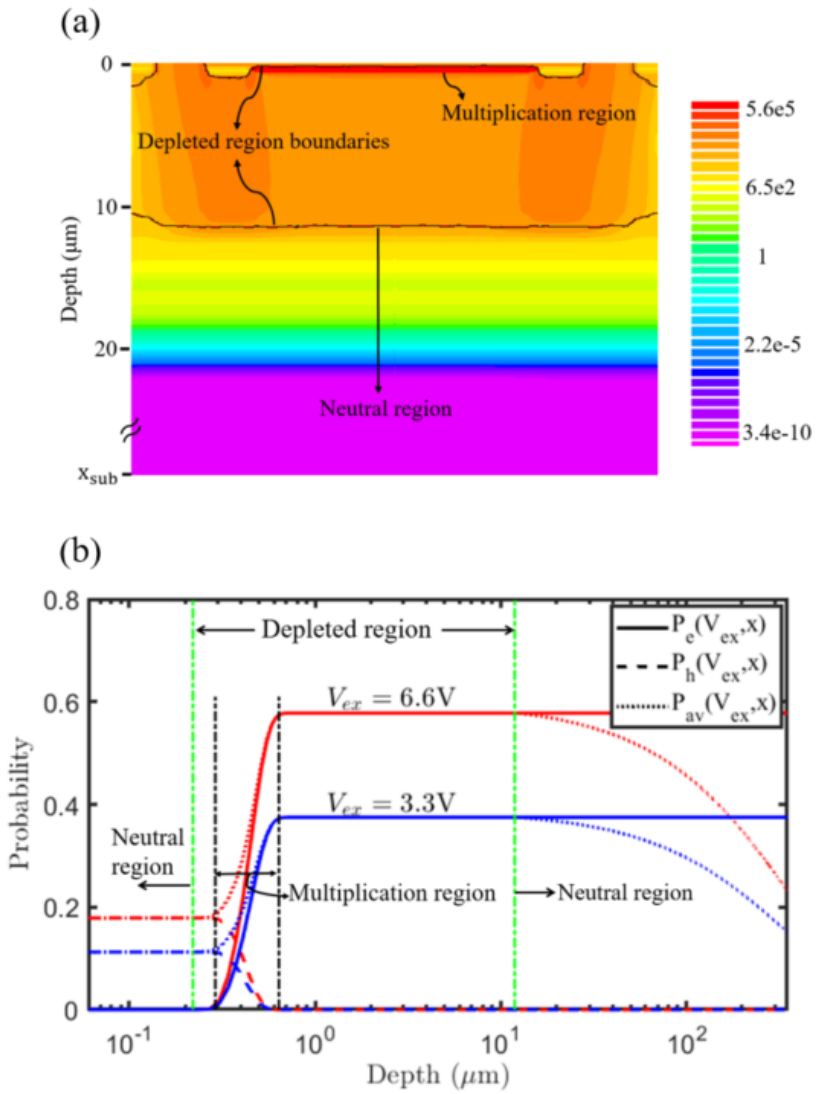

Figure 1.6: (a) Simulated 2D electric field and the depletion region boundaries of the n^+/p-well CMOS SPAD at V_{ex}= 6.6 V in logarithmic scale. (b) Electron and hole ATP distributions for excess biases of 3.3 V and 6.6 V at $\theta_0 = 0$. © 2021 IEEE. Reprinted, with permission, from [33].

potentially leading to an avalanche event. Consequently, within the depletion region and below the multiplication zone, $P_{\text{av}}(x)$ equates to $P_{\text{e}}(x)$ and maintains a constant value. This consistency arises from the fact that any electron generated within this region will traverse the entire multiplication zone to reach the cathode via n^+. Moreover, the impact of recombination within this area remains negligible due to the forceful drift of carriers in opposite directions for electrons and holes. Conversely, when an electron originates above the multiplication region, it moves towards the cathode without passing through the multiplication zone. As a result, P_{e} is equal to zero in proximity to the silicon surface.

It's evident that for electrons generated within the multiplication region, P_{e} rises from zero to reach a maximum value with increasing x. Conversely, a converse trend applies to the holes, as they move toward the anode. Due to the holes' impact ionization coefficient being smaller compared to that of

electrons, the maximum value of P_{h} is correspondingly smaller than the maximum P_{e}. It is anticipated that increasing the excess bias intensifies the electric field across the multiplication region. Consequently, both electron and hole impact ionization rates (γ_{e} and γ_{h}) increase. This increment results in amplified avalanche triggering probabilities (P_{e} and P_{h}) at V_{ex}=6.6 V, as evident in Figure 1.6b. It's important to emphasize that in the neutral regions exterior to the depleted area, a photo-generated minority carrier diffuses into the depletion region following a probability computed by Eq.1.8. Subsequently, it accelerates toward the multiplication zone to initiate an avalanche event. Therefore, when a photon is absorbed in a neutral region, it holds the potential to contribute to the effective avalanche probability P_{av}, as depicted in Figure1.6b.

At this stage, a comprehensive understanding of the probability of carrier-triggered avalanche events in various silicon regions under distinct biasing conditions has been gaiend. To delve deeper, Fig. 1.7 displays normalized photon absorption probabilities across different regions as a function of wavelength. The visualization highlights that at shorter wavelengths ($\lambda < 500$ nm), a substantial proportion of transmitted photons are absorbed in the neutral region above the depletion area. Conversely, across the rest of the spectrum, photons are predominantly absorbed within the depletion region. It's essential to note that these values are normalized concerning total absorption at each wavelength. Therefore, the sum of relative absorptions equals 100 % for each wavelength. Essentially, this figure compares the contributions of diverse regions to the overall absorption for each specific wavelength, clarifying the relative absorptions in the neutral zones for shorter versus longer wavelengths.

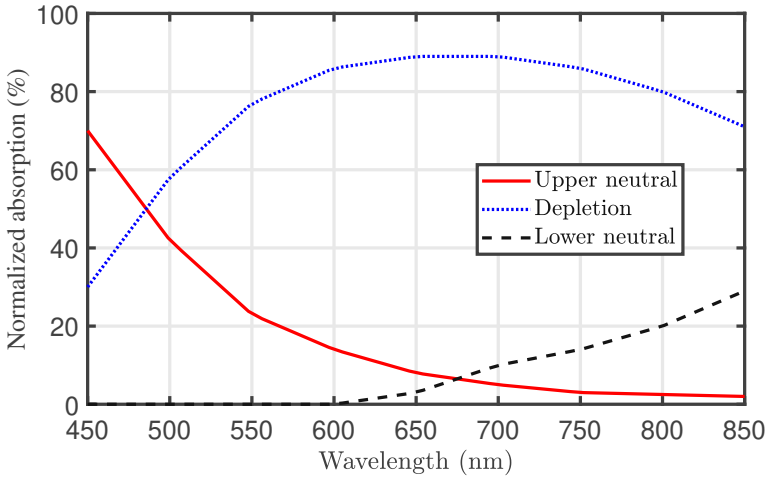

Figure 1.7: Normalized contribution of upper neutral, depletion, and lower neutral regions to the photon absorption probabilities as a function of wavelength ($\theta_0 = 0$). © 2021 IEEE. Reprinted, with permission, from [33].

1.6.5 Results verification

To verify the simulation and modeling outcomes through an optical perspective, I compute the PDP across various wavelengths and compare these results with the measured data. It's important to note that for a specific λ, different assumptions concerning the thickness of intermediate layers and the effective refractive index of the silicon nitride-based passivation layer can lead to a close match between the calculated optical transmission and experimental data. However, as I sweep through different λ values, the alignment between modeling, simulation, and experimental data only persists when the estimation methodology proves effective and these assumptions align with physical plausibility. This underscores the significance of ensuring the efficiency and validity of the estimation approach across a range of wavelengths for a robust match with experimental outcomes.

Figure. 1.8 illustrates the validation process, showcasing the comparison between calculated and measured spectra for two distinct excess bias values. This visual representation highlights the effectiveness of the approach and the reliability of assumptions regarding the parameters of intermediate layers within the CMOS technology. It's important to note that the PDP spectra at different excess bias voltages exhibit similar wavelength dependencies. Altering the applied voltage only influences the avalanche probability, while maintaining consistency in the optical absorption probability across the spectra.

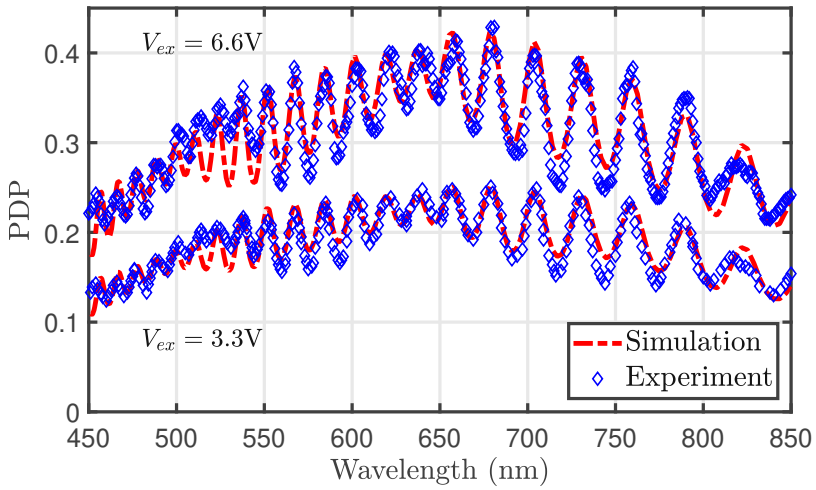

Figure 1.8: Measured and simulated photon detection probability as a function of λ ($\theta_0 = 0$). © 2021 IEEE. Reprinted, with permission, from [33].

From an electrical standpoint, evaluating the soundness of the modeling approach involves varying the applied excess bias voltage across the SPAD device. Under specific biasing conditions, diverse assumptions concerning doping profiles and parameters utilized for TCAD simulation (Table 1.2) might yield a calculated ATP and, consequently, an estimated PDP that aligns well with experimental results.

However, when varying the biasing levels, congruence between the modeling and experimental data is attained only if the applied approach and the foundational assumptions regarding device characteristics remain valid and accurate.

Figure. 1.9a illustrates the PDP, comparing both modeling and measurement approaches across various wavelengths as a function of the excess bias voltage. Notably, as the ATP rises with increasing excess bias, a corresponding augmentation in PDP is evident at higher voltage levels. The outcomes demonstrate that beyond a specific threshold (approximately 2 V), the PDP showcases a linear increment with the excess bias. This aligns with the behavior observed in the electric field strength within the multiplication zone, which exhibits a linear augmentation with increasing voltage levels.

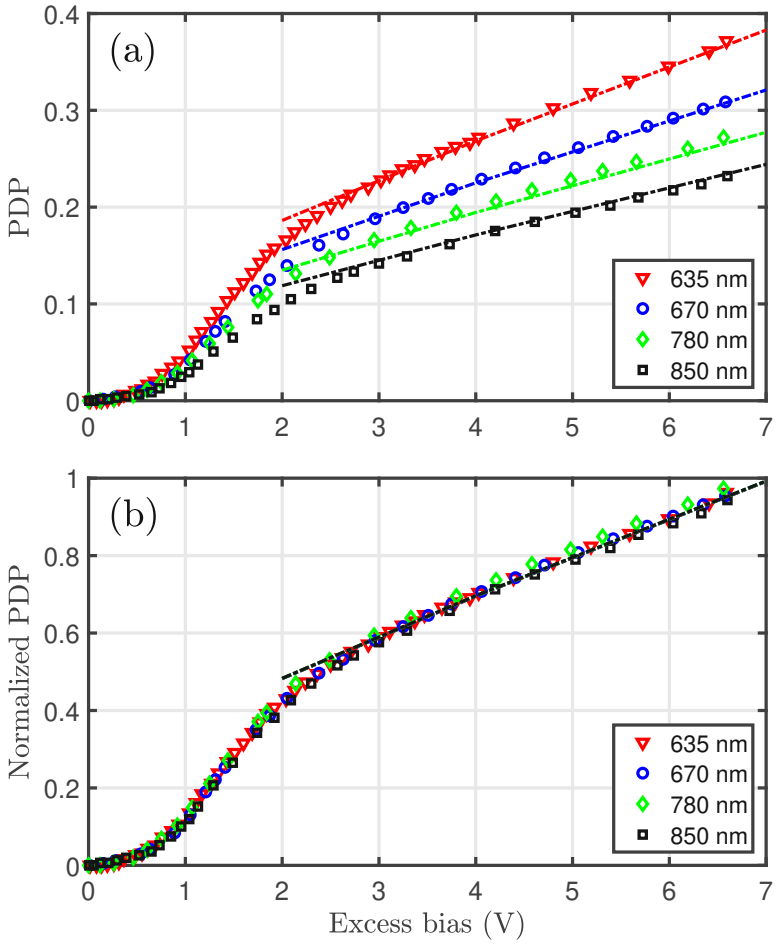

Figure 1.9: The obtained (a) and normalized (b) PDP based on experiment and simulation (dashed lines) data as a function of excess bias at different wavelengths ($\theta_0 = 0$). © 2021 IEEE. Reprinted, with permission, from [33].

At first glance, Figure.1.9a shows distinct rates of increase across different wavelengths. However, upon normalization of PDP values, as demonstrated in Figure.1.9b, it becomes evident that the behavior of PDP concerning the excess bias is wavelength-independent. Each PDP value at various wavelengths

is normalized to its corresponding value at an excess bias of 7 V. It's important to highlight that below a specific excess bias voltage (approximately 2 V in this case), the experimental measurement of PDP is notably influenced by the readout sensitivity of the electronic circuit, which is not accounted for in the presented modeling and simulation approach.

To underscore the advantages of the modeling and simulation approach, Figure.1.10a showcases the dependence of the PDP on the angular deviation of the incident light (θ_0) for two distinct wavelengths: one corresponding to a local PDP maximum (637 nm) and the other to a minimum (630 nm) in the PDP spectrum (Figure.1.4). Generally, the avalanche probability remains independent of θ_0. However, the absorption probability changes concerning θ_0 because photon transmission is a function of this parameter, as illustrated in Figure. 1.10a. Additionally, considering a non-zero θ_0 resulting in a deviation from the surface normal inside the silicon (depicted as θ_{Si} in Figure.1.10b), it affects the absorption profile within the silicon (e.g., Figure.1.5). For a given x, light takes a longer trajectory (by a factor of $1/\cos(\theta_{\mathrm{Si}})$) with an increased θ_{Si}. Consequently, the anticipated outcome would be a decrease in the average absorption depth as θ_{Si} increases. However, the simulation results indicate that this effect on the PDP is negligible because θ_{Si} is much smaller than θ_0, owing to the high refractive index of silicon. For instance, even at $\theta_0 = 60^\circ$, the light trajectory (i.e., the absorption depth) scales only by a factor of 1.03.

From Figure. 1.10, it's evident that the PDP diminishes with the augmentation of θ_0, attributed to the increase in reflection, resulting in fewer photons reaching the silicon. However, the PDP curves display fluctuations dependent on θ_0, showcasing a contrasting behavior between the two curves as θ_0 increases from zero. Specifically, at the initial stage ($0 < \theta_0 < 10^\circ$), the curve associated with the maximum (minimum) demonstrates a decrease (increase) concerning θ_0. The characterization of the PDP concerning θ_0 is notably valuable in practical detector design and applications. Defining the maximum detection angle corresponding to a minimally acceptable PDP is crucial, especially in applications like optical wireless communication [38]. However, experimentally determining these parameters can be arduous and time-consuming. Hence, employing a validated and reliable modeling and simulation approach, as presented here, can provide crucial insights into detector performance and aid in these practical applications.

1.7 Study of the effect of the electric field distribution on the PDP performance

Exploring diverse doping profiles available in different CMOS technologies opens the door to the design of varied SPAD structures. Understanding the impact of these diverse profiles on the electric field

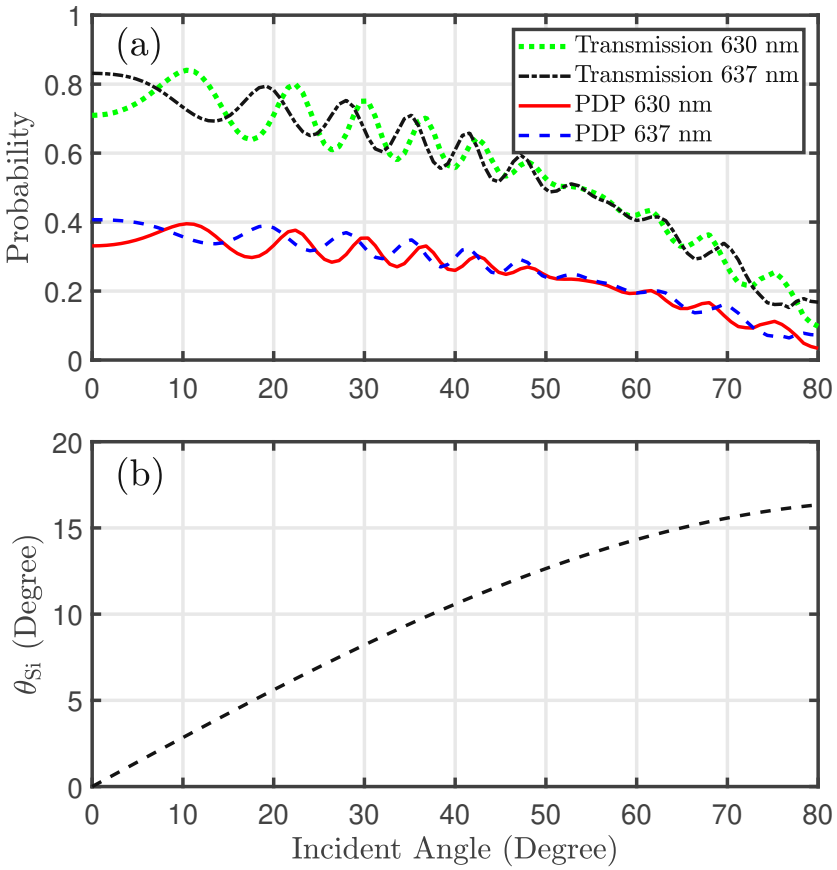

Figure 1.10: (a) The optical transmission and the PDP as a function of θ_0 at $V_{ex} = 6.6$ V. (b) Angular deviation of the light in the silicon from the surface normal (θ_{Si}) according to θ_0. © 2021 IEEE. Reprinted, with permission, from [33].

distribution within the device is pivotal in optimizing photodetection performance. This study delves into experimental and simulation-based PDP characterizations of two distinct reach-through SPADs featuring different doping profiles [39]. The aim is to investigate how the electric field distribution influences PDP performance. Essentially, this approach aligns with a form of electric-field engineering, achieved by comparing two distinct CMOS processes. To assess the PDP, the modeling methodology discussed in the preceding subsection has been applied.

1.7.1 SPAD structures

Here, the PDP of the above-discussed SPAD structure depicted in Figure 1.2 (referred to as SPAD1) is compared with another SPAD structure fabricated in a 0.35 μm high-voltage CMOS technology (SPAD2). Figure 1.11 illustrates the cross-section of SPAD2. This SPAD comprises an n^+ region and deep-p-well regions, while the diameter of the p-well is set to be smaller than that of the n^+ region. When the device is biased beyond the breakdown voltage ($V_{ex} = 6.6$V), a high electric field is es-

tablished at the n^+/p-well interface, known as the avalanche multiplication zone. To prevent edge breakdown, a deep-n-well region envelops the n^+/p-well region. The deep-n-well serves to reduce the effective p doping of the deep-p-well and p- epi layer, thereby extending the depletion region towards the p-substrate. This substantial widening of the drift region is pivotal for efficient photon absorption [34].

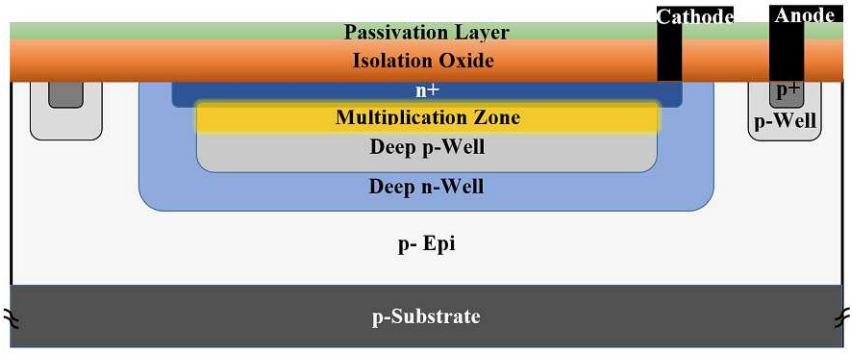

Figure 1.11: Cross section of the n^+/DPW SPAD (not to scale) [39].

1.7.2 Results comparison

Figure. 1.12 shows the PDP spectrum at an excess bias of 6.6 V for both SPAD structures, obtained from measurement and modeling.

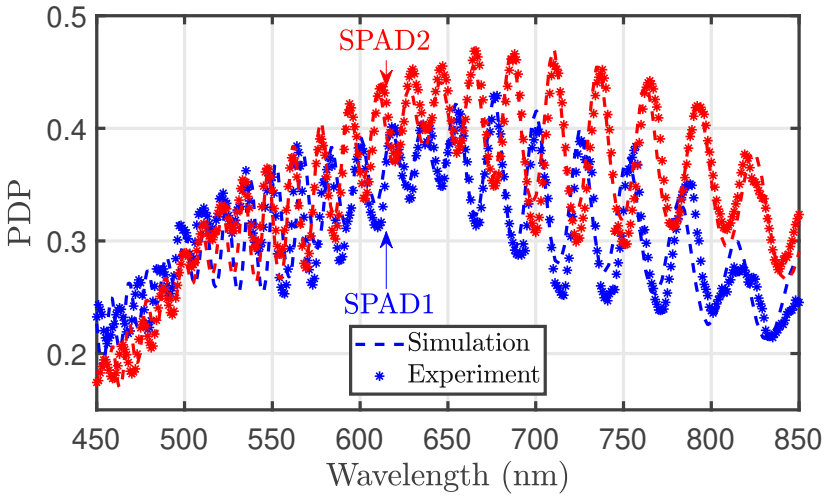

Figure 1.12: PDP spectra based on experiment (dotted) and simulation (dashed lines) at an excess bias of 6.6 V [39].

It is noticeable that SPAD2 exhibits a higher PDP at longer wavelengths ($\lambda \geq 580$ nm) compared to SPAD1. Considering that both SPADs are covered with similar layers (isolation and passivation stack), one would expect them to demonstrate similar optical characteristics. Hence, based on the model, the

discrepancy in the PDP between the two SPADs is primarily attributed to their distinct ATP. As the ATP is notably influenced by the electric field and the ionization coefficient distribution, TCAD simulations were conducted to delve into these parameters in both SPAD configurations.

Figure.1.13(top) demonstrates the electric field distributions (vertical cross-section at the center) within the depth range $x = [0; 2]\mu$m of the two SPADs under an excess bias voltage of 6.6 V. Upon closer examination of the electric field profile, it's discernible that while the maximum electric field value in SPAD2 is marginally lower than that of SPAD1, its high-field region is notably wider. This difference results in a wider but less intense distribution of the electron and hole ionization coefficients in SPAD2 in comparison to SPAD1, as depicted in Figure. 1.13(middle). The ionization coefficient at any depth (x) signifies the average number of electrons/holes generated by a carrier over a unit length along the field direction. Consequently, in SPAD2, ionization events occur across a thicker region, albeit with a reduced multiplication rate in contrast to SPAD1.

Accordingly, the electron and hole ATP distributions (Fig. 1.13(bottom)) for both SPADs, as a function of depth (x), are derived from the ionization coefficient profiles. Remarkably, despite having a lower maximum value of carrier ionization coefficients, SPAD2 exhibits higher $\mathrm{P_e}$ and $\mathrm{P_h}$ than SPAD1. This occurrence is attributed to the thicker ionization coefficient profile and, consequently, the multiplication region of SPAD2 compared to SPAD1. The thicker multiplication region in SPAD2 allows for more collisions within the wider high-field region, resulting in higher ATP.

Now, to clarify the observed PDP spectrum (Figure. 1.13), let's compare the ATP of the two SPADs. The higher PDP of SPAD2, particularly at long wavelengths, is attributed to a substantial fraction of the total transmitted photons being absorbed at greater depths (below the multiplication region). In this region, $\mathrm{P_e}$ of SPAD2 is higher than that of SPAD1. Conversely, shorter wavelength photons tend to be absorbed within or near the multiplication region, where the disparity between $\mathrm{P_e}$ and $\mathrm{P_h}$ in both structures is smaller. Consequently, the PDP of both SPADs is anticipated to exhibit no significant difference at shorter wavelengths.

1.8 PDP enhancement using an anti-reflection coating in CMOS-based SPADs

In CMOS-based implementations, the presence of isolation and passivation layers often leads to degraded photon transmission into the SPAD, exhibiting a wavelength-dependent behavior due to standing wave formation [32, 33]. To address this limitation, certain technologies incorporate an opto-window module, eliminating the passivation and isolation stack over the photosensitive area and adding an anti-reflection coating (ARC) layer on the top of the silicon. This ARC layer can significantly re-

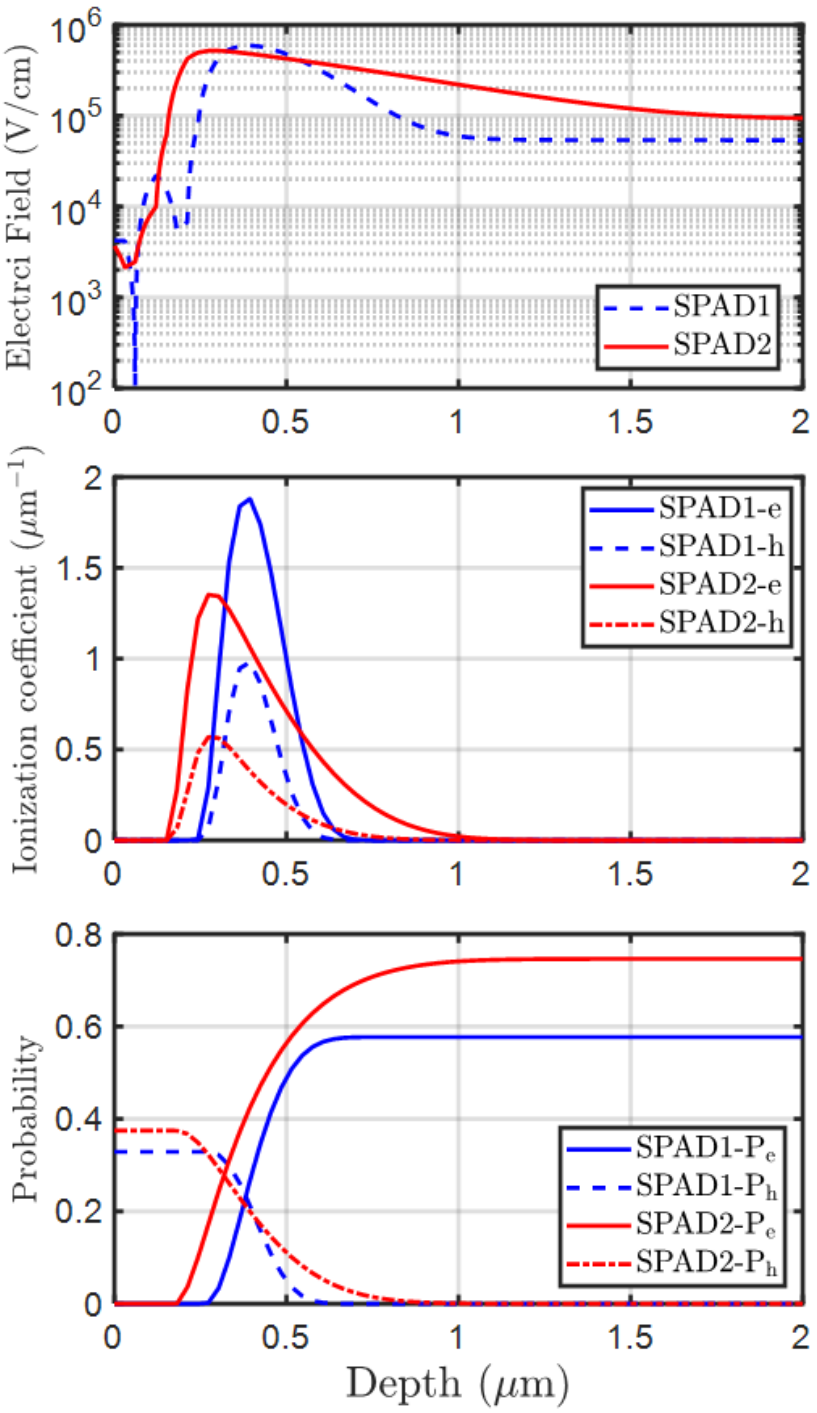

Figure 1.13: Extracted distributions of electric field (top), electron and hole ionization coefficients (middle), and electron and hole avalanche triggering probabilities (bottom) as a function of the depth (x) at an excess bias of 6.6 V [39].

duce reflections, potentially down to zero at a specific wavelength based on its characteristics, thereby suppressing fluctuations in the PDP spectrum.

The study outlined in [40] investigates the enhancement of the PDP in CMOS-SPADs using an ARC above the sensitive area, both through simulation and experimental analysis. The presented modeling

approach is adapted to carefully take the effect of the ARC layer into account when simulating the PDP of the SPAD. The study reveals how the ARC layer not only improves optical transmission but also prevents the penetration of standing waves into the shallow regions near the silicon surface, where the SPAD's multiplication region is established. Additionally, the optimal ARC layer thickness corresponding to maximal PDP enhancement across different wavelengths in the visible spectrum is extracted. This insight into ARC selection becomes invaluable when various ARC thicknesses are available within the CMOS process. Further details regarding these findings will be discussed in Section 2.1.

1.9 Fill factor enhancement using a virtual guard ring in cylindrical n^+/p-well CMOS single-photon avalanche diodes

Si-CMOS SPADs, relying on n^+/(deep)p-well and p^+/(deep)n-well structures, are widely utilized due to their integration compatibility with circuitry [34, 41–47]. These designs often incorporate physical guard rings to avoid premature edge breakdowns caused by localized high electric fields near the junction edge. Various physical guard rings such as diffusion guard rings [48], trench isolation guard rings (STI) [49], and low-doped guard rings [50,51] have been employed to lower the peripheral electric field. However, the presence of physical guard rings often results in a decreased fill factor, defined as the ratio of the active area (photo-sensitive area) to the total device area. This reduction becomes more pronounced when the SPAD is miniaturized, and the guard ring dimensions are comparable to those of the photo-sensitive area.

To overcome this challenge, virtual guard rings have been implemented in p^+/n-well SPADs to facilitate smaller structures [52–55]. In [56], I employ this concept in the n^+/p-well CMOS SPAD structure, featuring separate thick absorption and multiplication zones, which proves efficient for longer wavelengths for the first time. I investigate the effect of a virtual guard ring, replacing a physical guard ring, on the built-in electric field and the fill factor of the SPAD. Additionally, it is demonstrated that the lateral electric field at the edge of the active area diminishes the effective active area due to the deviation of the carrier path from their purely vertical trajectory towards the boundary outside the multiplication region. Previous studies have, to my knowledge, overlooked this effect, which is crucial when scaling down the SPAD. A comprehensive discussion of these findings will be presented in detail in Section 2.2.

1.10 Design of a novel avalanche photodiode based on electric field-line crowding concept

As discussed earlier, commonly employed designs for integrated Si CMOS avalanche photodiodes are based on planar p^+/n-well and n^+/p-well junctions. These structures present a trade-off between bandwidth and responsivity, particularly in the long-wavelength range, such as red and near-infrared light. Diodes featuring thin depleted absorption regions offer high bandwidth due to shorter charge carrier drift times [42, 46, 47, 57–59], with the detection region thickness typically in the order of hundreds of nanometers. However, such structures suffer from low responsivity as carriers generated under the thin absorption region contribute minimally to the output current. To address this limitation, a reach-through design concept was introduced to broaden the absorption region and consequently enhance responsivity [60–63]. These thicker APDs create a space-charge region with a thickness of around 10 µm. For instance, a reported maximum responsivity of 2.7×10^4 A/W for 5-nW optical power at 670 nm was achieved in Ref [61]. However, their major drawback lies in limited bandwidth due to longer carrier drift times in the thicker absorption zone.

Moreover, in planar structures, the photo-sensitive area is constrained by the p/n junction area, leading to lower sensitivity to carriers generated in the peripheral volume. Additionally, they often necessitate a guard ring to prevent premature edge breakdown, which further reduce the sensitive-area to total-area ratio [64–67]. This limitation becomes more significant when the APD is downsized, with the peripheral region comparable to the dimensions of the photo-sensitive area [56].

Reference [68] proposed a current-assisted avalanche photodiode that could collect charges generated in the peripheral volume. This APD utilized two surface electrodes with different potentials to create a drifting electric field guiding the photogenerated electrons in the peripheral volume towards the central multiplication region. While achieving a high ratio of sensitive-area to total-area, it achieved a maximum bandwidth of 275 MHz and 13 A/W responsivity at a wavelength of 830 nm. References [69–71] employed a charge-focusing concept to gather peripheral charge carriers in the design of single-photon avalanche photodiodes (SPADs). In [69,70], a customized fabrication process involved a shallow n-type implant between the cathode and anode, aiming to redistribute the electric field just below the silicon/silicon dioxide interface at the surface to reduce the dark count rate. Reference [72] presented a silicon photomultiplier (SiPM) utilizing a SPAD based on the field-line crowding effect. However, transistors could not be fabricated in the special SiPM detector process.

In [73], I adopt the field-line crowding concept to design a new APD fabricated in a standard CMOS process without process modification. This APD features a small spherical avalanching n-well/p-epi junction at the center and a thick volume in the p-epitaxial layer with a lower electric field around the

avalanching region as the absorption zone. The achieved maximum responsivity is 3.05×10^3 A/W at 5 nW optical power, with a maximum bandwidth of 1.6 GHz (R=32 A/W) at 200 nW optical power for the wavelength of 675 nm. Further details regarding the EFLC-APD will be discussed in Section 2.3.

1.11 Characterizing the EFLC-APD in the near-infrared range and assessing the influence of design parameters on its performance.

In the previous publication [73], I introduced the APD based on electric field-line crowding (EFLC) and provided its characterization at the wavelength of 675 nm. In this study [74], serving as a continuation of my earlier work [73], I present an expanded investigation into the performance of the EFLC-APD, specifically, delve into the modification of the electric field induced by design parameters such as cathode radius and diode size, offering insights into their impact on the device's characteristics. Furthermore, the characterization to the near-infrared regime (at 850 nm) is extended, which is particularly relevant for applications in light detection and ranging (LIDAR) sensors. This deeper exploration, especially at longer wavelengths (850 nm), significantly enhances the value of the previous research, providing a more comprehensive understanding of how these design parameters affect the frequency response and breakdown voltage of the EFLC-APD. This comprehensive understanding aids designers in optimizing EFLC-APD-based detectors across various CMOS technologies.

Moreover, an additional part included in this study involves the characterization of excess noise in the EFLC-APD, which is an important performance metric in the assessment of APDs. This study contributes further to the overall characterization of the EFLC-APD and its suitability for practical applications. Further insights and detailed outcomes regarding the characterization of the EFLC-APDs will be elaborated in Section 2.4.

1.12 n^+/p-well dot avalanche photodiode

Ref. [74] implemented the field-line crowding concept by employing a small n+/n-well structure, achieving a distributed electric field across the diode volume to guide photo-generated carriers in the peripheral region. The reported APDs achieved a maximum bandwidth of 1.6 GHz and a responsivity of R = 32 A/W at λ=675 nm with an operating voltage of 67 V. However, the high operational voltage of these diodes can present integration challenges with electronic circuits in some CMOS technologies. Additionally, enlarging the active area by simply increasing the surface anode radius becomes limited due to the diminishing electric field away from the center, hindering effective carrier transport towards the cathode.

The paper [75] introduces a novel CMOS-integrated dot avalanche photodiode (dot-APD) employing a small central n+/p-well hemispherical cathode/p-well structure. This design facilitates radial electric field generation for both vertical and peripheral charge collection. The achieved performance metrics include a bandwidth of 1.8 GHz and a responsivity of 9.7 A/W, all at a notably lower operating voltage of 24 V compared to the APD presented in Ref. [74]. Moreover, In this study, I propose a multi-dot structure (MD-APD), consisting of an array of several cathode/p-well dots with a shared anode. This design allows for easy enlargement of the active area by expanding the cathode dot array. The active area can be adjusted by increasing the number of cathode dots arrays or by altering the distance between the cathode dots (array's pitch size). Importantly, the responsivity and frequency response of the MD-APD are independent of the array size but are influenced by the array pitch size. This occurs because the electric field distribution remains unaffected by the number of cathodes but changes with the distances between them.

This advantageous design flexibility allows for expanding the active area while maintaining performance, positioning the multi-dot APD as a promising candidate for diverse applications, and showcasing its superiority over existing state-of-the-art APDs. A comprehensive and detailed discussion about the functionality and design considerations of these diodes will be presented in Section 2.5.

1.13 Large active area, low capacitance multi-dot PIN Photodiode

Here [76], the advantage of decoupling the P/N junction area from the light-sensitive area of dot structures is used for designing a multi-dot PIN (MD-PIN) photodiode to achieve a large light-sensitive area with a relatively small capacitance. The intention behind this is to expand the light-sensitive region of the photodiode, in contrast to the setup detailed in reference [77], where an ultra-sensitive optical receiver utilized a single-dot PIN photodiode with a light-sensitive area of 706 μm^2. Particularly in systems employing capacitive-feedback transimpedance amplifiers, such as in [77], maintaining low photodiode capacitance is critical for achieving optimal sensitivities. A 5×5 multi-dot PIN photodiode with an active area measuring 100 μm × 100 μm has exhibited a responsivity of 0.29 A/W and a bandwidth of 660 MHz at λ=675 nm, while maintaining a capacitance of 48 fF. This underscores its suitability for applications necessitating low capacitance and moderate bandwidth.

However, scaling the array introduces certain considerations. As the array size increases, the spacing between individual cathode dots must also grow. Ensuring an optimal pitch size becomes crucial to maintain an ideal electric field distribution across the photodiode's active region. Varying pitch sizes can lead to disparities in the electric field distribution, impacting the photodiode's performance. Achieving a balance between a larger light-sensitive area and managing challenges such as capacitance,

response speed, and electric field strength is essential. Furthermore, enlarging the array and increasing the number of cathode dots might result in heightened capacitance concerns. Larger cathode arrays could accumulate increased cumulative capacitance, potentially affecting the optical sensor's overall bandwidth and response speed. Additionally, having smaller cathode dots in larger arrays may require more metal lines for interconnection, possibly leading to a higher parasitic capacitance.

It's important to acknowledge that while my present research primarily focuses on the dot photodetector concept in silicon, there's a strong potential for extending this concept to other semiconductor materials. Implementing this concept to different technologies would demand a deep understanding of material-specific properties and meticulous optimization of fabrication processes. Although the fundamental principles governing the dot photodetector concept remain applicable, adapting device design and fabrication techniques would be necessary to align with the distinctive characteristics of the particular semiconductor technology involved. Design considerations and optimization strategies to enhance the performance of these diodes for various applications will be discussed in Section 2.6.

Chapter 2

Publications

2.1 Photon detection probability enhancement using an anti-reflection coating in CMOS-based SPADs, "Applied Optics 2021"

Seyed Saman Kohneh Poushi, Hiwa Mahmoudi, Michael Hofbauer, Bernhard Steindl, and Horst Zimmermann, "Photon detection probability enhancement using an anti-reflection coating in CMOS-based SPADs," Applied Optics, vol. 60, no. 25, pp. 7815–7820, 2021.

applied optics

Photon detection probability enhancement using an anti-reflection coating in CMOS-based SPADs

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This work presents a simulation and experimental study of the photon detection probability (PDP) enhancement in CMOS single-photon avalanche diodes (SPADs) using an anti-reflection coating (ARC) above the sensitive area. It is shown how the ARC layer can improve the PDP, not only by improving the optical transmission, but also by eliminating the penetration of the standing wave into a shallow region close to the silicon surface, where the multiplication region of the SPAD is formed. Furthermore, the appropriate ARC layer thickness corresponding to maximum PDP enhancement at different wavelengths over the visible spectrum is extracted to provide insight regarding the ARC selection if different ARC thicknesses are available within the CMOS process.

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1. INTRODUCTION

The high sensitivity and possibility of integration together with standard CMOS readout and signal processing circuits have made the single-photon avalanche diode (SPAD) a very attractive candidate for many photon-starved applications such as optical wireless communication, time-of-flight sensors, fluorescence microscopy, and biomedical imaging sensors [1–8]. The operation principle of SPADs is similar to a simple p-n junction structure reversely biased above its breakdown voltage (i.e., in the Geiger mode) with a strong electric field over a shallow region at the p/n interface (multiplication region), where the carriers gain kinetic energy to create a self-sustaining avalanche due to the impact ionization effect. Photon-generated carriers can reach this multiplication region and trigger a macroscopic avalanche event that can be easily detected by simple electronic circuits.

The detection probability of an incident photon depends on two terms: the probability that the incoming photon reaches the silicon and generates an electron–hole pair, and the probability that the photo-generated electron–hole pair initiates an avalanche event. Therefore, to evaluate the photon detection probability (PDP) as a key parameter in the SPAD performance characterization, one should consider both avalanche triggering and photon absorption probabilities [9–12]. There has been a variety of approaches to improve the avalanche triggering probability by manipulating the multiplication region depth and electric field distribution [13–17]. The scope of this work, however, is to investigate the optical properties (light transmission in the isolation/passivation layers) of CMOS SPADs and the influence of an anti-reflection coating (ARC) on the photon absorption probability.

In CMOS implementation, when the silicon is covered by isolation and passivation layers, the photon transmission into the SPAD sensitive area is degraded and shows a wavelength-dependent behavior due to the formation of standing waves [18]. To overcome this issue, in special CMOS technologies, an extra treatment is available to replace the isolation and passivation stack above the photodiodes by an ARC layer. In this work, we present a simulation and experimental study of the SPAD optical properties in the presence of the ARC layer. To simulate the PDP of the SPAD, we adopt the modeling approach presented in [18] to carefully take the effect of the ARC layer into account. The model can capture different optical and electrical parameters to consider the effects of wavelength, light incidence angle, and transmission/absorption profiles of the light. Therefore, it provides an understanding that cannot be achieved based on pure experimental analyses and offers better insight to the designer of a SPAD-based detector. The rest of the paper is organized as follows. In Section 2, the structure of the SPAD is described, and the measurement setup and modeling approach are explained in Section 3. The simulation and the experimental measurement results are discussed in Section 4, and the paper is concluded in Section 5.

2. DEVICE DESCRIPTION

Figure 1 shows the cross section of an n^+/deep-p-well SPAD fabricated in the 0.35 μm modular high-voltage CMOS process (XH035 of X-FAB Semiconductor Foundries), where an

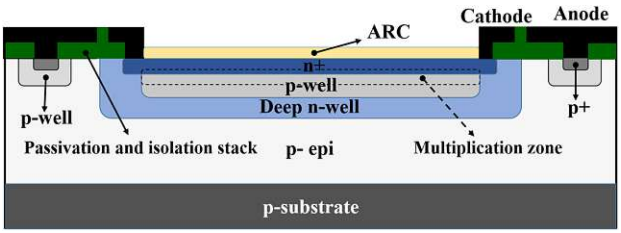

Fig. 1. Cross section of the n^+/DPW SPAD (not to scale).

ARC is available. The implementations comprise a shallow highly doped n^+ layer and a deep p-well region embedded in a p-doped epitaxial layer (p-epi) with a doping concentration of $\sim 1 \times 10^{15}$ and thickness of ~ 10 μm. In the Geiger-mode operation (biasing above the breakdown), a strong electric field is formed in a thin zone at the interface of n^+/deep p-well that serves as the avalanche multiplication zone. To eliminate the edge breakdown effect, the diameter of the deep p-well is formed to be smaller than that of the n^+ region. Furthermore, both regions are surrounded by a deep n-well region to decrease the effective doping concentration of the p-well and, accordingly, increase the breakdown voltage. A high breakdown voltage results in a complete depletion of p-epi layer when the SPAD is biased in breakdown. This remarkably increases the thickness of the drift region to extend the absorption zone and makes the SPADs more efficient at longer wavelengths (red and infrared light) [19].

In typical CMOS technologies, thick inter-metal oxide and passivation stacks cover the whole chip surface, and the incident photons can reach the silicon only after crossing these layers. Due to the refractive index mismatch at the interfaces, a part of the photons is reflected and these photons do not reach the silicon. Furthermore, because of a standing wave effect in these layers, the PDP shows a complex wavelength dependence as is explained in [18]. Some technologies provide a module of opto-window, in which the passivation and isolation stack over the photosensitive area is removed and a layer of ARC is deposited on the silicon. This can reduce the reflection down to zero at a specific wavelength, depending on the ARC layer characteristics, and suppress the fluctuations in the PDP spectrum. As shown later, the ARC layer characteristics need to be selected or optimized carefully to achieve a considerable improvement in the optical properties of the SPAD over a desirable range of the spectrum.

3. MEASUREMENT AND SIMULATION SETUP

A. Measurement Setup

A tunable light source built from the monochromator CM110 as well as the xenon light source ASB-XE-175, both from Spectral Products, coupled with a multimode fiber with a core diameter of 62.5 μm, was used for the PDP measurement to sweep the wavelength from 450 nm to 850 nm with a spectral width of ~1 nm. A 50/50 fiber splitter split up the light to feed it to a calibrated reference detector for measuring the current photon rate and to the fiber that feeds the light to the device under test. The fiber-coupled tunable optical attenuator DD-100-11 from OZOptics set the ratio of the optical power between the fiber that feeds the light to the sample and the fiber that leads to the power monitoring. This ratio was adjusted to be in the range of 10^5, leading to a light flux of 5×10^6 photons/second on the sample. It should be noted that the diameter of the fiber is smaller than the diameter of the active area, and it was held around 10 μm above the sample so that the total light was irradiated into the active area and almost all incident photons had the chance to be detected. The fiber was aligned by means of a motorized *xyz* stage from Thorlabs, built from three linear stages (KMTS50E/M). A fast active quenching/resetting circuit with a dead time of 9 ns was used to extinguish the avalanche current after each detection and then charge the SPAD again for the next photon detection. See [20] for more details about this active quenching/resetting circuit. The output data from the active quenching circuit was read by the digitizer NI PXIe-5162 coupled with the FPGA card NI PXIe-7972R, both cards of a PXI [PXI stands for peripheral component interconnect (PCI) extensions for instrumentation] system from National Instruments (NI). This PXI system also included the controller PXIe-8840, which allowed controlling the measurement setup and provided a graphical user interface.

B. PDP Modeling

The PDP is evaluated as the ratio of detected photons to the total number of incident photons. It is clear that due to a non-zero reflection coefficient, not every incident photon is transmitted into the silicon, and, in addition, the transmitted photons are absorbed inside the silicon in accordance with a probability distribution along the depth (x). A photo-generated carrier can move (i.e., drift or diffuse, depending on where the photon is absorbed) towards the multiplication region and trigger a self-sustaining avalanche event (i.e., a detectable current pulse). However, there is no guarantee that every photo-generated carrier creates an avalanche event due to the random nature of the avalanche process. Therefore, the PDP is estimated as a combination of two probability terms: the photon absorption probability (P_{ab}) and the avalanche triggering probability (P_{av}) given by

$$\mathrm{PDP}(\lambda) = \int_0^{x_{si}} P_{ab}(\lambda, x) \times P_{av}(x) \mathrm{d}x, \tag{1}$$

where $P_{ab}(\lambda, x)$ represents the photon transmission through the layers on top of the silicon and the photon absorption probability distribution inside the silicon, and $P_{av}(x)$ denotes the avalanche triggering probability, defined as the probability that the electron–hole pair generated at depth x initiates a self-sustaining avalanche. To calculate the PDP using Eq. (1), P_{av} and P_{ab} are obtained by means of TCAD (Geiger-mode device simulation feature of SILVACO Atlas) [21] and electromagnetic (CST Microwave Studio) [22] simulation tools, respectively [18]. It is important to note that because of structural symmetry (cylindrical structure) and the large diameter of the SPAD (~80 μm, which is around two orders of magnitude larger than the wavelength in the visible range), one can estimate both $P_{ab}(\lambda, x)$ and $P_{av}(x)$ as a function of x and assume negligible dependence on the radial direction. As a result, with a good approximation, the PDP model reduces to a one-dimensional numerical integration over the depth.

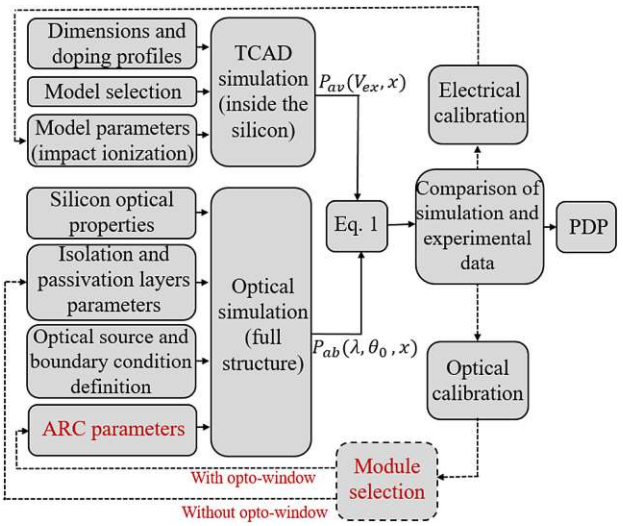

Fig. 2. Flow chart of the PDP modeling methodology including the module selection to consider the ARC layer.

Figure 2 represents a flow chart of the PDP modeling methodology based on Eq. (1) [18]. To obtain $P_{av}(x)$ by TCAD simulations, the structural parameters including the dimension of the structure and doping profiles are defined according to the layout design and the process design kit. In addition, the physics-based models including impact ionization, generation–recombination, and mobility need to be defined carefully and calibrated based on experimental data [18]. The TCAD simulation results to obtain $P_{av}(x)$ are independent of the application of the ARC layer, as a layer above the silicon can affect the photon transmission into the silicon, but not the electric field profile inside the silicon.

$P_{ab}(\lambda, x)$ is extracted by electromagnetic simulations performed using CST Microwave Studio software. Therefore, we need to define the optical properties of the silicon, the light source, and the boundary conditions in accordance with measurement conditions. Furthermore, the layer above the silicon (its thickness and refractive index) needs to be defined carefully, as it has a significant influence on the optical transmission into the silicon. Accordingly, the device is illuminated by a plane wave light source, and the light propagation inside each layer is calculated through solving Maxwell equations with the finite-difference time-domain (FDTD) method. Since the light is considered as a wave, the transmission is obtained by dividing the amount of light intensity inside the silicon (at the surface) by the total incident light intensity, which is equivalent to the probability that a photon is transmitted into the silicon. According to a similar argument, the photon absorption probability distribution as a function of depth (x) corresponds to the light absorption profile obtained from the simulation. In the SPAD with the isolation and passivation stack, a calibration of optical properties of these layers is required to obtain accurate optical simulation results [18] due to the lack of technology information, i.e., the exact values of the isolation stack thickness or the refractive index of the passivation layers.

Furthermore, we extend the PDP modeling methodology presented in [18] to include a module selection option, which allows us to replace the isolation and passivation layers by the ARC layer in the simulations, when the opto-window is available and used in the fabrication. In this case, the electromagnetic simulation is performed in the presence of the ARC layer to obtain $P_{ab}(\lambda, x)$. It should be mentioned that as the ARC layer thickness is not tightly controlled and has a tolerance, an optical calibration is essential to achieve good consistency between the simulation and experimental measurement results.

Accordingly, by obtaining these two probabilities ($P_{ab}(\lambda, x)$, $P_{av}(x)$), the calculation of PDP becomes a one-dimensional numerical integration problem that can be implemented in MATLAB.

4. MODELING AND MEASUREMENT RESULTS

To evaluate the effect of the ARC layer on the SPAD performance at different wavelengths, Fig. 3 shows the measured spectral PDP of the SPAD with and without the ARC layer for perpendicular light incidence at an excess bias of 6.6 V. The ARC layer having a thickness of 44 nm consists of Si_3N_4 ($n \simeq 2.0$). Furthermore, it indicates the corresponding simulation results obtained by the modeling approach, explained in the previous section.

First, it can be seen that the simulation results show an excellent match with the measurement data, therefore, we can conclude that the modeling approach and the corresponding calibrations are verified and reliable to investigate other effects or parameters that cannot be obtained experimentally. This will allow us to better understand the impact of the layers above the silicon on the SPAD performance, as shown later. Furthermore, both simulation and measurement results verify the PDP enhancement using the ARC layer at wavelengths below ~600 nm. This is due to the improved photon transmission into the silicon and the elimination of the standing wave effect that degrades the absorption profile, as shown in Fig. 4. At longer wavelengths, the ARC layer removes the fluctuations of the PDP; however, it does not increase the PDP at all wavelengths as compared to the PDP values when the complete isolation and passivation stack is present. This is due to the fact that the thickness of the ARC layer is optimized for smaller wavelengths, where it shows a maximum quarter-wave matching effect. But the matching effect is decreased at other wavelengths and can even degrade the photon transmission, as explained later.

To investigate the effect of the ARC layer on the photon transmission into silicon, Fig. 4(a) shows the transmission spectrum

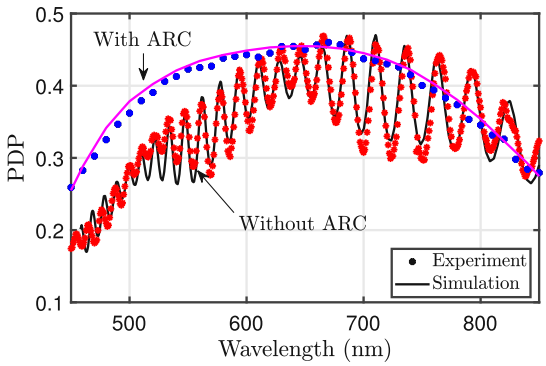

Fig. 3. Measured and simulated PDP spectrum of the SPAD with and without the ARC layer. The ARC layer thickness is 44 nm.

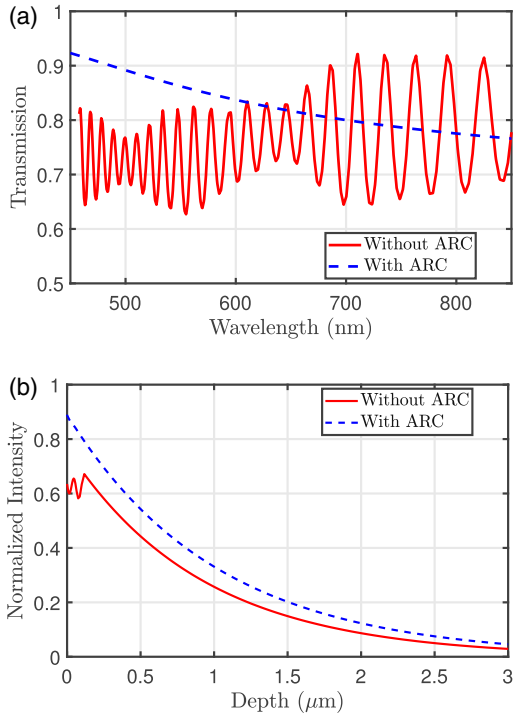

Fig. 4. (a) Optical transmission of the SPAD with and without the ARC layer. (b) Photon absorption probability as a function of depth x inside the silicon at a wavelength of 500 nm.

for both SPAD with the ARC layer and SPAD covered by the complete passivation and isolation stack based on optical simulations and calibrated parameters that fit the PDP spectrum. The fluctuations in the transmission spectrum of the SPAD without the ARC layer is because of the formation of standing waves in the passivation and isolation stack caused by destructive and constructive interference of multiple reflections of light at the interfaces. The ARC layer, however, suppresses this fluctuation effect and additionally reduces reflection losses in a specific wavelength range. In this wavelength range, the ARC layer acts like a quarter-wavelength transformer that reduces the reflection with minimal reflection at a specific wavelength (λ_{arc}), which sees the ARC thickness as a perfect quarter-wavelength. Furthermore, as shown in Fig. 4(b), when the ARC layer is not used, the standing wave in the isolation layer penetrates into the silicon and causes a ripple in the absorption profile within a narrow region (~200 nm) close to the silicon surface (indicated by zero depth). This can have a considerable effect, as the multiplication zone is formed very shallow and close to the surface in such SPAD structures. By eliminating the standing wave effect, the ARC layer provides an ideal exponential absorption profile inside the silicon with a maximum value at the surface.

As mentioned before, a given ARC layer provides a PDP enhancement only over a limited range of the visible spectrum. Therefore, to evaluate the PDP enhancement, we calculate the PDP using the proposed modeling methodology shown in Fig. 2, for different ARC thicknesses and for three different wavelengths as shown in Fig. 5.

It can be seen that there are optimum ARC thicknesses at which the PDP reaches a maximum for a wavelength. It is interesting to note that at each wavelength (λ), the optimum

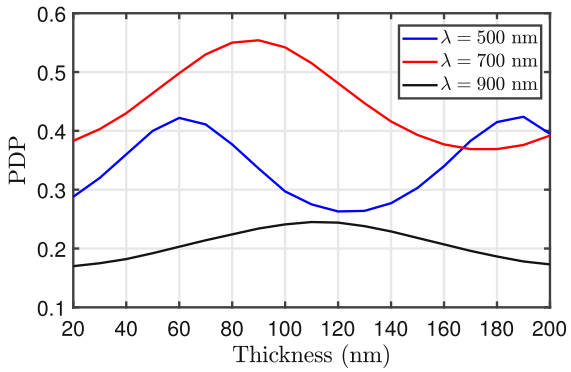

Fig. 5. PDP as a function of the ARC layer thickness for three different wavelengths.

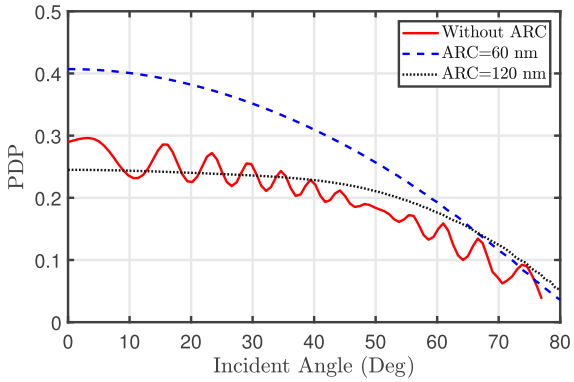

Fig. 6. PDP as a function of the angular deviation from the surface normal of the incident light ($\lambda = 500$ nm).

thickness (t_{opt}) corresponds to the quarter-wavelength taking the refractive index of the ARC layer (n_{arc}) into account, i.e., $t_{opt} = \lambda/(4n_{arc})$. This is due to the fact that the phase difference of the two reflected waves from the interface of air/ARC and ARC/silicon is π, leading to destructive interference. As a result, the reflected wave is at a minimum that leads a maximum transmission into the silicon. Furthermore, the PDP decreases to a minimum when the thickness goes to $\lambda/(2n_{arc})$, or in general, an integer multiple of $\lambda/(2n_{arc})$. Therefore, the PDP shows a periodic behavior with the ARC thickness, and to achieve considerable improvement in the optical properties of the SPAD using the ARC layer, one should pick the correct thickness for the desirable wavelength range according to the application. Another fact that can be observed from Fig. 5 is the robustness against the ARC thickness variations, especially at optimum thickness values. For example, if the thickness is around 60 nm corresponding to the first PDP maxima for $\lambda = 500$ nm, a $\pm 10\%$ variation will have a negligible effect on the PDP.

To gain further insight into the effect of the ARC layer in the presence of angular deviation of the incident light (θ_0) from the surface normal, Fig. 6 shows the dependency of the PDP on θ_0 for the SPAD structure without the ARC layer (i.e., with the complete isolation and passivation stack) as well as the structure with the ARC layer for two different ARC thickness values. The ARC thickness values are set to 60 nm and 120 nm in the simulations, corresponding to the maximum and minimum PDPs at $\lambda = 500$ nm, respectively (Fig. 5).

It is clear that the PDP shows a strong dependency on θ_0, as the photon transmission (reflection) is a function of θ_0. In general, the PDP deceases with increasing θ_0 because the reflection will increase and fewer photons can penetrate into the silicon. Nevertheless, in the structure without the ARC layer, the PDP shows θ_0-dependent fluctuations. This is due to the same reason for the λ-dependent fluctuations seen in Fig. 3. In fact, as the increase in θ_0, at a given λ, results in an increase in light trajectory, it has an effect similar to the increase in thickness or decrease in λ. These fluctuations are suppressed in the structure with the ARC layer, as it breaks the standing wave condition. It should be mentioned that for increasing θ_0, the absorption depth decreases (or the trajectory to the absorption depth for θ_0 increases). However, due to the large refraction index of silicon ($n = 3.5$) for $\theta_0 = 60°$, the absorption depth scales only by 1.03 [18]. Nevertheless, the ARC layer may enhance or degrade the PDP depending on its thickness, as explained before. It can be seen that the optimum ARC layer (60 nm thickness) retains its superiority for the tilted light source; however, its efficiency decreases for higher θ_0 values ($\sim 60°$). It is important to note that the ARC layer with a thickness of 120 nm (corresponding to the minimum PDP) can improve the PDP for $\theta_0 \geq 30°$ compared to that of the structure with the passivation and isolation stack.

It should be mentioned that the presented PDP modeling procedure can be implemented for other SPAD structures by adopting the optical simulation and/or the TCAD to study the influence of different ARC types on the PDP performance of different SPADs. Generally, there are different types of single- and multi-layer ARCs with different materials, including silicon nitride, silicon oxynitride, MgF_2, and HfO_2, used in various applications [23–27]. However, we are not aware what ARC options (i.e., material and thickness) are available in different CMOS technologies, as it could be confidential data. Certainly, CMOS compatibility has the highest priority not to contaminate the fab. Therefore, ASIC foundries will clearly prefer silicon nitride, silicon dioxide, and silicon oxynitride as material for ARC applications. Nevertheless, by following a similar procedure, the effect of different available ARC layers (different materials and/or different thicknesses) on the PDP performance of the SPAD can be characterized by simulation, and accordingly, the optimum available option will be selected to be used for the intended application. However, one should consider that using the ARC layer in CMOS-based structures requires additional process sequences to remove the thick dielectric stack on top of the sensitive area and to deposit the ARC layer instead. Therefore, it imposes additional costs and, in addition, can have undesirable effects (defects at the interface) on the silicon surface.

5. CONCLUSION

The PDP of SPADs can be improved by replacing the isolation and the passivation stack by an ARC above the sensitive area in CMOS technology, where the ARC is available. An experimental and simulation study is presented to evaluate the effects of the ARC layer on the PDP performance in CMOS SPADs. It is shown that by using an ARC layer optimized for shorter wavelengths in the visible range, the PDP is enhanced at wavelengths below ~600 nm, due to the improvement in photon transmission and the absorption profile within the silicon. In addition, the optimized ARC layer thickness that leads to maximum PDP enhancement at different wavelengths over the visible spectrum is extracted, which helps the designer select an effective ARC layer in CMOS technologies where different ARC types are available.

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Data Availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

REFERENCES

1. S. Huang, S. M. Patanwala, J. Kosman, R. K. Henderson, and M. Safari, "Optimal photon counting receiver for sub-dead-time signal transmission," J. Lightwave Technol. **38**, 5225–5235 (2020).
2. M. Widarsson, M. Henriksson, P. Mutter, C. Canalias, V. Pasiskevicius, and F. Laurell, "High resolution and sensitivity up-conversion mid-infrared photon-counting LIDAR," Appl. Opt. **59**, 2365–2369 (2020).
3. C.-M. Tsai and Y.-C. Liu, "Anti-interference single-photon LiDAR using stochastic pulse position modulation," Opt. Lett. **45**, 439–442 (2020).
4. P. W. Connolly, X. Ren, A. McCarthy, H. Mai, F. Villa, A. J. Waddie, M. R. Taghizadeh, A. Tosi, F. Zappa, R. K. Henderson, and G. S. Buller, "High concentration factor diffractive microlenses integrated with CMOS single-photon avalanche diode detector arrays for fill-factor improvement," Appl. Opt. **59**, 4488–4498 (2020).
5. A. Ghezzi, A. Farina, A. Bassi, G. Valentini, I. Labanca, G. Acconcia, I. Rech, and C. D'Andrea, "Multispectral compressive fluorescence lifetime imaging microscopy with a SPAD array detector," Opt. Lett. **46**, 1353–1356 (2021).
6. J. Jiang, A. D. C. Mata, S. Lindner, E. Charbon, M. Wolf, and A. Kalyanov, "Dynamic time domain near-infrared optical tomography based on a SPAD camera," Biomed. Opt. Express **11**, 5470–5477 (2020).
7. C. Bruschini, H. Homulle, I. M. Antolovic, S. Burri, and E. Charbon, "Single-photon avalanche diode imagers in biophotonics: review and outlook," Light Sci. Appl. **8**, 87 (2019).
8. R. K. Henderson, N. Johnston, F. M. Della Rocca, H. Chen, D. D.-U. Li, G. Hungerford, R. Hirsch, D. McLoskey, P. Yip, and D. J. Birch, "A 192×128 time correlated SPAD image sensor in 40-nm CMOS technology," IEEE J. Solid-State Circuits **54**, 1907–1916 (2019).
9. G. Gallina, F. Retière, P. Giampa, J. Kroeger, P. Margetak, S. B. Mamahit, A. D. S. Croix, F. Edaltafar, L. Martin, N. Massacret, M. Ward, and G. Zhang, "Characterization of SiPM avalanche triggering probabilities," IEEE Trans. Electron Devices **66**, 4228–4234 (2019).
10. Y. Xu, P. Xiang, X. Xie, and Y. Huang, "A new modeling and simulation method for important statistical performance prediction of single photon avalanche diode detectors," Semicond. Sci. Technol. **31**, 065024 (2016).
11. M. Mazzillo, A. Piazza, G. Condorelli, D. Sanfilippo, G. Fallica, S. Billotta, M. Belluso, G. Bonanno, L. Cosentino, A. Pappalardo, and P. Finocchiaro, "Quantum detection efficiency in geiger mode avalanche photodiodes," IEEE Trans. Nucl. Sci. **55**, 3620–3625 (2008).
12. C.-A. Hsieh, C.-M. Tsai, B.-Y. Tsui, B.-J. Hsiao, and S.-D. Lin, "Photon-detection-probability simulation method for CMOS single-photon avalanche diodes," Sensors **20**, 436 (2020).
13. M. Hofbauer, B. Steindl, K. Schneider-Hornstein, and H. Zimmermann, "Performance of high-voltage CMOS single-photon avalanche diodes with and without well-modulation technique," Opt. Eng. **59**, 040502 (2020).
14. D. Shin, B. Park, Y. Chae, and I. Yun, "The effect of a deep virtual guard ring on the device characteristics of silicon single photon

avalanche diodes," IEEE Trans. Electron Devices **66**, 2986–2991 (2019).
15. H. Zimmermann, B. Steindl, M. Hofbauer, and R. Enne, "Integrated fiber optical receiver reducing the gap to the quantum limit," Sci. Rep. **7**, 2652 (2017).
16. F. Acerbi and S. Gundacker, "Understanding and simulating SiPMs," Nucl. Instrum. Methods Phys. Res. A **926**, 16–35 (2019).
17. X. Lu, M.-K. Law, Y. Jiang, X. Zhao, P.-I. Mak, and R. P. Martins, "A 4-μm diameter SPAD using less-doped n-well guard ring in baseline 65-nm CMOS," IEEE Trans. Electron Devices **67**, 2223–2225 (2020).
18. H. Mahmoudi, S. S. K. Poushi, B. Steindl, M. Hofbauer, and H. Zimmermann, "Optical and electrical characterization and modeling of photon detection probability in CMOS single-photon avalanche diodes," IEEE Sens. J. **21**, 7572–7580 (2021).
19. B. Steindl, R. Enne, S. Schidl, and H. Zimmermann, "Linear mode avalanche photodiode with high responsivity integrated in high-voltage CMOS," IEEE Electron Device Lett. **35**, 897–899 (2014).
20. R. Enne, B. Steindl, M. Hofbauer, and H. Zimmermann, "Fast cascoded quenching circuit for decreasing afterpulsing effects in 0.35-μm CMOS," IEEE Solid-State Circuits Lett. **1**, 62–65 (2018).
21. Silvaco International, Atlas manual, https://www.silvaco.com.
22. CST User's Manual, https://www.3ds.com.
23. F. E. Thorburn, L. L. Huddleston, J. Kirdoda, R. W. Millar, L. Ferre-Llin, X. Yi, D. J. Paul, and G. S. Buller, "High efficiency planar geometry germanium-on-silicon single-photon avalanche diode detectors," Proc. SPIE **11386**, 113860N (2020).
24. C. Crews, M. Soman, D. Lofthouse-Smith, E. Allanwood, K. Stefanov, M. Leese, P. Turner, and A. Holland, "Predicting the effect of radiation damage on dark current in a space-qualified high performance CMOS image sensor," J. Instrum. **14**, C11008 (2019).
25. Y. Wang, X. Cheng, Z. Lin, C. Zhang, H. Xiao, F. Zhang, and S. Zou, "Analysis of IBAD silicon oxynitride film for anti-reflection coating application," J. Non-Cryst. Solids **333**, 296–300 (2004).
26. P. Jerram, D. Burt, N. Guyatt, V. Hibon, J. Vaillant, and Y. Henrion, "Back-thinned CMOS sensor optimization," Proc. SPIE **7598**, 759813 (2010).
27. Y. Matsuoka, S. Mathonnèire, S. Peters, and W. T. Masselink, "Broadband multilayer anti-reflection coating for mid-infrared range from 7 μm to 12 μm," Appl. Opt. **57**, 1645–1649 (2018).

2.2 Experimental and simulation study of fill-factor enhancement using a virtual guard ring in n^+/p-well CMOS single-photon avalanche diodes, "Optical Engineering 2021"

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Experimental and simulation study of fill-factor enhancement using a virtual guard ring in n^+/p-well CMOS single-photon avalanche diodes

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Abstract. The use of a physical guard ring in CMOS single-photon avalanche diodes (SPADs) based on n^+/(deep)p-well and p^+/(deep)n-well structures is a common solution to control the electric field of the SPADs periphery and prevent the premature lateral breakdown. However, this leads to a decrease of the detection efficiency, i.e., the fill-factor, especially when the SPADs size is reduced. Our paper presents an experimental and simulation study on replacing the physical guard ring by a virtual guard ring to improve the fill-factor and the scalability of a n^+/p-well SPAD implemented in 0.35-μm pin-photodiode CMOS technology. Accordingly, the optimization of the virtual guard ring and its superiority at downscaling are discussed, and the SPAD scalability in size with respect to the fill-factor is quantified in this technology. [DOI: 10.1117/1.OE.60.6.067105]

Keywords: single-photon avalanche diode; virtual guard ring; scalability; fill-factor.

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1 Introduction

Detecting weak optical signals is critical to a variety of opto-electronic applications, including time-of-flight sensors, quantum cryptography, optical wireless communication, and optical tomography in medical diagnostics. This makes the single-photon avalanche diode (SPAD) an attractive candidate as it has a sensitivity level of detecting single photons.[1–4] The SPAD operation can be thought as a simple diode with a reverse bias above its breakdown voltage and therefore, an absorbed photon generates an electron–hole pair, which might gain enough energy to create a self-sustaining avalanche due to a strong electric field formed in a multiplication zone. The self-sustaining avalanche has to be stopped by reducing the voltage to below breakdown by a quenching circuit (active or passive) and then needs to be recovered (reset) for the next detection.

Si-CMOS SPADs based on n^+/(deep)p-well and p^+/(deep)n-well are commonly used structures with the capability to be integrated with circuitry.[5–8] In these structures, a physical guard ring was used to avoid a premature edge breakdown due to locally concentrated electric field at the edge of the junction. A variety of different physical guard rings, including diffusion guard ring,[9] trench isolation guard ring (STI),[10] and low-doped guard ring,[11,12] have been used to decrease the peripheral electric field at the edge of the junction. Nevertheless, the existence of the physical guard ring degrades the fill-factor defined as the ratio of the photo-sensitive area (active area) to the total device area. As it is shown here, this degradation is more significant when the SPAD is downsized and the dimensions of the guard ring are comparable to the dimensions of the photo-sensitive area.

To address this issue, a virtual guard ring has been employed in p^+/n-well SAPDs to achieve smaller structures.[13–16] In Refs. 13 and 16, the virtual guard ring is exploited between active area and STI to separate the edge of the STI from the avalanche region to reduce the dark count rate

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(DCR) induced by STI interface traps, which limits the fill-factor. However, in SPADs with a deep multiplication region, the combination of the virtual guard ring and STI is efficient in downsizing the SPAD as studied in Refs. 15, 17, and 18. Reference 19 presents different deep virtual guard ring structures to be used in SPADs with a deeper multiplication region in p^+/deep n-well CMOS SPADs. Here, we employ this concept in the n^+/p-well CMOS SPAD structure with separate thick absorption and multiplication zones, which is efficient for longer wavelengths for the first time. The effect of a virtual guard ring replacing a physical guard ring on the built-in electric field and the fill-factor of the SPAD is studied. Furthermore, we demonstrate that the lateral electric field at the edge of the active area decreases the effective active area due to the deviation of the carrier path from their pure vertical trajectory toward the boundary out of the multiplication region. To the best of our knowledge, the previous studies have not considered this effect; however, it is critical in scaling down our SPAD. Here, the Geiger mode simulation is performed to investigate the electric field behavior inside the structure and evaluate the effective active area. Furthermore, we measure experimentally the radial dependency of the photon detection probability (PDP) defined as the probability that an incident photon is detected to determine the active area (i.e., the fill-factor). In addition, the effect of the virtual guard ring on the parasitic noises, including the DCR and afterpulsing probability (APP), and the breakdown voltage (V_{br}) as the key performance factors of the SPAD are studied.

A good agreement between the simulation and the experimental results is achieved for large SPADs of both structures. Then, the structure of a smaller SPAD with a virtual guard ring within the same CMOS technology is designed based on simulations and is fabricated, accordingly.

The remainder of the paper is organized as follows. In Sec. 2, the structure of the SPAD with physical and virtual guard rings is described. Section 3 compares the simulation and experimental results for larger SPAD structures of both guard ring types. Section 4 studies the downscaling effect on the fill-factor for both SPAD structures and finally, the paper is concluded in Sec. 5.

2 Device Structure and Measurement Setup

2.1 *Device Structure*

Figure 1 shows the cross-sections and the top view of the circular SPAD structures fabricated in the 0.35-μm modular sensor technology platform (XO035) of X-FAB semiconductor foundries. Both SPADs include a shallow n^+ and p-well regions formed on a p-doped epitaxial layer (p-epi) with a doping concentration of $\sim 2 \times 10^{13}$ $1/\text{cm}^3$ and a thickness of ~ 12 μm. In both structures, the diameter of the n^+ and p-well are 90 and 80 μm, respectively.

When the SPAD is reversely biased above its breakdown voltage (operating in Geiger mode), a strong electric field is established at the n^+/p-well junction that serves as an avalanche

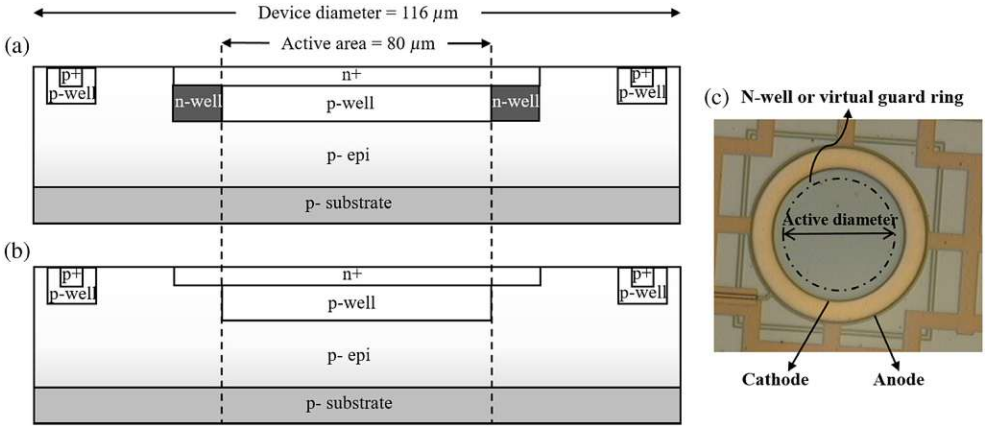

Fig. 1 Schematic cross-section (not to scale) of CMOS SPADs based on n^+/p-well structure with (a) the physical guard ring (SPAD1) and (b) the virtual guard ring (SPAD2). (c) Top view of these SPADs (there is no difference in the chip photos of both SPADs visible).

multiplication zone. At this voltage level, the depletion region extends down to the substrate, which means the whole epitaxial layer is depleted. Accordingly, the p-epi layer serves as a thick absorption zone, which makes the SPADs efficient to detect long wavelengths to be used in optical wireless communication systems and LIDAR/ToF sensor applications.

The only difference between these two SPAD structures is the form of the guard ring, which is necessary to avoid the curvature effect of the p–n junction and the formation of higher electric field at the edges resulting in a local edge breakdown. In SPAD1 [Fig. 1(a)], an n-well region (which is much lower doped than the n+ region) with a width of ~5 μm (here, after called physical guard ring) is present from the edge of the p-well to the edge of the n^+ region as it has been used in our previous SPADs.[3,20] In SPAD2 [Fig. 1(b)], the guard ring is made virtually as the diameter of p-well is less than that of the n^+ region so that the edge of n^+ region is surrounded by the low doped p-epi. Therefore, the electric field at the diode junction of n^+/p-well in the central region (including, the whole p-well) is higher than the peripheral electric field at the edges, and accordingly the central region reaches the breakdown voltage point earlier. As a result, the edge breakdown is avoided and the multiplication region is confined over the n^+/p-well junction. However, the use of these guard rings influences the built-in electric field and reduces the effective active area. A closer look into this effect using TCAD simulations and experimental measurements is presented in the following section.

2.2 *Measurement Setup*

The measurement setup is illustrated in Fig. 2. As laser source, a fiber coupled to a laser diode from Thorlabs is used (LPS-PM635-FC). We use two optical power meters in our setup. A fiber splitter is used to split up the light to feed it to the first optical power meter from Thorlabs for power monitoring (PM_{ref}) and to the fiber that feeds the light either to the device under test (DUT) or to the detector of a second power meter PM_{cal}. With attenuator Att2, the ratio between the optical power is set between the fiber that feeds the light to the DUT and the fiber that leads to the power monitoring. This ratio is set in the range of 10^5. For calibrating this ratio, the second power meter PM_{cal} is used that has a detector placed inside the dark box where the DUT is mounted. This high ratio guarantees that we get sufficient optical power at the power monitoring, when the photon rate at the DUT is set to 10×10^6 photons/s. Attenuator Att1 is used after calibrating the power ratio to reduce the photon rate at the SPAD. This light intensity is sufficiently low that any saturation and pile up effects are not observed. The setup is controlled by a PXI system. A digitizer (NI PXIe-5162) reads the output signals of the active quenching circuit (explained in detail in Ref. 20) and streams the data directly to an FPGA card (NI PXIe-7972R),

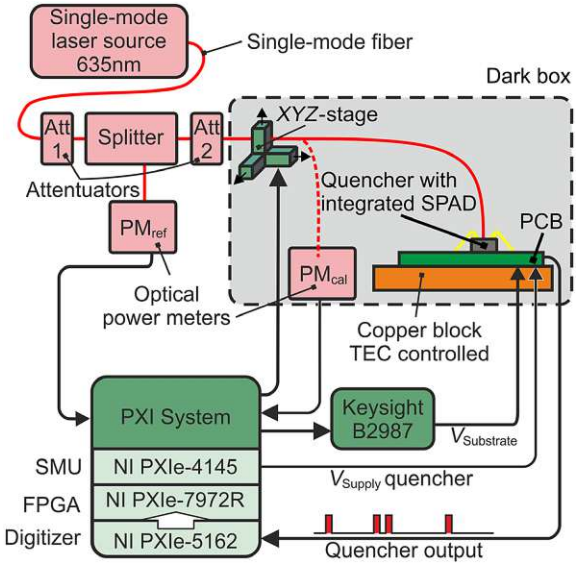

Fig. 2 Schematic of the measurement setup.

where the pulse statistics such as count rate and after pulsing probability are extracted. The active quenching circuit is supplied by an SMU card (NI PXIe-4145), and the substrate voltage is generated by a Keysight electrometer (B2987). The DUT's temperature is kept constant at 25°C by means of a thermo electric cooler. An XYZ-stage from Thorlabs built from three linear stages (KMTS50E/M) positions the fiber over the DUT and performs the XY sweep. The minimum achievable incremental movement corresponds to 50 nm and the bidirectional repeatability is 1.6 μm.

3 Comparison of Simulation and Experimental Results

To investigate the effect of the guard ring on the distribution of the electric field inside the SPAD, TCAD simulations are performed for both SPADs structures shown in Fig. 1. The structures are defined based on the SPADs' layouts and the process design kit information as well as the doping profiles (confidential data) provided by the foundry, and according to the cylindrically symmetric geometry of the SPADs, two-dimensional (2D) simulations are carried out along one diameter. The key parameters and the corresponding values used in the TCAD simulations are shown in Table 1.

Figure 3 shows the built-in electric field at an excess bias voltage of 6.6 V obtained by using the Geiger mode device simulation feature of SILVACO Atlas.[22] The 2D plots of the electric field distribution inside the two structures with the physical and virtual guard rings are shown in Figs. 3(a) and 3(b), respectively. Both SPADs show a similar electric filed profile (direction and strength) in the central area where the guard ring has no influence on the electric field. Therefore, in both structures, a vertical electric field [along the direction x as shown in Fig. 2(c)] is formed at the center of the device ($r = 0$) with a very high strength (700 kV/cm) at the interface of n^+/p-well (multiplication region) and a lower amplitude (8 kV/cm) over the depletion region (i.e., absorption region), which extends down to the substrate. As a result, when a photon is absorbed in the depletion region, the generated electron and the hole are promptly separated by the electric field (in opposite directions) and then, the minority carrier is accelerated toward the multiplication region.

Inside the multiplication zone, the strength of the electric field is significantly reduced when moving away from A toward the guard rings as is shown in Fig. 3(d). As a result, the avalanche multiplication region is limited to the junction of n^+/p-well where the electric field is very high and surrounded by the guard ring, and thus, the edge breakdown is avoided at the cost of a reduced active area. It can be seen from a lateral cross-section of the electric field through $A - A'$ ($x = 0.5$ μm), the high-electric field in SPAD1 starts falling down (at ~37 μm) earlier than in SPAD2 (at ~39 μm), which makes the multiplication region smaller. In addition, the r-component (i.e., the lateral component) of the electric field at the edge (i.e., the end of p-well)

Table 1 Key parameters used in the TCAD simulation performed by ATLAS.

Parameter	Discription	Value
An	Impact ionization constants for electron[21]	7.03×10^5 1/cm
En_crit		1.231×10^6 V/cm
Ap	Impact ionization constants for hole[21]	1.58×10^6 1/cm
Ep_crit		2.036×10^6 V/cm
taun	Electron life time	200 μs
taup	Hole life time	200 μs
L_e	Electron diffusion length	270 μm
L_h	Hole diffusion length	90 μm

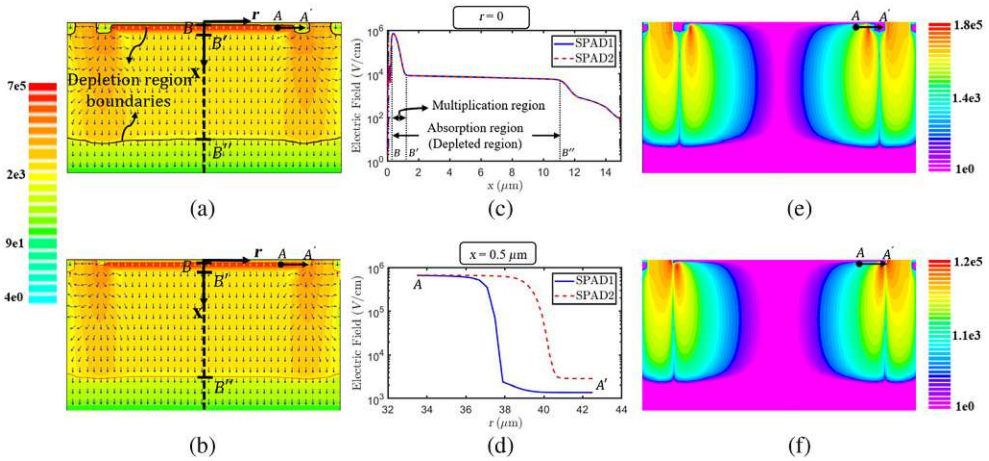

Fig. 3 2D plots of the electric field obtained by TCAD simulation for (a) SPAD1 and (b) SPAD2 in logarithmic scale. Arrows indicate the local electric field direction. (c) A vertical cross-section of the electric field at the center ($r = 0$) for both SPAD1 and SPAD2. (d) A lateral cross-section of the electric field through A–A' at $x = 0.5$ μm in SPAD1 and SPAD2. 2D plots of the r-component of the electric field for (e) SPAD1 and (f) SPAD2 in logarithmic scale.

grows due to the formation of a lateral p-well/n-well junction and a p-well/p-epi transition in SPAD1 and SPAD2, respectively, as shown in Figs. 3(e) and 3(f). As a result, the carriers photo-generated at the border of the active area [below A–A', see also Figs. 3(a) and 3(b)] are exposed to a non-vertical electric field, which deviates the generated minority carriers (i.e., the electrons) from their pure vertical trajectory toward the lower-electric field region (out of the multiplication region). Therefore, the active area covers a smaller area as compared to the area covered by the n^+/p-well junction in the layout and can be named as the effective active area in contrast to the physical active area defined by the layout dimensions.

To visualize the effective active area inside these structures, the avalanche triggering probability (ATP) is obtained by TCAD simulation. ATP is defined as the probability that either a photo-generated electron or a hole (as two independent events) at a position x initiates a self-sustaining avalanche event, depending on the impact ionization coefficients and the electric field. More details and how ATP leads to PDP are explained in our recent paper.[23] Figure 4 illustrates a 2D plot of the ATP for both structures. Here, in spite of the fact that the avalanche process happens only in the multiplication region, a carrier generated outside the multiplication region can reach this area and trigger an avalanche event. Therefore, the ATP corresponding to the avalanche triggering probability (for a self-sustaining avalanche) of the minority carries (i.e., electrons) below the multiplication zone extends to the p-well and p-epi regions and shows a maximum value (at the central region). In fact, it shows a fixed (maximum) value over this region ($r < 20.5$ μm and $r < 27.5$ μm, respectively) as we can assume a negligible recombination rate due to a strong drift toward the multiplication region. This means that an electron generated at any x ($r < 20.5$ μm and $r < 27.5$ μm, respectively) drifts toward the cathode and will flow through the whole multiplication region. Similarly, for the area above the multiplication region (n^+ layer), a minority carrier (i.e., a hole) can reach the multiplication region and trigger an avalanche event.

Figure 4 demonstrates that a larger effective active area is obtained with the virtual guard ring compared to the physical guard ring. The difference between the radii of the effective active areas in the two structures is larger than the ~2 to 3 μm predicted by Fig. 3(d) and is around 7 μm. This is due to the lateral electric field from the lateral diode (p-well/n-well) in SPAD1, which is stronger than that of the p-well/p-epi transition in SPAD2, and therefore, it has a stronger effect on the trajectory of the carriers toward the cathode and results in a narrower region with a high ATP. This proves an improvement of around 45% and accordingly, for the same diameter of 116 μm the fill-factors of 23% and 34% are obtained for SPAD1 and SPAD2 leading to the photon detection efficiencies (PDEs, PDE = PDP times fill-factor) of 7.75% and 11.46%, respectively.

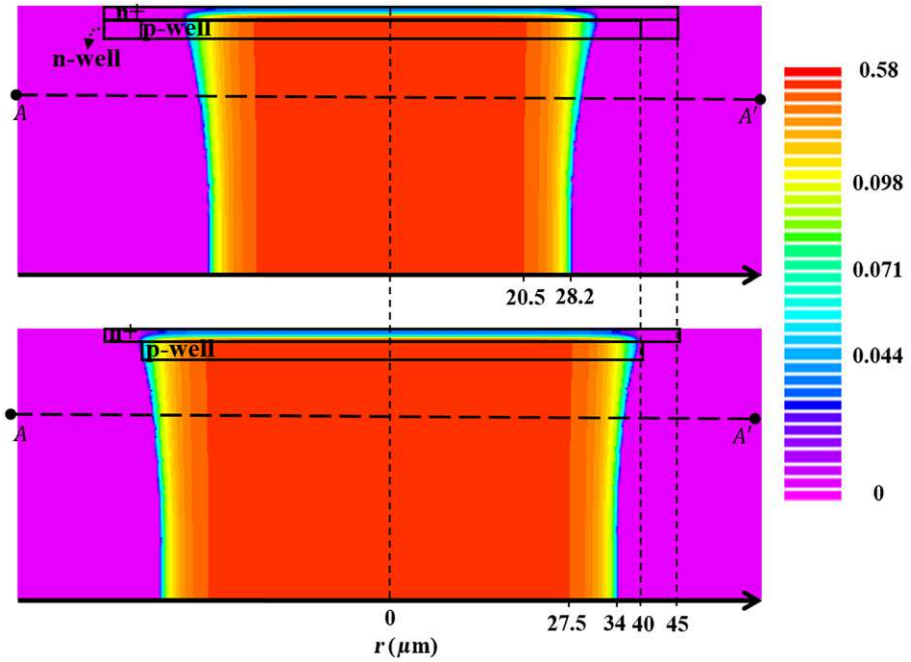

Fig. 4 2D plots of the ATP at an excess bias voltage of 6.6 V for (a) SPAD1 and (b) SPAD2.

To experimentally characterize the effective active area, the radial dependency of the PDP is measured at a wavelength of 635 nm. Figure 5(a) shows the measured PDPs for both structures as a function of the distance between the center of the SPAD and the center of the light source. Furthermore, ATPs (1D cross-section at $x = 5$ μm) obtained by simulation are added to this figure. It is worth mentioning that the ATP is independent of the wavelength; however, here we plot it for a cross-section depth equal to the penetration depth (σ) at $\lambda = 635$ nm. In fact, σ is a function of λ and defines the depth at which the optical power decays to $1/e$ of its value at the silicon surface. The result verifies the expected difference between the diameters of the effective active area of the two structures predicted by the simulation. Furthermore, the PDP curves show a smaller slope to zero as compared to the ATP curves because due to the actual beam widths the PDP is averaged over the light spot on the SPAD.

Figure 5(b) shows the reverse current in dependence on reverse voltage [i.e., the $I(V)$ curves] for SPAD1 and SPAD2. As it is shown, the breakdown voltage of SPAD1 is lower than that of SPAD2, which originates from the difference in the electric field distribution in the two SPADs. Table 2 shows a comparison of the parasitic noises at an excess bias of 6.6 V and of the breakdown voltages of SPAD1 and SPAD2. The breakdown voltage is read as the reverse voltage for a

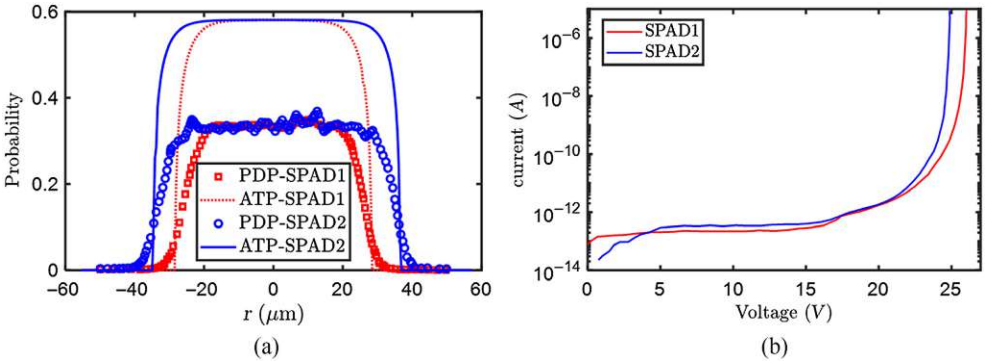

Fig. 5 (a) Measured radial PDPs and simulated 1D cross-sections of the ATP at an excess bias voltage of 6.6 V. (b) Measured $I(V)$ curves.

Table 2 Parasitic noise, breakdown voltage, and the PDE comparison of SPAD1 and SPAD2 at an excess bias of 6.6 V.

SPADs	DCR	APP	V_{br}	PDE
SPAD1	30.43 kcps	4.25%	25.8 V	7.75%
SPAD2	31.14 kcps	5.29%	24.9 V	11.46%

reverse current of 10 μA. It can be seen that the DCR and APP of SPAD2 are slightly higher than that of SPAD1, which is due to the fact that SPAD2 has a larger effective active area compared to SPAD1. Therefore, one can say that employing the virtual guard ring in this structure is efficient to improve the fill-factor while retaining its efficiency from the other performance factors point of view.

4 SPAD Scalability with the Virtual Guard Ring

Maintaining the overall sensitivity and providing an acceptable fill-factor is a challenge when the SPAD is scaled-down. Therefore, the fill-factor enhancement using the virtual guard ring becomes more significant in smaller SPADs. Here, we study the effect of the guard ring on the fill-factor of a SPAD with a diameter of 48 μm and the n^+ diameter of 30 μm. To achieve a higher fill-factor, the width of the virtual guard ring has to be minimized that the fill-factor is maximized but still the edge breakdown is not happening. According to the design rules and the doping profiles associated with the 0.35-μm CMOS technology, we have obtained a minimum width of around 1 μm for the virtual guard ring using TCAD simulations. In fact, if the width of the virtual guard ring (i.e., the radius of the n^+ minus the radius of the p-well) is smaller than 1 μm, the electric filed at the edges will be higher than in the center and as a result, the breakdown occurs at the edge area at a smaller reverse bias voltage and only the edge area of the diode will contribute to the SPAD operation in Geiger mode. Figure 6 shows this effect for a virtual guard ring of 0.5 μm where the active area is limited to the edges.

Now, we compare the smaller SPAD (device diameter = 48 μm, n^+ diameter = 30 μm) with the physical guard ring (p-well diameter = 20 μm, n-well width = 5 μm) to the SPAD with the minimized virtual guard ring (p-well diameter = 28 μm, guard ring width = 1 μm), using TCAD simulations as shown in Fig. 7. It can be seen that the effective active area of the SPAD with the physical guard ring is severely degraded and shows a fill-factor of less than 1%, which is not suitable for practical applications. On the other hand, the SPAD with the virtual guard ring retains its efficiency and provides a much higher fill-factor of around 22% (the radius of the effective active area is 11.3 μm at the cross section of A–A') leading to a PDE of 7.5%, which can be acceptable for many applications. According to these results, only the SPAD structure with a diameter of 48 μm and the virtual guard ring of 1 μm was fabricated in 0.35-μm OPTO-ASIC CMOS technology. This SPAD was characterized through a similar experiment as it was explained above. Its measured radial PDP at a wavelength of 770 nm and its measured

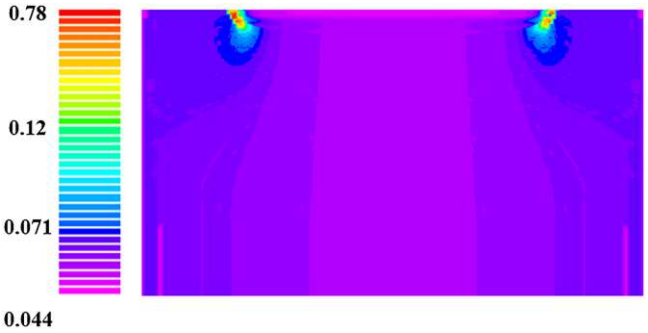

Fig. 6 2D plot of the ATP for the SPAD with a 0.5-μm virtual guard ring.

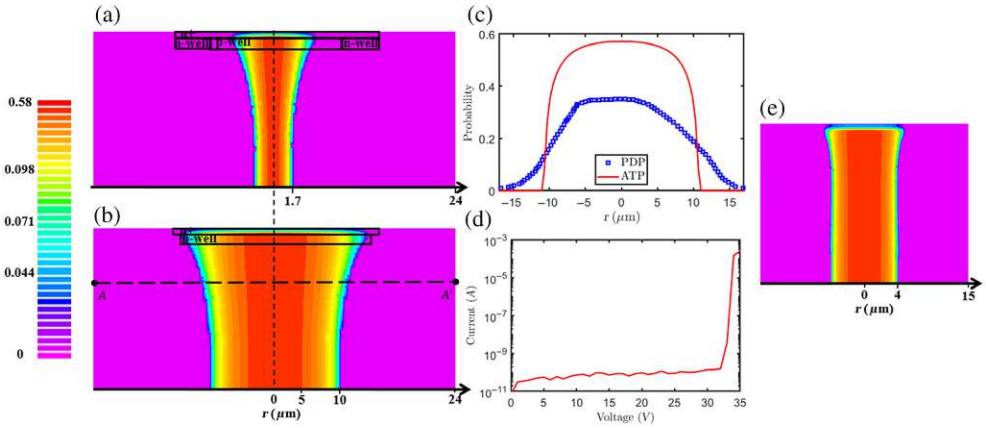

Fig. 7 2D plots of the ATP for the SPADs with a diameter of 48 μm and (a) the physical guard ring, (b) the virtual guard ring at an excess bias voltage of 6.6 V. (c) The measured radial PDP and a 1D cross-section of the ATP of the SPAD with the virtual guard ring at the depth of 5 μm and at an excess bias voltage of 6.6 V. (d) Measured $I(V)$ curve of the SPAD with the virtual guard ring. (e) A 2D plot of the ATP for a 1-μm-virtual-guard-ring SPAD with a diameter of 30 μm (n^+ diameter = 15 μm).

$I(V)$ curve are shown in Figs. 7(c) and 7(d), respectively. This SPAD is from a different process run and its breakdown voltage cannot be compared to those of SPAD1 and SPAD2. For this SPAD at an excess bias of 6.6 V, DCR and APP are 7.5 kcps and 14.2%, respectively. Figure 7(c) shows a comparison of the measured radial PDP and the simulated profile of the ATP at a depth of 5 μm [over A–A' as shown in Fig. 7(b)]. As it is mentioned above, the PDP curve decreases with a smaller slope compared to the ATP curve due to the fact that the measured PDP at each point is an average over the light spot on the SPAD. Here, a single-mode fiber with a core diameter of 8 μm was used for scanning the SPAD, which shows a larger difference between PDP and ATP compared to the result in Fig. 5(a).

To further investigate the scalability of the SPAD structure with virtual guard ring in the available 0.35-μm CMOS technology, we obtain the ATP for a structure with a diameter of 30 μm using TCAD simulations as is shown in Fig. 7(e). This result suggests that, at this size, it is possible to achieve a fill-factor of around 7%, which is not appropriate for application where high sensitivity is critical, e.g., optical receivers based on an array of a few SPADs. However, one may still consider this as an acceptable fill-factor for other applications, where large arrays consisting of hundreds or thousands of SPADs are used and the fill-factor is more critical. Table 3 shows a comparison of the key performance parameters of the SPAD in this work with those of previously published SPADs to better highlight the contribution of this work over the state of the art.

Table 3 Performance comparison of the implemented SPAD with literature.

SPADs	PDP at $\lambda = 635$ nm	DCR (cps/μm^2)	Diameter	Fabrication process
Ref. 15	7.2% at $V_{ex} = 2$ V	73 at $V_{ex} = 2$ V	4 μm	CMOS 65 nm
Ref. 16	10% at $V_{ex} = 3$ V	4.7 at $V_{ex} = 3$ V	30 μm	CMOS 180 nm
Ref. 19	9% at $V_{ex} = 5$ V	8.8 at $V_{ex} = 5$ V	15 μm	—
Ref. 24	15% at $V_{ex} = 4$ V	16 at $V_{ex} = 4$ V	12 μm	CMOS 180 nm
Ref. 25	15% at $V_{ex} = 4$ V	2 at $V_{ex} = 4$ V	20.4 μm	CMOS 180 nm
Ref. 26	7% at $V_{ex} = 11$ V	1.5 at $V_{ex} = 11$ V	—	CMOS 180 nm
This work	35% at $V_{ex} = 6.6$ V	3.2 at $V_{ex} = 6.6$ V	48 μm	CMOS 350 nm

To compare the performance of different SPADs, one should consider many parameters including the technology in which the SPAD is implemented, the size of the SPAD, and the measurement conditions. Nevertheless, as the SPAD presented in this paper is designed to be used for optical fiber receiver applications, its PDP is significantly larger than that of the other published results. To have an understandable DCR comparison, we should normalize the DCR by the SPADs' area. It is shown that the DCR/μm^2 of the presented SPAD is comparable with the other published results. Table 3 also includes the diameter of the SPADs to provide an insight into the size of the SPADs reported in literature. It is worth noting that the availability of doping profiles and the design rule limitations of the fabrication process play a key role in the scalability of SPADs. It is clear that advanced, smaller-node technologies offer higher scalability features. In addition, in technologies where higher doping concentrations are available, smaller structures can be fabricated. However, comparison of the scalability of different technologies is out of the scope of this work. According to our result, in the same technology using the same doping profiles, replacing the physical guard ring by the virtual guard ring can improve the effective fill-factor of the SPAD.

5 Conclusion

The use of a virtual guard ring is a practical solution to avoid the edge breakdown effect in SPAD devices and still preserve the fill-factor as an important performance metric. An experimental and simulation study on the effect of the virtual guard ring on the fill-factor and the scalability of a n+/p-well SPAD implemented in 0.35-μm CMOS technology is presented. A minimum guard ring width of 1 μm is obtained using TCAD simulation and is used to design smaller SPADs in this CMOS technology. A fill-factor of around 22% is achieved for a SPAD with a diameter of 48 μm, and it is shown that the fill-factor decreases to below 7% for a SPAD with the diameter less than 30 μm. We believe that higher fill-factors at smaller SPAD sizes are achievable only in more advanced CMOS technologies where doping concentrations are higher.

Acknowledgments

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References

1. J. Huikari et al., "Compact laser radar based on a subnanosecond laser diode transmitter and a two-dimensional CMOS single-photon receiver," *Opt. Eng.* **57**(2), 024104 (2018).
2. M. Gramegna et al., "European coordinated metrological effort for quantum cryptography," *Proc. SPIE* **10674**, 106741K (2018).
3. H. Zimmermann et al., "Integrated fiber optical receiver reducing the gap to the quantum limit," *Sci. Rep.* **7**(1), 2652 (2017).
4. C. Bruschini et al., "Single-photon avalanche diode imagers in biophotonics: review and outlook," *Light Sci. Appl.* **8**(1), 1–28 (2019).
5. M. Hofbauer et al., "Performance of high-voltage CMOS single-photon avalanche diodes with and without well-modulation technique," *Opt. Eng.* **59**(4), 040502 (2020).
6. I. I. Izhnin et al., "Single-photon avalanche diode detectors based on group IV materials," *Appl. Nanosci.*, 1–11 (2021).
7. W. Wang, Y. Zhang, and Z. Wei, "High-performance structure of guard ring in avalanche diode for single photon detection," *Int. J. Commun. Network Syst. Sci.* **10**(8), 1–6 (2017).
8. B. Steindl, R. Enne, and H. Zimmermann, "Thick detection zone single-photon avalanche diode fabricated in 0.35 μm complementary metal-oxide semiconductors," *Opt. Eng.* **54**(5), 050503 (2015).
9. J. A. Richardson et al., "Scaleable single-photon avalanche diode structures in nanometer CMOS technology," *IEEE Trans. Electron Devices* **58**(7), 2028–2035 (2011).

10. H. Finkelstein, M. J. Hsu, and S. C. Esener, "STI-bounded single-photon avalanche diode in a deep-submicrometer CMOS technology," *IEEE Electron Device Lett.* **27**(11), 887–889 (2006).
11. I. S. Alirezaei, N. Andre, and D. Flandre, "Enhanced ultraviolet avalanche photodiode with 640-nm-thin silicon body based on SOI technology," *IEEE Trans. Electron Devices* **67**(11), 4641–4644 (2020).
12. D. Bronzi et al., "SPAD figures of merit for photon-counting, photon-timing, and imaging applications: a review," *IEEE Sens. J.* **16**(1), 3–12 (2016).
13. S. Bose et al., "Parametric study of pn junctions and structures for CMOS-integrated single-photon avalanche diodes," *IEEE Sens. J.* **18**(13), 5291–5299 (2018).
14. T. Leitner et al., "Measurements and simulations of low dark count rate single photon avalanche diode device in a low voltage 180-nm CMOS image sensor technology," *IEEE Trans. Electron Devices* **60**(6), 1982–1988 (2013).
15. X. Lu et al., "A 4-μm diameter SPAD using less-doped n-well guard ring in baseline 65-nm CMOS," *IEEE Trans. Electron Devices* **67**(5), 2223–2225 (2020).
16. D. Han et al., "A scalable single-photon avalanche diode with improved photon detection efficiency and dark count noise," *Optik* **212**, 164692 (2020).
17. D. Shin et al., "The effect of a deep virtual guard ring on the device characteristics of silicon single photon avalanche diodes," *IEEE Trans. Electron Devices* **66**(7), 2986–2991 (2019).
18. J. Rhim et al., "Guard-ring dependence of noise characteristics for single-photon avalanche diodes in a standard CMOS technology," in *IEEE 14th Int. Conf. Group IV Photonics*, IEEE, pp. 155–156 (2017).
19. D. Shin et al., "Model-based guard ring structure guideline for the enhancement of silicon-based single-photon avalanche diode characteristics," *Proc. SPIE* **11285**, 112851O (2020).
20. R. Enne et al., "Fast cascoded quenching circuit for decreasing afterpulsing effects in 0.35-μm CMOS," *IEEE Solid-State Circuits Lett.* **1**(3), 62–65 (2018).
21. R. Van Overstraeten and H. De Man, "Measurement of the ionization rates in diffused silicon pn junctions," *Solid-State Electron.* **13**(5), 583–608 (1970).
22. Silvaco International, "Atlas manual," https://www.silvaco.com.
23. H. Mahmoudi et al., "Optical and electrical characterization and modeling of photon detection probability in CMOS single-photon avalanche diodes," *IEEE Sens. J.* **21**(6), 7572–7580 (2021).
24. C. Veerappan and E. Charbon, "CMOS SPAD based on photo-carrier diffusion achieving PDP > 40% from 440 to 580 nm at 4 V excess bias," *IEEE Photonics Technol. Lett.* **27**(23), 2445–2448 (2015).
25. C. Accarino et al., "Low noise and high photodetection probability SPAD in 180 nm standard CMOS technology," in *IEEE Int. Symp. Circuits and Syst.*, IEEE, pp. 1–4 (2018).
26. C. Veerappan and E. Charbon, "A low dark count pin diode based SPAD in CMOS technology," *IEEE Trans. Electron Devices* **63**(1), 65–71 (2016).

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2.3 CMOS Integrated 32 A/W and 1.6 GHz Avalanche Photodiode Based on Electric Field-Line Crowdin, "IEEE Photonics Technology Letters 2022"

CMOS Integrated 32 A/W and 1.6 GHz Avalanche Photodiode Based on Electric Field-Line Crowding

S. S. Kohneh Poushi, B. Goll, *Member, IEEE*, K. Schneider-Hornstein, M. Hofbauer, *Member, IEEE*, and Horst Zimmermann, *Senior Member, IEEE*

***Abstract*— This letter presents a new Si CMOS linear-mode avalanche photodiode (APD) based on an electric field distribution formed by field-line crowding. In this structure, a spherical avalanching electric field is enforced by field-line crowding due to the curvature of the half-sphere cathode (n-well). The electric field extends radially and, therefore, the entire low-doped epitaxial layer serves as charge collection zone. This APD can provide high responsivity and bandwidth due to its thick absorption zone and drift-based carrier transport. Measurements using a 675 nm laser source at 200 nW optical power show a maximum bandwidth of 1.6 GHz while the responsivity is 32 A/W. In addition, a maximum responsivity of 3.05 × 10^3 A/W at 5 nW optical power is achieved. Due to the high avalanche gain, large bandwidth, and CMOS compatibility without any process modification, this APD is a promising optical detector for many applications.**

***Index Terms*— Avalanche photodiode (APD), field-line crowding, CMOS integrated photodetector, spherical avalanching field.**

I. Introduction

DETECTION of low-power, high-bandwidth optical signals is required in many optical systems such as optical communication, time-of-flight sensing, and biomedical imaging. Due to the inherent gain of linear-mode avalanche photodiodes (APDs), the use of integrated APDs instead of standard pin photodiodes is interesting [1]–[3]. APDs fabricated in a complementary metal-oxide semiconductor (CMOS) technology have the advantages of low production cost and integration capability with electronic circuitry for read-out and signal processing.

Common design approaches towards integrated Si CMOS APDs are based on p^+/n-well [4]–[6] and n^+/p-well [7], [8] junctions. These devices demonstrate inevitably a trade-off between bandwidth and responsivity for the long-wavelength range (i.e. red and near-infrared light). The structures with a thin depleted absorption region provide a high bandwidth due to a shorter drift time of charge carriers. However, the carriers generated underneath the thin absorption region do not contribute to the output current resulting in a low responsivity [9].

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APDs based on the concept of separate absorption and multiplication regions were introduced to provide high responsivity, however, the bandwidth of such structures is generally limited by carrier drift time in a thick absorption zone [10], [11]. In Reference [10] a maximum responsivity of 2.7 × 10^4 A/W for 5-nW optical power at 670 nm, and a maximum bandwidth of 850 MHz (R = 20 A/W) were reported. The speed-optimizing technique of modulation doping was used to improve the bandwidth to 1.25 GHz while maintaining the same responsivity [12]. However, such bandwidth was achieved at a reverse voltage of 115 V with the drawback that the capability of the diode isolation from the circuits on the same chip is not good enough. Reference [13] presented a new structure called current-assisted avalanche photodiode (CA-APD) with separate absorption and multiplication regions. This APD employs two electrodes at the surface with different potentials to create an electric field for drifting the photogenerated electrons in the detection volume towards the central multiplication region. A bandwidth of 275 MHz and 13 A/W responsivity at 830 nm was reported for this APD.

Recently, [14] and [15] introduced an electric field-line crowding based single-photon avalanche photodiode (SPAD) fabricated in a CMOS process. They had to customize, i.e. to modify, the fabrication process to use a shallow n-type implant at the silicon surface between cathode and anode to redistribute the electric field just below the silicon/silicon dioxide interface at the surface of the device. A silicon photomultiplier (SiPM) used also a SPAD exploiting the field-line crowding effect [16]. But transistors cannot be fabricated in the special SiPM detector process.

In this work, we employ the field-line crowding concept to design a new APD fabricated in a standard CMOS process without any process modification. The APD uses a small spherical avalanching n-well/p- epi junction at the center and a thick volume in the p- epitaxial layer with lower electric field around the avalanching region as absorption zone (Fig. 1). This APD achieves a maximum responsivity of 3.05 × 10^3 A/W at 5 nW optical power and a maximum bandwidth of 1.6 GHz (R = 32 A/W) at 200 nW optical power for the wavelength of 675 nm.

II. APD Structure and TCAD Simulation

Fig. 1 shows the structure and doping regions of the APD fabricated in 0.18 μm high-voltage CMOS technology. The cathode comprises an n^+ region with a radius of 0.37 μm embedded in an n-well region with a radius of 0.6 μm.

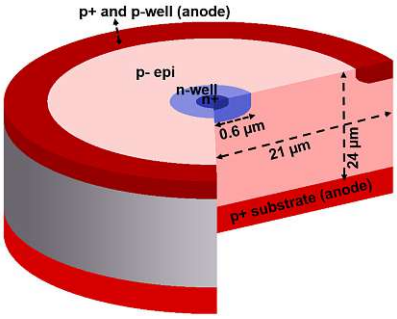

Fig. 1. Schematic 3-D drawing of the n^+/n-well field crowding based Si CMOS APD (not to scale).The APD is covered by an isolation and passivation stack.

The cathode is concentrically enclosed by a p+ region (anode) with an inner radius of 19 μm. These regions are formed on a low p-doped epitaxial layer (p- epi) with a thickness of $\sim$24 μm and a doping concentration of $\sim 1.5 \times 10^{13}$ cm^{-3}. The p+ substrate is also used as anode. The APD is covered by the standard isolation and passivation stack. At the operating voltage, a space-charge region is formed at the junction of the n-well and p- epi region and its electric field distribution can be derived from Gauss's law. The derivation assumes that the highly doped cathode is much smaller than the other device dimensions and that it forms an abrupt transition into the intrinsic layer. Based on these assumptions, the electric field distribution in the p- epi layer is approximately [15]

$$\mathrm{E}(d) \approx \frac{(V_r + V_{bi})d_n}{d^2}, \tag{1}$$

where d_n is the cathode's radius, V_r is the operation voltage, and V_{bi} is the built-in voltage. Accordingly, the electric field peak is at the n-well/p- epi junction and decays by moving radially away from the center at a rate of d^{-2} as can be seen in Fig. 2 (b). At the p-substrate contact ring, i. e. at r = 19 μm, the electric field has still a magnitude of 3500 V/cm. Below the cathode at r = 0 μm just at the transition to the p+ substrate (in a depth of 20 μm), the magnitude of the electric field is still 5 kV/cm. In "diagonal" direction along the dashed line in Fig. 2(a), is still 3 kV/cm at 25 μm away from the origin of coordinates. This high electric field strength enables fast carrier drift from a half sphere with a radius of about 20 μm, whereas the APD of [10] had only an about 8 μm thick drift region [17], which limited the bandwidth by a small contribution of slow carrier diffusion to 850 MHz.

The n-well radius is one of the most important factors in determining the breakdown voltage as the electric field strength depends on the curvature of the n-well/p- epi junction. A smaller cathode radius leads to a sharper field peak. Accordingly, the breakdown and operating voltages decrease by reducing the cathode radius [15], [16].

TCAD simulations were preformed using Silvaco's ATLAS [18] to obtain the electric field distribution inside the structure. When the APD is biased in linear mode (below the breakdown voltage), a spherical high electric field region is formed near the cathode (around n-well region) which acts as the multiplication region. The width of the multiplication region is $\sim$0.9 μm. The electric field extends towards the substrate and towards the surface anode but decreases by moving radially away from the center (Fig. 2(b)). Accordingly, the generated electrons and holes in the entire volume of the epitaxial layer are promptly separated by the electric field, and then the electrons are accelerated in the direction opposite to the electric field vector arrows (Fig. 2(a)) towards the multiplication region (cathode). Such a large thickness of the absorption region and the drift-based carrier transport improve the detector's responsivity and speed performance for long wavelengths, respectively.

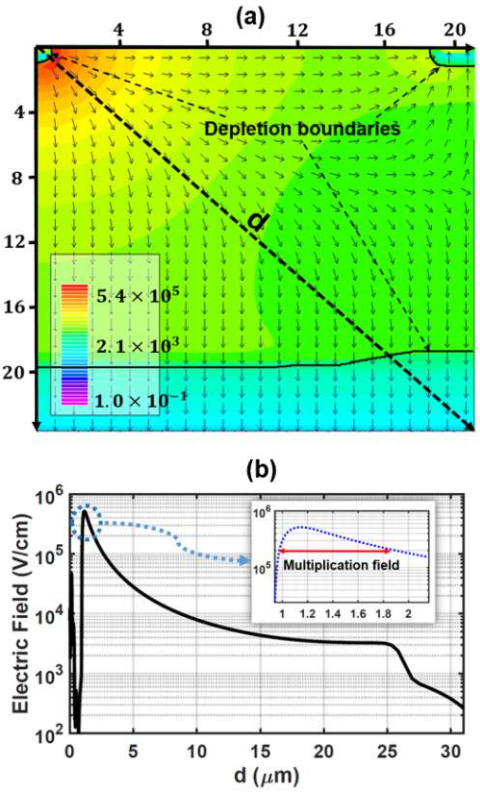

Fig. 2. (a) 2D Plot of the electric field within the APD obtained by TCAD simulations for a reverse voltage of 69 V. Arrows indicate the local electric field direction. (b) Radial cross-section of the electric field in the structure along the dashed line in sub-figure (a).

It is worth mentioning that this APD can be integrated with electronic circuitry on the same silicon chip as the used high voltage CMOS technology provides different wells to isolate the MOS transistors down to substrate potentials of −100 V.

III. Measurement Results

Here the APD is evaluated in terms of some key performance features such as gain, responsivity, and bandwidth. The measurements have been performed on wafer at 25 °C temperature regulated by a thermo chuck.

A. Currents, Gain and Responsivity

Fig. 3 illustrates the dark current and the photocurrent of the APD at different optical powers measured using an electrometer (Keysight B2987A). A 675 nm single-mode fiber with

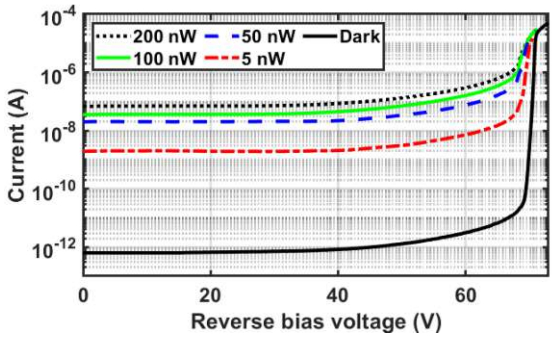

Fig. 3. Measured dark and photo currents as a function of reverse bias voltage for different optical powers (5 nW, 50 nW, 100 nW, 200 nW).

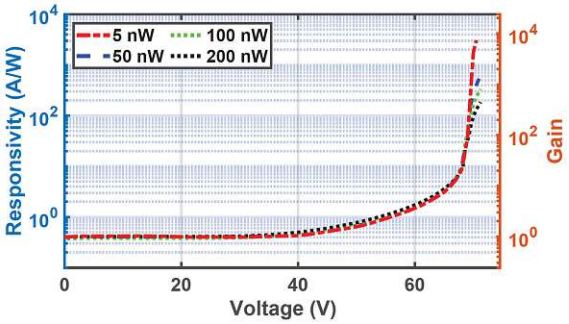

Fig. 4. Responsivity (left) and gain (right) as a function of reverse bias voltage for different optical powers.

a core diameter of 5 μm coupled with an optical attenuator was used to provide different optical power. A calibrated optical power meter was used to measure the optical power on the device under test. The dark characteristics shows the breakdown voltage of 70.7 V where the dark current reaches 1 μA. Based on the photocurrent characteristics, the gain and responsivity as a function of reverse bias voltage are obtained from the following equations:

$$\text{Gain(V)} = \frac{\text{I(V)} - \text{I}_{\text{dark}}\text{(V)}}{\text{I(V}_0\text{)} - \text{I}_{\text{dark}}\text{(V}_0\text{)}}, \quad (2)$$

$$\text{Responsivity(V)} = \frac{\text{I(V)} - \text{I}_{\text{dark}}\text{(V)}}{\text{Optical Power}}, \quad (3)$$

where I represents currents, and V_0 stands for a reference voltage for unity gain.

Fig. 4 shows the gain and responsivity for 5 nW, 50 nW, 100 nW, and 200 nW optical powers. An unamplified responsivity of 0.41 A/W at $\text{V}_0 = 1$ V and a maximum responsivity of 3.05×10^3 A/W at V = 70.5 V are achieved, which are comparable to the results reported in Reference [10]. It is observed that the gain and responsivity are independent of the optical power in a wide voltage range (below 68.94 V) where the gain is lower than 76.52 and the responsivity is lower than 30.6 A/W. However, with increasing voltage, the gain and responsivity achieved for higher optical power are smaller compared to that for lower optical powers because of the saturation effect of the multiplication process at high optical powers due to partial screening of the electric field by many charges [19]. Table I contains the responsivity and gain for different optical powers at $V_r = 70.5$ V.

TABLE I
DEPENDENCY OF RESPONSIVITY AND GAIN ON THE OPTICAL POWER AT $V_r = 70.5$ V

Parameters	5 nW	50 nW	100 nW	200 nW
Responsivity (A/W)	3.05×10^3	397	234	130
Gain	7.47×10^3	980	610	325

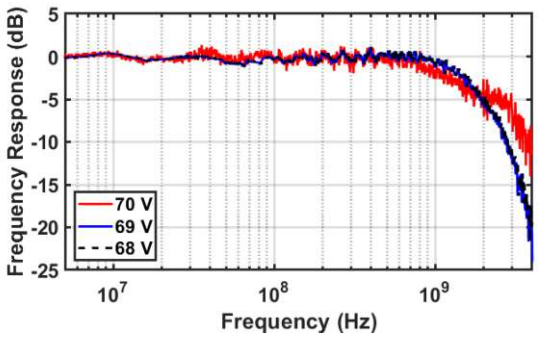

Fig. 5. Normalized frequency responses at 200 nW optical power for different operating voltages.

B. Frequency Response and Bandwidth

Fig. 5 shows the normalized frequency responses of the APD at an optical power of 200 nW ($\lambda = 675$ nm) for different gains, which were measured using a vector network analyzer (Rohde&Schwarz ZNB8). A high voltage bias-tee (Freq~5 MHz-18GHz) is used to supply the diode and send the RF signal back to the network analyzer.

The maximum bandwidth of 1.6 GHz was measured at $V_r = 69$ V, corresponding to the gain and responsivity of 80 and 32 A/W, respectively. This APD shows a bandwidth enhancement of $\sim$ 90% compared to the results reported in [10]. This is due to the large radius of the half-sphere high-field region of about 20 μm compared to a thickness of the drift region in [10] of only about 8μm, which lead to a small contribution of slow carrier diffusion.

It is observed that the bandwidths at $V_r = 68$ V and $V_r = 69$ V show almost the same value because the electric field in the absorption region, and consequently, the drift time doesn't vary significantly. The responsivity and gain of 10 A/W and 25 are repectively achieved at $V_r = 68$ V. The bandwidth drops at $V_r = 70$ V which is because of the avalanche build-up time. In fact, since the avalanche process takes time, the higher multiplication factor increases the avalanche build-up time and thus limits the bandwidth. This effect can be clearly seen in Fig. 5 for the multiplication factor of ~300 (R = 115 A/W) which results in a bandwidth of 1.28 GHz. However, as the optical power is 200 nW, the avalanche build-up time effect is not significantly dominant, and thus the bandwidth drop is low. The presented APD achieves the gain-bandwidth product of 128 GHz and 384 GHz,

TABLE II
PERFORMANCE COMPARISON OF LINEAR-MODE APDS (SM-APD: APD WITH SEPARATE ABSORPTION AND MULTIPLICATION REGION; CA-APD: CURRENT ASSISTED APD)

Parameters	Ref [10]	Ref [9]	Ref [6]	Ref [13]	Ref [12]	This work
Technology	0.35 μm	45 nm	0.25 μm	0.35 μm	0.35 μm	0.18 μm
Structure	n^+/p-well SM-APD	Double p-well/ deep p-well APD	p^+/n-well APD	p^+/n-well CA-APD	n^+/p-well SM-APD	n^+/n-well field crowding based APD
Area	Round r=60 μm	20×20 μm^2	10×10 μm^2	40×40 μm^2	Round r=60 μm	Round r=21 μm
Operating voltage	63 V	20.8 V	12.2 V	68 V	115 V	69 V
Optical power	500 nW	100 μW	1 mW	2 μW	2 μW	200 nW
Wavelength	670 nm	850 nm	850 nm	830 nm	670 nm	675 nm
Responsivity	20.5 A/W	0.56 A/W	0.2 A/W	13.17 A/W	20.5 A/W	32 A/W
Gain	50	23	16.7	43.9	50	80
Bandwidth	850 MHz	8.4 GHz	5.6 GHz	275 MHz	1.25 GHz	1.6 GHz
Gain-bandwidth product	42.5 GHz	193.2 GHz	93.5 GHz	12 GHz	62.5 GHz	128 GHz

corresponding to the gain and bandwidth of G = 80, BW = 1.6 GHz, and G = 300, BW = 1.28 GHz, respectively.

Table II shows a comparison of the key performance parameters of the presented APD with various silicon photodetectors fabricated in standard CMOS technologies. The field-crowding APD reduces the optical power and increases the avalanche gain as well as the bandwidth compared to the other APDs. Furthermore, the breakdown voltage of the suggested APD is comparable to that of the field-crowding SPAD of 67.3 V [14].

IV. CONCLUSION

To the best knowledge of the authors, the first electric field-line crowding linear-mode APD is presented. It is shown that at the operating voltage, a spherical multiplication region is formed around the n-well region (cathode). The electric field extends to the detection zone, but gradually decreases with moving radially away from the center. This results in a thick fully depleted absorption zone in which the photogenerated electrons drift towards the cathode. Due to such a thick absorption zone, an unamplified and a maximum responsivity of 0.41 A/W and of 7.47 × 10^3 A/W, respectively, at 5 nW optical power are achieved, which are comparable to the results reported in [10]. However, the maximum bandwidth of 1.6 GHz is measured which shows ∼90% improvement compared to that reported in [10].

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REFERENCES

[1] E. Kamrani, F. Lesage, and M. Sawan, "Low-noise, high-gain transimpedance amplifier integrated with SiAPD for low-intensity near-infrared light detection," *IEEE Sensors J.*, vol. 14, no. 1, pp. 258–269, Jan. 2014.
[2] O. Shcherbakova, L. Pancheri, N. Massari, G.-F. D. Betta, and D. Stoppa, "Linear-mode gain-modulated avalanche photodiode image sensor for time-of-flight optical ranging," *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 145–152, Jan. 2016.
[3] D. Milovancev, T. Jukic, N. Vokic, P. Brandl, B. Steindl, and H. Zimmermann, "VLC using 800-μm diameter APD receiver integrated in standard 0.35–μm BiCMOS technology," *IEEE Photon. J.*, vol. 13, no. 1, pp. 1–13, Feb. 2021.
[4] K. Iiyama, H. Takamatsu, and T. Maruyama, "Hole-injection-type and electron-injection-type silicon avalanche photodiodes fabricated by standard 0.18 μm CMOS process," *IEEE Photon. Technol. Lett.*, vol. 22, no. 12, pp. 932–934, Jun. 15, 2010.
[5] L. Pancheri, G.-F. D. Betta, and D. Stoppa, "Low-noise avalanche photodiode with graded junction in 0.15 μm CMOS technology," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 566–568, May 2014.
[6] M.-J. Lee, J.-M. Lee, H. Rucker, and W.-Y. Choi, "Bandwidth improvement of CMOS-APD with carrier-acceleration technique," *IEEE Photon. Technol. Lett.*, vol. 27, no. 13, pp. 1387–1390, Jul. 1, 2015.
[7] S. Nayak, A. H. Ahmed, A. Sharkia, A. S. Ramani, S. Mirabbasi, and S. Shekhar, "A 10-Gb/s –18.8 dBm sensitivity 5.7 mW fully-integrated optoelectronic receiver with avalanche photodetector in 0.13-μm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 8, pp. 3162–3173, Aug. 2019.
[8] M.-J. Lee and W.-Y. Choi, "A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain-bandwidth product," *Opt. Exp.*, vol. 18, no. 23, pp. 24189–24194, Nov. 2010.
[9] W. Zhi, Q. Quan, P. Yu, and Y. Jiang, "A 45 nm CMOS avalanche photodiode with 8.4-GHz bandwidth," *Micromachines*, vol. 11, no. 1, p. 65, Jan. 2020.
[10] B. Steindl, R. Enne, S. Schidl, and H. Zimmermann, "Linear mode avalanche photodiode with high responsivity integrated in high-voltage CMOS," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 897–899, Sep. 2014.
[11] B. Steindl, W. Gaberl, R. Enne, S. Schidl, K. Schneider-Hornstein, and H. Zimmermann, "Linear mode avalanche photodiode with 1-GHz bandwidth fabricated in 0.35-μm CMOS," *IEEE Photon. Technol. Lett.*, vol. 26, no. 15, pp. 1511–1514, Aug. 1, 2014.
[12] R. Enne, B. Steindl, and H. Zimmermann, "Speed optimized linear-mode high-voltage CMOS avalanche photodiodes with high responsivity," *Opt. Lett.*, vol. 40, no. 19, pp. 4400–4403, 2015.
[13] G. Jegannathan, H. Ingelberts, S. Boulanger, and M. Kuijk, "Current assisted avalanche photo diodes (CAAPDs) with separate absorption and multiplication region in conventional CMOS," *Appl. Phys. Lett.*, vol. 115, no. 13, Sep. 2019, Art. no. 132101.
[14] E. Van Sieleghem *et al.*, "A near-infrared enhanced silicon single-photon avalanche diode with a spherically uniform electric field peak," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 879–882, Jun. 2021.
[15] E. Van Sieleghem *et al.*, "A backside-illuminated charge-focusing silicon SPAD with enhanced near-infrared sensitivity," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1129–1136, Mar. 2022.
[16] E. Engelmann, W. Schmailzl, P. Iskra, F. Wiest, E. Popova, and S. Vinogradov, "Tip avalanche photodiode—A new generation silicon photomultiplier based on non-planar technology," *IEEE Sensors J.*, vol. 21, no. 5, pp. 6024–6034, Mar. 2021.
[17] B. Steindl, "Einzelphotonen-lawinendioden für integrierbare optische empfänger," Ph.D. dissertation, Inst. Electrodyn., Microw. Circuit Eng., Vienna Univ. Technol., Vienna, Austria, 2019.
[18] *Silvaco Atlas User's Manual*. Accessed: 2022. [Online]. Available: https://www.silvaco.com
[19] A. Karar *et al.*, "Investigation of avalanche photodiodes for EM calorimeter at LHC," CERN Accelerating Sci., Tech. Rep., SCAN-9510272, 1995.

2.4 A Near-Infrared Enhanced Field-Line Crowding Based CMOS-Integrated Avalanche Photodiode, "IEEE Photonics Journal 2023"

A Near-Infrared Enhanced Field-Line Crowding Based CMOS-Integrated Avalanche Photodiode

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***Abstract*—This paper presents a CMOS-integrated linear-mode avalanche photodiode based on electric field-line crowding (EFLC-APD) to form an effective multiplication zone and a wide absorption zone. The EFLC-APD possesses a hemispherical avalanching electric field at the n-well/p- epi junction formed due to the curvature of the half-sphere cathode. A lower electric field extends radially across the entire volume of the EFLC-APD towards the substrate and towards the surface anode. Because of such a distribution of the electric field, electrons photogenerated within the whole volume drift towards the cathode. Therefore, the EFLC-APD provides a large sensitive-area to total-area ratio while offering high responsivity and bandwidth for red and near-infrared light due to its thick absorption zone and drift-based carrier transport. It is shown that the electric field distribution can be modified by the design parameters such as cathode radius and diode size in addition to doping profiles. The EFLC-APD achieves a responsivity-bandwidth (R-BW) product of 49.5 $\frac{A}{W}$·GHz, corresponding to the responsivity and bandwidth of 33 A/W and 1.5 GHz, respectively, at the wavelength of 850 nm. In addition, a maximum responsivity of 3.05×10^3 A/W at 2 nW optical power is achieved for the red and near-infrared spectral range. Noise characterization resulted in an excess noise factor F = 6 measured at an avalanche gain of 56.7. Due to the high sensitive-area to total-area ratio, high responsivity, large bandwidth, and CMOS compatibility, this APD is a promising optical detector for many applications.**

***Index Terms*—CMOS integrated avalanche photodiode, linear-mode avalanche photodiode, field-line crowding, spherical avalanching field, near-infrared light.**

I. Introduction

THE ability to detect low-power optical signals is one of the main challenges in the field of applied optical sensors. The internal amplification makes linear-mode avalanche photodiodes (APDs) interesting optical detectors for many optical systems that require low light detection such as optical wireless communication (OWC) [1], [2], [3], [4], light detection and ranging applications (LIDAR) [5], [6], and imaging sensors [7], [8]. The use of APDs integrated with electronic circuitry by complementary metal-oxide semiconductor (CMOS) technology has become attractive in optical systems.

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Si CMOS integrated APDs typically use a planar n^+/p-well or a p^+/n-well junction to provide a space-charge region as detection zone and a high field region for multiplying the photo-generated carriers. The thickness of the detection region in these APDs is in the order of hundreds of nanometres [9], [10], [11], [12], [13], [14]. These structures achieve good results in terms of bandwidth because of a thin depleted absorption region. Ref. [13] reported a bandwidth of 8.4 GHz for an APD based on a p-well/deep n-well structure, and Ref. [14] achieved a bandwidth of 12 GHz for a spatially modulated APD. However, these APDs suffer from low responsivity due to the non-contribution of carriers generated under the thin absorption region to the output current. The maximum responsivities of the APDs reported in [13] and [14] for a wavelength of 850 nm are respectively 0.56 A/W and 0.03 A/W.

A so-called reach-through design concept was proposed to widen the absorption region, and thereby improve the responsivity [15], [16], [17], [18]. These thick APDs provide a space-charge region with a thickness in the range of 10 μm. A maximum responsivity of 2.7×10^4 A/W for 5-nW optical power at 670 nm was reported in Ref. [16]. The main drawback of such structures is their limited bandwidth due to the higher carrier drift time in a thick absorption zone. The maximum bandwidth reported in Ref. [16] is 850 MHz. Ref. [19] used a modulation doping technique for speed optimization to enhance the bandwidth to 1.25 GHz while maintaining the high responsivity but at a high reverse voltage of 115 V, where the diode could not longer be well isolated from the circuits on the chip.

Besides, in these planar structures, the photo-sensitive area is limited by the area of the p/n junction. In fact, carriers generated in the peripheral volume have a low probability of moving through the multiplication region and of leading to avalanche events, which leads to a limited sensitive-area to total-area ratio. In addition, they require a (virtual) guard ring to prevent premature edge breakdown due to a locally concentrated electric field at the edge of the junction, which further degrades the ratio of sensitive-area to total-area [20], [21], [22], [23]. This sensitive-area limitation is more substantial when the APD is downsized, in which the peripheral region is comparable to the dimensions of the photo-sensitive area [24].

Ref. [25] proposed a current-assisted avalanche photodiode that can collect charges generated in the peripheral volume. Two electrodes at the surface with different potentials are employed to form a drifting electric field for guiding the electrons

photogenerated in the peripheral volume towards the central multiplication region. This APD exhibits a high ratio of sensitive-area to total-area, however, achieves a maximum bandwidth of 275 MHz and 13 A/W responsivity at a wavelength of 830 nm.

Refs. [26], [27], [28] employed a charge-focusing concept to collect peripheral charge carriers in designing of single-photon avalanche photodiode (SPAD). In [26], [27], a customized fabrication process was utilized, involving a shallow n-type implant between the cathode and anode. This modification aimed to redistribute the electric field just below the silicon/silicon dioxide interface at the surface of the device, specifically to reduce the dark count rate. Ref. [29] presented a silicon photomultiplier (SiPM) that utilizes a SPAD based on the field-line crowding effect. However, transistors cannot be fabricated in the special SiPM detector process.

Recently, we presented a new Si CMOS APD based on the field-line crowding concept, which can be fabricated in a standard CMOS process without any process modification [30]. The EFLC-APD possesses a small hemispherical multiplication region around the n-well/p- epi junction and a thick depleted volume in the p- epitaxial layer with a lower electric field to guide charge carriers from the whole diode volume towards the multiplication region. This structure provides a maximum bandwidth of 1.6 GHz with a responsivity of R = 32 A/W at a wavelength of 675 nm while having a high sensitive-area to total-area ratio. The superiority of the EFLC-APD at down-scaling with maintaining the overall sensitivity and providing a large sensitive-area make it a very promising candidate to be used in array sensors.

In this article, we study the performance of the EFLC-APD for near-infrared light and improve the frequency response using electric field modification. TCAD simulation is used to study the effect of design parameters on the electric field distribution across the structure and consequently on the performance. The distributed field throughout the structure results in high bandwidth and responsivity due to providing a thick absorption region and drift-based carrier transport.

II. APD Structure

Fig. 1 shows a schematic 3-D drawing with the doping regions (a) and the top view (b) of the EFLC-APD fabricated in 0.18 μm high-voltage CMOS technology. The cathode of this APD consists of a hemispherical highly-doped n^+ region with a radius of 0.37 μm embedded in a half-sphere n-well region with a radius of rw. The round implant regions are made by using polygons with very short side lengths as well as 0, 90 and 135° angles that form the circle. The cathode is connected to the cathode pad with a track in metal layer 3 with a width of 2 μm as shown in Fig. 1(b). It should be noticed that the metal line used to connect the cathode to the cathode pad passes through the isolation layer on top of the active area. Since metal is an opaque material, therefore this area is practically no longer contributing to the absorption region, which degrades the sensitive-area to total-area ratio. The ratio of the area under the metal to the entire active area volume would be around 3.3% given by $\frac{2\times19}{19^2\times\pi}$. The cathode is surrounded by a p^+ and p-well ring (inner radius = ra) used as an anode ring. These regions are formed at the surface of a lightly p-doped ($\sim 1.5 \times 10^{13}$ cm^{-3}) epitaxial layer (p- epi) with a thickness of $\sim$24 μm. The p^+ substrate is also used as a substrate anode. On the top of the silicon, there is a standard isolation and passivation stack to protect the fabricated device from environmental influences.

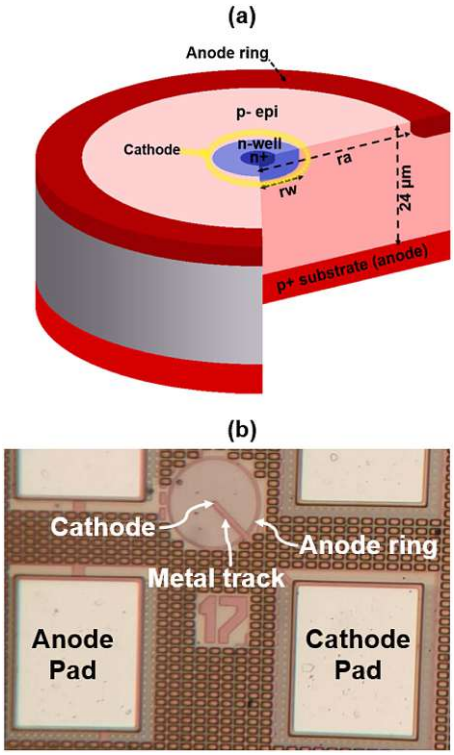

Fig. 1. (a) 3D schematic drawing (not to scale) and (b) top view of the fabricated EFLC-APD. The APD is covered by a standard isolation and passivation stack (not shown).

When the EFLC-APD is reversely biased, a hemispherical space-charge region forms around the cathode, which extends towards the substrate and the anode ring as the operating voltage increases. The electric field distribution of the space-charge region can be obtained from Gauss's law under two assumptions: the dimension of the highly doped cathode is much smaller than the whole diode volume, and it forms an abrupt transition into the intrinsic layer. Accordingly, the one-dimensional electric field in spherical coordinates is:

$$\mathrm{E}(d) \approx \frac{(V_r + V_{bi})\mathrm{rw}}{d^2}, \tag{1}$$

where V_{bi} is the built-in voltage, V_r is the operation voltage, and rw is the cathode's radius. According to 1, in reverse direction, a spherical high electric field region forms at the n-well/p- epi junction, and extends towards the substrate and towards the anode ring but decays by moving radially away from the center at a rate of d^{-2}.

III. TCAD Simulation

In order to study the electric field distribution inside the structure, TCAD simulations were performed using Silvaco's

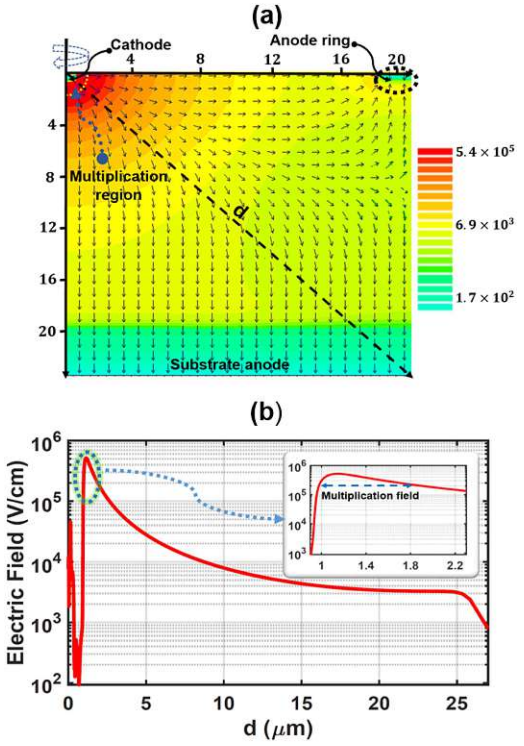

Fig. 2. (a) 2D plot of the electric field distribution across the EFLC-APD (rw = 0.6 μm, ra = 19 μm) at V_r = 69 V, corresponding to a gain (M) of 80. The breakdown voltage is 70.7 V. Vector arrows represent the local electric field direction. (b) Radial section of the electric field along the vector d in the structure.

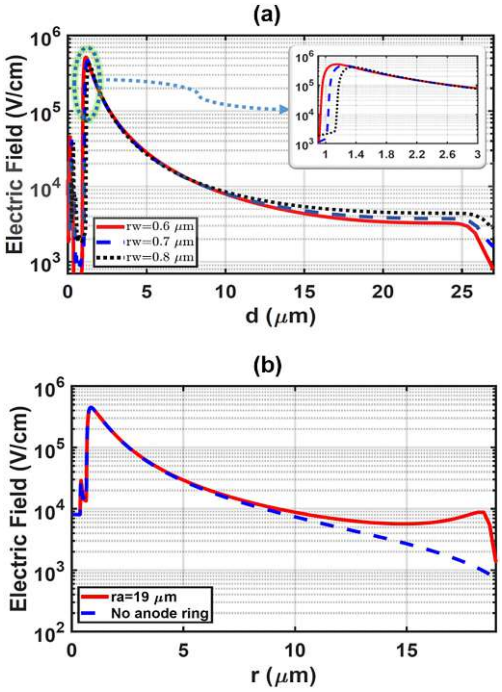

Fig. 3. (a) Radial cross-section of the electric field in the EFLC-APD with ra = 19 μm for different n-well radii. (b) Lateral cross-section of the electric field at the silicon surface of the EFLC-APD with rw = 0.6 μm. Simulations are done at an operating voltage of 69 V, 73.5 V, and 80 V for rw = 0.6 μm, rw = 0.7 μm, and rw = 0.8 μm, respectively, which all correspond to a gain of 80.

ATLAS [31]. Fig. 2(a) shows a 2D plot of the electric field within the EFLC-APD at an operating voltage of 69 V. It can be seen that a high field (E $\gtrsim 2 \times 10^5$ V/cm) region with a width of ~0.9 μm forms around the cathode, which is called multiplication region. This high field provides enough kinetic energy to create avalanche events due to impact ionization.

The electric field decreases by moving radially away from the center towards the substrate and towards the anode ring, but it is still in the range of thousands of V/cm at 25 μm away from the origin of coordinates as shown in Fig. 2(b). This electric field accelerates the photogenerated electrons in the direction opposite to the vector arrows and guides them towards the multiplication region. Due to such a distributed electric field throughout the structure, absorbed photons in the entire epitaxial layer have a very high chance to cause impact ionization by electrons drifting to the cathode, which results in a high sensitive-area to total-area ratio. Consequently, the large thickness of the detection zone provides high responsivity for long wavelengths, and the drift-based carrier transport mechanism enhances the detector's speed performance.

The distribution of the electric field changes with the radius of the n-well (rw) while the doping (implantation energy and dose as well as thermal budget) remains constant. Fig. 3(a) illustrates the electric field distribution for different n-well radii at a constant doping concentration. It can be seen that as the radius of the n-well decreases, the strength of the electric field increases in the multiplication region (see the inset in Fig. 3(a)) and decreases in the detection zone (see Fig. 3(a) especially for d = 10 to 25 μm). This is due to the fact that by decreasing the n-well radius, the curvature of the n-well region becomes sharper, leading to a higher electric field at the n-well/p-epi junction. Therefore, it should be considered that in order to provide enough electric field in the detection zone, EFLC-APDs with a larger size need an n-well with a larger radius.

Furthermore, the use of the anode ring redistributes the electric field in the lateral direction. Fig. 3(b) shows the lateral cross-section of the electric field at the silicon surface of the EFLC-APD structures with and without the anode ring. It can be seen that in the EFLC-APD with the anode ring, the electric field increases around the anode and then sharply drops. However, in the case there is no anode ring, the electric field is weaker, but could extend wider in the lateral direction. Here, the radius of the anode ring of ra = 19 μm is about the same as the vertical thickness of the effective intrinsic region (note: the p^+ substrate diffused a few μm into the grown 24 μm epi layer during the epitaxy and during the CMOS process) which is perfectly fitted to get the spherical shape.

It should be noted that changes in electric field distribution lead to different frequency responses of the diode. In fact, the frequency response is determined by the transit time of photogenerated electrons to reach the cathode. The transit time depends on the carrier drift distance and the drift velocity, which is proportional to the local electric field strength. The electric field gradually decreases (below the threshold required

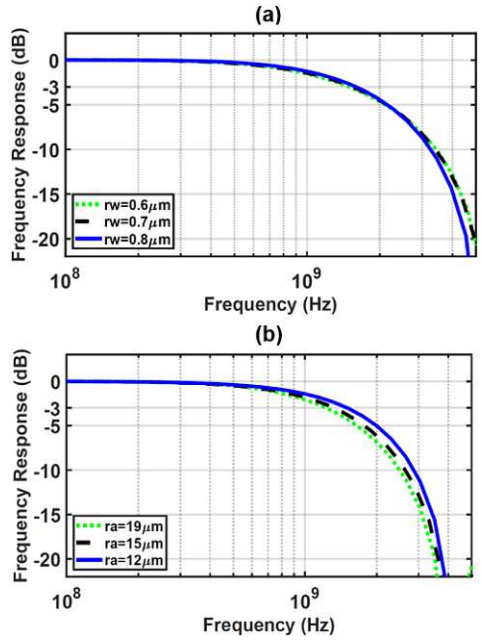

Fig. 4. Normalized frequency responses at $\lambda = 850$ nm for different (a) n-well radii and (b) diode sizes, extracted from TCAD simulations. Simulations are done at an operating voltage of (a) 69 V, 73.5 V, 80 V for rw $= 0.6$ μm, rw $=$ 0.7 μm, rw $= 0.8$ μm, respectively, and (b) 60 V, 64 V, 69 V for ra $= 12$ μm, ra $= 15$ μm, and ra $= 19$ μm, respectively. Note: these voltage values were selected to achieve a gain of 80 for each respective configuration.

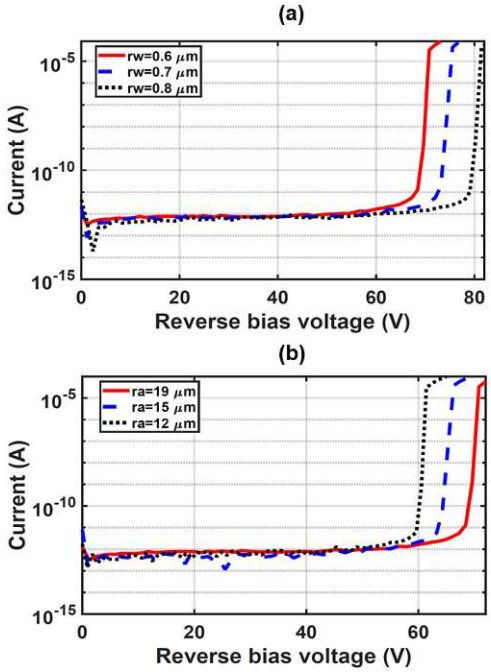

Fig. 5. Dark reverse characteristics for (a) different cathode radii with ra $=$ 19 μm, (b) different diode size with rw $= 0.6$ μm.

for saturated drift velocity) by moving radially away from the center. Accordingly, the bandwidth is limited by the drift time of photogenerated electrons absorbed in the thick absorption region far away from the center in the diagonal direction.

In order to study the influence of the electric field distribution on the frequency response, Fig. 4 represents the frequency response for the different n-well radii (rw) and different diode sizes (ra). The bandwidths achieved by the EFLC-APDs with a ra of 12 and different rw values of 0.6, 0.7, and 0.8 μm are 1.5, 1.54, and 1.59 GHz, respectively. The slight increase in bandwidth observed for the diodes with a larger n-well radius can be attributed to the slightly higher electric field in the detection zone, enabling faster carrier transit. According to Fig. 4(b), the speed can be improved by reducing the size of the diode, but at the cost of reducing the active area. The EFLC-APDs with an rw of 0.6 μm and different sizes of 19, 15, and 12 μm achieve bandwidths of 1.23, 1.35, and 1.5 GHz, respectively. This is because as the size of the diode decreases, the electric field strength distributed across the detection region increases and in addition, the radial carrier drift distance shortens. Furthermore, the effect of these parameters on the breakdown voltage is discussed in the following. Accordingly, such parameters should be optimized based on the requirements of the intended application.

IV. Measurement Results

Here, some key performance characteristics such as breakdown voltage, gain (M), responsivity (R), bandwidth (BW), and noise of the EFLC-APD are discussed. We have performed the measurements on wafer using a wafer prober at a constant temperature of 25 °C with probe heads. A Keysight B2987A electrometer was used to supply the voltage and measure the current.

A. Breakdown Voltage

As it was explained before, the distribution of the electric field within the structure changes as the radius of the n-well varies that leads to different breakdown voltages. Fig. 5(a) illustrates the dark characteristics of the EFLC-APDs with different n-well radii. The EFLC-APD with rw $= 0.6$ μm exhibits a breakdown voltage of 70.7 V, where the dark current reaches 1 μA. It is important to note that the presented APD is designed to operate at substrate potentials of about -69 V. However, the high-voltage (HV) CMOS process used for fabrication offers different wells to isolate the MOS transistors, enabling substrate potentials as low as -100 V. As a result, the high operating voltage of the EFLC-APD does not hinder the integration of such APD with readout circuits on the same silicon chip. It seems that the current is saturated at a current level of ~ 50 μA. This is because of high contact and series resistance. As the cathode is very small, there is only one contact via in the cathode, which makes a high contact resistance. Furthermore, we applied the biasing voltage only on the anode ring, not at the reverse substrate contact as we used a diced chip mounted on an insulating holder for the measurement. Therefore, there is a series resistance between the anode and cathode in the present device. It is, however, possible to reduce the series resistance by using a large-area p+/p-well anode contact at the silicon surface.

It can be seen that a larger n-well radius results in a higher breakdown voltage. This is because the electric field strength in the multiplication region (i.e., around the n-well) lowers with

increasing the n-well radius, and accordingly a higher operating voltage is required to provide the same avalanche gain. As a result, the operating voltage can be lowered by reducing the n-well radius. However, shrinking the n-well region is limited by a technology-associated design rule. The advanced, smaller-node technologies offer smaller n-well radii. In addition, they provide higher doping concentrations. Therefore, it is possible to design EFLC-APDs with lower breakdown voltage in advanced smaller node CMOS technologies. Of course, less lateral spread of the space-charge region and a reduction of the drift velocity will be the consequence. A high bandwidth, then, requires a reduction of the light-sensitive area (radius) or multi-dot structures with many cathode dots.

In addition, the breakdown voltage is influenced by the radius of the anode ring as the lateral electric field distribution inside the structure varies for different anode ring radii as mentioned in Section II. Fig. 5(b) shows the dark characteristics of the EFLC-APDs with different anode ring radii. It can be seen that by decreasing the anode ring radius, the breakdown voltage lowers. In fact, by reducing the anode radius from 19 μm to 12 μm, the breakdown voltage changes from 70.7 V to 60.5 V. This is due to the fact that by decreasing the diode size, the electric field is distributed over a smaller volume, leading to a higher intensity in the multiplication and detection zone.

B. Gain and Responsivity

The photodetection characterization of the EFLC-APD has been done for red ($\lambda = 675$ nm) and near-infrared light ($\lambda = 850$ nm). A multi-mode fiber with a lensed tip is used to provide a spotlight with a radius of 12.5 μm, which is smaller than the radius of the active area so that the total light was irradiated into the active area and all incident photons had the chance to be detected.

Fig. 6(a) shows the responsivity as a function of the reverse bias voltage at a low optical power (op) of 2 nW, obtained from the photocurrent characteristics, where the dark current has been subtracted. It can be seen that this APD shows almost the same responsivity for $\lambda = 850$ nm as it was obtained for $\lambda = 675$ nm in [30]. An unamplified responsivity ($M = 1$) of 0.42 A/W for 850 nm at $V_0 = 1$ V is achieved, which corresponds to the quantum efficiency of 61.4%. It should be mentioned that not every incident photon is transmitted into the silicon due to the non-zero surface reflectivity of the Si/isolation and passivation stack interface, which degrades the responsivity. Nevertheless, a maximum responsivity of 3.05×10^3 A/W at op = 2 nW and V = 70.5 V (rw = 0.6 μm, ra = 19 μm), which corresponds to a gain of 7.26×10^3, is achieved for both wavelengths (see the spectral response in Fig. 6).

Fig. 6(b) shows the spectral responsivity of the EFLC-APD with rw = 0.6 μm and ra = 19 μm at op = 2 nW for different gains. We used a Digikröm CM110 monochromator that swept the wavelength from 400 nm to 900 nm by steps of 1 nm, coupled with an optical attenuator to set the optical power at a constant value of 2 nW. The dependence of the photodiode responsivity on wavelength is as $R = \eta \cdot \frac{q\lambda}{hc}$, where η is the quantum efficiency. It can be seen that the responsivity is linearly proportional to

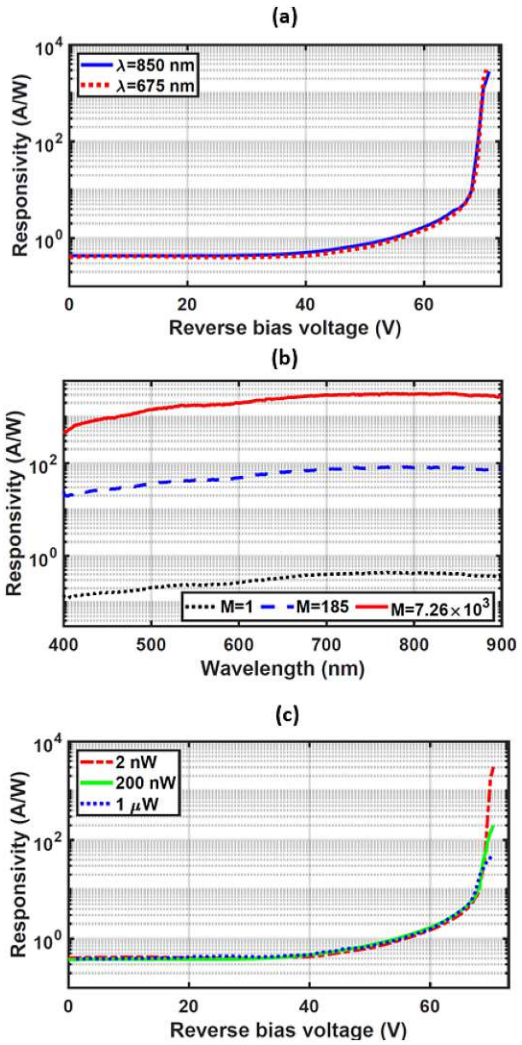

Fig. 6. (a) Responsivity as a function of reverse bias voltage at op = 2 nW. (b) Spectral responsivity at op = 2 nW for different gain M. (c) Responsivity at 850 nm as a function of reverse bias voltage for different optical powers. Measurements are done for the EFLC-APD with rw = 0.6 μm and ra = 19 μm.

the wavelength. This is because as the wavelength increases, the energy per photon becomes smaller, but each photon is still able to generate a carrier as long as the photon energy is larger than the bandgap energy. As a result, the responsivity is higher at longer wavelengths. However, at long wavelengths a considerable portion of the transmitted photons is absorbed in a deep depth where the electric field is very weak or non-existent to drive carriers towards the cathode. Therefore, the dominant transfer mechanism shifts from carrier drift to carrier diffusion, giving room to carrier recombination and resulting in a decrease in responsivity. In addition, there is an influence of the optical transmission through the isolation and passivation stack. The spectral responsivity shows an almost flat shape at long wavelengths (650 nm $< \lambda <$ 900 nm) with an unamplified maximum value of 0.44 A/W at $\lambda = 770$ nm at M = 1. Such high unamplified responsivity at long wavelengths is due to the thick detection zone as expected from the TCAD simulation results. It is shown that a maximum responsivity of 3.05×10^3 A/W at the gain of 7.26×10^3 is achieved for near-infrared wavelengths.

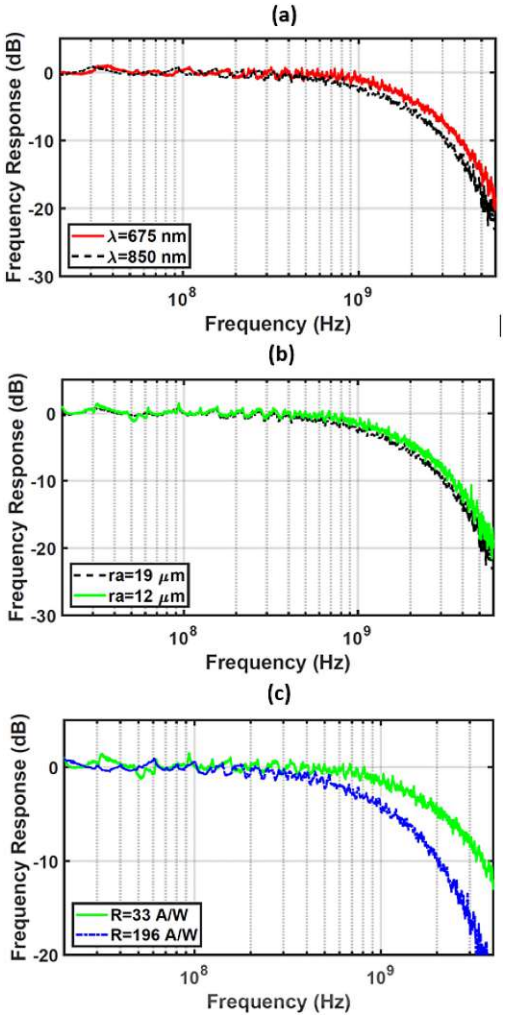

Fig. 7. Normalized frequency responses of (a) EFLC-APD with rw = 0.6 μm and ra = 19 μm for two wavelengths at M = 80. (b) EFLC-APD with rw = 0.6 μm and two diode sizes of ra = 12 μm and ra = 19 μm at λ = 850 nm and at M = 80. (c) EFLC-APD with rw = 0.6 μm and ra = 12 μm at different responsivities at λ = 850 nm.

Fig. 6(c) illustrates the dependency of the responsivity on the optical power. At different optical power, the maximum achievable responsivity is different. In fact, the maximum achievable responsivity is lower at higher optical power because of the saturation effect of the multiplication process at high optical powers due to partial screening of the electric field by many charges. Maximum responsivities for 850 nm of 196 and 48 A/W, both corresponding to the operating voltage of 70.5 V, are achieved at the optical powers of 200 nW and 1 μW, respectively.

C. *Frequency Response and Bandwidth*

The frequency response of the EFLC-APD (rw = 0.6 μm, ra = 19 μm) was measured for the two wavelengths of 675 nm and 850 nm with an optical power of 200 nW as shown in Fig. 7. Measurements were done using a vector network analyzer (Rohde & Schwarz ZNB8), which received the RF signal through a high voltage bias-tee (Freq ~5 MHz−18 GHz). The maximum bandwidth of 1.6 GHz for rw = 0.6 μm and ra = 19 μm is achieved at λ = 675 nm and V= 69 V, corresponding to the gain of 80 and responsivity of 32 A/W which demonstrates ~ 90% improvement compared to the results reported in Ref [16]. This is because the electric field is distributed across a larger thickness of about 20 μm compared to a thickness of the drift region in [16] of only about 8 μm, which left some contribution of slow carrier diffusion. Therefore, the contribution of slow carrier diffusion in this APD is significantly lowered compared to that of the APD in [16]. Nonetheless, the EFLC-APD uses the concept of separate multiplication and absorption region to achieve high responsivity with the inevitable bandwidth limitation by carrier drift time in a thick absorption zone.

The frequency response measured for the same EFLC-APD at λ = 850 nm shows a maximum achievable bandwidth of 1.2 GHz at the same gain (M = 80) and responsivity (R = 33 A/W). This bandwidth is 400 MHz lower compared to that obtained for a wavelength of 675 nm as reported in [30] due to the larger penetration depth of 850 nm light. However, the bandwidth is still 350 MHz larger than reported in [16] for 850 nm. This is due to the fact that more of the photons with longer wavelengths are absorbed deeper and thus the transit time of the photogenerated electrons to reach the cathode is higher.

It should be noticed that the frequency response is determined by the transit time of photogenerated electrons to reach the cathode, which could be reduced by shortening the carrier drift distance and increasing the electric field intensity. Since in this APD, the electrons generated in the peripheral volume are guided towards the multiplication region, and even the electrons generated far away from the cathode contribute to the photocurrent; thus, the frequency response is expected to improve by reducing the size (ra) of the EFLC-APD.

Fig. 7(b) presents the normalized frequency response of the EFLC-APDs with two different sizes (ra = 12 μm and ra = 19 μm) at λ = 850 nm and M = 80. It can be observed that by reducing ra from 19 μm to 12 μm, the bandwidth increases from 1.2 GHz to 1.5 GHz. This improvement is attributed to the electron drift time reduction due to the shortening of the radial carrier drift distance as well as to the increase in the electric field strength distributed across the detection zone as discussed in Section II. Since the responsivity remains the same for both structures, the APD with ra = 12 μm achieves a higher R-BW product. It is worth mentioning that we could enhance the bandwidth by shrinking the EFLC-APD while maintaining its responsivity. An important aspect that should be pointed out is that, due to the high sensitive-area to total-area ratio, it is possible to provide enough active area when it is downsized.

We should note that the bandwidth drops at higher responsivity because of the avalanche build-up time effect. In fact, at the maximum responsivity, we have the highest multiplication factor, and as the avalanche process takes time, the avalanche build-up time is high, which causes a bandwidth decrease. In order to demonstrate this effect, Fig. 7(c) shows the frequency response at the maximum responsivity of 196 A/W corresponding to the gain of 466 at the optical power of 200 nW. It shows that the bandwidth is reduced to 760 MHz. However, for this gain and optical power, the effect of avalanche build-up time is not strongly pronounced (compared to 1.5 GHz bandwidth at a gain

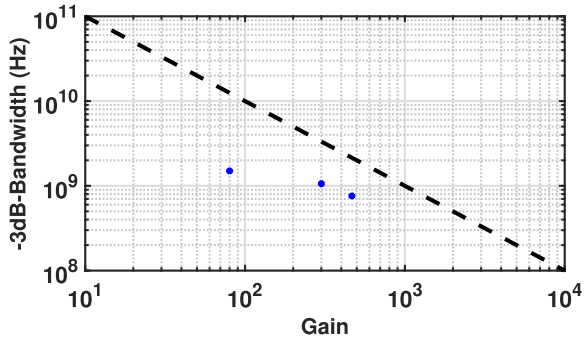

Fig. 8. Bandwidth vs. gain of EFLC-APD with rw = 0.6 μm and ra = 12 μm at the optical power of 200 nW. The dashed line represents the gain-bandwidth product of 1 THz [32].

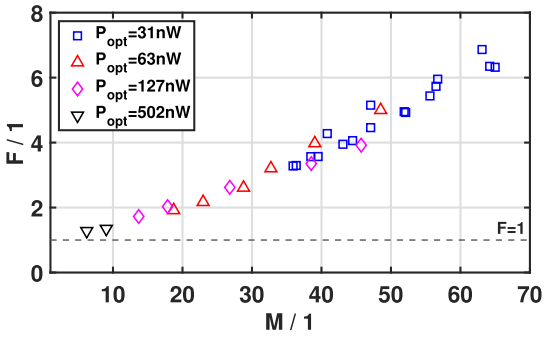

Fig. 9. Measured excess noise factor at $\lambda = 642$ nm. A relatively narrow dynamic range of the measurement system required a variety of optical power levels to cover a reasonable span of M.

of 80, we lose only a factor of about 2 in bandwidth). We expect higher bandwidth reduction at higher gains (at lower optical powers). Accordingly, based on the intended application, the trade-off between bandwidth and sensitivity can be optimized. For instance, in applications that work at low frequencies, one can utilize the maximum responsivity. Fig. 8 shows the bandwidth versus gain at the optical power of 200 nW. Bandwidths of 1.5, 1.06, and 0.76 GHz are obtained for gains of 80, 300, and 466, respectively. It can be seen that the bandwidth decreases with increasing gain. The dashed line in Fig. 8 represents a gain-bandwidth product of 1 THz that shows the gain-bandwidth product limit [32]. The left point (see Fig. 8) at M = 80 and a bandwidth of about 1.5 GHz approaches the bandwidth limit determined by the carrier drift time through the thick absorption zone.

D. Noise Characteristic

The signal-to-noise ratio enhancement, achieved by avalanche gain, is actually compromised by a gain dependent noise component. Models like the McIntyre's theory [33] or the dead-space model [34], [35] are well established to predict the APD excess noise factor F for devices with uniform electric field. However, for EFLC-APDs, these models are not applicable, since the electric field is predominately non-uniform (see Fig. 2a). Hence, in the following section, the noise characteristics of the EFLC-APD is studied experimentally.

The noise characterization method utilized in this study was based on the approach presented by [36]. Essentially the power spectral density (PSD) of the APD's photocurrent, stimulated by a laser source in DC mode, is measured for different avalanche gains (M). For this experiment, a 642 nm single-mode laser (Thorlabs, LP642-SF20) was used to exclude the effect of mode noise. Various values of M were obtained by adjusting the operating voltage while measuring the photocurrent using an electrometer (Keysight B2987A). The APD is reverse-biased by applying a negative voltage to the anode, while the cathode is connected to a transimpedance amplifier (TIA LMH3440, $R_T = 28\,\mathrm{k\Omega}$ and $BW = 200$ MHz, both measured). The TIA provides the necessary amplification to the photocurrent noise level to be distinguishable from the spectrum analyzer noise floor (R&S FSP, noise floor $\approx -155\,\mathrm{dBm/Hz}$ up to 500 MHz). However, it also poses an additional noise source, that was taken care of by calibration, done in post-processing. For every measured data point of M, the PSD was acquired (averaged over 5 sweeps from 10 MHz to 100 MHz with 10 kHz resolution bandwidth) with and without light. Their difference equals the PSD of the photocurrent. This calibration method is insufficient, if the photocurrent's PSD is much smaller than the TIA PSD, hence the system sensitivity was defined so that the APD noise has to be equal to the noise of the measurement system. The mean PSD of the TIA with connected APD, biased at -1 V, without light, was ≈ -127 dBm/Hz (generally a higher diode capacitance elevates the TIA noise spectrum, however for the presented APD the capacitance at smallest bias voltage is already dominated by the PCB parasitics, so the TIA PSD was effectively constant for all bias states up to a saturation limit, which is explained further below). A measurement run started by positioning the fiber (mode field diameter $\approx 5\,\mu$m) above the center of the APD surface. In fact, the fiber was adjusted to the position of maximum photocurrent. The photocurrent is measured at M = 1 ($V_r = -1$ V), which gives the reference value for the calculation of M. After that, the bias voltage is set to a starting value (determined by the system sensitivity and the optical power) and then increased in small steps. For every voltage point, the photocurrent I_{APD} (i.e., M) and the PSD is measured. At the end of each run another photocurrent measurement at M = 1 is done to ensure that the fiber is still properly positioned. Referring to [36], the excess noise factor F can be calculated for every data point by

$$F = \frac{\overline{PSD_{cal}} R_{term}}{2qMI_{APD}R_T^2}, \tag{2}$$

where q is the electron charge, R_{term} is the input resistance of the spectrum analyzer (50 Ω) and $\overline{PSD_{cal}}$ is the mean value of the calibrated PSD in the interval from 10 MHz to 100 MHz.

The result of the excess noise measurement is illustrated in Fig. 9. A variety of optical power levels was necessary to cover a reasonable span of M while respecting the dynamic range of the measurement system. Multiplied photocurrent levels had to be in the range of ≈0.4 to 1 μA, in order to be utilizable. The measured points within the dynamic range resulted in excess noise factors of 2, 4 and 6 at gains of 17.8, 39, and 56.7, respectively. It is important to mention that due to the non-uniform electric

TABLE I
PERFORMANCE COMPARISON OF LINEAR-MODE APDS (RT-APD: REACH-THROUGH APD; CA-APD: CURRENT ASSISTED APD)

Parameters	Ref [16]	Ref [38]	Ref [19]	Ref [25]	Ref [13]	Ref [30]	This work	This work
Technology	0.35 μm	0.25 μm	0.35 μm	0.35 μm	45 nm	0.18 μm	0.18 μm	0.18 μm
Structure	n^+/p-well RT-APD	p^+/n-well APD	n^+/p-well RT-APD	p^+/n-well CA-APD	Double p-well/ deep n-well APD	n^+/n-well EFLC-APD	n^+/n-well EFLC-APD	n^+/n-well EFLC-APD
Active area	r=30 μm	10×10 μm^2	r=30 μm	40×40 μm^2	20×20 μm^2	r=19 μm	r=12 μm	r=19 μm
Operating voltage	63 V	12.2 V	115 V	68 V	20.8 V	69 V	60 V	69 V
Optical power	500 nW	1 mW	2 μW	2 μW	100 μW	200 nW	200 nW	200 nW
Wavelength	670 nm	850 nm	670 nm	830 nm	850 nm	675 nm	850 nm	850 nm
Gain	50	16.7	50	43.9	23	80	80	80
Responsivity	20.5 A/W	0.2 A/W	20.5 A/W	13.17 A/W	0.56 A/W	33 A/W	33 A/W	33 A/W
Bandwidth	850 MHz	5.6 GHz	1.25 GHz	275 MHz	8.4 GHz	1.6 GHz	1.5 GHz	1.2 GHz
R-BW product	17.4 $\frac{A}{W}$·GHz	1.1 $\frac{A}{W}$·GHz	25.6 $\frac{A}{W}$·GHz	3.6 $\frac{A}{W}$·GHz	4.7 $\frac{A}{W}$·GHz	52.8 $\frac{A}{W}$·GHz	49.5 $\frac{A}{W}$·GHz	39.6 $\frac{A}{W}$·GHz

field, present in the EFLC-APD structure, neither McIntyre's theory [33] nor the dead-space model [34], [35] can be utilized to account for the excessive noise observed in these diodes. These models are derived for structures with uniform electric fields. Nevertheless, due to a wavelength dependence of the dead-space effect [37], higher excess noise has to be expected for increased wavelength.

V. COMPARISON

The excess noise factors obtained are comparable to those [36] of the planar n+/p-well APD in 0.35 μm high-voltage (HV) CMOS with a uniform electric field [16]. F of this 0.35 μm HV APD was 6 at M = 50 and about 6.5 at M = 60. When we compare the thickness of the multiplication region (where $E \gtrsim 2 \times 10^5$ V/cm), it is 0.73 μm in the 0.35 μm HV APD and about 0.9 μm in the EFLC 0.18 μm HV APD (both for M = 60). A thicker multiplication region is generally better for a lower excess noise. But the crowding of the multiplied carriers towards lower radius (like the crowding of the field lines when they approach to the inner end of the multiplication region) obviously counteracts this advantage of the thicker multiplication region.

To better highlight the contribution of this work over the state-of-the-art, Table 1 shows a comparison of the key performance parameters of the EFLC-APD with various silicon photodetectors fabricated in standard CMOS technologies. It should be noted that the achieved maximum bandwidth of 1.5 GHz shows 77% and 550% improvement compared to results reported in Ref. [16] and [25] for wavelengths of 670 and 830 nm, respectively. This APD additionally shows a responsivity improvement of 60% and 240% compared to results reported in Ref. [16] and [25] respectively. Furthermore, the presented EFLC-APD achieves a responsivity-bandwidth product of 49.5 $\frac{A}{W}$·GHz, corresponding to the responsivity and bandwidth of R = 33 A/W and BW = 1.5 GHz, respectively, which shows a significant improvement compared to the literature according to Table I.

VI. CONCLUSION

A characterization of the electric field-line crowding-based avalanche photodiode is presented. It is shown that a hemispherical electric field distribution formed across the entire volume of the EFLC-APD leads to a thick hemispherical detection zone in which the electrons generated in the entire volume are accelerated towards the cathode. The EFLC-APD achieves a maximum responsivity of 3.05 $\times 10^3$ A/W in the red and near-infrared spectral range due to its thick absorption region. Furthermore, because of the high electric field distributed over the structure, it provides a maximum bandwidth of 1.5 GHz at λ = 850 nm, that is an improvement of 77% and 550% compared to results reported in Ref. [16] and [25], respectively. In addition, the EFLC-APD shows the responsivity-bandwidth product of 49.5 $\frac{A}{W}$·GHz, which represents a significant improvement over the state-of-the-art. Also the excess noise was investigated, F=6 was measured at a gain of 56.7. Especially for range-finding sensors, which use near-infrared light, this APD should be well appropriate.

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REFERENCES

[1] M. M. Hossain et al., "Low-noise speed-optimized large area CMOS avalanche photodetector for visible light communication," *J. Lightw. Technol.*, vol. 35, no. 11, pp. 2315–2324, Jun. 2017.
[2] E. Kamrani, F. Lesage, and M. Sawan, "Low-noise, high-gain transimpedance amplifier integrated with SiAPD for low-intensity near-infrared light detection," *IEEE Sensors J.*, vol. 14, no. 1, pp. 258–269, Jan. 2014.
[3] L. Zhang et al., "A comparison of APD-and SPAD-based receivers for visible light communications," *J. Lightw. Technol.*, vol. 36, no. 12, pp. 2435–2442, Jun. 2018.
[4] P. Brandl, T. Jukić, R. Enne, K. Schneider-Hornstein, and H. Zimmermann, "Optical wireless APD receiver with high background-light immunity for increased communication distances," *IEEE J. Solid-State Circuits*, vol. 51, no. 7, pp. 1663–1673, Jul. 2016.

[5] H.-S. Cho, C.-H. Kim, and S.-G. Lee, "A high-sensitivity and low-walk error LADAR receiver for military application," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 61, no. 10, pp. 3007–3015, Oct. 2014.
[6] H.-Z. Song, "Avalanche photodiode focal plane arrays and their application to laser detection and ranging," in *Advances in Photodetectors-Research and Applications*. London, U.K.: IntechOpen, 2018, pp. 145–168.
[7] O. Shcherbakova, L. Pancheri, G.-F. Dalla Betta, N. Massari, and D. Stoppa, "3D camera based on linear-mode gain-modulated avalanche photodiodes," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 490–491.
[8] Y. Dong et al., "Germanium-tin on silicon avalanche photodiode for short-wave infrared imaging," in *Proc. Symp. VLSI Technol. (VLSI- Technol.): Dig. Tech. Papers*. IEEE, 2014, pp. 1–2.
[9] K. Iiyama, H. Takamatsu, and T. Maruyama, "Hole-injection-type and electron-injection-type silicon avalanche photodiodes fabricated by standard 0.18 μm CMOS process," *IEEE Photon. Technol. Lett.*, vol. 22, no. 12, pp. 932–934, Jun. 2010.
[10] F.-P. Chou, C.-W. Wang, Z.-Y. Li, Y.-C. Hsieh, and Y.-M. Hsin, "Effect of deep N-Well bias in an 850-nm Si photodiode fabricated using the CMOS process," *IEEE Photon. Technol. Lett.*, vol. 25, no. 7, pp. 659–662, Apr. 2013.
[11] S. Nayak, A. H. Ahmed, A. Sharkia, A. S. Ramani, S. Mirabbasi, and S. Shekhar, "A 10-Gb/s- 18.8 dBm sensitivity 5.7 mW fully-integrated optoelectronic receiver with avalanche photodetector in 0.13 μm CMOS," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 66, no. 8, pp. 3162–3173, Aug. 2019.
[12] M.-J. Lee and W.-Y. Choi, "A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain-bandwidth product," *Opt. Exp.*, vol. 18, no. 23, pp. 24189–24194, 2010.
[13] W. Zhi, Q. Quan, P. Yu, and Y. Jiang, "A 45 nm CMOS avalanche photodiode with 8.4 GHz bandwidth," *Micromachines*, vol. 11, no. 1, 2020, Art. no. 65.
[14] M.-J. Lee, "First CMOS silicon avalanche photodetectors with over 10-GHz bandwidth," *IEEE Photon. Technol. Lett.*, vol. 28, no. 3, pp. 276–279, Feb. 2016.
[15] Y. S. Kim, I. S. Jun, and K. H. Kim, "Design and characterization of CMOS avalanche photodiode with charge sensitive preamplifier," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 3, pp. 1376–1380, Jun. 2008.
[16] B. Steindl, R. Enne, S. Schidl, and H. Zimmermann, "Linear mode avalanche photodiode with high responsivity integrated in high-voltage CMOS," *IEEE Electron Device Lett.*, vol. 35, no. 9, pp. 897–899, Sep. 2014.
[17] B. Steindl, W. Gaberl, R. Enne, S. Schidl, K. Schneider-Hornstein, and H. Zimmermann, "Linear mode avalanche photodiode with 1-GHz bandwidth fabricated in 0.35-μm CMOS," *IEEE Photon. Technol. Lett.*, vol. 26, no. 15, pp. 1511–1514, Aug. 2014.
[18] Z. Cheng, H. Xu, and Y. Chen, "Design of low noise avalanche photodiode single element detectors and linear arrays through CMOS process," *Proc. SPIE*, vol. 10978, pp. 70–77, 2019.
[19] R. Enne, B. Steindl, and H. Zimmermann, "Speed optimized linear-mode high-voltage CMOS avalanche photodiodes with high responsivity," *Opt. Lett.*, vol. 40, no. 19, pp. 4400–4403, 2015.
[20] M.-J. Lee, H. Rucker, and W.-Y. Choi, "Effects of guard-ring structures on the performance of silicon avalanche photodetectors fabricated with standard CMOS technology," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 80–82, Jan. 2012.
[21] W. Wang, H.-A. Zeng, F. Wang, G. Wang, Y. Xie, and S. Feng, "A speed-optimized, low-noise APD with 0.18 μm CMOS technology for the VLC applications," *Modern Phys. Lett. B*, vol. 34, no. 29, 2020, Art. no. 2050321.
[22] T. Wang et al., "Effects of guard-ring's depth and space on the performance of silicon avalanche photodetector arrays with TCAD simulation," *Proc. SPIE*, vol. 12065, pp. 602–607, 2021.
[23] D. Shin, B. Park, Y. Chae, and I. Yun, "The effect of a deep virtual guard ring on the device characteristics of silicon single photon avalanche diodes," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 2986–2991, Jul. 2019.
[24] S. S. K. Poushi, H. Mahmoudi, M. Hofbauer, B. Steindl, K. Schneider-Hornstein, and H. Zimmermann, "Experimental and simulation study of fill-factor enhancement using a virtual guard ring in n/p-well CMOS single-photon avalanche diodes," *Proc. SPIE*, vol. 60, 2021, Art. no. 067105.
[25] G. Jegannathan, H. Ingelberts, S. Boulanger, and M. Kuijk, "Current assisted avalanche photo diodes (CAAPDs) with separate absorption and multiplication region in conventional CMOS," *Appl. Phys. Lett.*, vol. 115, no. 13, 2019, Art. no. 132101.
[26] E. Van Sieleghem et al., "A near-infrared enhanced silicon single-photon avalanche diode with a spherically uniform electric field peak," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 879–882, Jun. 2021.
[27] E. Van Sieleghem et al., "A backside-illuminated charge-focusing silicon SPAD with enhanced near-infrared sensitivity," *IEEE Trans. Electron Devices*, vol. 69, no. 3, pp. 1129–1136, Mar. 2022.
[28] K. Morimoto et al., "3.2 megapixel 3D-stacked charge focusing SPAD for low-light imaging and depth sensing," in *Proc. IEEE Int. Electron Devices Meeting*, 2021, pp. 20–2.
[29] E. Engelmann, W. Schmailzl, P. Iskra, F. Wiest, E. Popova, and S. Vinogradov, "Tip avalanche photodiode—A new generation silicon photomultiplier based on non-planar technology," *IEEE Sensors J.*, vol. 21, no. 5, pp. 6024–6034, Mar. 2021.
[30] S. K. Poushi, B. Goll, K. Schneider-Hornstein, M. Hofbauer, and H. Zimmermann, "CMOS integrated 32 A/W and 1.6 GHz avalanche photodiode based on electric field-line crowding," *IEEE Photon. Technol. Lett.*, vol. 34, no. 18, pp. 945–948, Sep. 2022.
[31] "Silvaco atlas user's manual." Accessed: 2022. [Online]. Available: https://www.silvaco.com
[32] D. Decoster and J. Harari, *Optoelectronic Sensors*. Hoboken, NJ, USA: Wiley, 2013.
[33] R. J. McIntyre, "Multiplication noise in uniform avalanche diodes," *IEEE Trans. Electron Devices*, vol. ED-13, no. 1, pp. 164–168, Jan. 1966.
[34] B. E. A. Saleh, M. M. Hayat, and M. C. Teich, "Effect of dead space on the excess noise factor and time response of avalanche photodiodes," *IEEE Trans. Electron Devices*, vol. 37, no. 9, pp. 1976–1984, Sep. 1990.
[35] M. M. Hossain et al., "Low-noise speed-optimized large area CMOS avalanche photodetector for visible light communication," *J. Lightw. Technol.*, vol. 35, no. 11, pp. 2315–2324, Jun. 2017.
[36] T. Jukić, P. Brandl, and H. Zimmermann, "Determination of the excess noise of avalanche photodiodes integrated in 0.35-μm CMOS technologies," *Proc. SPIE*, vol. 57, no. 4, 2018, Art. no. 044101.
[37] A. R. Pauchard, P.-A. Besse, and R. S. Popovic, "Dead space effect on the wavelengthdependence of gain and noise in avalanche photodiodes," *IEEE Trans. Electron Devices*, vol. 47, no. 9, pp. 1685–1693, Sep. 2000.
[38] M.-J. Lee, J.-M. Lee, H. Rücker, and W.-Y. Choi, "Bandwidth improvement of CMOS-APD with carrier-acceleration technique," *IEEE Photon. Technol. Lett.*, vol. 27, no. 13, pp. 1387–1390, Jul. 2015.

2.5 Area and Bandwidth Enhancement of an n^+/p-Well Dot Avalanche Photodiode in 0.35 μm CMOS Technology, "Sensors 2023"

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Area and Bandwidth Enhancement of an n^+/p-Well Dot Avalanche Photodiode in 0.35 µm CMOS Technology

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Abstract: This paper presents a CMOS-integrated dot avalanche photodiode (dot-APD) that features a small central n^+/p-well hemispherical cathode/p-well structure circularly surrounded by an anode ring. The dot-APD enables wide hemispherical depletion, charge collection from a large volume, and a small multiplication region. These features result in a large light-sensitive area, high responsivity and bandwidth, and exceptionally low junction capacitance. The active area can be further expanded using a multi-dot structure, which is an array of several cathode/p-well dots with a shared anode. Experimental results show that a 5 × 5 multi-dot APD with an active area of 70 µm × 70 µm achieves a bandwidth of 1.8 GHz, a responsivity of 9.7 A/W, and a capacitance of 27 fF. The structure of the multi-dot APD allows for the design of APDs in various sizes that offer high bandwidth and responsivity as an optical detector for various applications while still maintaining a small capacitance.

Keywords: CMOS-integrated dot avalanche photodiode; multi-dot APD; radial charge collection; active area enlargement; bandwidth enhancement

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1. Introduction

Because of the inherent gain, using linear-mode avalanche photodiodes (APDs) instead of standard pin photodiodes has become attractive in many optical systems where weak optical signal detection is required [1–7]. The use of a CMOS process for the production of integrated APDs with electronic circuitry for read-out and signal processing reduces the influence of parasitic effects, and furthermore offers a cost-effective production. Common design approaches towards CMOS-integrated APDs are based on planar n^+/p-well and p^+/n-well junctions. Refs. [8–15] present APDs with a thin combined absorption and multiplication region in the order of hundreds of nanometers thickness. These APDs provide a high bandwidth but suffer from low responsivity at long wavelengths (red and near-infrared light) due to their thin detection zone. Refs. [14,15] reported APDs that achieve a bandwidth of 8.4 GHz and 12 GHz while their maximum responsivities are 0.56 A/W and 0.03 A/W, respectively, at a wavelength of 850 nm.

In order to achieve a higher responsivity, the so-called reach-through APD was presented, which possesses a separate space-charge region with a larger thickness [16–20]. A 12 µm thick absorption region was present in [17,19,20]. In these APDs, the photo-generated electrons in the thick absorption zone drift upwards to the multiplication zone and can trigger the avalanche process, resulting in a high responsivity. However, carrier drift time in their thick absorption region generally limits the bandwidth. Based on the reach-through concept, Ref. [17] presented an APD with the responsivity and bandwidth of 20.5 A/W and 850 MHz at 670 nm. Refs. [19,20] used the lateral well modulation-doping technique to improve the bandwidth by manipulating the electric field distribution within the structure.

One of the main drawbacks of the planar structures is that the photo-sensitive area is proportional to the area of the p/n junction. In fact, since the electric field is limited to

below the p/n region, only the carriers generated in this area have a chance to cause impact ionization by electrons drifting to the multiplication region. Therefore, to increase the sensitive area, the p/n junction area has to be expanded, which leads to an increase in the junction's capacitance. Consequently, these APDs typically exhibit the trade-off between detector capacitance and the detection area. In addition, the proportionality of the active area to the p/n junction area results in a limited fill-factor defined as the ratio of the photo-sensitive area to the whole diode area. Moreover, the necessity of a guard ring to avoid premature edge breakdown in such structures causes further fill-factor degradation. This degradation is more noticeable in the scaled-down APD, where the dimensions of the guard ring are comparable to the photos-sensitive area dimensions. Accordingly, the scalability of such APDs to be used in multi-pixel detectors is an issue [21–23].

Guiding carriers generated in the peripheral volume towards the multiplication region can provide a near-unity fill-factor and overcome the scalability issue. A current-assisted avalanche photodiode is presented in [24] consisting of two electrodes at the surface with different potentials to collect photo-generated carriers in the peripheral volume. This APD achieved a near-unity fill-factor and a responsivity of 13 A/W, but its maximum bandwidth reported was 275 MHz at λ = 830 nm. Ref. [25] used the field-line crowding concept with a small n^+/n-well structure to form a distributed electric field over the whole diode volume to guide the photo-generated carriers in the peripheral volume. This device was realized in 0.18 µm CMOS with a 24 µm thick low-doped epitaxial layer. A maximum bandwidth of 1.6 GHz and a responsivity of R = 32 A/W at λ = 675 nm were achieved for an APD with a radius of 19 µm while having a near-unity fill factor.

This paper presents a dot avalanche-based APD that provides a near-unity fill factor and 9.7 A/W responsivity while achieving 1.8 GHz bandwidth at λ = 675 nm. The single dot structure possesses a small hemispherical n^+/p-well structure at the center. A spherically uniform high electric field is formed around the n^+/p-well junction, which serves as the multiplication region inside the p-well, and a weaker electric field extends radially throughout the diode to guide charge carriers from the entire diode volume towards the multiplication region. For applications that require a larger light-sensitive area, a multi-dot structure is proposed to increase the active area, which is a combination of several cathode/p-well dots with connected cathodes and with a shared anode. In the next sections, the design approach will be discussed in detail.

2. Single-Dot APD

Figure 1 shows the top view (a) and a cross-section (b) of the single-dot APD (SD-APD) fabricated in the 0.35 µm CMOS modular optical sensor technology platform (XO035) of X-FAB semiconductor foundries. A semi-hemispherical high-doped n^+ region embedded in a half-sphere p-well (PW) region as the multiplication region forms the cathode of this APD. The cathode is circularly surrounded by a p^+ and p-well as an anode, which all are formed on a lightly p-doped epitaxial layer (p- epi) with a doping concentration of $\sim 2 \times 10^{13}$ cm^{-3} and a thickness of ~12 µm. The p^+ substrate is also used as a backside anode as it is available at the back side of the chip (because the wafers were thinned by mechanical grinding) and can be connected to the anode supply.

In the SD-APD, unlike the planar structures that only have a vertical electric field, the electric field extends radially throughout the diode, which is used for vertical and peripheral charge collection. TCAD simulation is performed to study the electric field distribution inside the structure. According to the cylindrically symmetric geometry of the structure, two-dimensional (2d) simulations of half of the diode are carried out along one radius in the cylindrical coordinate system. In order to enhance the simulation accuracy and to optimize the simulation time, the mesh of grid points in the cathode region (n^+/p-well junction) is refined, while it becomes coarser towards the substrate and anode ring.

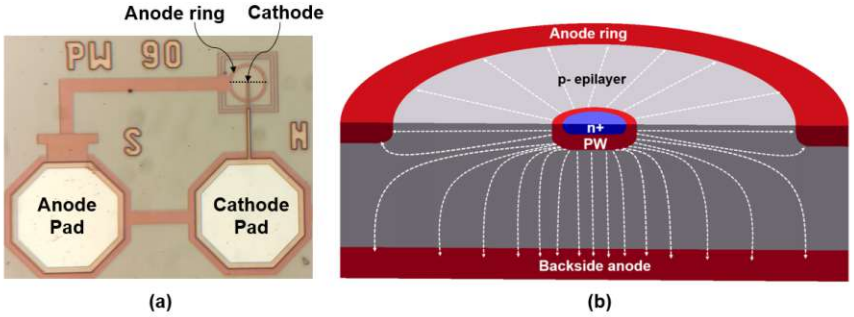

Figure 1. (**a**) Top view and (**b**) 3d schematic cross-section (not to scale) along the dashed line in sub-figure (**a**) of single-dot n^+/p-well APD fabricated in 0.35 µm CMOS technology. The cathode radius is 0.9 µm and the total diode radius is 14 µm.

Figure 2a shows a 2d plot of the electric field in the SD-APD at an operating voltage of 24.5 V (breakdown voltage = 25.2 V) simulated using the SILVACO Atlas. It can be seen that a semi-hemispherical multiplication region with a high electric field strength of 4.95×10^5 V/cm is formed at the junction of n^+/p-well with a width of ~0.4 µm at the critical field strength for impact ionization of 2×10^5 V/cm. Based on TCAD simulation results and according to the design rules and doping profiles associated with the 0.35 µm XO035 CMOS technology, the n^+ and p-well radii were set to 0.85 µm and 0.9 µm, respectively, to achieve a uniform high-field hemispherical distribution. It should be noted that the 0.85 µm size for the n^+ region radius is the minimum size available to form a round n^+ region based on the design rules and doping profiles of the 0.35 µm XO035 CMOS technology. Simulation results indicate that a p-well radius of less than 0.9 µm results in a non-uniform electric field distribution.

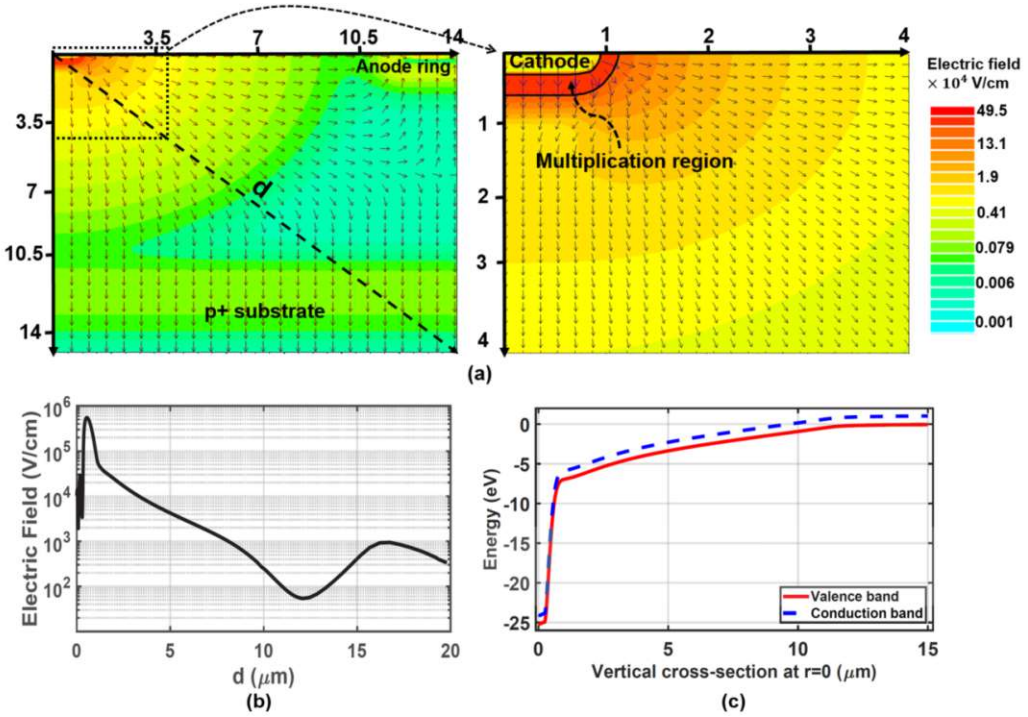

Figure 2. (**a**) 2d plot of the electric field distribution across the SD-APD obtained by TCAD simulations at the operating voltage of 24.5 V. Arrows indicate the local electric field direction. (**b**) Radial cross-section of the electric field along the dashed line (d) in the structure. (**c**) Energy band diagram along a vertical cross-section at r = 0 µm.

The electric field extends but lowers by moving radially away from the cathode towards the substrate, towards the anode ring and in a "diagonal" direction, as shown in Figure 2b. For example, at a "diagonal" distance of d = 10 µm from the origin of coordinates, the electric field is still ∼200 V/cm. Figure 2c shows the energy band diagram along a vertical cross-section at r = 0 µm. According to the energy band diagram when a photon is absorbed in the detection region, the generated electron and the hole are promptly separated by the electric field (drifting in opposite directions), and then, the electron drifts into the direction opposite to the electric field vector arrows towards the small multiplication region. This figure also shows that the reverse voltage of 24.5 V splits into about 7.5 V over the thick absorption region and 17 V over the multiplication region. In fact, due to the existence of the lateral component of the electric field, the peripheral carriers also have a chance to reach the multiplication region, where they can start impact ionization. Therefore, the whole diode area acts as the detection zone, which results in a large light-sensitive area. In addition, the drift-based carrier transport mechanism enhances the detector's speed performance.

Furthermore, since the electric field penetrates deeply into the structure (e.g., the electric field in a depth of 10 µm at r = 0 is ∼400 V/cm), the detection zone extends down to the p^+ substrate, which means the photo-generated carriers in the deep depth can drift towards the multiplication region and trigger an avalanche event. As a result, the large thickness of the detection region provides a high responsivity for long wavelengths. The responsivity and frequency response are assessed through TCAD simulations. The responsivity and bandwidth of 0.27 A/W and 1.25 GHz, respectively, have been obtained for the SD-APD. Such a concentrating electric field distribution causes a breakdown voltage of 25.2 V where the dark current reaches 1 µA [26] as can be seen in Figure 3a. However, the breakdown voltage varies as the radius of the p-well changes because the electric field distribution within the structure changes.

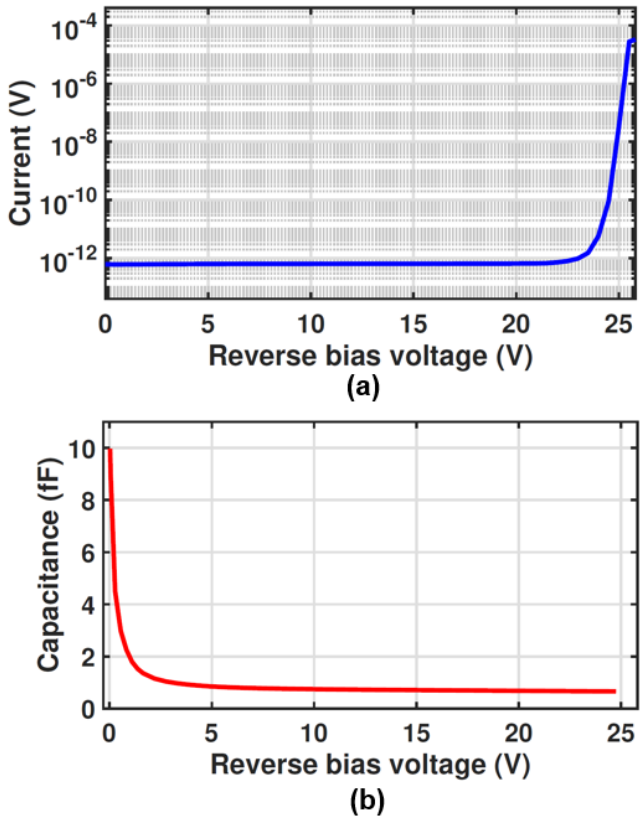

Figure 3. (**a**) Measured dark reverse characteristics and (**b**) Simulated capacitance of the SD-APD as a function of reverse bias voltage.

It is worth mentioning that the capacitance of the SD-APD is expected to be low due to the small area of the p/n junction. The capacitance of the SD-APD is evaluated using TCAD simulations as we cannot measure it due to the accuracy of our current equipment. Figure 3b presents the simulated capacitance of the SD-APD as a function of the reverse bias voltage. It can be seen that the capacitance is ∼10 fF at 0 V bias voltage and quickly drops to sub-Femto Farad values when increasing the reverse bias voltage. At the operating voltage of 24.5 V, the capacitance is 0.65 fF, which is significantly smaller than the typical values of a conventional planar CMOS APDs [17,27].

It is important to note that it is not possible to increase the size of the active area only by simply increasing the radius of the surface anode of the diode when a large active area is required (e.g., free space optical communications). Because, as previously shown (Figure 2), the electric field gradually decreases by moving radially away from the center, and therefore, at distances far from the center, the electric field is very weak or non-existent to drive carriers towards the cathode. Accordingly, the transfer mechanism is no longer carrier drift but carrier diffusion which decreases the responsivity and the bandwidth of the APD. The diffusion transport mechanism leads to a significant reduction in the bandwidth of the APD as the transit time of the photogenerated carriers to reach the cathode strongly increases. However, to increase the active area, a multi-dot structure is proposed, which can provide high responsivity and bandwidth, as detailed below.

3. Multi-Dot APD

Figure 4 shows the top view (a) and a 2d schematic cross-section (b) of the multi-dot APD (MD-APD) fabricated in the XO035 CMOS technology. The MD-APD is an array (5×5) of single-dot cathode/p-well structures, where the single cathodes are connected with tracks in metal layer 4 with a minimum width of 0.6 µm as shown in Figure 4a. The p^+ substrate is used as a shared backside anode. In addition, the dot cathode array is surrounded by a surface anode where the electric field of the boundary dots terminates, and defines the size of the diode. The APD is covered by the standard isolation and passivation stack to protect the fabricated device from environmental influences.

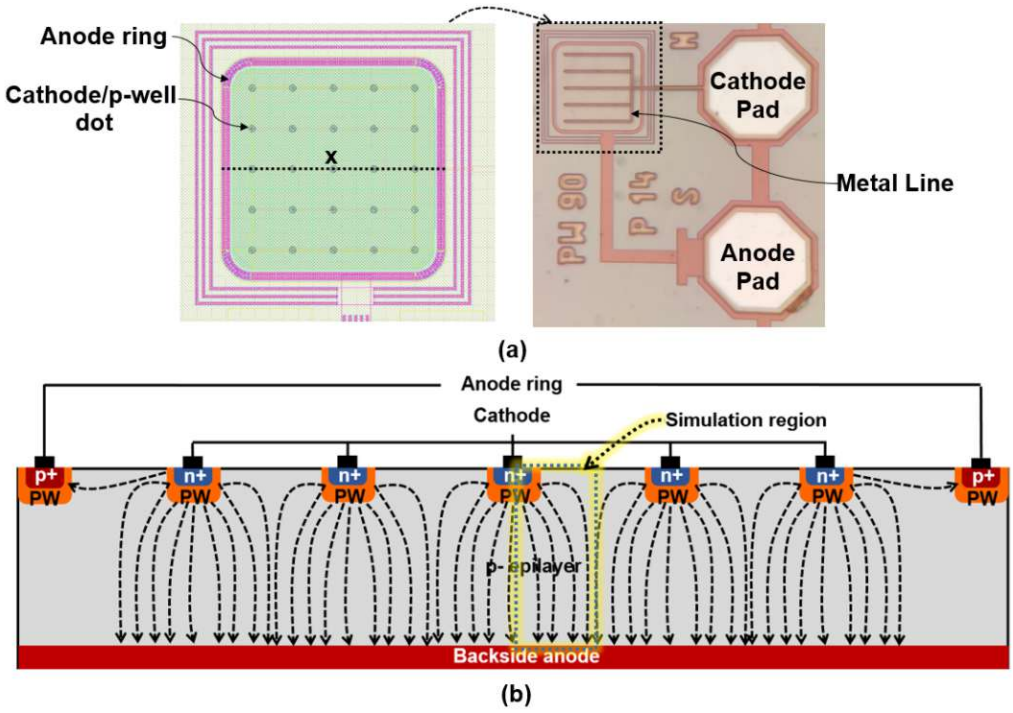

Figure 4. (**a**) Top view of the 5×5 array MD-APD fabricated in 0.35 µm CMOS technology. Left is the layout drawn in Cadence and right is a photograph of the fabricated chip. (**b**) is a schematic cross-section (not to scale) of the MD-APD along the dotted line (x) in sub-figure (**a**) left.

When the MD-APD is reversely biased, the hemispherical multiplication region is formed around each cathode dot. The area between the dots is fully depleted. The longest electric-field lines with the weakest electric field strength (between two dots) are high-lighted in Figure 4b. Therefore, the region under and between each cathode acts as a detection zone so that the photo-generated carriers are accelerated towards a cathode according to the local electric field direction. As a result, this structure achieves a large active area, while having a high responsivity and bandwidth.

Based on this approach, the active area can be easily enlarged by expanding the cathode dot array. In fact, the active area can be enlarged by increasing the number of cathode dots arrays and also by increasing the distance between the cathode dots (i.e., the array's pitch size). However, the pitch size of the array is an important parameter that affects the performance. Figure 5 is a zoomed top view of a cathode/p-well dot adjacent to other cathode/p-well dots in the array to visualize a half pitch and a half diagonal from the cathode center. The slowest response is expected if a photon is absorbed exactly in the center between four cathode/p-well dots, because this is where the longest drift distance along the silicon surface appears. This maximum lateral drift distance is $\frac{a}{\sqrt{2}}$, where a is the pitch of the n^+/p-well dot array.

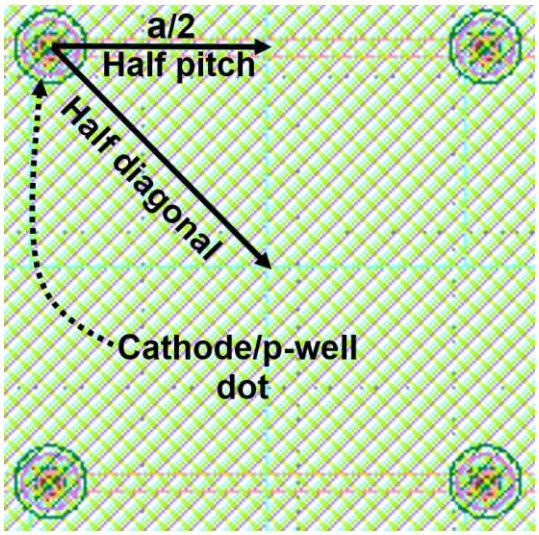

Figure 5. A zoomed top view of a cathode/p-well dot adjacent to other cathode/p-well dots in the array.

If the cathode dots are too far apart, there may not be a large enough electric field in the entire area between two cathodes to drive the photo-generated carriers to the cathode spot. Because, as discussed earlier, the electric field gradually drops by moving away from the center (multiplication region). Therefore, one cannot say that the entire area between two cathode/p-well dots is the detection zone, if the dots are too far apart. In addition, increasing the array's pitch size results in a lower bandwidth. This is due to the fact that the frequency response is determined by the transit time of photogenerated electrons to reach the cathode. The transit time depends on the carrier drift distance as well as the drift velocity, which is proportional to the local electric field strength. Accordingly, the transit time is expected to be higher in MD-APD with a larger array pitch size because the carrier drift distance increases and, additionally, the intensity of the electric field decreases over the larger distance from the cathode dots.

On the other side, in the case where the distance between two neighboring cathodes is small, more cathode dots are required to achieve the same active area compared to that of the MD-APD with larger pitch sizes. Increasing the number of cathode dots leads to an increase in the MD-APDs capacitance due to the fact that the MD-APDs capacitance is the sum of the capacitance of all single dots in the array plus parasitic capacitance (of metal tracks). In addition, in the MD-APDs with small pitch sizes, more metal lines are needed to connect the cathodes together, leading to a larger parasitic capacitance. Furthermore, a larger area of

the detection zone is covered by metal, which is an opaque material. Therefore this area is practically no longer called an absorption region because the incident photons are reflected by the metal before reaching the silicon. Accordingly, the pitch size of the array need to be optimized based on the requirements of the intended application.

We used TCAD simulations with ATLAS to estimate an optimal array pitch size (a) of the MD-APD. It should be noted that we could not simulate the whole structure of the MD-APD because it requires a 3d simulation. Simulations with Cartesian coordinates are performed for a 2d cross-section indicated in Figure 4b, which contains a half-cathode dot at the corner of a half-pitch-wide region. Figure 6 illustrates the electric field distribution for different pitch sizes a of 13, 10, 7, and 4 µm. These chosen simulation regions are sufficient because of symmetry reasons and boundary conditions of the simulator.

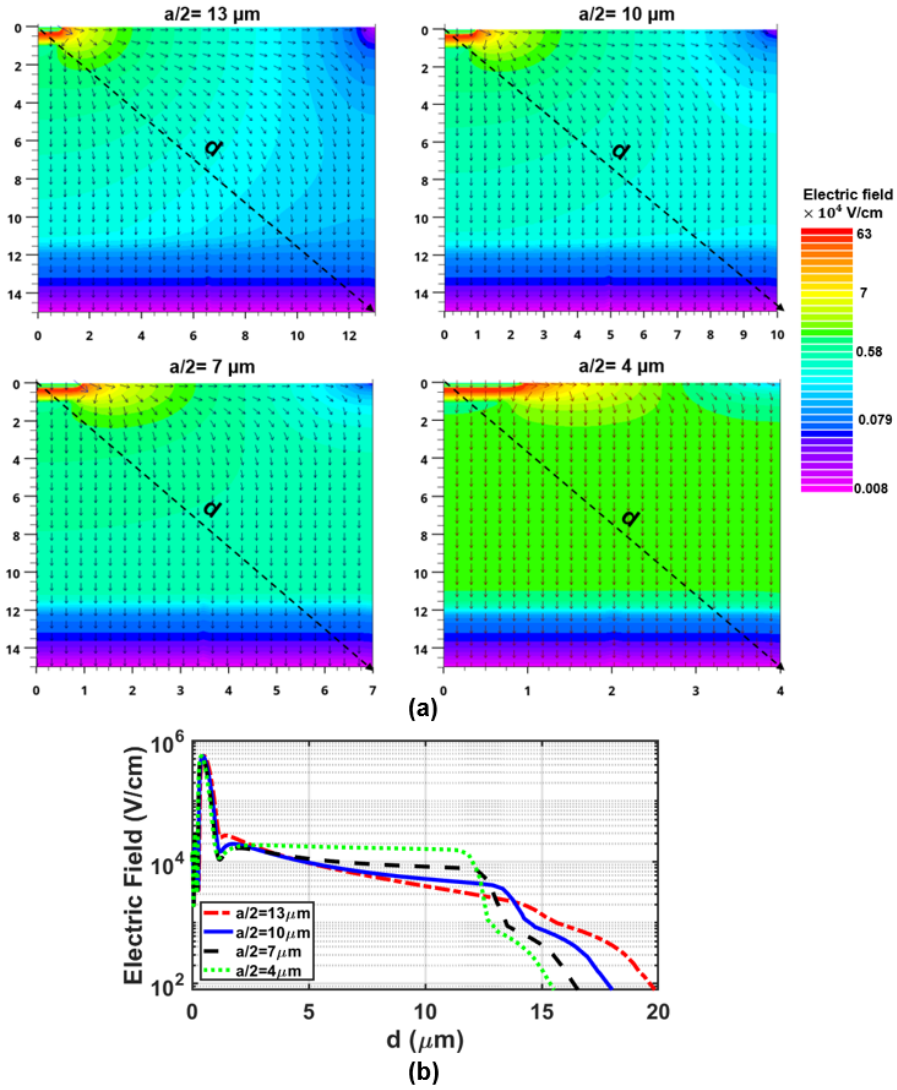

Figure 6. (**a**) 2d plot of the simulated electric field distribution in the 2d cross-section indicated in Figure 4b for different half pitch sizes $a/2$ of 13, 10, 7, and 4 µm at M = 40. (**b**) is the cross-section of the electric field along the dashed line (d) in sub-figure (**a**).

According to the electric field vector arrows, the electric field extends along the surface and then down towards the substrate. It is visualized that the strength of the electric field distributed across the detection zone decreases when the pitch size increases. It can be seen in Figure 6b that the electric field strength at a "diagonal" distance d of 10 µm from the origin of coordinates in the structure with a half pitch size of 4, 7, 10, and 13 µm are 16.3 kV/cm, 8.4 kV/cm, 5.3 kV/cm, and 4 kV/cm, respectively. A higher electric field

distributed across the detection region in smaller structures is expected to provide faster carrier drift transfer and thus lead to a higher bandwidth. Figure 7 shows the normalized frequency responses for the different half pitch sizes of 13, 10, 7, and 4 µm, at a wavelength of 675 nm and a gain of 40, obtained from TCAD simulations.

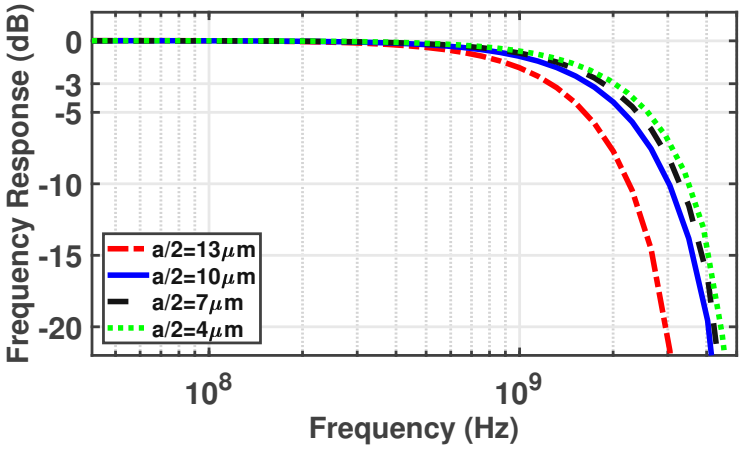

Figure 7. Normalized frequency responses at λ = 675 nm and M = 24 for different half pitch sizes of 13, 10, 7, and 4 µm, extracted from TCAD simulations.

Figure 7 demonstrates that a higher bandwidth is achieved by shrinking the distance between cathode dots because of the electron drift time reduction due to the shortening of the radial carrier drift distance and an increase in the electric field strength distributed across the detection zone. It is shown that the structures with an $a/2$ of 13, 10, 7, and 4 µm achieve the bandwidth of 1.25 GHz, 1.7 GHz, 1.85 GHz, and 2 GHz, respectively. Taking a closer look at the dependence of the bandwidth on the cathode dots distance, it can be seen that reducing the $a/2$ from 13 µm to 10 µm increases the bandwidth from 1.25 GHz to 1.7 GHz, while further reducing the distance provides less bandwidth improvement. This is due to the fact that in smaller structures, the $a/2$ is smaller than the depth of the structure, and hence the vertical carriers' transition from the deep depth (12 µm) limits the bandwidth, and therefore a further reduction of cathode dot distance has less influence on the bandwidth.

Now, the MD-APD can be designed according to TCAD simulation results and the above discussions. In the MD-APD design, a point that should be taken into account is that the bandwidth is limited by photo-generated carriers in the region between two adjacent cathode dots in the diagonal direction because it gives the longest drift distance (see Figure 5). The longest lateral drift distance along the silicon surface is $\frac{a}{2}\sqrt{2} = \frac{a}{\sqrt{2}}$. Here, the array pitch size of a = 14 µm is selected for the MD-APD structure in which the distance between two adjacent diagonal cathode dots is 20 µm. According to the simulated frequency response results for different distances of the cathode dots, it is expected that the MD-APD achieves a bandwidth between 1.7 GHz and 1.85 GHz, corresponding to $a/2$ = 7 µm and $a/2$ = 10 µm, respectively. Because carriers generated between two adjacent dots on the horizontal/vertical axis ($a/2$ = 7 µm) with a shorter drift distance and carriers generated in the area between two adjacent dots on the diagonal axis ($\frac{a}{\sqrt{2}}$ = 10 µm) with a longer drift distance contribute to the current flow (see Figure 5), so, the pitch a should be 14 µm. In the case where the pitch size of the array is a = 20 µm, the bandwidth reduction due to carrier transfer between diagonal cathodes is remarkable (see curve corresponds to $a/2$ = 13 µm from Figure 7) and thus the overall bandwidth significantly decreases. Therefore, an MD-APD shown in Figure 4 consisting of an array of 5 × 5 cathode dots with a pitch size of 14 µm can achieve a high bandwidth while providing an active area of 70 µm × 70 µm (exact active area: $5a^2 - a^2(1 - \pi/4) = 4858$ µm^2). However, MD-APDs with a smaller pitch size can achieve a slightly higher bandwidth, but at the cost of reducing the active area and increasing the capacitance.

Since there are different drift carrier path lengths in the MD structure, we should care about the timing jitter performance evaluation of the MD-APD. However, accurately calculating the jitter based on the transit time is challenging due to the variations in the electric field strength along the carrier's drift path. Therefore, we have conducted transient simulations under different conditions to estimate the largest possible jitter in the MD-APD. In the first simulation case, we have limited the incident light to the center of the structure (r = 0 to r = 0.5 µm), and therefore only the photogenerated carriers in the center reach the cathode with the shortest drift length. As a result, the rise time of the transient response corresponds to the shortest carrier transit time. The transient response (Figure 8) for this condition shows a rise time of 160 ps. In the second simulation case, we have limited the light irradiation to the edge of the half diagonal of the MD diode (r = 9.5 µm to r = 10 µm; analogously to the frequency response simulations of the MD structure above), resulting only in the photogenerated carriers with the longest drift path reaching the cathode. Accordingly, the rise time of the transient response corresponds to the longest carrier transit time. A rise time of 240 ps is obtained from the transient response results in this condition (Figure 8). The difference between these two values provides an estimation of the maximum jitter in the MD-APD, which is approximately 80 ps.

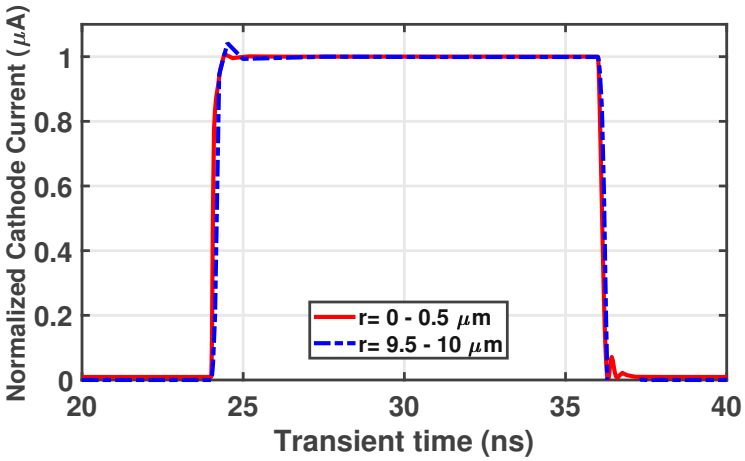

Figure 8. Transient response of MD-APD with a half diagonal 10 µm (pitch = 14 µm) at λ = 675 nm and M = 24, extracted from TCAD simulations.

4. Measurement Results

This section presents some key performance characteristics like capacitance, responsivity, and gain, as well as the bandwidth of the MD-APD, consisting of an array of 5 × 5 cathode dots with a pitch size of 14 µm fabricated in 0.35 µm CMOS technology. Measurements have been done on the wafer using a wafer probe station at 25 °C temperature regulated by a thermo chuck. A 675 nm laser source coupled with a multi-mode fiber with a core diameter of 62.5 µm feeds the light to the device under test. A Keysight B2987 electrometer was used to supply the voltage and measure the current.

4.1. Dark Reverse Characteristic and Capacitance

Figure 9a illustrates the dark reverse characteristics of the MD-APD as a function of the reverse bias voltage. The breakdown voltage of the MD-APD is 24.5 V (where the dark current reaches 1 µA) which is 0.7 V lower than that of the SD-APD. This is due to the fact that the electric field distribution in the multi-dot structure is different compared to that in the SD-APD.

Figure 9b illustrates the capacitance of the MD-APD, measured with an LCR meter Agilent 4284A at different reverse bias voltages with a frequency of 1 MHz and an ac amplitude of 100 mV. To subtract the effect of pad capacitance and measurement cables, the measurement was calibrated with an open structure (same pad size and metal track used for the MD-APD) on the same wafer.

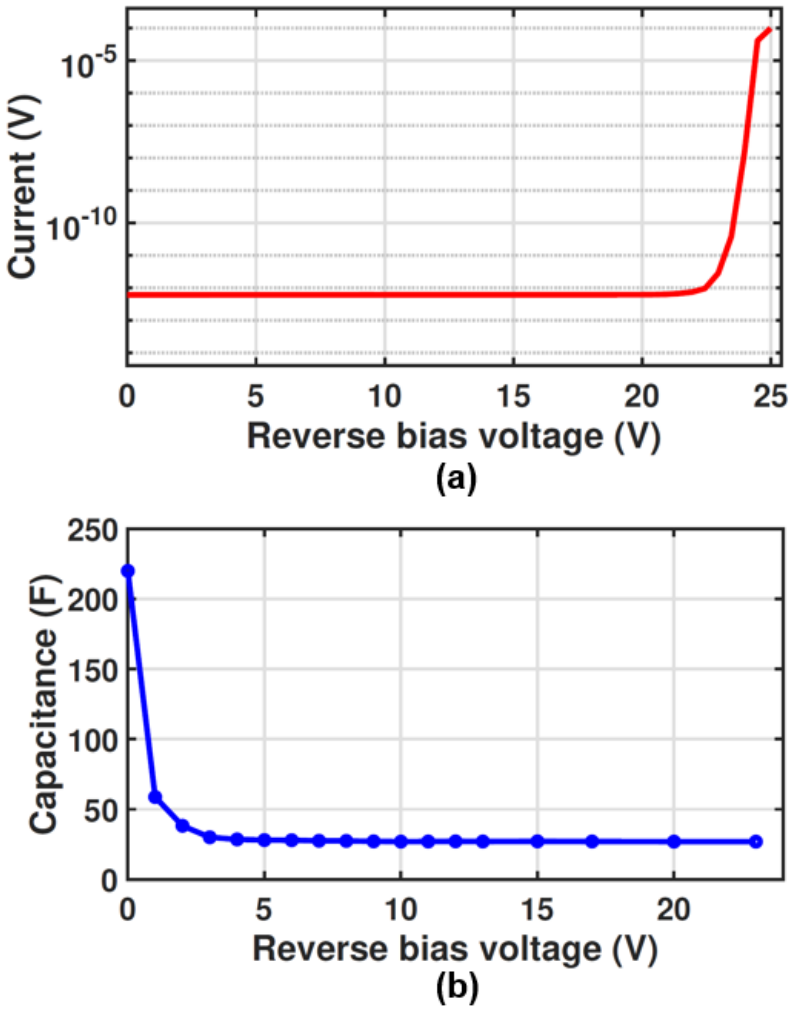

Figure 9. (**a**) Dark reverse characteristics and (**b**) capacitance of the MD-APD as a function of reverse bias voltage.

The total capacitance of the MD-APD includes the capacitance of the p-n junctions of all single cathode dots and the parasitic capacitance of the metal tracks used to connect the cathode dots. The high capacitance of 220 fF at the zero voltage originates from the junction capacitance of the cathode dots which was estimated to be about 10 fF from the TCAD simulation result for SD-APD (see Figure 3b). As the reverse bias voltage increases, the capacitance decreases rapidly to 27 fF, of which 16.25 fF can be estimated as the junction capacitance of the cathode dots (25 $\times$ 0.65 fF), and the 10.75 fF left can be attributed to parasitic metal track capacitances. It is worth noting that the advantage of the low capacitance of this APD is significant for designing an optical receiver with a high data rate. Because in the design of the transimpedance amplifier (TIA), one critical factor limiting the bandwidth is the diode capacitance.

4.2. Responsivity and Gain

The photodetection characterization of the MD-APD has been done for λ = 675 nm. A fiber splitter is used to split up the light to feed it to the optical power meter from Thorlabs for power monitoring and to the fiber that feeds the light to the device under test. Based on the photocurrent characteristics, the gain and responsivity as a function of reverse bias voltage are obtained, where the dark current has been subtracted. Figure 10a shows the responsivity and gain as a function of the reverse bias voltage at an optical power (op) of 200 nW.

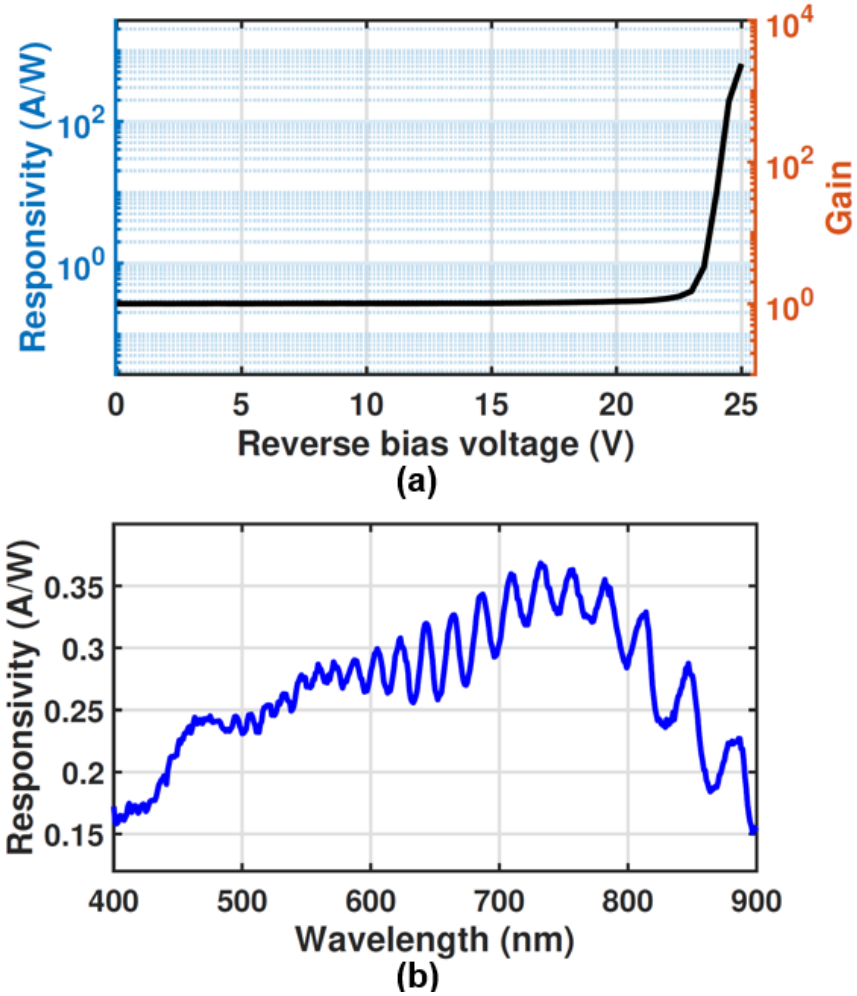

Figure 10. (**a**) Responsivity (left) and gain (right) of the MD-APD as a function of reverse bias voltage at λ = 675 nm and op = 200 nW. (**b**) Responsivity of MD-APD vs. wavelength (400 nm–900 nm) at M = 1 and op = 2 nW.

The APD shows a responsivity of 0.27 A/W at low bias voltages (Vop = 1 V) without gain (M = 1), which gives a quantum efficiency of about 50%. It is observed that the gain and responsivity are constant in a wide voltage range and then increase with a reverse bias voltage larger than about 20 V. At the operating voltage of 24 V, the responsivity and gain are 9.7 A/W and 36, respectively. However, the maximum achievable responsivity and gain depend on the optical power and decrease for higher optical power because of the saturation effect of the multiplication process at high optical powers. It should be mentioned that the diode can be biased at lower operating voltages, to work in the unamplified mode in the application where the optical power is high enough to be detected without amplification.

The spectral distribution of the unamplified responsivity (M = 1) is shown in Figure 10b. A monochromator (Digikrom CM110) is used to sweep the wavelength from 400 nm to 900 nm by steps of 1 nm. The light source is calibrated to provide a constant optical power of 2 nW over the spectrum using an optical power meter and a coupled variable optical attenuator. It can be seen that at λ = 675 nm and op = 2 nW, the responsivity of 0.27 A/W is achieved, which is as expected since the unamplified responsivity is independent of the optical power [25].

The λ-dependent fluctuations in the spectral responsivity originate from the formation of standing waves in the isolation and passivation stack covering the active region. Additionally, these layers lead to reflections for certain wavelengths that reduce the responsivity because not each incident photon is transmitted to the silicon (detection region).

Accordingly, higher responsivities can be achieved if the silicon surface is covered by an anti-reflection layer that transmits almost all incoming photons into the silicon. Nevertheless, the spectral responsivity shows an average unamplified responsivity of 0.33 A/W in the spectral range between 700 nm and 800 nm, which is due to the thick detection zone as expected from the TCAD simulation results. Furthermore, the maximum unamplified responsivity of 0.37 A/W is achieved at the wavelength of 732 nm.

4.3. Frequency Response

Figure 11 illustrates the normalized frequency response of the MD-APD measured at the operating voltage of 24 V (R = 9.7 A/W and M = 36) and an optical power of 200 nW (λ = 675 nm) using a vector network analyzer (Rohde&Schwarz ZNB8).

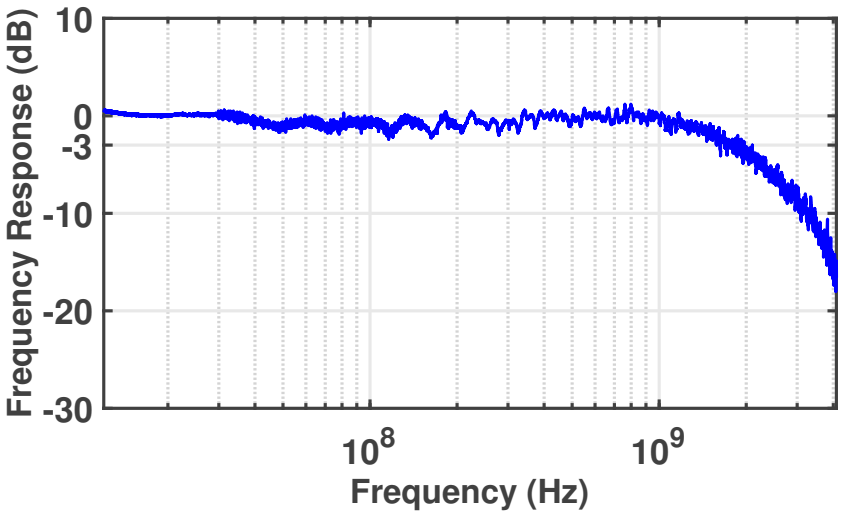

Figure 11. Normalized frequency responses at Vop = 24 V, op = 200 nW (λ = 675 nm).

The frequency response indicates a 3-dB bandwidth of 1.8 GHz, which is a promising value for reach-through-based APDs, because such structures show limited bandwidths due to a high carrier drift time in their thick absorption zone. Such a high bandwidth obtained for the MD-APD is because of the electron drift time reduction due to the large radius of the half-sphere high-field region throughout the structure. The measured 1.8 GHz bandwidth for the MD-APD with a pitch size of 14 µm demonstrates a good agreement between the simulation and the experimental results, as we expected a bandwidth between 1.7 GHz and 1.85 GHz from the simulation results.

5. Discussion

The research work presented in this study focuses on the development of a dot avalanche photodiode (APD) that overcomes the trade-off between the light-sensitive area and capacitance of planar APDs commonly used in optical communication systems. One of the main challenges with planar APDs is the need to decouple the light-sensitive area from the P/N-junction area to reduce the capacitance while maintaining the light-sensitive area. The proposed dot APD achieves this by using the lateral distribution of the electric field throughout the diode, enabling vertical and peripheral charge collection.

The innovative aspect of this work lies in enlarging the light-sensitive area by expanding the cathode dot array by offering low capacitance. The base for this is the very low capacitance of a single-dot APD at a large light-sensitive area. The performance of the multi-dot APD compared with various Si CMOS APDs shows a significant improvement in the responsivity-bandwidth product (R-BW product) of 17.46 $\frac{A}{W}$·GHz, corresponding to the responsivity and bandwidth of R = 9.7 A/W and BW = 1.8 GHz, respectively. Additionally, the capacitance of the multi-dot APD is four times smaller than that of planar APDs, while maintaining a comparable active area. Furthermore, the multi-dot APD shows significant

improvement in scalability and the ability to maintain its bandwidth and responsivity performance during up/down scaling.

It is worth emphasizing that the responsivity and frequency response of the MD-APD are independent of the array size but are affected by the array pitch size. This is due to the fact that the distribution of the electric field is independent of the number of cathodes in the array, but it changes with the change in the distance between the cathodes. However, the capacitance is proportional to the array size as the number of cathodes and metal connection length changes in different array sizes. In addition, as the drift path of carriers only depends on the array pitch size (i.e., shortest and longest paths) and is independent of the array size, the timing jitter is the same for different array sizes. Therefore, designing MD-APDs with different array sizes follows the same approach. This is one of the advantages of these structures, which makes it possible to easily expand the active area while maintaining the performance. These results demonstrate the superiority of the multi-dot APD over the state-of-the-art APDs and make it a promising candidate for a wide range of applications.

To better highlight, the contribution of this work over the state-of-the-art, the key performance parameters of the MD-APD are compared with various Si CMOS APDs and shown in Table 1.

Table 1. Performance comparison of linear-mode APDs.

Parameters	Ref. [17]	Ref. [28]	Ref. [19]	Ref. [24]	Ref. [14]	Ref. [25]	This Work
Structure	n^+/p-well RT-APD *	p^+/n-well APD	n^+/p-well RT-APD *	p^+/n-well CA-APD ⊕	Double p-well/ n-well APD	n^+/n-well EFLC-APD #	n^+/p-well MD-APD
Technology	0.35 µm	0.25 µm	0.35 µm	0.35 µm	45 nm	0.18 µm	0.35 µm
Active area	r = 43 µm	10 × 10 µm^2	r = 30 µm	40 × 40 µm^2	20 × 20 µm^2	r = 19 µm	70 × 70 µm^2
Capacitance	125 fF	-	≥100 fF	1 fF	-	≤1 fF	27 fF
Operating voltage	63 V	12.2 V	47 V	68 V	20.8 V	69 V	24 V
Optical power	500 nW	1 mW	1 µW	2 µW	100 µW	200 nW	200 nW
Wavelength	670 nm	850 nm	670 nm	830 nm	850 nm	675 nm	675 nm
Gain	50	16.7	20	43.9	23	80	36
Responsivity	20.5 A/W	0.2 A/W	7.4 A/W	13.17 A/W	0.56 A/W	32 A/W	9.7 A/W
Bandwidth	850 MHz	5.6 GHz	2.3 GHz	275 MHz	8.4 GHz	1.6 GHz	1.8 GHz
R-BW product	17.4 $\frac{A}{W}$·GHz	1.1 $\frac{A}{W}$·GHz	17.02 $\frac{A}{W}$·GHz	3.6 $\frac{A}{W}$·GHz	4.7 $\frac{A}{W}$·GHz	51.2 $\frac{A}{W}$·GHz	17.46 $\frac{A}{W}$·GHz

* RT-APD: reach-through APD; ⊕ CA-APD: current assisted APD; # EFLC-APD: electric field line crowding APD.

6. Conclusions

The characterization of a CMOS-integrated dot avalanche photodiode is presented. It is shown that a hemispherically uniform high electric field is formed around the central cathode, which serves as the multiplication region, and a lower electric field penetrates radially throughout the diode to guide charge carriers from the entire diode volume towards the multiplication region. Accordingly, because of the high electric field distributed over the structure, the presented APD offers a large light-sensitive area while achieving high responsivity and bandwidth at long wavelengths due to its thick absorption zone and drift-based carrier transport. The active area of 70 µm × 70 µm is achieved with the MD-APD, consisting of an array of 5 × 5 cathode/p-well dots with a pitch size of 14 µm. However, the active area can easily be further enlarged by expanding the dot array (keeping the same pitch), without changing the bandwidth and the responsivity. A responsivity-bandwidth product (R-BW product) of 17.46 $\frac{A}{W}$·GHz, corresponding to the responsivity and bandwidth of R = 9.7 A/W and BW = 1.8 GHz, respectively, is achieved for the MD-APD at λ = 675 nm and at an operating reverse voltage of 24 V. The 5 × 5 MD-APD offers the advantage of a low capacitance of 27 fF.

Author Contributions: Conceptualization, S.S.K.P., H.Z.; methodology and software simulation, S.S.K.P.; layout, K.S.-H.; experimental setup preparation, S.S.K.P., B.G. and M.H.; acquisition of experimental data S.S.K.P. and B.G.; data curation, writing—original draft preparation, S.S.K.P.; writing—review and editing, S.S.K.P. and H.Z.; supervision, project administration and funding acquisition, H.Z. All authors have read and agreed to the published version of the manuscript.

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References

1. Joo, J.E.; Lee, M.J.; Park, S.M. A CMOS optoelectronic receiver IC with an on-chip avalanche photodiode for home-monitoring LiDAR sensors. *Sensors* **2021**, *21*, 4364. [CrossRef] [PubMed]
2. Yu, X.; Chen, X.; Song, Y.; Zhang, L.; Jiang, J.; Wang, T.; Tong, S. Design and evaluation of a high-sensitivity digital receiver with the finite impulse response filter algorithm for free-space laser communication. *Opt. Eng.* **2020**, *59*, 036105. [CrossRef]
3. Hossain, M.M.; Ray, S.; Cheong, J.S.; Qiao, L.; Baharuddin, A.N.; Hella, M.M.; David, J.P.; Hayat, M.M. Low-noise speed-optimized large area CMOS avalanche photodetector for visible light communication. *J. Light. Technol.* **2017**, *35*, 2315–2324. [CrossRef]
4. Zheng, H.; Ma, R.; Liu, M.; Zhu, Z. High sensitivity and wide dynamic range analog front-end circuits for pulsed TOF 4-D imaging LADAR receiver. *IEEE Sens. J.* **2018**, *18*, 3114–3124. [CrossRef]
5. Song, H.Z. Avalanche photodiode focal plane arrays and their application to laser detection and ranging. In *Advances in Photodetectors-Research and Applications*; IntechOpen: London, UK, 2018.
6. Shcherbakova, O.; Pancheri, L.; Dalla Betta, G.F.; Massari, N.; Stoppa, D. 3D camera based on linear-mode gain-modulated avalanche photodiodes. In Proceedings of the 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, San Francisco, CA, USA, 17–21 February 2013; pp. 490–491.
7. Dong, Y.; Wang, W.; Xu, X.; Gong, X.; Lei, D.; Zhou, Q.; Xu, Z.; Yoon, S.F.; Liang, G.; Yeo, Y.C. Germanium-tin on silicon avalanche photodiode for short-wave infrared imaging. In Proceedings of the 2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers, Honolulu, HI, USA, 9–12 June 2014; pp. 1–2.
8. Iiyama, K.; Takamatsu, H.; Maruyama, T. Hole-Injection-Type and Electron-Injection-Type Silicon Avalanche Photodiodes Fabricated by Standard 0.18 µm CMOS Process. *IEEE Photonics Technol. Lett.* **2010**, *22*, 932–934. [CrossRef]
9. Pancheri, L.; Dalla Betta, G.F.; Stoppa, D. Low-Noise Avalanche Photodiode With Graded Junction in 0.15 µm CMOS Technology. *IEEE Electron. Device Lett.* **2014**, *35*, 566–568. [CrossRef]
10. Iiyama, K.; Shimotori, T.; Gyobu, R.; Hishiki, T.; Marayama, T. 10 GHz bandwidth of Si avalanche photodiode fabricated by standard 0.18 µm CMOS process. In Proceedings of the 2014 OptoElectronics and Communication Conference and Australian Conference on Optical Fibre Technology, Melbourne, Australia, 6–10 July 2014; pp. 243–244.
11. Chou, F.P.; Wang, C.W.; Li, Z.Y.; Hsieh, Y.C.; Hsin, Y.M. Effect of deep N-well bias in an 850-nm Si photodiode fabricated using the CMOS process. *IEEE Photonics Technol. Lett.* **2013**, *25*, 659–662. [CrossRef]
12. Nayak, S.; Ahmed, A.H.; Sharkia, A.; Ramani, A.S.; Mirabbasi, S.; Shekhar, S. A 10-Gb/s- 18.8 dBm Sensitivity 5.7 mW Fully-Integrated Optoelectronic Receiver With Avalanche Photodetector in 0.13 µm CMOS. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 3162–3173. [CrossRef]
13. Lee, M.J.; Choi, W.Y. A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain-bandwidth product. *Opt. Express* **2010**, *18*, 24189–24194. [CrossRef] [PubMed]
14. Zhi, W.; Quan, Q.; Yu, P.; Jiang, Y. A 45 nm CMOS Avalanche Photodiode with 8.4 GHz Bandwidth. *Micromachines* **2020**, *11*, 65. [CrossRef]
15. Lee, M.J. First CMOS silicon avalanche photodetectors with over 10-GHz bandwidth. *IEEE Photonics Technol. Lett.* **2015**, *28*, 276–279. [CrossRef]
16. Kim, Y.S.; Jun, I.S.; Kim, K.H. Design and characterization of CMOS avalanche photodiode with charge sensitive preamplifier. *IEEE Trans. Nucl. Sci.* **2008**, *55*, 1376–1380. [CrossRef]
17. Steindl, B.; Enne, R.; Schidl, S.; Zimmermann, H. Linear mode avalanche photodiode with high responsivity integrated in high-voltage CMOS. *IEEE Electron. Device Lett.* **2014**, *35*, 897–899. [CrossRef]

18. Cheng, Z.; Xu, H.; Chen, Y. Design of low noise avalanche photodiode single element detectors and linear arrays through CMOS process. *Proc. SPIE* **2019**, *10978*, 70–77.
19. Steindl, B.; Jukić, T.; Zimmermann, H. Optimized silicon CMOS reach-through avalanche photodiode with 2.3-GHz bandwidth. *Opt. Eng.* **2017**, *56*, 110501–110501. [CrossRef]
20. Enne, R.; Steindl, B.; Zimmermann, H. Speed optimized linear-mode high-voltage CMOS avalanche photodiodes with high responsivity. *Opt. Lett.* **2015**, *40*, 4400–4403. [CrossRef]
21. Morimoto, K.; Charbon, E. High Fill-Factor Miniaturized SPAD Arrays With a Guard-Ring-Sharing Technique. *Opt. Express* **2020**, *28*, 13068–13080. [CrossRef]
22. Lee, M.J.; Rucker, H.; Choi, W.Y. Effects of guard-ring structures on the performance of silicon avalanche photodetectors fabricated with standard CMOS technology. *IEEE Electron. Device Lett.* **2011**, *33*, 80–82. [CrossRef]
23. Poushi, S.S.K.; Mahmoudi, H.; Hofbauer, M.; Steindl, B.; Schneider-Hornstein, K.; Zimmermann, H. Experimental and simulation study of fill-factor enhancement using a virtual guard ring in n/p-well CMOS single-photon avalanche diodes. *Opt. Eng.* **2021**, *67105*, 1. [CrossRef]
24. Jegannathan, G.; Ingelberts, H.; Boulanger, S.; Kuijk, M. Current assisted avalanche photo diodes (CAAPDs) with separate absorption and multiplication region in conventional CMOS. *Appl. Phys. Lett.* **2019**, *115*, 132101. [CrossRef]
25. Poushi, S.K.; Goll, B.; Schneider-Hornstein, K.; Hofbauer, M.; Zimmermann, H. CMOS Integrated 32 A/W and 1.6 GHz Avalanche Photodiode Based on Electric Field-Line Crowding. *IEEE Photonics Technol. Lett.* **2022**, *34*, 945–948. [CrossRef]
26. Koyama, A.; Shimazoe, K.; Takahashi, H.; Hamasaki, R.; Orita, T.; Onuki, Y.; Otani, W.; Takeshita, T.; Kurachi, I.; Miyoshi, T.; et al. Development of Pixelated Linear Avalanche Integration Detector Using Silicon on Insulator Technology. In Proceedings of the International Symposium on Radiation Detectors and Their Uses (ISRD2016), Tsukuba, Japan, 18–21 January 2016; p. 030006.
27. Napiah, Z.A.F.M.; Gyobu, R.; Hishiki, T.; Maruyama, T.; Iiyama, K. Characterizing Silicon Avalanche Photodiode Fabricated by Standard 0.18 µm CMOS Process for High-Speed Operation. *IEICE Trans. Electron.* **2016**, *99*, 1304–1311. [CrossRef]
28. Lee, M.J.; Lee, J.M.; Rücker, H.; Choi, W.Y. Bandwidth improvement of CMOS-APD with carrier-acceleration technique. *IEEE Photonics Technol. Lett.* **2015**, *27*, 1387–1390.

2.6 Large Active Area, Low Capacitance Multi-dot PIN Photodiode in 0.35 μm CMOS Technology, "IEEE Photonics Journal 2024"

Large Active Area, Low Capacitance Multi-Dot PIN Photodiode in 0.35 μm CMOS Technology

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***Abstract*—This article presents a multi-dot PIN photodiode structure that addresses the inherent trade-off between the light-sensitive area and capacitance in conventional planar photodiodes commonly used in optical communication systems. This structure is a combination of several connected cathode dots and with a shared anode. The radial distribution of the electric field surrounding each cathode dot facilitates both vertical and peripheral charge collection, and accordingly, enables the region beneath and between the dots to function as a light-sensitive area with fast carrier drift. The key innovation of this work lies in the flexibility of the multi-dot structure for easy enlargement of the light-sensitive area by expanding the dot array, while still maintaining a small capacitance. Experimental results show that a 5 × 5 multi-dot PIN photodiode with a pitch of 20 μm corresponding to an active area of 100 μm × 100 μm achieves a capacitance of 48.8 fF, a responsivity of 0.294 A/W at a wavelength of 675 nm, and a bandwidth of 660 MHz at an operating voltage of 10 V. With a pitch of 15 μm that provides a light-sensitive area of 70 μm × 70 μm, the bandwidth increases to 930 MHz.**

***Index Terms*—CMOS, multi-dots photodiodes, light-sensitive area, low capacitance, PIN photodiodes, peripheral charge collection.**

I. Introduction

To ATTAIN high bandwidth, high transimpedance, and low noise in optical sensors and receivers, it is essential to have a photodetector with a small capacitance [1]. In image sensor pixels, there are photodiodes with an exceptionally low capacitance [2], [3], [4]. These photodiodes typically exhibit a capacitance in the order of femtofarad when employed in a small light-sensitive area of around 1 μm^2. However, many applications of optical sensors require a larger light-sensitive area to enable efficient coupling of the light signal to the photodiodes [5], [6]. The capacitance of P/N junctions in photodiodes shows a direct relationship with the photodiode's area [7]. As a result, expanding the sensitive area necessitates an increase in the size of the P/N junction, subsequently leading to an increase in the junction's capacitance. This trade-off between capacitance and detection area is commonly observed in planar photodiodes. Hence, it becomes necessary to decouple the P/N junction area from the light-sensitive area in order to achieve a larger light-sensitive region without simultaneously increasing the capacitance. This decoupling can be achieved by implementing lateral depletion techniques.

Photodiodes based on finger structure have been proposed to achieve low capacitance [8], [9], [10]. In [10] by employing a lateral PIN diode configuration with one N+ finger positioned between two P+ stripes in silicon, they could achieve a capacitance value of approximately 6 fF for a 30 × 30 μm^2 diode. However, these photodiodes offer a responsivity and bandwidth of 0.45 A/W and 110 MHz, respectively, at a wavelength of 660 nm and a reverse-bias voltage of 4 V. A further capacitance reduction can be achieved by shrinking the cathode finger to a cathode dot.

[11], [12], [13] presented spot and dot PIN photodiodes with a capacitance down to 1.14 aF/μm ^{2}. These photodiodes possess a small hemispherical cathode dot in a thick low-doped epitaxial layer and a vertical plus radial electric field to collect lateral charge carriers from the whole diode volume towards the cathode. Capacitances down to 0.8 fF have been achieved at a light-sensitive area of 706.9 μm^2. A responsivity of 0.38 A/W and and bandwidth of 310 MHz, at a wavelength of 635 nm and and a reverse-bias voltage of 30 V are achieved for such structures.

It is worth noting that in this configuration, the active region cannot be excessively enlarged due to the gradual decrease in the electric field as the radial distance from the center increases. Consequently, at large distances away from the center, the electric field becomes too weak to effectively drive carriers [14], [15]. In [16] we introduced an n+/p-well dot avalanche photodiode in 0.35 μm CMOS technology to enhance area and bandwidth. The APD was baised at an operating voltage of 24 V.

In this article, we present a multi-dot PIN photodiode structure based on the very low capacitance single-dot PIN photodiode, which can provide a large active area with low capacitance. The motivation of this is to increase the light-sensitive area of the photodiode compared to that used in ref. [12], where an ultra-sensitive optical receiver with a single-dot pin photodiode with a light-sensitive area of 706 μm ^{2} was introduced. In receivers exploiting the principle of capacitive-feedback transimpedance amplifiers like in [12], the low capacitance of the photodiode is essential for achieving best sensitivities. A capacitance of 48.8 fF is achieved for a 5 × 5 multi-dot PIN photodiode with an active area of 100 μm × 100 μm. Additionally, this

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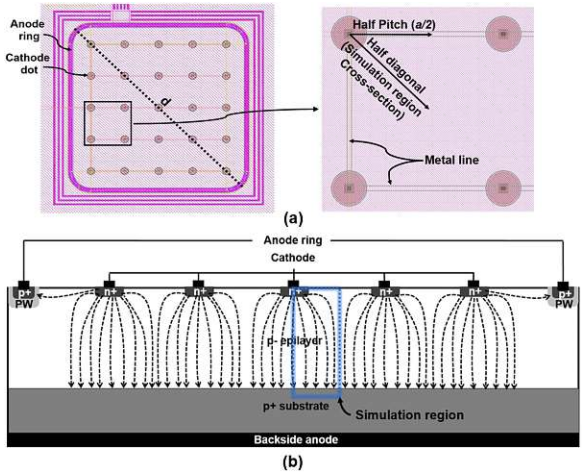

Fig. 1. (a) Top view of layout drawn in Cadence of the 5 × 5 array MD-PIN photodiode. Right is a zoomed top view of a cathode dot adjacent to other cathode dots in the array. (b) is a schematic cross-section (not to scale) of the MD-APD along the dotted line (d) in sub-figure (a-left).

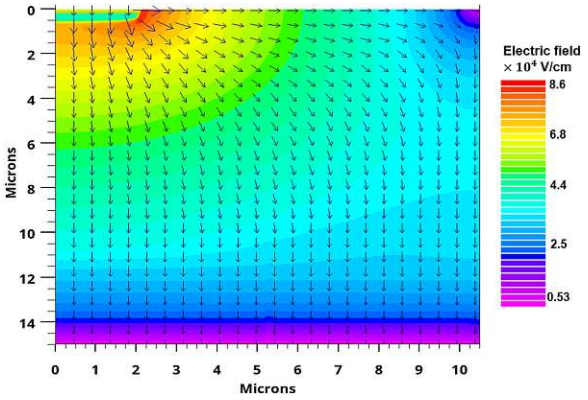

Fig. 2. (a) 2D plot of the simulated electric field distribution in the 2D cross-section indicated in Fig. 1(a) (right) with a half diagonal of 10.5 μm (i.e., a = 15 μm) at an operating voltage of 10 V. Arrows represent the local electric field direction.

photodiode demonstrates a responsivity and bandwidth of 0.294 A/W and 660 MHz, respectively, at a wavelength of 675 nm and a reverse-bias voltage of 10 V. Moreover, the active area can be readily expanded by enlarging the dot array while maintaining a small capacitance. Section II presents the device structure and design approach. In Section III experimental characterizations are discussed, and Section IV concludes the article.

II. Device Structure and Design Approach

Fig. 1 illustrates the top view (a) and a 2 d schematic cross-section (b) of the multi-dot (MD) PIN-photodiode structure. The MD-PIN configuration comprises an array (5 × 5) of semi-hemispherical high-doped n+ regions with a radius of 2 μm as cathode dots, which all are connected with tracks in metal layer 4 with a minimum width of 0.6 μm as shown in Fig. 1(a). The cathode dots are embedded in a lightly p-doped epitaxial layer (p-epi) with a doping concentration of $\sim 2 \times 10^{13}$ cm $^{-3}$ and a thickness of $\sim$12 μm. This cathode array is surrounded by a surface anode ring that defines the overall diode size. The p+ substrate serves as a shared backside anode. It should be mentioned that the MD-PIN photodiode is fabricated in the 0.35 μm CMOS modular optical sensor technology platform (XO035) of X-FAB semiconductor foundries without any process modification because this technology is a pin-photodiode process.

The electric field distribution inside the structure is studied using TCAD simulations with ATLAS [17]. It is important to emphasize that a 3 d simulation would be necessary to accurately model the entire structure of the MD-PIN configuration requiring a huge number of grid points and unacceptably long computation time. Nevertheless, a 2 d simulation focusing on a cross-section that features a half-cathode dot positioned at the corner of a half-pitch-wide region (see Fig. 1(a) (right)) can still provide valuable insights and reliable performance estimations because of symmetry reasons and boundary conditions of the simulator.

Fig. 2 shows a 2d plot of the electric field for the 2d cross-section region indicated in Fig. 1(b) by a blue rectangle at an operating voltage of 10 V (breakdown voltage = 63 V). It can be seen that, unlike planar structures that possess solely a homogenous vertical electric field, MD-PIN photodiodes feature an electric field that extends radially throughout the diode, which can be used for vertical and peripheral charge collection. When the diode is reversely biased, a spherically uniform high electric field is formed around each cathode dot, and a weaker (but still high) electric field extends radially throughout the diode to guide charge carriers from the entire diode volume towards the cathode dots.

Therefore, the region under and between all cathodes acts as a detection zone. When a photon is absorbed in these areas, the generated electron-hole pair is instantly separated by the electric field (see the field lines in Fig. 1(b)), causing them to drift in opposite directions. Then, the electron is effectively guided towards a respective cathode dot based on the local electric field direction, even that generated in the periphery between the cathode dots. This unique feature is attributed to the existence of the lateral component of the electric field. Thus, the entire diode area, including the spaces between cathode dots, functions as an extended detection zone. This characteristic significantly contributes to achieving a large light-sensitive area and efficient peripheral charge collection.

In addition, the capacitance of the MD-PIN photodiode is expected to be low because of the small areas of the p/n junctions. In fact, the total capacitance is the sum of the capacitance of all cathode dots in the array plus parasitic capacitance (of metal tracks).

It is worth knowing that the active area of the MD-PIN photodiode can be readily expanded by enlarging the cathode dot array. This can be achieved by increasing the number of cathode dot arrays or by adjusting the distance between the cathode dots, known as the array's pitch size. However, it is important to note that different array pitch sizes lead to different electric field distributions inside the structure. Fig. 3 shows a radial (at the surface) and a vertical (at r = 0) cross-sections of the electric field in the simulation region indicated in Fig. 1(b)

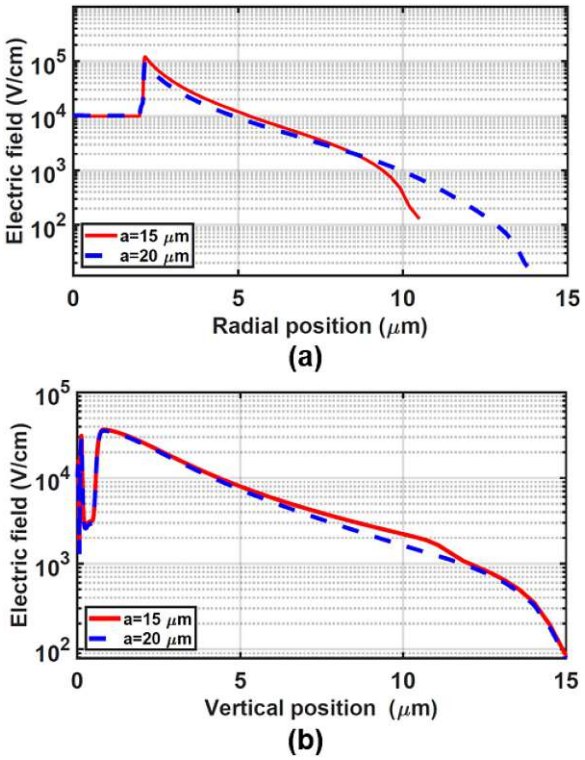

Fig. 3. (a) Radial (at the surface) and (b) vertical (at r = 0) cross-sections of the electric field in the simulation region indicated in Fig. 1 for two different pitches of $a = 15$ μm and $a = 20$ μm at an operating voltage of 10 V.

for two different pitches of $a = 15$ μm and $a = 20$ μm. It can be observed that the strength of the electric field within the detection zone decreases as the pitch size increases. Accordingly, it is crucial to optimize the pitch size of the array as it is a significant parameter that directly impacts the overall performance of the photodiode.

If the cathode spots in the MD-PIN photodiode are spaced too far apart, it can result in an insufficient electric field across the entire area between two cathodes to drive the photo-generated carriers towards the cathode spot as the electric field gradually decreases by moving away from the cathode dots' center reducing the drift velocity. Therefore, it is inaccurate to consider the entire area between two cathode spots as the detection zone when the dots are widely spaced. Furthermore, increasing the pitch size of the cathode dot array leads to a lower device's speed. This is attributed to the fact that the response speed is determined by the transit time required for photogenerated electrons to reach the cathode. The transit time relies on both the carrier drift distance and the drift velocity, which is influenced by the local electric field strength. In MD-PIN photodiodes with a larger array pitch size, the transit time is expected to be longer. This is due to the increased carrier drift distance and the weakened intensity of the electric field over the greater distance from the cathode spots (see Fig. 3(a)). An additional point that should be taken into account is that the slowest response occurs when a photon is absorbed exactly in the center between four cathode dots because it corresponds to the longest drift distance along the

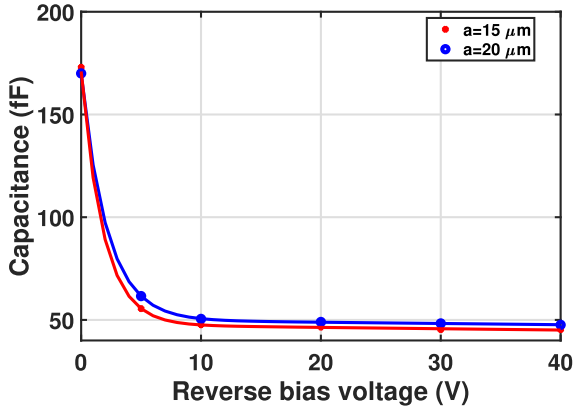

Fig. 4. Measured capacitance of the MD-PIN photodiodes as a function of reverse bias voltage.

silicon surface. The maximum lateral drift distance is calculated as $\frac{a}{\sqrt{2}}$, where a represents the pitch of the array.

Conversely, when the distance between neighboring cathodes in the MD-PIN photodiode is small, a greater number of cathode dots are required to achieve the same active area compared to an MD-PIN photodiode with larger pitch sizes. This increase in cathode dots results in a higher capacitance for the MD-PIN due to the cumulative effect of capacitance from each individual dot in the array. Moreover, MD-PIN photodiodes with small pitch sizes necessitate more metal lines to connect the cathodes, leading to a larger parasitic capacitance. Furthermore, as the pitch size decreases, a larger portion of the detection zone becomes covered by opaque metal. Consequently, this region can no longer be considered an absorption region since incident photons are reflected by the metal before reaching the silicon. Therefore, it is imperative to optimize the pitch size of the array based on the specific requirements of the intended application. TCAD simulation can be employed to determine the optimal array pitch size for the MD-PIN configuration.

III. Experimental Characterizations

In this section, the characterization of MD-PIN photodiodes, consisting of an array of 5 × 5 cathode dots with two different pitches, a = 15 μm and a = 20 μm, is presented. The active area of the photodiodes is 70 μm × 70 μm and 100 μm × 100 μm, respectively. These photodiodes were fabricated using the 0.35 μm CMOS modular optical sensor technology (XO035) provided by X-FAB semiconductor foundries. Key performance characteristics including responsivity, frequency response, and capacitance are examined. A comparative analysis is conducted between the two structures to assess the impact of the array's pitch size.

A. Capacitance

Fig. 4 depicts the capacitance characteristics of the MD-PIN photodiode, which were measured using an LCR meter (Agilent 4284 A) at various reverse bias voltages.

The measurements were performed at a frequency of 1 MHz with an AC amplitude of 100 mV. To account for the influence

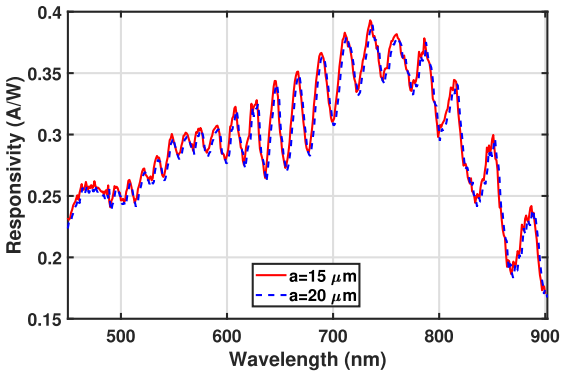

Fig. 5. Measured spectral responsivity of MD-PIN photodiodes with two pitch sizes of a = 15 μm and a = 20 μm at an operating voltage of 10 V.

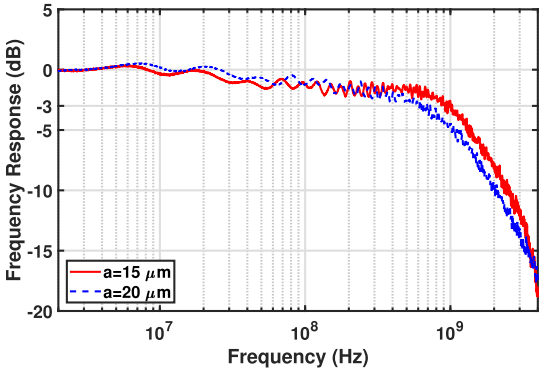

Fig. 6. Normalized frequency responses of MD-PIN photodiodes with two pitch sizes of a = 15 μm and a = 20 μm at an operating voltage of 10 V.

of pad capacitance and measurement cables, a calibration was conducted using an open structure on the same wafer, which had the same pad size and metal track outside of the MD-APD. The total capacitance of the MD-APD comprises the capacitance of the p-n junctions of each individual cathode dot and the parasitic capacitance of the metal tracks employed for interconnecting the cathode dots. The initial high capacitance of 170 fF at zero voltage primarily arises from the junction capacitance of the cathode dots. As the reverse bias voltage increases, the capacitance exponentially decreases to 46.3 fF and 48.8 fF at 10 V reverse bias for the MD-PIN photodiodes with a = 15 μm and a = 20 μm, respectively. The observed capacitance is similar for both structures since they possess an equal number of cathode spots. However, the structure with a pitch size of 15 μm exhibits a slightly lower capacitance, which can be attributed to the reduced parasitic capacitance resulting from the shorter metal paths connecting the cathode spots.

B. DC Characterization

The photodetection characterization of MD-PIN photodiodes with different pitch sizes (a = 15 μm and a = 20 μm) was conducted, as depicted in Fig. 5. For this purpose, a Digikrom CM110 monochromator was utilized to sweep the wavelength range from 400 nm to 900 nm in 1 nm increments. An optical attenuator was employed to maintain consistent optical power. The light was directed to the sample under test through a multi-mode fiber with a core diameter of 62.5 μm. To measure the current and supply the voltage, a Keysight B2987 electrometer was utilized.

Both structures exhibit nearly identical responsivity as the spotlight size (diameter= 62.5 μm) is smaller than the active area of both photodiodes. This ensures that the entire light is irradiated onto the active area, allowing all incident photons to be detected. Furthermore, despite the smaller electric field in the photodiode with a larger pitch size (a = 20 μm), there is a high enough electric field under and between the cathode dots (see Fig. 3) to guide the photogenerated carriers towards the cathode dots. However, the carriers' transit time will be longer, which will affect the speed of the device. A responsivity of 0.294 A/W is obtained at an operating voltage of 10 V for a wavelength of 675 nm, resulting in a quantum efficiency of approximately 54%. The maximum responsivity of 0.393 A/W is present at 735 nm. It should be noticed that in this technology, the entire surface of the photodiode is coated with a thick isolation oxide and a passivation stack. Consequently, incident photons must traverse these layers before reaching the silicon. Due to variations in the refractive indices of these distinct layers, a fraction of the incident photons undergo reflection at each interface. The interplay of multiple reflections of light at the interfaces of the isolation-oxide and passivation stack generates a standing wave, leading to fluctuations in the transmission profile as demonstrated in the spectral responsivity. However, some CMOS technologies provide a module of opto-window, in which the passivation and isolation stack over the photosensitive area is removed and a layer of ARC is deposited on the silicon. This can reduce the reflection and suppress the fluctuations in the spectral responsivity.

C. Frequency Response

The frequency responses were evaluated using a Rohde & Schwarz vector network analyzer ZNB8. The light from a 675 nm laser, with an average optical power of 200 μW, was coupled into the dot PIN photodiodes using a 62.5 μm multi-mode fiber. Photocurrents generated by the photodiodes were measured using a 50-ohm ground-signal probe connected to the 50-ohm input of the vector network analyzer through a Picosecond 5530B bias-tee (20 kHz-12.5 GHz).

Fig. 6 presents the measured frequency responses of MD-PIN photodiodes with different pitch sizes. The bandwidths of 660 MHz and 930 MHz are achieved for the MD-PIN photodiodes with pitch sizes of 20 μm and 15 μm, respectively. The results highlight that reducing the distance between cathode dots leads to higher bandwidth. This improvement can be attributed to the reduction in electron drift time, which is achieved by shortening the radial carrier drift distance and increasing the electric field strength across the detection zone.

In fact, the frequency response is determined by the transit time required for photogenerated electrons to reach the cathode. This transit time depends on both the carrier drift distance and the drift velocity, which in turn is directly influenced by the local electric field strength. Consequently, the MD-PIN photodiode with a larger array pitch size is expected to exhibit a higher

transit time due to the increased carrier drift distance and the weakened intensity of the electric field over the greater distance from the cathode dots. Conversely, reducing the pitch size brings the cathode dots closer, thereby shortening the radial carrier drift distance and intensifying the electric field strength throughout the detection zone. This reduction in drift time due to a shorter radial carrier drift distance and the heightened electric field strength contributes to achieving higher bandwidth.

The bandwidths of 660 MHz an 930 MHz observed at only 10 V reverse voltage are much larger than those of 520 MHz at 15 V as well as 300 MHz at 30 V of the spot and dot PIN photodiodes of [11], [13], respectively, mainly due to the thinner epitaxial layer (12 μm instaed of 24 μm). However, it is important to note that further reducing the distance between cathode dots does not provide significant additional bandwidth improvement. This is because in smaller structures, the half diagonal distance between two cathode dots, which represents the maximum radial drift path, becomes smaller than the depth of the structure (12 μm), and the vertical transition of carriers from this deep region limits the overall bandwidth. As a result, reducing the cathode dot distance beyond a certain point has a diminished impact on the bandwidth.

IV. Discussion and Comparison

The proposed MD-PIN photodiode, featuring a responsivity of 0.29 A/W and a bandwidth of 660 MHz at $\lambda = 675$ nm with a capacitance of 48 fF for an active area of 100 μm $\times$ 100 μm, demonstrates its efficacy in applications requiring low capacitance and moderate bandwidth. To provide a comprehensive perspective, we compared the MD-PIN with several commercially available silicon photodiodes. The high-speed photodiode from OSI Optoelectronics [18], with a responsivity of 0.36 A/W and a bandwidth of approximately 900 MHz at $\lambda = 850$ nm, exhibits a higher capacitance of 660 fF for an active area diameter of 150 μm. Meanwhile, the photodiode from Thorlabs [19], boasting a responsivity of 0.35 A/W and a rise/fall time of 35 ps/200 ps at $\lambda = 740$ nm, maintains a capacitance of 650 fF for the same active area diameter. Conversely, the photodiode from Hamamatsu [20] provides a significantly higher responsivity of 0.63 A/W, although with a limited bandwidth of 80 MHz at $\lambda = 870$ nm, and a substantially larger capacitance of 5 pF for an expansive active area of 880 μm $\times$ 880 μm.

To compare to a vertical pin photodiode with a single cathode having an area of 100 $\times$ 100 μm^2, we performed device simulations with ATLAS for the same fabrication process as it was used for the MD pin photodiodes. The -3 dB bandwidth obtained for 10 V reverse bias and 675 nm wavelength is 1.09 GHz and the capacitance of such a pin photodiode is 120 fF.

In addition, the ability to scale our photodiode to larger dimensions is an exciting avenue that underscores the versatility and potential of the multi-dot design. Changing the 5 $\times$ 5 photodiode array to a larger size comes with both opportunities and challenges. On one hand, increasing the array size while maintaining the number of cathode dots allows for more extensive light collection and potentially higher responsivity. This means that the photodiode can capture more incident photons, making it suitable for applications requiring enhanced light sensitivity.

However, the implications of scaling the array also involve certain considerations. As the size of the array increases, the spacing between individual cathode dots has to be increased. Maintaining the proper pitch size, however, is essential to ensure an optimal electric field distribution across the photodiode's active region. As we have discussed in Section II, different pitch sizes lead to variations in the electric field distribution, which can impact the photodiode's performance. It is crucial to balance the benefits of a larger light-sensitive area against the challenges posed by capacitance, response speed, and electric field strength.

Additionally, increasing the number of cathode dots while scaling to a larger array size can raise concerns related to capacitance. Larger cathode arrays may accumulate a higher cumulative capacitance, which can affect the whole optical sensor's bandwidth and response speed. Moreover, larger arrays with smaller cathode dots may necessitate an increased number of metal lines for interconnection, potentially leading to a larger parasitic capacitance.

To address the implications of scaling our MD-PIN photodiode to larger dimensions, we recommend a systematic analysis and optimization. This should include thorough TCAD simulations to determine the optimal pitch size, cathode dot size, and metal interconnection strategies to maintain the desired performance characteristics.

In summary, scaling the 5 $\times$ 5 array to larger dimensions presents exciting possibilities for our MD-PIN photodiode, but it also requires careful consideration and optimization to balance the advantages of enhanced light collection with the challenges related to capacitance, speed, and electric field distribution.

It is worth noting that while our current work is primarily focused on the dot photodetector concept implemented in silicon there is a strong possibility for this concept to be extended to other semiconductor materials. However, the implementation of the dot photodetector concept in other technologies would necessitate a thorough understanding of the material-specific properties and the optimization of fabrication processes. While the fundamental principles underlying the dot photodetector concept remain applicable, the device design and fabrication techniques would require adaptation to suit the unique characteristics of the specific semiconductor technology.

V. Conclusion

A characterization of the multi-dot PIN photodiode consisting of an array of single dots with interconnected cathodes and a shared anode is presented. It is shown that due to a vertical and radial distribution of the electric field around each cathode dot photo-generated carriers are accelerated towards the respective cathode dots, and thus, the region under and between each cathode dot acts as detection zone. A multi-dot PIN photodiode with an active area of 100 μm $\times$ 100 μm using a 5 $\times$ 5 multi-dot PIN photodiode with a pitch size of 20 μm is designed, which achieves a capacitance of 48.8 fF, a responsivity of 0.294 A/W, and a bandwidth of 660 MHz at an operating voltage of 10 V.

However, the active area can easily be enlarged by expanding the dot array, either by increasing the number of cathode dots or by adjusting the pitch size of the array. It is shown that it is crucial to optimize the array's pitch size based on the specific requirements of the intended application as it impacts the capacitance and speed of the diode.

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REFERENCES

[1] E. Säckinger, *Analysis and Design of Transimpedance Amplifiers for Optical Receivers*. Hoboken, NJ, USA: Wiley, 2017.
[2] X. Ruoyu, L. Bing, and Y. Jie, "A 1500 fps highly sensitive 256 CMOS imaging sensor with in-pixel calibration," *IEEE J. Solid State Circuits*, vol. 47, no. 6, pp. 1408–1418, Jun. 2012.
[3] T. Arai et al., "6.9 A 1.1 μm 33 mpixel 240 fps 3D-stacked CMOS image sensor with 3-stage cyclic-based analog-to-digital converters," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2016, pp. 126–128.
[4] J. Ma, D. Zhang, O. A. Elgendy, and S. Masoodian, "A 0.19 e-rms read noise 16.7 Mpixel stacked quanta image sensor with 1.1 μm-pitch backside illuminated pixels," *IEEE Electron Device Lett.*, vol. 42, no. 6, pp. 891–894, Jun. 2021.
[5] M. Vlaskovic, H. Zimmermann, G. Meinhardt, and J. Kraft, "Image sensor for spectral-domain optical coherence tomography on a chip," *Electron. Lett.*, vol. 56, no. 24, pp. 1306–1309, 2020.
[6] R. P. Jindal, "Silicon MOS amplifier operation in the integrate and dump mode for gigahertz band lightwave communication systems," *J. Lightw. Technol.*, vol. 8, no. 7, pp. 1023–1026, Jul. 1990.
[7] S. M. Sze, Y. Li, and K. K. Ng, *Physics of Semiconductor Devices*. Hoboken, NJ, USA: Wiley, 2021.
[8] A. Ghazi, H. Zimmermann, and P. Seegebrecht, "CMOS photodiode with enhanced responsivity for the UV/blue spectral range," *IEEE Trans. Electron Devices*, vol. 49, no. 7, pp. 1124–1128, Jul. 2002.
[9] B. Nakhkoob, S. Ray, and M. M. Hella, "CMOS integrated high speed light sensors for optical wireless communication applications," in *Proc. SENSORS*, 2012, pp. 1–4.
[10] W. Gaberl and H. Zimmermann, "Low-capacitance integrated silicon finger photodetector," in *Proc. IEEE 3rd Int. Conf. Group IV Photon.*, 2006, pp. 122–124.
[11] B. Goll, K. Schneider-Hornstein, and H. Zimmermann, "Dot PIN photodiodes with a capacitance down to 1.14 aF/μm 2," *IEEE Photon. Technol. Lett.*, vol. 35, no. 6, pp. 301–304, Mar. 2023.
[12] K. Schneider-Hornstein, B. Goll, and H. Zimmermann, "Ultra-sensitive PIN-photodiode receiver," *IEEE Photon. J.*, vol. 15, no. 3, Jun. 2023, Art. no. 7201409.
[13] B. Goll, K. Schneider-Hornstein, and H. Zimmermann, "Ultra-low capacitance spot PIN photodiodes," *IEEE Photon. J.*, vol. 15, no. 2, Apr. 2023, Art. no. 6800906.
[14] B. J. Baliga and S. K. Ghandhi, "Analytical solutions for the breakdown voltage of abrupt cylindrical and spherical junctions," *Solid-State Electron.*, vol. 19, no. 9, pp. 739–744, 1976.
[15] E. Engelmann, W. Schmailzl, P. Iskra, F. Wiest, E. Popova, and S. Vinogradov, "Tip avalanche photodiode–A new generation silicon photomultiplier based on non-planar technology," *IEEE Sensors J.*, vol. 21, no. 5, pp. 6024–6034, Mar. 2021.
[16] S. S. Kohneh Poushi, B. Goll, K. Schneider-Hornstein, M. Hofbauer, and H. Zimmermann, "Area and bandwidth enhancement of an n+/p-well dot avalanche photodiode in 0.35 μm CMOS technology," *Sensors*, vol. 23, no. 7, 2023, Art. no. 3403.
[17] "Silvaco atlas user's manual," 2023. [Online]. Available: https://www.silvaco.com
[18] 2023. [Online]. Available: https://www.osioptoelectronics.com/
[19] 2023. [Online]. Available: https://www.thorlabs.com/
[20] 2023. [Online]. Available: https://www.hamamatsu.com/eu/en.html

Bibliography

[1] J.-E. Joo, M.-J. Lee, and S. M. Park, "A CMOS optoelectronic receiver IC with an on-chip avalanche photodiode for home-monitoring LiDAR sensors," *Sensors*, vol. 21, no. 13, p. 4364, 2021.

[2] X. Yu, X. Chen, Y. Song, L. Zhang, J. Jiang, T. Wang, and S. Tong, "Design and evaluation of a high-sensitivity digital receiver with the finite impulse response filter algorithm for free-space laser communication," *Optical Engineering*, vol. 59, no. 3, p. 036105, 2020.

[3] M. M. Hossain, S. Ray, J. S. Cheong, L. Qiao, A. N. Baharuddin, M. M. Hella, J. P. David, and M. M. Hayat, "Low-noise speed-optimized large area CMOS avalanche photodetector for visible light communication," *Journal of Lightwave Technology*, vol. 35, no. 11, pp. 2315–2324, 2017.

[4] H. Zheng, R. Ma, M. Liu, and Z. Zhu, "High sensitivity and wide dynamic range analog front-end circuits for pulsed TOF 4-D imaging LADAR receiver," *IEEE Sensors Journal*, vol. 18, no. 8, pp. 3114–3124, 2018.

[5] H.-Z. Song, "Avalanche photodiode focal plane arrays and their application to laser detection and ranging," in *Advances in Photodetectors-Research and Applications*. IntechOpen, 2018.

[6] O. Shcherbakova, L. Pancheri, G.-F. Dalla Betta, N. Massari, and D. Stoppa, "3D camera based on linear-mode gain-modulated avalanche photodiodes," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*. IEEE, 2013, pp. 490–491.

[7] Y. Dong, W. Wang, X. Xu, X. Gong, D. Lei, Q. Zhou, Z. Xu, S.-F. Yoon, G. Liang, and Y.-C. Yeo, "Germanium-tin on silicon avalanche photodiode for short-wave infrared imaging," in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*. IEEE, 2014, pp. 1–2.

[8] J. Huikari, S. Jahromi, J.-P. Jansson, and J. Kostamovaara, "Compact laser radar based on a subnanosecond laser diode transmitter and a two-dimensional cmos single-photon receiver," *Optical Engineering*, vol. 57, no. 2, p. 024104, 2018.

[9] M. Gramegna, I. R. Berchera, S. Kueck, G. Porrovecchio, C. Chunnilall, I. Degiovanni, M. Lopez, R. Kirkwood, T. Kübarsepp, A. Pokatilov *et al.*, "European coordinated metrological effort for quantum cryptography," in *Quantum Technologies 2018*, vol. 10674. International Society for Optics and Photonics, 2018, p. 106741K.

[10] H. Zimmermann, B. Steindl, M. Hofbauer, and R. Enne, "Integrated fiber optical receiver reducing the gap to the quantum limit," *Sci. Rep.*, vol. 7, no. 1, p. 2652, 2017.

[11] C. Bruschini, H. Homulle, I. M. Antolovic, S. Burri, and E. Charbon, "Single-photon avalanche diode imagers in biophotonics: Review and outlook," *Light: Science & Applications*, vol. 8, no. 1, pp. 1–28, 2019.

[12] S. Sze, "Physics of semiconductor devices, book," *New York, Wiley-Interscience, 878 p*, 1981.

[13] E. D. Palik, *Handbook of optical constants of solids*. Academic press, 1998, vol. 3.

[14] D. E. Aspnes and A. Studna, "Dielectric functions and optical parameters of si, ge, gap, gaas, gasb, inp, inas, and insb from 1.5 to 6.0 ev," *Physical Review B*, vol. 27, no. 2, p. 985, 1983.

[15] S. Selberherr, *Analysis and simulation of semiconductor devices*. Springer Science & Business Media, 1984.

[16] Silvaco Atlas User's Manual. Available: https://www.silvaco.com, accessed:2019-2024.

[17] Synopsys 2023 Taurus-medici http://www.synopsys.com /silicon/tcad/device-simulation /taurus-medici.html, accessed:2019-2024.

[18] Synopsys 2023 Sentaurus http://www.synopsys.com/silicon/tcad /device-simulation/ sentaurus-device. accessed:2023.

[19] H. Zimmermann and H. Zimmermann, *Integrated silicon optoelectronics*. Springer, Berlin, 2010, vol. 148.

[20] S. Selberherr, *Analysis and simulation of semiconductor devices*. Springer Science & Business Media, 2012.

[21] M. Valdinoci, D. Ventura, M. Vecchi, M. Rudan, G. Baccarani, F. Illien, A. Stricker, and L. Zullino, "Impact-ionization in silicon at large operating temperature," in *1999 International Conference on Simulation of Semiconductor Processes and Devices. SISPAD'99 (IEEE Cat. No. 99TH8387)*. IEEE, 1999, pp. 27–30.

[22] T. Lackner, "Avalanche multiplication in semiconductors: A modification of Chynoweth's law," *Solid-State Electronics*, vol. 34, no. 1, pp. 33–42, 1991.

[23] W. Grant, "Electron and hole ionization rates in epitaxial silicon at high electric fields," *Solid-State Electronics*, vol. 16, no. 10, pp. 1189–1203, 1973.

[24] C. Crowell and S. Sze, "Temperature dependence of avalanche multiplication in semiconductors," *Applied Physics Letters*, vol. 9, no. 6, pp. 242–244, 1966.

[25] A. Chynoweth, "Ionization rates for electrons and holes in silicon," *physical review*, vol. 109, no. 5, p. 1537, 1958.

[26] V. Savuskan, I. Brouk, M. Javitt, and Y. Nemirovsky, "An Estimation of Single Photon Avalanche Diode (SPAD) Photon Detection Efficiency (PDE) Nonuniformity," *IEEE Sensors Journal*, vol. 13, no. 5, pp. 1637–1640, 2013.

[27] M. Mazzillo, A. Piazza, G. Condorelli, D. Sanfilippo, G. Fallica, S. Billotta, M. Belluso, G. Bonanno, L. Cosentino, A. Pappalardo, and P. Finocchiaro, "Quantum detection efficiency in geiger mode avalanche photodiodes," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 3620–3625, 2008.

[28] Y. Xu, P. Xiang, X. Xie, and Y. Huang, "A new modeling and simulation method for important statistical performance prediction of single photon avalanche diode detectors," *Semiconductor Science and Technology*, vol. 31, no. 6, p. 065024, 2016.

[29] G. Gallina, F. Retière, P. Giampa, J. Kroeger, P. Margetak, S. B. Mamahit, A. D. S. Croix, F. Edaltafar, L. Martin, N. Massacret, M. Ward, and G. Zhang, "Characterization of SiPM avalanche triggering probabilities," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4228–4234, 2019.

[30] C.-A. Hsieh, C.-M. Tsai, B.-Y. Tsui, B.-J. Hsiao, and S.-D. Lin, "Photon-detection-probability simulation method for CMOS single-photon avalanche diodes," *Sensors*, vol. 20, no. 2, p. 436, 2020.

[31] T. Leitner, A. Feiningstein, R. Turchetta, R. Coath, S. Chick, G. Visokolov, V. Savuskan, M. Javitt, L. Gal, I. Brouk *et al.*, "Measurements and simulations of low dark count rate single photon avalanche diode device in a low voltage 180-nm cmos image sensor technology," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1982–1988, 2013.

[32] S. K. Poushi, H. Mahmoudi, B. Steindl, M. Hofbauer, and H. Zimmermann, "Comprehensive modeling of photon detection probability in CMOS-based SPADs," in *IEEE SENSORS*. IEEE, 2020, pp. 1–4.

[33] H. Mahmoudi, S. S. K. Poushi, B. Steindl, M. Hofbauer, and H. Zimmermann, "Optical and electrical characterization and modeling of photon detection probability in CMOS single-photon avalanche diodes," *IEEE Sensors Journal*, vol. 21, no. 6, pp. 7572–7580, 2021.

[34] B. Steindl, R. Enne, and H. Zimmermann, "Thick detection zone single-photon avalanche diode fabricated in 0.35 μm complementary metal-oxide semiconductors," *Opt. Eng*, vol. 54, no. 5, p. 050503, 2015.

[35] R. J. McIntyre, "On the Avalanche Initiation Probability of Avalanche Diodes Above the Breakdown Voltage," *IEEE Trans. Electron Devices*, vol. 20, no. 7, pp. 637–641, 1973.

[36] CST User's Manual. Available: https://www.3ds.com.

[37] R. Van Overstraeten and H. De Man, "Measurement of the Ionization Rates in Diffused Silicon pn Junctions," *Solid-State Electronics*, vol. 13, no. 5, pp. 583–608, 1970.

[38] D. Milovančev, T. Jukić, B. Steindl, P. Brandl, and H. Zimmermann, "Optical Wireless Communication Using a Fully Integrated 400 μm Diameter APD Receiver," *The Journal of Engineering*, vol. 2017, no. 8, pp. 506–511, 2017.

[39] S. K. Poushi, H. Mahmoudi, M. Hofbauer, A. Dervic, and H. Zimmermann, "Photodetection characterization of SPADs fabricated in 0.35 μm PIN photodiode and high voltage CMOS technologies," in *2022 45th Jubilee International Convention on Information, Communication and Electronic Technology (MIPRO)*. IEEE, 2022, pp. 230–234.

[40] S. S. K. Poushi, H. Mahmoudi, M. Hofbauer, B. Steindl, and H. Zimmermann, "Photon detection probability enhancement using an anti-reflection coating in CMOS-based SPADs," *Applied Optics*, vol. 60, no. 25, pp. 7815–7820, 2021.

[41] M. Hofbauer, B. Steindl, K. Schneider-Hornstein, and H. Zimmermann, "Performance of high-voltage CMOS single-photon avalanche diodes with and without well-modulation technique," *Optical Engineering*, vol. 59, no. 4, p. 040502, 2020.

[42] K. Iiyama, H. Takamatsu, and T. Maruyama, "Hole-injection-type and electron-injection-type silicon avalanche photodiodes fabricated by standard 0.18 μm CMOS process," *IEEE Photonics Technology Letters*, vol. 22, no. 12, pp. 932–934, 2010.

[43] L. Pancheri, G.-F. Dalla Betta, and D. Stoppa, "Low-noise avalanche photodiode with graded junction in 0.15 μm CMOS technology," *IEEE Electron Device Letters*, vol. 35, no. 5, pp. 566–568, 2014.

[44] M.-J. Lee, J.-M. Lee, H. Rücker, and W.-Y. Choi, "Bandwidth improvement of CMOS-APD with carrier-acceleration technique," *IEEE Photonics Technology Letters*, vol. 27, no. 13, pp. 1387–1390, 2015.

[45] W. Wang, Y. Zhang, and Z. Wei, "High-performance structure of guard ring in avalanche diode for single photon detection," *International Journal of Communications, Network and System Sciences*, vol. 10, no. 8, pp. 1–6, 2017.

[46] S. Nayak, A. H. Ahmed, A. Sharkia, A. S. Ramani, S. Mirabbasi, and S. Shekhar, "A 10-Gb/s- 18.8 dBm sensitivity 5.7 mW fully-integrated optoelectronic receiver with avalanche photodetector in 0.13 μm CMOS," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 8, pp. 3162–3173, 2019.

[47] M.-J. Lee and W.-Y. Choi, "A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain-bandwidth product," *Optics Express*, vol. 18, no. 23, pp. 24 189–24 194, 2010.

[48] J. A. Richardson, E. A. Webster, L. A. Grant, and R. K. Henderson, "Scaleable single-photon avalanche diode structures in nanometer cmos technology," *IEEE Transactions on Electron Devices*, vol. 58, no. 7, pp. 2028–2035, 2011.

[49] H. Finkelstein, M. J. Hsu, and S. C. Esener, "Sti-bounded single-photon avalanche diode in a deep-submicrometer cmos technology," *IEEE Electron Device Letters*, vol. 27, no. 11, pp. 887–889, 2006.

[50] I. S. Alirezaei, N. Andre, and D. Flandre, "Enhanced ultraviolet avalanche photodiode with 640-nm-thin silicon body based on SOI technology," *IEEE Transactions on Electron Devices*, vol. 67, no. 11, pp. 4641–4644, 2020.

[51] D. Bronzi, F. Villa, S. Tisa, A. Tosi, and F. Zappa, "Spad figures of merit for photon-counting, photon-timing, and imaging applications: a review," *IEEE Sensors Journal*, vol. 16, no. 1, pp. 3–12, 2015.

[52] S. Bose, H. Ouh, S. Sengupta, and M. L. Johnston, "Parametric study of pn junctions and structures for CMOS-integrated single-photon avalanche diodes," *IEEE Sensors Journal*, vol. 18, no. 13, pp. 5291–5299, 2018.

[53] T. Leitner, A. Feiningstein, R. Turchetta, R. Coath, S. Chick, G. Visokolov, V. Savuskan, M. Javitt, L. Gal, I. Brouk *et al.*, "Measurements and simulations of low dark count rate single photon avalanche diode device in a low voltage 180-nm cmos image sensor technology," *IEEE Transactions on Electron Devices*, vol. 60, no. 6, pp. 1982–1988, 2013.

[54] X. Lu, M.-K. Law, Y. Jiang, X. Zhao, P.-I. Mak, and R. P. Martins, "A 4-μm diameter SPAD using less-doped n-well guard ring in baseline 65-nm CMOS," *IEEE Transactions on Electron Devices*, vol. 67, no. 5, pp. 2223–2225, 2020.

[55] D. Han, Y. Xu, F. Sun, and F. Song, "A scalable single-photon avalanche diode with improved photon detection efficiency and dark count noise," *Optik*, vol. 212, p. 164692, 2020.

[56] S. S. K. Poushi, H. Mahmoudi, M. Hofbauer, B. Steindl, K. Schneider-Hornstein, and H. Zimmermann, "Experimental and simulation study of fill-factor enhancement using a virtual guard ring in n/ p-well CMOS single-photon avalanche diodes," *Optical Engineering*, vol. 67105, pp. 067 105–067 105, 2021.

[57] F.-P. Chou, C.-W. Wang, Z.-Y. Li, Y.-C. Hsieh, and Y.-M. Hsin, "Effect of deep N-well bias in an 850-nm Si photodiode fabricated using the CMOS process," *IEEE Photonics Technology Letters*, vol. 25, no. 7, pp. 659–662, 2013.

[58] W. Zhi, Q. Quan, P. Yu, and Y. Jiang, "A 45 nm CMOS avalanche photodiode with 8.4 GHz bandwidth," *Micromachines*, vol. 11, no. 1, pp. 651–657, 2020.

[59] M.-J. Lee, "First CMOS silicon avalanche photodetectors with over 10-GHz bandwidth," *IEEE Photonics Technology Letters*, vol. 28, no. 3, pp. 276–279, 2015.

[60] Y. S. Kim, I. S. Jun, and K. H. Kim, "Design and characterization of CMOS avalanche photodiode with charge sensitive preamplifier," *IEEE Transactions on Nuclear Science*, vol. 55, no. 3, pp. 1376–1380, 2008.

[61] B. Steindl, R. Enne, S. Schidl, and H. Zimmermann, "Linear mode avalanche photodiode with high responsivity integrated in high-voltage CMOS," *IEEE Electron Device Letters*, vol. 35, no. 9, pp. 897–899, 2014.

[62] B. Steindl, W. Gaberl, R. Enne, S. Schidl, K. Schneider-Hornstein, and H. Zimmermann, "Linear mode avalanche photodiode with 1GHz bandwidth fabricated in 0.35 μm CMOS," *IEEE Photonics Technology Letters*, vol. 26, no. 15, pp. 1511–1514, 2014.

[63] Z. Cheng, H. Xu, and Y. Chen, "Design of low noise avalanche photodiode single element detectors and linear arrays through CMOS process," in *Advanced Photon Counting Techniques XIII*, vol. 10978. SPIE, 2019, pp. 70–77.

[64] M.-J. Lee, H. Rucker, and W.-Y. Choi, "Effects of guard-ring structures on the performance of silicon avalanche photodetectors fabricated with standard CMOS technology," *IEEE Electron Device Letters*, vol. 33, no. 1, pp. 80–82, 2011.

[65] W. Wang, H.-A. Zeng, F. Wang, G. Wang, Y. Xie, and S. Feng, "A speed-optimized, low-noise APD with 0.18 μ m CMOS technology for the VLC applications," *Modern Physics Letters B*, vol. 34, no. 29, p. 2050321, 2020.

[66] T. Wang, H. Peng, C. Xu, T. Shi, J. Chen, J. Deng, and H. Song, "Effects of guard-ring's depth and space on the performance of silicon avalanche photodetector arrays with TCAD simulation," in *AOPC 2021: Optical Sensing and Imaging Technology*, vol. 12065. SPIE, 2021, pp. 602–607.

[67] D. Shin, B. Park, Y. Chae, and I. Yun, "The effect of a deep virtual guard ring on the device characteristics of silicon single photon avalanche diodes," *IEEE Transactions on Electron Devices*, vol. 66, no. 7, pp. 2986–2991, 2019.

[68] G. Jegannathan, H. Ingelberts, S. Boulanger, and M. Kuijk, "Current assisted avalanche photo diodes (CAAPDs) with separate absorption and multiplication region in conventional CMOS," *Applied Physics Letters*, vol. 115, no. 13, p. 132101, 2019.

[69] E. Van Sieleghem, G. Karve, K. De Munck, A. Vinci, C. Cavaco, A. Süss, C. Van Hoof, and J. Lee, "A backside-illuminated charge-focusing silicon SPAD with enhanced near-infrared sensitivity," *IEEE Transactions on Electron Devices*, vol. 69, no. 3, pp. 1129–1136, 2022.

[70] E. Van Sieleghem, A. Süss, P. Boulenc, J. Lee, G. Karve, K. De Munck, C. Cavaco, and C. Van Hoof, "A near-infrared enhanced silicon single-photon avalanche diode with a spherically uniform electric field peak," *IEEE Electron Device Letters*, vol. 42, no. 6, pp. 879–882, 2021.

[71] K. Morimoto, J. Iwata, M. Shinohara, H. Sekine, A. Abdelghafar, H. Tsuchiya, Y. Kuroda, K. Tojima, W. Endo, Y. Maehashi *et al.*, "3.2 megapixel 3D-stacked charge focusing SPAD for low-light imaging and depth sensing," in *IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2021, pp. 20–2.

[72] E. Engelmann, W. Schmailzl, P. Iskra, F. Wiest, E. Popova, and S. Vinogradov, "Tip avalanche photodiode—a new generation silicon photomultiplier based on non-planar technology," *IEEE Sensors Journal*, vol. 21, no. 5, pp. 6024–6034, 2020.

[73] S. K. Poushi, B. Goll, K. Schneider-Hornstein, M. Hofbauer, and H. Zimmermann, "Cmos integrated 32 A/W and 1.6 GHz avalanche photodiode based on electric field-line crowding," *IEEE Photonics Technology Letters*, vol. 34, no. 18, pp. 945–948, 2022.

[74] S. S. K. Poushi, C. Gasser, B. Goll, M. Hofbauer, K. Schneider-Hornstein, and H. Zimmermann, "A near-infrared enhanced field-line crowding based CMOS-integrated avalanche photodiode," *IEEE Photonics Journal*, vol. 15, no. 3, pp. 1–9, 2023.

[75] S. S. K. Poushi, B. Goll, K. Schneider-Hornstein, M. Hofbauer, and H. Zimmermann, "Area and bandwidth enhancement of an n^+/p-well dot avalanche photodiode in 0.35 μm CMOS technology," *Sensors*, vol. 23, no. 7, pp. 3403–3418, 2023.

[76] S. S. K. Poushi, B. Goll, K. Schneider-Hornstein, and H. Zimmermann, "Large active area, low capacitance multi-dot pin photodiode in 0.35 μm CMOS technology," *IEEE Photonics Journal*, vol. 16, no. 1, pp. 1–6, 2024.

[77] K. Schneider-Hornstein, B. Goll, and H. Zimmermann, "Ultra-sensitive PIN-photodiode receiver," *IEEE Photonics Journal*, vol. 15, no. 3, pp. 1–9, 2023.

Appendix a

List of Own Publications

Journal articles

[J1] S. S. K. Poushi, B. Goll, K. Schneider-Hornstein, and H. Zimmermann, "Large active area, low capacitance multi-dot pin photodiode in 0.35 μm CMOS technology," IEEE Photonics Journal, vol. 16, no. 1, pp. 1–6, 2024.

[J2] C. Ribisch, M. Hofbauer, S. S. K. Poushi, A. Zimmer, K. Schneider-Hornstein, B. Goll and H. Zimmermann, "Multi-Channel Gating Chip in 0.18 µm High-Voltage CMOS for Quantum Applications," Sensors, 23(24), p.9644-9658, 2023.

[J3] S. S. K. Poushi, B. Goll, K. Schneider-Hornstein, M. Hofbauer, and H. Zimmermann, "Area and bandwidth enhancement of an n^+/p-well dot avalanche photodiode in 0.35 μm CMOS technology," Sensors, vol. 23, no. 7, p. 3403-3418, 2023.

[J4] S. S. K. Poushi, C. Gasser, B. Goll, M. Hofbauer, K. Schneider-Hornstein, and H. Zimmermann, "A near-infrared enhanced field-line crowding based CMOS-integrated avalanche photodiode," IEEE Photonics Journal, vol. 15, no. 3, pp. 1–9, 2023.

[J5] S. S. K. Poushi, B. Goll, K. Schneider-Hornstein, M. Hofbauer, and H. Zimmermann, "CMOS integrated 32 A/W and 1.6 GHz avalanche photodiode based on electric field-line crowding," IEEE Photonics Technology Letters, vol. 34, no. 18, pp. 945–948, 2022.

[J6] S. S. K. Poushi, H. Mahmoudi, M. Hofbauer, B. Steindl, K. Schneider-Hornstein, and H. Zimmermann, "Experimental and simulation study of fill-factor enhancement using a virtual guard ring in n^+/ p-well CMOS single-photon avalanche diodes," Optical Engineering, vol. 67105, p. 067105-067105, 2021.

[J7] S. S. K. Poushi, H. Mahmoudi, M. Hofbauer, B. Steindl, and H. Zimmermann, "Photon detection probability enhancement using an anti-reflection coating in CMOS-based SPADs," Applied Optics, vol. 60, no. 25, pp. 7815–7820, 2021.

[J8] H. Mahmoudi, S. S. K. Poushi, B. Steindl, M. Hofbauer, and H. Zimmermann, "Optical and electrical characterization and modeling of photon detection probability in CMOS single-photon avalanche diodes," IEEE Sensors Journal, vol. 21, no. 6, pp. 7572–7580, 2021.

Conference proceedings

[C1] A. Dervic, S. S. K. Poushi and H. Zimmermann, "Fully-integrated SPAD active quenching/resetting circuit in high-voltage 0.35 m CMOS for reaching PDP saturation at 650 nm," In 2021 24th International Symposium on Design and Diagnostics of Electronic Circuits Systems (DDECS) (pp. 1-5). IEEE.

[C2] S. S. K. Poushi, H. Mahmoudi, M. Hofbauer, A. Dervic, and H. Zimmermann, "Photodetection characterization of SPADs fabricated in 0.35 mPIN photodiode and high voltage CMOS technologies," in 2022 45th Jubilee International Convention on Information, Communication and Electronic Technology (MIPRO), IEEE, 2022, pp. 230–234.

[C3] S. S. K. Poushi, H. Mahmoudi, B. Steindl, M. Hofbauer, and H. Zimmermann, "Comprehensive modeling of photon detection probability in CMOS-based SPADs," in 2020 IEEE SENSORS, pp. 1–4.