Diploma Thesis

Controlled-Spalling of Thin Layers from 4H-Silicon Carbide Substrates for Biomedical Applications

submitted in satisfaction of the requirements for the degree of
Master of Science, MSc
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Diplomarbeit

Kontrolliertes Spalling von dünnen Schichten von 4H-SiC Substraten für biomedizinische Anwendungen

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Abstract

The following thesis presents and discusses a novel approach in creating thin monocrystalline layers out of 4H silicon carbide (4H-SiC) for biomedical applications.

Porosifying the surface of a single crystalline silicon carbide (4H-SiC) wafer with means of metal assisted photo chemical etching (MAPCE) promotes the adhesion of an electroplated nickel (Ni) layer. By utilizing a mechanical peel-off process, a Ni layer with tailored mechanical stress is first deposited and then peeled off such that also a thin layer of 4H-SiC is detached from the substrate. To create optimal peeling conditions, calculations are conducted to find appropriate parameters for a successful spalling process. The created sheet of SiC is characterised in a scanning electron microscope (SEM) to analyse its quality in regard of homogeneity, and thickness. These thin and flexible layers are especially important for creating electronics for biomedical applications as they can bend and stretch in the desired environment without comprising on its functionality and reliability for different applications like in-vivo drug delivery or as a robust electrode.

Kurzfassung

In der folgenden Arbeit wird ein neuartiger Ansatz zur Herstellung dünner Schichten aus einkristallinem 4H-Siliziumkarbid (4H-SiC) für biomedizinische Anwendungen vorgestellt und diskutiert.

Die Porösizierung der Oberfläche eines Wafers aus einkristallinem Siliziumkarbid (4H-SiC) mit Hilfe eines metall-katalytischen, photochemischen Ätzverfahren unterstützt die Haftung einer galvanisch aufgebrachten Nickelschicht (Ni). Diese aufgebrachte Ni-Schicht wird mit einer definierten, mechanischen Schichtspannung abgeschieden. Anschließend wird über ein mechansiches Abziehverfahren der Ni-Schicht auch eine dünne, 4H-SiC Schicht vom Substrat gelöst ("abgerissen"). Um optimale Schälbedingungen zu schaffen, werden Berechnungen durchgeführt, um geeignete Parameter für einen erfolgreichen Ablöseversuch zu finden. Die neu entstandene SiC-Schicht wird im Rasterelektronenmikroskop (REM) charakterisiert, um ihre Qualität in Bezug auf Homogenität und Dicke zu erfassen. Diese dünnen und flexiblen Schichten sind besonders wichtig für die Herstellung von Elektronikkomponenten für biomedizinische Anwendungen, da sie sich in der gewünschten Umgebung in die entsprechende Form biegen lassen und gedehnt werden können, ohne dabei ihre Funktionalität und Zuverlässigkeit für verschiedene Anwendungen wie die in-vivo Medikamentenabgabe oder als Elektrode zu beeinträchtigen.

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Finally, I sincerely dedicate this thesis to my parents, whose unwavering support have been the cornerstone of my academic journey. Your endless love, encouragement, and belief in me have provided the strength and motivation I needed to pursue my degree. Through countless sacrifices and selfless acts, you have given me the opportunity to focus on my studies and achieve my goals. This accomplishment is as much yours as it is mine, and I am forever grateful for everything you have done. Thank you from the bottom of my heart. I owe you more than any word can describe...

Contents

Chapter 1

Motivation

This chapter will comprise a compact historical outline of semiconductor history, explain the reasons for the material selection and why specific process steps are taken into consideration to achieve the goal of this thesis.

1.1 A Brief Semiconductor History

Mankind reached a new age dubbed *Information Age* during the mid of the 20th century at the time the first semiconductors reached mass manufacturing and many specialists in their respective fields were writing of the coming of a new era based on computers and communication technology [1]. The first germanium (Ge) point contact transistor was not only invented by the *Bell Telephone Laboratories* in late 1947, but six months later also in Europe, specifically at the *Westinghouse Electronics Cooperation* subsidiary in France by German scientists, Herbert Mataré and Heinrich Welker dubbed the *Transitron* with less noise, better stability and uniformity than the US counterpart. But the French government and *Westinghouse* failed to pursue this incredible finding because France started to use their funds in becoming a nuclear power [2]. The switch from Ge to silicon (Si) occurred in the 1950s to accommodate the demands of the US military establishments requiring the material to function reliably at high temperatures (125 °C) [3].

1.2 Material and Aim of this Thesis

Since then Si has been vastly used in the semiconductor industry due to its raw material availability and ten times lower cost in comparison to Ge [4]. But Si is not suitable for every application, for example, gallium arsenide (GaAs) as a compound semiconductor is superior regarding electron mobility which results in reduced parasitics and improved frequency response [5].

Due to higher demands to the semiconductor material, especially in harsher conditions such as higher power, higher temperature, higher frequency or even higher radiation, more research has been conducted in finding alternatives to Si, particularly since the start of the electro mobility boom which demands for faster charging speeds with higher current densities and higher temperatures resulting from it [6]. With their respective properties, wide band bap semiconductors like silicon carbide (SiC), gallium nitride (GaN) or even diamond show promising results. From the aforementioned semiconductors, SiC might be the most promising material for high power applications as the technology is already mature for mass production and commercial products are already on the market [7], [8]. Fundamentally, SiC possess another important attribute making this semiconductor applicable for a wide scope of use-cases: its bio- and hemocompatibility [9], [10], [11].

The information age, also dubbed silicon era, created many possibilities to measure biological activities. A lot of devices built for humans require body contact for an extended period of

time and this results in challenges in the way devices are designed and built, especially when implanted into the human body. Biocompatibility for devices is defined, that it should have positive effects on the individual, but still operate correctly and reliably [12]. So if the body recognises the devices as foreign, inflammatory response is initiated which leads to issues with long term reliability *in vivo*. Tests show that SiC does not initiate cytotoxic reactions *in vitro* [11]. Furthermore, hemocompatibility tests prove that SiC has a low platelet attachment and activation in comparison to other semiconductors like e.g. Si [11]. But research is ongoing for SiC, especially for the 3C-SiC variant and in future more knowledge about the behaviour of this semiconductor *in vivo* can be acquired.

To deploy SiC as a biocompatible semiconductor, most of the time, the material has to be of flexible nature as the human body is never in a static or rigid state. Unfortunately, SiC is been praised as a semiconductor with high mechanical and chemical stability which makes it a brittle and hard material [13], [14]. To achieve a flexible SiC substrate, a thin layer has to be created and this thesis will present a novel, mechanical and cost effective approach in achieving this goal with the means of controlled spalling.

Chapter 2

Introduction

Silicon carbide offers a plethora of attributes which are regarded as outstanding, but also comes with disadvantages. Mechanical and chemical stability is one of the characteristics which makes mechanical and chemical machining within wafer fabrication a challenge to overcome. To create thin layers of SiC, standard tools used in the industry for e.g. Si will not suffice as SiC is one of the hardest materials on earth and even the tools used primarily in the industry cause a lot of sawing loss. This chapter will introduce SiCs material properties, the challenges of wafer processing, new promising technologies emerging in the industry and a novel approach which has never been demonstrated so far, to the best of the author's knowledge.

2.1 Silicon Carbide's Outstanding Material Properties

As an established high power semiconductor material, the properties of SiC are already well researched. Approximately 70 years ago the first semiconductor crystal was discovered by Lely, and after important inventions like the high quality epitaxy process by Cree Inc., many devices were fabricated like SiC LEDs, high power and high frequency devices [15].

2.1.1 SiC Polymorphism

A wide variety of SiC crystal structures exist in general where each of them vary in their Si-C stacking sequence. That means the order of stacking in the crystal differs without changes in the chemical composition. This phenomena is called polytypism and each variant of SiC with its stacking sequence is a polytype. There are over 200 polytypes and the exact reasoning for why so many polytypes exist is not clear [16]. If one takes a look at a hexagonal/cubic close packed system, there are three possible sites donated as A, B and C as in Fig. 2.1 [16].

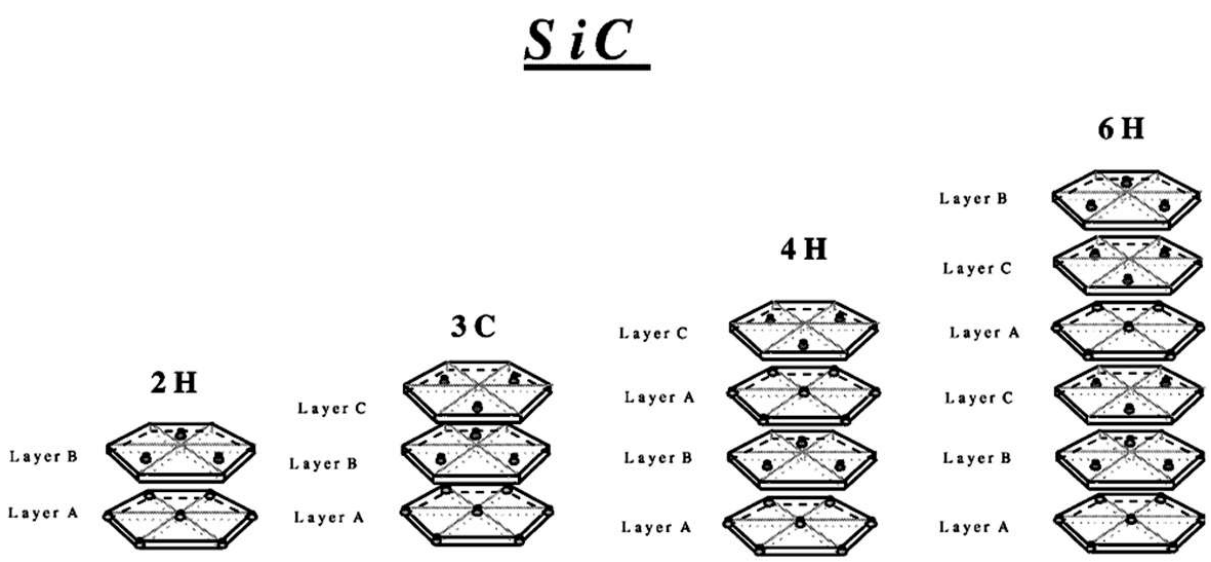


Fig. 2.1: A concept of how the crystal stacking occurs. The 2H and 3C structures are occupied like in a hexagonal and cubic close packed system, denoted with a A, B and C [17].

Two equal sites cannot succeed each other, for example, after an A site, the next layer can only be a B or C site [16]. The notation for the SiC variants (4H, 6H,..) are called *Ramsdell's notation* and represent the number of Si-C bilayers in the unit cell and the crystal system (H for hexagonal and C for cubic). How the most popular SiC crystals look like, is depicted in Fig. 2.2 [16].

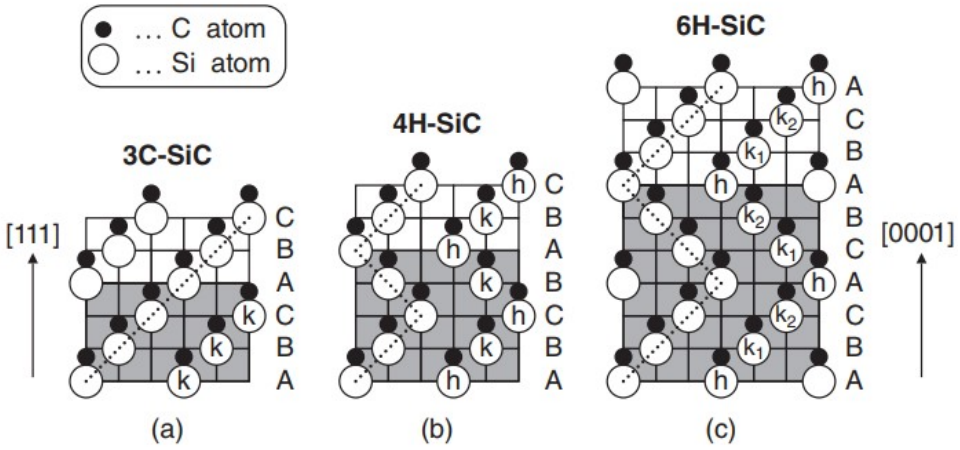


Fig. 2.2: A schematic overview of most popular SiC polytypes used in the industry: (a) 3C-SiC, (b) 4H-SiC and (c) 6H-SiC. Open circles represent Si atoms and closed ones are C atoms [16].

The most favoured SiC structures used in electronics are the 4H-SiC, 6H-SiC and 3C-SiC polytypes, whereas the 4H-SiC variant is mostly employed in power electronics due to the electron mobility and the higher band gap than other polytypes. Due to the higher band gap, the thermal generation of electron hole pairs is low compared to silicon which allows for higher operation temperatures where reliable functionality is given.

2.1.2 Mechanical and Chemical Properties

SiC is a material consisting of silicon and carbon atoms covalently bonded in a tetrahedron form, whereas each Si atom has exactly four c atom neighbours and vice versa [16]. The short bond lengths between the atoms, as seen in Fig. 2.3 are the reason for the high mechanical and chemical stability of the material, which is valid for all SiC polytypes [18].

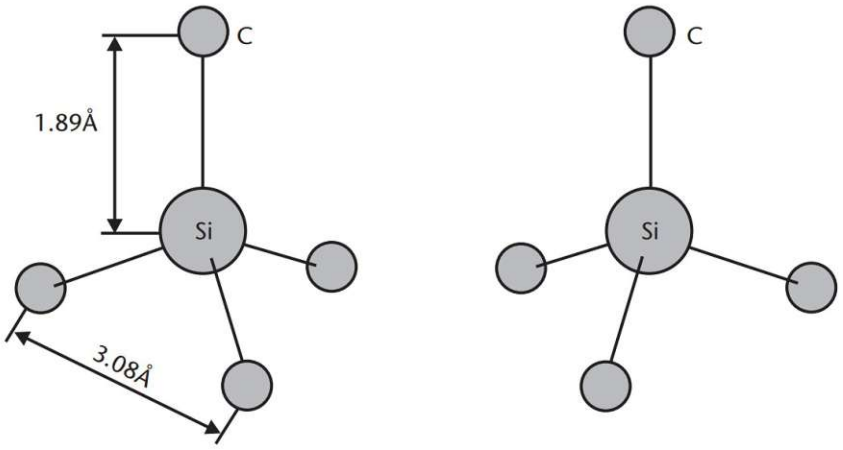


Fig. 2.3: All SiC crystals are built with bi-layers of C and Si in a tetrahedron form where the atoms are covalently bonded [18].

SiC with its different polytypes has the following properties in comparison to Si, GaN, GaAs and Diamond as seen in Tab. 2.1 [19], [20], [21]. The attributes show SiC to have a higher thermal conductivity and critical electric field compared to other semiconductors like Si or GaAs which makes it a suitable material for power electronics.

Tab. 2.1: Semiconductor comparison between SiC polytypes and other materials [19], [20], [21]

Properties	4H-SiC	6H-SiC	3C-SiC	Si	GaAs	2H-GaN	Diamond
Bandgap E_g [eV]	3,26	3,02	2,36	1,12	1,43	3,40	5,60
Critical Field E_C [MV/cm]	2,20	2,50	2,00	0,25	0,30	3,00	5,00
Sat. Velocity v_{sat} [10^7cm/s]	2,0	2,0	2,5	1,0	1,0	2,5	2,7
Electron Mobility μ_n [$cm^2/(V\,s)$]	$947_{\perp c}$ $1141_{\parallel c}$	$415_{\perp c}$ $87_{\parallel c}$	1000	1300	8500	400	2200
Dielectric Const. ϵ_r	10,0	10,0	9,7	11,9	13,0	9,5	5,0
Thermal Cond. γ [W/(cm K)]	3,5-5,9	3,5-5,9	3,5-5,9	1,5	0,5	1,3	20,0
Density ρ [g/cm^3]	3,2	3,2	3,2	2,3	5,3	6,1	3,5
Melting Point [°C]	2830	2830	2830	1420	1250	2500	4000
Direct/Indirect Bandgap	Indirect	Indirect	Indirect	Indirect	Direct	Direct	Indirect

For high frequency devices, SiC shows a better performance than Si due to its higher saturated drift velocity and lower permittivity. Through the higher thermal conductivity, a higher thermal flow can be achieved where heat can spread faster and more efficiently from critical device locations, such as junctions. These attributes make SiC an ideal semiconductor for high frequency, high power and high temperature devices as compared to Si or GaAs and contends strongly against GaN. In the contrary, GaN shines even more at high frequency operations because of its low output capacitance resulting in lower switching losses, but is outperformed at high power applications by SiC due to the latters limitation of the breakdown voltage which is limited up to 1000 V [22] [23] [24].

2.2 Thin layer Technologies

The outstanding material properties of SiC makes it an outstanding semiconductor to create superior devices than with Si, but this material has a big downside. Silicon carbide is very scarce in nature, found in rock samples from a meteor. Due to this, almost all of the SiC semiconductors are from synthetic origin [16]. Furthermore, producing SiC boules with the industry standard method of growing Si boules requires the material to transit into a liquid state. Silicon carbide's solid form does not have a stoichiometric liquid phase, hence, liquid SiC cannot be solidified without carbon precipitates, making it practically impossible to use melt growth for SiC bulk growth, so other methods are necessary to grow a pure crystal [16] [25]. By utilising the known procedures for SiC, whereas the modified Lely process is the state of the art, growing a pure SiC crystal is a lengthy and slow process (a few millimeters per hour) in comparison to the way Si is being grown with the Czochralski method [26]. This makes SiC wafers up to thirty times more expensive than conventional Si wafers according to a research conducted in 2015 [27]. The costs have surely reduced over the course of the years with improved manufacturing methods, but the SiC wafer price still remains much more expensive than Si.

For biomedical applications, a flexible chip is often necessary to handle the dynamic states of our body, like the pumping of our heart or the contraction/ exhalation of the lungs.

Furthermore, the high wafer costs calls for wafer reuse to make it economically attractive. The wafer thickness defined by the wafer manufacturer is chosen to guarantee thermal and mechanical stability during fabrication and processing [28]. Exfoliation of the device material enable wafer recycling, which reduces the costs associated with the wafer. Many researches in the industry use different techniques to use the expensive wafer or boule more than once. *Soitec S.A., Bernin, FR,* employs their modified SmartCut ™ process for SiC, dubbed SmartSIC ™ and *Infineon Technologies AG, Neubiberg, DE,* uses the SILTECTRA ™ COLD SPLIT technology to achieve similar results [29] [30].

In this thesis a novel spalling process for SiC named *Controlled Spalling* will be introduced and compared with the standard wire sawing method, as well as with the new technologies deployed by the aforementioned companies.

2.2.1 Wire Sawing

The wire sawing technique is the main slicing method in the industry for manufacturing brittle and hard materials like Si, SiC and sapphire. Multi-wire slurry sawing (MWSS) with slurry SiC abrasives is being utilised primarily for Si because of its smaller kerf loss and high throughput. A schematic overview is illustrated in Fig. 2.4 [31].

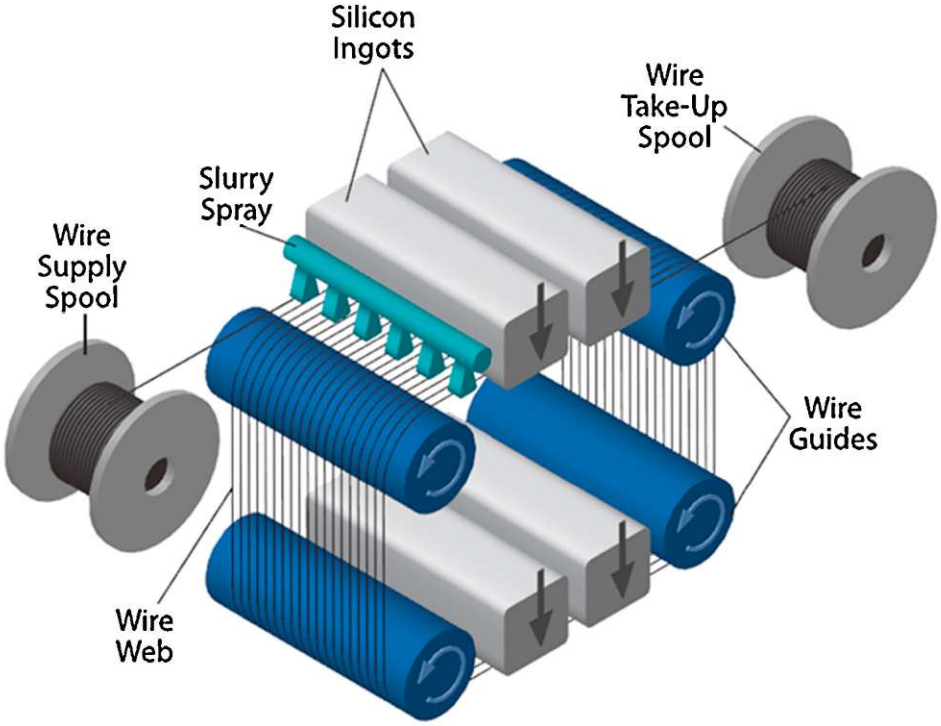


Fig. 2.4: An overview of multi-wire slurry sawing of wafers [31].

Most research conducted for wire sawing involves Si as it's the most employed semiconductor material in the world. But the shortcomings discovered with Si are also applicable to SiC as the manufacturing mechanism is the same and both semiconductors are brittle, whereas SiC is even harder, thus, causing additional challenges during processing. As cutting Si is achieved through slurry SiC abrasives, slicing SiC wafers is not feasible. So diamond wire sawing (DWS) technology is adapted for SiC and employed with stainless steel wires impregnated or electroplated with diamond grits which serve as cutting points. This method is the primary wafer slicing principle due to its low cost, ease of use and very mature manufacturing step as its established in the silicon cutting industry since the 1990s, as the silicon wafer size increased and no limitations exist regarding ingot diameter [31]. The principle behind diamond wire sawing is the direct interaction of the diamond grits with the wafer material, indenting and scratching into the target, carrying away the scratched material which is also considered as kerf loss [32] [33].

For SiC as a scarce material, having kerf loss during the slicing process reduces the yield which in turn increases the price per wafer. It has been reported that the kerf loss moves at a range of 200 µm - 250 µm, depending on the wire saw diameter and sawing speed [34] [35]. Furthermore, researches state that the sawing process can take up to 100 h with a 6-inch SiC wafer using the multi-wire sawing method [35] [36]. Additionally, machining very brittle and hard materials can cause damages to the substrate. Publications in this regard mention damage defects, residual stress and high surface roughness generated through wire sawing which require further polishing/ grinding steps to reduce the damages which causes the wafer price to rise even further [35] [37] [38].

For SiC to become more cost efficient, researchers have put their efforts into reducing the aforementioned downsides of wire sawing and even finding new approaches to reduce the manufacturing costs of the precious material so that the industry has a viable alternative to Si for specific applications, even by eliminating kerf loss [31] [35] [39].

2.2.2 SILTECTRA ™ Cold Split

A kerf-less method deployed by *Infineon* is called *SILTECTRA ™ Cold Split* and is based upon the method of stress induced controlled steady-state spalling [30] [40]. The principle behind *Cold Split* is based on thermal stress induced spalling and is illustrated in Fig. 2.5 and clearly depicts the possibility of splitting the wafer even after processing a device onto the substrate, represented by the red rectangular shapes.

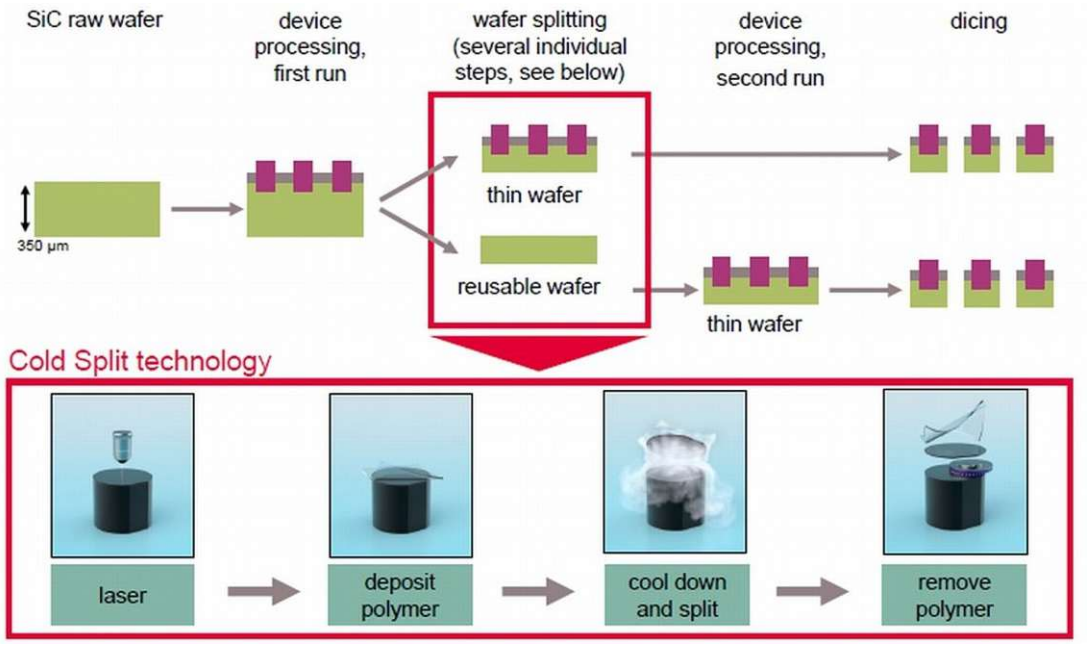


Fig. 2.5: The different process steps on how *SILTECTRA ™ Cold Split* is being performed [41].

The first step consists of laser conditioning using short laser pulses with a high-numerical-aperture, where the lateral plane of crack propagation is defined for the split process. By setting the laser photon energy below the material bandgap energy, the material appears transparent for the laser which can be set to penetrate to a specific depth, implementing a horizontal layer of modified material [30]. As the modified material layer is less resistant to stress than the semiconductor crystal, the crack will propagate along this plane [30]. The next step involves depositing a polymer layer (e.g. Polydimethylsiloxane). This polymer layer is cooled down to a level where the elastic modulus increases by over three times which generates the required stress, thus, the required force to achieve spalling [42]. Furthermore, temperatures of around −125 °C are being reported which makes use of a transition of the polymer to glass with a cooling time of approximately 1 min [30] [42]. In this state, applying a mechanical influence would split the semiconductor into two, where the new substrate has the desired thickness, depending on the laser penetration depth of the modified material. After the splitting process, the mother wafer is chemically-mechanically polished (CMP) and therefore prepared for a subsequent *Cold Split* process. The polymer is stripped from the substrate by mechanically peeling it off or etching it away [42].

As *Cold Split* is a kerf-less method, the amount of material waste is kept at a minimum, which is especially important for a precious semiconductor like SiC. Reports state that the amount of material lost is usually less than 100 µm [43]. In this report a study is conducted where the initial wafer started off with 500 µm. After the splitting process, which resulted in a 100 µm substrate, the subsequent CMP caused the mother wafer to have a thickness of 350 µm, thus, creating a

loss of 50 µm [43]. In comparison to the conventional wire-sawing process, *Cold Split* already achieves 50 % more wafers from a boule, thus, increasing the yield [44]. As the laser creates damages to the wafer and substrate, a polishing process is inevitable causing the loss of material and further processing steps. This makes this method more complex than wire-sawing and costly due to the fact the specific tools have to be acquired to employ this method as wire-sawing is already established for Si and slight modifications have to be made to include SiC.

This method is considered fairly young as first publications mention the process in 2013, so further research has to be conducted by *Infineon* and other researchers to improve yields and drive the costs of SiC substrates down by producing more wafers out of a single boule [42] [44] [45].

2.2.3 SMART SiC ™ Technology

SMART SiC ™ is based on the Smart Cut ™ process for Si developed in the 90s, whereas first experiments were conducted in 1991 at *CEA-Leti, Grenoble, FR,* which is a research institute in France. *Soitec* emerged from *CEA-Leti* as a start-up, offering the Smart Cut ™ process to the industry as an kerf-less alternative to wire-sawing [46]. Publications show that first research on adapting Smart Cut ™ for SiC go all the way back to 1997 where silicon carbide on insulator (SiCOI) structures were achieved with structures formed on polycrystalline SiC and on Si substrates [47]. The basic mechanism behind this technology is blistering, where this phenomenon comes into place when high dose implantations of inert gas or hydrogen ions in the material is done [46]. An overview of the process steps is depicted in Fig. 2.6 [48].

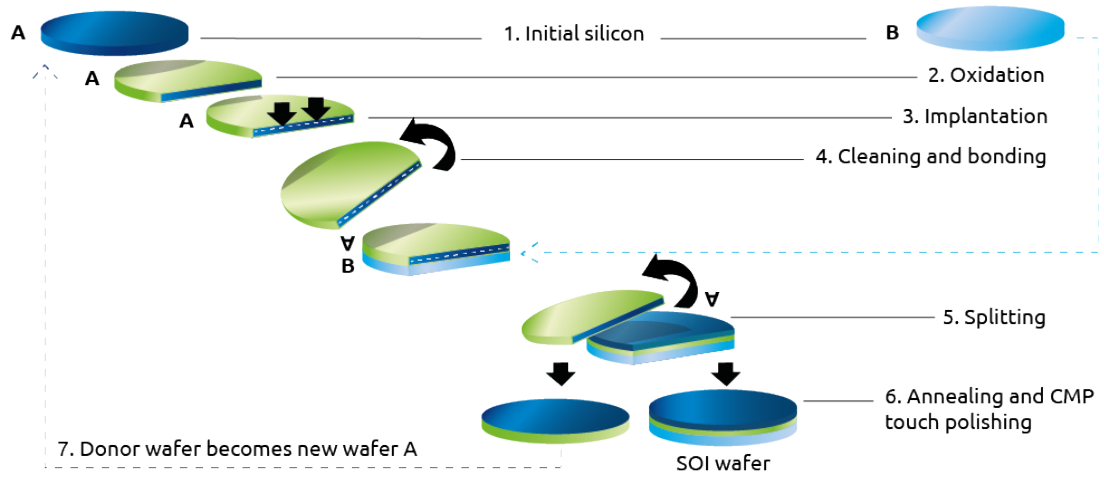


Fig. 2.6: Illustration of the Smart Cut ™ method with its process steps [48].

Starting off the process to create a silicon-on-insulator (SOI) wafer, the initial wafer (or *donor-wafer A* according to the schematics in Fig. 2.6) is thermally oxidized which in turn creates the buried oxide later in the process, therefore, isolating the silicon from the substrate once bonding occurs. Upon forming the oxide layer, the hydrogen (H) proton implantation step is conducted next. Depending on the implantation energy, the depth of the protons can be set, which in turn also defines the plane of separation for the splitting process. After implantation, the wafer is cleaned\polished by the means of CMP, flipped and the face where implantation occurred is bonded to the second wafer (acceptor wafer B in Fig. 2.6). In Step 5, splitting occurs through a two-phase heat treatment where in the first phase at around 400 °C - 600 °C, the donor wafer splits into two separate parts and can be reused again as a donor wafer for

another Smart Cut ™ run. The second heat treatment phase at around 1100 °C is performed to strengthen the chemical bonds between the freshly split layer and the Si wafer B. Finally, a CMP touch polishing phase is done to remove the micro roughness on the SOI structure which resulted from the splitting phase [49] [50].

This technique offers a very efficient material use of the expensive SiC wafer, especially since this method is also a kerf-less approach. Unfortunately, most literature on Smart Cut ™ and their analysis are based upon applying the procedure for Si. But the disadvantages can fundamentally also be translated to SiC.

Similarly to Cold-Split, a CMP step is included to iron out the micro cavities which results in a material loss comparable to *Cold Split*. As the H ion implantation is crucial for the basic mechanism of blistering to take place, a special proton implanter is necessary which results in higher costs than other wafer splitting methods [51]. Additionally, the implantation process causes the protons to collide with the atoms of the wafer which leads to structural defects, but the defects created near the implantation surface are removed via thermal annealing [52] [53]. Nevertheless, secondary defects arise like platelets formed at the end of the projected ranges and dislocation loops where these defects are barely removed [52] [53] [54] [55]. This makes an additional etching step necessary by removing a specific thickness of the wafer, causing even more wafer loss [51]. Furthermore, reports state that the efficiency of Si solar cells based on this kerfless thin wafer process is 13.2 % [53]. Other solar cells on the market, from Si crystalline cells to Si thin transfer submodules (35 µm thick), posses an efficiency of 26,7 % - 21,2 %, whereas the efficiency of the solar cell version with exfoliation through proton implantation is comparably low [56]. Research suggest that one of the main reasons for this low efficiency is the difficulty in texturing of (111) oriented wafers [57] [58].

Smart Cut ™ made remarkable progress in the last decades improving upon its technology and as time passes by, *Soitec* will further improve the process. At the *International Conference for Silicon Carbide and related materials* 2023, *Soitec* proposed that their SiC donor wafer on polycrystalline-SiC handle wafer has a upto 8 times better wafer conductivity than conventional SiC substrates on the market which allows for dies which are smaller for the given resistivity, thus, more dies can be made out of one wafer improving the yield and driving the costs down [59].

2.2.4 Physical Deposition Methods

Epitixial SiC thin film growth is a method which clearly differs from the above mentioned techniques introduced. Instead of cleaving off a thin layer from a mother substrate, the SiC layer is directly deposited onto a source of choice, where homoepitaxy stands for the growth of the deposit onto a substrate of the same material, and heteroepitaxy, where they differ from each other. A variety of growth techniques have been developed, from molecular beam epitaxy, sputtering to chemical vapour deposition (CVD), whereas, CVD is the most employed technique [26] [60] [61] [62]. But this technique cannot be primarily used for polycrystalline SiC substrates as the surface does not have an appropriate atomic periodicity for epitaxial growth [63].

CVD is a rather complicated process, but in simple terms, a target placed in a chamber gets heated up and gases containing the source material for the thin film decompose and deposit onto the target allowing a thin film to be created. The target is mostly a Si or SiC wafer which is being heated up to temperatures between 1400 °C - 1600 °C at pressures from 10 132,5 Pa - 101 325 Pa in the CVD chamber dubbed *reactor* [26]. With Si as the target, the additional challenge of having a lattice mismatch of approximately 20% if depositing cubic SiC, leads to a defective epitaxial film. By implementing a step before epitaxy, like the carbonisation of the Si surface which leads to the creation of a thin SiC layer, the SiC epilayer deposition is improved

[27]. As high temperatures are required, the reactor is designed in a way to have a reduced temperature gradient across the wafer and have a very good efficiency and uniform deposition [64] [65]. These CVD-reactors are called *hot-wall* CVD-reactors, where the wafer is placed on a heated susceptor inside a gas-flow channel. Typical hot-wall CVD reactors are illustrated in Fig. 2.7 and among them, the rotating holder and planetary warm-wall CVD-reactor are commonly used in the industry for mass production of SiC epitaxial wafers [64].

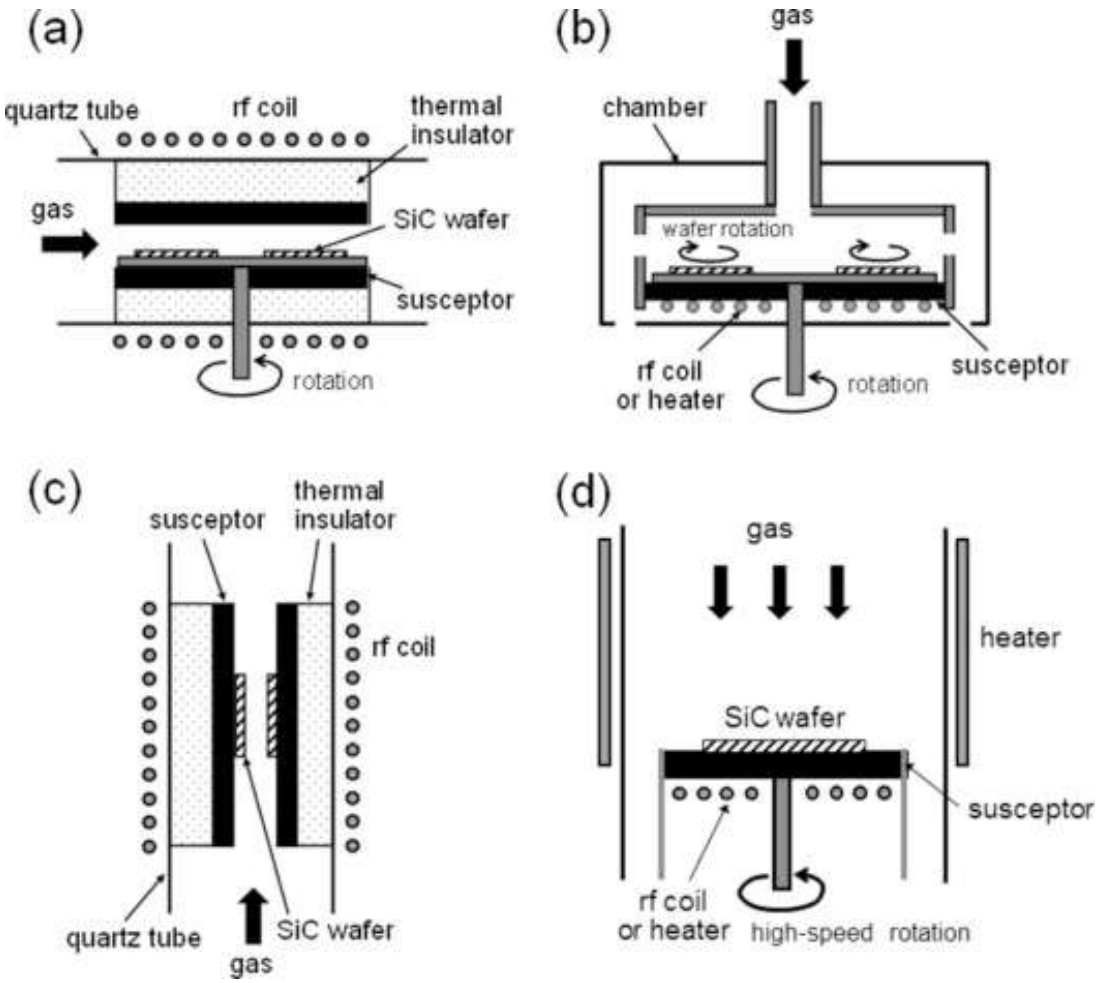


Fig. 2.7: Schematics of different hot-wall CVD reactors: (a) Horizontal hot-wall reactor, (b) hot-wall/ warm-wall planetary reactor, (c) chimney-type vertical hot-wall reactor, and (d) vertical quasi-hot-wall reactor [64].

The source gases used for growing SiC layers consist usually of a carbon (e.g. C_3H_8) and silicon source (e.g. SiH_4), whereas the carrier gas is H_2 [26] [61] [64]. The SiC growth process can be split up in two parts [64]:

1) *In-situ etching* with pure H_2, hydrocarbon/H_2, HCl/H_2 or SiH_4/H_2 as surface preparation step to remove subsurface damages which occur during substrate polishing at the same temperature as during SiC growth.

2) Main epitaxial growth, where the SiC layer is grown onto the substrate.

The growth-rate varies depending on the gas flow, temperature, reactor pressure and other factors, but typically ranges between 3 µm/h - 15 µm/h [64] [65]. Experimentally, even a few

hundreds of µm per hour have been achieved for thick epitaxial layers necessary for high-voltage devices and for creating even SiC boules, but the higher the growth rate, the higher the probability of defect generation in the grown SiC layer [26] [64].

This deposition technique allows for high quality, highly dense and pure thin layer creation. The level of control possible during deposition is unmatched in regard of layer thickness, surface morphology like surface roughness, the coating of complex shapes and reproducibility of the deposited layer in comparison to the kerfless layer transfer approach [65] [66]. But therein lies one of the problems of CVD. There are numerous control variables which have to be checked upon to ensure correct and appropriate layer deposition [67]. Furthermore, the production costs increases due to the high investment in complex CVD systems, the growth rate of several micro meters per hour increases production time which in turn also increases the cost through low throughput and, defect generation through dislocations or micropipes which decreases yield, thus, increasing costs even further [26] [64] [66] [67].

Chemical vapour deposition allows for SiC epilayers which are more controllable and have better characteristics than bulk sublimation-grown SiC wafers [26]. Research is in progress regarding increasing the growth rate and reducing the amount of defects during deposition for this technique to increase throughput and yield, therefore decreasing production costs [61] [64] [68]. As CVD is already established in the industry, efforts are made to improve it even more to get a viable, cost-friendly alternative in producing thin layers onto substrates in the future.

2.3 Controlled Spalling

In this thesis, the *controlled spalling* technology is utilised to achieve similar results to the previously mentioned, kerf-less methods. But in comparison to them, *controlled spalling* does not require any harsh processing steps like ion implantation with SMART SiC ™ or high/low temperatures similar to *Cold Split*. Unlike the aforementioned procedures where rather complex and expensive equipment is necessary, *controlled spalling* can be utilised with standard laboratory devices at room temperature which will not cause additional stress to the substrate and allows for cost friendly removal of substrate layers.

First observations of spalling were reported in 1985 where spontaneous spalling was deliberately performed by sputtering Nichrome on Si or GaAs wafers ranging from 2 to 4 inch in size creating 15 µm - 20 µm thin films. The authors of that time called the effect *spontaneous peeling* and predicted, that the technique can be utilised to produce thin layers for solar cell applications, peel away entirely finished circuits for SOI, reducing the fabrication cost as this peeling can be done over and over again on the same wafer and even create trenches which should have similar advantages as etching trenches in Si [69].

The fracture of brittle materials is known for a long time, but a useful mathematical model was developed in the late 1980s. With this model the fracture depth and the necessary tensile stress can be calculated with given material parameters [40].

Almost 30 years after the observation of the "spontaneous peeling" effect, researchers came up with a method to make this "spontaneous peeling" controllable, in which the fracture depth and propagation can be tuned. Naming it *controlled spalling*, the process has been used for Si, Ge and III-Vs (III-V refers to compound semiconductors containing elements from groups III and V in the periodic table) with, or without epitaxial structures [70].

Based upon the fracture in brittle substrates, this technique requires a stressor film on the surface of the brittle substrate. If certain conditions are met, fracture will move to a specific depth of the substrate, propagate parallelly to the surface and cause the removal of the top surface from the brittle substrate.

The method for SiC can be split up in five steps:

1) Sputtering of a platinum (Pt) conductor layer for Metal-Assisted-Photochemical-Etching (MAPCE).
2) Creating a porous structure by using MAPCE.
3) Electroplating a nickel (Ni) stressor layer which adheres due to the porous structure.
4) Applying a handle layer onto the stressor layer for the spalling process.
5) By using an external force and lifting off the handle layer, crack is initiated and propagates through the substrate.

An illustration to the steps can be seen in Fig. 2.8 [71].

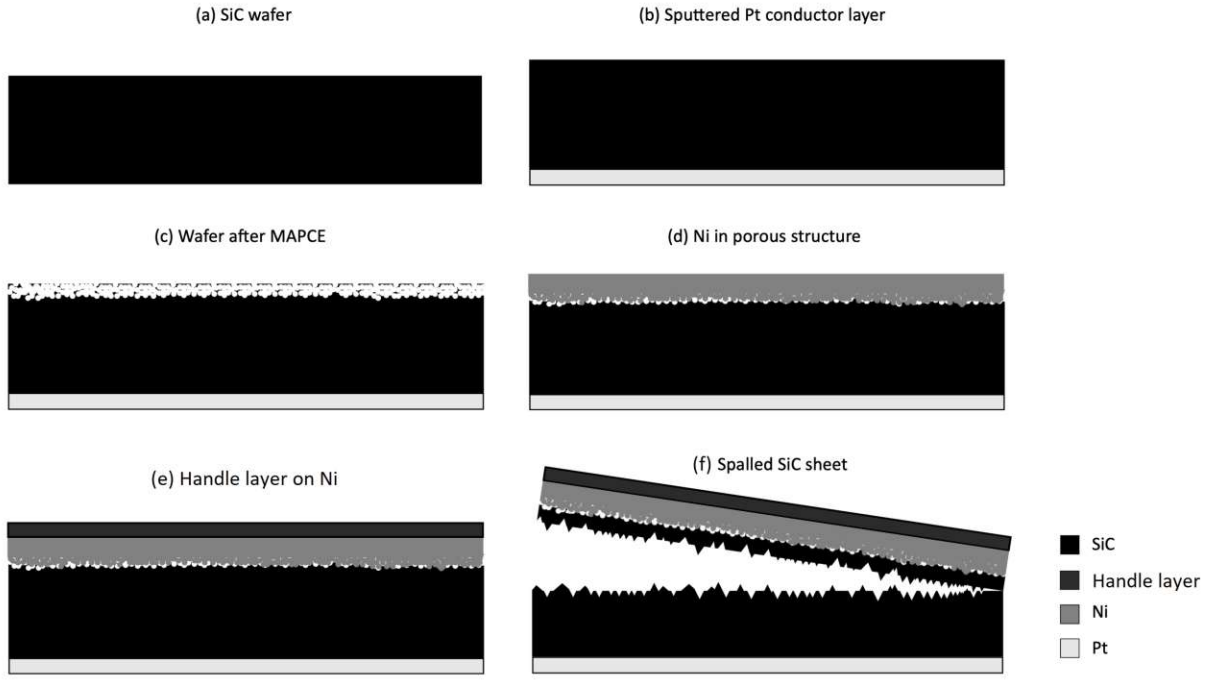


Fig. 2.8: Five step process to achieve controlled spalling: (a) Plain SiC substrate, (b) Pt conductive layer deposition, (c) etching a porous structure, (d) electroplated Ni layer is adhered to SiC substrate through porous structure, (e) handle layer is attached and (f) external force is used to lift off handle layer subsequently leading to spalled SiC layer [71].

To the best of the author's knowledge, controlled spalling via electro deposition has not been achieved for SiC due to its high hardness and the problem of electroplated layers not adhering to the SiC substrate. With the help of metal-assisted-photo-chemical-etching (MAPCE), a porous structure is created surface-near on the SiC substrate [72]. After porousifying the surface, the five steps depicted in Fig. 2.8 are achievable as there is no hindrance in electroplating a stressor layer onto the SiC substrate which paves the way for *controlled spalling*. At the last step of the spalling procedure, it is important to note, that the spalled SiC layer is a few µm thick, whereas the porous structure is a few 100 nm thin. Therefore, the crack propagates way beyond the porous structure and peels off a thin foil from the mother SiC substrate. This in turn enables

a cost-effective method and at same time being more gentle to the material than the other techniques, while using standard laboratory equipment, enabling SiC substrate reuse at room temperature which has not been demonstrated so far. Considering the high cost of SiC wafers in comparison to Si wafers, this feat is especially remarkable as it helps drive the cost of SiC further down making it more competitive.

Chapter 3

Theory

This chapter will provide theoretical insights on the process steps mentioned in the previous chapter to achieve *controlled spalling*.

3.1 MAPCE

Metal-assisted-photochemical-etching is being utilised to create a porous structure on the SiC surface. Porous materials can be used for catalytic applications due to their large surface area and for biotechnological applications, as these materials can be utilised as a semi-permeable membrane for sampling molecules [73]. For this research topic specifically, the porous structure is used as anchor point for Ni during electroplating so that a Ni layer can adhere to the surface.

Chemically seen, the process is similar to etching a porous layer on Si. Literature states, that the dissolution of the material takes place with two reactions [73] [74] [75]:

1) The formation of silicon dioxide (SiO_2).

2) Oxide removal in the electrolyte.

   -) Reaction of oxidation happens in the presence of positively charged carriers (holes), therefore, a sufficient concentrations of holes has to be present to initiate the pore etching process.

To fulfil the first criteria, the oxidation of the SiC surface, a thin noble metal layer has to be deposited onto the SiC substrate via e.g. sputter deposition. As soon as both materials come into contact, their respective Fermi levels become equal resulting in a Schottky contact. An annealing procedure creates an ohmic contact [76] [77]. This metal layer functions as the cathode, whereas the SiC surface acts as the anode. Once the substrate is in the etchant containing hydrofluoric acid (HF) and an oxidising agent like e.g. hydrogen peroxide (H_2O_2) or sodium persulfate ($Na_2S_2O_8$), the oxidising agent is reduced at the surface of the noble metal layer and SiC is oxidized at the anode [78]. For the reaction of the oxidation to occur, hence, to fulfil the second criteria of etching a porous layer, the generation of positively charged carriers is carried out with UV irradiation at an energy higher than the bandgap of the semiconductor [79]. With the ultra-violet (UV) light, valence electrons are excited to the conduction band for the weakening of the Si-C bonds and the oxidation of the SiC surface, which is then dissolved with HF [80] [81]. Additionally, the excitation generates an electric field which makes the depletion layer thinner. Utilising the noble metal contact, the electrons can leave the SiC substrate through the cathode, react with the oxidising agent and increase the etching rate through the consumption of electrons [77].

The chemical reaction equation at the metal layer cathode is

$$H_2O_2 + 2\,H^+ + 2\,e^- \longrightarrow 2\,H_2O \tag{3.1}$$

followed by the reaction at the SiC anode

$$\mathrm{SiC} + 2\,\mathrm{H_2O} + 4\,\mathrm{h^+} \longrightarrow \mathrm{SiO_2} + 4\,\mathrm{H^+} + \mathrm{CO_2} \tag{3.2}$$

$$\mathrm{SiO_2} + 6\,\mathrm{HF} \longrightarrow \mathrm{H_2SiF_6} + 2\,\mathrm{H_2O} \tag{3.3}$$

where at the end, the porous SiC structure is created.

3.2 Electroplating

Electroplating allows for a very cost-efficient possibility to deposit a thin layer of metal in comparison to CVD or sputter-deposition where complex machines are necessary. The biggest advantages lies herein, that standard laboratory equipment is sufficient to utilise this technique. The electroplating process in itself is a well understood method. Basically in the most cases, it consists of an electrolyte solution containing metal ions and two electrodes, whereas one will be the target of the deposition and the other is made up of the metal to be deposited. In this case, as soon as direct current is set up in a way to flow from one electrode to the other, the flow of current causes the anode to dissolve and the cathode to get plated with the metal [82]. An overview of the process can be seen in Fig. 3.1.

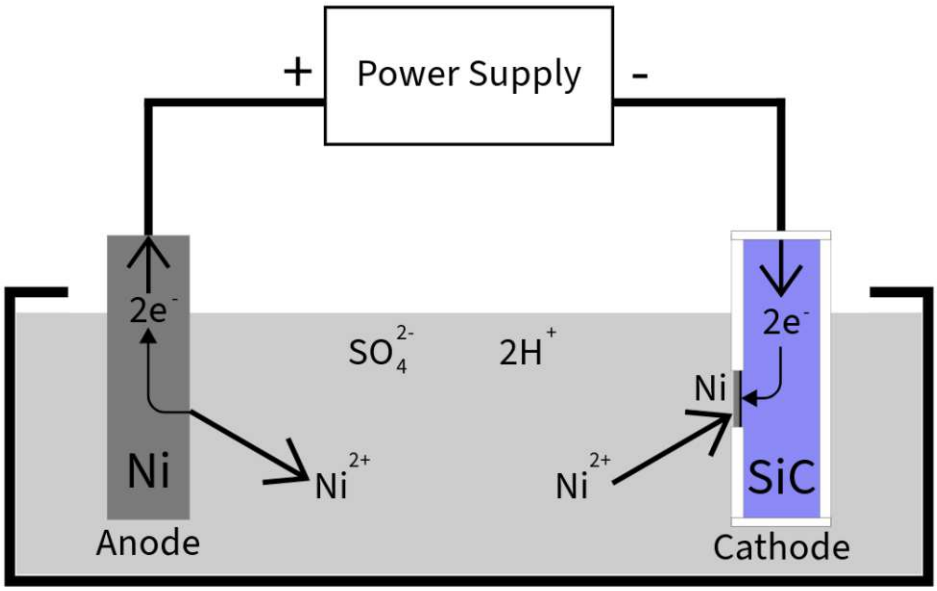


Fig. 3.1: Schematics of the Ni plating principle. The SiC substrate (cathode), which is being plated, is partly exposed to the Watt's bath solution.

Specifically, a Watt's bath is used for plating the porous surface of the SiC substrate which was found bei Oliver. P. Watts in 1916, where he formulated an electrolyte solution consisting of nickel sulfate, nickel chloride and boric acid [83]. He stated that the pH value of the electrolyte bath plays an important role in achieving consistent Ni plating results, so adding boric acid as a buffer to control the pH in the solution was necessary otherwise inefficient and poor plating will occur with nickel oxides being deposited [83] [84]. The principle behind this electrodeposition method is similar to other electroplating processes. Current flows between two electrodes, whereas one electrode (cathode) gets plated with Ni and the other electrode (anode) is dissolved if it is made up of nickel. The electrodes are immersed in an aqueous, conductive solution made

up of nickel salts and boric acid. As depicted in Fig. 3.1, the Ni in the solution is present as divalent, positively charged ions (Ni^{2+}). As soon as a current flows, the positive Ni ions react with two electrons ($2\,e^-$) and are converted to metallic nickel (Ni^0) at the cathode surface [85]. The reverse occurs at the anode, which is made of Ni, where the nickel is dissolved to form divalent, positively charged ions which enter the solution. Therefore, the electrochemical reaction can be written as

$$Ni^{2+} + 2\,e^- \rightleftharpoons Ni^0 \tag{3.4}$$

With this reoccurring cycle, the plating can go on as long as there is enough Ni at the anode and the pH stays constant [85].

The deposition amount m on the cathode is bound to Faraday's law

$$m = 1.095 \cdot aIt \tag{3.5}$$

and is directly proportional to the product of current I and time t multiplied with the current efficiency ratio a. In Eqn. 3.5, the proportionality constant 1.095 is derived from the atomic weight of nickel M divided by the number of electrons n in the electrochemical reaction times the Faraday's constant F as in Eqn. 3.6 [85].

$$\frac{M}{nF} = 1{,}095\,\mathrm{g/(A\,h)} \tag{3.6}$$

Expression 3.5 can be used to derive the average coating thickness by dividing it by the density of nickel d and the the surface area A, which is going to be electroplated [85].

$$h_s = \frac{m \cdot 100}{dA} = \frac{12.294 \cdot aIt}{A} \tag{3.7}$$

The factor 100 in Eqn. 3.7 is being used to derive the coating thickness in µm. With this film/substrate combination, tensile stress can be built up to achieve *controlled spalling*.

3.3 Controlled Spalling

Electrodeposition is conducted to attain lattice mismatch, induce structural defects, such as interstitial defects, and produce grain boundary regions to create residual stress in the Ni film, which in turn induces controlled spalling by applying an external force. In literature and controlled spalling terminology, the deposited Ni layer is labelled as *stressor layer* or *tensile layer* [70]. Basically, this technique is based on the fracture mechanics theorem which has been set up by Suo and Hutchinson for the *cracking in brittle substrates beneath adherent films* [40]. According to the theory to achieve spalling, the strain between layer and substrate which is caused by the aforementioned factors leading to the residual stress in the Ni stressor layer, has to generate an energy release rate G greater than the substrate's critical energy G_c, which means

$$\sigma_f{}^2 \cdot h_s \propto G > G_c\,, \tag{3.8}$$

and this energy release rate is dependent on the stress σ_f within the film and the stressor layer thickness h_s [40] [70] [86] [87]. By releasing this energy $G > G_c$, a crack is formed which travels to a specific depth and propagates parallel to the surface [87]. This parallel moving crack results into the removal of the upper surface of the substrate if the adhesion of the stressor layer is sufficient enough. If the residual stress in the deposited Ni stressor layer already generates an

energy release rate higher than the substrate's critical energy, then spalling will occur without any external force [69]. This way of spalling is called *spontaneous spalling* and is not desired as the crack propagation is not controllable which results in inhomogeneous spalled layers [88].

In this theoretical model, the researchers stipulated the stress field induced by the strain mismatch in the substrate/film layer is similar to the the stress produced during edge loading [40]. According to the theory, the crack tip consists of the mode I (opening stress) and mode II (shear stress) components as in Fig. 3.2.

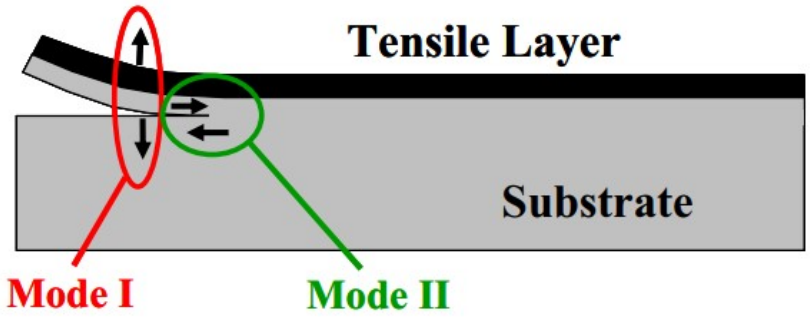


Fig. 3.2: A depiction of substrate spalling with the mode I and mode II stress components [89].

These stress intensity factors are calculated with the analysis from Suo and Hutchinson with

$$K_I = \frac{P}{\sqrt{2hA}}\cos(\omega) + \frac{M}{\sqrt{2h^3 I}}\sin(\omega) \tag{3.9}$$

$$K_{II} = \frac{P}{\sqrt{2hA}}\sin(\omega) - \frac{M}{\sqrt{2h^3 I}}\cos(\omega) \tag{3.10}$$

P = External, longitudinal load
M = External moment
ω = Function depending on material parameters
h = Stressor layer thickness
A = Dimensionless, positive number dependent on non dimensional, effective cross section
I = Dimensionless, positive number dependent on moment of inertia

where two composite beams are considered. These beams are under longitudinal load P and moment M and by applying an external force, the stress components initiate fracture [40]. In the case of the deposited Ni stressor layer, the discontinuity at the edge between substrate and stressor layer can initiate fracture [70]

Observing brittle materials, the crack moves along a trajectory where the shear stress is minimised, thus, the mode II stress K_{II} becomes zero [90]. In an ideal case, the deposited film with its stress field guides the fracture parallel to the surface. A depiction of this explanation can be seen in Fig. 3.3.

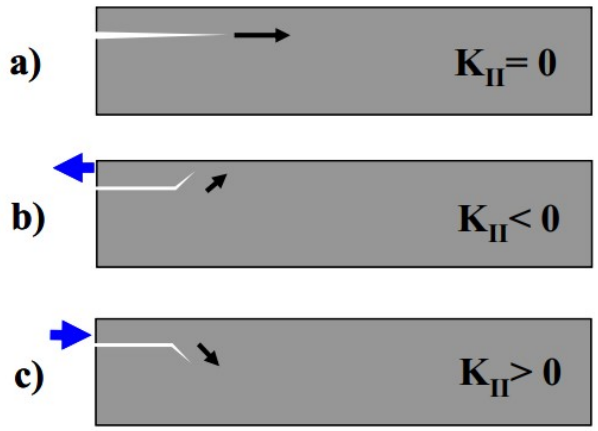


Fig. 3.3: The crack trajectory depending on the mode II stress [89].

To calculate the steady-state-cracking depth, hence, the maximum depth the crack will go to, the shear stress K_{II} has to be set to zero where the depth can be derived from.

$$K_{II} = \frac{P}{\sqrt{2hA}} \sin(\omega) - \frac{M}{\sqrt{2h^3 I}} \cos(\omega) = 0 \tag{3.11}$$

Suo and Hutchinson claim the steady-state-cracking depth relies heavily on the stressor layer/ substrate thickness ratio and stiffness ratio α between the bilayers, involving the plane strain elastic moduli and the Poisson's ratio of the respective materials [40]. The stiffness ratio α is calculated with

$$\alpha = \frac{(\overline{E}_{Ni} - \overline{E}_{SiC})}{(\overline{E}_{Ni} + \overline{E}_{SiC})} \tag{3.12}$$

whereas the plane strain elastic moduli $\overline{E}_i$ is defined by

$$\overline{E}_i = E_i \cdot (1 - \nu_i) \tag{3.13}$$

with E_i being the elastic modulus and ν_i the Poisson's ratio of the respective material.

Deriving the theoretical spall depth leads to solving Eqn. 3.9 to get an appropriate mode I opening stress K_I which is also dependent on the layer substrate thickness ratio and the residual stress σ_f of the Ni stressor layer [40] [89]. Setting this opening mode stress equal to the fracture toughness K_{IC} of the substrate, critical values of stressor layer thickness and residual stress σ_f can be determined to find the right combinations to allow appropriate crack propagation which is sufficient to break atomic bonds of the material. It's also detrimental to find thickness stress combinations which bring the substrate on the brink of spontaneous spalling, as controlled spalling relies on applying an external force to lead the crack propagation to get homogenous layers and therefore reduce the amount of polishing, to keep the material loss to a minimum.

The stress within the Ni stressor layer film σ_f consists of an intrinsic stress σ_I which is built up during a deposition process and a thermal stress σ_T.

$$\sigma_f = \sigma_I + \sigma_T \tag{3.14}$$

The thermal stress is generated through a mismatch of thermal expansion coefficients (CTE) due to different materials of the substrate/ stressor layer. Through a temperature change, this thermal stress is generated in a linear approximation, which is defined as

$$\sigma_T = E_{bf} \cdot (\alpha_s - \alpha_f)(T - T_0) \tag{3.15}$$

where E_{bf} is defined as the biaxial modulus of the Ni film

$$E_{bf} = \frac{E_f}{1 - \nu_f}$$

and α_s/α_f are the CTE of the SiC substrate and Ni film respectively. T is the reference and T_0 is the initial temperature. For a thermal tensile stress to occur, a stressor layer film with a higher CTE than the substrate has to deposited and then, the temperature has to be decreased [91].

Intrinsic stress occurs after deposition techniques like physical vapor deposition (PVD) and electroplating [92] [93]. The intrinsic stress of the deposited Ni layer onto the SiC substrate is caused by grain boundary relaxation due the interatomic forces being present at the gap between grains, thus, a lattice mismatch in the grains takes place between the two materials [94]. The stressor layer thickness is controllable through the factors in Eqn. 3.7 and the intrinsic stress generated through deposition can be calculated with a modified version of Stoney's formula

$$\sigma_I = \frac{E_{SiC} \cdot t_{SiC}^2 \cdot (\kappa - \kappa_0)}{6 \cdot t_{Ni}(1 - \nu_{SiC})} \tag{3.16}$$

E_{SiC} = Young's modulus of the substrate
t_{SiC} = Thickness of the substrate
κ_0 = Curvature of the substrate before stressor layer deposition
κ = Curvature of the substrate after stressor layer deposition
t_{Ni} = Thickness of the Ni stressor layer
ν_{SiC} = Poisson's ratio of the substrate

where most of the variables depend on material constants [95] [96] [97].

The curvature of the substrate before and after deposition can be calculated with the basic calculus of a line $y(x)$ where the curvature κ and the radius of the curvature r_{SiC}

$$\kappa = \frac{1}{r_{SiC}} = \frac{|y''|}{(1 + y'^2)^{\frac{3}{2}}} \tag{3.17}$$

is derived from the derivative and second derivative of $y(x)$ [98]. The appropriate function $y(x)$ can be found by using a white light interferometer on the plain substrate, as well as on the substrates after Ni deposition, which will give the surface displacement.

Controlled spalling is performed on a height and length adjustable ramp, where these parameters alter the conditions for the spalling initiation process. A depiction of the system can be seen in Fig. 3.4. A handle layer sticky tape is pre-adhered onto the substrate and the cylinder exerts a pull force which peels and spalls off a layer of SiC with the Ni stressor layer.

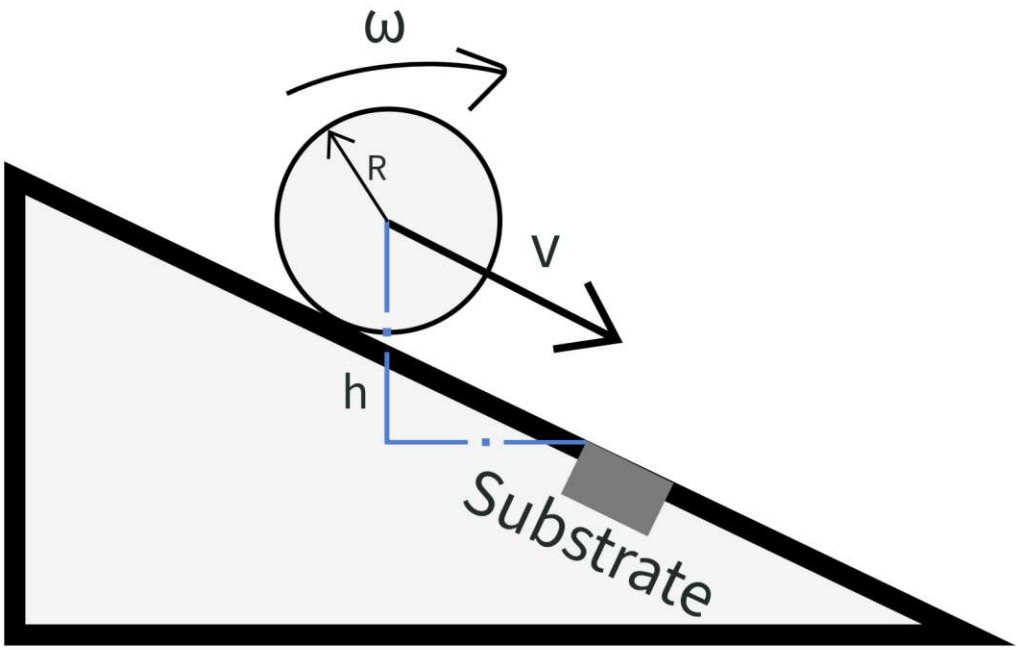


Fig. 3.4: Schematics on how the cylinder rolls on an inclined ramp.

By assuming that the cylinder has no friction, does not slip down the ramp and the whole setup does not change its material properties during the process, kinematics can be applied to the cylinder-ramp system

$$E_{KinTotal} = \frac{1}{2} \cdot m \cdot v_0^2 + \frac{1}{2} \cdot I \cdot \omega^2 \tag{3.18}$$

where the variables are defined as

$E_{KinTotal}$ = The total kinetic energy of the ramp system
m = Mass of the cylinder
v_0 = Velocity of the cylinder at the center of mass
I = Moment of inertia at the center of mass of the cylinder
ω = Rotational velocity.

With the assumptions previously mentioned and the law of energy conservation, the total kinetic energy of Eqn. 3.18 has to be equal to the potential energy

$$\frac{1}{2} \cdot m \cdot v_0^2 + \frac{1}{2} \cdot I \cdot \omega^2 = m \cdot g \cdot h \tag{3.19}$$

where g is the gravity constant and h is the height of the ramp. With the rotational velocity ω defined as

$$\omega = \frac{v_0}{R}$$

and the moment of inertia I of a solid cylinder is

$$I = \frac{1}{2} \cdot m \cdot R^2 \,,$$

Eqn. 3.19 can be rewritten as

$$\frac{1}{2} \cdot m \cdot v_0^2 + \frac{1}{2} \cdot \frac{1}{2} \cdot m \cdot R^2 \cdot \frac{v_0^2}{R^2} = m \cdot g \cdot h$$

out of which the velocity is derived from

$$v_0 = \sqrt{\frac{4}{3} \cdot g \cdot h}\,. \tag{3.20}$$

The force exerted by the cylinder to peel off the handle layer is ideally perpendicular to the velocity. Generally, the force F is defined as the mass of the cylinder m times the centripetal acceleration of the cylinder a_c, where this acceleration is a function of the cylinder velocity v_0 and radius R. Therefore, the force can be calculated by

$$F = m \cdot a_c = m \cdot \frac{v_0^2}{R} = \frac{4}{3} \frac{m \cdot g \cdot h}{R}\,. \tag{3.21}$$

With Eqn. 3.21, as most of the variables are constant, the force can be altered by changing the ramp height h. Increasing the height of the ramp also increases the peeling force F.

Chapter 4

Experimental Details

At first the pre-processing steps with their respective equipment are explained and how they are set up to prepare the sample. Furthermore, the main experimental setup with its features and configuration are described.

4.1 Substrate Properties

In this study, the sample used to conduct spalling experiments is a 4H-SiC substrate. The 4H-SiC variant has been selected due to this polytype being readily available and is commonly used in industry. Production grade 4-inch 4H-SiC wafers from *SiC-Crystal GmbH* (Nuremberg, Germany) were purchased with a thickness of 350 µm. These wafers were cut into 20 mm × 20 mm pieces by using standard dicing equipment.

4.2 Surface-near Porosification

The porosification process is done with the MAPCE procedure. Prior to etching, a noble metal layer of Pt is sputter deposited with a *Von Ardenne - LS730S* (Dresden, Germany) sputter equipment. The substrate is immersed into an etching solution consisting of hydroflouric acid (1,31 mol/l HF) and hydrogen peroxide (0,15 mol/l H_2O_2) which acts as an oxidation agent. To create the charge carriers for the oxidation reaction, a custom built UV - light source with a wavelength of 254 nm is utilised which illuminates the sample for the time it is immersed. A illustration of the setup is depicted in Fig. 4.1.

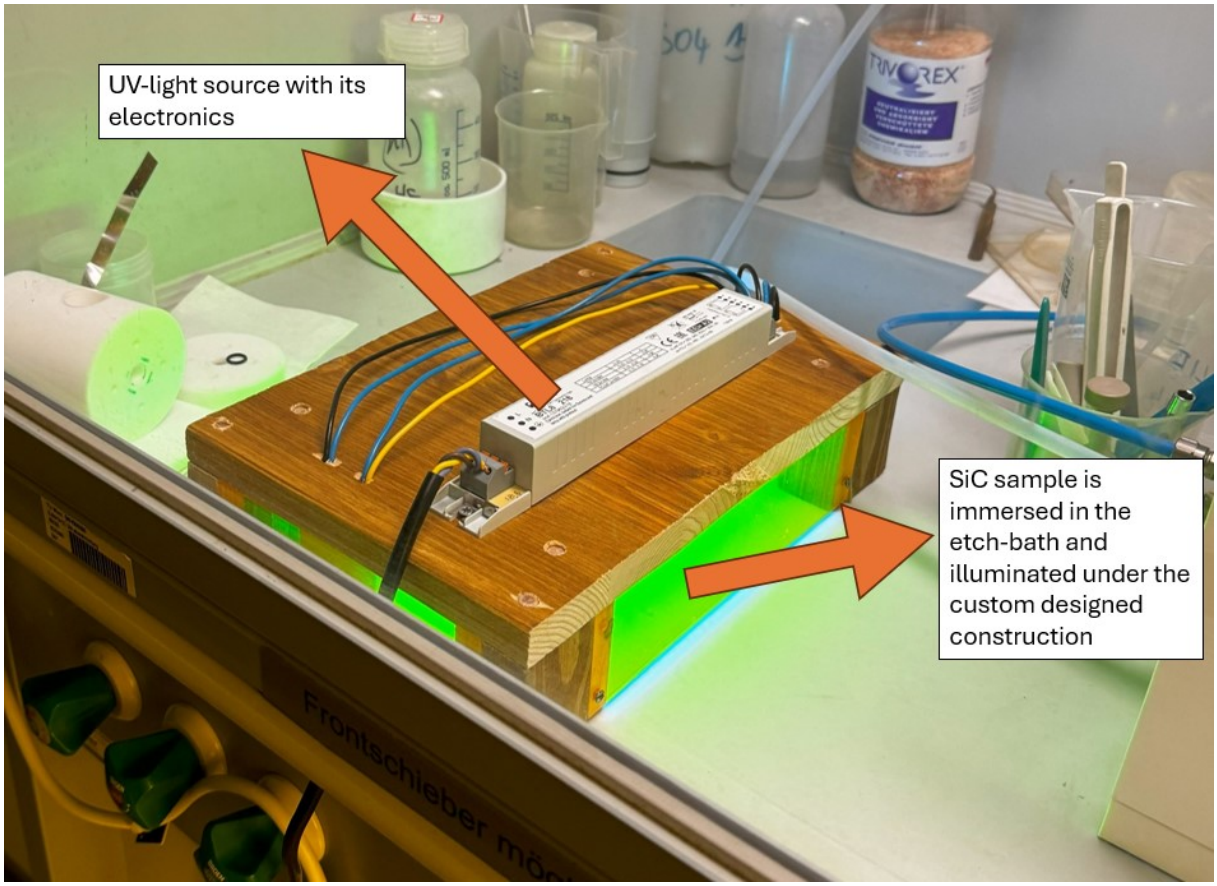


Fig. 4.1: Custom built UV light source illuminating the etching bath for the MAPCE procedure.

To control the depth of porosification, the etching times were varied between 15 min–45 min and the oxidising agent is replenished every 15 min to ensure a steady supply for the etching reaction [72].

4.3 Watt's Bath Setup

For the electrochemical deposition, a solution consisting of nickel sulfate hexahydrate (300 g/l $NiSO_4\,6\,H_2O$) and boric acid (35 g/l H_3BO_3) is used for the Watt's - electroplating bath. The liquid in its flask is placed upon a magnetic stirrer from *IKA ™C-MAG HS7* (Staufen, Germany) which is set to 60 °C and ensures a homogenous mixture by stirring the solution with approximately 550 min^{-1}. A custom designed and built substrate holder is used to fixate the sample into place, which serves as the cathode, exactly opposite to the Ni - anode which is also been fixated with a self-built holder as seen in Fig. 4.2. These holders and their fastening equipment are constructed out of non-conducting materials in order to prevent the holders from interfering in the Watt's electroplating bath.

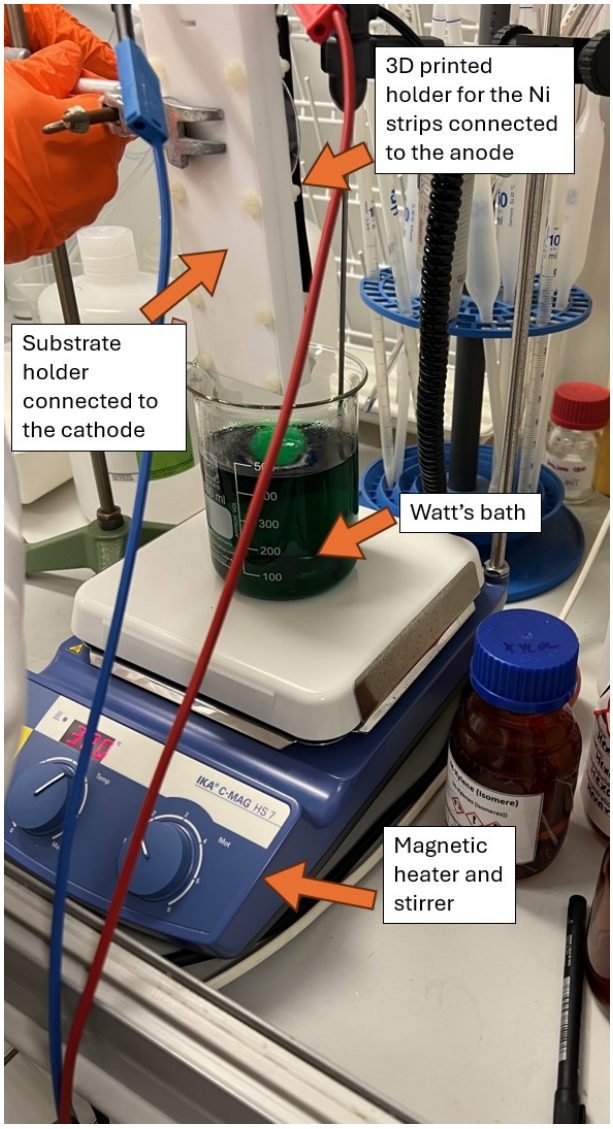


Fig. 4.2: Electroplating setup with the custom built substrate holder.

This substrate holder seals off the sample from the Watt's bath solution except for a circular area on the substrate with a diameter of 11 mm where the nickel will be deposited, as it is depicted in Fig. 4.3. To seal off the substrate entirely from the electroplating bath except for the exposed area, three different sealants were tested which were inserted between the two halves of the substrate holder. The sealants are displayed in Tab. 4.1. As the substrate itself has a 20 mm × 20 mm area, the plating diameter of 11 mm was selected in a way to leave enough areal headroom to fixate the sample for the upcoming spalling attempts.

Tab. 4.1: Sealants used for the custom substrate holder

Sealant #	Material
1	Viton ®FKM (fluorocarbon-based fluoroelastomer)
2	EPDM E9566 (ethylene-propylene-diene-monomer rubber)
3	Foam Rubber EPDM (ethylene-propylene-diene-monomer rubber)

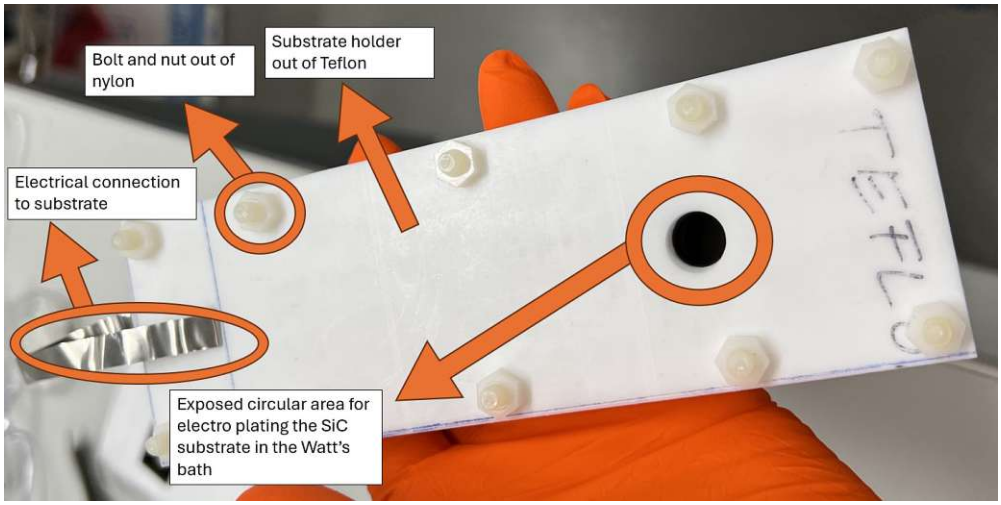


Fig. 4.3: Custom designed substrate holder with a 11 mm exposure for Ni deposition.

Controlling the deposition thickness is bound to a few variables, according to Egn. 3.7. To keep the number of parameters in a reasonable range, only the deposition current was varied between 0,02 A - 0,14 A in 0,02 A increments. The plating time was kept constant for 10 min.

4.4 Spalling Construction

To conduct spalling experiments, a self-designed and 3D printed ramp with a length of 121 cm was constructed with features to attach the substrate to the ramp. This ramp was designed in a modular way where the length can be varied to alter the velocity of the cylinder. The height of the ramp can also be varied between 0 cm - 40 cm to additionally influence the velocity of the rolling cylinder. The substrate is fixed with a double sided adhesive, which can be easily removed by pulling off the strips without damaging the substrate. Fig. 4.4a) depicts the spalling ramp and the orange circle shows, where the substrate is placed for the experiments as in 4.4b).

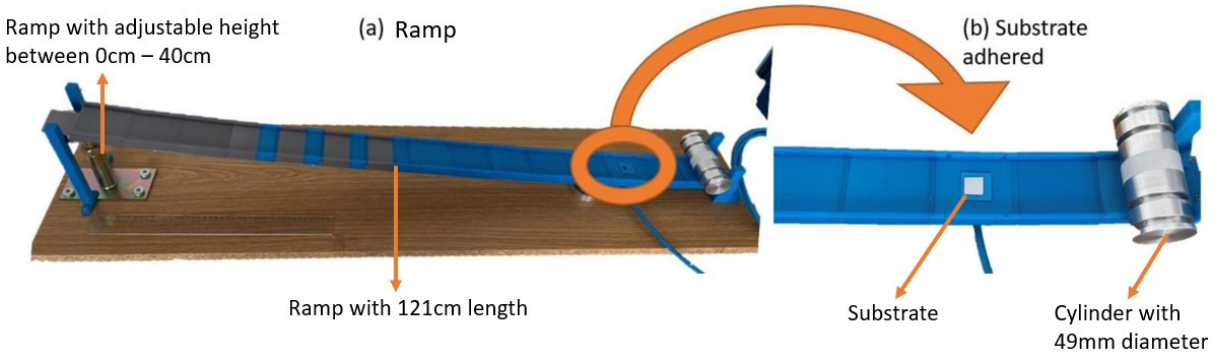


Fig. 4.4: Picture of the designed and manufactured ramp with a length of 121 cm used for controlled spalling experiments in (a). Close view on the position (b), where the sample to be spalled is placed, while spalling takes place by pulling off the handle layer with a thin foil attached to it. These handle layers have distinct peeling strengths as reported in Tab. 4.3.

Furthermore, another double sided, pressure sensitive tape is selected as a handle layer for flexible force transfer. This tape is partly applied onto the wafer piece and rolled out onto the

ramp so that the rolling cylinder adheres to it and strips off a thin foil while passing the wafer, as depicted in Fig. 4.5. This flexible tape aids in retrieving the spalled layer without damaging it.

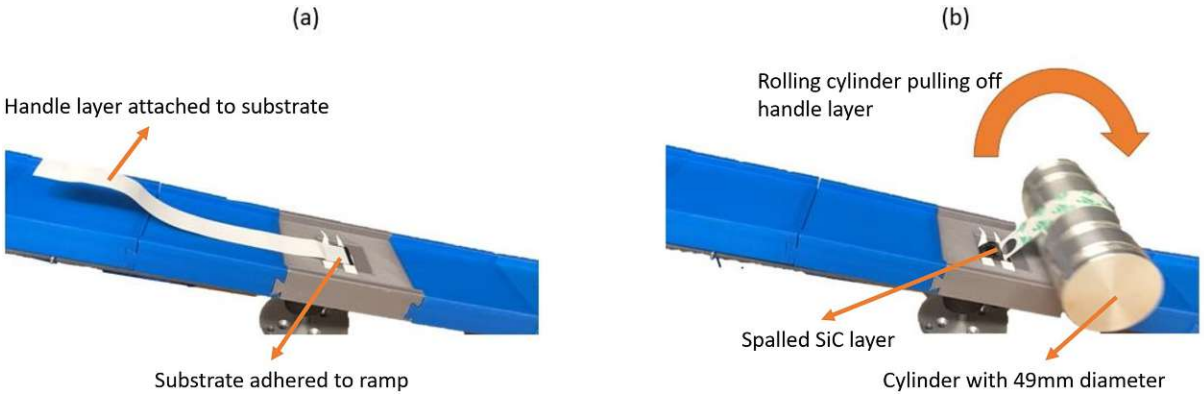


Fig. 4.5: Double-sided pressure tape prepared on the ramp and adhered to the substrate (a). When the cylinder rolls from the left side down the ramp, the handle layer adheres to the cylinder and peels off a thin foil from the wafer (b).

Three cylinders with different mass and diameters were evaluated as described in Tab. 4.2.

Tab. 4.2: Cylinder parameters

Cylinder #	Mass in [g]	Diameter in [mm]	Moment of Inertia in [kg m^2]
1	228,5	30	0,0001028
2	589,0	49	0,0007071
3	921,0	60	0,0016578

In addition, three different double sided sticky tapes from *3M* (Maplewood, Minnesota, U.S.) were tested with this setup. The attributes of these tapes are mentioned in Tab. 4.3.

Tab. 4.3: Double sided sticky tape parameters

Tape model	Peeling strength of tape in [N/mm]	Width in [mm]
3M 904	0,50	19
3M 98010LVC	1,16	12
3M 9087	1,55	19

To attain controlled spalling, the right combinations of porosification depth, Ni deposition thickness, cylinder weight, sticky-tape peeling strength and ramp height have to be found by conducting a series of experiments which are evaluated.

Chapter 5

Results and Discussion

5.1 Spalling Results

The results of the spalling experiments will be presented and discussed, including the problems during the initial tests, a few solutions and an interpretation on how controlled spalling has worked out.

5.1.1 First pre-investigations for Controlled Spalling

To assess the different parameters described in the previous chapter, a step-by-step approach is selected in finding the optimal setup for controlled spalling.

In the first instance, research is done by porosifying the C-face of the samples with 15 min, 30 min and 45 min MAPCE-times in order to find the minimum requirement for the Ni layer to ensure a sufficient adhesion to the SiC surface during electroplating.

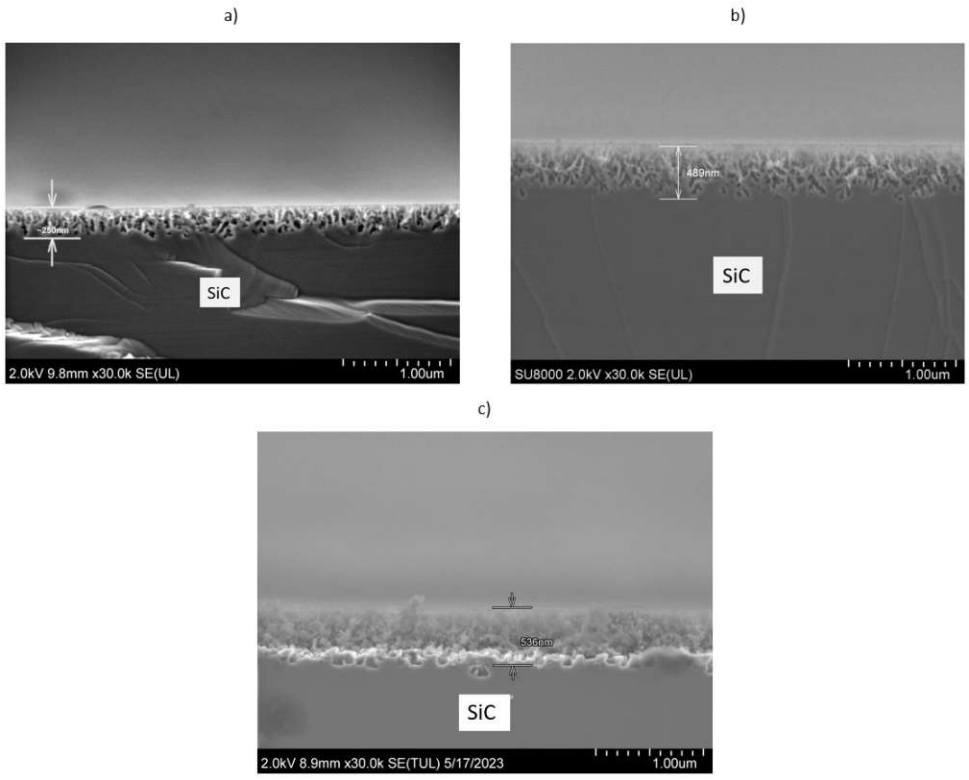


Fig. 5.1: Cross-sectional SEM micrographs to estimate the porosification depth results of 4H-SiC after different MAPCE times. a) shows the depth after 15 min, b) after 30 min and c) after 45 min of etching.

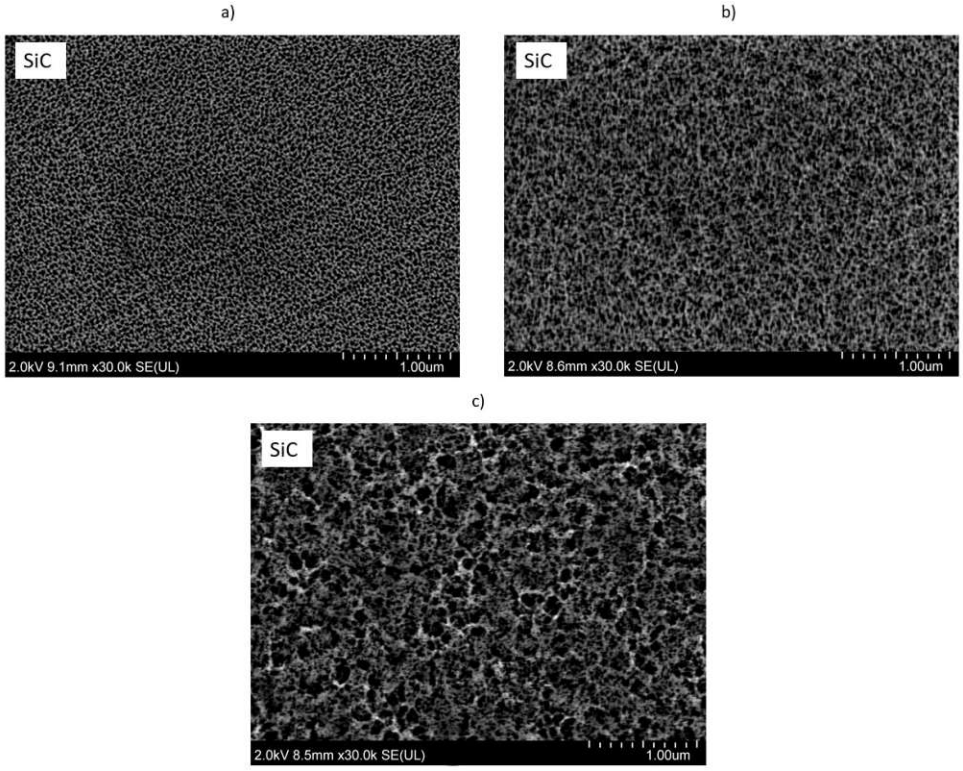


Fig. 5.2: SEM images in top view to demonstrate the degrees of porosification of the 4H-SiC after different MAPCE times. a) shows the porosity after 15 min, b) after 30 min and c) after 45 min of etching.

As described in chapter 4.2, the porosification depth and the amount of porosification is dependent on the etching time. In Fig. 5.1, scanning electron microscopy (SEM) images show that the longer etching times result in deeper porosification depth and a higher degree of porosification, as in Fig. 5.2. The visual lines in Fig. 5.2 a), which are scratches, stem from wafer polishing.

By using a series of SiC samples with various etching times and subsequently diverse porosification depths, electroplating investigations were conducted to find a appropriate sealant and evaluate the minimum required etching depth so that the Ni layer adheres to the SiC surface in a consistent manner. In the following tables, Tab. 5.1 and Tab. 5.2, the results of these experiments are presented. Out of the three sealants, only sealant #3 was able to hold the Watt's bath liquid from entering the substrate holder. Fig. 5.3 show the unsuccessful Ni electroplating attempt with the 15 min MAPCE sample.

Tab. 5.1: Sealant testing results

Sealant #	Material	Complete seal from plating liquid
1	Viton ®FKM	No
2	EPDM E9566	No
3	Foam Rubber EPDM	Yes

Tab. 5.2: Ni plating investigations to assess the required porous layer. A "Y" represents a consistent adhesion, a "P" an inconsistent and a "N" shows no adhesion.

Etching time in [min]	Ni Plating current of 0,07 A	Ni Plating current of 0,14 A
15	N	P
30	Y	Y
45	Y	Y

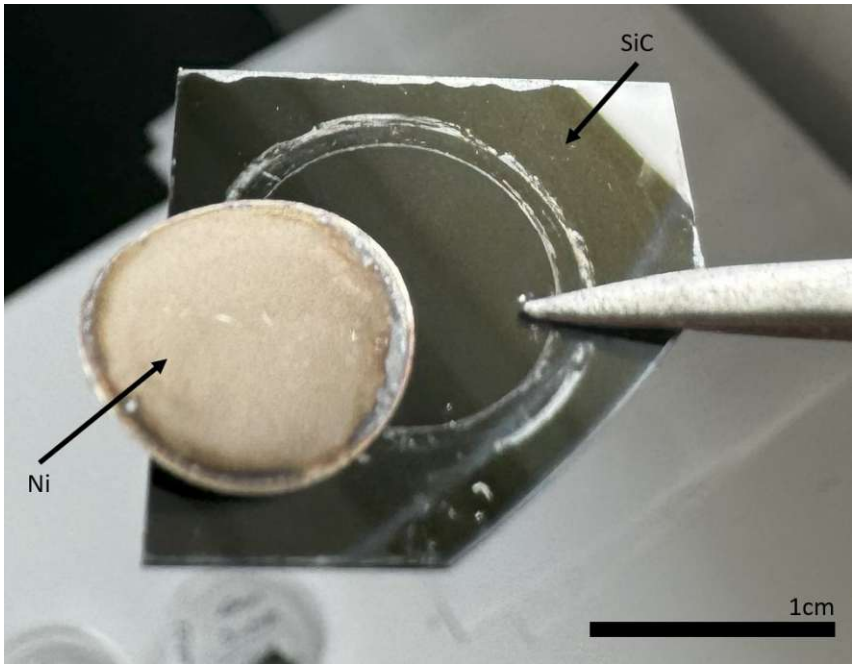


Fig. 5.3: Stressor layer not adhering on the 15 Min MAPCE sample.

If the level and depth of porosification is appropriate, then the electroplating attempts yield successful results as the Ni penetrates the pores and adheres to the SiC substrate. An illustration on how this Ni stressor layer adheres to the substrate can be seen in Fig. 5.4 [71].

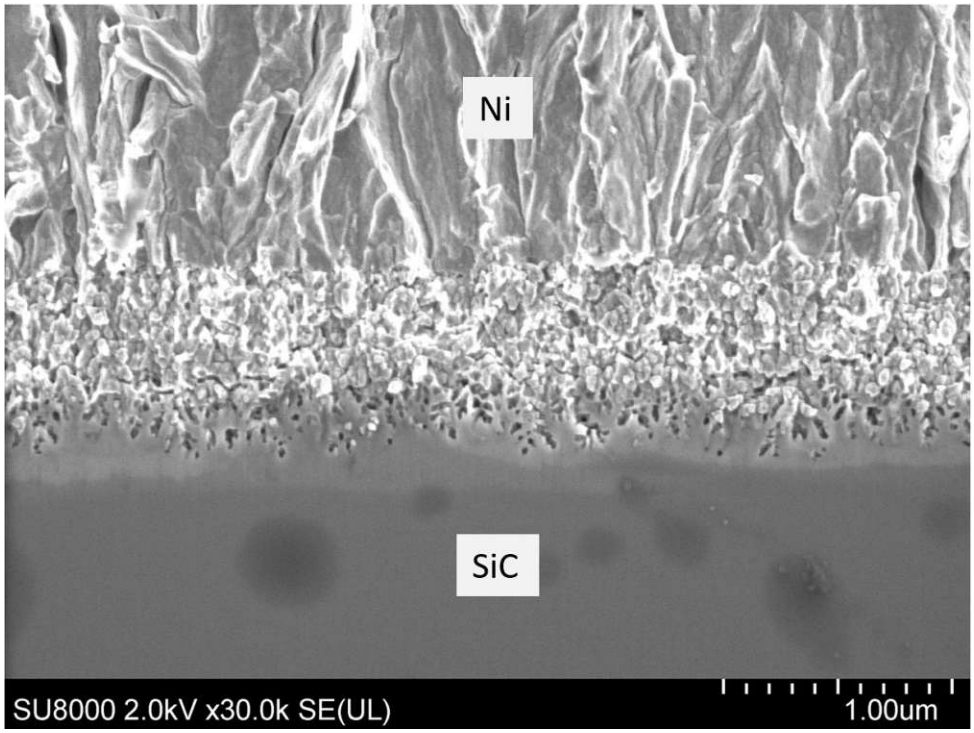


Fig. 5.4: Cross-sectional SEM analysis of the Ni-porosified SiC interface [71].

A typical current/voltage plating diagram is shown in Fig. 5.5, where the current is set to 0,10 A in this diagram.

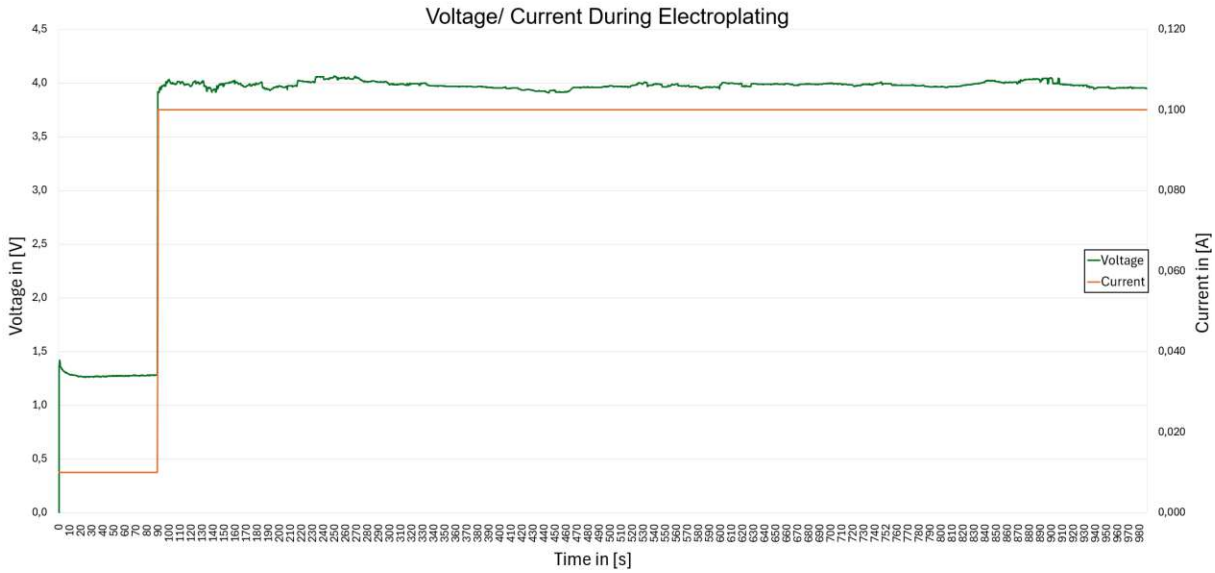


Fig. 5.5: Voltage/ current relation during electroplating process. The current was set at 0,01 A for 90 s and then increased to 0,10 A for 900 s.

The deposition amount is defined through Eqn. 3.5, so to ensure proper filling up of the pores, the current was set to 0,01 A for 90 s. After that, a specific current was set for an additional 900 s, depending on the stressor layer thickness desired.

Following the discovery of a minimum etching time of 30 min, the next experiments were conducted to achieve spontaneous spalling - a state where the energy released through the stress of the Ni stressor layer is higher than the substrate's critical energy, as explained in chapter 3.3. Once spontaneous spalling is achieved, the maximum applicable plating current is found. As the stressor layer thickness increases with higher currents according to Eqn. 3.7, which in turn also alters the residual stress of the deposited layer according to Eqn. 3.16, gradually increasing the current would increase the probability of achieving spontaneous spalling. However, spontaneous spalling did not occur. The current was set to 0,28 A with no spontaneous spalling to be detected. Drastically increasing the current to 0,49 A and 0,71 A also did not yield the results expected, but instead caused the stressor layer to have inhomogeneities as depicted in Fig. 5.6.

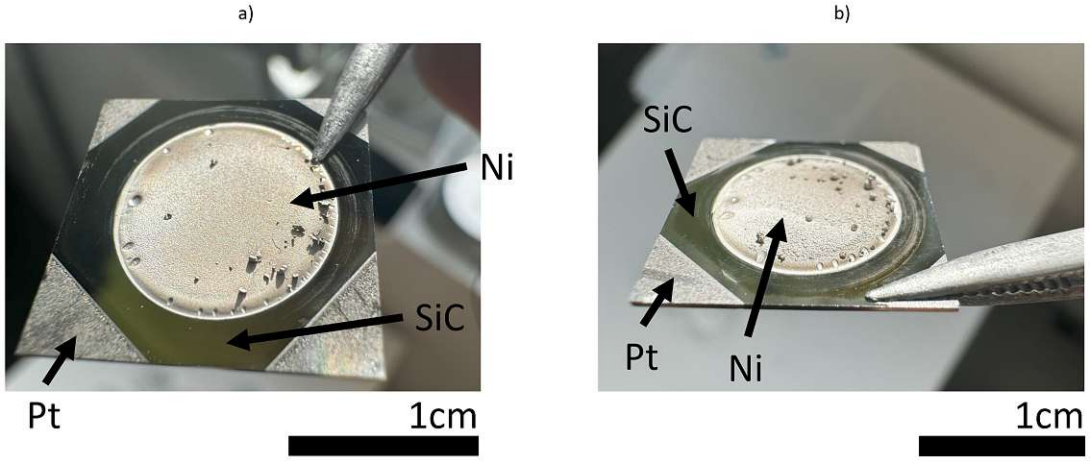


Fig. 5.6: Ni plating experiments with superficial unevenness. a) shows the stressor layer surface after plating with 0,49 A and b) after 0,71 A.

Even though spontaneous spalling was not achieved, further experiments were done with the remaining samples which did not have any surface abnormalities. To check if spalling is viable, the ramp was set to the maximum height of 40 cm, all three handle layer sticky tapes were used and the three cylinders mentioned in chapter 4.4 were deployed. The results of these pre-investigations are presented in Tab. 5.3.

Tab. 5.3: Experimental parameters for controlled spalling.

Experiment #	Cylinder #	Tape	Plating current in [A]	Ramp height in [cm]	Successful spalling
1	1	3M 904	0,28	40	No
2	2	3M 904	0,28	40	No
3	3	3M 904	0,24	40	No
4	1	3M 98010LVC	0,24	40	No
5	2	3M 98010LVC	0,20	40	No
6	3	3M 98010LVC	0,20	40	No
7	1	3M 9087	0,18	40	No
8	2	3M 9087	0,18	40	Inconsistent
9	3	3M 9087	0,16	40	No

In the next evaluation, other solutions were sought after as the experiments did not yield the results expected.

5.1.2 Second Series of Controlled Spalling Investigations

The first solution was to introduce a fracture initiation region for controlled spalling. A few tests were done with this technique via a high power laser to aid in the spalling process, as depicted in Fig. 5.7.

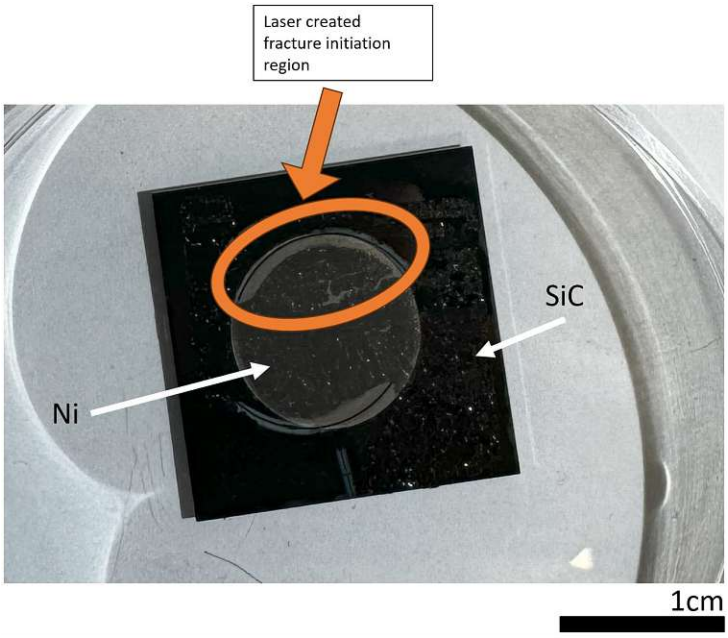


Fig. 5.7: Fracture initiation region around the stressor layer to ease the spalling procedure.

Investigation efforts were put into finding another solution. To get a better understanding of the surface topography and, therefore, how the Watt's bath plated the surface of the SiC substrate, a stylus profilometer was utilised from *BRUKER Corp. DekTakXT* (Billerica, Massachusetts, U.S.). A measurement of a sample with 0,14 A can be seen in Fig. 5.8.

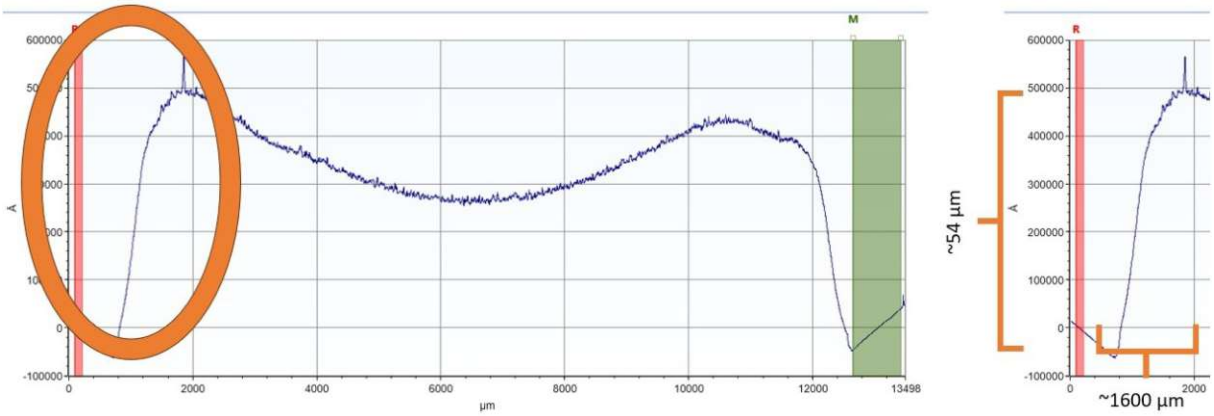


Fig. 5.8: Stylus profilometer measurement of the SiC substrate/ Ni stressor layer without any surface modifications prior to plating.

To define the sharp edges of the stressor layer, thus increasing the stress concentration, a pre-processing step is implemented defining a circular area with a custom built photomask utilising standard photolithography as seen in Fig. 5.9.

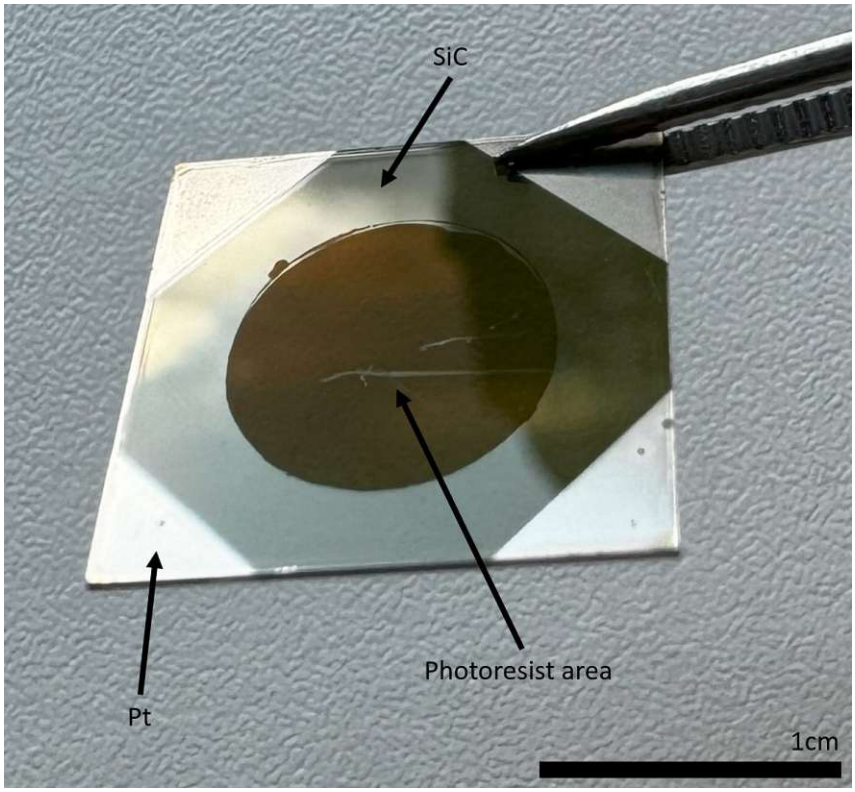


Fig. 5.9: SiC substrate after definition of a circular area with a custom built photomask utilising standard photolithography.

Due to this additional step, it is important to place the substrate appropriately in the plating substrate holder. The exposed area of the holder has to be correctly aligned with the photoresist area.

After the electroplating process with 0,08 A, a profilometer measurement was done to check on the improvements, as in Fig. 5.10.

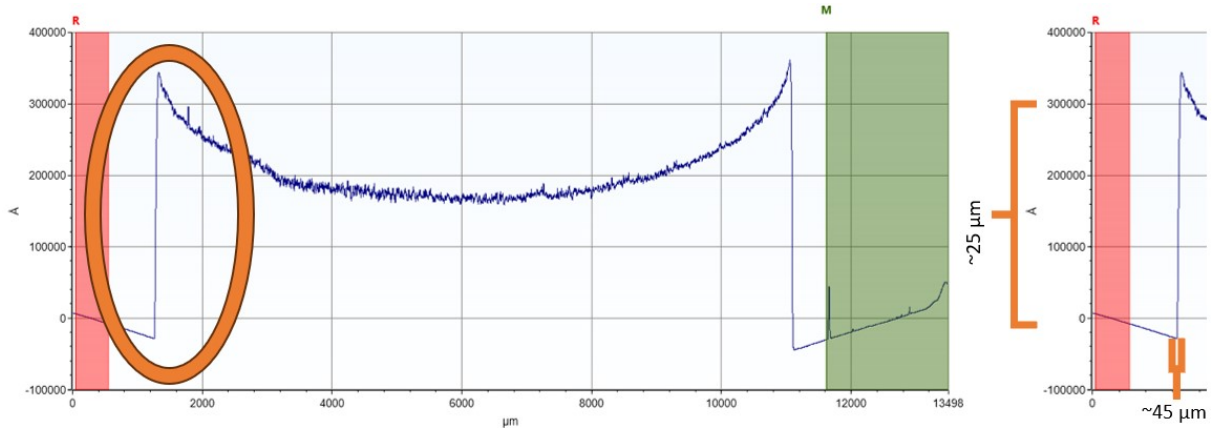


Fig. 5.10: Stylus profilometer measurement of the SiC substrate/ Ni stressor layer after surface modifications prior to plating.

To verify if the stress concentrations have increased at the edge between stressor layer and substrate, a new series of electroplating samples were created starting with 0,02 A - 0,16 A in 0,02 A increments to achieve spontaneous spalling. Tab 5.4 presents the results from this plating series.

Tab. 5.4: A series of electroplating samples showing the threshold current for spontaneous spalling.

Ni Plating current in [A]	Spontaneous spalling
0,02	No
0,04	No
0,06	No
0,08	No
0,10	Party
0,12	Partly
0,14	Yes
0,16	Yes

With Tab. 5.4, the threshold value can be determined for electroplating before the residual stress is high enough for the stressor layer to delaminate itself. For the next experimentations, the maximum current for the Watt's bath is kept at 0,08 A.

After creating a batch of samples ranging between 0,02 A - 0,08 A, each of the sample's stressor layer thickness is measured with the stylus profilometer and compared to the theoretical value evaluated through Eqn. 3.7 with a cathode efficiency of $0,955$, which are displayed in Tab. 5.5 and Fig. 5.11 [85].

Tab. 5.5: Stressor layer thickness for each plating sample.

Ni plating current in [A]	Theoretical stressor layer thickness in [µm]	Measured stressor layer thickness in [µm]
0,02	7,47	7,32
0,04	14,95	12,29
0,06	22,42	18,30
0,08	29,90	24,66

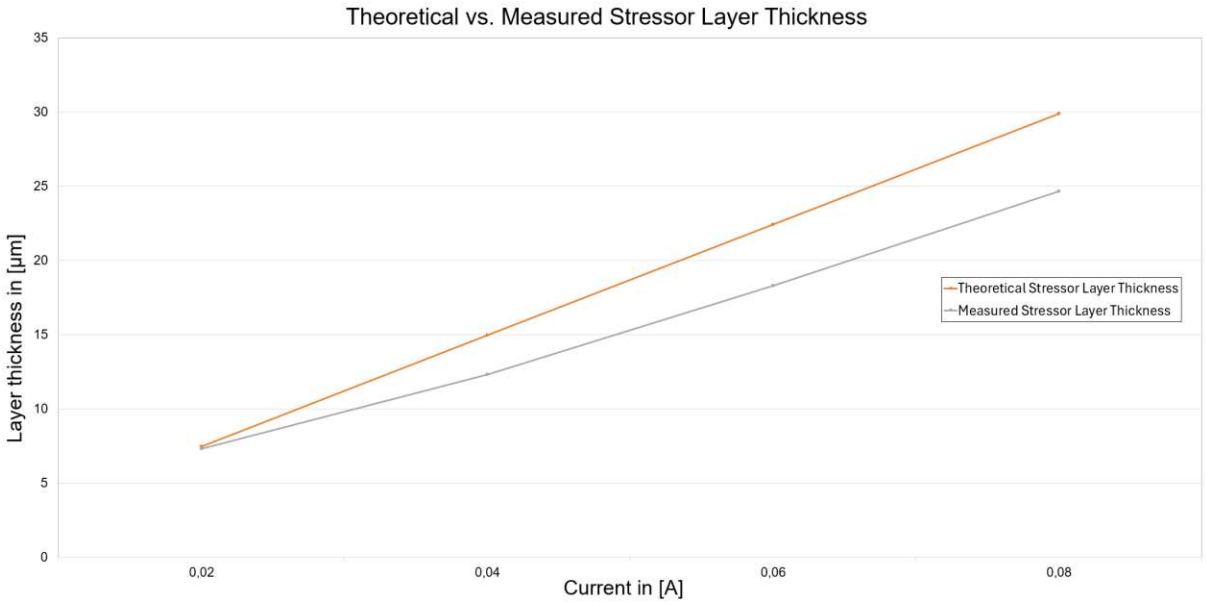


Fig. 5.11: A graphical comparison between theoretical and measured stressor layer thickness.

Before conducting the spalling experiments, the theoretical residual stress is evaluated by deriving the curvature through Eqn. 3.17 and utilising Stoney's formula which is defined by Eqn. 3.16. The curvature values are different for each sample as the current used during plating influences the stressor layer's bending, thus, gives different stress values. Tab. 5.6 showcases the calculated residual stress values.

Tab. 5.6: Residual stress values evaluated through a modified version of Stoney's formula.

Ni Plating current in [A]	Residual stress in [MPa]
0,02	27,69
0,04	154,44
0,06	119,25
0,08	163,43

Finally, a series of samples are produced to test out controlled spalling. With prior experience of spontaneous spalling occurring without any additional processing steps, no fracture initiation region is defined as the assumption is made, that the residual stress is high enough to overcome the fracture toughness of the substrate as soon as an external force is being applied. As with Tab. 5.3, three cylinders and three sticky tapes are used again for this trial. The results are listed in Tab. 5.7.

Tab. 5.7: Experimental parameters for controlled spalling with improved plating procedure.

Experiment #	Cylinder #	Tape	Plating current in [A]	Ramp height in [cm]	Successful spalling
10	1	3M 904	0,08	40	No
11	2	3M 904	0,08	40	No
12	3	3M 904	0,08	40	No
13	1	3M 98010LVC	0,08	40	No
14	2	3M 98010LVC	0,08	40	Yes
15	3	3M 98010LVC	0,08	40	Yes
16	1	3M 9087	0,08	40	No
17	2	3M 9087	0,08	40	Yes
18	3	3M 9087	0,08	40	Yes

Further experiments are conducted only with the other two remaining stick tapes and cylinders which were capable of achieving controlled spalling as in Tab. 5.8.

Tab. 5.8: Final controlled spalling experiments with optimised parameters.

Experiment #	Cylinder #	Tape	Plating current in [A]	Ramp height in [cm]	Successful spalling
19	2	3M 98010LVC	0,06	40	Yes
20	2	3M 98010LVC	0,04	40	No
21	2	3M 98010LVC	0,02	40	No
22	2	3M 9087	0,06	40	Yes
23	2	3M 9087	0,04	40	No
24	2	3M 9087	0,02	40	No
25	3	3M 98010LVC	0,06	40	Yes
26	3	3M 98010LVC	0,04	40	No
27	3	3M 98010LVC	0,02	40	No
28	3	3M 9087	0,06	40	Yes
29	3	3M 9087	0,04	40	No
30	3	3M 9087	0,02	40	No

In Fig. 5.12 a), a SiC substrate with its Ni stressor layer is illustrated, and in b), as well as in c), both sides of the spalled stressor layer with a thin layer of SiC can clearly be seen [71].

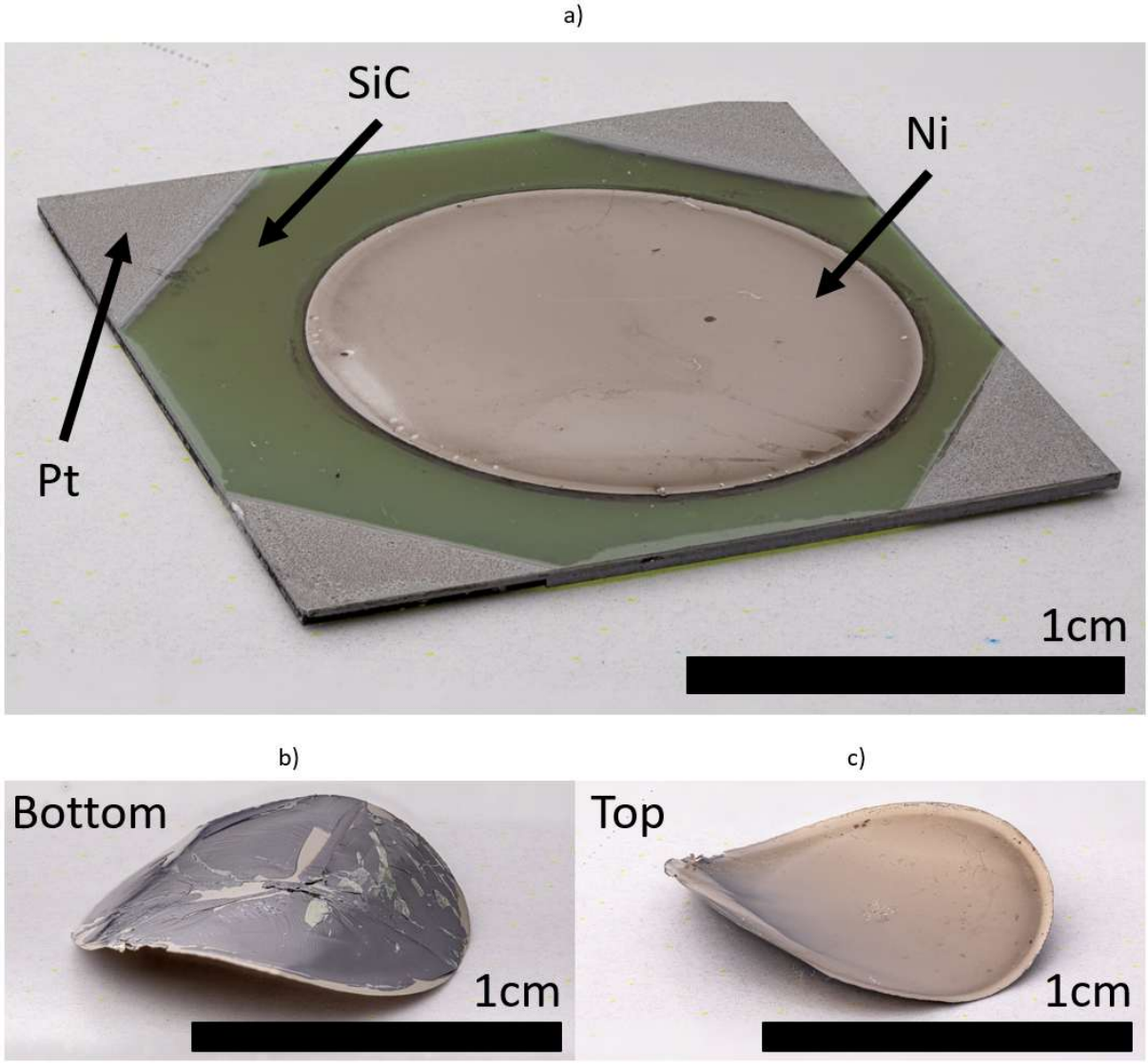


Fig. 5.12: a) displays a SiC substrate with a Ni stressor layer, ready for controlled spalling. b) and c) show the spalled Ni stressor layer accompanied with a thin layer of SiC which has been cleaved off from the spalling procedure [71].

To check upon the spalling depth and to compare with the theoretical assumptions, the stylus profilometer was used to measure the substrate which in turn gives insights about the crack propagation and the maximum spalling depth. The results are displayed in Tab. 5.9.

Tab. 5.9: Comparison between theoretical and measured spall depth.

Plating current in [A]	Theoretical spall depth in [µm]	Average measured spall depth in [µm]
0,08	18,91	24,91
0,06	15,12	23,85
0,04	-	-
0,02	-	-

To obtain the pure SiC layer from the spalled sheet, the Ni stressor layer was dissolved with *aqua regia*, a mixture of nitric acid and hydrochloric acid. This spalled SiC layer is then analysed with a *Fourier Transform Infrared Spectroscopy* (FTIR) to check upon the quality. The FTIR analysis, where reflectivity is plotted against the wavenumber, is displayed in Fig. 5.13.

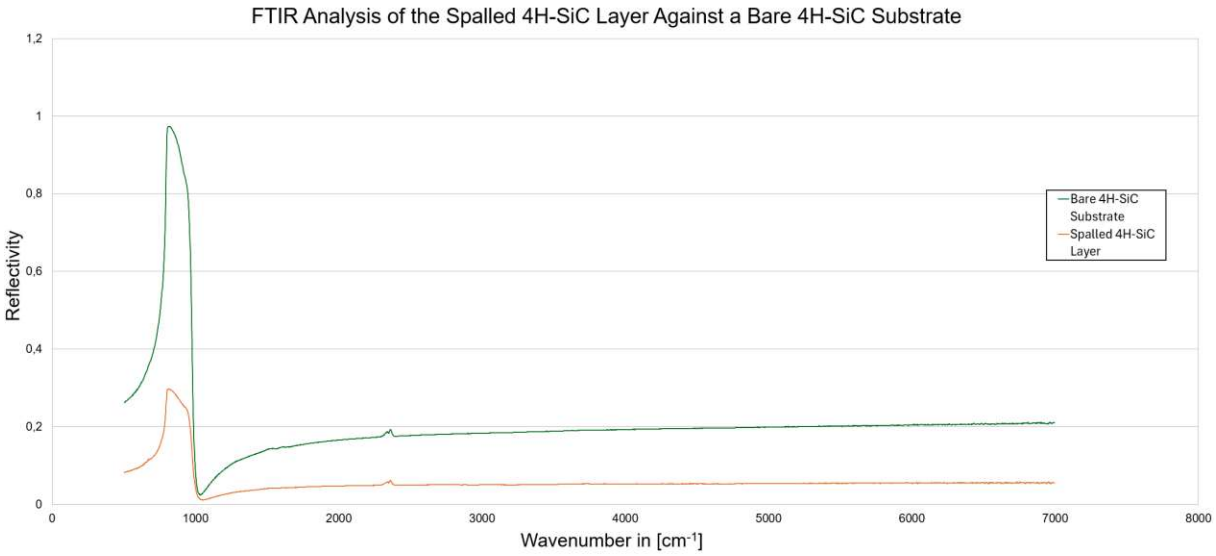


Fig. 5.13: FTIR analysis of the successfully spalled 4H-SiC layer in comparison to a bare 4H-SiC substrate.

5.2 Discussion

5.2.1 First Pre-Investigations for Controlled Spalling

According to the observations in Tab. 5.2, the 15 min sample proved to be not suitable as the Ni layer did not adhere at all at the lower plating current, or adhered sporadically at the higher plating current with the Ni layer just falling off as in Fig. 5.3. Starting with the 30 min samples, each plating attempt led to the Ni layer to hook into the porous structure and therefore proves to be the minimum etching time, thus, the minimum depth of porosity required. This feat has not been achieved so far in SiC research as these layers would usually not adhere to the SiC substrate and therefore paves the way to achieve controlled spalling via residual stress through a stressor layer which is electroplated.

Out of the three sealants from Tab. 5.1, only sealant #3 was able to hold off the Watt's bath solution from entering the wafer holder. The other two sealants were much more rigid than the third one, thus, not creating a tight fit between the two parts of the wafer holder which caused a minor leakage.

As described in chapter 3.3, the stress built up on the Ni stressor layer is a combination of intrinsic and thermal stress. The thermal stress in its own cannot generate enough energy to achieve the requirements of controlled spalling without intentionally applying a high temperature [99]. As the Watt's bath is set to around 60 °C and the substrate is pulled out of the bath where room temperature is prevalent, the thermal stress σ_T is ruled out of Eqn. 3.14 and therefore the Ni stressor layer stress σ_f is equal to the intrinsic stress σ_I.

In the first electroplating pre-investigations, no matter the amount of current applied, all samples did not behave the way anticipated. Spontaneous spalling did not occur, but instead, the higher the current was set, the more inhomogeneous Ni layers were deposited as illustrated

in Fig. 5.6. At first, the current was increased in a controlled manner of 0,02 A increments. But to achieve spontaneous spalling, the current was drastically increased. This was done to find a value where the stressor layer would peel off itself due to high stress concentrations. If everything went according to plan, the current would be gradually decreased in order to find a threshold value where the stressor layer would not detach itself automatically. But unfortunately, the stressor layer never reached the state of spontaneous spalling, but instead the Ni surface started to become less smooth with tiny hills on it as depicted in Fig. 5.6. These inhomogeneous layers arised at and above current of 0,49 A which made them unusable for controlled spalling as attaching the handle layer requires the stressor layer to have a smooth surface so that the adhesion is effective. As it seems, the over-limiting current at and above 0,49 A was reached making the electroplating process uncontrollable. The assumption is made, that high current densities lead to the formation of porous micro branches of Ni oxides which are created through the fast formation and detachment of hydrogen bubbles. Furthermore, a critical over-potential of the electrodes which results from the absorption of Ni not bonded in complexes, but instead, crystals grow in the presence of the porous Ni hydroxide layer leading to the limited transport of cations [100] [101]. Commonly, a dendritic formation takes place with these conditions mentioned [100].

Even though spontaneous spalling did not occur, the assumption is made that applying an external force should suffice to trigger the crack propagation, hence, to achieve controlled spalling. For the initial spalling experimentations, the remaining samples with a smooth surface were used.

The first attempts of Tab. 5.3 did not show the expected results, as neither of the experiments showed consistent controlled spalling outcomes. The first three spalling attempts used the weakest stick tape in combination with all three cylinders. Further tests employed the next stronger sticky tape, whereas all three cylinder types were used again. Even the strongest handle layer sticky tape did no peel off a SiC layer. In one occasion, experiment # 8 was an exception as the first attempt resulted in a spalled layer, but further attempts with the same parameters did not work accordingly, thus, making it irreproducible. Further spalling efforts only led to pulling off the Ni layer without any SiC layer. With no spontaneous spalling occurring, regardless of stressor layer thickness and, inconsistent controlled spalling attempts, improvements had to be found to achieve the goal of detaching a thin SiC layer with an stressor layer.

To improve the process, different parameters can be considered. Starting with the MAPCE etching bath composition, up to the Watt's electroplating bath chemistry, many of the variables can be tweaked. Before any of the parameters are changed, the help of literature was consulted.

5.2.2 Second Series of Controlled Spalling Investigations

Looking at literature and publications of other researchers conducting controlled spalling on materials like Ge or GaN, prior to pulling off the handle layer, a well-defined fracture initiation region is introduced for controlled spalling to take place [70] [88]. Applying this knowledge to the SiC substrate process, a high-power laser was used to define the fracture initiation region as shown in Fig. 5.7. Unfortunately, this step did not improve the condition and ease the spalling procedure despite occasional and uncontrollable spalling was achieved.

It was recognised that the stressor layer did not abruptly terminate at the interface to the substrate, as controlled spalling with Ge substrates was successfully achieved where this feature was present [70] [88]. The next step lies in analysing the surface topography.

The measurement in Fig. 5.8 clearly shows the slope of the deposited Ni layer. The layer increases to 54 µm, on a length scale of 1600 µm. Setting both values into relation, the Ni layer gradually rises to its maximum height which goes against the goal on how to build-up the stress concentration field at this location. Usually, designing machine elements is accompanied by

avoiding sudden changes or discontinuities to the geometry to prevent stress concentrations, so gradual changes to the geometry are implemented to prevent specific places to have maximum stress, thus, reducing the likelihood of the material to fail when it is in operation [102]. An example of such design rules can be seen in Fig. 5.14.

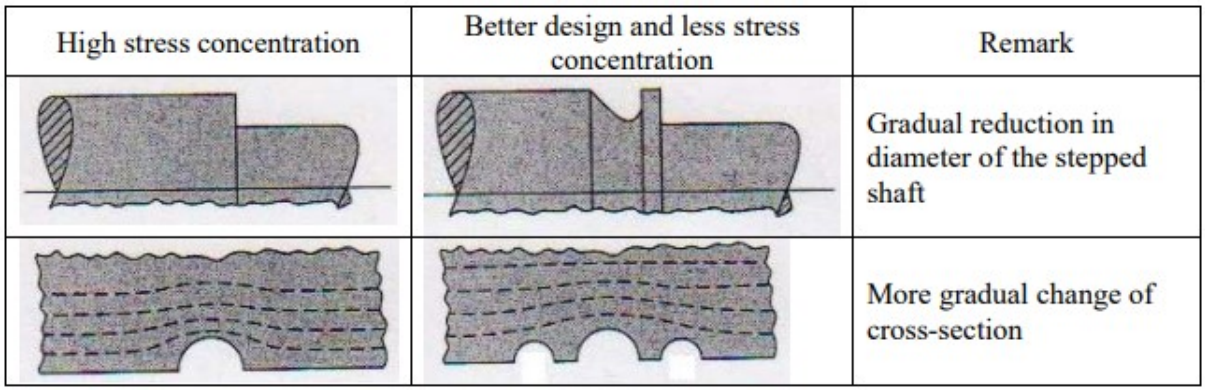


Fig. 5.14: Schematics on how stress concentrations are built and design suggestions to prevent them [103].

In the case of controlled spalling, building up the stress concentration through the sudden change in geometry and the corresponding "failure" is favoured to detach the stressor layer. The emphasis has been set onto finding a possibility to improve the slope by making it steeper, thus, increasing the stress concentration at the edge.

Patterning and etching or material deposition is a common procedure in the electronic industry to create complex structures like micro electro mechanical systems via the use of photolithography. This technique can also be used to form electro deposited structures through molds [104] [105]. After processing the surface of the SiC substrate to create a porous structure with the MAPCE procedure, an additional step is applied by using standard photolithography with a custom photomask to create a cylindrical mold in the middle of the substrate surface, as seen in Fig. 5.9. For the Ni electro deposition process, none of the Watt's bath composition was changed. An additional drawback to the addition of the photolithography step is the loss of freedom in placing the SiC substrate into the substrate holder. As the exposed area of the substrate holder has a diameter of 11 mm, the photoresist mold is made smaller with a diameter of 10 mm to ensure a headroom in substrate placement. After plating the newly modified SiC substrate with a current of 0,08 A, a stylus profilometer measurement is done to check on the development. The profilometer diagramm is depicted in Fig. 5.10 and weighed up against the measurement in Fig. 5.8 which represents the stressor layer without the photolithography pre-processing step.

This new measurement shows a run of approximately 45 µm which constitutes to a 97,12 % decrease in comparison to the measurement of the stressor layer without the photolithography step, which is a significant improvement in the steepness of the slope.

After applying this pre-processing step, the next batch of samples are created with a current range between 0,02 A - 0,16 A as shown in Tab.5.4, where spontaneous spalling already occur partly at currents over 0,10 A and a complete detachment of the stressor due to residual stress takes place at currents above 0,14 A. It can be concluded that the energy released through residual stress of the electroplated Ni layer surpasses the substrate's critical energy at a current at and above 0,10 A, as described previously in Eqn. 3.8. For the final controlled spalling analysis, sample plating current will range from 0,02 A to 0,08 A.

With the help of the profilometer, the stressor layer thickness is compared to the calculated results as illustrated in Fig. 5.11 and show a approximate similarity where the difference is smaller at lower current values than the higher ones.

Stoney's formula gives an estimation of the residual stress values, as displayed in Tab. 5.6. As the current increases, the bending of the Ni stressor layer increases too, thus, giving a higher curvature value. The 0,06 A sample is identified as an outlier as the bending measurement did not yield the typical "bath tub" form, the other samples displayed like in Fig. 5.8 or Fig. 5.10. Instead, most of the bending happens at side of the stressor layer which skewed the curvature calculation. The residual stress value of the 0,06 A sample is assumed to be between the 0,04 A and 0,08 A samples. Papers which report about controlled spalling for other semiconductors mention residual stress values ranging between 200 MPa - 800 MPa which coincide with the values in Tab. 5.6 as this thesis aims to find the minimum value necessary [89] [88].

To understand the way controlled spalling works, selected reports of other researchers were analysed where other substrate materials were used. But unfortunately, no information is provided regarding the attributes of the handle layer. So this thesis gives some insights and experimental data on three handle layers.

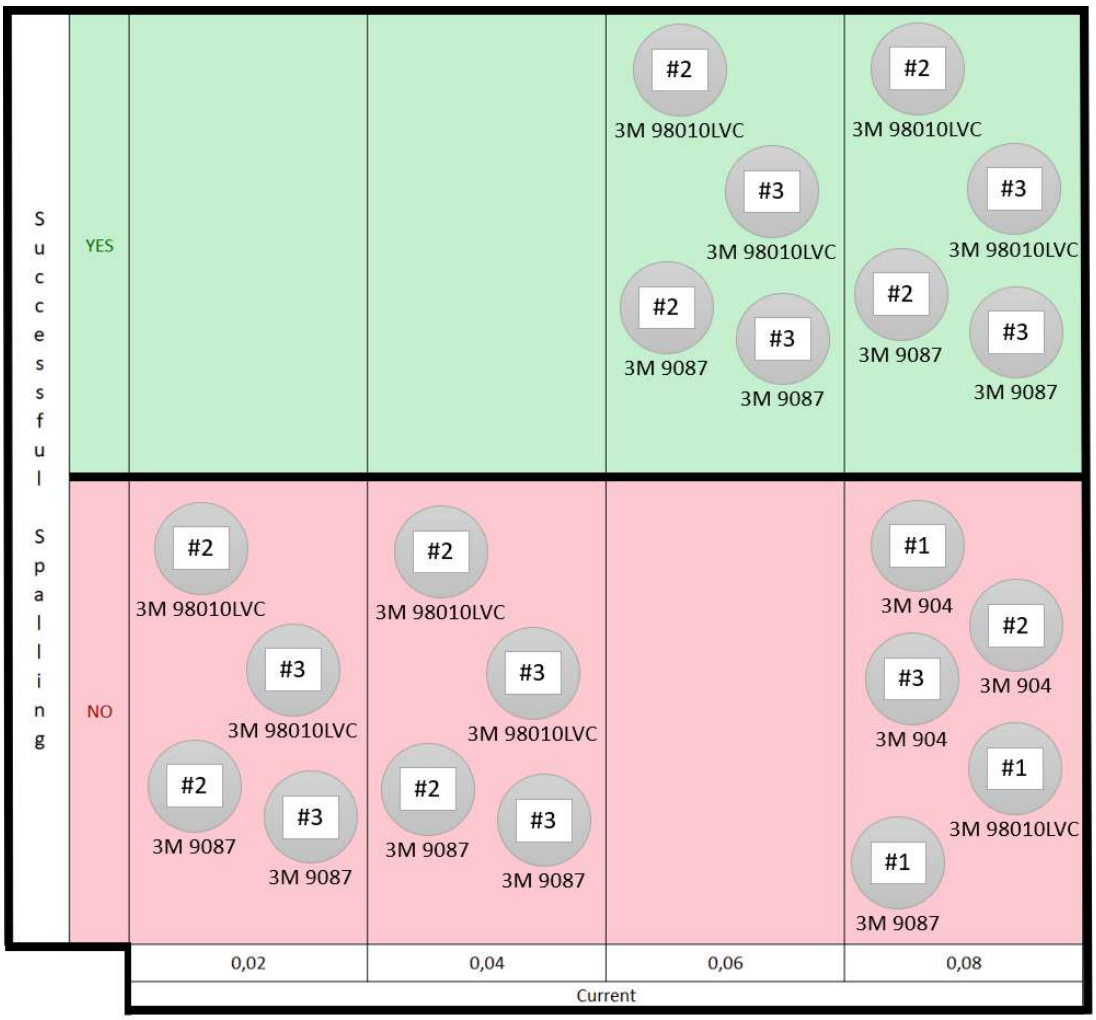
The results of the next controlled spalling experiments of Tab. 5.7 show a clearly distinguishable pattern. Analysing these results, neither the weakest sticky tape model *3M 904*, nor the lightest cylinder # 1 were able to encourage controlled spalling. The pairing also did not matter as combining the lightest cylinder with the strongest stick tape or the heaviest cylinder with the weakest handle layer did not improve the situation. At times the strongest sticky tape just halted the lightest cylinder from rolling. The worse sticky tape peeled off without detaching the Ni stressor layer. The experimentation proceeded with the remaining cylinders and sticky tapes.

Finally, the controlled spalling experiments were repeated with cylinder 2 and 3, as well as with the handle layers *3M 98010LVC* and *3M 9087*.

It can be noted that if cylinder 2 and handle layer *3M 98010LVC* achieve controlled spalling, then it can be assumed that the external energy is high enough to generate an energy release greater than the substrate's critical energy, as per Eq. 3.8. This in turn also means that the stronger sticky tape in combination either with cylinder 2 or 3 would also lead to a spalled layer. The same can be said for the behaviour of the cylinders. Controlled spalling with cylinder 2 would result in the same result with the heavier cylinder 3, as it applies even more force, thus, generating an energy release higher than the substrate's critical energy.

In conclusion, the results in Tab. 5.8 are filled out in the way described in the previous paragraph. If controlled spalling is achieved with e.g. cylinder 2 and handle layer *3M 98010LVC*, then this automatically means, that spalling can also be achieved with e.g. the heavier cylinder 3 and the same handle layer *3M 98010LVC*, etc.

With the final spalling results, the pre-processing step of using standard photolithography with a custom photomask to create a cylindrical trench proves to be the correct modification to increase the stress intensity at the edges. With this feat, the probability for controlled spalling increases drastically as displayed in Tab. 5.8 where both cylinders paired with one of the two handle layers were able to peel off the stressor layer accompanied by a thin layer of SiC. A graphical representation of Tab. 5.8 for a better overview is displayed in Fig. 5.15.



Tape model	Peeling Strength in [N/mm]
3M 904	0,50
3M 98010LVC	1,16
3M 9087	1,55

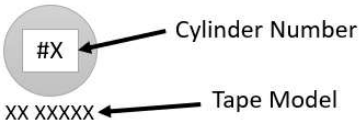


Fig. 5.15: A graphical overview of the final spalling results.

It can be shown with the final controlled spalling attempts that samples with the plating current of 0,02 A and 0,04 A do not possess the stress attributes necessary to achieve spalling via an external force. For the given setup and process steps, the ideal range sits between 0,06 A - 0,08 A, as the stress concentrations are low enough for the sample to not transit into the state of spontaneous spalling, but high enough to achieve controlled spalling with an external stimuli.

The difference in theoretical and measured spalling depth is explained through the way on how spalling is being achieved. Most probably, the peel off force being applied is not linear, thus, the crack propagation is not homogeneous. Furthermore, this measured value is the average of all the hills and valleys, hence, deep crack propagations alters the calculated value.

A FTIR analysis gives insights about the quality of the material and if other material substances are present. Standard FTIRs on the market can detect concentrations of components approximately greater than 3 % - 5 % of the total [106] [107]. So anything beneath that value

will go undetected. After dissolving the Ni stressor layer from the spalled SiC layer, FTIR was used to see if residues of Ni are still present in the sample by checking on the peaks of reflectivity across different spatial frequencies. These peaks are in the reststrahlen band. The reststrahlen band of a material is a reflective spectrum due to the restrahlen effect [108]. This effect is defined through the change in refractive index of a medium in which electromagnetic radiation cannot propagate. More than one peak indicates that the material is not pure. With observing the course of the plot in Fig. 5.13, the peak of the spalled SiC layer coincides with the peak of a SiC substrate. Researchers state, the reststrahlen band of SiC is found between $600\,\mathrm{cm}^{-1}$ - $1200\,\mathrm{cm}^{-1}$, which proves upon the quality of the spalled SiC layer even more as the peak is found in that range [108]. As there are no other peaks in the plot, the quest of obtaining a pure SiC layer is been achieved successfully, thus, traces of Ni can not be ruled out due to the detection limits of the FTIR.

Chapter 6

Conclusion

6.1 Summary

A novel technique for creating a thin layers of SiC through Ni electroplating is being presented dubbed *Controlled Spalling*. Other thin layer technologies like *SmartSIC*™ or *SILTECTRA*™ *COLD SPLIT* also create thin layers from SiC substrates for the industry, but the manufacturing is coupled with expensive equipments and complicated process steps, thus making the end product expensive. Controlled spalling on the contrary uses standard laboratory equipment and the processing steps are executed at room temperature which ensures cost effectivity.

The aim of this thesis was to design and perform experiments on important parameters in order to find a way in overcoming the substrate's critical energy to peel off a thin SiC layer. Attaching a stressor layer onto the SiC substrate proves to be a challenge, as simply electroplating the said layer onto the substrate's surface results in insufficient adhesion of the stressor layer. With the help of MAPCE, a porous structure is created surface-near. Depending on the etching time, the level and depth of porosity can be tailored to increase adhesion of the stressor layer to the substrate. After finding the appropriate etching parameters, the threshold current value for electroplating was experimentally evaluated. This value is defined as the current which causes the plated layer to delaminate due to the energy generated through the residual stress being higher than the substrate's critical energy. First experiments did not yield the expected results as spontaneous spalling never occurred. It was assumed that applying an external force should still suffice in enforcing controlled spalling, but controlled spalling was not achieved. According to literature, a pre-conditioning of the substrate with an additional step before the controlled spalling procedure by defining a fracture region to initiate the spalling procedure. This fracture region was created with a high power laser. Unfortunately, controlled spalling still did not take place. After conducting measurements of the steepness of the deposited stressor layer via a stylus profilometer measurement, it was hypothesised that the stress concentration cannot build up due to the lack of sudden change in geometry. To tackle this problem, a pre-processing step is introduced by spin coating a photoresist with a circular opening. The opening area acts as a cylindrical trench to guide the electroplated layer into the desired form. After electroplating the pre-processed substrate, another stylus profilometer measurement was conducted to check upon the improvements. This profilometer measurement proved the steeper side walls of the deposited stressor layer, thus, increasing the stress concentration at the edge. During the steady current increments for the Ni electroplating step, spontaneous spalling was achieved, which also translates to the threshold current value for the next batch of samples. Attempting the spalling trials for the next series of samples yielded the results expected by using the parameters and laboratory equipment presented. By achieving controlled spalling, the aim of this thesis is therefore also reached. The aim of presenting a viable, cheap and easy to execute solution in creating thin layers from conventional silicon carbide substrates.

6.2 Outlook

Controlled Spalling via an electroplated stressor layer has never been achieved on SiC and this thesis serves as a proof-of-concept. As many of the parameters have been set constant to reduce the amount of experiments due to constraints, a lot of the mentioned parameters can be tweaked for optimisation. Similarly, the controlled spalling process itself should be improved in future by defining a crack initiation region, as well as a continuous force transfer to ensure homogeneous SiC layers from the spalling procedure. If these criteria are met, then *Controlled Spalling* might be defined as a very cost and time effective technique for a layer transfer approach to an alternative substrate which opens up an another route compared to established industry standards currently on the market.

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Abbreviations

CMP Chemical-mechanical polish

CTE Coefficient of Thermal Expansion

CVD Chemical vapour deposition

DWS Diamond wire sawing

FTIR Fourier Transform Infrared Spectroscopy

GaAs Gallium Arsenide

GaN Gallium Nitride

Ge Germanium

H Hydrogen

HF Hydrofluoric acid

MAPCE Metal-assisted photochemical etching

MWSS Multi-wire slurry sawing

Ni Nickel

Pt Platinum

PVD Physical Vapor Deposition

SEM Scanning Electron Microscopy

Si Silicon

SiC Silicon Carbide

SiCOI Silicon carbide on insulator

SOI Silicon on insulator

UV Ultra-violet

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Appendix A

Spall Depth Calculations

Theoretical Spall Depth Calculations

```
<< Utilities`CleanSlate`;
CleanSlate[];
ClearInOut[];
(*Theory by J.W.Hutchinson & Z.Suo –
 Mixed Mode Cracking in Layered Materials(1991)*)
(*Poisson numbers*)
vNi = 0.31;
vSiC = 0.157;

(*Material Modulus, in this case one needs the plane strain elastic modulus*)
                Modulus
ENi = 201 * 10^9 / (1 - vNi^2);
ESiC = 444 * 10^9 / (1 - vSiC^2);

(*Lattice Strain Mismatch Alpha: Takes strain into account between electroplated film
   and the substrate due to differences in lattice size and arrangement*)
α = (ENi - ESiC) / (ENi + ESiC);
h = 40 * 10^-6; (*Stressor layer thickness*)
λ0 = 350 * 10^-6 / h;
(*Substrate Thickness divided by stressor layer thickness according to H/S paper*)
                Dicke
```

```
In[•]:= e = (1 + α) / (1 - α); (*Stiffness ratio between two materials*)
Δ = (λ^2 + 2 * e * λ + e) / (2 * (λ + e));
(*measureing the levels of neutral axis depending on lambda, elastic properties*)
Δ0 = (λ0^2 + 2 * e * λ0 + e) / (2 * (λ0 + e));
(*measureing the levels of neutral axis depending on lambda0, elastic properties*)
A = λ + e;
i = (e * (3 * (Δ - λ)^2 - 3 * (Δ - λ) + 1) + 3 * Δ * λ * (Δ - λ) + λ^3) / 3;
A0 = λ0 + e; (*dimensionless effective cross section*)
i0 = (e * (3 * (Δ0 - λ0)^2 - 3 * (Δ0 - λ0) + 1) + 3 * Δ0 * λ0 * (Δ0 - λ0) + λ0^3) / 3;
(*Moment of inertia of the beam per unit width*)
  Moment
C1 = A / A0; (*Non - dimensional number*)
C2 = A / i0 * ((λ0 - Δ0) - (λ - Δ)); (*Non - dimensional number*)
C3 = i / i0; (*Non - dimensional number*)
p = σ * h * (1 - C1 - C2 * ((1 / 2) + λ0 - Δ0)); (*external load: longitudinal load*)
m = σ * h^2 * (((1 / 2) + λ - Δ) - C3 * ((1 / 2) + λ0 - Δ0)); (*external load: moment*)
U = ((1 / A) + (1 / (λ0 - λ)) + ((12 * (Δ + ((λ0 - λ) / 2))^2) / (λ0 - λ)^3))^-1;
(*dimensionless, positive number, A --> Non dimensional effective cross section*)
V = ((1 / i) + (12 / (λ0 - λ)^3))^-1; (*dimensionless,
positive number, i --> Moment of inertia*)
                                Moment
y = ArcSin[((12 * (Δ + ((λ0 - λ) / 2))) / (λ0 - λ)^3) * Sqrt[U * V]];
    Arkussinus                                          Quadratwurzel
ω = 52 Degree;
      Grad
K1 = (p / (Sqrt[2 * U * h])) * Cos[ω] + (m / (Sqrt[2 * V * h^3])) * Sin[ω + y];
          Quadratwurzel        Kosinus       Quadratwurzel          Sinus
(*stress intensity factors*)
K2 = (p / (Sqrt[2 * U * h])) * Sin[ω] - (m / (Sqrt[2 * V * h^3])) * Cos[ω + y];
          Quadratwurzel        Sinus       Quadratwurzel          Kosinus

l = FindRoot[ArcTan[K2 / K1] == 0, {λ, 0.6}];
    ermittle Nu· Arkustangens
(*Calculating steady state cracking depth with K2 = 0,
whereas the Lambda starting point is selected with the table 5*)
(*Why Arctan? The relative amount of mode II to mode I is specified by the
                                                    imaginäre Einheit I
  mode angle PSI with tan(PSI) = K2/K1. With the proposal of Hutchinson/ Suo,
                                          mit
that at steady state cracking depth, K2 = 0,
the the angle PSI corresponds to 0 too*)
rall = λ /. l
spallDepth = rall * h
```

Appendix B

Intrinsic Stress Calculations

Stoney Formula for stressor layer

```
<< Utilities`CleanSlate`;
CleanSlate[];
ClearInOut[];
Clear["Global`*"];
```
bereinige

```
(*Curvature of substrate, before and after stressor layer*)
κ0 = 0.01444078;
κ = 0.62235;

(*Thickness of stressor layer tf and substrate ts*)
```
Dicke
```
ts = 350 * 10^-6 ;
tf = 40 * 10^-6;

(*Young's  modulus of substrate, SiC*)
Es = 444 * 10^9;

(*Poisson Ratio of substrate, SiC*)
Nys = 0.157;
```
(CleanSlate) Contexts purged: {Global`}

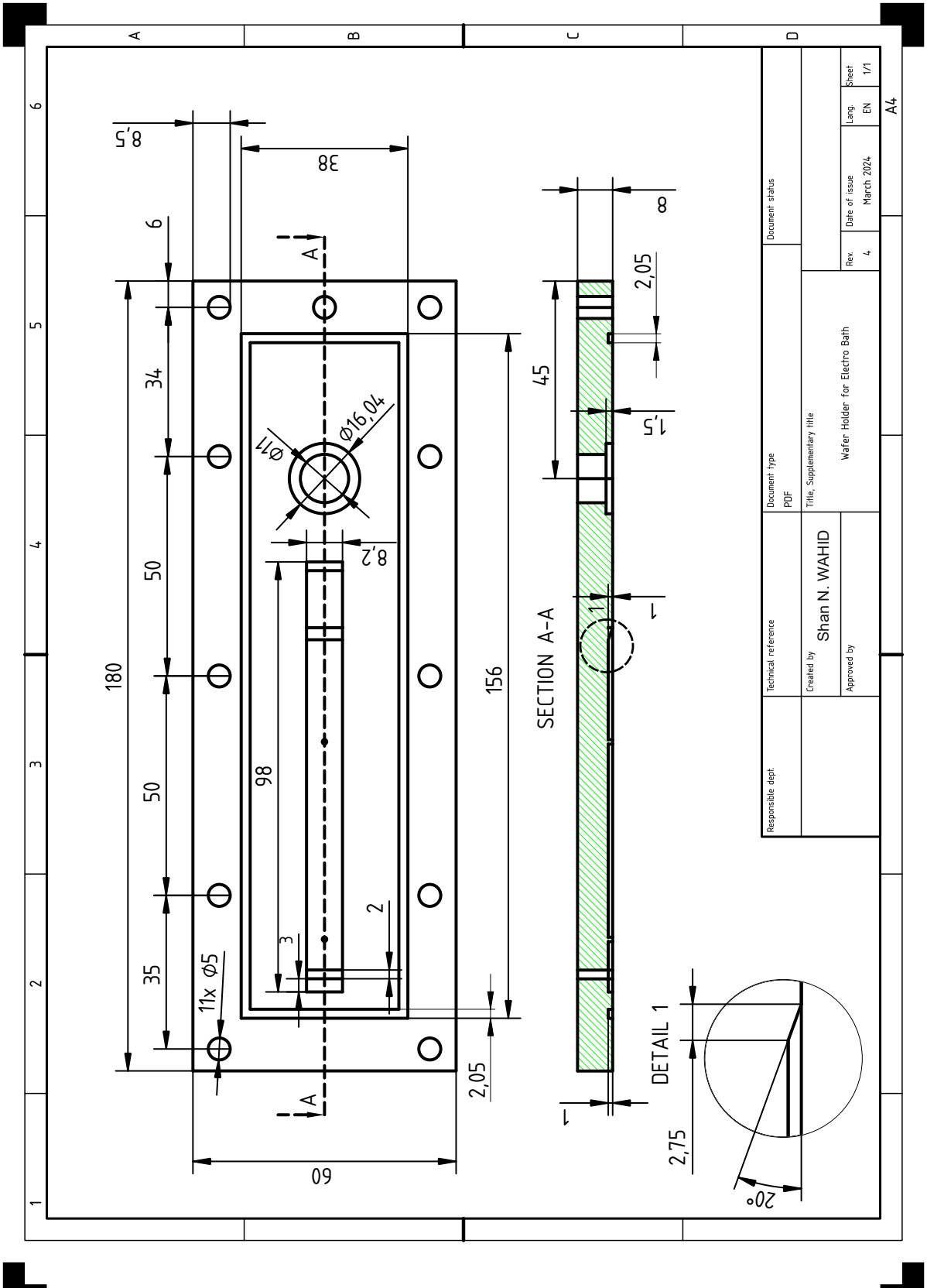
(CleanSlate) Approximate kernel memory recovered: 18 Kb

Modified Stoney formula for thin layer on substrate

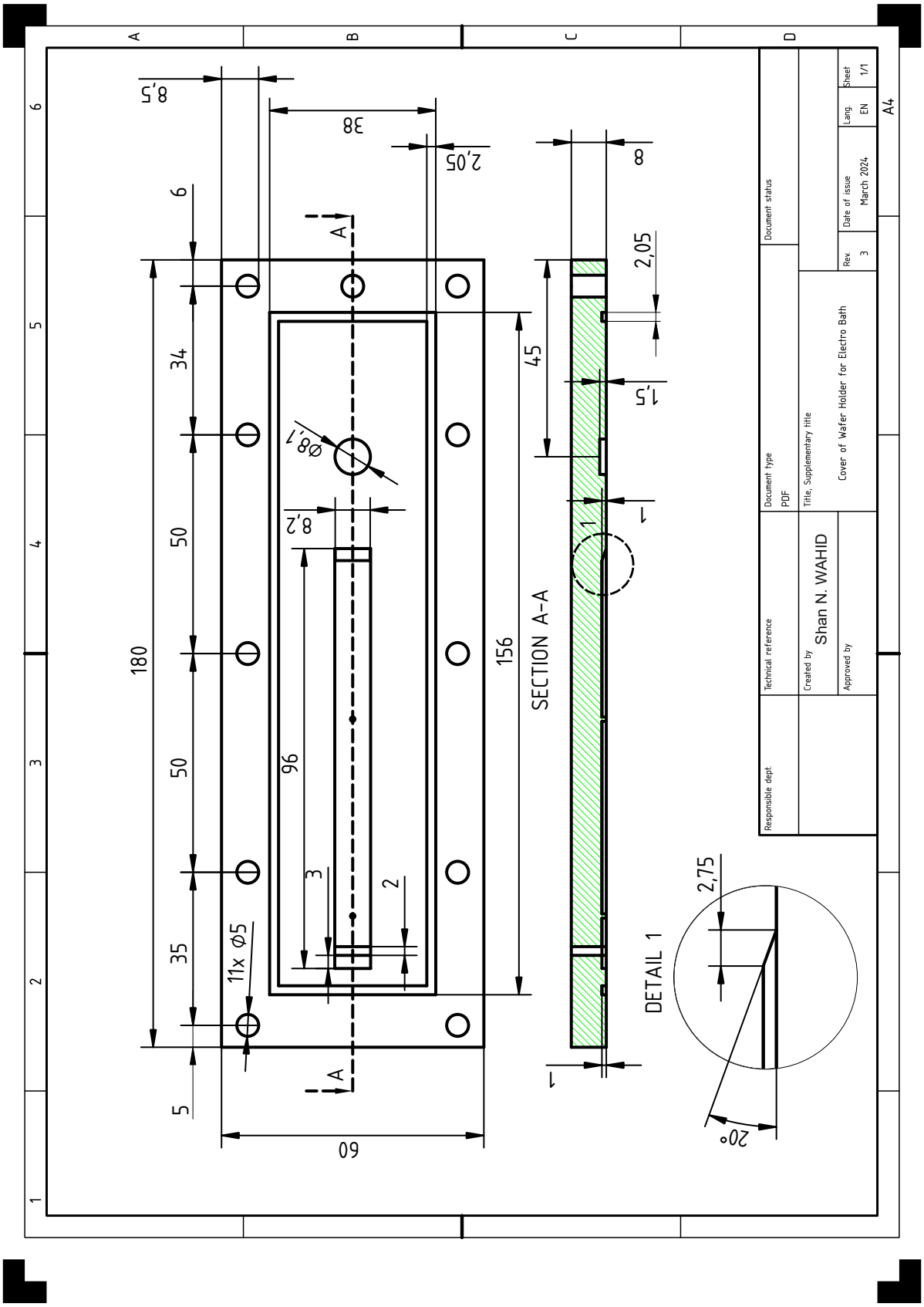
In[•]:=
```
sigmaR = (Es * (ts^2) * (κ - κ0)) / (6 * tf * (1 - Nys))
```

Appendix C

Custom Substrate Holder for Electro Plating

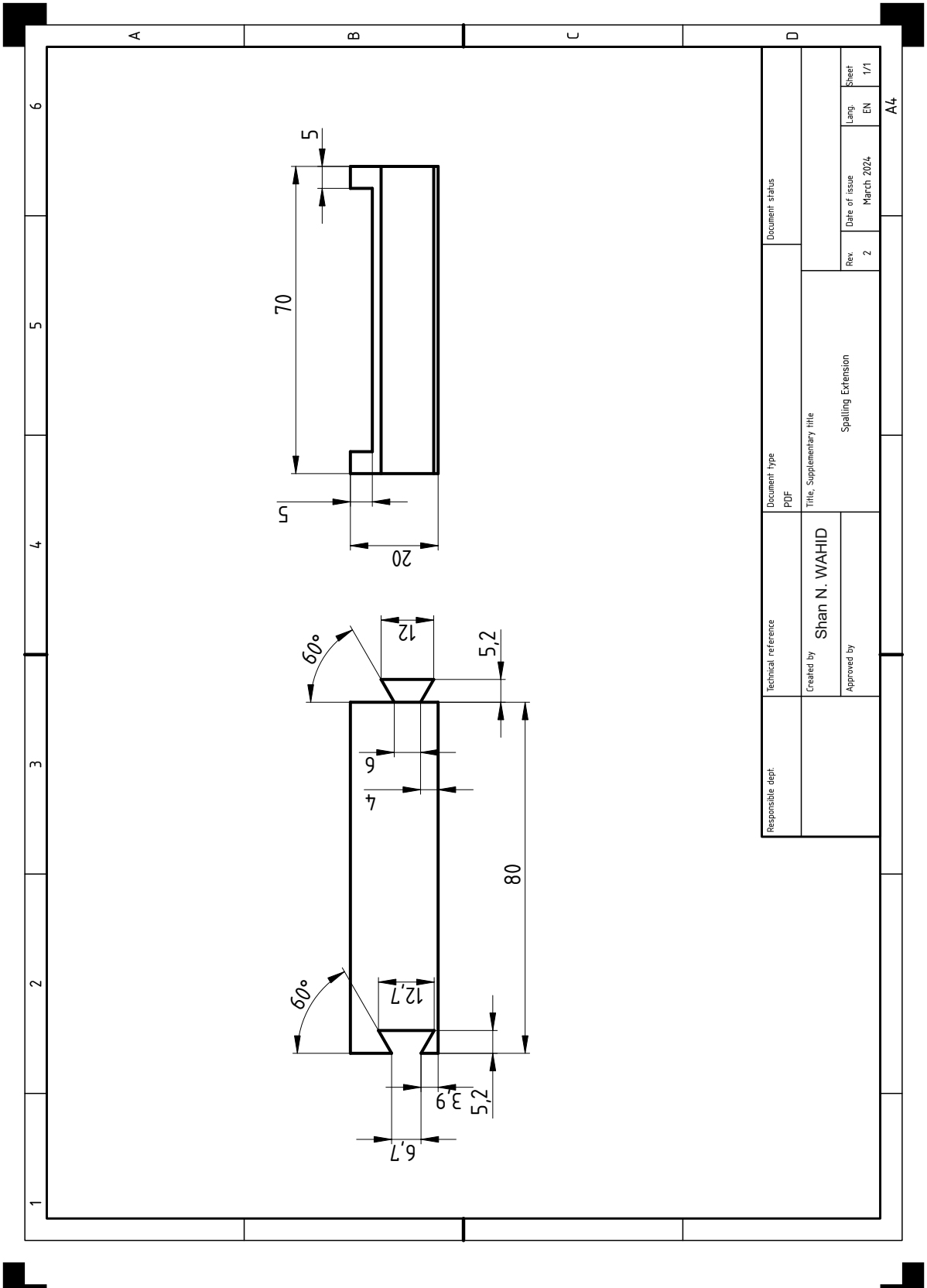


C.1 Cover



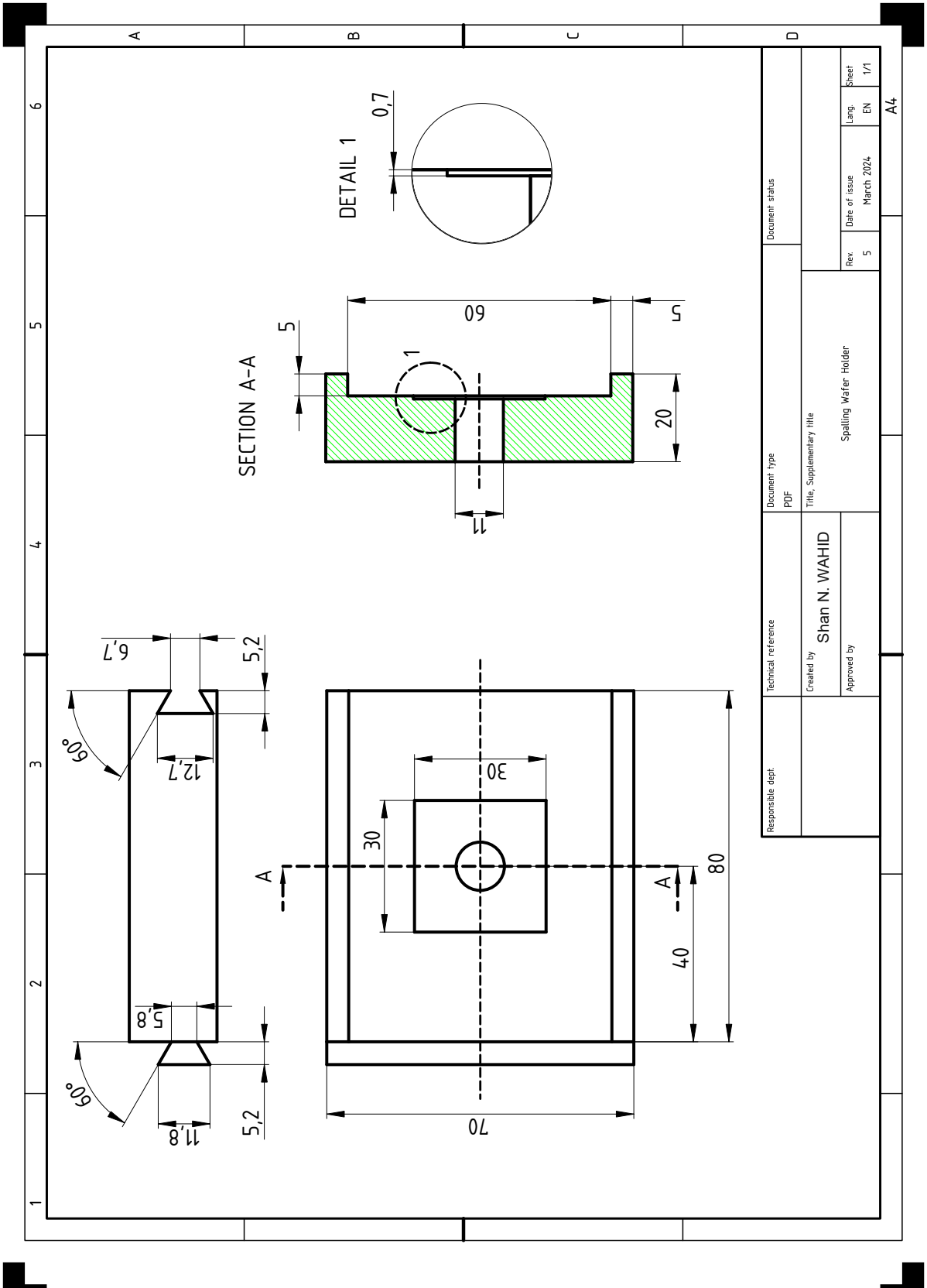
Appendix D

Spalling Ramp - Extension



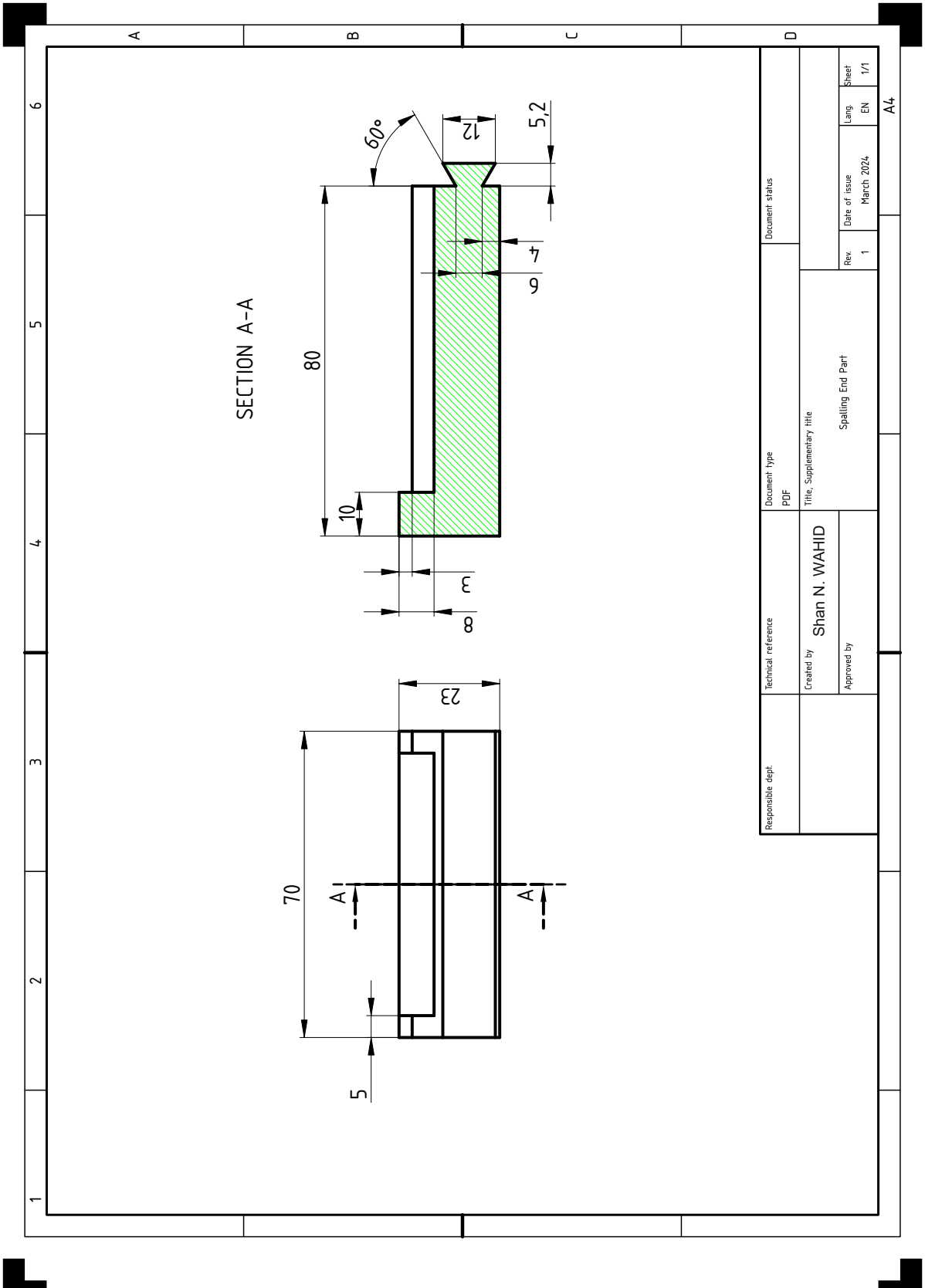
Appendix E

Spalling Ramp - Wafer Holder



Appendix F

Spalling Ramp - End Part



Sworn declaration

I declare that this thesis has been composed solely by myself and that it has not been submitted, in whole or in part, in any previous application for a degree. Except where states otherwise by reference or acknowledgment, the work presented is entirely my own.

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Vienna, on the June 3, 2024

Shan Nizam Wahid, BSc