OE Optical Engineering

RESEARCH PAPER

Cascoded active quencher using a bipolar transistor for fast discharging of a single-photon avalanche

Bernhard Goll,* Michael Hofbauer, and Horst Zimmermann
Technische Universität Wien, Institute of Electrodynamics, Microwave and Circuit Engineering, Vienna, Austria

ABSTRACT. An active quenching circuit in 0.35 μm bipolar complementary metal oxide semiconductor (BiCMOS) technology with a high quenching slew rate is introduced. Quenching transients of an integrated single-photon avalanche diode (SPAD) measured by means of an integrated mini-pad are shown. An NPN transistor as quenching switch enables an active quenching time of 350 ps from an excess bias voltage of 6.6 V and a quenching slew rate of 15 V/ns. Active resetting of the SPAD can be achieved in 550 ps. The power consumption of the BiCMOS quenching circuit is 8.6 mW at 40 Mcounts/s and 3 mW in the idle state.

 [DOI: 10.1117/1.OE.63.7.076102]

Keywords: bipolar complementary metal oxide semiconductor; single-photon avalanche diode; active quenching

Paper 20231141G received Nov. 28, 2023; revised Jun. 9, 2024; accepted Jun. 14, 2024; published Jul. 9, 2024.

1 Introduction

Single-photon avalanche diodes (SPADs) are prone to dark counts and after-pulsing, that is, due to an avalanche that has no photon as its root cause. Dark counts occur without light illumination and are due to thermal excitation or band-to-band tunneling. The dark count rate (DCR) is an important characteristic value of SPADs. After-pulses are correlated to previous avalanches and to the charge flow through the SPAD during an avalanche event. They are mainly originated from charge carriers, which are released from occupied deep-level traps.[1] The probability for the appearance of an after-pulse is characterized by the after-pulsing probability (APP). It is known that fast active quenching reduces the avalanche charge flowing through the SPAD and therefore lowers the APP.[2] Due to the easy gate drive of metal-oxide-semiconductor field-effect transistors (MOSFETs) as switches, many active quenching circuits (AQCs) in complementary metal-oxide semiconductor (CMOS) technology were proposed.[3–7] With a 20 μm diameter SPAD, a quenching time of about 1 ns was achieved in 0.35 μm CMOS for an excess bias voltage of 6 V.[3] In 0.18 μm high-voltage CMOS with an excess bias of 9 V, a 50 μm diameter thin SPAD was quenched in 1 ns.[5] In standard 0.18 μm CMOS with a SPAD diameter of 10 μm and an excess bias of 3.5 V, a quenching time of 0.7 ns was achieved.[6]

An AQC in 0.35 μm CMOS exploiting 5 V transistors and double cascoding showed a reaction time of the comparator of 0.82 ns and needed (additional) 0.88 ns to quench a SPAD with an active diameter of 40 μm and an excess bias of 13.2 V.[7] It is, however, also well known that bipolar transistors possess a higher transconductance and a better driver capability than MOSFETs[8] and therefore will improve AQCs. The first bipolar AQCs were realized with discrete bipolar junction transistors (BJTs).[1,9,10] Bipolar standard components were implemented in

*Address all correspondence to Bernhard Goll, bernhard.goll@tuwien.ac.at

0091-3286/2024/$28.00 © 2024 SPIE

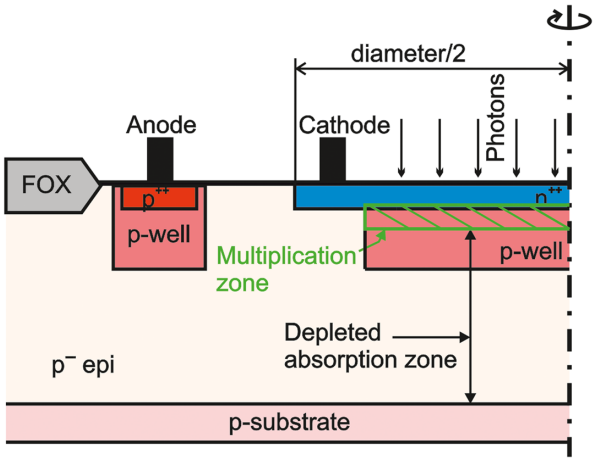

Fig. 1 Cross section of SPAD.

AQCs in Ref. 11. Bipolar transistors in bipolar complementary metal oxide semiconductor (BiCMOS) quenching chips were exploited in Refs. 12 and 13. An off-chip InGaAs SPAD with a diameter of 25 μm was quenched from an excess bias voltage of 5.5 V within 920 ps according to post-layout simulation.[13] The power consumption of the BiCMOS AQC of Ref. 13 was 30 mW.

Lowering the APP with the help of reducing the quenching time of the SPAD instead of increasing the dead time might reduce the amount of pixels, which are necessary for a data receiver with a distinct data rate and sensitivity, and therefore lower chip area as well as power consumption. We applied bipolar transistors in the comparator of an AQC to reduce the reaction time.[14] In this work, we investigate an AQC in the same 0.35 μm BiCMOS technology as in Ref. 14 using a bipolar transistor as quenching transistor. The SPAD is shortly described in Sec. 2. Sections 3 introduces the AQC, Sec. 4 presents measured results, and Sec. 5 concludes the paper.

2 Structure of SPAD

The cross-section of the integrated SPAD is presented in Fig. 1. The SPAD is fabricated in a low-doped epitaxial layer with a thickness of about 12 μm having a boron doping of about 2×10^{13} cm^{-3}. This epitaxial layer serves as thick absorption zone. The bulk of the wafer (p-substrate in Fig. 1) is highly p+ doped. The SPAD is cylinder symmetrical with an n++ diameter of 32 μm and an active (p-well) diameter of 29 μm. A virtual guard ring prevents premature edge breakdown. No process modifications were applied in the PIN-photodiode BiCMOS process used.

The SPAD being well appropriate for 600 to 850 nm was described in detail in Refs. 15 and 16. The thick absorption zone depletes fully at about 19 V[15] and the breakdown voltage V_{BD} was 24.9 to 25.8 V. The probability of the detection of a photon by a SPAD causing a self-sustaining avalanche is described with the photon detection probability (PDP). At 6.6 V excess bias voltage, the PDP is 36.7% at 635 nm and 26.5% at 850 nm (Supplementary Material in Ref. 16). However, due to the thick low-doped epitaxial layer, the SPAD has a larger volume for thermal generation and interaction with traps and its DCR and APP are larger than those of "thin" p+/n-well SPADs, such as, for example, in Ref. 6. Therefore, a dedicated, fast AQC is needed.

3 Circuit with Bipolar Quenching Transistor

Figure 2 shows the circuit diagram of the active quencher. The circuit of the active quencher is located in a deep n-well and therefore isolated from substrate down to −100 V. It needs +3.3 V (V_+) and −3.3 V (V_-) supply voltages. T0 is an NPN transistor used as quenching switch. Because of the simple usage of MOSFETs as cascode transistors, n-channel metal-oxide semiconductor (NMOS) transistor N0 is added in series to transistor T0, to allow an excess bias of 6.6 V for the SPAD, although the BJT and the MOSFETs are specified for a nominal supply

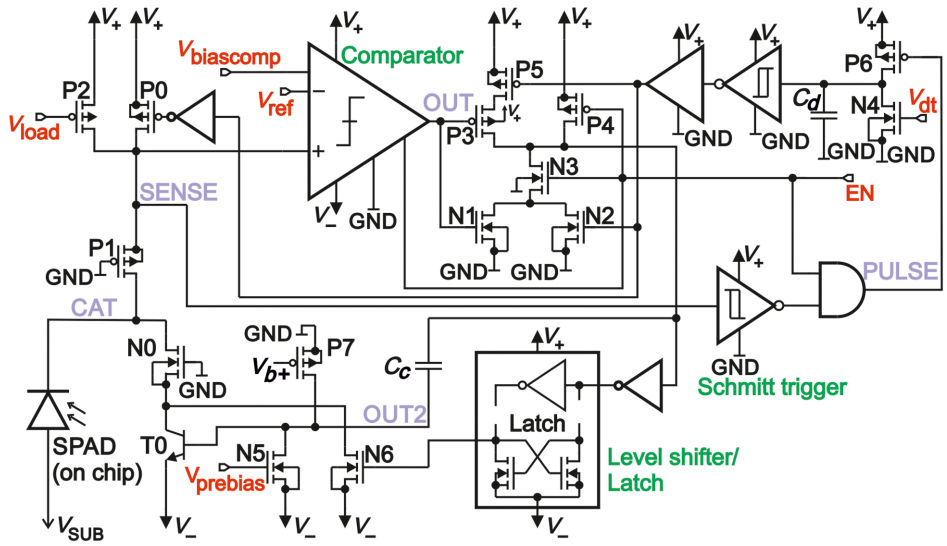

Fig. 2 Circuit diagram of active quenching chip.

voltage of 3.3 V. The recharging switch P0 is connected in series with P1 correspondingly. The cascode configuration of both the quenching switch (T0 and N0) and the resetting switch (P0 and P1) guarantee that the breakdown voltages of these four transistors are not exceeded although the voltage swing of the CAT node and therefore the excess bias of the SPAD is 6.6 V. To bring the SPAD into the Geiger mode, its anode, which is the substrate of the chip, that is, V_{SUB}, has to be connected to a lower voltage than $V_+ - V_{\mathrm{BD}} = 3.3\ \mathrm{V} - V_{\mathrm{BD}}$. Lowering V_{SUB} increases the excess bias until its maximum value of 6.6 V for $V_{\mathrm{SUB}} = -V_{\mathrm{BD}} - |V_-| = -V_{\mathrm{BD}} - 3.3\ \mathrm{V}$ is reached. Then, the SPAD is operated by the AQC with the maximum excess bias voltage of 6.6 V but still reaching V_{BD} during quenching.

After charging the cathode of the SPAD (CAT node) with transistor P0 to voltage V_+, P0 is turned off for awaiting a photon. P5 and N1 are on and P3 and N2 are off. A small current, which is controlled with a bias voltage V_{load} at the gate of transistor P2, is fed to the cathode of the SPAD (node CAT) to compensate for leakage currents (and fed to T0; see below). If a photon triggers an avalanche, the avalanche begins to grow. Since P1 is conducting and P2 delivers only a small current, the voltage at node CAT drops (P0 is off. N0 and T0 are almost off, because of the prebiasing described below) and consequently the potential at the SENSE node falls below the detection threshold of the comparator set by V_{ref}. The output (OUT) of the comparator, which uses two NMOS differential amplifiers (see Fig. 3) instead of BJTs to save electrical power compared to Ref. 14, then also goes down and switches on P3 (see Fig. 2) and N1 off. The rising edge at the drain of P3 is capacitively coupled to the base of the NPN transistor T0 and switches it on. The active quenching starts and T0 pulls the CAT node down to V_-.

Transistors P7 and N5 set the potential at the base of T0 (node OUT2) with the help of voltage V_{prebias}. This reduces the time of charging node OUT2 for turning on T0 and thus leads

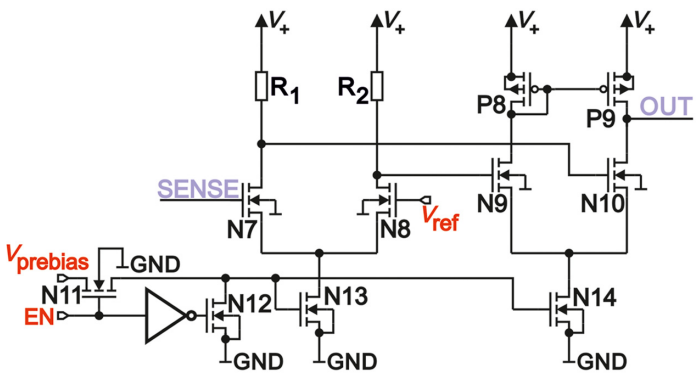

Fig. 3 Circuit of comparator.

to a faster response for quenching. A small collector current of T0 may flow through N0, P1, and P2 because of this prebiasing. Node CAT is pulled to $V\_$ and node SENSE goes to a potential near 0 V, thanks to protection offered by transistor P1. Because of dynamic coupling to OUT2, a small transistor N6 is turned on after a short delay. This guarantees a defined low potential near $V\_$ at node CAT during the whole quenching phase, because T0 is turned on only for a short time (but long enough time for fast quenching) due to capacitive coupling via coupling capacitor (Cc) until OUT2 returns to the steady state potential. This short delay is defined by N5, P7, and the Cc. In such a way, the duration of the active quenching phase by T0 is limited to a minimum to keep the power dissipation small.

A Schmitt trigger, which is connected to node SENSE detects the voltage drop during active quenching and turns off transistor P6. N4 discharges capacitance C_d to introduce a delay to define the dead time. The length of the dead time can be controlled with bias voltage V_{dt}, which adjusts the current through N4. The minimum overall dead time of the quencher in combination with the SPAD is set for $V_{\mathrm{dt}} = 3.3$ V and amounts to 7.1 ns. By reducing the value of C_d, however, the dead time could be reduced by about 2 ns. When P5 is turned off (N2 is turned on), T0 is kept off and the potential at the base of T0 is restored. Node CAT will be charged again to V_+ by P0 for a new photon detection. Every detection of an avalanche event leads to a pulse at node PULSE in Fig. 2. Therefore, this node is connected via output drivers, which are not shown in Fig. 2, to an output pad of the chip.

The Schmitt trigger is a standard circuit based on CMOS inverter and detects the voltage drop, which is originated from fast active quenching, on node CAT (via node SENSE). The fast quenching was initiated by the comparator via Cc and turning on T0 (see Fig. 2). Detection of this voltage drop with the Schmitt trigger initiates recharging of the node CAT with transistor P0 after a delay, which is defined by capacitance C_d. When P0 is turned on, transistor N6 is turned off (T0 was only turned on for a short time) and P5 disconnects the lane of the fast comparator. After recharging of node CAT, which is again detected by the Schmitt trigger, P0 is turned off and P5 is turned on again to be ready for a new detection of the beginning of an avalanche with the comparator and subsequent fast quenching.

The Schmitt trigger has a hysteresis in the way that node PULSE is switched to V_{DD} when node SENSE is near to GND (node CAT is near to $V\_$). On the other hand, node PULSE is switched to GND when recharging of node CAT (detected with node SENSE) is near to V_{DD} and already done. This ensures that, for example, P0 is not turned off too early, when node CAT is still recharging and therefore did not reach V_{DD} yet. The delay time of the logical path between node SENSE and transistor P5 helps to enhance the robustness of the circuit against process and temperature variations of the Schmitt trigger for detection.

It is possible to enable or disable the quencher when connecting pad EN to 3.3 or 0 V, respectively. Setting EN to 0 V turns off transistor N3 and P4 is switched on. Node PULSE is set to 0 V thus turning off P0. Hence transistor N6 is turned on via the level shifter and the cathode of the SPAD (node CAT) is held nearby $V\_$, which results to a cathode-anode voltage of the SPAD of below breakdown. The comparator is disabled in turning off current sources N13 and N14.

The simulated power consumption (post-layout) of the proposed circuit (quencher and output driver) is 8.6 mW for 40 Mcounts/s, which is by a factor of 6.7 less than that of the AQC using a bipolar differential amplifier in the comparator.[14] Between photon counts, that is, in the idle state, when the quencher is enabled and waiting for a photon, the chip dissipates only 3 mW.

The layout is presented in Fig. 4. The chip has dimensions of 1060 μm times 920 μm with a size of the prober pad of 42 $\mu\mathrm{m}^2$. The active area of the BiCMOS active quenching, active resetting circuit is 27,905 $\mu\mathrm{m}^2$ (without output driver). The chip was fabricated in XFAB 0.35 μm PIN-photodiode CMOS adding an NPN transistor process module.

4 Measurement Results

A Picoprobe Model 35 with an input capacitance of 50 fF contacted the prober pad visible in Fig. 4 and an oscilloscope MSOV204A from Keysight stored the measured transients. Dark counts (and their after-pulses) were exploited with the chip inside of a dark box. During the measurement, the temperature of the chip was held constant at 25°C with the help of a

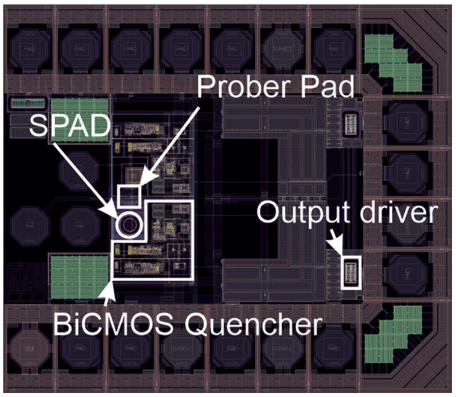

Fig. 4 Layout of active quenching chip.

thermoelectric cooler. Figure 5 depicts the obtained transients for substrate potentials from −26 to −30 V, that is, for excess bias voltages from 2.6 to 7.1 V for a breakdown voltage of ∼26.2 V. However, for $V_{SUB} = -30$ V, the avalanche cannot be quenched robustly anymore due to a maximum possible excess bias of 6.6 V thus after-pulsing increases dramatically (see Fig. 6).

For the reference voltage $V_{ref} = 3.1$ V, that is, a detection threshold of 0.2 V, the reaction time (duration from the transient crossing V_{ref} to the start of active quenching, that is, turning on of T0) of the AQC is shortest. During this reaction time, the passive quenching of the SPAD with P2 as quenching resistor continues. The 90% to 10% fall time during active quenching is 350 ps as marked in Fig. 5. This is 130 ps faster than that of 480 ps of a pure CMOS AQC in the same 0.35 μm technology.[17] It should be mentioned that these 480 ps may be too optimistic because this value is from simulation and not from measurement due to the lack of a prober pad in Ref. 17. Compared to the BiCMOS quencher of Ref. 14 with a wide NMOS quenching transistor and a quenching time of 550 ps, T0 reduces the quenching time by 200 ps. The slew rate during active quenching is 15 V/ns. It should be mentioned that T0 had to drive also the capacitance of the prober pad and of the picoprobe, which add up to a load of 80 fF in sum. Without prober pad and picoprobe, the BiCMOS AQC can switch even faster. Recharging takes place within 550 ps. 7.1 ns after the absorption of the last photon, the next photon can be detected enabling a maximum count rate of 140 Mcounts/s.

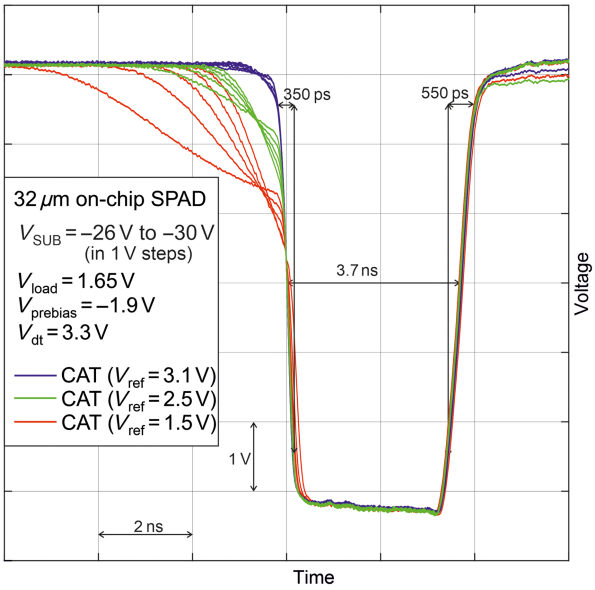

Fig. 5 Measured transient responses at the CAT node for different V_{ref} and V_{SUB}. $V_{SUB} = -26$ V results to a lower excess bias of 3.1V than $V_{SUB} = -30$ V. A lower excess bias causes slower discharging of CAT at the beginning.

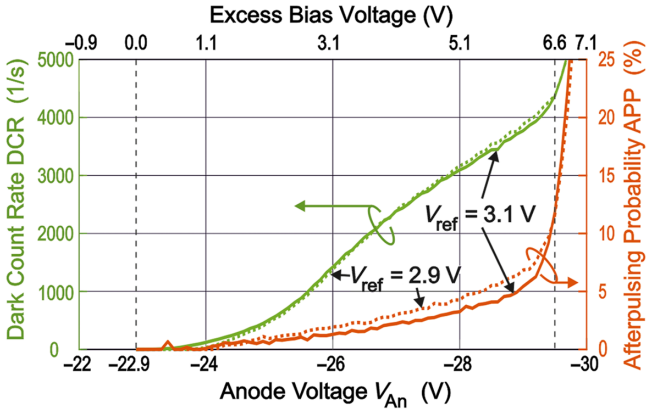

Fig. 6 Measured DCR and APP.

When analyzing the photon count signal at the output pad (equivalent to node PULSE in Fig. 2) for no light on the SPAD, the DCR and the APP can be measured for the SPAD in combination with the active quencher. Figure 6 presents the measured DCR and APP. The APP was determined according to the method of inter-arrival time.[18] The APP is lower for the higher reference voltage, which means a smaller detection threshold for a Geiger mode event. For $V_{\text{ref}} = 2.9$ V, the detection threshold is a bit below 400 mV (because of a small voltage drop across P2 due to the prebias current of T0). For $V_{\text{ref}} = 3.1$ V, the detection threshold is somewhat lower than 200 mV. The APP is below 5% for substrate voltages (anode voltages) down to −28.3 V ($V_{\text{ref}} = 2.9$ V) and −28.9 V ($V_{\text{ref}} = 3.1$ V).

5 Discussion, Comparison, and Conclusion

A reduction of APP is crucial for SPADs to reduce, for example, the bit error rate in SPAD data receivers. A fast active quenching reduces the avalanche charge flowing through the SPAD and therefore it lowers the APP.[2,3] The usage of an NPN transistor as quenching transistor reduces the active quenching phase considerably compared to pure CMOS AQCs. In contrast to the drain area of an NMOS transistor, a NPN transistor has a smaller emitter area for the same transconductance and therefore less parasitic capacitance at its output, that is, at its collector. This reduces the overall capacitance at node CAT, which decreases the charge flow for a given voltage drop even for the passive quenching at the beginning. The fast active quenching time of 350 ps indicates a lower capacitive load as well. Compared to an active quencher in the same 0.35 μm BiCMOS technology, which used a bipolar differential amplifier in the comparator,[14] the power consumption is reduced by a factor of 6.7 (see Table 1). To reduce the power consumption, the comparator was designed for the supply rails of $V_+ = 3.3$ V and GND (instead of +3.3 V and −3.3 V, that is, instead of a total supply voltage of 6.6 V, used in Ref. 14) and CMOS transistors were used instead of BJTs. Charging and discharging of lower parasitic capacitances due to the on-chip SPAD further reduces the consumed power compared to quenchers with off-chip SPADs. As an example, a quencher in 0.35 μm SiGe BiCMOS with an InGaAs off-chip SPAD needed a power consumption of 30 mW.[13]

Compared to nanometer CMOS technologies, which usually require a low supply voltage of about 1 V (as in Ref. 2) or 0.7 V (as in Ref. 19, the quencher in a 0.35 μm technology with its 3.3 V supply voltage is able by exploiting cascoding to drive the SPAD with an excess bias up to 6.6 V. A larger excess bias increases the PDP of the SPAD. For a voltage swing of 6.6 V, a quenching time of 350 ps is competitive with nanometer CMOS technologies when considering speed (see Ref. 2 in Table 1). However, cascoding would result in only 2 V swing (= excess bias) and the PDP would be much smaller using the technology of Ref. 2.

The total quenching time is larger than that of a thin p+/n-well SPAD in Refs. 6 and 19 because of the slower avalanche build-up of our thick SPAD and in turn a longer passive quenching phase in 0.35 μm (Bi)CMOS. This is a consequence of the higher doping of the wells in the thin p+/n-well SPADs in Refs. 6 and 19, because those SPADs have a lower series resistance and are capable to conduct more current during an avalanche than our SPAD with p−-epi absorption

Table 1 Comparison of SPADs and AQCs at room temperature.

Ref.	Technology	(μm)	Max. vex (V)	PDP @ λ (%)/(nm)	APP (%)	Dead time (ns)	DCR (cps)	Overall quenching time (ns)	Active quenching time (ps)	Power consumption (mW)
2	28 nm FD-silicon-on-insulator CMOS	25	1.0	—	~8 ~42	50 5	—	~0.7	~250	—
6	0.18 μm CMOS	10	3.5	34/450 2.5/850	0.75	~5	6900	0.7	—	—
13	0.35 μm SiGe BiCMOS	25a	5.5	—	<0.05	>1000	—	0.92	300b	30c
14	0.35 μm BiCMOS	34	6.6	—	—	10	—	—	550	58d
17	0.35 μm CMOS	80	6.6	35.1/635	4.8	9.5	~31,000	1.1 (sim.)	480 (sim.)	10.03e
19	65 nm CMOS	10	0.7	23.8/420 ~2/850 @V_{ex} = 0.5 V	~0	3.35	20,000 @V_{ex} = 0.5V	0.1	—	—
This work	0.35 μm BiCMOS	32	6.6	36.7/635 26.5/850	11.6	7.1	4400	1.23 (V_{ref} = 3.1 V)	350f	8.6d

[a]Off-chip InGaAs SPAD
[b]80% to 20% rise time
[c]Simulated
[d]For a photon count of 40 Mcounts/s including output driver
[e]For a photon count of 100 Mcounts/s without output driver
[f]90% to 10% fall time

zone. On the other hand, there is a tendency for thin SPAD to lower diameters which reduces DCR and to some extend APP (also depending on dead time and excess bias) to account for the generally higher doping concentrations in modern standard nm-CMOS technologies, which tend to increase DCR and APP. In Table 1, it can be seen that a thick SPAD has its advantage for detection at near infrared wavelengths (PDP of 26.5% at 850 nm), which is one of the transmission windows of a glass fiber and at the wavelengths used in many ranging and light detection and ranging (LIDAR) systems.

The detection threshold of 200 mV compared to 100 mV in Ref. 17 caused also a slightly longer passive quenching phase leading to the total quenching time of 1.23 ns. There will be a cost advantage for optical sensors and receivers in 0.35 μm BiCMOS compared to 0.18 μm CMOS, especially in low-volume ASIC fabrication due to a large difference in mask costs. The dead time is reduced to 7.1 ns compared to 9.5 ns in Ref. 17. Having this shortened dead time in mind, the after-pulsing probabilities of 2.08% and 1.36% for V_{ref} of 2.9 and 3.1 V, respectively, at $V_{ex} = 3.3$ V are good values increasing to about 11.6% for $V_{ex} = 6.6$ V.

Finally, it should be mentioned that, in comparison to circuits with only a few CMOS transistors as in Refs. 2 and 19, which are therefore appropriate for large pixel arrays, our solution has more functionality, such as, for example, an excess voltage up to 6.6 V, adjustment of the dead time from 7.1 ns to large values ($V_{dt} = 0$ V) or fine adjustment of the detection threshold with V_{ref} and a comparator. But, of course, our circuit is not appropriate for application in arrays with many pixels.

Code and Data Availability

Data and code are not publicly available but can be provided upon reasonable request.

Acknowledgments

The authors thank Austrian Science Foundation (FWF) for its support (Grant No. P32393-N30). The authors have no relevant financial interests in the paper and no other potential conflicts of interest to disclose.

References

1. S. Cova et al., "Avalanche photodiodes and quenching circuits for single-photon detection," *Appl. Opt.* **35**(12), 1956–1976 (1996).
2. M. Dolatpoor Lakeh et al., "An ultrafast active quenching active reset circuit with 50% SPAD afterpulsing reduction in a 28 nm FD-SOI CMOS technology using body biasing technique," *MDPI Sens.* **21**(12), 4014 (2021).
3. D. Bronzi et al., "Fast sensing and quenching of CMOS SPADs for minimal afterpulsing effects," *IEEE Photonics Technol. Lett.* **25**(8), 776–779 (2013).
4. G. Giustolisi, A. D. Grasso, and G. Palumbo, "Integrated quenching-and-reset circuit for single-photon avalanche diodes," *IEEE Trans. Instrum. Meas.* **64**(1), 271–277 (2015).
5. F. Ceccarelli et al., "Fully integrated active quenching circuit driving custom-technology SPADs with 6.2-ns dead time," *IEEE Photonics Technol. Lett.* **31**(1), 102–105 (2019).
6. Y. Xu, J. Lu, and Z. Wu, "A compact high-speed active quenching and recharging circuit for SPAD detectors," *IEEE Photonics J.* **12**(6), 6803208 (2020).
7. A. Dervić et al., "High slew-rate quadruple-voltage mixed-quenching active-resetting circuit for SPADs in 0.35-μm CMOS for increasing PDP," *IEEE Solid-State Circuits Lett.* **4**(1), 18–21 (2021).
8. W. Sansen, *Analog Design Essentials*, Springer, New York (2006).
9. S. Cova, A. Longoni, and G. Ripamonti, "Active-quenching and gating circuits for single-photon avalanche diodes (SPADs)," *IEEE Trans. Nucl. Sci.* **29**(1), 599–601 (1982).
10. F. Acerbi et al., "Fast active quenching circuit for reducing avalanche charge and afterpulsing in InGaAs/InP single-photon avalanche diode," *IEEE J. Quantum Electron.* **49**(7), 563–569 (2013).
11. J. Liu et al., "Fast active-quenching circuit for free-running InGaAs(P)/InP single-photon avalanche diodes," *IEEE J. Quantum Electron.* **52**(10), 1–6 (2016).
12. R. Mita, G. Palumbo, and G. Fallica, "A fast active quenching and recharging circuit for single-photon avalanche diodes," in *Proc. 2005 Eur. Conf. Circuit Theory and Des.*, Vol. **3**, pp. III/385–III/388 (2005).
13. A. Ruggeri et al., "Integrated circuit for subnanosecond gating of InGaAs/InP SPAD," *IEEE J. Quantum Electron.* **51**(7), 1–7 (2015).
14. B. Goll, B. Steindl, and H. Zimmermann, "Cascoded active quencher for SPADs with bipolar differential amplifier in 0.35 μm BiCMOS," *IEEE Photonics J.* **14**(2), 1–8 (2022).
15. B. Steindl et al., "Linear mode avalanche photodiode with high responsivity integrated in high-voltage CMOS," *IEEE Electron Device Lett.* **35**(9), 897–899 (2014).
16. H. Zimmermann et al., "Integrated fiber optical receiver reducing the gap to the quantum limit," *Sci. Rep.* **7**, 2652 (2017).
17. R. Enne et al., "Fast cascoded quenching circuit for decreasing afterpulsing effects in 0.35-μm CMOS," *IEEE Solid-State Circuits Lett.* **1**(3), 62–65 (2018).
18. M. Hofbauer, B. Steindl, and H. Zimmermann, "Temperature dependence of dark count rate and after pulsing of a single-photon avalanche diode with an integrated active quenching circuit in 0.35 μm CMOS," *J. Sens.* **2018**, 9585931 (2018).
19. W. Jiang, R. Scott, and M. J. Deen, "High-speed active quench and reset circuit for SPAD in a standard 65 nm CMOS technology," *IEEE Photonics Technol. Lett.* **33**(24), 1431–1434 (2021).

Bernhard Goll received his MSc degree in 2003 and his PhD in 2007 in electrical engineering from TU Wien. Since 2003, he has worked at the Institute of Electrodynamics, Microwave and Circuit Engineering at TU Wien. His field of interest is analog circuit design, especially optical receivers. He has authored and coauthored more than 80 publications and conference contributions.

Michael Hofbauer received his Dipl.-Ing. degree in electrical engineering and his PhD sub auspiciis praesidentis from TU Wien, Vienna, Austria, in 2011 and 2017, respectively. Since 2011, he has been a project assistant, and later a university assistant, at the Institute of Electrodynamics Microwave and Circuit Engineering, TU Wien. His interests are in integrated optoelectronics, radiation effects, electronic-photonic integration, and optical sensing. He has authored and coauthored more than 80 publications and conference contributions, as well as one book.

Horst Zimmermann received his Dr.-Ing. degree from the University Erlangen-Nürnberg in 1991, became Alexander-von-Humboldt Research-Fellow at Duke University, and joined Kiel University in 1993, working on optoelectronic integration. Since 2000, he has been a professor in electronic circuits at TU Wien. His main interests are in optoelectronic (Bi)CMOS circuits. He (co)authored 10 books and over 600 publications. He is senior member of IEEE, and was primary guest editor of "Optical Detectors: Technology and Applications," IEEE JSTQE (November/December 2014).