Hardware Model Checking Competition 2024

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***Abstract*—The Hardware Model Checking Competition 2024 (HWMCC'24) was the 12th competitive event for hardware model checking tools. The competition was affiliated to the 24th conference on Formal Methods in Computer-Aided Design 2024 (FMCAD'24), which took place in Prague, Czech Republic, from October 14 to 18, 2024.**

***Index Terms*—Automated Reasoning, Model Checking, Hardware Verification, Word-level Reasoning, Bit-Vectors, Certificates**

The Hardware Model Checking Competition (HWMCC'24) in 2024 is the 12$^{\text{th}}$ incarnation in this series of competitive events to evaluate hardware model checking. Since it started in 2007 it was repeated annually with some exceptions. After the previous competition in 2020 the organizers took a break to resume the competition in 2024. The competition in 2024 is affiliated, as most of the time, with the conference on Formal Methods in Computer-Aided Design (FMCAD), which is considered the primary venue for formal hardware verification. Alternatively in 2007, 2008, 2010 and 2014 it was affiliated with the conference of Computer-Aided Verification (CAV).

The previous competition in 2020 continued with word-level tracks, which were introduced in 2019. These word-level tracks focus on bit-vector models with and without arrays in the BTOR2 format [1]. This suggests that model checkers participating in this track should make use of SMT solvers over the theory of bit-vectors. Before 2019 all competition tracks used bit-level models in the AIGER format [2], but were split into safety, multi-property, liveness and deep tracks. Since 2014 and particularly in 2017, the last competition before 2019, the ABC tool [3] dominated almost all bit-level tracks.

One motivation for moving to word-level tracks is the conjecture that SMT solving is more effective than plain SAT solving if the models are given in terms of bit-vectors. However, in 2019 the word-level model checkers could not fulfill this promise and were trailing ABC by a large margin in terms of performance. This was particularly the case for unsatisfiable properties, where a bad state violating the single safety property can not be reached. Note, that ABC was run on AIGER models obtained from the BTOR2 models through bit-blasting, except for the array track, as bit-blasting of BTOR2 models with arrays is difficult. Having arrays, modelling memory or caches, is considered a feature of SMT solvers and should give them an advantage over bit-level reasoning.

In 2020 the picture changed and word-level model checkers started to become competitive to ABC on the bit-vector track without arrays, while not losing their advantage on bit-vector models with arrays, as bit-blasting arrays was still not available. Therefore, the organizers of HWMCC'24 decided to continue both word-level tracks, i.e., with and without arrays.

While the previous competition in 2020 focused on word-level exclusively, the single safety property track came back in 2024. However, as a novel feature, participating model checkers are required to produce model-checking certificates. These certificates were actually AIGER circuits and should have an inductive property. They further need to simulate the original circuit as formalized in [4], [5], [6]. The tool CERTIFAIGER is used to check both requirements using SAT solvers. The goal of the certified track is to increase trust in verification results produced by model checkers, following the success story of proof producing SAT solvers in both academia and industry, e.g., producing proofs became mandatory in the main track of the SAT competition in 2016 [7].

More details on the competition, including provided tools, submission procedure and deadlines, the results and their presentation are available at the competition home page [8].

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