Unterschrift Betreuer

TECHNISCHE UNIVERSITÄT WIEN
Vienna University of Technology

DIPLOMARBEIT

A Physical Approach to High-Bandwidth, Low Insertion Impedance Current Measurement for High-Frequency Switching Wide-Bandgap Devices

ausgeführt am Insitut für Angewandte Physik
der Technischen Universität Wien
und am Austrian Institute of Technology

unter der Anleitung von
Ao.Univ.Prof. DI Dr.techn. Martin Gröschl
Univ.-Prof. DI Dr.techn. Markus Makoschitz

durch

DI(FH) Stephan Ledinger

Matrikelnummer: 1029127

Signiert von: Stephan Ledinger
Datum: 12.09.2024 18:01:50
TRUST
Dieses Dokument ist digital signiert!
Dieses mit einer qualifizierten elektronischen Signatur versehene Dokument hat gemäß Art. 25 Abs. 2 der Verordnung (EU) Nr 910/2014 vom 23. Juli 2014 ("eIDAS-VO") die gleiche Rechtswirkung wie ein handschriftlich unterschriebenes Dokument.
Prüfinformation: Informationen zur Prüfung der elektronischen Signatur finden Sie unter: www.a-trust.at/pdf

Wien, am 12. September 2024

Unterschrift Student

Abstract

Since its invention by Julius Edgar Lilienfeld in 1926, the field-effect transistor FET led the way to the invention of the metal-oxide-semiconductor field-effect transistor (MOSFET) in the 1960s. Contrary to their poor performance in the beginning, MOSFETs soon improved their switching characteristics and switching is what they are mostly known and used for in power electronics today. Until the introduction of MOSFETs based on silicon carbide (SiC) in 2011 and high electron mobility transistors HEMTs based on gallium nitride (GaN) in 2010, Si and other semiconductors with band gaps $<2\,\mathrm{eV}$ were the only options for power electronics designs. Since then, transistors based on WBG semiconductors became the focus for new developments in the field. Compared to traditional Si, GaN and SiC transistors offer improved electrical features due to their wide bandgaps of 3.4 eV and 3.26 eV. The most prominent improvements are the higher blocking voltage, faster switching speed, and superior thermal characteristics. The improved switching behaviour of GaN and SiC transistors is the key ingredient for more efficient power converters and thus helps to save substantial amounts of energy in power conversion on big and small scales. This thesis focuses on the improved switching performance of GaN transistors, which is mainly a result of a) the high electron mobility of the GaN substrate, hence the very low R_{DS-ON} and b) the reduced parasitic capacitance and inductance. The latter is a result of the compact package and improved connection between package and chip. GaN devices allow switching within 1 ns. To achieve such fast slew rates, the rest of the electrical circuitry must be dimensioned accordingly. The copper traces of the commutation and driver loop must feature lowest possible impedances. When developing power converters, it is essential to know the voltage and current across the switch. Their product is the power loss of the switching transistor, which has the most impact on the correct function and efficiency of the power converter. Additionally, voltage and current indicate if the switching process is precise, without transient oscillations or even ringing after switching. The evaluation is done by measuring the voltage v_{DS} and current i_{DS} across drain and source of the transistor. Voltage sensing is straight forward and can be done with some custom made test points at the PCB. The current measurement requires a sensor to be fitted into the commutation path, which inevitably adds insertion impedance for the measured current. The amount of inserted impedance highly depends on the sensor type and implementation design. Conventional sensors and shunts usually come with high parasitics and a

bandwidth which is too low to capture the fast transient. Furthermore, galvanically isolated current sensing would be preferable. To evaluate current sensing for WBG semiconductors, this thesis takes a look at suitable physical phenomena and current sensors based on these effects. Custom made PCBs for the so-called double pulse test with two GaN transistors in a half bridge configuration were developed and tested in three different variations. These variations feature two different current sensors, firstly the established coaxial shunt (CSR) and secondly the novel Infinity Sensor, a specifically optimized Rogowski coil, developed and sold by the University of Bristol. The third variant features both sensors in combination, enabling measurement verification. All three variants were used for double pulse tests, a common evaluation procedure for transistor switching. Measurements were taken, post-processed, and assessed for the technical feasibility of the sensors as well as their limitations for the intended purpose. Further technologies for current sensing were considered theoretically and partially adapted to the existing PCBs, but not tested yet. These are described in the outlook and future work. A miniaturized version of the coaxial shunt was proposed, which is called ultra fast current shunt (UFCS). Another promising technology is the fibre optical current sensor (FOCS) which uses the Faraday effect, and combines galvanic isolation and very low parasitic impedance. Until now, this technology is only used for high voltage applications with very high currents. Again, miniaturization could lead the way for this technology to the application in power electronics as mFOCS.

Kurzfassung

Nach der Erfindung des Feldeffekttransistors (FET) durch Julius Edgar Lilienfeld 1926, führte der Weg der Silizium-basierten Halbleiter zur Erfindung des Metall-Oxid-Halbleiter-Feldeffekttransistors MOSFET in den 1960ern. Das anfänglich schlechte Schaltverhalten von MOSFETs wurde schnell verbessert und war bald ein Vorteil, der die MOSFETs zu den wichtigsten Komponenten der Leistungselektronik machte. Bis zur Markteinführung von Transistoren, basierend auf Galliumnitrid (GaN) 2010 und Siliziumkarbid (SiC) 2011, waren dotiertes Silizium und andere Halbleiter mit einer Bandlücke von $<2\,\mathrm{eV}$ das Mittel der Wahl für die Grundbausteine in der Leistungselektronik. Seither sind Wide-Bandgap Halbleiter in den Fokus für Neuentwicklungen in der Leistungselektronik gerückt. GaN- und SiC-Transistoren bieten aufgrund ihrer größeren Bandlücken von $3.4\,\mathrm{eV}$ und $3.26\,\mathrm{eV}$ verbesserte elektrische Eigenschaften verglichen mit traditionellem Si. Die wichtigsten Verbesserungen sind höhere Sperrspannungen, eine schnellere Schaltgeschwindigkeit, und verbesserte thermische Eigenschaften. Das schnellere Schalten der SiC- und GaN-Transistoren ist der Schlüssel zu effizienteren Leistungsumrichtern und ermöglicht damit erhebliche Energieeinsparungen in der Leistungsumwandlung auf großen und kleinen Skalen. Daher wurde in dieser Arbeit das verbesserte Schaltvermögen von GaN-Transistoren betrachtet. Das schnellere Schalten ergibt sich a) aufgrund der verbesserten Elektronen-Mobilität, welches einen niedrigeren R_{DS-ON} zur Folge hat und b) wegen der geringeren parasitären Kapazitäten und Induktivitäten im Vergleich zu Si-Transistoren. Letzteres ist ein Resultat der kompakteren Packages und der besseren Anbindung des Chips im Package. Dadurch sind Schaltvorgänge im Bereich von $1\,\mathrm{ns}$ möglich. Um diese Schaltzeiten des GaN-Transistors zu erreichen, muss der Rest der elektrischen Schaltung entsprechend optimiert sein. Die Leiterbahnen im Kommutierungs- und Treiberpfad sind mit möglichst geringer Impedanz auszulegen. Bei der Entwicklung von Leistungsumrichtern ist die Kenntnis von Strom und Spannung am schaltenden Transistor im Kommutierungspfad von besonderem Interesse, da sich aus ihrem Produkt die Schaltverluste berechnen. Diese sind maßgeblich für die Effizienz des Gerätes verantwortlich. Außerdem zeigen Strom und Spannung ob der Schaltvorgang „sauber“, also ohne Einschwingvorgänge und resonantes Nachschwingen erfolgt ist. Dies geschieht mittels Messung der Spannung v_{DS} und des Stromes i_{DS} zwischen Drain und Source des Transistors. v_{DS} kann über angepasste Abgriffe an der Leiterplatte mittels Tastkopf erfasst werden. Für die Strommessung

muss ein Sensor in den Kommutierungspfad eingebracht werden, der unweigerlich zusätzliche Impedanz für den zu messenden Strom bedeutet. Die Höhe der Impedanz hängt stark vom Sensortyp und dessen Implementierung ab. Marktübliche Stromwandler und Shunts sind mit einer zu hohen parasitären Induktivität behaftet und weisen außerdem bei der hier notwendigen Kompaktheit eine zu niedrige Bandbreite für GaN-Schaltvorgänge auf. Außerdem wäre es vorteilhaft, wenn der Stromsensor vom Messsignal galvanisch isoliert wäre.
Um Strommessmethoden für WBG-Halbleiter zu evaluieren, wurden im Zuge dieser Arbeit geeignete physikalische Phänomene und damit realisierte Strommessmethoden untersucht. Zu diesem Zweck wurden Leiterplatten für sogenannte Doppelpulstests mit zwei GaN Schalter in Halbbrückenkonfiguration in drei verschiedenen Varianten entwickelt und getestet. Diese drei Varianten enthalten zwei unterschiedliche Stromsensoren: a) einen am Markt verfügbaren Koaxial-Shunt (CSR) und b) den neuartigen, von der Universität Bristol entwickelten und vertriebenen Infinity Sensor. Die dritte Variante enthält beide Sensoren in Kombination zur Verifikation. Alle drei Varianten wurden mit dem etablierten Testverfahren des Doppelpulstests betrieben, Messergebnisse erfasst, aufbereitet, und evaluiert. Zu diesem Zweck wurde im Leistungselektronik-Labor des AIT eine Prüfzelle mit allen notwendigen periphären Geräten aufgebaut und in Betrieb genommen. Die damit erfassten Messergebnisse wurden diskutiert und davon die technische Eignung und Limitierung der jeweiligen Sensortechnologie erarbeitet. Weitere Strommessmethoden wurden theoretisch betrachtet und bereits in Schaltungen integriert, aber noch nicht vermessen. Diese sind Teil des Ausblicks auf zukünftige Arbeiten. Dies betrifft vor allem die miniaturisierte Form des Koaxial-Shunts, der Ultra Fast Current Shunt (UFCS) genannt wird. Eine weitere vielversprechende Technologie, die sowohl galvanische Isolation als auch besonders niedrige parasitäre Impedanz vereint, ist die des faseroptischen Stromsensors auf Basis des Faraday-Effekts. Dieser wird Fibre Optical Current Sensor (FOCS) genannt und ist bisher nur in der Hochspannungstechnik für sehr hohe Stromstärken in Verwendung. Auch hier könnte die Miniaturisierung dieser Technologie den Weg zu mFOCS weisen und deren Anwendung in der Leistungselektronik ermöglichen.

Contents

1. Introduction

Since the first patent on a field-effect transistor (FET) by Julius Edgar Lilienfeld in 1926 [33], silicon (Si) became a dominant material in electronic switching devices. Further development led to the invention of the metal-oxide-semiconductor field-effect transistor (MOSFET) in the 1960s [27]. From the successive improvements of the semiconductor technology, the field of power electronic emerged, where low switching losses and high power density are performance indicators of power converters. Because of their 1.12 eV bandgap, Si-based switches face a limit of those performance indicators. These limitations of Si led to efforts to develop wide-bandgap (WBG) semiconductors, where bandgaps of >3 eV seemed theoretically possible, but practically unfeasible for decades. Since their first appearance on the market (GaN 2010 [7], SiC 2011 [1]), WBG devices have come to the focus in power electronics to replace Si. Currently, there are two technologies on the market; MOSFETs based on silicon carbide (SiC) and high electron mobility transistors (HEMT) based on gallium nitride (GaN). Their improved electrical parameters allow the construction of power converters with higher current density and blocking voltage compared to Si, which leads to higher efficiency and power density. This thesis focuses on the improved slew rate (switching speed) of WBG semiconductors and how to measure it. Due to the low parasitic capacitance and high electron mobility of the substrate of the WBG devices, current slopes below 1 ns can be achieved. [46] compares the hard switching performance of Si and GaN transistors. The Si switch has an output capacitance of $C_o = 1.63\,\text{nF}$ and $R_{DS-ON} = 40\,\text{m}\Omega$ when the equivalent GaN switch features only 286 pF and $R_{DS-ON} = 27\,\text{m}\Omega$. These parameters can only realize the desirable steep current ramps if the rest of the PCB is optimized to fit the electrical parameters of the WBG transistor. Designing the commutation loop with its copper traces and electronic components with as little impedance as possible is of crucial importance. When it comes to measuring the voltage, there is not much to add to the circuit, because usually two test points can be fit in unused corners of the PCB and are sufficient for picking up v_{DS} of the transistor. Current sensing requires changes of the PCB, because a sensor has to be introduced to the current loop, unless R_{DS-ON} is used as current viewing resistor (CVR), which is a choice of low precision. Added impedance mainly means insertion inductance of the current sensor. Firstly, a sensor usually has its own inductance, secondly the attachment of the sensor to the existing PCB also adds impedance. Inevitably, every added impedance already changes the measured

current. Generally, the insertion impedance of any current sensor must be kept small enough so the influence on the current stays below an acceptable level. This is usually no issue with low frequency AC and DC currents and standard sensors. But when it comes to fast switching WBG devices, adding the wrong sensor, e.g. a current shunt with straight, parallel leads, can add too much impedance so that the transistors get destroyed because of the increased switching losses. Additionally, such high-impedance sensors do not offer enough bandwidth to capture the fast transient. Furthermore, isolated measurement techniques are desirable in this environment. Isolation allows direct processing of the measured signal from the commutation loop without any further isolating element, tied to potential loss of bandwidth and precision. By measuring the switching current v_{DS} and voltage v_{DS} at all relevant transistors, a power converter can be designed and tested to operate more efficiently and safely [36], [35].

With traditional Si MOSFETs, a standard testing procedure, the so-called double pulse test (DPT) with common current sensors was used. Changing from Si to WBG devices and the introduction of new highly compact packages poses the problem that these current sensors aren't suitable for the DPT anymore. Hence, this thesis is an attempt to facilitate the DPT with GaN transistors in a half-bridge configuration and improved methods of current sensing. The novel, so-called Infinity Sensor [24] is compared to a coaxial shunt resistor (CSR). Both technologies were integrated into three newly designed PCBs with: i) CSR, ii) Infinity Sensor, and iii) CSR and Infinity Sensor in combination. Additionally, other new concepts for high bandwidth current sensing are discussed and were partially fitted onto the DPT PCBs but not tested yet. A promising upgrade is proposed in [49], where an ultra fast current shunt (UFCS) offers improved electrical parameters due to the miniaturization and additional differential amplifier and filter. Another entirely new technology in the field is the fibre optical current sensors (FOCS), which is currently available as a product of ABB for high currents in high voltage power stations [29]. Due to their fundamental working principle which uses the Faraday effect, the FOCS measure the current based on the change of the angle of the circular polarization of light in a fibre, coiled around the current carrying conductor. Here the idea again is to miniaturize this sensor and create (mFOCS), which would allow isolated, low-insertion impedance current measurements for PCB-sized applications.

Coming back to different types of power transistors, there are some relevant key parameters that are crucial in power electronics. Some of them, like the parasitic capacitances and DS resistance are often sketched in equivalent circuits, which are generally used to describe and model electronic components. An equivalent circuit of a GaN transistor is given in figure 1.1. The shown parasitic elements are not specific features of GaN devices but are present as well in IGBTs and Si/SiC

MOSFETs. The crucial difference between these technologies is the size of these parasitic capacitances.

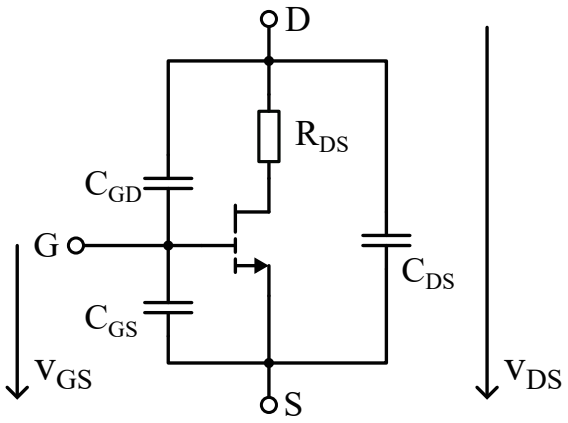


Figure 1.1.: Equivalent circuit of a GaN transistor with parasitic capacitances

Often, the parasitic capacitances are referred to as shown in the equivalent circuit of figure 1.1. Sometimes, the capacitances are merged to represent the parasitics for specific values, like shown in equations 1.1 to 1.3, where C_{iss} is the input capacitance, C_{oss} is the output capacitance, and C_{rss} represents the reverse transfer capacitance which is also called the feedback capacitance.

$$C_{iss} = C_{GS} + C_{GD} \tag{1.1}$$

$$C_{oss} = C_{DS} + C_{GD} \tag{1.2}$$

$$C_{rss} = C_{GD} \tag{1.3}$$

Exemplary values for common power MOSFET devices (Si, SiC) in comparison to GaN transistors are listed in table 1.1. V_{BR-DS} is the reverse break down voltage, which describes the maximum blocking voltage of the transistor between drain and source.

Type	**Bandgap**	$\mathbf{C_{iss}}$	$\mathbf{C_{oss}}$	$\mathbf{C_{rss}}$	$\mathbf{R_{DS-ON}}$	$\mathbf{V_{BR-DS}}$
Si [55]	1.12 eV	4.81 nF	230 pF	5 pF	53 mΩ	600 V
SiC [60]	3.26 eV	215 pF	19 pF	2.2 pF	800 mΩ	1.7 kV
GaN [52]	3.4 eV	518 pF	126 pF	5.9 pF	25 mΩ	650 V

Table 1.1.: Comparison of main electrical parameters of different transistor types

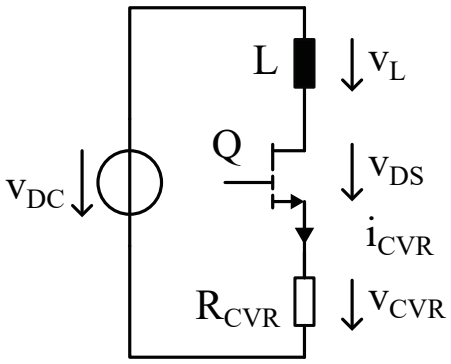
2. State of the art

2.1. Physical phenomena for current sensing

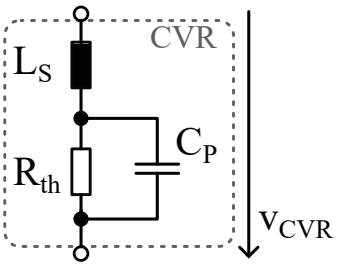
Currently, there are two main phenomena that allow electrical current sensing, the electrical resistance and the electromagnetic induction. Additionally, the Faraday effect has become a third alternative to the first two physical phenomena available for sensing electrical current.

2.1.1. Electrical resistance

To use electrical resistance for current measurement, the voltage v_{CVR} across a specific part of a circuit of known electrical resistance R_{CVR} is measured. Such a resistor is often called current viewing resistor (CVR). By applying Ohm's Law, the current $i_{CVR} = v_{CVR}/R_{CVR}$ can be deduced. An exemplary measurement circuit with a CVR is given in figure 2.1a. R_{CVR} is placed in series with the existing circuit containing a voltage source V_{DC}, and inductor L and the transistor Q. As long as the CVR is purely ohmic, the voltage v_{CVR} is direct proportional to the current i_{CVR} by the factor $1/R_{CVR}$



(a) Simple measurement circuit with CVR



(b) Equivalent circuit of a real CVR

Figure 2.1.: Simplified schematic of current measurement with CVR and equivalent circuits for a real CVR and a transistor

Some intricacies arise when the di/dt of the current is higher than the bandwidth of the CVR. At this point, modelling the CVR with its resistive, inductive, and capacitive components becomes obligatory, in order to obtain the frequency dependency of the CVR. Figure 2.1b illustrates such an equivalent circuit with the ideal resistance R_{CVR}, the series inductance L_S, and the parallel capacitance C_P. Another issue with CVRs is the conflict of interest between resolution (R_{CVR} as large as possible) and interference of the original circuit (R_{CVR} as small as possible).

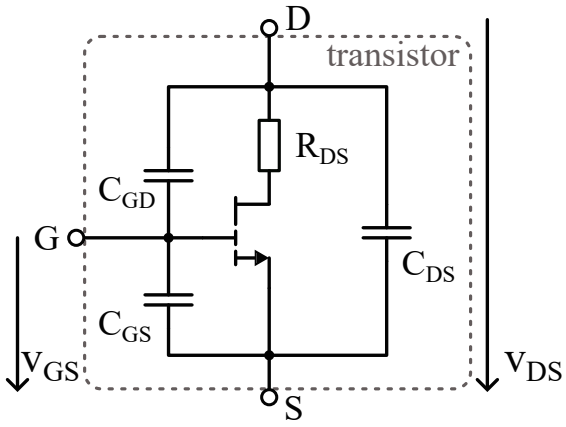


Figure 2.2.: Equivalent circuit of a GaN transistor depicting R_{DS}

Sometimes it is not even necessary to add a CVR to a circuit, when there is already a known resistive component in the circuit for a specific purpose, which can be used to measure v_{CVR} and calculate the current. R_{DS} of a transistor, shown in figure 2.2, can be used to obtain the drain-source current i_{DS}. When the transistors becomes conductive, R_{DS} becomes R_{DS-ON}. By measuring the voltage across drain and source v_{DS} and knowing the value of R_{DS-ON} as exact as possible, the current can be deduced. This method is dependent on the exact value of R_{DS-ON}. Because R_{DS-ON} is temperature dependent, using this method is a complex task. Finding precise values for R_{DS} can be done with the so-called pulsed IV-method, which is described in [25] but was not used in this thesis.

2.1.2. Electromagnetic induction

The physical phenomenon of electromagnetic induction can be used to measure currents because the flow of an electrical current creates a magnetic field, which induces a voltage in an adjacent conductor or semiconductor. The technologies based on the electromagnetic induction can be divided into two main sections, a) with magnetic cores and b) without magnetic cores. A concept of a simple current transformer is illustrated in figure 2.3, were a coil is wrapped around a core. This simple device is a current transformer and can be placed around a current carrying wire (red), through which the current I flows. This current creates the magnetic field B, which induces a current of size I/N in the measurement coil, where N is the number of turns of the coil.

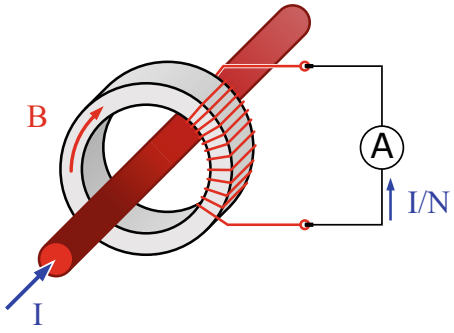


Figure 2.3.: Concept of a current transformer with a coil around a core, taken from [9]

Current transducers with magnetic cores are usually cheap but slow and therefore were not considered in this work. An exception is the closed loop flux-compensated current sensor. Magnetic techniques without core come in various forms.
Hall effect sensors usually use the deflection of flowing charge carriers like electrons in a semiconductor. They work very well in compact packages, feature good precision, and their bandwidth is relatively high but limited to several MHz. Current transformers with air cores are very fundamental in many applications, but are limited to AC currents and offer only a limited bandwidth. Rogowski coils extend the capabilities of air coil current transformers in the upper bandwidth region of several 100 MHz. Like a standard CT, a Rogowski coil has a self-resonance frequency of the sense winding, which intrinsically puts a limit to the bandwidth. Additionally, the primary side inductance of high frequency current transducers depends on the electromagnetic coupling factor. This leads to a parasitic inductance in the range of 10 nH...50 nH, which would be unacceptable for measurements at a GaN device, which has a typical package inductance of approximately 300 pH.

These limitations are very much dependent on the design of the coil, which led to the idea and development of the Infinity Sensor, which is one of the two main current sensing technologies covered in this work.

2.1.3. Faraday effect

Another magnetic phenomenon for current sensing is the Faraday effect, where the magnetic field rotates the circular polarization of light. Because this is a very subtle effect and polarization can't be measured easily, this technology has only been used for current sensing with very high currents in high voltage power distribution. Nevertheless, it will be mentioned in the outlook of this work, because future developments of this technique might be fruitful for power electronics as well.

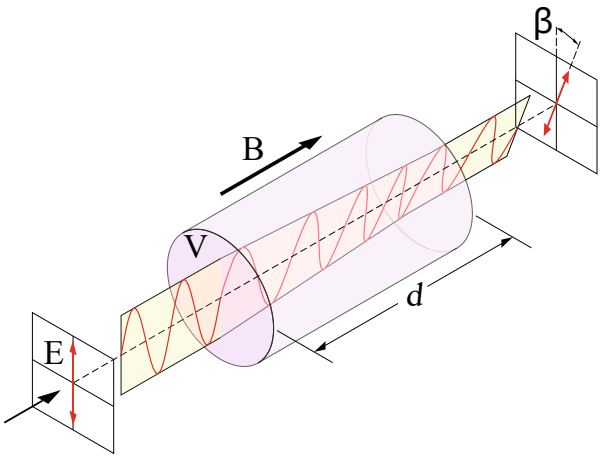


Figure 2.4.: Polarization rotation due to the Faraday effect, taken from [6], changed symbol of the Verdent constant to V

The Faraday effect describes the linear influence of the magnetic field B on the circular polarization of light, see figure 2.4. Equation 2.1 describes the relation between B and the change of the polarization angle β of light over a distance d. V is the Verdet constant, which describes the characteristics of the Faraday effect for a specific materials.

$$\beta = V\,B\,d \tag{2.1}$$

2.2. Current sensor technologies

2.2.1. Current sensor requirements

Accordingly, the next sections will cover technologies that are relevant for power electronic development and operation. For the specific purpose of this thesis, to measure currents with high bandwidth in the commutation loop (see section 3.2.7) of fast switching wide bandgap transistors, only two technologies are currently feasible; the CSR and the Infinity Sensor. The latter falls into the category of Rogowski coils. General requirements for sensors, but especially for the application in power electronics are:

- transfer function
  - preferably linear relation current → output signal
  - high sensitivity $v_{out}/i_{measure}$
- wide bandwidth
  - preferably starting at 0 Hz
  - reaching at least $2 \cdot f_{Signal}$
- low insertion impedance: influence current ← sensor as small as possible
- galvanic isolation
- thermal stability of the output signal
- high precision and resolution
- step response time
- physical size

2.2.2. Coaxial shunt resistor

A coaxial shunt resistor (CSR) is a special form of the more general family of so-called current-viewing resistors (CVR). CVRs offer a very simple and effective principle to measure currents by means of Ohm's Law, see equation (2.2).

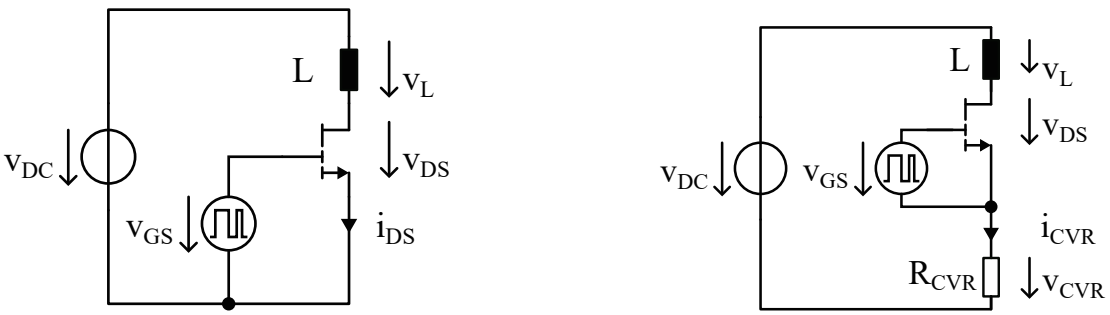
$$i_{CVR}(t) = \frac{v_{CVR}(t)}{R_{CVR}} \tag{2.2}$$

In order to measure the current $i_{DS}(t) = i_{CVR}(t)$ in figure 2.5a, the CVR is introduced to the current path between the transistor's source pin and the ground

path, figure 2.5b. Despite their simplistic character, CVRs have to be chosen carefully, because they are part of the commutation loop (see section 3.2.7). The main aspects to consider when choosing a CVR are:

1. added resistance in comparison to the impedance of the commutation loop
2. added inductance in comparison to the impedance of the commutation loop
3. bandwidth of the CVR
4. suitable size of measured signal v_{CVR}

The added resistance of the CVR will introduce the intended, measurable voltage v_{CVR} which corresponds to the current i_{CVR}, which is supposed to be equal to the actual current i_{DS}. Assuming that the supply voltage v_{DC} is provided by a controlled power supply, v_{DC} is constant and will be the same in both variants of the circuit in figure 2.5. In the example circuit, i_{DS} is dependent on $v_{DC} = v_L + v_{DS}$. Introducing the CVR into the circuit, figure 2.5b, the current through the transistor, i_{CVR} is different to i_{DS} because Kirchhoff's law claims that $v_{DC} = v_L + v_{DS} + v_{CVR}$. This leads to the conclusion that the last value v_{CVR} should be as small as possible, ideally $0\,\Omega$, in order to measure the true value of i_{DS} as precisely as possible. But there is a limit to this principle, because the size of v_{CVR} needs to stay in a suitable range of the measurement device with acceptable SNR of at least 45 dB, which is approximately the SNR of the used oscilloscope. This means that there is a fundamental trade-off concerning the value of R_{CVR}. The measurements taken for this thesis use a CVR as a reference for the Infinity Sensor. The chosen CVR has a nominal resistance of $50\,\mathrm{m}\Omega$. Assuming that the test currents in the DPT setup will be below 50 A, the maximum voltage at the CVR will be $v_{CVR} = 2.5\,\mathrm{V}$ at the maximum supply voltage of $v_{DC} = 400\,\mathrm{V}$. This means that the CVR contributes to roughly 0.625 % of v_{DC} in the voltage loop.



(a) Example circuit (b) Example circuit with CVR

Figure 2.5.: Working principle of CVR

Like every physical resistor, a CVR not only comprises of its ohmic resistance but also of its parasitic inductance and capacitance. The bandwidth of a CVR is limited by the composition of these aspects. There are ways to compensate these effects partially, e.g. by means of well adjusted RC-circuits. But these added components take up even more valuable space on the PCB, which is rarely suitable for tightly packed power electronics.

Pulse energy

The deposited pulse energy at a CVR can be calculated according to equation (2.3).

$$E_{CVR} = R_{CVR} \int i_{CVR}^2 dt \tag{2.3}$$

During a single double pulse test, the current through the CSR shows approximately the signal i_{DS} in figure 3.2. i_{DS} consists of two parts. Firstly, the current is linearly increased over the adjustable time t_I until the desired current i_{DS-max} is achieved. Secondly, the current is approximately constant at a value of i_{DS-max} over a duration of t_P. Most energy is deposited when i_{DS-max}= 60 A, t_I= 30 µs, and t_P= 2 µs. The resulting energy per DPT E_{DPT} is given in table 2.1 for the used CSRs. For the tests of this thesis, the DPT was performed with a frequency of 100 Hz, which means that the dissipated power at the CRS is $P_{continuous} = 100 \cdot E_{DPT}$. The table also shows the maximum rated power loss P_{max} which each of these CSRs can dissipate. E_{max} is the maximum energy the CSR can handle during a brief and single current event, during which the CSR is expected to experience a temperature rise of approximately 80 K and can not be reused until it reaches room temperature again. Comparing $P_{continuous}$ to P_{max} shows that the used CSRs operate far below their energy limit. For the facilitated DPTs, smaller CSRs with an wattage closer to $P_{continuous}$ would have been preferable, because smaller CSRs also come with less insertion inductance. An extended discussion on the suitability of CSRs for double pulse tests is given in [61].

Table 2.1.: Calculated pulse energy E_{DPT} during a single DPT, resulting continuous power loss $P_{continuous}$. Taken from the used CSRs data sheet [2], [3]: rated power loss P_{max}, and maximum rated energy E_{max}

Model	**Resistance**	E_{DPT}	$P_{continuous}$	P_{max}	E_{max}
SSDN-414-01	10 mΩ	432 µJ	43.2 mW	2 W	6 J
SSDN-414-05	50 mΩ	2.16 mJ	216 mW	2 W	2 J

2.2.3. Hall effect current sensor

The working principle of a Hall effect current sensor is shown in figure 2.6. The current i is sent trough a piece of conductor (blue) at which a perpendicularly orientated constant magnetic field (B), is present. When electrons move through this area, they experience a Lorentz force because of the presence of the magnetic flux B. The Lorentz force is given in equation 2.4

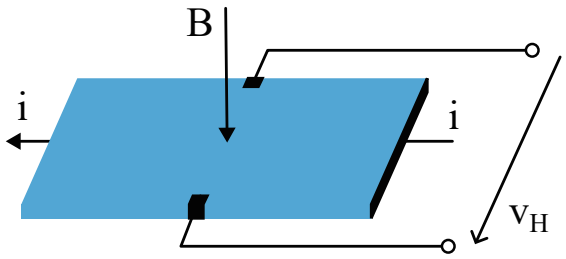


Figure 2.6.: Working principle of a Hall effect current sensor

$$\vec{F} = q(\vec{E} + \vec{v} \times \vec{B}) \tag{2.4}$$

Hall effect current sensors offer a bandwidth starting at DC and reaching up to several MHz. Subsequently, the Hall effect alone can't be used for high bandwidth current measurements at GaN transistors. The authors in [40] proposed a new approach for a high-bandwidth high-common-mode rejection ratio (CMRR) current measurement based on a Hall effect sensor for a 4.8 MHz GaN-inverter power source. There, different possibilities to combine low-frequency (LF) and high-frequency (HF) current sensors to cover the desired frequency spectrum are compared. The compared techniques and obtained results for the frequency response data are shown in table 2.2. The LF sensor in all combinations was the ACS733 Hall effect sensor IC by Allegro [38]. The ACS733 offers a bandwidth from DC to 1 MHz with a current range up to ±65 A and a sensitivity of 20 mV/A. The HF sensors to complement the LF Hall sensor were a PCB-integrated Rogowski coil [43], galvanically isolated inductor voltage sensing (IVS), and a current transformer (CT). Like shown in table 2.2, the Hall effect sensor was evaluated separately and in two combinations, Hall+IVS and Hall+CT. These combinations were simulated, built and tested by means of a vector network analyzer (VNA) and finally evaluated as part of a hardware demonstrator. The results of this evaluation are given in table 2.2 and show that the Hall effect current sensor on its own is capable of providing sensible measurements up to $f_x = 1\,\text{MHz}$, which is not sufficient for many WBG applications. Combining the Hall effect current sensor with the IVS offers a combined bandwidth of $f_x = 10\,\text{MHz}$.

Table 2.2.: Sensor bandwidth data for a combination of LF Hall effect sensors and HF CTs at a nominal sensitivity of 33 mV/A, taken from [40]

Sensor	$\mathbf{f_x}$	$\mathbf{f_{45°,x}}$	$\mathbf{f_{c,HF}}$	$\mathbf{f_{filt}}$
Hall only	1.4 MHz	490 kHz	N.A.	N.A.
Hall+IVS	10 MHz	8.2 MHz	350 Hz	15.2 kHz
Hall+CT	35 MHz	16.5 MHz	1 kHz	24.5 kHz

The IVS bandwidth has a LF-limit $f_{c,HF}$ of 350 Hz. The frequency for the cross-over filter f_{filt} of the combiner circuit 2.7 was set to 15.2 kHz. Best results were achieved when combining the Hall effect current sensor with the CT, providing an overall bandwidth of up to 35 MHz. The filter for the combiner circuit was set to $f_{filt} = 24.5\,\text{kHz}$ in this case, because the CT has a lower limit to its bandwidth of $f_{c,HF=1\,\text{kHz}}$. Despite the improved bandwidth, the sensor can't be used for the intended purpose of this thesis, because of its size and excessive high insertion impedance.

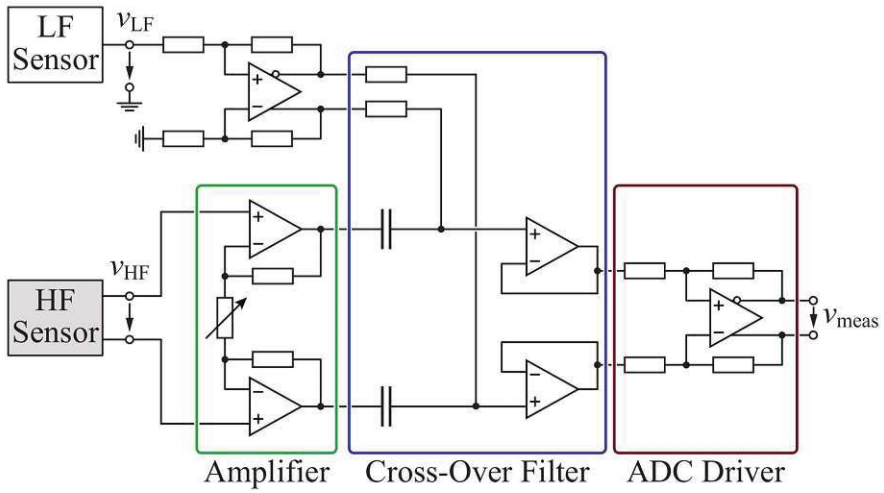


Figure 2.7.: Working principle of the fully differential combiner circuit, taken from [40]

2.2.4. Rogowski coil

In 1912 Walter Rogowski and Wilhelm Steinhaus published their article "Die Messung der magnetischen Spannung" [43], where they also describe the idea of the nowadays common and so-called Rogowski coil. Their technique allows to measure the AC current through a conductor by means of an isolated coil, which is flexible due to it's helical windings and non-metallic core. A sketch of the Rogowski coil's working principle is given in figure 2.8. The advantages of the Rogowski coil are the galvanically isolated measurement of the AC current and the mechanical flexibility of the coil, which allows to install the measurement coil at existing circuits without the need of interrupting the current carrying conductor. Because the helically wound coil does not feature a ferromagnetic core like traditional current transducers, the otherwise common problem of magnetic saturation of the core is eliminated. This also offers a high bandwidth of the Rogowski coil, which is usually limited by the mandatory integration circuitry, of which an example is conceptually shown as operational amplifier voltage integrator in figure 2.8. The main disadvantage of the Rogowski coil is the lower limit of bandwidth. Because the Rogowski coil measures the derivative of the current like shown in equation 2.5, the current signal requires the integration of $v(t)$ and thus the DC component is lost. Typical devices start at a minimum signal frequency of ∼100 Hz, like the CWT Ultra-mini of PEM UK [53].

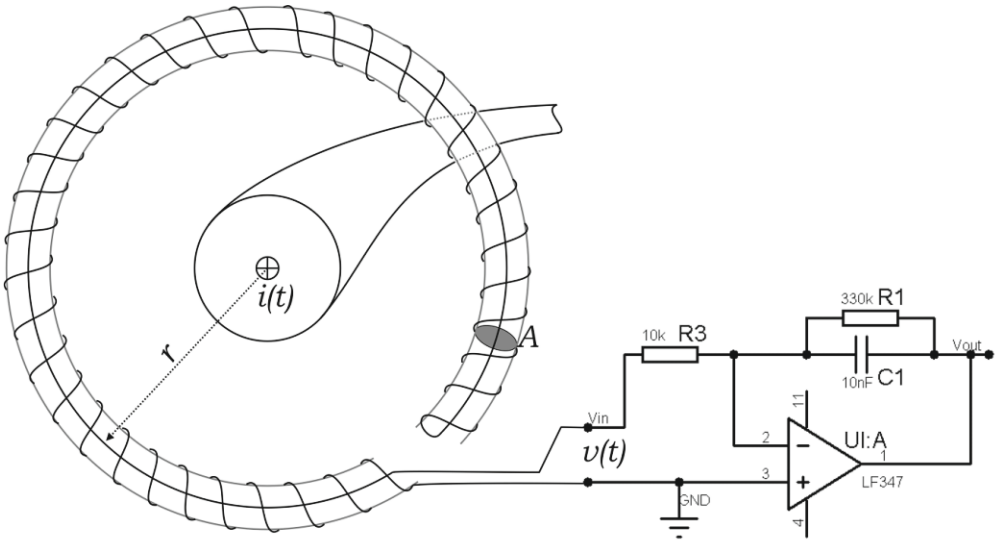


Figure 2.8.: Working principle of a Rogowski coil, taken from [8] CC BY-SA 3.0

$$v(t) = -\frac{AN\mu_0}{l}\frac{di(t)}{dt} \tag{2.5}$$

Equation 2.5 describes the induced voltage at the terminals of a Rogowski coil, shown in figure 2.8. A describes the cross-sectional area of the wound wire and N is the number of turns of the wire with cross section A. μ_0 is the vacuum magnetic permeability and $l = 2\pi R$ describes the length of the wound wire coil. $di(t)/dt$ is the derivative of the current $i(t)$ through the conductor which the Rogowski coil enfolds.

$$v_{out} = \int v(t)dt = -\frac{AN\mu_0}{l}i(t) + C \tag{2.6}$$

Because of $v(t)$ represents the derivative of the current $i(t)$, the coil output voltage must be integrated like shown in equation 2.6. v_{out} describes the integrated output signal of the amplifier in figure 2.8. Importantly, with the integration comes the integration constant C, which is unknown and represents the DC component of the measured current. This is a fundamental flaw of the Rogowski coil.

$$L_T = \mu_0 N^2 (R - \sqrt{R^2 - r^2}) \tag{2.7}$$

Equation 2.7 describes the inductance L_T of a toroid with an outer radius R and coil radius r and N number of turns.

2.2.5. Infinity Sensor

The Infinity Sensor was invented by the Electrical Energy Management Group at the Department of Electrical and Electronic Engineering of the University of Bristol [4]. The research group for high-bandwidth sensing for wide-band gap power conversion has been using the idea for this sensor, a flat, rudimentary Rogowski coil since 2016 on power electronic PCBs. Since then, this idea was transformed into a product, the Infinity Sensor, which is available in its second version.

Fundamental working principle

The Infinity Sensor version 2 is a planar, ∞-like trace (hence the name) on a 3 mm x 8 mm PCB, see figure 2.9 and 2.10. This PCB is divided into 3 sections. The middle section has a 3 mm wide copper trace on the bottom of the sensor with soldering pads on both sides. This copper trace carries the current i_{trace} to be measured by the sensor. The sensor is electrically and mechanically connected to the circuit of interest by soldering both of the sensor pads to the mother-PCB. On the top side of the middle section is the 50 Ω coaxial MHF4[5] signal output connector. Below run the traces of the sensor coils. As shown in figure 2.10, the two coils on opposite sides are electrically in series with each other. The left coil is wound clockwise and the right coil is wound counter-clockwise. At the center, there is a diagonal connection of two opposite pairs of the coil's wires. The other pair connects to the contact pads on the top of the sensor.

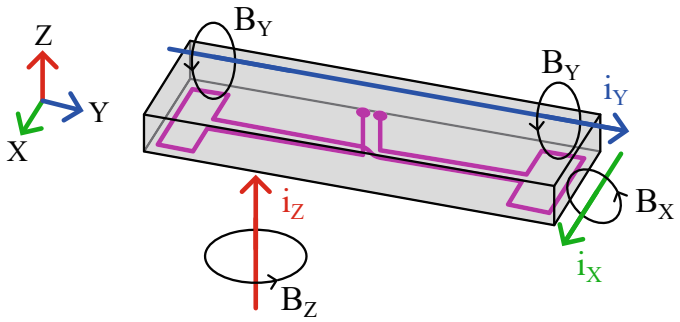


Figure 2.9.: Magnetic coupling of the Infinity Sensor coil with currents in X, Y, and Z directions, redrawn according to [56]

Like a Rogowski coil, the output signal of the Infinity Sensor v_s in equation 2.8 is the derivative of the current i_T multiplied by a constant M, which represents the mutual inductance between the coil and the current carrying copper trace below it. The integration constant I_0 is unknown, which poses a challenge when interpreting the output signal. A partial solution to this issue is presented in section 3.5.3.

$$v_S(t) = M\frac{di_T(t)}{dt} \tag{2.8}$$

$$i_T(t) = \int \frac{v_S(t)}{M}dt + I_0 \tag{2.9}$$

Table 2.3 lists the important electrical parameters of the Infinity Sensor V2. The usable frequency band is 3 orders of magnitude wide, ranging from 1 MHz to 1 GHz. Importantly, the sensitivity is highly dependent on the mechanical orientation and involved materials as well as the manufacturing tolerances of the double coils on the sensor. Therefore, the uncertainty of ∼8.2 % is relatively high.

Table 2.3.: Key parameters of the Infinity Sensor V2, taken from the data sheet [11]

Parameter	Value	Uncertainty
Sensitivity = 1/M	0.1 V/Ans	∼8.2 %
Low frequency cut-off (−3 dB)	1 MHz	-
High frequency cut-off (−3 dB)	1 GHz	-

The second version of the Infinity Sensor was drastically downsized compared to the prototype, compare figure 2.10 and figure 2.13. Version 2 is based on the small variant of version 1, and it's coils were scaled down even further. A bigger variant was dropped entirely. Besides the smaller size, the main advantage of the version 2 sensor is that the current carrying trace is now attached to the sensor bottom side, whereas version 1 was attached above the copper layer of the mother-PCB. By attaching the current trace directly, the distance between the current path and the coil can be manufactured more precisely and the sensor's characteristics are more reproducible.

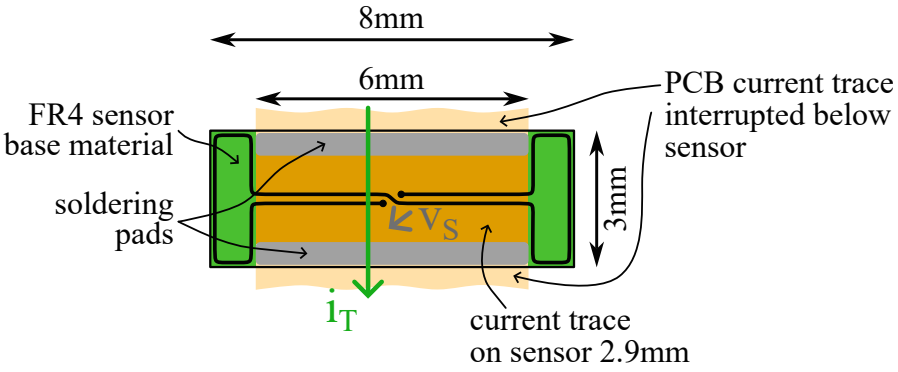


Figure 2.10.: Dimensions of the Infinity Sensor V2 [11]

Figure 2.10 shows the dimension and main features of the used Infinity Sensor V2. The solder pads for the current carrying copper trace also function as the mechanical attachment points to the mother-PCB. An image of the top and bottom side of the sensor is shown in figure 2.11 with the MHF4-connector on the top side, where the output signal v_S is attached to a coaxial cable.

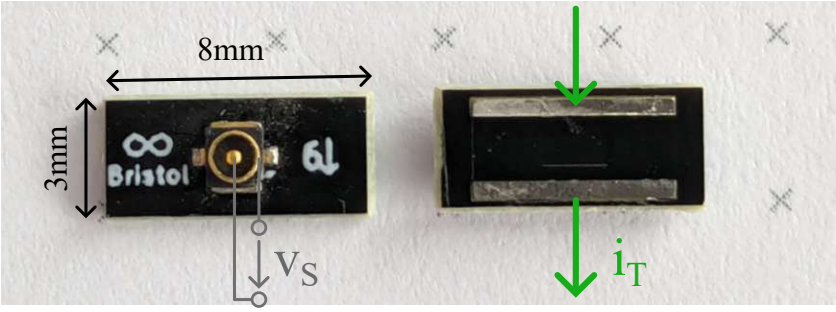


Figure 2.11.: Top and bottom view of the Infinity Sensor V2 [56]

Prototype

The first version of the Infinity Sensor was produced in two sizes which were both substantially larger than the V2 of the sensor. The dimensions of both sizes are given in figure 2.13. Both sensors had two small, electrically not connected pads for mechanical positioning by soldering (not shown in figure 2.13).

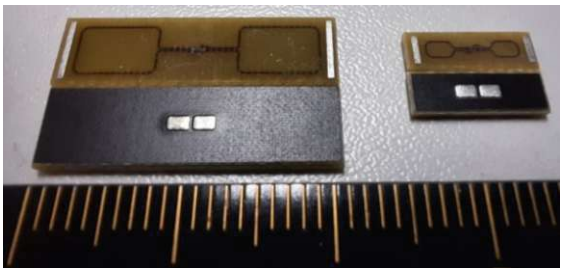
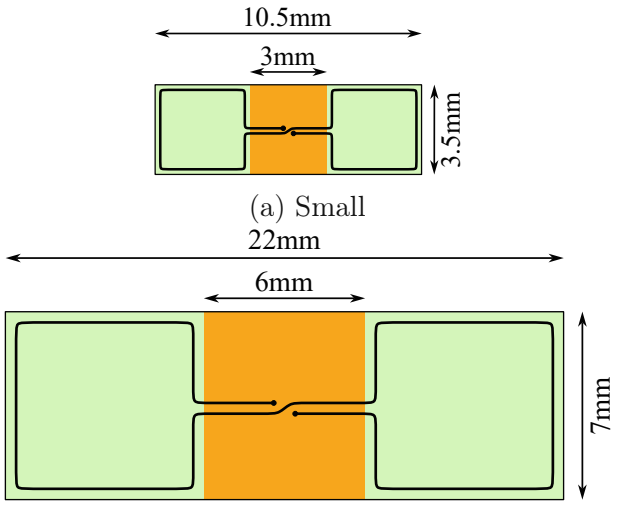


Figure 2.12.: Photo of Infinity Sensor version 1 large and small, top and bottom side



(a) Small

(b) Large

Figure 2.13.: Dimensions of the Infinity Sensor version 1

Application of the Infinity Sensor

The most common position for the Infinity Sensor's application is in the commutation loop, right after the source of the low-side transistor. For all PCBs produced for this thesis which include the Infinity Sensor, the sensor was located at this position, like shown in figure 2.14. The copper trace right after the source pad of the low-side GaN transistor Q_4 widens to connect with the return path of the gate driver and immediately afterwards connects to the Infinity Sensor V2 pad. The Infinity Sensor v1 had no electrical connection to the commutation path and was glued on top of the existing copper trace. This was advantageous if the PCB was also used without the sensor or if the usage of the sensor was not considered during the PCB design. The disadvantage of this method with the Infinity Sensor v1 was the small but significant error in the distance between the sensor coils and the copper trace on the PCB. Depending on the gluing method, silkscreen and solder stop thickness of the PCB, the distance between the current carrying copper trace and the sensor coil is difficult to determine. The Infinity Sensor v1 was hard to apply reproducibly.
The Infinity Sensor V2 solves this problem but requires the commutation loop to be interrupted for 2.9 mm, see figure 2.10. The current will be routed onto the sensor's current trace. This facilitated reproducible results when using the Infinity Sensor V2 on more than one PCB, the distance between the sensing coils and the current trace is smaller compared to V1, which results in better sensitivity and reduced size. Because the distance is fixed at the production process it can be manufactured small and reproducible.

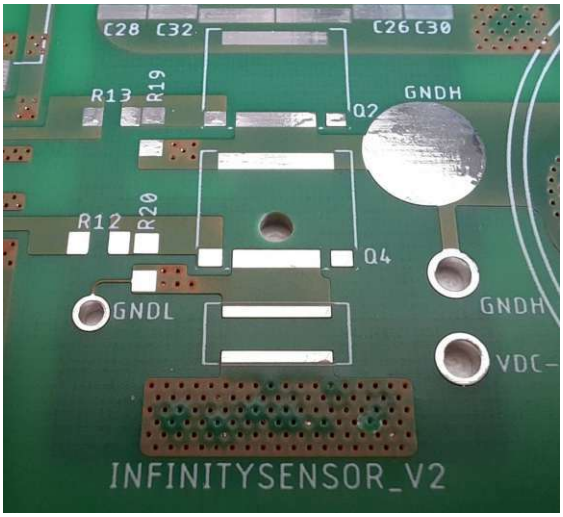


Figure 2.14.: Photo of the PCB layout to accommodate the Infinity Sensor V2

For voltages between the sensor pads and the MHF4-connector exceeding 250 V, a silicon sealant (K-704 by Kafuter) is recommended. This sealant was not used, because the Infinity Sensor was always located at the low-side source trace, where the negative pole of the 400 V PSU was connected and grounded (VDC- in figure 2.14). If the Infinity Sensor is used in different locations, like in the gate driver loop, on the high-side transistor, the usage of the silicone sealant is highly recommended.

2.2.6. Comparison

A discussion of several state of the art current sensor technologies, which are reasonable candidates for PCB integration is given in [56]. These technologies are listed in table 2.4, represented by some exemplary products on the market or published concepts of present day academia. The most relevant features for PCB integration in the context of GaN and SiC DPT are bandwidth, insertions inductance, and galvanic isolation.

Table 2.4.: State of the art current sensors comparison, taken from [56]

Current sensing device	**Band-width**	**Insertion**		**Power device**	**Galvanic isolation**	**Sensing in control circuit**
		resistance	**inductance**			
Split core current probe TCP0030A	120 MHz	0.85 Ω @ 120 MHz	>10 nH	SiC	Yes	No
Current transformer Pearson 2877	200 MHz	20 mΩ	N/A	SiC	Yes	No
Coaxial shunt SDN-414-10	2 GHz	100 mΩ	2 nH	GaN/ SiC	No	No
Virginia Tech SMD Shunt	N/A	100 mΩ	N/A	GaN	No	Yes
Cambridge SMD Shunt	100 MHz	100 mV @ I_{max}	300 pH	GaN	No	Yes
Planar Rogowski coil	100 MHz	N/A	N/A	SiC	Yes	Yes
Current sensor based on magnetic coupling	170 MHz	N/A	N/A	GaN	Yes	Yes
Infinity Sensor	225 MHz	4.2 mΩ	200 pH	GaN/ SiC	Yes	Yes

The comparison shows that the Infinity Sensor provides the lowest insertion impedance of the compared products while also featuring galvanic isolation and high bandwidth. The only downsides of the Infinity Sensor, which are not noted in table 2.4, are the lack of its DC-capability and the necessary post processing of its measurement signal.

2.3. Voltage measurement

The voltage measurements facilitated for this thesis were solely done with a modern digital storage oscilloscope (DSO), the MSO58 of Tektronix [19]. The core technology of DSOs are high speed analog to digital converters (ADC), which translate an analog signal to digital information at a sampling rate high enough to satisfy the Whittaker-Nyquist-Shannon theorem, see section 3.3.2. The data sheet of the MSO58 and online resources do not mention which type of ADC is implemented, but the most common ADC architectures for DSOs are the so-called Flash-ADC and Pipeline-ADC. Details to the voltage measurements done for this thesis can be found in section 3.3.2.

3. Methodology

This chapter addresses the chosen methods to evaluate the high bandwidth current measurement of the Infinity Sensor and one of the state of the art current measurements techniques, the coaxial shunt resistor. In order to do so, the double pulse test, a common procedure [31] to assess the switching behaviour of power semiconductors is chosen. This is an obvious choice, because the DPT is an existing tool of power converter design and development and thus the main field of application for the Infinity Sensor and CSR. As discussed in the outlook chapter 6, two improved techniques were proposed in [32] and [15], in which the DPT evolves into the so-called N-pulse test (NPT) and a pulse width modulation ramp (PWM ramp). For this thesis, the scope was limited to the established DPT. A set of PCBs was developed based on existing concepts of [35], to accommodate the CSR and Infinity Sensor. The PCB design was done with the PCB development suite Eagle and included several iterations until the final PCB for measurement was ready. During the design and testing loop, the earlier prototype version 1 of the Infinity Sensor was replaced by the now available Infinity Sensor V2. The conducted DPTs have specific requirements for the rest of the measurement system, which will be discussed in this chapter as well as the post processing of the acquired data.

3.1. Double pulse test

In order to evaluate the capabilities and limitations of a power semiconductor, especially during switching, it is common to facilitate a double pulse test DPT, see [15]. The DPT has become a common test procedure to evaluate semiconductor switching devices [31]. The DPT offers the advantage of testing the transistor as the device under test (DUT) in a simplified setup before the implementation in a fully-fledged power converter. Despite the simplified test setup, the DPT is designed in a way that allows to gain findings about the transistor and its driver implementation. The DUT can be operated at currents and voltages like in the full power converter, but without the need to actually run a complete device at full output power. A simplified schematic of an exemplary DPT setup is illustrated in figure 3.1. Generally, the DPT represents a half-bridge inverter, where one of the two switches, usually the high-side, is bypassed by an inductor. For the

correct operation of the DPT, the bypassed switch needs to conduct current in reverse direction, see figure 3.1 phase 2. When testing MOSFETs, the intrinsic body diode covers this function. If an IGBT is to be tested, the IGBT needs to be either reverse conductive or an external diode for reverse conduction must be added externally. GaN devices are HEMT and do not comprise a physical body diode like MOSFETs. Under the right conditions they are conductive in reverse direction and operate like a diode with additional forward voltage depending on the gate driver turn-off voltage. The reverse conduction of GaN devices is described in detail in the data sheet [52] and various articles like [50]. The DPT was initially used for Si-based BJTs and IGBTs. [15] discusses if the DPT is still an adequate method to determine electrical characteristics of GaN devices. An adapted DPT method with N pulses instead of double pulses is proposed in the outlook. Another method for measuring the switching losses of power semiconductors is calorimetry. This method is increasingly used although the effort higher and the overall process is slower.

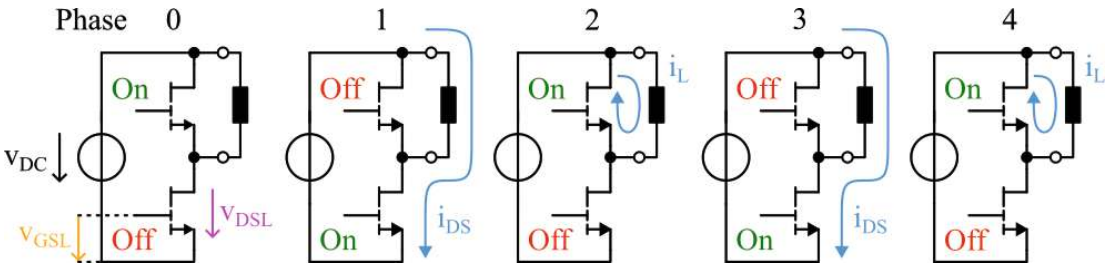


Figure 3.1.: Simplified circuit phases of a DPT

Figure 3.1 depicts the simplified circuit of the DPT. The relevant components, two GaN transistors in a half-bridge configuration, an inductor, and the DC power supply are shown. The half-bridge is supplied by a DC source with v_{DC}. The gates of the high-side and low-side GaN transistors are driven by a dedicated, isolated gate driver-IC, which is omitted in this picture for simplicity. Nevertheless, the gate driver voltage of the low-side and the state of both GaN transistors are annotated to describe the function of the gate driver-IC during the DPT. The inductor is connected in parallel to the high-side GaN transistor and is a component specifically added for the DPT to the otherwise standard half-bridge. The inductor acts as an energy storage with integrating characteristics.

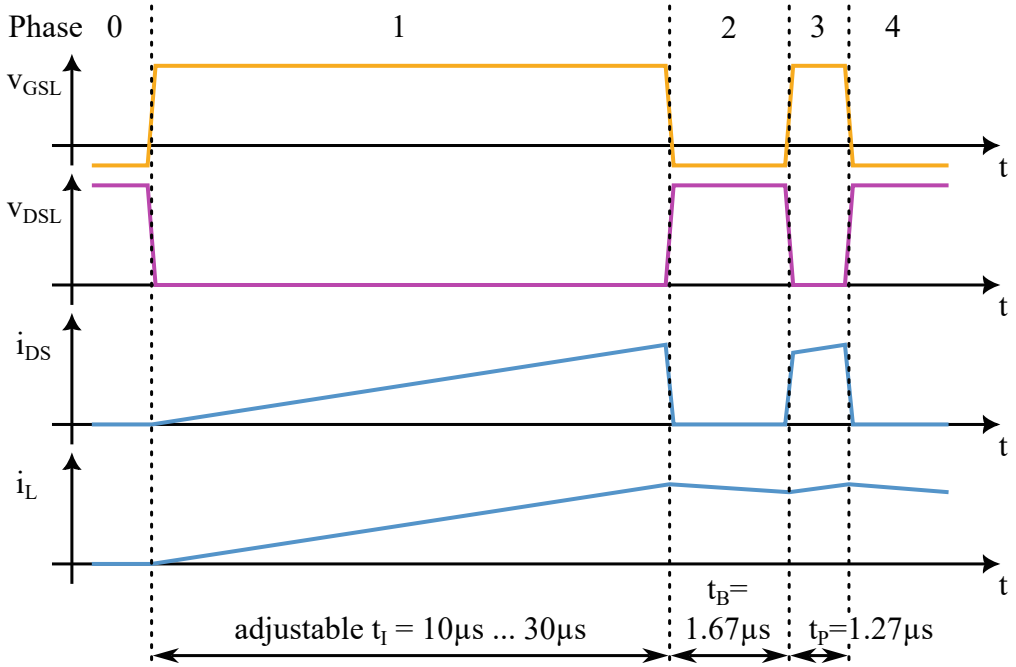


Figure 3.2.: Chronological phases of a DPT

A single DPT consists of 5 phases, as shown in the simplified schematic in Figure 3.1. Figure 3.2 shows the corresponding signals involved. Before the DPT starts, both GaN transistors are switched off and v_{DC} is switched on. Once the whole circuit is ready, the gate drivers become active. Once the gate drivers are active, phase 0 is established and the GaN transistors are always switched in alternating states. Subsequently, when entering phase 0, the high-side GaN transistor will be switched on and the low-side will remain off. How the gate drivers are triggered and operate is explained in detail in figure 3.20.

- Phase 0 of the DPT is the precondition where no current will flow through the switches and the inductor. This is the idle state of the DPT and the circuit is waiting for the external trigger signal to switch to the next phase. $v_{DSL} = v_{DC}$ during this state, because the low-side GaN transistor blocks the entire supply voltage.

- On entering phase 1, the GaN transistors both switch states and current is allowed to flow through the inductor and the low-side transistor. Because of its time dependent nature, the inductor acts as an integrator, see equation 3.1 and 3.2. During phase 1, the current i_L is increased by a linear rate, defined by the value of L, see equation 3.4 and figure 3.3.

- After phase 1, phase 2 is started when the transistors switch states again

and the low-side GaN starts blocking, while the high-side switch is able to conduct current in reverse direction. This is a break phase, where the before integrated current i_L is maintained and continues to flow through the inductor and the high-side transistor.

- On entering phase 3, both transistors switch states once again. The preserved current iL becomes the testing current step for the low-side transistor. This is the second, actual testing pulse of the DPT. Phases 0, 1, and 2 were necessary to prepare the full testing current for the second pulse in phase 3. i_L becomes the drain source current i_{DS} of a fully functional power converter for the low-side transistor. By adjusting the integration time in phase 1, which is the duration t_I of the first pulse, the current for the second pulse step can be adjusted. The timing is shown in figure 3.2. t_I is usually adjusted in a range between 10 µs and 30 µs to achieve the corresponding current values according to figure 3.3. The break time t_B is fixed at 1.67 µs as well as the fixed duration of the second pulse $t_P = 1.27$ µs.

- Phase 4 is reached after the second pulse in phase 3, the switch states of the transistors alternate one last time and the current i_L decays over a longer period of time until the next DPT is started.

As can be seen in figure 3.2, the current does not stay constant in phase 2, but decays due to the fact that both the inductor and the high-side transistor have low but non-zero resistance, which define the rate at which the energy is dissipated.

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{3.1}$$

$$i_L(t) = \int v_L(t)dt + I_0 \quad \text{and} \quad I_0 = 0\,\text{A} \tag{3.2}$$

In summary, during a DPT, the first of the two pulses is used to ramp up the current to a certain, desired test current for the second pulse. During the first pulse, the inductor acts as an integrator, see equation 3.2. This relation was used to calculate a rough estimation of the required on-time of the first pulse. Equation 2.8 can be simplified and transformed to 3.3. With an air core inductor of i_{CVR} $L = 810$ µH and voltages from $v_L = 100\,\text{V}...400\,\text{V}$, current ramps can be achieved based on adjusting the integration time t_I in figure 3.3. After t_B=1.67 µs (phase 2), the second pulse is started, now with a steep current ramp and the full DC voltage v_{DC}, simulating a real switching process with adjustable current.

$$\Delta t = L\frac{\Delta i}{u_L} \tag{3.3}$$

$$\Delta i_L = u_L \frac{\Delta t}{L} \tag{3.4}$$

After each DPT, the test setup is left to wait for the next DPT to be triggered. During this time, all components can cool down again and the next triggered DPT starts with the same conditions. In the chosen test setup, the function generator triggers the DPT periodically with a frequency of 100 Hz. Hence, the tested transistor on the low-side has time to cool down after each DPT cycle and the power losses can dissipate to the ambient air. This helps finding the right settings and dimensions of the driver loop and commutation loop components, while avoiding the thermal destruction of the transistor due to too high power losses of a non-optimized circuit. In a real power converter, switching processes would occur with much higher frequencies of 10 kHz and more, depending on the required input and output voltage of the power converter. Therefore, the DPT is an important tool of power converter development which allows for testing transistors in unknown conditions without destroying them each time.

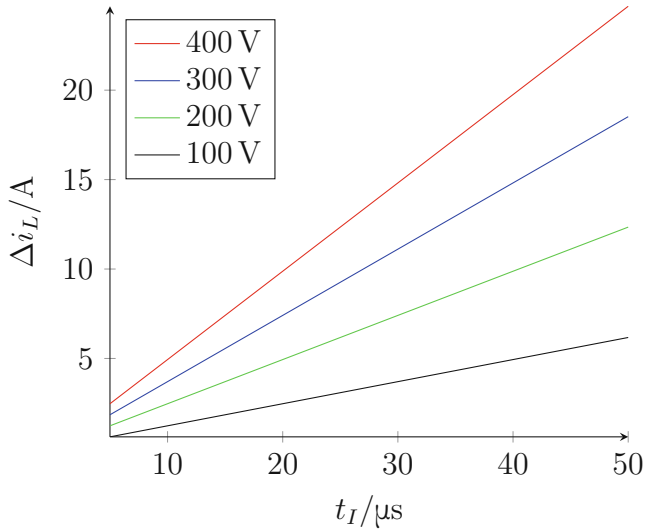


Figure 3.3.: Achieved current ramps Δi_L depending on the DC voltage v_{DC} and the duration Δt of the first pulse

3.2. PCB design for the double pulse test

The design of a PCB is split in two main parts, the schematic and layout. The design of the schematic with mostly abstract symbols for the required electronic components and component values is the first step from an idea to the actual PCB. After the electronic circuit has been defined in the schematic, a corresponding layout is designed based on the schematic. For this thesis, the schematic and layout design software Eagle ©Autodesk [17] was used. Eagle is an affordable software package, located somewhere between hobbyist and professional software. The schematic of the DPT PCBs in this thesis was drawn from scratch with Eagle, but was based on an earlier design from September 2019 by Sumanta Biswas and Markus Makoschitz [35], designed with the professional PCB design software package OrCAD ©Cadence Design Systems [18].

3.2.1. PCB layer stack

These PCBs are made from FR4 carrier material with 4 copper layers. The total thickness of the PCBs is 1.76 mm and each copper layer was produced with a thickness of 70 µm, which is twice as thick as the 35 µm standard copper layers. The extra thick copper layers were chosen to further decrease the parasitic inductance of the commutation loop and to increase the ampacity as well as the thermal conductivity of the PCBs. The details of the layer composition of the PCBs are illustrated in figure 3.4.

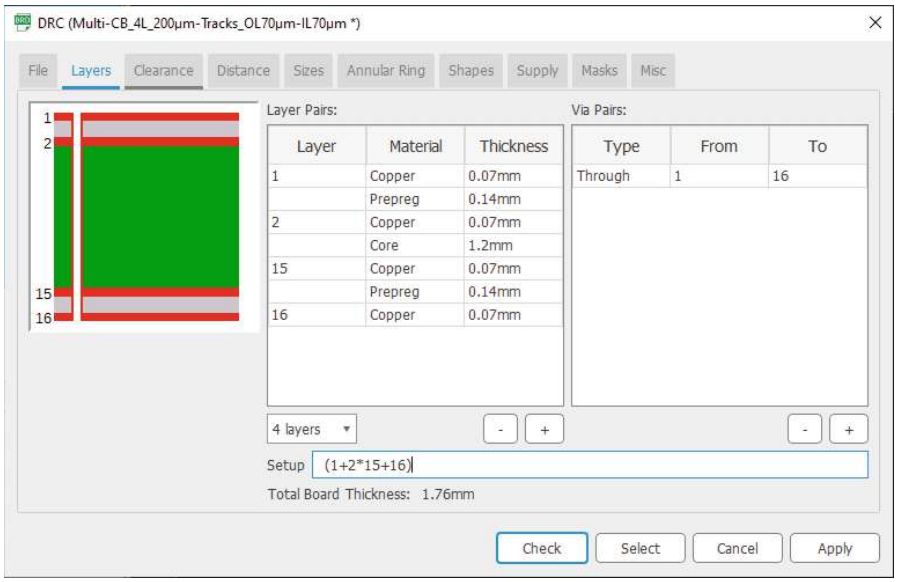


Figure 3.4.: Layer setup of all produced PCBs

3.2.2. Schematic

A schematic for the DPT PCB was drawn in the Eagle Schematic Editor. After several iterations, the final version for this thesis was produced in four different variations, but only the most representative schematic with a combination of the Infinity Sensor V2 and the CSR is displayed in figure 3.5.

Table 3.1.: List of final schematics and PCBs

Name	Sensors
GaN DPT V4 2022-11-15 Infinity	Infinity Sensor V2
GaN DPT V4 2022-11-15 Coax	CSR
GaN DPT V4 2022-11-15 Combo	Infinity Sensor V2 + CSR
GaN DPT V4 2022-10-28 SMD*	SMD-Shunt

*no measurements, see future work chapter 6

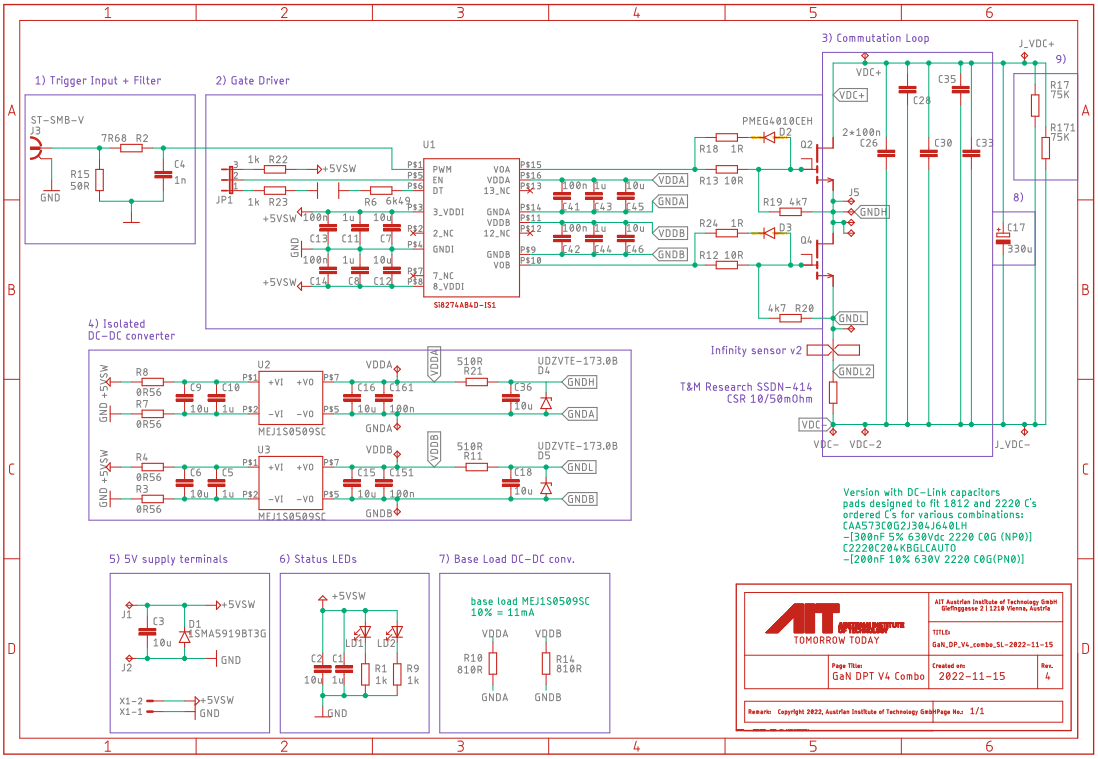


Figure 3.5.: Schematic of the DPT PCB with Infinity Sensor V2

3.2.3. Trigger input, DC capacitor and discharge resistors

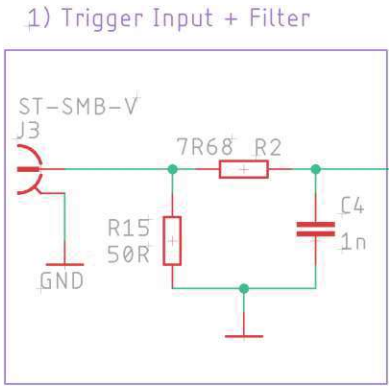
Figure 3.6a shows the J_3 SMA-connector, which is used to supply the DPT PCB with the external trigger signal, provided by the double pulse generation-PCB, described in section 3.2.8. The coaxial line is terminated by the 50 Ω resistor R_{15}. R_2 and C_4 act as a low pass filter, to cut off any signals with frequencies higher than 20.723 MHz, see 3.5 and 3.6.

$$\tau_C = R_2 C_4 = 7.68\,\Omega \cdot 1\,\text{nF} = 7.68\,\text{ns} \tag{3.5}$$

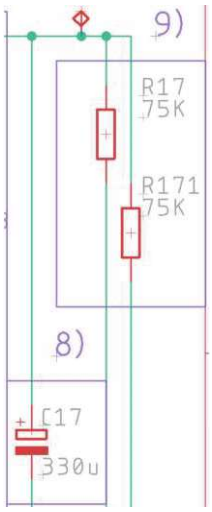
$$f_C = \frac{1}{2\pi R_2 C_4} = \frac{1}{2\pi \tau_C} = 20.7\,\text{MHz} \tag{3.6}$$

Figure 3.6b shows the electrolytic capacitor C_{17} which buffers the DC supply voltage of the commutation loop v_{DC} and the discharge resistors R_{17} and R_{171}. These resistors guarantee that the capacitors of the commutation loop will be discharged to 1 % after 61 s, equal to 5 τ_{DC} (equation 3.7) as soon as v_{DC} is disconnected. These resistors were used purely for safety reasons and would normally not be part of a half-bridge.

$$\tau_{DC} = \frac{1}{\frac{1}{R_{17}} + \frac{1}{R_{171}}} C_{17} = 37.5\,\text{k}\Omega \cdot 330\,\mu\text{F} = 12.375\,\text{s} \tag{3.7}$$



(a) Trigger input and low pass filter



(b) DC capacitor and discharge resistors

Figure 3.6.: Details of the schematic for the DPT PCB V4 with Infinity Sensor V2 and CSR in combination

3.2.4. Isolated DC-DC converters

To supply the dual gate driver U_1 for the high-side and low-side transistors with an isolated DC voltage of 9 V, two isolated DC-DC converters U_2 and U_3 were used. These are MEJ1S0509SC of the manufacturer Murata [39], which offer galvanically isolated conversion of the 5 V DC-supply to 9 V for each driver circuit. These were specifically manufactured for gate drivers and offer a high-potential DC isolation of 5.2 kV as well as a high common-mode transient isolation (CMTI) of >200 kV/µs. The latter is especially important for fast switching gate drivers with high voltages and current transients on the commutation side.

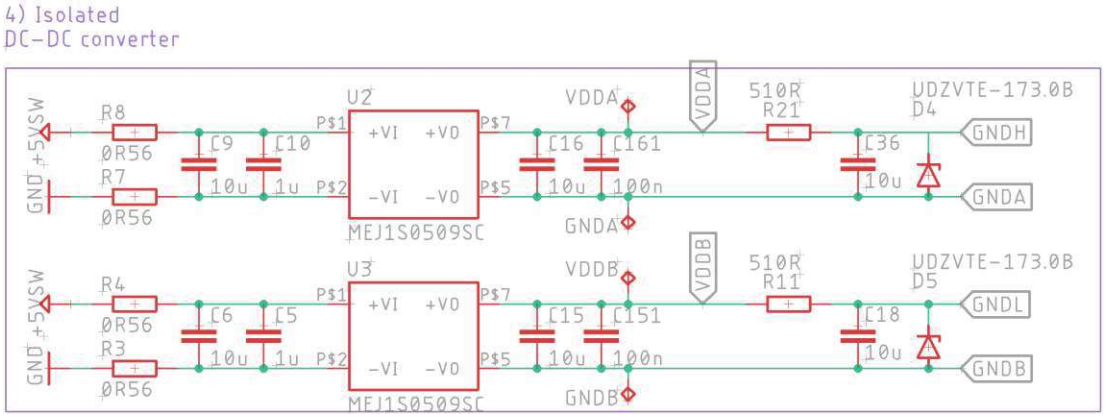


Figure 3.7.: Schematic detail of the DC-DC converters for the high and low-side driver

The DC-DC converters are supplied by the 5 V external power supply. For each converter two buffer capacitors with 10 µF and 1 µF are placed very close to the input pins to provide enough energy during switching. The same goes for the output pins, where an additional 100 nF capacitor is used to cover even faster switching surges parallel to another combination of 10 µF and 1 µF buffer capacitors for the 9 V output voltage. The isolated output voltages of 9 V VDD_A and VDD_B relative to GND_A and GND_B are supplied to the driver IC. Additionally, GND_H and GND_L are connected to the source pins of the high-side and low-side GaN transistors, see subsection 3.2.6. By providing two GND-reference potentials to the gate voltage V_{GSH} and V_{GSL}, separated by a 3 V Zener diode, the GaN transistors can be switched on by the driver with 6 V and switched off with −3 V. This allows faster clearing of the gate capacity and locks the off-state, preventing unintentional switching caused by fast current transients close-by, see subsection 3.2.6 where the driver loop will be described. To provide the reverse gate voltage of −3 V, Zener diodes D_4 and D_5 are used. Their type is UDZVTE-173.0B of the manufacturer ROHM, which feature a Zener voltage of 3 V and a maximum power

dissipation of P_D=200 mW. To guarantee that P_D is not exceeded, series resistors R_{21} and R_{11} with a resistance of 510 Ω are used. Both Zener diodes are buffered by 10 µF capacitors C_{36} and C_{18} in close proximity.

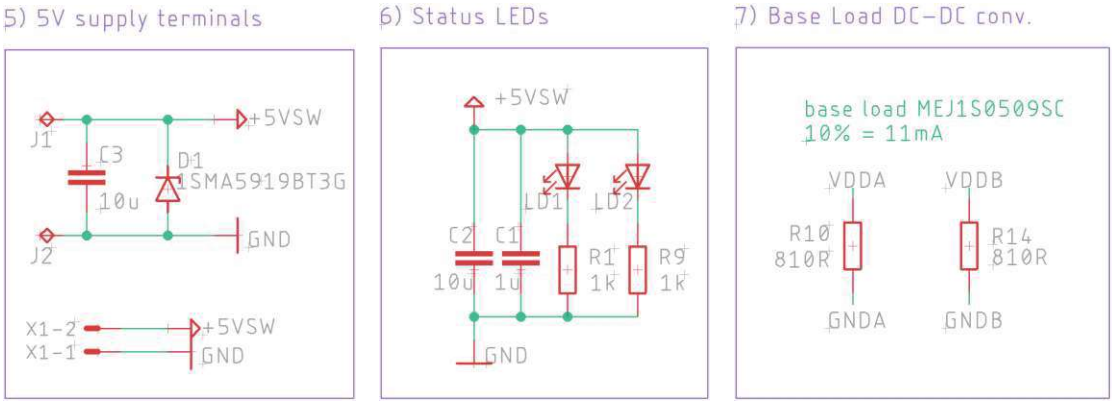
$$i_Z = \frac{VDD_B - GND_L}{R_{11}} = \frac{6\,\mathrm{V}}{510\,\Omega} = 11.76\,\mathrm{mA} \tag{3.8}$$

The series resistors R_{21} and R_{11} are dimensioned statically, when the driver IC is not consuming any current at GND_H and GND_L. In this situation, the Zener diodes will consume the Zener current i_Z of 11.76 mA which can be calculated like shown in equation 3.8. Accordingly, the actual power dissipation p_Z of the Zener diodes can be calculated in equation 3.9 and is well below the maximum rated P_D=200 mW.

$$p_Z = u_Z\, i_Z = 3\,\mathrm{V} \cdot 11.76\,\mathrm{mA} = 35.3\,\mathrm{mW} \tag{3.9}$$

3.2.5. Supply, status and base load

Figure 3.8a depicts the supply terminals, where the external 5 V PSU is connected either to the 4 mm safety connectors J_1 and J_2 or to the quick connector X_1. A 10 µF buffer capacitor C_3 is used close to the terminals as well as a protective diode D_1 in reverse direction.



(a) Supply driver side (b) Status LEDs (c) Base load of the DC-DC converters

Figure 3.8.: Details of the schematic for the DPT PCB V4 with Infinity Sensor V2 and CSR in combination

Figure 3.8b shows the status LEDs LD_1 and LD_2 with their series resistors R_1 and R_9. They indicate the presence of the 5 V supply on both sides of the PCB.

C_1 and C_2 are additional buffer capacitors for the 5 V supply voltage with 1 µF and 10 µF.

Figure 3.8c depicts base load resistors for the MEJ1S0509SC DC-DC converters. According to their data sheet [39], they operate accurately upwards from at least 10% of their 110 mA maximum load. The resistance for R_{10} and R_{14} was chosen to be 810 Ω, well below the calculated value of 818.2 Ω in equation 3.10.

$$R_{10} = \frac{VDD_A - GND_A}{i_B} = \frac{9\,\text{V}}{11\,\text{mA}} = 818.2\,\Omega \tag{3.10}$$

3.2.6. Driver loop

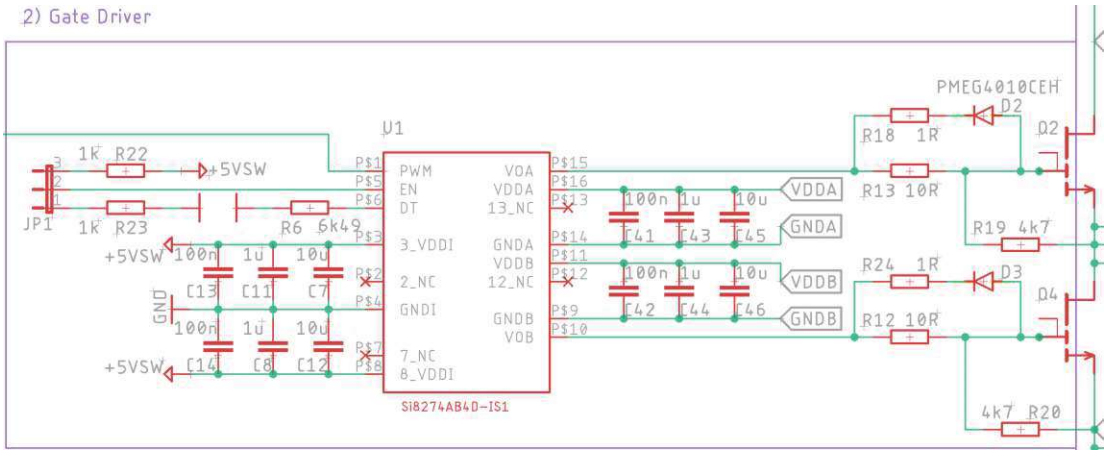


Figure 3.9.: Simplified schematic of the half-bridge PCB with focus on the GaN transistor drivers

$$t_{DT} = 2.02\,\text{ns} \cdot \frac{R_6}{1\,\text{k}\Omega} + 7.7\,\text{ns} = 2.02\,\text{ns} \cdot 6.49 + 7.7\,\text{ns} = 20.88\,\text{ns} \tag{3.11}$$

Figures 3.10 and 3.11 show simplified schematics of the low-side gate driver circuit during the ON- and OFF-state. Additionally to figure 3.9, the DC-DC power supply for the low-side is shown as well. U_3 is the isolated DC-DC converter, which supplies the 9 V for the driver IC U_1 and is fed by the 5 V supply of the PCB. The high-side DC-DC converter and gate driver circuitry is omitted for simplicity, but uses the same dimensions and thus works the same way as the low-side driver. C_{15} buffers the VDD_B output voltage of U_3. D_5 is a Zener diode, with an operating point adjusted by R_{11} and the Zener voltage is buffered by C_{18}, details illustrated in section 3.2.4. U_1 is shown with simplified internal components, where the trigger input signal is connected to the PWM pin. The signal is transferred to the high side driver via an AND gate, where the second input pin is the EN enable pin of

the IC but is omitted as well for simplicity. The low-side driver receives the trigger signal via its own AND gate, but the PWM trigger signal is negated. The output signal of the logic gates are passed through a galvanically isolated section of the IC to the output drivers of U_1. These output drivers are supplied by their own isolated DC-DC converters U_2 and U_3, described in section 3.2.4. Focusing on the low-side, the output driver of U_1 used VDD_B and GND_B and when activated, the current flows in a route across R_{12} and R_{20}, indicated by the green arrow in figure 3.10. Because the source of the low-side GaN transistor Q_4 is connected to GND_L and GND_L is connected at the Zener diodes cathode, the gate driving voltage during the ON-state is 6 V. By introducing D_3 and R_{24} the gate driver circuit allows asymmetric current paths for the ON- and OFF-state. During the ON-state, current from the gate driver can only flow through R_{12} (10 Ω), but through R_{12} (10 Ω) and R_{24} (1 Ω) during the OFF-state, see red arrow in figure 3.11.

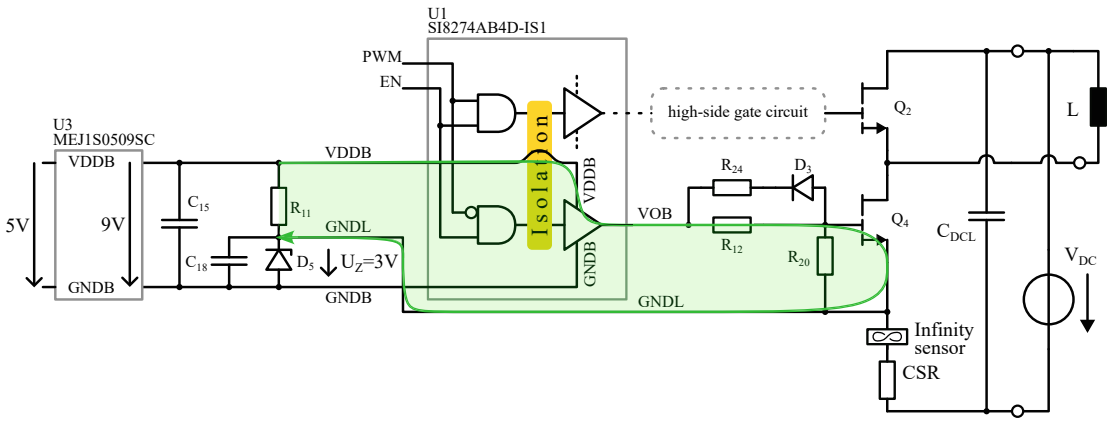


Figure 3.10.: On-state of the low-side driver loop, simplified schematic

D_3 allows to adjust the speed of the ON- and OFF-switching processes individually. When switching on, the current is limited by the 10 Ω of R_{12}. When switching off, the current is approximately limited by the 909 mΩ parallel resistance of R_{12} and R_{24} for the shown configuration in figure 3.9. The PCB was designed in such a way that R_{12} and R_{24} can be changed quickly and comparative measurements were done with different resistance values of R_{12}. Nevertheless, these measurements were not extensive enough for conclusions and thus are not included in this thesis. A detailed analysis of the different transient switching behaviours will be part of future work.

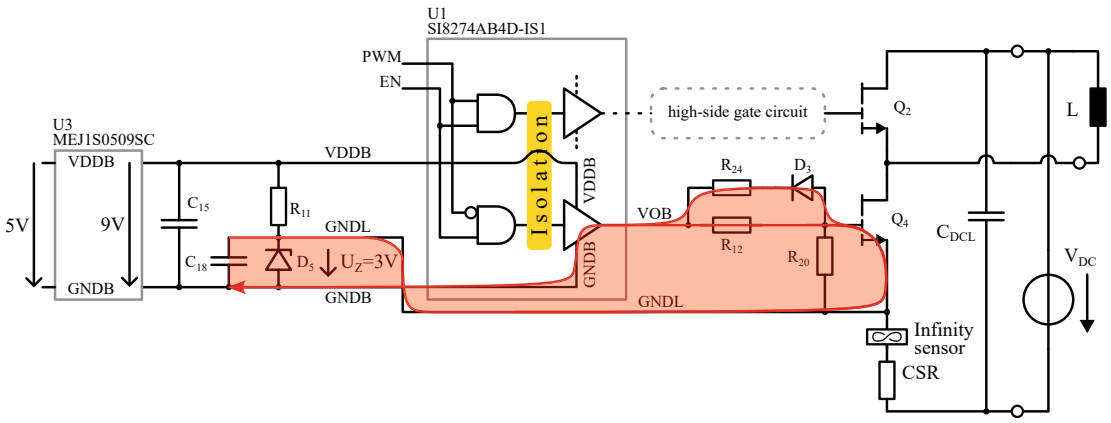


Figure 3.11.: OFF-state of the low-side driver loop, simplified schematic

However, there is a crucial difference between the ON- and OFF-state, determined by the fact that the D_5 Zener diode clamps v_{GS} to 6 V during the ON-state and to −3 V during the OFF-state. The negative voltage at v_{GS} offers an effective measure against accidental activation of the low-side transistor when it was just switched off and the high-side transistor is already conductive. Such an unintended activation would result in a fatal short circuit of the DC voltage v_{DC}. During such an event, both transistors would realise their ON-resistance R_{DS-ON} of 25 mΩ at the same time. The resulting short circuit current i_{sh} calculated in equation 3.12 to be approximately 8 kA would destroy both transistors.

$$i_{sh} = \frac{v_{DC}}{R_{DS-ON} + R_{DS-ON}} = \frac{400\,\text{V}}{50\,\text{m}\Omega} = 8\,\text{kA} \tag{3.12}$$

The negative OFF-voltage of −3 V, provided by the Zener diode of the gate driver circuit helps preventing accidental short circuits when the low-side GaN transistor must be switched off while the high-side transistor is switched on and vice versa.

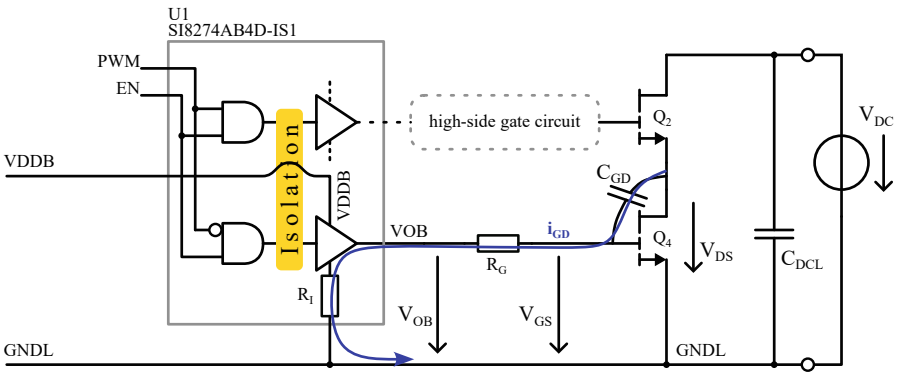


Figure 3.12.: Simplified schematic with parasitic gate-drain capacitance of the low-side GaN transistor

Specifically, such an unintentional switching could happen because of parasitic activation of the transistor when the transient of dv_{DS}/dt is high enough to overcome the threshold V_{th} of the gate-source voltage v_{GS} of the GaN transistor. The threshold voltage V_{th} of the used GS66516T GaN transistor by GaN Systems is typically 1.7 V but can be as low as 1 V, according to the data sheet [52]. The involved parasitic capacitance C_{GD}, also called reverse transfer capacitance C_{rss}, has a value of 5.9 pF and is shown in figure 3.12. R_G is the total resistance of the gate driver, R_I is the internal resistance of the gate driver.

$$i_{GD} = C_{GD}\frac{dv_{DS}}{dt} \tag{3.13}$$

When a switching process occurs, dv_{DS}/dt becomes $>0\,\mathrm{V\,s^{-1}}$ and a transient parasitic current i_{GD} from drain to gate will flow through C_{GD}, R_G, and R_I. The value of the i_{GD} is directly proportional to C_{GD} and the rate of change of v_{DS}, see equation 3.13.

$$v_{GS} = i_{GD}(R_G + R_I) \tag{3.14}$$

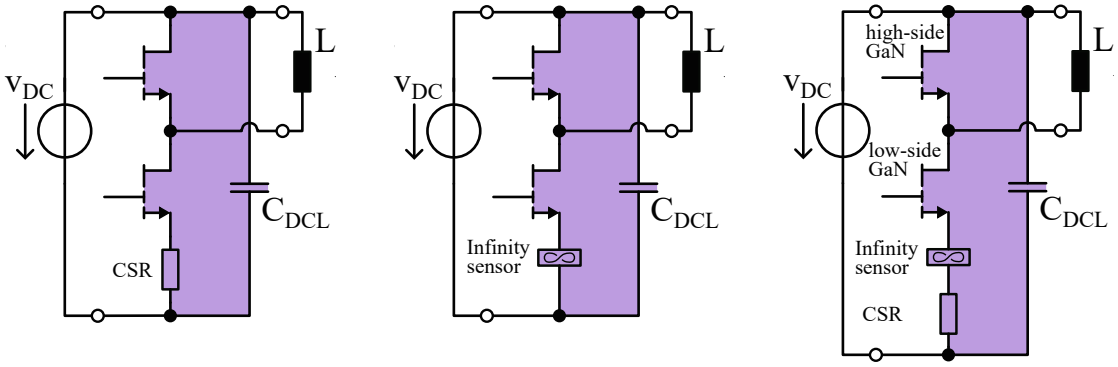
This current will cause the gate-source voltage v_{GS} to rise to a value which is proportional to $(R_G{+}R_I)$, illustrated in equation 3.14. As soon as v_{GS} rises above V_{th}, the GaN transistor will switch on. By offsetting the GND reference voltage of the gate driver GND_B by -3 V relative to $GNDL$, like shown in figure 3.11, the parasitic rise of v_{GS} will not be able to reach the threshold V_{th} and thus effectively prevents parasitic switching.

3.2.7. Commutation loop

The commutation loop of a power converter PCB is a critical area in terms of resistance and inductance. Figure 3.13a shows a simplified schematic of a half-bridge configuration. The commutation loop, illustrated in blue between the transistors and the DC-link capacitors C_{DCL}. Within this area, the current commutes between high-side and low-side transistor. How fast the current can commute from one transistor to the other determines the overall switching speed of the power stage. Therefore, the inductance and resistance of this area should be as low as possible. Figure 3.13b shows the same simplified schematic with commutation loop, but with the added inductor L for the DPT. Adding L does not affect the commutation loop and therefore the inductor does not need to be located right at the PCB and can be connected as external component via cables, see figure 3.24

(a) Without DPT setup (b) With DPT setup

Figure 3.13.: Simplified schematic of a half-bridge with commutation loop (purple area)



(a) CSR (b) Infinity Sensor (c) Infinity Sensor + CSR

Figure 3.14.: Simplified schematic of a half-bridge for DPT + sensors with commutation loop (purple area)

Figure 3.14a through 3.14c show the commutation loop of the DPT with added current sensors, used for the measurements in this thesis.

Figure 3.14a and 3.14b show the versions with only one of the sensors in each circuit. The last circuit 3.14c depicts the PCB version with the Infinity Sensor V2 and the CSR in series. All three diagrams show that every sensor will add additional impedance to the commutation path and the results need to be interpreted accordingly.

The layout of the commutation loop of the DPT PCB with only the Infinity Sensor V2 is shown on the left side of figure 3.14a, where all other parts of the PCB were omitted. The right side of figure 3.15 shows a simplified cross section of the PCB, to visualize the actual copper traces, forming the commutation loop on layer 1 and 2.

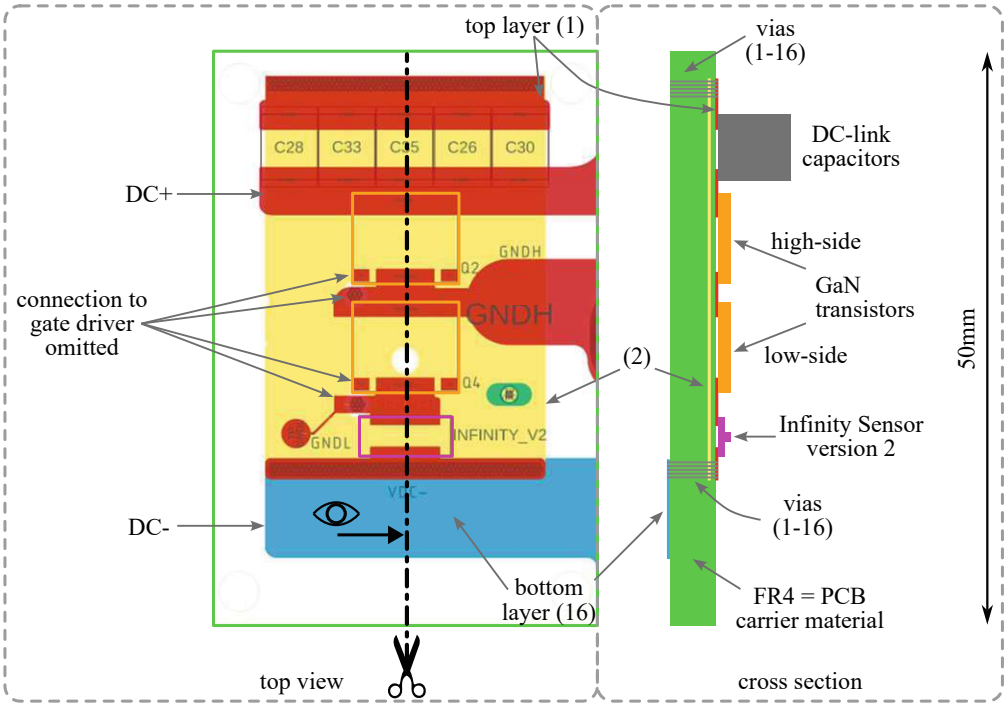


Figure 3.15.: Detail of the commutation loop PCB layout: top-view on the left and cross section on the right

The high-side Q_2 and low-side Q_4 GaN transistors are located as close as possible, with a narrow copper path on the top layer (red) to electrically connect the top-sides source with the low-side drain pad, as well as the GNDH-signal, where the inductor for the DPT is connected. The PCBs were manufactured with 4 layers, see figure 3.4 but mostly layer 1 and 2 were used for the commutation loop. This was done to reduce the parasitic inductance of the commutation loop.

A simplified model of the parasitic inductance on a PCB copper loop is given in equation 3.15 [30].

$$L_{PCB} = \mu_0 \frac{e}{w} l \tag{3.15}$$

L_{PCB} is the resulting inductance of two opposite PCB copper traces with a width w and distance e, forming a loop of length l, cross section shown in figure 3.16. μ_0 is the vacuum magnetic permeability, which is a natural constant and has a defined value of $\sim 1.2566\,\mu\mathrm{N/A^2}$.

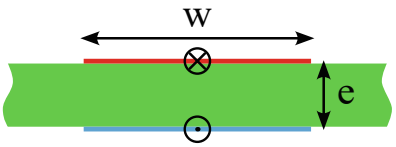


Figure 3.16.: Dimensional sketch for simplified model of parasitic inductance of PCB traces, red = copper trace of top layer current flowing orthogonally into the image, blue = copper trace of bottom layer, current flowing orthogonally out of the image

Further discussions on the topic of parasitics can be found in [58] and [34], the latter also focuses on the parasitics in the gate driver circuit.

Based on this model, one goal during the PCB design process was to reduce parasitic inductance on a few key principles without detailed analysis or simulation.

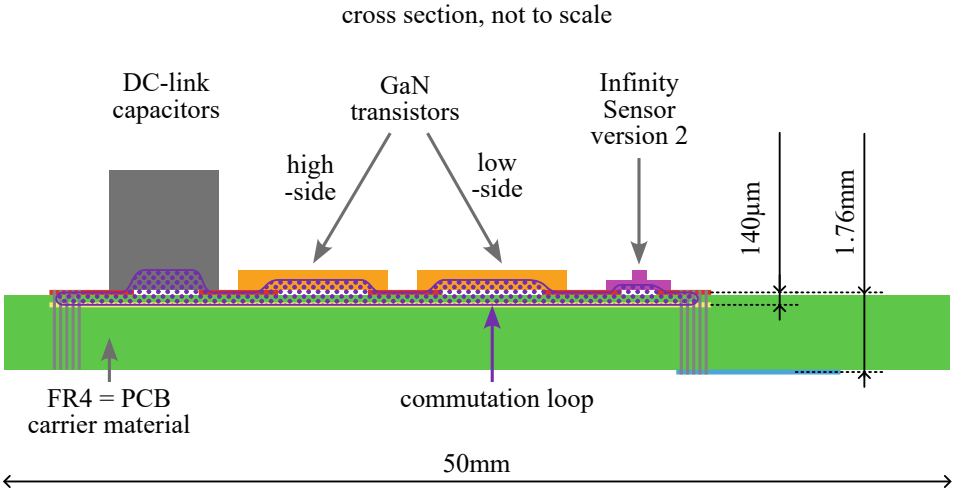


Figure 3.17.: Detailed cross section of the DPT PCB at the commutation loop, visualizing the current path with Infinity Sensor V2

The first principle is to pack the current carrying copper layers as close as possible, which means to make e in equation 3.15 as small as possible. By choosing layer 1 on top of the PCB for the drain-source-path and layer 2 for the return path, a distance of 140 µm was achieved, see figure 3.17.

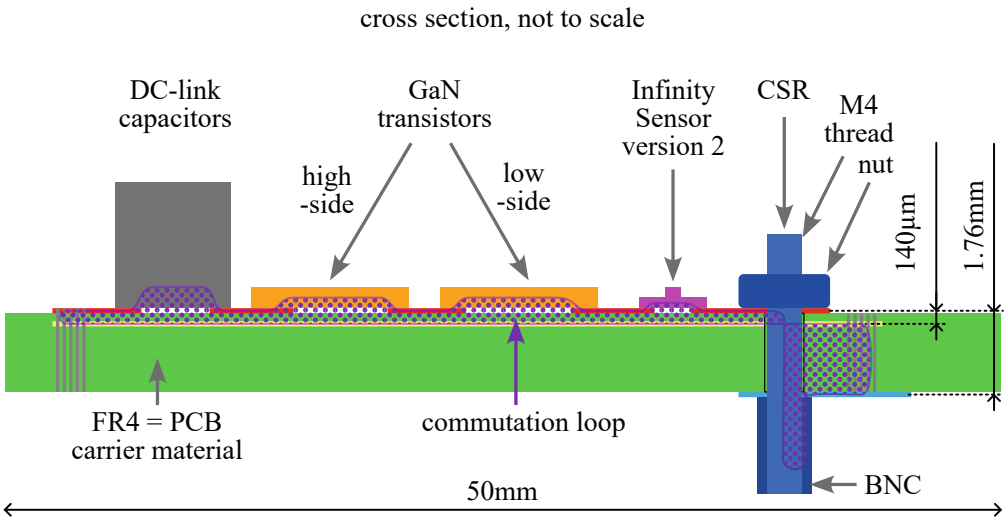


Figure 3.18.: Detailed cross section of the DPT PCB at the commutation loop, visualizing the current path with Infinity Sensor V2 and CSR in series

When using the CSR, at least some parts of the current path have to deviate from layer 1 and layer 2, see figure 3.18. Because of this extra routing, the CSR comes with extra insertion inductance additional to its own inductance. The second principle is to widen the copper traces as much as possible, in order to increase w in equation 3.15.

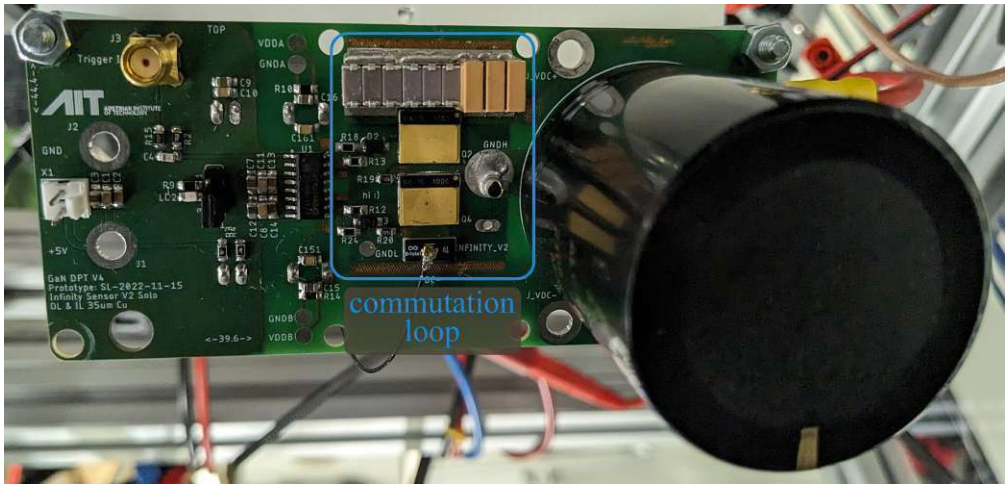


Figure 3.19.: Image of the commutation loop on the built and tested DPT PCB with the Infinity Sensor V2

Figure 3.19 depicts one of the produced and tested PCBs with the Infinity Sensor V2 in the commutation loop. The blue rectangle roughly marks the commutation loop copper traces of layer 1 (top) and layer 2 (the first inner layer). The only areas where the copper traces had to be constricted is right at the GaN transistors and at the Infinity Sensor.

3.2.8. Double pulse generation

The driver IC SI8274AB4D-IS1 of the driver loop, described in 3.2.6 takes a single, ground referenced input signal on its PWM-pin and transforms it into two complementary and isolated gate driving signals for the high-side and low-side GaN transistors. The logic of this process in the driver IC is deterministic and hard wired, the involved time delays are as well deterministic. The timing is specifically designed in such a way that the transistors both switch complementarily and very shortly after each other in such a way that they never are conductive at the same time, avoiding a hard short circuit. The complementary logic of the driver IC is shown conceptually in figure 3.20, where v_{GSL} is the gate driving voltage of the low-side GaN transistor and v_{GSH} respectively for the high-side. v_T is the trigger input signal at the PWM-pin of the driver IC and v_{AFG} is the PWM-signal provided by the 3350B function generator (AFG).

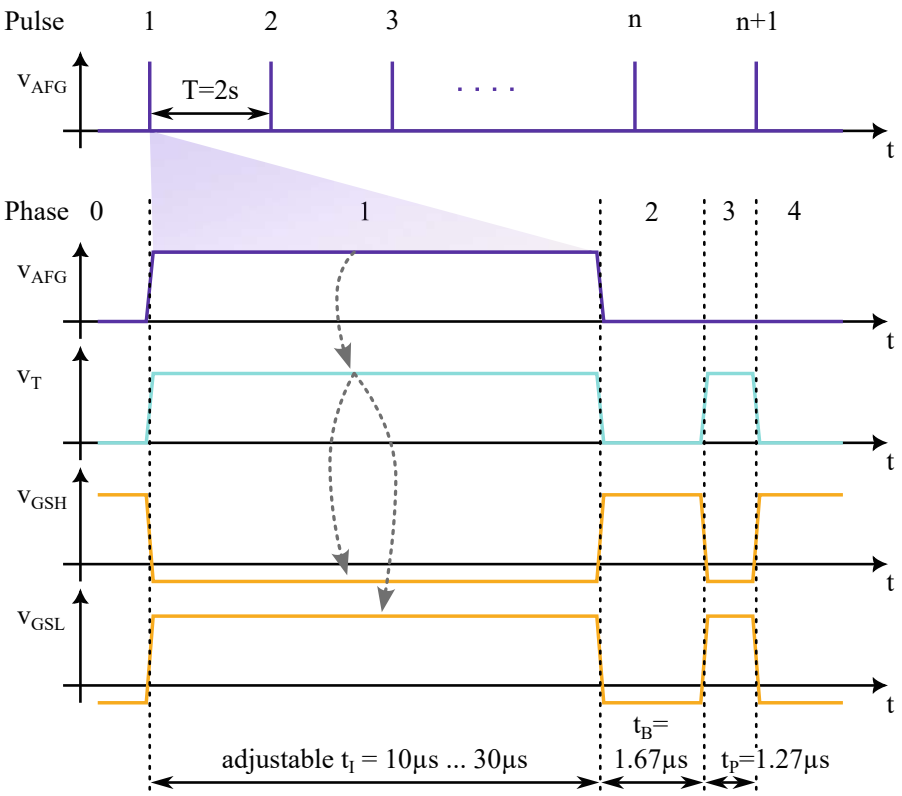


Figure 3.20.: Chronological phases of the DPT trigger signals

As figure 3.20 shows, the pulse of the AFG results in two consecutive pulses of the trigger signal v_T and thus produces the DPT. The first pulse of v_T is exactly as long as the ON-time t_I of v_{AFG} and t_I is adjustable at the AFG. t_I is the integration

time of the DPT. The second pulse follows the first after t_B=1.67 µs and has a fixed duration of t_P=1.27 µs. Therefore, the second pulse is not generated by the AFG but by an intermediate PCB for the double pulse generation. The schematic of this PCB is illustrated in figure 3.21. It is based on a design from [35] and the main component is a 74AC14D hex inverter with Schmitt-Trigger inputs. The input signal v_{AFG} is fed in at the SMA connector J_3 and the first two inverters $U1_D$ and $U1_E$, in combination with the diode D_1 and the forward connection to $U1_B$ function as a feed through of the first pulse with a duration of t_I, adding a fixed propagation delay time $t_{PD} = 8$ ns for each inverter. The inverters $U1_B$ and $U1_C$ are used to provide the output signal v_T in a non-inverted fashion at the first SMA connector J_1 and inverted at the second SMA connector J_2. The inverted signal was not used for the DPT in this thesis. The inverters described so far provide the first pulse of the DPT with a duration of t_I and the deterministic delay of $4t_{PD}$ between v_{AFG} and v_T. The remaining inverters $U1_F$ and $U1_A$ provide the second pulse for the DPT after a short break of t_B=1.67 µs and with a fixed duration of t_P=1.27 µs.

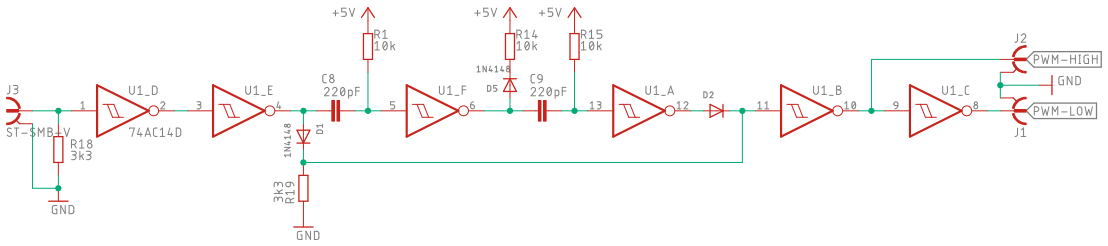


Figure 3.21.: Schematic of the PCB for the double pulse generation from a single, AFG-provided PWM pulse

$$\tau = RC = 10\,\text{k}\Omega \cdot 220\,\text{pF} = 2.2\,\mu\text{s} \tag{3.16}$$

After the first pulse, the output of $U1_E$ switches to low, pulling the input of $U1_F$ low as well, until C_8 is charged by R_1. This causes an inverted sequence at the output of $U1_F$, where the same procedure is repeated when the low output of $U1_F$ pulls the input of $U1_A$ low and C_9 starts charging via R_{15}. The first delay, caused by charging C_8, generates t_B and the second delay, caused by charging C_9, generates the duration of the second pulse t_P. The time constant τ of the RC-circuit is given in equation 3.16. The inverters will switch after a shorter duration than τ, because the threshold voltage of the inverters at a supply voltage of 5 V is in the range between 1.1 V and 3.9 V. Theoretically, the duration of t_B and t_P would be the same, because the same component values of 220 pF for C_8 and C_9, and 10 kΩ for the resistors R_1 and R_15 are used. The measured values of t_B and t_P

are off by 400 ns because of the tolerances of the used components. The capacitors have a tolerance of ± 10 % and the resistors ± 10 %. Nevertheless, this deviation is acceptable, because the exact durations are not important for the DPT as long as the deviation stays the same and is smaller than the total pulse duration, which is the case. In conclusion the function of the diodes in the circuit of figure 3.21 can be described as follows: D_1 prevents the output of $U1_A$ from having an influence on the input of $U1_F$. D_2 prevents $U1_A$ from pulling the input of $U1_B$ low when the signal of $U1_E$ is high.

3.3. Measurement setup

Figure 3.22 shows an abstracted schematic of the measurement setup. In the middle, the device under test (DUT), the DPT PCB is depicted (blue). The DUT is connected to Tektronix MSO58 Oscilloscope (yellow). Depending on the tested DUT, one or two direct coaxial connections are made by means of RG316 cables from the SMA connectors of the CSR and the MHF4 connector of the Infinity Sensor. The voltage measurement is done by means of a P5100A 1:100 single ended voltage probe. To complete the DPT circuit, an external air core inductor with an inductance of 789 µH is connected by means of 4 mm laboratory cables with safety connectors. The air core inductor is a single copper wire, wound on an acrylic carrier bobbin, see figure 3.24. The RLC-meter (table 3.2 was used to measure the the air core of the inductance of L =789 µH. The DPT PCB is supplied with 5 V on the driver side by means of the AimTTi PL601 DC PSU (purple) and a twin-1mm² cable. The 200 V...400 V for the DC-link capacitors of the DPT PCB is supplied by means of a Delta Elektronika SM660-AR-11/1 (purple) and two 4 mm laboratory cables and safety connectors. The output voltage of the 400 V PSU was constantly monitored by means of a DMM for safety reasons (red).

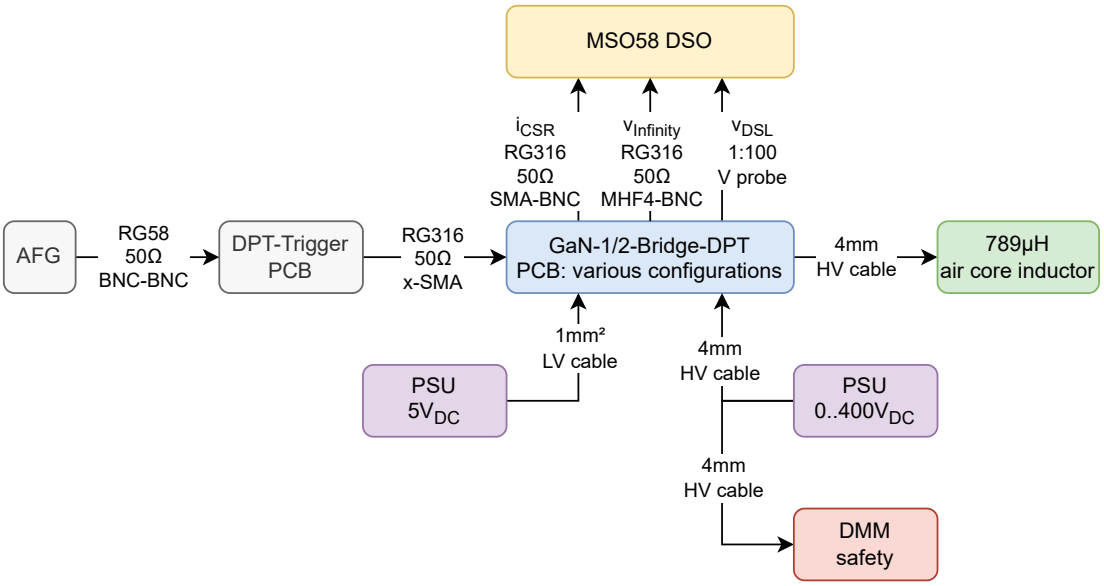


Figure 3.22.: Measurement setup for the Double Pulse Test

Figure 3.23 shows the test setup in the AIT power electronics laboratory. The 19" rack on the left side holds the MSO58 digital storage oscilloscope and the function generator for the trigger signal (AFG). The current signals are connected to the DSO by means of RG316 coaxial cables. The 19" rack on the right side was

entirely assembled for the DPT of this thesis and carries the safety test cell, which was also custom built for this thesis. The safety test cell provides an protected environment for the DPT PCBs while they are tested. Aluminum frames which are connected to PE hold acrylic glass walls to protect the surrounding area and prevent accidental touching of the PCB during operation of the DC voltage.

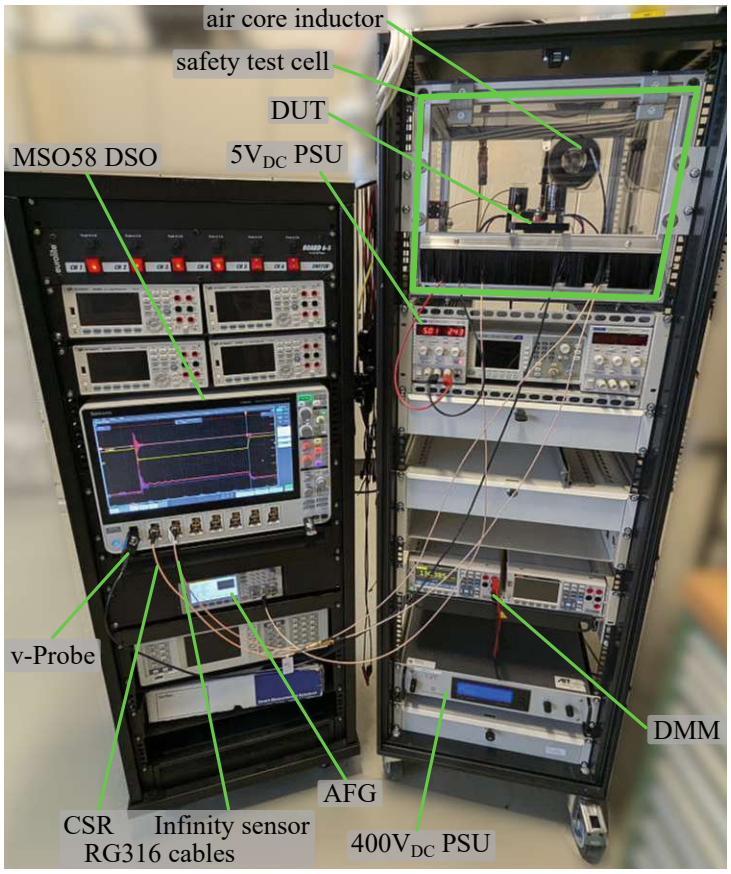
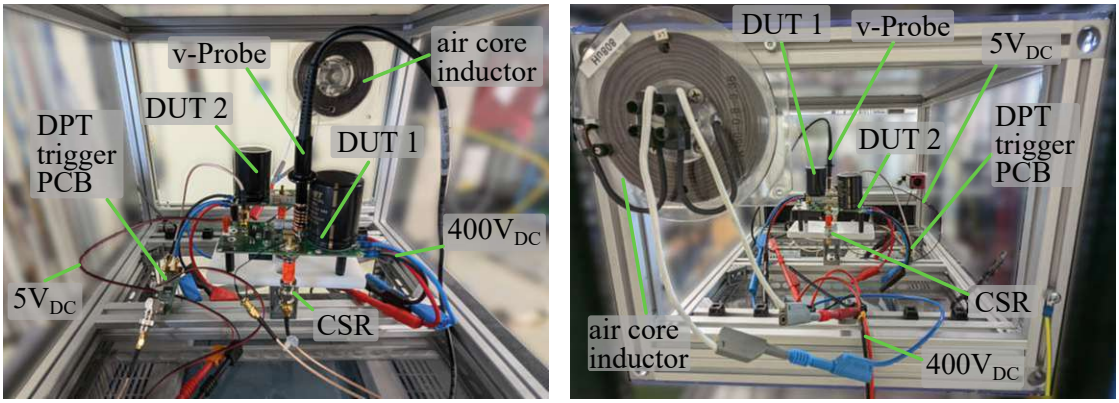


Figure 3.23.: Picture of the measurement setup for the DPT at the AIT power electronics laboratory

Below the test cell the 5 V PSU is located. The Delta Elektronika DC voltage supply for up to 400 V can be found at the bottom of the rack. The DC output terminals are connected by means of 4 mm safety connectors to the DPT PCB in the safety test cell. Above the DC power supply a DMM is located, which is permanently connected to the output of the DC power supply as an additional safety measure, indicating when DC voltage is present at the test setup.



(a) Front view (b) Rear view

Figure 3.24.: Interior of safety test cell with 2 DUT

Figure 3.24 shows two close up images of the opened safety test cell. Inside, a test rig made from white POM-C isolation material and black PE standoffs holds two DPT PCBs at the same time. The electrical connections to the DSO are shown as well as the connections to the 5 V and 400 V PSUs are shown. On the back side of the safety test cell, the air core inductor for the DPT is mounted.

3.3.1. Equipment

All essential equipment used for measurements in this work is listed in table 3.2. Additional unspecific equipment was used to design, produce and test the PCBs but is not documented due to their irrelevant nature to the measurement process.

Table 3.2.: Measurement equipment

Name	**Manufacturer**	**Type**	**Serial#**	**misc.**
MSO58	Tektronix	DSO	C010633	Opts: 5-BW-1000
P5100A	Tektronix	DSO-Probe	C007948	500 MHz, 40 MΩ 2.5 pF, 100x
33500B	Keysight	AFG	MY52202623	FW:3.05-1.19-2.00-52-00
AFG1062	Tektronix	AFG	AFG1062 2131005	-
RSDM 3055	RS Pro	DMM	SDM35GB C6R0145	-
PL601	AimTTi	DC PSU	557885	0-60V, 0-1.5A
Resistomat 2316	Burster	Milliohm-Meter	399556	+/-60 µΩ
SSDN-414-05	T&M Research	CSR	AIT CSR1	50.46 mΩ
SSDN-414-05	T&M Research	CSR	AIT CSR2	50.20 mΩ
SSDN-414-01	T&M Research	CSR	AIT CSR3	10.31 mΩ
SSDN-414-01	T&M Research	CSR	AIT CSR4	10.16 mΩ
L1 808uH	BLM	Air Core Inductor	K150-0.8-3.35	789.0 µH +/-0.8%
U1733C	Agilent	LCR-Meter	MY53160008	+/-0.8%
SM660-AR-11/1	Delta Elektronika	DC PSU	10071525	0-600V
Bode 100	Omicron Lab	VNA	PC182H	Rev.2

Table 3.3 shows the manufacturers specifications of the used CSRs for the DPT. The exact values of each individual CSR are illustrated in table 3.2 and were incorporated into the measurement data acquisition on the DSO by dividing v_{CSR} by R_{CSR} and thus, only the resulting current i_{CSR} was recorded.

Table 3.3.: Manufacturer specifications of the T&M Research CSRs [2], [3]

Model	Resistance	Bandwidth	Rise time	E_{max}
SSDN-414-01	10 mΩ	400 MHz	1 ns	6 J
SSDN-414-05	50 mΩ	2 GHz	180 ps	2 J

The CSRs used for measurements of the commutation current i_{DS} were calibrated by means of the Resistomat 2316 Milliohm-Meter 3.2. The according calibration data is given in table 3.4.

Table 3.4.: CSR calibration

Name	Manufacturer	Serial#	Value	Uncertainty
SSDN-414-05	T&M Research	AIT CSR1	50.46 mΩ	±10 μΩ
SSDN-414-05	T&M Research	AIT CSR2	50.20 mΩ	±10 μΩ
SSDN-414-01	T&M Research	AIT CSR3	10.31 mΩ	±10 μΩ
SSDN-414-01	T&M Research	AIT CSR4	10.16 mΩ	±10 μΩ

3.3.2. Oscilloscope

Modern power electronics development requires precise Digital Storage Oscilloscopes (DSOs) to measure relevant signals of circuits at any stage of the development process, from the first prototype to the final product. DSOs allow to simultaneously measure several voltage signals at their input channels. These channels are usually represented at the DSOs front panel by means of coaxial BNC connectors. These BNC connectors use their outer ring for shielding off noise from inner signal wire. The shielding is usually connected to the electrical ground reference of the entire DSO. Signals are measured by means of probes, which are connected to the DSO at the BNC connector. Many different kinds of probes are used for specific purposes, like high and low voltage, high and low bandwidth, isolated probes, etc. This needs to be taken into consideration when measuring two or more non-isolated signals at the same time. In this case, all the measured signals must use the same reference voltage level at the electric circuit, unless highly specialized and expensive isolation probes are used, like the Tektronix isoVu, see outlook chapter 6.

Vertical resolution

Typical DSOs have theoretical vertical resolutions of 8 bits. Some oscilloscopes offer vertical resolutions of up to 16 bits, like the used DSO in this thesis. The Tektronix MSO58 allows to switch between the so-called low resolution mode with

a vertical resolution of 8 bits at full sampling rate and 12 bits at half sampling rate. The high resolution mode of the MSO58 allows to use a vertical resolution of up to 16 bits, at the expense of the sample rate. Table 3.5 is taken from the manufacturers data sheet [19] and shows the achievable vertical resolution at specific sampling rates. The datasheet mentions that the ADCs of the DSO capture the connected signals with 12 bits vertical resolution.

Table 3.5.: Vertical resolution of the MSO58 DSO, taken from the MSO58 data sheet [19]

Parameter	**Value**
ADC Resolution	12 bits
Vertical Resolution	8 bits @ 6.25 GS/s 12 bits @ 3.125 GS/s 13 bits @ 1.25 GS/s (High Res) 14 bits @ 625 MS/s (High Res) 15 bits @ 312.5 MS/s (High Res) 16 bits @ ≤125 MS/s (High Res)
Sample Rate	6.25 GS/s on all ADC channels (160 ps resolution)
Record Length (std.)	62.5 Mpoints on all ADC channels

Effective number of bits

The effective number of bits (ENOB) describes the quality of the analog-digital conversion of a specific electronic measurement. The concept of the ENOB is derived from the idea that the theoretical number of bits of any ADC conversion leads to a certain signal to noise ratio (SNR), like described in equation 3.17, given the input is a sine wave signal with an amplitude equal to the full scale input of the ADC. Details to the fundamental relations between SNR and ENOB can be found in [28] and [45]. Generally, the SNR is defined as the logarithmic relation of the signal power P_S to noise power P_N and signal amplitude A_S to noise amplitude A_N squared, see eqution 3.17. For these considerations, sine-like signal forms of P and A are assumed. Later considerations, where also distortions of the sine-like signals are taken into account lead to the term signal-to-noise and distortion ratio (SINAD).

$$SNR = 10 \cdot \log(\frac{P_S}{P_N}) = 10 \cdot \log(\frac{A_S}{A_N})^2 \tag{3.17}$$

The theoretical SNR_{th} of an ADC with B bits is defined as shown in equation 3.18 [28], where 1.76 dB is the SNR from the quantisation noise.

$$SNR_{ADC-th} \approx 1.76\,\text{dB} + 6.02 \cdot B \tag{3.18}$$

Applying equation 3.18 to the MSO58 12bit ADC delivers a theoretical SNR of the used DSO of 74 dB.

$$SNR_{MSO58-th} \approx 1.76\,\text{dB} + 6.02 \cdot 12 = 74\,\text{dB} \tag{3.19}$$

The ENOB can be derived by rearranging equation 3.18 to get the number of bits B, see equation 3.20.

$$B \approx \frac{SNR - 1.76\,\text{dB}}{6.02} \tag{3.20}$$

B is the integer number of bits of a theoretical ADC, when the input amplitude (IA) equals the full scale amplitude (FSA) with a perfect sine wave, distortions and frequency dependencies neglected. To account for the latter, equation 3.20 can be extended by means of using the SINAD instead of the SNR accounting for noise and distortion.

$$ENOB = \frac{SINAD - 1.76\,\text{dB}}{6.02} \tag{3.21}$$

Where SINAD is generally defined as given in equation 3.22, where P_D is the power of the signal distortion and A_D is the respective amplitude.

$$SINAD = 10 \cdot \log(\frac{P_S}{P_N + P_D}) = 10 \cdot \log(\frac{A_S}{A_N + A_D})^2 \tag{3.22}$$

The resulting equation is given in 3.21, which can be further extended by the $20 * \log \frac{FSA}{IA}$ term. This term takes into consideration that a measured signal amplitude is most likely smaller than the full scale amplitude of the measurement device, see equation 3.23. The 1.76 dB term is a constant offset that arises in the formula for the SNR of an ideal ADC due to the quantization error, reflecting the relationship between the ADC resolution and the quantization noise.

$$ENOB = \frac{SINAD_m - 1.76\,\text{dB} + 20log(\frac{FSA}{IA})}{6.02} \tag{3.23}$$

Considering the ENOB, the claimed number of bits of a measurement device like an oscilloscope is put into a realistic perspective of how accurate a given signal can be measured with the setup at hands. For the used Tektronix MSO58 oscilloscope, the ENOB values are provided in the data sheet [19] and are given in table 3.6 as well as the the corresponding calculated SINAD values.

Table 3.6.: ENOB and SINAD of the MSO58 DSO, taken from MSO58 data sheet [19]: "2 GHz models, High Res mode, 50 Ω, 10 MHz input with 90% full screen" (only 1 GHz mode was used)

Bandwidth	ENOB	SINAD
1 GHz	7.0	43.9 dB
250 MHz	7.8	48.7 dB
20 MHz	8.7	54.1 dB

Voltage probe and adapter for GND shielding

Typical voltage probes for oscilloscopes feature a 1:10 attenuation, 300 V rms maximum voltage, and 200 MHz bandwidth. Because these limits are not sufficient for measuring the v_{DS} voltage on the low side GaN transistor, a single ended Tektronix P5100A voltage probe was used for this task. The P5100A [22] has an attenuation of 1:100 and a maximum voltage of 1 kV rms, 2.5 kV peak, which allows to measure the maximum voltage used during the DPT of $v_{DC} = 400\,\mathrm{V}$. The signal from the probe is fed directly to the oscilloscope with a maximum input voltage of $v_{50\Omega} = 5\,\mathrm{V}rms, \pm 20\,\mathrm{V}peak$. The input configuration of 50 Ω and $v_{1M\Omega} = 300\,\mathrm{V}rms, \pm 20\,\mathrm{V}peak$ for 1 MΩ was used. With an input impedance of 40 MΩ and 2.5 pF, the P5100A has a bandwidth of 500 MHz, which is barely suitable for measuring voltage signals with rise and fall times of 10 ns.

Whittaker–Nyquist–Shannon theorem

Claude Shannon [47] formulated the following theorem in his 1949 paper about communication in the presence of noise:

Theorem 1 *If a function f(t) contains no frequencies higher than W cps, it is completely determined by giving its ordinates at a series of points spaced 1/2 W seconds apart.*

The intuitive justification is that, if f(t) contains no frequencies higher than W, it cannot change to a substantially new value in a time less than one-half cycle of the highest frequency, that is, 1/2 W.

Nowadays, when talking about signal acquisition the theorem can be referred to as Whittaker–Nyquist–Shannon theorem. In 1915 Sir Edmund Taylor Whittaker published his work on interpolation theory [59], which was later cited by Claude Shannon in his aforementioned paper of 1949. Also Harry Nyquist substantially contributed to the theorem with his 1928 work on certain topics in telegraph

transmission theory, where he formulated the threshold frequency $f_s/2$, which essentially is the limit of a signal frequency that can be successfully picked up with a sampling frequency of f_s [41].

Applying the Whittaker–Nyquist–Shannon theorem to the bandwidth of the used voltage probe results in a maximum frequency of the measured signal:

$$f_{max_{signal}} = \frac{f_{max_{probe}}}{2} \tag{3.24}$$

Accordingly, the smallest time step that can be picked up by the 500 MHz probe is 4 ns.

$$\Delta t_{min} = \frac{1}{f_{max_{signal}}} \tag{3.25}$$

Taking a look at the topic from the opposite side, a general recommendation in many oscilloscope handbooks [21] is to approximate the minimum required bandwidth B_{min} by means of the expected rise time t_r of the measured signal. The rise time is determined as the time a signal takes to rise from 10% to 90% of its full amplitude. Oscilloscopes and probes do not feature a flat frequency response from 0 Hz to their full bandwidth. Their frequency response can be roughly approximated by a RC-circuit, forming a low pass. This low pass has an attenuation of −3 dB at the maximum bandwidth. If the minimum rise time of the measured signal is known, the minimum bandwidth of the DSO is recommended to be calculated according to equation 3.26 [21].

$$B_{min} = 0.35/t_r \tag{3.26}$$

A more systematic approach comes from the central limit theorem when considering all relevant components of a measurement system as individual low pass filters [13]. When using a combination of N instruments, represented as N individual low pass filters, the total system bandwidth B_{sys} of the entire system is a combination of the individual filter bandwidth, see equation 3.27.

$$B_{sys} = \frac{1}{\sqrt{(\frac{1}{B_1})^2 + ... + (\frac{1}{B_N})^2}} \tag{3.27}$$

Equation 3.27 can be reduced to equation 3.28 if all filters feature the same bandwidth B.

$$B_{sys} = \frac{B}{\sqrt{N}} \tag{3.28}$$

For the used system consisting of the MSO58 DSO and TPP0850 voltage probe, the system bandwidth B_{sys} can be derived like shown in equation 3.29. The individual bandwidths are B_P of the voltage probe and B_O of the DSO.

$$B_{sys} = \frac{1}{\sqrt{(\frac{1}{B_P})^2 + (\frac{1}{B_O})^2}} \tag{3.29}$$

Table 3.7 lists relevant parameters of the used voltage probes. Additionally, the calculated combined bandwidth B_{sys} and the resulting minimum time step Δt_{min} are given. All measurements in the results chapter were captured with the TPP0850 probe. Because of its low V_{max}, the TPP1000 probe was used for Vv_{GS} measurements only. The P5100A probe was used for measurements during the prototyping phase of the DPT PCBs.

Table 3.7.: Bandwidth data of used DSO voltage probes

Probe	B_P	V_{max}	**Attenuation**	B_{sys}	Δt_{min}
Tektronix P5100A	500 MHz	2.5 kV	1/100	447 MHz	4.47 ns
Tektronix TPP0850	800 MHz	2.5 kV	1/100	625 MHz	3.2 ns
Tektronix TPP1000	1 GHz	300 V	1/10	707 MHz	2.83 ns

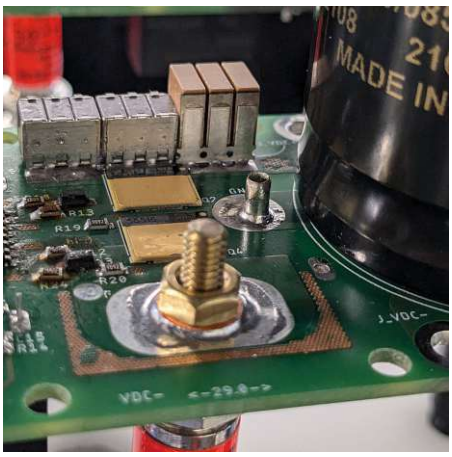
Figure 3.25 shows the used voltage probe and DPT PCB features for the voltage measurement. Figure 3.25a shows the probe tip without GND clip. Because of the high dv/dt and di/dt in the surrounding of the voltage measurement location, picking up the GND reference signal of the probe with the GND clip and crocodile clip is not appropriate, because the created GND loop would pick up too much noise.

Therefore, a custom made GND shield, figure 3.25b, was made from bare copper wire, connected to the clip attachment ring of the probe, wound around and down the voltage probe tip in a helix. At the end of the helix, the copper wire can be bent to attach to the GND potential of the PCB close by. Using this GND shield increased the noise immunity of the voltage measurement to a point where the resulting signal quality was apparently sufficient.

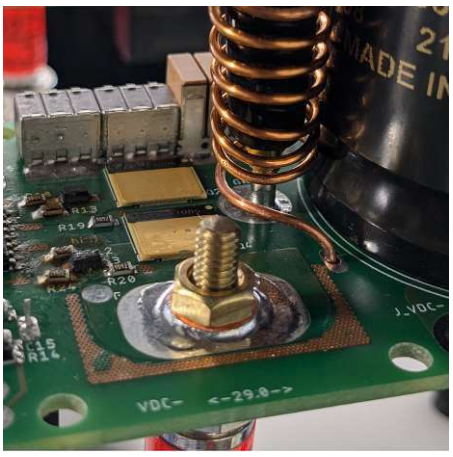
(a) Without GND clip

(b) With custom GND shield

Figure 3.25.: Tektronix TPP0850 voltage probe



(a) Location of the voltage contact points on the DPT PCB



(b) Voltage tip with custom-made GND shield attached to DPT PCB

Figure 3.26.: Tektronix TPP0850 voltage probe and attachment points for v_{DS} measurement on the DPT PCB

Figure 3.26a depicts the measurement location of v_{DS} on the low side GaN transistor on the DPT PCB. Bare metal ferules were soldered to the two test points for the signals $GNDH$ and $GNDL$ with $v_{DSL} = GNDH - GNDL$. These ferules mechanically secure and electrically connect the voltage probe tip and GND shield to the PCB, shown in-situ in figure 3.26b.

3.4. Uncertainty

The calculation of the uncertainty in this thesis is based on the recommendations of the guide to the expression of uncertainty in measurement (GUM), [26]. There are three relevant measurement uncertainties in this thesis:

1. voltage measurement with the DSO
2. current measurement with the CSR + DSO
3. current measurement with the Infinity Sensor + DSO

3.4.1. Voltage measurements

The MSO58 DSO measures voltages with its internal ADC directly. Therefore, the uncertainty of the voltage measurement of the DSO u_{DSO} is a good estimation for the uncertainty of the voltage measurement u_V in general.

$$u_V = u_{DSO} \tag{3.30}$$

Table 3.8.: DC Gain Accuracy of the MSO58 DSO, according to the data sheet [19]

Termination	**Range**	**DC Gain Accuracy**
50 Ω	>1 mV/Div	± 0.6 % of full scale
50 Ω	1 mV/Div 500 µV/Div	± 1 % of full scale
1 MΩ	>1 mV/Div	± 0.5 % of full scale
1 MΩ	1 mV/Div 500 µV/Div	± 1 % of full scale

The uncertainty of the DSO voltage measurements can be found in the MSO58 data sheet [19], see table 3.8. Because the three measurements of 3.4 were captured by the DSO with different termination impedances, there are also three different uncertainties involved. The DC voltage v_{DC} was captured with 1 MΩ and a full scale of 500 V, which results in an uncertainty u_{VDC} of ± 0.5 % or ± 2.5 V. The uncertainties for all three voltage measurements are listed in table 3.9.

Table 3.9.: Uncertainties of voltage measurements, based on the MSO58 DSO data sheet [19]

Signal	**Full scale**	**V/div**	u_{rel}	u_{abs}
v_{DC}	500 V	50 V	±0.5 %	±2.5 V
v_{CSR}	2.5 V	250 mV	±0.6 %	±15 mV
$v_{Inf.}$	1 V	100 mV	±0.6 %	±6 mV

Because the measurement of the DC voltage v_{DC} can be taken directly from the DSO without any further calculation, the expanded uncertainty is derived with a coverage factor of $k = 2$ to be $U_{DC} = \pm 1\,\%$ or $\pm 5\,\mathrm{V}$ [26].

3.4.2. Current measurement CSR

Equation 3.31 shows Ohm's law, which allows to derive the current i_{CSR} from the measured voltage v_{CSR} and the measured value of the resistance R_{CSR}.

$$I = \frac{V}{R} \tag{3.31}$$

Accordingly, the compound uncertainty of i_{CSR} must be derived from the uncertainties of both quantities v_{CSR} and R_{CSR} like shown in equation 3.32 to 3.34.

$$u_I = \sqrt{\left(\frac{\partial I}{\partial V}\right)^2 u_V^2 + \left(\frac{\partial I}{\partial R}\right)^2 u_R^2} = \sqrt{\left(\frac{u_V}{R}\right)^2 + \left(-\frac{V \cdot u_R}{R^2}\right)^2} \tag{3.32}$$

$$\frac{u_I}{I} = \sqrt{\left(\frac{u_V}{V}\right)^2 + \left(\frac{u_R}{R}\right)^2} \tag{3.33}$$

$$\frac{u_I}{I} = \sqrt{\left(\frac{15\,\mathrm{mV}}{2.5\,\mathrm{V}}\right)^2 + \left(\frac{10\,\mu\Omega}{50.46\,\mathrm{m}\Omega}\right)^2} = \pm 0.6003\,\% \tag{3.34}$$

Equation 3.34 shows that the uncertainty of R_{CSR} is negligible compared to the uncertainty of the voltage measurement v_{CSR}. As a result, the compound uncertainty of the current measurement with the CSR can be derived to be $U_{I-CSR} = 1.2\,\%$ (with a coverage factor of $k = 2$).

3.4.3. Current measurement Infinity Sensor

The calculation of the current based on the voltage signal from the Infinity Sensor V2 is illustrated below in equation 3.35.

$$i_T(t) = \int \frac{v_S(t)}{M} dt + I_0 \tag{3.35}$$

Because the DC-offset current I_0 is unknown, a method for estimating I_0 by means of the average of the signal v_S is described in section 3.5.3. Because I_0 is estimated by averaging v_S over a certain time frame, the uncertainty of I_0 is as well approximated by the uncertainty of v_S, hence the term u_V/V appears twice in the calculation of the uncertainty in equation 3.36.

$$\frac{u_I}{I} = \sqrt{\left(\frac{u_V}{V}\right)^2 + \left(\frac{u_M}{M}\right)^2 + \left(\frac{u_V}{V}\right)^2} \tag{3.36}$$

The uncertainty of the current measurement with the Infinity Sensor is calculated to be:

$$\frac{u_I}{I} = \sqrt{2(0.006)^2 + (0.041)^2} = \pm 4.19\,\% \tag{3.37}$$

Based on the result of equation 3.37 and considering a coverage factor of $k = 2$, the compound uncertainty of the current measurement with the Infinity Sensor V2 is $U_{I-Inf.} = \pm 8.37\,\%$. Because of the later mentioned measurement data post processing, especially the averaging of the current derived from the Infinity Sensor, the $U_{I-Inf.}$ might be substantially lower. $U_{I-Inf.}$ is dominated by the uncertainty of the sensitivity of the Infinity Sensor, which is an order of magnitude larger than the uncertainty of the involved voltage measurement. All relevant uncertainties for the measurements of this thesis are listed below in table 3.10.

Table 3.10.: Compound uncertainties of measurements (coverage factor $k = 2$)

Signal	U_{rel}	U_{abs}
v_{DC}	$\pm 1\,\%$	$\pm 5\,\mathrm{V}$
i_{CSR}	$\pm 1.2\,\%$	$\pm 600\,\mathrm{mA}$
$i_{Inf.}$	$\pm 8.37\,\%$	$\pm 4.2\,\mathrm{A}$

3.5. Measurement data processing

All measured data was captured by the Tektronix MSO58 digital storage oscilloscope. Several other oscilloscopes were used in the beginning of the development phase of the DPT PCB as well. These DSOs showed weaknesses and ultimately did not qualify for measuring and processing of the di/dt signal from the Infinity Sensor.

3.5.1. Low-side drain-source voltage

The drain-source voltage v_{DS} was measured by means of a single-ended 1 : 100 voltage probe and did not require any further data processing on the oscilloscope.

3.5.2. Low-side drain-source current: CSR

When measuring the drain-source current i_{DS} in combination with a CSR, the voltage signal from the CSR can be connected directly to the input channel of the oscilloscope by means of a 50 Ω coaxial cable with BNC and SMA connectors. The input channel configuration is set to an impedance of 50 Ω. The obtained signal is then fed into a so-called math-channel of the DSO to calculate the current based on the voltage signal and the known resistance R_{CSR} of the CSR, see equation 2.2. Additionally, adjustments of the bandwidth of the input channel to the bandwidth of the CSR was made whenever the CSR had a lower bandwidth than the maximum bandwidth of the DSO input channel.

3.5.3. Low-side drain-source current: Infinity Sensor

Because the Infinity Sensor uses the same physical principle as a Rogowski coil, the output voltage signal of the sensor is proportional to the derivative of the current below, di_S/dt, see equation 3.38. Hence, the voltage signal from the Infinity Sensor picked up at the MHF4-connector must be integrated by the measurement system, see equation 3.39, where i_S is the calculated sensor current, v_S is the picked up voltage signal from the sensor, and I_0 is the unknown integration constant.

$$v_S(t) = \frac{i_S(t)}{dt} \tag{3.38}$$

$$i_S(t) = \int \frac{v_S(t)}{M} dt + I_0 \tag{3.39}$$

Equation 3.39 is the theoretical idea for the sensor signal processing. But there are two unknown aspects to this equation:

1. The scaling factor: The Infinity Sensor, like a Rogowski coil, senses the derivative of the current. Besides noise, the actual signal is only a fraction of the derivative of the current. This scaling factor is reflected by the coefficient M, the mutual inductance.

2. The DC-offset of the current: I_0

Experimental use of the Infinity Sensor and its prototypes led to the practical solutions to these unknown parameters. The data sheet of the Infinity Sensor V2 [11] provides these solutions and lists recommendations on how to setup and process the measured voltage signal from the sensor. These instructions are listed below in table 3.11. The scaling factor is set to 10^{10}. The DC-offset is determined by taking the average of v_S during a time frame where no current switching is happening, see equations 3.40 and 3.41. While working with the Infinity Sensor for this thesis, another possible solution for the DC-offset was found useful and used henceforward. This solution will be discussed in section 3.5.4.

Table 3.11.: Instructions for measuring currents with the Infinity Sensor V2 on an DSO, taken from the data sheet [11]

1.	Ensure that the scope trigger and time offset are configured in such a way that the output signal from the sensor is zero at the start time of the signal trace.
2.	Zoom-in on a portion of the measured signal where no current switching event is taking place.
3.	Take the average of the signal over the zoomed-in period. This is the $DC - offset$ = AVG3 in equation 3.40 below.
4.	Activate a maths-channel on the oscilloscope and enter the function: $10e9 * integral(CH_{sense} - DC - offset)$, where CH_{sense} is the reference for the channel that is being used to capture the sensor's output voltage.

$$\text{AVG3} = \frac{\text{CH3}_{Right} - \text{CH3}_{Left}}{\text{Time}_{Right} - \text{Time}_{Left}} \tag{3.40}$$

$$\text{MATH3} = 10\text{e}9 \text{ integral}(\text{CH3 - AVG3}) \tag{3.41}$$

Despite the recommendations on post processing the signal from the Infinity Sensor, the integration constant I_0 can't be determined accurately and this is an obvious flaw of Rogowski coils in general. When using the Infinity Sensor in combination with a CSR during a DPT, it becomes quite clear that the integrated signal

from the Infinity Sensor is drifting a lot when compared to the CSR signal. This comes as no surprise, because of the physical nature of the condensed Rogowski style of the sensor. To tackle this issue, two techniques were tried and showed useful results:

1. Estimating the offset-current by measuring the mean of the captured v_{sensor} during one captured frame of the DSO
2. Averaging up to 100 captured and calculated i_{DS} signals

The second method will be discussed in chapter 3.5.5. The first method is based on the recommendations of the Infinity Sensor supplier, University of Bristol, taken from the data sheet of the sensor [11].

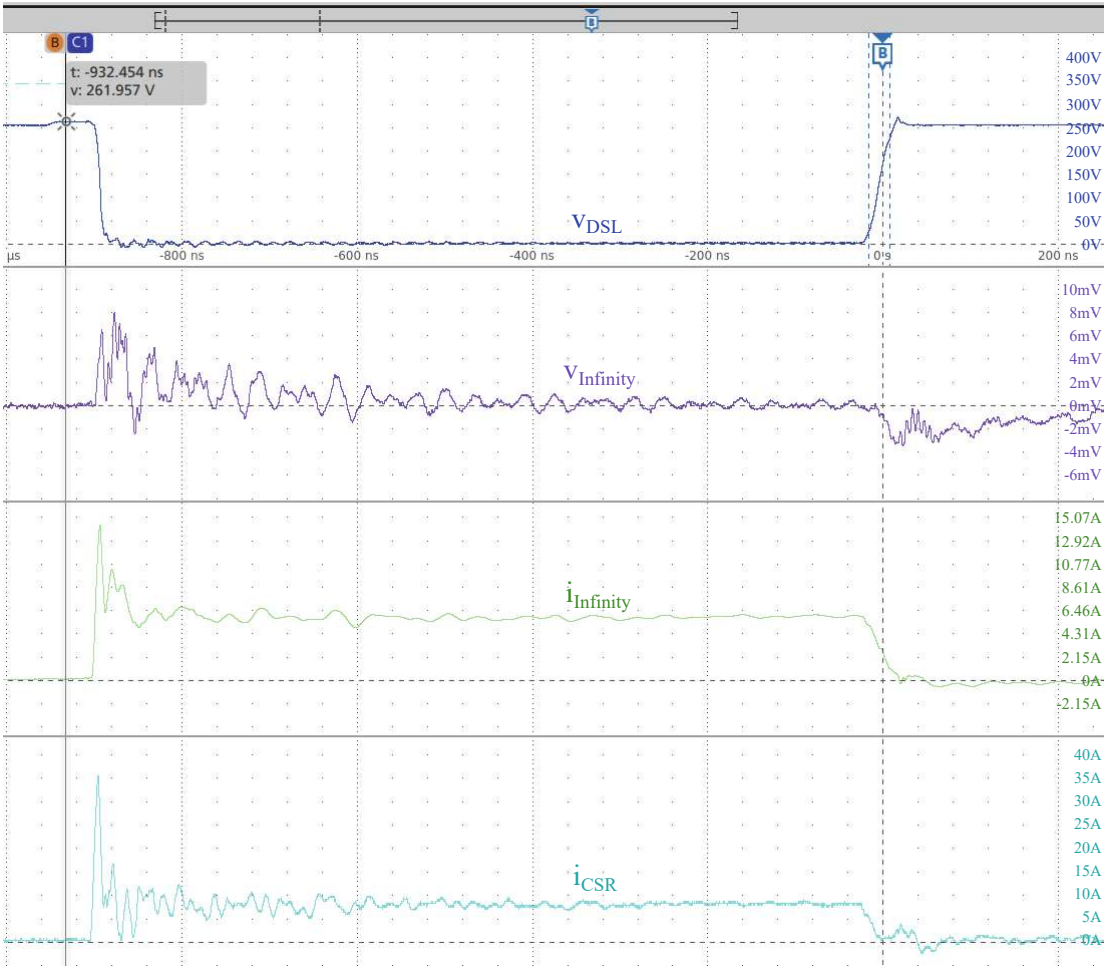


Figure 3.27.: Example of a measurement of the raw sensor signal $v_{Infinity}$ and the integration result $i_{Infinity}$, together with the low-side drain-source voltage v_{DSL} and the current through the CSR i_{CSR}

Figure 3.27 shows the raw voltage signal $v_{Infinity}$ from an Infinity Sensor V2 and the integrated signal $i_{Infinity} = i_{DSL}$ during the on-phase of the second pulse of a DPT. The graph of the Infinity Sensor's voltage signal $v_{Infinity}$ (violet) shows the expected fluctuations caused by the induction due to the change of the measured current below the sensor. The integrated and processed graph $i_{Infinity}$ (green) depicts the calculated current. Comparing this signal to the signal of the CSR i_{CSR}, which was a plain division of $\frac{v_{CSR}}{R_{CSR}}$, leads to the conclusion that both sensors qualitatively measure the same phenomenon and deliver a good fit. Given that both sensors now measure and deliver the right signal, the question arises which measurement is closer to the true value and which sensor gives a more reliable signal, also in terms of bandwidth.

3.5.4. Alternative method: dynamic DC-offset

The solution proposed by the Infinity Sensor V2 data sheet [11] for estimating the DC-offset for the integration of v_S to get i_S is to zoom the DSO to a region where the current i_S is known to be 0 A. Then, a time frame across this 0 A-region, denoted A in figure 3.28, is used to calculate the average value of $v_S \rightarrow v_{fix}$. This value is then used as the constant $AVG3$ in equation 3.41. When using this solution for the DC-offset to take measurements for this thesis, it became clear that this method works for a short amount of time. The best value for the offset is drifting, because of the presence of noise and surrounding influences. Exemplary signals taken by means of this method are shown in figure 3.29, denoted with their respective value of 0 µV, 1000 µV, and 1200 µV. As the blue curves v_{fix} show clearly, the constant offset signals look like they are the sum of the true curve and some scalar product of a constant with time, see equation 3.42. i_S is the measured signal, i'_S is the true signal of the measured current, α is a supposedly constant value, depending on the DC-offset $AVG3$ and t is time.

$$i_S = i'_S + \alpha t \tag{3.42}$$

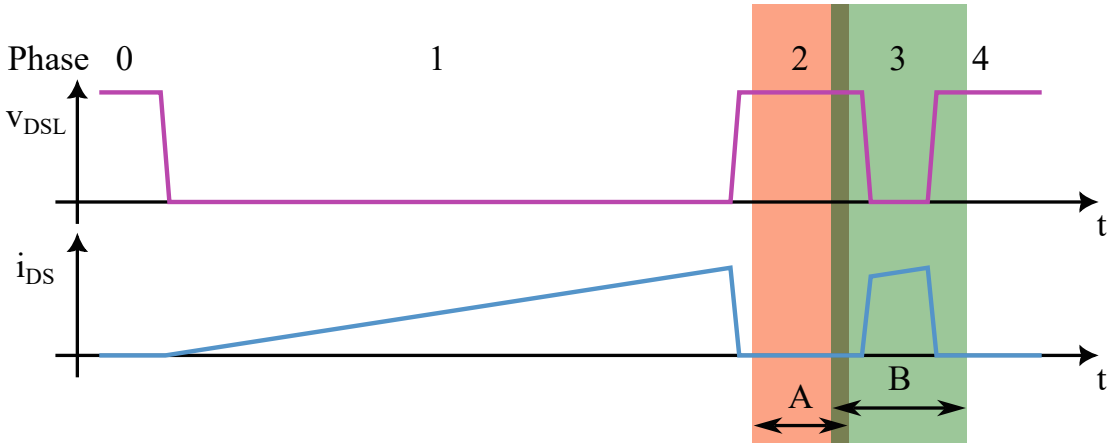


Figure 3.28.: Visualization of the used time frames to measure the DC-offset: A (red) marks the used time frame to determine the constant DC-offset v_{fix} and B (green) marks the time frame which was used to dynamically calculate the DC-offset v_{dyn}

This solution is based on the recommended calculation of the average while no switching is taking place, which means the current is practically constant. But instead of taking the average during a phase of constant current, it is also possible to take the average of v_S across the time span of a switching process. The only requirement for this method to work properly is to capture not only

one but two switching events within the averaging time span. In this thesis, this was done by capturing the second pulse of the DPT in one frame, see figure 3.29. The average is then dynamically calculated based on a measurement-channel of the DSO. This channel uses two cursor positions and calculates the average of v_S between these two cursors. The result of this measurement-channel is used as the DC-offset (AVG3) for the integration-channel of the DSO. Because this measurement-channel is updated dynamically with every trigger of the DSO, the DC-offset is as well repeatedly updated and corrected for the newly changed values. Note that this method only works if both cursors are set to locations where v_S has roughly the same value, predominantly when the current is expected to be 0 A. Otherwise the signal is skewed.

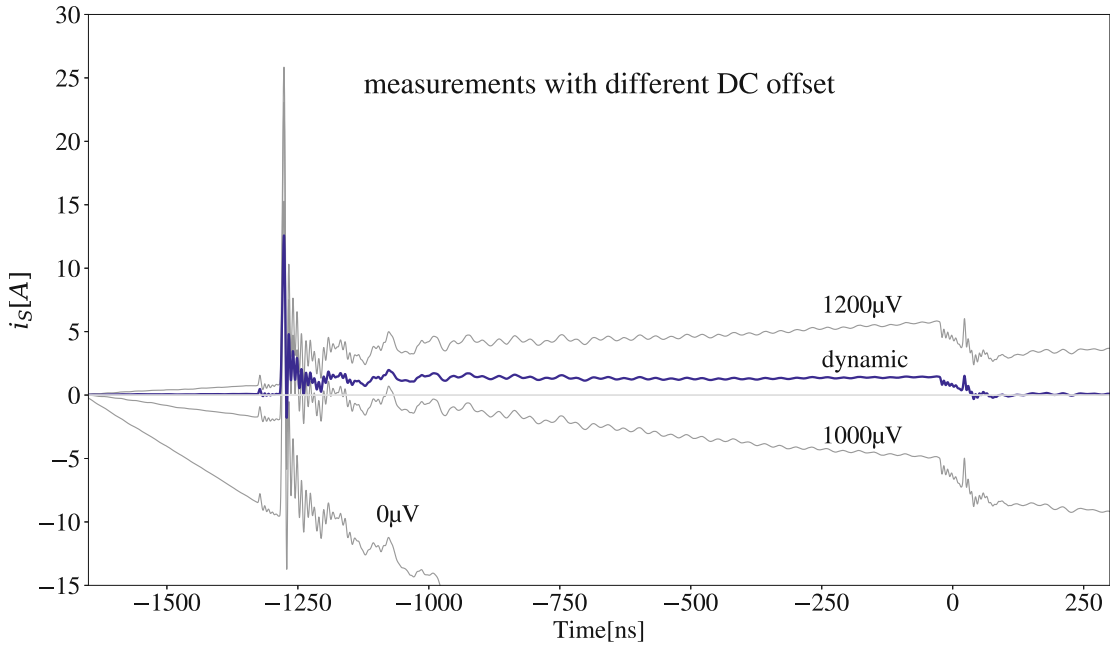
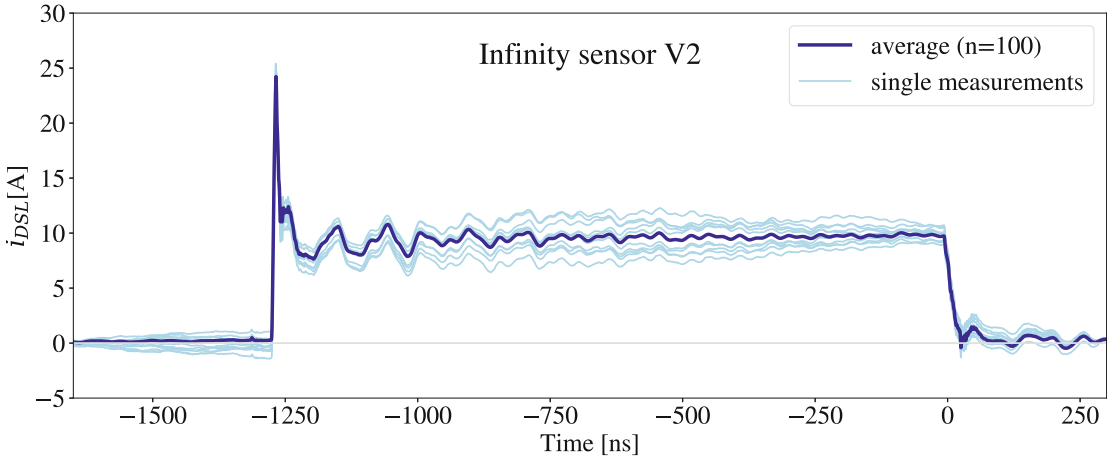


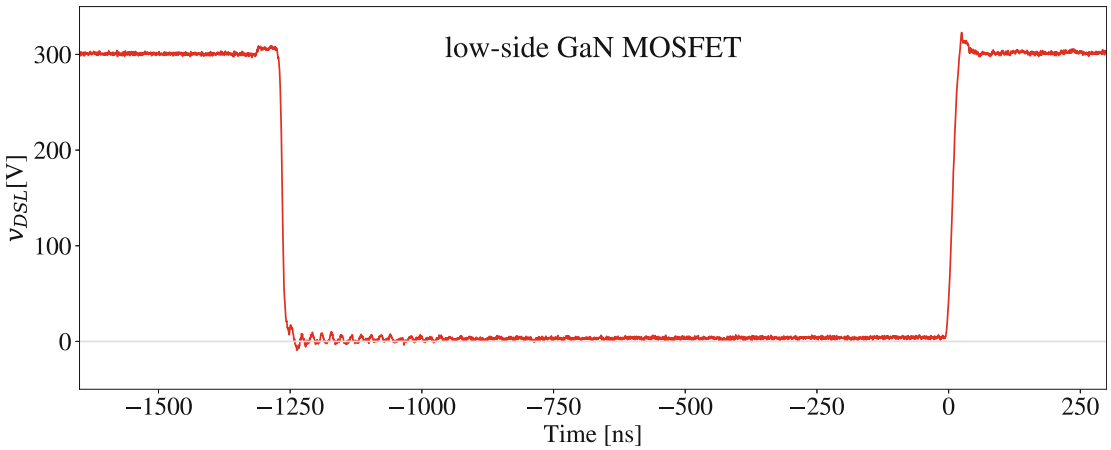
Figure 3.29.: Comparison of four different measurements taken with the Infinity Sensor V2: using constant DC-offset values v_{fix} at the signal integration (grey) and dynamic DC-offset values v_{dyn} (darkblue)

3.5.5. Averaging method

Because the induced voltage at the Infinity Sensor is very small and floating, the measured signal is drifting over time, even on the small scales of the oscilloscopes μs time frame. Additionally, the SNR is also decreasing with decreasing input signals. This means, that any noise from the high di/dt environment of the sensor must be avoided by shielding. Any noise that can't be shielded will add to the voltage signal and make the result look the single measurements in figure 3.30a. When working with periodic measurements of the same phenomenon like the DPT with the Infinity Sensor, averaging can help a lot with eliminating noise from a measurement.



(a) Ten individual samples and the averaged signal (n=100) of the i_{DSL} current signal from the Infinity Sensor V2



(b) Corresponding voltage signal across the low-side GaN transistor

Figure 3.30.: Averaging of the current signal from the Infinity Sensor

Figure 3.30 depicts exemplary measurement data from the Infinity Sensor V2 i_{DSL}, where the light-blue curves show 10 individual signals taken in consecutive DPT pulses. The dark-blue curve shows the average of 100 consecutive samples. The averaging was done by the DSO automatically. The lower diagram depicts v_{DSL} is for reference and showing a single measurement. Because the voltage signal of v_{DSL} was very stable, no averaging was used there. An examination of figure 3.30a shows that the current is fluctuating from each measurement to the next. The general signal form is qualitatively the same, and especially when the current is changing with high di/dt, the deviation of the signals is smaller. The longer the current stays approximately the same, the higher the deviation of the individual signals from the average become.

3.5.6. Software packages

Post processing of measured data and plotting of figures was done by means of the programming language Python 3.12 [44]. Additional packages were utilized for specific purposes, like pandas 2.2.2 [51] for reading and selecting the measurement data from CSV-files. Numpy 2.0.0 [14] was used for the correct calculation of real numbers with floating point arithmetic. Scipy 1.14.0 [54] was used for the numerically integration of measured data and matplotlib 3.9.1 [16] was used for plotting diagrams.

4. Results

4.1. Hardware demonstrators

To test the novel approach of the Infinity Sensor and compare it to a CSR, several PCBs for double pulse testing were produced. A brief overview of the produced PCBs is given in figure 4.1. Some additional iterations of the PCB design were necessary, in order to correct some errors and improve the overall performance of the DPT PCBs. These versions are not listed in this work and the measurement data from testing the predecessor of the final PCBs is omitted as well, due to irrelevance for the conclusions. The first version of the PCB was produced for version 1 of the Infinity Sensor, which was available in two sizes, small and large. For each size, a PCB was manufactured with both the Infinity Sensor alone and in combination with the CSR. Also, a version with only the CSR was produced as well. The Infinity Sensor version 1, small and large, are shown in figure 2.13

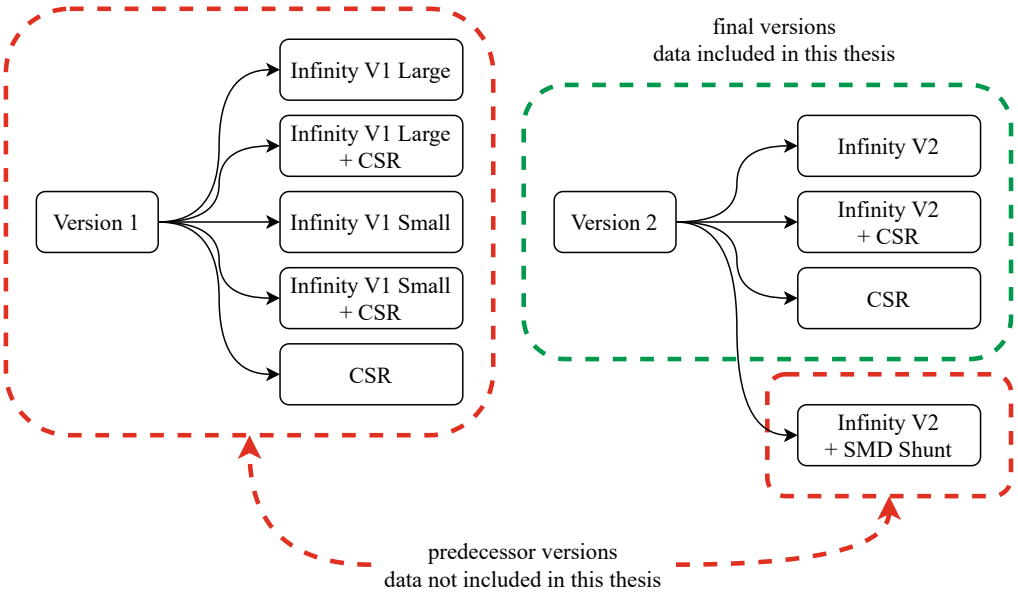


Figure 4.1.: Versions of produced PCBs

4.2. Measured data

After several produced and tested versions of the DPT PCB, a final set of PCBs was produced and tested. This set is based on the same principle design with some variations of the current sensor at the low-side GaN transistor. The presented measurement data in this thesis does not include all the measurements during the development phase of the DPT PCBs. Only a small portion of the overall taken measurements are used for the plots in this thesis, to show the observed phenomena.

4.2.1. Voltage measurements

This section gives an overview of several voltage measurements taken mostly from the low-side drain-source voltage v_{DSL}, focusing on how the measured data is processed and displayed as a reference for the current measurements.

Measuring voltage and current across the transistor is the ultimate objective of a DPT, as these measurements deliver the power losses which enable the evaluation of the switching performance.

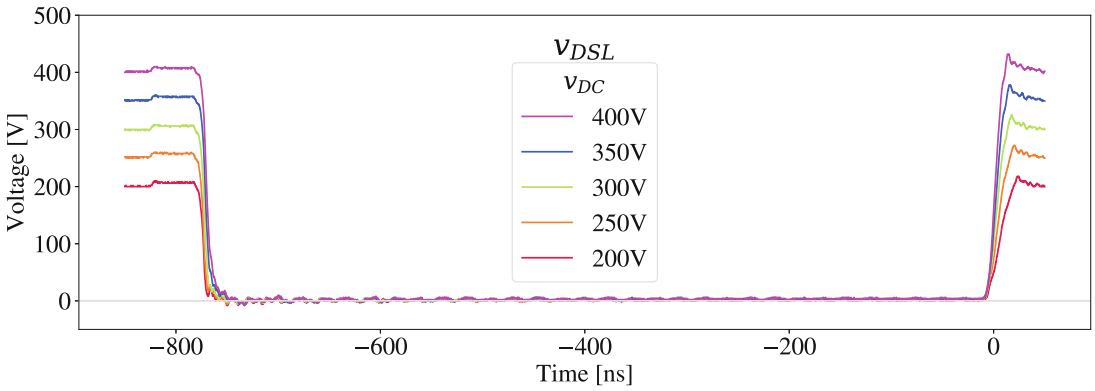


Figure 4.2.: ON-state of the low-side GaN transistor, $R_{Gate} = 10\,\Omega$, $V_{GS-ON} = 6\,\text{V}$, $V_{GS-OFF} = -3\,\text{V}$

Figure 4.2 shows the low-side drain-source voltage v_{DSL} during the ON-state of the low-side GaN transistor for five different DC supply voltages v_{DC}. All five measurements were taken with the exact same setup in consecutive orders, starting at 200 V and increasing by 50 V up to 400 V. All signals of each measurement were captured, processed and stored by the MSO58 DSO. Later, the captured and stored measurement data (CSV-files) were transferred to a PC and post-processed. For the graphs in figure 4.2 to 4.4, the v_{DSL} voltage signals of each of the five

measurements were taken and added to the same file, using trigger voltage, which was the same during all measurements, as a reference ($t = 0\,\text{ns}$).

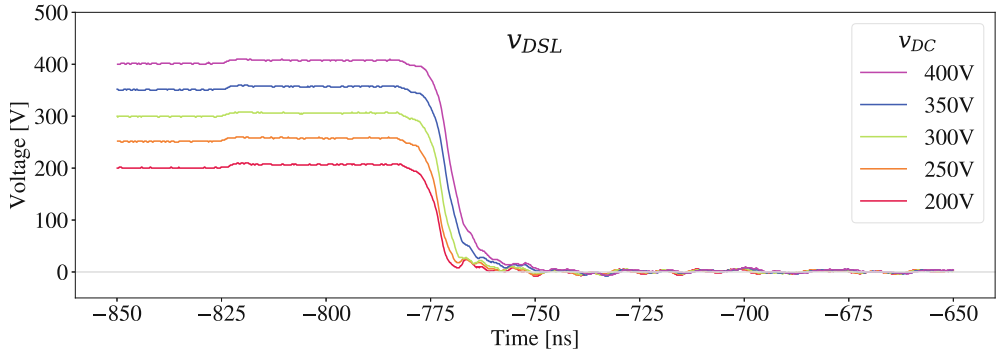


Figure 4.3.: Switching from OFF- to ON-state of the low-side GaN transistor, $R_{Gate} = 10\,\Omega$, $V_{GS-ON} = 6\,\text{V}$, $V_{GS-OFF} = -3\,\text{V}$

Figure 4.3 uses the same measurement data composition but is a zoomed in view on the switching process from the OFF- to the ON-state. Generally, evaluating and improving the switching process of transistors is a very important step in power electronics development. Practically all of the power losses occur during switching and modern power converters feature switching frequencies of up to several 100 MHz. In order to calculate the switching losses, the voltage and current across the transistor need to be measured with sufficient precision to capture all features of the relevant signals. Further details on the power losses will be discussed in chapter 4.2.3.

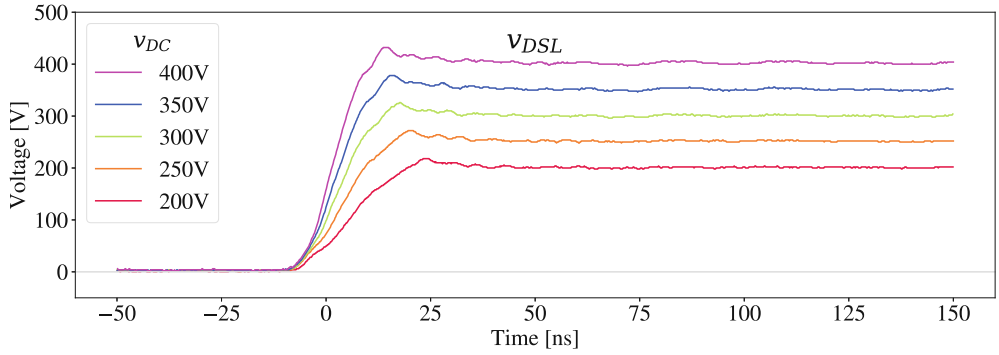


Figure 4.4.: Switching from ON- to OFF-state of the low-side GaN transistor, $R_{Gate} = 10\,\Omega$, $V_{GS-ON} = 6\,\text{V}$, $V_{GS-OFF} = -3\,\text{V}$

Figure 4.4 displays the same detailed zoom on the measured v_{DSL} for the subsequent switching process from ON- to OFF-state. Again, this view is valuable for

evaluating the power losses. All signals in figure 4.4 show a clean rise of v_{DSL} from 0 V to v_{DC} with minor overshooting and oscillation afterwards. The rise time is approximately 20 ns to 25 ns.

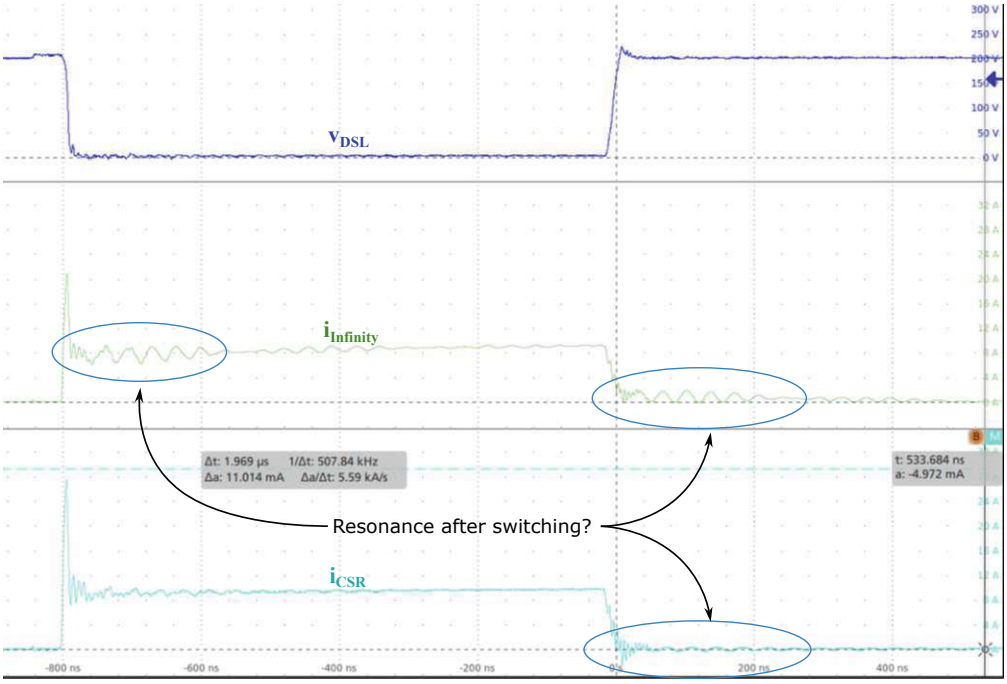


Figure 4.5.: Oscillations of the current signals after switching from OFF- to ON-state and ON- to OFF-state of the low-side GaN transistor

The PCB design and testing for this thesis took several iterations, as the DPT setup was not ready from the first moment. Under these circumstances, the measurements showed different degrees of faulty switching processes, ranging from not working at all to the more interesting partially working examples. Such an example is given in figure 4.5, where the current signals of both sensors show resonance after the switching for approximately 200 ns. Because the voltage signal hardly shows any sign of the same resonance, the depicted resonance likely is an artefact of the measurement. A possible solution to such phenomena is proposed in the outlook.

4.2.2. Current measurements

This subsection focuses on the current measurements taken from double pulse tests. Figure 4.6 shows the current signal from both sensors, the CSR and the Infinity Sensor version 2 at each DC supply voltage level from 200 V...400 V.

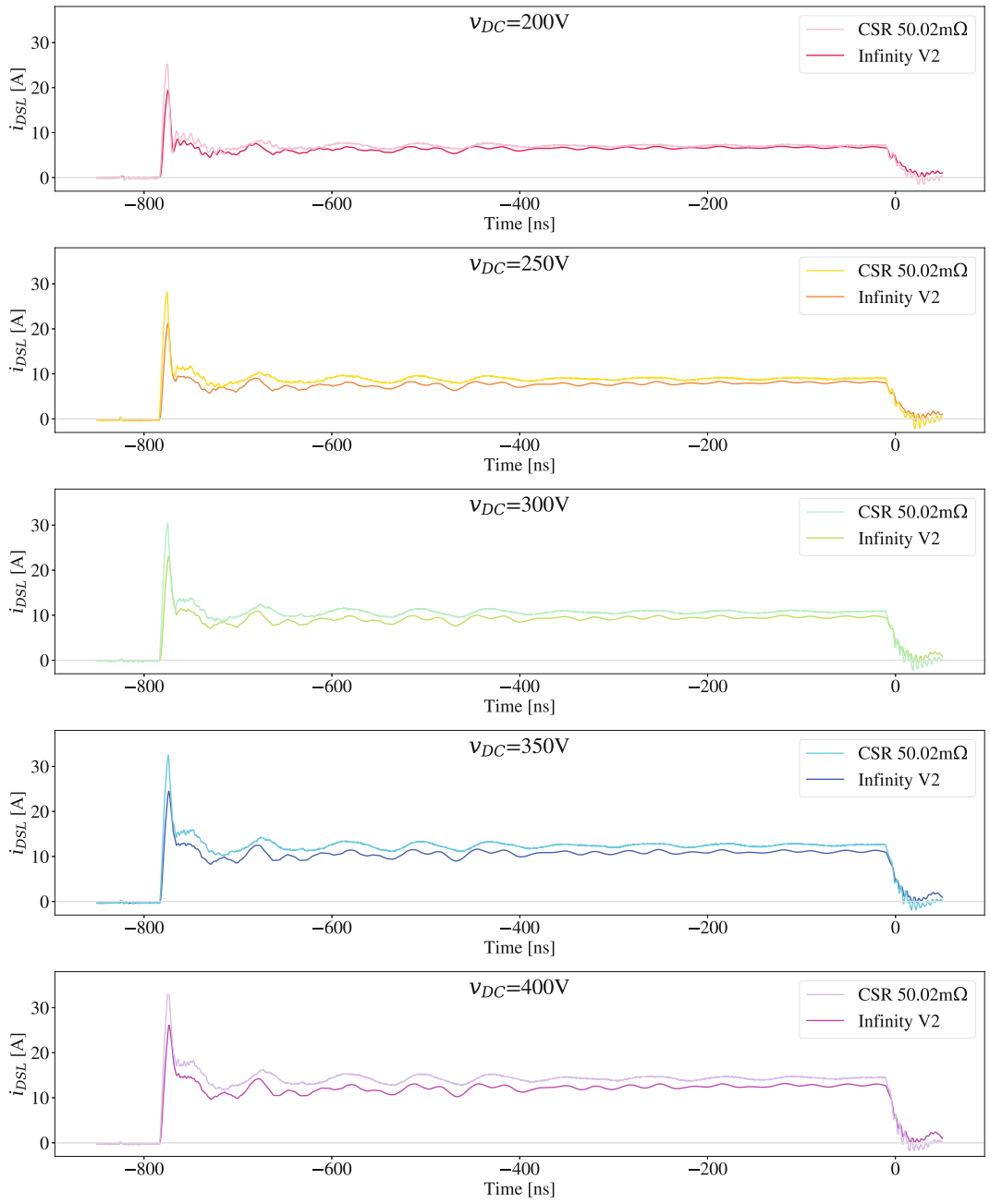


Figure 4.6.: Comparison of the drain-source current signals from the CSR and the Infinity Sensor V2 during the ON-state of the second pulse of the DPT at the low-side GaN transistor for five different DC supply voltages

These comparisons demonstrate that the Infinity Sensor V2 and the CSR deliver equivalent results.

4.2.3. Power losses

If voltage and current measurements across a switch deliver trustworthy signals, the switching power losses can be calculated. As mentioned before, the power dissipation at a switch is of high interest for power electronics development. During switching, both current and voltage across the switch change from 0 to X and Y to 0, or the other way around when switching back. Before and after the switching process, either the voltage or the current is theoretically 0 V or 0 A and no power loss happens, as can be seen in equation 4.1.

$$p_{Loss}(t) = v_{DSL}(t) \cdot i_{DSL}(t) \tag{4.1}$$

The MSO58 DSO offers automatic calculation of the power loss by means of a math-channel, which multiplies the current and voltage signal permanently. This proved useful while working live on the DPT PCB, especially during the prototyping phase. For later measurements captured for this thesis, the power loss was calculated in post processing on a PC with the scripting language python and the matplotlib-library. The DSO-calculated power loss does not include any new information from the measured object itself but offer important live information for the DSO operator. Because the information about the power loss is already contained in the voltage and current signals, the live calculated power loss was not stored additionally. Hence, storage space is saved because the power channel is not included in the CSV file of the DSO export. During post processing and plotting of stored data, the calculation can be redone easily. Once the power loss is calculated, the next logical step is to integrate power over time for a specific switching process, see 4.2, where $E_{On/Off}$ is the total dissipated energy during a switching event. t_1 marks the start of the switching process and t_2 the end. This is where the main advantage of the post processing is coming to effect against the live calculation of the DSO. When working and calculating live on the DSO, every decision and error made is locked in place and can't be changed easily later on, especially when exporting screen shots instead of waveforms (CSV). By post processing, every step can be redone until the calculation and plot fits the desired purpose. Post processing offers convenience when choosing the integration limits t_1 and t_2 for the calculation of the dissipated energy.

$$E_{On/Off} = \int_{t_1}^{t_2} p_{Loss}(t)dt \tag{4.2}$$

Two exemplary plots of switching events are given in figure 4.7 and 4.8. These figures show the current signal i_{DSL} from the Infinity Sensor V2 on top, the voltage across the low-side GaN transistor v_{DSL} in the middle, and the calculated power loss at the transistor p_{Loss} on the bottom. The green area below the p_{Loss}-curve

marks the energy $E_{On/Off}$ dissipated during switching. This amount of energy was transformed to heat and has to be transported away from the transistor by the cooling system and the surrounding PCB components. The evaluation of the power losses during switching is important, because if the dissipated energy is higher than the cooling system capacity, the temperature will rise inevitably until thermal failure of the transistor.

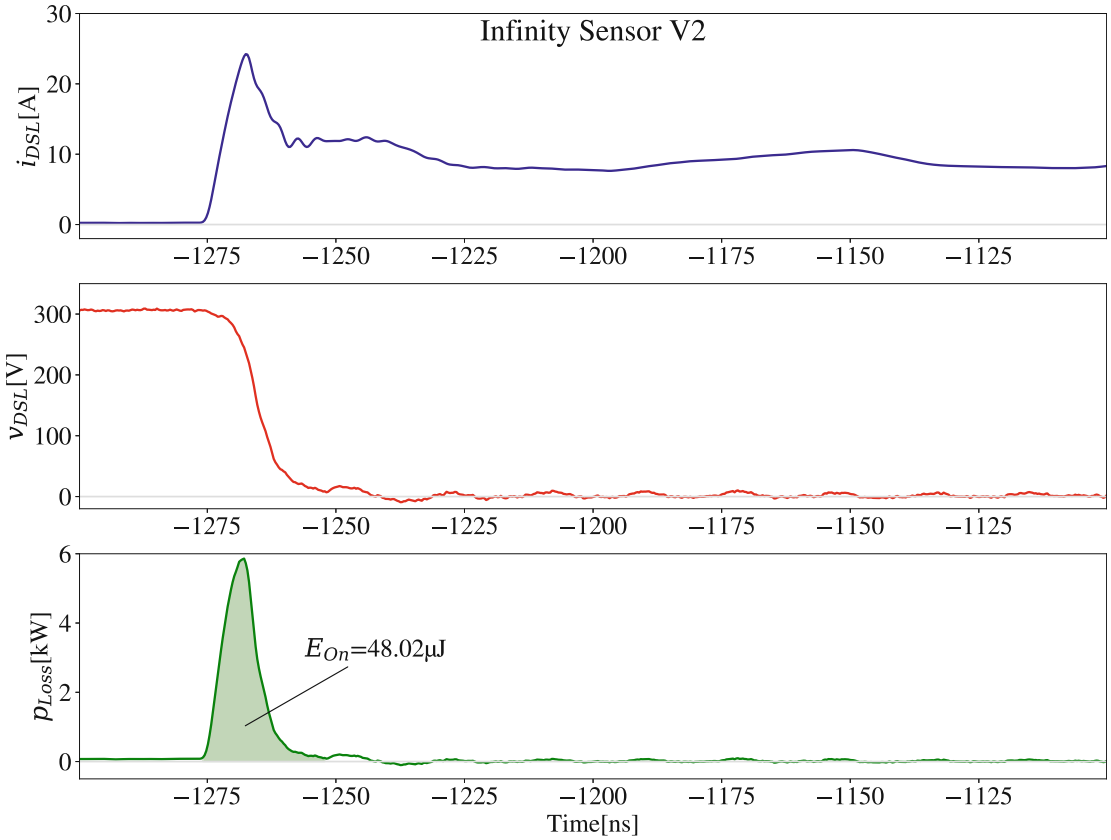


Figure 4.7.: Power loss while switching from OFF- to ON-state of the low-side GaN transistor; top curve shows the current, picked up by the Infinity Sensor V2, second curve shows the voltage measurement across drain and source, and the bottom curve shows the calculated power dissipation

Comparing both transient processes of switching on in figure 4.7 and off in figure 4.8 shows that there is a huge difference in power loss and dissipated energy. While figure 4.8 shows moderate overshooting of the voltage when switching off, figure 4.7 depicts very high overshooting of the current by almost 140 % of the average current during the rest of the ON-phase. The reasons for overshooting are a topic of its own, but these two zoomed in regions of the same DPT pulse were specifically chosen to display the relevance of calculating power loss and dissipated

energy during transient events. Ideally, the areas below p_{Loss} should be as small as possible. When switching to OFF-state during a DPT, the calculated area E_{Off}, see figure 4.8, represents the energy which is transferred to the DC-link capacity. Therefore, E_{Off} only partially represents switching losses, see equation 4.3.

$$E_{Off} = E_{OSS} + E_{resistive} \tag{4.3}$$

It consists of the output capacitance stored energy $E_{OSS} = 17\,\mu J$ ([52]) and actual resistive losses due to the resistance in the commutation loop. In the illustrated chase in figure 4.8, the resistive losses sum up to approximately $8\,\mu J$.

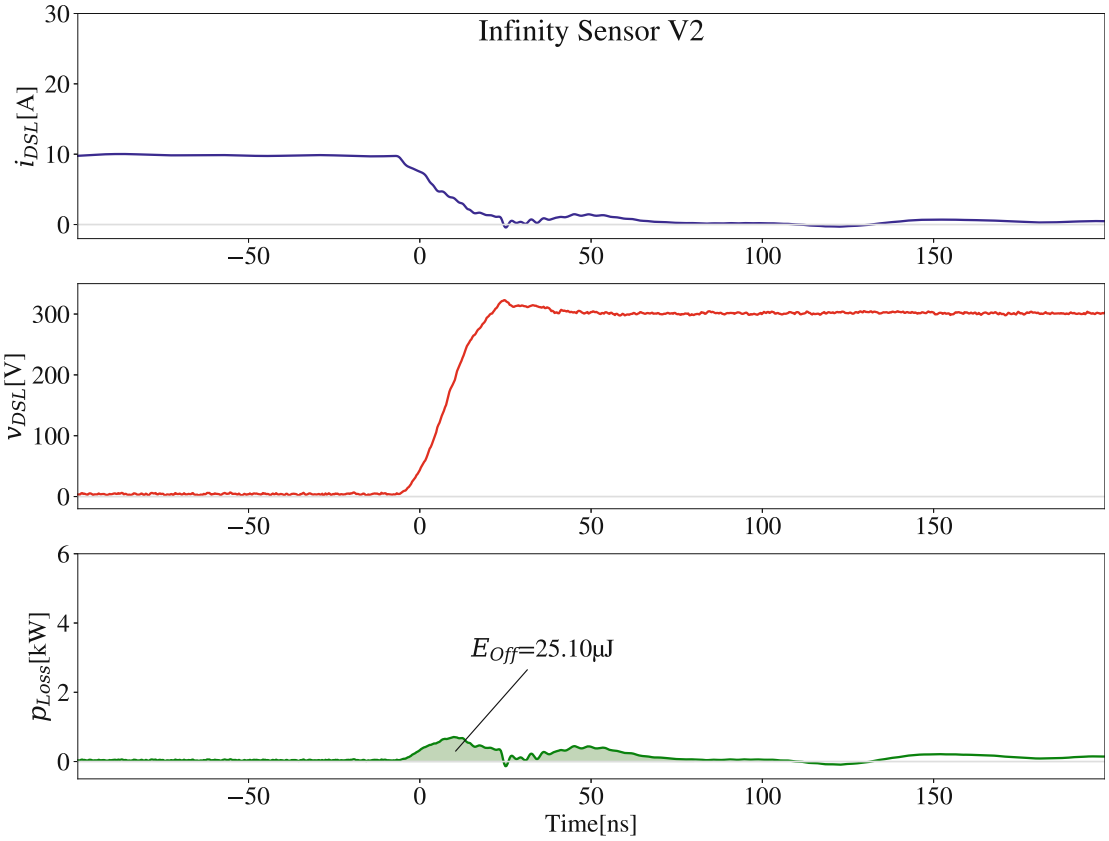


Figure 4.8.: E_{Off} while switching from ON- to OFF-state of the low-side GaN transistor; top curve shows the current, picked up by the Infinity Sensor V2, second curve shows the voltage measurement across drain and source, and the bottom curve shows the calculated power dissipation

Besides measuring the current signals during a DPT, the drain-source voltage v_{DSL} was also picked up directly by means of the oscilloscope and the single ended 1 : 100 voltage probe, described in section 2.3 and 3.3.2. Figure 4.9 shows these

drain-source voltages during the second pulse of the DPT at different DC voltages v_{DC}. A specific region is marked in black, indicating a feature of all voltage curves right before switching on at $\sim -800\,\text{ns}$. At $-810\,\text{ns}$ v_{DSL} rises in all curves by 6 V. Before this rise, the high-side GaN transistor is in its conductive ON-state. When the gate driver switches the ON-state from high to low-side and vice versa, it uses a fixed dead time t_{DT} of 20.88 ns, see equation 3.11 in section 3.2.6. By doing so, a straight short circuit of v_{DC} is prevented, because both transistors are switched off for the duration of t_{DT} before the ON-state is activated on one of them. As a result, a 6 V rise of v_{DSL} can be observed. During this short time, v_{DSL} is equal to $\sim v_{DC}$.

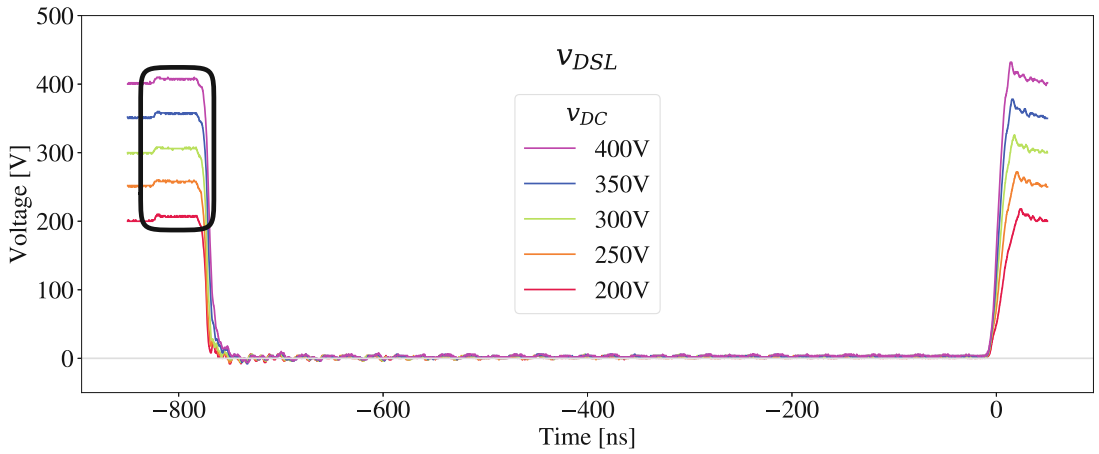


Figure 4.9.: Phenomenon of high-side GaN switching off before low-side transistor switches, observable at the low-side drain-source voltage v_{DSL} at five different DC supply voltages v_{DC}, $R_{Gate} = 10\,\Omega$, $V_{GS-ON} = 6\,\text{V}$, $V_{GS-OFF} = -3\,\text{V}$

5. Discussion

After the first iterations of the DPT PCB with the CSR and Infinity Sensor V1, the DPT worked properly and both sensors delivered current signals of the same shape and roughly the same values. Both sensors were off by roughly 10 % in the best case. The Infinity Sensor V1 was tested on several, identical PCBs and delivered a wide range of results. Naturally, there are some variations between the PCBs, because the used components come with tolerances. Despite using specifically tight component tolerances, deviations between the PCBs remain. The resulting variations of the current measurement results will always consist of a combination of PCB and component tolerances and the effects of the Infinity Sensor. At first it was unclear if the high variety of the results was mainly caused by the sensor or the component and soldering tolerances of the PCBs. After the second version of the Infinity Sensor became available, the DPT PCB was adapted for it and tested. The new version with the sensor-embedded current-carrying copper trace delivered very reliable results. This made clear that the hitherto wider variations were caused by either the production tolerances of the Infinity Sensor V1 or the less reproducible application of the sensor to the PCBs.

1. **Comparability:** Despite the largely improved results with the second version of the Infinity Sensor, each variant of the DPT PCB had its own unique and unknown combination of component values within the known tolerances embedded. This means that every comparison between CSR and Infinity Sensor comes with this unknown degree of uncertainty. As an attempt to escape these limitations, a PCB was produced where both sensors were used in series. These results are given in figure 4.6. The only remaining issue with this PCB is that the undisturbed current, without any sensor, has to flow through not only one but two sensors with added insertion impedance. The next step to counter this issue would be to produce a DPT PCB where both sensors can be used successively. By doing so, each sensor would be embedded in the same PCB with the exact same peripheral components. Thus the tolerance issues when comparing the sensors would be fixed. This PCB is part of the future work on this topic.

2. **Infinity Sensor restrictions:** The data sheet of the Infinity Sensor delivers specific instructions on how and where to use it. These specifications come

as no surprise, when the sensor is used and the need to carefully post-process the signal becomes evident. Unlike the CSR, where a simple scalar division delivers the current signal in any situation within the bandwidth, the Infinity Sensor works well in specific situations and can be used to evaluate switching losses of GaN transistors.

3. **Infinity Sensor calculation:** The voltage signal from the Infinity Sensor needs to be integrated to deliver the current signal. Naturally, the DC-offset is lost in such a sensor. The data sheet instructions deliver a method for the approximation of this offset by measuring the average of the sensor signal over a period of constant current. This fixed value is then subtracted during the online integration of the signal. This method requires several tries to find a fitting value for the DC-offset and, depending on the amount of noise and changes to the environment of the test setup, needs to be updated often, in order to deliver reliable results. Possibly, the integration of the sensor and the entire test setup has several flaws. Without these flaws, the method described in the data sheet would probably work more reliably.

4. **Infinity Sensor dynamic method:** Nevertheless, an even better, dynamically updated method was found when operating the DPT with the Infinity Sensor for this thesis. Modern DSOs offer the possibility to dynamically capture the mean value (v_{dyn}) of a signal and use the constantly updated v_{dyn} in the subsequent math-channel. All results of this thesis are based on this new method, except for figure 3.29, were the comparison of these methods is discussed.

5. **Infinity Sensor averaging:** Despite these measures, the current signal is prone to noise and fluctuates substantially compared to the voltage signal of v_{DS} and the current signal i_{CSR}. Because the DPT is not measured once, but was triggered constantly with 100 Hz, the already processed current signal from the Infinity Sensor was averaged 100 times as a final step. The result is a clear representation of the current, shown in figure 3.30a. This figure also shows that the Infinity Sensor works best, when di/dt is high, and deviations increase over time, when di/dt is close to 0.

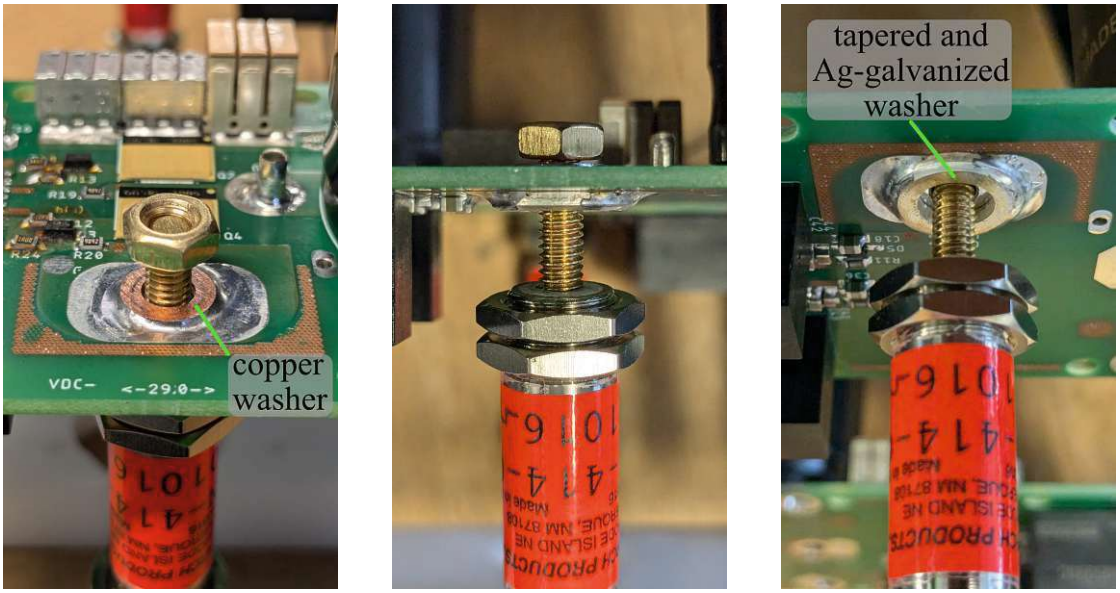
6. **CSR:** When using a CSR for current measurements in this thesis, the main advantage was that the current signal i_{CSR} is directly proportional to the v_{CSR} signal picked up by the oscilloscope. Additionally, the bandwidth of the CSR is high enough to deliver reliable results up to 2 GHz. On the downside, the CSR comes with an insertion inductance of $\sim$ 2 nH, which is an order of magnitude higher than the 200 pH of the Infinity Sensor V2.

Also, the insertion resistance of 10 mΩ...50 mΩ is higher than the Infinity Sensor's 4.2 mΩ.

7. **CSR installation:** Another disadvantage of the CSR is displayed in the images of figure 5.1, where a method of firmly contacting the CSR with the PCB is shown. In figure 5.1a the partially unscrewed CSR is shown as well as a copper washer, which was soldered to the PCB and flushed with a file to improve contact issues between the M4 nut of the CSR and the tinned copper top layer of the PCB. A similar approach was taken at the bottom side of the PCB, where a tapered and Ag-galvanized washer was used to improve the electrical contact between the CSR's GND-M10 nut and the copper bottom layer. In some cases, a CSR was usable without adding any washers at the top and bottom copper layers. Nevertheless, the process of unscrewing a CSR and re-installing it or using a different CSR did not produce reliably reproducible results. Using the washers without soldering them to the PCB improved reproducibility, but best results were achieved with soldered washers. The disadvantage of using washers on both sides is the added resistance and inductance to the already high insertion values of the CSR compared to the Infinity Sensor.

8. **CSR spacial requirements:** Because the T&M Research CSR measures 57 mm in length and 10 mm in diameter, the installation of the CSR requires substantial space on the PCB's dimension of 111 mm x 50 mm. Because of its dimensions and also its relatively high price of $\sim$ 400 € compared to the $\sim$ 20 £ for the Infinity Sensor V2, the CSR is mostly used in prototypes and development PCBs but not in finished products. Figure 5.1a gives a very good impression of the size of the CSR, where the M4 nut takes up approximately the same area on the PCB as one of the GaN transistors. A solution to the excessive use of PCB real estate and high insertion impedance of the CSR is offered by the ultra fast current shunt (UFCS) and will be discussed in the outlook 6.3.

9. **CSR de-embedding:** Because of the insertion impedance of the CSR, the measured i_{CSR} signal does not precisely represent the current i_{DS}, which would flow without the CSR. By modelling the impedance of the CSR, [61] showed that the CSR can be de-embedded from the setup and a better representation of i_{DS} can be derived. The results in this thesis are entirely based on measurements without de-embedding, which will be part of future work on this topic.



(a) Top view (b) PCB edge (c) Bottom view

Figure 5.1.: Images of soldered and faced washers on the top and bottom side of the PCB to accommodate the CSR

6. Outlook

For the facilitated test setup, some improvements would have been possible but were not implemented for the measurements for this thesis, because of time and cost limitations. These are:

- **High bandwidth voltage probe:** Some voltage probes offer a bandwidth above the used 500 MHz and 800 MHz for this thesis. The downside of these high-bandwidth probes is that they usually are offered with 1 : 10 attenuation, which is too low for the $v_{DC} = 400\,\mathrm{V}$. High-bandwidth probes with higher attenuation are costly and were not available during the measurements for this thesis.

- **Isolated voltage probe:** Isolated voltage probes with high bandwidth and attenuation are desirable devices in power electronics development. They are relatively new and costly, because they facilitate highly specialized optical fibres for signal isolation and power supply on both sides of the isolation barrier. Such an isolated voltage probe is the Tektronix isoVu [20], which would allow simultaneous and potential-independent measurements of signals like v_{DSH}, v_{DSL}, v_{GSH}, and v_{GSL}.

- **Cable length:** Generally, all measured signals were connected to the DSO by coaxial cables of roughly the same length. Nevertheless, there were some deviations because of coupling issues with individual sensors. For example, the Infinity Sensor had an additional 20 cm cable length because of the adapter from the sensor's MHF4 connector to the SMA connector.

- **PCB motherboard:** To improve comparability of different sensors, one PCB-motherboard with fixed components tolerances could be used. The only thing to be changed when taking measurements for different sensors should be a separate small PCB-section with the individual sensor.

6.1. N-pulse test and PWM-ramp

The authors in [15] propose two improved methods based on the DPT to better evaluate the characteristics of GaN devices. Both tests are adapted to better represent the continuous operation mode of the WBG devices. Figure 6.1 shows a conceptual comparison of the three different test modes. The gate-source voltages of the tested low-side transistor are shown in comparison. The first curve is the already presented DPT mode, which was used for this thesis. The first pulse integrates the current up to the desired value and the second pulse is the actual test for the low-side power device. Like described in [15], this test does not properly simulate switching process of the transistor like it would happen in a continuously switching power converter. The switching history of these devices has a significant effect on the n-th switching pulse. In a real power converter, the WBG device would be switched continuously with high frequency. After the initial boot up the power transistors will reach a steady state after some switching processes.

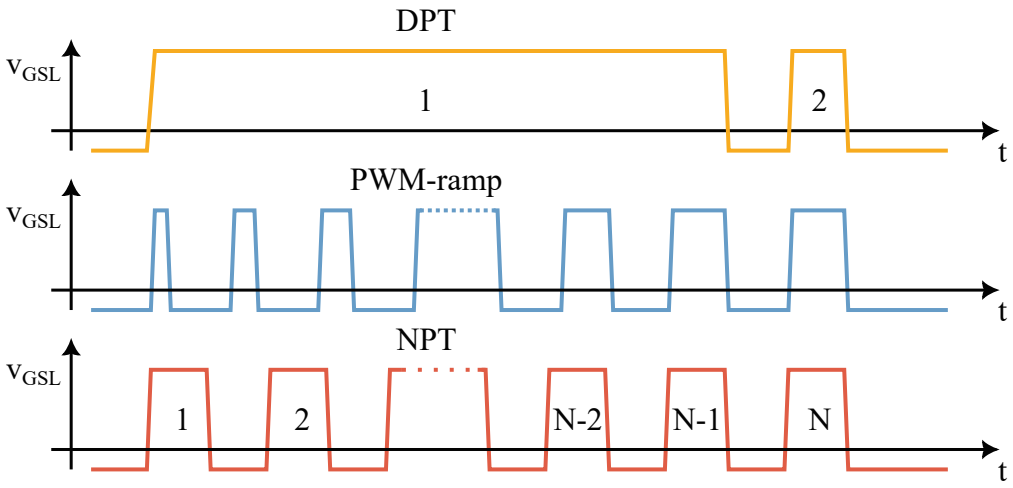


Figure 6.1.: Comparison of v_{GSL} for double pulse test, PWM-ramp, and N-pulse test

The PWM-ramp and NPT try to mimic this effect. The PWM-ramp, illustrated by the blue curve in figure 6.1 starts with very short ON-pulses and the duty cycle is increased with every pulse over roughly the duration of the first pulse of the DPT until it reaches 50 % the final test pulse. The NPT features N equally spaced pulses with a duration of the final test pulse. The duration of both newly proposed methods before the final test pulse is adjusted in such a way that the final pulse does not differ from the preceding pulse. The authors in [32] further refined a test method for SiC devices in MV-applications $> 1\,\mathrm{kV}$.

6.2. Assessment of the commutation loop inductance

In [12] Harry Dymond describes a method to determine the power loop inductance of a switching cell by measuring the ringing frequency of the voltage signal during a specific time frame. This time frame starts when the low-side GaN transistor turns off and stops before the high-side GaN transistor turns on. See −5 ns to 50 ns in figure 6.3. During this time, the two output capacitances of both GaN transistors are in series and resonate with the parasitic inductance of the power loop, causing the observed ringing of the v_{DS} voltage signal. The same phenomenon has been observed during measurements for this thesis and offers an opportunity for further investigation. A challenge when analyzing this signal for the resonance frequency of the v_{DS} voltage signal is the high bandwidth necessary to accurately pick up the signal within the limitations of Shannon's theorem [47]. The voltage probes used in [12] are given in table 6.1.

Signal	**Probe**	**Bandwidth**	v_{max}
v_{DS}	PMK PHV1000	400 MHz	1 kV
v_{GSHS}	Tektronix IsoVu TIVH08	1 GHz	2.5 kV
v_{GSLS}	Tektronix TPP1000	1 GHz	300 V

Table 6.1.: Probes used to derive ringing resonance frequency in [12], v_{GSHS} = gate-source voltage on the high side GaN transistor, v_{GSLS} = Gate-Source voltage on the low side GaN transistor, see figure 6.2

Figure 6.2 shows which voltages measurements were taken in [12] by means of the probes, listed in table 6.1.

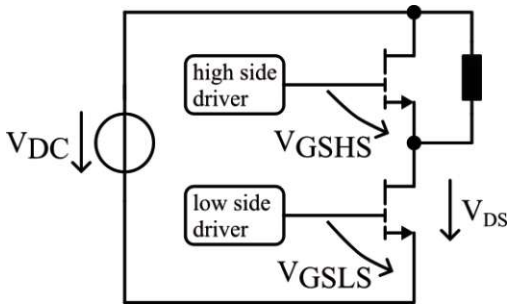


Figure 6.2.: Simplified schematic of the DPT half bridge with assigned voltages

Figure 6.3 shows an exemplary measurement from this thesis, where the ring-

ing of the signal during and after switching is apparent. In future work, this phenomenon could be measured with a voltage probe, which features a higher bandwidth.

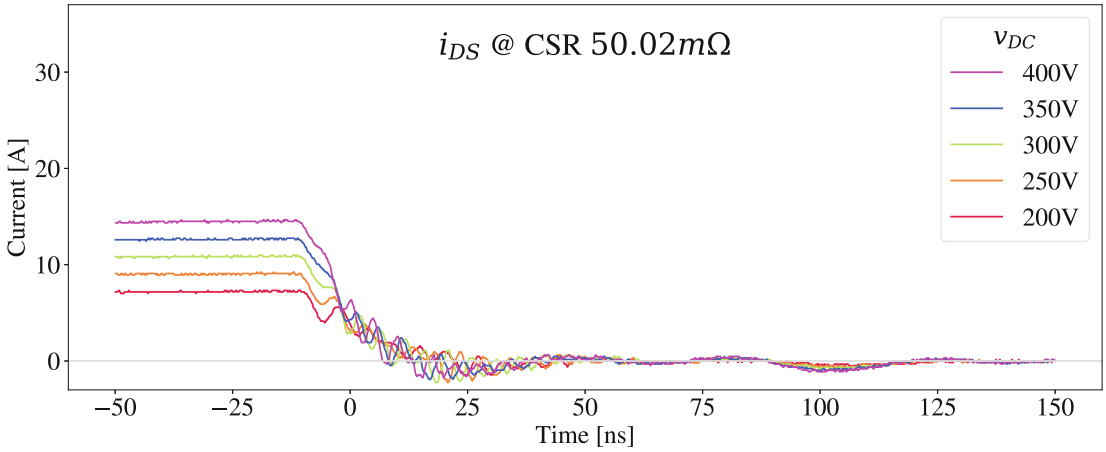


Figure 6.3.: Exemplary measurement with ringing phenomena after switching low-side GaN transistor OFF

The obtained measurements can be used to approximate the commutation loop inductance L_{loop} according to equation 6.1 [12], where f_0 is the measured resonance frequency and C_{tot} is the series capacitance of the used GaN devices.

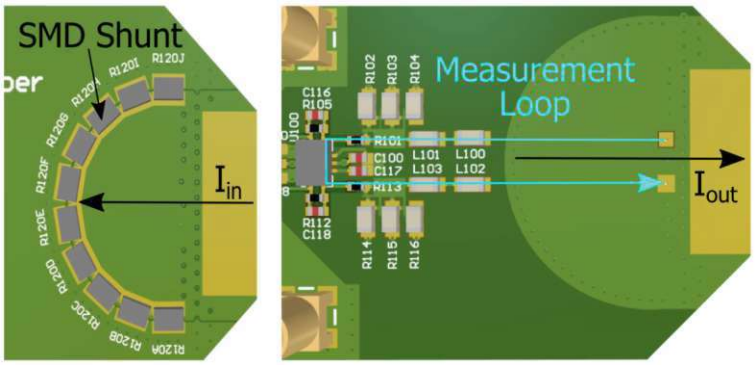
$$L_{loop} = \frac{1}{4\pi^2 f_0^2 C_{tot}} \tag{6.1}$$

The resonance frequency $f_0 = 180\,\text{MHz}$ in figure 6.3 and $C_{tot} = 57\,\text{pF}$. Applying these values in equation 6.2 delivers a loop inductance of $L_{loop} = 14\,\text{nH}$.

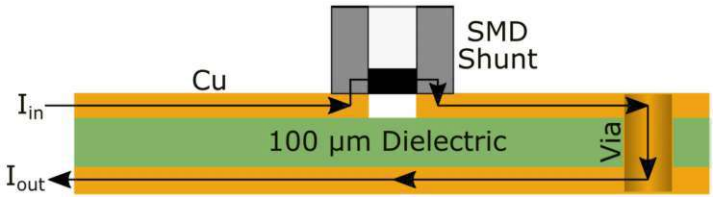
$$L_{loop} = \frac{1}{4\pi^2\,(180\,\text{MHz})^2\,57\,\text{pF}} = 14\,\text{nH} \tag{6.2}$$

6.3. Ultra fast current shunt (UFCS)

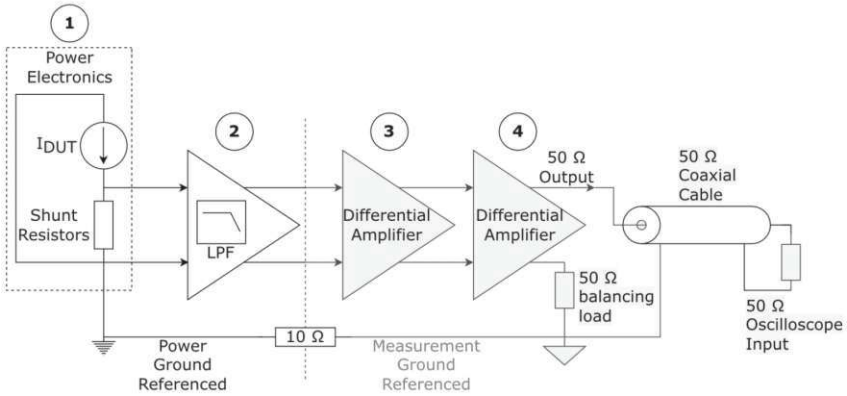
Luke Shillaber proposed a new design of a coaxial shunt resistor, specifically tailored for the needs of power electronics development, see [49].



(a) Concept PCB of the UFCS-I, top view on the left and bottom view on the right side, taken from [49]



(b) Concept PCB of the UFCS-I, cross section of the PCB-tip, showing the two layer version, taken from [49]



(c) Outline of the proposed current measurement setup with differential amplifier and low pass filter, taken from [49]

Figure 6.4.: Concept of the UFCS-I, drawings taken from [49]

Figure 6.4 shows the insertable version of the proposed UFCS. SMD shunt resis-

tors are arranged in a semi-circle on the left side of figure 6.4a and on the right side the measurement circuitry is shown on the PCB. The functional block diagram of this circuit is depicted in figure 6.4c, consisting of a low pass filter and differential amplifiers. Figure 6.4b shows the cross section of the UFCS. The current flows radially outwards on the top side of the PCB, passing through the SMD shunt resistors, after which the voltage is picked up by the measurement system. To partially compensate the mutual inductance of the shunts, the current is then fed through the vias to the bottom side of the PCB, where the current flows in the opposite direction.

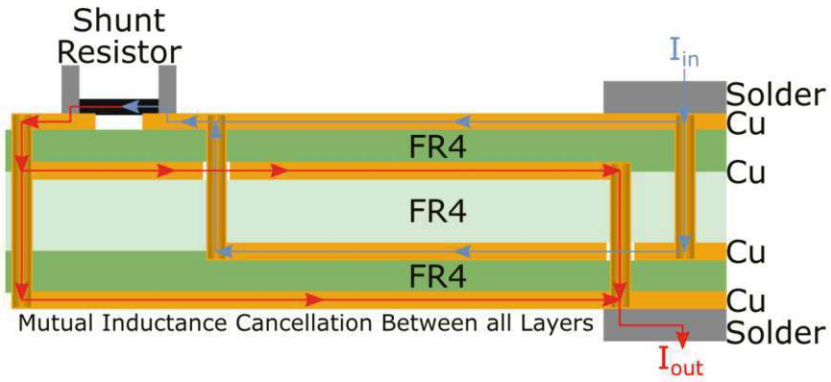


Figure 6.5.: Improved UFCS-I composition with 4 instead of 2 layers, resulting in partial cancellation of the mutual inductance, image taken from [49]

An improved version of this technique was presented in [49], shown in figure 6.5. Here, the mutual induction compensation is improved by using 4 instead of 2 PCB layers. Due to the reduced distance between the current carrying layers, the compensation of the mutual induction is increased, compared to the version shown in figure 6.4. Besides the insertable UFCS, an embedded version was also presented. The embedded version is even more optimized and thus offers less insertion induction than the insertable UFCS. The measured and calculated values of the two proposed systems are given in table 6.2, which was taken from the same paper. There, also other relevant current measurement probes for high bandwidth, low insertion impedance current sensing are presented, including the Infinity Sensor and the CSR.

Table 6.2.: Comparison of current measurement probes, taken from [49]

Probe	**Type**	**Quoted Bandwidth**	**Insertion inductance**	**Rise time**	**DC capable**
T&M SDN-414-10 [3]	Coaxial Shunt	2 GHz	5 nH-7 nH	180 ps	Yes
PEM CWT Mini 50HF [53]	Rogowski Coil	50 MHz	Application Dependent	12.5 ns	No
University of Bristol Infinity Sensor [56]	Rogowski Coil	225 MHz	200 pH	1.56 ns	No
Dresden University of Technology SMD Shunt [37]	SMD Shunt	Not Given	<500 pH	N/A	Yes
Integrated Current Measurement [57]	Pick-Up Coil	Not Given	<330 pH	N/A	No
Cambridge University Compensated Shunt [48]	SMD Shunt	150 MHz	<600 pH	2.33 ns*	Yes
Surface Mount Coaxial Shunt Resistor [62]	SMD Shunt	Up to 2.23 GHz***	120 pH	Not Given	Yes
Cambridge Ultra Fast Current Shunt Embedded (UFCS-E) [49]	SMD Shunt	1.55 GHz	~ 20 pH	355 ps	Yes
Cambridge Ultra Fast Current Shunt Insertable (UFCS-I) [49]	SMD Shunt	1.48 GHz	260 pH	355 ps	Yes

6.4. Miniature fibre optical current sensor

Like discussed in chapter 2, the Faraday effect is an additional yet almost unused phenomenon in current sensing technology. The other two, well established technologies for sensing electrical currents with the electrical resistance and the electromagnetic induction have some disadvantages for the application in PCBs with WBG semiconductors. When using the electrical resistance for current sensing, the main disadvantages are that the measurement is not galvanically isolated from the measured current and the added resistance for the measurement alters the characteristic of the circuit. Electromagnetic induction allows isolated measurements and comes without added resistance. Nevertheless, every electromagnetically coupled sensor comes with some insertion inductance for the measured circuit. Many of these current sensors impose an insertion inductance, which is

too high for the intended purpose of high-bandwidth current sensing. The Infinity Sensor is one of the few electromagnetically coupled sensors with acceptable insertion inductance [49], [56]. Fibre optical current sensors (mFOCS) use the Faraday effect to measure the electrical current.

The company ABB already released a commercially available FOCS-product to measure the current in high voltage substations [29] and [10]. This sensor for currents in the range of kA is specifically made for high voltage applications and respectively has dimensions ranging from $\sim 10\,\mathrm{cm}$ to $1\,\mathrm{m}$ when attached around the copper bars of a high voltage substation. The main objective of this sensor is providing galvanic isolation for the current measurement. For the application in power electronics, the galvanic isolation is also important, but the voltages and currents are much lower. The ABB sensor also is not optimized for high bandwidth as desired in power electronics.

Several patents and books by Reiner Thiele describe improved methods to use the Faraday effect for measurements of currents down to mA and with higher precision. Figure 6.6 shows one of these concepts, where the circular polarization is used to measure the current i. Two optical fibre coils are used to double the efficiency of the Faraday effect and to automatically eliminate the birefringence. Details can be found in [42] and offer interesting options for future sensor development to be applied in power electronics.

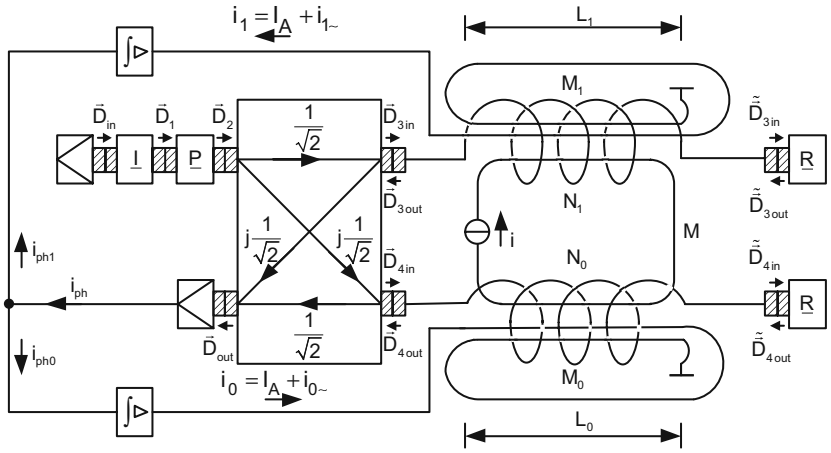


Figure 6.6.: Optical components of the FOCS with circular polarized light and control loop, taken from [42]

7. Acknowledgement

This thesis took a while from start to finish.
For people supporting me, my gratitute shall not diminish.
Representative for all of them, I'd like to mention a few. I thank my professor Ao.Univ.Prof. DI Dr.techn. Martin Gröschl for supervising my thesis. I'm thankful towards the Austrian Institute of Technology for offering the opportunity to work on this thesis and supplying all necessary hardware and software. Especially, I'd like to thank my supervisor Univ.-Prof. DI Dr.techn. Markus Makoschitz for proposing the topic and providing technical guidance as well as continuous feedback. I thank Sumanta Biswas for offering technical support and prior work, which used to develop the hardware for this thesis. I'm grateful to Gudrun Offenberger, Michaela Hatzenbichler, and Stefan Florian Mayer for proofreading and their enduring emotional support. Thank you very much!

Bibliography

[1] Semiconductor Today, Juno Publishing and Media Solutions Ltd, Suite no. 133, 20 Winchcombe Street, Cheltenham, GL52 2LY, UK. URL: https://www.semiconductor-today.com/news_items/2011/JAN/CREE_180111.htm (visited on 07/01/2024).

[2] URL: https://www.tandmresearch.com/index.php?mact=ListIt2Products,cntnt01,detail,0&cntnt01item=series-sdn_2&cntnt01template_summary=Side&cntnt01returnid=19 (visited on 07/01/2024).

[3] URL: https://www.tandmresearch.com/index.php?mact=ListIt2Products,cntnt01,detail,0&cntnt01item=series-sdn-414&cntnt01template_summary=Side&cntnt01returnid=19 (visited on 07/01/2024).

[4] URL: https://research-information.bris.ac.uk/en/projects/high-bandwidth-sensing-for-wide-bandgap-power-conversion-2 (visited on 07/01/2024).

[5] URL: https://www.i-pex.com/product/mhf-4 (visited on 07/01/2024).

[6] DrBob (assumed). *Polarization rotation due to the Faraday effect.* URL: https://en.wikipedia.org/wiki/Faraday_effect#/media/File:Faraday-effect.svg (visited on 07/25/2024).

[7] Lidow Alex et al. *GaN Transistors for Efficient Power Conversion.* article. EPC Efficient Power Conversion Corporation, 2012. URL: https://epc-co.com/epc/campaigns/WhatIsGaN/GaN%20Transistors%20for%20Efficient%20Power%20Conversion-chapter-1.pdf (visited on 07/01/2024).

[8] Luque Alfredo. *Schematic drawing of a Rogowski coil used as an AC current sensor, and connected to an integrator circuit to obtain an output voltage proportional to the instantaneous value of the current i(t).* URL: https://commons.wikimedia.org/w/index.php?curid=14135709 (visited on 07/01/2024).

[9] Biezl. *Prinzip des Durchsteckwandlers*.
URL: https://de.wikipedia.org/wiki/Stromwandler#/media/Datei:Stromwandler_Zeichnung.svg (visited on 07/01/2024).

[10] K. Bohnert et al.
Fiber-Optic Current and Voltage Sensors for High-Voltage Substations.
Invited paper at 16th International Conference on Optical Fiber Sensors, October 13-17, 2003, Nara Japan Technical Digest, pp 752-754.
ABB Switzerland Ltd, Corporate Research, CH-5405 Baden-Dättwil, Switzerland, Oct. 2003.
URL: https://search.abb.com/library/Download.aspx?DocumentID=1262334&LanguageCode=en&DocumentPartId=&Action=Launch (visited on 07/25/2024).

[11] University of Bristol.
Infinity Sensor GHZ BANDWIDTH AC CURRENT SENSOR.
data sheet. Version 1.3. Electrical Energy Management Group, Faculty of Engineering, University of Bristol, Bristol, United Kingdom, Nov. 2022.
URL: https://www.infinitysensor.com/resources (visited on 07/01/2024).

[12] Harry C. P. Dymond et al. "Probing Techniques for GaN Power Electronics: How to Obtain 400+ MHz Voltage and Current Measurement Bandwidths without Compromising PCB Layout". In: *PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. 2022, pp. 1–10.
DOI: 10.30420/565822010.

[13] S. Engelberg. "The central limit theorem and low-pass filters".
In: *Proceedings of the 2004 11th IEEE International Conference on Electronics, Circuits and Systems, 2004. ICECS 2004*. 2004, pp. 65–68.
DOI: 10.1109/ICECS.2004.1399615.

[14] Charles R. Harris et al. "Array programming with NumPy".
In: *Nature* 585.7825 (Sept. 2020), pp. 357–362.
DOI: 10.1038/s41586-020-2649-2.
URL: https://doi.org/10.1038/s41586-020-2649-2.

[15] Mohammad Hedayati et al.
"Investigating GaN power device double-pulse testing efficacy in the face of VTH-shift, dynamic Rdson, and temperature variations". In: *2021 IEEE Applied Power Electronics Conference and Exposition, APEC 2021*.
Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC.

Institute of Electrical and Electronics Engineers (IEEE), 2021, pp. 2291–2298. DOI: 10.1109/APEC42165.2021.9487358.

[16] J. D. Hunter. "Matplotlib: A 2D graphics environment". In: *Computing in Science & Engineering* 9.3 (2007), pp. 90–95. DOI: 10.1109/MCSE.2007.55.

[17] Autodesk Inc. *EASILY APPLICABLE GRAPHICAL LAYOUT EDITOR, Version 9.5, Manual*. manual. 90925951. 2019. URL: https://www.autodesk.com/support/technical/product/eagle (visited on 09/20/2019).

[18] Cadence Design Systems Inc. 2022. URL: https://resources.pcb.cadence.com/technical-papers (visited on 12/09/2022).

[19] Tektronix Inc. *5 Series MSO Mixed Signal Oscilloscope Datasheet*. data sheet. Tektronix, Inc., 14150 SW Karl Braun Drive, P.O. Box 500, Beaverton, OR 97077, USA, Apr. 2020. URL: https://download.tek.com/datasheet/MSO5-Datasheet-EN-US-48W-60850-26.pdf (visited on 07/01/2024).

[20] Tektronix Inc. *Isolated Measurement Systems TIVM1, TIVM1L, TIVH08, TIVH08L, TIVH05, TIVH05L, TIVH02, TIVH02L Datasheet*. data sheet. Tektronix, Inc., 14150 SW Karl Braun Drive, P.O. Box 500, Beaverton, OR 97077, USA, Dec. 2022. URL: https://download.tek.com/datasheet/TIVH-Datasheet-51W612173.pdf (visited on 07/01/2024).

[21] Tektronix Inc. *Measurement System Signal Integrity: Important Factors to Consider*. technical brief. Tektronix Inc., 14150 SW Karl Braun Drive, P.O. Box 500, Beaverton, OR 97077, USA, May 2010. URL: https://download.tek.com/document/55W-18024-3.pdf (visited on 07/01/2024).

[22] Tektronix Inc. *Passive High Voltage Probes P5100A-TPP0850-P5122-P5150-P6015A Datasheet*. data sheet. Tektronix, Inc., 14150 SW Karl Braun Drive, P.O. Box 500, Beaverton, OR 97077, USA, Oct. 2023. URL: https://download.tek.com/datasheet/P5100A-TPP0850-P5122-P5150-P6015A-Datasheet-EN-US-56W-10262-15.pdf (visited on 07/01/2024).

[23] Wikimedia Foundation Inc. URL: https://en.wikipedia.org/wiki/FR-4 (visited on 06/22/2024).

[24] University of Bristol Infinity Sensor. *Infinity Sensor*. 2022.
URL: https://www.infinitysensor.com/ (visited on 07/01/2024).

[25] Armin Jafari et al. "Comparison of Wide-Band-Gap Technologies for Soft-Switching Losses at High Frequencies". In: *IEEE Transactions on Power Electronics* 35.12 (2020), pp. 12595–12600.
DOI: 10.1109/TPEL.2020.2990628.

[26] Working Group 1 of the Joint Committee for Guides in Metrology (JCGM/WG 1).
JCGM GUM-6:2020, Guide to the expression of uncertainty in measurement — Part 6: Developing and using measurement models. 2020.
URL: https://www.bipm.org/documents/20126/2071204/JCGM_GUM_6_2020.pdf (visited on 07/01/2024).

[27] Dawon Kahng. *Electric field controlled semiconductor device*.
US Patent no. 3,102,230. 1960.
URL: https://patents.google.com/patent/US3102230A/en (visited on 07/01/2024).

[28] Walt Kester. *Understand SINAD, ENOB, SNR, THD, THD + N, and SFDR so You Don't Get Lost in the Noise Floor*.
Analog Devices, Inc., 2009.
URL: https://www.analog.com/media/en/training-seminars/tutorials/MT-003.pdf (visited on 07/01/2024).

[29] Bohnert Klaus and Guggenbach Peter.
A revolution in high dc current measurement. ABB Review 1/2005.
ABB Switzerland Ltd, Fiber-Optic Current Sensors, Dept. ATPR / FOCS, Austrasse, CH-5300 Turgi, Switzerland, 2005.
URL: https://search.abb.com/library/Download.aspx?DocumentID=9AKK100580A1677&LanguageCode=en&DocumentPartId=&Action=Launch (visited on 07/25/2024).

[30] Adrien Letellier et al. "Calculation of Printed Circuit Board Power-Loop Stray Inductance in GaN or High di/dt Applications".
In: *IEEE Transactions on Power Electronics* 34.1 (2019), pp. 612–623.
DOI: 10.1109/TPEL.2018.2826920.

[31] David Levett, Ziqing Zheng, and Tim Frank.
Double Pulse Testing: The How, What and Why. article.
Infineon Technologies, 2022.
URL: https://www.infineon.com/dgdl/Infineon-Double_pulse_testing-Bodos_power_systems-Article-v01_00-

EN.pdf?fileId=5546d46271bf4f920171ee81ad6c4a1f (visited on 07/01/2024).

[32] Haiguo Li et al. "Improved Double Pulse Test for Accurate Dynamic Characterization of Medium Voltage SiC Devices". In: *IEEE Transactions on Power Electronics* 38.2 (2023), pp. 1779–1790. DOI: 10.1109/TPEL.2022.3210749.

[33] J.E. Lilienfeld. *Method and apparatus for controlling electric currents*. US Patent no. 1,745,175. 1926. URL: https://patents.google.com/patent/US1745175A/en (visited on 07/01/2024).

[34] Juncheng Lu et al. "Design consideration of gate driver circuits and PCB parasitic parameters of paralleled E-mode GaN HEMTs in zero-voltage-switching applications". In: *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2016, pp. 529–535. DOI: 10.1109/APEC.2016.7467923.

[35] Markus Makoschitz and Sumanta Biswas. "Light Load Efficient Silicon Power Converters Based on Wide Bandgap Circuit Extensions". In: *Applied Sciences* 10.14 (2020). ISSN: 2076-3417. DOI: 10.3390/app10144730. URL: https://www.mdpi.com/2076-3417/10/14/4730.

[36] Markus Leopold Makoschitz et al. *Wide Band Gap Technology: Efficiency Potential and Application Readiness Map*. English. report. May 2020. URL: https://pecta.iea-4e.org/files/otherfiles/0000/0186/PECTA_Report_Total-V10final-May-2020.pdf (visited on 07/01/2024).

[37] Markus Meissner et al. "Current measurement of GaN power devices using a frequency compensated SMD shunt". In: *PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. 2019, pp. 1–8.

[38] Allegro MicroSystems. *1 MHz Bandwidth, Galvanically Isolated Current Sensor IC in SOIC-16 Package*. data sheet. Allegro MicroSystems, LLC, 955 Perimeter Road, Manchester, NH 03103-3353, U.S.A., Oct. 2018. URL: https://www.allegromicro.com/en/products/sense/current-sensor-ics/zero-to-fifty-amp-integrated-conductor-sensor-ics/acs732-3 (visited on 07/01/2024).

[39] Ltd. Murata Manufacturing Co.
MEJ1 Series 5.2kVDC Isolated 1W DC-DC Converters. Aug. 2022. URL: https://www.murata.com/products/productdata/8807029768222/kdc-mej1.pdf?1719372615000 (visited on 07/01/2024).

[40] Pascal S. Niklaus, Dominik Bortis, and Johann W. Kolar.
"High-Bandwidth High-CMRR Current Measurement for a 4.8 MHz Multi-Level GaN Inverter AC Power Source". In: *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*. 2021, pp. 200–207.
DOI: 10.1109/APEC42165.2021.9487044.

[41] H. Nyquist. "Certain Topics in Telegraph Transmission Theory".
In: *Transactions of the American Institute of Electrical Engineers* 47.2 (1928), pp. 617–644. DOI: 10.1109/T-AIEE.1928.5055024.

[42] Thiele Reiner, Würfel Richard, and Eisenbeiß Max.
Stromsensor mit zirkularem Polarisator und Regelkreis.
Springer Vieweg Verlag, 2017. ISBN: 978-3-658-18472-8.

[43] W. Rogowski and W. Steinhaus.
"Die Messung der magnetischen Spannung".
In: *Archiv f. Elektrotechnik 1, 141–150* (1912).
URL: https://doi.org/10.1007/BF01656479 (visited on 07/01/2024).

[44] G. van Rossum. *Python tutorial*. Tech. rep. CS-R9526.
Amsterdam: Centrum voor Wiskunde en Informatica (CWI), May 1995.
URL: https://www.python.org/ (visited on 07/01/2024).

[45] Dr. Andrew Schaefer.
The Effective Number of Bits (ENOB) of my R&S Digital Oscilloscope.
Rodhe&Schwarz, Apr. 2011. URL:
https://cdn.rohde-schwarz.com/pws/dl_downloads/dl_application/application_notes/1er03/ENOB_Technical_Paper_1ER03_1e.pdf
(visited on 07/01/2024).

[46] Diego Serrano et al. "Advantages of Gallium Nitride over Silicon transistors in softswitched Resonant Switched Capacitor Converters". In: *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*. 2018, pp. 1–6.

[47] C.E. Shannon. "Communication in the Presence of Noise".
In: *Proceedings of the IRE* 37.1 (1949), pp. 10–21.
DOI: 10.1109/JRPROC.1949.232969.

[48] Ed Shelton et al.
"Design and measurement considerations for WBG switching circuits".
In: *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*. 2017, P.1–P.10.
DOI: 10.23919/EPE17ECCEEurope.2017.8099377.

[49] Luke Shillaber et al. "Ultra Fast Current Shunt (UFCS): A Gigahertz Bandwidth Ultra Low Inductance Current Sensor".
In: *IEEE Transactions on Power Electronics* (2022), pp. 1–13.
DOI: 10.1109/TPEL.2022.3184638.

[50] Julian Styles. *Common misconceptions about the body diode*.
GaN Systems, Oct. 2019.
URL: https://gansystems.com/wp-content/uploads/2020/01/Common-misconceptions-about-the-MOSFET-body-diode.pdf (visited on 07/02/2024).

[51] The pandas development team. *pandas-dev/pandas: Pandas*. Version latest. Feb. 2020. DOI: 10.5281/zenodo.3509134.
URL: https://doi.org/10.5281/zenodo.3509134.

[52] Howard Tweddle.
GS66516T Top-side cooled 650 V E-mode GaN transistor Datasheet.
data sheet. GaN Systems Inc., 2021.
URL: https://gansystems.com/gan-transistors/gs66516t/ (visited on 07/01/2024).

[53] PEM UK. *CWT Ultra-mini*. data sheet.
Power Electronic Measurements Gloucester House, 162 Wellington Street, Long Eaton, Nottingham NG10 4HS United Kingdom, Feb. 2020. URL: https://www.pemuk.com/Userfiles/CWTum/CWTUM_DS_Feb_2020.pdf (visited on 07/28/2024).

[54] Pauli Virtanen et al.
"SciPy 1.0: Fundamental Algorithms for Scientific Computing in Python".
In: *Nature Methods* 17 (2020), pp. 261–272.
DOI: 10.1038/s41592-019-0686-2.

[55] Inc. Vishay Intertechnology. *SiHG47N60E E Series Power MOSFET*.
data sheet. Vishay Intertechnology, Inc. 63 Lancaster Avenue, Malvern, Pennsylvania 19355-2143, USA, July 2017.
URL: https://www.vishay.com/docs/91474/sihg47n60e.pdf (visited on 07/01/2024).

[56] Jianjing Wang et al. “Infinity Sensor: Temperature Sensing in GaN Power Devices using Peak di/dt”.
In: *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2018, pp. 884–890. DOI: 10.1109/ECCE.2018.8558287.

[57] Kangping Wang et al. “A High-Bandwidth Integrated Current Measurement for Detecting Switching Current of Fast GaN Devices”.
In: *IEEE Transactions on Power Electronics* 33.7 (2018), pp. 6199–6210. DOI: 10.1109/TPEL.2017.2749249.

[58] Kangping Wang et al. “A Multiloop Method for Minimization of Parasitic Inductance in GaN-Based High-Frequency DC–DC Converter”.
In: *IEEE Transactions on Power Electronics* 32.6 (2017), pp. 4728–4740. DOI: 10.1109/TPEL.2016.2597183.

[59] E. T. Whittaker. “XVIII.—On the Functions which are represented by the Expansions of the Interpolation-Theory”.
In: *Proceedings of the Royal Society of Edinburgh* 35 (1915), pp. 181–194. DOI: 10.1017/S0370164600017806.

[60] Inc. Wolfspeed. *C2M1000170J Silicon Carbide Power MOSFET C2MTM MOSFET Technology N-Channel Enhancement Mode*. data sheet. Wolfspeed, Inc. 4600 Silicon Drive, Durham, North Carolin 27703, USA, Jan. 2024. URL: https://assets.wolfspeed.com/uploads/2024/01/Wolfspeed_C2M1000170J_data_sheet.pdf (visited on 07/01/2024).

[61] Wen Zhang, Zheyu Zhang, and Fred Wang.
“Review and Bandwidth Measurement of Coaxial Shunt Resistors for Wide-Bandgap Devices Dynamic Characterization”.
In: *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*. 2019, pp. 3259–3264. DOI: 10.1109/ECCE.2019.8912750.

[62] Wen Zhang et al. “High-Bandwidth Low-Inductance Current Shunt for Wide-Bandgap Devices Dynamic Characterization”.
In: *IEEE Transactions on Power Electronics* 36.4 (2021), pp. 4522–4531. DOI: 10.1109/TPEL.2020.3026262.

Acronyms

ADC Analog to Digital Converter. 22, 50

AFG arbitrary function generator. 42, 48

BJT bipolar junction transistor. 24

CMRR common-mode rejection ratio. 12

CMTI common-mode transient isolation. 31

cps counts per second = frequency. 52

CSR coaxial shunt resistor. 2, 9, 48

CSV comma separated values. 68, 72

CT current transformer. 12

CVR current viewing resistor. 1, 5, 9

DC direct current. 48

DMM digital multi meter. 48

DPT double pulse test. 2, 23

DSO Digital Storage Oscilloscope. 22, 48, 49

DUT device under test. 23, 45

duty cycle the percentage of a rectangular signal at which the signal is high, relative to the periode of the signal. 82

Eagle easily applicable graphical layout editor, Eagle is a schematic and layout design software, ©Autodesk Inc.[17]. 28

ENOB effective number of bits: quantifies the quality of the analog-digital conversion of an electronic measurement device with ADC or DAC. 50

FET field-effect transistor. 1

FOCS fibre optical current sensor. 2, 88

FR4 flame retardant, FR4 is the NEMA grade designation for glass-reinforced epoxy laminate material[23]. 28

FSA full scale amplitude. 51

GaN gallium nitride. 1

GUM guide to the expression of uncertainty in measurement. 56

HEMT high electron mobility transistor. 1

HF high-frequency. 12

IA input amplitude. 51

IC integrated circuit. 24, 42

IGBT insulated gate bipolar transistor. 2, 24

IVS galvanically isolated inductor voltage sensing. 12

LF low-frequency. 12

mFOCS miniature fibre optical current sensor. 2, 88

MHF4 micro high frequency coaxial connector 50Ω. 16, 18, 20, 59, 81

MOSFET metal-oxide-semiconductor field-effect-transistor. 1

NPT n pulse test. 23

OrCAD OrCAD is a schematic and layout design software, ©Cadence Design Systems Inc.[18]. 28

PCB printed circuit board. 48

PE Polyethylene. 47

POM-C Polyoxymethylene-C. 47

PSU power supply unit. 48

PWM pulse width modulation. 23, 82

Si silicon. 1

SiC silicon carbide. 1

SINAD Signal to noise Ratio plus Distortion. 50, 51

SMA subminiatur version A, coaxial connector. 30, 81

SMD surface mount device. 86

SNR signal to noise ratio. 10, 50, 51

UFCS ultra fast current shunt. 2, 79, 85, 86

VNA vector network analyzer. 12, 48

WBG wide-bandgap. 1

A. Appendix

A.1. DPT PCB with Infinity Sensor V2

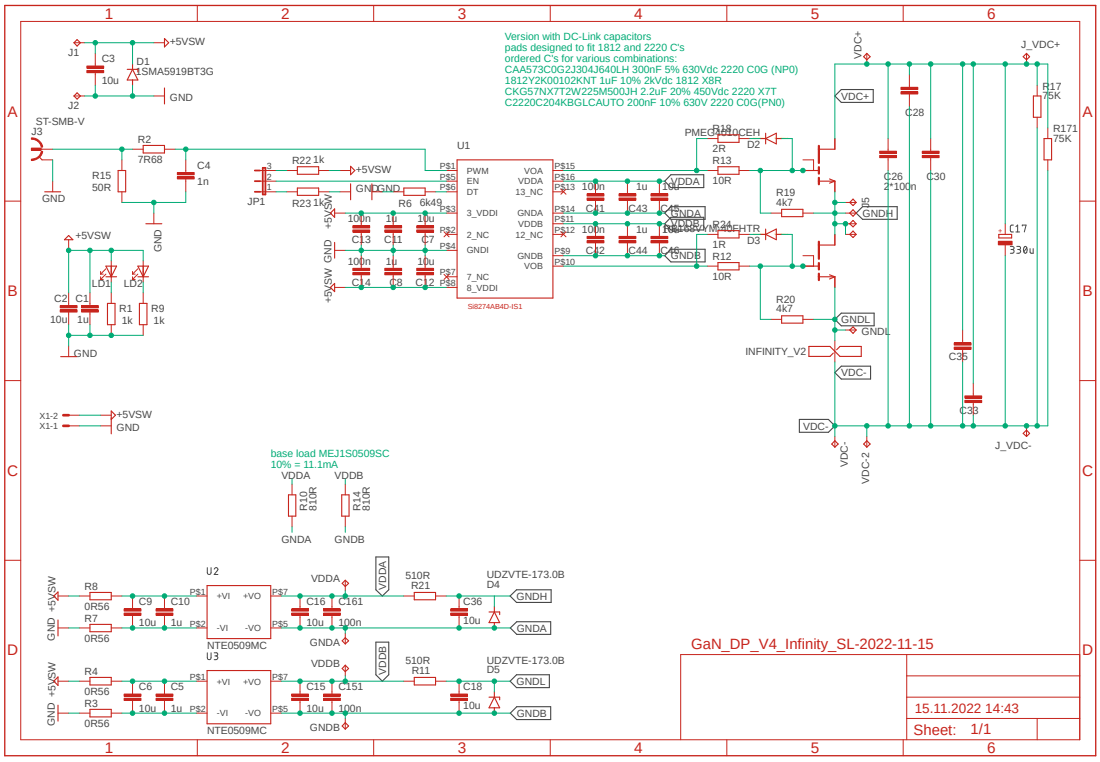
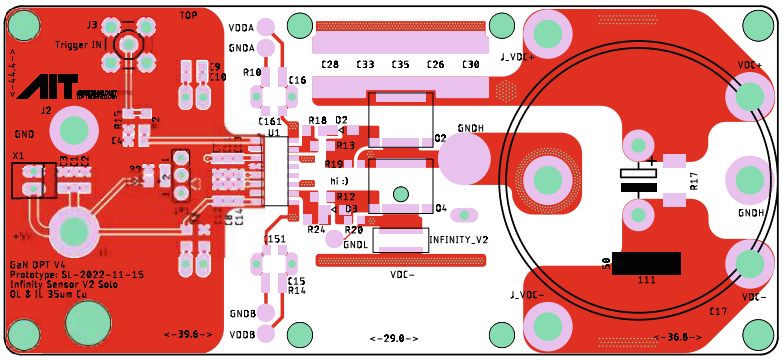
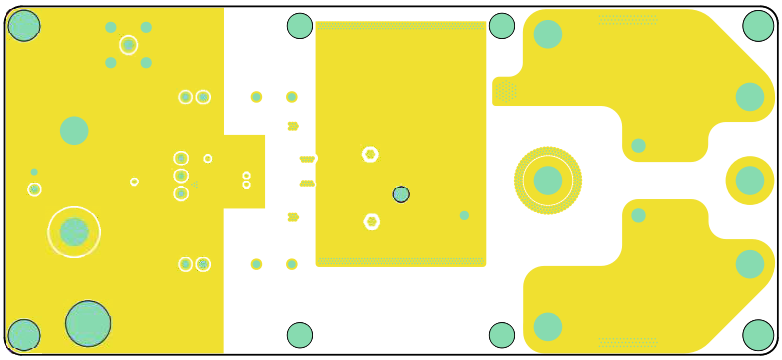


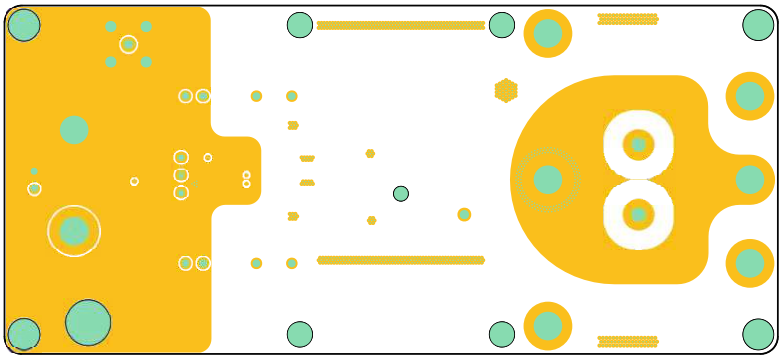
Figure A.1.: Schematic of the DPT PCB with Infinity Sensor V2



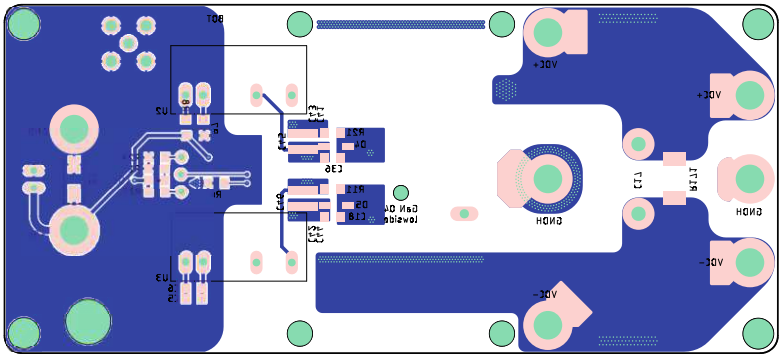
(a) Top layer (1) 70μm thick



(b) First inner layer (2) 70μm thick



(c) Second inner layer (15) 70μm thick



(d) Bottom layer (16) 70μm thick

Figure A.2.: Copper layers of the DPT PCB with the Infinity Sensor V2

A.2. DPT PCB with CSR

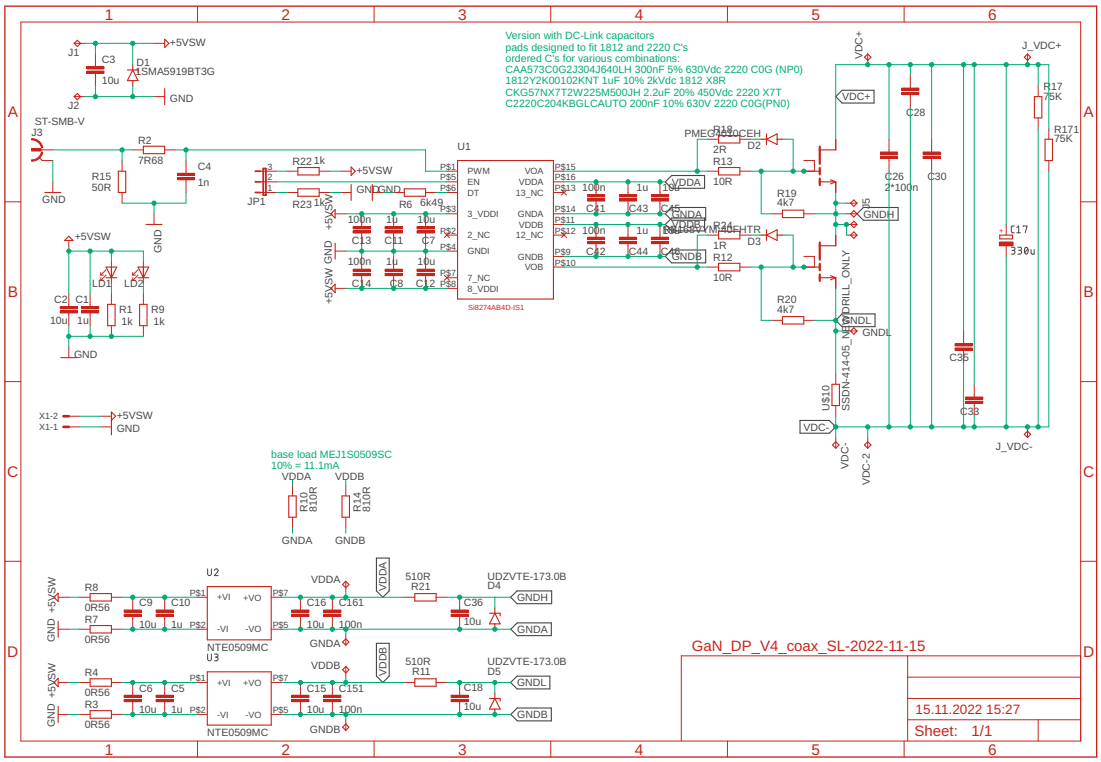
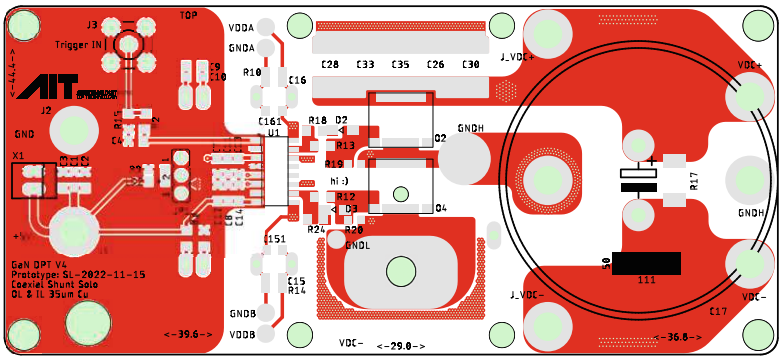
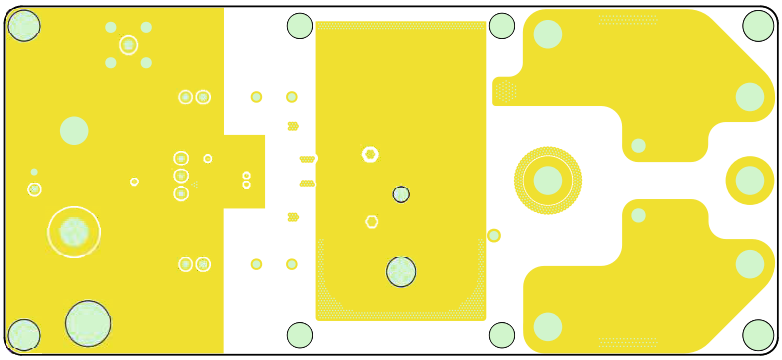


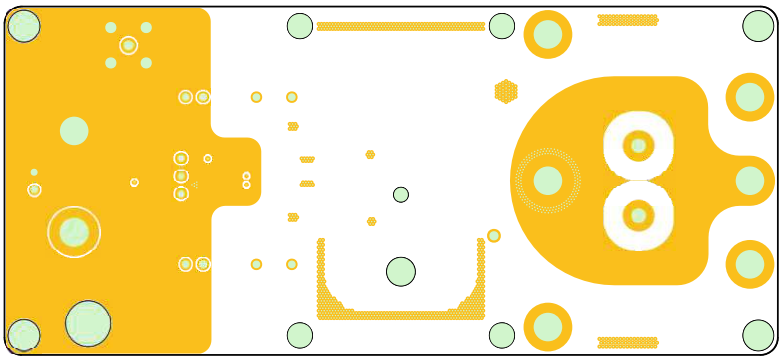
Figure A.3.: Schematic of the DPT PCB with Infinity Sensor V2



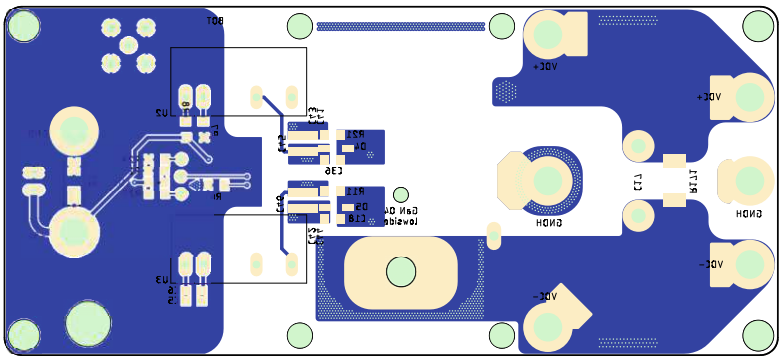
(a) Top layer (1) 70μm thick



(b) First inner layer (2) 70μm thick



(c) Second inner layer (15) 70μm thick



(d) Bottom layer (16) 70μm thick

Figure A.4.: Copper layers of the DPT PCB with the CSR

A.3. DPT PCB with Infinity Sensor V2 and CSR in combination

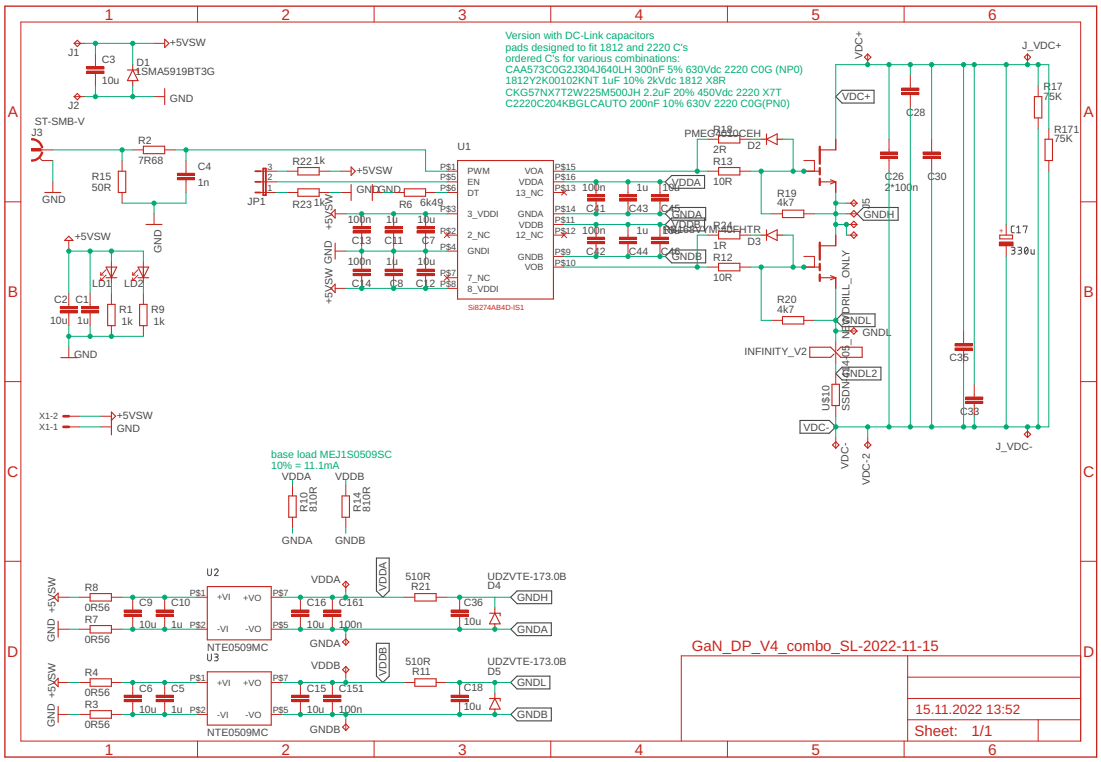
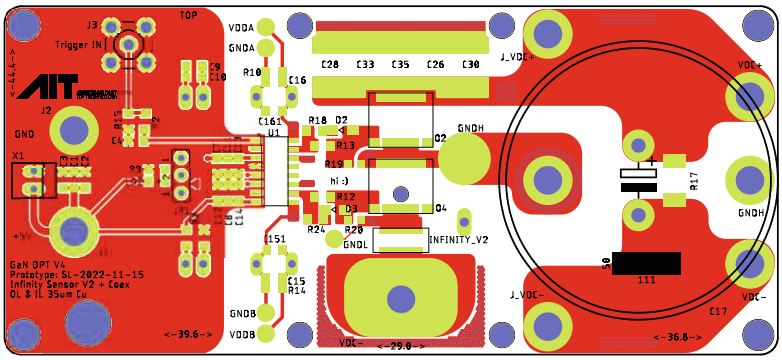
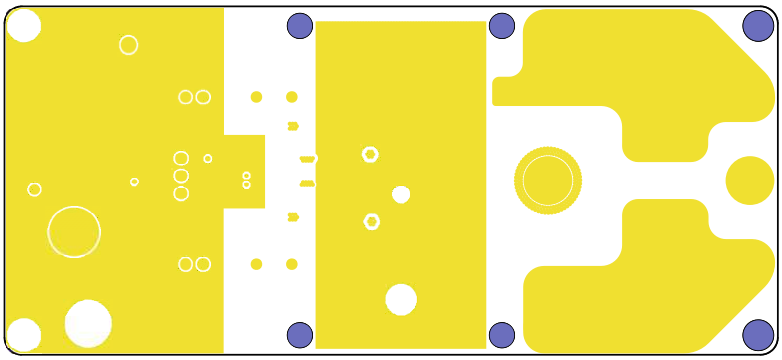


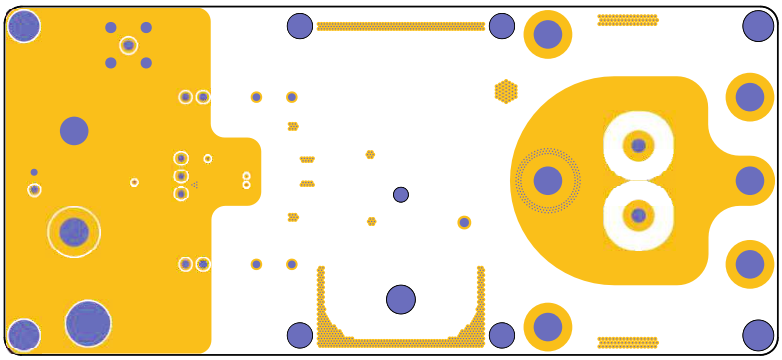
Figure A.5.: Schematic of the DPT PCB with Infinity Sensor V2



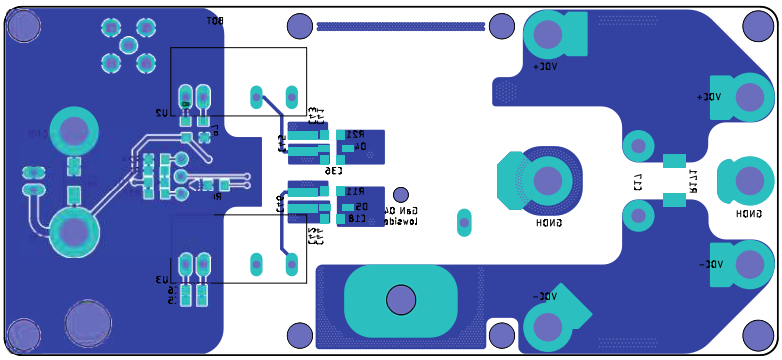
(a) Top layer (1) 70μm thick



(b) First inner layer (2) 70μm thick



(c) Second inner layer (15) 70μm thick



(d) Bottom layer (16) 70μm thick

Figure A.6.: Copper layers of the DPT PCB with the Infinity Sensor V2 and CSR in combination