DISSERTATION

Devices and Circuits for Stateful Logic and Memristive Sensing Applications

ausgeführt zum Zwecke der Erlangung des akademischen Grades
eines Doktors der technischen Wissenschaften

unter der Betreuung von
Privatdoz. Viktor Sverdlov
und
O.Univ.Prof. Siegfried Selberherr

eingereicht an der Technischen Universität Wien
Fakultät für Elektrotechnik und Informationstechnik
von

Hiwa Mahmoudi

[redacted]

Matr. Nr. 1029453

[redacted]

Wien, im April 2014 _____

To Xalo Rêbwar

Kurzfassung

Die Skalierung der CMOS-Technologie steht vor fundamentalen physikalischen und finanziellen Grenzen. Die steigende Nachfrage nach kostengünstiger Elektronik mit verbesserte Leistung beschleunigte die Erforschung neuer Konzepte und alternativer Technologien, um bestehende CMOS-Lösungen zu ersetzen oder zumindest zu ergänzen. Die Ruhezustandsverlustleistung auf Grund von Leckströmen ist zu einer bedeutenden Herausforderung in heutigen CMOS-VLSI-Schaltungen geworden. Die Einführung von Nichtflüchtigkeit in CMOS-Schaltungen ist eine vielversprechende Lösung, um dieses Problem zu bewältigen. Speziell die aufstrebenden nichtflüchtigen Widerstandsschaltspeicher, welche vielversprechende Kandidaten für zukünftige universelle Speicher sind, sind sehr attraktiv. Diese haben auch großes Potenzial für neue Anwendungen jenseits der nichtflüchtigen Speicher, da diese neue funktionale Merkmale für Berechnungen sowie Messungen ermöglichen, die in konventionellen Systemen nicht zugänglich sind.

Diese Dissertation befasst sich mit zustandsbehafteter Logik auf Bauelement-, Schaltungs- und Architekturebene. Zustandsbehaftete Logik erlaubt die simultane Verwendung von memristiven Bausteinen als nichtflüchtige Speicher (Flipflop) und Recheneinheit (Gatter). Daher verwirklicht nichtflüchtige Logik in Speicherschaltungen einen inhärent energieverbrauchslosen Ruhezustand und eröffnet die Möglichkeit einer Abkehr von der Von Neumann Architektur. Neben der Anwendung als Speicher oder Logikgatter sind auch Analog- und Messapplikationen möglich. Die einzigartigen Eigenschaften von memristiven Bauelementen werden für neuartige ladungs- und flussbasierte Messschemata genutzt.

Auf Grund seiner unbegrenzten Zustandshaltung und Kompatibilität mit CMOS wird die STT-MTJ (spin-transfer torque magnetic tunnel junction) als ein sehr vorteilhaftes Bauteil für zustandsbehaftete Logik vorgeschlagen. Zusätzlich wird gezeigt, dass diese im Gegensatz zu anderen Bauelementen (z.Bsp. Memristoren basierend auf Titandioxid) keine Zustandsdriftfehlerakkumulation wegen ihrer Bistabilität aufweisen. Daraus resultierend wird die Notwendigkeit eines Auffrischungskreises in zustandsbehafteten Logikschaltkreisen eliminiert. Ein neues auf STT-MTJ-basierendes Implikationslogikgatter mit einer stromgesteuerten Schaltungstopologie wird vorgeschlagen. Eine Zuverlässigkeitsmodellierung und eine Analyse zustandsbehafteter Logikarchitekturen zur Optimierung und zum Vergleich unterschiedlicher zustandsbehafteter Logikgatter wird präsentiert. Es wird gezeigt, dass das Implikationsgatter die dem aktuellen Stand der Technik entsprechenden Gatter bezüglich Zuverlässigkeit und Energieverbrauch übertrifft. Eine inhärent strukturelle Asymmetrie des vorgeschlagenen

Implikationslogikgatters verursacht jedoch eine signifikante Begrenzung des Fan-Out und der Flexibilität von Berechnungen. Dank der einfachen Integration von MTJs oberhalb von CMOS-Schaltkreisen kann dieses Asymmetrie-Problem mittels der Verwendung des Zugriffstransitors einer Ein-Transistor/Ein-MTJ-Zelle (1T/1MTJ) als spannungsgesteuerter Widerstand elegant gelöst werden. Da die 1T/1MTJ-Zelle das Basiselement des kommerziellen STT-operierenden MRAM (magnetoresisitve random-access memory) darstellt, kann die vorgeschlagene Implementierung auf eine zustandsbehaftete STT-MRAM-Logikarchitektur erweitert werden. Die Logikarchitektur bietet ein vollständiges Logiksystem, weist eine simple Schaltkreisstruktur auf, delokalisiert die Berechnungsexekution, adressiert das Fan-Out-Problem und eliminiert die Notwendigkeit von Zwischenschaltkreisen. Es wird dadurch auch die parallele Ausführung von Berechnungen ermöglicht. Die Vorteile der MRAM-basierten zustandsbehafteten Logik werden auf Logikfunktionsausführungsebene demonstriert und auf Schaltungsebene für MRAM-basierte nichtflüchtige Halb- und Volladdiererimplementationen belegt.

Zusätzlich werden in dieser Dissertationsschrift neue ladungs- und flussbasierte Messschemata vorgeschlagen, in dem die einzigartige Eigenschaft von memristiven Bauteilen den applizierten Strom- und Spannungsverlauf aufzuzeichnen genutzt wird. Die memristive Messmethode reduziert die Kapazitäts-, Induktivitäts- und Leistungsmessung auf eine (simple) Widerstandsmessung. Unter Ausnützung der speziellen Eigenschaften der Domänenwanddynamik und deren Abhängigkeit von Form und Geometrie eines Domänenwand-Spintronik-Memristors, wird die Möglichkeit ladungsbasierter Kapazitäts- und flussbasierter Induktivitätsbestimmung mittels zweier unterschiedlicher geometrischer Profile für Domänenwand-Spintronik-Memristoren aufgezeigt. Die memristive Messmethode ist auch für zeitlich variierende Induktivitäten und Kapazitäten geeignet und zeigt daher großes Potenzial für Verwendung in induktiven und kapazitiven Sensoranwendungen.

Abstract

The scaling of CMOS technology is facing fundamental physical and financial limitations. The increasing demand for cost effective electronics with enhanced performance has accelerated the investigation of new concepts and alternative technologies to replace or at least to supplement CMOS. Standby power dissipation due to leakage has become a major challenge of today's CMOS VLSI circuits. Introducing non-volatility into CMOS circuits is a promising solution to overcome this issue. Especially, emerging non-volatile resistance switching memory (memristive) devices, which are promising candidates for future universal memory, are very attractive. They also have a great potential to lead novel applications beyond the non-volatile memory by the possibility to provide novel functional properties in computing as well as sensing that are not accessible in conventional systems.

In this thesis, stateful logic systems are studied at the device, circuit, and architecture levels. Stateful logic enables memristive devices to serve simultaneously as non-volatile memory (latches) and computing units (gates). Therefore, it inherently realizes non-volatile logic-in-memory circuits with zero-standby power and opens the door for a shift away from the Von Neumann architecture. Besides memory and logic applications also analog and sensing applications are feasible. The unique properties of the memristive devices are exploited to introduce novel non-volatile charge- and flux-based sensing schemes.

Because of unlimited endurance and CMOS compatibility, the spin-transfer torque magnetic tunnel junction (STT-MTJ) is proposed as a very favorable device for stateful logic. In addition, it is shown that unlike other devices (e.g. memristors based on titanium dioxide), the STT-MTJ-based logic gates do not show any state drift error accumulation due to the magnetic bistability. As a result, the need for refreshing circuits in stateful logic circuits is eliminated. A new STT-MTJ-based implication logic gate with a current-controlled circuit topology is proposed. Reliability modeling and analysis of the stateful logic architectures for optimization and comparison of different stateful logic gates are presented. It is demonstrated that the implication gate outperforms state-of-the-art gates in terms of reliability and energy consumption. However, an inherent structural asymmetry of the proposed implication logic gate causes significant limitations for the non-volatile fan-out and the flexibility of the computations. Thanks to the easy integration of MTJs on top of a CMOS circuit, an elegant solution is presented to address this asymmetry issue by using the access transistors of one-transistor/one-MTJ (1T/1MTJ) cells as voltage-controlled resistors. Because

a 1T/1MTJ cell is the basic element of the commercialized STT-operated magnetoresistive random-access memory (MRAM), the proposed implementation becomes generalizable to a stateful STT-MRAM logic architecture. This logic architecture is computationally complete, has a simple circuit structure, delocalizes computational executions, addresses the fan-out issue, and eliminates the need for intermediate circuitry. It also enables parallel computations. Advantages of the MRAM-based stateful logic are demonstrated at the level of logic functions executions and are proven at the circuit level by considering MRAM-based non-volatile half adder and full adder implementations.

In addition novel charge- and flux-based sensing schemes are proposed in this thesis by using the unique ability of memristive devices to record the historic profile of the applied current/voltage. The memristive sensing method reduces the capacitance, inductance, and power measurements to a (simple) resistance measurement. Using the pecularities of the domain wall dynamics depending on the shape and the geometry of a domain wall spintronic memristor, the possibility of charge-based capacitance and flux-based inductance sensing is demonstrated, when two different spatial shapes of the domain wall spintronic memristors are employed. The memristive sensing method is also suitable for measuring time-varying inductances and capacitances and thus shows great potential for use in inductive and capacitive sensor applications.

Kurte

Biçûkkirdinî têknolojîy CMOS xerîke rrûberrûy berbestgelî binerretîy fîzîkî û abûrî bibêt-ewe. Zêdebûnî dawakarî bo amêre êlêktironîyekan be nirxî guncaw û lêhatûyîy perepêd-iraw, gerran bedway çemkgelî niwê û têknolojîy cêgirewey hênawete ara takû cêgey CMOS bigrinewe yan lanîkem alîkarî bin. Hêzî ledestçû lekatî "standby" da behoy dizekirdin buwete milmilanêyekî serekî bo xulgekanî CMOS-VLSIî em serdeme. Hênanî cêgîryetî (non-volatility) bonaw xulgekanî CMOS rrêgeçareyekî dillxoşkere bo zallbûn beser em kêşe da. Betaybet, serhelldanî amêrgelî bîrgey cêgîr wekû swîçî bergir-binema û bîrge-bergir (memory-resistor; memristor), ke berbijêrgelêkî dillxoşker-in bo dahatûy bîrgey gişтî, zor serincrrakêşe. Ciya le bîrgey cêgîr, ew amêrgele herweha bellênderî kellkgelî niwên ewîş le rrêgey dabînkirdinî taybetmendîgelî niwê le jimêrkarî û herweha le hestpêkirdin da ke le sîstimgelî nerîtî da leberdest da nîn.

Lem têze da, sîstime mentiqîye doxhellgirekan (stateful logic systems) le astekanî amêr (device), xulge (circuit) û mê'marî (architecture) da lekollîneweyan leser kirawe. Mentiqî doxhellgir detwanêt amêre "memristive"ekan hawkat wekû bîrgey cêgîr (flip-flop) û herweha yekey jimêrkarî (derwazey mentiqî) bekar bihênêt. Kewate, be şêwazêkî sirûştî mentiqî-naw-bîrgey cêgîr be hêzî "zero-standby" be dest dexat û derkey dûrkewtinewe le mê'marîy "Von Neumann" dekatewe. Cige le kellkgelî mentiq û bîrge, herweha kellkgelî "analog" û hestpêkirdin cêy hîwain. Taybetmendîye nawazekanî amêre "memristive"ekan bo nasandinî nexşe niwêkanî hestpêkrdinî barge (charge)-binema û lêşaw (flux)-binema bekar hênrawin.

Beboney bergegirtinî bêsinûr û tiwanayîy xoguncandin letek CMOS, STT-MTJ (spin-transfer torque magnetic tunnel junction) wek amêrêkî zor pesindkiraw bo mentiqî doxhellgir pêşniyar kirawe. Herweha, nîşan dirawe ke be pêçewaney amêrekanî dîke (bo wêne "memristor"î "titanium dioxide"-binema), derwaze mentiqîyekanî STT-MTJ-binema, behoy seqamgîrîy dûlayeney mugnatîkî, hîç seryekkewtineweyekî helley giwastinewey dox (state drift error) nîşan naden. Kewate, kêşey pêwîstî be xulgekanî niwêkirdinewe le xulge mentiqîye doxhellgirekan çareser dekrêt. Derwazeyekî mentiqîy "implication"î niwê leser binemay têknolojîy STT-MTJ û topolojîy xulgeyî ke be tezû kontiroll dekrên pêşniyar kirawe. Modêlsazîy mitmanepêkirawyetî û şîkarîy mê'marîye mentiqîye doxhellgirekan xirawnete berçaw bo başтirkrdin û hellsengandinî derwazegelî mentiqîy doxhellgirî ciyawaz. Selmênrawe ke derwazey "implication"î pêşniyarkiraw be pêwergelî mitmanepêkirawî û lekarkirdinî wize serkewtûtire le başтirîn derwazekanî henûke. Bellam, nahawcêyîyekî sirûştîy em derwazeye debête hoy sinûrdarkirdinî berçaw bo "fan-out"î cêgîr û herweha kemkirdinî sazgarîy jimêrkarîyekan. Xoşbextane

behoy yekxistinî sakarî MTJ leser xulgey CMOS, rrêgeçarêkî jîrane pêşkeş kirawe takû kêşey nahawcêyetî çareser bikat be bekarhênanî transistor-ekanî xanegelî yek transistor/yek MTJ (1T/1MTJ) wekû bergirêk ke be volltaj kontiroll bikrêt. Leber ewey ke xaney 1T/1MTJ xiştî binerretîye bo têknolojîy STT-MRAM (STT-magnetoresistive random-access memory) ke nêrdirawete bazarrîş, piyadesazîy pêşniyarkiraw gişitgîr debêt bo astî mê'marîy mentiqîy STT-MRAM-î doxhellgir. Em mê'marîye mentiqîye le rriwangey jimêrkarîyewe tekmîle, pêkhateyekî xulgeyîy sakarî heye, jimêrkarî le şêwazî nawçeyî der dehênêt, kêşey "fan-out" çareser dekat, û pêwîstî be komelle xulgey nawincî derrewênêtewe. Herweha, tiwanayîy jimêrkarîy hawrêk derrexsênêt. Qazancekanî mentiqî doxhellgirî MRAM-binema le astî îcray nexşekanî mentiq pîşan dirawe û le astî xulge da le rrêgey leberçawgirtinî piyadesazîy xulgegelî tewawkoker û nîwkokerî cêgîr selmênrawe.

Herweha, nexşe niwêkanî hestpêkirdinî barge-binema û lêşaw-binema lem têze da pêşniyar kirawin ewîş le rrêgey bekarhênanî tiwanayîy nawazey amêrî "memristive" lebo tomarkrdinî sîmay mêjûyîy tezû û volltaj. Şêwazî hestpêkirdinî "memristive" pêwerekanî bargegirî, handerî, û hêz kem dekatewe ta astî pêwerêkî bergirîy sade. Be bekarhênanî taybetmendîyekanî cimucûllî dîwarî pawan ke bestirawetewe be şikll û hendesey "memristor"î spintironic, tiwanayîy hestpêkirdinî bargegirîy barge-binema û handerîy lêşaw-binema pîşan dedrê, ewîş le katêk da ke dû şikllî ciyawazî "memristor"î spintironic bekar dehênrên. Şêwazî hestpêkirdinî "memristive" herweha bo pêwanî handerî û bargegirîy bigorr-bepêy-kat şiyawe û kewate lêhatuyîyekî mezin pîşan dedat bo sazkirdinî hestpêkerî "memristive"î hander-binema (inductive) û bargegir-binema (capacitive).

Acknowledgment

First and foremost, I would like to express my deepest thanks to my advisors, Prof. Siegfried Selberherr and Doz. Viktor Sverdlov, for giving me the opportunity to carry out my doctoral study at the Institute for Microelectronics. Siegfried provided an excellent working atmosphere, where I had the freedom to pursue various ideas and the possibility to enhance my research skills and to attend numerous international conferences. Viktor continuously guided and supported me and I really appreciate his motivation as well as constructive and frank comments which significantly improved the quality of my work.

I am also very grateful to Prof. Bernd Meinerzhagen who kindly agreed to take part in the examining committee.

Furthermore, I am indebted to Thomas Windbacher for his consistent guidance on my research during the last two years, the German translation of the abstract, and the careful proofreading of the thesis. He has been always willing to provide his feedback whenever I needed.

My sincere thanks also goes to Prof. Hans Kosina for his considerable support at the very beginning of my doctoral research and Mahdi Pourfath for his help and kindness made adapting to my new life in Vienna easier.

I want to express my gratitude to Prof. Erasmus Langer who has been a very co-operative head and other members of the institute for their support over the recent years, among them Wolfhard H. Zisser, Hossein Karamitaheri, Johann Cervenka, Franz Schanovsky, Manfred Katterbauer, Ewald Haslinger, Renate Winkler, and Markus Kampl.

Last but not the least, I am ever thankful to my friend and teacher Kake Foad and to my family members; my parents Mehîn and Heme-Elî, my lovely wife Sureya, and my sisters Şîwa and Şîma for their love, support, patience, and trust.

Contents

List of Figures

List of Tables

List of Abbreviations

1T/1MTJ	One-Transistor/One-MTJ
AP	Antiparallel
BL	Bit Line
CC-IMP	Current-Controlled IMP
CMOS	Complementary Metal-Oxide-Semiconductor
CRI	Combined Reprogrammable-Implication
DW	Domain Wall
DWM	DW Motion
FA	Full Adder
HA	Half Adder
HRS	High-Resistance State
IMP	Implication
ITRS	International Technology Roadmap for Semiconductors
LLG	Landau-Lifshitz-Gilbert
LRS	Low-Resistance State
MgO	Magnesium Oxide
MR	Magnetoresistance
MRAM	Magnetoresistive RAM
MTF	Magnetic Thin-Film
MTJ	Magnetic Tunnel Junction
NIMP	Negated IMP
P	Parallel
P-IMP	Parallel IMP
RAM	Random-Access Memory
RG	Reliable Gap
S-IMP	Serial IMP
SD	State Drift
SDE	SD Error
SL	Source Line
STT	Spin-Transfer Torque
SW	Switching Window
TMR	Tunnel Magnetoresistance
TiO_2	Titanium Dioxide
VC-IMP	Voltage-Controlled IMP
WL	Word Line
XOR	Exclusive OR

1. Introduction

1.1. Motivation

The exponential growth of the semiconductor industry has successfully proceeded for about four decades supported by continued improvement of complementary metal-oxide-semiconductor (CMOS) technology. For the next several years, there will be no apparent substitutes for the CMOS technology and its future development is already charted by the International Technology Roadmap for Semiconductors (ITRS) [1]. However, fundamental physical and economic limitations [2–4] such as leakage, high power densities, process variability, and soaring costs will bring the scaling of CMOS devices to an end. Therefore, besides exploring and introducing new materials, device structures, and design technologies, investigating possible alternative technologies to replace or at least to supplement CMOS is important to proceed with the performance enhancement of logic devices and circuits [5–15]. Right now there are many different devices under investigation with widely varying performance parameters e.g. energy, speed, area, et cetera. Spintronic devices [16–29] especially magnetoresistive devices [30,31] with a tunnel barrier junction structure [32], are strong candidates due to their non-volatility and compatibility with CMOS technology [33–40].

Despite the advantages of high speed and unlimited endurance, the first generation of magnetic tunnel junctions (MTJs) [41–43], which utilized Oersted fields for the magnetization switching, was unfavorable in terms of scalability and energy consumption. By using the spin-transfer torque [44,45] switching technique [46,47], the second generation of the MTJ (STT-MTJ) [48–50] eliminates the need for current lines adjacent to memory cells, which were required previously for generating a switching field. Thus, by using the same interconnects for reading and writing operations, the STT-MTJ is more scalable and yields smaller switching energies [22,23]. Magnetoresistive random-access memory (MRAM) with STT-MTJs as memory elements combines the speed of static RAMs (SRAMs), the density of dynamic RAMs (DRAMs), the non-volatility of flash memory, and has all the characteristics of a universal memory [39]. STT-MTJ technology is also attractive for building logic configurations which combine non-volatile memories and logic circuits (so-called logic-in-memory architecture [51]) to overcome scaling obstacles of CMOS logics [37,52–60]. Furthermore, STT-operated spintronic devices realize memristive behavior [61–68].

The memristor (memory-resistor) is the fourth fundamental circuit element predicted from a symmetry argument of circuit theory in 1971 [69]. However, its first physical

realization, in titanium dioxide (TiO_2), was announced about four decades later [70]. It can be thought as a passive programmable resistor. It holds a resistance state that depends on the history of the applied voltage/current even when the power is off. Memristive devices and systems [71–73] are capable of storing and processing information and offer unique properties which cannot be achieved in conventional electronic circuits by combining resistors, capacitors, and inductors. The most obvious application of memristive devices is non-volatile memory. Their great potential has attracted significant attention for developing alternative logic architectures [74–83]. In addition, memristive devices can be used as artificial synapses for neuromorphic applications [84–91]. As a basic element added to the circuit theory [92], memristors are also potentially suited for a wide range of tasks including analogue-to-digital and digital-to-analogue converters [93], electronic filters [94], temperature [95,96] and power [97] sensors, oscillators [98], signal processing [99], differential [100] and programmable [101] analog circuits, and control systems [102,103].

1.2. Scope of the Thesis

Recently, it has been shown that a fundamental Boolean logic operation called material implication (IMP) is naturally realized using TiO_2 memristive switches to enable stateful logic by using memristive devices simultaneously as latches and logic gates [76]. Stateful logic inherently provides a non-volatile logic-in-memory architecture with zero-standby power and is free from the leakage power issue. It also allows to shorten the interconnection delay by eliminating the need for intermediate sense amplifiers as well as the data transfer between separate memory and logic units and, by that, to lift a prerequisite of the Von Neumann computing architecture. In this thesis, implication logic gates are studied and optimized using an accurate nonlinear memristive device switching model. It is shown that due to error accumulation in TiO_2 memristive devices, spintronic devices are preferable to build up stateful logic circuits, as they do not show error accumulation and exhibit almost unlimited endurance.

A novel spintronic stateful logic gate is proposed, which stores the result of the implication logic operation directly into the memory devices. This thesis covers several issues regarding device, circuit, and architecture levels of the proposed logic framework. Special emphasis is put on the performance analyses of stateful logic devices and circuits and it is shown that the reliability is an essential prerequisite of stateful logic systems. Furthermore, it is demonstrated that the presented logic gate, which enables an implication logic framework, significantly improves the reliability compared to similar circuits available from literature, which are based on reprogrammable architectures to realize conventional Boolean logic operations including AND, OR, NAND, and NOR operations.

Due to an easy integration of MTJs on top of a CMOS circuit plane, hybrid CMOS/MTJ circuits are used to facilitate the generalization of the proposed logic gates to large-

scale non-volatile logic circuits. An innovative idea to utilize the access transistors of the one-transistor/one-MTJ (1T/1MTJ) cells not only as on-off switches but also as voltage-controlled resistors, is presented to address an asymmetry issue in the implication logic gates and to extend the functionality of the STT-MRAM architectures to perform logic operations with no extra hardware added. It is shown that the STT-MRAM-based logic provides non-volatile logic fan-out and exhibits high flexibility with regard to the delocalized computations execution, and eliminates the need for intermediate circuitry. It also enables parallel non-volatile computations and, therefore, it is suited for implementing complex logic functions. Advantages of the MRAM-based stateful logic are demonstrated by considering the STT-MRAM-based implication of the fundamental arithmetic functions. Through design examples like a stateful full adder, the possible tradeoffs to optimize the execution time, the energy consumption, and the reliability of the MRAM-based stateful logic architectures are also investigated.

The last part of the thesis describes novel charge- and flux-based sensing schemes utilizing the unique property of memristors to memorize the historic profile of the applied current/voltage. The device history can be revealed instantaneously by measuring its varying resistance (memristance). The proposed method, which is independent of the memristor material, can be used for capacitance, inductance, and power measurements. Although inductance and capacitance sensing are far from being new problems, the use of a memristor reduces the measurement to a straightforward resistance measurement. Depending on the sensing application, particular characteristics of the memristor are exploited. In order to have the possibility of both charge- and flux-based sensing, we suggest spintronic memristors which exhibit rich geometry dependent behavior with regard to the dynamic properties of a propagating magnetic domain wall in a magnetic device. The memristive sensing method is also suited for measuring time-varying inductances and capacitances and has the potential to be used in novel inductive and capacitive sensors.

1.3. Thesis Outline

The thesis is organized as follows. Chapter 2 reviews the background knowledge on memristive devices and systems. TiO_2-based stateful logic gates are studied in Chapter 3. Chapter 4 concentrates on spintronic stateful logic devices and circuits. A new improved implication logic gate is proposed, analyzed, and compared to the existing logic gates. Its generalization for large-scale logic application and parallelization for high performance computing is described in Chapter 5. Chapter 6 describes new memristive sensing schemes and explains how spintronic memristors can be used for coincident charge- and flux-based sensing. Finally, Chapter 7 concludes the thesis with a brief summary and an an outlook to possible future development.

2. Fundamentals of Memristive Devices and Systems

2.1. Theory

2.1.1. Memristor: The Fourth Element

The four fundamental circuit variables are electric current i, voltage v, charge q, and flux φ, where q and φ are defined as the time integrals of i and v, respectively [72].

$$q(t) := \int_{-\infty}^{t} i(\tau)\, d\tau, \tag{2.1}$$

$$\varphi(t) := \int_{-\infty}^{t} v(\tau)\, d\tau. \tag{2.2}$$

The three conventional two-terminal basic circuit elements resistor, capacitor, and inductor are defined in terms of the constitutive relationships between two of these four variables as [69]

$$R = dv/di, \tag{2.3}$$

$$C = dq/dv, \tag{2.4}$$

$$L = d\varphi/di. \tag{2.5}$$

R, C, and L are the resistance, capacitance, and inductance, respectively. Eq. 2.1-Eq. 2.5 express five from six possible relations between the fundamental circuit variables (Fig. 2.1). For the sake of completeness, Leon Chua postulated the existence of a fourth fundamental two-terminal circuit element called memristor (memory resistor) [69] characterized by a constitutive relationship between q and φ in which q and φ are not necessarily accessible to any physical interpretation [72]. The constitutive relation of charge-controlled and flux-controlled memristors are obtained as Eq. 2.6 and Eq. 2.7, respectively [72].

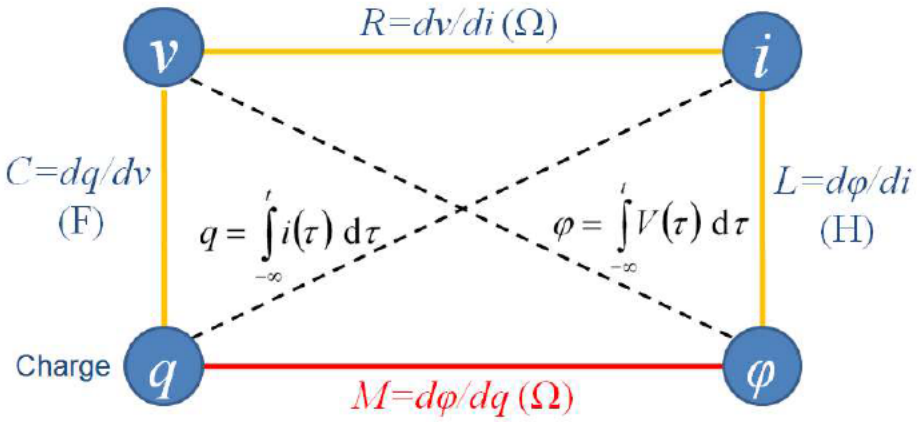

Figure 2.1.: Chua's symmetry argument.

$$\varphi = \varphi(q) \tag{2.6}$$

$$q = q(\varphi) \tag{2.7}$$

By taking the time derivatives we obtain

$$\frac{d\varphi}{dt} = \frac{d\varphi(q)}{dq}\frac{dq}{dt} = M(q)\frac{dq}{dt} \tag{2.8}$$

and

$$\frac{dq}{dt} = \frac{dq(\varphi)}{d\varphi}\frac{d\varphi}{dt} = W(\varphi)\frac{d\varphi}{dt}, \tag{2.9}$$

where

$$M(q) = \frac{d\varphi(q)}{dq} \tag{2.10}$$

and

$$W(\varphi) = \frac{dq(\varphi)}{d\varphi} \tag{2.11}$$

are the memristance and the memductance of the memristors as a function of q and φ, respectively. $M(q)$ and $W(\varphi)$ have the units of Ohms (Ω) and Siemens (S) as according to the definitions (Eq. 2.1 and Eq. 2.2) we have $dq/dt = i$ and $d\varphi/dt = v$ and thus we can simplify Eq. 2.8 and Eq. 2.9 to Eq. 2.12 and Eq. 2.13, respectively.

$$v = M(q)i \tag{2.12}$$

$$i = W(\varphi)v \tag{2.13}$$

In fact, a charge (flux)-controlled memristor is characterized by a $q - \varphi$ curve and its memristance (memductance) at q (φ) is equal to the slope of the curve $\varphi = \varphi(q)$ ($q = q(\varphi)$). A device with $dM(q)/dq = 0$ ($dW(\varphi)/dq = 0$) is just a linear resistor (conductor), while if $dM(q)/dq \neq 0$ ($dW(\varphi)/dq \neq 0$) the device operates like a variable resistor (conductor) and exhibits memristive behavior. In Chapter 6 we will see that memristors with $dM(q)/dq = \text{const.}$ ($dW(\varphi)/dq = \text{const.}$) are suited for a new charge (flux)-based memristive sensing scheme.

The memristor acts as a programmable resistor since its electrical resistance depends on the time integral of the applied current/voltage. Ideally, when the power is turned off ($i = v = 0$), the memristor preserves its resistance forever, as the values of q and φ are left unchanged [72]. Therefore, it records the historic profile of the applied current or voltage in the memristance/memductance which can be revealed instantaneously by measuring its electrical resistance. This is a unique property of memristors which cannot be realized by electric circuits combining resistors, capacitors, and inductors. The most straightforward application of a memristor is non-volatile memory either as an analog (continuously tunable or multilevel) memory or as a digital switch, depending on the physical operating mechanisms of the resistance switching in the memristive device. In general, one can say a memristor operates as an analog device in a low-voltage regime, while under large voltages it operates as a digital switch between two states, characterized by low and high resistances corresponding to the minimum and the maximum achievable resistance values limited by the physical properties of the device.

Since the memristor is a passive device, its current-voltage characteristic exhibits a hysteresis loop pinched at the origin and confined to the first and the third quadrants [72]. In fact, when the current (voltage) applied to the memristor goes to zero at $t = t_0$, the memristor acts as an ordinary resistor (conductor) with a finite resistance $R = M_0$ (conductance $G = W_0$) and thus the voltage (current) of the memristor goes to zero as well. Therefore, the $i - v$ curve passes through the origin and pinches the memristor hysteresis loop. It is clear that the $i - v$ characteristics of any nonlinear resistor (e.g. memristor) cannot be a straight line that passes through the origin, otherwise it is a linear resistor. Four decades after Chua's seminal paper ([69]) on memristor, he recently has shown that all forms of two-terminal non-volatile memories based on resistance switching can be classified as memristor since they demonstrate memristor fingerprint characterized as a pinched $i - v$ hysteresis loop [72, 73].

2.1.2. Memristive Systems

The definition of a memristor can be extended to a (passive two-terminal) memristive system [71] described by two coupled equations as

$$v = R(w, i)\, i, \tag{2.14}$$

called State-dependent Ohm's law [72] and

$$\frac{dw}{dt} = f(w, i), \tag{2.15}$$

called State equation [72], where v is the voltage across the device, R represents the generalized (nonlinear) resistance of the device, w denotes a state variable which can be a vector $w = (w_1, w_2, ..., w_n)$, i is the current through the device, and f expresses the functional dependence of dw/dt on w and i. The $i - v$ curve passes through the origin $(v, i) = (0, 0)$ as $R(w, 0) \neq \infty$ [72]. As we will see later, the state variable w can describe physically reasonable device parameters and thus this general definition of a memristive system can be successfully utilized to model various memristive devices with different operating mechanisms.

2.2. Physical Implementation

Physical demonstration of the memristor was missed for decades. However, as Chua showed recently, regardless the device material and switching mechanism, any resistance switching phenomenon depicts a memristive behavior [72,73]. This phenomenon was observed in titanium dioxide (TiO_2) [104] even before Chua's envision in 1971. Nevertheless, it revived interests in memristor development only after Hewlett Packard Laboratories announced the first memristor array fabricated in 2008 [70] based on a $Pt/TiO_2/Pt$ thin-film structure. Moreover, it has been shown that due to ionic motion in metal/oxide/metal thin-film stacks, including both anion-based [105–108] and cation-based [109–114] switching materials, these structures exhibit resistance switching and thus demonstrate memristive behavior forming an important class of memristive devices [82,115].

The electrons spin degree of freedom allows for realization of a memristive behavior when the spin-transfer torque effect is employed to change the resistance state of a spintronic device. After the first announcement of the memristor based on TiO_2 thin-films, the spin-based memristor has drawn a lot of attention as it ensures a more convenient control of the resistive state, than the ionic transport, especially at the nanoscale. Therefore, several spintronic memristive devices [61–68,116,117] have been proposed and explored.

Furthermore, there have been several reports of providing memristive behavior by using new internal state variables based on other phenomena and technologies like insulator-to-metal phase transition [118], phase change memory [119], piezoelectric effect [120], chemical immobilization of ferritin molecules [121], defect-scattering in a single-walled carbon nanotube [122], nickel titanium smart alloy [123,124], Graetz bridge loaded with an RLC filter [125], thickening/thinning of Ag nanofilaments in

amorphous manganite thin-films [126], nanoscale plasmonic [127], multi-terminal silicon nanowires [128], and volatile resistive switching effect at a prototypical Schottky metal/oxide interface [129].

2.3. Memristive Device Modeling

Beside the extensive efforts for physical implementation of resistance switching and memristive devices, significant progress has also been made regarding the modeling [88, 130–144] as well as better understanding of the working principles and improving the performance [145–159] of the memristive devices. However, most of the presented memristor models rely on a linear ionic drift model for TiO_2 memristive devices suggested in [70] which is not adequately accurate, especially in high voltage switching regimes, and can be used only for limited applications as will be shown in Chapter 3. In [139] a more detailed but quite complicated and computationally expensive physical model based on the Simmons tunneling barriers [160] is presented. It takes into account the asymmetric switching behavior as well as the nonlinearities observed in TiO_2 memristive devices [148–150]. To my best knowledge, this nonlinear ionic drift model [139] (its SPICE implementation is presented in [140]) is up to now the most accurate model for the TiO_2 memristive devices. More computationally effective and simpler models including nonlinearities of memristive devices as well as additional physical operating mechanisms for different types of memristive devices, have been presented in [141–144] based on voltage/current thresholds.

3. TiO_2-Based Memristive Stateful Logic Gates

3.1. Overview

At present, the most commonly used logic circuits consist of memory units for data storage and separated logic units for holding data and performing arithmetic and logical operations, which are typically implemented based on CMOS technology (Fig. 3.1). These CMOS-based logic circuits retain information as long as power is applied (volatility) and any power supply interruption can cause loss of information. As the dimensions of the CMOS transistors shrink down the leakage currents increase. As a result, the continuously powered memory units cause large static (standby) power consumptions in CMOS-based logic circuits. In fact, they have become as large as the dynamic power consumption [3]. Furthermore, the increasing length of the interconnections between logic and memory limits the chip performance and results in the increment of both power and interconnection delay.

As one of the solutions of the above-described problems, non-volatility has been introduced to the logic circuit. Non-volatile elements retain the information and the logical state of the system is not lost, if the power supply is interrupted. In addition, distributing non-volatile memory elements over the CMOS logic circuit plane (logic-in-memory architecture [51]) combines logic and memory elements and allows extremely

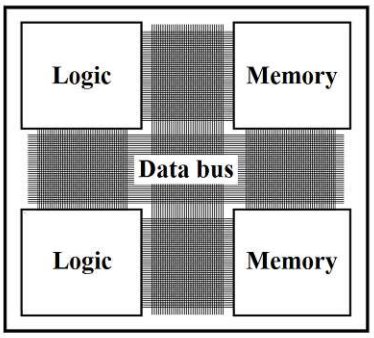

Figure 3.1.: Separated logic and memory units in a two-dimensional CMOS logic system.

low standby power consumption as well as instant start-up, by holding the information in the non-volatile elements and eliminating the need for refreshing pulses which are critical for CMOS-based memory elements. In addition, the use of non-volatile memory devices for novel computational architectures enables the application of the same elements as latches and logic gates, called stateful logic [76]. Stateful logic inherently realizes logic-in-memory circuits with zero-standby power, extends non-volatile electronics from memory to logic applications, and allows to shorten the interconnection delay. This opens the door for innovation in computational paradigms by shifting away from the Von Neumann architecture which transfers the information back and forth between the separated memory and logic units [26, 56, 57, 59, 60, 76].

3.2. Implication Logic

Recently, it has been shown that a fundamental Boolean logic operation called material implication (IMP) is naturally realized in a simple circuit (Fig. 3.2) combining a conventional resistor and two TiO_2 memristive switches [76, 77]. This provides stateful logic where non-volatile memory devices are used as the computing elements.

Material implication (IMP) is a fundamental two-input (e.g. s and t) Boolean logic operation ($s \rightarrow t$), which reads 's implies t' or 'if s, then t', and is equivalent to '(NOT s) OR t' ($\overline{s} + t$) as shown in Table 3.1. The symbols s and t are chosen as they represent the logic states of a source (S) and a target (T) memory element in the stateful logic gate. The operations IMP and NIMP (negated IMP) form a computationally complete logic basis in combination with any operation from the sets C and C′, respectively, for which C = {NOT, FALSE, XOR, NIMP} and C′ = {NOT, TRUE, XNOR, IMP} and are therefore able to compute arbitrary Boolean functions.

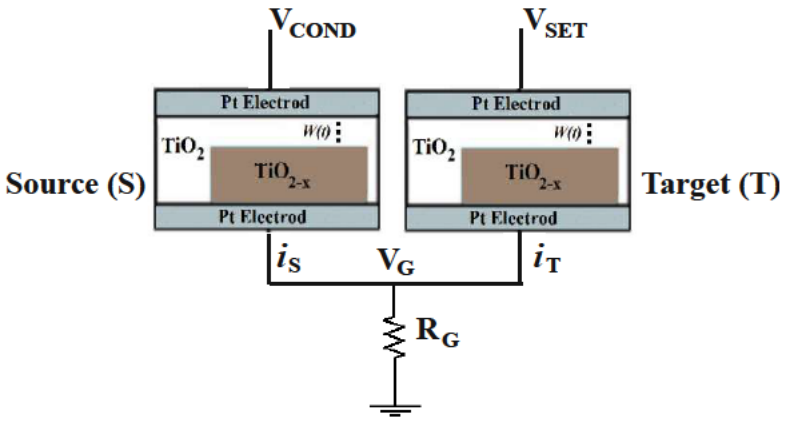

Figure 3.2.: Circuit topology of the TiO_2 memristive implication logic gate.

Table 3.1.: Truth tables of the basic implication operations, IMP and NIMP (negated IMP).

State	s	t	$s \rightarrow t$	$\overline{t \rightarrow s}$
1	0	0	1	0
2	0	1	1	1
3	1	0	0	0
4	1	1	1	0

Besides the AND, OR, and NOT operations, the IMP operation has been classified by Whitehead and Russell as one of the four basic logic operations in 1910 [161]. However, by modeling Boolean logic with circuits built with relays and switches, Shannon founded modern digital electronics [162] only based on AND, OR, and NOT operations due to their straightforward implementation. Since then, the IMP operation has been ignored in digital electronics. Only recently, it was demonstrated that memristive switches intrinsically enable the IMP operation in a crossbar array [76].

Fig. 3.2 shows the circuit topology of the TiO_2 memristive implication logic gate [76] combining two TiO_2 memristors, S and T, with a conventional resistor R_G. The initial resistance states of the source (S) and target (T) memristors (denoted by the logic variable s and t, respectively) are the logic inputs of the gate. The final resistance state of T after performing the logic operation (t') is the logic output of the gate. Performing the logic operation ($t' = s \rightarrow t$) involves simultaneous application of two negative voltage pulses, V_{SET} and V_{COND}, to the non-common terminals of S and T. V_{COND} is a negative voltage with smaller amplitude than V_{SET} ($|V_{SET}| > |V_{COND}|$).

Table 3.2.: Realized conditional switching behavior is equivalent to the operation IMP or NIMP depending on the definitions for the high and low resistance states (HRS and LRS) as logical '0' and '1'.

	Implication operation (conditional switching)				HRS≡0, LRS≡1			HRS≡1, LRS≡0		
					$t' = s \rightarrow t$			$t' = \overline{t \rightarrow s}$		
State	s	t	s'	t'	s	t	t'	s	t	t'
1	HRS	HRS	HRS	**LRS**	0	0	**1**	1	1	**0**
2	HRS	LRS	HRS	LRS	0	1	1	1	0	0
3	LRS	HRS	LRS	HRS	1	0	0	0	1	1
4	LRS	LRS	LRS	LRS	1	1	1	0	0	0

Therefore, the voltage drop on S is smaller than V_{ON} (the voltage level required for memristor high-to-low resistance switching) and it remains unchanged after the operation for any input patterns. However, depending on the resistance state of S, the voltage V_{COND} changes the voltage level on the common terminal of S and T (V_G) and modulates the voltage drop on the target memristor T. This provides a conditional switching behavior in T, which is shown in Table 3.2. In fact, the negative voltage pulse V_{SET} enforces a high-to-low resistance switching of T only, when both memristors are initially in the high resistance state (State 1). The voltage V_{SET} has a higher amplitude compared to V_{ON} as it must compensate the voltage drop on R_G.

According to Table 3.2, depending on the logical definitions for the memristor low (LRS) and high (HRS) resistance states, LRS $\equiv$ logic '1' and HRS $\equiv$ logic '0' or vice-versa, the realized conditional switching behavior is corresponding to the IMP or NIMP (negated IMP) operation (Table 3.1). In accordance with the convention of Shannon, if we define HRS $\equiv 1$ and LRS $\equiv 0$, the logic output of the implication gate corresponds to the NIMP operation as

$$\{t' = t \text{ NIMP } s\} \equiv \overline{t \rightarrow s} \equiv \{t' = t.\overline{s} = t \text{ AND } \overline{s}\}, \tag{3.1}$$

where t' is the final state of the variable t after the operation. In combination with the low-to-high resistance switching, which corresponds to the TRUE operation (writing logic '1') according to the above definition, the NIMP operation forms a complete logic basis to compute any Boolean function. Therefore, it enables stateful logic operations by memristive devices used simultaneously as non-volatile memory and logic gates [76]. For instance, stateful universal NOR and NAND operations can be performed in three and five sequential steps as Eq. 3.2 and Eq. 3.3, respectively.

$$\begin{aligned}
&\text{Step 1 (TRUE)}: && a = 1 \\
&\text{Step 2 (NIMP)}: && \overline{a \rightarrow b} \equiv \{a' = a.\overline{b} = \overline{b}\} \\
&\text{Step 3 (NIMP)}: && \overline{a \rightarrow c} \equiv \{a' = a.\overline{c} = \overline{b}.\overline{c} = \overline{b + c} = b \text{ NOR } c\}
\end{aligned} \tag{3.2}$$

$$\begin{aligned}
&\text{Step 1 (TRUE)}: && a = 1 \\
&\text{Step 2 (NIMP)}: && \overline{a \rightarrow b} \equiv \{a' = a.\overline{b} = \overline{b}\} \\
&\text{Step 3 (NIMP)}: && \overline{c \rightarrow a} \equiv \{c' = c.\overline{a} = c.b\} \\
&\text{Step 4 (TRUE)}: && a = 1 \\
&\text{Step 5 (NIMP)}: && \overline{a \rightarrow c} \equiv \{a' = a.\overline{c} = \overline{c.b} = b \text{ NAND } c\}
\end{aligned} \tag{3.3}$$

Here, a (a') represents the initial (final) logic variable equivalent to the resistance state of a third memristor storing the logic result of intermediary logic steps and the final result of stateful NAND and NOR operations. It should be noted that each logic variable (e.g. a) used as an input in Step i is equal to the final logic value (a') from the previous step (Step $i-1$) since it has been directly stored in a non-volatile memory element (A).

3.3. Modeling

As explained before, by applying the voltage pulses V_{SET} and V_{COND}, a (desired) high-to-low resistance switching (shown in bold in Table 3.2) is enforced in T only in State 1. However, the current flowing through the memristors tends to decrease their electrical resistances and change the internal state variable w. This phenomenon is called "state drift" (SD) [163] and its accumulation after a specific number of sequential (N)IMP operations causes an undesired switching event (computation error) either in S or T. This is due to the fact that, although the TiO_2 memristive switches are used as two-resistance-state devices for binary data storage, they actually act as analog elements since the parameter w changes continuously [143]. The design procedure of the IMP gate involves determining the proper values of the circuit parameters (R_G, V_{SET} and V_{COND}) to minimize the SD errors (SDEs). The design procedure presented in [163], which is the only existing design procedure to the author's knowledge, is based on a linear ionic drift model for the TiO_2 memristive devices described below. However, as it is shown in the following, a more accurate model of the TiO_2 memristive device has to be employed to analysis and optimize the stateful logic gates.

According to Fig. 3.2, the voltage drops on S and T are given by

$$v_S = V_{COND} - V_G = i_S M_S \tag{3.4a}$$
$$v_T = V_{SET} - V_G = i_T M_T, \tag{3.4b}$$

where

$$V_G = (i_S + i_T) R_G. \tag{3.5}$$

V_G denotes the voltage drop on R_G and i_S (i_T) and M_S (M_T) are the current and the memristances of the memristive devices S (T), respectively. As, in general, the memristance is a nonlinear resistance which depends on the historic profile of the current (voltage) applied to the memristor, M_S and M_T are a function of i_S (v_S) and i_T (v_T) as well as their initial resistance states (the logic input pattern). Therefore, in order to optimize the implication gate and to investigate the switching behavior of S and T, one has to solve Eq. 3.4 coupled with an appropriate memristor device model which accurately describes the $i - v$ characteristics of S and T. In the following, two TiO_2 memristor device models and simulation studies obtained from these models are presented.

Fig. 3.3 shows a schematic of the TiO_2 memristor structure containing a sandwiched TiO_2 thin film and two platinum (Pt) electrodes. During an electroforming process, as dopant acting oxygen vacancies are created in the TiO_2 thin-film except a narrow tunnel barrier of w [139]. Therefore, the thin film is divided into a (high conducting) doped region and an (insulating) undoped region and its total resistance (internal resistance) is equal to the sum of the variable resistances on each region:

$$R_{int} = R_{doped} + R_{undoped} \tag{3.6}$$

The resistance switching mechanism of the device is related to the drift motion of dopants (oxygen vacancies) due to an electric field across the device [115]. Therefore, this device shows memristive behavior as the width of the undoped region (w in Fig. 3.3) and thus the total electrical resistance of the device depends on the historic profile of the applied voltage/current to the device. According to the mathematical definition of a memristive system (Eq. 2.14), w is an internal state variable which here describes the effective width of the undoped region and determines the resistance state of the memristive device.

3.3.1. Linear Ionic Drift Memristive Model

Based on Eq. 2.14 and Eq. 2.15, a simple linear ionic drift model [70] describes the internal resistance as

$$R_{\text{int}} = \frac{w(t)}{w_{\text{max}}} R_{\text{off}} + \left(1 - \frac{w(t)}{w_{\text{max}}}\right) R_{\text{on}} \tag{3.7}$$

and

$$\frac{dw}{dt} = \frac{\mu_{\text{v}} R_{\text{on}}}{w_{\text{max}}} i(t), \tag{3.8}$$

where R_{off} and R_{on} are the maximum and the minimum resistances, respectively, w_{max} denotes the maximum thickness of the undoped region, and μ_{v} is the average mobility of the oxygen vacancies in the TiO_2 thin-film. According to the linear ionic drift model, by time-integrating the state equation (Eq. 3.8), we obtain that the modulation of the state variable w is proportional to the charge passing through the device ($\Delta w \propto \Delta q$).

In order to compare the switching dynamic behavior (including the switching time and the switching energy) predicted by the linear ionic model with some recently obtained experimental data, let's define ΔQ as the amount of charge that by passing through the memristor modulates the memristance from its minimum to its maximum value ($\Delta w = w_{\text{max}}$). A voltage pulse with a fixed amplitude of v_0 and the duration of τ_0 is applied to the memristor to perform an on-to-off (OFF) switching.

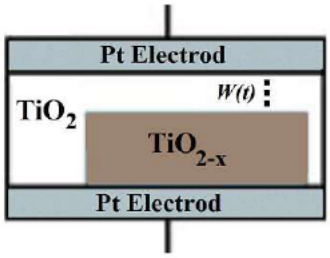

Figure 3.3.: Schematic of the TiO_2 memristive device cross section.

$$\Delta Q = \int_0^{\tau_0} i(t)dt = \int_0^{\tau_0} \frac{v_0}{R_{\text{int}}(w)}dt, \tag{3.9}$$

where according to Eq. 3.8 we have

$$i(t)dt = \frac{w_{\text{max}}}{\mu_{\text{v}} R_{\text{on}}}dw. \tag{3.10}$$

Therefore, ΔQ is obtained as

$$\Delta Q = \int_0^{w_{\text{max}}} \frac{w_{\text{max}}}{\mu_{\text{V}} R_{\text{on}}}dw = \frac{w_{\text{max}}^2}{\mu_{\text{V}} R_{\text{on}}}. \tag{3.11}$$

According to Eq. 3.11, derived from the linear ionic drift model, ΔQ has a constant value and is independent of the v_0 and τ_0. Therefore, it predicts that the switching time is inversely proportional to the voltage pulse amplitude ($\tau_0 \propto v_0^{-1}$). Indeed, according to the State-dependent Ohm's law for a memristive system (Eq. 2.14), at a time t_0 ($0 < t_0 < \tau_0$) where the electrical resistance of the memristor is R_0 ($R_{\text{on}} < R_0 < R_{\text{off}}$), the rate of the charge flow (i) is directly proportional to the voltage pulse amplitude (v_0). As a result, the amount of charge flowing through the memristor is proportional to the product of the voltage level and the time ($\Delta q \propto v_0 \Delta t$) and thus we have $\Delta Q \propto v_0 \tau_0$. As according to the memristor linear ionic drift model ΔQ is a constant, the switching time required for a complete switching from R_{on} to R_{off} must be inversely proportional to the pulse amplitude ($\tau_0 \propto v_0^{-1}$).

The OFF-switching energy consumption is also obtained as function of ΔQ by

$$\mathcal{E}_{\text{switch}} = \int_0^{\tau_0} v_0 i(t)dt = v_0 \Delta Q. \tag{3.12}$$

This predicts an *inverse* relationship between the switching energy and the switching time as $\mathcal{E}_{\text{switch}} \propto v_0 \propto \tau_0^{-1}$. However, these predictions regarding the switching dynamic behavior ($\tau_0 \propto v_0^{-1}$ and $\mathcal{E}_{\text{switch}} \propto \tau_0^{-1}$) are quite inconsistent with experimental data which demonstrate an inverse log-linear relationship between the switching time and the voltage pulse amplitude as $\tau_0 \propto \exp(-v_0)$ [150] and a *direct* log-log relationship between the switching energy and the switching time as $\log(\mathcal{E}_{\text{switch}}) \propto \log(\tau_0)$ [76]. The main reason is that the switching dynamic behavior is significantly affected by the electron tunneling effect through the insulating region which exponentially decrease the total electrical resistance of the TiO_2 memristor device during the switching [139]. Therefore, although the linear ionic drift model has been used to simulate the electrical properties of the memristor for different applications [88, 130–135], in a high voltage regime, however, the tunneling effect dominates the memristor $i - v$ characteristics. For the sake of (acceptable) fast switching, the applied voltage levels in logic applications are so high that the memristive devices act as digital switches with two resistance states of R_{on} and R_{off}. As a result, it is necessary to use a more accurate

model for digital (logic) applications. The switching dynamic behavior obtained from the nonlinear ionic drift model [139] explained below, shows a good agreement with experimental data. For example, this model predicts a *direct* log-log relationship between the switching energy and the switching time ($\log(\mathcal{E}_{\text{switch}}) \propto \log(\tau_0)$) for both micro-scale ($5 \times 5\ \mu\text{m}^2$) and nano-scale ($50 \times 50\ \text{nm}^2$) TiO_2 memristive devices (see Fig. S7 in Supplementary Information of [139]).

3.3.2. Nonlinear Ionic Drift Memristive Model

To the author's best knowledge, the nonlinear ionic drift model presented in [139], which uses the Simmons $i - v$ expression for the insulating region as a rectangular barrier with image forces [160], is up to now the most accurate model for the TiO_2 memristive devices. By using physically reasonable parameters, it properly describes both the static electric conduction as well as the switching dynamic behaviors and provides a good fit to the experimental data from micro-scale and nano-scale TiO_2 memristive devices which exhibit switching behaviors effectively insensitive to the device size [139].

According to this model, the voltage across the thin-film is given by

$$v_{\text{int}} = iR_{\text{doped}} + v_{\text{g}} \tag{3.13}$$

where v_{g} is the voltage across the insulating region which acts as a tunneling barrier and i is the current flowing through the device and its functional form is determined by [139]

$$i = \frac{j_{0A}}{\Delta w^2}\left[\phi_{\text{I}}\, \mathrm{e}^{\left(-B\sqrt{\phi_{\text{I}}}\right)} - (\phi_{\text{I}} + e|v_{\text{g}}|)\, \mathrm{e}^{\left(-B\sqrt{\phi_{\text{I}}+e|v_{\text{g}}|}\right)}\right]. \tag{3.14}$$

The quantities from Eq. 3.14 are given by [139]

$$j_0 = \frac{e}{2\pi h},\ \Delta w = w_2 - w_1, \tag{3.15}$$

$$w_1 = \frac{1.2\lambda w}{\phi_0},\ w_2 = w_1 + w\left(1 - \frac{9.2\lambda}{3\phi_0 + 4\lambda - 2e|v_{\text{g}}|}\right), \tag{3.16}$$

$$\lambda = \frac{e^2 ln(2)}{8\pi k \varepsilon_0 w}, \tag{3.17}$$

$$B = \frac{4\pi\Delta w\sqrt{2m}}{h}, \tag{3.18}$$

$$\phi_{\mathrm{I}} = \phi_0 - e|v_{\mathrm{g}}|\frac{w_1 + w_2}{w} - \frac{1.15\lambda w}{\Delta w}\ln\left(\frac{w_2(w - w_1)}{w_1(w - w_2)}\right), \tag{3.19}$$

where A describes the insulating region area, e is the electron charge, h is Planck's constant, ϕ_0 is the barrier height, k is the dielectric constant, and m is the electron mass. The modulation of the effective insulating region width w with respect to the device current has been expressed

for $i > 0$ (OFF switching):

$$\frac{dw}{dt} = f_{\mathrm{off}}\sinh\left(\frac{i}{i_{\mathrm{off}}}\right)\exp\left[-\exp\left(\frac{w - a_{\mathrm{off}}}{w_{\mathrm{c}}} - \frac{|i|}{b}\right) - \frac{w}{w_{\mathrm{c}}}\right] \tag{3.20}$$

with the fitting parameters $f_{\mathrm{off}} = 3.5 \pm 1$ μm/s, $i_{\mathrm{off}} = 115 \pm 4$ μA, $a_{\mathrm{off}} = 1.20 \pm 0.02$ nm, $b = 500 \pm 90$ μA, and $w_{\mathrm{c}} = 107 \pm 4$ pm;

and

for $i < 0$ (ON switching):

$$\frac{dw}{dt} = f_{\mathrm{on}}\sinh\left(\frac{i}{i_{\mathrm{on}}}\right)\exp\left[-\exp\left(\frac{w - a_{\mathrm{on}}}{w_{\mathrm{c}}} - \frac{|i|}{b}\right) - \frac{w}{w_{\mathrm{c}}}\right] \tag{3.21}$$

with the fitting parameters $f_{\mathrm{on}} = 40 \pm 10$ μm/s, $i_{\mathrm{on}} = 8.9 \pm 0.3$ μA, $a_{\mathrm{on}} = 1.80 \pm 0.01$ nm, $b = 500 \pm 90$ μA, and $w_{\mathrm{c}} = 107 \pm 3$ pm for physical TiO_2 memristive devices characterized in [139]. The model fits the experimental data using the device parameters determined as $\phi_0 = 0.95 \pm 0.03$ eV, $A = 10^4 \pm 2500$ nm^2, $k = 5 \pm 1$, $R_{\mathrm{doped}} = 215\Omega$ [139].

The total resistance of the device (memristance) is equal to

$$R_{\mathrm{total}} = \frac{v_{\mathrm{out}}}{i} = R_{\mathrm{int}} + R_{\mathrm{Pt}} = R_{\mathrm{doped}} + \frac{|v_{\mathrm{g}}|}{i} + R_{\mathrm{Pt}} \tag{3.22}$$

where v_{out} is the applied voltage on the memristor, i is the current flowing through the device, and $R_{\mathrm{Pt}} = 2.4\mathrm{k}\Omega$ accounts for the Pt electrodes resistance [140].

This model properly describes the nonlinear switching dynamics arising from the ionic motion which modulates the effective width of the insulating region (Eq. 3.20 and Eq. 3.21) as well as the electron tunneling effect through the insulating region which is a function of the width of the insulating region and the applied voltage/current (Eq. 3.14). Eq. 3.20 and Eq. 3.21 successfully model the nonlinear drift velocity of ionized dopants [139] featuring an exponential dependence on the applied current/voltage [149] and the asymmetric switching behavior [139] caused by the voltage polarity dependent competitive or cooperative behavior of ionic drift and diffusion [148].

Fig. 3.4a shows the initial memristances (before any modulation in w) for different values of w as a function of the applied voltage. It illustrates that the instantaneous value of the memristance exponentially decreases with respect to the applied voltage during the switching. In fact, the electrical resistance of the device depends on the applied voltage. Therefore, low-voltage measurements are used to readout the memristance [76], which not only allows us to provide non-destructive reads but also reduces the tunneling effect. Due to the coupling between Eq. 3.14 and Eq. 3.22, the memristance needs to be calculated numerically. Fig. 3.4b shows the memristance as a function of w when a readout voltage of 0.2 V is applied to the device. It illustrates that a sub-nanometer modulation in the insulating region effective width provides a $k\Omega - M\Omega$ readout ON-OFF-switching regime [139].

Fig.3.5 shows the dependence of the memristance during ON (high-to-low resistance) switching as it follows from the linear and nonlinear ionic drift models. Due to a high voltage level applied ($V = 1.5V$), the tunneling effect trough the insulating undoped region dominates the memristor $i - v$ characteristics [139]. Therefore, during the switching, the total resistance is even lower than R_{on}, in contrast to the behavior predicted by the linear model according to Eq. 3.7. From Fig.3.5 one can see that the TiO_2 component announced by Hewlett Packard (HP) in 2008 [70], at least at high voltage regimes, is rather a memristive system [71] than a memristor as its electrical resistance at a time is not only a function of historic profile of the applied voltage/current but also of the instantaneous value of the applied voltage/current due to electron tunneling. Furthermore, Fig. 3.5 demonstrates that when the linear model to obtain the $i - v$ characteristics of S and T, the voltage drops v_S and v_T (Eq. 3.4) will be wrongly predicted and the implication gate optimization will not be reliable.

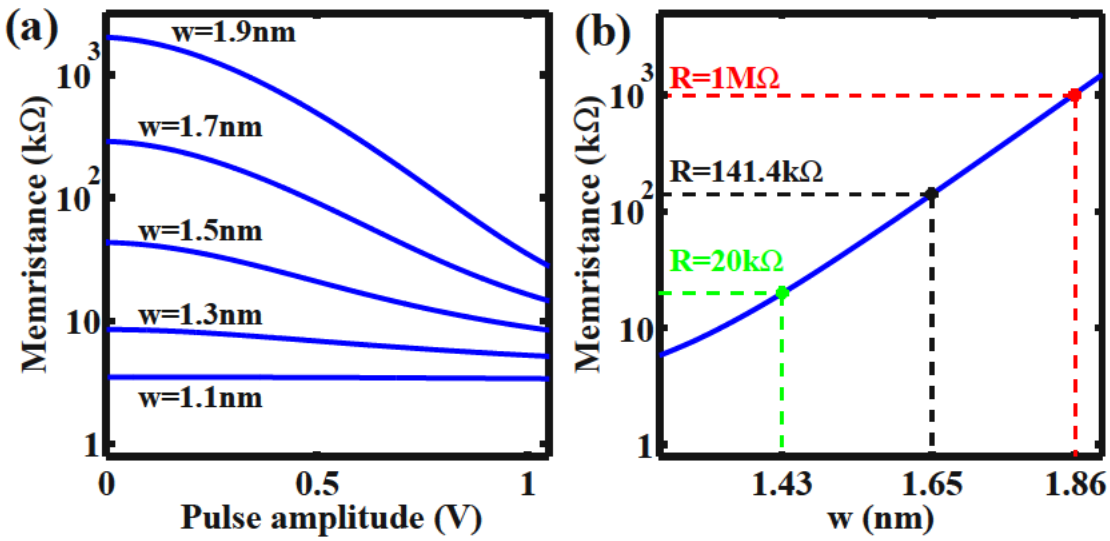

Figure 3.4.: (a) $M - V$ characteristics of the TiO_2 memristor for different values of w. (b) $M - w$ characteristics plotted for a readout voltage of 0.2 V.

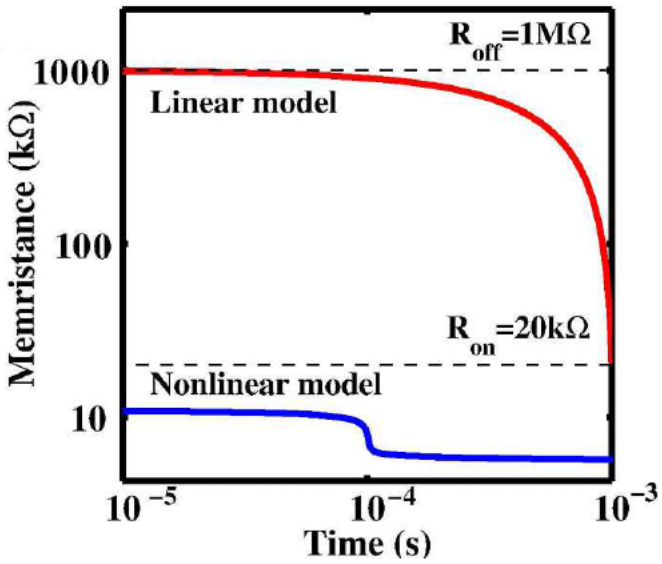

Figure 3.5.: Memristance profile of the TiO_2 memristive device during a high-to-low resistance switching according to the linear and nonlinear models.

The linear model can be useful only in analysis and design of low voltage applications ($-0.5\text{V} < v_\text{M} < 0.5\text{V}$) where the tunneling is negligible.

3.4. Simulation Results

In order to analyze the TiO_2-based memristive circuit (Fig. 3.2), the nonlinear model is used for each TiO_2 memristive switch and thus, coupled with the equation Eq. 3.4, Eq. 3.13–Eq. 3.22 are numerically solved for both S and T. Fig. 3.6 shows the modulation of the tunnel barrier widths w_S and w_T during the implication operation for all possible input patterns (State 1–State 4) described in Table 3.2. It illustrates that for pulse durations between 1–10 ms, only in State 1, the target memristor (T) is switched and in all other cases both S and T are left unchanged. Accordingly, correct logic behavior is achieved for all input states and the logic result is stored as the final resistance state of T. Here, the initial tunnel barriers are $w_\text{off} = 1.86$ nm and $w_\text{on} = 1.43$ nm which are equivalent to $M_\text{off} = 1\text{M}\Omega$ and $M_\text{on} = 20\text{k}\Omega$ at the readout voltage of 0.2 V (Fig. 3.4). The circuit parameters $R_\text{G} = 4.41$ kΩ, $\text{V}_\text{SET} = -2.28$ V, and $\text{V}_\text{COND} = -2.14$ V are optimized to minimize the SDE as is explained below.

According to Fig. 3.6, the dominant SDs occur in State 1 (Fig. 3.6a) in T ($\text{SD}_\text{T1} = w_\text{T} - w_\text{on}$) and in State 3 (Fig. 3.6c) in T ($\text{SD}_\text{T2} = w_\text{off} - w_\text{T}$). Therefore, maximizing the modulation of the voltage V_G between State 3 and State 1 ($\Delta V_\text{G} = |V_\text{G3} - V_\text{G1}|$) minimizes the possible SDEs in T. Fig. 3.7 shows ΔV_G as a function of R_G for different

values of $V_{S,C}$ where

$$V_{S,C} = \frac{V_{SET} - V_{COND}}{V_{SET}}. \tag{3.23}$$

As follows from Fig. 3.7, the optimum R_G corresponds to the maximum ΔV_G which maximizes the modulation of the voltage drop on T between State 3 and State 1 and thus minimizes the SDEs in T shown in Fig. 3.6. Therefore, it is uniquely defined by the memristor's properties, V_{SET} and V_{COND}. By using Fig. 3.7, an optimum R_G is obtained for each value of $V_{S,C}$ and then one can optimize $V_{S,C}$ to minimize the gate error (Fig. 3.8).

In fact, the voltage modulation ΔV_G increases with increased V_{COND} and minimizes

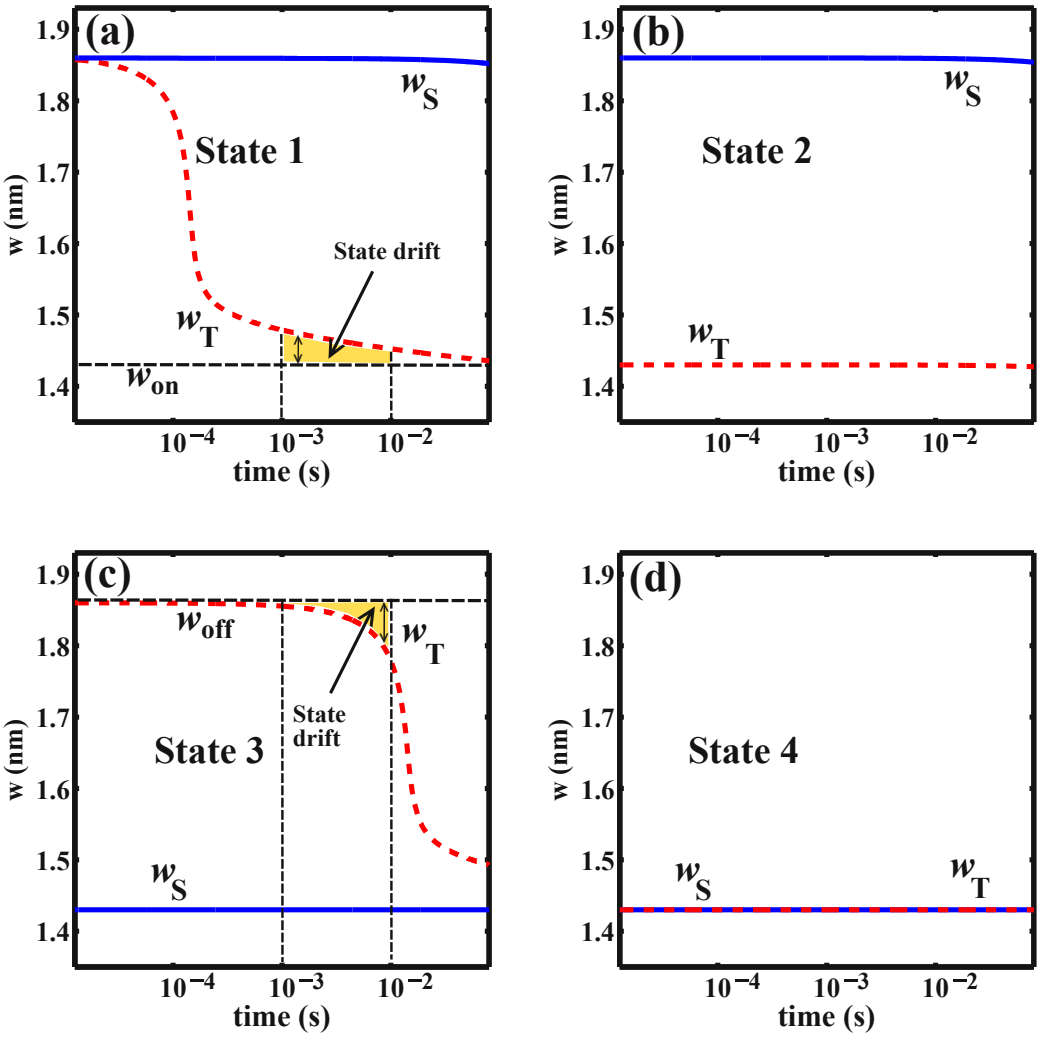

Figure 3.6.: Modulation of w_S and w_T during the logic operation for different input patterns.

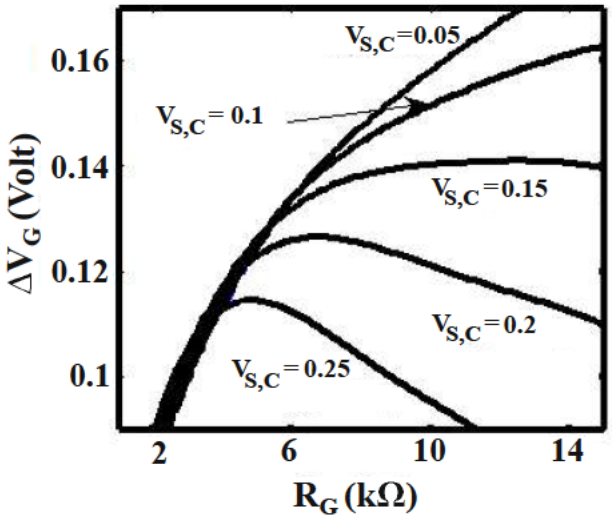

Figure 3.7.: ΔV_{G} as a function of R_{G} for different values of $V_{\mathrm{S,C}}$.

the SD in memristor T. However, an increase in $\mathrm{V_{COND}}$ results in an increasing error on memristor S, because it tends to switch S in State 1 ($\mathrm{SD_{S1}} = w_{\mathrm{off}} - w_{\mathrm{S}}$) and State 2 ($\mathrm{SD_{S2}} = w_{\mathrm{off}} - w_{\mathrm{S}}$). Therefore, there is an optimum $V_{\mathrm{S,C}}$ for which the total state drift ($\mathrm{SD_{total}}$) defined as normalized root mean square error as shown in Fig. 3.8. Optimum $\mathrm{V_{COND}}$ and $\mathrm{R_G}$ are determined at any $\mathrm{V_{SET}}$ by

$$\mathrm{SD_{total}} = \frac{\sqrt{\mathrm{SD_{T1}^2} + \mathrm{SD_{T3}^2} + \mathrm{SD_{S1}^2} + \mathrm{SD_{S2}^2}}}{2(w_{\mathrm{off}} - w_{\mathrm{on}})}. \tag{3.24}$$

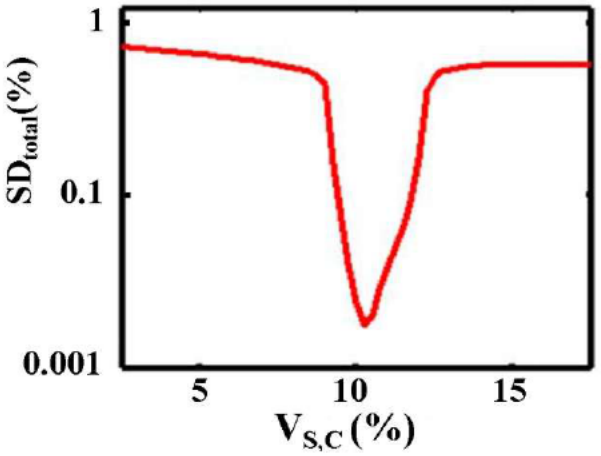

Figure 3.8.: Total state drift as a function of $V_{\mathrm{S,C}}$.

TiO_2 memristive switches enable stateful implication logic by serving simultaneously as non-volatile memory and logic gates. Although the digital data is stored in the high- and low-resistance state of the memristive device, the internal state variable w shows analog behavior (Fig. 3.6). Therefore, during the logic operations the voltage drops on S and T tend to push w toward w_{on}, also when their switching is undesired. This causes the state drift error, which accumulates in sequential logic steps and results in a one-bit error after a certain number of implication operations. Thus, refreshing circuitry is required to avoid this error [163]. Fig. 3.9 shows the cumulative SD in T during 20 implication operations with 1 ms pulse duration when T and S are in high and low resistance states, respectively (State 3). It illustrates that after 14 steps the sate variable w is equal to the median value of $(w_{\text{off}} + w_{\text{on}})/2 \simeq$1.65 nm which can be readout either as high- or low-resistance state. Whereas any resistance switching in State 3 is considered as an undesired switching, the initial logic state of T has to be rewritten before w reaches 1.65 nm. It is worth mentioning that the linear model predicts a SD of 48.9% [163] for a particular design example which means a refreshing is required after each implication operation. Compared to the nonlinear ionic drift model, the linear drift model exhibits higher state drift values since it assumes that the state drift is directly proportional to the current or voltage of the memristive devices. However, according to experimental data, the ionic drift velocity shows an exponential dependence on the applied current or voltage [149] which is taken into account in the nonlinear model by Eq. 3.20 and Eq. 3.21. Once again one has to note that, as high switching voltages are used for (high-speed) computing, the memristor nonlinear model has to be used to take the tunneling effect and dynamical memristor behavior into account.

Fig. 3.10 shows only a slight increase of the optimized V_{SET} pulse amplitude with the implication switching time decreased in contrast to the linear model. This results in large power consumption benefits at higher IMP speed (Fig. 3.11) and shows a good

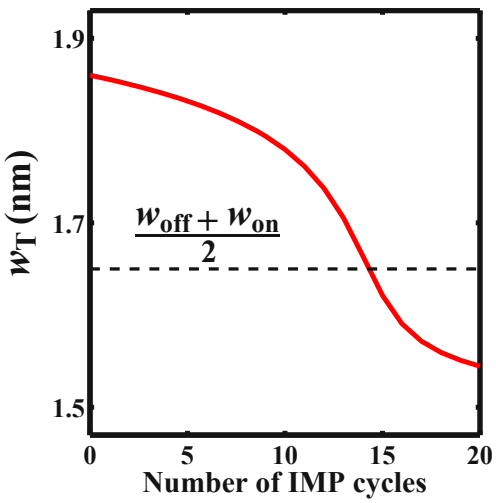

Figure 3.9.: Cumulative state drift effect in T for State 3.

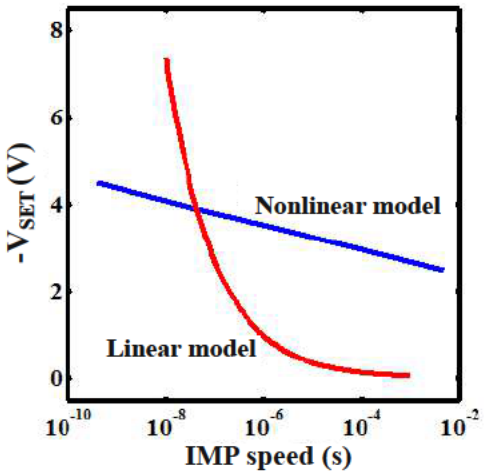

Figure 3.10.: Optimized V_{SET} pulse amplitude as a function of the pulse duration (IMP speed) based on the linear and the nonlinear memristor models.

agreement between simulations based on the nonlinear model and the available experimental data (see Fig. S5(b) in Supplementary Information of [76]) which demonstrates a decrease in switching energy of a TiO_2 memristive device with the pulse duration decreased. In fact, Fig. 3.11 demonstrates that when the linear model is used, event the trend of the average implication energy consumption ($\overline{\mathcal{E}}_{\mathrm{IMP}}$) is wrongly predicted

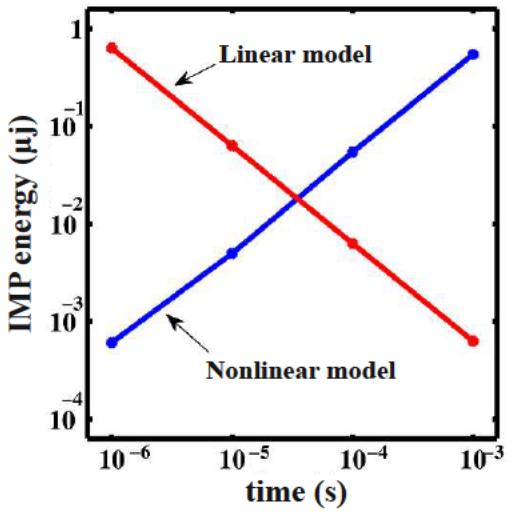

Figure 3.11.: Average implication operation energy ($\overline{\mathcal{E}}_{\mathrm{IMP}}$) as a function of the IMP speed based on the linear and the nonlinear memristor models.

as it shows an increase with the IMP speed increased.

$$\overline{\mathcal{E}}_{\mathrm{IMP}} = \frac{1}{4}\sum_{i=1}^{4} \mathcal{E}_{\mathrm{IMP}}(i), \tag{3.25}$$

where $\mathcal{E}_{\mathrm{IMP}}(i)$ denotes the implication energy consumption when the memristive devices S and T are initially in State i.

3.5. Summary

The realization of the stateful implication logic, a new kind of logic based on material implication which is computationally complete, provides zero-standby power for intrinsic logic-in-memory designs based on TiO_2 memristive devices. In this chapter, studies on TiO_2-based memristive stateful logic gates are presented. As under high voltage regimes required for (relatively) high-speed computing (Fig. 3.10), the electron tunneling significantly affects the electrical behavior of the of TiO_2 memristive devices, a nonlinear memristor model has been employed to analyze and optimize the TiO_2-based memristive stateful logic gates. The circuit parameters of the gate are optimized to ensure correct implication logic behavior and to minimize the state drift error accumulations for different input patterns. Simulation results based on the nonlinear memristor model show a good agreement with experimental observations and illustrate that, in order to avoid a state computation error, a refreshing is required after a limited number of logic steps (10–20 steps) as the state drift errors accumulate in sequential logic steps. This is very unfavorable as it needs extra hardware for refreshing and increases complexity. Furthermore, limited number of cycles for reversibly and reliably switching (so-called endurance) is still a major challenge for metal/oxide/metal technology to be used as universal memory cells or computing devices [164–167]. Compared to the spintronic devices, TiO_2 memristive switches exhibit at least three orders of magnitude lower endurance [82]. In addition, spintronic devices provide a very fine level of control and faster switching [65, 168] compared to the TiO_2 memristive devices which exhibit a very low mobility of dopants (oxygen vacancies) in the TiO_2 thin film [70].

4. Spintronic Memristive Stateful Logic Gates

4.1. Overview

Spintronics emerged with the discovery of the giant magnetoresistance (GMR) of magnetic multilayers in 1980s [30,31] which brought the Nobel prize to Fert and Grünberg in 2007 [24]. Spintronic devices exploit the electrons' spin degree of freedom to provide novel functional properties. Spin dependent tunneling in magnetoresistive devices with a tunnel barrier junction structure shows a higher resistance as well as a higher resistance modulation compared to other magnetoresistive devices [32]. Therefore, magnetic tunnel junctions (MTJs) are very favorable for magnetoresistive random-access memory (MRAM) technology [22, 23]. Despite the advantages of CMOS compatibility, high speed, and unlimited endurance, the first generation of MTJs [41–43], which utilized Oersted fields for the magnetization switching, was unfavorable in terms of scalability and energy consumption. By using the spin-transfer torque [44,45] switching technique [46,47], the second generation of the MTJ (STT-MTJ) [48–50] eliminates the need for current lines adjacent to memory cells, which were required previously for generating a switching field. Thus, by using the same lines for reading and writing operations, the STT-MTJ is more scalable and allows for smaller switching energies [22, 23].

As one of the most promising non-volatile storage technologies, STT-MTJ is also attractive for non-volatile logic applications to overcome scaling obstacles of CMOS logic circuits like the leakage power issue [37, 52–60]. By using the STT-MTJ technology the effective area and interconnection delay can be reduced due to an easy three-dimensional integration of the MTJs on top of the CMOS layers (Fig. 4.1). However, in hybrid CMOS/MTJ logic circuits the MTJs are used only as ancillary devices, which store solely the computation results. Therefore, sensing amplifiers [169] are required to read the data at each logic stage and to provide the next stage with an appropriate voltage or current signal as input. This increases the device count, delay, and power consumption. In addition, the generalization to large-scale logic systems is problematic. The use of spintronic devices as the main computing elements (logic gates) in novel computational architectures is a promising solution to address the above-described issues. The focus of this chapter is stateful logic gates which employ spintronic devices as logic gates.

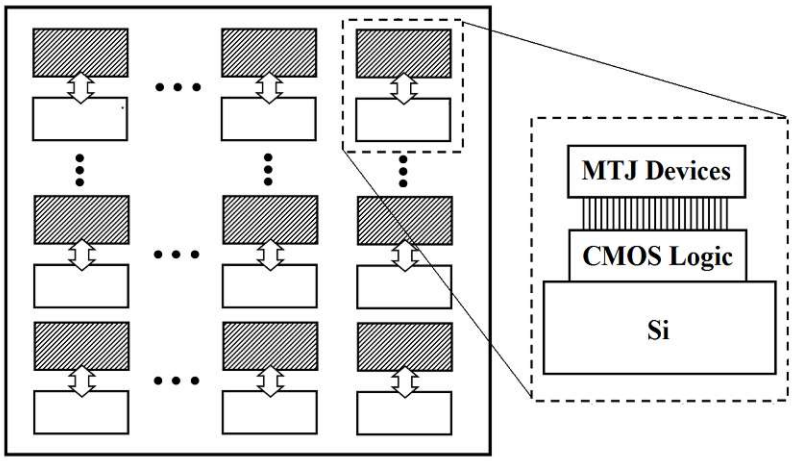

Figure 4.1.: Logic-in-memory architecture and the three-dimensional structure of the magnetic logic circuits.

4.2. Implication Logic Using DW-TMR Memristors

Combining the domain wall (DW) motion induced by the spin-transfer torque (STT) [44, 45] with the tunnel magnetoresistance (TMR) effect [170] has launched new concepts for spintronic memristive devices [62, 65, 97]. The TMR effect is observed as a change in the electrical resistance of a magnetic device depending on the relative magnetization states of two ferromagnetic layers separated by a non-magnetic insulating layer (whether ferromagnetic layers are in a parallel or an antiparallel alignment). Compared to the memristive devices based on ionic motion (e.g. TiO_2 memristor), spintronic memristors are more favorable in terms of speed, endurance, fine-tunability, and CMOS compatibility [66, 82, 117, 137]. In this section it is shown that the implication logic operation can be implemented based on DW-TMR memristive devices (Fig. 4.2), with the DW positions serving as state variables. This enables stateful logic operations that extends spintronics from non-volatile memory to logic applications, for which the spintronic memristor serves simultaneously as gate and latch.

4.2.1. DW-TMR Memristor

The STT effect allows to manipulate the local magnetization in a magnetic device by transfusion of magnetic momentum from a spin polarized current. Therefore, a spin-polarized current can induce motion in magnetic domain walls. Because of its potential applications, STT domain wall motion (STT-DWM) has generated wide interest and has been well studied theoretically and experimentally [171–178]. In a spintronic device, when the total electrical resistance depends on the magnetization state, on one hand, and the current flowing through the device can modulate the magnetization

state, on the other hand, the device exhibits memristive capabilities [61–68]. In fact, the magnetization state and thus the electrical resistance of such a device becomes a function of the historic profile of the current or the voltage applied to the device which represents memristive behavior.

Fig. 4.2 shows the basic structure [97, 138] and a (possible) top view [65] of a domain wall tunnel magnetoresistance (DW-TMR) memristor comprising an insulating layer and two ferromagnetic layers, a reference layer with a fixed (pinned) magnetization state and a free layer which is divided into two segments by a magnetic domain wall. The electrical resistance of the device depends on the relative orientation of the magnetization directions. A complete antiparallel alignment results in a high-resistance state (HRS; R_{H}) of the device, while a fully parallel alignment places it in a low-resistance state (LRS; R_{L}). The total resistance (memristance) of the device is modeled by two resistors connected in parallel R_{P} and R_{AP} as [138]

$$R_{\mathrm{P}} = \frac{R_{\mathrm{L}}}{r} \tag{4.1}$$

and

$$R_{\mathrm{AP}} = \frac{R_{\mathrm{H}}}{1-r}, \tag{4.2}$$

where x is the domain wall position, r represent the relative DW position ($0 \leq r = x/L \leq 1$), and L denotes the length of the free layer. Therefore, the $i-v$ characteristics of the device is obtained as

$$v = R(r)i, \tag{4.3}$$

where

$$M(r) = R(r) = \frac{R_{\mathrm{H}}\, R_{\mathrm{L}}}{rR_{\mathrm{H}} + (1-r)R_{\mathrm{L}}}. \tag{4.4}$$

When the DW velocity $V_{\mathrm{DW}}(t)$ is proportional to the applied current density ($j(t) =$

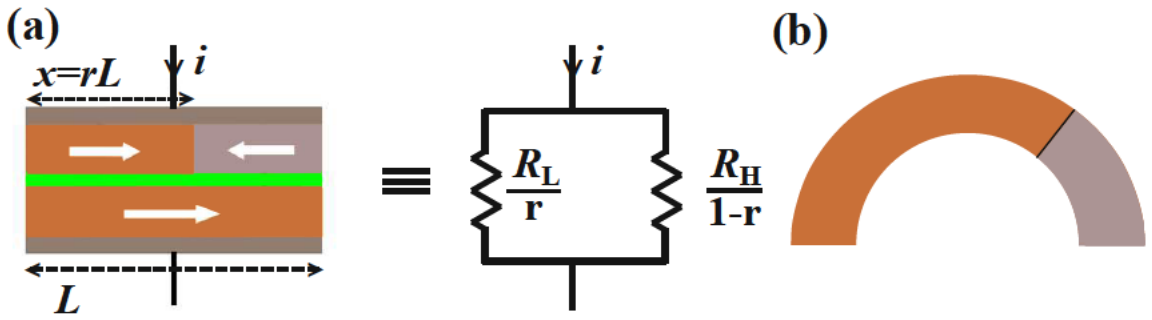

Figure 4.2.: (a) DW-TMR memristor structure and its equivalent circuit.
(b) A top view of the free layer of a DW-TMR memristor.

$i(t)/A$), the dynamics of r is obtained as [138]

$$\frac{dr}{dt} = \frac{1}{L}\frac{dx}{dt} = \frac{1}{L}V_{\mathrm{DW}}(t) = \frac{\Gamma_{\mathrm{DW}}}{L}\ j_{\mathrm{eff}}(t), \tag{4.5}$$

where

$$j_{\mathrm{eff}}(t) = \begin{cases} 0, & j(t) < j_{\mathrm{cr}} \\ j(t), & j(t) \geq j_{\mathrm{cr}} \end{cases} \tag{4.6}$$

Γ_{DW} is a DW velocity coefficient related to the device characteristics and A is the DW cross-sectional surface. The DWM appears when the current density $j(t)$ is above a critical current density (j_{cr}) [138]. Eq. 4.4 and Eq. 4.5 demonstrate that the device acts as a memristive system. Recently, a physical realization of DW-TMR memristive devices has been reported in [65].

4.2.2. Domain Wall Dynamics

The DW-TMR memristor model described above includes simplifying assumption from [138] regarding the dynamics of the current-induced DWM ($V_{\mathrm{DW}} \propto j_{\mathrm{eff}}$). Here, a more accurate modeling of the current-induced DWM is presented which can be used to drive the State equation (Eq. 2.15) of the DW-based devices operating as memristive systems (see Section 2.1.2).

The modified Landau-Lifshitz-Gilbert (LLG) equation [179] with an added spin-torque term [45] can be used to describe the magnetization dynamics of a current-induced DWM as [175, 176]

$$\frac{\partial \vec{\mathrm{m}}}{\partial t} = -\gamma_0 \vec{\mathrm{m}} \times \vec{\mathrm{H}}_{\mathrm{eff}} + \alpha \vec{\mathrm{m}} \times \frac{\partial \vec{\mathrm{m}}}{\partial t} - \frac{jP\mu_{\mathrm{B}}}{eM_{\mathrm{s}}}\left[(\vec{\mathrm{u}}.\vec{\nabla})\vec{\mathrm{m}} - \beta \vec{\mathrm{m}} \times \left((\vec{\mathrm{u}}.\vec{\nabla})\vec{\mathrm{m}}\right)\right]. \tag{4.7}$$

$\vec{\mathrm{m}}(r)$ is a unit vector representing the direction of the local magnetic moments, γ_0 is the gyromagnetic ratio, $\vec{\mathrm{H}}_{\mathrm{eff}}$ denotes the effective magnetic field, α represents the Gilbert damping parameter. The third term in Eq. 4.7 represents the spin-torque term of the current flowing in the direction $\vec{\mathrm{u}}$, where j shows the injected current density, P denotes the spin polarization of the current, μ_{B} is the Bohr magneton, M_{s} represents the saturation magnetization, and β defines the strength of the non-adiabatic spin-torque.

By using the collective coordinate approach which assumes that the configuration of the DW can be explained by the collective coordinates the DW position (x) and the angle between spins at the wall center and the easy plane (ϕ), the LLG is simplified to Eq. 4.8 [180, 181].

$$\frac{d\phi}{d\hat{t}} + \alpha\frac{d\hat{x}}{dt} = \beta\ \hat{j}, \tag{4.8a}$$

$$\frac{d\hat{x}}{d\hat{t}} - \alpha\frac{d\phi}{d\hat{t}} = \sin(2\phi) + \hat{j}, \tag{4.8b}$$

where $\hat{t} \equiv tv_c/\lambda$, $\hat{x} \equiv x/\lambda$, $\hat{j} \equiv jP\mu_B/(e\gamma_0\lambda K_\perp)$, represent the aspect parameters time, DW position, and current density which are normalized to dimensionless units. Here, $v_c \equiv \gamma_0\lambda K_\perp/M_s$ is a constant with the velocity dimension, $\lambda = \sqrt{J/K}$ is the DW thickness, $K_\perp$ is the hard-axis anisotropy, J is exchange coupling constant, and K denotes the easy-axis anisotropy.

4.2.3. DW-TMR-Based Implication Logic

Fig. 4.3 shows an implication logic gate exploiting the DW-TMR memristive devices as non-volatile memory as well as logic gates. The implication operation is performed by applying the voltage pulses V_{SET} and V_{COND} which tend to enforce high-to-low resistance switching in the memristive device S and T.

The electrical resistances of S and T depend on the position of their DWs x_S and x_T which act as the state variables. The realization of the implication logic operating relies on a threshold current density below that the DWs does not move. Similar to the TiO_2-based implication logic gate, a high-to-low resistance switching is enforced in the target device (T) only when both S and T are in the high resistance state (State 1 shown in Table 3.2). Therefore, the conditional switching behavior equivalent to the basic operation of the implication logic is feasible using DW-TMR memristors.

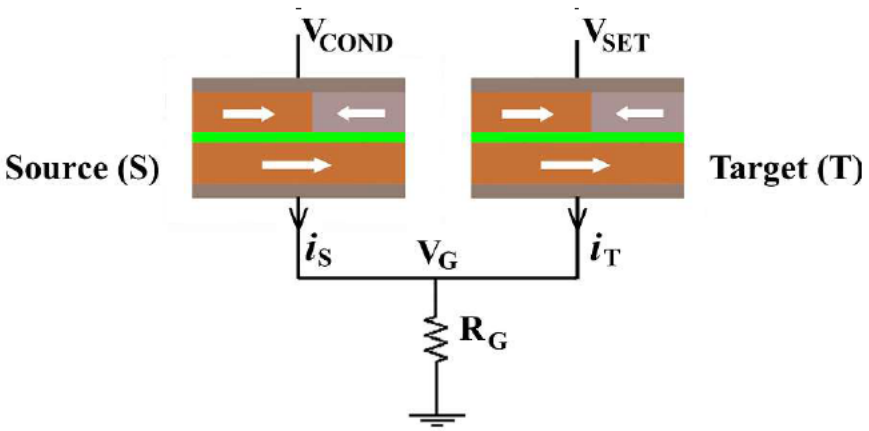

Figure 4.3.: DW-TMR-based implication logic gate.

In order to analyze the DW-TMR-based implication logic gate (Fig. 4.3), Eq. 4.4–Eq. 4.6 are numerically solved for both S and T coupled with Eq. 3.4 where i_S and i_T are the currents following through S and T, respectively. M_S and M_T represent their memristances which are a function of $r_S = x_S/L$ and $r_T = x_T/L$, respectively.

4.2.4. Simulation Results and Discussion

When S and T are in the high-resistance state (State 1), the current passing through T (j_{T1}) is above the critical current j_{cr} required for the STT-DWM (Fig. 4.4). Due to the voltage drop on R_G, the current passing through S (j_{S1}) is below j_{cr} and thus its DW does not move. Therefore, a high-to-low resistance switching is enforced only in T and M_S is left unchanged (State 1 in Fig. 4.5). As during the switching M_T decreases, the current density j_{T1} (j_{S1}) is increased (decreased). This acts as a positive feedback between j_{T1} and M_T which accelerates the current-induced DWM and allows reducing the time required for the implication operation. The memristor devices are characterized in [138] with physical dimensions and electrical parameters assumed as: the length of $L = 200$ nm, the width of $z = 10$ nm, the thickness of $h = 7$ nm, $R_H = 7.5$ kΩ, $R_L = 2.5$ kΩ, $\Gamma_v = 2 \times 10^{16}$ nm^3 C^{-1}, and $j_{cr} = 20$ nA nm^{-2}.

The resistance states of S and T are left unchanged for other combinations of initial states (State 2 – State 4 shown in Fig. 4.5). In fact, their current densities are below

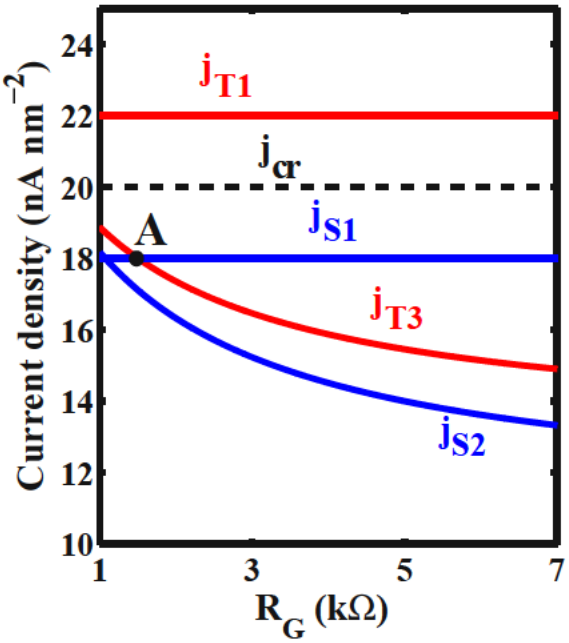

Figure 4.4.: Initial current densities passing through the DW-TMR memristor devices S and T as a function of R_G.

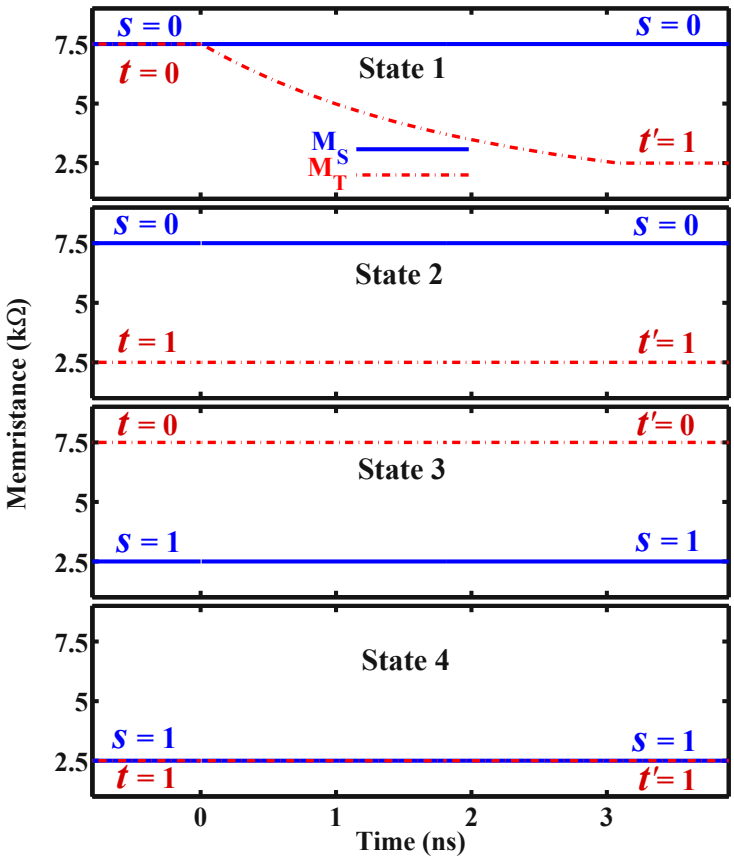

Figure 4.5.: M_S and M_T during the implication operation for different initial logic states (State 1 – State 4) explained in Table 3.2.

j_{cr} when they are initially in the high resistance state (j_{S2} in State 2 and j_{T3} in State 3 shown in Fig. 4.4). Therefore, the DW-TMR memristive gate exhibits the conditional switching behavior shown in Table 3.2. This is equivalent to the basic operation of the implication logic and enables spintronic stateful logic.

Fig. 4.6 shows the energy consumption of the DW-TMR gate ($\mathcal{E}_i$) at different initial states (State i) as a function of R_G

$$\mathcal{E}_i = \int_0^{\tau_{imp}} [M_S i_S^2 + M_T i_T^2 + R_G (i_S + i_T)^2] dt, \tag{4.9}$$

According to Fig. 4.6, a higher R_G increases the implication energy consumption. However, its minimum value is limited by State 3 to provide a correct logic behavior as shown in Fig. 4.4. In fact, a higher R_G increases the difference between j_{T1} and j_{T3} and ensures that M_T is not switched in State 3. Therefore, Point A for which $j_{S1} = j_{T3}$ (shown in Fig. 4.4) indicates an optimum value of R_G to ensure the correct logic behavior in all states.

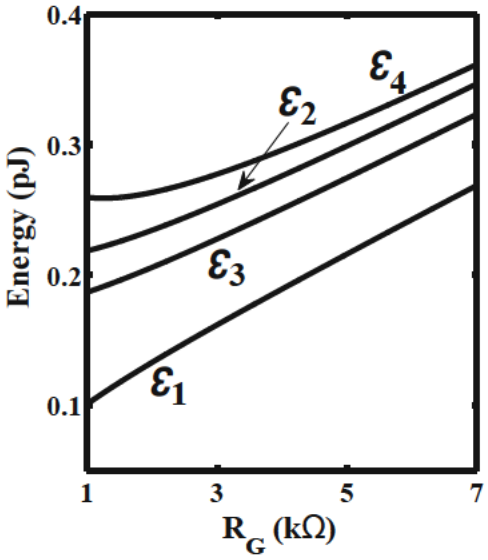

Figure 4.6.: Implication operation energy ($\mathcal{E}_i$) as a function of R_G in State i.

For more accurate analysis regarding the state drift errors, the one-dimensional model of magnetic DWs (see Section 4.2.2) has been used to investigate the DW dynamics in S and T during the implication operation. Here, coupled with Eq. 4.4 for S and T, Eq. 3.4 is numerically solved to calculate M_S (M_T) as a function of x_S (x_T), while the dynamics of x_S (x_T) is obtained by using Eq. 4.8. The memristor device geometries are supposed as $L = 100\lambda$, $z = 4\lambda$, and the free layer thickness as $h = \lambda$. Fig. 4.7 shows the DW dynamics of S and T for all possible inputs (State 1 to State 4). Due to their polarities, the voltage pulses V_{SET} and V_{COND} tend to increase r_S and r_T to enforce parallel alignment between free and pinned layers of S and T.

Since, the structure of the DW-TMR memristor devices is based upon existing magnetic memory technology it combines the advantages of CMOS compatibility, high speed, high density, almost unlimited endurance, and scalability and thus is very promising for spintronic memristors implementation [65]. However, although in stateful implication logic the DW-TMR memristors are used as two-resistance-state devices, they exhibits analog behavior as the DW displacement is continuous in value and is proportional to the amplitude of the injected current and the pulse duration. Therefore, similar to the TiO_2-based logic gates, this causes a state drift error during the implication operation. This error accumulates in sequential logic steps and is very unfavorable for stateful logic as it results in a computation error after a certain number of logic steps. According to Fig. 4.7, the major state drift error happens in x_T. It illustrates that after one implication operation the state drift error is about 10% and 5% in State 1 and State 3, respectively. Therefore, a refreshing is required after less than 10 logic steps as an accumulated error of $> 50\%$ cause a one-bit error in the readout. In the next section the realization of implication logic using STT-MTJs is demonstrated, which does not suffer from error accumulation problems. It

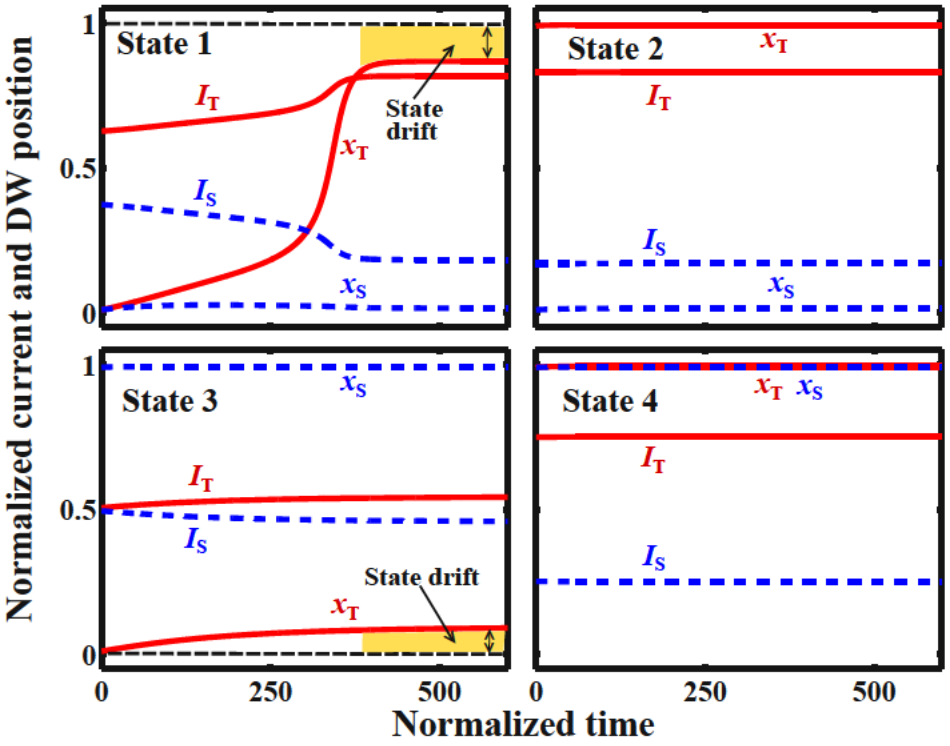

Figure 4.7.: The current signals (i_S and i_T) and the DW position ratios (r_S and r_T) of S and T during the implication operation.

is based on the STT-MRAM technology which has recently been commercialized by Everspin [182].

4.3. Novel Implication Logic Gates Using STT-MTJs

4.3.1. Device Principles

The basic structure of the magnetic tunnel junction consists of a free and a fixed (pinned) ferromagnetic layer separated by a tunneling oxide (Fig. 4.8). The magnetization of the free layer has a bistable configuration and can be switched between a parallel and an antiparallel state compared to the fixed magnetization direction of the pinned layer. The MTJ exploits the tunnel magnetoresistance effect associated with the relative angle between the magnetizations of the free and the pinned layers. An antiparallel alignment results in a high-resistance state (HRS; R_{AP}) of the MTJ, while the parallel alignment places it in a low-resistance state (LRS; R_P). The MTJ resistance modulation is described by the tunnel magnetoresistance (TMR) ratio and is defined as TMR $= (R_{AP} - R_P)/R_P$. Nowadays, the tunneling oxide is usually

MgO. Due to the enhanced spin filtering, MgO-based MTJs exhibit a high TMR ratio which is facilitated to read-out the MTJ resistance state via the TMR effect [38]. The TMR ratio record of up to 604% [183] reported in MgO-based MTJs is close to the theoretical maximum (∼1000%) [184, 185].

The magnetic state of the MTJ free layer can be switched either by a magnetic field or by a spin-polarized current via the STT effect. Compared to the first generation of MTJs, which utilized a magnetic field for switching, the STT switching technique exhibits pure electrical read/write operations and renders the current-carrying wire generating the magnetic field superfluous. This brings significant advantages with respect to scalability and energy consumption [22]. It makes the STT-MTJ a suitable candidate for a universal memory which combines the advantages of CMOS compatibility, non-volatility, high switching speed, high integration density, unlimited endurance, and scalability. Furthermore, the STT-MTJ shows memristive behavior [62, 72] as its magnetic state and thus the corresponding resistance is a function of the historic profile of the current passing through the MTJ. Indeed, the STT-MTJ exhibits the memristor fingerprint [72] characterized by a pinched $i-v$ hysteresis loop [186, 187].

In the following, the STT-MTJ-based realization of the stateful implication logic operation is demonstrated by using the conventional implication gate topology and a novel topology which significantly improves the performance of the STT-MTJ-based implication logic gates (Fig. 4.12). In the STT-MTJ-based logic gates, due to the magnetic bistability of the MTJ caused by an intrinsic damping in its magnetic free layer [23], the magnetization of the free layer can relax to its initial state when there is enough time (in the range of sub-nanosecond [188]) between sequential logic operations. Therefore, unlike the TiO_2 and the domain wall based logic gates, where the state drift errors are accumulated as described before, the need for refreshing circuitry in the STT-MTJ-based stateful logic systems is eliminated. In order to analyze and compare the performance of the STT-MTJ-based logic gates, considerations regarding the reliability of these gates are explained in the next section.

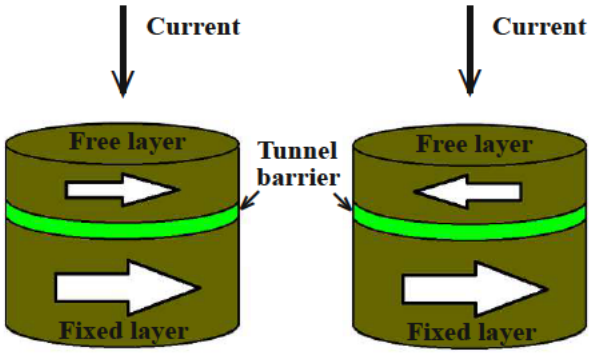

Figure 4.8.: Sketch of basic MTJ structure with a bistable (parallel/antiparallel) magnetization configuration in the free layer.

4.3.2. Reliability Modeling and Analysis

Initially, there was no performance analysis regarding STT-MTJ-based logic gates available, which are very favorable for stateful logic applications as discussed before. However, as it is shown in the following, the reliability analysis of the stateful logic operations is as an essential prerequisite for benchmarking and performance comparison of different STT-MTJ-based logic architectures. Here, based on the mechanism of the conditional switching behavior in stateful logic, a framework needed to perform the reliability modeling and analysis for the STT-MTJ-based stateful logic gates is described and used for investigating, optimizing, and comparing different STT-MTJ-based logic gates and architectures.

4.3.2.1. Reliable Switching

In order to analyze the stateful logic gates explained before and to further extend stateful logic to cover more devices and circuit topologies, the conditional switching behavior of a memristive device can be described by using Fig. 4.9, which shows the switching dynamic of a memristive element as a function of the applied voltage/current pulse amplitude. The horizontal axis denotes the voltage (or current) level applied to a memristive element for a specific time (a pulse duration of τ). The solid curve indicates the high-to-low (or low-to-high) resistance switching behavior of the device where the vertical axis represents a normalized internal state variable of the device. The internal state variable can represent the deterministic switching model of the memristive device (e.g. $w(t)$ in a TiO_2 memristive switch or the relative domain wall position r in a spintronic memristor) or the switching probability of a spintronic memristive element with a stochastic switching model (e.g. P_{sw} in a STT-MTJ). Region A shows a reliable switching region for which the dashed line represents the minimum reliable switching voltage (V_a) (or a corresponding current I_a). Region B denotes a reliable non-switching region for which the dashed line represents the maximum reliable non-switching voltage (V_b) below that the disturbance due to the applied voltage/current is negligible and it cannot force a switching event. When $V_b \neq 0$, the memristive device has a nonzero switching voltage/current threshold which is in general a function of the pulse duration τ.

In the TiO_2 or the DW-TMR memristive implication logic gates explained before, there are four possible high-to-low resistance switching cases depending on the initial resistance states, when the voltage pulses V_{SET} and V_{COND} are applied to the gates. However, only when both S and T are in the high resistance state (State 1), the voltage drop on T (the current flowing through T) is higher than V_a. In the other cases, the voltage drops on S and T are below V_b and, therefore, undesired switching events are avoided. For example, as in State 3 S is in the low-resistance state, the voltage or current of T is decreased and thus its high-to-low resistance switching is avoided. This conditional switching behavior, which comprises a set of desired and

undesired switching events, corresponds to implication logic. Similarly, in a STT-MTJ-based logic gate, depending on the initial resistance states of all MTJs a target (output) MTJ is switched or not. Reliability of such a conditional switching behavior can be defined as a function of the switching probabilities (P_{sw}) of desired switching events as well as $1 - P_{sw}$ for undesired switching events. This basic discussion can be used to study, optimize and compare STT-MTJ-based logic gates. Furthermore, it provides a better understanding of the conditional switching mechanism in stateful logic which paves the way for the proposal of logic gate with novel topologies. In the following, a SPICE model of the STT-MTJs is presented and modified to have the capability of calculating the reliabilities and error probabilities in the STT-MTJ-based logic gates.

4.3.2.2. Modified STT-MTJ SPICE Model

The STT-MTJ SPICE model presented in [189] includes a (deterministic) decision circuit to control a bistable circuit which shows an immediate switching between parallel and antiparallel states (Fig. 4.10). The decision circuit comprises two capacitors (C_1 and C_2) excited by two current sources (I_1 and I_2) connected in parallel to realize the relationship between the critical switching time and the critical switching current.

In fact, the rate of the charge/discharge of the capacitors is a function of the current

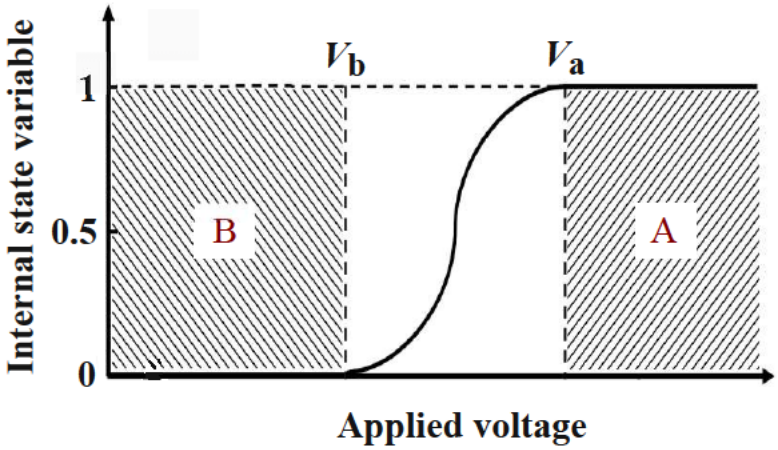

Figure 4.9.: Normalized internal state variable of a memristive device as a function of the applied voltage.

flowing through the MTJ (i) and is determined by [189]

$$I_1 = \exp\left(-\Delta\left[1 - \frac{i}{I_{C0(AP\rightarrow P)}}\right]\right) \tag{4.10}$$

and

$$I_2 = \exp\left(-\Delta\left[1 - \frac{i}{I_{C0(P\rightarrow AP)}}\right]\right). \tag{4.11}$$

Δ is the thermal stability factor and is equal to $\mathcal{E}_b/k_BT$. $\mathcal{E}_b$ represents the energy barrier between the parallel and the antiparallel magnetization states of the MTJ, k_B is the Boltzmann constant, and T is the temperature. $I_{C0(AP\rightarrow P)} > 0$ and $I_{C0(P\rightarrow AP)} < 0$ denote the critical currents for the antiparallel-to-parallel and parallel-to-antiparallel switching cases and are extrapolated to the critical switching time $t_0 = 1$ns. It has been shown that the time required to charge the capacitors C_1 and C_2 by exactly 1 V with the capacitance of 1 nF are given by [189]

$$t_{C1} = \frac{(1\ nF)(1\ V)}{I_1} = 1\ \text{ns} \times \exp\left(\Delta\left[1 - \frac{i}{I_{C0(AP\rightarrow P)}}\right]\right) \tag{4.12}$$

and

$$t_{C2} = \frac{(1\ nF)(1\ V)}{I_2} = 1\ \text{ns} \times \exp\left(\Delta\left[1 - \frac{i}{I_{C0(P\rightarrow AP)}}\right]\right). \tag{4.13}$$

In the thermally-activated switching regime (switching time t >10 ns), Eq. 4.12 (Eq. 4.13) is identical to the relationship between the critical switching time t_p and the critical switching current (I_C) of antiparallel-to-parallel (parallel-to-antiparallel) MTJ switching as [189]

$$I_C = I_{C0}\left[1 - \Delta \ln(\frac{t_p}{t_0})\right]. \tag{4.14}$$

As the critical values of switching time and current are usually defined for the MTJ switching probability of 50% [189], the decision circuit enforces an immediate switching to the bistable circuit as soon as the switching probability is 50%. The curve fitting circuit is used to take the voltage-dependent effective TMR ratio into account, which is important to determine the resistance-voltage characteristic of the MTJ. This SPICE model covers the major electrical characteristics of the STT-MTJs. It is, however, not possible to calculate the switching probabilities of the STT-MTJs required for reliability analysis and comparison of the STT-MTJ-based logic gates only based on this SPICE model (Fig. 4.11). Therefore, in order to calculate the STT-MTJ switching probability (P_{sw}), the theoretical expression for the thermally-activated switching regime [190] is used

$$P_{sw} = 1 - \exp\left(-\frac{\tau}{t_0}\exp\left[-\Delta\left(1 - \frac{I_{MTJ}}{I_{C0}}\right)\right]\right), \tag{4.15}$$

where I_{MTJ} is current flowing through the MTJ and τ is the pulse duration.

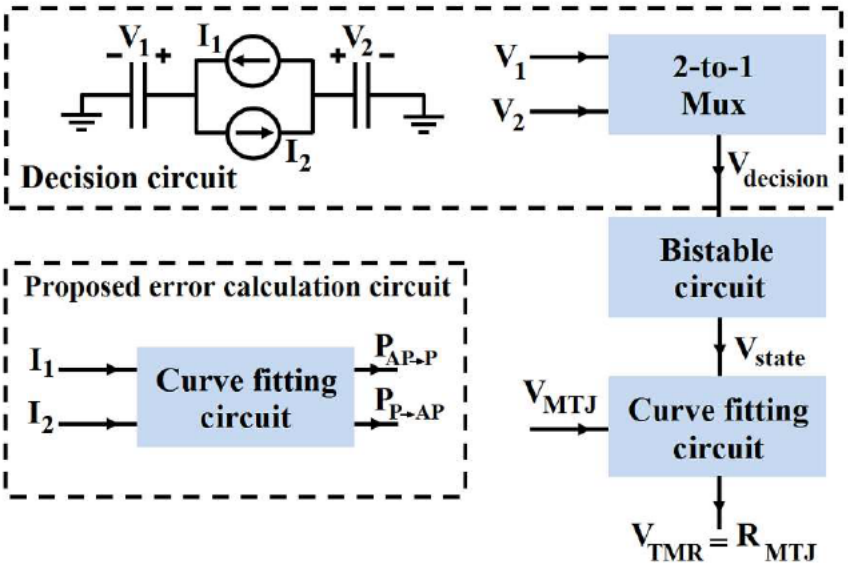

Figure 4.10.: Simplified equivalent circuit of the MTJ SPICE model and the proposed error calculation circuit.

Eq. 4.15 has been experimentally verified in [50] and can be added to the STT-MTJ SPICE model for switching probability (error) calculations by using a curve fitting

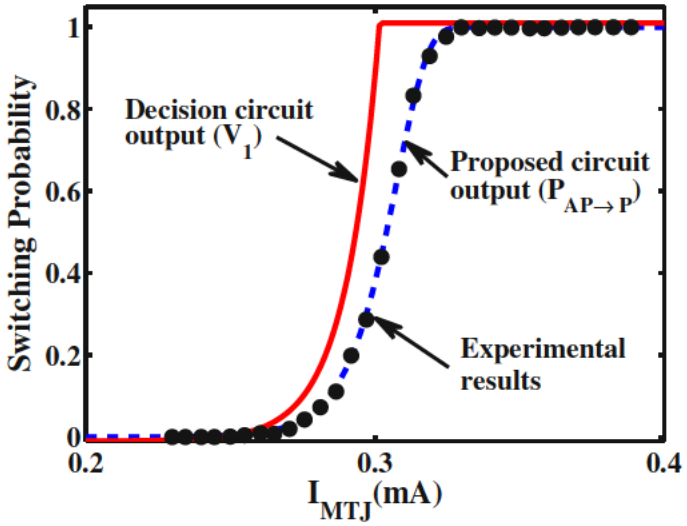

Figure 4.11.: STT-MTJ switching probability as a function of the applied current based on the modified STT-MTJ SPICE model compared to the decision signal V_1 from the (unmodified) SPICE model.

circuit shown in Fig. 4.10 characterized as

$$P_{\mathrm{AP}\rightarrow\mathrm{P}} = 1 - \exp\left(-\frac{\tau}{t_0} I_1\right) \tag{4.16}$$

and

$$P_{\mathrm{P}\rightarrow\mathrm{AP}} = 1 - \exp\left(-\frac{\tau}{t_0} I_2\right). \tag{4.17}$$

Fig. 4.11 compares the experimental results from [50] with the unmodified and the modified STT-MTJ SPICE models. It illustrates that although the decision signals V_1 in the (old) STT-MTJ SPICE predicts the correct critical switching current where the probability of the switching is 50%, it cannot fit the experimental data equally well.

In order to calculate the current flowing through the STT-MTJs in the stateful MTJ logic gates (described later), the voltage-dependent effective TMR model [191] is used, which determines the resistance characteristic of the MTJs in the antiparallel MTJ state as a function of the MTJ voltage (v_{MTJ}) as

$$R_{\mathrm{AP}} = R_{\mathrm{P}}(1 + \mathrm{TMR}_v) = R_{\mathrm{P}}\left(1 + \frac{\mathrm{TMR}_0}{1 + \frac{v_{\mathrm{MTJ}}^2}{V_{\mathrm{h}}^2}}\right). \tag{4.18}$$

TMR_0 and TMR_v are the TMR ratio under zero and non-zero bias voltage across the MTJ, respectively. $\mathrm{V_h}$ is the bias voltage equivalent to $\mathrm{TMR}_v = \mathrm{TMR}_0/2$.

4.3.3. Improved Implication Logic Gate

As explained before, due to the magnetic bistability of the MTJ, STT-MTJ logic gates eliminate error accumulation in stateful logic and thus are inherently suited for digital computing and are preferable over TiO_2-based or domain wall-based technologies, which exhibit error accumulation due to their analog behavior. In this section, STT-MTJs are employed to perform implication logic based on the conventional voltage-controlled (VC) implication gate topology (Fig. 4.12a) and a novel current-controlled (CC) topology (Fig. 4.12b). Based on the description of the reliable conditional switching cases (Section 4.3.2.1) and the modified STT-MTJ model (Section 4.3.3), the performance of these gates are compared and it is demonstrated that the proposed CC-IMP gate outperforms the conventional VC-IMP gate in terms of reliability and power consumption.

Similar to the memristive stateful implication gate (Table 3.2), in the voltage- and current-controlled implication gates (Fig. 4.12a and Fig. 4.12b) the logic operation

(N)IMP is realized based on a conditional switching in the target MTJ (T). Depending on the initial resistance states of the source and the target MTJs, an AP–to–P STT switching event is enforced in the target MTJ only, when both MTJs are initially at antiparallel (high resistance) states (State 1). For the other input patterns (State 2, State 3, and State 4), the resistance states of the MTJs are left unchanged as shown in Table 3.2. In the MTJ-based voltage-controlled implication (VC-IMP) gate (Fig. 4.12a), the logic operation is executed by simultaneously applying the voltage pulses V_{COND} and V_{SET}. As $|V_{\mathrm{COND}}| < |V_{\mathrm{SET}}|$, the voltage drop on S is smaller than the critical voltage level required for STT switching and thus S is left unchanged. The resistance state of S provides a voltage modulation across T through R_{G}. Due to this modulation, T switches, when S is in the high resistance state (State 1), but remains unchanged, when S is in the low resistance state (State 3).

In the CC-IMP gate (Fig. 4.12b) the logic operation is performed by applying the current pulse I_{imp} to the gate. I_{imp} is applied in a direction which tends to enforce AP–to–P switching events to both MTJs. The current I_{imp} is split between S and T inversely proportional to the total resistance of each branch. The current split depends on the input pattern as the resistance value of each branch is a function of the logic state of its MTJ. According to Table 3.2 there are four possible AP–to–P switching events containing State 1 and State 3 for T and State 1 and State 2 for S.

In order to better understand the operation of the implication gate, Fig. 4.13 shows the switching probabilities of S (P_{s}) and T (P_{t}) as a function of the current level applied to the implication gate (I_{imp}) for all possible AP–to–P switching events P_{t1}, P_{t3}, P_{s1}, and P_{s2}. The current direction of I_{imp} is fixed, so that only high-to-low resistance switching is feasible in both MTJs for any input combination. When both MTJs are initially in the high resistance state (State 1), low I_{imp} values ($\approx$ 0.4 mA) can not

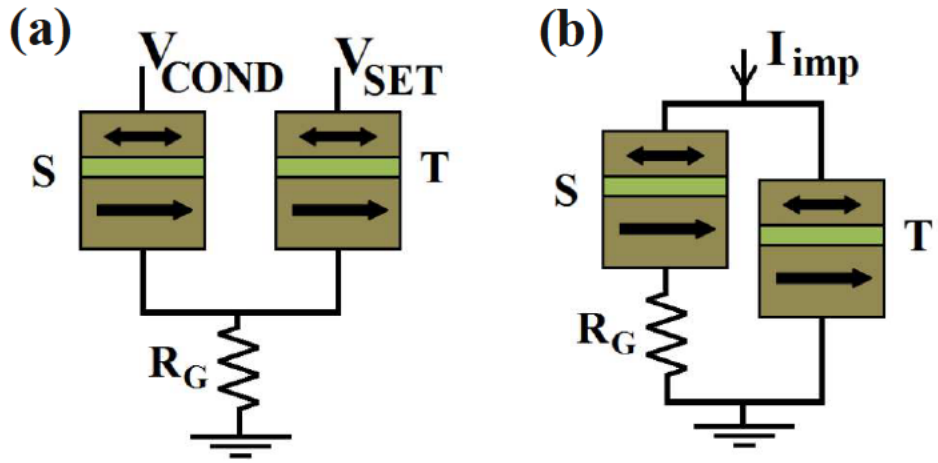

Figure 4.12.: STT-MTJ-based implication logic gates based on (a) the conventional voltage-controlled and (b) the proposed current-controlled topologies.

enforce any switching, because the currents flowing through both MTJs are below the required switching current.

For a correct implication logic behavior, T (S) must (not) switch to the low resistance state. Thus, I_{imp} has to be chosen in a way that T exhibits a high switching probability and S remains unchanged (within the reliable gap RG shown in Fig. 4.13). This gap is controlled by R_{G} as it limits the current flow through S. In State 2 S is in the high resistance state and the current flowing through S is lower than the value required for STT switching due to R_{G} and the low resistance state of T. In State 3, although T is in the high resistance state, I_{imp} does not switch T ($P_{\mathrm{t3}} \simeq 0$) since S is in the low resistance state. This requires a high enough S resistance modulation (high TMR) and also restricts the upper limit for R_{G}. When both MTJs are in the low resistance state (State 4), there is no possible switching event as the direction of the I_{imp} is fixed.

The reliability of the implication operation in State 1 is proportional to the multiplication of the probability of the desired switching event in T (P_{t1}) and the term $1 - P_{\mathrm{s1}}$, where P_{s1} is the probability of the undesired switching event in S. Therefore, in State 1, the error probability (E_1) is

$$E_1 = 1 - P_{\mathrm{t1}}(1 - P_{\mathrm{s1}}). \tag{4.19}$$

In State 2 and State 3, there are only undesired switching events (P_{s2} and P_{t3}) in S

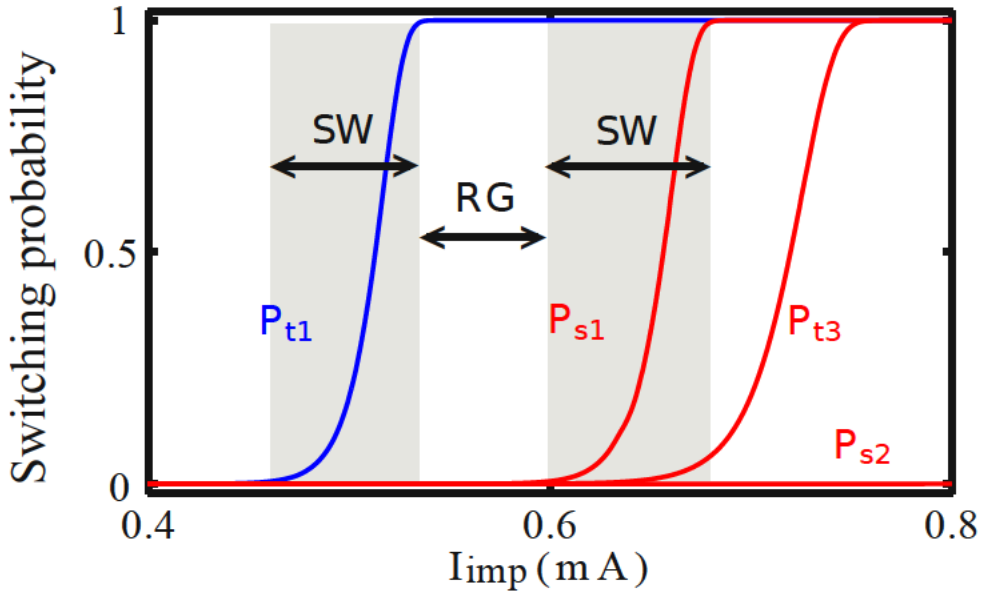

Figure 4.13.: AP–to–P switching probabilities of T and S in the CC-IMP gate as a function of I_{imp}.

and T, respectively. Therefore, the error probabilities are given by

$$E_2 = P_{s2}, \qquad E_3 = P_{t3}. \tag{4.20}$$

When both MTJs are in the low resistance state (State 4), there is no possible switching event and the error probability E_4 is zero. It is obvious that a reliable logic behavior of an operation is ensured only, when the logic gate exhibits correct functionality for all input patterns. Therefore, by assuming equal incidence probabilities for all input patterns, the average implication error probability ($\overline{E}_{IMP}$) is obtained by

$$\overline{E}_{IMP} = \frac{1}{4}\sum_{i=1}^{4} E_i = \frac{1}{4}(1 - P_{t1} + P_{s1}P_{t1} + P_{s2} + P_{t3}). \tag{4.21}$$

From a circuit point of view, the parameters (I_{imp} and R_G in the CC-IMP and V_{COND}, V_{SET}, and R_G in the VC-IMP gates) can be optimized to minimize the error probability $\overline{E}_{IMP}$ for given MTJ device characteristics. Fig. 4.14a shows the error probabilities E_i for different input states of the CC-IMP gate as function of I_{imp} for a fixed R_G with MTJ devices characterized by TMR = 250%, $\Delta = 40$, $I_{C0}(AP \rightarrow P) = 325\ \mu A$, and $R_P = 1.8\ k\Omega$. I_{imp} has to be high enough to enforce a desired switching of T in State 1. However, there is an optimum I_{imp}, as increasing I_{imp} increases the probabilities for undesired switching events in both T and S in State 1, State 2, and State 3.

In the CC-IMP gate R_G provides a structural asymmetry which increases the current flowing through T compared to S, when both MTJs are in the high resistance state (State 1). Therefore, increasing R_G reduces the error probability E_1 as it increases (decreases) the probability of the desired (undesired) switching event P_{t1} (P_{s1}) as shown in Fig. 4.14b. However, its maximum value is limited by E_3. In State 3, S is in the low resistance state and thus the current flowing through S is increased as compared to State 1. Therefore, the current flowing through T is decreased to a lower level, below the critical current required for the STT switching. Because a higher R_G decreases the effective resistance modulation of its corresponding branch (the source branch comprises R_G and S), it increases the error probability E_3 (Fig. 4.14b).

As explained before, a higher R_G reduces the error probabilities in State 1 and State 2 but is limited by the required current modulation in State 3. The current modulation in State 3 relies on the modulation of the MTJ resistance between its antiparallel and parallel magnetization states described by the MTJ's TMR ratio. From this follows that the TMR ratio is the main device parameter affecting the reliability of the implication gate. A higher TMR ratio provides a higher current modulation and allows higher values of R_G for CC-IMP circuit parameters optimization. Fig. 4.15a shows the two dominant error probabilities (E_1 and E_3) for two different TMR ratios. It illustrates that a higher TMR ratio has a negligible effect on E_1 but it decreases E_3. Therefore, for MTJs with increased TMR, the CC-IMP gate with optimized circuit parameters exhibits a more reliable logic behavior. In fact, as the current modulation

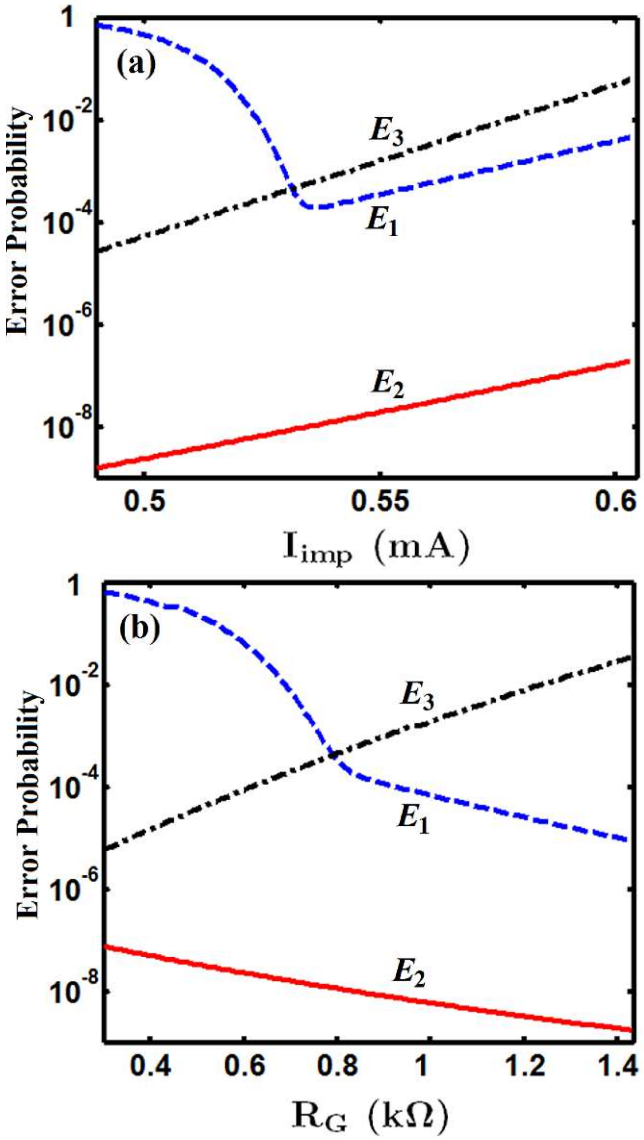

Figure 4.14.: Error probabilities (E_i) for different input states of the CC-IMP logic gate as function of (a) I_imp and (b) R_G.

between State 1 and State 3 depends on the TMR ratio, a higher TMR ratio allows for higher values of R_G (lower E_1 shown in Fig. 4.14b) when the circuit parameters are optimized. Fig. 4.15b shows an example of a two-dimensional circuit parameters optimization for the CC-IMP logic gate.

In order to compare the performance of the CC-IMP and VC-IMP gates, the circuit parameters are optimized and the error probabilities and the energy consumptions are calculated. According to Fig. 4.16, the optimal R_G of the implication gate based on the conventional topology (Fig. 4.12a) is higher by a factor of two to three as compared

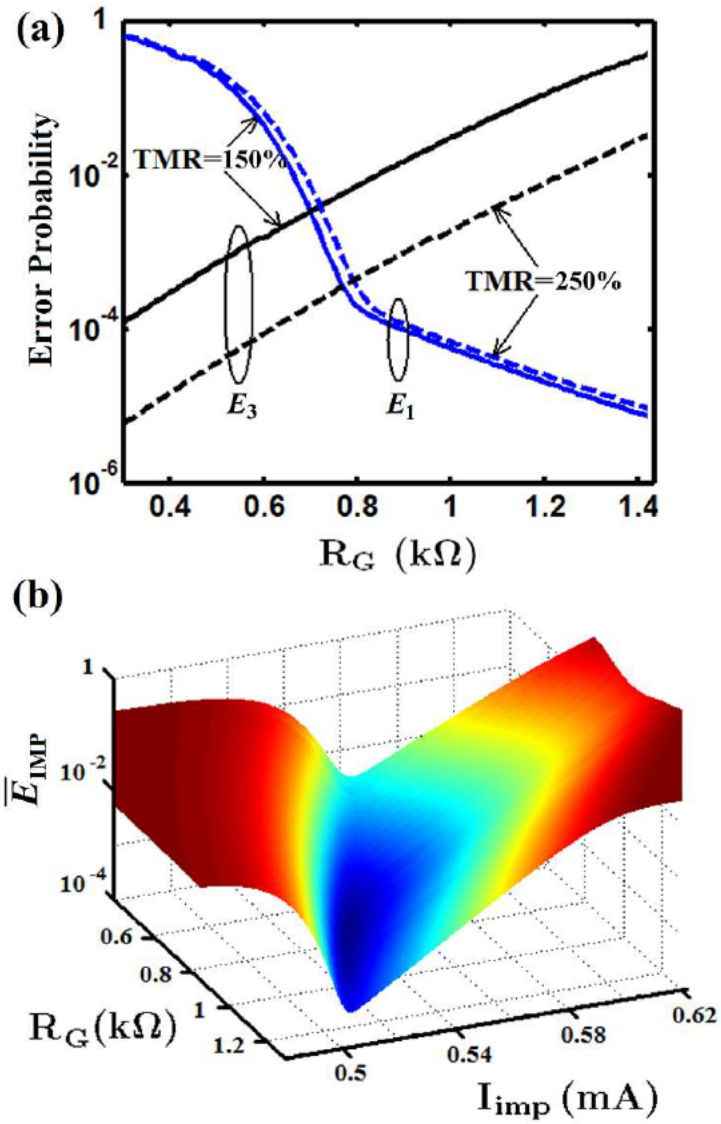

Figure 4.15.: (a) Dominant error probabilities (E_1 and E_3) for different TMR ratios. (b) Circuit parameters optimization in the CC-IMP gate with TMR ratio and optimum R_G and I_{imp} of 250%, 0.8 kΩ, and 0.5 mA, respectively.

to the proposed topology (Fig. 4.12b). Furthermore, in the conventional voltage-controlled gate topology the current flowing through R_G is equal to the sum of the switching current i_T and the modulation current i_S ($I_G = i_S + i_T$) while it is only equal to the switching current i_T in the novel current-controlled gate topology ($I_G = i_T$). Therefore, for a fixed current level and a given switching time, the implication energy consumption is about 60% lower in the novel implication gate topology than in the conventional topology. A comparison of the implication energy consumption in the two topologies is shown in Fig. 4.17a.

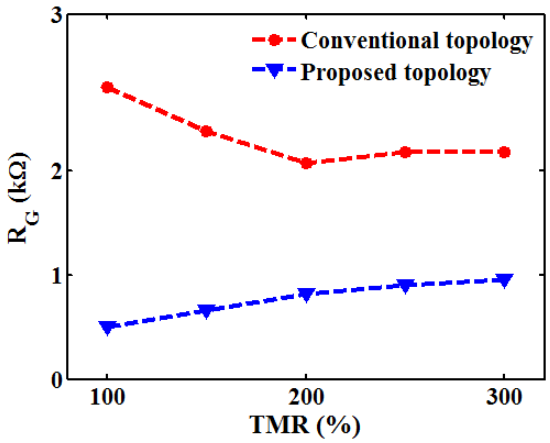

Figure 4.16.: Optimized R_G in the conventional (VC-IMP) and the proposed (CC-IMP) implication logic gates depending on the TMR ratio.

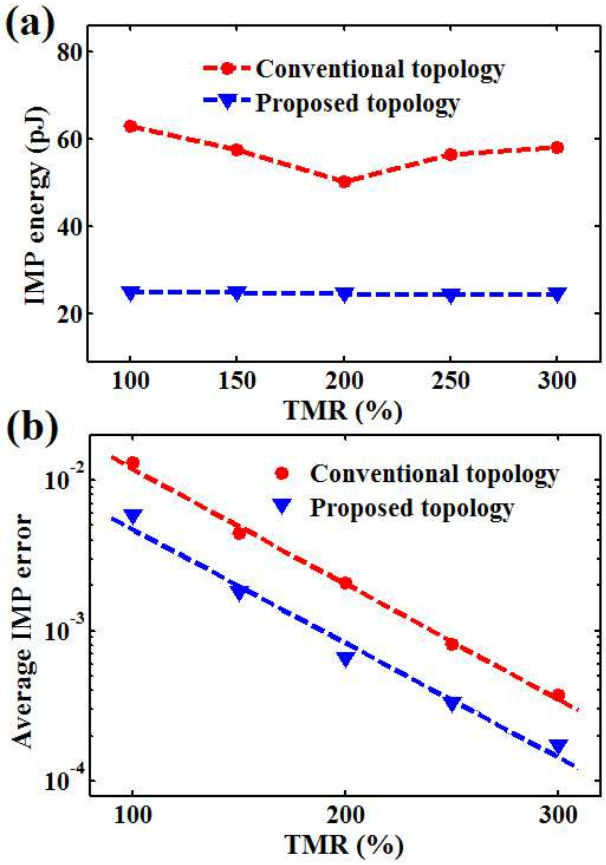

Figure 4.17.: (a) The IMP energy consumption and (b) the average error depending on the TMR ratio for both conventional and proposed topologies.

Robust implication logic behavior requires a high enough state dependent modulation in both topologies. This modulation on the target MTJ (T) which is caused by the difference between the high and low resistances of the source MTJ (S), is directly proportional to the TMR ratio of the MTJ. Therefore, from the device point of view, we expect that the error $\overline{E}_{\mathrm{IMP}}$ decreases with the increase of the TMR ratio which is a determinant device parameter for the logic reliability. Fig. 4.17b demonstrates that the error E_{imp} decreases exponentially with increasing TMR ratio. At a fixed TMR ratio the CC-IMP gate topology provides a higher modulation on T, thus reduces the average error probability by about 60% as compared to the conventional one. As the proposed CC-IMP gate enables a more energy-efficient and reliable implementation for implication logic framework, in the following we employ the CC-IMP gate for the performance comparison between the STT-MTJ-based implication logic gates and the state-of-the-art (reprogrammable) gates.

4.4. Reprogrammable Logic Using STT-MTJs

Recently, it has been demonstrated that by using direct communication between STT-MTJs, logic operations can be realized for which the MTJ devices are used simultaneously as memory and computing elements in intrinsic logic-in-memory architectures. In [55] and [56] experimental demonstrations of two-input and three-input reprogrammable logic gates (Fig. 4.18) are reported to realize the basic Boolean logic operations AND, OR, NAND, NOR, and the Majority operation. This section describes the operating principle and presents a reliability analysis of the reprogrammable gates.

The basic Boolean logic operations using reprogrammable gates are executed in two sequential steps. These steps comprise an appropriate preset operation (parallel or antiparallel state) in the output MTJ and then applying a voltage pulse (V_{A}) with a proper amplitude to the gate. Depending on the logic states of the input MTJs ($\mathrm{X_i}$), the preset in the output MTJ (Y), and the voltage level applied to the gate, a conditional switching behavior in the output MTJ is provided that corresponds to a particular logic operation [56].

Table 4.1 and Table 4.2 illustrate how the AND, OR, NAND, and NOR operations are performed employing the two-input reprogrammable gate in two steps. The variable x_{i} show the logic states of an input MTJ ($\mathrm{X_i}$) and y represents the logic state of the output MTJ (Y). In order to perform a logic operation, first a preset of $y = 1$ (setting Y in the high-resistance state (HRS) shown in Table 4.1) or $y = 0$ (setting Y in the low-resistance state (LRS) shown in Table 4.2) is performed in the output MTJ (Step 1). In Step 2 a proper voltage level ($V_{\mathrm{A}} < 0$ or $V_{\mathrm{A}} > 0$ with optimized amplitude explained in Section 4.3.2) is applied to the gate to enforce the desired (high-to-low or low-to-high) resistance switching event in the output MTJ to execute the logic operation AND/OR or NAND/NOR. Compared to the (N)AND operation,

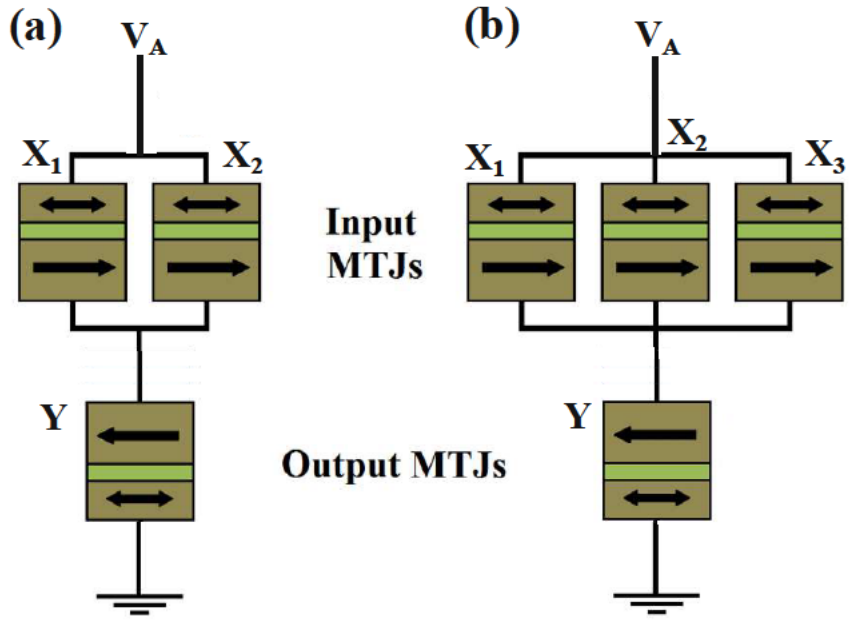

Figure 4.18.: STT-MTJ-based (a) two-input and (b) three-input reprogrammable logic gates. X_i (Y) shows an input (output) MTJ.

the (N)OR operation requires a lower voltage amplitude ($|V_A|$), as it must enforce a desired switching event only, if both input MTJs are in the low resistance state (State 1). For the (N)AND operation the switching events are enforced not only in State 1 but also when only one of the inputs is in the low resistance state (State 2 and State 3). These switching events in State 2 and State 3 are desired switching events for the (N)AND operation, while they are undesired events for the (N)OR operation.

Table 4.1.: Realized conditional switching behavior is equivalent to the AND and OR operations with a preset of $y = 1$ using the two-input reprogrammable gate. Desired switching events in the output (y') are indicated by boldface type.

Input Patterns			$y' \leftarrow x_1$ AND x_2		$y' \leftarrow x_1$ OR x_2	
			Step 1	Step 2	Step 1	Step 2
State	x_1	x_2	y	y'	y	y'
1	LRS (0)	LRS (0)	HRS (1)	**LRS (0)**	HRS (1)	**LRS (0)**
2	LRS (0)	HRS (1)	HRS (1)	**LRS (0)**	HRS (1)	HRS (1)
3	HRS (1)	LRS (0)	HRS (1)	**LRS (0)**	HRS (1)	HRS (1)
4	HRS (1)	HRS (1)	HRS (1)	HRS (1)	HRS (1)	HRS (1)

Table 4.2.: Realized conditional switching behavior is equivalent to the NAND and NOR operations with a preset of $y = 0$ using the two-input reprogrammable gate.

Input Patterns			$y' \leftarrow x_1$ NAND x_2		$y' \leftarrow x_1$ NOR x_2	
			Step 1	Step 2	Step 1	Step 2
State	x_1	x_2	y	y'	y	y'
1	LRS (0)	LRS (0)	LRS (0)	**HRS (1)**	LRS (0)	**HRS (1)**
2	LRS (0)	HRS (1)	LRS (0)	**HRS (1)**	LRS (0)	LRS (0)
3	HRS (1)	LRS (0)	LRS (0)	**HRS (1)**	LRS (0)	LRS (0)
4	HRS (1)	HRS (1)	LRS (0)	LRS (0)	LRS (0)	LRS (0)

Conditional switching corresponding to specific logic operations in reprogrammable logic gates (Fig. 4.18) are performed by applying a proper voltage V_A to the gates. For given MTJ device characteristics, the value of the circuit parameter V_A has to be optimized to ensure a reliable conditional switching behavior of the output MTJ for any possible input pattern. Indeed, for any logic operation performed by the reprogrammable gates, this optimization is required to maximize (minimize) the switching probability in the output MTJ ($P \rightarrow 1$ or $P \rightarrow 0$), when it is a desired (an undesired) switching event in Step 2 (Table 4.1 and Table 4.2). Therefore, for the reliability analysis, the error probability of a given input state (State i) is defined as $E_i = 1 - P_i$ ($E_i = P_i$) for a desired (undesired) switching event, where P_i is the switching probability of the output MTJ in State i. It should be noted that the input MTJs are left unchanged and thus their switching probabilities are negligible as the current flowing through the output MTJ splits between the inputs, and their currents are below the critical current required for the STT switching.

Similar to the implication gates (Eq. 4.21), by assuming equal incidence probabilities for all input patterns, we obtain the average error probability ($\overline{E}_b$) of a basic logic operation b implemented by the reprogrammable gate as

$$\overline{E}_b = \frac{1}{2^n} \sum_{i=1}^{2^n} E_i, \tag{4.22}$$

where n is the number of input MTJs. By using Table 4.1, Table 4.2, and Eq. 4.22,

$\overline{E}_{\mathrm{b}}$ is obtained for the two-input (N)OR and (N)AND operations as

$$\overline{E}_{\mathrm{OR}} = \overline{E}_{\mathrm{NOR}} = \frac{1}{4}\sum_{i=1}^{4} E_{\mathrm{i}} = \frac{1}{4}[(1-P_1)+P_2+P_3+P_4], \tag{4.23}$$

$$\overline{E}_{\mathrm{AND}} = \overline{E}_{\mathrm{NAND}} = \frac{1}{4}\sum_{i=1}^{4} E_{\mathrm{i}} = \frac{1}{4}[(1-P_1)+(1-P_2)+(1-P_3)+P_4], \tag{4.24}$$

where P_{i} is the switching probability of the output MTJ in State i.

It is important to note that for the AND and OR operations P_{i} represents the probability for antiparallel to parallel (AP–to–P) magnetization switching, while it is the probability for the P–to–AP switching in the case of NAND and NOR operations. In order to calculate P_{i} for different input patterns and various logic operations, we use Eq. 4.15 which express the MTJ's switching probability as a function of the applied current. For calculating the current flowing through each MTJ, the voltage-dependent effective TMR model (Eq. 4.18) is used coupled with Kirchhoff's laws applied to the two- and three-input reprogrammable gates (Fig. 4.18).

Fig. 4.19 shows the different values of P_{i} for the AND (left) and the NAND (right) logic operations based on the two-input reprogrammable gate as a function of V_{A}. MTJs are characterized as TMR = 200%, $\Delta = 40$, $I_{\mathrm{C0}}(\mathrm{AP} \rightarrow \mathrm{P}) = 325\ \mu\mathrm{A}$, and

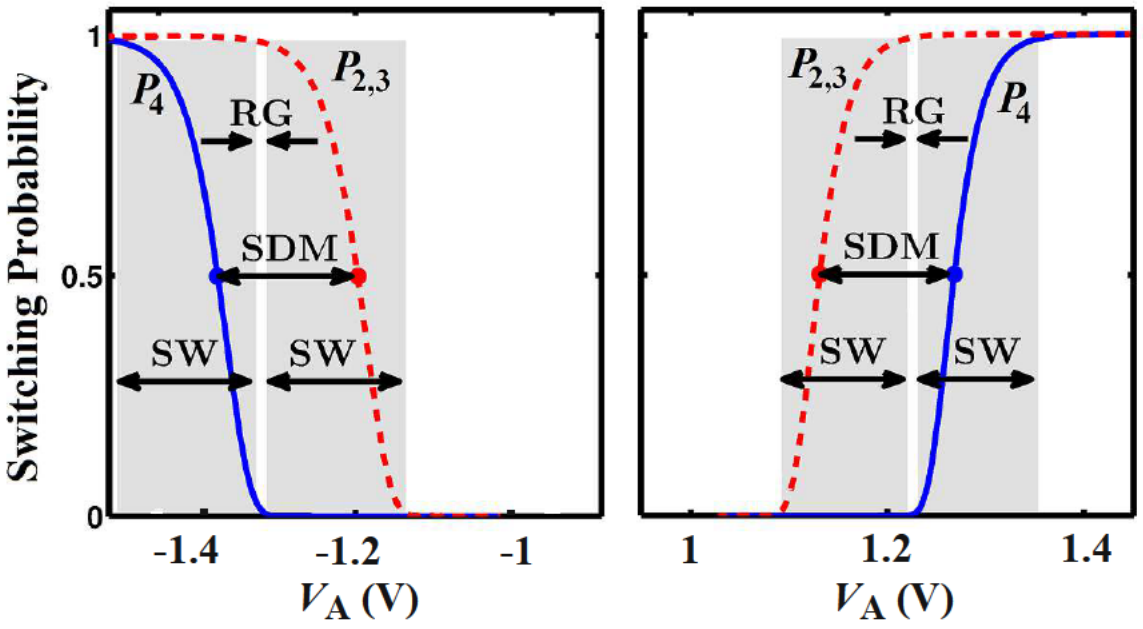

Figure 4.19.: Switching probabilities of the nearest desired ($P_{2,3}$) and undesired (P_4) switching events shown for the AND (left side) and NAND (right side) operations.

$R_P = 1.8$ kΩ. For a voltage level V_A chosen within the reliable gap (RG) opened between the switching windows (SWs) of the nearest desired ($P_{2,3}$) and undesired (P_4) switching events, the average error probability is minimized. Fig. 4.20 shows the average error probabilities ($\overline{E}_b$) for different logic operations for the two- and three-input reprogrammable gates as a function of V_A. It illustrates that for each operation there is an optimal V_A and for both two- and three-input gates the operations AND and NAND offer higher reliability as compared to the other logic operations.

In fact, as it is shown in Table 4.1 and Table 4.2, the operations AND and NAND exhibit undesired switching when the inputs (x_1 and x_2) are in high-resistance state (State 4), but a desired switching when one of the inputs is in the low-resistance state (State 2 or State 3); and the operations OR and NOR exhibit a desired switching when the inputs (x_1 and x_2) are in the low-resistance state (State 1) but undesired switching when one of the inputs is in the high-resistance state (State 2 or State 3). Eq.4.25 shows that the change in resistance at the input (R_{in}) is higher when there is a modulation between State 4 and State 2 (or State 3) rather than a modulation between State 1 and State 2 (or State 3) ($|R_{in}(4) - R_{in}(2,3)| > |R_{in}(2,3) - R_{in}(1)|$).

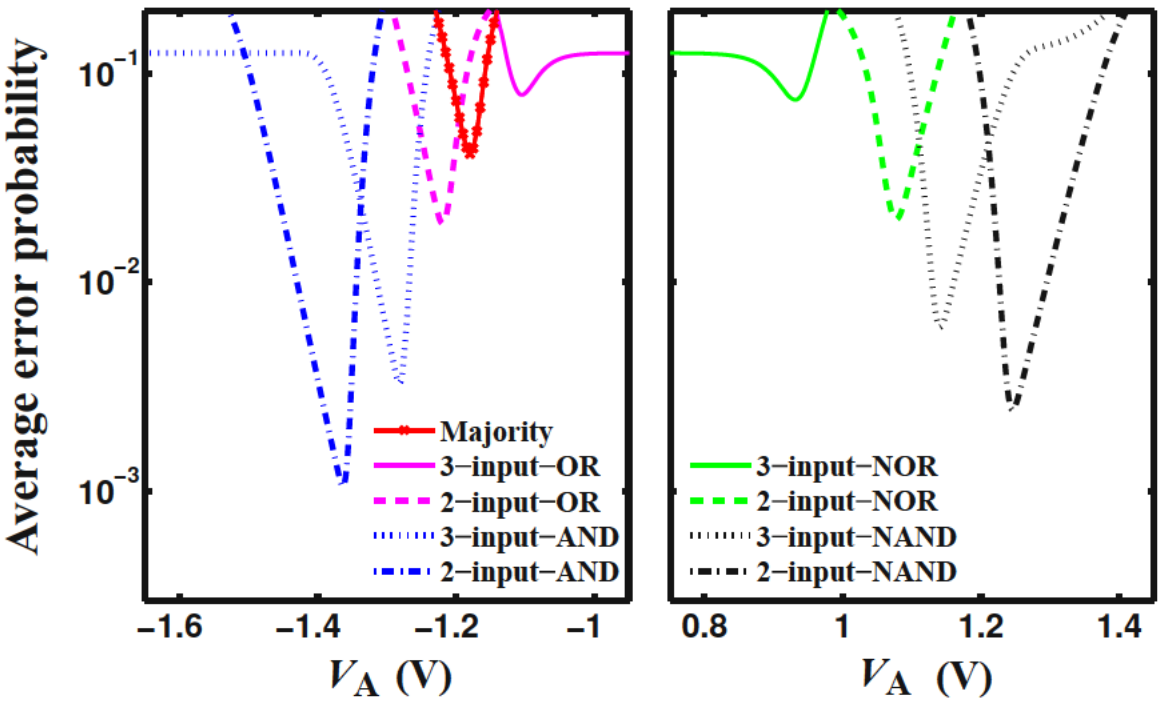

Figure 4.20.: Average error probabilities for the basic reprogrammable operations as a function of V_A.

$$
\begin{aligned}
|\Delta R_{\text{in}}(4,3)| - |\Delta R_{\text{in}}(3,1)| &= (R_{\text{in}}(4) - R_{\text{in}}(3)) - (R_{\text{in}}(3) - R_{\text{in}}(1)) \\
&= (R_{\text{in}}(4) - R_{\text{in}}(2)) - (R_{\text{in}}(2) - R_{\text{in}}(1)) \\
&= \left(\frac{R_{\text{AP}}}{2} - \frac{R_{\text{P}}\ R_{\text{AP}}}{R_{\text{P}} + R_{\text{AP}}}\right) - \left(\frac{R_{\text{P}}\ R_{\text{AP}}}{R_{\text{P}} + R_{\text{AP}}} - \frac{R_{\text{P}}}{2}\right) \\
&= \frac{(R_{\text{P}} - R_{\text{AP}})^2}{2(R_{\text{P}} + R_{\text{AP}})} > 0
\end{aligned} \tag{4.25}
$$

It is clear that a higher resistance modulation in the input MTJs provides a higher current modulation in the output MTJ of a reprogrammable logic gate (Fig. 4.18). As a result, according to Eq.4.25, the current flowing through the output MTJ has a higher modulation, when State 2 (or State 3) is compared to State 4 rather than to State 1.

$$
\begin{aligned}
|R_{\text{in}}(4) - R_{\text{in}}(2,3)| > &|R_{\text{in}}(2,3) - R_{\text{in}}(1)| \\
\Rightarrow &|I_{\text{out}}(4) - I_{\text{out}}(2,3)| > |I_{\text{out}}(2,3) - I_{\text{out}}(1)|
\end{aligned} \tag{4.26}
$$

Therefore, the modulation between the nearest desired ($P_{2,3}$) and undesired (P_4) switching events for the (N)AND operation is higher than that of between the nearest desired (P_1) and undesired ($P_{2,3}$) events for the (N)OR operation. Thus, the (N)AND operation provide a more reliable behavior (Fig. 4.20).

The logic implementation using MTJ-based logic gates relies on a state dependent current modulations on the output (target) MTJs. These modulations are caused by the changes in the MTJs' resistances for different initial logic states. According to Eq. 4.18, the resistance modulation between the high and low resistance states in the MTJ with antiparallel and parallel magnetization alignments is proportional to the TMR ratio of the MTJs. Therefore, from a device point of view, the average error probabilities of all MTJ-based operations are expected to decrease with increasing TMR ratio. In fact, as we will see later, the TMR ratio is considered as a very important device parameter for the reliability of all STT-MTJ-based logic gates. The width of the reliable gap between the switching probabilities in the reprogrammable gate (P_{i} in Fig. 4.19) is enlarged for a higher TMR ratio as the difference between the different input states originates from the modulation between the HRS and the LRS of the MTJs (Table 4.1 and Table 4.2). It is also clear that a resistance modulation (the difference between the HRS and the LRS states) of one input MTJ causes a higher current modulation in the output MTJ, when it is only connected (in parallel) to one other input MTJ rather than two input MTJs. Therefore, compared to the three-input reprogrammable gate, the two-input reprogrammable gate provides a higher current modulation in its output MTJ and thus exhibits a more reliable logic behavior (see P_{i} for different operations in Fig. 4.20). Accordingly, in the following we employ only the two-input gate for the performance analysis and comparison between the reprogrammable and the implication logic architectures.

4.5. Comparison of Improved Implication and Reprogrammable Gates

Fig. 4.21 compares the average error probabilities ($\overline{E}$) of different logic operations using the CC-IMP gate ((N)IMP operation) and a two-input reprogrammable logic gate (AND, OR, NAND, and NOR operations) as a function of TMR ratio with optimized circuit parameters (I_{imp}, R_{G}, and V_{A}) at each point. The MTJ device parameters are given as $R_{\text{P}} = 1.8\ \text{k}\Omega$, $\Delta = 40$, $I_{\text{C0}}(AP \rightarrow P) = 325\ \mu A$, and $I_{\text{C0}}(P \rightarrow AP) = 425\ \mu A$. It illustrates that the error decreases exponentially with increasing TMR ratio and for the same device characteristics, the implication gate exhibits a more reliable logic behavior as compared to the reprogrammable gate. It has to be mentioned that these results are obtained in the MTJ thermally-activated switching regime ($t = 50$ ns), which is rather slow for logic applications. However, as the MTJ-based logic mainly relies on a current modulation required for STT switching, the superior reliability of the implication gate is independent of the switching regime as it is demonstrated below in Fig. 4.22.

Fig. 4.22 compares the maximum current modulations $(I_{\text{d}} - I_{\text{u}})/I_{\text{d}}$ for each MTJ-based operation as a function of the TMR ratio. I_{d} is the minimum current required for a desired resistance switching and I_{u} is the maximum current which can enforce an undesired resistance switching. For example, in the implication gate I_{d} (I_{u}) is the

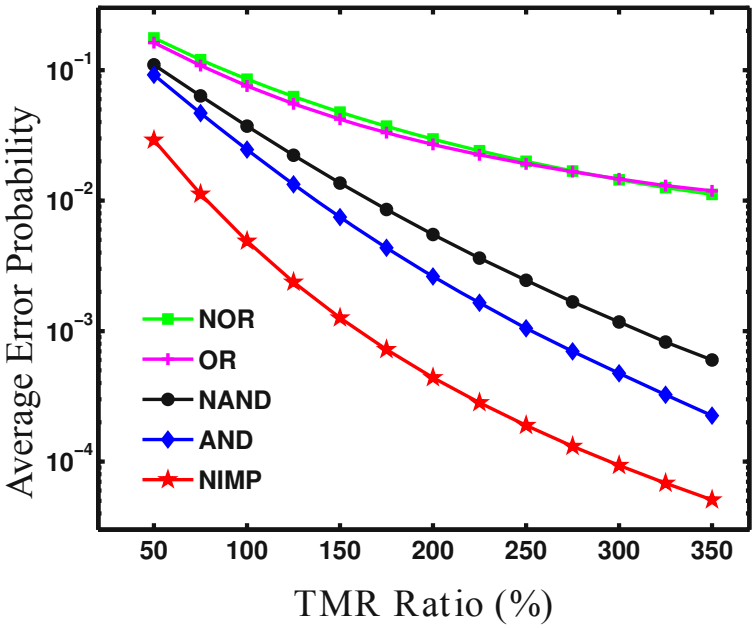

Figure 4.21.: Average error probabilities for the implication and two-input reprogrammable logic gates as a function of the TMR ratio.

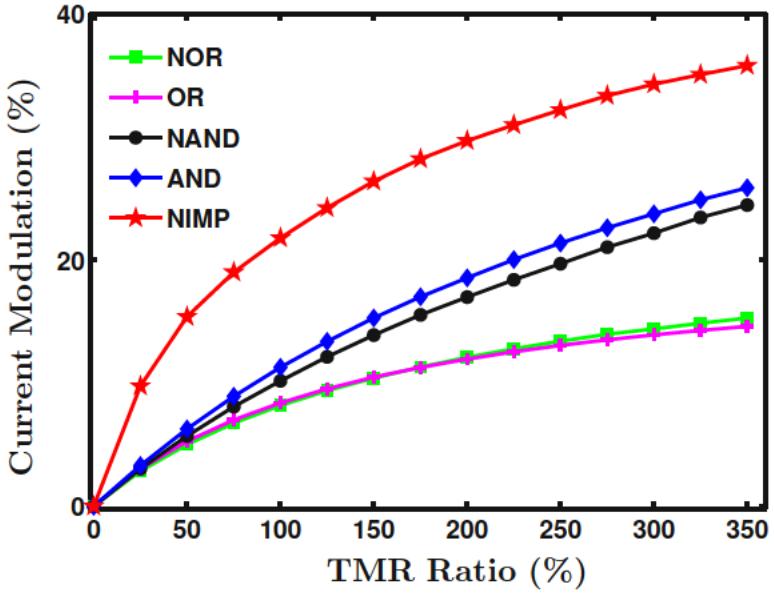

Figure 4.22.: Maximum current modulation $(I_d - I_u)/I_d$ in implication and two-input reprogrammable logic gates as a function of the TMR ratio.

current flowing through T (S) in State 1. For the reprogrammable-based AND operation I_d (I_u) is the current flowing through the output MTJ in State 4 (State 2 and State 3). As shown in Fig. 4.22, the implication gate allows higher current modulations compared to the highest modulation by the reprogrammable-based AND operation. Therefore, it opens a wider gap between desired and undesired switching events and thus inherently enables a more reliable logic behavior. In fact, with the implication logic gate, R_G provides one more degree of freedom for the circuit parameters' optimization. Therefore, the basic logic operation by the implication logic gate exhibits five times more reliable behavior as compared to the most reliable operation (AND) implemented by the reprogrammable gate (Fig. 4.21). The record TMR ratio of 604% [183] makes the MgO-based MTJ a major candidate for STT-operated magnetoresistive random-access memories (STT-MRAMs) and promises highly reliable MTJ-based logic architectures.

In order to preform a fair comparison, we assume the same MTJ device characteristics for both logic gates and determine the minimum possible error probabilities (corresponding to optimized circuit parameters as shown in Fig. 4.15b and Fig. 4.20) for implementing the same binary Boolean functions using the implication and the reprogrammable logic gates. For implication-based logic, appropriate sequential steps of NIMP and TRUE operations must be executed to perform a specific logic function as designed before. With the reprogrammable gate, a network of basic logic operations including AND, OR, NAND, and NOR has to be constructed. Each basic operation includes a preset (TRUE or FALSE) and a conditional switching event (Table 4.1

and Table 4.2)). We define the average error probability of a complex Boolean logic function (f) implemented by using a sequence of the basic logic operations as

$$\overline{E}_{\mathrm{f}} = 1 - R(f) = 1 - \prod_{i=1}^{n_{\mathrm{f}}} [1 - \overline{E}_{\mathrm{b}}(i)], \tag{4.27}$$

where $R(f)$ is the reliability of f, n_{f} indicates the total number of required basic logic operations for implementing f, and $\overline{E}_{\mathrm{b}}(i)$ corresponds to the average error probability of the $i-$th basic logic operation. Since by applying high enough voltage/current highly reliable TRUE and FALSE operations can be executed, we suppose that the error probability of a TRUE or FALSE operation is negligible compared to the error probabilities of conditional switching events in both implication and reprogrammable gates. Therefore, n_{f} is equal to the total number of the conditional switching events required for performing f based on either implication or reprogrammable gates.

As an example, performing an implication-based NOR operation requires three sequential steps including one TRUE and two NIMP operations as shown in Eq. 3.2. Therefore, for TMR = 250% (Fig. 4.21), $n_{\mathrm{f}} = 2$ and

$$\overline{E}_{\mathrm{NOR}} = 1 - [1 - \overline{E}_{\mathrm{NIMP}}]^2 \simeq 2 \times \overline{E}_{\mathrm{NIMP}} \simeq 5.6 \times 10^{-4}. \tag{4.28}$$

With the reprogrammable gate, one can directly perform NOR in two steps including one FALSE and one conditional switching as shown in Table 4.2), for which $n_{\mathrm{f}} = 1$ and

$$\overline{E}_{\mathrm{NOR}} = 1 - [1 - \overline{E}_{\mathrm{NOR}}]^1 \simeq 2.4 \times 10^{-2} \tag{4.29}$$

Table 4.3.: Average error probabilities for 7 distinct binary Boolean functions based on the implication and reprogrammable logic architectures for TMR = 250%.

	Reprogrammable	Reprogrammable*	Implication
AND	$\simeq 1.6 \times 10^{-3}$	$\simeq 1.6 \times 10^{-3}$	$\simeq 5.6 \times 10^{-4}$
OR	$\simeq 2.2 \times 10^{-2}$	$\simeq 1.1 \times 10^{-2}$	$\simeq 8.4 \times 10^{-4}$
NAND	$\simeq 3.6 \times 10^{-3}$	$\simeq 3.6 \times 10^{-3}$	$\simeq 8.4 \times 10^{-4}$
NOR	$\simeq 2.4 \times 10^{-2}$	$\simeq 8.8 \times 10^{-3}$	$\simeq 5.6 \times 10^{-4}$
NOT	$\simeq 3.6 \times 10^{-3}$	$\simeq 3.6 \times 10^{-3}$	$\simeq 2.8 \times 10^{-4}$
IMP	$\simeq 2.6 \times 10^{-2}$	$\simeq 8.8 \times 10^{-3}$	$\simeq 5.6 \times 10^{-4}$
NIMP	$\simeq 5.2 \times 10^{-3}$	$\simeq 5.2 \times 10^{-3}$	$\simeq 2.8 \times 10^{-4}$

A more efficient way to reduce the error probability with the reprogrammable gate is designing and performing the logic function f only based on the more reliable AND and NAND operations (Fig. 4.20 and Fig. 4.21). Therefore, a reprogrammable-based NOR operation can be indirectly executed as a combination of two NAND and one AND operations (in a sequential manner) for which $n_f = 3$ and

$$\overline{E}_{\mathrm{NOR}} = 1 - [1 - \overline{E}_{\mathrm{AND}}][1 - \overline{E}_{\mathrm{NAND}}]^2 \simeq 8.8 \times 10^{-3}. \tag{4.30}$$

This kind of design (shown as reprogrammable* in Table 4.3) exhibits a more reliable behavior as compared to the direct realization of the reprogrammable-based NOR operation. However, its error is still about one order of magnitude higher than the implication-based implementation. This shows that the implication logic has a great potential to form a highly reliable MTJ-based logic framework.

Table 4.3 shows the average error probability ($\overline{E}_f$) of different Boolean functions for implication and reprogrammable logic gates based on Eq. 4.27 and the error values shown in Fig. 4.21 for TMR=250%. Reprogrammable* shows the results for the designs with minimized error probabilities based on AND and NAND operations. For the sake of completeness, performing the NOT operation requires one TRUE and one NIMP (NAND) operation using the implication (reprogrammable [56]) logic architecture.

$$\begin{aligned} &\mathrm{TRUE} : t = 1 \\ &\mathrm{NIMP} : \overline{t \rightarrow s} \equiv \{t' = t.\overline{s} \equiv \mathrm{NOT}\ s\} \end{aligned} \tag{4.31}$$

$$\begin{aligned} &\mathrm{TRUE} : a_2 = 1 \\ &\mathrm{Preset} : b_1 = 0 \\ &\mathrm{NAND} : b_1 \leftarrow \overline{a_1.a_2} \equiv \mathrm{NOT}\ a_1 \end{aligned} \tag{4.32}$$

4.6. Effect of the MTJ Device Parameters on Reliability

As mentioned before, the TMR ratio is considered as a very important device parameter for the reliability of the conditional switching in MTJ-based logic gates. However, other MTJ device parameters also affect the reliability. Fig. 4.23 shows the switching probabilities of the MTJ device in the thermally-activated switching regime (Eq. 4.15) as a function the MTJ current for different values of the thermal stability factor Δ. It illustrates that a higher Δ provides sharper switching dynamics (switching windows shown in Fig. 4.19 and Fig. 4.13). As decreasing the SWs increases the width of the reliable gaps opened between the SWs of the desired and undesired switching events, we expect a more reliable logic behavior for a higher Δ. In fact, according to Eq. 4.15, the dominant term for the switching probability calculation is $\exp[-\Delta(1 - I/I_{C0})]$.

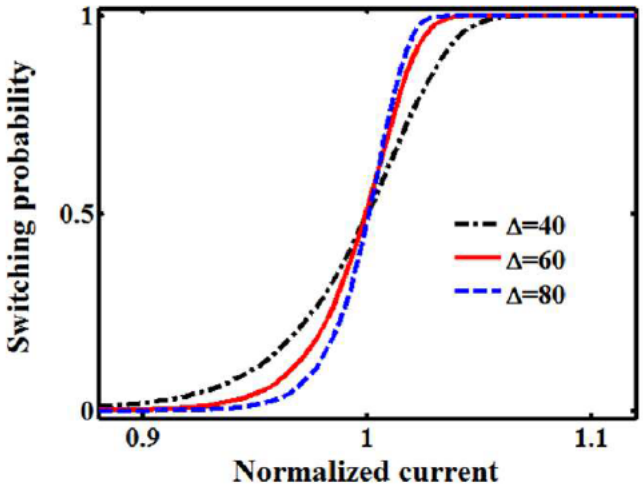

Figure 4.23.: Switching dynamics of the MTJ device as function of the applied current plotted for different values of Δ.

The modulation of the term I/I_{C0} depends on the TMR ratio and its impact has been studied before. Nevertheless, a higher Δ magnifies the effect of this modulation. Therefore, for all MTJ-based logic operations, a higher Δ decreases the error probabilities. Indeed, Fig. 4.24 shows the average error probabilities of the basic operations of the CC-IMP and the two-input reprogrammable gates as a function of the thermal

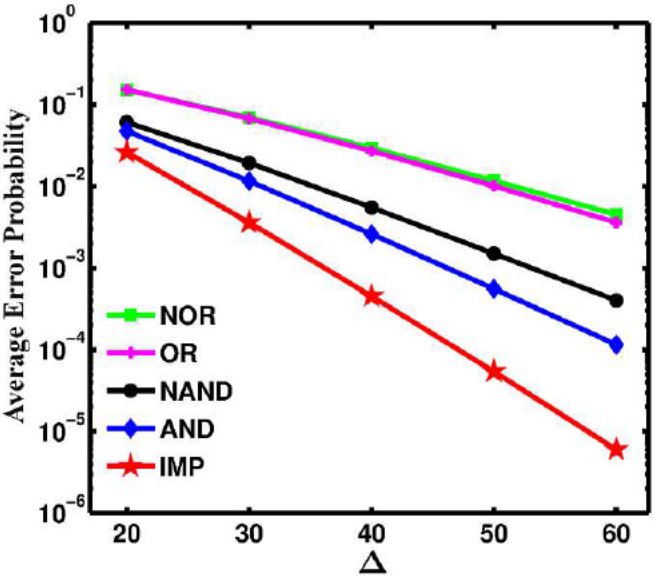

Figure 4.24.: Average error probabilities for the basic operations of the two-input reprogrammable gate (AND, OR, NAND, and NOR) and the proposed CC-IMP gate (IMP) as a function of Δ for TMR = 200%.

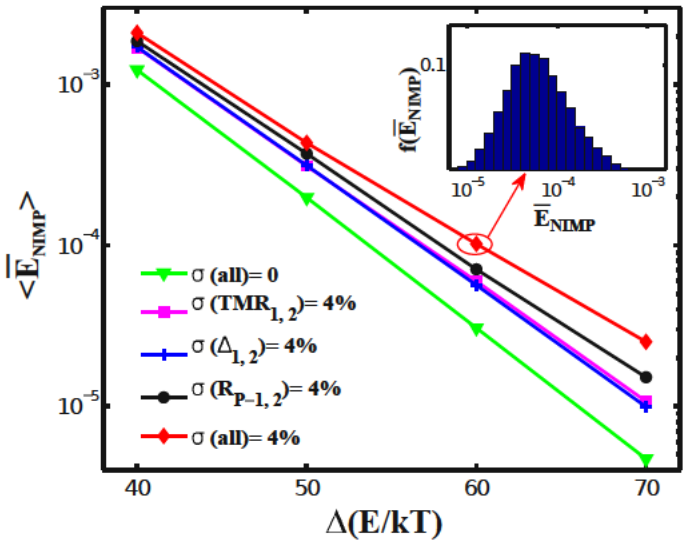

Figure 4.25.: Expectation values of the NIMP error probability ($< \overline{E}_{\mathrm{NIMP}} >$) as a function of Δ.

stability factor Δ. It illustrates that the error decreases exponentially with Δ and for the same device characteristics and TMR = 200%, the CC-IMP gate exhibits always a more reliable logic behavior as compared to the two-input reprogrammable gate. At each point the circuit parameters (I_{imp} and R_{G} in Fig. 4.15b and V_{A} in Fig. 4.20) are optimized to minimize the error probability. As it is shown in [38], although a lower Δ value allows easier STT switching, a minimum value of $\Delta = E/k_{\mathrm{B}}T = 40$ is required for low write and read error rates in STT-MRAM technology. A similar trade-off is encountered in the design of the MTJ-based logic gates. According to Eq. 4.15, the error values are independent of the absolute values of I_{C0} and R_{P}, as the computations can be generalized by normalizing all current and resistance values to I_{C0} and R_{P}, respectively. Furthermore, the effect of the pulse durations (τ) is negligible as compared to the internal exponential term in Eq. 4.15.

In order to investigate the effect of the MTJ device-to-device variations, Fig. 4.25 shows the expectation value for the NIMP error probabilities ($< \overline{E}_{\mathrm{NIMP}} >$) as a function of Δ under MTJ device variations with Gaussian distribution [192]. The spread of the variations ($\sigma\% = \sigma/\mu$) is assumed to be 4% in Δ, TMR ratio and R_{P} [192] for both target and source MTJs ($\sigma_{1,2}$). The mean values (μ) for TMR ratio and R_{P} are equal to 250% and $R_{\mathrm{P}} = 1.8$ kΩ, respectively. For each point, circuit parameters are fixed to the values which minimize the error and the average error probability for all combinations of input states ($\overline{E}_{\mathrm{NIMP}}$) with 10000 random variations is calculated. Then the expectation error values are obtained by $\sum f(\overline{E}_{\mathrm{NIMP}})\overline{E}_{\mathrm{NIMP}}$, where $f(\overline{E}_{\mathrm{NIMP}})$ is the distribution function of the errors (shown inset in Fig. 4.25). As it is expected, MTJ device variations increase the error probabilities as shown in Fig. 4.25.

4.7. Summary

The realization of the spintronic stateful logic operations is demonstrated. In contrast to the TiO_2-based devices, spintronic devices exhibit almost unlimited endurance which is an essential demand for logic computation. STT-MTJ is proposed as a very favorable device for stateful logic as it inherently eliminates the (state drift) error accumulation which is an important shortcoming in the TiO_2 and domain wall based devices.

A novel (current-controlled) STT-MTJ-based logic gate is proposed. It significantly improves the performance of the implication logic as compared to the conventional (voltage-controlled) gate topology. A reliability modeling and analysis is presented for optimizing and comparing STT-MTJ-based logic gates. It is shown that the proposed implication logic gate allows to implement Boolean logic functions based on an up to now ignored propositional logic operation of material implication and significantly improves the reliability of the MTJ-based logic compared to similar circuits available from literature based on reprogrammable architectures which realize conventional Boolean logic operations including AND, OR, NAND, and NOR operations.

5. Stateful STT-MRAM Arrays for Large-Scale Logic Circuits

5.1. Overview

In Chapter 4 it has been described how the direct communication between STT-MTJs via implication and reprogrammable circuit topologies realizes stateful logic operations. This intrinsically enables logic-in-memory architectures and extends the functionality of non-volatile memory circuits to incorporate logic computations. Nevertheless, in order to generalize the MTJ-based logic gates to large-scale logic circuits for performing more complex logic functions, there are some issues which need to be addressed. For example, it is necessary to use the logic result of one implication or reprogrammable gate as the input for the next logic stage (non-volatile logic fan-out). However, as shown in Fig. 4.12 and Fig. 4.18, the input and the output MTJs are physically connected to each other and any additional connection to other MTJs will disturb the conditional switching behavior of the output (target) MTJ. This highly localizes the logic computations and limits the possibility of performing logic operations between different inputs located in arbitrary parts of the logic circuits. Therefore, intermediate circuitry is required to perform extra read/write operations to readout the data stored in the output (target) MTJ and to write it to an input (source) MTJ, which increases complexity, energy consumption, and delay.

In the current-controlled implication circuit topology (Fig. 4.12b), the target MTJ cannot be used as a source MTJ for the next logic stage due to a structural asymmetry caused by the resistor R_G. In the reprogrammable circuit topologies (Fig. 4.18), the output MTJ cannot be used as an input MTJ as its parallel connection to other MTJs limits the possibility to perform the conditional switching required for MTJ-based logic. Furthermore, in order to cover all logic input patterns, independent access to initialize all input MTJs is necessary. Therefore, magnetic-field-based switching is used for the input MTJs [56]. This requires extra wiring for generating a current-induced Oersted field and thus in contrast to STT-switching is prohibitive from both scalability and energy consumption points of view [22].

Due to the easy integration of MTJs on top of a CMOS circuit into a one-transistor/one-MTJ (1T/1MTJ) cell, hybrid CMOS/MTJ technology is promising to address the above mentioned issues for extending the MTJ logic gates to large-scale non-volatile

circuits. Since the 1T/1MTJ cell is the basic memory cell in the STT-MRAM structure [39, 50], a STT-MRAM array can be used as a magnetic logic circuit for the development of innovative non-volatile large-scale logic architectures. STT-MRAM combines the speed of static RAM (SRAM), the density of dynamic RAM (DRAM), the non-volatility of flash memory, and has all the characteristics of a universal memory [39]. In this chapter, it is shown how the MTJ reprogrammable and implication stateful logic gates can be generalized to large-scale logic systems based on the STT-MRAM arrays. This enables the extension of non-volatile MRAM from memory to logic computing applications and eliminates the need for sensing amplifiers and intermediate circuitry [169] as compared to the MTJ logic presented before as well as other hybrid CMOS/MTJ non-volatile logic proposals [193].

In the common STT-MRAM architecture (Fig. 5.1), the 1T/1MTJ cell contains one MTJ to store the binary data and an access transistor to control the current flowing through the MTJ [50]. The cells are coupled in parallel between the current-carrying source lines (SLs) and bit lines (BLs) as shown in Fig. 5.1. The gate terminals of the access transistors are coupled to the word lines (WLs) in order to apply proper voltage signals to a specific MTJ for read/write operations (memory mode) through the SL and the BL in the MRAM array. For the read operation, a select voltage and a read current are applied to the specific WL and BL. The reading current flows through the selected MTJ, and by sensing the generated voltage difference between the SL and the BL, the resistance (logic) state of the selected MTJ is sensed. The read current must be low enough to prevent an undesired switching, which is referred to as a read disturbance. During a write operation, a select voltage and a write current (voltage) are applied to the specific WL and BL. According to the polarity of the current (voltage) applied to the current-carrying lines (SL and BL), the AP–to–P or P–to–AP switching is enforced in the selected MTJ depending on the desired binary states (logical '0' or '1'). In the following it is shown how STT-MRAM arrays can be combined to realize MTJ logic gates without the need for intermediate circuitry and independent CMOS logic units.

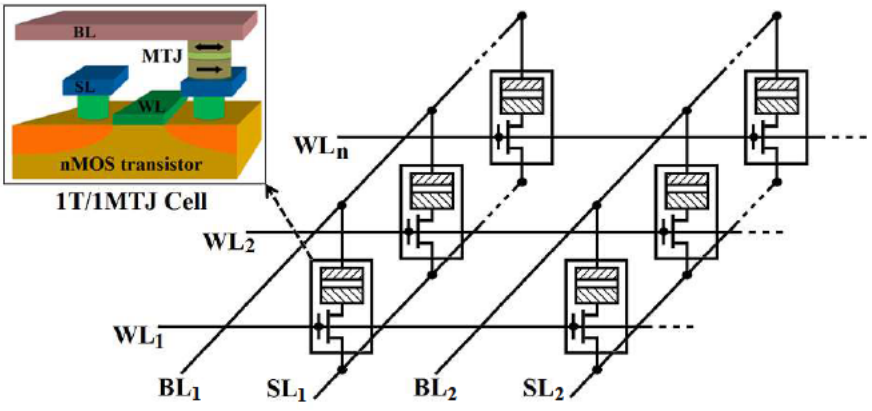

Figure 5.1.: Common STT-MRAM architecture based on the 1T/1MTJ structure.

5.2. Implementation of the Reprogrammable Architecture

Fig. 5.2 shows two STT-MRAM arrays which are connected in series. In the logic mode, the access transistors of the 1T/1MTJ cells are used to select simultaneously two STT-MTJs (inputs) in one array and one STT-MTJ (output) in the other array. Due to the serial connection of the arrays, the current flowing through the output MTJ has a reverse polarity direction compared to the input MTJs. This means that, for example, if the current flowing through the output MTJ tends to enforce an AP–to–P switching, the current flowing through the input MTJs is in the P–to–AP switching direction. Therefore, the three simultaneously selected MTJs (two inputs and one output) form the circuit topology required for the two-input reprogrammable gate shown in Fig. 4.18a. By applying the voltage difference V_A to the BLs of the arrays, the desired switching (Step 2 in Table 4.1 and Table 4.2) is enforced in the output MTJ.

Depending on the specified basic logic operation (AND, OR, NAND, or NOR), V_A has to be optimized as shown in Fig. 4.20. A corresponding preset (Step 1) is performed in the output MTJ beforehand, by selecting the desired access transistor and applying the write current/voltage signal to the BL and SL of the output array, like in the common write operations in the memory mode. Compared to the MTJ-based reprogrammable circuits (Fig. 4.18a and Fig. 4.18b), which require extra wiring for generating a current-induced Oersted field for independent access to the input MTJs [56], the STT-MRAM-based implementation enables independent STT writing of the input MTJs by using the access transistors. This brings significant advantages related to scalability and energy consumption. However, the non-zero ON resistance of the access transistors decreases the effective TMR ratio of the 1T/1MTJ cells by about 10% [192]. According to Fig. 4.21, this increases the average error probabilities by a factor of < 2. Therefore,

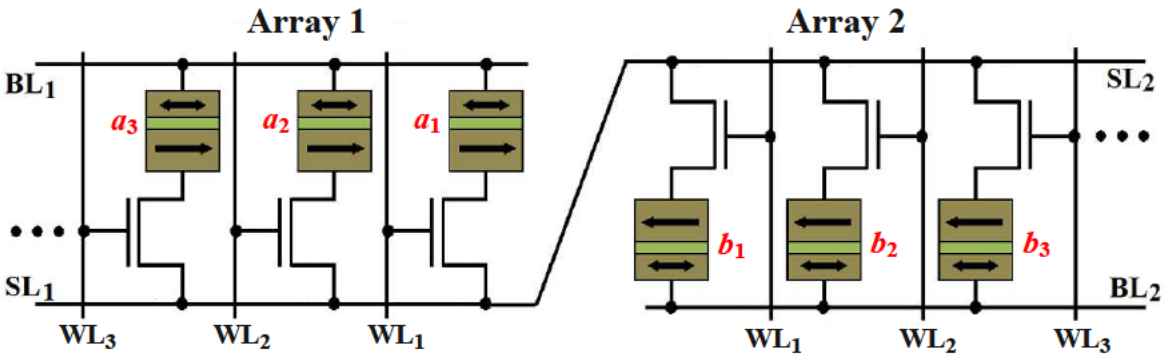

Figure 5.2.: Proposed STT-MRAM-based reprogrammable logic architecture including two common STT-MRAM arrays connected in series.

MTJs with higher TMR ratio are required to compensate the reliability decrease.

The effect of the channel resistances of the access transistors (R_{on}) can be taken into account by using the following equations [194]:

$$R_{on} = \frac{V_{DS}}{\mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]} \quad : V_{DS} \leq V_{GS} - V_{TH}, \tag{5.1a}$$

$$R_{on} = \frac{V_{DS}}{\mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})} \quad : V_{DS} > V_{GS} - V_{TH}. \tag{5.1b}$$

V_{GS} (V_{DS}) is the voltage difference between the gate (drain) and the source of the access transistor, μ_n denotes the mobility of electrons, C_{ox} indicates the gate oxide capacitance per unit area, W (L) represents the channel width (length), and λ is the channel-length modulation coefficient in saturation ($V_{DS} > V_{GS} - V_{TH}$).

For the STT-MRAM-based reprogrammable implementation of more complex Boolean logic functions, a sequence of basic logic operations including AND, OR, NAND, and NOR has to be constructed. As an example, we consider the implementation of the exclusive OR (XOR) function which is a fundamental logic function in arithmetic circuits. The output of the XOR function (a_1 XOR $a_2 \equiv a_1 \oplus a_2$) is logic '1', if ONLY one of the inputs is '1' and can be expressed as '$a_1.\overline{a_2}+\overline{a_1}.a_2$' or '$(a_1+a_2).(\overline{a_1.a_2})$'. It can be shown that the design based on the last expression requires a minimum of sequential steps (6 steps) for implementation using the STT-MRAM arrays as follows:

$$\begin{aligned}
\text{Preset} &: b_1 = 1 \\
\text{OR} &: b_1 = a_1 + a_2 \\
\text{Preset} &: b_2 = 0 \\
\text{NAND} &: b_2 = \overline{a_1.a_2} \\
\text{Preset} &: a_3 = 1 \\
\text{AND} &: a_3 = b_1.b_2 \equiv a_1 \oplus a_2 \equiv a_1 \text{ XOR } a_2.
\end{aligned} \tag{5.2}$$

a_i and b_i are the logic variables equivalent to the resistance states of the MTJs in the Array 1 and Array 2, respectively (Fig. 5.2). a_1 and a_2 are the input variables stored in two MTJs in the Array 1 and the final result (a_3) is written in an MTJ in Array 1. There are two intermediate basic operations on a_1 and a_2 (OR and NAND), the respective results (b_1 and b_2) are stored in two arbitrary MTJs in Array 2 for performing the final basic operation (AND). b_1 and b_2 are the inputs of the final operation and Array 2 (Array 1) acts as the input (output) array.

As the output of one operation can be used as the input data for the next logic stage, complex Boolean logic functions are designed by executing a well defined set of subsequent basic operations. Furthermore, the MTJs can be selected arbitrarily (two

in the input array and one in the output array). The computation framework in the STT-MRAM architecture is flexible and not localized like in the MTJ circuits shown in Fig. 4.18 and Fig. 4.12. MRAM-based logic not only extends the functionality of the STT-MRAM architecture to perform non-volatile logic, but also eliminates the need for data transfer between separated memory and logic units which allows to shift away from the Von Neumann architecture and to shorten the interconnection delay.

By assuming the optimized V_{A} for each basic operation, we use the minimum $\overline{E}_{\mathrm{b}}(i)$ values (Fig. 4.20) for calculating $\overline{E}_{\mathrm{f}}$. For example, by using Eq. 4.27 and Fig. 4.21 for TMR = 300%, the average error probability of the XOR function described in Eq. 5.2 is obtained as

$$\overline{E}_{\mathrm{XOR}} = 1 - (1 - \overline{E}_{\mathrm{OR}})(1 - \overline{E}_{\mathrm{NAND}})(1 - \overline{E}_{\mathrm{AND}}) \simeq 2 \times 10^{-2}. \tag{5.3}$$

For the sake of higher reliability, one can design a complex logic function based solely on the AND and NAND operations, as these are more reliable compared to the OR and NOR operation in the reprogrammable implementation. However, the reliability-based design increases the number of required basic logic operations for implementation and thus, increases the computation time and the energy consumption. For example, the reliability-based design of the XOR function requires the following steps in the reprogrammable MRAM-based logic architecture:

$$\begin{aligned}
&\text{Preset} : b_1 = 1 \\
&\text{AND} : b_1 = a_1.a_2 \\
&\text{Preset} : a_3 = 0 \\
&\text{Preset} : b_2 = 1 \\
&\text{NAND} : a_3 = \overline{b_1.b_2} = \overline{b_1} = \overline{a_1.a_2} \\
&\text{Preset} : b_1 = 0 \\
&\text{NAND} : b_1 = \overline{a_1.a_3} = \overline{a_1.\overline{b_1}} = \overline{a_1.\overline{a_1.a_2}} \\
&\text{Preset} : b_2 = 0 \\
&\text{NAND} : b_2 = \overline{a_2.a_3} = \overline{a_2.\overline{a_1.a_2}} \\
&\text{Preset} : a_3 = 0 \\
&\text{NAND} : a_3 = \overline{b_1.b_2} = (a_1 + a_2).(\overline{a_1.a_2}) \equiv a_1 \oplus a_2
\end{aligned} \tag{5.4}$$

The average error probability of the XOR operation for this design is about $\simeq 5 \times 10^{-3}$, which is four times smaller than that of the design with minimized steps. However, the number of sequential steps and therefore, the computation time and the energy consumption are approximately doubled.

5.3. Implementation of the Improved Implication Architecture

5.3.1. Structural Asymmetry

By replacing the MTJ devices with 1T/1MTJ cells, the implication logic gates are realized in MRAM arrays to provide large-scale non-volatile magnetic circuits (Fig. 5.3). Due to the structural asymmetry caused by R_G, two MRAM arrays are required in this asymmetric implementation. For performing the implication operation, a source (target) MTJ can be selected only in the source (target) MRAM array which is (not) serially connected to R_G. Although this architecture enables independent STT writing of the input MTJs to eliminate the difference between reading, writing, and performing logic operations, intermediate read/write operations are required to readout the output of any logic operation from the target array and to write it in the source array as an input for the next logic steps. In fact, as there is a need for a physical resistor R_G which is connected in series to S, S (T) can be used only as source (target) MTJ for the implication operations and the logic result stored in T cannot be used as a source input for the next implication operation. Therefore, performing implication operation between two inputs from the same array is not possible without intermediate read/write operations.

Fig. 5.4 shows a simplified implication logic circuit architecture based on the STT-MRAM architecture to realize the MTJ-based current-controlled implication gate (Fig. 5.4). This circuit enables stateful logic for which the need of using extra charge-

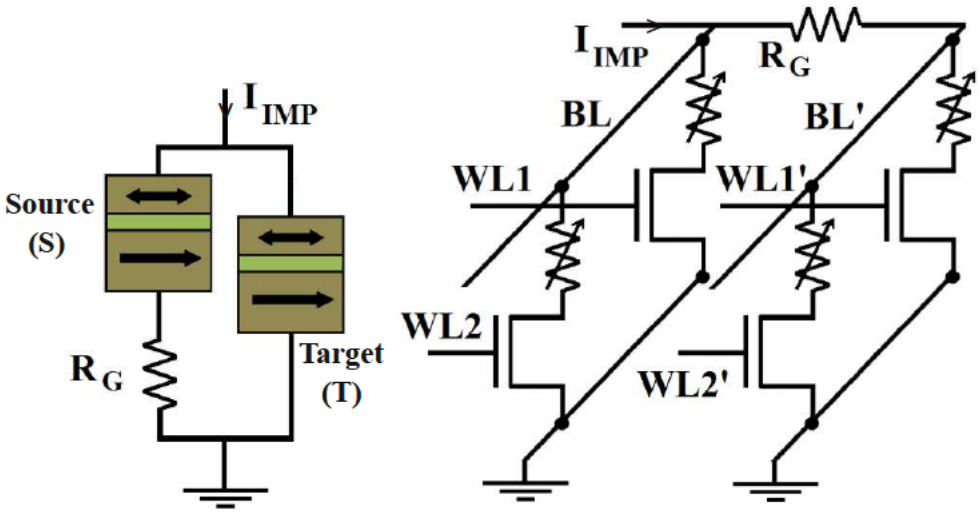

Figure 5.3.: Asymmetric 1T/1MTJ-based implementation (right) of the CC-IMP logic gate (left).

based logic gates is eliminated and the memory cells serve simultaneously as logic gates and latches via implication operation. The implication operation between two cells $C_{i,j}$ and $C_{i,j'}$ ($t_{i,j} \leftarrow s_{i,j'}$ IMP $t_{i,j}$) can be performed by simultaneous selection of the i-th WL, the j-th (target) and the j'-th (source) SLs which are connected to the ground directly and via R_G, respectively, and by applying the current source I_{imp} to the j-th and j'-th BLs. The result of the implication operation is written in $C_{i,j}$.

Compared to the common STT-MRAM architecture, the SL and the BL drivers are more complicated as they have to provide more selection capabilities. Furthermore, two *work cells* are added to each WL, since it has been shown that with two additional memory elements all Boolean functions can be performed on any number of the storage cells [195]. These work cells can also be used to connect different WLs. Indeed, in order to perform the implication between memory cells from different WLs, one has to copy the logic data stored in a memory cell into a work cell from the other WL. This increases the required time and energy consumption and limits the flexibility of the computation.

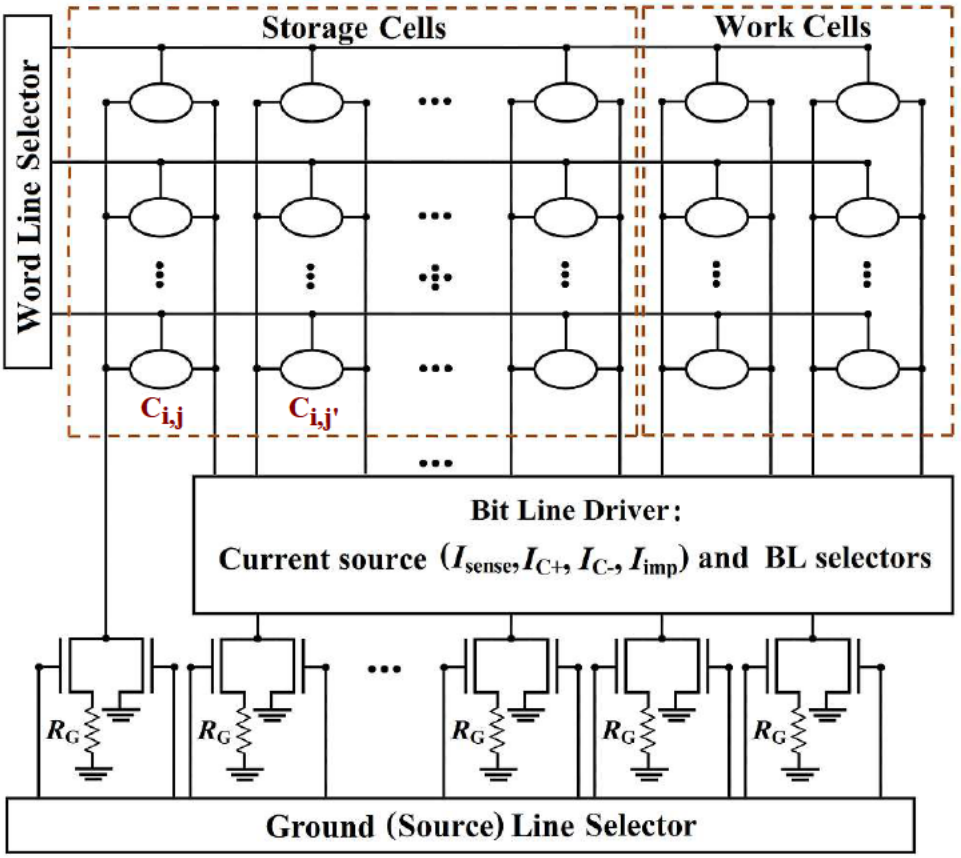

Figure 5.4.: Asymmetric MRAM-based implication logic architecture.

It should be noted that the nonzero ON resistance of the access transistors (R_{on}) decreases the effective TMR ratio of the 1T/1MTJ cells which can be defined as

$$TMR_{eff} = \frac{R_{AP} - R_P}{R_P + R_{on}} \tag{5.5}$$

Therefore, a robust implication operation needs MTJs with sufficiently high TMR ratio and electrical resistance. According to Fig. 4.17b, an implication reliability of 99.9% requires a TMR ratio higher than 250% when the effective TMR ratio of a 1T/1MTJ is decreased by about 10%-30% based on the MTJ and the transistor devices characterized in [50].

5.3.2. Addressing the Asymmetry Issue

The inherent asymmetry of the proposed implication logic gate causes a significant limitation in the flexibility of the computations and forces extra read/write operations in the MRAM-based architectures shown in Fig. 5.3 and Fig. 5.4 as discussed before. This problems can be addressed by an innovative solution for the asymmetry issue by using the access transistors as voltage-controlled resistors to eliminate the need for a physical R_G. If voltage pulses with different amplitudes are applied to the different WLs, the transistors have different bias points (Fig. 5.5) and thus exhibit different channel resistances. Fig. 5.6a shows the MTJ- and the MRAM-based CC-IMP circuit topologies. In the MRAM array, the structural asymmetry required for the CC-IMP is

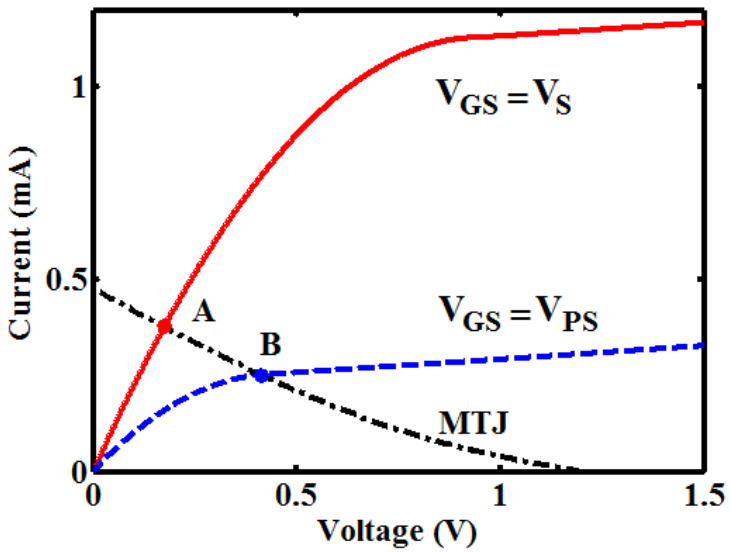

Figure 5.5.: Bias points of the access transistor in a 1T/1MTJ cell for the selecting (point A) and pre-selecting (point B) voltages applied to the word line of the cell.

provided, when the select and pre-select voltage signals (V_s and V_{ps}) are applied to two arbitrary WLs. As $V_{ps} < V_s$, the transistors exhibit different channel resistances and the required structural asymmetry is implicitly provided by the pre-selected transistor featuring a higher resistance which acts as R_G. The logic operation is performed by applying simultaneously the current I_{imp} to the common BL and V_s and V_{ps} to the WLs of the target and the source 1T/1MTJ cells, respectively. The logic result is stored as the final resistance state of the selected (target) MTJ, which can be used now as a source input by pre-selection in the next operations. This significantly reduces the complexity, energy consumption, and delay as it eliminates the need for extra hardware like the source line selector shown required in the MRAM architecture (shown Fig. 5.4) as well as the intermediate read/write operations needed for reading (writing) the target (source) data of the current (next) logic stage.

Fig. 5.6b shows the required circuit signals to implement the universal NOR operation ($a_3 \leftarrow a_1$ NOR a_2) in three steps, one TRUE and two NIMP operations, as shown in Eq. 3.2. According to Eq. 4.27, the reliability of the implication-based NOR is then obtained as $\overline{E}_{NOR} = 1 - (1 - \overline{E}_{IMP})^2$ which is $\simeq 1.9 \times 10^{-4}$ for TMR = 300%. For

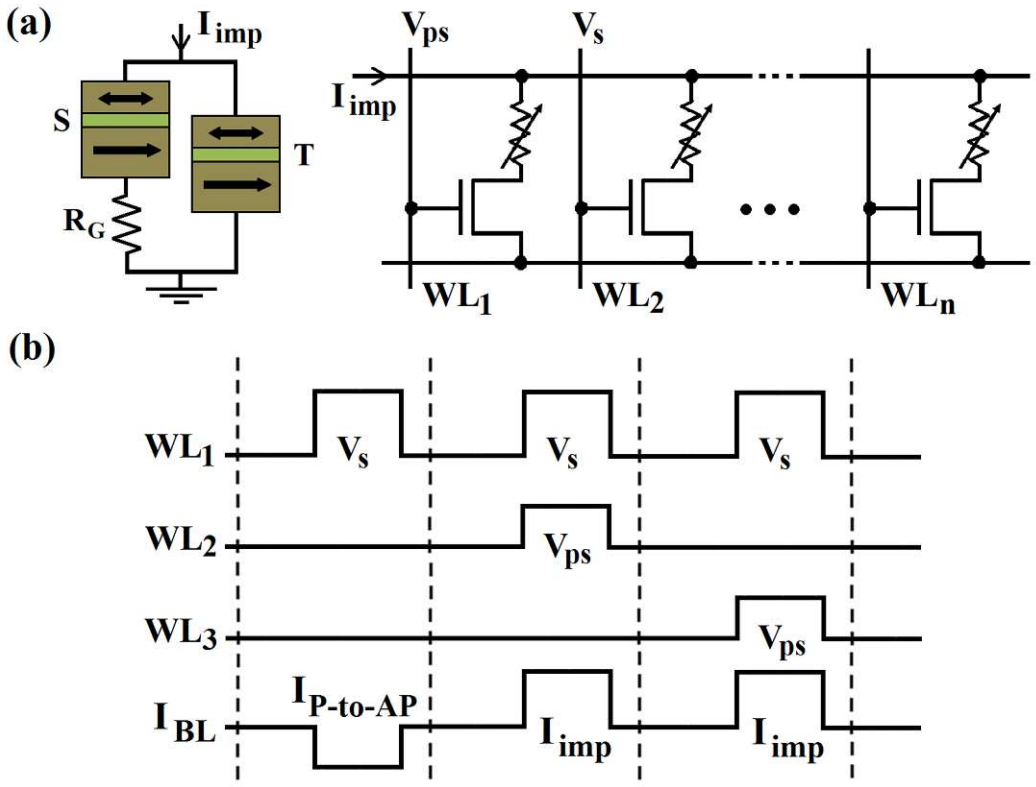

Figure 5.6.: (a) MTJ- and MRAM-based implication logic architectures with no need for a physical R_G. (b) Circuit signals for performing the universal NOR operation in MRAM-based implication logic architecture.

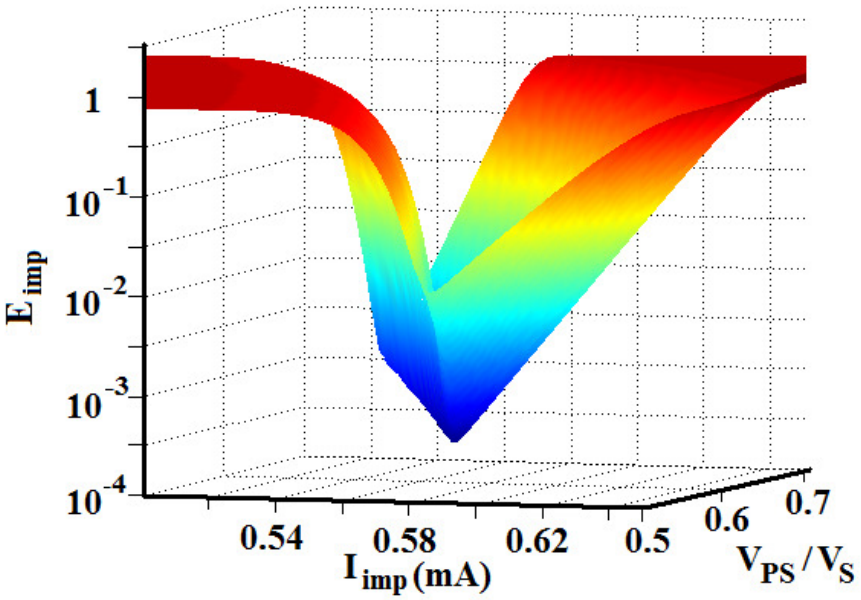

Figure 5.7.: Circuit parameters optimization for minimum error probability of the symmetric implication gate.

a given MTJ and transistor device characteristics, the values of the circuit parameter (I_{imp} and $V_{\text{ps}}/V_{\text{s}}$) are optimized (Fig. 5.7) by using Eq. 5.1 and the reliability model presented in the previous chapter.

5.4. Complex Logic Functions Using Improved Symmetric Implication

In the symmetricized MRAM-based implication logic architecture (Fig. 5.6a), complex logic functions are implemented by using subsequent FALSE (TRUE) and IMP (NIMP) operations. Regardless of the number of inputs, only two extra (*work*) memory elements [195] are needed to compute all Boolean logic functions with maximum $n-2$ inputs in an array with n 1T/1MTJ cells. Nevertheless, in different logic function designs presented in the following we try to minimize the error probabilities and the total logic steps (equivalent to the total operation time and energy consumption) rather than the number of required extra memory elements (equivalent to area), since two cells out of kilobytes or megabytes are negligible.

As an example, in the implication logic the XOR function can be designed as [76]:

$$\begin{aligned} a_1 \oplus a_2 &\equiv a_1.\overline{a_2} + \overline{a_1}.a_2 \\ &\equiv (a_1 \text{ IMP } a_2) \text{ IMP } (a_2 \text{ NIMP } a_1). \end{aligned} \tag{5.6}$$

In the MRAM logic architecture, its implementation ($a_3 = a_1 \oplus a_2$) comprises the following sequential steps (Eq. 5.7) on four MTJs, where two MTJs are inputs (a_1 and a_2) and two MTJs act as *work* MTJs.

$$\begin{aligned}
&\text{TRUE} : a_3 = 1 \\
&\text{NIMP} : \overline{a_3 \rightarrow a_1} \equiv \{a_3' = a_3.\overline{a_1} = \overline{a_1}\} \\
&\text{TRUE} : a_4 = 1 \\
&\text{NIMP} : \overline{a_4 \rightarrow a_2} \equiv \{a_4' = a_4.\overline{a_2} = \overline{a_2}\} \\
&\text{NIMP} : \overline{a_2 \rightarrow a_1} \equiv \{a_2' = a_2.\overline{a_1}\} \\
&\text{NIMP} : \overline{a_4 \rightarrow a_3} \equiv \{a_4' = a_4.\overline{a_3} = \overline{a_2}.a_1\} \\
&\text{TRUE} : a_1 = 1 \\
&\text{NIMP} : \overline{a_1 \rightarrow a_2} \equiv \{a_1' = a_1.\overline{a_2} = 1.(\overline{a_2.\overline{a_1}}) = \overline{a_2} + a_1\} \\
&\text{NIMP} : \overline{a_1 \rightarrow a_4} \equiv \{a_1' = a_1.\overline{a_4} = (\overline{a_2} + a_1).(a_2 + \overline{a_1})\} \\
&\text{TRUE} : a_3 = 1 \\
&\text{NIMP} : \overline{a_3 \rightarrow a_1} \equiv \{a_3' = a_3.\overline{a_1} = a_2.\overline{a_1} + \overline{a_2}.a_1 \equiv a_1 \oplus a_2\}
\end{aligned} \tag{5.7}$$

According to Eq. 4.27, as the implementation includes seven NIMP operations, the reliability of the implication-based XOR for TMR = 300% is obtained as

$$\overline{E}_{\text{XOR}} = 1 - (1 - \overline{E}_{\text{IMP}})^7 \simeq 6.5 \times 10^{-4}. \tag{5.8}$$

This is about one order of magnitude smaller than that of the most reliable design with the reprogrammable architecture for the same MTJ device characteristics and it requires the same number of sequential steps compared to its reprogrammable counterpart comprising 11 operations (Eq. 5.4).

5.4.1. Non-Volatile Logic Fan-Out

In the magnetoresistive (MR) non-volatile logic the resistance states of the MR devices are the physical state variables. This is different compared to CMOS logic where information is represented by charge or voltage. Most of the previous proposals for MR-based logic circuits [19, 52, 54, 193, 196–199] require intermediate circuitry for sensing the data stored in each non-volatile magnetic element to implement fan-out functions [169]. This increases the power consumption, time delay, area, and integration complexity. A possible remedy is to switch to direct communication between the MR devices thus removing intermediate circuitry [26, 56, 57, 200–202]. However, this makes the computations localized by confining them to the MR devices which are directly coupled. Therefore, in the state-of-the-art, large-scale integration of complex logic functions is difficult or may be even impossible by using the non-volatile logic-in-memory concept due to the hard linking between different gates and the need for sensing amplifiers and intermediate circuitry. In the STT-MRAM-based implication

logic with symmetric implementation (Fig. 5.6a), the issue of the non-volatile logic fan-out function can be addressed as follows.

The output information of a logic operation (IMP/NIMP) can be used to perform the next operation with an arbitrary MTJ in the array as a source or a target input. This provides high flexibility with regard to the non-volatile logic fan-out function. However, when the (N)IMP operation is executed, the target data is not available anymore, as the (N)IMP result is written into the target MTJ. Therefore, as long as the data is used only as the source data in the subsequent operations, multiple logic fan-output is not required. But, when the data has to be reused after being the target data of an operation, implication-based NOT and COPY (2×NOT) operations are executed to keep the data available. As a consequence, when multiple fan-out is required, a set of FALSE (TRUE) and IMP (NIMP) operations are performed to execute NOT and COPY operations in the implication MRAM array (Fig. 5.6a). This allows to copy information from the source MTJ (which could be the target MTJ of the previous operation) to an arbitrary target MTJ in the array without the need for intermediate sensing. As an example, the next section describes the STT-MRAM-based implementation in the implication logic framework.

5.4.2. Stateful STT-MRAM-based Full Adder

A full adder is a basic element of arithmetic circuits. As is well known, it adds three binary inputs (a_1, a_2, and c_{in}) and produces two binary outputs, sum (s) and carry (c_{out}) obtained as

$$s = a_1 \text{ XOR } a_2 \text{ XOR } c_{\text{in}} \tag{5.9}$$

and

$$c_{\text{out}} = (a_1 \text{ AND } a_2) \text{ OR } (c_{\text{in}} \text{ AND } (a_1 \text{ XOR } a_2)). \tag{5.10}$$

Since the implication gates cannot fan-out, a logical value which is required as the target variable for an implication operation has to be copied in a *work* (additional) cell (a_3, a_4, or a_5), if it is needed as an input for subsequent operations. Eq. 5.12 and Eq. 5.13 show the TRUE/NIMP and the FALSE/IMP-based implementations of a stateful full adder using the MRAM implication logic arrays, respectively. The detailed derivations are given in Appendix A.

$$\begin{gathered}\{a_3 = 1,\ \overline{a_3 \rightarrow a_1},\ a_4 = 1, \overline{a_4 \rightarrow a_2}, \overline{a_4 \rightarrow a_3}, \overline{a_2 \rightarrow a_1},\\ a_5 = 1, \overline{a_5 \rightarrow a_2}, \overline{a_5 \rightarrow a_4}, \overline{a_2 \rightarrow a_2}, \overline{a_1 \rightarrow a_4}, a_4 = 1,\\ \overline{a_4 \rightarrow c_{\text{in}}}, \overline{c_{\text{in}} \rightarrow a_3}, a_3 = 1, \overline{a_3 \rightarrow a_1}, \overline{a_3 \rightarrow c_{\text{in}}}, a_1 = 1, \overline{a_1 \rightarrow a_3}, \}\\ \equiv \{a_1 = a_1.a_2 + c_{\text{in}}.(a_1 \oplus a_2) = c_{\text{out}}\}\end{gathered} \tag{5.11}$$

$$\{a_2 = 1, \overline{a_2 \rightarrow a_4}, a_3 = 1, \overline{a_3 \rightarrow a_5}, \overline{a_3 \rightarrow a_2}, \overline{a_5 \rightarrow a_4},$$
$$a_2 = 1, \overline{a_2 \rightarrow a_3}, \overline{a_2 \rightarrow a_5}, a_4 = 1, \overline{a_4 \rightarrow a_2}\}$$
$$\equiv \{a_4 = a_1 \oplus a_2 \oplus c_{\text{in}} = s\} \tag{5.12}$$

$$\{a_3 = 0,\ a_1 \rightarrow a_3,\ a_4 = 0, a_2 \rightarrow a_4, a_3 \rightarrow a_4, a_5 = 0,$$
$$a_4 \rightarrow a_5, a_4 = 0, a_2 \rightarrow a_4, a_4 \rightarrow a_3, a_3 \rightarrow a_5, a_1 \rightarrow a_4,$$
$$a_1 = 0, a_5 \rightarrow a_1, c_{\text{in}} \rightarrow a_1, a_2 = 0, a_1 \rightarrow a_2, a_4 \rightarrow a_2\}$$
$$\equiv \{a_2 = a_1.a_2 + c_{\text{in}}.(a_1 \oplus a_2) = c_{\text{out}}\}$$

$$\{a_3 = 0, c_{\text{in}} \rightarrow a_3, a_1 = 0, a_5 \rightarrow a_1, a_3 \rightarrow a_1,$$
$$a_3 = 0, a_1 \rightarrow a_3, c_{\text{in}} \rightarrow a_5, a_5 \rightarrow a_3\}$$
$$\equiv \{a_5 = a_1 \oplus a_2 \oplus c_{\text{in}} = s\} \tag{5.13}$$

The FALSE/IMP-based design involves only 27 subsequent (9 FALSE and 18 IMP) operations on three input cells (a_1, a_2, and c_{in}) and three additional cells (a_3, a_4, or a_5), in contrast to the earlier proposed implication-based scheme [203] with 19 FALSE and 18 IMP operations (37 total) for generating s and c_{out}, respectively, and four additional cells. Therefore, this design decreases the total implementation time by about 30% and reduces energy consumption and device count (area). As 'a_{i} NIMP 1' and 'a_{i} NIMP a_{j}' are equivalent to 'NOT a_{i}' and 'a_{i} AND (NOT a_{j})', respectively, some operations can be omitted to minimize the total effort.

In the magnetic full adders based on the logic-in-memory architecture presented in [54] and [204], the MTJs are used only as ancillary devices which store the result of the logic computations performed by the transistors. Therefore, the logic operations are still performed by CMOS logic elements and 26 transistors for logic, 8 for MTJ writing, and 4 MTJs for storing data are required. In contrast, the MRAM-based implication architecture exploits the MTJs as the main devices for computations and eliminates the need for extra logic gates. It therefore brings considerable benefit regarding the device count. Furthermore, a key limitation of the magnetic full adders in [54] and [204] is the necessity of different kind of inputs and outputs for which some inputs or outputs are voltage signals, whereas the others are the resistance state of the MTJ elements. This mismatch causes the need for extra hardware and increases complexity.

5.5. Toward High Performance STT-MRAM-Based Stateful Logic

The energy consumptions and the average error probabilities of the same Boolean logic functions are calculated by using the improved MTJs SPICE model and the reliability analysis method explained in Chapter 4. The same device (MTJ and transistor) characteristics are assumed for both implementations and the circuit parameters are optimized for TMR = 300% with respect to their minimum error probabilities of the basic logic operations (Fig. 4.21).

Fig. 5.8a shows the energy consumptions of implication- and reprogrammable-based

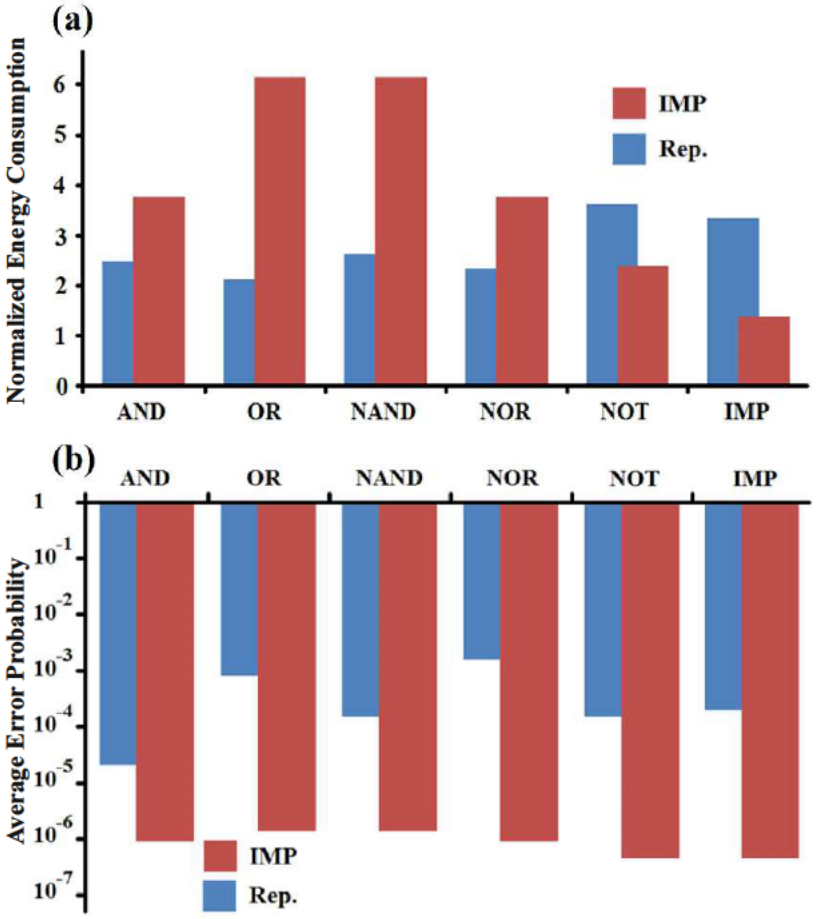

Figure 5.8.: (a) Normalized energy consumption and (b) minimum average error probabilities plotted for MRAM-based implication (IMP) and reprogrammable (Rep.) implementations of some basic Boolean logic operations. The energy is normalized by the TRUE operation switching energy which is equal to 18 pJ for a pulse duration of $t = 50$ ns in the simulations.

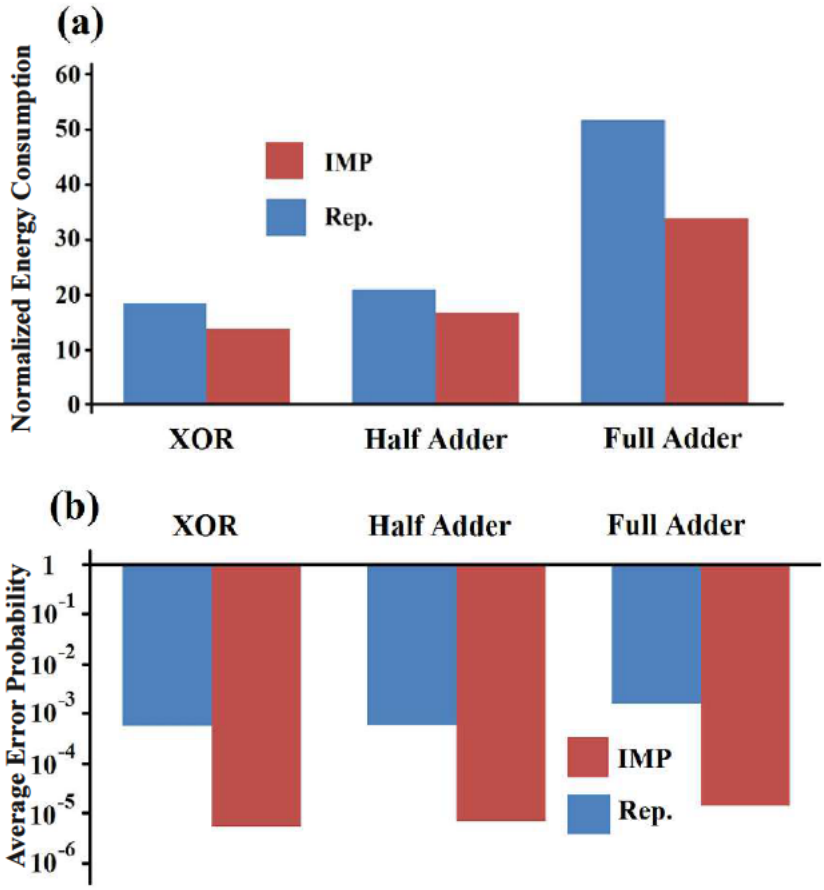

Figure 5.9.: (a) Normalized energy consumption and (b) minimum average error probabilities plotted for different logic functions.

implementations of some basic Boolean logic operations. The energy consumptions are normalized by the amount of energy required for AP–to–P MTJ switching which is equal to 18 pJ for pulse duration of $t = 50$ ns in the simulations. Due to the mismatch between the intrinsic logic functions of the gates, the implication-based implementation requires more steps and thus more energy (by an average factor of ∼1.4) to implement the basic operations. However, even for the intrinsic functions of the reprogrammable gate, the implication logic exhibits about 1-3 orders of magnitude higher reliability than the reprogrammable logic architecture (Fig. 5.8b).

In order to see the performance at larger circuits, the energy consumptions and the average error probabilities of more complex Boolean functions including an XOR, a half adder, and a full adder are compared in Fig. 5.9a and Fig. 5.9b. Only AND and NAND operations are used to provide the most reliable design for the reprogrammable architecture. Nevertheless, Fig. 5.9b shows that the implication-based implementation of more complex functions exhibits about two orders of magnitude higher reliability than the most reliable design with the reprogrammable architecture. Furthermore, for com-

plex logic functions which are not inherently covered by the gates, the implication logic architecture performs also better with respect to the power consumption (Fig. 5.9a). In combination with '0' and '1' writing operations, both reprogrammable-based AND-NAND and implication-based IMP-NIMP logic functions form complete logic bases. Thus, any Boolean logic function can be computed in a series of subsequent steps using these architectures. Furthermore, combining implication and (N)AND-based reprogrammable frameworks in MRAM arrays is a possible direction in designing large-scalable MRAM-based logic circuits featuring a minimized number of logic steps and an optimized error, delay, and power consumption.

5.5.1. Combined Reprogrammable-Implication Logic

The implication logic outperforms the reprogrammable architecture in most aspects as explained before (Fig. 5.9) and thus is expected to be the implementation of choice for MRAM-based stateful logic circuits. However, in the following more design tradeoffs are discussed by combining these logic architectures.

Due to their computational completeness, implication and reprogrammable MRAM-based stateful logic architectures can be used independently to design any Boolean logic function. However, their combination can minimize the number of required logic steps as it provides more degrees of freedom by employing more fundamental logic operations and choosing the gates with the best performance with respect to their desired attributes. Thus, the execution time and the energy consumption of complex logic functions can be reduced. For example, in the combined reprogrammable-implication (CRI) architecture the XOR function can be designed as:

$$\begin{aligned}
&\text{TRUE}: a_3, a_4 = 1\\
&\text{NIMP}: \overline{a_3 \rightarrow a_1} \equiv \{a_3' = a_3.\overline{a_1} = \overline{a_1}\}\\
&\text{NIMP}: \overline{a_4 \rightarrow a_2} \equiv \{a_4' = a_4.\overline{a_2} = \overline{a_2}\}\\
&\text{Preset}: b_1 = 0\\
&\text{NAND}: b_1 = \overline{a_1.a_4}\\
&\text{Preset}: b_2 = 0\\
&\text{NAND}: b_2 = \overline{a_2.a_3}\\
&\text{Preset}: a_5 = 1\\
&\text{AND}: a_5 = \overline{b_1.b_2} \equiv a_1 \text{ XOR } a_2,
\end{aligned} \tag{5.14}$$

According to Fig. 5.10a, the CRI design provides a lower energy consumption compared to both implication and reprogrammable designs. However, its error probabilities is higher than the implication design (Fig. 5.10b) since it employs basic reprogrammable operations.

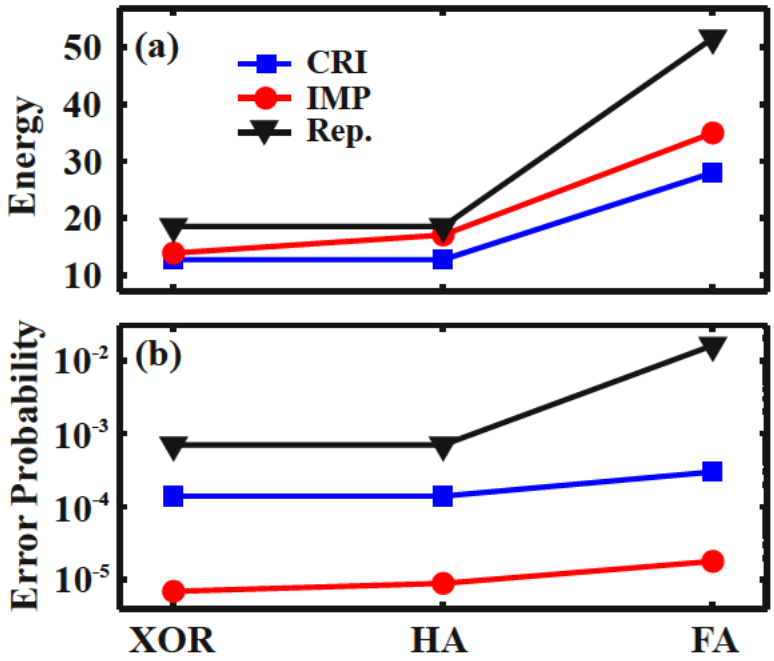

Figure 5.10.: (a) Energy consumption for complex logic functions. (b) $\overline{E}_{\mathrm{f}}$ for different MRAM-based implementations of functions XOR, half adder (HA), and full adder (FA).

5.5.2. Parallel STT-MRAM-Based Computation

Parallelization of several MRAM arrays can be used to simultaneously perform operations on the same word lines to decrease the number of required serial steps. For example, the required steps to implement the XOR function presented in Eq. 5.7 can be performed in parallel in the MRAM structure shown in Fig. 5.11. By applying the single/dual mode voltage signals to the word lines (Fig. 5.6b) to execute TRUE/NIMP (FALSE/IMP) operations, the corresponding MTJs are selected or pre-selected in all arrays. Therefore, by applying relevant current signals ($I_{\mathrm{P-to-AP}}$ or I_{imp}) simultaneously to all current-carrying lines (SLs and BLs), the computations are performed in parallel. This significantly reduces the total time needed for implementing XOR functions on binary data (a_i and a_j) stored in the i-th and j-th MTJs of each array. Similarly, reprogrammable operations can be parallelized when the two group of coupled arrays are connected in series.

For more complicated applications in which intermediate results have to be used as input for the next logic steps (e.g. n-bit full adders, where $n > 1$) only some parts of the computations can be performed in parallel. As an example, Fig. 5.12 shows a two-bit full adder in which the carry output from the first full adder (c_{out}) is connected to the carry input of the second full adder (c'_{in}). Therefore, it is not possible to perform all computations in parallel.

Assuming that a_1 (a_2) and a'_1 (a'_2) are stored in the first (second) MTJs in the MRAM arrays 1 and 1′ which have coupled WLs, the AND and the XOR functions between (a_1, a_2) and (b_1, b_2) can be performed in parallel (Fig. 5.12). In fact, when for performing a logic operation a_1 and a_2 are selected or pre-selected through the corresponding WLs, a'_1 and a'_2 are also selected or pre-selected as they share the same WL with a_1 and a_2, respectively. Therefore, if the same current pulses are applied to both BL and BL′, the same logic operations will be performed in parallel in both arrays. After performing the first AND and XOR operations in parallel, c_{out} (c'_{in}) is calculated without parallelization. This part of the calculations is performed in Array 1 and it cannot be parallelized with other computations in Array 1′. Then by using a read/write operation the result is written into the MTJ in Array 1′ which is in the same WL as the MTJ that holds c_{in} in Array 1. After that, the last XOR functions are performed in parallel to calculate s_1 and s_2 and finally the calculations are continued to compute c'_{out} in Array 1′. As a result, by parallelization of the MRAM-based logic arrays, the total calculation time required for the implication-based and CRI-based implementations of a two-bit full adder are decreased by about 40% and 50% (Fig. 5.13). It is worth noting that the parallelization does not affect the reliability and the energy consumption since only some steps are performed in parallel while the total number of logic operations is still fixed.

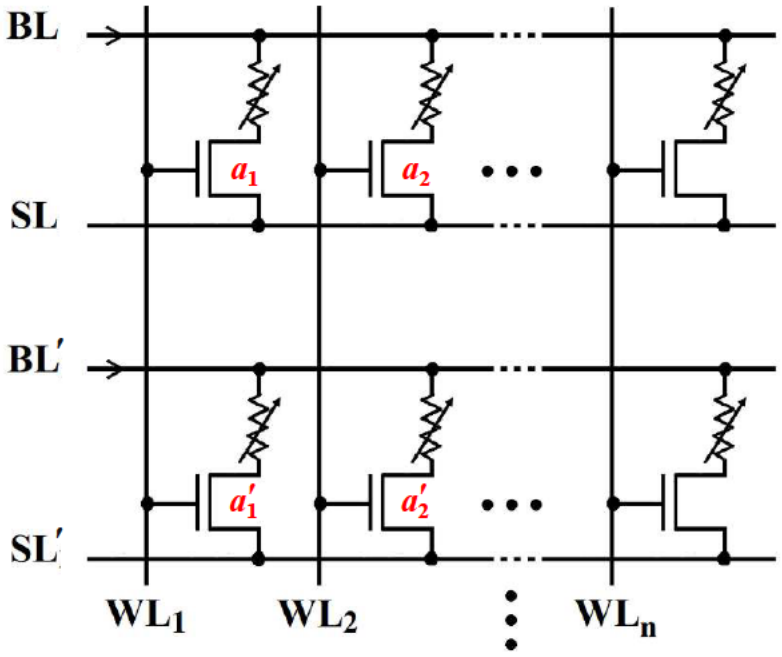

Figure 5.11.: Coupled MRAM arrays based on the common STT-MRAM architecture suited for parallel MRAM-based computations.

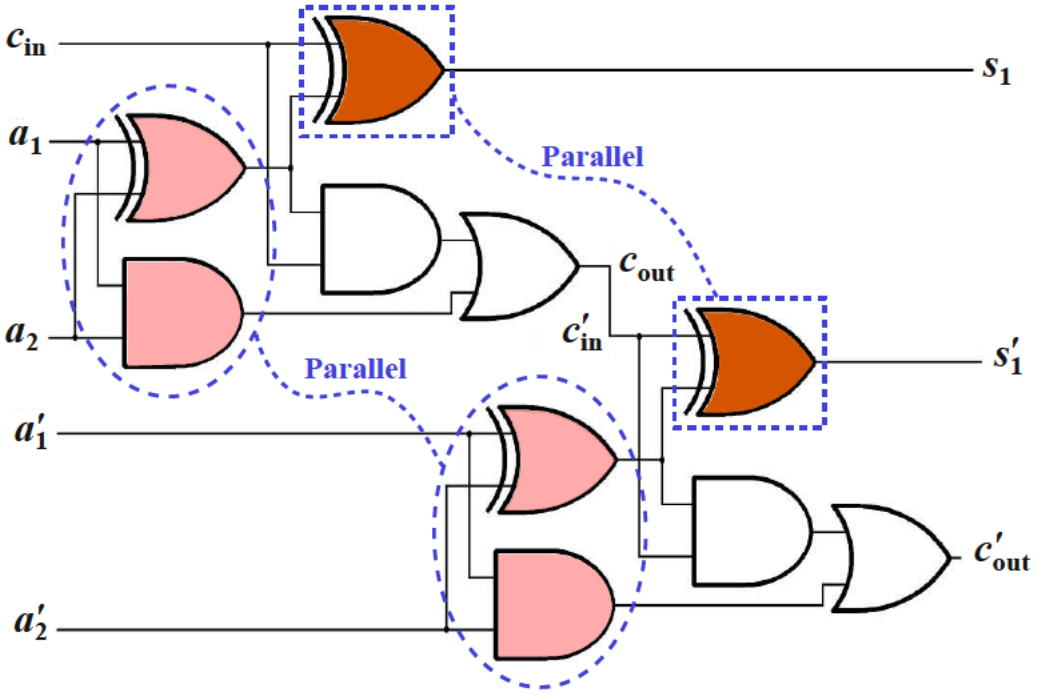

Figure 5.12.: Logic diagram of a two-bit full adder.

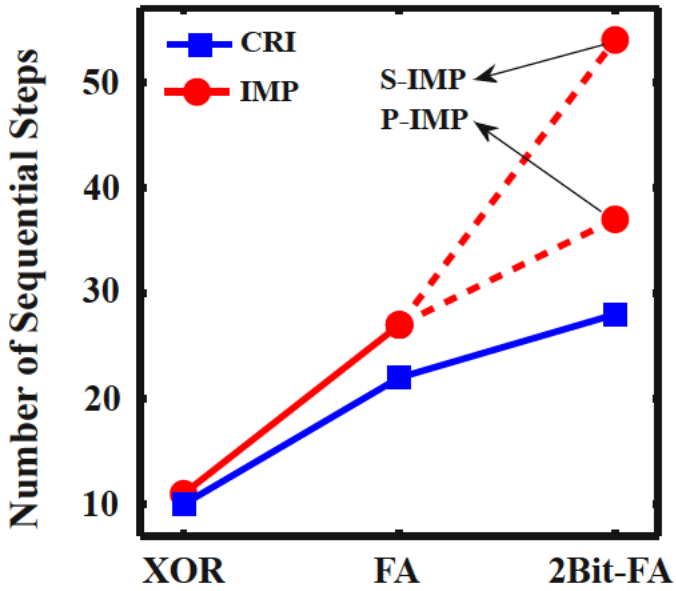

Figure 5.13.: Required sequential steps for serial (S-IMP) and parallel (P-IMP) MRAM-based implication and combined reprogrammable-implication (CRI) architectures.

5.6. Summary

Because of the easy integration with CMOS, the MTJ-based logic gates are generalizable to STT-MRAM-based stateful logic architectures by using hybrid CMOS/MTJ technology. By utilizing the access transistors of the 1T/1MTJ cells not only as on-off switches but also as voltage-controlled resistors, the circuit implementation of the structural asymmetry in the improved implication logic gates is addressed. This STT-MRAM-based logic implementation enables non-volatile logic fan-out and provides high flexibility with regard to the use of arbitrary MTJs as input and output. The implementation is computationally complete, has a simple circuit structure (STT-MRAM), delocalizes computational execution, and eliminates the need for intermediate circuitry. It also enables parallel non-volatile computations and, therefore, it is suited for complex logic functions evaluation and opens an alternative path towards zero-standby power logic systems, shifting away from the Von Neumann architecture by eliminating the need for data transfer between separate memory and logic units to shorten the interconnection delay.

A performance analysis and comparison of the MRAM-based implication and reprogrammable logic architectures is presented. It is shown that for the intrinsic (N)AND and (N)OR operations, the reprogrammable gate requires slightly less power than the corresponding implication-based implementation. However, MRAM-based implication logic enables a more reliable logic behavior as compared to the reprogrammable gates. Furthermore, the implication architecture outperforms the reprogrammable gate for more complex logic functions and is thus the implementation of choice for large-scale logic circuits. As an example, the implementation of a stateful full adder based on the STT-MRAM implication logic architecture is described. Compared to the previous implication-based design, the total number of logic steps is decreased by about 30% and thus less execution time and energy are required. The possible tradeoffs to optimize the execution time, energy consumption, and the reliability of the reprogrammable and implication MRAM-based stateful logic architecture are also described. It is shown that a combined reprogrammable-implication logic architecture minimizes the total number of the required logic steps and thus the energy consumptions. However, it decreases the reliability of the MRAM-based computation. It is demonstrated that the parallelization of MRAM-based computations can significantly reduce the execution time.

6. Memristive Charge- and Flux-Based Sensing

6.1. Overview

The memristor concept has attracted strong attention due to its practical demonstration based on different technologies like metal/oxide/metal thin-film and spintronic. It has the potential to lead to novel applications beyond non-volatile memory due to its functional properties, which are not accessible in electronic circuits combining resistors, capacitors, and inductors. As the fourth fundamental circuit element, the memristor is potentially suited for a wide range of tasks (Chapter 1). In this Chapter, it is shown how the unique ability of the memristor to memorize the history of the applied current or voltage leads to novel sensing capabilities which cannot be achieved by RLC-networks alone. The historic profile of the applied current or voltage memorized in the memristance change can be revealed instantaneously by keeping track of its varying resistance. In principle, this storage capability, which is independent of the memristor material, can reduce the charge (flux)-based capacitance (inductance) sensing to a simple resistance measurement.

The behavior of the basic electrical circuits are determined by Kirchhoff's current (KCL) and voltage (KVL) laws. A resistor relates the voltage and the current by a (linear) relationship called Ohm's law. Its resistance, therefore, can be determined by measuring the current and the voltage simultaneously. Since a capacitor and an inductor relate their voltage and current through differential equations (Section 2.1.1), the capacitance and the inductance are typically measured indirectly and their measurement techniques are entirely different from those used for a resistor. Approaches to measuring C and L are based on time domain techniques and frequency domain techniques. For example, in the time domain techniques C is calculated by measuring the oscillation period of a relaxation oscillator [205, 206] or the time required to reach a threshold voltage in a charge-discharge circuit [207, 208]. In the frequency domain technique an AC signal of a known frequency is applied to a capacitive divider (CC circuit) or an RC circuit. The magnitude and the phase of the output signal across the capacitor or the resistor are measured to determine C [209, 210].

6.2. Memristive Sensing Principles

The memristive sensing scheme explained below can be classified as a novel charge-discharge (time domain) technique in which the capacitance or the inductance is calculated by measuring the memristance (memductance) and thus eliminates the need for time (frequency) measurement. In fact, the memristance (in the unit of Ω) or memductance (in the unit of $\mathrm{S} = \Omega^{-1}$) of a memristor can be simply determined by Ohm's law, which makes the memristive sensing straightforward and fast. Furthermore, because a memristor holds the information even if its voltage/current is turned off (non-volatility), it allows for measurement circuits with low leakage power consumption and new functionalities.

6.2.1. Charge-Controlled Memristors

6.2.1.1. Capacitance Sensing

Consider a charge-controlled memristor connected in series with a capacitor as shown in Fig. 6.1. According to Eq. 2.4 and Eq. 2.10 for the capacitance and memristance, respectively, we have

$$C = \frac{dq_\mathrm{C}}{dv_\mathrm{C}} = \frac{dq_\mathrm{C}/dt}{dv_\mathrm{C}/dt} = \frac{i_\mathrm{C}}{dv_\mathrm{C}/dt} \tag{6.1}$$

and

$$\frac{dM(q)}{dt} = \frac{dM(q)}{dq_\mathrm{M}}\frac{dq_\mathrm{M}}{dt} = \frac{dM(q)}{dq_\mathrm{M}} i_\mathrm{M}. \tag{6.2}$$

As $i_\mathrm{M} = i_\mathrm{C}$, by substituting i_M from Eq. 6.2 into Eq. 6.1 we obtain

$$C = \left(\frac{dM(q)}{dq_\mathrm{M}}\right)^{-1} \frac{dM/dt}{dv_\mathrm{C}/dt} = \left(\frac{dM(q)}{dq_\mathrm{M}}\right)^{-1} \frac{dM}{dv_\mathrm{C}}. \tag{6.3}$$

The term dM/dq_M is related to the intrinsic properties of the memristor. For a linear resistor this term is zero. However, it is nonzero for a memristive device or system as it is supposed to memorize the history of current flowing through the modulation in its memristance. A charge-controlled memristor with the term dM/dq_M being constant is suited for charge-based capacitance sensing as it can reduce the measurement to a simple memristance measurement. In fact, on one hand, as $dv_\mathrm{C} \propto dq_\mathrm{C}$ and $dq_\mathrm{C} = dq_\mathrm{M}$, we have $dv_\mathrm{C} \propto dq_\mathrm{M}$. On the other hand, as for the memristor the term dM/dq_M is constant, we have $dq_\mathrm{M} \propto dM$. Therefore, $dv_\mathrm{C} \propto dM$ and thus dM/dv_C is equal exactly to $\Delta M/\Delta v_\mathrm{C}$. As a result, Eq. 6.3 is written as

$$C = \left(\frac{dM(q)}{dq}\right)^{-1} \frac{\Delta M}{\Delta v_\mathrm{C}} = \left(\frac{dM(q)}{dq}\right)^{-1} \frac{M(t=t_0) - M(t=0)}{v_\mathrm{C}(t=t_0) - v_\mathrm{C}(t=0)}. \tag{6.4}$$

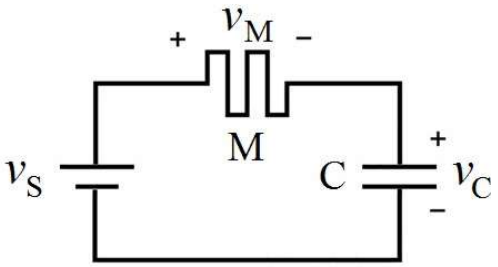

Figure 6.1.: A diagram of the charge-based memristive capacitance sensing circuit.

This means that one can calculate the capacitance by measuring the modulation of the memristance and the voltage across the capacitor (or the memristor). Therefore, unlike other time domain capacitance measurement methods, memristive sensing does not need extra hardware for time/frequency measurement since the time parameter has been implicitly taken into account in the memristance modulation. Furthermore, to measure the memristance modulation, a simple circuit can be employed to switch the memristor from the MC circuit (Fig. 6.1) to a basic readout circuit employing an arbitrary resistance read method [97], without loosing the information during the switching due to the non-volatility of the memristor. During the readout, the memristance and the charge in the capacitor can be reset to the initial state for which the M and v_C are equal to $M(t = 0)$ and $v_C(t = 0)$, respectively. Then, for the next measurement, one should measure only $M(t = t_0)$ and probably $v_C(t = t_0)$ if the capacitor is not fully charged ($v_C < v_s$).

6.2.1.2. Power Monitoring

The unique ability of a memristor to record the historic profile of the voltage/current applied makes it suitable for power measurement [97]. The total energy generated by an electric power supply $\mathcal{E} = \int V_s(t)I_s(t)dt$, where $V_s(t)$ is the voltage across the source and $I_s(t)$ is the current flowing through it. For a circuit powered by a DC voltage source (Fig. 6.2) [97], the energy is given by:

$$\mathcal{E} = V_s \int_{t_1}^{t_2} I_s(t)dt = V_s \Delta q_M = V_s \Delta M \left(\frac{dM(q)}{dq_M} \right)^{-1} \tag{6.5}$$

Therefore, a charge-controlled memristor with a constant term $dM(q)/dq_M$ reduces the power measurement to a memristance measurement. To minimize the impact of the memristor on measurements, the memristance has to be much smaller than the circuit resistance.

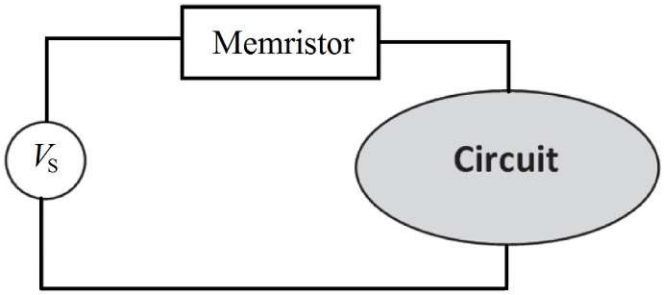

Figure 6.2.: A diagram of the memristive power monitoring circuit with a charge-controlled memristor.

6.2.2. Flux-Controlled Memristors

6.2.2.1. Inductance Sensing

According to Eq. 2.5 and Eq. 2.11 for the inductance and memductance of a flux-controlled memristor, respectively, we have

$$L = \frac{d\varphi_L}{di_L} = \frac{d\varphi_L/dt}{di_L/dt} = \frac{v_L}{di_L/dt} \tag{6.6}$$

and

$$\frac{dW(\varphi)}{dt} = \frac{dW(\varphi)}{d\varphi_M}\frac{d\varphi_M}{dt} = \frac{dW(\varphi)}{d\varphi}v_M. \tag{6.7}$$

When a flux-controlled memristor is connected in parallel to an inductor ($v_M = v_L$ in Fig. 6.3), the inductance is obtained as

$$L = \left(\frac{dW(\varphi)}{d\varphi_M}\right)^{-1}\frac{dW/dt}{di_L/dt} = \left(\frac{dW(\varphi)}{d\varphi_M}\right)^{-1}\frac{dW}{di_L}. \tag{6.8}$$

A flux-controlled memristor with a constant $dW/d\varphi_M$ term is thus suited for flux-based inductance measurement. For a common conductor the term $dW/d\varphi_M$ is zero. However, it is nonzero for a memristive device and is related to the intrinsic properties of the memristor. Based on a similar discussion presented above for the MC circuit, in the ML circuit with a memristor with $dW/d\varphi_M = \text{const.}$, we get $di_L \propto dW$. Therefore, Eq. 6.8 is simplified to

$$L = \left(\frac{dW(\varphi)}{d\varphi_M}\right)^{-1}\frac{\Delta W}{\Delta i_L} = \left(\frac{dW(\varphi)}{d\varphi_M}\right)^{-1}\frac{W(t=t_0) - W(t=0)}{i_L(t=t_0) - i_L(t=0)}. \tag{6.9}$$

Hence, the flux-controlled memristor in the ML circuit reduces the inductance measurement to a straightforward memductance measurement.

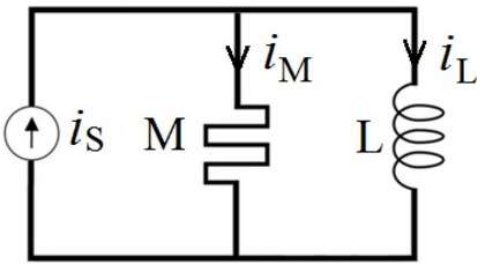

Figure 6.3.: Basic memristor-inductor (ML) circuit for flux-based sensing.

6.2.2.2. Power Monitoring

Similar to the charge-based power monitoring, in a circuit powered by a DC current source (Fig. 6.4) [97], a flux-controlled memristor with the term $dW(\varphi)/d\varphi$ being constant reduces the power measurement to a memductance measurement.

$$\mathcal{E} = I_s \int V_s(t)dt = I_s \Delta\varphi_M = I_s \Delta W \left(\frac{dW(\varphi)}{d\varphi_M}\right)^{-1} \tag{6.10}$$

To minimize the impact of the memristor on measurements, the memductance must be much smaller than the circuit conductance. In the following section we study different spintronic memristors which are suited for both charge- and flux-based measurements.

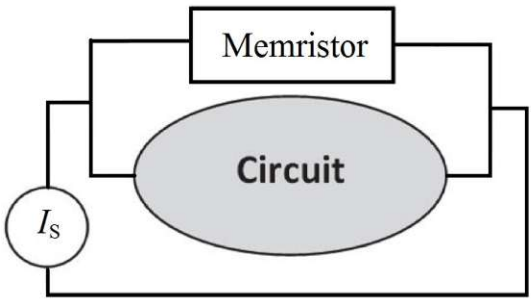

Figure 6.4.: A diagram of the memristive power monitoring circuit using a flux-controlled memristor.

6.3. Memristive Devices for Sensing

6.3.1. TiO_2-Based Memristors

According to Eq. 3.7, the term dM/dq for the TiO_2-based memristor is obtained as

$$\frac{dM(q)}{dq} = \frac{R_{\text{int}}(w)}{dw}\frac{dw}{dq} = \frac{R_{\text{off}} - R_{\text{on}}}{w_{\text{max}}}\frac{dw}{dq}. \tag{6.11}$$

From Eq. 3.8, we then obtain

$$dw = \frac{\mu_{\text{v}} R_{\text{on}}}{w_{\text{max}}} i_{\text{M}}(t)dt = \frac{\mu_{\text{v}} R_{\text{on}}}{w_{\text{max}}} dq. \tag{6.12}$$

Therefore, we get

$$\frac{dM(q)}{dq} = \frac{R_{\text{int}}(w)}{dw}\frac{dw}{dq} = \frac{\mu_{\text{v}} R_{\text{on}}}{w_{\text{max}}^2}(R_{\text{off}} - R_{\text{on}}) \backsimeq \frac{\mu_{\text{v}} R_{\text{on}} R_{\text{off}}}{w_{\text{max}}^2} = \text{const.} \tag{6.13}$$

Thus, according to Eq. 6.4 and Eq. 6.5, this device can be used for charge-based memristive sensing. Let us consider a memristor-capacitor (MC) circuit shown in the inset of Fig. 6.5d. Fig. 6.5a shows the $i-v$ characteristics of the memristor, when the MC circuit is excited by a step voltage source $v_{\text{s}}(t) = u(t)$ where $u(t)$=0 for $t < 0$ and 1 for $t > 0$. The memristor exhibits different behavior for different capacitances. As it is expected, the smaller the capacitance the smaller the charging time (Fig. 6.5b) as well as the smaller the charge modulation. Thus, the memristance exhibits smaller modulation for smaller capacitance (Fig. 6.5c). This is the key idea to measure the capacitance by using Eq. 6.4 based on the modulations of the voltage across the capacitor and the memristance. According to Eq. 6.4, if the measurement is performed after the capacitor is fully charged ($\Delta v_{\text{C}} = 1$ V), only the memristance modulation has to be measured. However, depending on the readout resolution, the measurement can be performed in a time interval (much) shorter than the full charge time (Fig. 6.5d). In Fig. 6.5, the TiO_2-based memristor device characteristics are assumed as $R_{\text{on}} = 100\Omega$, $R_{\text{off}}/R_{\text{on}} = 360$, $\mu_{\text{v}} = 10^{-10}\text{cm}^2\text{s}^{-1}\text{V}^{-1}$, and $w_{\text{max}} = 5\text{nm}$ [70].

6.3.2. Spintronic Memristors

6.3.2.1. Magnetoresistive Devices

Fig. 6.6 shows two magnetoresistive spintronic memristors with current-induced domain wall motion in a giant magnetoresistance spin-valve (Fig. 6.6a) and a tunneling device (Fig. 6.6b). The electrical resistance (conductance) of these devices $R(r)$ ($G(r)$) is a function of the DW position ($x = rL$) in the magnetic free layer [95, 97, 138]. A

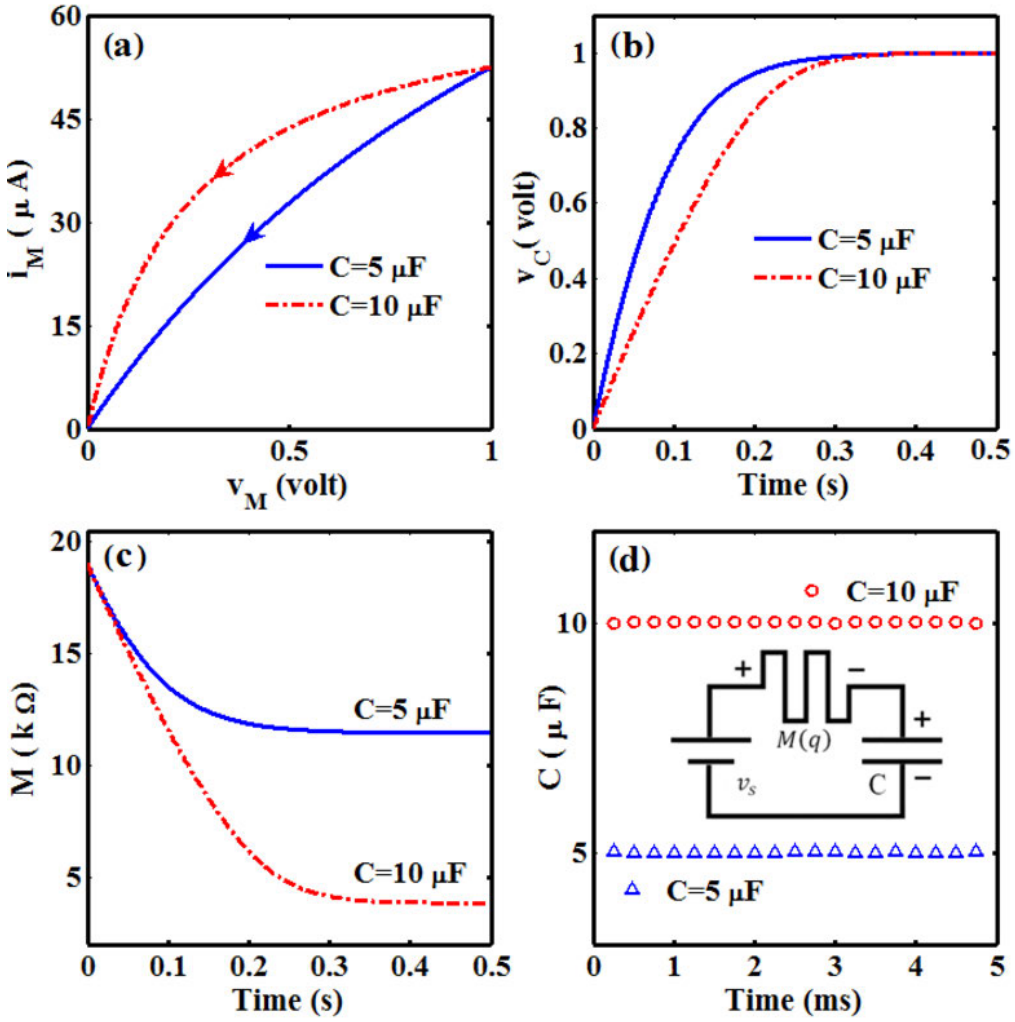

Figure 6.5.: (a) TiO_2 memristor $i - v$ curves. (b) The voltage of the capacitor and (c) the memristance as a function of time. (d) Obtained capacitances by using Eq. 6.4.

complete antiparallel alignment results in a high-resistance state (HRS; $R_{\mathrm{H}} = G_{\mathrm{L}}^{-1}$) of the device, while a fully parallel alignment places it in a low-resistance state (LRS; $R_{\mathrm{L}} = G_{\mathrm{H}}^{-1}$).

For the domain wall giant magnetoresistance (DW-GMR) the memristor $R(r)$ is given by [97]

$$\begin{aligned} R(r) = \frac{v_{\mathrm{M}}}{i_{\mathrm{M}}} &= R_{\mathrm{P}}(r) + R_{\mathrm{AP}}(r) = rR_{\mathrm{L}} + (1-r)R_{\mathrm{H}} \\ &= R_{\mathrm{H}} - r(R_{\mathrm{H}} - R_{\mathrm{L}}) = (1 - r\mathrm{GMR})R_{\mathrm{L}}, \end{aligned} \tag{6.14}$$

where x is the domain wall position, $r = x/L$ represent the relative DW position, and L denotes the length of the free layer. GMR $= (R_{\mathrm{H}} - R_{\mathrm{L}})/R_{\mathrm{L}}$ is the giant magnetoresistance ratio. According to Eq. 4.4, the electrical conductance of the domain wall tunnel magnetoresistance (DW-TMR) memristor is obtained as [138]

$$\begin{aligned} G(r) = \frac{i_{\mathrm{M}}}{v_{\mathrm{M}}} &= G_{\mathrm{P}}(r) + G_{\mathrm{AP}}(r) = rG_{\mathrm{H}} + (1-r)G_{\mathrm{L}} \\ &= (1 + r\mathrm{TMR})G_{\mathrm{L}} \end{aligned} \tag{6.15}$$

TMR $= (G_{\mathrm{H}} - G_{\mathrm{L}})/G_{\mathrm{L}}$ is the tunneling magnetoresistance ratio. The term dM/dq ($dW/d\varphi$) is obtained from Eq. 6.16 (Eq. 6.17) for the DW-GMR (DW-TMR) memristors, where V_{DW} is the DW velocity.

$$\frac{dM(q)}{dq} = \frac{dR(r)}{dr}\frac{dr}{dq} = -R_{\mathrm{L}}\mathrm{GMR}\frac{dr/dt}{dq/dt} = \frac{-R_{\mathrm{L}}\mathrm{GMR}}{L}\frac{V_{\mathrm{DW}}}{i_{\mathrm{M}}} \tag{6.16}$$

$$\frac{dW(\varphi)}{d\varphi} = \frac{dG(r)}{dr}\frac{dr}{d\varphi} = G_{\mathrm{L}}\mathrm{TMR}\frac{dr/dt}{d\varphi/dt} = \frac{G_{\mathrm{L}}\mathrm{TMR}}{L}\frac{V_{\mathrm{DW}}}{v_{\mathrm{M}}} \tag{6.17}$$

According to Eq. 6.16 (Eq. 6.17), in the DW-GMR (DW-TMR) memristor the term dM/dq ($dW/d\varphi$) is a constant and thus is suited for charge- (flux)-based measurement, if there is a linear relationship between the domain wall velocity (V_{DW}) and the current i_{M} (voltage v_{M}). It can be shown that a linear dependence of the DW velocity with respect to the applied current or voltage is expected, when the ratio

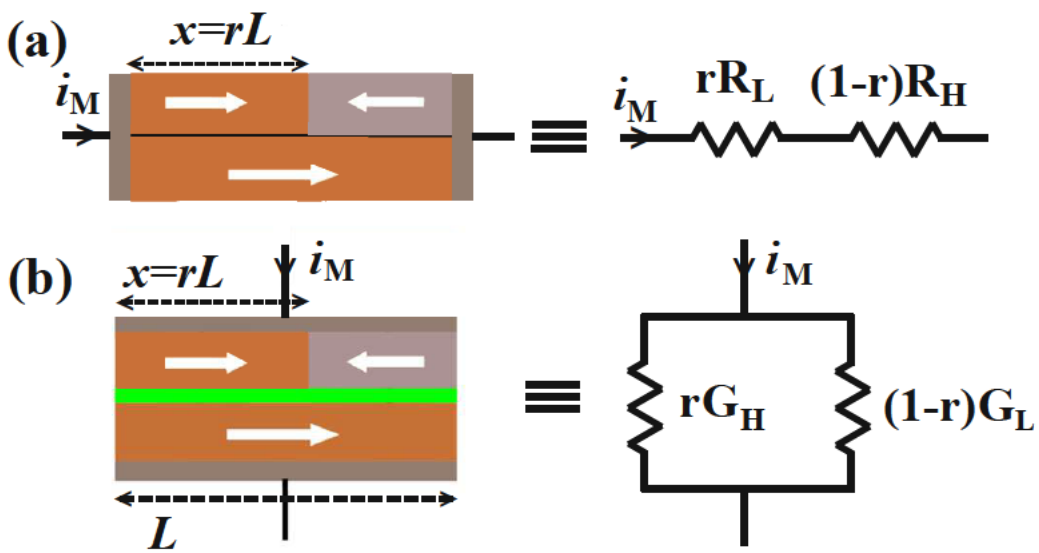

Figure 6.6.: (a) DW-GMR and (b) DW-TMR memristor structures and their equivalent circuits.

β/α is nonzero, where α is the damping parameter and β defines the strength of the non-adiabatic spin-torque [175, 176]. In fact, for $\beta = 0$ the DW exhibits a threshold current density required for current-induced motion, even when in the absence of an extrinsic pinning [171, 177]. Thus, only in the presence of non-adiabatic spin-torque ($\beta \neq 0$), the DW-GMR and the DW-TMR memristors can be used for charge- and flux-based sensing. In fact, the non-adiabatic spin-torque allows for a non-zero mobility of the DW where the mobility is proportional to the ratio β/α [211, 212]. A comprehensive interpretation of the non-adiabatic spin-torque expressed by β is still subject to controversial discussions and there are also difficulties to experimentally characterize β [175, 213–215]. In [214] experimental data shows β/α ratios of ~ 0.7 and ~ 0.6 for CoNi multilayers and FePt alloy thin films, respectively.

As an example of a spintronic capacitance sensor, Fig. 6.7a shows the average DW velocity as a function of the current passing through the DW-GMR memristor (connected in series to a capacitor as shown in Fig. 6.1a) based on the one-dimensional model of DW dynamics explained in Section 4.2.2. According to Eq. 6.16, the memristor is suited for capacitance sensing when $\beta \neq 0$. Fig. 6.7b illustrates that when the MC circuit (Fig. 6.1a) is excited by a step voltage the final domain wall position in the DW-GMR memristor and thus the memristance value is a function of the capacitance value. The sensitivity increases with the ratio β/α, but at the cost of decreased sensing range. In fact, the increase in the ratio β/α, increases the DW velocity and thus the sensitivity. It should be noted that for $\beta \neq 0$, the DW propagation is characterized by a linear regime and a nonlinear regime above the Walker breakdown [175, 216, 217]. Above a critical current value called the Walker breakdown, the DW motion becomes non-uniform (oscillatory) which is unfavorable for memristive sensing as discussed in the following.

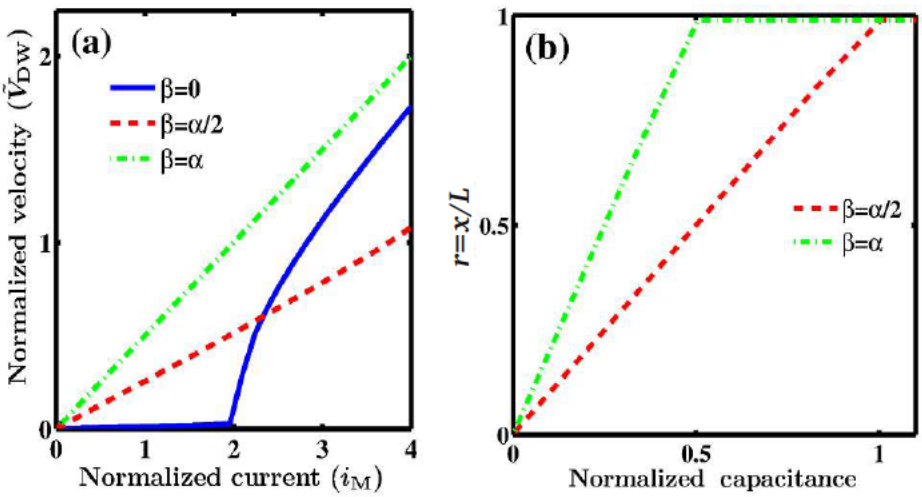

Figure 6.7.: (a) Average domain wall velocity as a function of i_M. (b) Final relative domain wall position (r) as a function of capacitance.

6.3.2.2. Magnetic Thin-Film Element

The dynamic properties of a propagating magnetic DW are strongly affected by the device geometry [218]. A magnetic thin-film (MTF) element with varying width $a(x)$ and constant thickness b (Fig. 6.8a) has been proposed as a spintronic (DW-MTF) memristor [62] based upon the STT-induced DW motion in the film-length direction x. The reaction force exerted by the domain wall to the electrons acts as the wall resistance [62]. The current-induced DW motion exhibits memristive properties, when the thin-film aspect ratio (a/b) is varying with x. Indeed, when the thickness of the device is fixed, the mobility of the DW and thus the electrical resistance of the device, becomes a function of the thin-film element width $a(x)$ and is expressed as [62]

$$R(x) = \widetilde{R}\left(\frac{a}{\widetilde{a}}\right)^{-(k+1)}, \tag{6.18}$$

where $\widetilde{R}$ and $\widetilde{a}$ are the resistance and the width of the element, respectively, when the DW is located at $\widetilde{x}$ and k determines the DW mobility scaling with the aspect ratio as $\mu \sim (a/b)^k$ [62]. Therefore, when the spatial dependence of the element width as a function of the DW position is given by

$$a(x) = \widetilde{a}\left(\frac{x}{\widetilde{x}}\right)^{\rho}, \tag{6.19}$$

the $i - v$ characteristics of the device is obtained as

$$v = R(x)i, \tag{6.20}$$

where we have [62]

$$R(x) = \widetilde{R}\left(\frac{x}{\widetilde{x}}\right)^{-\rho(k+1)}. \tag{6.21}$$

Since the dynamics of the magnetic domain wall motion (dx/dt) is a function of x and current density $(i/(a(x)b))$, the latter equation shows that this device is a memristive system (Eq. 2.14 and Eq. 2.15). For an idealistic case in which the DW velocity is proportional to the current density, the $\varphi - q$ and $q - \varphi$ constitutive relations of the domain wall magnetic thin-film (DW-MTF) memristor are determined as [62]

$$\varphi(q) = \Upsilon_1 q^{\left(\frac{1-\rho k}{\rho+1}\right)} \tag{6.22}$$

and

$$q(\varphi) = \Upsilon_2 \varphi^{\left(\frac{\rho+1}{1-\rho k}\right)}, \tag{6.23}$$

where Υ_1 and Υ_2 are constant coefficients and ρ determines the spatial dependence of the element's width on x (Eq. 6.19) [62, 173]. According to Eq. 2.10 (Eq. 2.11) and

Eq. 6.22 (Eq. 6.23), for charge (flux)-controlled DW-MTF memristor we obtain

$$\frac{dM(q)}{dq} = \frac{d^2\varphi(q)}{dq^2} = \Upsilon_1 \left(\frac{1-\rho k}{\rho+1}\right)\left(\frac{1-\rho k}{\rho+1}-1\right) q^{\left(\frac{1-\rho k}{\rho+1}-2\right)} \tag{6.24}$$

and

$$\frac{dW(\varphi)}{d\varphi} = \frac{d^2q(\varphi)}{d\varphi^2} = \Upsilon_2 \left(\frac{\rho+1}{1-\rho k}\right)\left(\frac{\rho+1}{1-\rho k}-1\right) \varphi^{\left(\frac{\rho+1}{1-\rho k}-2\right)}. \tag{6.25}$$

Therefore, in order to keep the terms dM/dq and $dW/d\varphi$ fixed, the appropriate device geometries for charge- and flux-based memristive sensing methods are (uniquely) determined by

$$\frac{dM(q)}{dq} = \text{const} \;\Rightarrow\; \frac{1-\rho k}{\rho+1} - 2 = 0 \;\Rightarrow\; \rho = -\frac{1}{k+2} \tag{6.26}$$

and

$$\frac{dW(\varphi)}{d\varphi} = \text{const} \;\Rightarrow\; \frac{\rho+1}{1-\rho k} - 2 = 0 \;\Rightarrow\; \rho = \frac{1}{2k+1}. \tag{6.27}$$

In fact, different device geometries can provide different memristive behaviors required for various sensing applications. With a spatial shape of $\rho = -1/(k+2)$ ($\rho = 1/(2k+1)$), the DW-MTF memristor is suited for charge (flux)-based sensing.

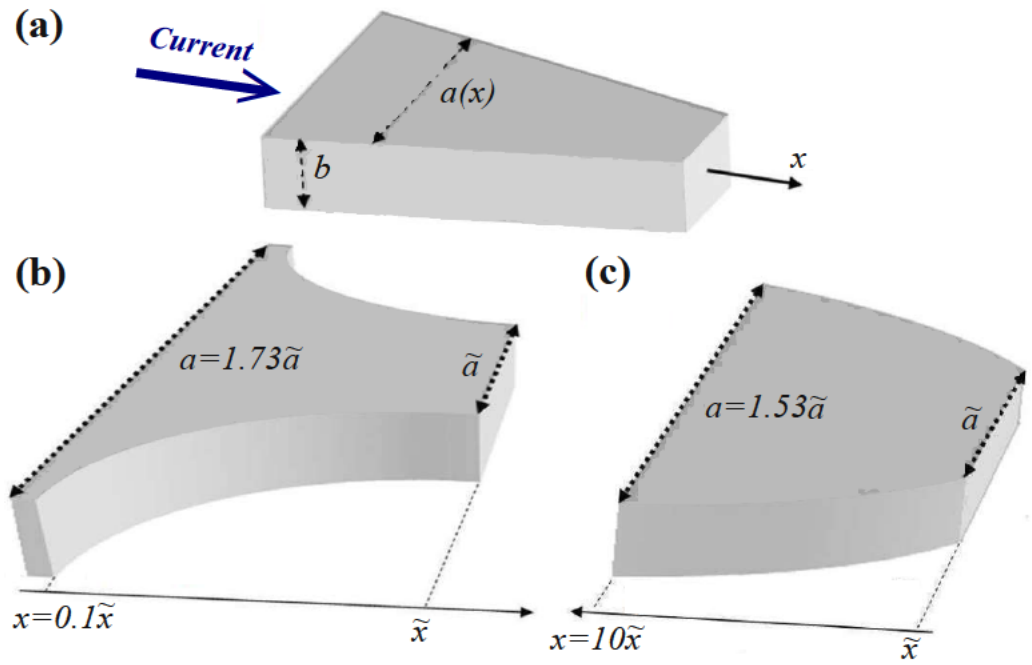

Figure 6.8.: (a) Domain wall magnetic thin-film (DW-MTF) spintronic memristor with appropriate geometries for (b) charge-based and (c) flux-based sensing.

Fig. 6.8 shows schematic geometries for memristive sensing where the parameter k is supposed equal to 2.2 [173].

Fig. 6.9 shows an example of inductance sensing by using the DW-MTF memristor with proper geometry based on Eq. 6.9. The applied current is $i_s(\omega_0 t) = i_0 u(t)$ and all axes are dimensionless, with current, memductance, voltage, time, and angular frequency normalized in units of i_0, $\widetilde{W}$, $i_0\widetilde{W}$, $2\pi\widetilde{W}\widetilde{\varphi}/i_0$, and $i_0/\widetilde{W}\widetilde{\varphi}$. $\widetilde{W}$ is the memductance when the domain wall position is $\widetilde{x}$ and $\widetilde{\varphi}$ is equal to $\widetilde{W}/2\Upsilon_2$. According to Fig. 6.9a, the memristor shows different memristive behavior for different inductances connected in parallel. Therefore, by using Eq. 6.9 (Fig. 6.9d), the amount of inductance can be calculated when the current (Fig. 6.9b) and memductance (Fig. 6.9c) modulations are known.

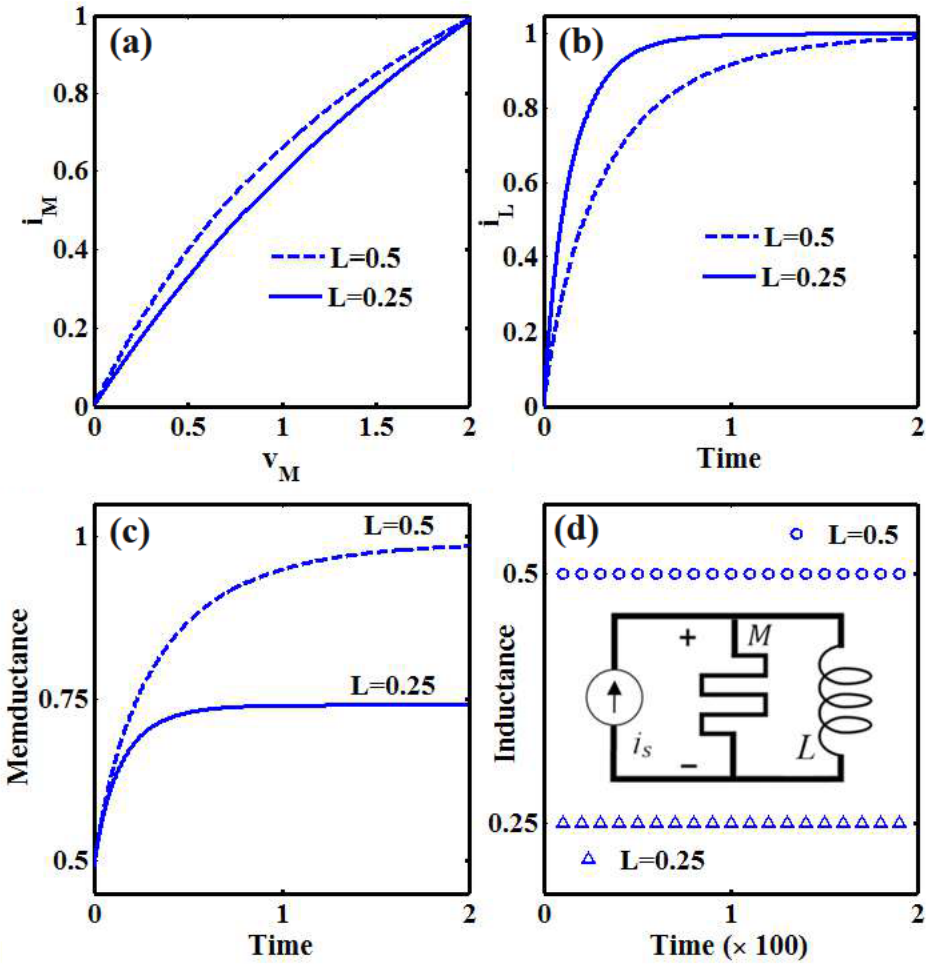

Figure 6.9.: (a) DW-MTF memristor $i-v$ curves. (b) The current flowing through the inductor and (c) the memductance as a function of time. (d) The electric circuit for flux-based inductance sensing and the obtained inductances by using Eq. 6.9.

Fig. 6.10 and Fig. 6.11 show the simulation results for memristive measurement of time-varying capacitors and inductors. The voltage v_s and current i_s sources are pulse trains with a 50% duty cycle and a magnitude of v_0 and i_0 and the capacitance and inductance are normalized by $\widetilde{q}/v_0$ and $\widetilde{\varphi}/i_0$, respectively. $\widetilde{q}$ ($\widetilde{\varphi}$) is equal to $\widetilde{M}/2\Upsilon_1$ ($\widetilde{W}/2\Upsilon_2$), where $\widetilde{M}$ ($\widetilde{W}$) corresponds to the memristance (memductance) when domain wall is located at $\widetilde{x}$. By sampling i_M and v_M the capacitance (inductance) can be calculated using Eq. 6.4 (Eq. 6.9). Fig. 6.12 shows a DW-MTF memristor structure suited for both capacitance and inductance sensing. The term dM/dq ($dW/d\varphi$) is constant for $x < \widetilde{x}$ ($x > \widetilde{x}$) and the corresponding memristance and memductance are shown in Fig. 6.13.

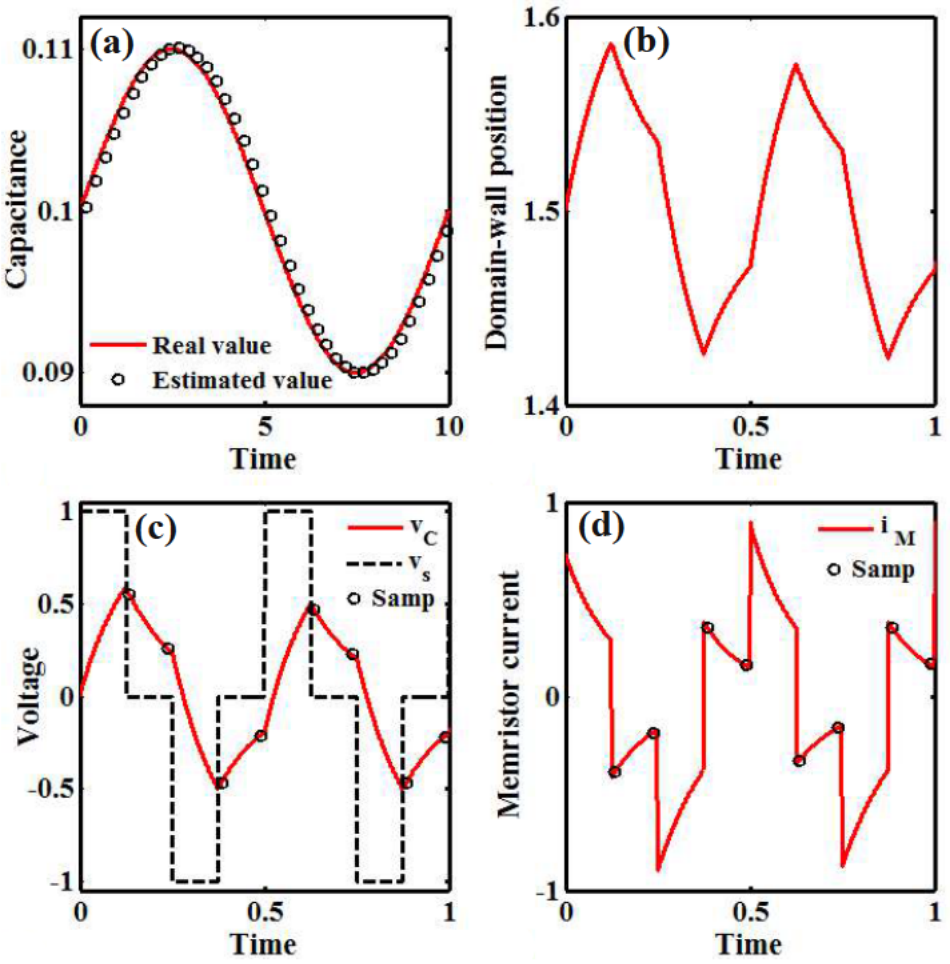

Figure 6.10.: (a) Time-varying capacitance and memristive measurement results. (b) The domain wall position and (c) the source voltage v_s and the voltage across the capacitor v_C and (d) the current flowing through the memristor i_M with respect to time.

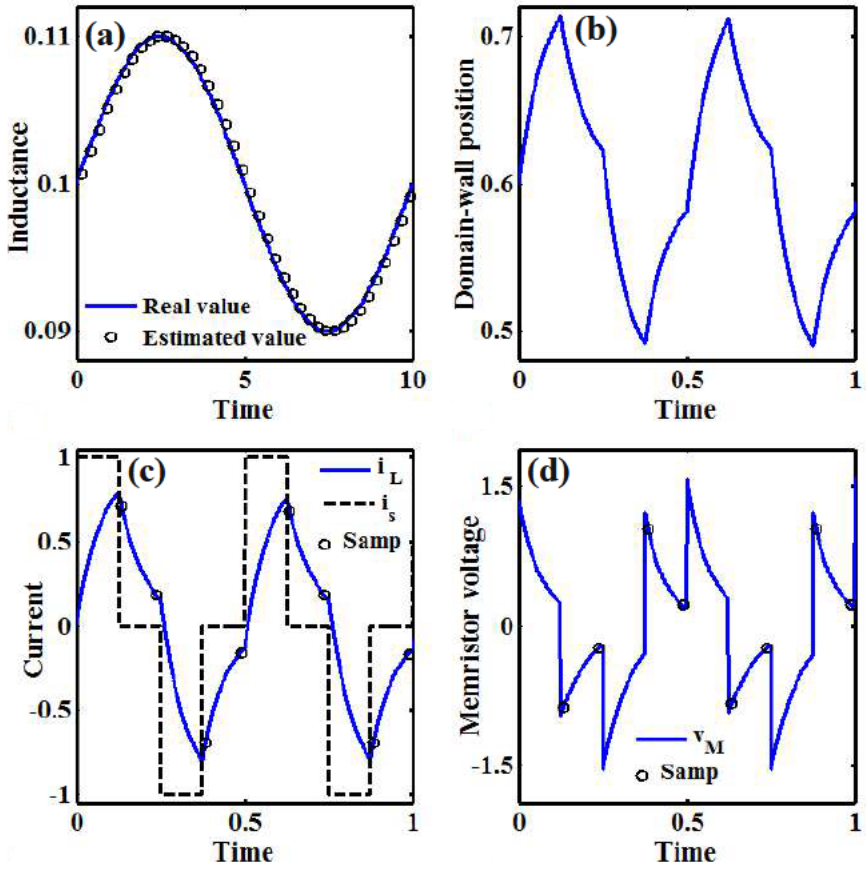

Figure 6.11.: (a) Time-varying inductance and memristive measurement results. (b) The domain wall position and (c) the source current i_s and the current flowing through the inductor i_L and (d) the voltage of the memristor v_M with respect to time.

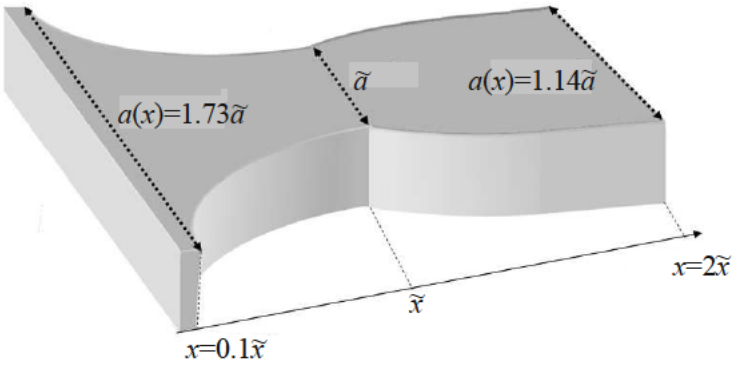

Figure 6.12.: Proposed DW-MTF memristor structure for simultaneous capacitance and inductance sensing.

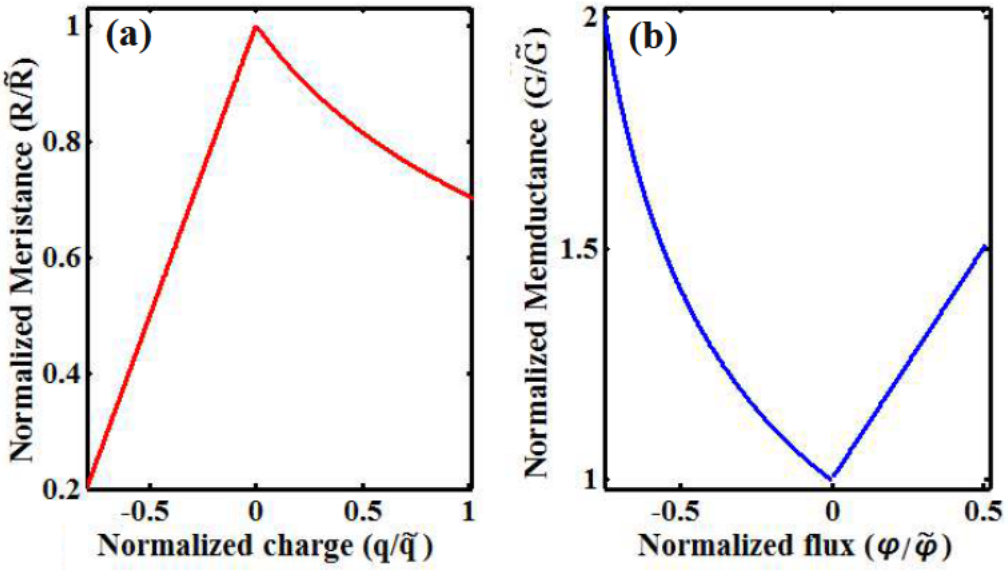

Figure 6.13.: (a) $M(q)$ as a function of charge and (b) $W(\varphi)$ as a function of flux for the DW-MTF memristor structure shown in Fig. 6.12.

6.3.3. Domain Wall Dynamics

In order to take a closer look at the DW dynamics in a patterned structure, the one-dimensional model of DW dynamics (Section 4.2.2) is employed to analyze the DW-MTF-based memristive sensing. The dynamic properties of a propagating magnetic DW are strongly affected by the device geometry [218]. The varying width of the DW-MTF element (Fig. 6.12) is taken into account by assuming the current density and the number of spins ($N(x) = a(x)\widetilde{N}/\widetilde{a}$) in the DW [171] as a function of the DW position x. Therefore, Eq. 4.8 is solved for $j(x) = \widetilde{j}\left(\frac{\widetilde{a}}{a(x)}\right) = \widetilde{j}\left(\frac{\widetilde{x}}{x}\right)^{\rho}$ and $M_{\mathrm{s}}(x) = \widetilde{M_{\mathrm{s}}}\left(\frac{a(x)}{\widetilde{a}}\right) = \widetilde{M_{\mathrm{s}}}\left(\frac{\widetilde{x}}{x}\right)^{-\rho}$.

Fig. 6.14 shows the geometry dependence of the DW dynamics for zero and nonzero non-adiabatic spin-torque values. In the absence of the non-adiabatic term (Fig. 6.14a), there is a geometry dependent threshold current required to move a DW. Therefore, for the currents below a current threshold the memristive behavior can not be observed. In the presence of the non-adiabatic term (Fig. 6.14b), the average DW velocity increases linearly with the applied current for low current values. Therefore, with $\beta \neq 0$, the memristive behavior is observed and with proper geometry, the device can be used for memristive sensing. Above a (geometry dependent) critical current corresponding to the Walker breakdown [175, 216, 217], the DW motion shows complex behaviors. Therefore, the memristive sensing has to be performed in a low current regime, which for a given sensing resolution, increases the sensing time.

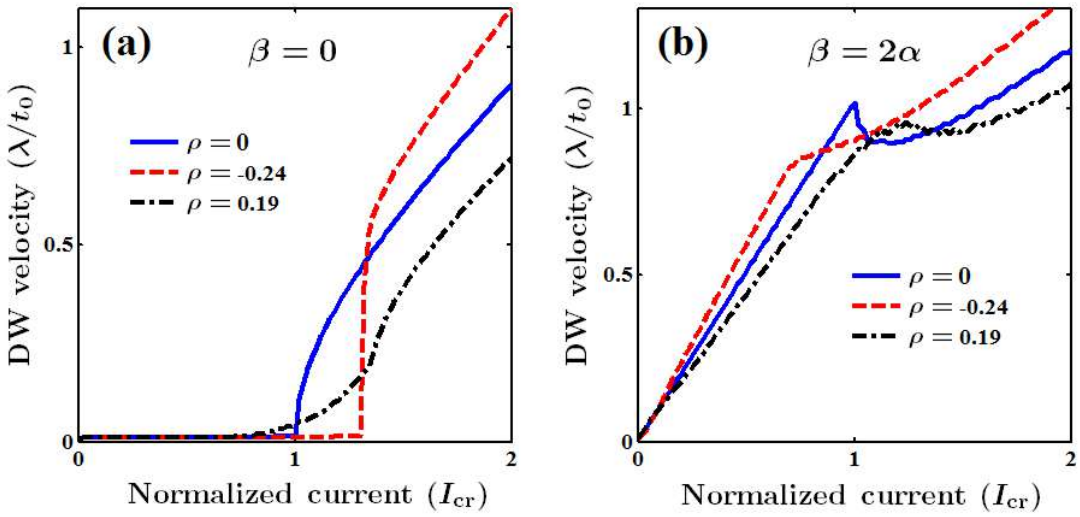

Figure 6.14.: Time-averaged domain wall velocity (a) in the absence and (b) in the presence of the non-adiabatic spin-torque effect plotted for different geometrical structures (ρ).

6.4. Sensitivity

The sensitivity of the memristive charge (flux)-based sensing scheme is determined by the value of the memristance (memductance) modulation with respect to the charge (flux) applied to the memristor. The amount of charge needed to pass through the memristor to change the memristance from its minimum to its maximum value for the TiO_2 memristor is relatively high and is in the range of tens to hundreds of microcoulombs for a nanometer-scale motion of the doping front as the mobility of dopants (oxygen vacancies) in the TiO_2 thin film is quite low ($\sim 10^{-10}\text{cm}^2\text{s}^{-1}\text{V}^{-1}$ [70]). However, it turns out that it is in the range of nanocoulombs to picocoulombs in the spintronic memristors for a micrometer-scale motion of the magnetic domain wall (extracted from data presented in [95,172,173]) Therefore, the memristive sensor based on the TiO_2 memristors can measure capacitances in the range of to microfarad to nanofarad. Because spin-based memristors can be more finely tuned compared to the TiO_2 memristor [65,168], they are promising for measuring capacitances of 3-6 orders of magnitude smaller than that measured by using the TiO_2 memristor. Nano-scale feature size, low cost and the integration capabilities are other advantages of spintronic memristors [97].

6.5. Summary

Novel charge- and flux-based memristive sensing schemes are presented based on the unique property of memristors to memorize the charge (time integral of current) and the flux (time integral of voltage). The proposed methods can be used for capacitance, inductance, and power measurements. Although inductance and capacitance sensing are far from being new problems, the use of a memristor reduces the measurement to a straightforward resistance measurement which can be performed fast. We have shown that the TiO_2 memristor can be used for charge-based measurements. Spintronic memristors are proposed for both charge- and flux-based capacitance and inductance measurement. The effect of the device geometry on the memristive behavior of a spintronic device is studied to determine proper geometries for memristive charge- and flux-based sensing. In the presence of the non-adiabatic spin-torque effect, the spintronic memristor shows memristive behaviors at low current/voltage regimes and within the desired geometries the device has a constant modulation of the memristance (memductance) with respect to the charge (flux) applied, which can be used for capacitance (inductance) measurement or both. Spintronic memristors show 3-6 orders of magnitude higher sensitivities compared to the TiO_2 memristor devices.

Since the memristor holds the information, it is possible to use the memristor in a readout circuit which measures the memristance and also resets the memristor for the next measurement. Thus, unlike other time domain methods, memristive sensing does not need extra hardware for time/frequency measurement. In fact, a memristive sensor can be simply implemented by using a switch. Furthermore, memristor devices are fabricated in nano-scale dimension and this makes memristors a candidate for low power micro-system applications. The memristive sensing method is suitable for measuring time-varying inductances and capacitances and it has the potential to be used in novel inductive and capacitive sensors. For example, the simplest form of a capacitor consists of two metal plates, separated by an insulator and the capacitance is expressed as $C = \varepsilon_0 \varepsilon_r A/d$ where ε_0 denotes the permittivity of free space, ε_r is the dielectric constant of the insulating material between the plates, A express the area of the plates, and d is the distance between the plates. The capacitance changes, if at least one of the parameters ε_r, A, or d is changed. By measuring the capacitance periodically, any movement of the plates or changing in the dielectric constant (e.g. due to a finger-touch on the dielectric) can be measured or detected. Due to the non-volatility, zero-leakage, high endurance, and small cell size of the memristors, memristive sensing is promising for ultra-low power capacitive (e.g. touch) sensors.

7. Conclusions and Outlook

TiO_2-based and spintronic memristive devices as well as implication and reprogrammable circuit topologies are potential candidates as the basic (latch/gate) building blocks of the stateful logic systems. TiO_2-based memristive implication logic gates are studied based on a nonlinear memristor device model which successfully takes into account the dynamic switching behavior and the nonlinearities observed in TiO_2 memristive devices. The gates are optimized to minimize the state drift error accumulations and to ensure correct implication logic behavior for different input patterns. It is shown that the use of refreshing circuitry after a limited number of logic steps (10–20 steps) is unavoidable due to the state drift errors accumulated in sequential logic steps. This is very unfavorable as it needs extra hardware and increases complexity. Furthermore, limited endurance is still a major challenge for metal/oxide/metal technology to be used as universal memory cells or computing devices.

Spintronic memristive devices, especially the tunnel magnetoresistance (TMR)-based devices, show almost unlimited endurance and sufficiently high resistance modulation. In addition, spintronic devices provide a very fine level of control and faster switching compared to the TiO_2 memristive devices which exhibit a very low mobility of dopants in the TiO_2 thin film. It is shown that the implication logic operation can be implemented based on domain wall (DW) TMR memristive devices, with the DW position serving as state variable. This enables stateful logic operations that extends spintronics from non-volatile memory to logic applications, for which the spintronic memristor serves simultaneously as a logic gate and a latch. However, similar to the TiO_2-implication gate, the DW-TMR-based gate also suffers from the state drift error accumulation.

The spin-transfer torque magnetic tunnel junction (STT-MTJ) is proposed as a very favorable device for stateful implication logic as it inherently eliminates the state drift error accumulation due to its magnetic bistability. Furthermore, it has a great potential, because of its CMOS compatibility, scalability, unlimited endurance, and fast switching speed. A new improved current-controlled gate topology is proposed for STT-MTJ-based implication logic. Reliability modeling and analysis is presented for optimizing and comparing the STT-MTJ-based logic gates. It is demonstrated that the proposed implication gate provides a more energy-efficient and reliable implementation as compared to the conventional (voltage-controlled) implication gate topology. It is also demonstrated that the implication logic framework based on the proposed gate topology significantly improves the reliability of the MTJ-based logic compared to the

earlier proposed reprogrammable logic framework which is based on common Boolean logic operations including AND, OR, et cetera.

STT-MRAM-based logic architectures are presented to facilitate the generalization of the MTJ logic gates to large-scale non-volatile logic circuits. The asymmetry issue of the proposed implication logic gate is addressed by exploiting the access transistors of one-transistor/one-MTJ cells not only as on-off switches but also as voltage-controlled resistor. Therefore, the functionality of the STT-MRAM circuit is extended to include stateful logic operations with no extra hardware added. STT-MRAM stateful logic provides non-volatile logic fan-out, exhibits high flexibility with regard to the delocalized computations execution, and eliminates the need for intermediate circuitry. It also enables parallel non-volatile computations and, therefore, it is suited for large-scale logic applications and opens an alternative path towards zero-standby power logic systems, shifting away from the Von Neumann architecture. It is shown that for the intrinsic (N)AND and (N)OR operations, the reprogrammable gate requires slightly less power than the corresponding implication-based implementation. Besides the fact that the MRAM-based implication logic enables a more reliable logic behavior as compared to the reprogrammable gates, it outperforms the reprogrammable gate for more complex logic functions and is thus the implementation of choice for large-scale logic circuits. Through design examples like fundamental arithmetic functions, the advantages of the MRAM-based stateful logic implementation are described and the possible tradeoffs to optimize the execution time, the energy consumption, and the reliability of the MRAM-based stateful logic architectures are also investigated. It is also shown that, at the cost of reduced reliability, a combined reprogrammable-implication logic architecture reduces the total number of the logic steps and thus the energy consumptions.

The MRAM-based stateful logic via the improved implication logic gate is based on STT-MRAM memory technology which has already been commercialized. However, an experimental demonstration of the improved implication logic gate is still missing. Because of the already reported successful fabrication of the reprogrammable gates, on one hand, and improved reliability of the novel implication gate demonstrated in the thesis, on the other hand, we believe that the fabrication of this novel gate is quite feasible. As it is shown in this work, the reliability is an essential prerequisite of the MTJ-based logic circuits. We demonstrated that the reliability increases almost exponentially with the TMR ratio and the thermal stability factor of the MTJ. Due to the strong ongoing efforts towards improving the STT-MRAM technology, these parameters keep increasing which results in higher reliability. It is demonstrated that, independent of the MTJ switching regime, the improved implication logic gate intrinsically provides a more reliable conditional switching behavior as compared to the reprogrammable gate. Nevertheless, future work may involve the investigation of the level of superiority of the implication gate in subnanosecond (precessional) MTJ switching regime. This is of interest to explore limits and to inquire design tradeoffs in very high-speed MTJ logic architectures. At the architecture level, investigating

general methods to design Boolean logic functions based on the basic implication logic operations with minimized logic steps is another necessary future research direction.

The novel functional properties of emerging memristive devices have the potential to lead applications beyond non-volatile memory and logic. The last part of the thesis describes novel charge- and flux-based memristive sensing schemes based on the unique property of memristors to record the time integral of the applied current or voltage signals. The proposed method reduces the capacitance, inductance, and power measurements to a straightforward resistance measurement. Spintronic memristive devices are proposed for both charge- and flux-based capacitance and inductance measurement. The effect of the device geometry on the memristive behavior of a spintronic device caused by the dynamic properties of a propagating magnetic domain wall is studied. Particular geometries corresponding to appropriate memristive characteristics are exploited for charge- and flux-based sensing applications. It is shown that in the presence of the non-adiabatic spin-transfer torque, the spintronic memristor exhibits a constant modulation of the memristance (memductance) with respect to the charge (flux) and can be used for capacitance (inductance) measurement. The memristive sensing method is also suited for novel ultra-low leakage capacitive and inductive sensor applications in nano-scale. For example, the capacitance changes due to any movement of the capacitor plates or a change in the dielectric constant (e.g. due to a finger-touch) can be measured or detected in future memristive capacitive sensors.

Appendix A.

Implication-Based Full Adder

A full adder adds three binary inputs (a_1, a_2, and c_{in}) and has two outputs, sum (s) and carry (c_{out}) given by

$$s = a_1 \text{ XOR } a_2 \text{ XOR } c_{\text{in}} \tag{A.1}$$

and

$$\begin{aligned} c_{\text{out}} &= (a_1 \text{ AND } a_2) \text{ OR } (c_{\text{in}} \text{ AND } [a_1 \text{ XOR } a_2]) \\ &\equiv (a_1 \text{ AND } a_2) \text{ OR } (c_{\text{in}} \text{ AND } [a_1 \text{ OR } a_2]). \end{aligned} \tag{A.2}$$

In implication-based logic systems the realized logic operation is equivalent to the operation IMP or NIMP depending on the logical definitions for the high and low resistance states as explained in Table 3.2). Here the detailed implementations of a stateful full adder using the MRAM implication logic arrays are presented.

Table A.1.: Full adder truth table.

a_1	a_2	c_{in}	s	c_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A.1. NIMP-Based Full Adder

$$
\begin{aligned}
&\text{TRUE} : a_3 = 1 \\
&\text{NIMP} : \overline{a_3 \rightarrow a_1} \equiv \{a_3' = a_3.\overline{a_1} = \overline{a_1}\} \\
&\text{TRUE} : a_4 = 1 \\
&\text{NIMP} : \overline{a_4 \rightarrow a_2} \equiv \{a_4' = a_4.\overline{a_2} = \overline{a_2}\} \\
&\text{NIMP} : \overline{a_4 \rightarrow a_3} \equiv \{a_4' = a_4.\overline{a_3} = \overline{a_2}.a_1\} \\
&\text{NIMP} : \overline{a_2 \rightarrow a_1} \equiv \{a_2' = a_2.\overline{a_1}\} \\
&\text{TRUE} : a_5 = 1 \\
&\text{NIMP} : \overline{a_5 \rightarrow a_2} \equiv \{a_5' = a_5.\overline{a_2} = \overline{a_2} + a_1\} \\
&\text{NIMP} : \overline{a_5 \rightarrow a_4} \equiv \{a_5' = a_5.\overline{a_4} = (\overline{a_2} + a_1).(a_2 + \overline{a_1}) \equiv \overline{a_1 \text{ XOR } a_2}\} \\
&\text{NIMP} : \overline{a_3 \rightarrow a_2} \equiv \{a_3' = a_3.\overline{a_2} = \overline{a_1}.\overline{a_2}\} \\
&\text{NIMP} : \overline{a_1 \rightarrow a_4} \equiv \{a_1' = a_1.\overline{a_4} = a_1.a_2\} \\
&\text{TRUE} : a_4 = 1 \\
&\text{NIMP} : \overline{a_4 \rightarrow c_{\text{in}}} \equiv \{a_4' = a_4.\overline{c_{\text{in}}} = \overline{c_{\text{in}}}\} \\
&\text{NIMP} : \overline{c_{\text{in}} \rightarrow a_3} \equiv \{c_{\text{in}}' = c_{\text{in}}.\overline{a_3} = c_{\text{in}}.(a_1 + a_2)\} \\
&\text{TRUE} : a_3 = 1 \\
&\text{NIMP} : \overline{a_3 \rightarrow a_1} \equiv \{a_3' = a_3.\overline{a_1} = \overline{a_1.a_2}\} \\
&\text{NIMP} : \overline{a_3 \rightarrow c_{\text{in}}} \equiv \{a_3' = a_3.\overline{c_{\text{in}}} = (\overline{a_1.a_2}).\left(\overline{c_{\text{in}}.(a_1 + a_2)}\right) \equiv \overline{c_{\text{out}}}\} \\
&\text{TRUE} : a_1 = 1 \\
&\text{NIMP} : \overline{a_1 \rightarrow a_3} \equiv \{a_1' = a_1.\overline{a_3} = c_{\text{out}}\} \\
&\text{TRUE} : a_2 = 1 \\
&\text{NIMP} : \overline{a_2 \rightarrow a_4} \equiv \{a_2' = a_2.\overline{a_4} = c_{\text{in}}\} \\
&\text{TRUE} : a_3 = 1 \\
&\text{NIMP} : \overline{a_3 \rightarrow a_5} \equiv \{a_3' = a_3.\overline{a_5} = a_1 \text{ XOR } a_2\} \\
&\text{NIMP} : \overline{a_3 \rightarrow a_2} \equiv \{a_3' = a_3.\overline{a_2} = (a_1 \text{ XOR } a_2).\overline{c_{\text{in}}}\} \\
&\text{NIMP} : \overline{a_5 \rightarrow a_4} \equiv \{a_5' = a_5.\overline{a_4} = c_{\text{in}}.\overline{(a_1 \text{ XOR } a_2)}\} \\
&\text{TRUE} : a_2 = 1 \\
&\text{NIMP} : \overline{a_2 \rightarrow a_3} \equiv \{a_2' = a_2.\overline{a_3} = \overline{(a_1 \text{ XOR } a_2)} + c_{\text{in}}\} \\
&\text{NIMP} : \overline{a_2 \rightarrow a_5} \equiv \{a_2' = a_2.\overline{a_5} = \left(\overline{(a_1 \text{ XOR } a_2)} + c_{\text{in}}\right).(\overline{c_{\text{in}}} + (a_1 \text{ XOR } a_2))\} \\
&\text{TRUE} : a_4 = 1 \\
&\text{NIMP} : \overline{a_4 \rightarrow a_2} \equiv \{a_4' = a_4.\overline{a_2} = ((a_1 \text{ XOR } a_2).\overline{c_{\text{in}}}).\left(c_{\text{in}}.\overline{(a_1 \text{ XOR } a_2)}\right)\} \\
&\qquad\qquad \equiv \{a_4' = c_{\text{in}} \text{ XOR } a_1 \text{ XOR } a_2 \equiv s\} \qquad \text{(A.3)}
\end{aligned}
$$

A.2. IMP-Based Full Adder

$$
\begin{aligned}
&\text{FALSE} : a_3 = 0 \\
&\quad \text{IMP} : a_1 \rightarrow a_3 \equiv \{a_3' = \overline{a_1} + a_3 = \overline{a_1}\} \\
&\text{FALSE} : a_4 = 0 \\
&\quad \text{IMP} : a_2 \rightarrow a_4 \equiv \{a_4' = \overline{a_2} + a_4 = \overline{a_2}\} \\
&\quad \text{IMP} : a_3 \rightarrow a_4 \equiv \{a_4' = \overline{a_3} + a_4 = a_1 + \overline{a_2}\} \\
&\text{FALSE} : a_5 = 0 \\
&\quad \text{IMP} : a_4 \rightarrow a_5 \equiv \{a_5' = \overline{a_4} + a_5 = \overline{a_1}.a_2\} \\
&\text{FALSE} : a_4 = 0 \\
&\quad \text{IMP} : a_2 \rightarrow a_4 \equiv \{a_4' = \overline{a_2} + a_4 = \overline{a_2}\} \\
&\quad \text{IMP} : a_4 \rightarrow a_3 \equiv \{a_3' = \overline{a_4} + a_3 = a_2 + \overline{a_1}\} \\
&\quad \text{IMP} : a_3 \rightarrow a_5 \equiv \{a_5' = \overline{a_3} + a_5 = \overline{a_2}.a_1 + \overline{a_1}.a_2 \equiv a_1 \text{ XOR } a_2\} \\
&\quad \text{IMP} : a_1 \rightarrow a_4 \equiv \{a_4' = \overline{a_1} + a_4 = \overline{a_1} + \overline{a_2}\} \\
&\text{FALSE} : a_1 = 0 \\
&\quad \text{IMP} : a_5 \rightarrow a_1 \equiv \{a_1' = \overline{a_5} + a_1 = \overline{a_1 \text{ XOR } a_2}\} \\
&\quad \text{IMP} : c_{\text{in}} \rightarrow a_1 \equiv \{a_1' = \overline{c_{\text{in}}} + a_1 = \overline{c_{\text{in}}} + \overline{a_1 \text{ XOR } a_2}\} \\
&\text{FALSE} : a_2 = 0 \\
&\quad \text{IMP} : a_1 \rightarrow a_2 \equiv \{a_1' = \overline{a_1} + a_2 = c_{\text{in}}.(a_1 \text{ XOR } a_2)\} \\
&\quad \text{IMP} : a_4 \rightarrow a_2 \equiv \{a_4' = \overline{a_4} + a_2 = (a_1.a_2) + c_{\text{in}}.(a_1 \text{ XOR } a_2) \equiv c_{\text{out}}\}
\end{aligned}
$$

$$
\begin{aligned}
&\text{FALSE} : a_3 = 0 \\
&\quad \text{IMP} : c_{\text{in}} \rightarrow a_3 \equiv \{a_3' = \overline{c_{\text{in}}} + a_3 = \overline{c_{\text{in}}}\} \\
&\text{FALSE} : a_1 = 0 \\
&\quad \text{IMP} : a_5 \rightarrow a_1 \equiv \{a_1' = \overline{a_5} + a_1 = \overline{a_1 \text{ XOR } a_2}\} \\
&\quad \text{IMP} : a_3 \rightarrow a_1 \equiv \{a_1' = \overline{a_3} + a_1 = c_{\text{in}} + \overline{a_1 \text{ XOR } a_2}\} \\
&\text{FALSE} : a_3 = 0 \\
&\quad \text{IMP} : a_1 \rightarrow a_3 \equiv \{a_3' = \overline{a_1} + a_3 = \overline{c_{\text{in}}}.(a_1 \text{ XOR } a_2)\} \\
&\quad \text{IMP} : c_{\text{in}} \rightarrow a_5 \equiv \{a_5{}' = \overline{c_{\text{in}}} + a_5 = \overline{c_{\text{in}}} + a_1 \text{ XOR } a_2 \\
&\quad \text{IMP} : a_5 \rightarrow a_3 \equiv \{a_5' = \overline{a_5} + a_3 = c_{\text{in}}.(\overline{a_1 \text{ XOR } a_2}) + \overline{c_{\text{in}}}.(a_1 \text{ XOR } a_2)\} \\
&\qquad\qquad \equiv \{a_5' = c_{\text{in}} \text{ XOR } a_1 \text{ XOR } a_2 \equiv s\} \qquad \text{(A.4)}
\end{aligned}
$$

Bibliography

[1] International Technology Roadmap for Semiconductors (ITRS), Chapter PIDS, 2011. [Online]. Available: http://www.itrs.net/

[2] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, "Limits to Binary Logic Switch Scaling - a Gedanken Model," *Proc. IEEE*, vol. 91, pp. 1934–1939, 2003.

[3] N. S. Kim, T. Austin, D. Baauw, T. Mudge, K. Flautner, J. S. Hu, M. J. Irwin, M. Kandemir, and V. Narayanan, "Leakage Current: Moore's Law Meets the Static Power," *Computer*, vol. 36, pp. 68–75, 2003.

[4] K. Rupp and S. Selberherr, "The Economic Limit to Moore's Law," *Proc. IEEE*, vol. 98, pp. 351–353, 2010.

[5] J. Gautier, "Beyond CMOS: Quantum Devices," *Microelec. Engin.*, vol. 39, pp. 263–272, 1997.

[6] J. A. Hutchby, G. I. Bourianoff, V. V. Zhirnov, and J. E. Brewer, "Extending the Road Beyond CMOS," *Circuits and Devices Magazine, IEEE*, vol. 18, pp. 28–41, 2002.

[7] G. I. Bourianoff, P. A. Gargini, and D. E. Nikonov, "Research Directions in Beyond CMOS Computing," *Solid-State Electron.*, vol. 51, pp. 1426–1431, 2007.

[8] R. Huang, H. Wu, J. Kang, D. Xiao, X. Shi, X. An, Y. Tian, R. Wang, L. Zhang, X. Zhang, and Y. Wang, "Challenges of 22nm and Beyond CMOS Technology," *Sci. China F: Inf. Sci.*, vol. 52, pp. 1491–1533, 2009.

[9] D. Bouvet, L. Forró, A. M. Ionescu, Y. Leblebici, A. Magrez, K. E. Moselund, G. A. Salvatore, N. Setter, and I. Stolitchnov, "Materials and Devices for Nanoelectronic Systems Beyond Ultimately Scaled CMOS," in *Nanosystems Design and Technology*. Springer, 2009, pp. 23–44.

[10] A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond-CMOS Logic," *Proc. IEEE*, vol. 98, pp. 2095–2110, 2010.

[11] B. Dellabetta and M. J. Gilbert, "Performance Characteristics of Strongly Correlated Bilayer Graphene for Post-CMOS Logic Devices," *Proceedings of Silicon Nanoelectron. Workshop, DOI: 10.1109/SNW.2010.5562544*, pp. 1–2, 2010.

[12] S. K. Banerjee, L. F. Register, E. Tutuc, D. Basu, S. Kim, D. Reddy, and A. H. MacDonald, "Graphene for CMOS and Beyond CMOS Applications," *Proceedings of the IEEE*, vol. 98, pp. 2032–2046, 2010.

[13] K. Bernstein, R. K. Cavin, W. Porod, A. Seabaugh, and J. Welser, "Device and Architecture Outlook for Beyond CMOS Switches," *Proceedings of the IEEE*, vol. 98, pp. 2169–2184, 2010.

[14] V. Sverdlov, *Strain-Induced Effects in Advanced MOSFETs*, S. Selberherr, Ed. Springer-Verlag, Wien - New York, 2011.

[15] D. E. Nikonov and I. A. Young, "Overview of Beyond-CMOS Devices and a Uniform Methodology for Their Benchmarking," *Proc. IEEE*, vol. 101, pp. 2498–2533, 2013.

[16] S. A. Wolf, D. D. Awschalom, R. A. Buhrman, J. M. Daughton, S. V. Molnar, M. L. Roukes, A. Y. Chtchelkanova, and D. M. Treger, "Spintronics: a Spin-Based Electronics Vision for the Future," *Science*, vol. 294, pp. 1488–1495, 2001.

[17] D. D. Awschalom, D. Loss, and N. Samarth, *Semiconductor Spintronics and Quantum Computation*. Springer, 2002.

[18] D. D. Awschalom, M. E. Flatté, and N. Samarth, "Spintronics," *Scientific American*, vol. 286, pp. 66–73, 2002.

[19] A. Ney, C. Pampuch, R. Koch, and K. H. Ploog, "Programmable Computing with a Single Magnetoresistive Element," *Nature*, vol. 425, pp. 485–487, 2003.

[20] I. Žutić, J. Fabian, and S. D. Sarma, "Spintronics: Fundamentals and Applications," *Rev. Mod. Phys.*, vol. 76, p. 323, 2004.

[21] M. Fuhrer, "Spintronics: A Path to Spin Logic," *Nat. Phys.*, vol. 1, pp. 85–86, 2005.

[22] C. Chappert, A. Fert, and F. N. V. Dau, "The Emergence of Spin Electronics in Data Storage," *Nat. Mater.*, vol. 6, pp. 813–823, 2007.

[23] Y. Huai, "Spin-Transfer Torque MRAM (STT-MRAM): Challenges and Prospects," *AAPPS Bull.*, vol. 18, pp. 33–40, 2008.

[24] A. Fert, "Nobel Lecture: Origin, Development, and Future of Spintronics," *Rev. Mod. Phys.*, vol. 80, p. 1517, 2008.

[25] L. Bogani and W. Wernsdorfer, "Molecular Spintronics Using Single-Molecule Magnets," *Nat. Mater.*, vol. 7, pp. 179–186, 2008.

[26] B. Behin-Aein, D. Datta, S. Salahuddin, and S. Datta, "Proposal for an All-Spin Logic Device with Built-in Memory," *Nat. Nanotechnol.*, vol. 5, pp. 266–270, 2010.

[27] S. Sanvito, "Molecular Spintronics," *Chem. Soc. Rev.*, vol. 40, pp. 3336–3355, 2011.

[28] R. Jansen, "Silicon Spintronics," *Nat. Mater.*, vol. 11, pp. 400–408, 2012.

[29] G. H. Fecher, *Spintronics: From Materials to Devices*. Springer, 2013.

[30] M. N. Baibich, J. M. Broto, A. Fert, F. N. V. Dau, F. Petroff, P. Etienne, G. Creuzet, A. Friederich, and J. Chazelas, "Giant Magnetoresistance of (001)Fe/(001)Cr Magnetic Superlattices," *Phys. Rev. Lett.*, vol. 61, pp. 2472–2475, 1988.

[31] G. Binash, P. Grünberg, F. Saurenbach, and W. Zinn, "Enhanced Magnetoresistance in Layered Magnetic Structures with Antiferromagnetic Interlayer Exchange," *Phys. Rev. B*, vol. 39, pp. 4828–4830, 1989.

[32] H. Fujimori, S. Mitani, and S. Ohnuma, "Tunnel-Type GMR in Metal-Nonmetal Granular Alloy Thin Films," *Mater. Scien. and Engin. B*, vol. 31, pp. 219–223, 1995.

[33] S. Yuasa, T. Nagahama, A. Fukushima, Y. Suzuki, and K. Ando, "Giant Room-Temperature Magnetoresistance in Single-Crystal Fe/MgO/Fe Magnetic Tunnel Junctions," *Nat. Mater.*, vol. 3, pp. 868–871, 2004.

[34] S. S. P. Parkin, C. Kaiser, A. Panchula, P. M. Rice, B. Hughes, M. Samant, and S.-H. Yang, "Giant Tunnelling Magnetoresistance at Room Temperature with MgO (100) Tunnel Barriers," *Nat. Mater.*, vol. 3, pp. 862–867, 2004.

[35] B. N. Engel, J. Akerman, B. Butcher, R. W. Dave, M. DeHerrera, M. Durlam, G. Grynkewich, J. Janesky, S. V. Pietambaram, N. D. Rizzo, J. M. Slaughter, K. Smith, J. J. Sun, and S. Tehrani, "A 4-Mb Toggle MRAM Based on a Novel Bit and Switching Method," *IEEE Trans. Magn.*, vol. 41, pp. 132–136, 2005.

[36] J.-G. J. Zhu and C. Park, "Magnetic Tunnel Junctions," *Materials Today*, vol. 9, pp. 36–45, 2006.

[37] S. Ikeda, J. Hayakawa, Y. M. Lee, F. Matsukura, Y. Ohno, T. Hanyu, and H. Ohno, "Magnetic Tunnel Junctions for Spintronic Memories and Beyond," *IEEE Trans. Electron Devices*, vol. 54, pp. 991–1002, 2007.

[38] E. Chen, D. Apalkov, Z. Diao, A. Driskill-Smith, D. Druist, D. Lottis, V. Nikitin, X. Tang, S. Watts, S. Wang, S. Wolf, A. Ghosh, J. Lu, S. Poon, M. Stan, W. Butler, S. Gupta, C. Mewes, T. Mewes, and P. Visscher, "Advances and Future Prospects of Spin-Transfer Torque Random Access Memory," *IEEE Trans. Magn.*, vol. 46, pp. 1873–1878, 2010.

[39] C. Augustine, N. Mojumder, X. Fong, H. Choday, S. P. Park, and K. Roy, "STT-MRAMs for Future Universal Memories: Perspective and Prospective," *Proceedings of the 28th International Conference on Microelectronics (MIEL)*, pp. 349–355, 2012.

[40] K. L. Wang, J. G. Alzate, and P. K. Amiri, "Low-Power Non-Volatile Spintronic Memory: STT-RAM and Beyond," *J. Phys. D: Appl. Phys.*, vol. 46, p. 074003, 2013.

[41] T. Miyazaki, T. Yaoi, and S. Ishio, "Large Magnetoresistance Effect in 82Ni-Fe/Al-Al_2O_3/Co Magnetic Tunneling Junction," *J. Magn. and Magn. Mater.*, vol. 98, pp. L7–L9, 1991.

[42] T. S. Plaskett, P. P. Freitas, N. P. Barradas, M. F. D. Silva, and J. C. Soares, "Magnetoresistance and Magnetic Properties of NiFe/Oxide/Co Junctions Prepared by Magnetron Sputtering," *J. Appl. Phys.*, vol. 76, pp. 6104–6106, 1994.

[43] T. Miyazaki and N. Tezuka, "Giant Magnetic Tunneling Effect in Fe/Al_2O_3/Fe Junction," *J. Magn. and Magn. Mater.*, vol. 139, pp. L231–L234, 1995.

[44] J. C. Slonczewski, "Current-Driven Excitation of Magnetic Multilayers," *J. Magn. and Magn. Mater.*, vol. 159, pp. L1–L7, 1996.

[45] L. Berger, "Emission of Spin Waves by a Magnetic Multilayer Traversed by a Current," *Phys. Rev. B, Condens. Matter*, vol. 54, pp. 9353–9358, 1996.

[46] E. B. Myers, D. C. Ralph, J. A. Katine, R. N. Louie, and R. A. Buhrman, "Current-Induced Switching of Domains in Magnetic Multilayer Devices," *Science*, vol. 285, pp. 867–870, 1999.

[47] R. H. Koch, J. A. Katine, and J. Z. Sun, "Time-Resolved Reversal of Spin-Transfer Switching in a Nanomagnet," *Phys. Rev. Lett.*, vol. 92, p. 088302, 2004.

[48] Y. Huai, F. Albert, P. Nguyen, M. Pakala, and T. Valet, "Observation of Spin-Transfer Switching in Deep Submicron-Sized and Low-Resistance Magnetic Tunnel Junctions," *Appl. Phys. Lett.*, vol. 84, pp. 3118–3120, 2004.

[49] G. D. Fuchs, N. C. Emley, I. N. Krivorotov, P. M. Braganca, E. M. Ryan, S. I. Kiselev, J. C. Sankey, D. C. Ralph, R. A. Buhrman, and J. A. Katine, "Spin-Transfer Effects in Nanoscale Magnetic Tunnel Junctions," *Appl. Phys. Lett.*, vol. 85, pp. 1205–1207, 2004.

[50] M. Hosomi, H. Yamagishi, T. Yamamoto, K. Bessho, Y. Higo, K. Yamane, H. Yamada, M. Shoji, H. Hachinoa, C. Fukumoto, H. Nagao, and H. Kano, "A Novel Nonvolatile Memory with Spin Torque Transfer Magnetization Switching: Spin-RAM," *Tech. Dig. - Int. Electron Devices Meet. (IEDM)*, pp. 459–462, 2005.

[51] W. H. Kautz, "Cellular Logic-in-Memory Arrays," *IEEE Trans. Comput.*, vol. 100, pp. 719–727, 1969.

[52] J. G. Wang, H. Meng, and J. P. Wang, "Programmable Spintronics Logic Device Based on a Magnetic Tunnel Junction Element," *J. Appl. Phys.*, vol. 97, p. 10D509, 2005.

[53] W. Zhao, E. Belhaire, C. Chappert, F. Jacquet, and P. Mazoyer, "New Non-Volatile Logic Based on Spin-MTJ," *Phys. Status Solidi (a)*, vol. 205, pp. 1373–1377, 2008.

[54] S. Matsunaga, J. Hayakawa, S. Ikeda, K. Miura, H. Hasegawa, T. Endoh, H. Ohno, and T. Hanyu, "Fabrication of a Nonvolatile Full Adder Based on Logic-in-Memory Architecture Using Magnetic Tunnel Junctions," *Appl. Phys. Express*, vol. 1, p. 091301, 2008.

[55] A. Lyle, J. Harms, S. Patil, X. Yao, D. Lilja, and J. P. Wang, "Direct Communication Between Magnetic Tunnel Junctions for Nonvolatile Logic Fan-out Architecture," *Appl. Phys. Lett.*, vol. 97, p. 152504, 2010.

[56] A. Lyle, S. Patil, J. Harms, B. Glass, X. Yao, D. Lilja, and J. P. Wang, "Magnetic Tunnel Junction Logic Architecture for Realization of Simultaneous Computation and Communication," *IEEE Trans. Magn.*, vol. 47, pp. 2970–2973, 2011.

[57] D. E. Nikonov, G. I. Bourianoff, , and T. Ghan, "Proposal of a Spin Torque Majority Gate Logic," *IEEE Electron Device Lett.*, vol. 32, pp. 1128–1130, 2011.

[58] Y. Gang, W. Zhao, J. O. Klein, C. Chappert, and P. Mazoyer, "A High-Reliability, Low-Power Magnetic Full Adder," *IEEE Trans. Magn.*, vol. 47, pp. 4611–4616, 2011.

[59] X. Yao, J. Harms, A. Lyle, F. Ebrahimi, Y. Zhang, and J. P. Wang, "Magnetic Tunnel Junction-Based Spintronic Logic Units Operated by Spin Transfer Torque," *IEEE Trans. Nanotechnol.*, vol. 11, pp. 120–126, 2012.

[60] M. Natsui, D. Suzuki, N. Sakimura, R. Nebashi, Y. Tsuji, A. Morioka, T. Sugibayashi, S. Miura, H. Honjo, K. Kinoshita, S. Ikeda, T. Endoh, H. Ohno, and T. Hanyu, "Nonvolatile Logic-in-Memory Array Processor in 90nm MTJ/MOS Achieving 75% Leakage Reduction Using Cycle-Based Power Gating," *Proceedings of the International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 194–195, 2013.

[61] Y. V. Pershin and M. D. Ventra, "Spin Memristive Systems: Spin Memory Effects in Semiconductor Spintronics," *Phys. Rev. B*, vol. 78, p. 113309, 2008.

[62] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "Spintronic Memristor Through Spin-Torque-Induced Magnetization Motion," *IEEE Electron Device Lett.*, vol. 30, pp. 294–297, 2009.

[63] P. Krzysteczko, G. Reiss, and A. Thomas, "Memristive Switching of MgO Based Magnetic Tunnel Junctions," *Appl. Phys. Lett.*, vol. 95, p. 112508, 2009.

[64] H.-J. Jang, O. A. Kirillov, O. D. Jurchescu, and C. A. Richter, "Spin Transport in Memristive Devices," *Appl. Phys. Lett.*, vol. 100, p. 043510, 2012.

[65] A. Chanthbouala, R. Matsumoto, J. Grollier, V. Cros, A. Anane, A. Fert, A. V. Khvalkovskiy, K. A. Zvezdin, K. Nishimura, Y. Nagamine, H. Maehara, K. Tsunekawa, A. Fukushima, and S. Yuasa, "Vertical-Current-Induced Domain-Wall Motion in MgO-Based Magnetic Tunnel Junctions with Low Current Densities," *Nat. Phys.*, vol. 7, pp. 626–630, 2011.

[66] J. Grollier, A. Chanthbouala, R. Matsumoto, A. Anane, V. Cros, F. N. van Dau, and A. Fert, "Magnetic Domain Wall Motion by Spin Transfer," *Comptes Rendus Physique*, vol. 12, pp. 309–317, 2011.

[67] W. Cai, T. Schmidt, U. Jorges, and F. Ellinger, "A Feedback Spin-Valve Memristive System," *IEEE Trans. Circuits Syst. I*, vol. 59, pp. 2405–2412, 2012.

[68] Q. Li, T.-T. Shen, Y.-L. Cao, K. Zhang, S.-S. Yan, Y.-F. Tian, S.-S. Kang, M.-W. Zhao, Y.-Y. Dai, Y.-X. Chen, G.-L. Liu, L.-M. Mei, X.-L. Wang, and P. Grünberg, "Spin Memristive Magnetic Tunnel Junctions with CoO-ZnO Nano Composite Barrier," *Scientific Reports*, vol. 4, p. 3835, 2014.

[69] L. O. Chua, "Memristor-The Missing Circuit Element," *IEEE Trans. Circuit Theory*, vol. 18, pp. 507–519, 1971.

[70] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The Missing Memristor Found," *Nature*, vol. 453, no. 7191, pp. 80–83, 2008.

[71] L. O. Chua and S. M. Kang, "Memristive Devices and Systems," *Proceedings of the IEEE*, vol. 64, pp. 209–223, 1976.

[72] L. O. Chua, "Resistance Switching Memories are Memristors," *Appl. Phys. A*, vol. 102, no. 4, pp. 765–783, 2011.

[73] ——, "If Its Pinched It's a Memristor," in *Memristors and Memristive Systems*. Springer New York, 2014, pp. 17–90.

[74] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, and R. S. Williams, "Memristor-CMOS Hybrid Integrated Circuits for Reconfigurable Logic," *Nano Lett.*, vol. 9, pp. 3640–3645, 2009.

[75] J. Borghetti, Z. Li, J. Straznicky, X. Li, D. A. Ohlberg, W. Wu, D. R. Stewart, and R. S. Williams., "A Hybrid Nanomemristor/Transistor Logic Circuit Capable of Self-Programming," *Proc. of the Natl. Acad. of Sci.*, vol. 106, pp. 1699–1703, 2009.

[76] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "Memristive Switches Enable Stateful Logic Operations via Material Implication," *Nature*, vol. 464, pp. 873–876, 2010.

[77] X. Sun, G. Li, L. Ding, N. Yang, and W. Zhang, "Unipolar Memristors Enable Stateful Logic Operations via Material Implication," *Appl. Phys. Lett.*, vol. 99, p. 072101, 2011.

[78] S. Shin, K. Kim, and S. Kang, "Reconfigurable Stateful NOR Gate for Large-Scale Logic-Array Integrations," *IEEE Trans. Circuits Syst. II*, vol. 58, pp. 442–446, 2011.

[79] S. Shin, K. Kim, and S.-M. Kang, "Memristive XOR for Resistive Multiplier," *Electron. Lett.*, vol. 48, pp. 78–80, 2012.

[80] J. Rajendran, H. Manem, R. Karri, and G. S. Rose, "An Energy-Efficient Memristive Threshold Logic Circuit," *IEEE Trans. Comput.*, vol. 61, pp. 474–487, 2012.

[81] S. Shin, K. Kim, and S.-M. Kang, "Resistive Computing: Memristors-Enabled Signal Multiplication," *IEEE Trans. Circuits Syst. I*, vol. 60, pp. 1241–1249, 2013.

[82] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive Devices for Computing," *Nat. Nanotechnol.*, vol. 8, pp. 13–24, 2013.

[83] D. Fan, M. Sharad, and K. Roy, "Design and Synthesis of Ultra Low Energy Spin-Memristor Threshold Logic," *arXiv preprint arXiv:1402.2648*, 2014.

[84] Y. V. Pershin, S. L. Fontaine, and M. D. Ventra, "Memristive Model of Amoeba Learning," *Phys. Rev. E*, vol. 80, no. 2, p. 021926 (6 pp), 2009.

[85] Y. V. Pershin and M. D. Ventra, "Experimental Demonstration of Associative Memory with Memristive Neural Networks," *Neur. Netw.*, vol. 23, pp. 881–886, 2010.

[86] S. Jo, T. Chang, I. Ebong, B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale Memristor Device as Synapse in Neuromorphic Systems," *Nano Lett.*, vol. 10, pp. 1297–1301, 2010.

[87] P. Krzysteczko, J. Münchenberger, M. Schäfers, G. Reiss, and A. Thomas, "The Memristive Magnetic Tunnel Junction as a Nanoscopic Synapse-Neuron System," *Adv. Mater.*, vol. 24, pp. 762–766, 2012.

[88] R. Kozma, R. E. Pino, and G. E. Pazienza, *Advances in Neuromorphic Memristor Science and Applications*. Springer New York, 2012.

[89] F. Alibart, S. Pleutin, O. Bichler, C. Gamrat, T. Serrano-Gotarredona, B. Linares-Barranco, and D. Vuillaume, "A Memristive Nanoparticle/Organic Hybrid Synapstor for Neuroinspired Computing," *Adv. Func. Mater.*, vol. 22, pp. 609–616, 2012.

[90] G. D. Howard, L. Bull, B. D. L. Costello, E. Gale, and A. Adamatzky, "Evolving Memristive Neural Networks," in *Memristor Networks*. Springer International Publishing, 2014, pp. 293–322.

[91] Y. Chen, H. Li, and Z. Sun, "Spintronic Memristor as Interface Between DNA and Solid State Devices," in *Memristors and Memristive Systems*. Springer New York, 2014, pp. 281–298.

[92] Y. N. Joglekar and S. J. Wolf, "The Elusive Memristor: Properties of Basic Electrical Circuits," *Eur. J. Phys.*, vol. 30, pp. 661–675, 2009.

[93] Y. V. Pershin, E. Sazonov, and M. D. Ventra, "Analogue-to-Digital and Digital-to-Analogue Conversion with Memristive Devices," *Electron. Lett.*, vol. 48, pp. 73–74, 2012.

[94] A. Ascoli, R. Tetzlaff, F. Corinto, M. Mirchev, and M. Gilli, "Memristor-Based Filtering Applications," *Proceedings of the 14th IEEE Latin-American Test Workshop*, pp. 1–6, 2013.

[95] X. Wang, Y. Chen, G. Ying, and H. Li, "Spintronic Memristor Temperature Sensor," *IEEE Electron Device Lett.*, vol. 31, pp. 20–22, 2010.

[96] X. Bi, C. Zhang, H. Li, Y. Chen, and R. E. Pino, "Spintronic Memristor Based Temperature Sensor Design with CMOS Current Reference," *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pp. 1301–1306, 2012.

[97] X. Wang and Y. Chen, "Spintronic Memristor Devices and Application," *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pp. 667–672, 2010.

[98] M. Itoh and L. O. Chua, "Memristor Oscillators," *Int. J. Bifu. Chaos*, vol. 18, pp. 3183–3206, 2008.

[99] B. Mouttet, "Proposal for Memristors in Signal Processing," *In Nano-net 2008*, vol. 58, pp. 11–13, 2009.

[100] S. Shin, K. Kim, and S. Kang, "Memristor-Based Fine Resolution Programmable Resistance and its Applications," *Proceedings of the International Conference on Communications, Circuits and Systems*, pp. 948–951, 2009.

[101] Y. V. Pershin and M. D. Ventra, "Practical Approach to Programmable Analog Circuits With Memristors," *IEEE Trans. Circuits Syst. I*, vol. 57, pp. 1857–1864, 2010.

[102] H. H.-C. Iu, D. S. Yu, A. L. Fitch, V. Sreeram, and H. Chen, "Controlling Chaos in a Memristor Based Circuit Using a Twin-T Notch Filter," *IEEE Trans. Circuits Syst. I*, vol. 58, pp. 1337–1344, 2011.

[103] T. Wey and W. Jemison, "An Automatic Gain Control Circuit with TiO_2 Memristor Variable Gain Amplifier," *Anal. Dig. Sign. Proc.*, vol. 73, pp. 663–672, 2012.

[104] F. Argall, "Switching Phenomena in Titanium Oxide Thin Films," *Solid-State Electron.*, vol. 11, pp. 535–541, 1968.

[105] S. Seo, M. J. Lee, D. H. Seo, E. J. Jeoung, D.-S. Suh, Y. S. Joung, I. K. Yoo, I. R. Hwang, S. H. Kim, I. S. Byun, J.-S. Kim, J. S. Choi, , and B. H. Park, "Reproducible Resistance Switching in Polycrystalline NiO Films," *Appl. Phys. Lett.*, vol. 85, pp. 5655–5657, 2004.

[106] B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, "Resistive Switching Mechanism of TiO_2 Thin Films Grown by Atomic-Layer Deposition," *J. Appl. Phys.*, vol. 98, p. 033715, 2005.

[107] K. Szot, W. Speier, G. Bihlmayer, and R. Waser, "Switching the Electrical Resistance of Individual Dislocations in Single-Crystalline $SrTiO_3$," *Nat. Mater.*, vol. 5, pp. 312–320, 2006.

[108] B. J. Choi, J. J. Yang, M.-X. Zhang, K. J. Norris, D. A. A. Ohlberg, N. P. Kobayashi, G. Medeiros-Ribeiro, and R. S. Williams, "Nitride Memristors," *Appl. Phys. A*, vol. 109, pp. 1–4, 2012.

[109] Z. Wang, P. B. Griffin, J. McVittie, S. Wong, P. C. McIntyre, and Y. Nishi, "Resistive Switching Mechanism in $Zn_xCd_{1-x}S$ Nonvolatile Memory Devices," *IEEE Electron Device Lett.*, vol. 28, pp. 14–16, 2007.

[110] T. Sakamoto, K. Lister, N. Banno, T. Hasegawa, K. Terabe, and M. Aono, "Electronic Transport in Ta_2O_5 Resistive Switch," *Appl. Phys. Lett.*, vol. 91, p. 092110, 2007.

[111] W. Guan, M. Liu, S. Long, Q. Liu, and W. Wang, "On the Resistive Switching Mechanisms of Cu/ZrO_2:Cu/Pt," *Appl. Phys. Lett.*, vol. 93, p. 223506, 2008.

[112] C. Chen, Y. C. Yang, F. Zeng, and F. Pan, "Bipolar Resistive Switching in Cu/AlN/Pt Nonvolatile Memory Device," *Appl. Phys. Lett.*, vol. 97, p. 083502, 2010.

[113] R. Huang, L. Zhang, D. Gao, Y. Pan, S. Qin, P. Tang, Y. Cai, and Y. Wang, "Resistive Switching of Silicon-Rich-Oxide Featuring High Compatibility with CMOS Technology for 3D Stackable and Embedded Applications," *Appl. Phys. A*, vol. 102, pp. 927–931, 2011.

[114] W. Lu, D. S. Jeong, M. Kozicki, and R. Waser, "Electrochemical Metallization Cells-Blending Nanoionics into Nanoelectronics?" *Mater. Res. Soc. Bull.*, vol. 37, pp. 124–130, 2012.

[115] J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive Switching Mechanism for Metal/Oxide/Metal Nanodevices," *Nat. Nanotechnol.*, vol. 3, pp. 429–433, 2008.

[116] J. Münchenberger, G. Reiss, and A. Thomas, "A Memristor Based on Current-Induced Domain-Wall Motion in a Nanostructured Giant Magnetoresistance Device," *J. Appl. Phys.*, vol. 111, p. 07D303, 2012.

[117] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, M. Bibes, A. Barthélémy, and J. Grollier, "A Ferroelectric Memristor," *Nat. Mater.*, vol. 11, pp. 860–864, 2012.

[118] T. Driscoll, H.-T. Kim, B.-G. Chae, M. D. Ventra, and D. N. Basov, "Phase-Transition Driven Memristive System," *Appl. Phys. Lett.*, vol. 95, p. 043503, 2009.

[119] H.-S. Wong, S. Raoux, S. Kim, J. Liang, J. P. Reifenberg, B. Rajendran, M. Asheghi, and K. E. Goodson, "Phase Change Memory," *Proceedings of the IEEE*, vol. 98, pp. 2201–2227, 2010.

[120] A. Ukil, "Memristance View of Piezoelectricity," *IEEE Sensors J.*, vol. 11, pp. 2514–2517, 2011.

[121] F. Meng, L. Jiang, K. Zheng, C. F. Goh, S. Lim, H. H. Hng, J. Ma, F. Boey, and X. Chen, "Protein-Based Memristive Nanodevices," *Small*, vol. 7, pp. 3016–3020, 2011.

[122] A. W. Bushmaker, C.-C. Chang, V. V. Deshpande, M. Amer, M. W. Bockrath, and S. B. Cronin, "Memristive Behavior Observed in a Defected Single-Walled Carbon Nanotube," *IEEE Trans. Nanotechnol.*, vol. 10, pp. 582–586, 2011.

[123] E. Kyriakides, C. Hadjistassou, and J. Georgiou, "A New Memristor Based on NiTi Smart Alloys," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1403–1406, 2012.

[124] J. Georgiou, E. Kyriakides, and C. Hadjistassou, "NiTi Smart Alloys for Memristors with Multi-Time-Scale Volatility," *Electron. Lett.*, vol. 48, pp. 877–879, 2012.

[125] F. Corinto, A. Ascoli, and M. Gilli, "A Novel Elementary Memristive System," *Proceedings of the 20st IEEE/IFIP International Conference on VLSI and System-on-Chip (VLSI-SoC)*, pp. 76–81, 2012.

[126] D. Liu, H. Cheng, X. Zhu, G. Wang, and N. Wang, "Analog Memristors Based on Thickening/Thinning of Ag Nanofilaments in Amorphous Manganite Thin Films," *ACS Appl. Mater. Interfaces*, vol. 5, pp. 11 258–11 264, 2013.

[127] A. Emboras, I. Goykhman, B. Desiatov, N. Mazurski, L. Stern, J. Shappir, and U. Levy, "Nanoscale Plasmonic Memristor with Optical Readout Functionality," *Nano Lett.*, vol. 13, pp. 6151–6155, 2013.

[128] D. Sacchetto, Y. Leblebici, and G. D. Micheli, "Silicon Nanowire-Based Memristive Devices," in *Memristors and Memristive Systems*. Springer New York, 2014, pp. 253–280.

[129] M. Yang, N. Qin, L. Z. Ren, Y. J. Wang, K. G. Yang, F. M. Yu, W. Q. Zhou, S. X. W. M. Meng, D. H. Bao, and S. W. Li, "Realizing a Family of Transition-Metal-Oxide Memristors Based on Volatile Resistive Switching at a Rectifying Metal/Oxide Interface," *J. of Phys. D: Appl. Phys.*, vol. 47, p. 045108, 2014.

[130] S. Benderli and T. A. Wey, "On SPICE Macromodelling of TiO_2 Memristors," *Electron. Lett.*, vol. 45, pp. 377–379, 2009.

[131] Ádam Rák and G. Cserey, "Macromodelling of the Memristor in SPICE," *IEEE Trans. Computer-Aided Design*, vol. 29, pp. 632–636, 2010.

[132] V. Biolkova, Z. Kolka, Z. Biolek, and D. Biolek, "Memristor Modeling Based on Its Constitutive Relation," *Proceedings of the European Conference of Systems, and European Conference of Circuits Technology and Devices, and European Conference of Communications, and European Conference on Computer Science*, pp. 261–264, 2010.

[133] S. Shin, K. Kim, and S. Kang, "Compact Models for Memristors Based on Charge-Flux Constitutive Relationships," *IEEE Trans. Computer-Aided Design*, vol. 29, pp. 590–598, 2010.

[134] D. Batas and H. Fiedler, "A Memristor SPICE Implementation and a New Approach for Magnetic Flux-Controlled Memristor Modeling," *IEEE Trans. Nanotechnol.*, vol. 10, pp. 250–255, 2011.

[135] J. T. Diao and X. B. Tian, "A Simulation Method for Memristor Based Dopant Drift Model," *Appl. Mechan. and Mater.*, vol. 239, pp. 915–920, 2013.

[136] Y. Chen and X. Wang, "Compact Modeling and Corner Analysis of Spintronic Memristor," *Proceedings of the IEEE/ACM International Symposium on Nanoscale Architectures*, pp. 7–12, 2009.

[137] H. H. Li and M. Hu, "Compact Model of Memristors and Its Application in Computing Systems," *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pp. 673–678, 2010.

[138] M. Hu, H. Li, Y. Chen, X. Wang, and R. Pino, "Geometry Variations Analysis of TiO_2 Thin-Film and Spintronic Memristors," *ASP-DAC*, pp. 23–30, 2011.

[139] M. D. Pickett, D. B. Strukov, J. L. Borghetti, J. J. Yang, G. S. Snider, D. R. Stewart, and R. S. Williams, "Switching Dynamics in Titanium Dioxide Memristive Devices," *J. Appl. Phys.*, vol. 106, p. 074508, 2009.

[140] H. Abdalla and M. D. Pickett, "SPICE Modeling of Memristors," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1832–1835, 2011.

[141] F. Z. Wang, N. Helian, S. Wu, M.-G. Lim, Y. Guo, and M. A. Parker, "Delayed Switching in Memristors and Memristive Systems," *IEEE Electron Device Lett.*, vol. 31, pp. 755–757, 2010.

[142] C. Yakopcic, T. M. Taha, G. Subramanyam, R. E. Pino, and S. Rogers, "A Memristor Device Model," *IEEE Electron Device Lett.*, vol. 32, pp. 1436–1438, 2011.

[143] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "TEAM: ThrEshold Adaptive Memristor Model," *IEEE Trans. Circuits Syst. I*, vol. 60, pp. 211–221, 2013.

[144] Y. V. Pershin and M. D. Ventra, "SPICE Model of Memristive Devices with Threshold," *Radioengineering*, no. 2, 2013.

[145] S. H. Jo, K.-H. Kim, and W. Lu, "Programmable Resistance Switching in Nanoscale Two-Terminal Devices," *Nano Lett.*, vol. 9, pp. 496–500, 2008.

[146] S. C. Chae, J. S. Lee, S. Kim, S. B. Lee, S. H. Chang, C. Liu, B. Kahng, H. Shin, D.-W. Kim, C. U. Jung, S. Seo, M.-J. Lee, and T. W. Noh, "Random Circuit Breaker Network Model for Unipolar Resistance Switching," *Adv. Mater.*, vol. 20, pp. 1154–1159, 2008.

[147] R. L. McCreery and A. J. Bergren, "Progress with Molecular Electronic Junctions: Meeting Experimental Challenges in Design and Fabrication," *Adv. Mater.*, vol. 21, pp. 4303–4322, 2009.

[148] D. B. Strukov, J. L. Borghetti, and R. S. Williams, "Protein-Based Memristive Nanodevices," *Small*, vol. 5, pp. 1058–1063, 2009.

[149] D. Strukov and R. S. Williams, "Exponential Ionic Drift: Fast Switching and Low Volatility of a Thin-Film Memristors," *Appl. Phys. A*, vol. 94, pp. 515–519, 2009.

[150] G. Medeiros-Ribeiro, F. Perner, R. Carter, H. Abdalla, M. D. Pickett, and R. S. Williams, "Lognormal Switching Times for Titanium Dioxide Bipolar Memristors: Origin and Resolution," *Nanotechnol.*, vol. 22, p. 095702, 2011.

[151] J. J. Yang, F. Miao, M. D. Pickett, D. A. Ohlberg, D. R. Stewart, C. N. Lau, and R. S. Williams, "The Mechanism of Electroforming of Metal Oxide Memristive Switches," *Nanotechnol.*, vol. 20, p. 215201, 2009.

[152] N. Gergel-Hackett, B. Hamadani, B. Dunlap, J. Suehle, C. Richter, C. Hacker, and D. Gundlach, "A Flexible Solution-Processed Memristor," *IEEE Electron Device Lett.*, vol. 30, pp. 706–708, 2009.

[153] D.-H. Kwon, K. M. Kim1, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, "Atomic Structure of Conducting Nanofilaments in TiO_2 Resistive Switching Memory," *Nat. Nanotechnol.*, vol. 5, pp. 148–153, 2010.

[154] J. P. Strachan, M. D. Pickett, J. J. Yang, S. Aloni, A. L. D. Kilcoyne, G. Medeiros-Ribeiro, and R. S. Williams, "Direct Identification of the Conducting Channels in a Functioning Memristive Device," *Adv. Mater.*, vol. 22, pp. 3573–3577, 2010.

[155] F. Miao, J. J. Yang, J. Borghetti, G. Medeiros-Ribeiro, and R. S. Williams, "Observation of Two Resistance Switching Modes in TiO_2 Memristive Devices Electroformed at Low Current," *Nanotechnol.*, vol. 22, p. 254007, 2011.

[156] J. L. Tedesco, L. Stephey, M. Hernandez-Mora, C. A. Richter, and N. Gergel-Hackett, "Switching Mechanisms in Flexible Solution-Processed TiO_2 Memristors," *Nanotechnol.*, vol. 23, p. 305206, 2012.

[157] Z. Fan, X. Fan, A. Li, and L. Dong, "In Situ Forming, Characterization, and Transduction of Nanowire Memristors," *Nanoscale*, vol. 5, pp. 12 310–12 315, 2013.

[158] Y. Yang and W. Lu, "Nanoscale Resistive Switching Devices: Mechanisms and Modeling," *Nanoscale*, vol. 5, pp. 10 076–10 092, 2013.

[159] M. K. Hota, M. K. Bera, and C. K. Maiti, "Switching Mechanism in Au Nanodot-Embedded Nb_2O_5 Memristors," *J. Nanosc. Nanotech.*, vol. 14, pp. 3538–3544, 2014.

[160] G. J. Simmons, "Generalized Formula for the Electric Tunnel Effect between Similar Electrodes Separated by a Thin Insulating Film," *J. Appl. Phys.*, vol. 34, pp. 1793–1803, 1963.

[161] A. Whitehead and B. Russell, *Principia Mathematica*. Cambridge at the University Press, 1910.

[162] C. E. Shannon, *A Symbolic Analysis of Relay and Switching Circuits*. Master's thesis, MIT, 1940.

[163] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based IMPLY Logic Design Procedure," *Proc. IEEE Int. Conf. Comput. Design*, pp. 142–147, 2011.

[164] Z. Wei, Y. Kanzawa, K. Arita, Y. Katoh, K. Kawai, S. Muraoka, S. Mitani, S. Fujii, K. Katayama, M. Iijima, T. Mikawa, T. Ninomiya, R. Miyanaga, Y. Kawashima, K. Tsuji, A. Himeno, T. Okada, R. Azuma, K. Shimakawa, H. Sugaya, I. Takagi, R. Yasuhara, K. Horiba, H. Kumigashira, and M. Oshim, "Highly Reliable TaO_x ReRAM and Direct Evidence of Fedox Reaction Mechanism," *Tech. Dig. - Int. Electron Devices Meet. (IEDM)*, p. 293, 2008.

[165] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-Based Resistive Switching Memories-Nanoionic Mechanisms, Prospects, and Challenges," *Adv. Mater.*, vol. 21, pp. 2632–2663, 2009.

[166] A. Chung, J. Deen, J.-S. Lee, and M. Meyyappan, "Nanoscale Memory Devices," *Nanotechnol.*, vol. 21, p. 412001, 2010.

[167] J. J. Yang, M.-X. Zhang, J. P. Strachan, F. Miao, M. D. Pickett, R. D. Kelley, G. Medeiros-Ribeiro, and R. S. Williams, "High Switching Endurance in TaOx Memristive Devices," *Appl. Phys. Lett.*, vol. 97, p. 232102, 2010.

[168] N. Savage, IEEE Spectrum, 2009. [Online]. Available: http://spectrum.ieee.org/semiconductors/devices/spintronic-memristors/

[169] W. Zhao, C. Chappert, V. Javerliac, and J.-P. Nozie, "High Speed, High Stability and Low Power Sensing Amplifier for MTJ/CMOS Hybrid Logic Circuits," *IEEE Trans. Magn.*, vol. 45, pp. 3784–3787, 2009.

[170] M. Julliere, "Tunneling Between Ferromagnetic Films," *Phys. Lett. A*, vol. 54, pp. 225–226, 1975.

[171] G. Tatara and H. Kohno, "Theory of Current-Driven Domain Wall Motion: Spin Transfer Versus Momentum Transfer," *Phys. Rev. Lett.*, vol. 92, p. 086601, 2004.

[172] A. Yamaguchi, T. Ono, S. Nasu, K. Miyake, K. Mibu, and T. Shinjo, "Real-Space Observation of Current-Driven Domain Wall Motion in Submicron Magnetic Wires," *Phys. Rev. Lett.*, vol. 92, p. 077205, 2004.

[173] L. Berger, "Analysis of Measured Transport Properties of Domain Walls in Magnetic Nanowires and Films," *Phys. Rev. B*, vol. 73, p. 014407, 2006.

[174] M. Hayashi, L. Thomas, C. Rettner, R. Moriya, Y. B. Bazaliy, and S. S. P. Parkin, "Current Driven Domain Wall Velocities Exceeding the Spin Angular Momentum Transfer Rate in Permalloy Nanowires," *Phys. Rev. Lett.*, vol. 98, p. 037204, 2007.

[175] A. Thiaville, Y. Nakatani, J. Miltat, and Y. Suzuki, "Micromagnetic Understanding of Current-Driven Domain Wall Motion in Patterned Nanowires," *Europhys. Lett.*, vol. 69, p. 990, 2005.

[176] L. Thomas and S. Parkin, "Current Induced Domain-wall Motion in Magnetic Nanowires," in *Handbook of Magnetism and Advanced Magnetic Materials*. Wiley Online Library, 2007, pp. 1–41.

[177] T. Koyama, D. Chiba, K. Ueda, K. Kondou, H. Tanigawa, S. Fukami, T. Suzuki, N. Ohshima, N. Ishiwata, Y. Nakatani, K. Kobayashi, and T. Ono, "Observation of the Intrinsic Pinning of a Magnetic Domain Wall in a Ferromagnetic Nanowire," *Nat. Mater.*, vol. 10, pp. 194–197, 2011.

[178] J. Shibata, G. Tatara, and H. Kohno, "A Brief Review of Field-and Current-Driven Domain-Wall Motion," *J. of Phys. D: Appl. Phys.*, vol. 44, p. 384004, 2011.

[179] W. F. Brown, "Thermal Fluctuations of a Single-Domain Particle," *Phys. Rev.*, vol. 130, pp. 1677–1686, 1963.

[180] J. Ryu and H. W. Lee, "Current-Induced Domain Wall Motion: Domain Wall Velocity Fluctuations," *J. Appl. Phys.*, vol. 105, pp. 093 929–093 929, 2009.

[181] R. A. Duine, A. S. Nunez, and A. H. MacDonald, "Thermally Assisted Current-Driven Domain-Wall Motion," *Phys. Rev. Lett.*, vol. 98, p. 056605, 2007.

[182] Everspin Technologies. [Online]. Available: http://www.everspin.com/spinTorqueMRAM.php

[183] S. Ikeda, J. Hayakawa, Y. Ashizawa, Y. M. Lee, K. Miura, H. Hasegawa, M. Tsunoda, F. Matsukura, and H. Ohno, "Tunnel Magnetoresistance of 604% at 300 K by Suppression of Ta Diffusion in CoFeB/MgO/CoFeB Pseudo-Spin-Valves Annealed at High Temperature," *Appl. Phys. Lett.*, vol. 93, p. 082508, 2008.

[184] W. H. Butler, X.-G. Zhang, T. C. Schulthess, and J. M. MacLaren, "Spin-Dependent Tunneling Conductance of Fe|MgO|Fe Sandwiches," *Phys. Rev. B*, vol. 63, p. 054416, 2001.

[185] J. Mathon and A. Umersky, "Theory of Tunneling Magnetoresistance of an Epitaxial Fe/MgO/Fe(001) Junction," *Phys. Rev. B*, vol. 63, p. 220403, 2001.

[186] Z. Diao, M. Pakala, A. Panchula, Y. Ding, D. Apalkov, L.-C. Wang, E. Chen, and Y. Huai, "Spin-Transfer Switching in MgO-Based Magnetic Tunnel Junctions," *J. Appl. Phys.*, vol. 99, p. 08G510, 2006.

[187] Z. M. Zeng, P. K. Amiri, G. Rowlands, H. Zhao, I. N. Krivorotov, J.-P. Wang, J. A. Katine, J. Langer, K. Galatsis, K. L. Wang, , and H. W. Jiang, "Effect of Resistance-Area Product on Spin-Transfer Switching in MgO-Based Magnetic Tunnel Junction Memory Cells," *Appl. Phys. Lett.*, vol. 98, p. 072512, 2011.

[188] H. Kronmüller, "General Micromagnetic Theory," *Handbook of Magnetism and Advanced Magnetic Materials*, 2007.

[189] J. D. Harms, F. Ebrahimi, X. F. Yao, and J. P. Wang, "SPICE Macromodel of Spin-Torque-Transfer-Operated Magnetic Tunnel Junctions," *IEEE Trans. Electron Devices*, vol. 57, pp. 1425–1430, 2010.

[190] Y. Higo, K. Yamane, K. Ohba, H. Narisawa, K. Bessho, M. Hosomi, and H. Kano, "Thermal Activation Effect on Spin Transfer Switching in Magnetic Tunnel Junctions," *Appl. Phys. Lett.*, vol. 87, p. 082502, 2005.

[191] Y. Zhang, W. Zhao, Y. Lakys, J. O. Klein, J. V. Kim, D. Ravelosona, and C. Chappert, "Compact Modeling of Perpendicular-Anisotropy CoFeB/MgO Magnetic Tunnel Junctions," *IEEE Trans. Electron Devices*, vol. 59, pp. 819–826, 2012.

[192] R. Beach, T. Min, C. Horng, Q. Chen, P. Sherman, S. Le, S. Young, K. Yang, H. Yu, X. Lu, W. Kula, T. Zhong, R. Xiao, A. Zhong, G. Liu, J. Kan, J. Yuan, J. Chen, R. Tong, J. Chien, T. Torng, D. Tang, P. Wang, M. Chen, S. Assefa, M. Qazi, J. DeBrosse, M. Gaidis, S. Kanakasabapathy, Y. Lu, J. Nowak, E. O'Sullivan, T. Maffitt, J. Sun, and W. Gallagher, "A Statistical Study of Magnetic Tunnel Junctions for High-Density Spin Torque Transfer-MRAM (STT-MRAM)," *Tech. Dig. - Int. Electron Devices Meet. (IEDM)*, pp. 306–308, 2008.

[193] W. Zhao, L. Torres, Y. Guillemenet, L. V. Cargnini, Y. Lakys, J.-O. Klein, D. Ravelosona, G. Sassatelli, and C. Chappert, "Design of MRAM based Logic Circuits and its Applications," in *ACM Great Lakes Symposium on VLSI*, 2011, pp. 431–436.

[194] B. Razavi, *Fundamentals of Microelectronics*. Wiley, 2006.

[195] E. Lehtonen, J. H. Poikonen, and M. Laiho, "Two Memristors Suffice to Compute All Boolean Functions," *Electron. Lett.*, vol. 46, pp. 239–240, 2010.

[196] J. Shen, "Logic Devices and Circuits Based on Giant Magnetoresistance," *IEEE Trans. Magn.*, vol. 33, pp. 4492–4497, 1997.

[197] R. Richter, L. Bar, J. Wecker, , and G. Reiss, "Nonvolatile Field Programmable Spin-Logic for Reconfigurable Computing," *Appl. Phys. Lett.*, vol. 80, p. 1291, 2002.

[198] H. Meng, J. G. Wang, and J. P. Wang, "A Spintronics Full Adder for Magnetic CPU," *IEEE Electron Device Lett.*, vol. 26, pp. 360–362, 2005.

[199] J. P. Wang and X. F. Yao, "Programmable Spintronic Logic Devices for Reconfigurable Computation and Beyond," *J. Nanoelectron. Optoelectron.*, vol. 3, pp. 12–23, 2008.

[200] L. Leem and J. S. Harris, "Magnetic Coupled Spin-Torque Devices for Nonvolatile Logic Applications," *J. Appl. Phys.*, vol. 105, p. 07D102, 2009.

[201] V. Höink, J. W. Lau, and W. F. Egelhoff, "Micromagnetic Simulations of a Dual-Injector Spin Transfer Torque Operated Spin Logic," *Appl. Phys. Lett.*, vol. 96, p. 142508, 2010.

[202] F. E. J. H. A. Lyle, X. F. Yao and J. P. Wang, "The 3-Bit Gray Counter Based on Magnetic-Tunnel-Junction Elements," *IEEE Trans. Magn.*, vol. 46, pp. 2216–2219, 2010.

[203] K. Bickerstaff and E. E. Swartzlander, "Memristor-Based Arithmetic," *Asilomar conf. on Sig., Sys., and Comp.*, pp. 1173–1177, 2010.

[204] S. Matsunaga, J. Hayakawa, S. Ikeda, K. Miura, T. Endoh, H. Ohno, and T. Hanyu, "MTJ-Based Nonvolatile Logic-in-Memory Circuit, Future Prospects and Issues," *Proceedings of the Conference on Design, Automation and Test in Europe (DATE)*, pp. 433–435, 2009.

[205] Y. Liu, S. Chen, M. Nakayama, and K. Watanabe, "Limitations of a Relaxation Oscillator in Capacitance Measurements," *IEEE Trans. Instrum. Meas.*, vol. 49, pp. 980–983, 2000.

[206] W. S. Snyder and D. V. Ess, "Capacitance Sensor Using Relaxation Oscillator," Patent US 07 307 485 B1, 2007. [Online]. Available: http://www.lens.org/lens/patent/US_7307485_B1

[207] H. Nobumi and S. Takeo, "An RC Discharge Digital Capacitance Meter," *IEEE Trans. Instrum. Meas.*, vol. 32, pp. 316–321, 1983.

[208] Z. Albus, "PCB-Based Capacitive Touch Sensing With MSP430," Texas Instruments, Dallas, Application Report SLAA363A, 2007. [Online]. Available: http://www.ti.com/lit/an/slaa363a/slaa363a.pdf

[209] "Capacitance and Inductance Measurements Using an Oscilloscope and a Function Generator," Tektronix, Application Note, 2007. [Online]. Available: http://www.tek.com/document/application-note/capacitance-and-inductance-measurements-using-oscilloscope-and-function-ge

[210] C. Liguori, "Capacitance and Inductance Measurement," in *Handbook of Measuring System Design*, 2005.

[211] S. Zhang and Z. Li, "Roles of Nonequilibrium Conduction Electrons on the Magnetization Dynamics of Ferromagnets," *Phys. Rev. Lett.*, vol. 93, p. 127204, 2004.

[212] E. D. Ranieri, P. E. Roy, D. Fang, E. K. Vehsthedt, A. C. Irvine, D. Heiss, A. Casiraghi, R. P. Campion, B. L. Gallagher, T. Jungwirth, and J. Wunderlich, "Piezoelectric Control of the Mobility of a Domain Wall Driven by Adiabatic and Non-Adiabatic Torques," *Nat. Mater.*, vol. 12, pp. 808–814, 2013.

[213] G. Tatara, H. Kohno, and J. Shibata, "Microscopic Approach to Current-Driven Domain Wall Dynamics," *Phys. Rep.*, vol. 468, pp. 213–301, 2008.

[214] C. Burrowes, A. P. Mihai, D. Ravelosona, J.-V. Kim, C. Chappert, L. Vila, A. Marty, Y. Samson, F. Garcia-Sanchez, L. D. Buda-Prejbeanu, I. Tudosa, E. E. Fullerton, and J.-P. Attane, "Non-Adiabatic Spin-Torques in Narrow Magnetic Domain Walls," *Nat. Phys.*, vol. 6, pp. 17–21, 2010.

[215] M. Eltschka, M. Wötzel, J. Rhensius, S. Krzyk, U. Nowak, M. Kläui, T. Kasama, R. E. Dunin-Borkowski, L. J. Heyderman, H. J. van Driel, and R. A. Duine, "Nonadiabatic Spin Torque Investigated Using Thermally Activated Magnetic Domain Wall Dynamics," *Phys. Rev. Lett.*, vol. 105, p. 056601, 2010.

[216] N. L. Schryer and L. R. Walker, "The Motion of 180° Domain Walls in Uniform DC Magnetic Fields," *J. Appl. Phys.*, vol. 45, pp. 5406–5421, 2003.

[217] A. Mougin, M. Cormier, J. P. Adam, P. J. Metaxas, and J. Ferré, "Domain Wall Mobility, Stability and Walker Breakdown in Magnetic Nanowires," *Europhys. Lett.*, vol. 78, p. 57007, 2007.

[218] J. Wunderlich, D. Ravelosona, C. Chappert, F. Cayssol, V. Mathet, J. Ferre, j. P Jamet, and A. Thiaville, "Influence of Geometry on Domain Wall Propagation in a Mesoscopic Wire," *IEEE Trans. Magn.*, vol. 37, pp. 2104–2107, 2001.

List of Publications

Publications in Scientific Journals

[1] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Reliability-Based Optimization of Spin-Transfer Torque Magnetic Tunnel Junction Implication Logic Gates"; Advanced Materials Research - Print/CD, 845 (2014); 89 - 95.

[2] T. Windbacher, A. Makarov, **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Novel Bias-Field-Free Spin Transfer Oscillator"; Journal of Applied Physics, 115 (2014), 17; 17C901–1 – 17C901–3.

[3] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Reliability Analysis and Comparison of Implication and Reprogrammable Logic Gates in Magnetic Tunnel Junction Logic Circuits"; IEEE Transactions on Magnetics, 49 (2013), 12; 5620 – 5628.

[4] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Implication Logic Gates Using Spin-Transfer-Torque-Operated Magnetic Tunnel Junctions for Intrinsic Logic-In-Memory"; Solid-State Electronics, 84 (2013); 191 – 197.

[5] **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Influence of Geometry on the Memristive Behavior of Domain Wall Spintronic Memristors and its Applications for Measurement"; Journal of Superconductivity and Novel Magnetism, 26 (2013), 5; 1745 – 1749.

[6] T. Windbacher, **H. Mahmoudi**, A. Makarov, V. Sverdlov, S. Selberherr: "Multiple Purpose Spin Transfer Torque Operated Devices"; Facta Universitatis, 36 (2013), 3; 227 – 238.

Chapter in Book

[1] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Stateful STT-MRAM-Based Logic for Beyond Von Neumann Computing"; in *Semiconductor Device Technology: Silicon and Materials*. CRC Press (In press–2014).

Patents

[1] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Electronic Circuit"; Patent: Europe, No. EP 12193826.0; submitted: 2012–11–22.

[2] T. Windbacher, **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Spin Torque Magnetic Integrated Circuit"; Patent: Europe, No. EP 13161375.4; submitted: 2013–03–27.

[3] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Electronic Circuit"; Patent: International, No. PCT/EP2013/073707; Patent priority number EP 12193826.0; submitted: 2013–11–13.

[4] T. Windbacher, **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Spin Torque Magnetic Integrated Circuit"; Patent: International, No. PCT/EP2014/054985; Patent priority number EP 13161375.4; submitted: 2014–03–12.

Publications in Conference Proceedings

[1] V. Sverdlov, J. Ghosh, **H. Mahmoudi**, A. Makarov, D. Osintsev, T. Windbacher, S. Selberherr: "Modeling of Spin-Based Silicon Technology"; Talk: International Conference on Ultimate Integration on Silicon (ULIS), Stockholm, Sweden; (invited) 2014–04–07 – 2014–04–09; in: "Proceedings of the 15th International Conference on Ultimate Integration on Silicon (ULIS)", (2014), 4 pages.

[2] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "High Performance MRAM-Based Stateful Logic"; Poster: International Conference on Ultimate Integration on Silicon (ULIS), Stockholm, Sweden; 2014–04–07 – 2014–04–09; in: "Proceedings of the 15th International Conference on Ultimate Integration on Silicon (ULIS)", (2014), 4 pages.

[3] T. Windbacher, **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Influence of Magnetization Variations in the Free Layer on a Non-Volatile Magnetic Flip Flop"; Talk: International Conference on Ultimate Integration on Silicon (ULIS), Stockholm, Sweden; 2014–04–07 – 2014–04–09; in: "Proceedings of the 15th International Conference on Ultimate Integration on Silicon (ULIS)", (2014), 4 pages.

[4] T. Windbacher, A. Makarov, **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Novel Bias-Field-Free Large Gain Spin-Transfer Oscillator"; Talk: Annual Conference on Magnetism and Magnetic Materials, Denver, USA; 2013–11–04 – 2013–11–08; in: "Abstract Book of 58th Annual Conference of Magnetism and Magnetic Materials (MMM)", (2013), 456–457.

[5] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Performance Analysis and Comparison of Two 1T/1MTJ-based Logic Gates"; Talk: International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Glasgow, Scotland, United Kingdom; 2013–09–03 – 2013–09–05; in: "Proceedings of the 18th International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)", (2013), 163 – 166.

[6] T. Windbacher, **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Rigorous Simulation Study of a Novel Non-Volatile Magnetic Flip Flop"; Talk: International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Glasgow, Scotland, United Kingdom; 2013–09–03 – 2013–09–05; in: "Proceedings of the 18th International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)", (2013), 368 – 371.

[7] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "STT-MRAM-Based Reprogrammable Logic Gates for Large-Scale Non-Volatile Logic Integration"; Poster: International Conference on Nanoscale Magnetism (ICNM), Istanbul, Turkey; 2013–09–02 – 2013–09–06; in: "Proceedings of the International Conference on Nanoscale Magnetism", (2013), 208.

[8] T. Windbacher, **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Novel Non-Volatile Magnetic Flip Flop"; Poster: International Conference on Spintronics and Quantum Information Technology (SPINTECH), Chicago Illinois USA; 2013–07–29 – 2013–08–02; in: "Proceedings of Seventh International School on Spintronics and Quantum Information Technology", (2013), 1 page.

[9] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "STT-MTJ-Based Implication Logic Circuits for Non-Volatile Logic-in-Memory Applications"; Talk: Symposium on CMOS Emerging Technologies, Whistler, BC, Canada; (invited) 2013–07–17 – 2013–07–19; in: "Book of Abstracts of the 2013 Symposium on CMOS Emerging Technologies (CMOS ET 2013)", (2013), 1 page.

[10] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "MRAM-based Logic Array for Large-Scale Non-Volatile Logic-in-Memory Applications"; Talk: Proceedings of the 2013 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), New York City, USA; 2013–07–15 – 2013–07–17; in: "Proceedings of the 2013 IEEE/ACM International Symposium on Nanoscale Architectures", (2013), 2 pages.

[11] T. Windbacher, **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Novel MTJ-Based Shift Register for Non-Volatile Logic Applications"; Talk: Proceedings of the 2013 IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH), New York City, USA; 2013–07–15 – 2013–07–17; in: "Proceedings of the 2013 IEEE/ACM International Symposium on Nanoscale Architectures", (2013), 2 pages.

[12] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Design and Applications of Magnetic Tunnel Junction Based Logic Circuits"; Talk: The 9th Conference on Ph.D. Research in Microelectronics & Electronics- PRIME 2013, Villach, Austria; 2013–06–24 – 2013–06–27; in: "Proceedings of the 9th Conference on Ph.D. Research in Microelectronics & Electronics", (2013), 157 – 160.

[13] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Optimization of Spin-Transfer Torque Magnetic Tunnel Junction-Based Logic Gates"; Poster: International Workshop on Computational Electronics (IWCE), Nara, Japan; 2013–06–04 – 2013–06–07; in: "Proceedings of the 16th International Workshop on Computational Electronics (IWCE 2013)", (2013), 244 - 245.

[14] V. Sverdlov, **H. Mahmoudi**, A. Makarov, D. Osintsev, J. Weinbub, T. Windbacher, S. Selberherr: "Modeling Spin-Based Devices in Silicon"; Talk: International Workshop on Computational Electronics (IWCE), Nara, Japan; (invited) 2013–06–04 – 2013–06–07; in: "Proceedings of the 16th International Workshop on Computational Electronics (IWCE 2013)", (2013), 70 – 71.

[15] **H. Mahmoudi**, T. Windbacher, V. Sverdlov, S. Selberherr: "Impact of Device Parameters on the Reliability of the Magnetic Tunnel Junction Based Implication Logic Gates"; Poster: International Workshop "Functional Nanomaterials and Devices", Kyiv, Ukraine; 2013-04-08 – 2013-04-11; in: "Proceedings of the 7th International Workshop "Functional Nanomaterials and Devices"", (2013), 68 – 69.

[16] **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "MTJ-based Implication Logic Gates and Circuit Architecture for Large-Scale Spintronic Stateful Logic Systems"; Talk: European Solid-State Device Research Conference (ESSDERC), Bordeaux, France; 2012–09–17 – 2012–09–21; in: "Proceedings of the 42th European Solid-State Device Research Conference (ESSDERC)", (2012), 254 – 257.

[17] **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "A Robust and Efficient MTJ-based Spintronic IMP Gate for New Logic Circuits and Large-Scale Integration"; Talk: International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Denver, USA; 2012–09–05 – 2012–09–07; in: "Proceedings of the 17th International Conference on Simulation of Semiconductor Processes and Devices", (2012), 225 - 228.

[18] **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Spintronic Stateful Logic Gates using Magnetic Tunnel Junctions Written by Spin-Transfer Torque"; Poster: The 7th International Conference on Physics and Applications of Spin-related Phenomena in Semiconductors (PASPS-VII), Eindhoven, the Netherlands; 2012–08–05 – 2012–08–08; in: "Book of Abstracts", (2012), P–6.

[19] **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Novel Memristive Charge- and Flux-Based Sensors"; Talk: The 8th Conference on Ph.D. Research in Microelectronics & Electronics- PRIME 2012, Aachen, Germany; 2012–06–12 – 2012–06–15; in: "Proceedings of the 8th Conference on Ph.D. Research in Microelectronics & Electronics", (2012), 4 pages.

[20] **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "State Drift Optimization of Memristive Stateful IMP Logic Gates"; Poster: International Workshop on Computational Electronics (IWCE), Madison, WI, USA; 2012–05–22 – 2012–05–25; in: "Proceedings of the 15th International Workshop on Computational Electronics (IWCE 2012)", (2012), 243 – 244.

[21] **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Influence of Geometry on Memristive Behavior of the Domain Wall Spintronic Memristors and its Applications for Measurements"; Poster: International Conference on Superconductivity and Magnetism, Istanbul, Turkey; 2012–04–29 – 2012–05–04; in: "Proceedings of International Conference on Superconductivity and Magnetism (ICSM 2012)", (2012), 1 page.

[22] **H. Mahmoudi**, V. Sverdlov, S. Selberherr: "Domain-Wall Spintronic Memristor for Capacitance and Inductance Sensing"; Talk: International Semiconductor Device Research Symposium (ISDRS), Washington DC , USA; 2011–12–07 – 2011–12–09; in: "Proceedings of the International Semiconductor Device Research Symposium (ISDRS 2011)", (2011), 2 pages.

Publication Statistics

	Author	Co-author	Total
Journals	4	2	6
Conferences	15	7	22
Chapter in book (under review)	1	0	1
Patents (pending)	1	1	2
Total	21	10	31

Curriculum Vitae

March 21st, 1985
Born in Baneh, Kurdistan, Iran

June 2003
High school graduation in Mathematics & Physics

September 2003 – September 2007
B.Sc. in Electrical Engineering-Telecommunication
K.N.Toosi University of Technology, Tehran, Iran

September 2007 – September 2009
M.Sc. in Electrical Engineering-Microelectronic Devices
Sharif University of Technology, Tehran, Iran

September 2009 – February 2011
Ph.D. student in Electrical Engineering (Quited)
Sharif University of Technology, Tehran, Iran

April 2011 – Present
Ph.D. student in Electrical Engineering
Institute for Microelectronics, Technische Universität Wien, Vienna, Austria