D I S S E R T A T I O N

The Simulation of Emission from Printed Circuit Boards under a Metallic Cover

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von

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Abstract

The subject of this dissertation is the development of an efficient simulation method for the electromagnetic emission from printed circuit boards (PCB), which are situated under a metallic cover at an electrically short distance. Examples of such configurations are automotive control devices, where the PCBs are often parallel to a metallic enclosure cover, mobile devices, like cell phones with metallic shields or parallel PCBs, slim DVD, enclosures and devices with PCBs parallel to a metallic cooling device.

An investigation of memory- and simulation time efforts of several numerical methods for the simulation of the emissions from complex PCBs in the frequency range from a few kHz to several GHz reveals that three-dimensional full wave solutions are extremely costly in the mid-term. Emission simulations have to consider integrated devices, which together with their enclosure are sources of emission, and external devices, which interact with the device under investigation by connectors and cables. Both increase the complexity problem of the simulation, especially, if numerous simulations are necessary in a computer aided design (CAD) optimization process.

In this work the emission mechanisms, such as conducted emission, direct radiation of transmission line loops, or common mode radiation of components on the PCB and their model description in the literature are investigated in a first step. From these mechanisms based models, an efficient simulation method is developed. Modeling the mechanisms leads to a significant simplification of the numerical problem. The assignment of the models to source and coupling path enables a simulation domain separation and an efficient optimization. An example for the advantage of assigning this model to a source is the common mode inductance of a component on the PCB. This inductance is assigned to the component and independent of any attached cable on the PCB, which acts as the antenna.

The components on the PCB and the PCB interconnection structures excite an electromagnetic field between the PCB ground plane and the metallic cover. Electromagnetic emission is caused by this field, which couples to the external environment at the slots between the ground plane and the cover plane. The parallel plane field is described by a cavity model, which has frequently been used in the literature for the modeling of power plane fields. This cavity model is based on a two-dimensional Helmholtz equation, which can efficiently be solved by established numerical and analytical methods. This work shows that the excitations of the cavity field by the sources on the PCB can be described by an analytical expression. For the description of the emission from the parallel plane slots, a new approach of domain decomposition with port interfaces based on the equivalent source theorem is presented. With the interface ports of the cavity model and the analytical description of the excitation, a common mode coupling path model from the sources on the PCB to the interface slots is established. This coupling path model is independent of the sources on the PCB and of the external environment of the device. It is valid for every kind of source, independent of whether it couples magnetically or electrically. For magnetic coupling sources below the first resonance, there is a direct relation to the common mode inductivity, which has been used in the literature to model the common mode emission from integrated circuits (ICs) and traces on a PCB. The model in this work is valid as long as the separation distance

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from the cover to the PCB ground plane is electrically small. This condition holds in most applications up to high cavity modes. In the literature the common mode coupling from ICs is modeled by μTEM measurements or by field scan methods. For direct IC radiation, the literature describes a modeling approach with dipoles, based on simulated IC currents. The measurement modeling methods need a prototype device. The dipole model has no explicit relationship to the common mode coupling mechanism and needs therefore three-dimensional full wave simulation to consider the enclosure of a device. The analytical method for the description of the excitation presented here enables a modeling based on the geometry of the IC package and the conducted currents, which can be obtained with network simulation. The main advantages of the method presented here are the explicit formulation of the common mode coupling and the fully simulation based modeling, without any measurements. This enables an efficient modeling of the common mode coupling from ICs to the enclosure by analytical and powerful numerical (i.e. FEM) methods.

For initial information about the emission from an enclosure with a slot, a fully analytical model is used to calculate the free space radiation. The model applies a new method for considering the radiation loss in the calculation of the cavity field. The radiation loss is considered by an admittance network, connected to interface ports at the slot of the enclosure. This admittance network is expressed by an analytical far field solution.
In addition to this fully analytical method, the work presents various implementation options for the developed simulation method, which can be used for the optimization and efficient prediction of the emissions of complex devices by simulation.

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Kurzfassung

Gegenstand der Dissertation ist die Entwicklung eines effizienten Verfahrens zur Simulation der elektromagnetischen Emission, die von Leiterplatten ausgeht, welche in elektrisch kurzem Abstand parallel zu einer leitenden Abdeckung angeordnet sind. Solche Anordnungen findet man zum Beispiel in automotiven Steuergeräten, wo die Leiterplatten oft unter einer metallischen Gehäuseabdeckung liegen, in Mobiltelefonen, wo oft metallische Schirmungen oder parallele Leiterplatten zum Einsatz kommen, in schmalen DVD Gehäusen und bei Leiterplatten, die parallel zu metallischen Kühlkörpern platziert sind.

Eine Betrachtung des Speicher- und Rechenzeitaufwandes der verschiedenen numerischen Methoden für die Simulation der Emissionen von komplexer Leiterplatten im Frequenzbereich von wenigen kHz bis einigen GHz zeigt, dass dreidimensionale Vollwellenlösungen mittelfristig nur mit enorm hohem Aufwand möglich sind. Integrierte Bauteile, die zusammen mit ihrem Gehäuse ebenso Quellen der Emission sind, müssen genauso berücksichtigt werden wie externe Beschaltungen, die über Kabel und Stecker mit den Leiterplatten verbunden sind. Beides verschärft das Problem der Komplexität in der Simulation, vor allem, wenn es darum geht im Sinne eines CAD Prozesses eine Optimierung durchzuführen, für die eine Vielzahl von Simulationen erforderlich ist.

In dieser Arbeit werden daher in einem ersten Schritt die Mechanismen der Emissionsentstehung, wie leitungsgebundene Emission, direkte Abstrahlung von Leiterschleifen, oder „Common Mode“-Auskopplung von Bauteilen auf der Leiterplatte und die Modellbeschreibung dieser Mechanismen in der Literatur betrachtet, um ausgehend davon eine effiziente Simulationsmethode abzuleiten. Dieser Ansatz geht davon aus, dass die Beschreibung der Mechanismen auf einfachere numerische Probleme zurückführt und durch die Herstellung des Bezugs zu Koppelpfad und Quelle sowohl eine Trennung der Simulationsdomänen, wie auch eine effiziente Optimierung möglich ist. Beispiel dafür ist die Beschreibung der „Common Mode“-Induktivität eines Bauteils auf der Leiterplatte, die unabhängig von dem an die Leiterplatte angeschlossenen Kabel berechnet werden kann, welches als Antenne wirkt.

Die Emission von Leiterplatten, die parallel zu einer metallischen Abdeckung angeordnet sind, geht von den Bauteilen und Leiterbahnen auf der Leiterplatte aus, die ein Feld zwischen der geschlossenen Masselage und der Abdeckung anregen, welches an den Schlitzen von Leiterplatte und Abdeckung auskoppelt. Für die Beschreibung dieses Parallelplattenfeldes wird ein Holraumresonatormodell verwendet, wie es in der Literatur bereits zur Modellierung von Versorgungsflächen über der Masselage verwendet wurde. Das Modell beruht auf einer zweidimensionalen Helmholtzgleichung für die effiziente analytische und numerische Lösungsverfahren zur Verfügung stehen. Es wird gezeigt, dass die Anregung dieses Feldes durch die Quellen auf der Leiterplatte mit einer analytischen Beziehung beschrieben werden kann. Für die Beschreibung der Auskopplung der Emission von den Schlitzen zwischen Leiterplatte und Abdeckung wird ein neuer Ansatz zur Trennung von Simulationsdomänen über Portschnittstellen verwendet, der auf dem Prinzip äquivalenter Quellen beruht. Mit den Schnittstellenports, der Parallelplattenfeldlösung, und der Beschreibung der Anregung wird der „Common Mode “-Koppelpfad von den Quellen auf der Leiterplatte zu den Schlitzen beschrieben, der unabhängig von der Quelle und auch unabhängig von der

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externen Umgebung des Gerätes ist. Diese Koppelpfadbeschreibung ist gültig für jede Art von Quelle gleichgültig, ob diese in erster Linie magnetisch, oder elektrisch koppelt. Bei magnetisch koppelnden Quellen und Frequenzen unterhalb der ersten Holraumresonanz besteht ein direkter Zusammenhang zur „Common Mode“-Induktivität, die in der Literatur zur Beschreibung der „Common Mode “-Emission von Leiterbahnen und ICs verwendet wird. Der hier beschriebene Ansatz ist gültig, solange der Abstand zwischen Leiterplatte und Abdeckung elektrisch klein bleibt, was in den meisten Anwendungsfällen bis zu höheren Hohlraummoden der Fall ist. Das „Common Mode“-Koppelverhalten von ICs wird laut Literatur messtechnisch durch μTEM Messungen oder durch Feld-Scan ermittelt. Für die Modellierung der Direktabstrahlung von ICs findet man in der Literatur neben diesen messtechnischen Methoden auch die Modellierung mit Dipolen aus simulierten Strömen. Die messtechnischen Modellierungsmethoden erfordern einen IC-Prototyp. Die Modellierung mit Dipolen stellt keinen direkten Bezug zum „Common Mode“-Koppelverhalten her und erfordert dreidimensionale Feldsimulation zur Berücksichtigung eines Gerätegehäuses. Die hier gezeigte analytische Beziehung zur Modellierung der Anregung ermöglicht eine Beschreibung mit der Geometrie des IC-Gehäuses und den leitungsgebunden Strömen, wobei der Bezug zum „Common Mode“-Koppelverhalten erhalten bleibt. Damit kann die „Common Mode“-Auskopplung von ICs im Gehäuse analytisch oder mit effizienten Simulationsmethoden (z.B. FEM) simuliert werden.

Zur raschen Abschätzung der Emission von Gehäusen mit Schlitz wird mit dem Modellierungsansatz ein rein analytisches Modell zur Berechnung der Freiraumabstrahlung vom Schlitz abgeleitet. Das Modell verwendet dazu eine neue Methode zur Berücksichtigung der Abstrahlverluste bei der Berechnung des Hohlraumfeldes. Die Verluste der Abstrahlung werden dabei berücksichtigt, indem ein Verlustnetzwerk an die Schnittstellenports am Schlitz angeschaltet wird. Das Verlustnetzwerk wird zuvor aus einer analytischen Fernfeldlösung ermittelt.

Die Arbeit zeigt zusätzlich zu diesem rein analytischen Verfahren vielfältige Umsetzungsmöglichkeiten des Simulationsansatzes zur Optimierung von Geräten und zur effizienten Vorhersage der Emission mittels Simulation.

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List of Acronyms

APEMC	Asia-Pacific Symposium on ElectroMagnetic Compatibility
CAD	Computer Aided Design
CAN	Controller Area Network
CD	Compact Disc
CISPR	Comité International Spécial des Perturbations Radioélectriques
CMOS	Complementary Metal Oxide Semiconductor
DVD	Digital Video Disc
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
ESL	Equivalent Series Inductance L
FDFD	Finite Differences Frequency Domain
FDTD	Finite Differences Time Domain
FEM	Finite Element Method
FFT	Fast Fourier Transformation
FIT	Finite Integration Technique
FR4	Flame Retardant glass-fiber reinforced epoxy
GMRES	Generalized Minimal RESidual method
HFSS®	High Frequency Simulation Software
IC	Integrated Circuit
ICEM	Integrated Circuit Electrical Model
IEC	International Electrotechnical Comission
IμE	Institute for MicroElectronics
IMIC	Interface Model for Integrated Circuits
ITRS	International Technology Roadmap for Semiconductors
LCR	Inductance L Capacitance Resistance
LIN	Local Interconnect Network
LISN	Line Interface Simulation Network
MLFMM	Multi Level Fast Multipole Method
MoM	Method of Moments
MOS	Metal Oxide Semiconductor
μTEM	Micro Transversal ElectroMagnetic
NSPWMLFMA	Non-directive Stable Plane Wave Multi Level Fast Multipole Algorithm
PCB	Printed Circuit Board
PEC	Perfect Electric Conduction
PEEC	Partial Equivalent Electric Circuit
PMC	Perfect Magnetic Conduction
RF	Radio Frequency
SAP	Smart Analysis Program
SiP	System in Package

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SMA	Sub Miniatur RF connector, version A
SoC	System on Chip
SPI	Serial Peripheral Interface
TE	Transversal Electric
TLM	Transmission Line Method
TM	Transversal Magnetic
TQFP	Thin Quad Flat Patch
VLSI	Very Large Scale Integration

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List of Symbols

Symbol	Definition	Description
E_{max}	V/m	Maximum electric far field density
I_{dm}	A	Differential mode current
f	Hz	Frequency
A	m^2	Surface area, loop area
r	m	Distance from Source point to field observation point
h	m	Parallel plane separation distance
ϵ_r	$-$	Relative dielectric constant of the material
I_{noise}	A	Noise current
W	m	Width of rectangular parallel planes (y-dimension)
L	m	Length of rectangular parallel planes (x-dimension)
Q	$-$	Quality factor of a resonator
σ	S/m	Conductivity
$\tan(\delta)$	$-$	Loss tangent
f_r	Hz	Resonance frequency
m, n	$-$	Positive integer values
E_{max}^{res}	V/m	Maximum radiated electric far field from an antenna
I_{ant}	A	Antenna feed point current
U_{ant}	V	Antenna feed point voltage
R_1, R_2	Ω	Resistances in a circuit
R_k	Ω	Coupling resistance
I_{cm}	A	Common mode current
U_b	V	Supply (battery) voltage
U_m	V	Measurement voltage
C_k	F	Coupling capacitance
L_1, L_2	H	Self inductances of two loops
M	H	Mutual inductance of two loops
L_k	H	Coupling inductance of two loops
L_{s1}, L_{s2}	H	Stray inductances of two loops
$\vec{E}$	V/m	Electric field density
$\vec{H}$	A/m	Magnetic field density
$\vec{J}$	A/m^2	Electric current density
ϵ	F/m	Permittivity of a material
μ	H/m	Permeability of a material
j	$-$	Imaginary unit: $\sqrt{-1}$ / Integer index
i	$-$	Integer index
ω	$1/s$	Angular frequency: $2\pi f$
E_x	V/m	x-direction component of $\vec{E}$
E_y	V/m	y-direction component of $\vec{E}$
E_z	V/m	z-direction component of $\vec{E}$
$k_{lossless}$	$1/m$	lossless wave number: $\omega\sqrt{\mu\epsilon}$

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Symbol	Definition	Description
L'_c	H	Parallel plane inductance
C'_c	F/m^2	Capacitance per parallel plane area
t'_{c_i}	m	Plane thickness of metal plane i
t'_{s_i}	m	Skin depth of metal plane i
R'_c	Ω	Parallel plane resistance
G'_c	S	Parallel plane conductance
J_z	A/m^2	z-direction component of $\vec{J}$
$\mathcal{C}$	m	Boundary curve of a parallel plane structure
$U_i(x_i, y_i)$	V	Parallel plane voltage at position (x_i, y_i)
$Z_{ij}(x_i, y_i, x_j, y_j)$	Ω	Mutual plane impedance matrix element
W_e	m	Effective width of rectangular parallel planes
L_e	m	Effective length of rectangular parallel planes
k_m	$1/m$	Rectangular parallel plane eigenvalue of x-direction
k_n	$1/m$	Rectangular parallel plane eigenvalue of y-direction
k	$1/m$	Wave number
L_{mn}	$-$	Two dimensional fourier series coefficient
(x_i, y_i)	(m, m)	Position of port with index i on parallel planes
(x_j, y_j)	(m, m)	Position of port with index j on parallel planes
$(\Delta x, \Delta y)$	(m, m)	Parallel plane discretization for LCR grid method
$\tilde{U}$	V	Approximate parallel plane voltage distribution
Res	V/m^2	Residuum (Approximation error) of $\tilde{U}$
W_g	$-$	Finite element weighting function
α_k	$-$	Finite element base functions
$\tilde{u}_k$	V	Nodal approximation of the parallel plane voltage
ξ_i, η_i, ζ_i	$-$	Barycentric (triangular) coordinates of triangle i
A_i	m^2	Area of the triangle with index i
$\mathbf{K}$	$-$	System matrix
$\tilde{\mathbf{U}}$	V	Approximate solution vector
$\mathbf{F}$	V	Excitation vector
$\tilde{\mathbf{U}}_n$	V/m	Solution vector normal derivation
$\mathbf{R}$	m	Boundary weighting matrix
K_{kl}	$-$	System matrix elements
F_l	V	Excitation vector elements
$\mathbf{Z}$	Ω	Parallel plane impedance matrix
I_m	A	Measurement port current
I_s	A	Trace current at the source position
I_l	A	Trace current at the load position
K_{couple}	$-$	Trace to cavity coupling factor
Z_w	Ω	Characteristic trace impedance
γ	$-$	Trace propagation constant
Z_l	Ω	Trace load impedance
l	m	Effective trace length
ll	m	Horizontal trace length
d	m	Trace distance from the ground plane
C_{13}	F	Capacitance of trace and cover
C_{23}	F	Capacitance of cover and ground plane
C_{12}	F	Capacitance of trace and ground plane
K_{couple_md}	$-$	Coupling factor from mode decomposition
φ	V	Electrostatic potential

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Symbol	Definition	Description
K_{couple_a}	$-$	Analytical coupling factor
$U_{m_{tr}}$	V	Plane voltage of model with a trace
w_{tr}	m	Trace width
ϵ_0	F/m	Permittivity of vacuum
d_s	m	Field scan height above the ground plane
$\underline{J}_s$	A/m^2	Complex scanned current density
Jr_s, Ji_s	A/m^2	Components of complex, scanned current density
K_s	$-$	Coupling factor in scan height
α, β, γ, δ	$-$	Coupling constants
d_{ic}	m	Median coupling factor of an IC interconnect path
d_i	m	Distance to ground of IC interconnect segment i
l_i	m	Length of interconnect segment i
U_{cm}	V	Common mode voltage
L_{cm}	H	Common mode inductance of a trace above ground
L_{cm_p}	H	Common mode inductance of a trace between two planes
U_{AB}	V	Differential voltage at opposite plane ports
M_c	H	Coupling inductance from a trace to parallel planes
L_{cm_meas}	H	Measured common mode inductance
Z_{21}	Ω	Transfer impedance
$\vec{n}$	$-$	Surface normal vector
I_{sp}	A	Parallel plane excitation current
$U_{m,n}$	V	Parallel plane voltage at mode m,n
$K_s(x_{sp,y_{sp}})$	A	Source term of parallel plane voltage
$K_{meas}(x,y)$	$-$	Observation point term of parallel plane voltage
$f_{r_{open}}$	Hz	Resonances of rectangular power planes
$\vec{A}$	A	Magnetic vector potential
$\vec{F}$	V	Electric vector potential
$\vec{r}$	m	Vector from origin to field observation point
$\vec{r}'$	m	Vector from origin to source point
$\vec{r}_1'$	m	Vector from source to field observation point
D_a	m	Active antenna dimension
ξ	rad	Angle between $\vec{r}$ and $\vec{r}'$
$\vec{M}$	V/m^2	Magnetic current density
$\vec{E}_{far}$	V/m	Approximate electric far field density
$\vec{H}_{far}$	A/m	Approximate magnetic far field density
λ_0	m	Wavelength in vacuum
$\vec{S}$	W/m^2	Pointing vector
$\vec{S}_{cr}$	W/m^2	Pointing vector of ports with indexes c and r
Y_{a_cr}	S	Admittance matrix elements
$\mathbf{U}_m$	V	Measurement voltage vector
$\mathbf{U}p$	V	Interface port voltage vector
$\mathbf{Y}_a$	S	Radiation admittance matrix
$\kappa(\mathbf{Y}_a)$	$-$	Condition number of matrix $\mathbf{Y}_a$
$\lambda_{min}(\mathbf{Y}_a)$	S	Minimum eigenvalue of matrix $\mathbf{Y}_a$
$\lambda_{max}(\mathbf{Y}_a)$	S	Maximum eigenvalue of matrix $\mathbf{Y}_a$
S_{min}	$-$	Threshold value for matrix condition number
R_{21}	dB	Emission reduction estimation for d reduction
R_{S21}	dB	Emission reduction estimation for shielding
Ric_{12}	dB	Emission reduction estimation for ground under an IC

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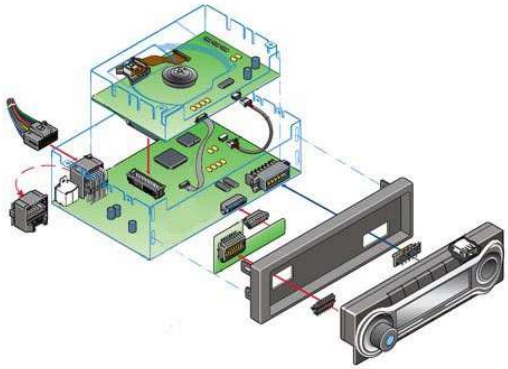
1. Motivation and Objectives

The objective of this work is the development of an efficient method for the simulation of electromagnetic emission from complex printed circuit boards, which are parallel to a metallic plane at an electrically short distance.

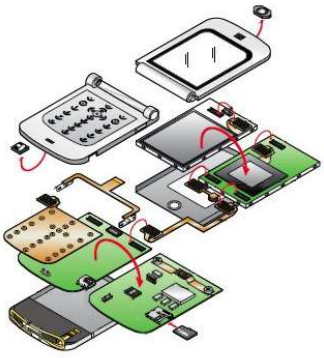
Arrangements of printed circuit boards parallel to a metallic cover plane are used in various applications. Some examples are automotive control devices, mobile devices, parallel stacked PCBs in rack applications, PCBs parallel to a cooling device, computer motherboards mounted parallel to an enclosure plane, CD/DVD and hard disk drives. Figure 1.1 and Figure 1.2 illustrate the arrangements of PCBs parallel to a metallic enclosure or parallel to a PCB ground plane for some example applications.

(a) Motor control device.

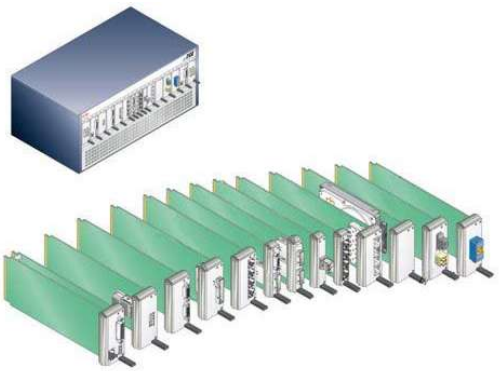


(b) Car audio device.

Figure 1.1: Automotive applications with a PCB parallel to metallic enclosure planes [1].



(a) Cell phone.



(b) Rack mounted parallel PCB stack.

Figure 1.2: Mobile and industrial applications with parallel stacked PCBs [1].

The main challenges for the electromagnetic emission simulation of such devices are handling their complexity, and covering a broad frequency band from the kHz up to the GHz range. Frequency ranges of some emission standards are listed in Table 1.1.

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Subject	Euro Norm	CISPR/IEC	Frequency Range
Sound and television broadcast receivers - Radio disturbance characteristics - Limits and methods of measurement.	EN 55013	CISPR 13	9 kHz to 400 MHz
Limits and methods of measurement of radio disturbance characteristics of electrical motor-operated and thermal appliances for household and similar purposes.	EN 55014	CISPR 14	9 kHz to 400 MHz
Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement.	EN 55022	CISPR 22	9 kHz to 400 MHz
Radio disturbance characteristics for the protection of receivers used on board vehicles, boats and on devices - Limits and methods of measurement.	EN 55025	CISPR 25	150 kHz to 2.5 MHz

Table 1.1: European and international standards and regulations for some device classes [2].

The following list of technical facts from a typical automotive control device, of the BOSCH MED17 generation, gives a perception of the complexity.

- ➢ Number of active and passive components: 598
- ➢ Number of integrated circuits: 18
- ➢ Number of connector pins: 181
- ➢ Number of power stages with $I > 1A$: 37
- ➢ Microcontroller (32bit) clock rate: 150 MHz
- ➢ Bus interfaces:
  - ➪ 3 CAN at clock rate: 2 MHz
  - ➪ Peripheral μs-bus at clock rate: 10 MHz
  - ➪ Flexray bus at clock rate: 10 MHz
  - ➪ 2 SPI interfaces at clock rate: 2 MHz
  - ➪ 2 LIN interfaces at clock rate: 2 MHz
- ➢ Number of PCB layers: 6
- ➢ Minimum trace width: 125 μm
- ➢ PCB board size: 160 mm x 190 mm

In addition to this complex device internal structure, a quantitative electromagnetic emission simulation has to consider external appliances which are connected to the control device by a cable harness. Although mobile devices are smaller, the integration density in the package is much higher. Usually industrial and computer PCBs are also very dense, sizeable, and are operated at even higher clock rates. Therefore, the complexity is a challenge for the

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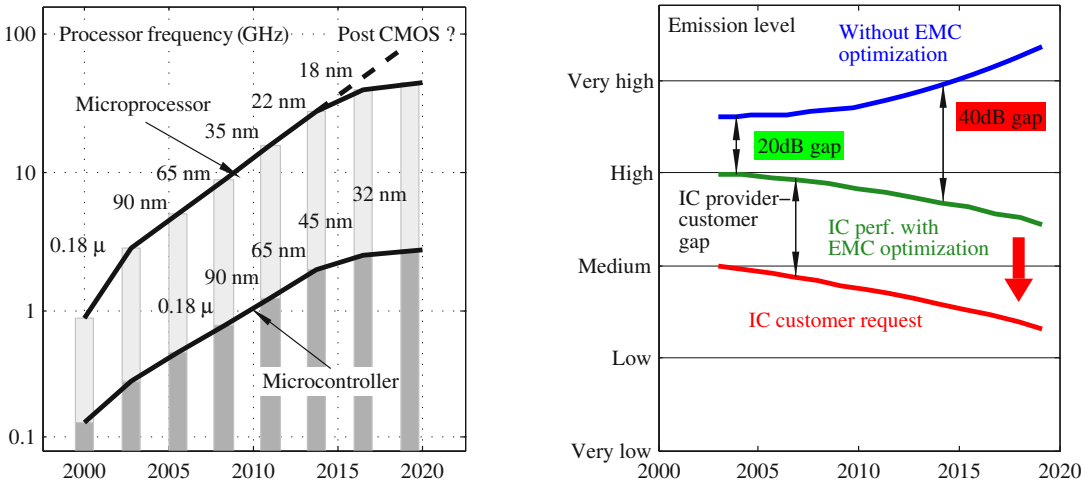
EMC simulation in nearly every application. The complexity will further increase, because the strong demand of rising functionality leads to more density and higher clock rates in the future. Figure 1.3 from [3] depicts a forecast on microprocessor and microcontroller clock rates and emission requirements until 2020. The content of Figure 1.3(a) is based on data from ITRS [4], which sets industry and technology milestones for the next 15 years. By 2020 processors are imaginable to run at about 25GHz. By 2016 the ITRS road map projects the minimum physical gate length of transistors to be close to 9nm, which is considered by most researchers to be kind of the physical limit of silicon. The saturation scenario considers several limiting factors for frequency increase, such as, for example, MOS mobility degradation and interconnect delay. In fact, there is a five year gap between microprocessor development and microcontroller development regarding density and clock rates. This enables a further MOS technology based performance enhancement of microcontrollers beyond 2020. According to [4], functional diversification by integration of analog, RF, power, and passive functions provides additional opportunities beyond scaling in order to increase device performance.
The described complexity increase of microcontrollers provides an impression of the future complexity increase of electronic devices, because nearly every electronic device will be based on a processor or controller. The increased controller performance and functionality will lead to enhanced peripherals and busses, more connector pins, more device interfaces, and denser enclosure designs.

Figure 1.3(b) depicts the evolution of the RF emissions from ICs [3]. There is a strong IC customer pressure for achieving low emissions. IC designs without EMC optimization suffer from high RF emissions and require expensive on board decoupling and filtering. Therefore, EMC concerns have increased in importance. Within the last 10 years low emission and high immunity to interference have emerged as the key differentiators of overall IC performances. A 20dB emission reduction could be achieved by design guidelines and new EMC knowledge in 2000. EMC optimization will lead to a further emission reduction of about 40dB in 2020. Examples have already been presented [5]. However, the technology trend towards more density and higher clock rates leads to higher emissions. Thus, a gap is expected to remain between the customer demand and the emission level of the devices. To meet the customer requirements, low emission design guidelines and simulation based design techniques for SoC and SiP have to be enhanced and generalized.



(a) Core frequency increase until 2020.

(b) Maximum emission level.

Figure 1.3: Increase in IC complexity, clock rates, and emission requirements [3].

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Every electronic device must be compliant to dedicated EMC requirement regulations. Table 1.1 lists some important standards for specific classes of devices. A new device is tested to be EMC compliant at the end of the development cycle on final prototype devices. The failure of this test necessitates a costly redesign and increases the time taken to market the product. Figure 1.4 depicts costs of change, adaptability and optimized quality assurance investment over the life cycle of typical large-scale series fabrication products in a qualitative diagram.

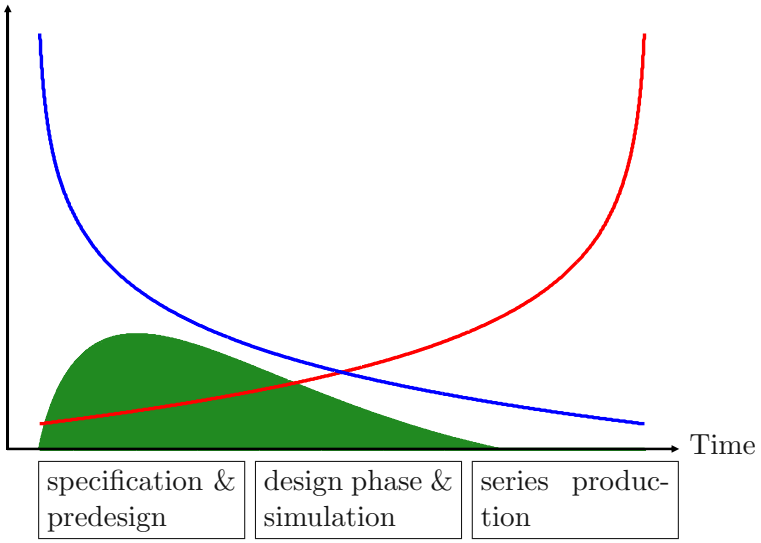

Figure 1.4: **Cost of change**, **Adaptability**, and **Optimized quality assurance investment** over product life cycle. Qualitative diagram for typical large-scale series fabrication products.

In the definition, specification, and predesign phase of the product life cycle, adaptability is at a maximum, when costs of change are at their lowest. The uncertainties of the functional device definition, which is not finalized in the very early stage, inhibit accurate quantitative simulations of the final device. However, with progressing product definition, the quality assurance investment must increase to benefit from high adaptability at low costs. Most predesign definitions can scarcely be changed in the later design process and have a significant influence on the attainable quality performance. Conceptual simulations in the predesign phase powerfully support design decisions in the functional product definition process.
The required quality performance of a product must be reached in the design phase to achieve 100% first pass yield. The 100% yield is necessary to enable the supplier of a product to omit rework phases in the project road map, without any failure risk on agreed customer deadlines. Only simulation provides the opportunity to make performance predictions and optimizations as long as no prototype is available. There must not remain any open quality issues, when a product has been finalized and series fabrication has started.
The main motivation of electromagnetic emission simulation is to ensure the EMC compliance in the design phase of a new device, in order to avoid redesign costs and time delays. However, the simulation methods must be very efficient to enable simulation based CAD of EMC properties within short, time optimized product development cycles. The objective of this work is to develop efficient methods by using analytical and semi-analytical methods, domain decomposition, and methods with an explicit assignment to source and coupling path. This enables fast conceptual simulations in the predesign phase and swift product quality performance optimization in the design phase.

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2. State of the art

There are no state of the art methods available for the efficient simulation of all electromagnetic emissions from the kHz to the GHz range of complex devices, such as described in Chapter 1.
For accurate simulation of these devices, the ICs, the active and passive components, the structures on the PCB, external cabling and external electromagnetic environment (i.e. scattering objects), and even the software coding have to be properly considered in the model [6][7][8][9]. Currently three somewhat differing approaches for the development of suitable simulation methods for this purpose can be found in the literature.

- ➢ Three-dimensional full wave numerical simulation of the whole model.
- ➢ Semi-analytical multipole macro modeling of EMI sources to achieve a reduction of the three-dimensional model.
- ➢ Analytical and numerical modeling of the EMI effects to classify sources and coupling paths regarding their potential to exceed emission limits.

These three approaches, their current state, and their future potential to meet the objectives of the EMI simulation task are described in the following sections.

2.1. The three-dimensional full wave simulation approaches

Intense research has been carried out to solve complex EMC models with three-dimensional full wave simulation. The following discussion of time and frequency domain methods based on recently published examples points out the current state of the methods and their potential to meet the EMC simulation requirements in the future. It reveals that there is actually no single method capable of performing the emission simulations with the required efficiency. That will also be the case in the medium-term.

2.1.1. Time domain methods

The model of an 8 layer interposer PCB was simulated with the FIT method using CST STUDIO SUITE® [10]. The interposer PCB has a size of 32mm x 32mm with layer thicknesses varying between 13μm and 21μm. Trace width is 25μm and trace to trace separation is 20μm. The key facts from the signal integrity, crosstalk simulation of the interposer listed in Table 2.1 impressively reveal the progress in the development of numerical simulation and parallel computing. However, EMC simulations of whole devices have to deal with multiple ICs on complex PCBs within sizeable enclosures and complex cabling. The FIT method of CST STUDIO SUITE® performs a time domain simulation, where the model is exited by a time domain signal and the transients have to decay for the length of the simulated signal period. For a Gaussian shaped pulse that means vanishing model energy within the simulated signal duration. Sizeable metallic enclosures usually have resonances of a reasonably high quality. The frequency domain result is obtained by application of a FFT to the time domain simulation result and the frequency resolution of the FFT is given by the overall duration of the transformed time domain signal. Since the model energy will decrease significantly more slowly for a model with high quality resonances, a simulation time magnitudes higher than

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in Table 2.1 will be necessary to achieve a reasonable frequency resolution. For instance, a resolution of 1MHz at an enclosure resonance of 100MHz may require a signal duration of up to $1\mu s$: much longer than the simulated signal duration of $300ps$ in Table 2.1. This will be even worse for devices with attached cables. A 3m cable in air has its first $\lambda/4$ resonance at 25MHz. Assuming, due to a resonance in the model, a simulated signal time that is 10 times larger, the CPU time per signal from Table 2.1 would increase from 38h to 15 days! However, simulations with a meshing time of 3h and a simulation time per signal of about 38h are also not suitable for an efficient EMC design process. Due to the ongoing increase in computation performance, a significant reduction in the simulation time can be expected in the future. Assuming an unlikely processor clock rate of 25GHz in 2020 versus 2GHz in 2007 according to Figure 1.3(a) and further additional performance enhancements, a reduction in the simulation time by a factor 50 from 38h to 45 minutes can be estimated. However, the model complexity will also increase in the future. That and the previously mentioned increase of simulation time from high quality enclosure resonances are not considered in this estimation of 45 minutes. Assuming the same model complexity, 45 minutes are also far too much to enable multiply simulations in an optimization process with a very high degree of freedom.

Total number of nodes	594,000,000
Number of unknowns	3,564,000,000
Number of processors	20
Peak memory/processor	7.5GB
CPU meshing time	3h
Signal duration	300ps
CPU time/signal	38h

Table 2.1: Key facts of the interposer simulation carried out by [10].

The efficiency of every time domain method, not only of the FIT method, depends heavily on the signal time duration. An accurate high frequency response requires a short time step and, thus, a large number of iterations to simulate a long signal duration. The situation is even worse for the explicit Yee's FDTD method [11], which requires a time step smaller than the time that the light needs to propagate through the smallest mesh cell, known as the CFL (Courant-Friedrichs-Levy) condition [12]. Geometric structures on a PCB demand a fine mesh, which requires a much smaller time step than would be necessary to cover the highest frequency in the simulation. Implicit FDTD methods, such as the CN-FDTD (Crank-Nicolson) or the ADI-FDTD (Alternating Directions Implicit) are a solution to avoid this restriction. However, the implicit methods require matrix inversions [13][14]. A restriction to high frequencies is also given for the finite element time domain method [15]. The previously mentioned time domain methods require a volume discretization of the simulation domain. Methods with volume meshing are suitable for inhomogeneous simulation domains. However, the simulation of free space radiation efforts to mesh a certain amount of free space surrounding the device under investigation and, additionally, the application of a matched surface condition on the boundary of the surrounding free space. This is a significant drawback for emission simulations. The partial equivalent electric circuit (PEEC) method enables a simulation based only on surface discretization and can be formulated for time and frequency domain simulations [16][17][18]. Although the PEEC method needs only surface discretization, the model size limit is significantly lower than that of the previously mentioned methods, because the PEEC method is formulated with dense matrixes. Recent

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publications present some numerical solutions, such as, for instance, model order reduction, to extend the PEEC model size limit [19][20][21]. However, the PEEC method is just another way of solving the electric field integral equation (EFIE) [18], and it therefore has the same limitations regarding an increase in speed, as, for instance, the method of moments (MoM). The following subsection presents recent enhancements of the MoM with the fast multipole method (FMM). It shows also restrictions, especially for the modeling of the near field region, which is relevant for dense enclosures.

2.1.2. Frequency domain methods

Frequency domain methods obtain a solution for one frequency at one simulation. Therefore, multiple simulations have to be performed to obtain a broad band solution. However, fast frequency sweep interpolation techniques have been developed for efficient broad band simulations [22]. Therefore, the main restriction for the frequency domain methods consists of the model size determined by the number of unknowns. Methods with volume discretization, such as, for instance, the finite element method (FEM) or the finite difference frequency domain method (FDFD) are generally based on sparse matrices, which enable models to be solved with significantly more unknowns than methods with dense matrices, like the classical method of moments. However, sparse matrix methods are also not capable of handling complex PCBs inside a metallic enclosure. For example, the interposer simulation of [10] was meshed cubically with 594.000.000 mesh nodes. Assuming a mesh size reduction by a factor 5 by tetrahedral meshing, the remaining 118.800.000 mesh nodes would require about 5.7e9 nonzero elements to be handled in a sparse matrix, with a memory requirement of about 91GByte. Methods, that require only surface discretization, such as the standard MoM, the boundary element method (BEM), or the PEEC method may be used to avoid the meshing of the surrounding space [23]. However, these methods are initially based on dense matrices and, therefore, require significantly more memory and a larger simulation time. Thus, none of these methods is capable of handling a complex PCB under a metallic enclosure cover.

Recent developments of three-dimensional full wave simulation methods are fast multipole methods used to simulate electrically large scattering and enclosure shielding models [24][25][26][27][28]. The MLFMM drastically reduces the memory cost for field integral equation solutions to O(N logN), where N is the number of unknowns. In comparison, a standard MoM algorithm requires $O(N^2)$ memory. However, this memory reduction is feasible solely on electrically large models, because the MLFMM uses only propagating plane waves and therefore succumbs to a severe numerical instability, when dealing with interactions of source and observer points which are closer than approximately one wavelength. The recently developed NSPWMLFMA which is numerically stable in the near field region, is however based on dense matrices [26]. Therefore, it is not suitable for PCB, slim enclosure, and IC package simulations with dense structures in the near field region.
This work presents an efficient simulation method for the cavity field between a PCB ground plane and a metallic enclosure cover, which is parallel to the ground plane at an electrically short distance. The interface of the cavity field to the external environment of the device is given by the open slots at the cavity boundaries. A new domain separation approach by port interfaces and a PMC boundary condition at the slot surfaces enables the separate simulation of the internal and the external field with different methods. The internal field can be calculated with the efficient cavity model, while the external environment can be simulated with any three-dimensional full wave method which is able to handle a PMC boundary condition and excitation current ports. The fast multipole method provides a powerful opportunity for this external device environment simulation, because recent developments by [28] enable a coupling with network simulations.

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The mentioned examples, based on recently published manuscripts, indicate that there is actually no single method capable of handling the whole device EMC simulation. Every method has some constraints which limit the usable model size, frequency range or domain. Combining different methods provides an efficient solution to overcome this problem. The cavity model of this work handles the internal enclosure simulation with maximum efficiency by analytical or two-dimensional numerical methods. The external environment (i.e. a cable harness) may be modeled by existing efficient methods for this purpose. An efficient approach for the modeling of the emissions from cable harnesses was published in [29][30].

2.2. The semi-analytical approach based on EMI source multipole macro modeling

A semi-analytical approach for the simulation of EMC emissions from complex devices, PCBs, and ICs utilizes a multipole macro modeling of the radiation from subsystems [31]. The method describes the emissions from a subsystem (i.e PCB trace, IC) by a multipole expansion with spherical base functions of the Helmholtz equation. The multipole moments are obtained by three-dimensional full wave simulations for layout elements or by near field measurements for ICs. For the consideration of an enclosure, the multipoles are used as excitations in a three-dimensional full wave simulation. This simulation has to consider the external device environment, such as external cabling and scattering objects. This is a drawback for the optimization of devices, because resonances from external structures, which cannot be changed by the design are included in the simulation results and have to be distinguished from the device behavior. The external environment has to be simulated for every optimization design change.
The domain separation method presented in this work enables the device to be optimized independently of the external environment and the emissions to be investigated in different environments. Only one simulation per external environment is necessary.
Another problem of the multipole expansion method is the modeling of ICs. A measurement based modeling as presented by [31] needs a prototype device and a test board. The emissions depend on the software coding and the external circuitry [6][8]. Even if all necessary data of the IC could be obtained by simulations, it would be difficult to generate a port controlled multipole model. There are currently no IC multipole models in the literature, which consider all dependencies generally.
The method presented here utilizes established network simulation and an analytical description of the common mode coupling to the enclosure, which enables quick modeling.

2.3. Analytical and numerical modeling of the EMI effects to classify sources and coupling paths regarding their potential to exceed emission limits

The previously mentioned methods do not provide insight into the coupling process. However, this is required in order to classify sources and geometric elements for the device optimization. A method that does not provide explicit information on the coupling process would need to be very fast, to enable optimizations with a much higher degree of freedom than a method that provides that insight. However, the previously described methods are not that fast. Therefore, researchers concentrated on the modeling of the emission effects, and common

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mode coupling has been found to be a significant mechanism of electromagnetic emission initiated by sources on a PCB [32][33][34]. The common mode coupling inductance for the current driven mode has been formulated analytically for a trace above a finite ground plane [35][36][37]. Analytical models for the voltage driven mechanism were developed for a PCB with attached cables [38][39]. All formulations consider the PCB and the trace, but not the influence of an enclosure. According to Chapter 1, a metallic plane is parallel to the PCB at an electrically short distance in many applications. This plane has a significant influence on the common mode coupling impedance. Some configurations have been modeled with FDTD simulation tools [40][41].
The two-dimensional Helmholtz equation was utilized to efficiently model the cavity field between the power- and groundplane of a PCB for the purpose of power integrity analysis [42][43]. Traces were introduced into the cavity field model by mode decomposition for signal integrity and power integrity simulations on PCB level [44].
This work develops a model for the field between the ground plane of a PCB and a parallel metallic cover based on this two-dimensional Helmholtz equation. Traces on the PCB are efficiently introduced into the cavity model by an analytical formulation without mode decomposition. The introduction contains explicit information of the common mode coupling. The thereby obtained insight enables the reduction of device optimization only on relevant parameters. The common mode inductance of a trace above a ground plane without a metallic enclosure derived by [36] and [37] depends on a factor d/W (d...trace height above the ground plane, W... ground plane width). It is shown in this work that the same dependence can be obtained from the cavity model and the analytical trace factor. Therefore, the coupling effect, described by the cavity model, is the same as that of a trace above a ground plane. Powerful analytical and numerical methods are presented for the solution of the two-dimensional Helmholtz equation. The external environment of the enclosure can be simulated with another established simulation program, according to a new domain separation method, as mentioned previously. The next section describes an additional application of the proposed cavity model for fast predesign investigations.

2.4. Analytical model for the free space radiation of a cubical enclosure intended for fast predesign investigations

A fully analytical model is presented in this work for the free space radiation from a cubical metallic enclosure with a slot at one parallel-plane edge. The radiation loss is considered at the cavity field formulation by the connection of an admittance network to ports at the slot of the enclosure.
In [45] and [46] the radiation loss was calculated from the far field expressions of a cavity model without consideration of the radiation loss. Afterwards this loss was introduced into the cavity model by a quality factor. When the radiation loss becomes the dominant loss mechanism, this method fails, because the radiated power calculated from the model without the radiation loss will be far too high.
The method of this work accurately considers radiation, because the admittances are calculated independently of the cavity model.
Another modeling method for the calculation of the shielding effectiveness and wire coupling inside a cubical enclosure was utilized by [47][48][49][50]. This method models the field inside the enclosure by a superposition of rectangular cavity TE and TM modes. Wires are segmented and each segment is coupled to each TE and TM mode with mutual coupling impedances. These coupling impedances are calculated in advance. The enclosure size is not restricted in this method. However, the method cannot be generalized to arbitrary enclosure geometries.

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The method of this work can deal with arbitrary parallel-plate shapes. The analytical model for the cubical enclosure is just a special case intended for first estimations in a predesign phase. Since the method in this work introduces traces only by their vertical segments to the cavity, without mode decomposition, it is more efficient and provides better insight for the optimization.

2.5. Modeling of the common mode coupling from ICs to the cavity field

An emission simulation of a device has also to consider ICs and active components. This requires IC emission models which can be efficiently integrated into the emission modeling technique of the device. The evolution of IC standard modeling methods for RF emission in Table 2.2 was presented by [3] in May 2008.

Bandwidth	Type	2005	2010	2015	2020
Below 3 GHz	Conducted	Industrial use (ICEM)			
	Radiated	Solution exists (ICEM dipole)	Industrial use		
3-10 GHz	Conducted	NOT known	Solution exists	Industrial use	
	Radiated	NOT known	Solution exists	Industrial use	
10-40 GHz	Conducted	NOT known	NOT known	Solution exists	Industrial use
	Radiated	NOT known	NOT known	Solution exists	Industrial use

Table 2.2: Evolution of IC standard modelling methods for RF emission [3].

According to Table 2.2, there are currently no IC standard modeling methods available for the frequency range above 3GHz.
The table indicates that a solution for radiated emission IC modeling exists below 3GHz. This method models the radiated field of an IC by dipoles placed along the interconnects of the lead frame. The dipole moments are modeled by the interconnect currents from a network simulation with an ICEM model [51]. Therefore, the modeling method requires only simulations, but no measurements. Although a comparison of results from this method with three-dimensional full wave simulation demonstrated good agreements for canonical structures, a comparison of IC model results with measurements showed some significant deviations of about 6dB [52]. The main reasons for the deviations were reported by [52] to be inaccuracies of the utilized geometrical package model and uncertainties of the currents on the package. There are currently no results with increased accuracy from this modeling approach in the literature.
Another approach for modeling the near field of an IC has been presented by [6]. This method models the package with the three-dimensional full wave simulation program HFSS® and in-

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troduces excitation ports at the chip side and on the PCB side of the package. The ports are excited by frequency domain excitations, obtained by FFT of time domain network simulations with an ICEM model. A good agreement of simulation results to measurement results has been achieved by this method on a 16bit microcontroller with a 144pin TQFP package. Both methods of [6] and [52] require three-dimensional full wave simulation for the consideration of an enclosure. They do not provide an explicit relation from the IC model sources to the common mode coupling from the IC to the enclosure. This makes optimization inefficient and prevents an integration into the cavity device model developed in the course of this dissertation and predictive simulations of μTEM measurement results.
The common mode coupling is also the coupling mechanism from an IC to a μTEM cell, which is evident, because the magnetic and the electric common mode coupling moments of an IC can be obtained by μTEM measurements [53]. Main standardized EMC measurements for ICs are based on μTEM cells [54]. This indicates the significance of the common mode coupling. The coupling of the IC to the μTEM cell is also modeled in [6]. However, the results of this modeling show deviations from the measurement results above 300MHz and the modeling is carried out by using lumped coupling capacitors which have no relation to the previously mentioned near field model.
This work models the common mode coupling from a trace on a PCB to the parallel-plane cavity field between the PCB ground plane and a metallic enclosure cover by an analytical formulation. Only the vertical current segments of the trace couple to the cavity. Therefore, the coupling can be described by the currents on the two trace ends (source and load positions), which are obtained from a network simulation of the trace, the load, and the source. The common mode coupling of an IC can be modeled by the same approach. The currents on the IC package can be obtained by network simulation with an ICEM model, as already presented by [6] and [52]. With these currents on the vertical elements of the package, the common mode coupling can be modeled accurately up to high cavity resonance frequencies in the GHz range. The model provides explicit information about the influence of every individual geometric package part on the overall common mode coupling of the device. This information enables efficient EMC optimization of both the package geometry and the part placement inside an enclosure.

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3. Electromagnetic emissions mechanisms from PCBs

3.1. Conducted emission - Radiated emission

Cables connected to a device carry unwanted transient signals and other disturbances to other devices. This is the general conducted emission definition [55]. The conducted emissions are measured with voltage and current measurements on the cables. Such measurement methods are standardized, for instance, for automotive appliances in CPSPR25 [56]. The voltage measurement method measures the conducted emissions only on the power and eventually the ground cable on a LISN (Line Interface Simulation Network). However, that is of utmost relevance, because the disturbances on the power supply are distributed to other devices by the power delivery network. The current measurement method with a coupling coil measures the common mode current on a multi-wire cable harness. The measured conducted emissions are initiated by galvanic coupling, electric and magnetic near field coupling, and even from radiated far fields. Transient signals and disturbances on the cables also cause radiated emission. Thus, every PCB emission mechanism that causes radiated emissions from cables attached to the PCB is also relevant for the conducted emissions. The following description of emission mechanisms from the PCB, therefore does not further distinguish between radiated and conducted emission mechanisms.

All radiated and conducted emission measurement methods have different measurement sensitivities for different emission frequency ranges and different emission coupling mechanisms. This is the main reason for the application of different methods for device EMC compliance measurements.

Emission from PCBs can be classified based on the following two main mechanisms:

- ➢ Direct radiation from PCB sources.
  - ⇨ Differential mode signals on the PCB and on attached cables.
- ➢ Emissions through galvanic coupling, electric and magnetic near field coupling to cables, long nets, and mechanical structures, which can be interpreted as antennas.
  - ⇨ Common mode coupling from the differential mode signals.
  - ⇨ Unintentional, parasitic signals on the PCB and on attached cables.

3.2. Direct radiation from PCB sources

Every PCB structure that carries transient voltages and currents radiates some electromagnetic power. Structures on the PCB are traces, planes, the interconnects of device packages, discrete passive components, and connectors. As long as these structures are small compared to the wavelength, they are not efficient antennas, and therefore, the radiation usually remains low [57]. The following design expressions for the estimation of the maximum radiated field from trace loops and from rectangular planes on the PCB enable the efficient identification of critical structures on the PCB.

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3.2.1. Direct radiation from trace and IC package loops on the PCB

According to [58] the estimation for the maximum radiated electric far field density from a loop current I_{dm} on a PCB as depicted in Figure 3.1 is

$$E_{max}(f) \approx \left(2.6 \cdot 10^{-14} \frac{Vs^2}{Am^2}\right) \cdot \frac{I_{dm}(f)A}{r} f^2, \tag{3.1}$$

where A is the loop area, r is the distance of the field observation point from the loop and $I_{dm}(f)$ is the magnitude of the harmonic at frequency f of the loop current I_{dm}. The current $I_{dm}(f)$ can be obtained from standard time domain network simulation and FFT. Note that this is a first order estimation, intended to classify the direct radiation of PCB loops regarding their ability to exceed an emission limit. This estimation considers neither the influence of shields on the PCB, nor the influence of an enclosure.

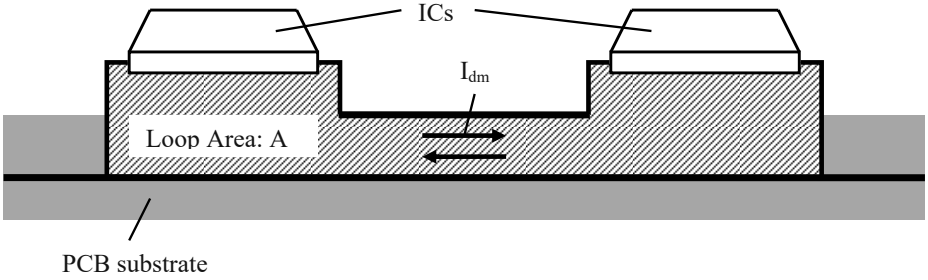

Figure 3.1: Radiating current loop on a PCB.

3.2.2. Direct radiation from plane edges on the PCB

According to [59] the estimation for the maximum radiated electric far field density from rectangular power planes on a PCB as depicted in Figure 3.2 is

$$E_{max}(f) \approx (120\Omega) \cdot \frac{I_{noise}(f)h}{r\epsilon_r W} \cdot Q \qquad \text{with} \qquad Q = \left(\tan(\delta) + \frac{1}{h}\sqrt{\frac{W\sqrt{\epsilon_r}}{(592\Omega)\sigma}}\right)^{-1}, \tag{3.2}$$

where σ is the conductivity of the planes, r is the distance of the field observation point from the PCB, $I_{noise}(f)$ is the magnitude of the harmonic at frequency f of the noise current I_{noise}, ϵ_r is the relative permittivity, and $\tan(\delta)$ is the loss tangent of the PCB substrate. Maximum radiation occurs at the parallel plane resonances

$$f_r \approx \frac{c_0}{2\pi\sqrt{\epsilon_r}} \sqrt{\left(\frac{m\pi}{L}\right)^2 + \left(\frac{n\pi}{W}\right)^2}, \tag{3.3}$$

where m and n are positive integer values and c_0 denotes the speed of light in vacuum. Note that this is a good first order estimation, intended to classify the direct radiation of PCB planes regarding their ability to exceed an emission limit. This estimation considers neither the influence of shields on the PCB, nor the influence of an enclosure or the influence of the position of the noise current on the planes. The power plane noise current I_{noise} has to be obtained from a network simulation which considers the integrated circuits with ICEM models [60], [61] and the power plane impedance. The power plane impedance for rectangular planes is obtained from (4.18) [59]. A powerful finite element method for the impedance simulation of fairly arbitrary shaped planes is described in Section 4.4.

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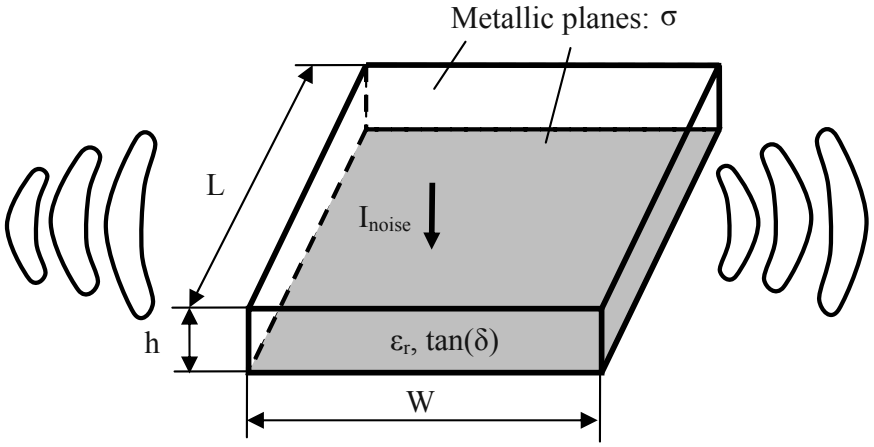

Figure 3.2: Radiating current loop on a PCB.

3.2.3. Direct radiation from a PCB which is parallel to a metallic cover plane at an electrically short distance

This parallel plane structure radiates from the slots and apertures at the open edges of the parallel plane structure, established by the PCB ground plane and the metallic cover plane. An efficient method, based on a cavity model, is developed in this work to describe this radiation. The radiated field from the structures on the PCB is scattered at the parallel planes and, thus, only the cavity mode fields can propagate to the edges. Therefore, the cavity model, which considers the coupling of PCB structures to the cavity field, describes the radiated emission accurately. An efficient model for predesign investigations of the free space radiation of a rectangular enclosure with a slot on one edge is presented in Chapter 7.

3.3. Emissions through galvanic coupling, electric and magnetic near field coupling to cables, long nets, and mechanical structures, interpreted as antennas

Generally all emission mechanisms in this section are common impedance coupling mechanisms. Figure 3.3 illustrates the common impedance coupling mechanisms of a source circuit to a victim circuit. A common resistor R_k couples the two circuits in Figure 3.3(a) galvanically. The coupling capacitance C_k in Figure 3.3(b) couples a noise voltage to a victim circuit. Inductive coupling of a source loop and a victim loop is depicted in Figure 3.3(b). The right circuit diagram in Figure 3.3(b) is equivalent to the left diagram. It illustrates the possibility to consider the inductive coupling with a coupling inductance L_k. The victim circuit in Figure 3.3 is a sensitive sensor circuit and the measurement of the sensor voltage is denoted by U_k. However, the victim circuit may also be any other circuit on the PCB. Extended circuits on the PCB, circuits with attached cables, or sizeable daughter boards are the unintentional emission antennas which are supplied from the coupled currents and voltages. When the antenna of the victim circuit is located far away from the coupling fields, the whole coupled field will not change significantly, even when the antenna is replaced by a different one. Therefore, the coupling impedances enable the description of the source coupling to an antenna, independent of the antenna. This provides the opportunity to classify the PCB structures regarding their emissions relevance with only the coupling impedances and without considering the antenna structure. For example, the consideration of a cable attached to a PCB in an emission simulation will also show the cable resonances. However,

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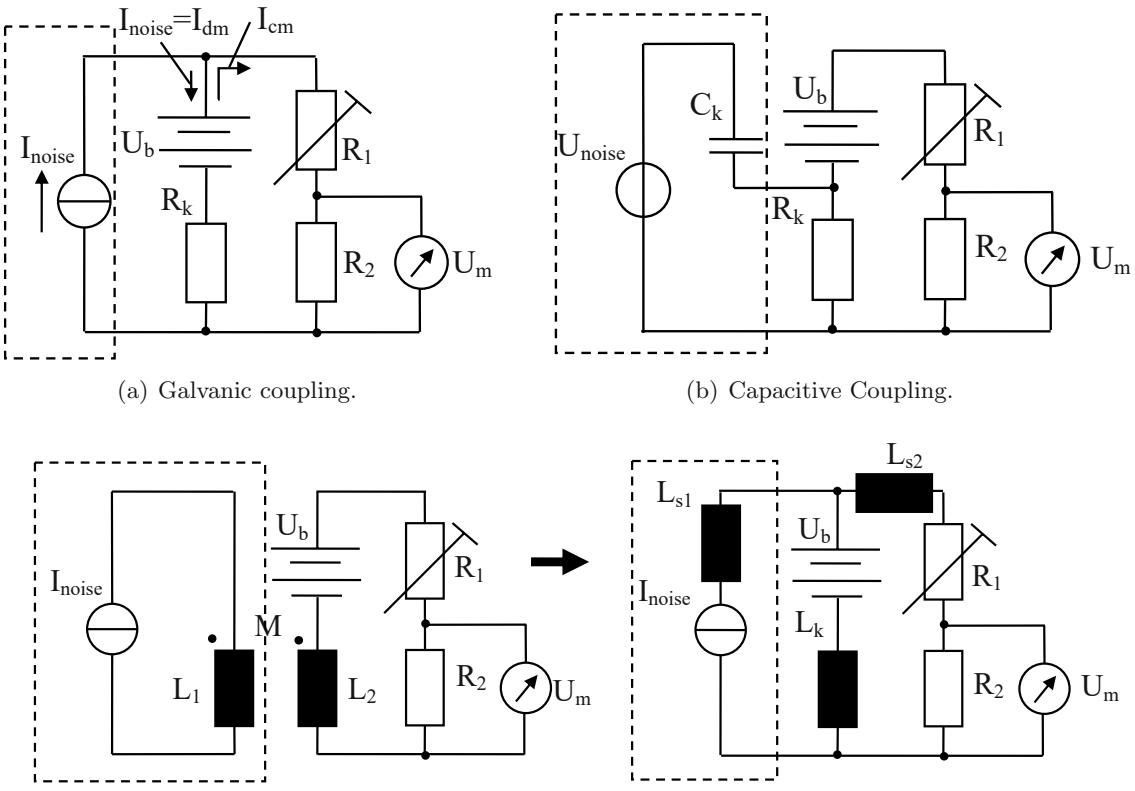
when this cable cannot be modified by the PCB designer and, especially, when the PCB should be connected to different cables in different applications, a simulation result including these resonances is misleading. The PCB emission optimization can be performed more efficiently by omitting the cable, just by simulating the coupling impedances. A separate simulation of the antenna can be used for quantitative prediction simulations. According to [62], the maximum radiated far field from cables can be estimated roughly with a simple line resonator model. The estimated maximum electric fields from monopol and dipole antennas at their resonance are [62]

$$E_{max}^{res} \approx (60\Omega) \cdot \frac{I_{ant}}{r} \quad \Longleftrightarrow \quad E_{max}^{res} \approx \frac{U_{ant}}{r} \cdot \begin{cases} 1.64 & \text{(monopol.)} \\ 0.82 & \text{(dipol.)} \end{cases} \tag{3.4}$$

U_{ant} and I_{ant} are the antenna voltage and the antenna current, respectively, and r is the distance of the field observation point from the antenna position.



(a) Galvanic coupling.

(b) Capacitive Coupling.

(c) Inductive Coupling.

Figure 3.3: The coupling mechanisms between an emission source circuit and another circuit. The dotted frame marks the source circuit branch.

The coupling can be interpreted as an unwanted common mode coupling. This is shown in Figure 3.3(a), where the current through the victim circuit is denoted as the common mode current I_{cm}, which flows in the same direction as the current in the source path I_{noise}. The voltage and the current driven common mode coupling from traces on the PCB to attached cables, as described in [40], are also common impedance couplings. For the current driven mode the common mode inductance of a trace has been formulated by [35], [59] and for the voltage driven mode the common mode capacitance by [38], [39], both independent of a cable attached to the PCB. Section 5.7 links the field coupling of PCB sources to the cavity field

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between the PCB ground plane and a parallel metallic cover plane to the common mode coupling described in [35].

In the following an example for common impedance coupling in a power delivery network is presented. Every real power supply has a nonzero impedance. Thus, currents from one device cause a voltage noise on that impedance, which is conducted to other devices connected to the same power supply. An example is an automotive control device connected to the board power net which also supplies many other electronic devices. Another example is a three-phase converter for an electric drive, supplied from a transformer station which might supply a whole village. Figure 3.4 depicts a push-pull switching stage, supplied from a battery, which also supplies a sensitive sensor circuit. Power supply noise generated from the switching circuit couples to the sensitive circuit through a non zero resistive impedance of the power supply R1 and an inductive coupling of the loops considered with a coupling factor K1 which partly couples the inductance of the source path L3 and the inductance of the victim path L6. As an alternative to the coupling factor, one could also consider the inductive coupling with an inductance in series to the resistor R1. Note that common impedance coupling

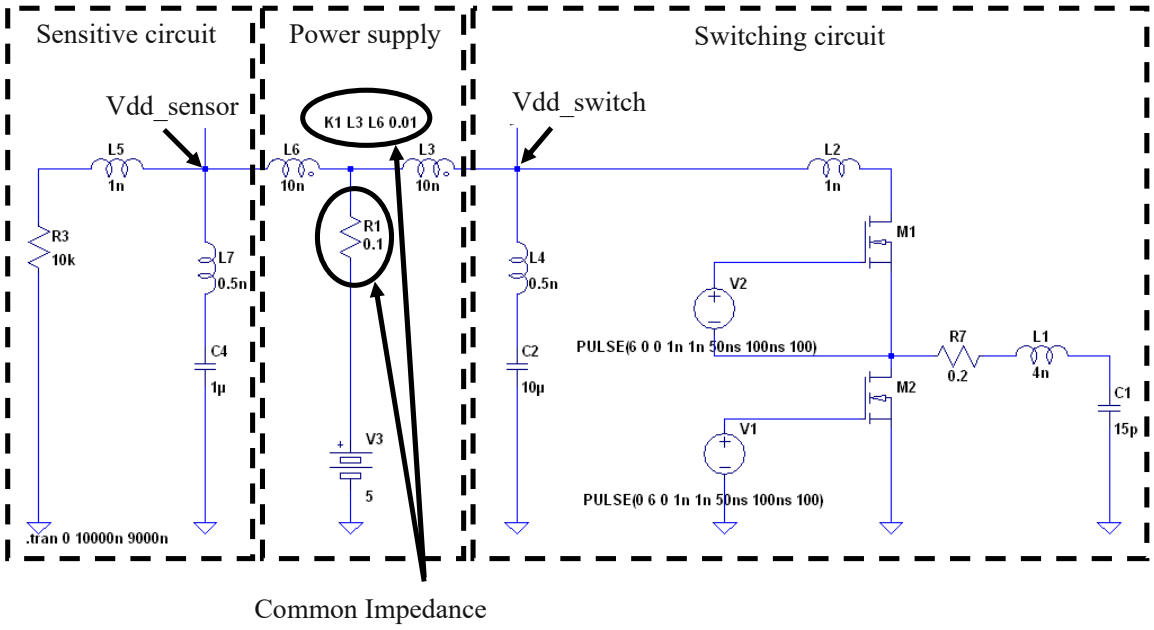

Figure 3.4: Example for conducted emissions. The supply noise of a push-pull stage is conducted to a sensitive sensor circuit, connected to the same power supply. Simulation setup in LTSpice [63].

occurs not only on the plus branch of the supply. Common impedances are also in the ground branch. Low impedance grounding and separate ground routing to a star point are measures to minimize the coupling in the ground branch. The supply in Figure 3.4 is decoupled with low inductive capacitances, both in the source and also in the victim path. Low inductance can be achieved by capacitors with low equivalent series inductance (ESL), or by a parallel connection of multiple capacitors with the same capacitance value. The simulation of the model was carried out with LTSpice [63]. After a time domain transient analysis a FFT is performed with Barlett-Hann windowing to obtain the frequency domain power supply noise. Figure 3.5 depicts the simulation result for the supply noise at the sensor supply connection and the supply connection of the switching circuit. Although decoupling significantly reduces the supply noise at the sensitive circuit, emission can be observed. Further noise reduction

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at the sensitive circuit requires additional decoupling and filtering.

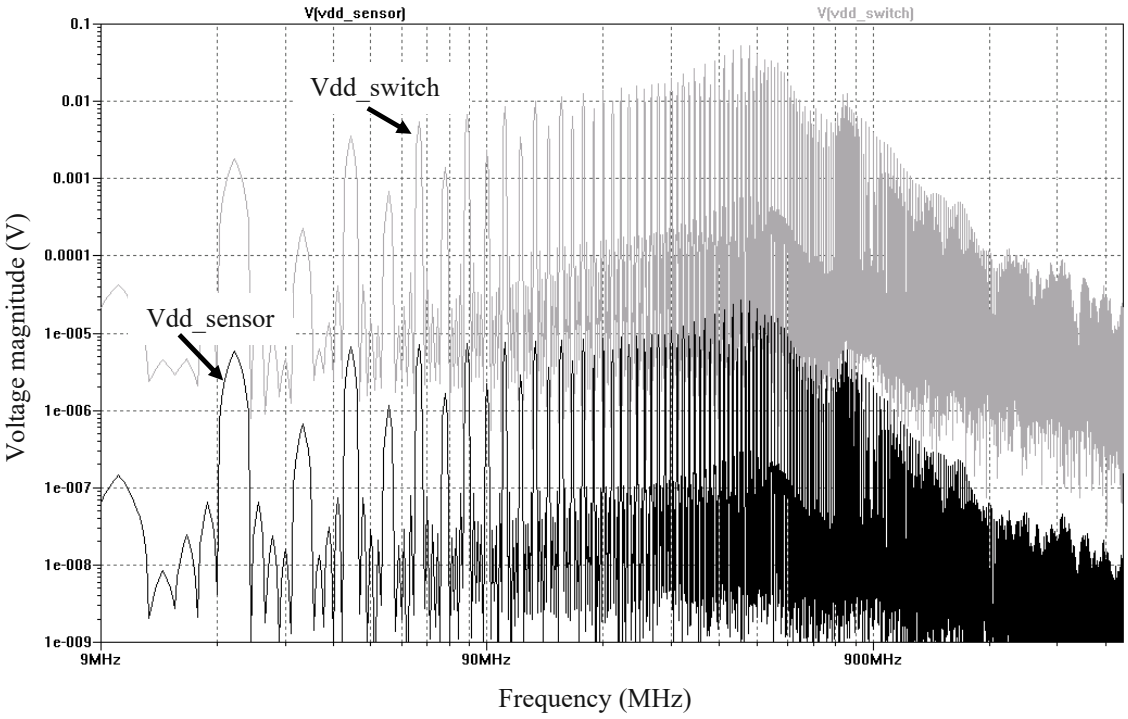

Figure 3.5: Simulation result of the model in Figure. 3.4. Common impedance coupling at a shared power supply causes conducted power noise at a sensitive circuit.

Like in this example, standard network simulation is generally performed to describe conducted emissions from common impedance coupling. The circuit model has to consider the parasitics of the power delivery network, the models of filter and decoupling components, and models for the emission sources. Noise sources are all current switching components, such as, inverters for AC motors, switched power supplies, or core noise generated from a microcontroller. Accurate models of these sources are necessary for the emission simulation, because even a slight change of the transient current shape may change the spectrum significantly. Standardized ICEM models are used for the accurate simulation of the supply noise from integrated circuits [60], [61]. An accurate and efficient EMC modeling technique for discrete components was presented in [64]. The passive power delivery network on the PCB can be extracted, for example, with the methods in [42], [43], [65]. Models for power cabling can be obtained for uniform cabling with transmission line theory and for non-uniform cables with three-dimensional simulation, for example, with the method in [30].

The next part contains the development of a cavity model for the efficient simulation of the emissions from a printed circuit board under a metallic enclosure cover. The model enables the explicit calculation of the common mode coupling impedances from printed circuit board structures to the interface at the apertures of the enclosure. This provides the opportunity to optimize the interior of the device independent of the external environment.

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4. Cavity model of the electromagnetic field between PCB and metallic cover

4.1. Derivation of the two-dimensional Helmholtz equation model

Figure 4.1 depicts a cross-section of the volume between a PCB ground plane and a metallic cover. This volume contains the metallic layout structures on the PCB, the active and passive components, metallic cooling structures, thin sheets of PCB dielectric material, and for the most part air. In case of a PCB stack the metallic cover plane is given by the ground plane of the parallel PCB.

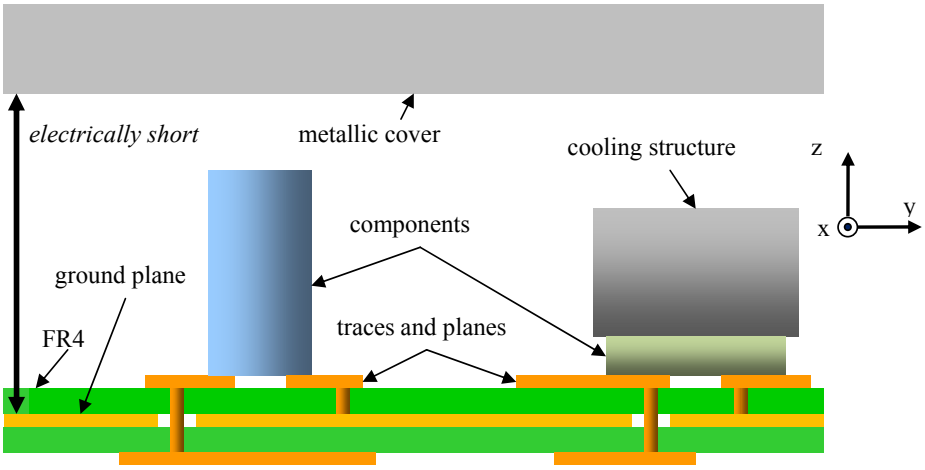

Figure 4.1: Cross-section of the volume between the PCB ground plane and the metallic enclosure cover.

All metallic PCB layout structures, the components on the PCB, and metallic cooling devices will be introduced into the field formulation by excitation ports in a second step and, thus, these parts are neglected for the derivation of the cavity field equation. Therefore, the field is derived for a volume that contains only isolating dielectric layers. The first and the third Maxwell equations for harmonic signals

$$\vec{\nabla} \times \vec{E} = -j\mu\omega\vec{H}, \qquad \vec{\nabla} \times \vec{H} = \vec{J} + j\epsilon\omega\vec{E} \tag{4.1}$$

are combined to

$$\vec{\nabla}(\vec{\nabla} \cdot \vec{E}) - \vec{\nabla}^2\vec{E} = -j\mu\omega\vec{J} + \mu\epsilon\omega^2\vec{E}. \tag{4.2}$$

Where $\vec{E}$ is the electrical field strength, $\vec{J}$ is the current density, ϵ is the permittivity of the layer, μ is the permeability of the layer and $\omega = 2\pi f$, with the frequency f.
The dielectric layers of such applications (air, FR4,...) are usually homogenous regarding their macroscopic electrical parameters. Therefore, there are no charges ($\vec{\nabla} \cdot \vec{E} = 0$) inside

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one layer and the first term of (4.2) vanishes, leading to the three-dimensional, vectorial Helmholtz equation

$$\vec{\nabla}^2\vec{E} + \mu\epsilon\omega^2\vec{E} = j\mu\omega\vec{J}. \tag{4.3}$$

Equation (4.3) is general for homogenous materials without volume charges. It can be reduced to a scalar two-dimensional Helmholtz equation by the following conditions:

$$\text{Perfect conducting cover and ground plane: } \vec{n}\times\vec{E} = 0 \qquad E_x = E_y = 0 \tag{4.4}$$

$$\text{Electrically small cover to ground plane distance: } \qquad \frac{\partial}{\partial z} = 0 \tag{4.5}$$

Condition (4.4) is reasonable for emission simulation of enclosures, because the main loss mechanism is the radiation loss from the enclosure slots, which dominates compared to the conduction loss of the metallic planes [45]. However, conduction and dielectric losses will be considered in the cavity model, without noticeable violation of the condition.
Condition (4.5) limits the frequency range for the model. Table 4.1 list the frequency limits for some cover to ground plane distances based on the often used $\lambda/10$ lumped element criterion and the more tolerable $\lambda/8$ condition for short antennas. The table demonstrates that the whole CISPR25 frequency range of 2.5GHz is covered up to a plane separation of 15mm and nearly covered up to 20mm. The maximum frequency limit is beyond 1 GHz even at a plane separation distance of 30mm.

Plane separation (mm)	3.0	5.0	7.0	10.0	12.0	15.0	20.0	30.0
$\lambda/10$ limit (GHz)	10.0	6.0	4.3	3.0	2.5	2.0	1.5	1.0
$\lambda/7$ limit (GHz)	12.5	7.5	5.4	3.8	3.1	2.5	1.9	1.3

Table 4.1: Frequency limits of the cavity model for several plane separation distances.

The two-dimensional, scalar, and lossless Helmholtz equation for the cavity field inside the enclosure is

$$\Delta E_z + k^2_{lossless}E_z = j\mu\omega J_z \qquad \text{with} \qquad k_{lossless} = \omega\sqrt{\mu\epsilon}. \tag{4.6}$$

A formulation for the voltage U on the planes is obtained by multiplying (4.6) with the plane separation distance h:

$$\Delta U + \mu\epsilon\omega^2 U = j\mu\omega h J_z. \tag{4.7}$$

Equation (4.6) is expressed as a two-dimension transmission line equation

$$\Delta U + L'_c C'_c\omega^2 U = j\omega L'_c J_z, \tag{4.8}$$

with

$$L'_c = \mu h \quad \text{and} \quad C'_c = \frac{\epsilon}{h}. \tag{4.9}$$

According to transmission line theory, the introduction of conduction and dielectric losses into (4.8) yields

$$\Delta U + [\omega^2 L'_c C'_c - j(C'_c R'_c + L'_c G'_c) - R'_c G'_c]U = (j\omega L'_c + R'_c)J_z. \tag{4.10}$$

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The surface resistance which considers conduction losses is

$$R'_c = R_{c_1} + R'_{c_2} \quad \text{where} \quad R_{c_i} = \begin{cases} 1/(t_{s_i}\sigma_i) & \text{,if } t_{s_i} < t \\ 1/(t_{c_i}\sigma_i) & \text{,if } ts \geq t_{c_i} \end{cases} \quad \text{with} \quad t_{s_i} = \sqrt{\frac{2}{\omega\mu\sigma_i}}. \tag{4.11}$$

Where R_{c_1} and R_{c_2} are the surface resistances of the lower and upper plane respectively. With i=1 and i=2 for the two planes, t_{c_i} is the plane thickness, σ_i is the conductivity of the plane metal, and t_{s_i} is the skin depth of the plane. The dielectric losses of the isolation layer are considered in (4.10) by

$$G'_c = \omega C'_c \tan(\delta). \tag{4.12}$$

Where $\tan(\delta)$ is the loss tangent of the material. To meet the requirement (4.4), the term $R'_c G'_c$ of (4.10) must be small compared to $k_{lossless}$. On the right hand side term $(j\omega L'_c + R'_c)$, R'_c must be small compared to $j\omega L'_c$. This is in fact the case for the indented application of the method, because of the highly conducting metallic planes and the significant portion of air in the volume. Therefore, these terms can be neglected. With this simplification (4.9) and (4.12), the equation for the voltage distribution inside the cavity, becomes

$$\Delta U + \omega^2\mu\epsilon\left(1 - \frac{j}{Q(\omega)}\right)U = j\omega\mu h J_z \qquad \text{with} \qquad Q(\omega) = \frac{1}{\frac{R'_c}{\mu\omega h} + tan(\delta)}. \tag{4.13}$$

$Q(\omega)$ is the total quality factor which considers the conduction and the dielectric losses. Finally, the Helmholtz equation for the electric field strength, which considers conduction and dielectric losses is

$$\Delta E_z + \omega^2\mu\epsilon\left(1 - \frac{j}{Q(\omega)}\right)E_z = j\omega\mu h J_z. \tag{4.14}$$

4.1.1. Boundary condition at the edges of the parallel planes

At the edges of the cavity boundary-conditions have to be considered for the solution of (4.13). The Dirichlet condition

$$U\Big|_{\mathcal{C}} = 0 \quad \text{, for perfect electric conducting (PEC) boundaries } \mathcal{C}, \tag{4.15}$$

is used for closed metallic enclosure walls. The Neumann condition

$$\vec{n} \cdot \vec{\nabla} U\Big|_{\mathcal{C}} = 0 \quad \text{, for perfect magnetic conducting (PMC) boundaries } \mathcal{C}, \tag{4.16}$$

is used to consider open boundaries without losses, because it enforces a vanishing current flow perpendicular to the boundary edge segment. The normal vector on the edge curve $\mathcal{C}$ is $\vec{n}$.
Other boundary conditions can be considered by the introduction of excitation ports at the boundary edge in addition to one of the two mentioned boundary conditions. PMC boundary conditions (4.16) are used in Chapter 6 together with ports at the boundary to establish an interface to the external environment of the device, which enables a separate simulation of the internal and external device domains.

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4.1.2. Summary of the cavity model equations

Cavity model equations			Reference
$L'_c = \mu h$	$C'_c = \frac{\epsilon}{h}$		(4.9)
$R'_c = R_{c_1} + R_{c_2}$	$R_{c_i} = \begin{cases} 1/(t_{s_i}\sigma_i) & \text{,if } t_{s_i} < t \\ 1/(t_{c_i}\sigma_i) & \text{,if } ts \geq t_{c_i} \end{cases}$	$t_{s_i} = \sqrt{\frac{2}{\omega\mu\sigma_i}}$	(4.11)
$G'_c = \omega C'_c \tan(\delta)$			(4.12)
$\Delta U + \omega^2\mu\epsilon\left(1 - \frac{j}{Q(\omega)}\right)U = j\omega\mu h J_z$	$Q(\omega) = \frac{1}{\frac{R'_c}{\mu\omega h} + tan(\delta)}$		(4.13)
$\Delta E_z + \omega^2\mu\epsilon\left(1 - \frac{j}{Q(\omega)}\right)E_z = j\omega\mu h J_z$			(4.14)
$U\Big\vert_{\mathcal{C}} = 0$	PEC boundaries		(4.15)
$\vec{n}\cdot\vec{\nabla}U\Big\vert_{\mathcal{C}} = 0$	PMC boundaries		(4.16)

4.2. Analytical solution methods for the two-dimensional Helmholtz equation

A solution of (4.13) with n_{port} excitation ports, defined between the cover and the bottom plane (Figure 4.2), relates the port voltages $U_i(x_i, y_i)$ on the ports with index i to the currents $I_j(x_j, y_j)$ on the ports with index j by the impedance matrix Z_{ij}. The coordinates of port i and port j are (x_i, y_i) and (x_j, y_j) respectively.

$$U_i(x_i, y_i) = \sum_{j=1}^{n_{port}} (Z_{ij}(x_i, y_i, x_j, y_j) I_j(x_j, y_j)) \qquad \text{with} \qquad i = 1 \ldots n_{port}. \tag{4.17}$$

An analytical solution for rectangular parallel planes with four open edges depicted in Figure 4.2 was presented by [42]. In this solution, the coefficients of the impedance matrix in (4.17) are

$$Z_{ij} = \frac{j\omega\mu h}{L_e W_e} \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[\frac{L_{mn} N_{mni} N_{mnj}}{k_m^2 + k_n^2 - k^2}\right], \tag{4.18}$$

with

$$N_{mni} = \cos(k_m x_i)\cos(k_n y_i)\,\mathrm{sinc}\left(\frac{k_m W x_i}{2}\right)\mathrm{sinc}\left(\frac{k_n W y_i}{2}\right), \tag{4.19}$$

$$N_{mnj} = \cos(k_m x_j)\cos(k_n y_j)\,\mathrm{sinc}\left(\frac{k_m W x_j}{2}\right)\mathrm{sinc}\left(\frac{k_n W y_j}{2}\right), \tag{4.20}$$

$$k_m = \frac{m\pi}{L_e},\ k_n = \frac{n\pi}{W_e},\ L_e = L + \frac{h}{2},\ W_e = W + \frac{h}{2}, \tag{4.21}$$

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$$L_{mn} = \begin{cases} 1 & \text{, if } m = 0 \vee n = 0, \\ 2 & \text{, if } (m \neq 0 \vee n = 0) \wedge (m = 0 \vee n \neq 0), \\ 4 & \text{, if } m \neq 0 \vee n \neq 0, \end{cases} \tag{4.22}$$

and

$$\mathrm{sinc}(x) = \frac{\sin(x)}{x}. \tag{4.23}$$

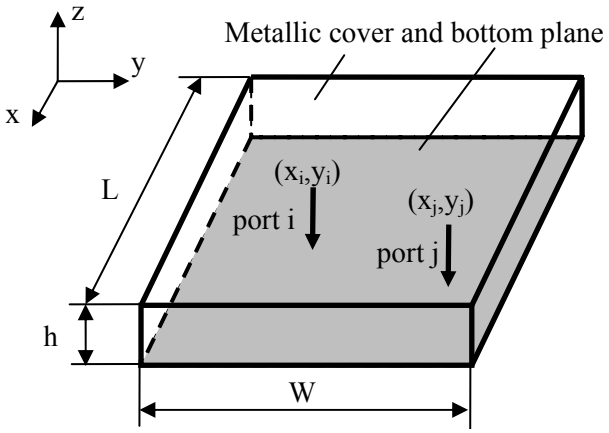

Figure 4.2: Rectangular, parallel metallic planes with four open edges. Equation (4.18) contains the port impedance matrix elements.

In (4.18) $k = \omega/c_l$ denotes the wave number, with the speed of light c_l. L_e and W_e are the effective plane length and width, respectively. These effective dimensions consider the fringing fields at the cavity edges according to [45]. [43] also provides an analytical solution for equilateral triangular parallel planes with three open edges. Chapter 7 of this work presents an analytical solution for rectangular parallel planes with one open and three closed edges. This is a powerful solution for predesign investigations of the radiated emissions from the slot of a slim cubical enclosure, because discussion of the bias functions of the model provides direct information about the influence of the source position on the emission level.
The analytical method of [43] enables the calculation of parallel plane cavities with fairly arbitrary shapes by connecting rectangular or equilateral triangular parallel-plane segments. This method is illustrated in Figure 4.3.

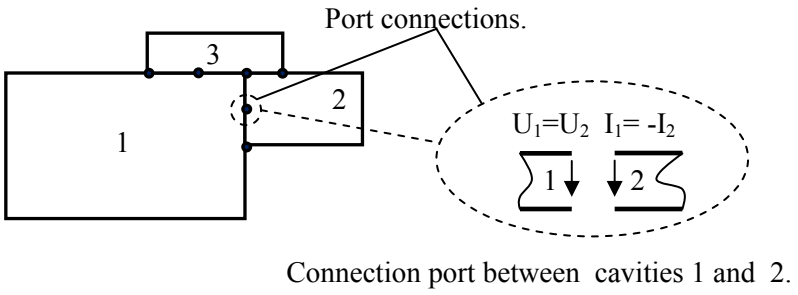

Figure 4.3: Three rectangular cavities are connected together with interface ports.

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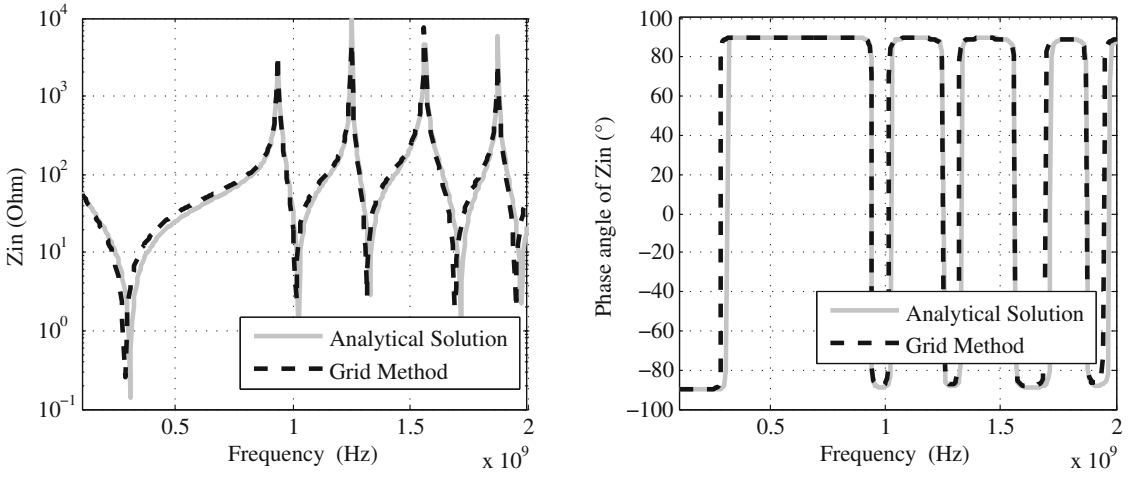
4.3. Inductance, capacitance, resistance (LCR) grid solution method for the two-dimensional Helmholtz equation

Through cartesian discretization of the differential operator in (4.13), [66] obtained a finite difference method on a rectangular grid. With interpretation according to the TLM method [67], [68], a method with lumped inductances, capacitances, resistances and admittances on a rectangular mesh was presented by [65] and [69]. The value for the lumped resistance is obtained from (4.11) and that for the lumped admittance from (4.12). The value of the lumped inductance is calculated directly from (4.9), while the lumped capacitance is obtained by multiplication of the capacitance from (4.9) with $\Delta x \Delta y$. Δx and Δy denote the rectangular grid cell lengths in x-direction and in y-direction, respectively. Other circuit elements can be introduced easily at every point of the grid. The circuit structure of the lumped elements on the grid leads to a sparse matrix. However, a very fine grid has to be used to obtain reasonably good accuracy. Figure 4.4 depicts a comparison of the analytic results from (4.18) to the LCR grid method results for the impedance Z_{in} of a port at position ($x = 10mm$, $y = 10mm$) on a rectangular cavity with dimensions $L = 160mm$, $W = 120mm$ and $h = 7mm$. A grid spaciny of $\Delta x = \Delta y = 2mm$ was used for the LCR grid method simulation. Even with that fine grid the comparison shows some slight deviations of the impedance magnitude minima, which indicate a small inaccuracy of simulated inductance. This is a disadvantage of the method, because the necessity of the fine grid leads to higher simulation costs compared to the FEM method in Section 4.4.
Rectangular planes have been used for the comparison in Figure 4.4 to enable the comparison with the analytical solution. When the method is used for planes with edges that are not parallel to one of the cartesian directions $\vec{e}_x$ or $\vec{e}_y$, a dense grid will be necessary to obtain an accurate discretization of the geometry at that edge. Although sub-gridding at the edge is an opportunity to reduce the overall mesh size, the effort for geometry discretization is much higher compared to the finite element method in Section 4.4, which uses triangular meshing.



(a) Magnitude comparison.

(b) Phase angle comparison.

Figure 4.4: Comparison of Z_{in} between the analytical solution (4.18) and the LCR grid method solution. Cavity dimensions are ($L = 160mm$, $W = 120mm$, $h = 7mm$), the position of the port for the Z_{in} is ($x = 10mm$, $y = 10mm$) and the grid spacing is $\Delta x = \Delta y = 2mm$.

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4.4. FEM solution for the two-dimensional Helmholtz equation

Finite element methods (FEM), initially developed for structural mechanics [70], are widely used for numerical simulations of electromagnetic fields [15], [23], [71], [72], [73]. Some advantages of the finite element method are listed below.

- ➢ A sparse system matrix enables the simulation of problems with a large number of unknowns.
- ➢ Suitable for inhomogeneous simulation domains.
- ➢ Adaptability to arbitrary geometries by triangular meshes for two-dimensional simulations and tetrahedral meshes for three-dimensional problems.
- ➢ Suitable for inhomogeneous simulation domains.
- ➢ Existence of an unambiguous solution for elliptical partial differential equations. This means convergence of the solution error towards zero with mesh refinement.

The finite element method provides an approximate solution $\tilde{U}$ for the elliptical partial differential equation (4.13). The residuum (approximation error) of this solution is

$$Res = \Delta\tilde{U} + \omega^2\mu\epsilon\left(1 - \frac{j}{Q(\omega)}\right)\tilde{U} + j\omega\mu h J_z. \tag{4.24}$$

For consistence to the voltage and current directions, defined by the impedance matrix in (4.17), a negative sign has been used for the current density J_z, as opposed to the sign in (4.13). The residuum Res, weighted with a function W_g, will vanish on average over the simulation domain. This is expressed in the variation integral

$$\int_{\mathcal{A}}\left(\Delta\tilde{U} + \omega^2\mu\epsilon\left(1 - \frac{j}{Q(\omega)}\right)\tilde{U} + j\omega\mu h J_z\right)W_g \,\mathrm{d}\mathcal{A} = 0. \tag{4.25}$$

$\mathcal{A}$ denotes the whole simulation domain, that is, the parallel plane surface. Applying Green's theorem, (4.25) is transformed to the weak formulation

$$\int_{\mathcal{A}}\left(\vec{\nabla}\tilde{U}\cdot\vec{\nabla}W_g - \omega^2\mu\epsilon\left(1 - \frac{j}{Q(\omega)}\right)\tilde{U}W_g\right)\mathrm{d}\mathcal{A} - \int_{\partial\mathcal{A}}\left(W_g\frac{\partial}{\partial_n}\tilde{U}\right)\mathrm{d}s = \int_{\mathcal{A}}\left(j\omega\mu h J_z W_g\right)\mathrm{d}\mathcal{A}. \tag{4.26}$$

$\partial\mathcal{A}$ is the boundary curve of the parallel plane surface $\mathcal{A}$, $\mathrm{d}s$ is the line segment of this boundary curve and $\partial/\partial_n\tilde{U}$ is the normal derivation of $\tilde{U}$ at the boundary. $\tilde{U}$ is expressed by

$$\tilde{U} = \sum_{k=1}^{p}\alpha_k(x,y)\tilde{u}_k. \tag{4.27}$$

Where α_k denote the finite element base functions, $\tilde{u}_k$ are the values of the solution at the mesh points, and p denotes the number of mesh nodes. According to the method of Galerkin, the weighting function is

$$W_g = \sum_{k=1}^{p}\alpha_k(x,y). \tag{4.28}$$

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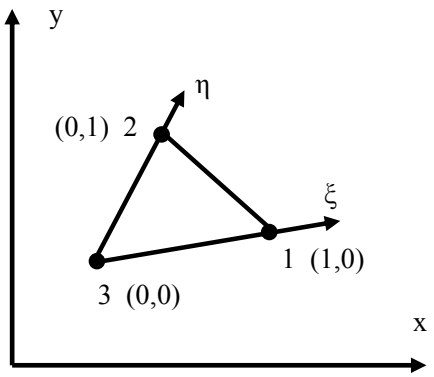

Figure 4.5: Barycentric (triangular) coordinates ξ and η. Coordinates (ξ,η) become (1,0), (0,1), and (0,0) in the nodes 1, 2, and 3, respectively.

Linear base functions on a triangular mesh are selected for the finite element discretization. Barycentric coordinates are utilized according to Figure 4.5.
With this coordinate system definition the base functions are

$$\alpha_1 = \xi,\ \alpha_2 = \eta,\ \text{and}\ \alpha_3 = 1 - \xi - \eta, \tag{4.29}$$

with indexes according to the triangle node numbers in Figure 4.5. The relation of the barycentric to the cartesian coordinates of the triangular nodes is

$$\begin{pmatrix}\xi_i\\ \eta_i\\ \zeta_i\end{pmatrix} = \frac{1}{2A_i}\begin{pmatrix}a_{1i} & b_{1i} & c_{1i}\\ a_{2i} & b_{2i} & c_{2i}\\ a_{3i} & b_{3i} & c_{3i}\end{pmatrix}\begin{pmatrix}1\\ x\\ y\end{pmatrix} = \frac{1}{2A_i}\begin{pmatrix}x_{2i}y_{3i} - x_{3i}y_{2i} & y_{2i} - y_{3i} & x_{3i} - x_{2i}\\ x_{3i}y_{1i} - x_{1i}y_{3i} & y_{3i} - y_{1i} & x_{1i} - x_{3i}\\ x_{1i}y_{2i} - x_{2i}y_{1i} & y_{1i} - y_{2i} & x_{2i} - x_{1i}\end{pmatrix}\begin{pmatrix}1\\ x\\ y\end{pmatrix}, \tag{4.30}$$

with

$$A_i = \frac{1}{2}\,\text{abs}\begin{vmatrix}1 & x_{1i} & y_{1i}\\ 1 & x_{2i} & y_{2i}\\ 1 & x_{3i} & y_{3i}\end{vmatrix}. \tag{4.31}$$

A_i is the surface area of the triangle with index i. With equations (4.27) and (4.28), (4.26) becomes the linear equation system

$$\mathbf{K}\tilde{\mathbf{U}} - \mathbf{R}\tilde{\mathbf{U}}_n = \mathbf{F}, \tag{4.32}$$

for the voltages $\tilde{\mathbf{U}}$ on the mesh nodes. $\tilde{\mathbf{U}}_n$ denotes the vector of the normal derivatives of $\tilde{\mathbf{U}}$ at the boundary. At open boundaries the PMC boundary condition requires vanishing $\tilde{\mathbf{U}}_n$. On closed metallic edges a Dirichlet boundary has to be introduced, by setting the boundary node voltage to zero and reducing the order of the linear system accordingly. Since the weighting function is set to zero in the boundary nodes with Dirichlet condition, the term with $\tilde{\mathbf{U}}_n$ vanishes also at Dirichlet boundaries and (4.32) is reduced to

$$\mathbf{K}\tilde{\mathbf{U}} = \mathbf{F}. \tag{4.33}$$

The system matrix elements K_{kl} are obtained from the solution of

$$K_{kl} = \int_{\mathcal{A}} \left[\vec{\nabla}\alpha_k \cdot \vec{\nabla}\alpha_l - \omega^2\mu\epsilon\left(1 - \frac{j}{Q(\omega)}\right)\alpha_k\alpha_l\right] \mathrm{d}\mathcal{A}. \tag{4.34}$$

The term $\vec{\nabla}\alpha_k \cdot \vec{\nabla}\alpha_l$ in(4.34) becomes

$$\vec{\nabla}\alpha_k \cdot \vec{\nabla}\alpha_l = \left(\frac{\partial\alpha_k}{\partial x}\vec{e}_x + \frac{\partial\alpha_k}{\partial y}\vec{e}_y\right)\cdot\left(\frac{\partial\alpha_l}{\partial x}\vec{e}_x + \frac{\partial\alpha_l}{\partial y}\vec{e}_y\right) = \frac{\partial\alpha_k}{\partial x}\frac{\partial\alpha_l}{\partial x} + \frac{\partial\alpha_k}{\partial y}\frac{\partial\alpha_l}{\partial y}. \tag{4.35}$$

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With the base functions

$$\alpha_k = \xi \text{ and } \alpha_l = \eta \tag{4.36}$$

and (4.30), the partial derivatives of (4.35) become

$$\begin{aligned}
\frac{\partial \alpha_k}{\partial x} &= \frac{\partial \alpha_k}{\partial \xi}\frac{\partial \xi}{\partial x} = \frac{b_{ki}}{2A_i} \\
\frac{\partial \alpha_l}{\partial x} &= \frac{\partial \alpha_l}{\partial \xi}\frac{\partial \xi}{\partial x} = \frac{b_{li}}{2A_i} \\
\frac{\partial \alpha_k}{\partial y} &= \frac{\partial \alpha_k}{\partial \xi}\frac{\partial \xi}{\partial y} = \frac{c_{ki}}{2A_i} \\
\frac{\partial \alpha_l}{\partial y} &= \frac{\partial \alpha_k}{\partial \xi}\frac{\partial \xi}{\partial y} = \frac{c_{li}}{2A_i}.
\end{aligned} \tag{4.37}$$

Using these partial derivatives expressions (4.34) becomes

$$K_{kl} = \int_{\mathcal{A}} \left[\frac{b_{ki}b_{li} + c_{ki}c_{li}}{4A_i^2} - \omega^2 \mu\epsilon \left(1 - \frac{j}{Q(\omega)}\right) \xi\eta \right] \mathrm{d}\mathcal{A}. \tag{4.38}$$

Utilizing

$$\int_{\mathcal{A}} \xi^a \eta^b \zeta^c \mathrm{d}\mathcal{A}_i = 2\mathcal{A}_i \frac{a!b!c!}{(a+b+c+2)!}, \tag{4.39}$$

from [23], the integral of (4.38) is solved analytically and the coefficients of the FEM matrix K_{kl} finally become

$$K_{kl} = \sum_{i=1}^{p} \left[\frac{b_{ki}b_{li} + c_{ki}c_{li}}{4A_i} - \omega^2 \mu\epsilon \left(1 - \frac{j}{Q(\omega)}\right) K_{kli}^{(1)} \right] \tag{4.40}$$

with

$$K_{kli}^{(1)} = \begin{cases} A_i/6 & \text{,if } k = l \\ A_i/12 & \text{,if } k \neq l. \end{cases} \tag{4.41}$$

At the node position (x_l, y_l) the port excitation current is

$$J_z(x, y) = I_l \delta(x_l, y_l). \tag{4.42}$$

$\delta(x_l, y_l)$ is the Dirac pulse function and l is the node index running from one to the number of nodes p. With (4.26), (4.28), (4.36), and (4.42), the coefficients of the excitation vector $\mathbf{F}$ in (4.33) become

$$F_l = \int_{\mathcal{A}} (j\omega\mu h I_l \delta(x_l, y_l)\eta)\, \mathrm{d}\mathcal{A} = j\omega\mu h I_l, \tag{4.43}$$

because the weighting function η is unity at node position (x_l, y_l) according to the base function definition in (4.29). With this port current excitation definition the impedance matrix, which relates the voltages on the mesh nodes to the node excitation currents, is

$$\mathbf{Z} = j\omega\mu h \mathbf{K}^{-1}. \tag{4.44}$$

Figure 4.6 depicts a comparison of the analytic results from (4.18) to the FEM results for the impedance Z_{in} of a port at position $(x = 10mm, y = 10mm)$ on a rectangular cavity with dimensions $L = 160mm$, $W = 120mm$ and $h = 7mm$. Although this FEM simulation was carried out using a very coarse mesh with $\Delta x = \Delta y = 10mm$, the results of this simulation match the analytical solution well. Thus, the proposed FEM method provides an efficient and accurate solution for arbitrarily shaped parallel plane cavities. In the case of a large number

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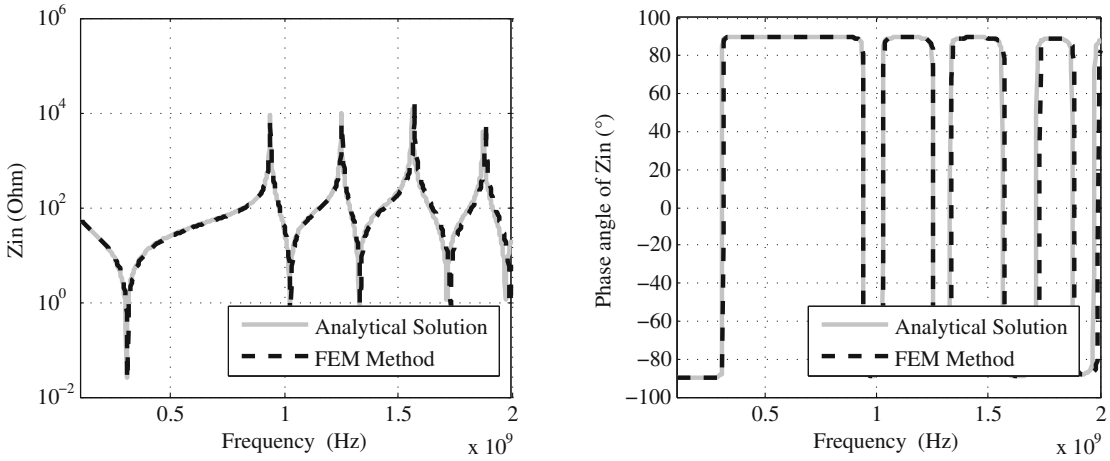
of excitation ports, the FEM method is even more efficient than the analytical solution. While the analytical method requires the calculation of the double sum term in (4.18) for each coefficient in the port impedance matrix (4.17), the FEM solution requires only one inversion of the sparse system matrix $\mathbf{K}$. Linear base functions and a triangular mesh enable an efficient, analytical composition of the system matrix $\mathbf{K}$ and the excitation vector $\mathbf{F}$ with (4.40) and (4.43) respectively. Since a high accuracy is achieved with the linear base functions even on a coarse mesh, there is no need for higher order base functions. Table 4.2 contains a summary of the FEM equations.



(a) Magnitude comparison.

(b) Phase angle comparison.

Figure 4.6: Comparison of Z_{in} between the analytical solution (4.18) and the FEM solution. Cavity dimensions are ($L = 160mm$, $W = 120mm$, $h = 7mm$), the position of the port for the Z_{in} is ($x = 10mm$, $y = 10mm$) and the mesh spacing is $\Delta x = \Delta y = 10mm$.

In the following the FEM equations are summarized.

FEM equations		Reference
$\mathbf{K}\tilde{\mathbf{U}} = \mathbf{F}$		(4.33)
$\mathbf{Z} = j\omega\mu h\mathbf{K}^{-1}$		(4.44)
$K_{kl} = \sum_{i=1}^{p}\left[\frac{b_{ki}b_{li}+c_{ki}c_{li}}{4A_i} - \omega^2\mu\epsilon\left(1-\frac{j}{Q(\omega)}\right)K_{kli}^{(1)}\right]$	$K_{kli}^{(1)} = \begin{cases} A_i/6 & \text{,if } k=l \\ A_i/12 & \text{,if } k\neq l \end{cases}$	(4.40)
$F_l = j\omega\mu h I_l$		(4.43)
$\begin{pmatrix} b_{1i} & c_{1i} \\ b_{2i} & c_{2i} \\ b_{3i} & c_{3i} \end{pmatrix} = \begin{pmatrix} y_{2i}-y_{3i} & x_{3i}-x_{2i} \\ y_{3i}-y_{1i} & x_{1i}-x_{3i} \\ y_{1i}-y_{2i} & x_{2i}-x_{1i} \end{pmatrix}$		(4.30)

Table 4.2: Summary of the FEM equations.

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5. Introduction of sources and PCB layout structures to the cavity model

Efficient power integrity analysis with cavity models for rectangular power planes obtained from (4.13) and (4.14) have been presented by [42] and [43]. While power-ground planes are excited by currents, which are galvanically supplied to the planes, an enclosure is excited by common mode coupling from a PCB trace to the cavity between the ground plane and the cover. Since the models (4.13) and (4.14) can only be excited by currents supplied to the planes, the common mode coupling of a trace also has to be introduced into these models by current sources, connected to the upper and lower plane.
According to conditions (4.4) and (4.5) only the TMzm (magnetic field transversal in the z direction) mode m=0 is considered in the cavity model and the electric field has thus only a z-component. This is also sufficient in case of a trace within the cavity, because higher order parallel plate modes, excited by the horizontal trace current, decay rapidly and cannot reach the surrounding edges. Therefore, any horizontal current can be neglected and the vertical trace currents at the source (s) and load (l) positions (Figure 5.1) couple to the cavity. Excitations are introduced into the cavity model (4.13) by vertical currents on ports between the upper and lower plane.

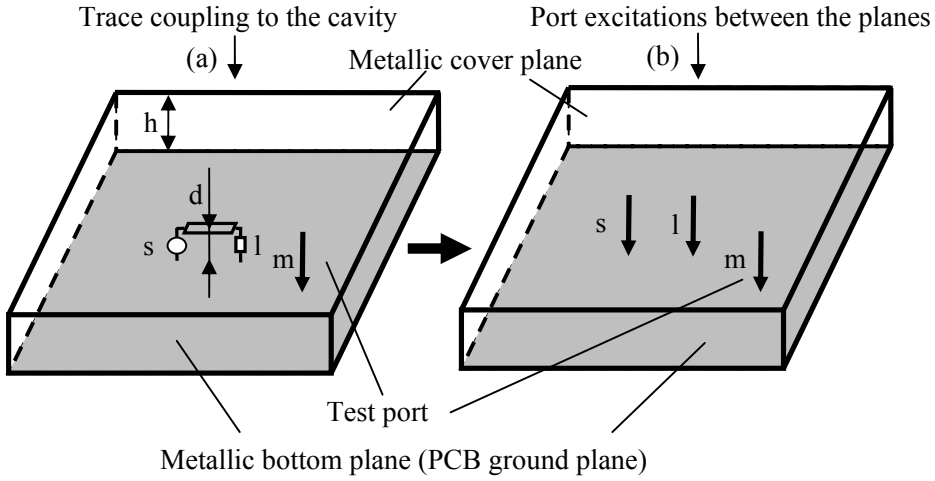

Figure 5.1: A trace which couples to the parallel planes is introduced into an analytical cavity formulation by two ports at positions s (source) and l (load). The validation of the trace introduction is performed by a voltage comparison on test ports m between the planes in model (a) and (b).

The port excitation currents in Figure 5.1(b) are the trace currents at the source (s) and the load (l) in Figure 5.1 (a) multiplied by the constant factor K_{couple}. This mode conversion factor accounts for the coupling from the trace to the common mode cavity field. Port m in Figure 5.1 has been introduced for the voltage measurement between the planes. With (4.17), the voltage on the test port U_m can be expressed by

$$U_m = Z_{mm} I_m + (Z_{ms} I_s + Z_{ml} I_l) K_{couple}. \tag{5.1}$$

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Indices are assigned to the port definition in Figure 5.1. The trace voltages and currents at the port positions s and l in Figure 5.1 (a) can be expressed by transmission line theory with

$$U_s = U_l \cosh(\gamma l) - I_l Z_w \sinh(\gamma l), \tag{5.2}$$

and

$$I_s = \frac{U_l}{Z_w} \sinh(\gamma l) - I_l \cosh(\gamma l). \tag{5.3}$$

Z_w is the characteristic impedance of the trace, γ is the complex propagation factor of the trace, and l is the trace length. The negative sign of I_l in (5.2) and (5.3) is consistent with the definition of the same current flow direction for all ports. The relation of the load voltage to the load current is given by the load impedance

$$Z_l = -U_l / I_l. \tag{5.4}$$

(5.3) and (5.4) lead to

$$I_s = -\left(\sinh(\gamma l)\frac{Z_l}{Z_w} + \cosh(\gamma l)\right) I_l. \tag{5.5}$$

Since port m acts like a voltage probe, the current $I_m = 0$. With $I_m = 0$, (5.1), and (5.5) the transfer impedance of the current at the source of the trace to the voltage on the test port becomes

$$\frac{U_m}{I_s} = \left(Z_{ms} - \frac{Z_{ml}}{\sinh(\gamma l)\frac{Z_l}{Z_w} + \cosh(\gamma l)}\right) K_{couple}. \tag{5.6}$$

Equation (5.6) describes the voltage between the two planes at the test port m for a given trace source current. The vertical connections of the trace have to be considered by using an effective trace length l (Figure 5.2) in (5.6). Since (5.6) does not consider the back coupling

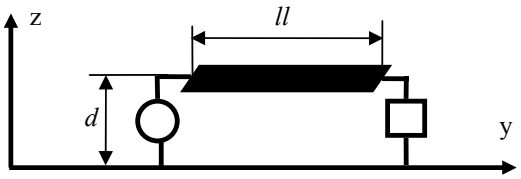

Figure 5.2: Effective trace length to be used in 5.6.

from the cavity field to the trace, it is valid in case of emission simulation, where the trace currents are determined by the trace geometry above the ground plane, the source, and the load. The dielectric layers in printed circuit boards are usually thin, compared to the distance from the ground plane to a parallel metallic enclosure cover. Therefore, the influence of the metallic cover plane on the characteristic impedance of the traces is negligible and the currents on the traces can be simulated with this characteristic impedance, the driver, and the load models. Characteristic impedances with and without the metallic cover plane can be compared with numerical simulation.
Although the back coupling is small, it has to be considered for susceptibility simulations of sensitive devices. In this case, the transmission line equations of the trace have to be integrated into the impedance matrix (4.17) with additional back coupling terms. However, this work concentrates on the emission simulation, where the back coupling can be neglected. Equation (5.6) is an example of the introduction of one trace into a cavity model with one

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measurement port. Multiple traces can be considered in a cavity model by the introduction of trace currents from (5.5) to (4.17) as excitations.
The coupling factor K_{couple} in (5.6) is obtained by mode decomposition, or expressed analytically as distance ratio. Both methods are described in the following sections.

5.1. Calculation of K_{couple} with mode decomposition

The introduction of wires into a rectangular enclosure by a multi-mode analogous transmission line theory has been presented by [49] and [50]. The introduction of traces to the parallel-plane cavity field formulations in Chapter 4 can be achieved by mode decomposition [44]. The cover plane return current is identified as the parasitic common mode current depicted in Figure 5.3.

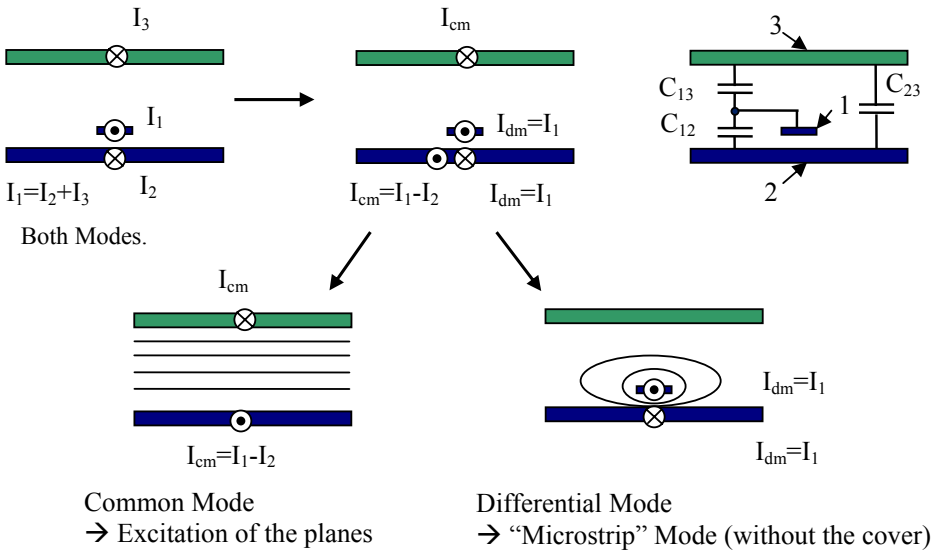

Figure 5.3: Identification of the cover plane return current as the parasitic common mode current.

The conductor with number 1 in Figure 5.3 is the trace, the ground plane is assigned to number 2 and the cover plane to number 3. The partial capacitances between these conductors are indexed accordingly. A source which drives the traces against the ground plane will excite both, the differential mode and the common mode currents. The partial capacitance between the cover and the ground plane C_{23} is high, due to the large extent of these planes. A source current that drives the trace is divided by the capacitances C_{12} and C_{13}. Therefore, the excitation of the cavity field I in (4.13) by the trace is expressed by the trace currents multiplied by the coupling factor

$$K_{couple} = K_{couple\_md} = \frac{C_{13}}{(C_{13} + C_{12})} \tag{5.7}$$

To extract the $1/2n_{co}(n_{co} - 1)$ partial capacitances between n_{co} conductors, the Laplace equation

$$\vec{\nabla}(\epsilon\vec{\nabla}\varphi) \qquad \text{with} \qquad \begin{cases} \varphi = V & \text{, on conductor boundaries} \\ \epsilon\vec{n}\cdot\vec{\nabla}\varphi = 0 & \text{, on open boundaries with no charges} \end{cases} \tag{5.8}$$

for the electrostatic potential φ has to be solved for $1/2 \cdot n_{co}(n_{co} - 1)$ different voltage

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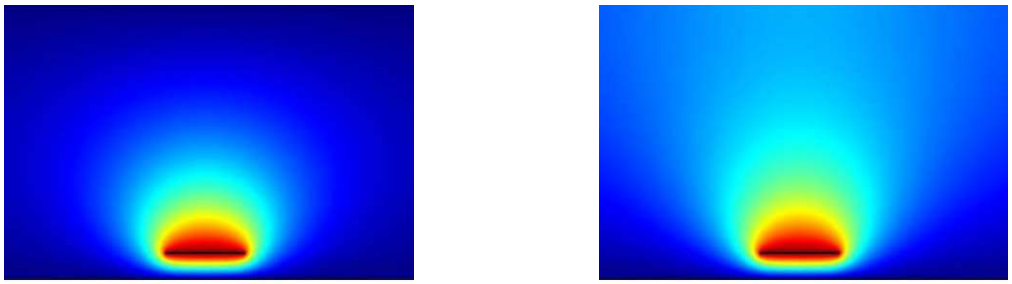
distributions [71], [74]. The surface normal vector at the boundary is $\vec{n}$. The Smart Analysis Program (SAP), a FEM based interconnect simulation software from [75], performs this partial capacitance extraction automatically. SAP is also capable of automated resistance and inductance extraction of interconnects.
Figure 5.4 depicts the difference in the electrostatic potential distribution between a trace with and without cover plane.



(a) Field with cover plane.

(b) Field without cover plane.

Figure 5.4: Electrostatic potential with and without the metallic cover plane (qualitative diagram).

5.2. Expression of K_{couple} by a distance ratio factor

Analytical solutions can be obtained from (4.13) and (4.14) for rectangular planes. This has been performed for power integrity analysis by [42] and [43]. This work presents an analytical solution for a rectangular enclosure in Chapter 7. Mode decomposition requires numerical field simulation to extract the partial capacitances in the cross section of transmission lines on the PCB under the metallic enclosure cover. To enable a purely analytical solution for efficient design investigations, sources, traces, and planes are introduced into the cavity field by an analytical distance ratio factor. Complex PCBs usually consist of numerous traces and planes with different geometric shape, which also requires numerous simulations in a mode decomposition approach. Therefore, the efficiency of numerical algorithms for the solution of the cavity field inside enclosures can also be enhanced significantly by utilization of the proposed analytical introduction method.
The mode, considered in the cavity model, implies that the field does not vary in z-dimension. Therefore, the coupling factor K_{couple} can generally be expressed by a distance ratio weighting factor

$$K_{couple} = K_{couple\_a} = \frac{d}{h} \tag{5.9}$$

According to Figure 5.1 h denotes the vertical distance from the ground plane to the metallic enclosure cover and d is the vertical distance of the trace from the ground plane.

Table 5.1 compares K_{couple_a} from (5.9) to K_{couple_md} from (5.7) for different trace and plane geometries. Values for K_{couple_md} were obtained by numerical capacitance extraction with the Smart Analysis Program (SAP) from [75]. A trace thickness of 35μm was used in the simulations, because this is often the copper layer thickness of PCBs. The difference between the two methods for the calculation of the coupling factor K_{couple} is smaller than three percent even for large trace distances to the ground plane, as in rows 4 and 5. The slight deviation can be explained by the trace thickness, which is considered in the numerical simulation,

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but not in (5.9). On a dB scale, usually utilized to compare emission results, a deviation of three percent equals $0.26dB$. In comparison, the overall emission measurement uncertainty is usually larger than 3dB, even in very accurate laboratories. This measurement uncertainty considers, among other uncertainties, the antenna factor uncertainty, the antenna position tolerance, the site attenuation deviation, and the test receiver tolerances. Therefore, the accuracy of the analytical factor (5.9) is sufficient for EMC emission simulations.

Nr.	b	h	d	C_{12}	C_{13}	K_{couple_md} $C_{13}/(C_{13}+C_{12})$	K_{couple_a} d/h	difference
	mm	mm	mm	F/m	F/m			%
1	2.0	7	0.20	113.81	3.46	0.02946	0.02857	-3.0
2	2.0	7	0.65	45.40	4.74	0.09445	0.09286	-1.7
3	2.0	7	1.50	25.15	6.94	0.21637	0.21429	-1.0
4	2.0	7	3.00	15.06	11.62	0.43550	0.42857	-1.6
5	0.1	7	0.65	16.76	1.76	0.09521	0.09286	-2.5
6	2.0	10	0.65	46.47	3.26	0.06555	0.06500	-0.8
7	2.0	15	0.65	47.39	2.18	0.04406	0.04333	-1.7
8	2.0	20	0.65	47.91	1.64	0.03305	0.03250	-1.7

Table 5.1: Comparison of K_{couple_md} with the distance ratio coupling factor K_{couple_a} for several different plane/trace geometries. b is the trace width.

5.3. Validation of the trace introduction by HFSS® simulations

An empirical validation of the proposed trace introduction method with (5.6) and (5.9) is carried out by HFSS® simulations. HFSS® is a FEM based three-dimensional full wave simulation tool from Ansoft® [76].
A first HFSS® enclosure model with a trace, depicted in Figure 5.5(c), is simulated with ports at the source and the load positions of the trace and three measurement ports at the slot. In a second HFSS® model, presented in Figure 5.5(d), the trace is removed and ports are defined between the bottom and the cover plane of the enclosure in the same positions as the trace load and source ports in the first model. The enclosure cover has been removed in Figure 5.5(c) and Figure 5.5(d) to enable a view of the inside. The enclosure with cover is depicted in Figure 5.5(b), and Figure 5.5(a) depicts the bounding box, with absorbing boundaries at the surface, that surrounds the enclosure in the simulation models. Lumped ports are defined in HFSS® on rectangular surfaces which are small compared to the wavelength of the highest simulated frequency. HFSS® calculates the S-parameter matrix of the ports, which is transformed to a Z-parameter matrix. Proven convergence of the HFSS® simulation is given through a monotone decrease of S-parameter results differences from two consecutive adaptive mesh refinement iterations. For the model in Figure 5.5(c) the transfer impedance from the trace source port to a measurement port at the slot is

$$\frac{U_{m_{tr}}}{I_s} = Z_{ms_{tr}} - \frac{Z_{ml_{tr}} Z_{la_{tr}}}{Z_{ll_{tr}} + Z_l}, \tag{5.10}$$

where $Z_{ms_{tr}}$, $Z_{ml_{tr}}$ and $Z_{la_{tr}}$ are the Z-parameters of this HFSS® model and Z_l is an arbitrary trace load. HFSS® would also enable the trace load in the model to be defined and the transfer impedance to, thus, be obtained directly instead of using (5.10). However, this would require one HFSS® simulation for each load. Therefore, results for different loads

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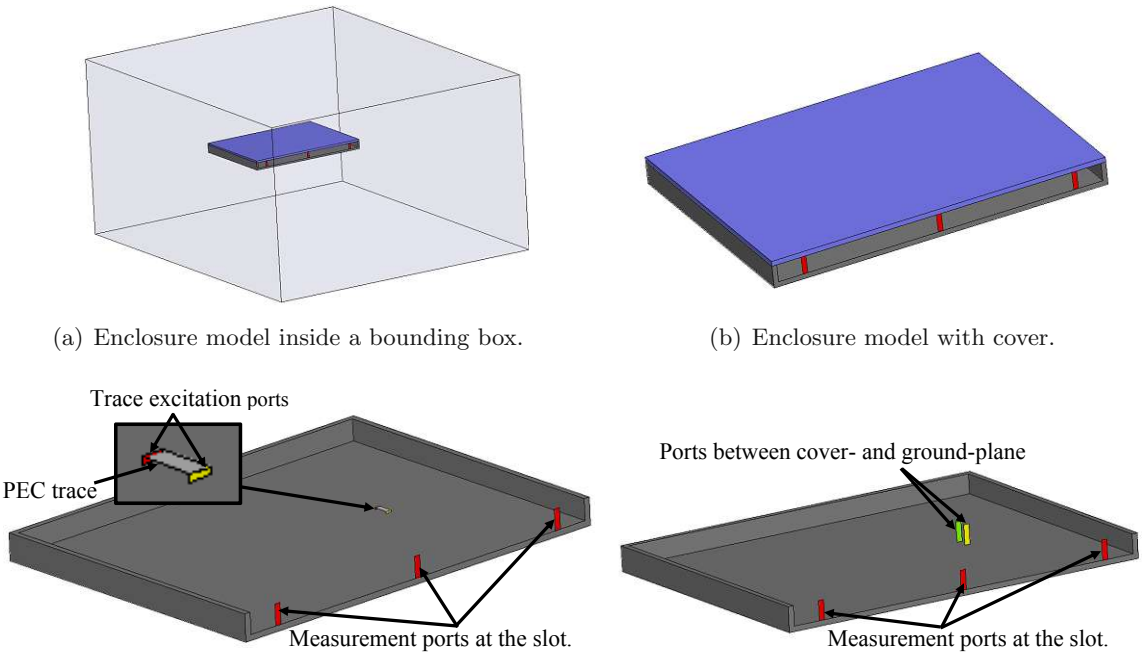
are obtained efficiently by the described model which requires only one HFSS® simulation. According to the described trace introduction method, the transfer impedance is also obtained with (5.6) and (5.9) and the Z-matrix (4.17) of the HFSS® model in Figure 5.5(d). The characteristic impedance of the trace in (5.6) is calculated in accordance with [77]

$$Z_w = (60\Omega)\ln\left[\frac{f_1(w_t/d)}{w_t/d} + \sqrt{1+\left(\frac{2d}{w_t}\right)^2}\right], \tag{5.11}$$

and

$$f_1(w_t/d) = 6 + (2\pi - 6)e^{-(30.666d/w_t)^{0.7528}}, \tag{5.12}$$

where w_t is the trace width and d is the trace height above the ground plane. Equation (5.11) with the adjustment function (5.12) approximates the exact conformal mapping solution from [78], [79], for the characteristic impedance of a thin sheet trace in air. The approximation uncertainty is below 0.03% for $w_t/d \leq 1000$.
For the purpose of simulating traces on a real PCB, the dielectric material of the PCB has to be considered with appropriate formulations [77], [80]. A comparison of the transfer impedances from both models validates the trace introduction method without any further simplifications, as there would be, if the cavity model were to be used instead of HFSS® simulation. For instance, the radiation from the open enclosure slot is considered by surrounding the enclosure with the boundary box in the HFSS® model (Figure 5.5(a)).



(a) Enclosure model inside a bounding box.

(b) Enclosure model with cover.

(c) Model with a trace (cover removed).

(d) Model with ports (cover removed).

Figure 5.5: HFSS® models for the validation of the trace introduction method.

Figure 5.6 depicts the results of the described transfer impedance comparison for a trace at position (x=67mm, y=50mm), the measurement port at position (x=67mm, y=104mm) and trace loads of 0 Ohm, 1e9 Ohm, and 50 Ohm. The trace length is l=5mm, the trace width is w_t=2mm, the trace height above ground is d=0.65mm, and the enclosure dimensions are (L=134mm, W=104mm, h=7mm). To cover the whole ground-plane area, comparisons from nine trace positions are collected in Appendix A.1.

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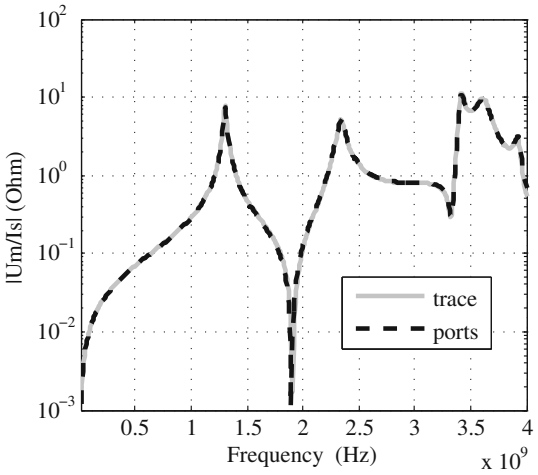
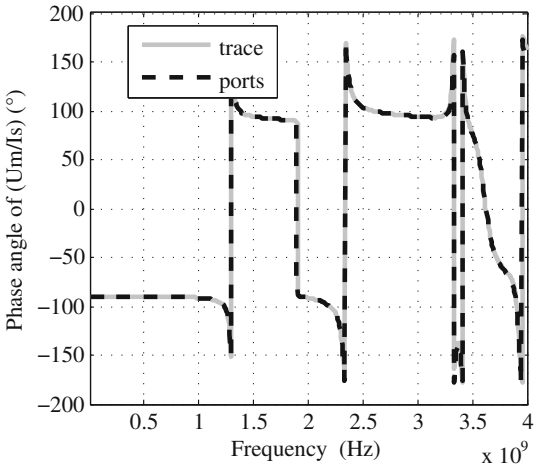
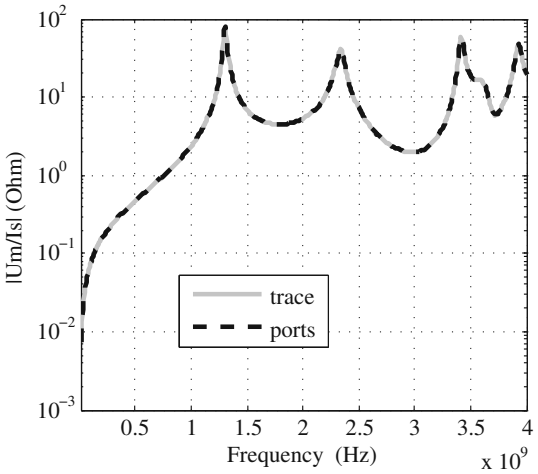


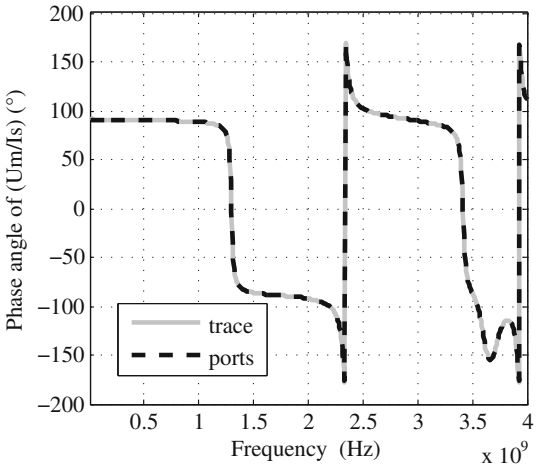
(a) Load: 0 Ohm, magnitude.



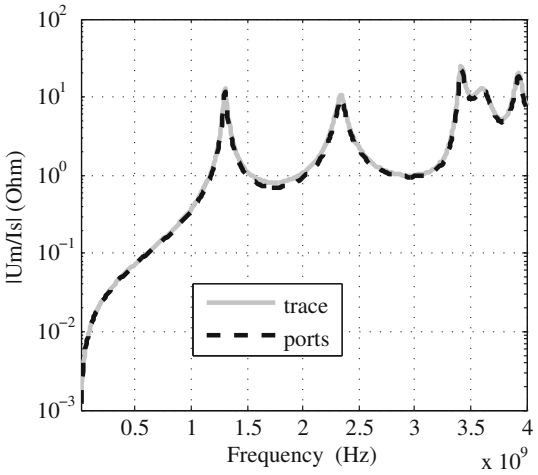
(b) Load: 0 Ohm, phase angle.



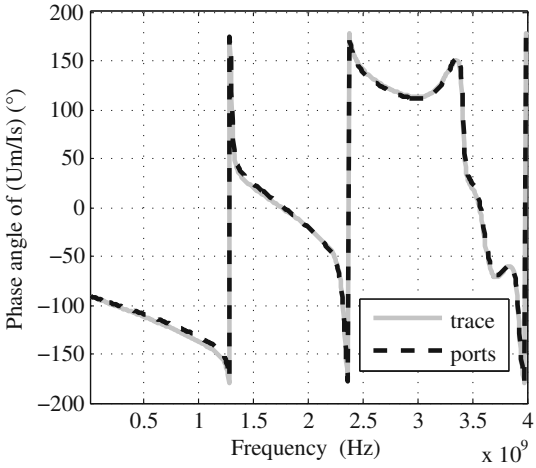
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure 5.6: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (67mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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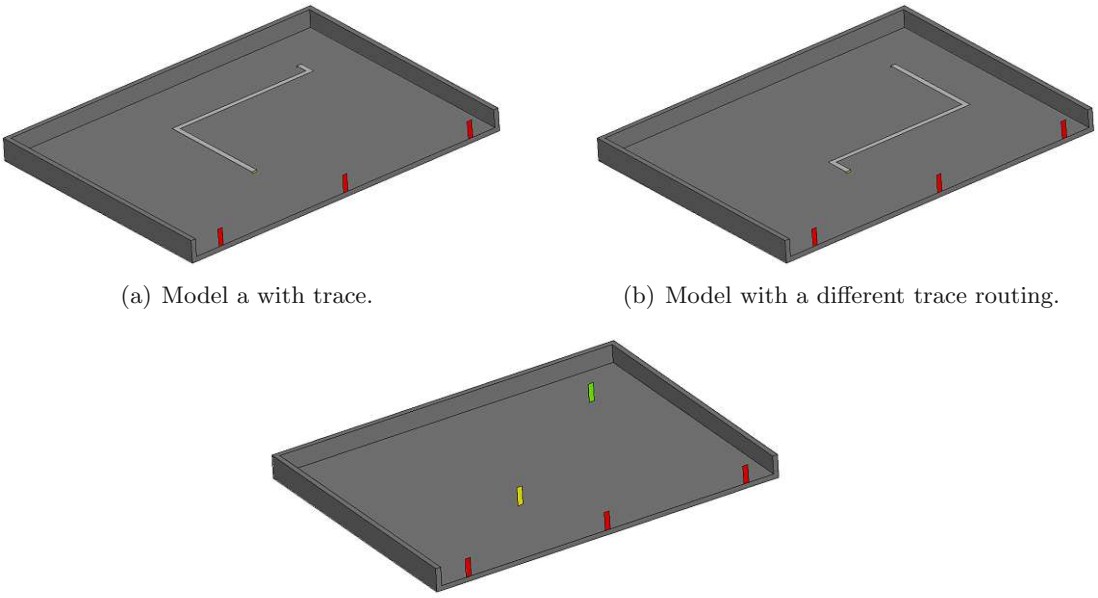
More comparisons are presented for a variation of the enclosure height, for a variation of the trace height above the ground plane, and for parallel planes with four open edges in Appendix A.2. All comparisons show very good agreement, both in magnitude and phase. Thus, the proposed trace introduction method with the analytical coupling factor is generally sufficient for electromagnetic emission simulation.

5.4. Independence of the common mode coupling from the horizontal trace routing

It has previously been mentioned that only the vertical current segments of the trace couple to the cavity. Therefore, the trace introduction method only considers these vertical source and load currents in (5.6). Transfer impedance comparisons as described before are carried out for the two trace routings in Figure 5.7, to validate the independence of the coupling from the horizontal trace segments. The trace length in both models is l=110mm, the trace width w_t=2mm, the trace hight above the ground plane is d=0.65mm, and the enclosure dimensions are (L=134mm, W=104mm, h=7mm). The comparison of the transfer functions to the meas port at (x=67mm, y=104mm) for the models in Figure 5.7(a) and in Figure 5.7(b) are depicted in Figure 5.8 and Figure 5.9 respectively. Comparison results of the transfer impedance to the other two measurement ports are presented in Appendix A.2

Magnitude and phase comparisons show a very good agreement of both models in Figure 5.7(a) and in Figure 5.7(b) to the results obtained with (5.6), (5.9) and the impedance matrix (4.17) from the model in Figure 5.7(c). That confirms the independence of the common mode coupling from the horizontal trace routing and validates the trace introduction method.



(a) Model a with trace.

(b) Model with a different trace routing.

(c) Model with ports at the trace source- and load positions.

Figure 5.7: HFSS® models with a different trace routing between identical source and load positions.

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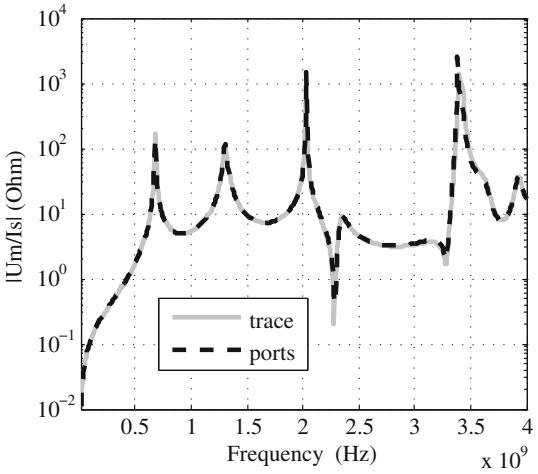
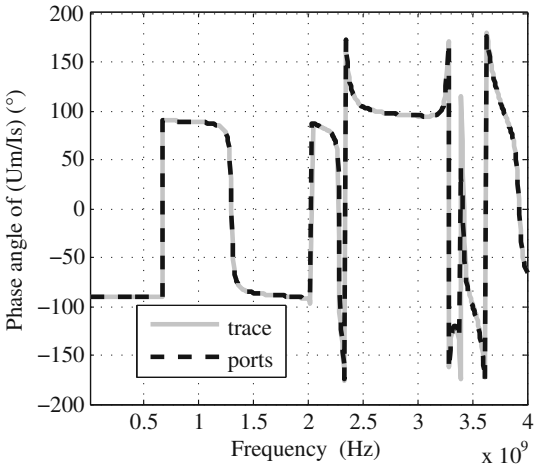
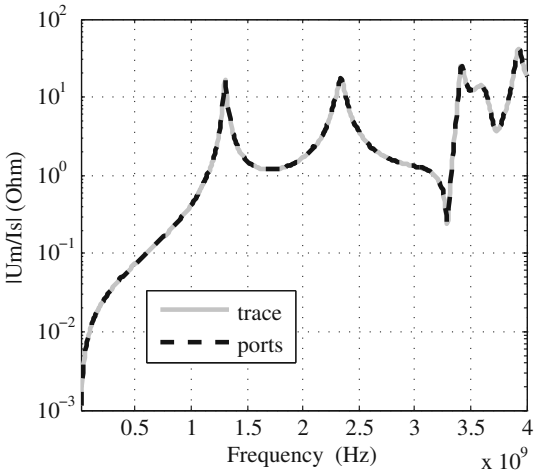


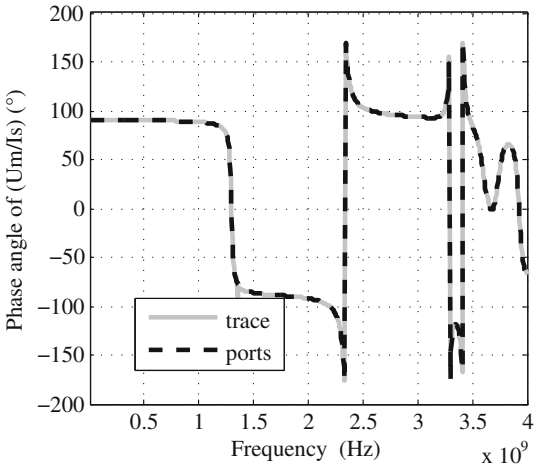
(a) Load: 0 Ohm, magnitude.



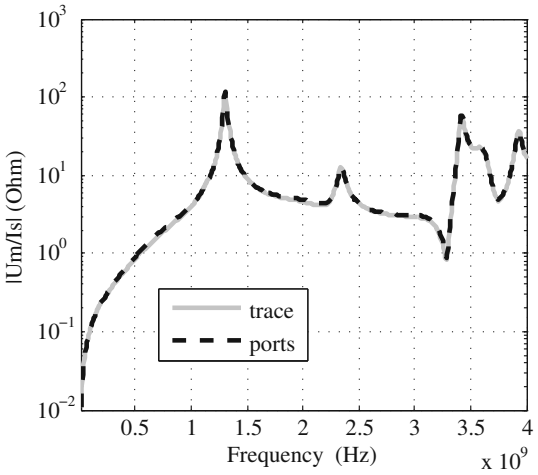
(b) Load: 0 Ohm, phase angle.



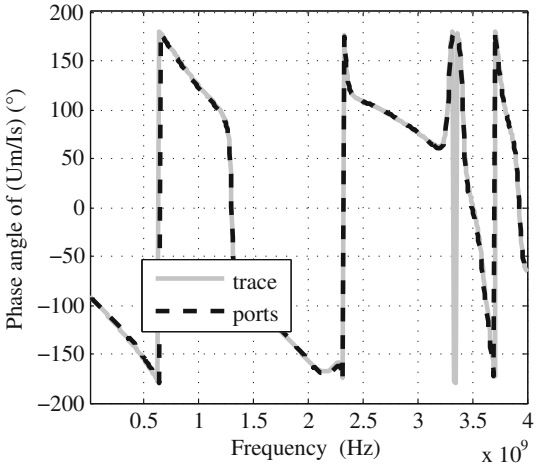
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure 5.8: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). Comparison of HFSS results from a model with a trace (Figure 5.7(a)) to the results obtained with (5.6), (5.9) and a HFSS model with ports.

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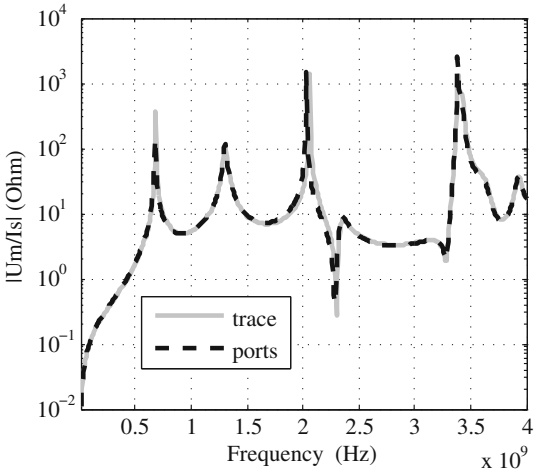
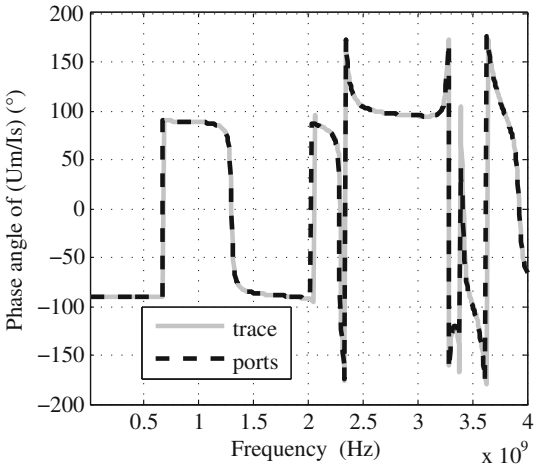
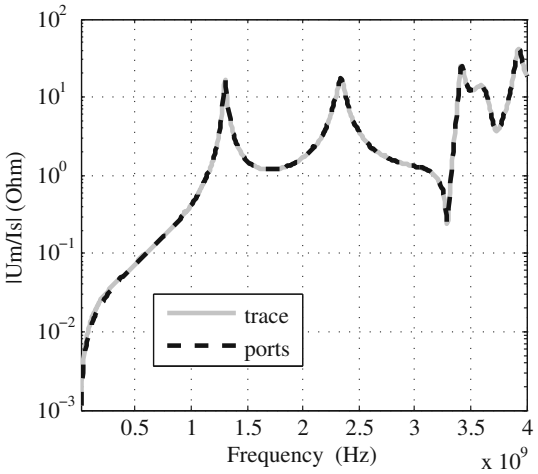


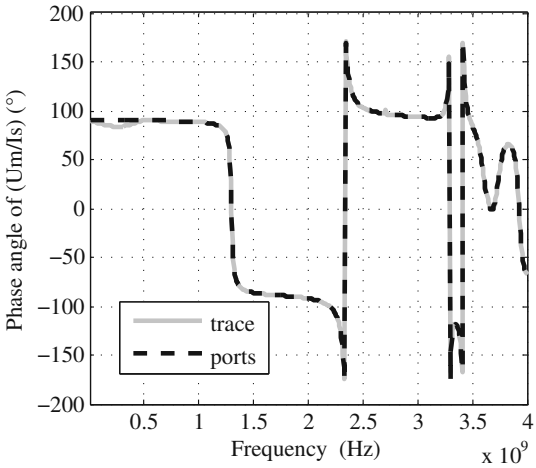
(a) Load: 0 Ohm, magnitude.



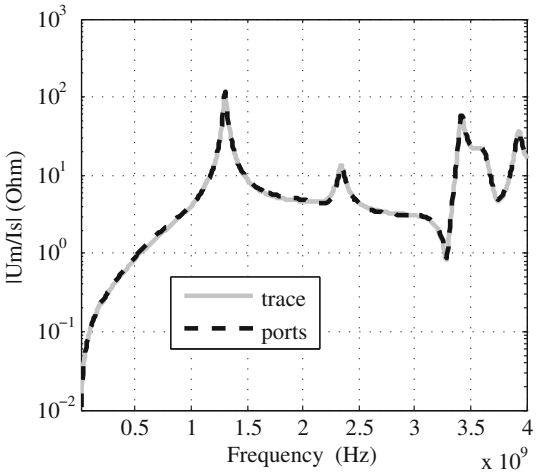
(b) Load: 0 Ohm, phase angle.



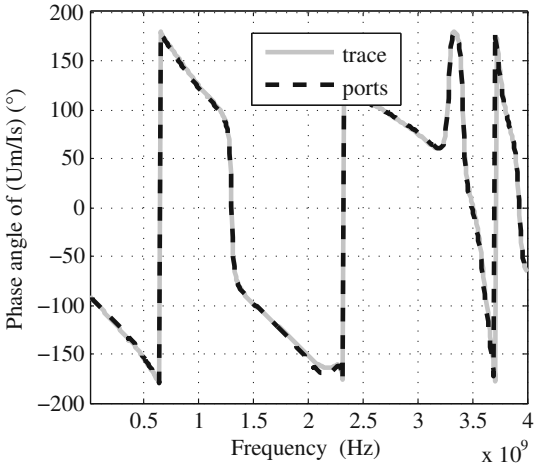
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure 5.9: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). Comparison of HFSS results from a model with a trace (Figure 5.7(b)) to the results obtained with (5.6), (5.9) and a HFSS model with ports.

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5.5. Link of the common mode coupling to the near field above the PCB

Near field scanning over a PCB is a state of the art method to investigate the EMC performance experimentally [81], [82]. Usually the magnetic field vector components $|H_x|$, $|H_y|$ and $H_{mag} = \sqrt{|H_x|^2 + |H_y|^2}$ are scanned versus frequency as depicted in Figure 5.10. Phase information can either be obtained with a double probe time domain scanner [83], [84], or by the method of [85], which obtains the phase from two magnitude scans with different scan heights above the PCB. Increased field value areas on the PCB are observed as potential elec-

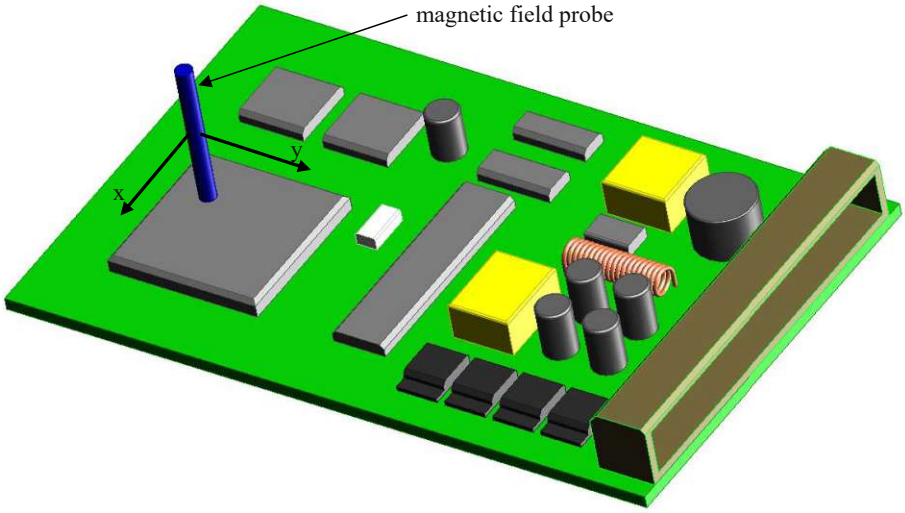

Figure 5.10: Scanning the magnetic field above the PCB with a magnetic field probe.

tromagnetic emission sources. However, there is actually no direct relation from the scanned field values to the coupling of the PCB to a cavity field. The coupling of an IC to the cavity field inside a μTEM cell is tested with the standardized IC EMC compliant measurement of [54]. Therefore, investigations have been carried out to predict the results of these IC μTEM measurements with scanned field data and with simulations. [81] utilizes empirical formulations for a first order prediction of μTEM cell IC measurements from near field measurement data. [6] and [52] modeled the coupling from an IC to a μTEM cell with coupling capacitors. These models had some inaccuracies especially for frequencies above 300MHz and did not reveal any relationship to the near field above the IC. Only three-dimensional full wave simulations or the mulipole method of [31] enable an accurate prediction of the PCB or IC cavity coupling from near field data. However, these methods do not preserve the initial near field localization of the critical sources on the PCB.
It has previously been described that only the vertical current segments couple to the cavity. This enables a direct relation to be expressed from the scanned near field to the common mode coupling. The third Maxwell equation in air

$$\vec{\nabla}\vec{H} = \vec{J} + j\omega\epsilon_0\vec{E}, \tag{5.13}$$

relates the magnetic field density $\vec{H}$ to the electric field density, $\vec{E}$ and the current density $\vec{J}$. The dielectric constant in air is ϵ_0. Equation (5.13) is utilized to express the vertical current density

$$J_s = Jz + j\omega\epsilon_0 E_z = \frac{\partial}{\partial x}H_y - \frac{\partial}{\partial y}H_x, \tag{5.14}$$

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which excites the cavity field. This current density can be introduced into a cavity model with the weighting factor

$$K_{couple} = d_s/h, \tag{5.15}$$

where d_s denotes the height of the scanning plane above the parallel ground plane. When a scan would be carried out directly on the trace, without any distance of the scan plane (theoretically), the current J_s would become the trace current and the coupling weighting factor would become d/h. Equation (5.14) reveals that not the field density values, but their derivatives are significant for the common mode coupling to the cavity. Therefore, a scan plot of 5.14 will provide much more precision for coupling source identification. Figure 5.11 depicts both, $|H_x|$ and $|\partial H_x/\partial y|$, along a short trace in y-direction. The vertical segments that couple to the cavity can clearly be localized from $|\partial H_x/\partial y|$. $|H_x|$ is nearly constant along the whole horizontal trace segment which does not couple to the cavity. For maximum source localization accuracy, the scan has to be performed as close as possible along the PCB or IC surfaces and the scan heights above the PCB ground plane must be taken into account using (5.15) for the classification of the source coupling potentials.

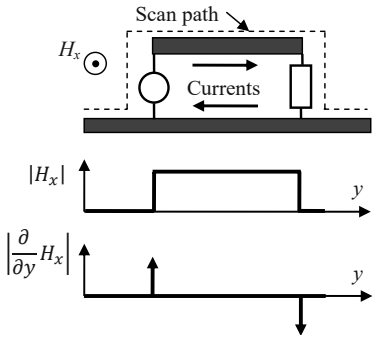

Figure 5.11: $|H_x|$ and $|\partial H_x/\partial y|$ along the y direction. $|\partial H_x/\partial y|$ enables an accurate identification of the coupling current segments, while $|H_x|$ is high along the whole trace length.

The following subsections describe some application opportunities for (5.14) and (5.15) beyond source identification.

5.5.1. Prediction of μTEM IC measurements from near field scan data.

Since the distance from the ground to the septum of a μTEM cell is electrically short, the μTEM field can be described using the cavity model of Chapter 4. A scan, performed above the IC, very close to the surface of the IC, enables the extraction of the excitation currents. The source currents with the coupling factors, together with the cavity model, enable the simulation of the μTEM cell measurement result.
A μTEM cell measurement requires the production of a test board. With the prediction of the μTEM cell measurement results from field scan data, this costly test board is not necessary, because the scan measurement can be performed on an application board. There will be some deviations to the μTEM cell measurement with a test board, because the currents on the IC also depend on the external PCB layout and there will be differences between the test and the application board. However, this is not a drawback, but an advantage, because the simulation based on the application board near field measurement will provide an even better view into the cavity coupling of the intended application.

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5.5.2. IC EMC model validation with near field scan data

The next section describes the IC EMC modeling with an ICEM model and a geometrical package description. Such models can be validated easily with scan measurements. The vertical cavity excitation sources, extracted from the scan data with (5.14) and (5.15), must match the EMC IC coupling model results from a simulation. The comparison has to be drawn with the IC on the same board under the same operational conditions. This means the same length of traces to the IC, the same PCB layer stack, the same power supply decoupling, the same running software, the same bus activity, and the same peripheral activity. In the case of deviations of scan measurement from simulation data, the simulation model can be adapted easily, because the comparison is made on individual excitation sources which allow an individual adjustment of source parameters in the model. For instance, an inaccuracy in the geometrical package description, which leads to a slight difference of the source position or the d/h factor may be corrected with the near field validation. Microcontrollers, but also smart power ICs, enable the peripheral and core activity to be controlled by software. Running different EMC validation software provides the opportunity for an individual check of the models for each IC module. Many devices provide a software slew rate control for the outputs. It is mandatory to use the same slew rates as in the final application for all EMC simulations and in each EMC validation software.

5.5.3. Behavior modeling of geometrically complex components

A circuit module consists of the circuit components and the layout interconnects on the PCB. For the purpose of investigating the coupling to the cavity, depending on the placement of the module inside an enclosure, when the circuit and layout structure are not subject to change, a measurement based behavioral modeling of the module can be performed. The coupling sources of the model are obtained from a single scan, (5.14), and (5.15), even for modules with geometrically complex and nonlinear components, such as, for instance, coils or transformers and active components with no readily available EMC model.

Changing also the module circuit and layout requires component models which can be introduced in a network simulation to obtain the module currents and voltages. A behavior modeling of passive and linear components can be performed by VNA (vector network analyzer) S-parameter measurements. Some network simulation tools support a direct introduction of S-parameter data from VNA measurements, while others require a circuit model which also can be obtained from the S-parameter tables [86], [87], [88]. However, the component pin currents from the network simulation cannot be used to investigate the coupling of the component to an enclosure, because this depends on the geometric distribution of the currents on the component. The coupling current sources

$$J_s(x,y) = \sum_{n=1}^{Pn} [\alpha_n(x,y) I_n] \tag{5.16}$$

which describe the coupling to an enclosure are related linearly to the component pin currents I_n. The linear weighting factors $\alpha_n(x,y)$ for the Pn component pin currents can be obtained from Pn scan measurements with different pin current combinations. Circuitry or the layout around the component must be altered to generate different pin currents. Equation (5.16) and the S-parameter table establish together a behavior model of the component, which enables a simulation based design of a circuit module.

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5.6. Modeling the coupling from integrated circuits

[6] accurately simulated the near field of a microcontroller IC, only utilizing the currents on the package and neglecting the currents on the die. Both [6] and [52] explained that the near field of an IC can be modeled with the currents on the IC package. The near field of the IC is directly related to the IC common mode coupling to the cavity field, as presented in the previous section. Therefore, the common mode coupling of an IC can also be modeled only from the currents on the package. It is also evident that only the vertical segments of the package couple to the cavity, because these segments are large compared to the vertical interconnects on the die. An introduction of the vertical segments from the package interconnects with their associated currents according to the previously described method correctly models the coupling of the IC to the cavity. A standard ICEM model for conducted emission simulations accurately describes the currents and voltages on the package of the device. A freeware tool for ICEM modeling and further IC EMC issues has been presented by [89] and ICEM modeling is described in the ICEM cookbook [90]. ICEM package modeling issues are described in [91][92]. Chip level passive distribution network ICEM modeling was presented in [93][94][95] and dynamic IC switching current ICEM modeling was present in [96][97]. Examples for accurate VLSI ICEM models have been presented by [60] and [61]. The positions and lengths of the vertical package interconnects are obtained from a mechanical package drawing or from CAD data. The lengths of the vertical segments are used to obtain the associated coupling factors d/h for the introduction of the package excitation currents to the cavity model. Package coding is regulated by the JEITA [98] standard EIAJ ED-7303B. The package code includes information about the material of the package body, package specific features, the basic package designation, the package terminal number, the package nominal dimension, and the terminal in-line interval. Table 5.2 contains a list of some basic IC package type designations. All packages, with exception of the BGA type, are lead frame packages. The vertical segments of a lead frame package are the pins and the bond wires, while the vertical segments of a BGA package are the balls, the vias of an interposer PCB, and the vertical bond wire segments.

Acronym	Designation	Lead frame (yes/no)
BGA	Ball Grid Array	no
QFP	Quad Flat Package	yes
SOP	Small Outline Package	yes
DIP	Dual In-Line Package	yes

Table 5.2: Some basic packages type designations.

The package specific feature code, which is added to package designation before the basic designation, determines, among other package properties the seated height of the package. Table 5.3 contains a list of seated hight codes. The maximum seating height determines the maximum possible vertical segment length of a package. Thin packages are usually realized utilizing reverse bonding with a bonding wire height lower than 10mil (0.2mm). In the case of very short bonding heights compared to the pin heights of a lead frame package, the bonding wire can be neglected and the enclosure can be modeled only with the coupling segments at the pin positions. However, most packages contain bond wires with similar heights as the lead frame, which cannot be neglected. The bond wires also have to be modeled in BGA type packages. Since the bond wire lengths are usually short, the bond wires can be modeled with a constant height obtained from the mean height of the bond wire shape. The coupling factor 5.9 is expressed with the mean value of the vertical bond wire heights d_i, weighted

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Seated hight code	Meaning	Maximum seated height
L	Low profile	$1.2mm < \text{L} \leq 1.7mm$
T	Thin	$1.0mm < \text{T} \leq 1.2mm$
V	Very thin	$0.8mm < \text{V} \leq 1.0mm$
W	Very very thin	$0.65mm < \text{W} \leq 0.8mm$
U	Ultra thin	$0.5mm < \text{U} \leq 0.65mm$
X	Extremely thin	$\text{X} \leq 0.5mm$

Table 5.3: Seated height package code information.

with their respective lengths l_i

$$K_{couple} = \frac{d_{ic}}{h} = \frac{1}{h}\frac{\sum_{i=1}^{s}[d_i l_i]}{\sum_{i=1}^{s} l_i}. \tag{5.17}$$

s denotes the number of segments with different heights above the PCB ground plane along the bond wire. This enables a simplified model for the cavity coupling of each package pin, especially when the bond wires are short, with low height. This enables an introduction of the bond segments to a median loop with vertical segments only at the pins of the lead frame. A thin QFP package is depicted in Figure 5.12. The high frequency currents on the package and the associated loop with its vertical segments is depicted in Figure 5.13. Note that the return current even of a fast signal might not flow over the ground pin which is closest to the signal pin, when the package has more than one ground pin, because the high ohmic resistances of the interconnects on the die have a significant influence on the overall loop impedance. Therefore, the correct ground pin has to be considered for the introduction into the cavity model. In contrast to a lead frame package, the vertical segments on a BGA package are the lead balls, the vias of the interposer, and the bond wires.

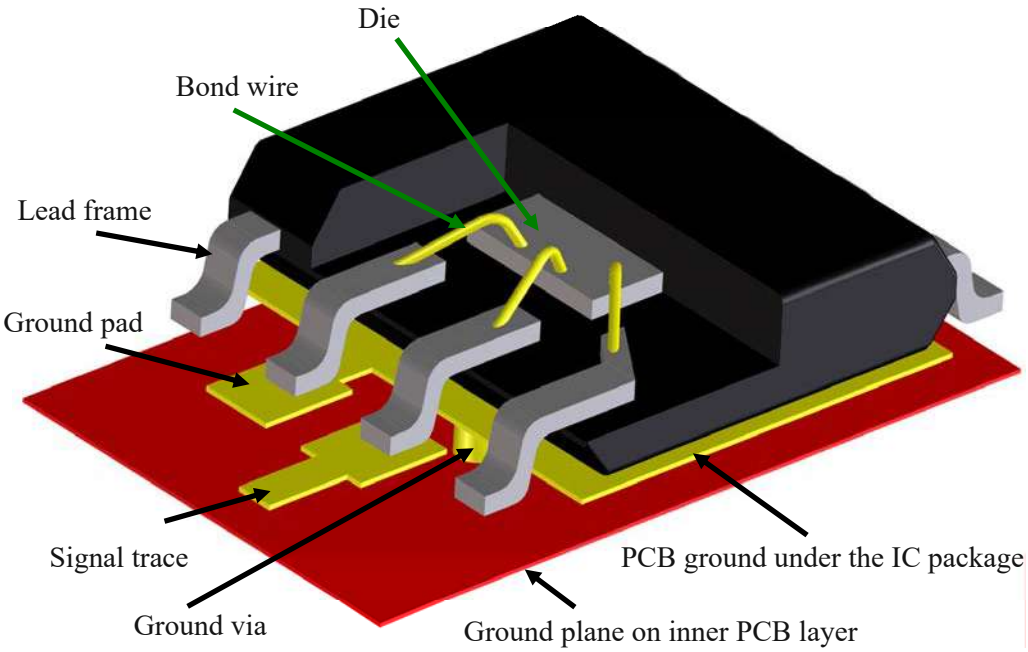

Figure 5.12: Thin QFP package with eight pins, mounted on a PCB.

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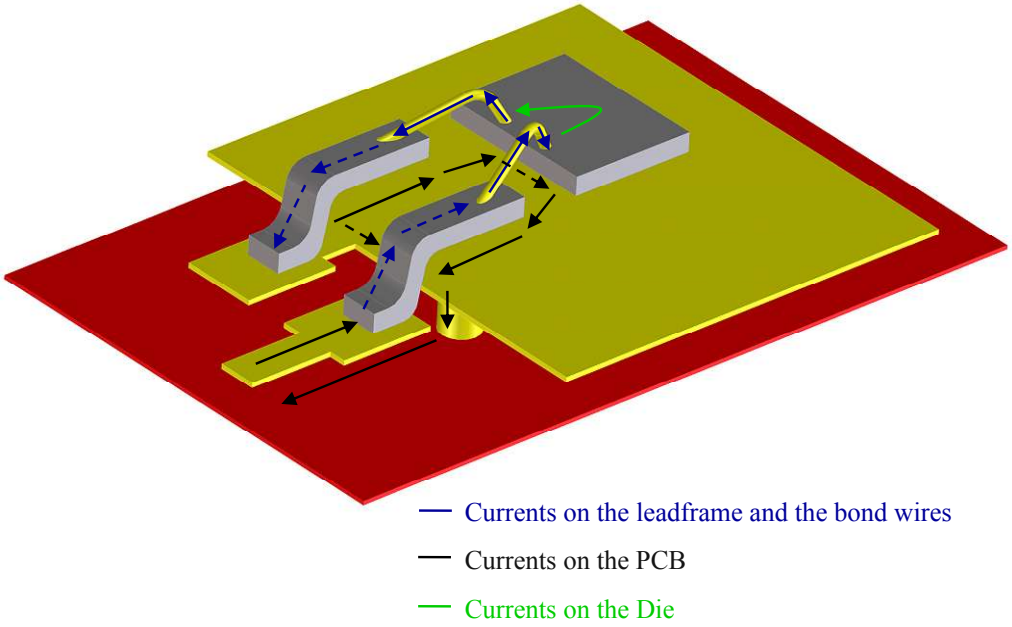
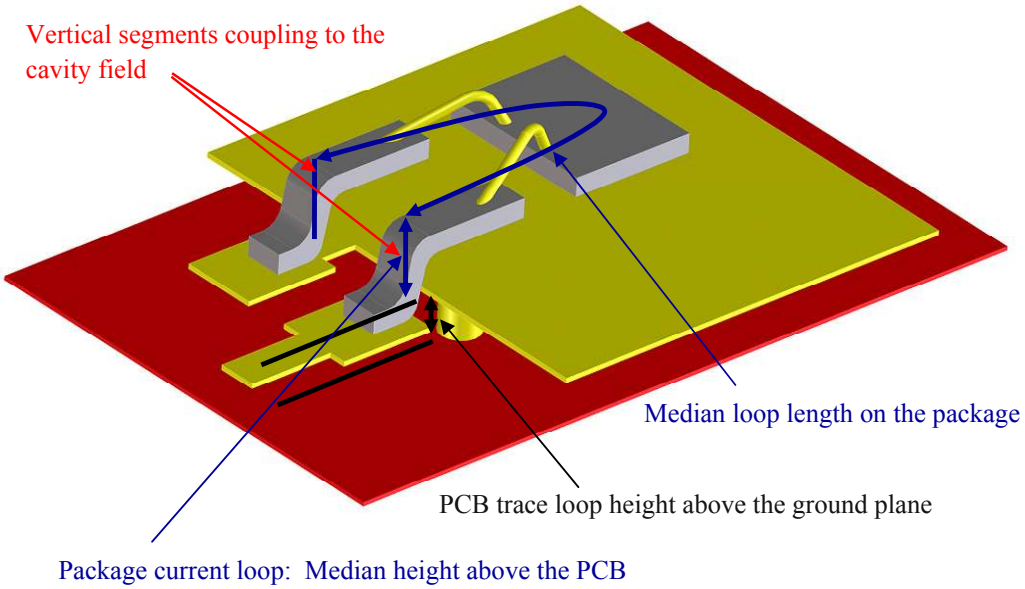


(a) Current flow path on the PCB, the IC package, and the die. The vertical current segments are on the pins of the leadframe and on the bond wires. The dotted current arrows indicate that the current is flowing on the lower side of the lead frame pins, according to a shorter current loop.



(b) Current loops on the PCB and on the IC package. Introduction of the IC into the cavity model is performed with the vertical current segments of the package current loop at the pins of the leadframe. Median height and length values are used to model the current loop on the package. Note that the vertical bond wire segments can only be included into the median loop, when their height is low. A comparison of the simulation results, with and without explicit modeling of the vertical bond wire segments, should be made to validate the simplified package model.

Figure 5.13: High frequency current flow path on the IC package in Figure 5.12 and the associated loop with its vertical and horizontal current segments. The plastic mold and the remaining pins of the package as depicted in Figure 5.12 have been removed to enable the illustration of the current path.

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5.7. Link to the current driven common mode mechanism and the common mode inductance of a trace inside a cavity.

The magnetic flux lines wrapping around the ground plane of a PCB cause a voltage between wires which are connected at the PCB [32]. Figure 5.14 shows the magnetic flux and the associated common mode voltage U_{cm}, which drives the cables, connected to the PCB like an antenna source voltage.

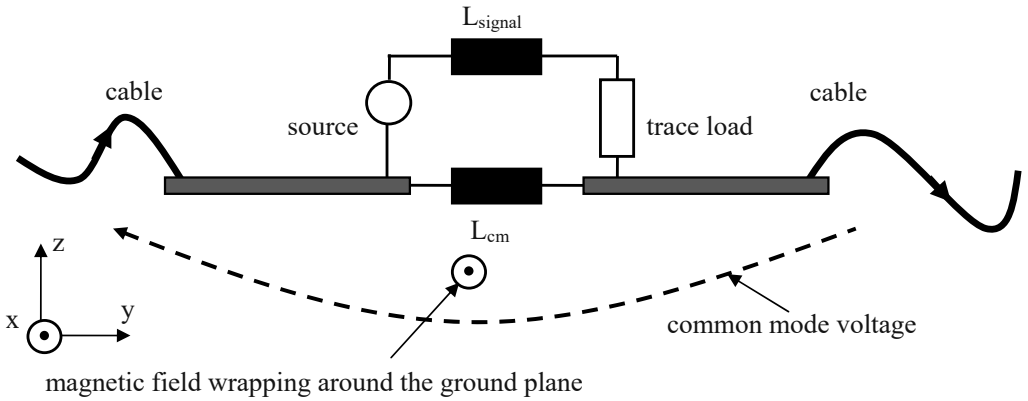

Figure 5.14: Model illustrating the physics of the current driven common mode mechanism as described in [32].

The differential mode current on the trace I_{dm} and common mode inductance L_{cm} determine the common mode voltage

$$U_{cm} = j\omega L_{cm} I_{dm}. \tag{5.18}$$

For a trace in the symmetry line (x=L/2) of the ground plane (Trace a in Figure 5.15) the common mode inductance is

$$L_{cm} = \frac{4\mu d l_{tr}}{\pi^2 L}, \tag{5.19}$$

according to [36]. The trace length is l_{tr}.

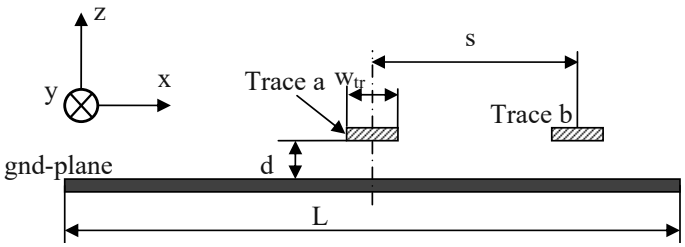

Figure 5.15: Trace a in the symmetry line of the ground plane and Trace b located at a distance s from that symmetry line.

The trace inductance for a trace located at a distance s from the ground plane symmetry line (Trace b in Figure 5.15) is

$$L_{cm} = \frac{\mu l_{tr}}{2\pi} \ln \left| 2\frac{s+jd}{L} + \sqrt{4\left(\frac{s+jd}{L}\right)^2 - 1} \right|, \tag{5.20}$$

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according to [37]. For a trace in the symmetry line of the ground plane (s=0) [37] reduced (5.20) to

$$L_{cm} = \frac{\mu d l_{tr}}{\pi L}. \tag{5.21}$$

The equations (5.19) and (5.21) have been obtained for a narrow trace ($w_{tr} \ll L$) above the PCB ground plane and without a metallic cover plane. For a parallel plane structure ($w_{tr} = L$, trace width = ground plane width) the common mode inductance is

$$L_{cm\_p} = \frac{h \mu l_{tr}}{2L} \tag{5.22}$$

according to [36], where h is the plane separation distance.

A μ-TEM cell measurement and a hybrid coupler was carried out by [99] for the coupling from heat sinks to cables and by [100] for the magnetic field coupling to cables. This measurement configuration is shown in Figure 5.16. The coordinate system definition is consistent with those in Figure 5.14 and Figure 5.15.

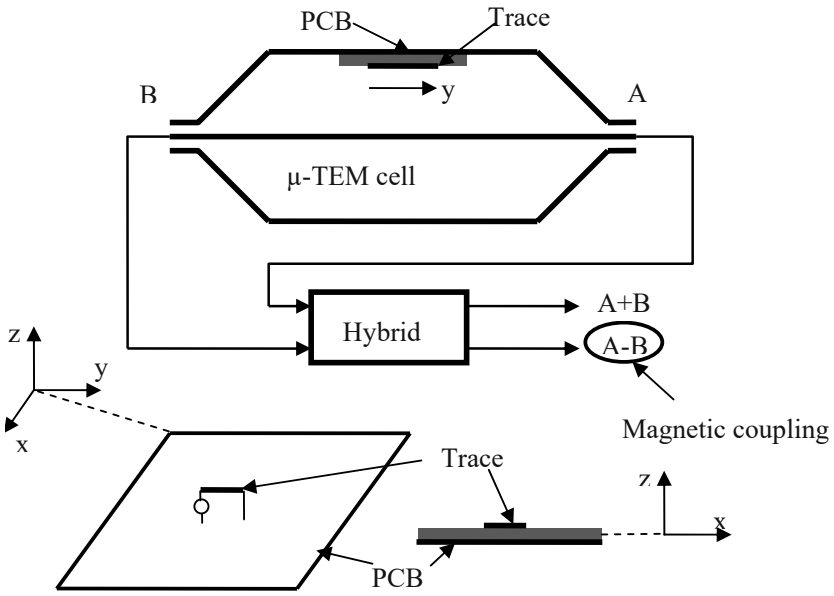

Figure 5.16: Measurement configuration of [100] to obtain the magnetic coupling moment of a trace or an IC.

The magnetic field coupling moment is obtained from the $A-B$ output of the hybrid coupler by [100].
To obtain the magnetic coupling of a trace to the cavity between two parallel rectangular planes, the model depicted in Figure 5.17 is utilized.
Neglecting the *sinc*() terms in (4.19) and (4.20) and inserting these equations into (4.18) yields

$$Z_{ij} = \frac{j\omega\mu h}{LW} \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} \left[\frac{L_{mn} \cos(k_m x_i) \cos(k_n y_i) \cos(k_m x_j) \cos(k_n y_j)}{k_m^2 + k_n^2 - k^2} \right], \tag{5.23}$$

for the mutual impedance between two parallel-plane ports. With the ports and sources in

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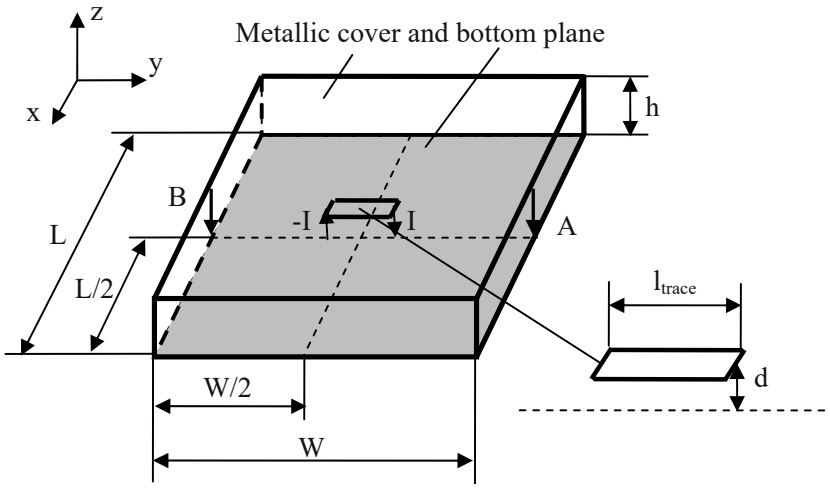

Figure 5.17: Model for the derivation of the coupling inductance from a trace to the cavity.

Figure 5.17 the voltage difference of port A and B becomes

$$U_{AB} = -\frac{j\omega\mu h I}{LW}\frac{d}{h} \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[\frac{L_m L_n \left(\cos\left(\frac{n\pi}{W}\left(\frac{W}{2}+\frac{l_{tr}}{2}\right)\right)-\cos\left(\frac{n\pi}{W}\left(\frac{W}{2}-\frac{l_{tr}}{2}\right)\right)\right)\left(1-(-1)^n\right)\cos^2\left(\frac{m\pi}{2}\right)}{\left(\frac{m\pi}{L}\right)^2+\left(\frac{n\pi}{W}\right)^2-\left(\frac{2\pi}{\lambda}\right)^2}\right], \quad (5.24)$$

where λ is the wavelength. The factors L_m are one for $m = 0$ and two for nonzero m. The factors L_n are one for $n = 0$ and two for nonzero n. The factor d/h considers the trace coupling according to Section 5.2. According to the factor $(1-(-1)^n)$ terms with even n vanish. For low frequencies $W \ll \lambda$ the nominator term $(2\pi/\lambda)$ may be neglected. With this simplification, (5.24) becomes

$$U_{AB} = j\omega L_{cm\_p} I = \frac{4j\omega\mu d I}{LW}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[\frac{L_m \sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi l_{tr}}{2W}\right)\left(1-(-1)^n\right)}{\left(\frac{2m\pi}{L}\right)^2+\left(\frac{n\pi}{W}\right)^2}\right]$$
$$= \frac{8j\omega\mu d I}{LW}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[\frac{L_m(-1)^n \sin\left(\frac{(2n+1)\pi l_{tr}}{2W}\right)}{\left(\frac{2m\pi}{L}\right)^2+\left(\frac{(2n+1)\pi}{W}\right)^2}\right]. \quad (5.25)$$

The coupling inductance is

$$M_c = \frac{8\mu d}{LW}\sum_{n=0}^{\infty}\left\{(-1)^n \sin\left(\frac{(2n+1)\pi l_{tr}}{2W}\right)\left[\frac{1}{\left(\frac{(2n+1)\pi}{W}\right)^2}+\sum_{m=1}^{\infty}\frac{2}{\left(\frac{2m\pi}{L}\right)^2+\left(\frac{(2n+1)\pi}{W}\right)^2}\right]\right\}. \quad (5.26)$$

With

$$\sum_{m=1}^{\infty}\frac{1}{a^2+m^2} = \frac{1}{2}\frac{\pi\coth(a\pi)a-1}{a^2}, \quad (5.27)$$

(5.26) is simplified to

$$M_c = \frac{4\mu d}{\pi}\sum_{n=0}^{\infty}\left[(-1)^n \sin\left(\frac{(2n+1)\pi l_{tr}}{2W}\right)\frac{\coth\left(\frac{(2n+1)\pi L}{2W}\right)}{2n+1}\right]. \quad (5.28)$$

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For small traces $l_{tr} \ll W$ the function described by the fourier series in (5.28) is approximated by the first term of its Taylor series, developed around $l_{tr} = 0$ and (5.28) becomes

$$M_c = \frac{2\mu d l_{tr}}{W} \sum_{n=0}^{\infty} \left[(-1)^n \coth\left(\frac{(2n+1)\pi L}{2W} \right) \right]. \tag{5.29}$$

With

$$\sum_{n=0}^{\infty} \left[(-1)^n \coth\left(\frac{(2n+1)\pi L}{2W} \right) \right] \approx \frac{\pi}{4} \coth\left(\frac{L\pi}{2W} \right) \tag{5.30}$$

and

$$\coth(x) \approx \frac{1}{x} \quad \forall \quad |x| < 1, \tag{5.31}$$

the coupling inductance for $L < (2/\pi)W \approx 0.6W$ becomes

$$M_c = \frac{\mu d l_{tr}}{L}. \tag{5.32}$$

The common mode inductance is associated with the flux wrapping around only one of the two planes. Thus, the coupling inductance has to be divided by a factor of two to obtain the common mode inductance [36]. Therefore, the common mode inductance of a trace inside a parallel plane cavity is

$$L_{cm\_p} = \frac{\mu d l_{tr}}{2L}. \tag{5.33}$$

Note that (5.33) becomes exactly (5.22) of [36], when the trace height above the ground plane becomes the plane separation distance h. Equation (5.22) has been verified experimentally by [36]. This provides evidence that the current driven common mode coupling mechanism of a trace inside a parallel-plane cavity is described sufficiently with the cavity model. The cavity model describes not only the current driven common mode mechanism for a tiny trace in the symmetry line of the cavity, but also the current driven common mode coupling for arbitrary traces inside the cavity.
The verification of the common mode inductance by measurement has been carried out as follows. Figure 5.18(a) shows the measurement setup with the VNA (vector network analyzer) ZVB4 from Rhode&Schwarz. A trace loop above a copper plane is connected to one port of the VNA. The trace is terminated with 0 Ohm to the ground copper plane. A wire loop is soldered to both ends of the copper plane and a SMA connector in this loop is connected to the second VNA port for the measurement of the induced common mode loop voltage. This is illustrated in Figure 5.18(b) and Figure 5.18(c). The measured S parameters are converted to Z parameters and the common mode inductance

$$L_{cm\_meas} = \frac{X_{21}}{\omega} \quad \text{,with} \quad Z_{21} = R_{21} + jX_{21} \tag{5.34}$$

is calculated from the measurement results. The measurement is carried out for a trace above ground without a cover plane in Figure 5.18(b) and for a configuration with a cover plane at a distance of 10mm from the ground plane as depicted in Figure 5.18(d). The cover plane was tightly arranged with foam plates with a dielectric constant close to that of air and an adhesive tape. The dimensions for the test device are listed in Table 5.4.

Figure 5.18(e) shows good agreement of the measured common mode inductances to the analytical results from (5.21) of 0.08nH for the configuration without a cover plane and to the result from (5.33) of 0.12nH for the configuration with a cover plane. This confirms that the current driven common mode coupling is sufficiently described with the cavity model.

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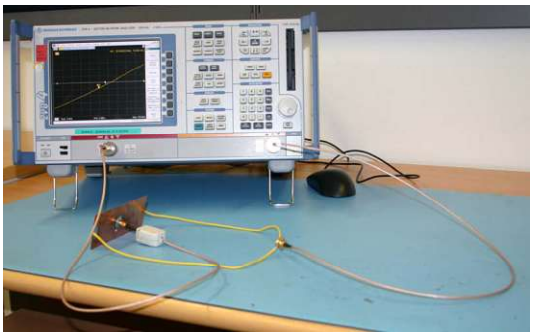
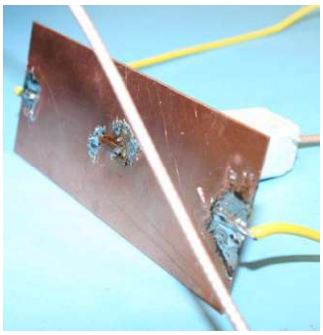
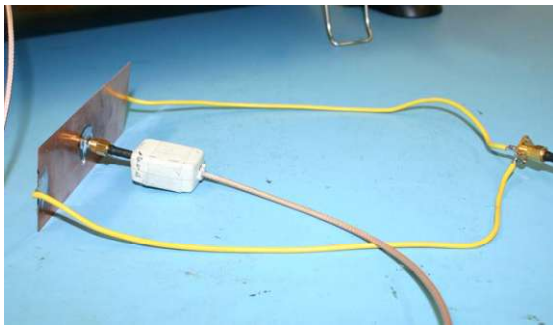


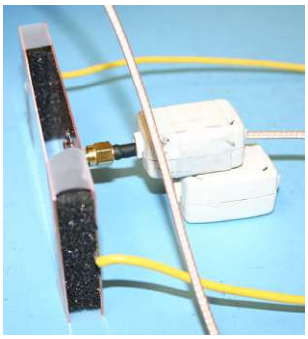
(a) Measurement setup overview.



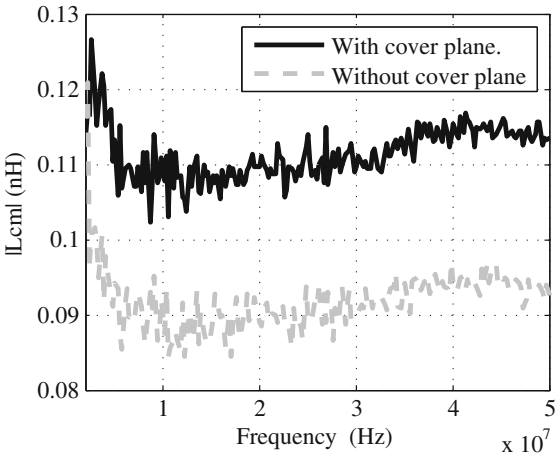
(b) Trace loop above ground.



(c) Induced voltage measurement loop.



(d) Trace inside a cavity.



(e) Measured common mode inductances.

Figure 5.18: Measurement setup and results for the validation of the common mode inductance.

Designation	Dimension	
W	120	mm
L	50	mm
l_{tr}	10	mm
d	1	mm
h	10	mm
w_{tr}	2	mm

Table 5.4: Dimensions of the test device.

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5.8. Design consequences

According to (5.9), the common mode coupling of layout structures such as traces and power-planes to the enclosure cavity field can be reduced by a reduction of the trace to ground plane distance d, which is determined by the dielectric layer thickness of the PCB. In comparison with standard PCB layer stacks, HDI technology with ultra thin layers or thin outer layers of standard PCBs will reduce the common mode coupling and the electromagnetic emissions accordingly. However, impedances of high speed signal traces have to be preserved by trace width reduction when the layer thickness is reduced.
Since the common coupling depends only on the vertical currents, the EMC design has to concentrate on the vertical interconnects of EMC critical components and on the PCB. The coupling from components on the PCB can be reduced by the selection of packages with shorter vertical interconnects. For instance, if a flash memory IC with a fast clock input is available with a BGA or a QFP package, the BGA type should be selected. A different package has other package inductances and capacitances. Thus, a signal integrity analysis is necessary when another package type is selected. The current magnitude frequency spectrum on the IC pins should be obtained from the transient signal integrity analysis by FFT. The current spectrum together with the reduced coupling factor from the changed package provide quantitative information about the achievable reduction of the emission level. A ground plane area on the outer PCB layer directly under the IC, as depicted in Figure 5.12, reduces the height of the package loop d compared to a PCB layout with a ground plane only in an inner layer. Although the distance of the enclosure cover to the PCB ground h is also reduced by raising the ground by the distance Δd, d/h is effectively reduced, because $h \gg d \Rightarrow (d-\Delta d)/(h-\Delta d) < d/h$. Therefore, the ground should be routed directly under the IC and this ground has to be connected to the global PCB ground plane by vias, at least in the positions of the fast signal pins to enable the short current return path, depicted in Figure 5.13(a). A current loop on an IC is not generally the shortest, with the lowest inductance, because high resistive tracks on the die can lead to a lower overall loop impedance of extended loops. In particular, to reduce the magnetic coupling from the IC, the magnetic loop is effectively reduced by a ground plane under the package.

5.9. Necessity to consider the influence of the external environment at the cavity field simulation

The cavity field model (4.13) provides, together with the source introduction (5.9), an efficient method for the simulation of the internal enclosure fields. However, the model has to be extended to consider the influence of the emissions from the open slots at the edges of the parallel planes. Slots can be allocated on an enclosure to enable a cooling air flow, or for connectors which establish the functional interface of the device. Figure 5.19(a) depicts the connector at the enclosure slot of an automotive control device, and Figure 5.19(b) depicts the back plane of a personal computer enclosure with connector and coolant air slots. Coupling of the internal fields to cables and direct radiation from the slots have a significant influence on the internal enclosure field, due to the emission losses. [45] and [101] have shown a rising influence of the radiation loss from the edges of power planes with increasing plane separation distance h. An enclosure usually has a much higher cover to PCB ground plane-separation h than power-ground planes, while dielectric losses are much lower. Therefore, the radiation loss from the slots becomes the dominant loss mechanism from enclosures without cables. The coupling to cables introduces additional losses. Both have to be considered in the simulation of the internal enclosure fields in order to obtain accurate field results for a subsequent simulation of the device emissions.

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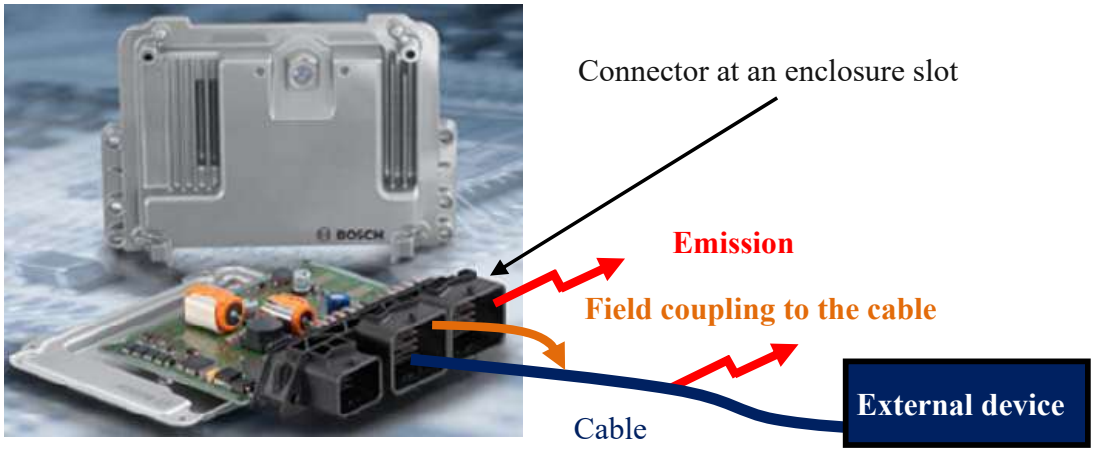
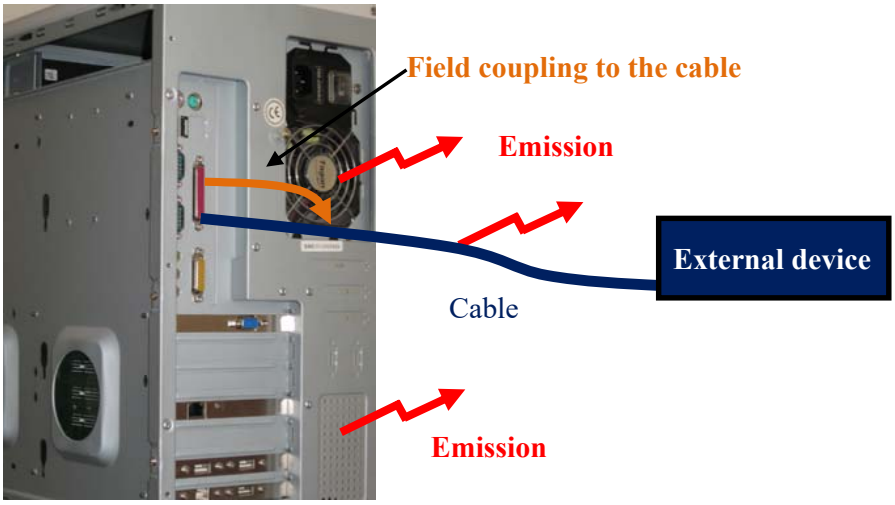
Chapter 6 describes a method to consider these couplings by a new domain decomposition approach. This method is not restricted to slots at the edges of slim enclosures, like that in Figure 5.19(a). It can generally be utilized for every metallic enclosure with apertures, as for example the personal computer enclosure in Figure 5.19(b).



(a) Motor control device with cable harness.



(b) Back plane of a personal computer enclosure.

Figure 5.19: The field inside a metallic enclosure causes direct radiation from the enclosure apertures. Coupling from the internal fields to cables at the connectors causes additional emissions. Large apertures or cable emissions can have a significant influence on the internal enclosure field. Thus, the external environment of the enclosure has to be considered at the internal field simulation.

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6. Domain decomposition with PMC boundaries and port interfaces

The proposed cavity model for the simulation of the parallel-plane field inside the enclosure has been optimized for this purpose by a reduction of the general Maxwell equations in Chapter 4. This reduction is only admissible under the conditions (4.4) and (4.5), which are fulfilled inside the enclosure, but not in the external device environment. Thus, an interface between the cavity model and another simulation model of the external environment is necessary for the consideration of external influences on the internal cavity field. An interface which enables separate simulations of the external and the internal model and an integration of both simulation results in a common network simulation is established by utilizing equivalent source theory. Figure 6.1 depicts the subject of equivalent source theory, that the external field outside of an object is preserved, when the object is replaced by a PMC object of the same shape with electric currents on the surface, which are obtained from the initial field. Alternatively, the object can be replaced by a PEC object with magnetic currents on the surface, also preserving the external field [102].

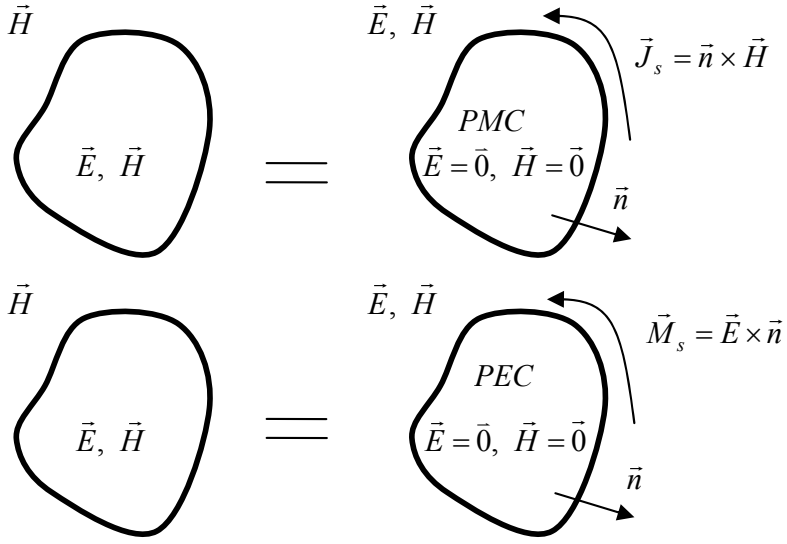

Figure 6.1: Equivalent source theory. Electric current sources and a PMC boundary condition on the surface of an obstacle cause the same fields. Magnetic current sources and a PEC boundary condition cause also the same fields.

Another valid model preserves the field inside the object and replaces the external environment of the object by PMC material and electric currents on the object surface. PEC in the volume outside of the object and magnetic currents on the object surface will preserve the internal fields accordingly. A PMC surface with an electric surface current is, from a circuit point of view, equivalent to an ideal current source, while a PEC surface with a magnetic surface current is equivalent to an ideal voltage source.
The described equivalent source theory enables a general simulation domain separation with every standard full-wave simulation tool that supports PMC boundary conditions and elec-

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tric current ports, or PEC boundary conditions and magnetic current ports. A separate domain simulation of the internal and the external domains of an object and integration of both results can be performed with the following simulation procedure:

1. Replace the object in the simulation model with a PMC object of the same shape.
2. Arrange electric current ports parallel to the outer object surface (i.e. on a triangular mesh).
3. Simulate the external model with three-dimensional full wave simulation or obtain an analytical solution.
4. Obtain a port impedance network from the simulation results.
5. Return to the initial model and remove the external environment.
6. Declare a PMC boundary at the surface of the object.
7. Arrange electric current ports parallel to the inner object surface (i.e. on a triangular mesh).
   The ports must be positioned identically to the ports in the previous simulation to enable a correct connection.
8. Simulate the internal model with three-dimensional full wave simulation, or with the cavity model (if the object is an enclosure).
9. Obtain a port impedance network from the simulation results.
10. Implement both network models in a standard network simulation program.
11. Perform a network simulation to obtain joint domain results.

Alternatively to a PMC boundary together with an electric current port, PEC boundaries together with magnetic current ports may also be used. Since the external and the internal simulation are separated, the external simulation can be performed with either PMC boundaries together with electric current ports, or PEC boundaries together with magnetic current ports, while the internal simulation can be performed with a different boundary and port current definition. The described procedure is general and can be performed on every three-dimensional object. The number of ports which have to be arranged along the object's surface to obtain accurate results depends on the maximum frequency of the simulation and the object size. Ports must not be declared on metallic walls of the object. High frequency fields decay rapidly inside a metallic wall and cannot excite the other domain. Therefore, these surfaces are modeled as they are. This significantly reduces the necessary number of surface ports, if the object is an metallic enclosure. At slim enclosure apertures ports must only be arranged perpendicular to the slot edges, due to the vanishing electric field tangential along the metallic edges. Thus, this domain separation approach is efficient for emission and shielding effectiveness simulations even on large metallic enclosures.

The inner domain of devices as described in Chapter 1 is simulated by using the cavity model (4.13) with PMC boundaries at the slot surfaces and multiple ports between the upper and lower planes just in front of the PMC surface inside the enclosure. The result of this simulation is an impedance matrix (4.17) model of the internal device domain. Although energy dissipation is caused by radiation and coupling to cables from enclosure slots, the PMC boundary condition is a much more realistic model of the slot than a PEC boundary. An enclosure model with PMC surfaces and no surface current ports does not consider emissions

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from the slot. However, this ideal model has nearly the same cavity modes as a model that considers the emissions, and thus provides good first order information about the resonance frequencies. Therefore, it is proposed to implement the interface at the slots with a PMC boundary condition and electric currents on the slot surface.
Another simulation has to be performed for the external device domain using PMC or PEC boundaries at the slots with electric or magnetic current ports respectively at the same slot positions, but outside of the enclosure.
Every available three-dimensional full-wave simulation tool can be used for this simulation. The results of both the internal model and the external model simulations are combined in a network simulation program according to the previously described procedure. As an alternative to the numerical simulation of the external enclosure domain, an analytical model for the free space radiation loss is obtained in Section 7.2, utilizing magnetic current sources at the slot. A port admittance matrix from this analytical solution is introduced into the cavity model for the consideration of the slot radiation in the calculation of the field on the inside of the enclosure. With the field on the enclosure slot and the external free space radiation solution, the radiation of the slot from a slim enclosure is expressed analytically. This purely analytical application of the domain decomposition method provides a powerful method for predesign investigations.

Advantages of the proposed domain decomposition approach:

- ➢ Numerically stable separate simulation of both domains.
- ➢ Applicable with every three-dimensional full-wave simulation tool which supports either PMC boundaries and electric current ports, or PEC boundaries and magnetic current ports.
- ➢ A change in one of the separated models requires only a new simulation of this model. This enables efficient device optimization.
- ➢ Models of different tools and methods can be combined.
- ➢ Significant reduction of interface ports at metallic enclosures.
- ➢ External environment influences can be considered in the cavity model (4.13).
- ➢ The results of a separated device provide insight into pure device properties which are not overlaid from external influences (i.e. resonances).
- ➢ Different environment models can be connected with a device model.
  The behavior of the device in different environments can be studied efficiently.

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7. Analytical model for the radiated emissions from the slot of a rectangular enclosure:

This chapter describes the derivation of an analytical model for the radiated emissions from an enclosure with three closed and one open edge depicted in Figure 7.1. A trace above the ground plane of the PCB couples to the cavity and causes radiation from the slot of the enclosure. Intended applications of this model are fast predesign investigations on the influences of enclosure dimensions, placement of potentially critical components, and the PCB layer stack. Especially the first resonances of parallel-plane structures depend mainly on the maximum overall enclosure dimensions in x and y direction and not so much on details of the enclosure shape. Therefore, the model provides good first order information even about quantitative emission values for practical enclosures. The in depth description of the model derivation in this chapter shall provide guidance for the derivation of such enclosure models with different boundaries, for example, an enclosure with connector slots on the front and the back edges.

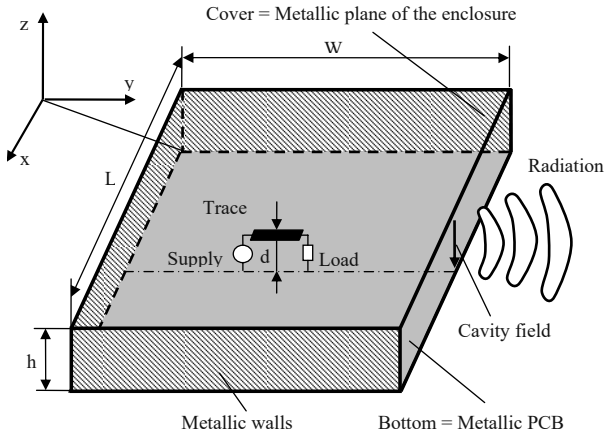

Figure 7.1: A trace on the PCB couples to the cavity and causes radiation from the cavity slots.

7.1. Analytical cavity model for a rectangular enclosure with three closed edges and one open slot

7.1.1. Derivation of the cavity model with the separation method

Applying the method of Bernoulli [103], the homogenous part of (4.13) is expressed by

$$\frac{1}{X(x)}\frac{\partial^2}{\partial x}X(x)+\frac{1}{Y(y)}\frac{\partial^2}{\partial y}Y(y)+k^2=0 \qquad \text{with} \qquad U(x,y)=X(x)Y(y), \tag{7.1}$$

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which enables separation to

$$\frac{1}{X(x)}\frac{\partial^2}{\partial x}X(x) = -k_m^2 \qquad \text{and} \qquad \frac{1}{Y(y)}\frac{\partial^2}{\partial y}Y(y) = -k_n^2, \tag{7.2}$$

with

$$-k_m^2 - k_n^2 + k^2 = 0 \qquad \text{and} \qquad k^2 = \omega^2\mu\epsilon\left(1 - \frac{j}{Q(\omega)}\right). \tag{7.3}$$

The general solution of these equations is

$$X(x) = A_m \sin(k_m x) + B_m \cos(k_m x) \qquad \text{and} \qquad Y(y) = C_n \sin(k_n x) + D_n \cos(k_n x). \tag{7.4}$$

The PMC boundary (4.16) on the open slot and the PEC boundaries (4.15) on the metallic walls according to Figure 7.1 are introduced by

$$\begin{aligned} X(0) = X(L) = 0 \quad &\Rightarrow \quad B_m = 0 \vee k_m = \tfrac{m\pi}{L} \quad \forall \quad m \in \mathbb{N}_0, \\ Y(0) = 0 \quad &\Rightarrow \quad D_n = 0, \\ \tfrac{\partial}{\partial y}Y(y) = 0\Big|_{y=W} \quad &\Rightarrow \quad k_n = \tfrac{(2n+1)\pi}{2W_e} \quad \forall \quad n \in \mathbb{N}_0. \end{aligned} \tag{7.5}$$

k_m and k_n are the eigenvalues of (4.13) for the rectangular enclosure in Figure 7.1. The fringing fields at the slot are considered by using the effective enclosure width $W_e = W + h/4$ instead of W. In [45] $W_e = W + h/2$ has been taken to consider the fringing fields for planes with two open boundaries associated with dimension W, but as the enclosure in Figure 7.1 has only one open edge, the correction must be performed by using $W_e = W + h/4$. An additional correction has to be carried out to consider the wall thickness d_w of the enclosure. This is not necessary in the case of power planes on a PCB, because the conducting layers are thin, although, a metallic enclosure usually has thicker walls. To consider a non-negligible wall thickness of the enclosure, the effective enclosure dimension in y-direction is

$$W_e = W + h/4 + d_w. \tag{7.6}$$

With (7.5) and (7.4) the solution of the homogenous part of (4.13) results in

$$U(x,y) = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty}(L_{m,n}\sin(k_m x)\sin(k_n y)) \tag{7.7}$$

$L_{m,n}$ are parameters which depend on the integer pair m and n. These parameters are obtained by the following solution of (4.13). The port excitation with a current I_{sp} on source point (x_{sp}, y_{sp}) is expressed by

$$J_z(x,y) = -I_{sp}\delta(x_{sp}, y_{sp}), \tag{7.8}$$

where $\delta(x_{sp}, y_{sp})$ is the Dirac impulse. Consistency with standard voltage and current direction of the impedance matrix (4.17) is achieved with the negative sign. Inserting (7.7)

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and (7.8) into (4.13), multiplying with $\sin(k_{m1}x)\sin(k_{n1}y)$ and integrating over the area ($0 \leq x \leq L$, $0 \leq y \leq W$) yields

$$\int_{y=0}^{W_e}\int_{x=0}^{L}\left[\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}(L_{mn}\sin(k_m x)\sin(k_n y)\sin(k_{m1}x)\sin(k_{n1}y))\mathrm{d}x\mathrm{d}y\right](-k_m^2-k_n^2+k^2)$$
$$= -j\omega\mu h\int_{y=0}^{W_e}\int_{x=0}^{L}[I_{sp}\delta(x_{sp},y_{sp})\sin(k_{m1}x)\sin(k_{n1}y)\mathrm{d}x\mathrm{d}y]\,. \quad (7.9)$$

Where $m1 \in \mathbb{N}_0$ and $n1 \in \mathbb{N}_0$. The right hand side of (7.9) becomes

$$-j\omega\mu I_{sp} sin(k_{m1}x_{sp})\sin(k_{n1}y_{sp}). \quad (7.10)$$

The left hand side of (7.9) vanishes for all $m \neq m1$ and also for all $n \neq n1$ according to the orthogonality of the base functions $\sin(k_m x)$ to $\sin(k_{m1}x)$ and $\sin(k_n y)$ to $\sin(k_{n1}y)$, respectively. For $m = m1$ and $n = n1$ the left hand side integral solutions are

$$\int_{x=0}^{L}\left[\sin^2(\frac{m\pi x}{L})\mathrm{d}x\right] = \frac{L}{2}, \quad (7.11)$$

and

$$\int_{x=0}^{W_e}\left[\sin^2(\frac{(2n+1)\pi x}{2W})\mathrm{d}y\right] = \frac{W_e}{2}. \quad (7.12)$$

Finally, the solution of (4.13) for the rectangular enclosure in Figure 7.1 becomes

$$U(x,y) = \frac{j4\omega\mu h I_{sp}}{LW_e}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[\frac{\sin(k_m x_{sp})\sin(k_n y_{sp})\sin(k_m x)\sin(k_n y)}{k_m^2+k_n^2-k^2}\right]. \quad (7.13)$$

With (7.13) the coefficients of the impedance matrix (4.17) are

$$Z_{ij} = \frac{j4\omega\mu h}{LW_e}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[\frac{\sin(k_m x_i)\sin(k_n y_i)\sin(k_m x_j)\sin(k_n y_j)}{k_m^2+k_n^2-k^2}\right]. \quad (7.14)$$

The resonance frequencies of the enclosure obtained from the zeros of $k_m^2+k_n^2-k^2$ are

$$f_r = \frac{c_l}{2\pi}\frac{1}{\sqrt{1-\frac{j}{Q(\omega)}}}\sqrt{\left(\frac{m\pi}{L}\right)^2+\left(\frac{(2n+1)\pi}{2W_e}\right)^2} \approx \frac{c_l}{2\pi}\sqrt{\left(\frac{m\pi}{L}\right)^2+\left(\frac{(2n+1)\pi}{2W_e}\right)^2}, \quad (7.15)$$

where $c_l = 1/\sqrt{\mu\epsilon}$ denotes the speed of light in the cavity.

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7.1.2. Summary of the analytical cavity model of the rectangular enclosure with a slot on one edge

Cavity model for a rectangular enclosure with a slot on one edge		Reference
$U_i(x_i,y_i)=\sum_{j=1}^{n_{port}}(Z_{ij}(x_i,y_i,x_j,y_j)I_j(x_j,y_j))\quad\text{with}\quad i,j=1\ldots n_{port}$		(4.17)
$Z_{ij}=\frac{j4\omega\mu h}{LW_e}\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\left[\frac{\sin(k_m x_i)\sin(k_n y_i)\sin(k_m x_j)\sin(k_n y_j)}{k_m^2+k_n^2-k^2}\right]$		(7.14)
$k_m=\frac{m\pi}{L}\quad\forall\quad m\in\mathbb{N}_0$	$k_n=\frac{(2n+1)\pi}{2W_e}\quad\forall\quad n\in\mathbb{N}_0$	(7.5)
$W_e=W+h/4+d_w$		(7.6)
$f_r=\frac{c_l}{2\pi}\frac{1}{\sqrt{1-\frac{j}{Q(\omega)}}}\sqrt{\left(\frac{m\pi}{L}\right)^2+\left(\frac{(2n+1)\pi}{2W_e}\right)^2}\approx\frac{c_l}{2\pi}\sqrt{\left(\frac{m\pi}{L}\right)^2+\left(\frac{(2n+1)\pi}{2W_e}\right)^2}$		(7.19)

7.1.3. Interpretation of the analytical model

The maxima of the cavity field inside and the radiated emission from the enclosure slot are observed at the resonance frequencies, where the denominator $k_m^2+k_n^2-k^2$ of (7.13) has its minima. At these frequencies (7.13) can be approximated by the dominating term with the minimum denominator,

$$U_{m,n}\approx\frac{j4\omega\mu h}{LW}\frac{K_s(x_{sp},y_{sp})K_{meas}(x,y)}{k_m^2+k_n^2-k^2}, \tag{7.16}$$

with the source dependent term

$$K_s(x_{sp},y_{sp})=I_{sp}\sin(k_m x_{sp})\sin(k_n y_{sp}), \tag{7.17}$$

and the term,

$$K_{meas}(x,y)=\sin(k_m x)\sin(k_n y), \tag{7.18}$$

which depends on the position of the voltage measurement. The index of $U_{m,n}$ denotes the cavity resonance mode, which is characterized by the integer pair m and n. Both $K_s(x_{sp},y_{sp})$ and $K_{meas}(x,y)$ vanish at the metallic enclosure walls. Therefore, placing a single current source closer to a metallic enclosure wall will reduce the cavity field and the emissions. Below the second resonance mode, the maximum field is in the middle of the slot at position $x=L/2$, $y=W$ and the maximum field in every enclosure cross section $y=y_{cr}\leq W$ is located at $x=L/2$. Increasing the distance of a single source from the symmetry line $x=L/2$ will reduce the emissions up to the second resonance frequency. The maxima of the enclosure field are at the enclosure slot $y=W$ for every resonance mode. According to (5.1) a trace above the ground plane of a PCB is not a single current source, because both, the source and the load currents, excite a cavity field. A short trace with negligible phase shift between the source and the load current couples to the cavity with the currents I_s at the source position and $I_l=-I_s$ at the load position. A superposition of two terms of (7.16), one with the excitation I_l and the other with the excitation $I_l=-I_s$ will consider the coupling from the

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short trace. Therefore, this trace coupling can be investigated with the derivatives of (7.17). Since the partial derivatives normal to the enclosure edges have their maxima at the metallic enclosure walls, the coupling of a differential source to the cavity is at a maximum, when it is positioned perpendicular and close to an enclosure wall. The partial derivative in x direction of (7.17) vanishes in the symmetry line $x = L/2$ below the second resonance. Therefore, a symmetric placement of a trace perpendicular to this symmetry line reduces the coupling and the emissions significantly below the second resonance of the enclosure. Both partial derivatives of (7.17) vanish in the middle of the slot at position $x = L/2$, $y = W$ up to the second resonance mode of the cavity field. Moving a differential source to that position in an arbitrary direction will reduce the coupling to the cavity at the first enclosure resonance. These design guidelines have been obtained simply by a discussion of the analytical cavity model equations. Although these rules have been extracted for the rectangular enclosure in Figure 7.1, the main facts regarding the placement of sources and traces close, parallel or perpendicular to metallic walls or enclosure symmetry lines can be generalized for arbitrarily shaped enclosures.

Perfect electrically conducting planes, air in the cavity, and a perfect magnetically conducting boundary at the slot have been used to derive the cavity field formulation (7.13), neglecting any losses, which leads to significant deviations at the resonance frequencies compared to a real lossy situation. An enclosure (Figure 7.1) usually has a much higher plane separation h than power-ground planes on a PCB. Therefore, the radiation loss becomes the dominant loss mechanism [45], [59], [101] and must be considered in the cavity model to obtain a reasonably good solution. The next section will consider the radiation loss in the cavity model and provide analytical expressions for the calculation of the radiated emissions from the slot. A quantitative investigation of radiated emission and coupling from sources to the enclosure will be presented based on that model. Quantitative classification of EMC design guidelines, such as placement and layout rules, is necessary to obtain information on their practical relevance for the intended application. An example for the relevance of quantitative EMC rule classification is the crosstalk from a digital signal trace to an analog circuit trace. Whether this coupling is relevant or not depends on the spectrum of the digital signal, the sensitivity of the analog circuit and the layout routing of the traces. A cost optimized design cannot be reached with global rules applied to all signals. An EMC engineer must have quantitative information, if the coupling is relevant for a decision about shielding, trace routing, and ground separation efforts.

The cavity modes depend on the cavity boundaries. Parallel rectangular planes with four open edges have been investigated for power integrity analysis purposes by [42] and [43]. They expressed the resonances of the rectangular power planes with

$$f_{r_{open}} = \frac{c_l}{2\pi}\sqrt{\left(\frac{m\pi}{L}\right)^2 + \left(\frac{n\pi}{W}\right)^2}. \tag{7.19}$$

Table 7.1 lists the resonance frequencies for the first modes of rectangular power-planes with four open edges and of a rectangular enclosure with three closed edges and one open slot according to Figure 7.1, both with the same size of L=160mm and W=120mm. Since (7.17) and (7.18) vanish for all $m = 0$, the enclosure resonances with $m = 0$ are compensated and do not exist.

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		power-planes		enclosure	
m	n	$f_{r_{open}}$ (MHz)	exists	f_r (MHz)	exists
0	0	0	no	625	no
1	0	938	yes	1127	yes
0	1	1250	yes	1875	no
1	1	1563	yes	2096	yes
2	0	1875	yes	1976	yes

Table 7.1: First resonance frequencies of rectangular parallel plane cavities with L=160mm and W=120mm and different boundaries. One with four open edges (power-planes), the other with one open slot and three closed metal edges (enclosure).

Power planes with four open edges have more resonances and different resonance frequencies than the enclosure. Resonance frequencies of the same modes are shifted some hundred MHz. In particular the first and the second resonance frequencies are interesting with respect to the previously mentioned design rules which are related to the symmetry line $x = L/2$ of the enclosure. In an enclosure with the dimensions L=160mm, W=120mm and $h = 15mm$, these rules are valid up to 1976 MHz, a broad band of the 2.5GHz CISPR25 frequency range according to Table 4.1.

7.2. Analytical consideration of the radiation loss and a model for the free space radiation from the enclosure slot

Analogous to patch antennas, the radiated field of the parallel-plate structure is conveniently calculated by the use of the equivalence source method [102], [104], [105], [106], described in Chapter 6. This method has been utilized by Leone [59] to calculate the free space radiation for parallel rectangular power planes with four open edges. Since the radiation loss of power planes with a very small plane separation is low compared to the conduction and the dielectric losses, [59] neglected the radiation loss. However, that is not sufficient in the case of power planes with higher plane separation and especially not for an enclosure, where the plane separation is much higher and the radiation loss becomes the dominant loss mechanism. [45] considered the radiation loss in the cavity field calculation with a quality factor which was obtained by a far field calculation of the lossless cavity model. However, this approach fails, because the radiation from the lossless model is much higher than that of a model which would correctly consider the radiation loss. Thus, the radiation loss obtained from the lossless model is too high, which explains the deviations of the calculation from the measurement results in [45]. Therefore, the domain separation method of Chapter 6 is utilized here to consider the radiation loss at the slot of the enclosure. A radiation loss admittance matrix from ports at the slot surface is obtained from a far field calculation without the cavity model. This loss admittance matrix is therefore independent of the cavity model and considers the radiation loss correctly for each voltage distribution along the slot surface. In a second step the admittance matrix is introduced into the cavity model and the common calculation yields the internal enclosure field and the slot field distribution under consideration of the radiation loss. The radiated far field is calculated from the slot field distribution utilizing a far field approximation approach. This provides an analytical model for efficient predesign investigations about the field distribution inside the enclosure, at the enclosure slot, and in the far field region.

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7.2.1. Calculation of the far field from the slot field distribution

The electromagnetic field from electric and magnetic current sources in an unbounded homogenous region can be expressed generally from

$$\vec{E} = -\vec{\nabla} \times \vec{F} + \frac{1}{j\omega\varepsilon}(\vec{\nabla} \times \vec{\nabla} \times \vec{A} - \vec{J}) \tag{7.20}$$

and

$$\vec{H} = \vec{\nabla} \times \vec{A} + \frac{1}{j\omega\mu}(\vec{\nabla} \times \vec{\nabla} \times \vec{F} - \vec{M}) \tag{7.21}$$

with

$$\vec{A}(\vec{r}) = \frac{1}{4\pi} \iiint \frac{\vec{J}(\vec{r}\,')e^{-jk|\vec{r}-\vec{r}\,'|}}{|\vec{r}-\vec{r}\,'|} \mathrm{d}\tau' \tag{7.22}$$

and

$$\vec{F}(\vec{r}) = \frac{1}{4\pi} \iiint \frac{\vec{M}(\vec{r}\,')e^{-jk|\vec{r}-\vec{r}\,'|}}{|\vec{r}-\vec{r}\,'|} \mathrm{d}\tau', \tag{7.23}$$

where $\vec{E}$ is the electric field density, $\vec{H}$ is the magnetic field density, $\vec{A}$ is the magnetic vector potential, $\vec{F}$ is the electric vector potential, $\vec{r}\,'$ is the vector to the magnetic and the electric current sources in (7.22) and (7.23) respectively, μ is the permeability, and ε is the permittivity of the homogenous region τ'. This is described in more detail in [102].
With the angle ξ between the vectors $\vec{r}$ and $\vec{r}\,'$, depicted in Figure 7.2, the distance $|\vec{r}_1|$ can be approximated with

$$\begin{aligned} |\vec{r}_1| = \sqrt{|\vec{r}|^2 + |\vec{r}\,'|^2 - 2|\vec{r}||\vec{r}\,'|\cos(\xi)} &\approx \sqrt{|\vec{r}|^2 - 2|\vec{r}||\vec{r}\,'|\cos(\xi) + (|\vec{r}\,'|\cos(\xi))^2} \\ &= |\vec{r}| - |\vec{r}\,'|\cos(\xi) = |\vec{r}| - \vec{r}\,'\vec{e}_r \end{aligned} \tag{7.24}$$

in the far field, where $|\vec{r}|$ becomes large compared to $|\vec{r}\,'|$. The direction of $|\vec{r}|$ is $\vec{e}_r$. For antennas with an active dimension D_a, such as, for example, the length of a dipole, or the length of an aperture, the far field region condition is

$$|\vec{r}| \geq \frac{2D_a^2}{\lambda_0} \tag{7.25}$$

according to [104]. The wavelength in air is λ_0.

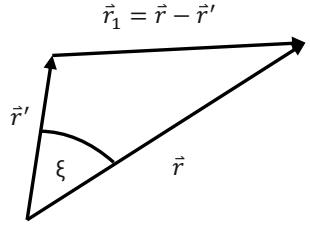

Figure 7.2: Angle ξ between the vectors $\vec{r}$ and $\vec{r}\,'$.

With (7.24) the electric vector potential (7.23) in the far field region becomes

$$\vec{F}(\vec{r}) \approx \frac{1}{4\pi} \frac{e^{-jk|\vec{r}|}}{|\vec{r}|} \iiint \vec{M}(\vec{r}\,')e^{jk\vec{r}\,'\vec{e}_r} \mathrm{d}\tau'. \tag{7.26}$$

The magnetic vector potential becomes

$$\vec{A}(\vec{r}) \approx \frac{1}{4\pi} \frac{e^{-jk|\vec{r}|}}{|\vec{r}|} \iiint \vec{J}(\vec{r}\,')e^{jk\vec{r}\,'\vec{e}_r} \mathrm{d}\tau'. \tag{7.27}$$

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The radiation from the enclosure is mainly determined by the electric voltage distribution at the slot [59]. From this voltage distribution an equivalent magnetic source current on the slot is obtained as depicted in Figure 7.3 for the calculation of the radiated electric far field. With (7.20) the electric far field from magnetic current sources

$$\vec{E} = -\vec{\nabla} \times \vec{F} \tag{7.28}$$

is applied on (7.26) to obtain the far field approximation for the electric field density

$$\vec{E}(\vec{r}) \approx \frac{jk}{4\pi} \frac{e^{-jk|\vec{r}|}}{|\vec{r}|} \iiint M(\vec{r}\,') e^{jk\vec{r}\,'\vec{e}_r} (\vec{e}_r \times \vec{e}_m) \mathrm{d}\tau', \tag{7.29}$$

according to [59], [69], where $\vec{e}_m$ is the direction of the magnetic current density $\vec{M}(\vec{r}\,')$.

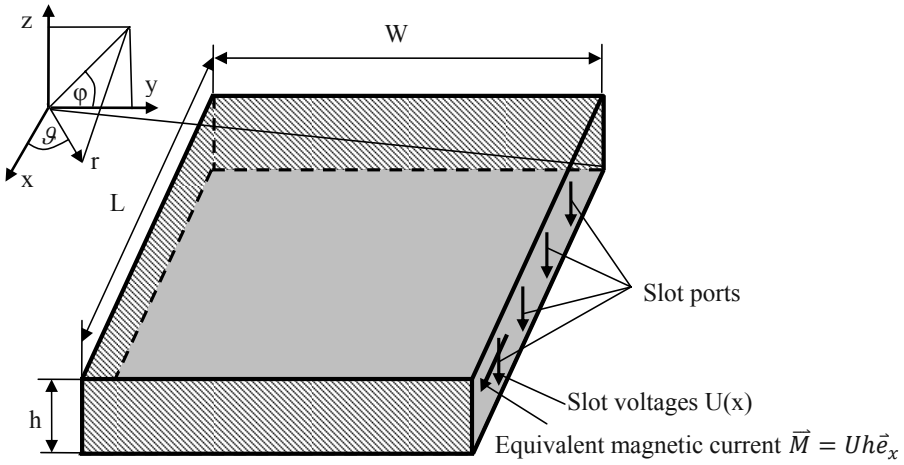

Figure 7.3: Equivalent magnetic current sources at the enclosure slot for the derivation of the radiated far field from the slot. This spherical angle definition was used, because it enables simpler radiation field expressions.

With the coordinate system definition and the equivalent magnetic current sources at the slot depicted in Figure 7.3, (7.29) for the electric far field becomes

$$\vec{E}_{far} = -\frac{jk}{4\pi} \frac{e^{-jkr}}{r} \sin(\vartheta) \vec{e}_\varphi \int_{x=0}^{L} \left\{ U(x) e^{jkx\cos(\vartheta)} \mathrm{d}x \right\}. \tag{7.30}$$

The magnetic far field is described with

$$\vec{H}_{far} = -\frac{jk^2}{4\pi} \frac{e^{-jkr}}{r} \frac{1}{\omega\mu} \sin(\vartheta) \vec{e}_\vartheta \int_{x=0}^{L} \left\{ U(x) e^{jkx\cos(\vartheta)} \mathrm{d}x \right\} \tag{7.31}$$

accordingly. With a declaration of p interface ports at the slot of the enclosure, (7.30) is discretized to

$$\vec{E}_{far} = -\frac{jk}{4\pi} \frac{e^{-jkr}}{r} \sin(\vartheta) \vec{e}_\varphi \frac{L}{p} \sum_{i=1}^{p} \left\{ U_i e^{jkx_i\cos(\vartheta)} \right\} \tag{7.32}$$

and (7.31) is discretized to

$$\vec{H}_{far} = -\frac{jk^2}{4\pi} \frac{e^{-jkr}}{r} \frac{1}{\omega\mu} \sin(\vartheta) \vec{e}_\vartheta \frac{L}{p} \sum_{i=1}^{p} \left\{ U_i e^{jkx_i\cos(\vartheta)} \right\}. \tag{7.33}$$

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U_i denote the voltages at the p slot ports with the integer index $i \in [1, p]$. The far field condition (7.25) for the enclosure depicted in Figure 7.3 becomes

$$|\vec{r}| \geq \frac{2L^2}{\lambda_0} \tag{7.34}$$

7.2.2. Derivation of an admittance matrix for the consideration of the radiation loss at the cavity field simulation

The pointing vector

$$\vec{S} = \vec{E} \times \vec{H}^* \tag{7.35}$$

is obtained from a multiplication of (7.32) and (7.33). Since this is a multiplication of the two summations, every term in the summation of (7.32) is multiplied with every term in the summation of (7.33), yielding p^2 terms,

$$\vec{S}_{cr} = \frac{k^3}{16\pi^2}\frac{1}{\omega\mu}\sin^2(\vartheta)\vec{e}_r\left(\frac{L}{p}\right)^2 U_c U_r^* e^{[jk(x_c - x_r)\cos(\vartheta)]}, \tag{7.36}$$

which are the self- and mutual pointing vectors of the slot ports with the indexes c and r. An integration of these vectors over the sphere is carried out to obtain the total power values of the slot ports with the indexes c and r.

$$S_{cr} = \frac{k^3}{8\pi^2\omega\mu}U_c U_r^*\left(\frac{L}{p}\right)^2 \int_{\vartheta=0}^{\pi}\left\{\sin^3(\vartheta)e^{[jk(x_c - x_r)\cos(\vartheta)]}\mathrm{d}\vartheta\right\} \tag{7.37}$$

This pointing power is divided through the voltages U_c and U_r^* on the slot ports c and r, respectively, to obtain an admittance matrix element

$$Y_{a\_cr} = \frac{S_{cr}}{U_c U_r^*} = \frac{k^3}{8\pi^2\omega\mu}\left(\frac{L}{p}\right)^2 \int_{\vartheta=0}^{\pi}\left\{\sin^3(\vartheta)e^{[jk(x_c - x_r)\cos(\vartheta)]}\mathrm{d}\vartheta\right\} \tag{7.38}$$

assigned to these slot ports. The index c denotes the column and the index r denotes the row of the admittance matrix element Y_{a_cr} in the admittance matrix $\mathbf{Y}_a$. Since (7.38) is independent of the voltages at the slot ports, the admittance matrix $\mathbf{Y}_a$ enables the far field pointing power for arbitrary slot port voltage distributions to be calculated. Equation (7.38) was obtained without utilizing the cavity model and is therefore independent of that model. A connection of the admittance network described with $\mathbf{Y}_a$ to p slot ports declared in a cavity model is an analytical application of the domain decomposition approach in Chapter 6, because the admittance matrix introduces the influence of the free space radiation into the cavity model. This enables the correct consideration of the radiation loss in the cavity field calculation.
With this cavity model simulation which considers the radiation loss, the radiated electric far field is calculated from the slot port voltages utilizing (7.32) and the radiated magnetic far field is calculated with (7.33). Equations (7.32) and (7.33) have only one vector component in the spherical coordinate system, defined in Figure 7.3. Equation (7.38) is also much simpler with this coordinate system definition, compared to the commonly used definition. The number of ports p that is necessary to achieve certain accuracy depends on the maximum frequency. A calculation with increased p can be carried out to check whether p is sufficiently high.

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7.2.3. Introduction of the radiation loss admittance matrix into the cavity model matrix

The relation of the port voltages to the port currents is given by the impedance matrix

$$\begin{pmatrix} U_m \\ U_s \\ U_l \\ U_1 \\ \vdots \\ U_p \end{pmatrix} = \begin{pmatrix} Z_{mm} & Z_{ms} & Z_{ml} & Z_{m1} & \dots & Z_{mp} \\ Z_{sm} & Z_{ss} & Z_{sl} & Z_{s1} & \dots & Z_{sp} \\ Z_{lm} & Z_{ls} & Z_{ll} & Z_{l1} & \dots & Z_{lp} \\ Z_{1m} & Z_{1s} & Z_{1l} & Z_{11} & \dots & Z_{1p} \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ Z_{pm} & Z_{ps} & Z_{pl} & Z_{p1} & \dots & Z_{pp} \end{pmatrix} \begin{pmatrix} I_m \\ I_s \\ I_l \\ I_1 \\ \vdots \\ I_p \end{pmatrix} \tag{7.39}$$

where indexes m, s, and l are assigned to a measurement port, a port at the source position of a trace inside the enclosure, and a port at the load position of this trace, respectively. The indices 1 to p are assigned to the interface ports at the slot of the enclosure. The elements of the impedance matrix are calculated analytically with (7.14) for a slim ($h \ll \lambda$) rectangular enclosure with a slot on one edge. With $I_m = 0$ at the voltage measurement port, matrix (7.39) is separated to the slot port matrix equation

$$\begin{pmatrix} U_1 \\ \vdots \\ U_p \end{pmatrix} = \begin{pmatrix} Z_{1s} & Z_{1l} \\ \vdots & \vdots \\ Z_{ps} & Z_{pl} \end{pmatrix} \begin{pmatrix} I_s \\ I_l \end{pmatrix} + \begin{pmatrix} Z_{11} & \dots & Z_{1p} \\ \vdots & \ddots & \vdots \\ Z_{p1} & \dots & Z_{pp} \end{pmatrix} \begin{pmatrix} I_1 \\ \vdots \\ I_p \end{pmatrix} \tag{7.40}$$

with the matrix notation

$$\mathbf{U}_p = \mathbf{Z}_{ps}\mathbf{I}_s + \mathbf{Z}_{pp}\mathbf{I}_p, \tag{7.41}$$

and the measurement port matrix equation

$$U_m = \begin{pmatrix} Z_{ms} & Z_{ml} \end{pmatrix} \begin{pmatrix} I_s \\ I_l \end{pmatrix} + \begin{pmatrix} Z_{m1} & \dots & Z_{mp} \end{pmatrix} \begin{pmatrix} I_1 \\ \vdots \\ I_p \end{pmatrix} \tag{7.42}$$

with the matrix notation

$$\mathbf{U}_m = \mathbf{Z}_{ms}\mathbf{I}_s + \mathbf{Z}_{mp}\mathbf{I}_p. \tag{7.43}$$

The admittance matrix $\mathbf{Y}_a$ with the elements from (7.38) relates the voltage vector $\mathbf{U}_p$ to the the current vector $\mathbf{I}_p$ at the interface ports with

$$\mathbf{U}_p = -\mathbf{Y}_a^{-1}\mathbf{I}_p. \tag{7.44}$$

This leads to the final formulation for the voltage on the test port

$$\mathbf{U}_m = (\mathbf{Z}_{ms} - \mathbf{Z}_{mp}(\mathbf{Z}_{pp} + \mathbf{Y}_a^{-1})^{-1}\mathbf{Z}_{ps})\mathbf{I}_s, \tag{7.45}$$

and the voltages on the interface ports

$$\mathbf{U}_p = \mathbf{Y}_a^{-1}(\mathbf{Z}_{pp} + \mathbf{Y}_a^{-1})^{-1}\mathbf{Z}_{ps}\mathbf{I}_s. \tag{7.46}$$

When the radiation loss becomes very low, $\mathbf{Y}_a$ is almost singular. For a nearly singular $\mathbf{Y}_a$, (7.45) can be simplified to

$$\mathbf{U}_m = \mathbf{Z}_{ms}\mathbf{I}_s \tag{7.47}$$

and (7.46) to

$$\mathbf{U}_p = \mathbf{Z}_{ps}\mathbf{I}_s, \tag{7.48}$$

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to avoid matrix inversion in such a case. Since (7.47) and (7.48) neglect the radiation loss, these equations may only be used at frequencies, where $\mathbf{Y}_a$ is nearly singular.
The internal enclosure voltages and the slot voltages between the metallic cover and bottom plane are modeled accurately with (7.45), (7.46), (7.47), and (7.48). With the voltages at the slot (7.32) and (7.33) the free space far field radiation from the enclosure slot can be calculated analytically. This model enables efficient, quantitative investigations in the predesign phase of a device, especially regarding placement decisions. Design rules, derived from the discussion of the analytical cavity model in Section 5.8 and Subsection 7.1.3 are investigated in Chapter 8 regarding their quantitative relevance in the radiated far field.

7.2.4. Summary of the equations for the introduction of the radiation loss into the cavity model and the far field calculation

Radiation loss consideration and far field equations	Reference
$\vec{E}_{far} = -\frac{jk}{4\pi}\frac{e^{-jkr}}{r}\sin(\vartheta)\vec{e}_{\varphi}\frac{L}{p}\sum_{i=1}^{p}\left\{U_i e^{jkx_i\cos(\vartheta)}\right\}$	(7.32)
$\vec{H}_{far} = -\frac{jk^2}{4\pi}\frac{e^{-jkr}}{r}\frac{1}{\omega\mu}\sin(\vartheta)\vec{e}_{\vartheta}\frac{L}{p}\sum_{i=1}^{p}\left\{U_i e^{jkx_i\cos(\vartheta)}\right\}$	(7.33)
$\mathbf{Y}_a : Y_{a\_cr} = \frac{k^3}{8\pi^2\omega\mu}\left(\frac{L}{p}\right)^2\int_{\vartheta=0}^{\pi}\left\{\sin^3(\vartheta)e^{[jk(x_c-x_r)\cos(\vartheta)]}\mathrm{d}\vartheta\right\}$ with $c,r = 1..p$	(7.38)
$\mathbf{U}_m = (\mathbf{Z}_{ms} - \mathbf{Z}_{mp}(\mathbf{Z}_{pp} + \mathbf{Y}_a^{-1})^{-1}\mathbf{Z}_{ps})\mathbf{I}_s \quad \vert\, [\kappa(\mathbf{Y}_a) - 1] \leq S_{min}$	(7.45)
$\mathbf{U}_m = \mathbf{Z}_{ms}\mathbf{I}_s \quad \vert\, [\kappa(\mathbf{Y}_a) - 1] > S_{min}$	(7.47)
$\mathbf{U}_p = \mathbf{Y}_a^{-1}(\mathbf{Z}_{pp} + \mathbf{Y}_a^{-1})^{-1}\mathbf{Z}_{ps}\mathbf{I}_s \quad \vert\, [\kappa(\mathbf{Y}_a) - 1] \leq S_{min}$	(7.46)
$\mathbf{U}_p = \mathbf{Z}_{ps}\mathbf{I}_s \quad \vert\vert\, [\kappa(\mathbf{Y}_a) - 1] > S_{min}$	(7.48)
$\kappa(\mathbf{Y}_a) = \lvert\lambda_{max}(\mathbf{Y}_a)/\lambda_{min}(\mathbf{Y}_a)\rvert$	-
$\mathbf{Z}_{ps} = \begin{pmatrix} Z_{1s} & Z_{1l} \\ \vdots & \vdots \\ Z_{ps} & Z_{pl} \end{pmatrix}$	(7.40), (7.41)
$\mathbf{Z}_{pp} = \begin{pmatrix} Z_{11} & \dots & Z_{1p} \\ \vdots & \ddots & \vdots \\ Z_{p1} & \dots & Z_{pp} \end{pmatrix}$	(7.40), (7.41)
$\mathbf{Z}_{ms} = \begin{pmatrix} Z_{ms} & Z_{ml} \end{pmatrix}$	(7.42), (7.43)
$\mathbf{Z}_{mp} = \begin{pmatrix} Z_{m1} & \dots & Z_{mp} \end{pmatrix}$	(7.42), (7.43)

The condition number of matrix $\mathbf{Y}_a$ is $\kappa(\mathbf{Y}_a)$ and $\lambda_{max}(\mathbf{Y}_a)$ and $\lambda_{min}(\mathbf{Y}_a)$ are the maximum and minimum eigenvalues, respectively. S_{min} denotes a threshold value which determines whether or not matrix $\mathbf{Y}_a$ is nearly singular. An extension of the equations to include more ports is performed by simply adding additional rows and columns to the matrixes.

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7.3. Comparison of the analytical model results to HFSS® simulations and measurement results

For the validation of the analytical models of Section 7.1 and Section 7.2, results for the electric far field density from an enclosure with dimensions depicted in Figure 7.4 are obtained with the analytical models, with three-dimensional full wave simulation, and with measurements.

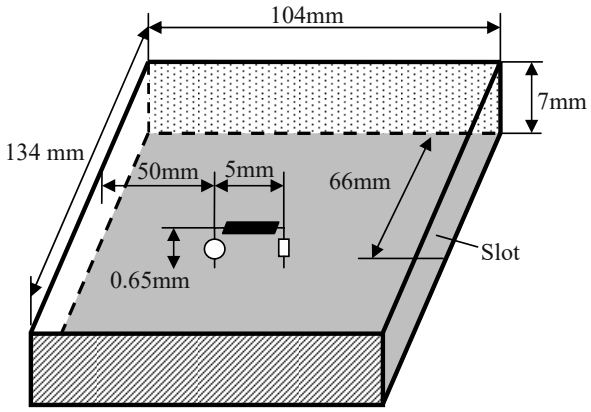
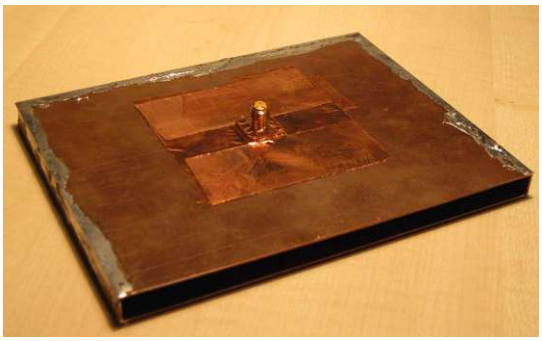


Figure 7.4: Enclosure dimensions and source position for the validation of the analytical model results for the electric far field.

The geometric dimensions are practically relevant, because they are similar to those of the parallel plane cavity between the PCB ground plane and the enclosure bottom of a typical automotive control device depicted in Figure 1.1(a). However, there are geometrical deviations between the shape of an automotive control device enclosure and a rectangular enclosure. Therefore, the validation of the analytical model is carried out on a rectangular test enclosure. The test enclosure in Figure 7.5 is manufactured from copper sheets which are soldered together at the edges. Thus, the geometry dimensions of the test enclosure match the simulation models. The comparison is carried out for $0\,\Omega$, $50\,\Omega$, and $1e9\,\Omega$ (open in the measurement). A removable SMA connector with a short copper trace soldered to the rigid SMA wire was used to enable the change of the trace loads. Figure 7.5(a) depicts the test enclosure with mounted SMA connector.



(a) Enclosure with removable SMA connector.

(b) SMA connector with test trace removed.

Figure 7.5: Copper test enclosure for the validation with measurements.

To obtain a reasonably good contact of the SMA connector ground to the enclosure, a conducting silver painting and conducting copper tapes were used to mount the connector.

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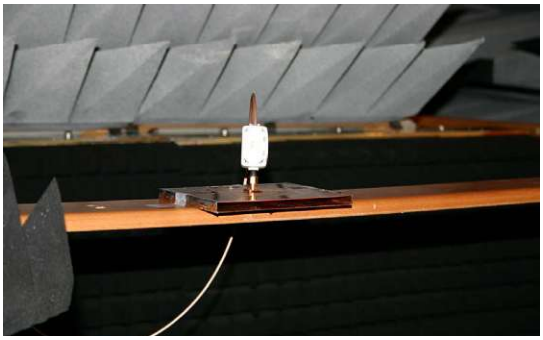
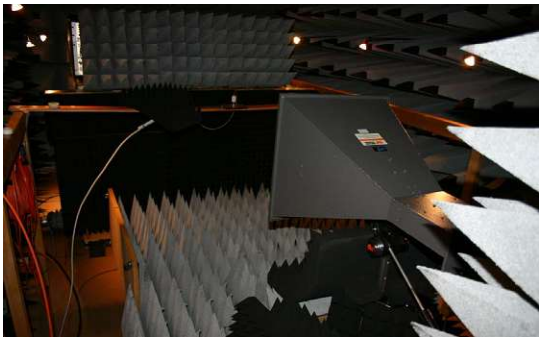
Before mounting the connector, the copper plane surface was cleaned accurately and the surface oxide was removed. Figure 7.5(b) shows the test enclosure with removed SMA connector. The measurements have been carried out with a horn antenna (Amplifier Research [107] AT4002A in Figure 7.6(d)) and a vector network analyzer (Rhode & Schwarz ZVB4) inside a semi-anechoic chamber. Pyramid absorbers have been added on the bottom of the chamber, between the measurement antenna and the test device to obtain similar conditions to those in a fully anechoic chamber. These absorbers can be seen in Figure 7.6(a). The electric field was calculated and measured 1m in front of the enclosure slot. This position has been selected as the main lob of the electric field distribution is oriented in this direction for some of the resonance frequencies within the evaluated frequency range of 800 MHz to 4 GHz. The position is consistent with CISPR 25 Edition 3 [56] for automotive component emission measurements above 1 GHz. A measurement setup overview is depicted in Figure 7.6(c) and the connection of the network analyzer cable to the enclosure SMA connector is depicted in Figure 7.6(b). Table 7.2 contains a summary of the measurement equipment.

(a) Bottom absorbers for anechoic conditions.



(b) Connection of the enclosure.



(c) Measurement setup overview.

(d) Antenna (Amplifier Research AT4002A).

Figure 7.6: Setup for the validation measurement with a horn antenna from 800MHz to 4GHz.

Equipment	Designation	Supplier
Horn antenna	AT4002A	Amplifier Research [107]
Network analyzer	ZVB4	Rhode & Schwarz [108]
Calibration set	R&S®ZV-Z21	Rhode & Schwarz [108]
Ferrite Sleeve	7427114	Würth Elektronik [109]
Ferrite Sleeve	7427733	Würth Elektronik [109]

Table 7.2: Measurement equipment.

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Ferrite sleeves have been arranged on the coaxial cables, close to the connectors, to suppress currents on the cable shield. The ferrite sleeve, 7427114 from Würth Elektronik [109], applied close to the SMA connector of the enclosure provides an impedance of about 200 Ω at about 1 GHz. A second sleeve 7427733 was applied on the antenna cable. The network analyzer was calibrated with a two port TOSM calibration using the calibration set R&S®ZV-Z21 from Rhode & Schwarz [108]. The measurement bandwidth was 10Hz for maximum noise suppression. The comparison of the cavity model results, the HFSS® simulation results, and the measurement results depicted in Figure 7.8 shows a reasonably good agreement. This confirms the analytical models of Section 7.1 and Section 7.2. The utilized equation (7.32) for the electric far field considers only the radiation from the enclosure slot and neglects the metallic enclosure walls that have some influence on the radiation diagram above the first resonance frequency. However, this is a reasonable simplification, also applied to obtain basic radiation characteristics of horn antennas [104]. Therefore, (7.32) can be used to obtain a good first order information about the radiated field. Figure 7.8 shows not only slight deviations between the measurement results and the cavity model results. It also shows some deviations of the measurement results from the results of the three-dimensional full wave simulation with HFSS®, which considers the influence of the enclosure walls. Thus, the comparison deviations in Figure 7.8 can be explained mainly from the test enclosure tolerances and test site uncertainties. However, there are maximal 3dB magnitude deviations between the maxima of the cavity model results and the measurements.

The consideration of the radiation loss for the calculation of the slot voltages is crucial to obtain the correct voltage distribution inside the enclosure and the correct radiated far field. Figure 7.7 shows a comparison between the electric far-field obtained from a cavity field model which considers the radiation loss and a cavity model which neglects the radiation loss. For practical simulation investigations an EMC engineer needs quantitative information about the electric far field magnitude, especially at the resonances at which the radiation is at its maximum. A model that neglects the radiation loss with deviations at the resonances of more than 30dB is not sufficient for EMC simulation purposes.

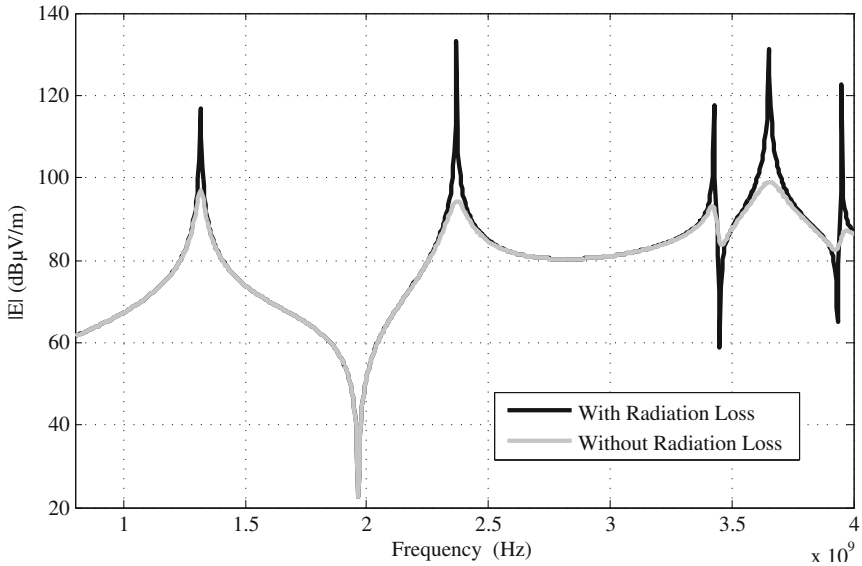

Figure 7.7: Electric far field, one meter in front of the enclosure slot. Comparison of the cavity model results, which includes the radiation loss by introducing the admittance matrix $\mathbf{Y}_a$, into the results obtained from a cavity field which does not consider the radiation loss.

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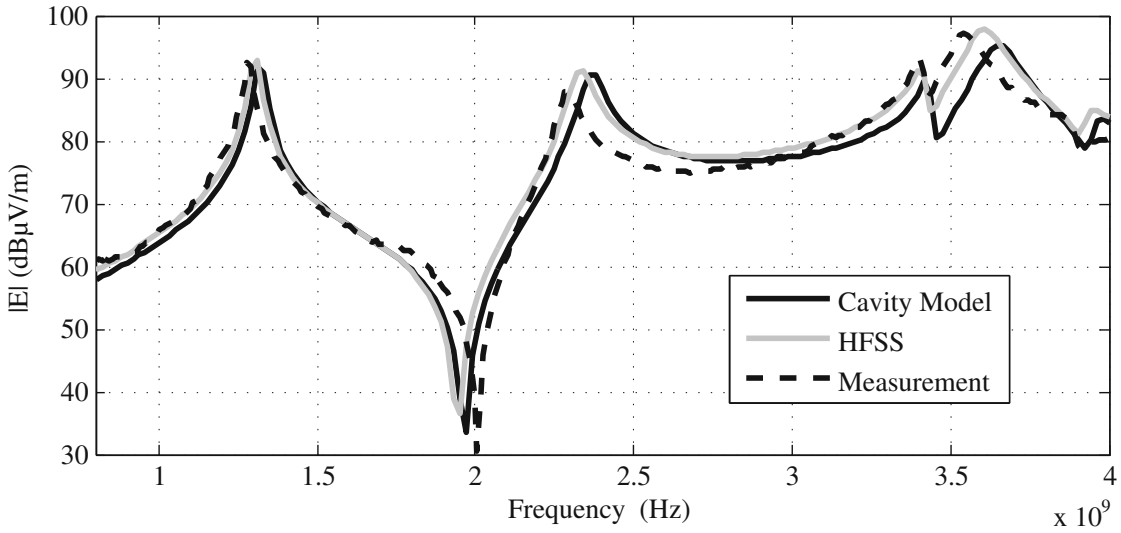
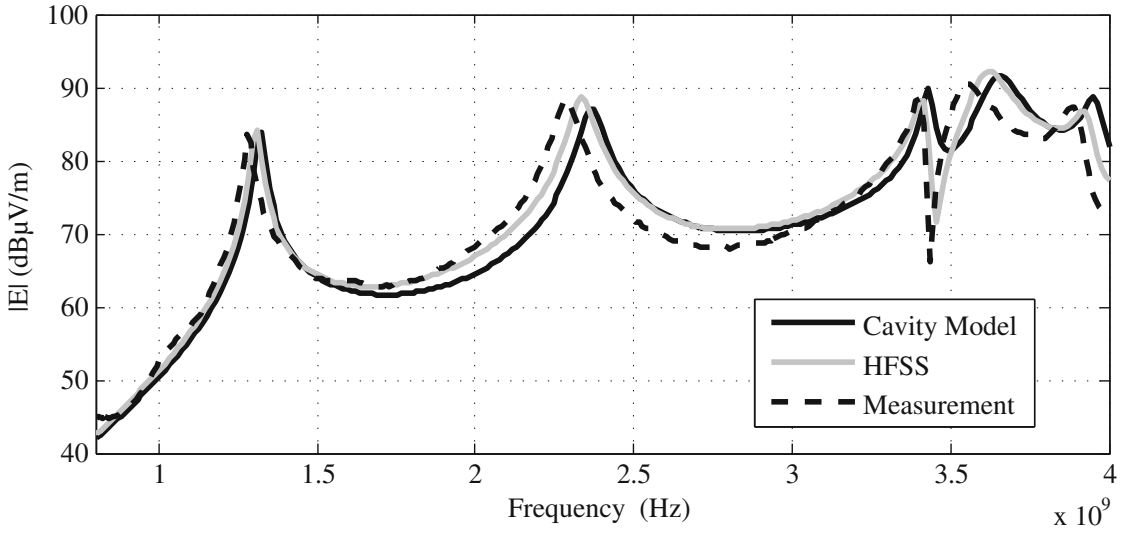
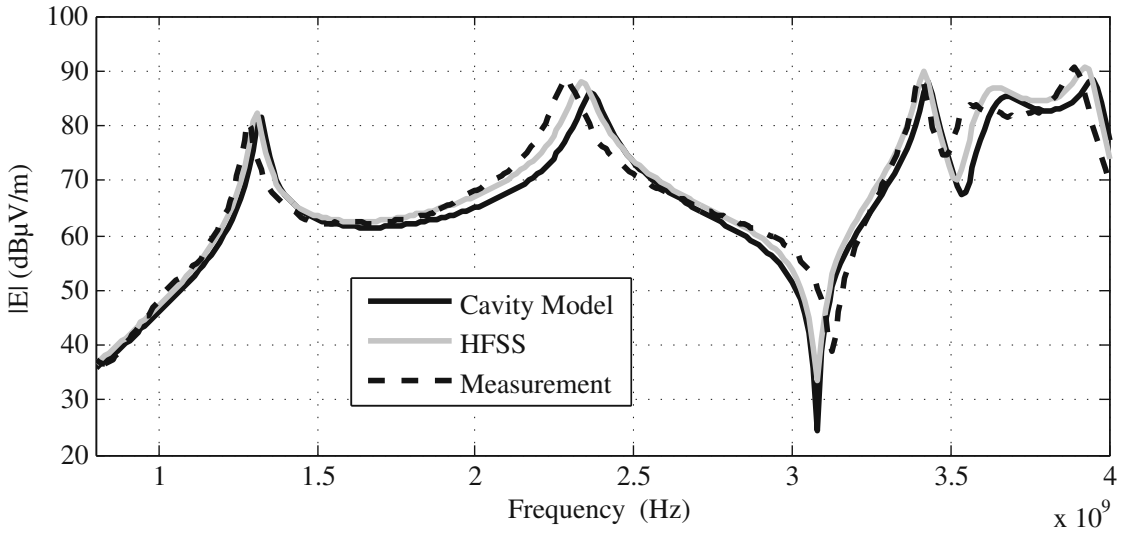


(a) Load: 0 Ω.



(b) Load: 50 Ω.



(c) Load: 1*e*9 Ω.

Figure 7.8: Electric far-field 1m in front of the enclosure slot. Comparison of the cavity model results with the HFSS® simulation results and measurement results.

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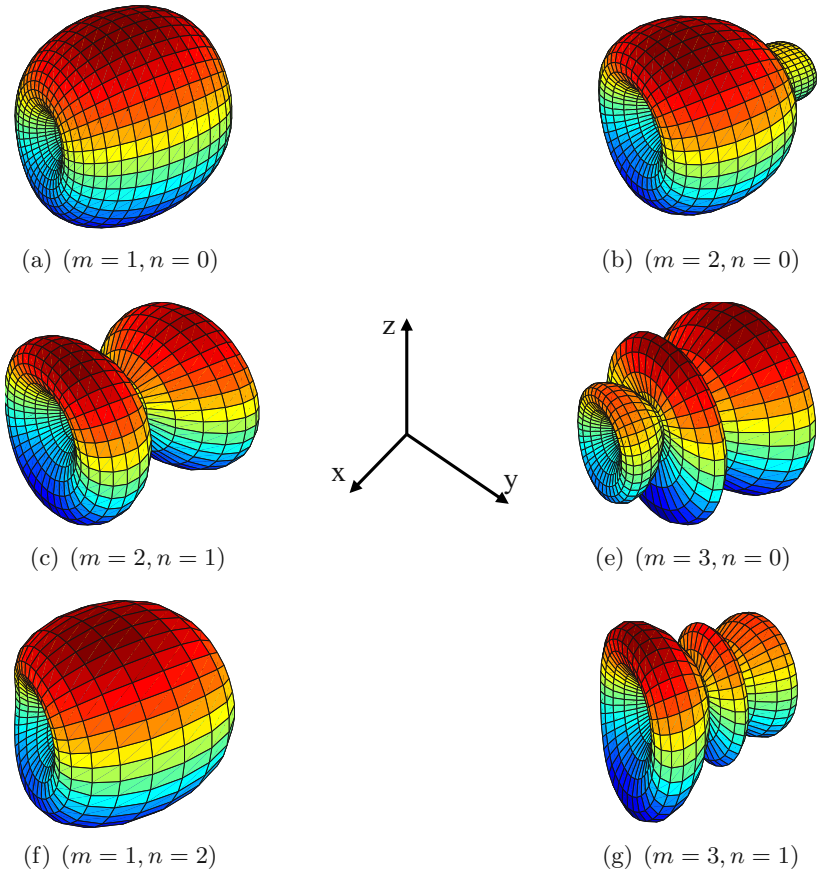
7.4. Radiation diagrams for the rectangular enclosure with a slot on one edge

Radiation diagram shapes vary with the positions, the amplitudes, and the phase relations of the parallel plane excitation currents. For instance, placing a trace symmetric to the symmetry line of the enclosure compensates the first resonance and thus changes the shape of the radiation diagram. The radiation diagrams for the first six resonance modes of a rectangular enclosure with the dimensions $L = 134mm$, $W = 104mm$, $h = 7mm$ and the excitation current position at $x = L/4 = 33.5mm$, $y = -3W/4 = -78mm$ are presented in Figure 7.9. After the calculation of the voltages at the slot ports, the diagrams have been obtained with (7.32). A method for an approximate estimation of the enclosure wall influences was presented in [110]. The accurate calculation of the walls requires three-dimensional full wave simulation. However, the directivity and also the wall influence is low for an enclosure with $h \ll \lambda$ and the diagrams obtained with (7.32) provide good first order information about the spherical radiated field distribution.
The diagrams in Figure 7.9 also show significant radiation on the back side of the enclosure. A shift of the source position out of the symmetry line of the enclosure causes asymmetry in the radiation diagram. The main lob is oriented parallel to the symmetry line of the enclosure in the middle of the slot up to the first enclosure resonance. This is also the main lob orientation for many higher order modes.



(a) $(m = 1, n = 0)$ (b) $(m = 2, n = 0)$

(c) $(m = 2, n = 1)$ (e) $(m = 3, n = 0)$

(f) $(m = 1, n = 2)$ (g) $(m = 3, n = 1)$

Figure 7.9: Radiation diagrams of a rectangular enclosure with dimensions $L = 134mm$, $W = 104mm$ and $h = 7mm$. A single source is driving a current from the cover to the bottom plane at position $x = L/4 = 33.5mm$, $y = -3W/4 = -78mm$.

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8. Design rules for PCBs inside a metallic enclosure with apertures

PCB EMC rules are commonly used to obtain a PCB layout with sufficiently good EMC properties to achieve EMC compliance of a device. Design guidelines for PCB layout are described by [111], [112], [113], [114], and [115]. The four most important PCB design rules are [111]:

- ➢ Minimize the loop areas associated with high-frequency power and signal currents.
- ➢ Do not split, gap, or cut the signal return plane.
  - ⇨ A nearby current return path has to be provided for transient signal traces.
- ➢ Do not locate high-speed circuitry between connectors.
- ➢ Control signal transition times.
  - ⇨ Use a logic family which is only as fast as the application requires.
  - ⇨ Put a resistor or a ferrite in series with a device's output.

Additional rules depend on the application and on the enclosure of the device. The EMC performance of a device with a metallic enclosure and a PCB inside depends on the coupling of the sources on the PCB to the field at the apertures of the enclosure. The aperture field causes direct radiation and coupling to cables which are leaving the enclosure. Feed through filters are a solution to reduce the EMI from these cables. However, this is too costly for devices with multiple pin connectors, such as, for example, boards with backplane connectors or automotive control devices as depicted in Figure 1.1(a). The field coupling from traces and components on the PCB to the enclosure apertures is not only relevant for the electromagnetic emission from a device. The coupling from internal sources to the external field is the same as the coupling from external sources to the internal field, according to the reciprocal principle [102]. Therefore, the coupling is also relevant for the susceptibility of a device. This chapter investigates the quantitative differences of the radiated power from the slot of a slim rectangular enclosure between different trace connection routings and source placements on the PCB. Traces are modeled with 0.2mm width and 0.65mm height above the ground plane. They are driven with a 10mV source voltage with a source impedance equal to the characteristic impedance of the trace Z_w. This simulates an IC driver output with correct series termination. At the load position traces are terminated with a 10pF capacitance, simulating the input capacitance of typical IC inputs. Although the values will vary for real devices and other trace geometries, the comparison provides a reasonable quantitative insight for practically situations. For single sources a source current of 10μA is used in the calculations. One may weight the diagram values with the actual harmonic magnitude values of signals in a dedicated application to obtain quantitative first order predesign information about the EMC performance of a device. The design rules in Section 5.8 and in Section 7.1.3 are validated to provide quantitative information about their relevance on the design. Especially the rules regarding the trace routing close to metallic enclosure walls can be generalized to arbitrary enclosure shapes. Finally, this chapter presents a table with a summary of the extracted rules with quantitative information.

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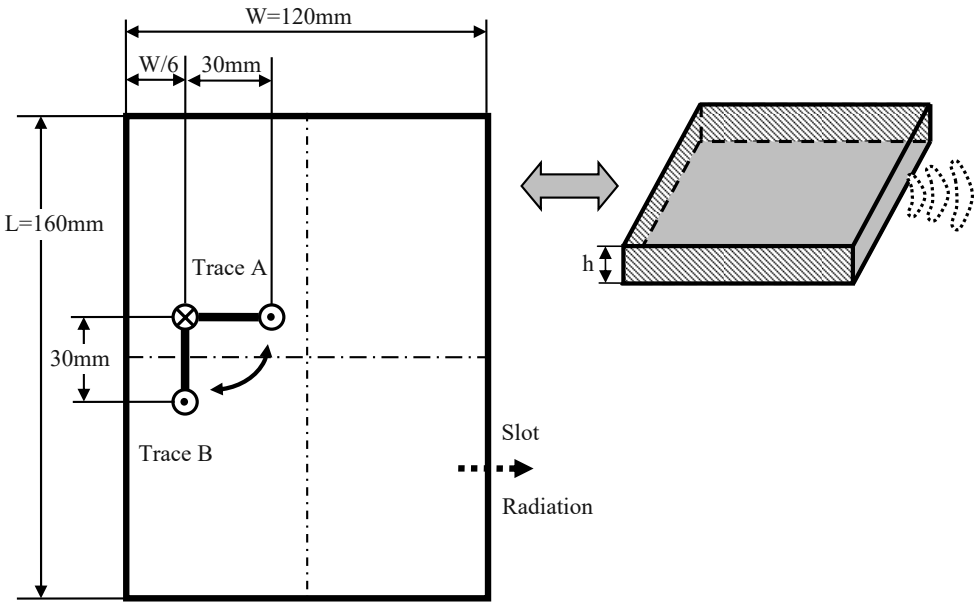
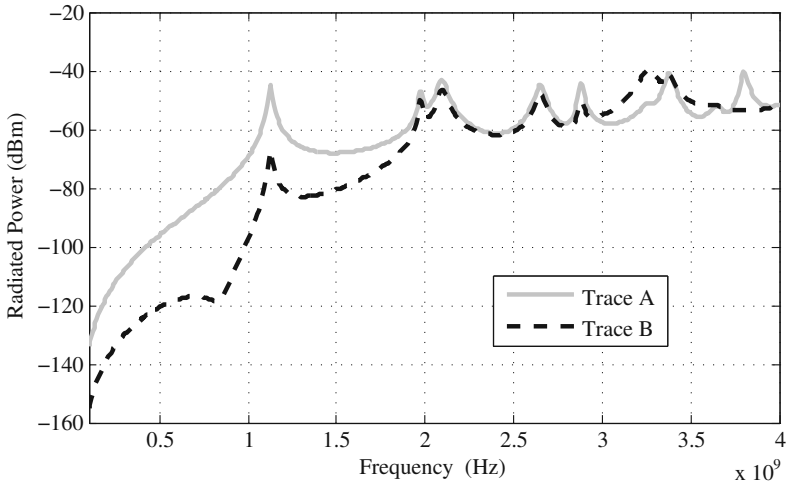
8.1. Rule 1: Trace placement symmetric to the enclosure symmetry reduces the coupling up to the second enclosure resonance

Figure 8.1(b) shows a radiated power reduction of 20dB below 1.2GHz and yet 10dB up to 1.5GHz, when the trace placement is changed from that of Trace A to that of Trace B, as depicted in Figure 8.1(a). It is recommended to place critical traces symmetric to the enclosure symmetry line. This must be considered when placing the driver and source IC on the PCB layout. Therefore, the rule cannot be used for every trace on the PCB and the designer should focus on critical signal lines, such as, for instance, fast clock signal traces.



(a) Placement of Trace A and Trace B.



(b) Overall radiated power from the enclosure slot.

Figure 8.1: The trace width is 0.2mm, the trace height above the ground plane is 0.65mm. A 10mV voltage source with an impedance equal to the characteristic impedance of the trace Z_w drives the trace which is terminated with a 10pF capacitance.

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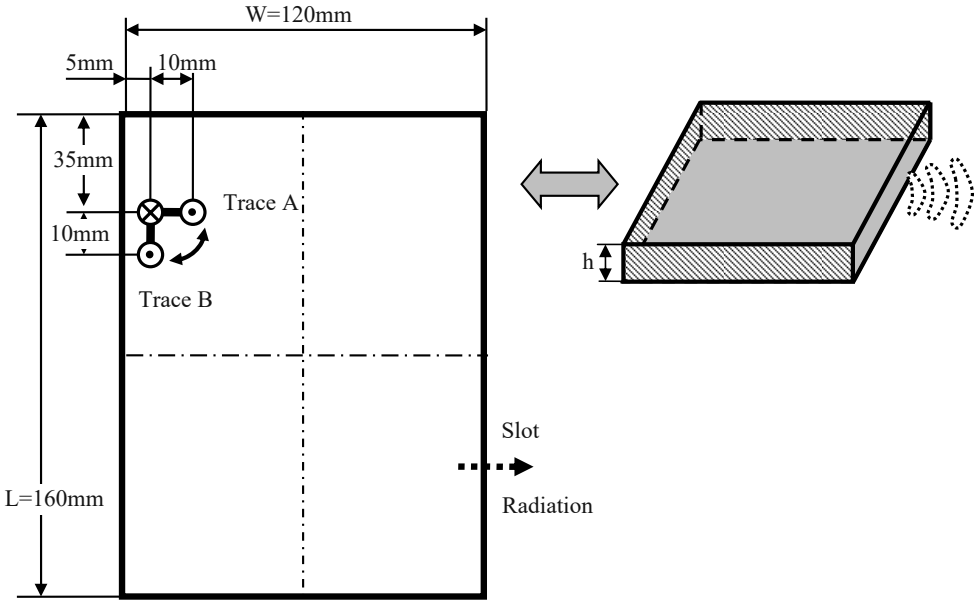
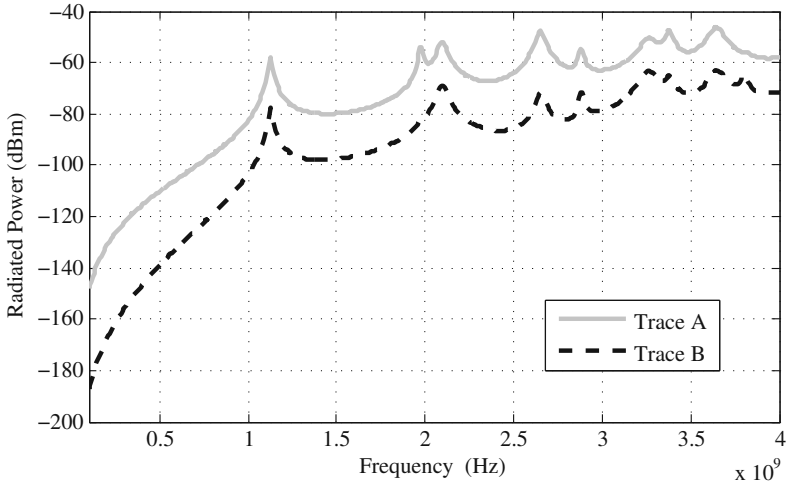
8.2. Rule 2: Trace placement parallel and close to metallic enclosure walls reduces EMI, trace placement orthogonal and close to enclosure walls increases EMI

Figure 8.2(b) shows a radiated power reduction of 20dB over the whole frequency range from 100MHz to 4GHz when the trace placement is changed from that of Trace A to that of Trace B, as depicted in Figure 8.2(a). It is recommended to place critical traces parallel and close to the metallic enclosure walls. This must already be considered, when placing the driver and receiver ICs on the PCB.



(a) Placement of Trace A and Trace B.



(b) Overall radiated power from the enclosure slot.

Figure 8.2: The trace width is 0.2mm, the trace height above the ground plane is 0.65mm. A 10mV voltage source with an impedance equal to the characteristic impedance of the trace Z_w drives the trace which is terminated with a 10pF capacitance.

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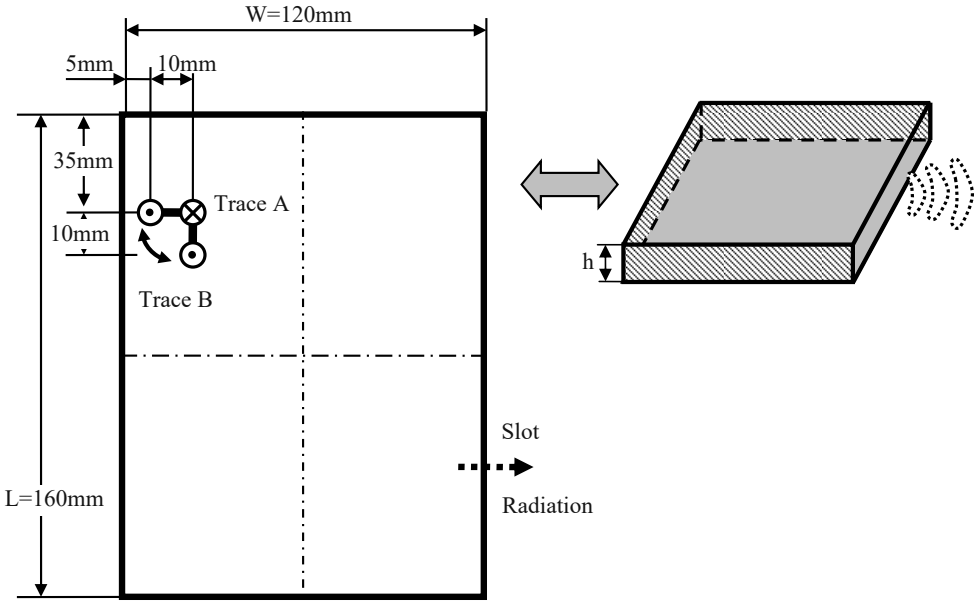
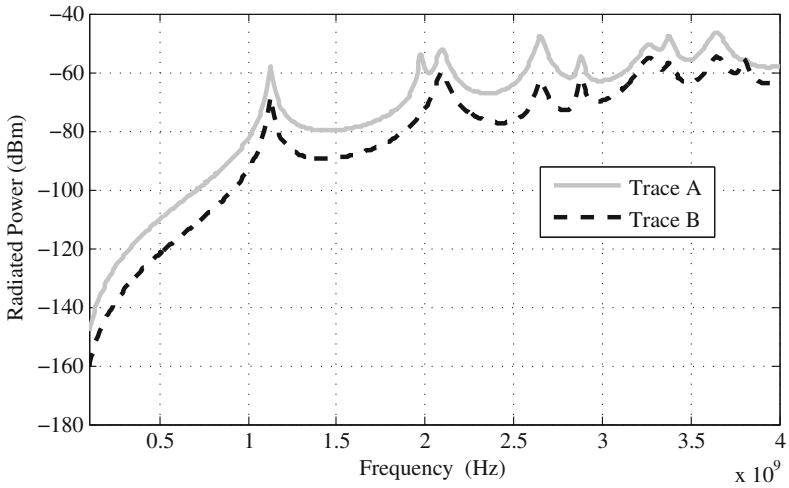
Trace B in Figure 8.2(a) is closer to the back wall than Trace A. Therefore, it cannot be determined which part of the emission reduction in Figure 8.2(b) is obtained from the closer placement and which part from the parallel placement of Trace B to the enclosure wall. Therefore, Figure 8.3 depicts the comparison with a Trace B parallel to the enclosure wall at the maximum distance of Trace A from that wall. The result of the comparison in Figure 8.3(b) shows that 10dB of the 20dB in Figure 8.2(b) reduction can be assigned to the parallel placement and 10dB to the closer placement.



(a) Routing of Trace A and Trace B.



(b) Overall radiated power from the enclosure slot.

Figure 8.3: The trace width is 0.2mm, the trace height above the ground plane is 0.65mm. A 10mV voltage source with an impedance equal to the characteristic impedance of the trace Z_w drives the trace which is terminated with a 10pF capacitance.

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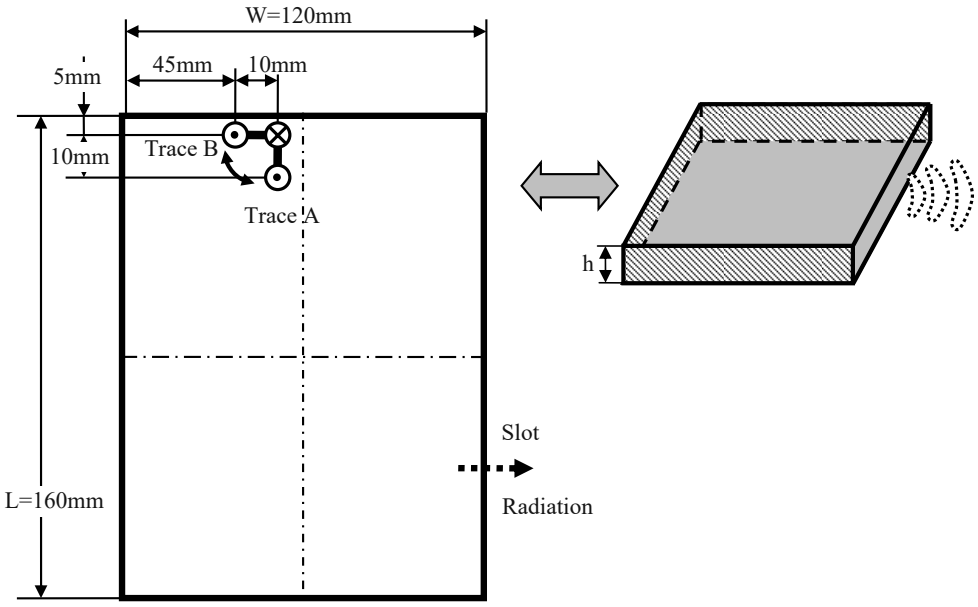
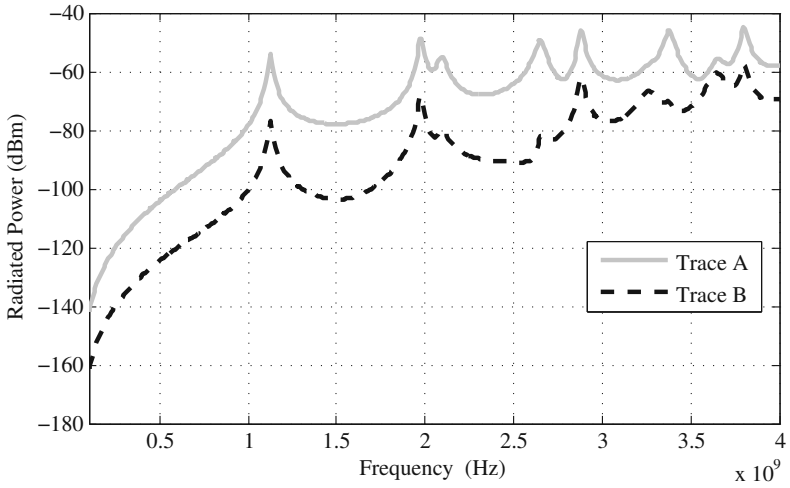
The same emission reduction of 20dB is also observed in Figure 8.4, when the Trace B is arranged closer and parallel to a side wall of the enclosure.



(a) Routing of Trace A and Trace B.



(b) Overall radiated power from the enclosure slot.

Figure 8.4: The trace width is 0.2mm, the trace height above the ground plane is 0.65mm. A 10mV voltage source with an impedance equal to the characteristic impedance of the trace Z_w drives the trace which is terminated with a 10pF capacitance.

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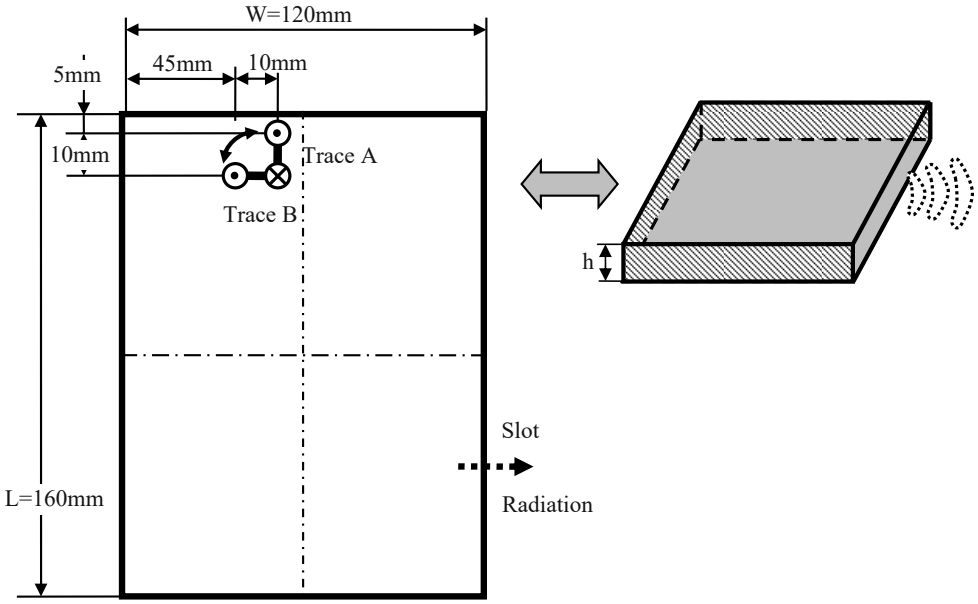
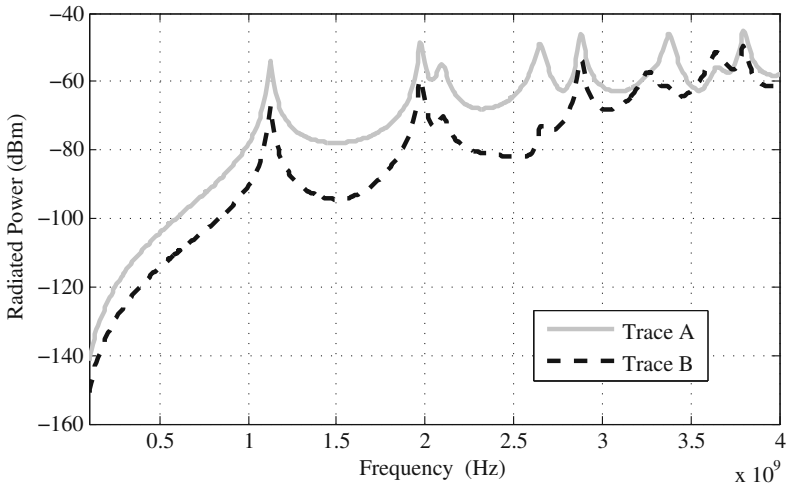
A comparison with a Trace B parallel to the enclosure wall at the maximum distance of Trace A from that wall in Figure 8.5 shows a similar result as for the back wall. Nearly 10dB emission reduction is achieved with a closer placement of the trace to the enclosure wall and 10dB reduction results from the orientation of the trace parallel to the wall.



(a) Routing of Trace A and Trace B.



(b) Overall radiated power from the enclosure slot.

Figure 8.5: The trace width is 0.2mm, the trace height above the ground plane is 0.65mm. A 10mV voltage source with an impedance equal to the characteristic impedance of the trace Z_w drives the trace which is terminated with a 10pF capacitance.

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The design rule is generalized to fairly arbitrary shaped, and even electrically large metallic enclosures as follows. The field inside a metallic enclosure can generally be described by an eigenfunction superposition. Since the eigenfunctions can be obtained from a homogenous solution of the Maxwell equations, the following investigation of the field close to a metallic enclosure wall is carried out from the homogenous Maxwell equations. A smooth metallic enclosure surface can be approximated locally by the tangential plane. The fields close to a metallic plane are expressed in a coordinate system with one coordinate direction normal (index $\perp$) to the plane and two coordinate directions parallel (index $\parallel$) to the plane. The electric field, the magnetic field, and the vector operator $\vec{\nabla}$ are expressed within this coordinate system. With

$$\vec{E} = \vec{E}_\parallel + \vec{e}_\perp E_\perp, \quad \vec{H} = \vec{H}_\parallel + \vec{e}_\perp H_\perp, \quad \text{and} \quad \vec{\nabla} = \vec{\nabla}_\parallel + \vec{e}_\perp \partial_\perp, \tag{8.1}$$

the Maxwell curl equations for the electric field become

$$\partial_\perp \vec{E}_\parallel - j\omega\mu\vec{e}_\perp \times \vec{H}_\parallel = \vec{\nabla}_\parallel E_\perp, \quad \vec{\nabla} \times \vec{E}_\parallel = -j\omega\mu H_\perp \vec{e}_\perp, \tag{8.2}$$

and the Maxwell curl equations for the magnetic field become

$$\partial_\perp \vec{H}_\parallel + j\omega\epsilon\vec{e}_\perp \times \vec{E}_\parallel = \vec{\nabla}_\parallel H_\perp, \quad \vec{\nabla} \times \vec{H}_\parallel = j\omega\epsilon E_\perp \vec{e}_\perp. \tag{8.3}$$

From the Maxwell divergence equations

$$\vec{\nabla}\vec{E} = 0, \quad \vec{\nabla}\vec{H} = 0, \tag{8.4}$$

follows

$$\vec{\nabla}_\parallel \vec{E}_\parallel = -\partial_\perp E_\perp, \quad \vec{\nabla}_\parallel \vec{H}_\parallel = -\partial_\perp H_\perp. \tag{8.5}$$

With consideration of the PEC boundary at the metallic plane

$$\vec{E}_\parallel = \vec{0}, \quad H_\perp = 0, \tag{8.6}$$

and (8.2) follows

$$\partial_\perp \vec{H}_\parallel = \vec{0}. \tag{8.7}$$

Considering

$$\vec{\nabla}_\parallel(\vec{\nabla}_\parallel \vec{E}_\parallel) = -\vec{\nabla}_\parallel(\partial_\perp E_\perp) \tag{8.8}$$

from (8.5), the normal derivative of (8.2) becomes

$$\partial_\perp(\partial_\perp \vec{E}_\parallel) = -\vec{\nabla}_\parallel(\vec{\nabla}_\parallel \vec{E}_\parallel) \tag{8.9}$$

Directly on the metallic plane $\vec{\nabla}_\parallel \vec{E}_\parallel$ vanishes, because $\vec{E}_\parallel = \vec{0}$ constant along the plane $\mathcal{C}$, and (8.9) becomes

$$\partial_\perp(\partial_\perp \vec{E}_\parallel) = \vec{0}\Big|_{\mathcal{C}}. \tag{8.10}$$

Thus, the normal derivative of the field component parallel to the metallic plane has a maximum at this plane $\mathcal{C}$, which is expressed by

$$\boxed{|\partial_\perp \vec{E}_\parallel| \rightarrow \text{ maximum}\Big|_{\mathcal{C}}}. \tag{8.11}$$

The tangential electric field vanishes at the metallic plane and the derivative of the field becomes a maximum. Consequently, a differential coupling to that field must reach a maximum, when a trace is oriented orthogonal to the wall, because the coupling of a differential source depends on the field derivative. Close to the walls, emission reduction reaches a maximum according to the vanishing tangential electric field. For the enclosure depicted in Figure 7.1, this also follows from the interpretation of (7.17).

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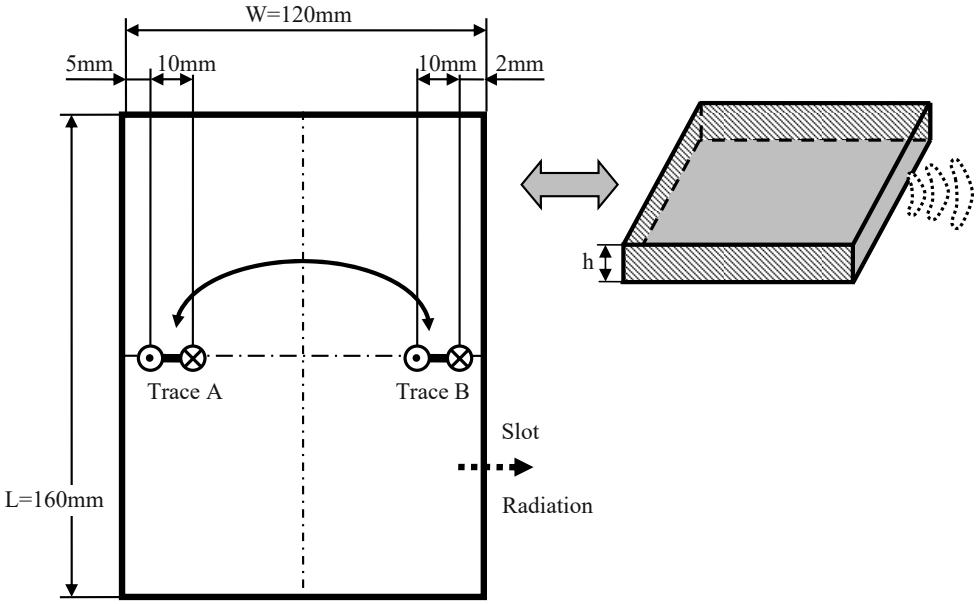
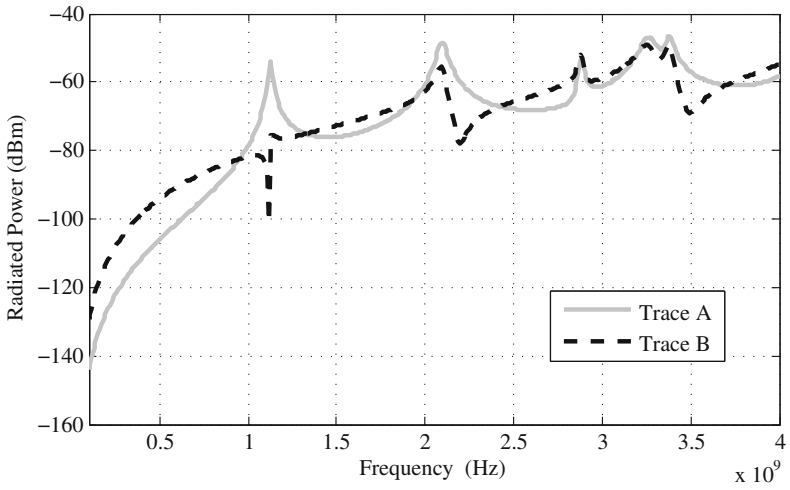
8.3. Rule 3: Trace placement in the middle of the enclosure slot reduces the EMI at the first resonance



(a) Routing of Trace A and Trace B.



(b) Overall radiated power from the enclosure slot.

Figure 8.6: The trace width is 0.2mm, the trace height above the ground plane is 0.65mm. A 10mV voltage source with an impedance equal to the characteristic impedance of the trace Z_w drives the trace which is terminated with a 10pF capacitance.

Figure 8.6 shows a reduction of the emission at several resonances of more than 20dB. However, the radiated emission is increased in the frequency range below the first resonance. Therefore such a trace placement should only be selected in the case of enough margin to the EMC compliance limit at low frequencies and a known EMI problem at the first resonance of the enclosure.

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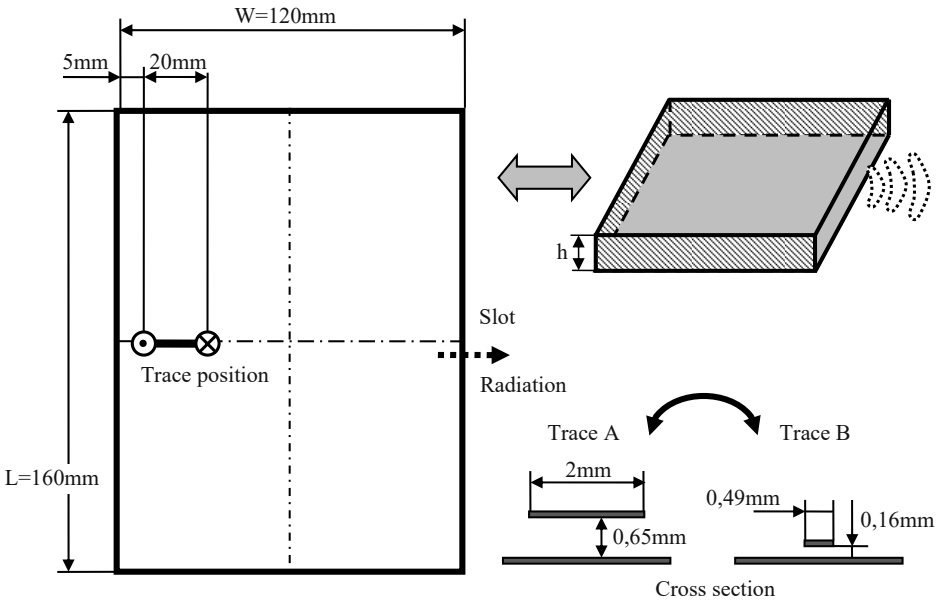
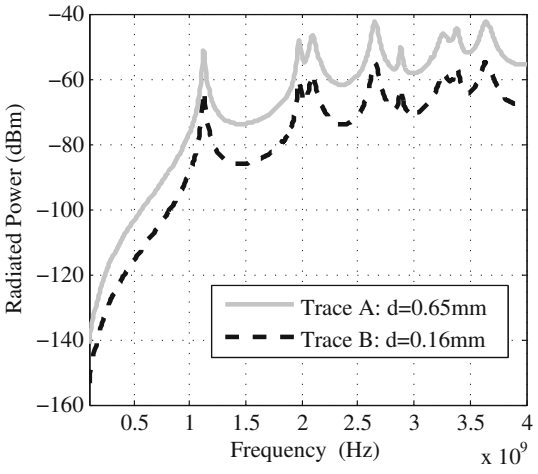
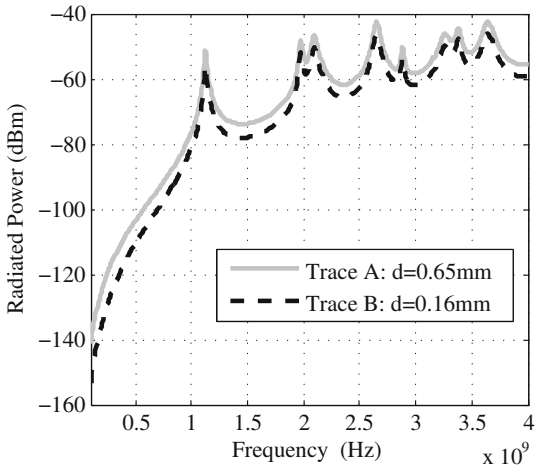
8.4. Rule 4: Reduction of the trace height d above the ground plane reduces EMI



(a) Routing of Trace A and Trace B.



(b) Radiated power. Width of Trace B: b=0.49mm.



(c) Radiated power. Width of Trace B: b=2mm.

Figure 8.7: A 10mV voltage source with an impedance equal to the characteristic impedance of the trace Z_w drives the trace which is terminated with a 10pF capacitance.

With reduction of the trace height above the PCB ground plane, the radiated emission is reduced in the whole frequency band by the factor

$$R_{21} = 20 \log \left(\frac{d_2}{d_1} \right), \tag{8.12}$$

where d_1 denotes the initial trace height above the ground plane and d_2 denotes the new, reduced trace height above the ground plane. This reduction can only be realized, when the trace width is also reduced, to conserve the characteristic impedance of the trace Z_w.

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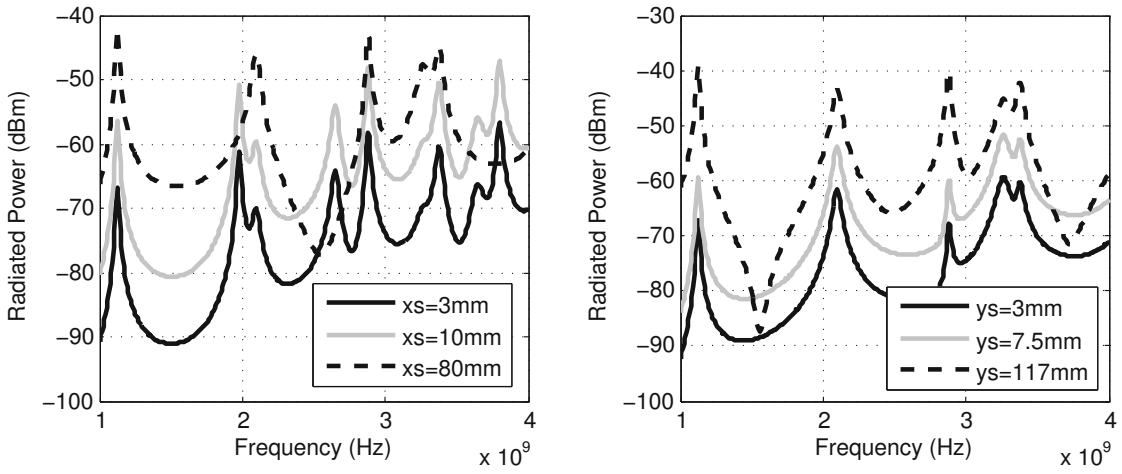
Figure 8.7(b) shows the emission reduction of about 12dB when the trace width is correctly reduced. A reduction of the trace height above the ground plane without reduction of the trace width leads to a reduction of Z_w through the increased capacitance. This will increase the trace currents, which almost compensates the emission reduction effect from the height reduction, as illustrated in Figure 8.7(c). The reduction of the trace height above the ground plane can be realized by using thinner dielectric layers for the PCB. A PCB layer thickness change has has an influence on every circuit net, which is routed on the copper layers around the changed dielectric layer. Thus, a dielectric layer thickness change must be carried out very carefully. A correct characteristic impedance of a trace, which matches the termination impedances is crucial for all high speed signal traces which are not electrically short, in order to avoid reflections and ensure signal integrity. Therefore, the design of these signal nets has to be checked and eventually adapted at any thickness change of PCB layers. The power distribution network on the PCB also has to be checked and eventually changed to ensure power integrity.

8.5. Rule 5: Single source placement closer to an enclosure wall reduces EMI

Placement of a source closer to a metallic wall reduces the radiated emission from that source. This design guideline can be generalized to arbitrary metallic enclosures with apertures, even when the enclosure is large compared to the wavelength in each dimension. The electric field vanishes tangential to the wall and thus it decreases approaching the wall. Therefore, the coupling of a source, which is parallel to the wall must be reduced, when the source is placed closer to that wall.



(a) Source variation in x-direction (y_s=60mm). (b) Source variation in y-direction (x_s=80mm).

Figure 8.8: Excitation of the enclosure with a single current of 10μA supplied directly to the planes at the position (x_s,y_s).

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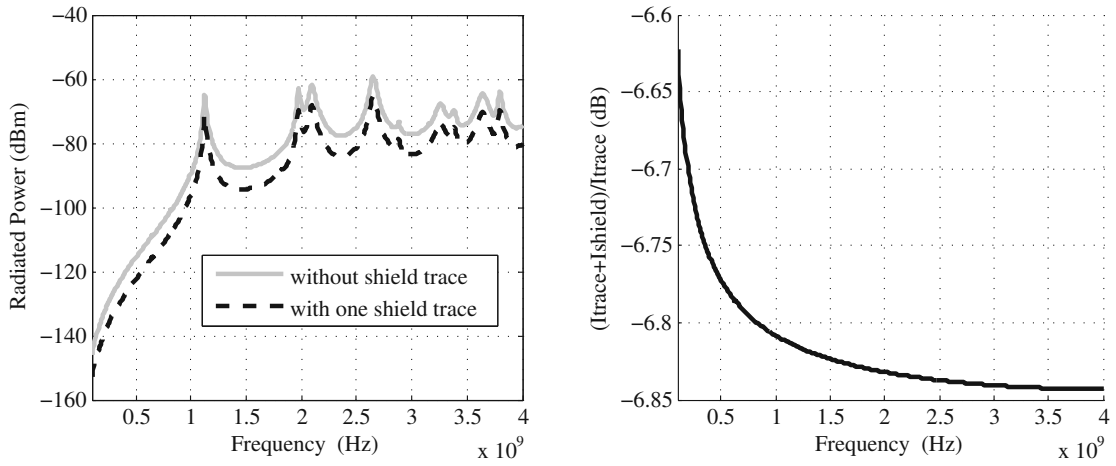
8.6. Rule 6: Shielding reduces the common mode coupling

Shielding of a critical trace with a second trace which is connected to the ground plane at the source and the load position of the shielded trace reduces the common mode coupling. The reduction is caused by the induced current on the shield, which flows in the opposite direction from the trace wire current and thus partially compensates the common mode coupling from the trace current to the enclosure field. The achievable emission reduction with shielding can be estimated from

$$Rs_{21} = 20\log\left|\frac{I_{trace} + I_{shield}}{I_{trace}}\right|, \tag{8.13}$$

where I_{trace} denotes the current on the critical trace and I_{shield} denotes the current on the shield. According to the same flow direction definition of both currents I_{trace} and I_{shield}, there is a positive sign in the nominator of (8.13). The following Figures 8.9, 8.10, and 8.11 show radiated emission reductions achieved by the shielding of traces with different dimensions. A 10mV voltage source with an impedance equal to the characteristic impedance of the trace Z_w drives the trace and the trace is terminated with a 10pF capacitance. The trace is routed straight from $(x_s = 50mm, y_s = 20mm)$ to $(x_s = 50mm, y_s = 30mm)$. The trace supply, termination, and routing is kept equal to this definition for all examples. Figure 8.9 indicates an emitted power reduction of about 6dB from one shield, parallel to a trace with 0.2mm width, 0,65mm above the ground plane. A second shield wire on the other side of the trace leads to an emission reduction of about 13dB, as depicted in Figure 8.10. However, the current magnitude difference of the shield current and the critical trace current increases with increasing trace width and with decreasing trace height above the ground plane. Thus, Figure 8.11 shows an emitted power reduction of only 2dB from one shield, parallel to a trace with 2mm width, 0,65mm above the ground plane.



(a) Radiated power.

(b) Estimated reduction from 8.13 .

Figure 8.9: Comparison of the radiated emission without and with one 0.2mm shield trace (width=0.2mm, height above the ground plane=0.65mm) parallel to the trace with a distance of 0.2mm and terminated to ground.

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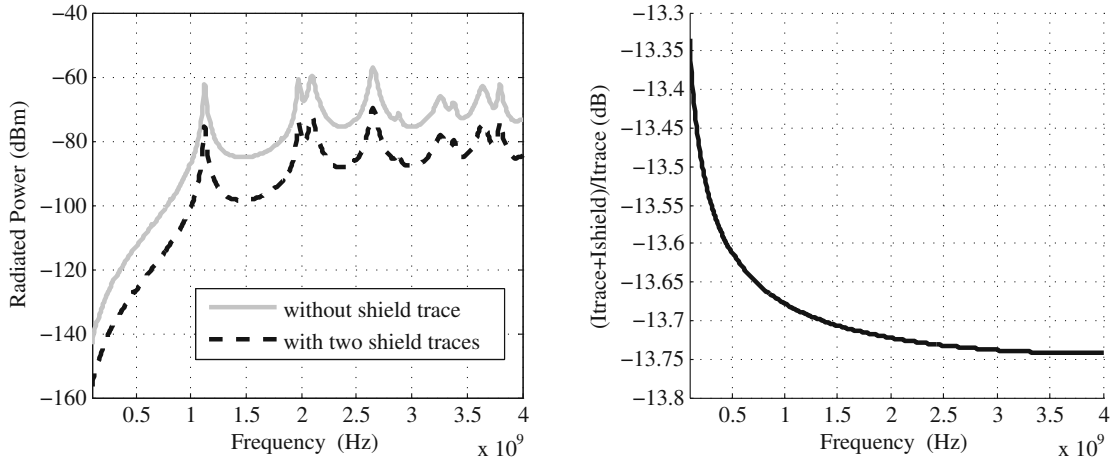
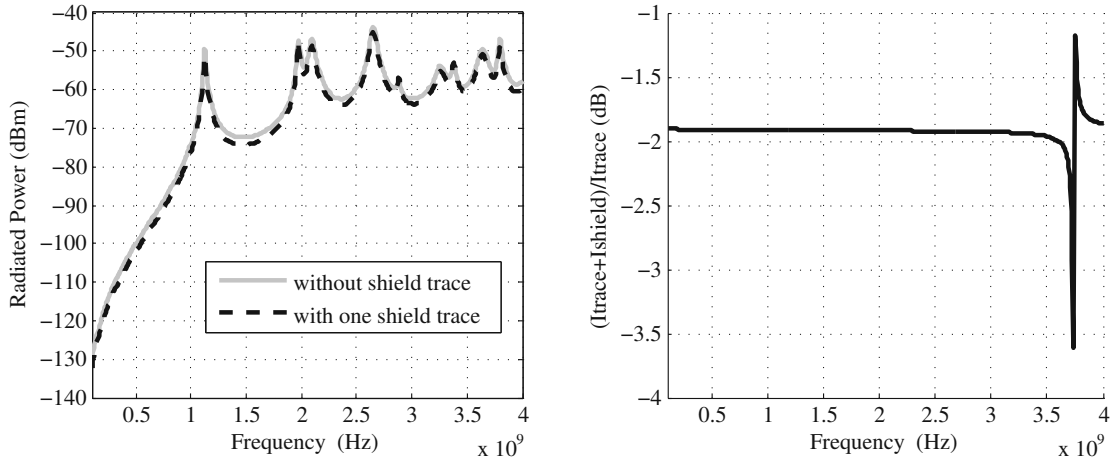


(a) Radiated power. (b) Estimated reduction from 8.13 .

Figure 8.10: Comparison of the radiated emission without and with 0.2mm shields parallel on both sides of the trace (width=0.2mm, height above the ground plane=0.65mm) at a distance of 0.2mm and terminated to ground.



(a) Radiated power. (b) Estimated reduction from 8.13 .

Figure 8.11: Comparison of the radiated emission without and with one 0.2mm shield trace parallel to the trace (width=2mm, height above the ground plane=0.65mm) with a distance of 0.2mm and terminated to ground.

Therefore, coplanar shielding provides only reasonable common mode emission reduction for traces, of which the length-capacitance to ground is strongly influenced by the shield traces. This is only the case for traces with low trace width and large distance from the ground plane. Routing of a trace between two ground planes provides an opportunity for emission reduction, as well as of wide traces. However, each interconnect between two components must have vertical sections which leave the PCB to enable the connection of these components. These vertical interconnects cause common mode coupling which is not reduced by the shield on the PCB. Therefore, interconnects routed between two ground layers and coplanar shielded on the PCB cannot completely eliminate the common mode coupling.

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8.7. Rule 7: A ground plane under an IC reduces EMI

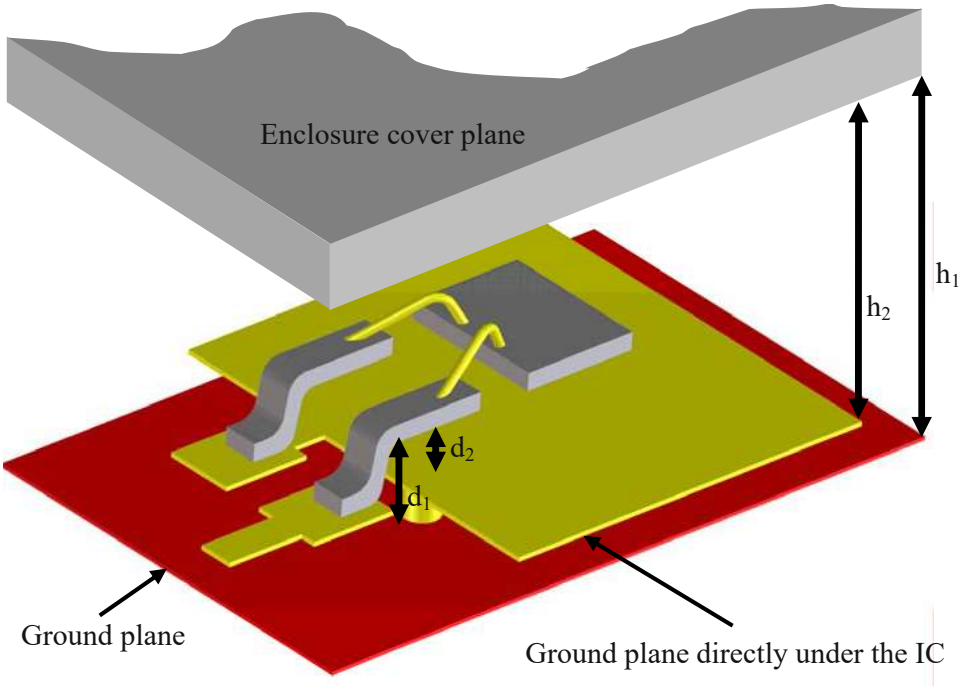

Figure 8.12: A ground plane directly under the IC reduces the height of the IC current loop above ground from d_1 to d_2. This also reduces the h_1 to h_2.

The coupling to the enclosure field is reduced by

$$Ric_{12} = 20 \log \left(\frac{d_2/h_2}{d_1/h_1} \right) \tag{8.14}$$

With $d_2 < d_1 \ll h_2 < h_1$ and $\Delta d = d_1 - d_2$ the coupling reduction becomes

$$Ric_{12} \approx 20 \log \left(1 - \frac{\Delta d}{d_1} \right) \tag{8.15}$$

Table 8.1 contains some examples for the achieved common mode coupling reduction with a ground plane directly under the IC. High reduction can be obtained for IC packages with low seating heights and for PCBs with only one inner layer ground plane which has a significant distance from the component layers.

IC package loop height	Δd	Coupling reduction
mm	mm	dB
0.80	0.4	-3.5
0.80	1.6	-9.5
1.00	0.4	-2.9
1.00	1.6	-8.3
1.20	0.4	-2.5
1.20	1.6	-7.4

Table 8.1: Common mode coupling reduction from a ground plane under the IC.

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8.8. Summary of the design guidelines

➢ **Rule 1: Trace placement symmetric to the enclosure symmetry reduces the coupling up to the second enclosure resonance**

- ⇨ The trace source and load positions are symmetric to the enclosure symmetry.
- ⇨ The guideline must be considered at component placement on the PCB.
- ⇨ The load dependent emission reduction is greater than 20dB compared to a trace, parallel to the enclosure symmetry line. Example in Figure 8.1.

➢ **Rule 2: Trace placement parallel and close to metallic enclosure walls reduces EMI, trace placement orthogonal and close to enclosure walls increases EMI**

- ⇨ The guideline must be considered at component placement on the PCB.
- ⇨ The load dependent emission reduction is greater than 20dB compared to a trace, normal to the enclosure wall. Example in Figure 8.2.
- ⇨ Emission reduction from the closer placement is about 10dB (Figure 8.3).
- ⇨ Emission reduction from the parallel orientation is about 10dB (Figure 8.3).

➢ **Rule 3: Trace placement in the middle of the enclosure slot reduces the EMI at the first resonance**

- ⇨ The guideline must be considered at component placement on the PCB.
- ⇨ The load dependent emission reduction is typically greater than 20dB compared with a different trace placement. Example in Figure 8.6.
- ⇨ The emission below the first resonance is higher.

➢ **Rule 4: Reduction of the trace height d above the ground plane reduces EMI**

- ⇨ Realizable with thin dielectric layers on the PCB and thin IC packages.
- ⇨ A trace width reduction must be carried out, when the dielectric layer thickness of the PCB is changed to conserve the characteristic impedance of the traces.
- ⇨ Check the power distribution impedances and transfer parameters.
- ⇨ Broad band EMI reduction estimation: $R_{21} = 20\log(d_2/d_1)$

➢ **Rule 5: Single source placement closer to an enclosure wall reduces EMI**

- ⇨ The guideline must be considered at component placement on the PCB.
- ⇨ A first order estimation of the emission reduction that is correct close to the wall gives $R_{21} = 20\log(a_2/a_1)$, where a_1 is the initial distance from the source to the wall and a_2 is the new, reduced distance.

➢ **Rule 6: Shielding reduces the common mode coupling**

- ⇨ EMI reduction for coplanar shielding: $Rs_{21} = 20\log|(I_{trace} + I_{shield})/I_{trace}|$.
- ⇨ PCB shielding cannot reduce the coupling from the vertical interconnects to ICs.
- ⇨ Coplanar shielding is efficient for narrow traces, high above the ground plane.

➢ **Rule 7: A ground plane under an IC reduces EMI**

- ⇨ EMI reduction according to the obtained d/h reduction ⇒ **Rule 4**.
- ⇨ Vias must connect this ground with the global PCB ground plane, at least close to fast signal IC pads.

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Appendices

A. Validation of the analytic common-mode coupling factor d/h

This appendix contains an empirical validation of the analytical coupling factor with HFSS® simulations. Each figure depicts a comparison of two HFSS® simulation results. One of these two simulations was performed with ports between the parallel planes, the other simulation, with a trace. The transfer impedance from the source at the trace to the ports at the slot of the enclosure is obtained directly from the HFSS® model with the trace. For the comparison the transfer impedance is obtained by application of the trace introduction method using equations (5.6), (5.9) and the impedance matrix from the HFSS® simulation with the ports between the enclosure cover and bottom. Section 5.3 contains a more detailed description of the validation procedure.

A.1. Variation of the trace position

A variation of trace position on the enclosure bottom plane (ground plane) is carried out for a 5mm trace with 0.65mm height above the ground plane.

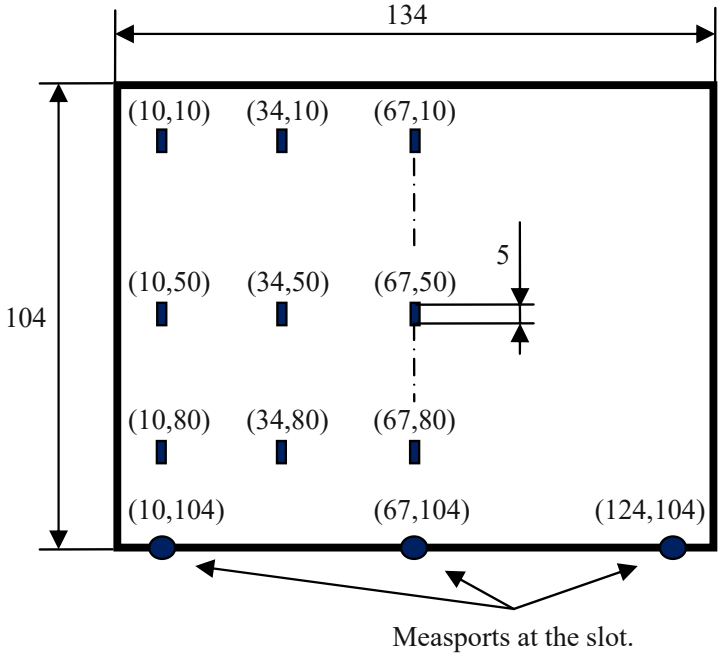

Figure A.1: Trace positions used for the transfer impedance comparison. Value dimensions in millimeters. The enclosure height is 7mm, the trace height above ground is 0.65mm and trace width is 2mm

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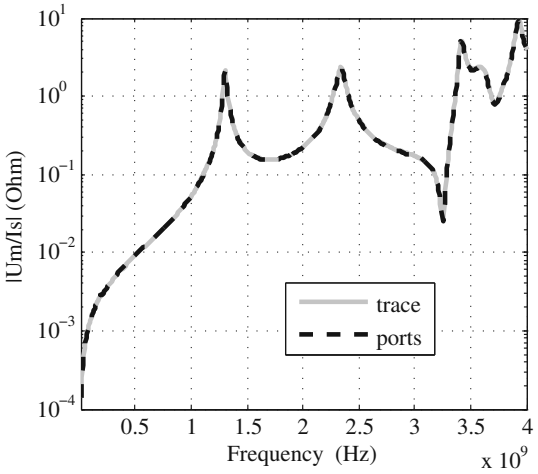
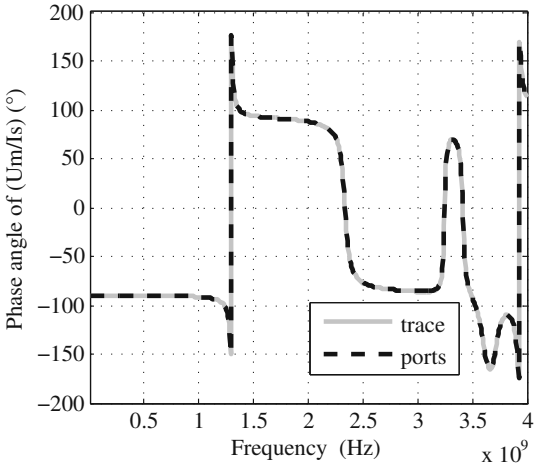
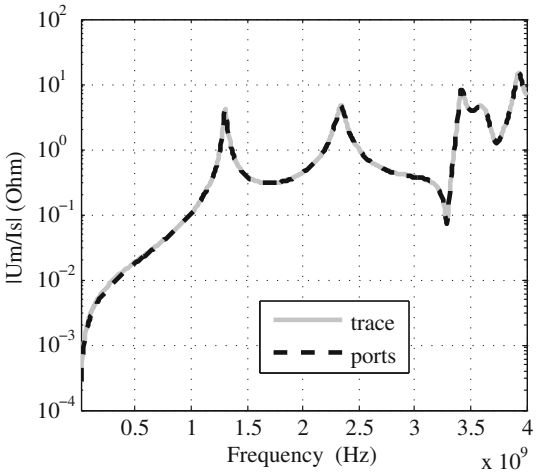


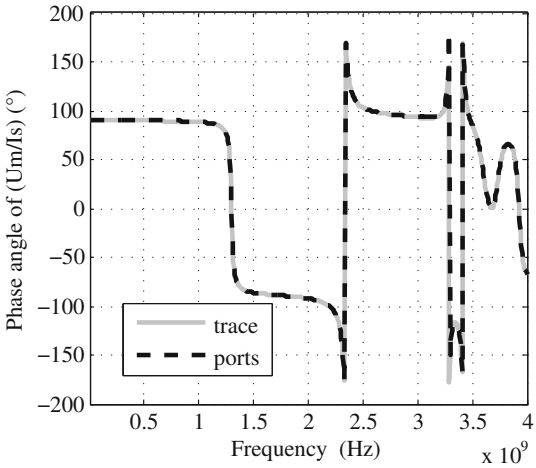
(a) Load: 0 Ohm, magnitude.



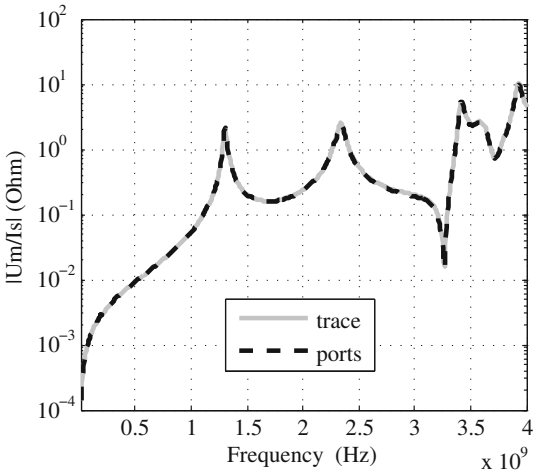
(b) Load: 0 Ohm, phase angle.



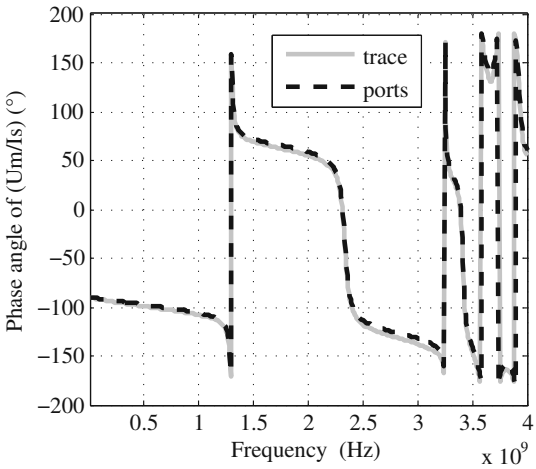
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.2: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (10mm,10mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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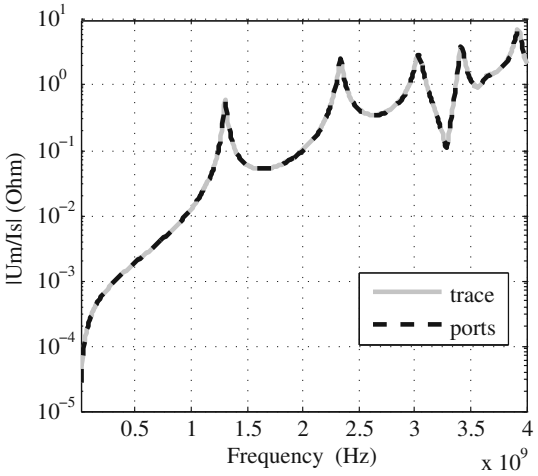

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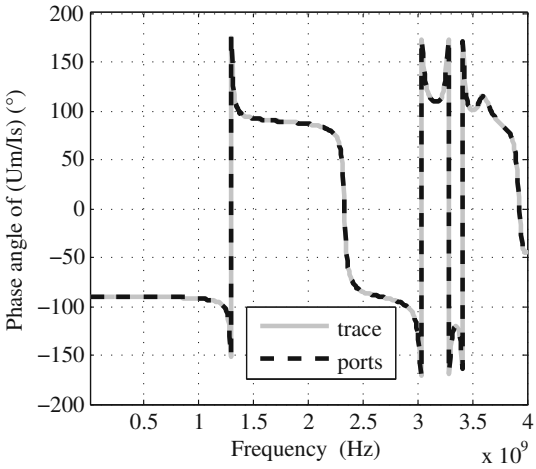
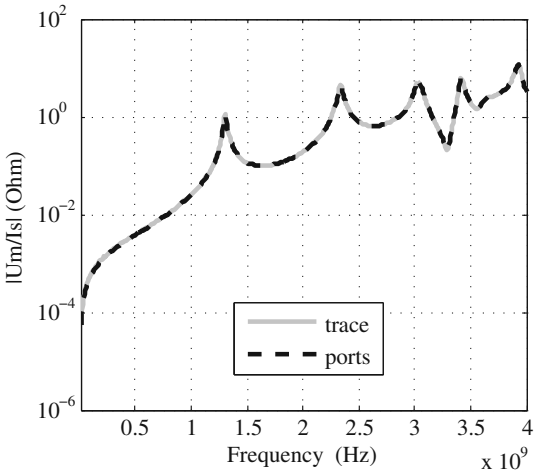
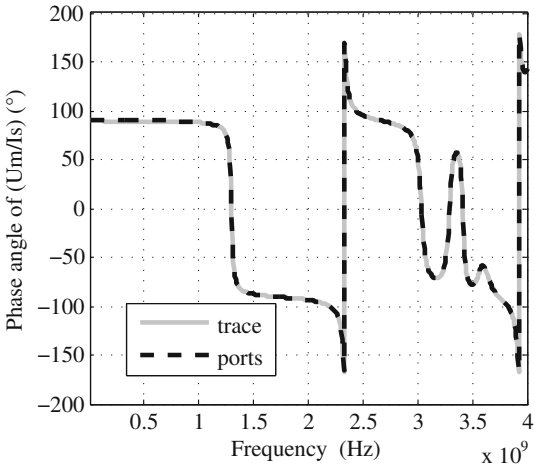


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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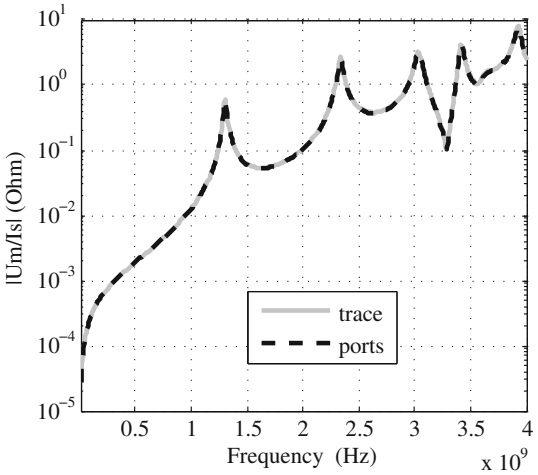
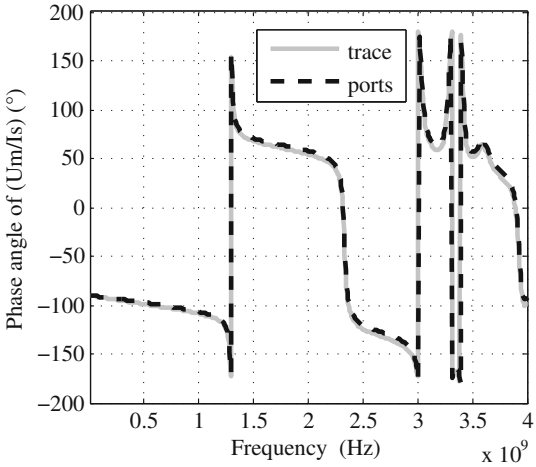


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.3: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). The trace is located at position (10mm,10mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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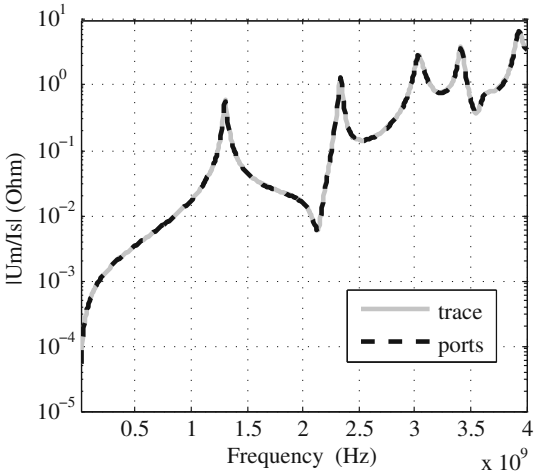

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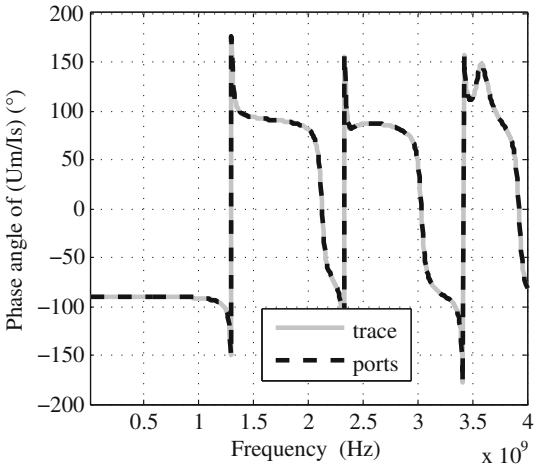
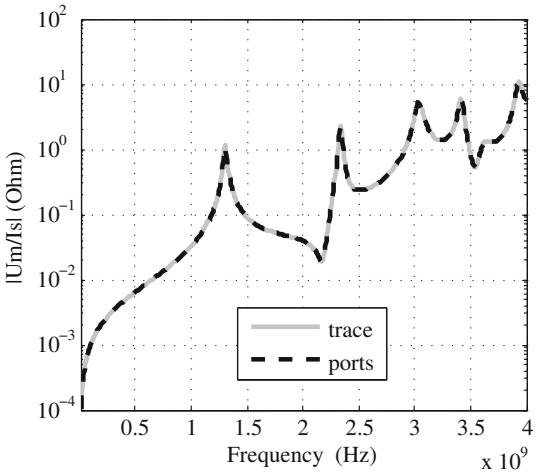
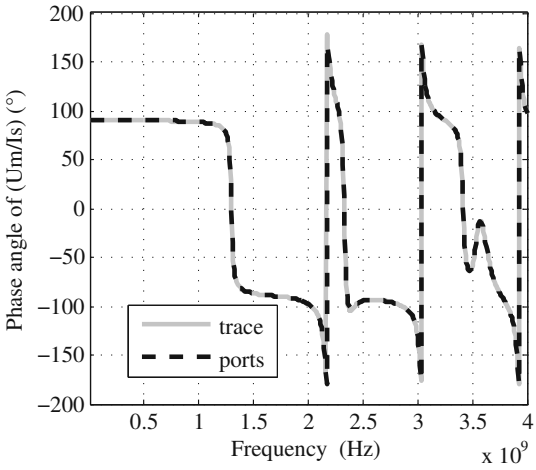


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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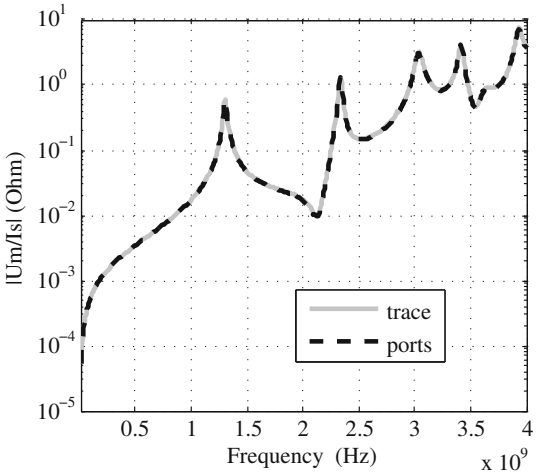
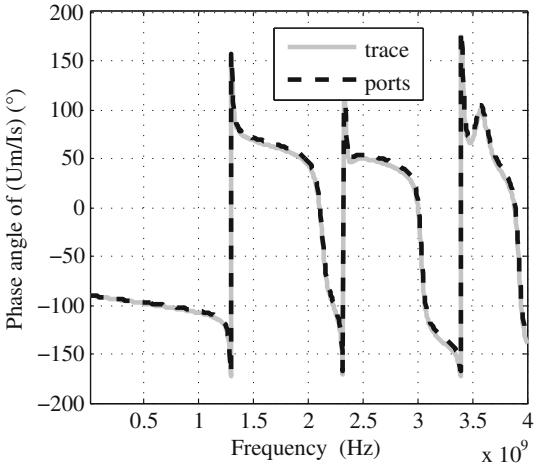


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.4: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). The trace is located at position (10mm,10mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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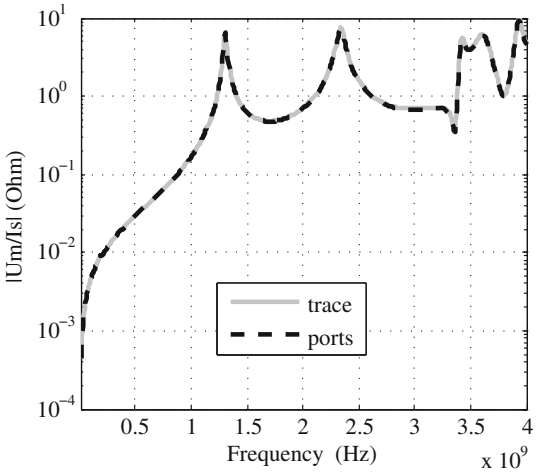

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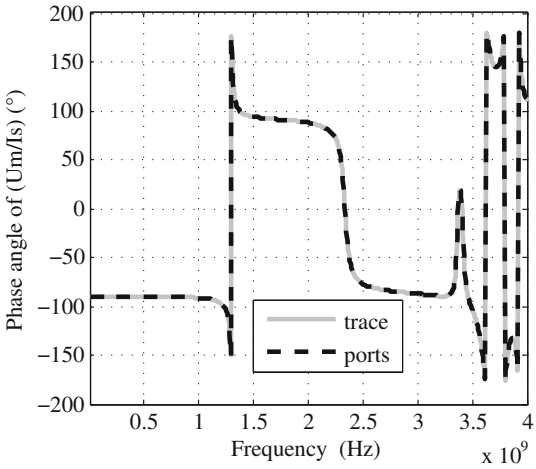
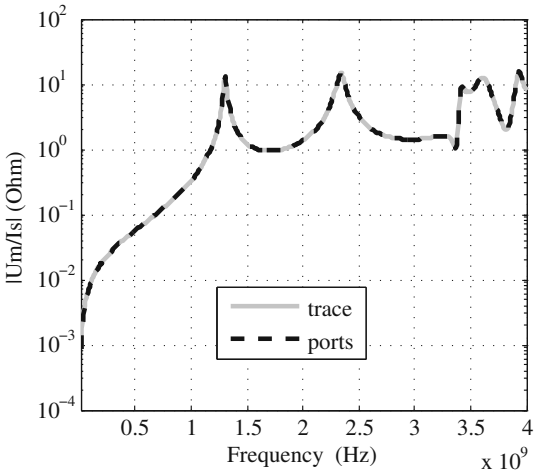
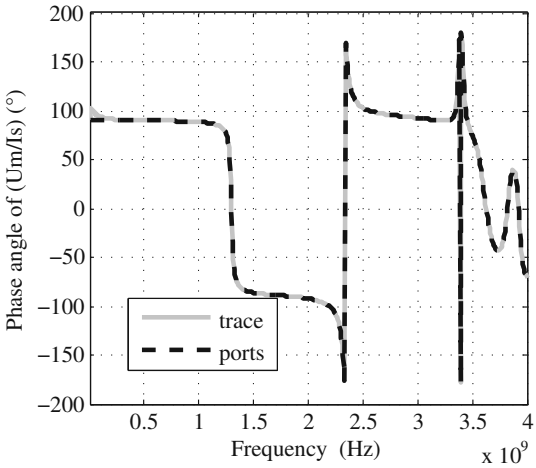


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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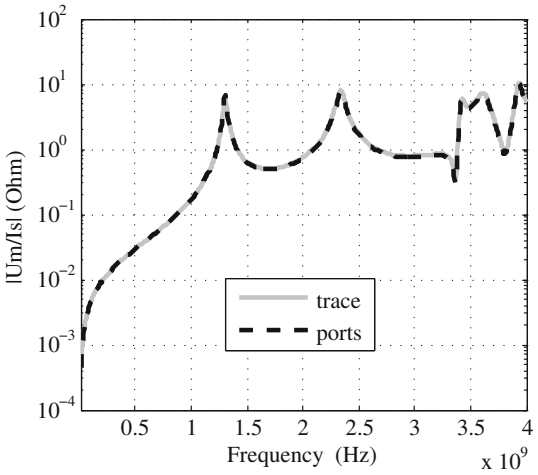
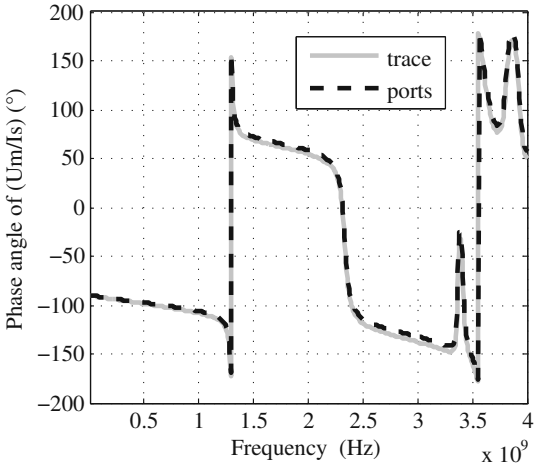


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.5: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (35mm,10mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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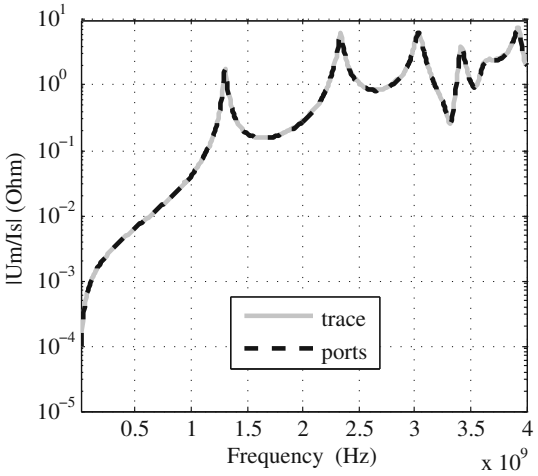

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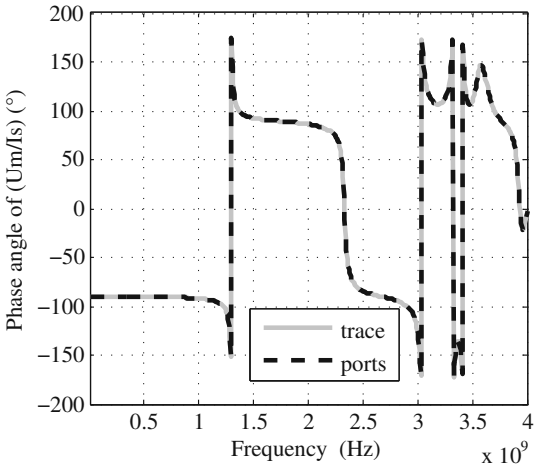
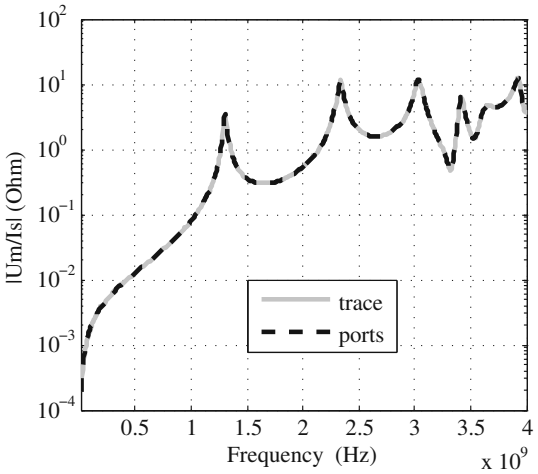
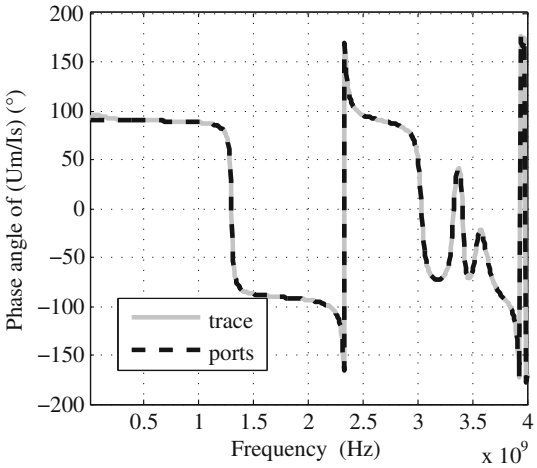


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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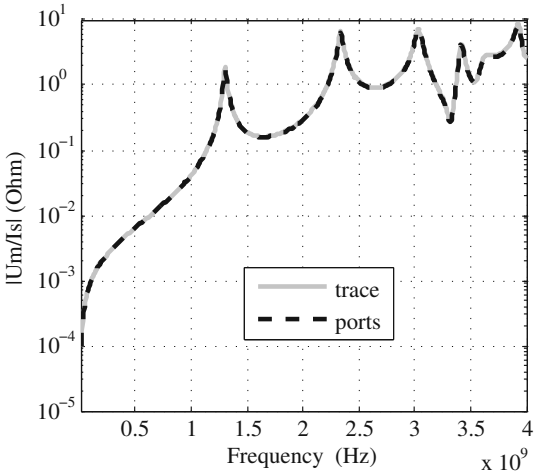
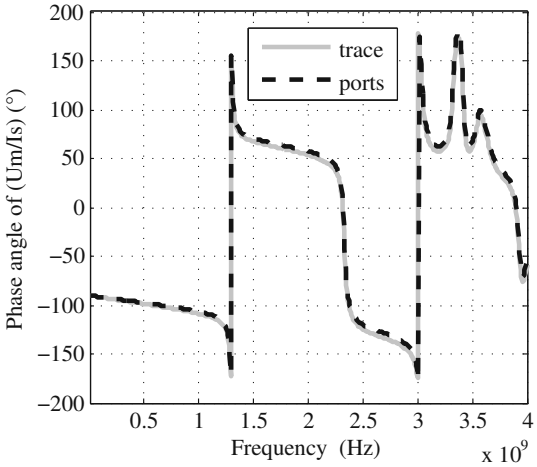


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.6: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). The trace is located at position (35mm,10mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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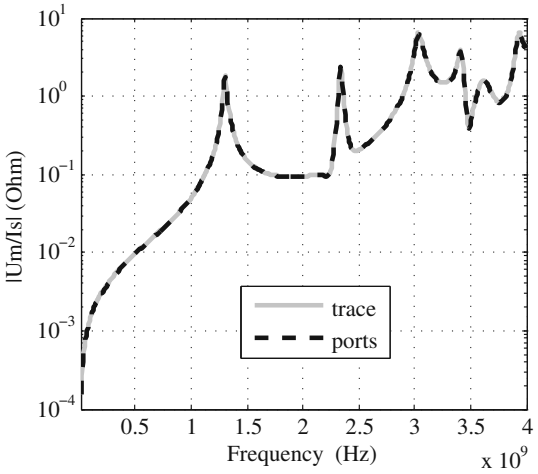

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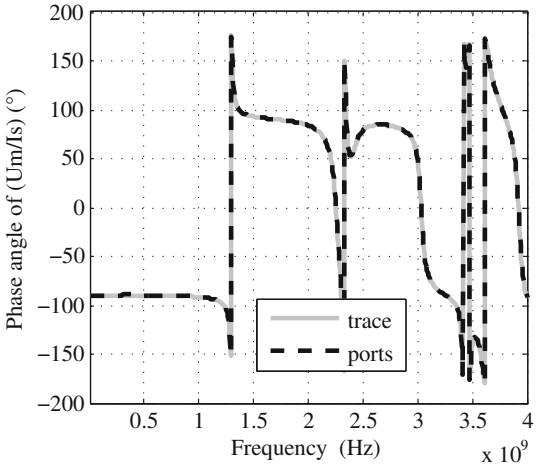

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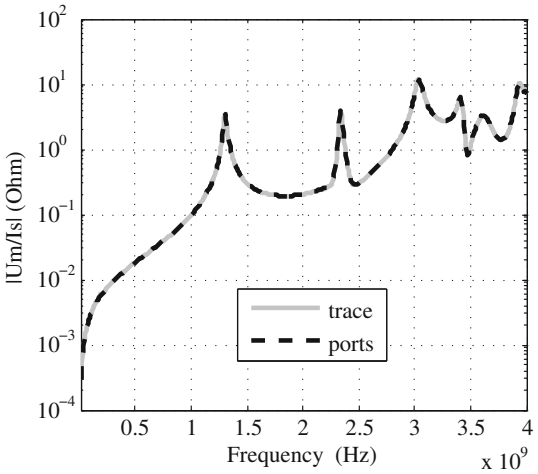
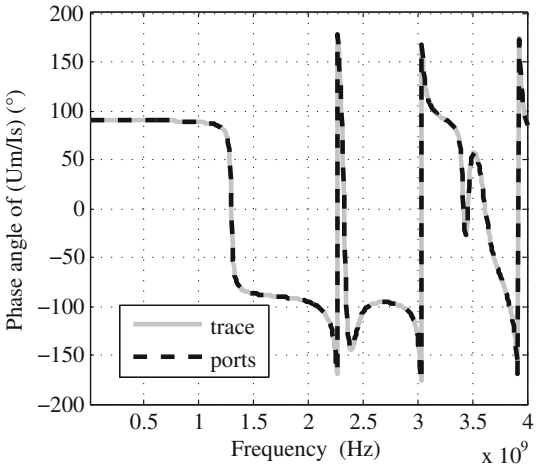


(c) Load: 1e9 Ohm, magnitude.



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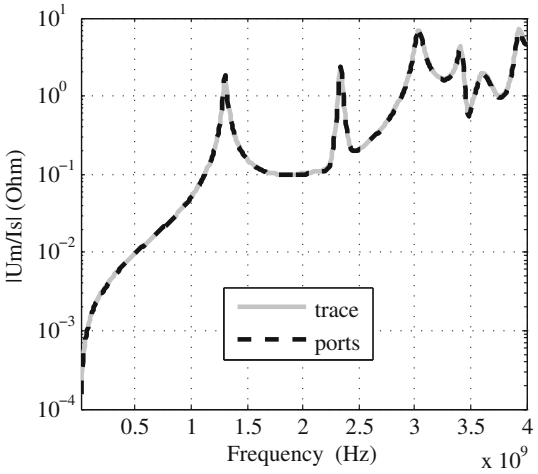
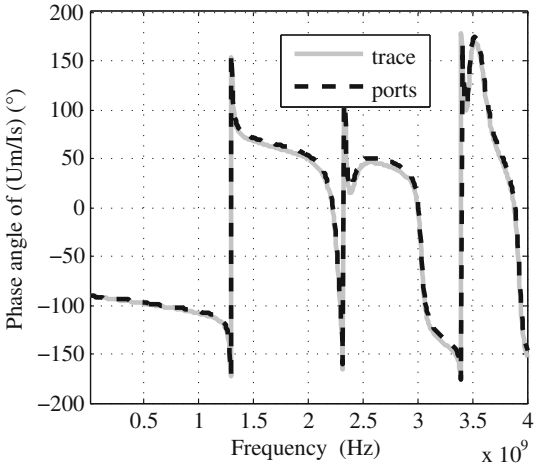


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.7: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). The trace is located at position (35mm,10mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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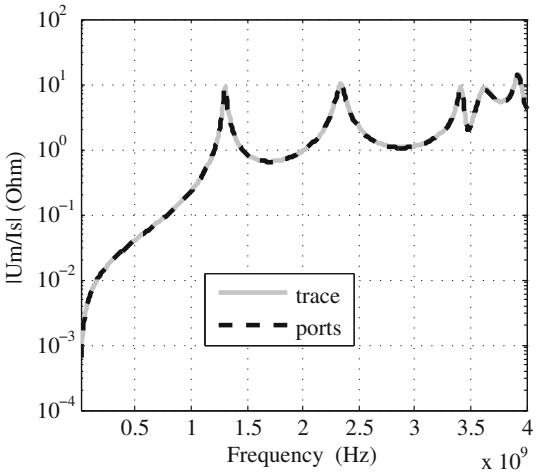

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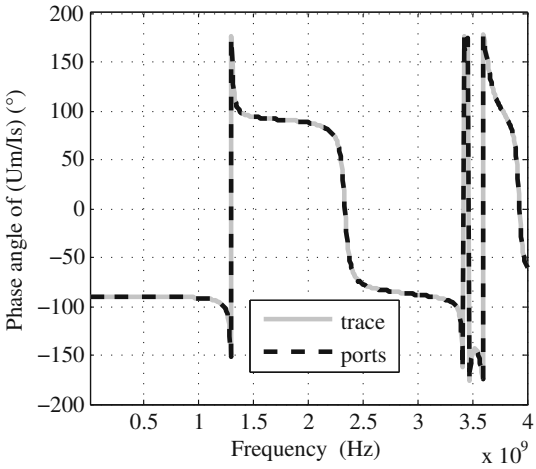
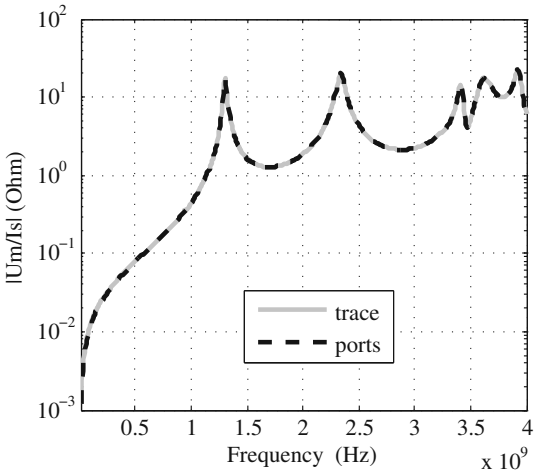
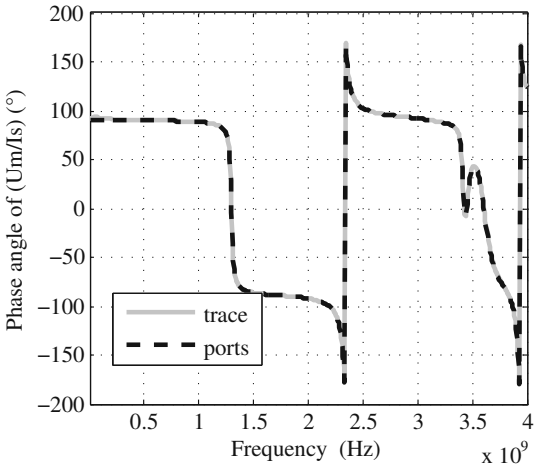


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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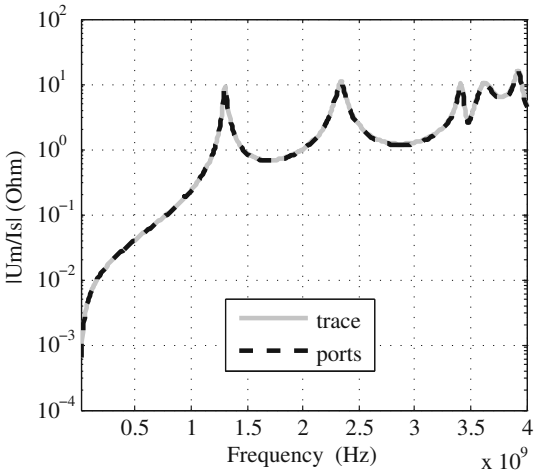
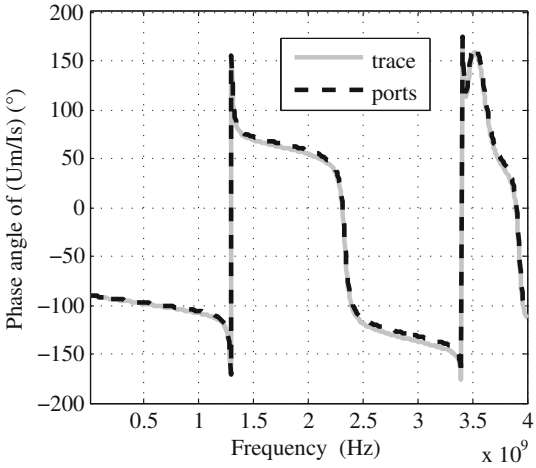


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.8: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (67mm,10mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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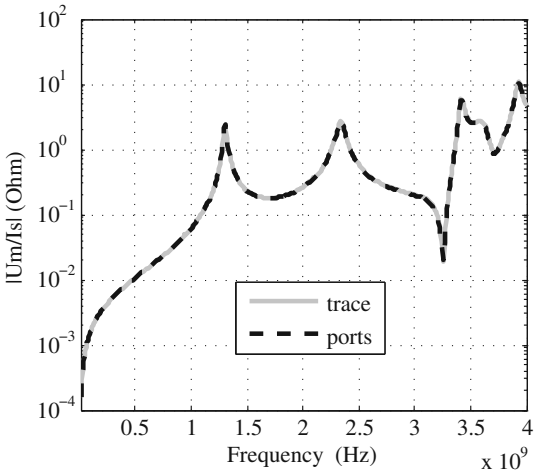

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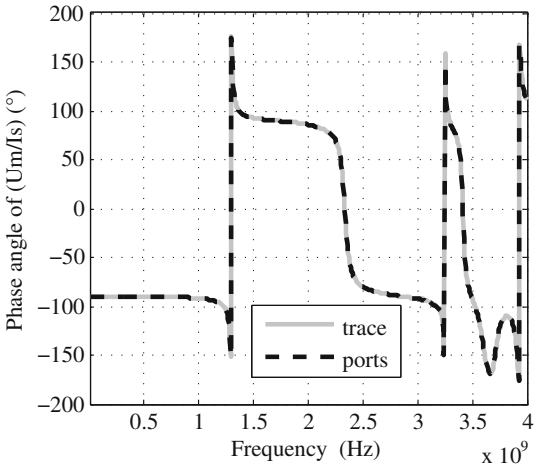

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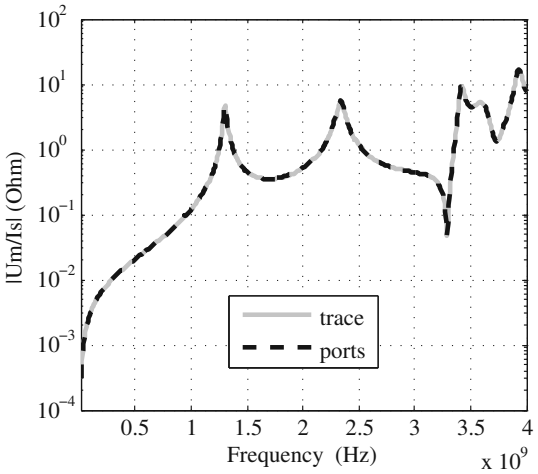
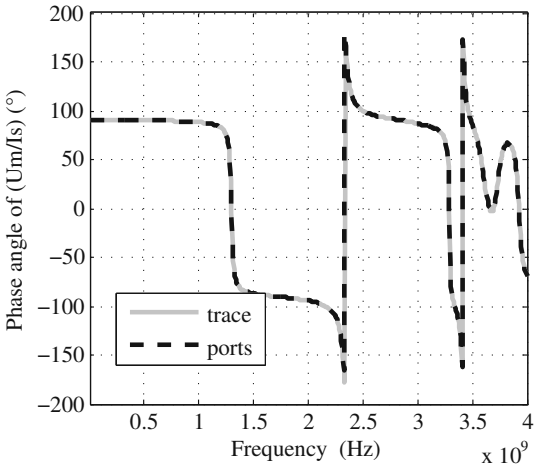


(c) Load: 1e9 Ohm, magnitude.



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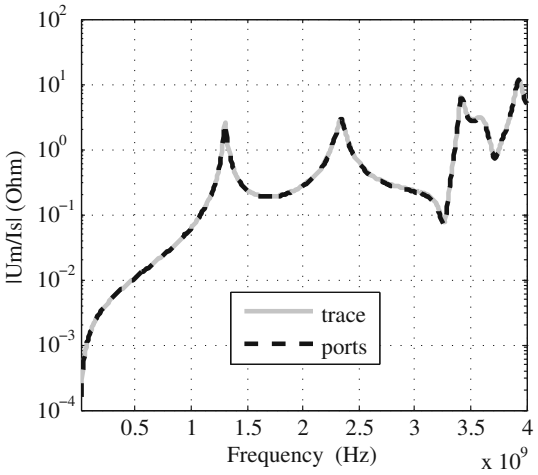
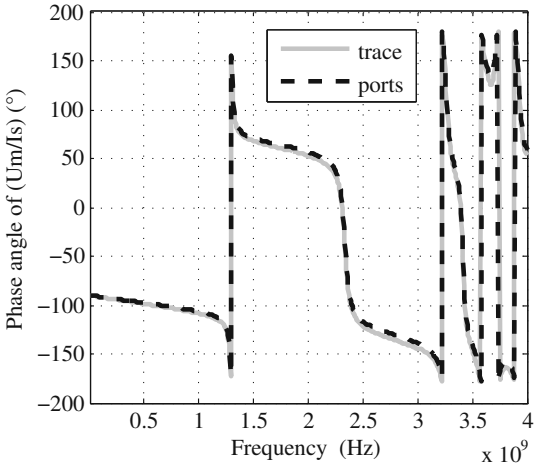


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.9: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). The trace is located at position (67mm,10mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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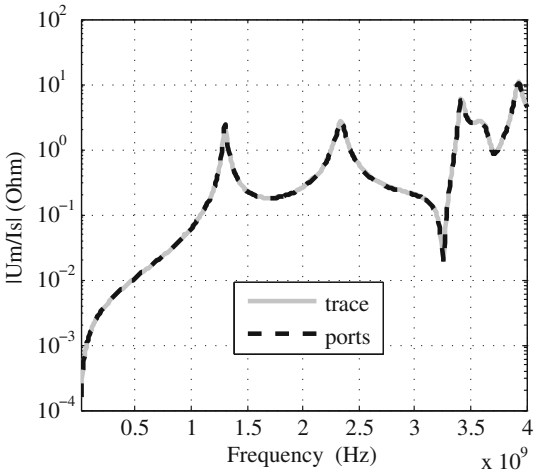

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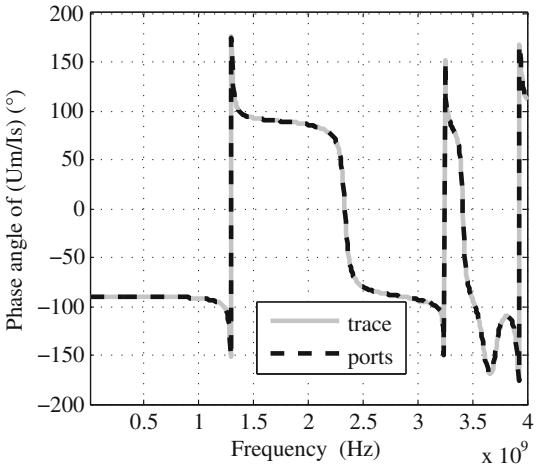

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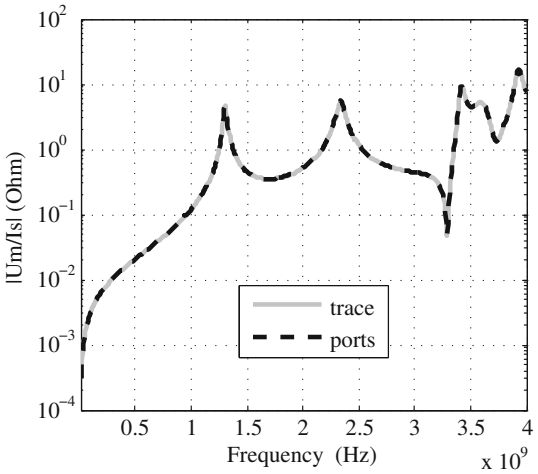
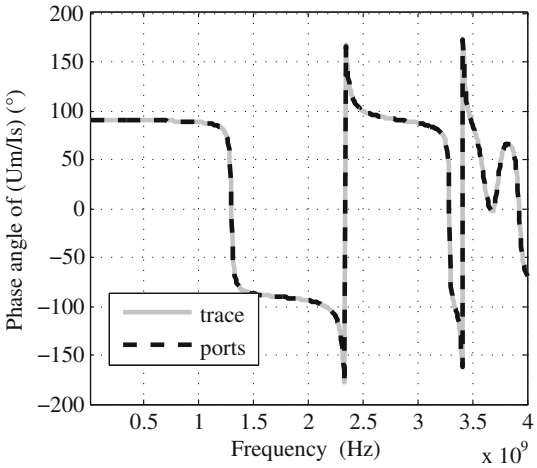
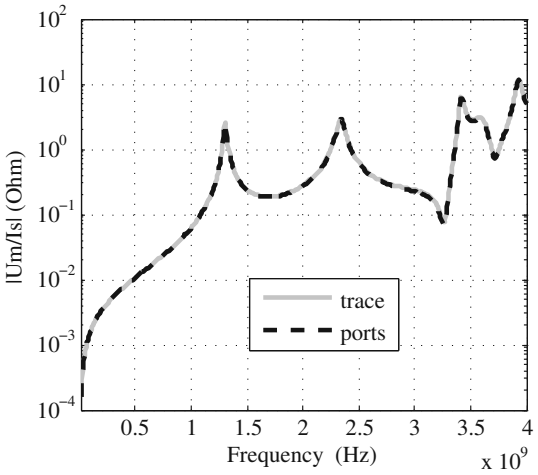


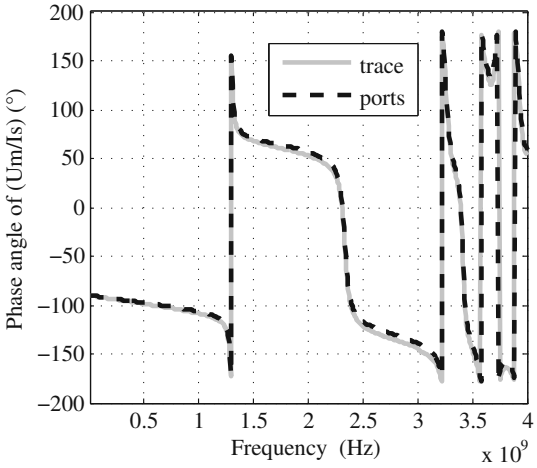
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.10: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). The trace is located at position (67mm,10mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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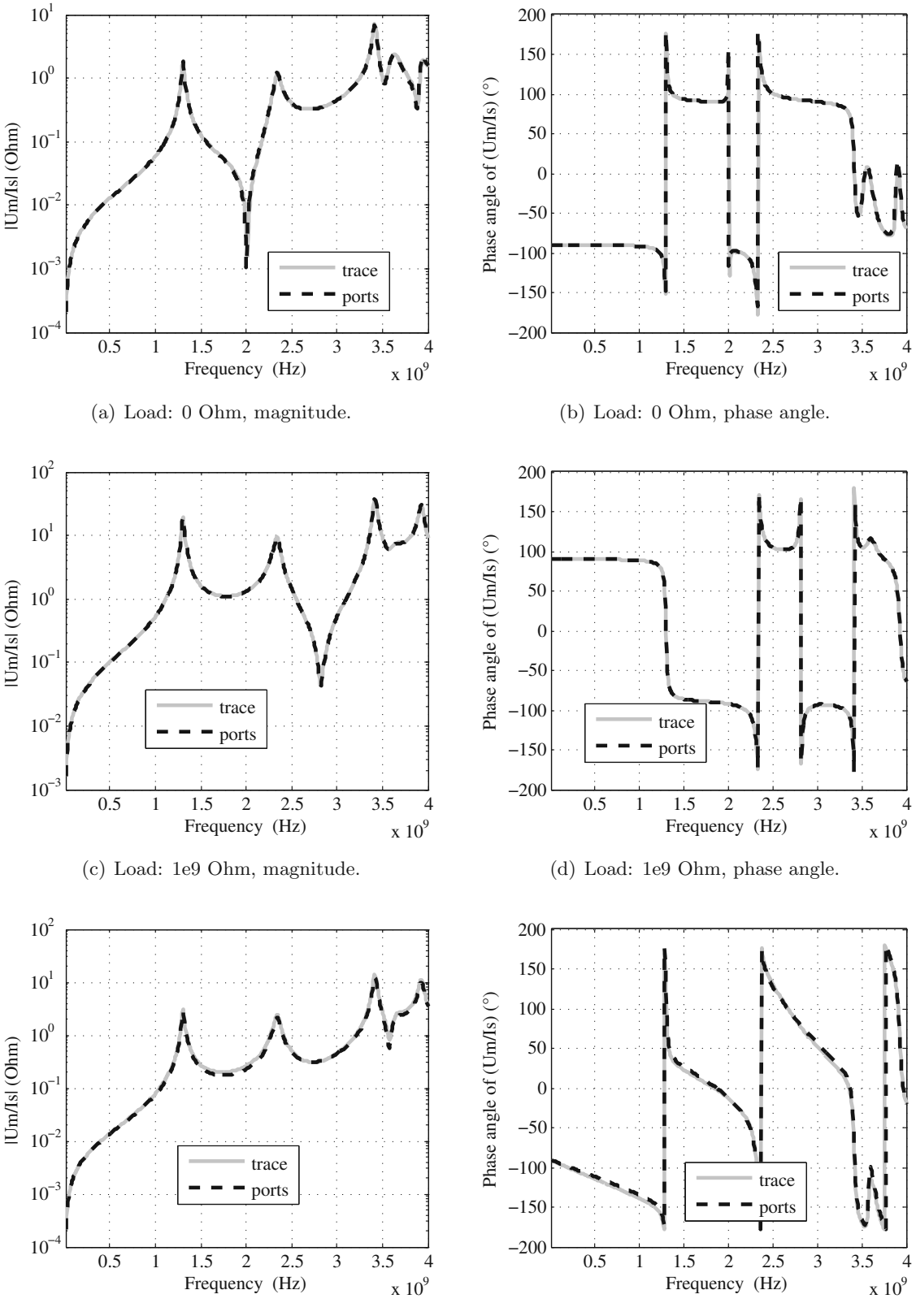

(a) Load: 0 Ohm, magnitude.

(b) Load: 0 Ohm, phase angle.

(c) Load: 1e9 Ohm, magnitude.

(d) Load: 1e9 Ohm, phase angle.

(e) Load: 50 Ohm, magnitude.

(f) Load: 50 Ohm, phase angle.

Figure A.11: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (10mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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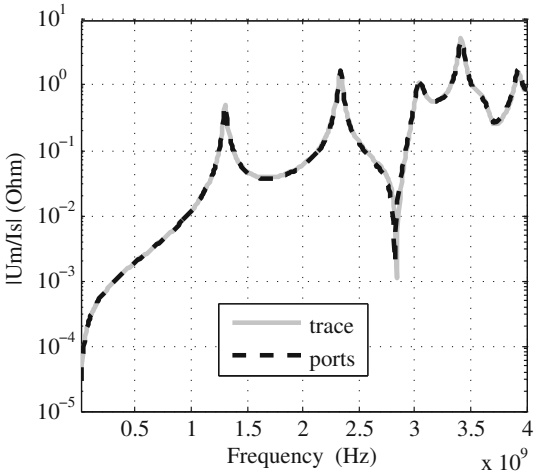
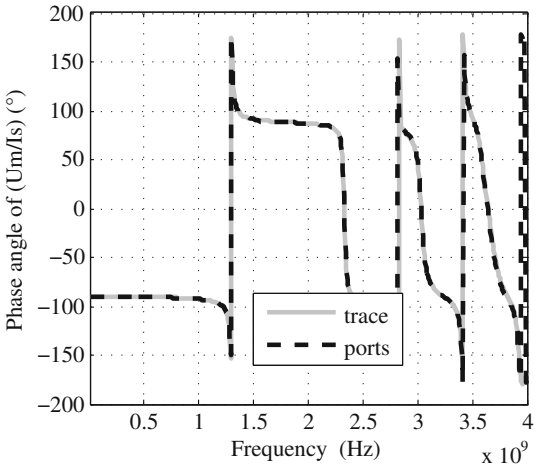
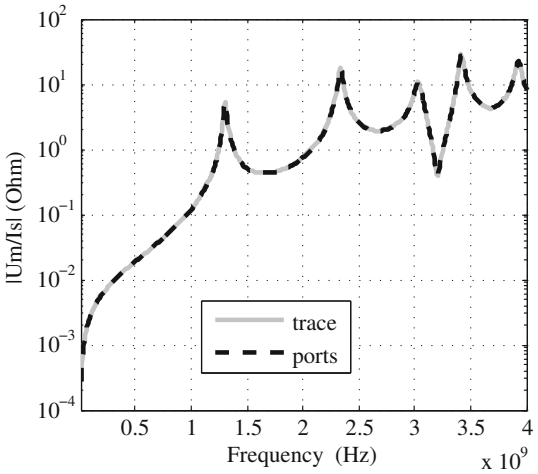


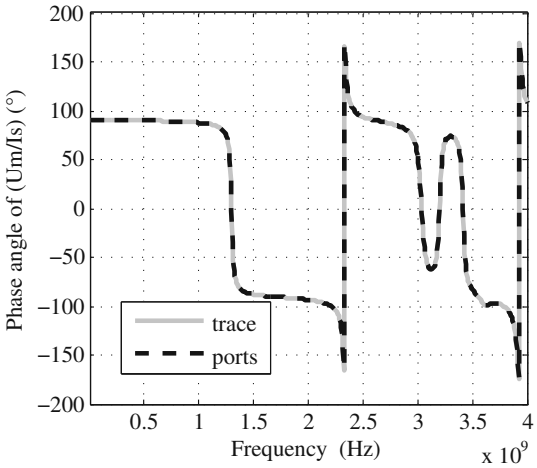
(a) Load: 0 Ohm, magnitude.



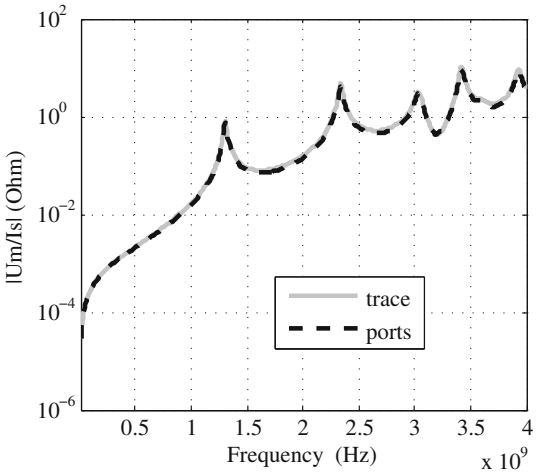
(b) Load: 0 Ohm, phase angle.



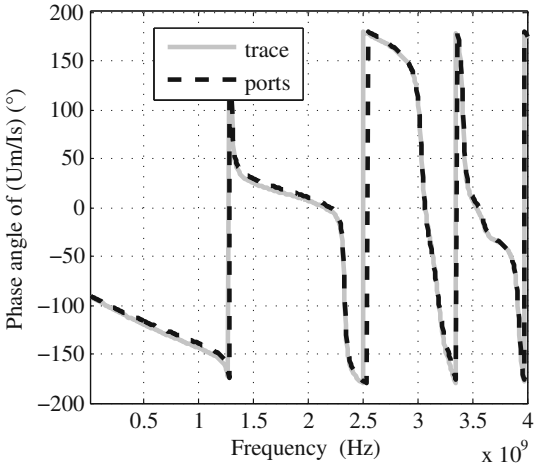
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.12: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). The trace is located at position (10mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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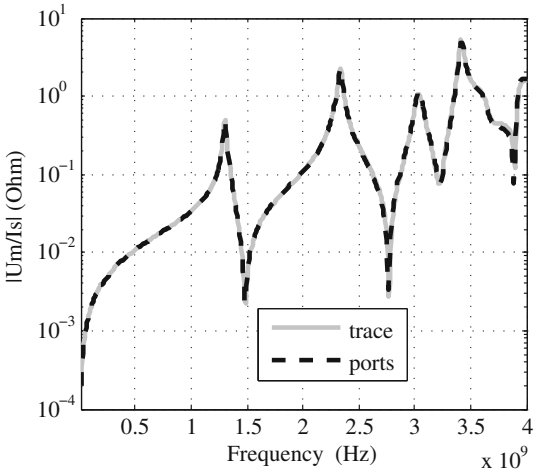
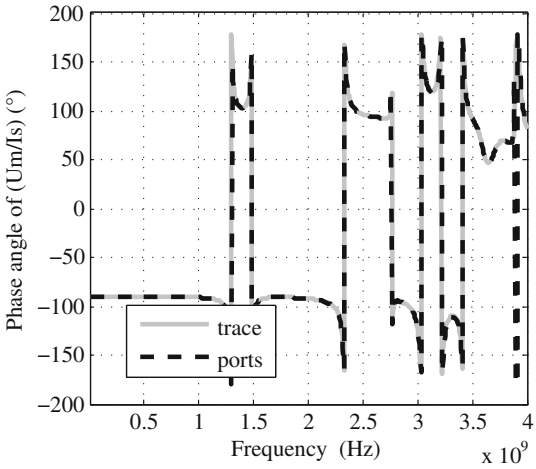
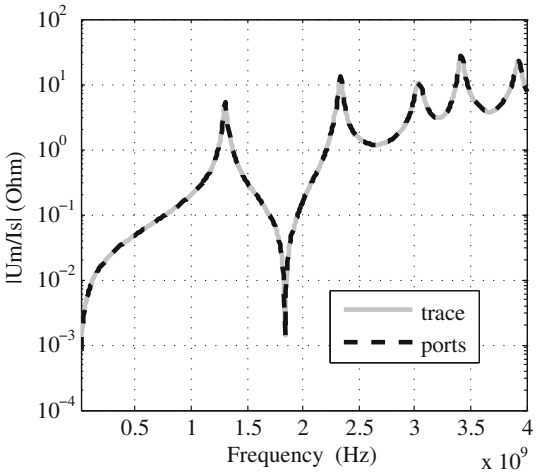


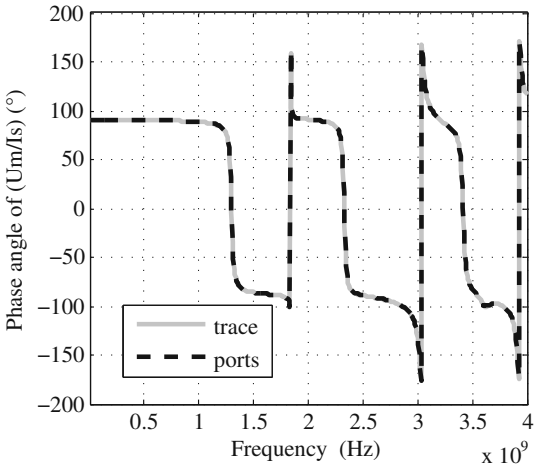
(a) Load: 0 Ohm, magnitude.



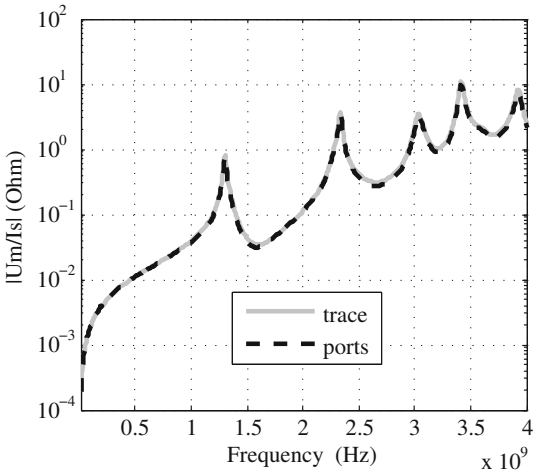
(b) Load: 0 Ohm, phase angle.



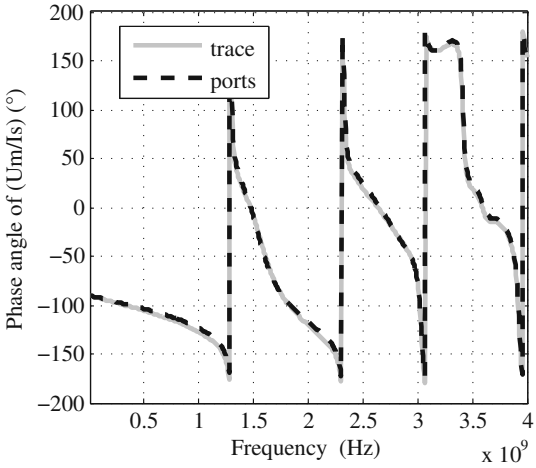
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.13: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). The trace is located at position (10mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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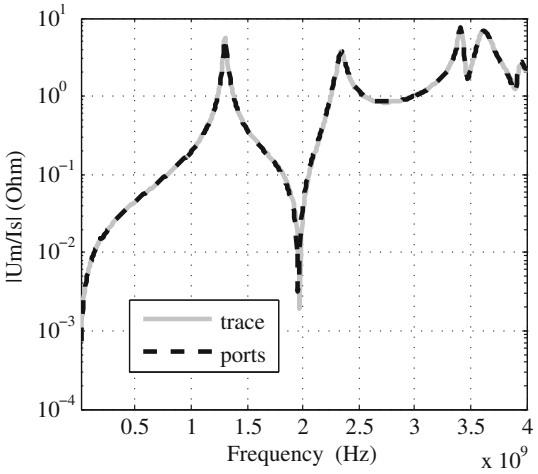

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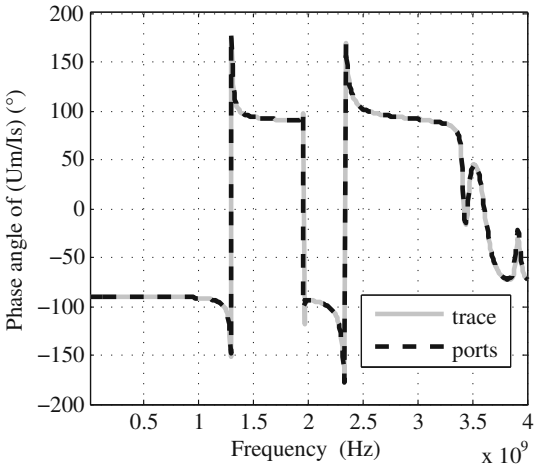
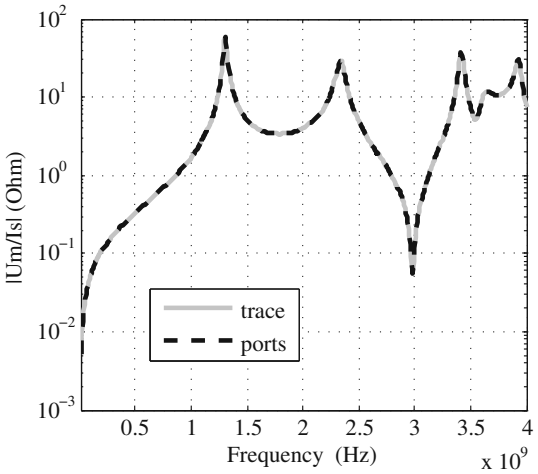
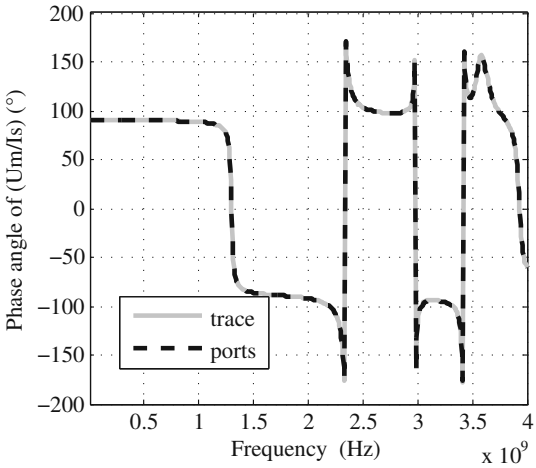


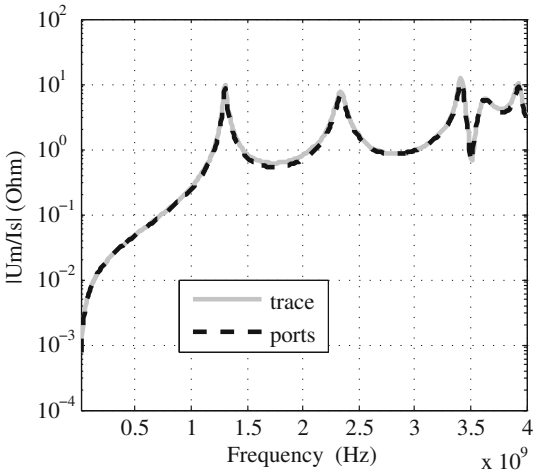
(b) Load: 0 Ohm, phase angle.



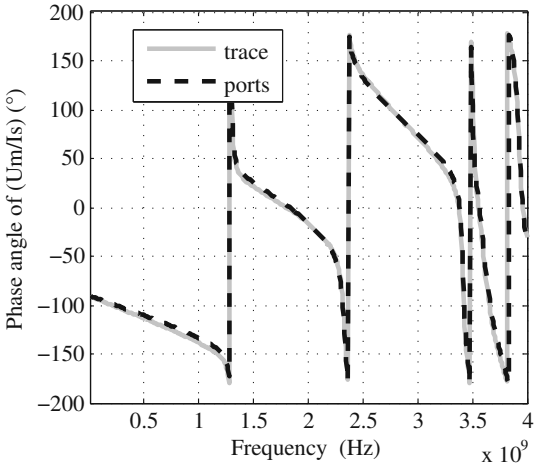
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.14: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (35mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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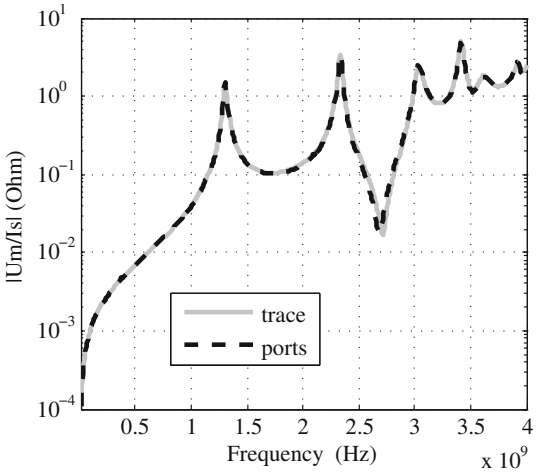

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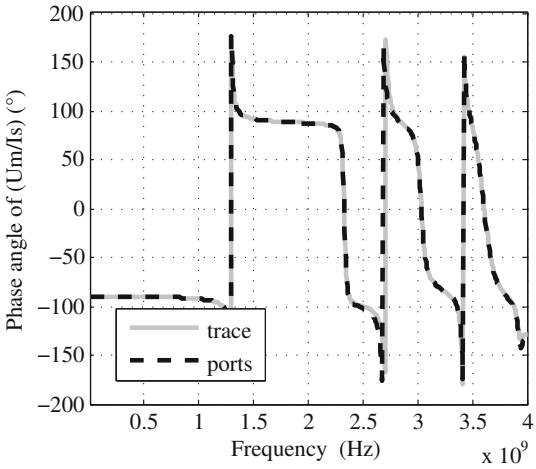

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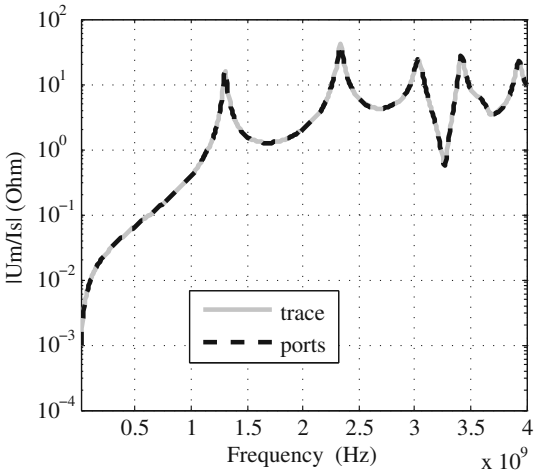
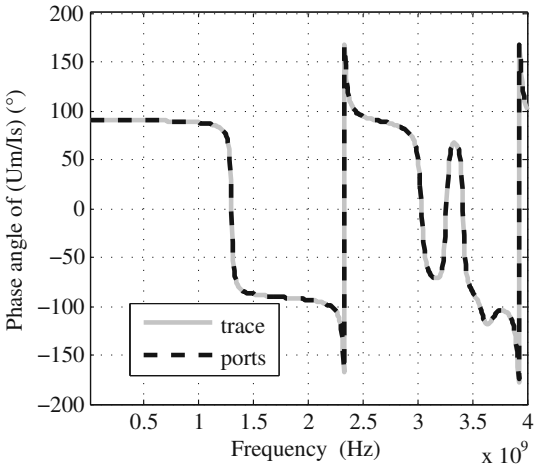


(c) Load: 1e9 Ohm, magnitude.



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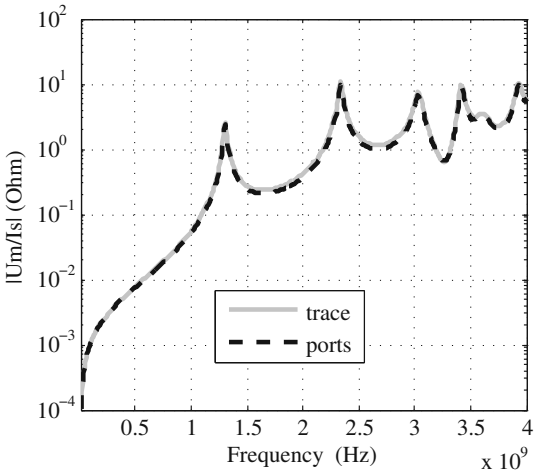
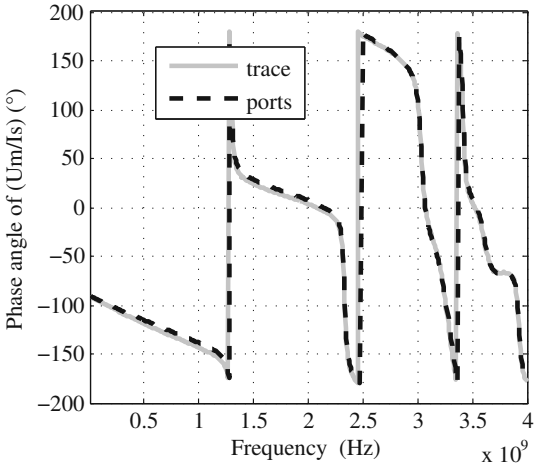


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.15: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). The trace is located at position (35mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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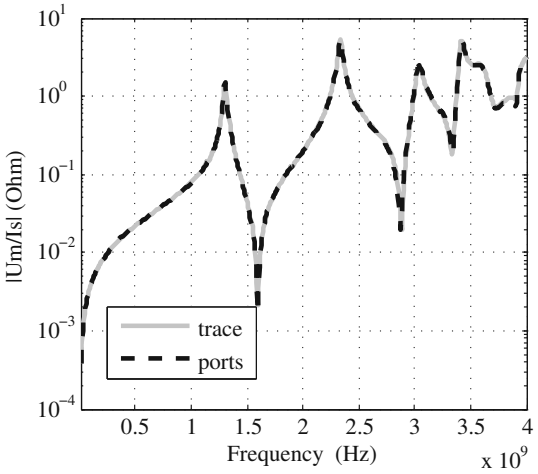

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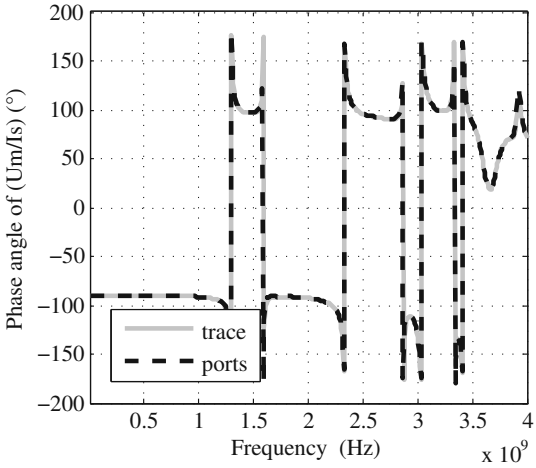
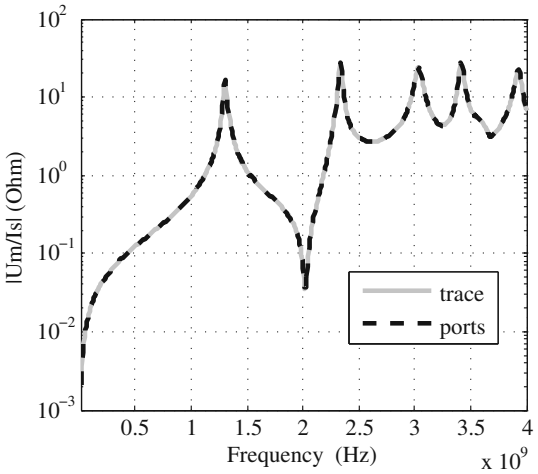
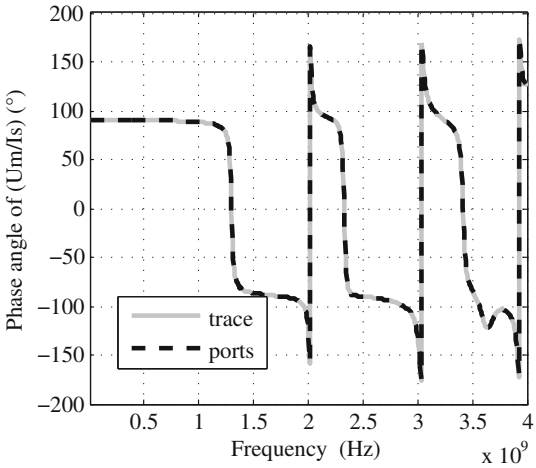


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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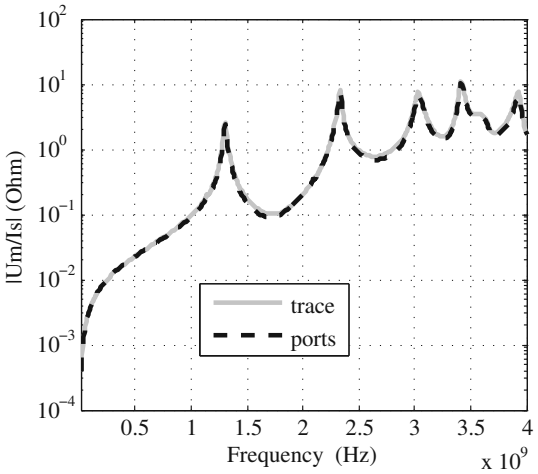
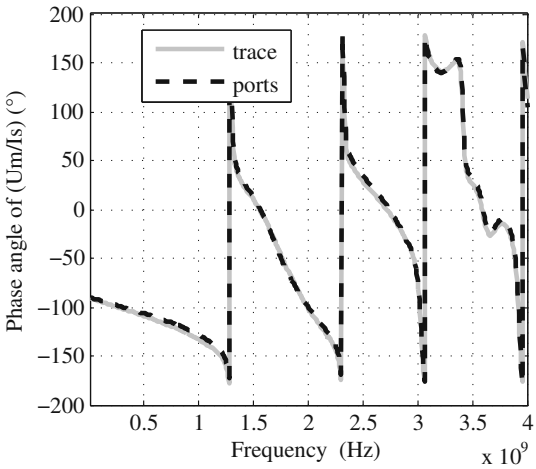


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.16: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). The trace is located at position (35mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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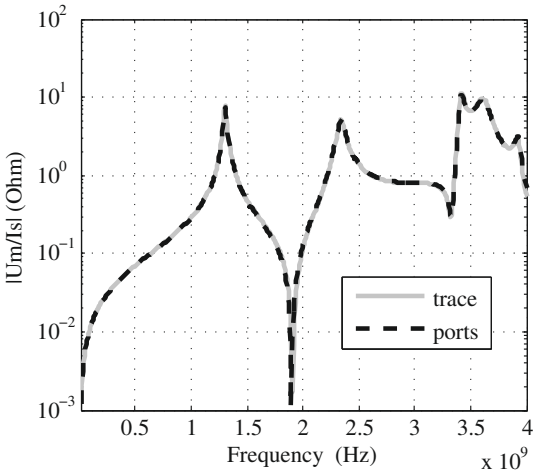
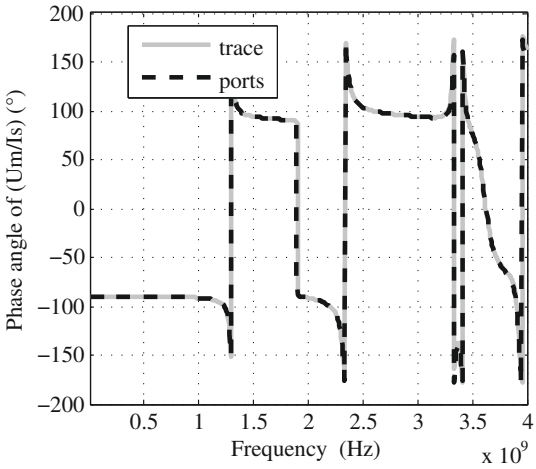
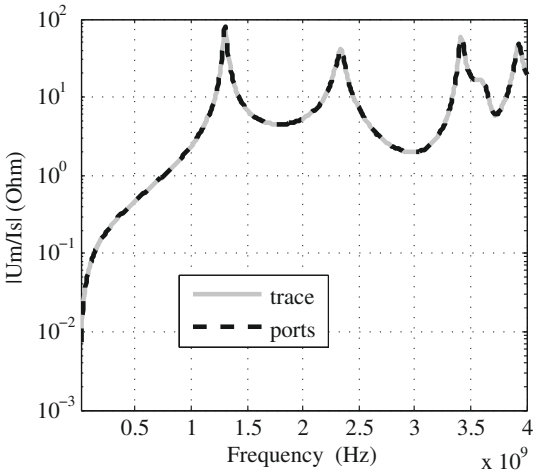


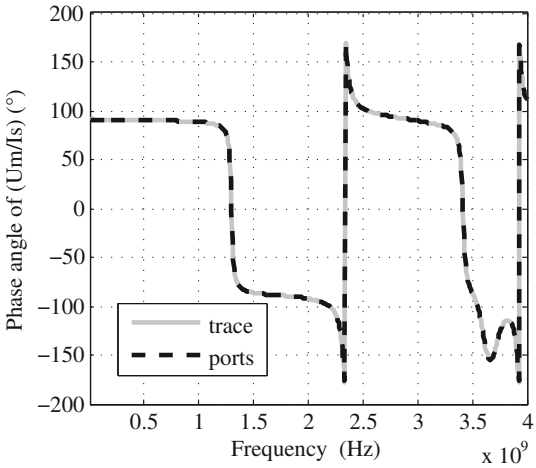
(a) Load: 0 Ohm, magnitude.



(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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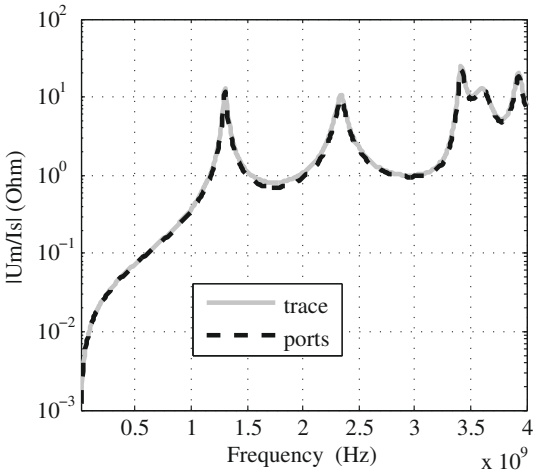
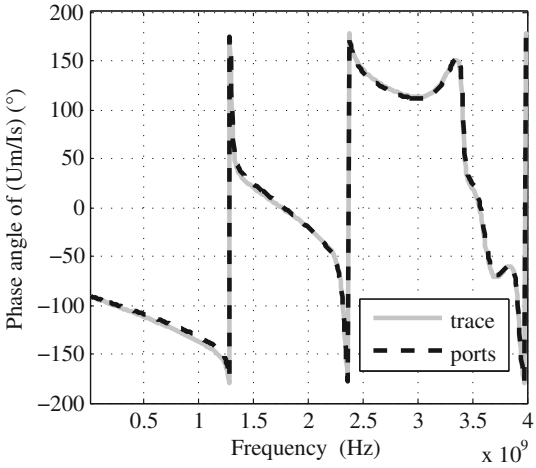


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.17: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (67mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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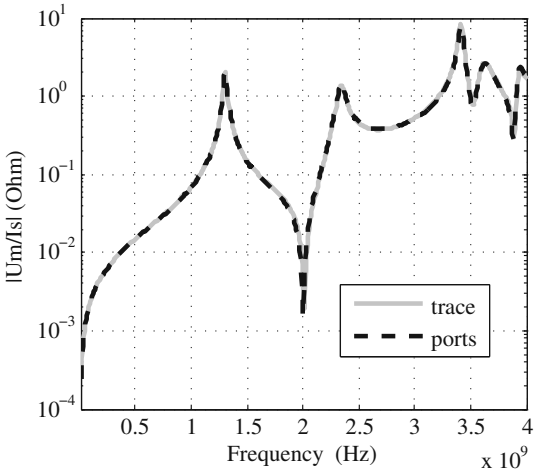
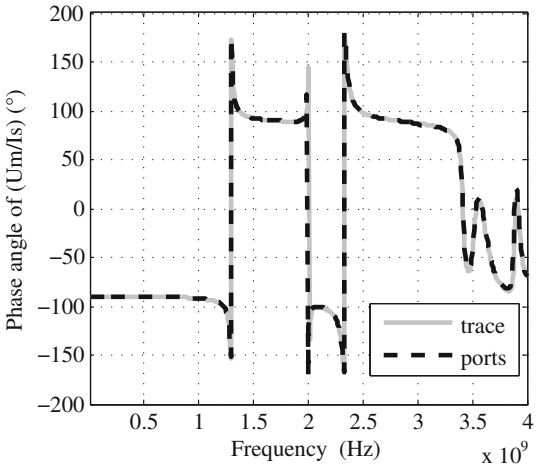
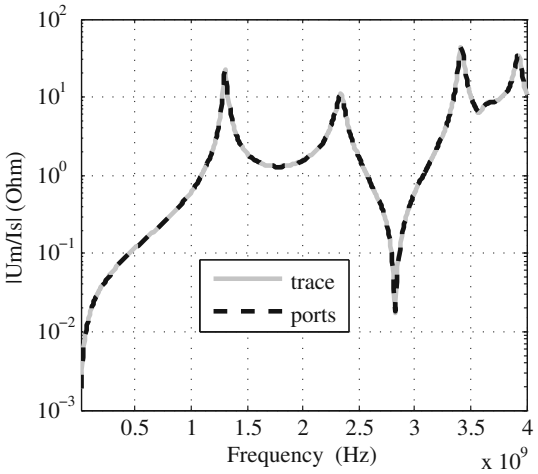


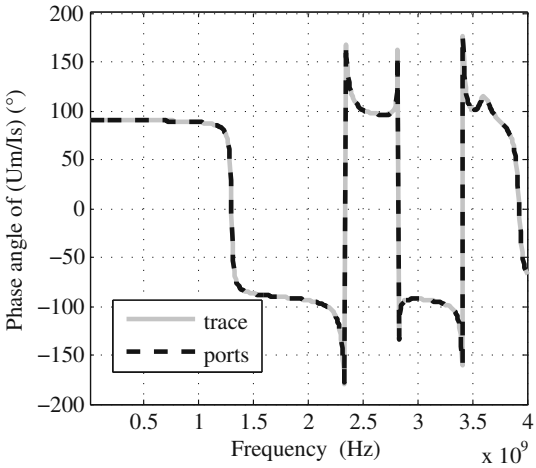
(a) Load: 0 Ohm, magnitude.



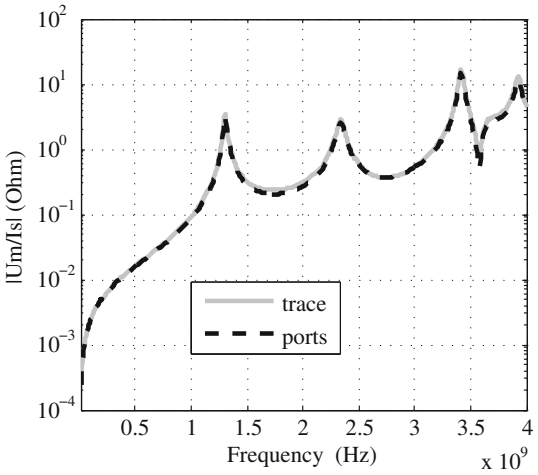
(b) Load: 0 Ohm, phase angle.



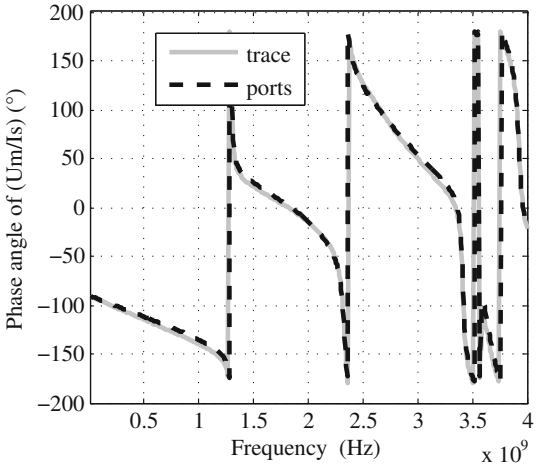
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.18: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). The trace is located at position (67mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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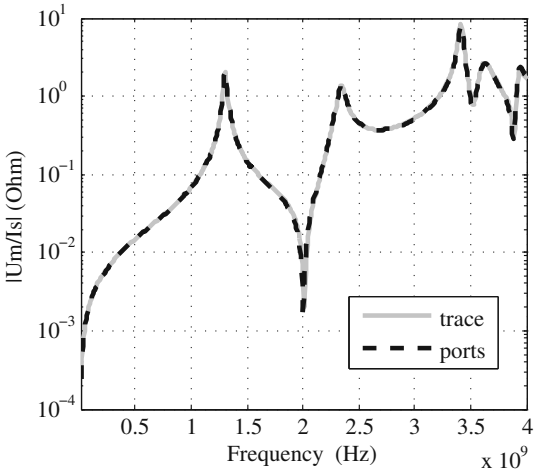
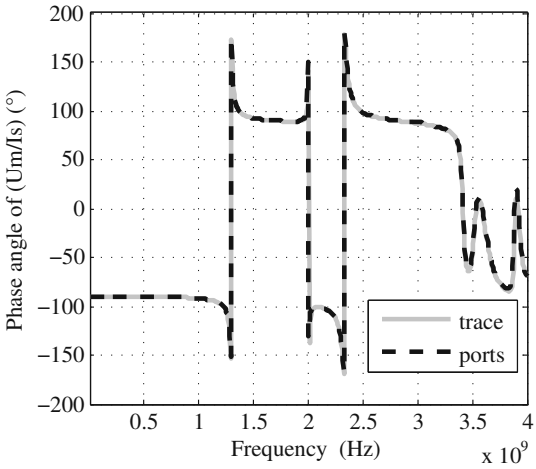
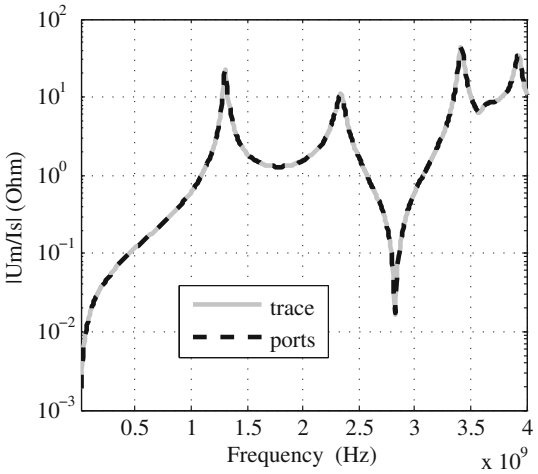


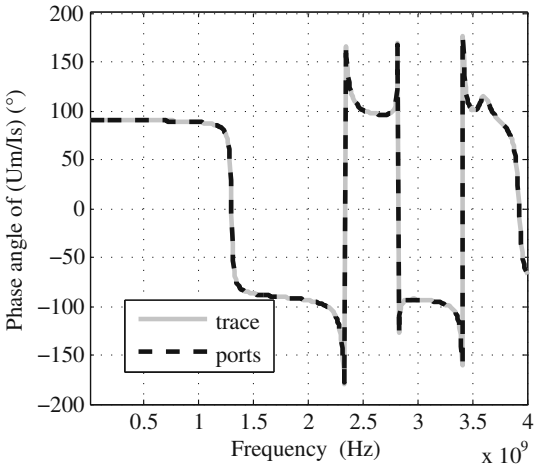
(a) Load: 0 Ohm, magnitude.



(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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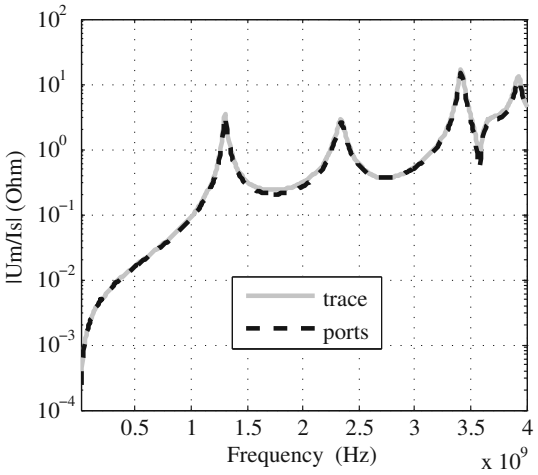
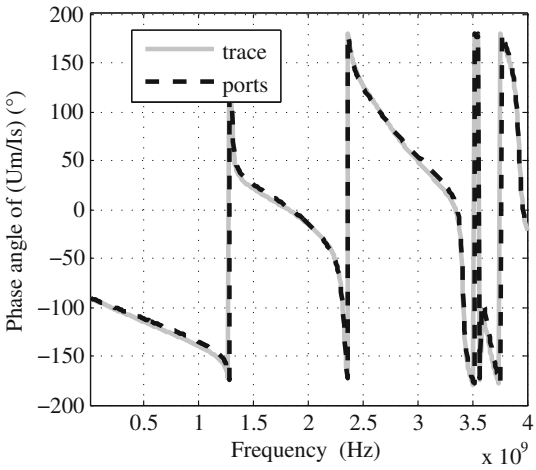


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.19: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). The trace is located at position (67mm,50mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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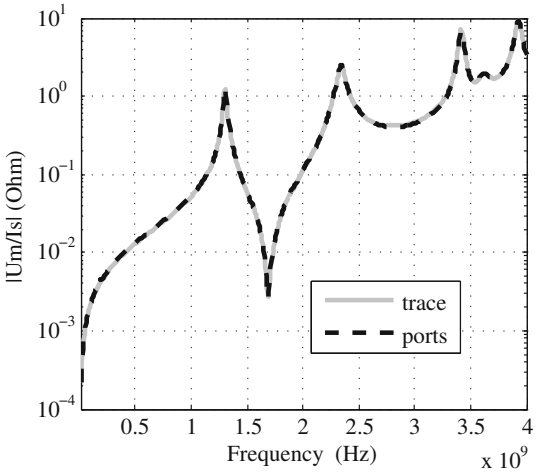

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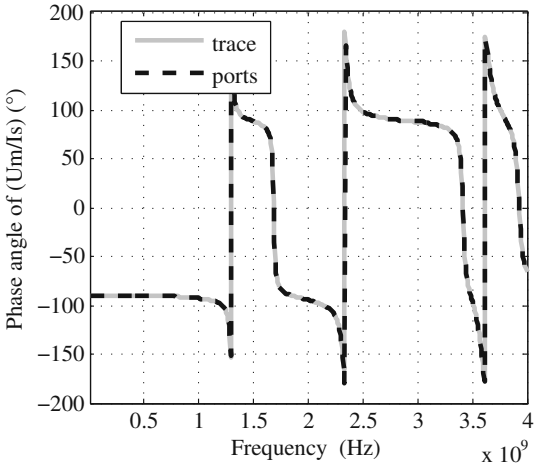

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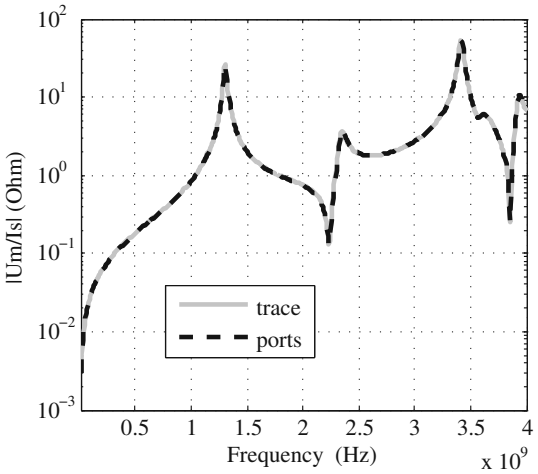

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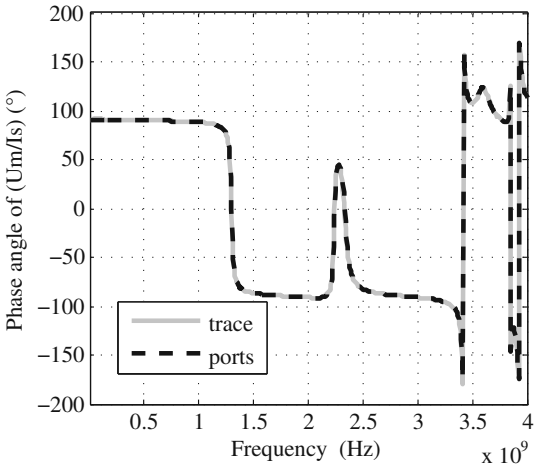

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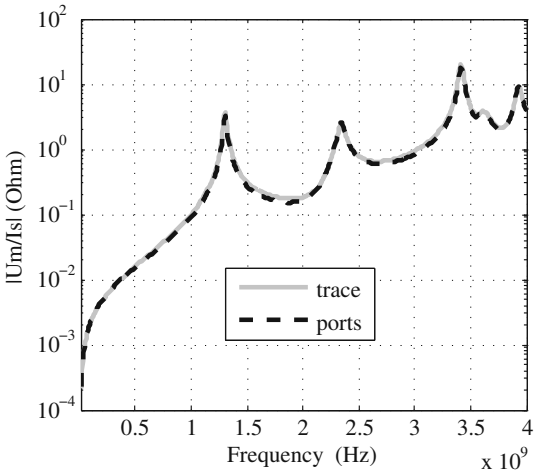
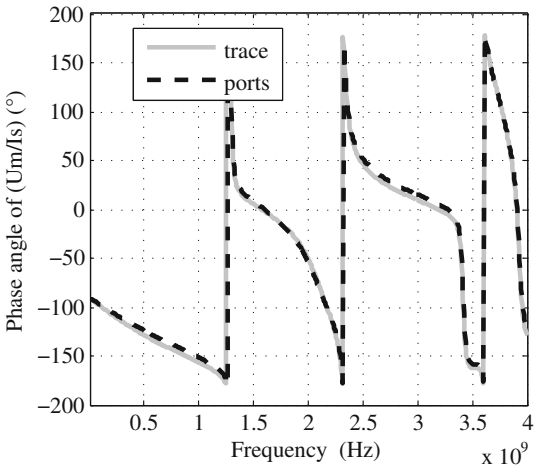


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.20: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (10mm,80mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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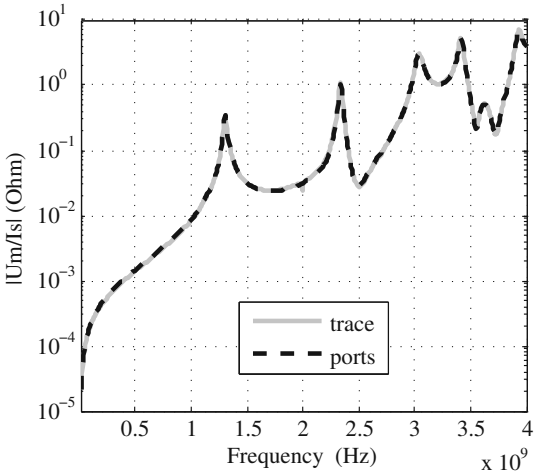

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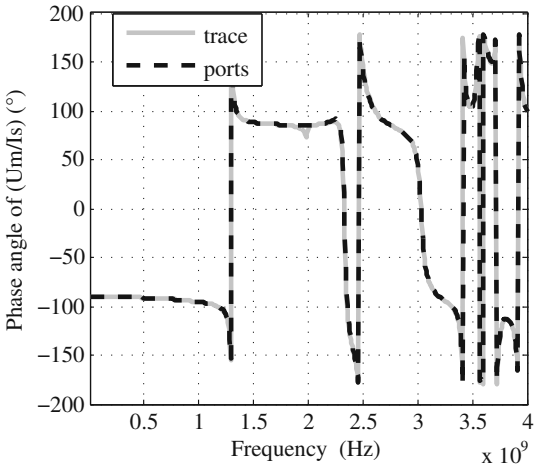
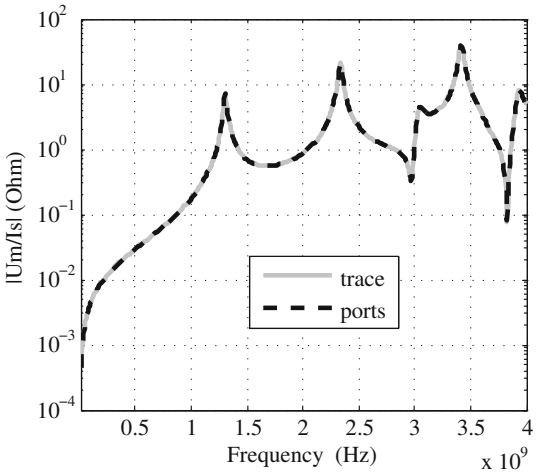
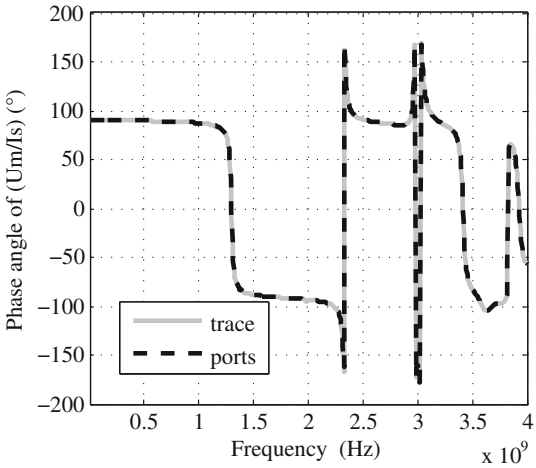


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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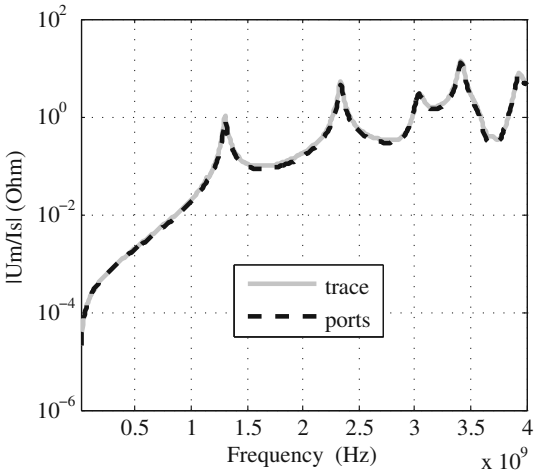
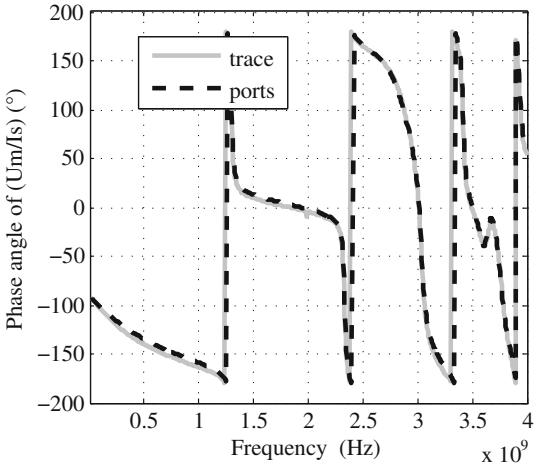


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.21: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). The trace is located at position (10mm,80mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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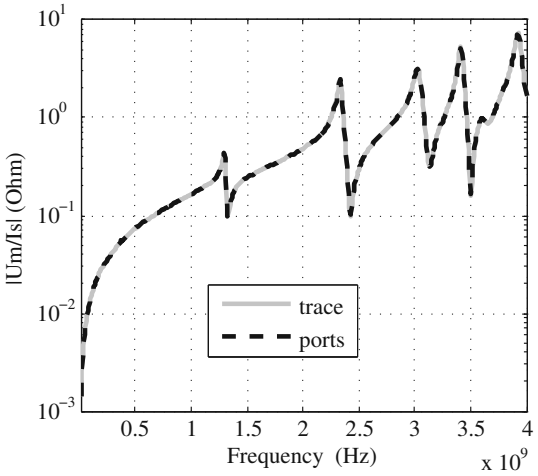

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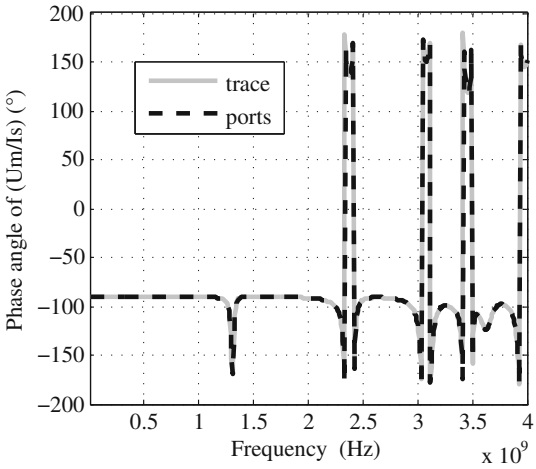
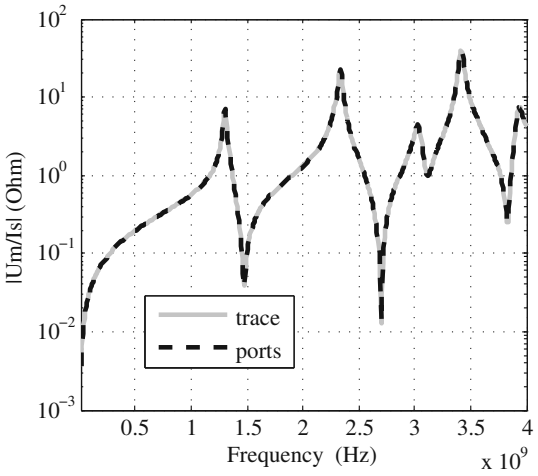
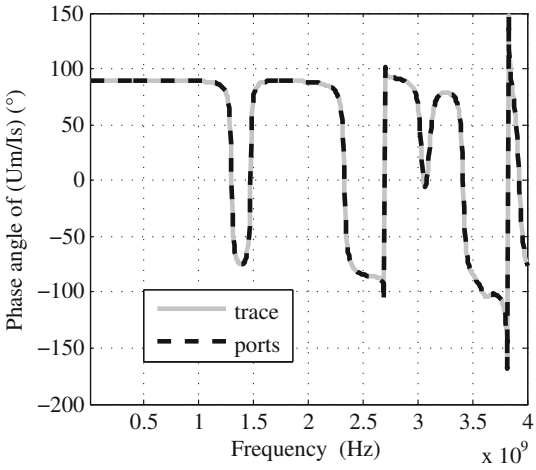


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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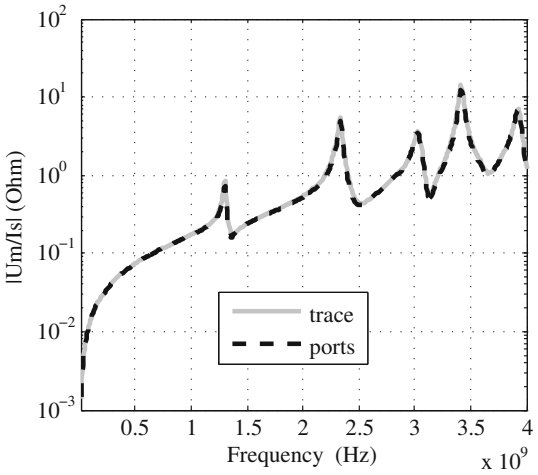
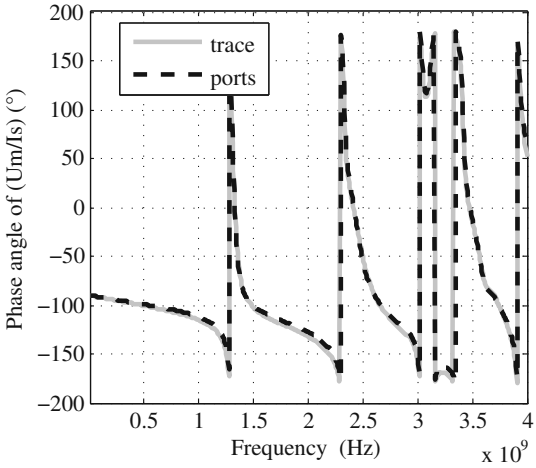


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.22: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). The trace is located at position (10mm,80mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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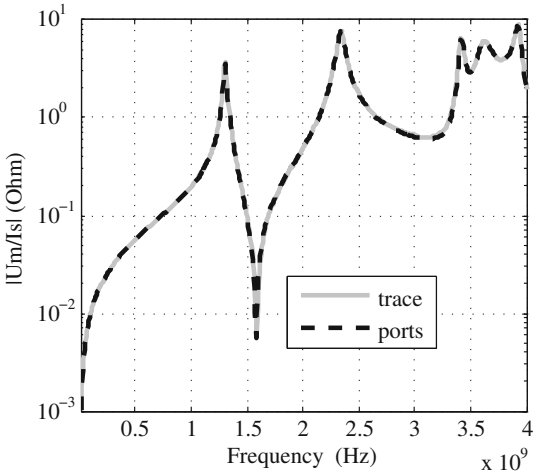

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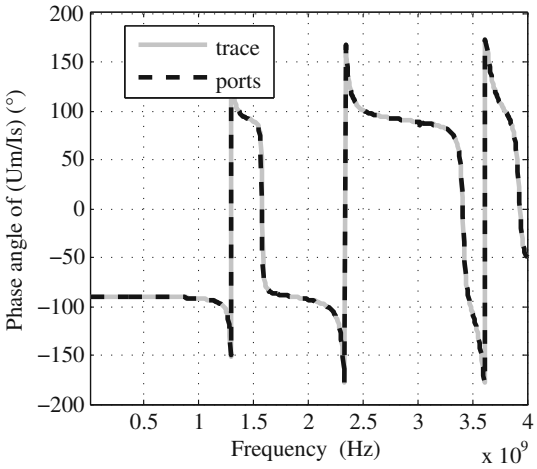
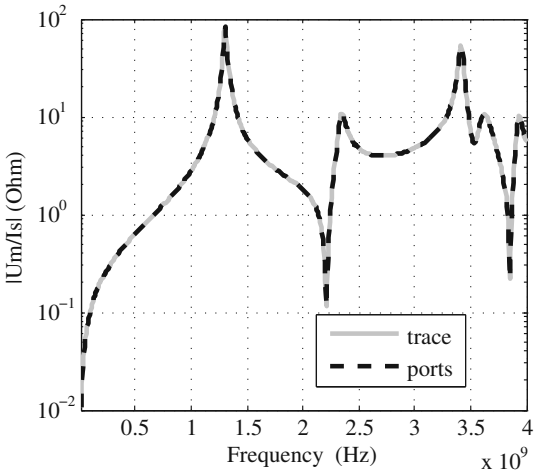
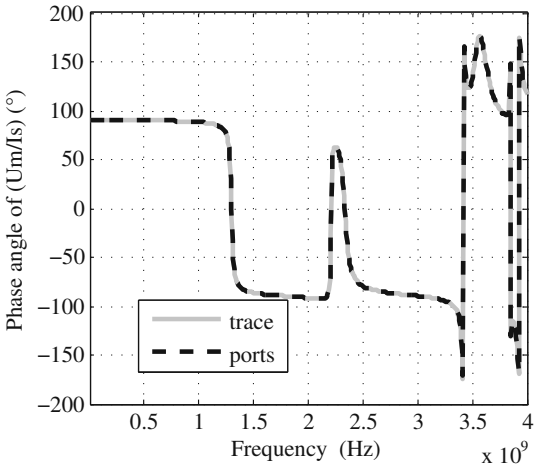


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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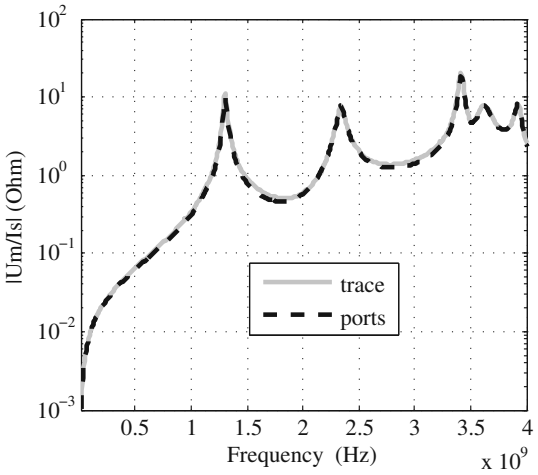

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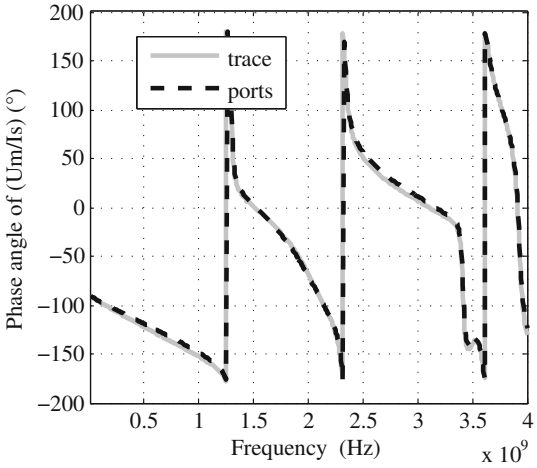

(f) Load: 50 Ohm, phase angle.

Figure A.23: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (35mm,80mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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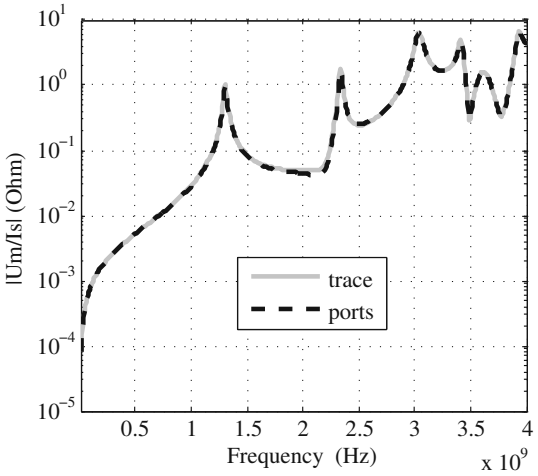

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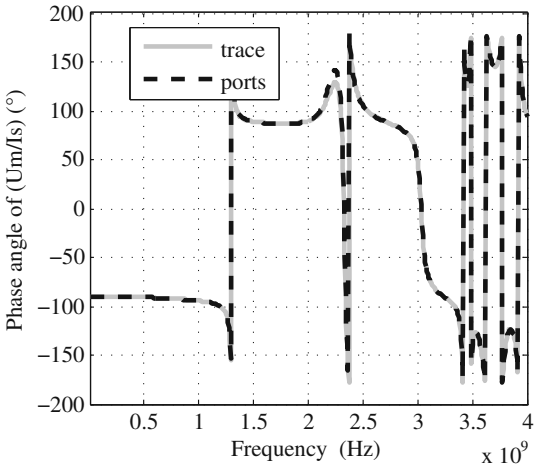

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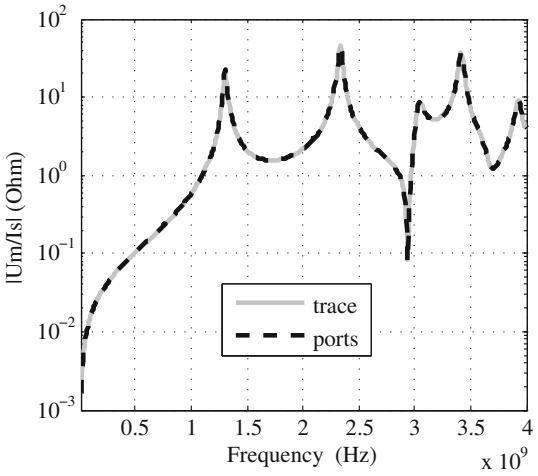
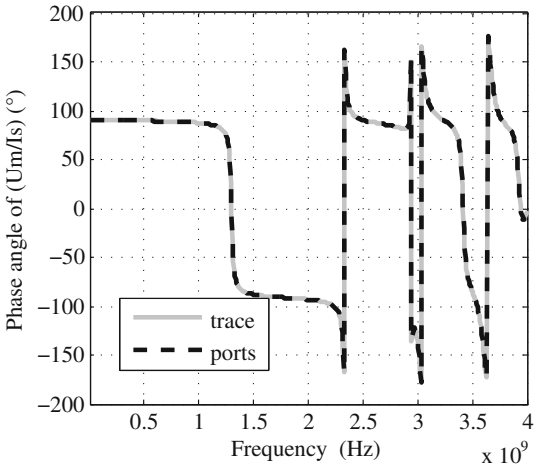


(c) Load: 1e9 Ohm, magnitude.



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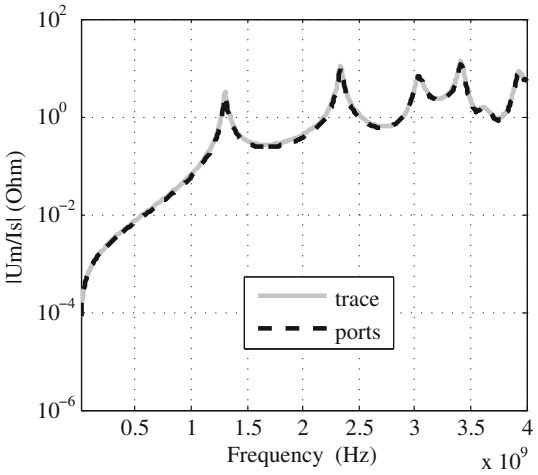
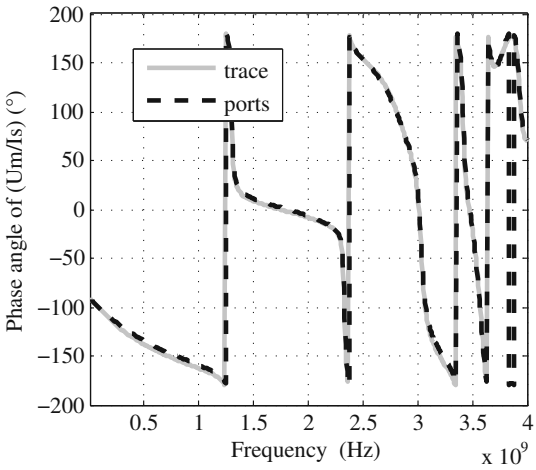


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.24: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). The trace is located at position (35mm,80mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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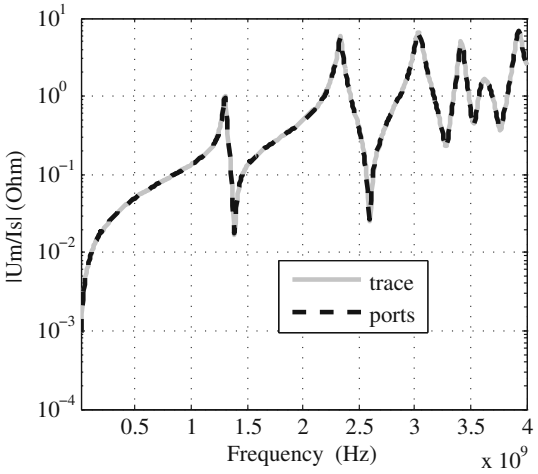

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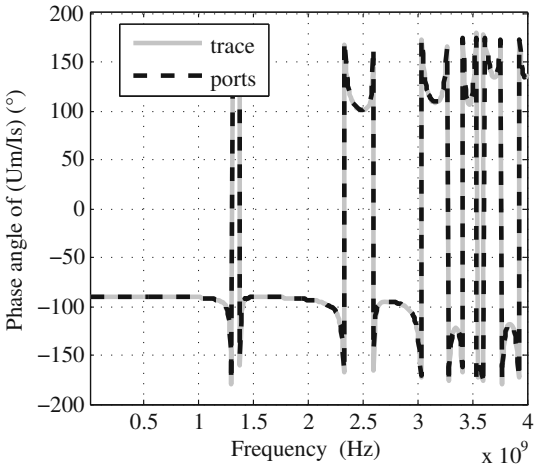

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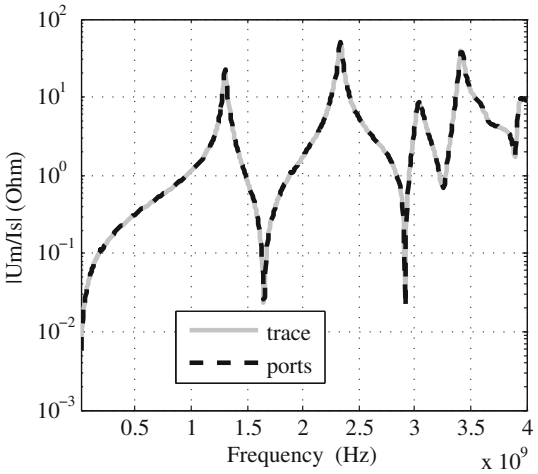
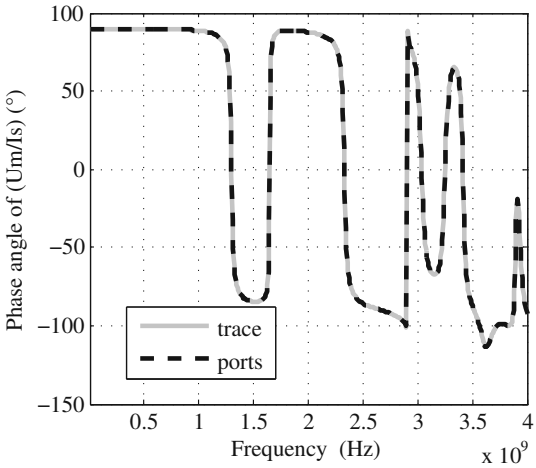


(c) Load: 1e9 Ohm, magnitude.



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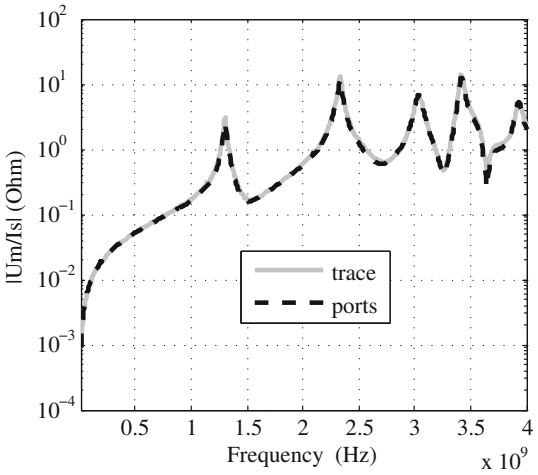
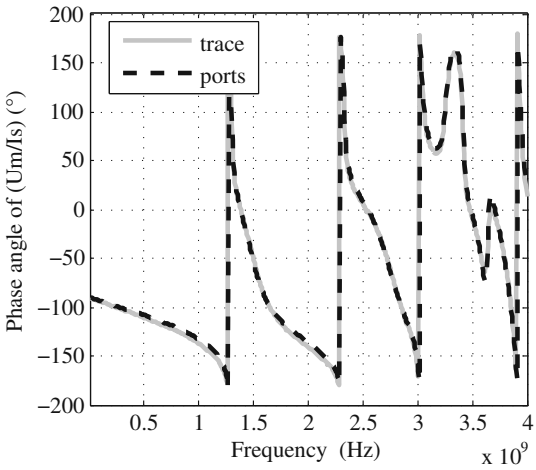


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.25: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). The trace is located at position (35mm,80mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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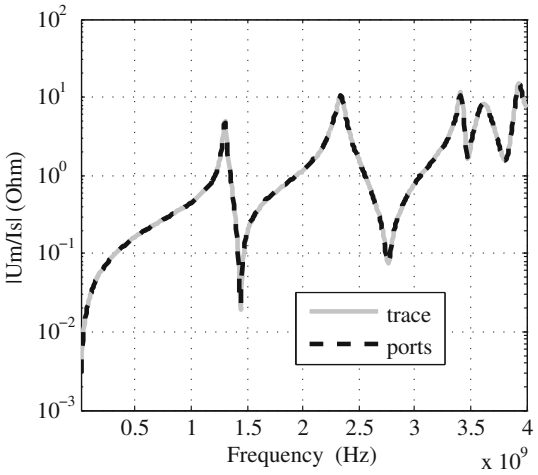
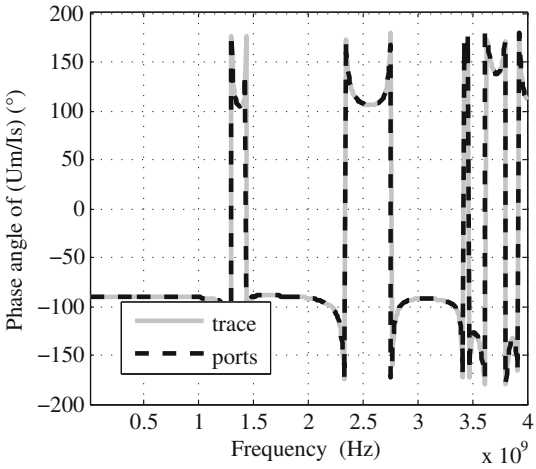


(a) Load: 0 Ohm, magnitude.



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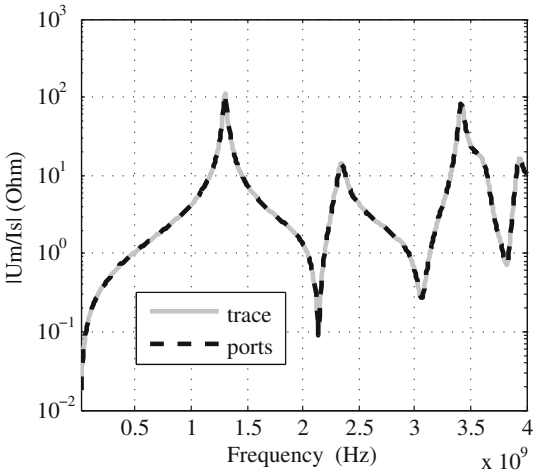
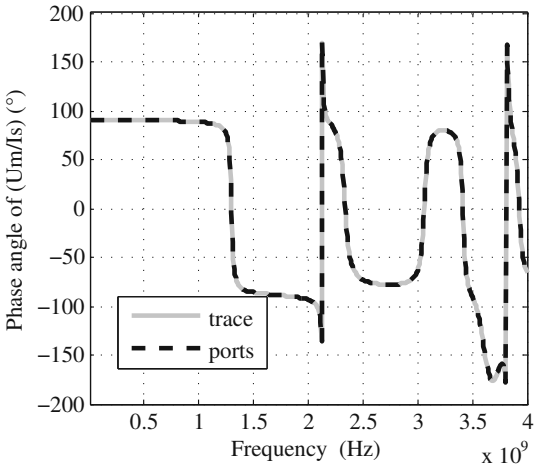


(c) Load: 1e9 Ohm, magnitude.



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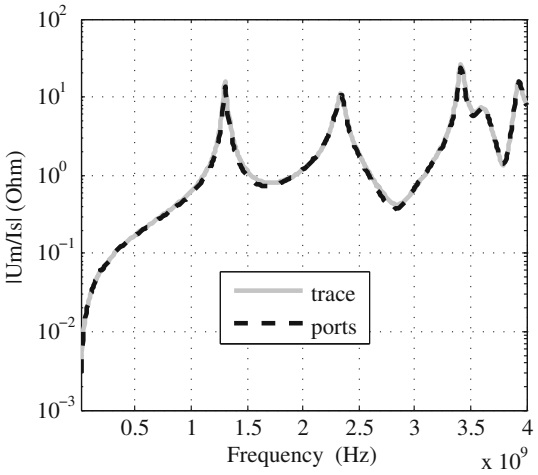
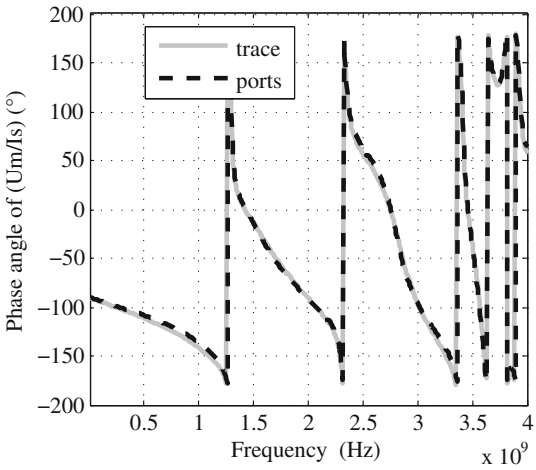


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.26: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). The trace is located at position (67mm,80mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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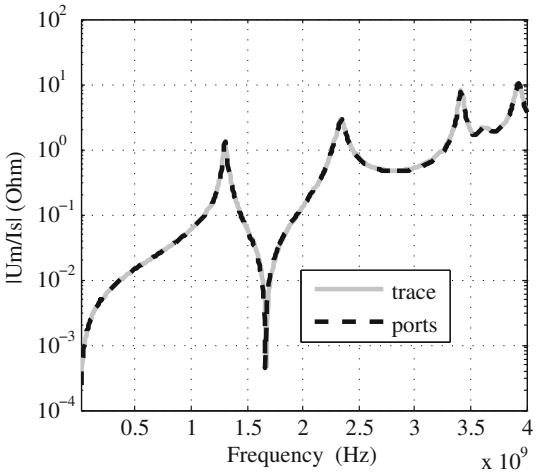

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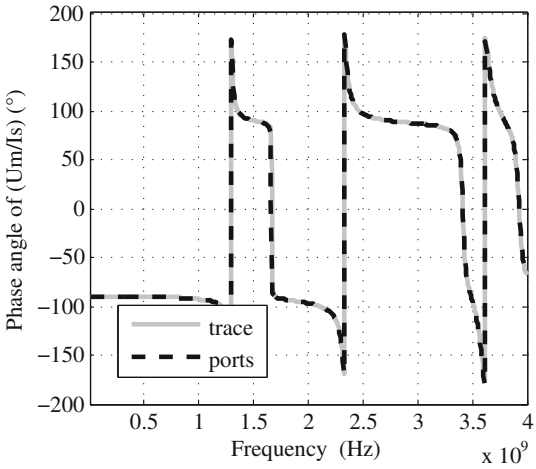
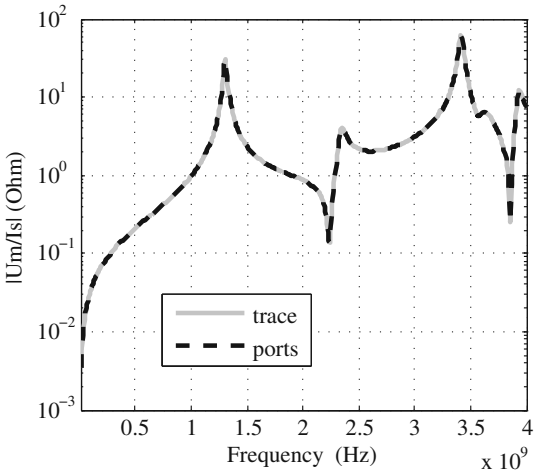
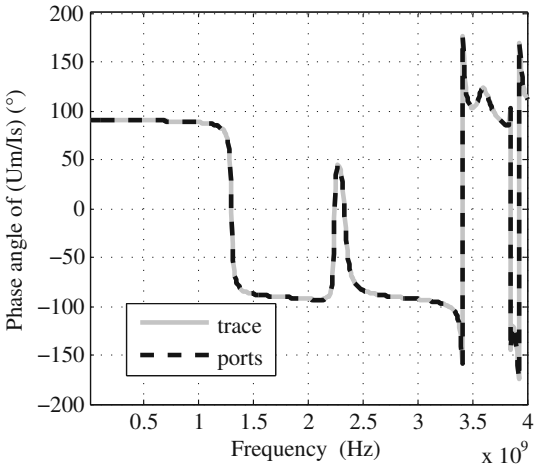


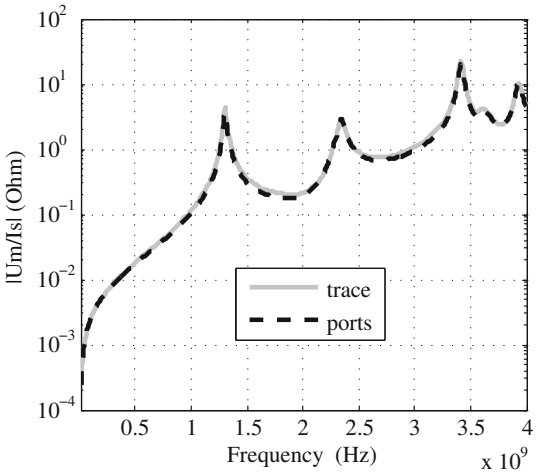
(b) Load: 0 Ohm, phase angle.



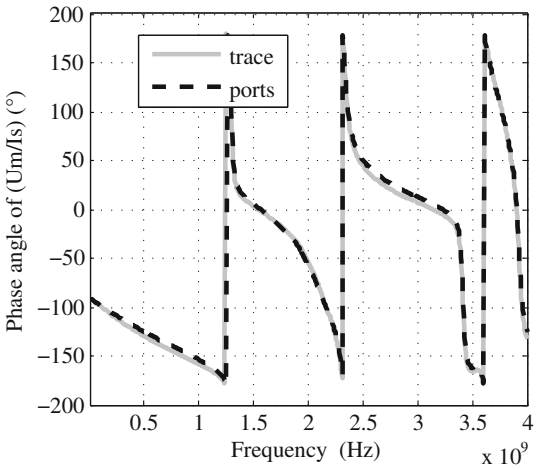
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.27: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). The trace is located at position (67mm,80mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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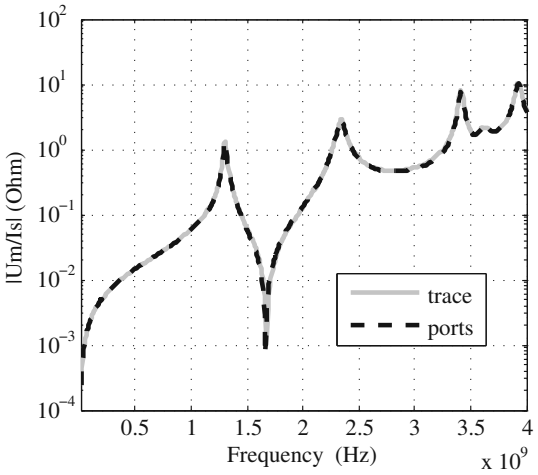

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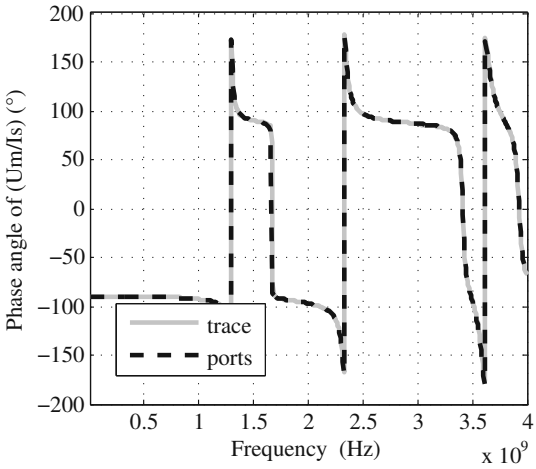
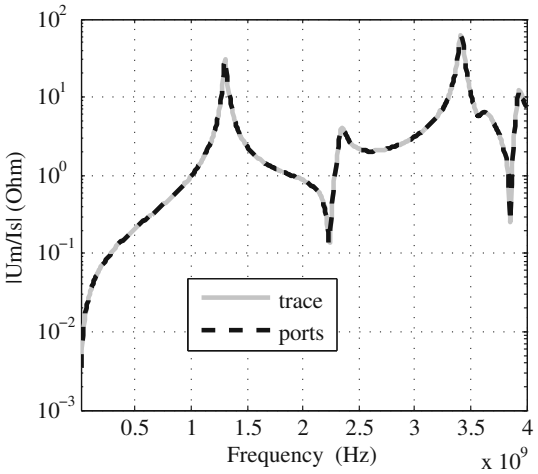
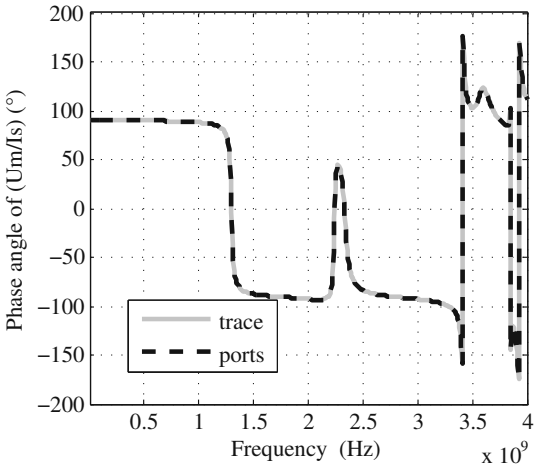


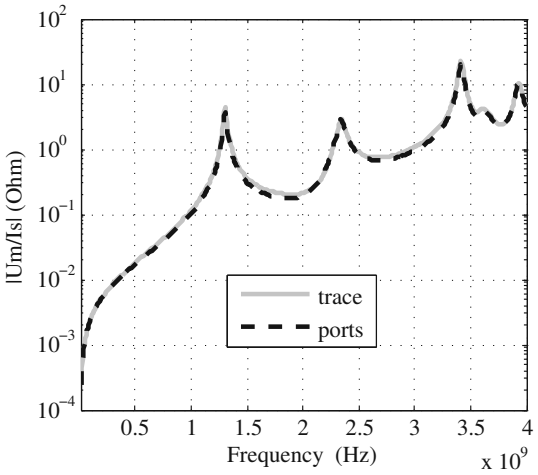
(b) Load: 0 Ohm, phase angle.



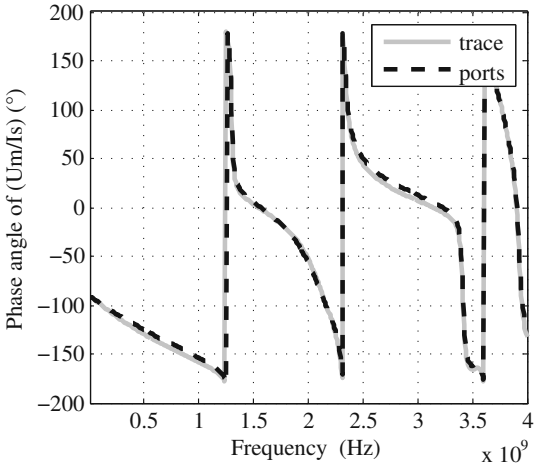
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.28: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). The trace is located at position (67mm,80mm) and the trace length is 5mm. Trace orientation in y-direction. Comparison of HFSS results from a model with a trace and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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A.2. Variation of the enclosure height and the trace height above the ground plane, comparisons of the transfer impedance for parallel planes with four open edges and comparison of the transfer impedance for the two different trace routings in Figure 5.7

The previous validation comparisons for the coupling factor d/h have been carried out for an enclosure height of 7mm. This section contains comparisons for the enclosure with the heights 10mm and 15mm, respectively.

Additional comparisons are presented for trace heights above the ground plane of 1.5mm and 3mm. The good agreement of all comparisons validate the trace introduction coupling factor d/h for an enclosure, consisting of parallel rectangular planes with three closed and one open edges, depicted in Figure 7.1.

The calculation of the coupling from PCB sources to the cavity field inside a slim enclosure for emission simulation purposes is the intended application of this dissertation. However, the trace introduction method can also be utilized to calculate the coupling of traces to the parallel plane field of power planes. Parallel planes with four open edges may represent the ground and the power plane on a PCB and a trace between these two planes couples to the power delivery network. Therefore, additional comparisons are presented in this appendix for rectangular parallel planes with four open edges, to prove that the coupling factor is independent of the cavity boundaries. These comparisons also show a very good agreement.

In Section 5.4 a transfer impedance comparison was carried out for different routings of the horizontal routings of two traces with the same trace lengths and same source and load positions on the ground plane. The model configurations are depicted in Figure 5.7. The comparison for the slot measurement port at position (64mm, 104mm) is presented in Figure 5.8 and Figure 5.9. Transfer impedance comparisons for the two other slot measurement ports at (10mm, 104mm) and (124mm, 104mm) are presented in this appendix. The good agreement in these comparisons validates the independence of the trace to cavity coupling from the horizontal trace routing.

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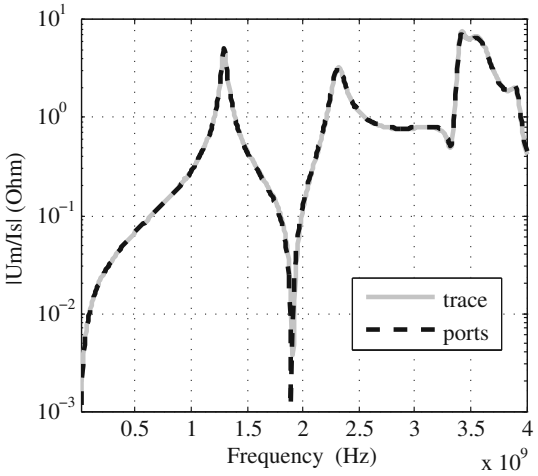
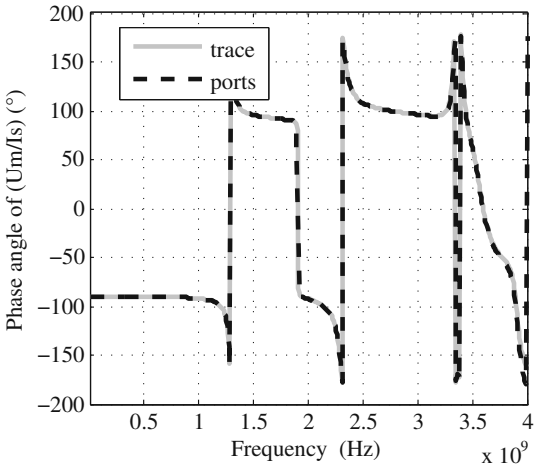
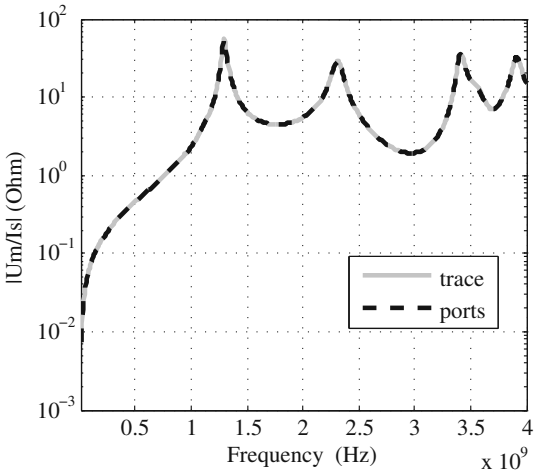


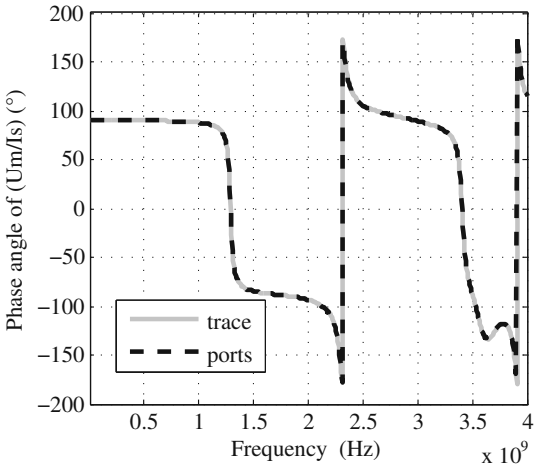
(a) Load: 0 Ohm, magnitude.



(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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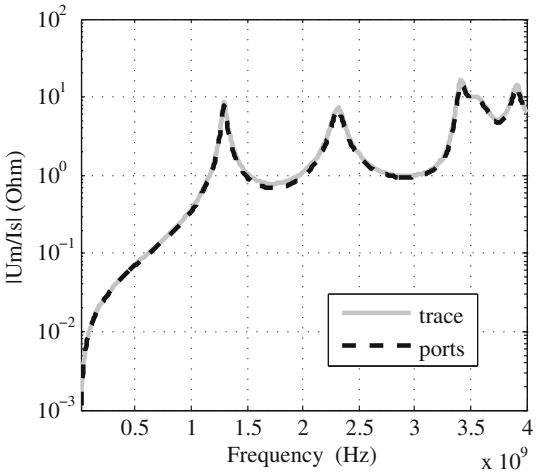
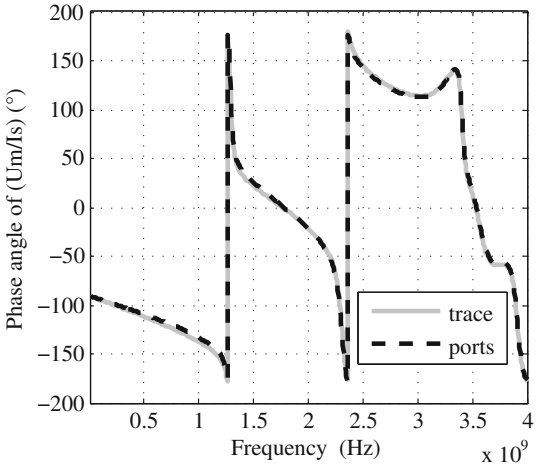


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.29: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm))to the results obtained with (5.6), (5.9) and a HFSS model with ports. The enclosure height h=10mm.

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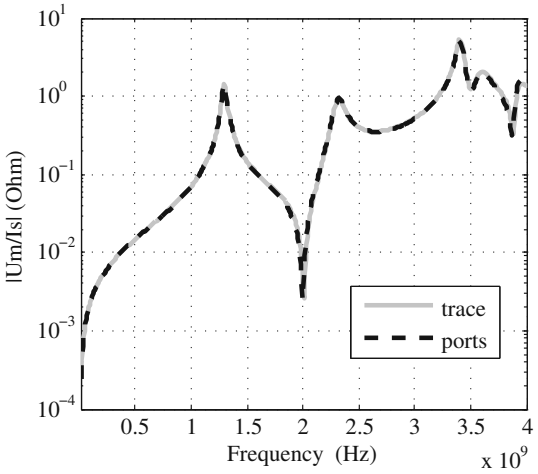

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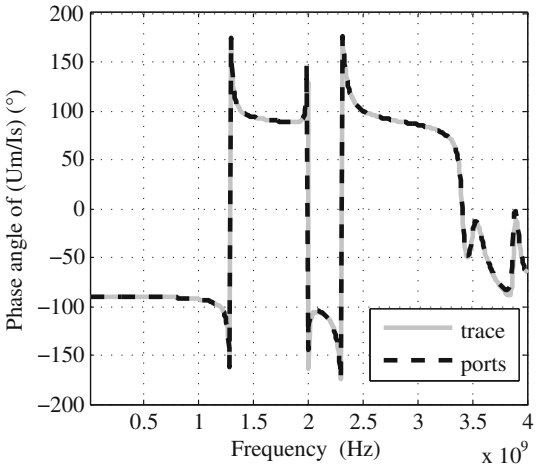
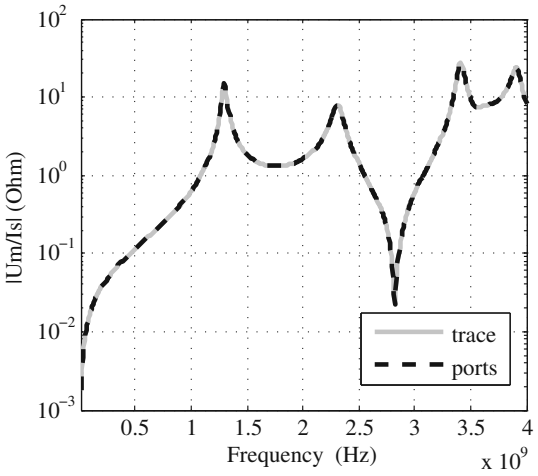
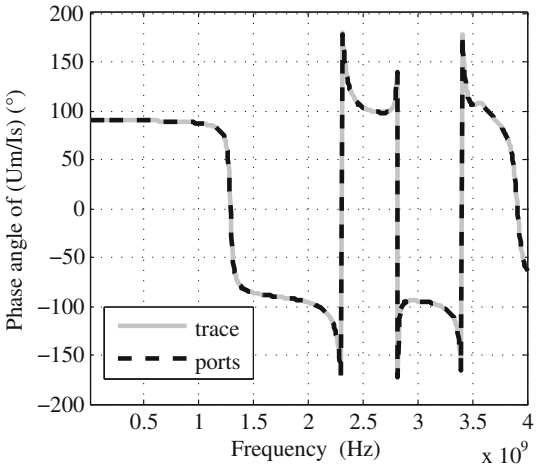


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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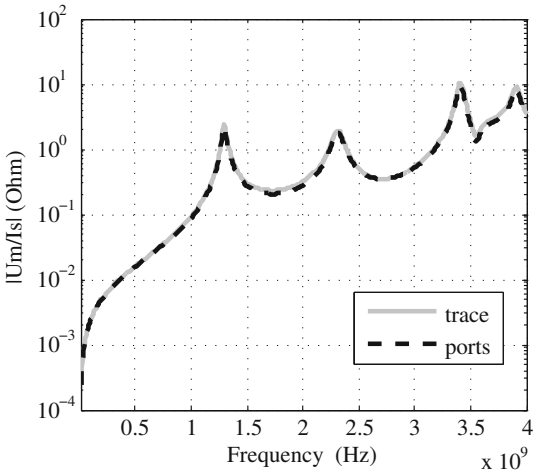
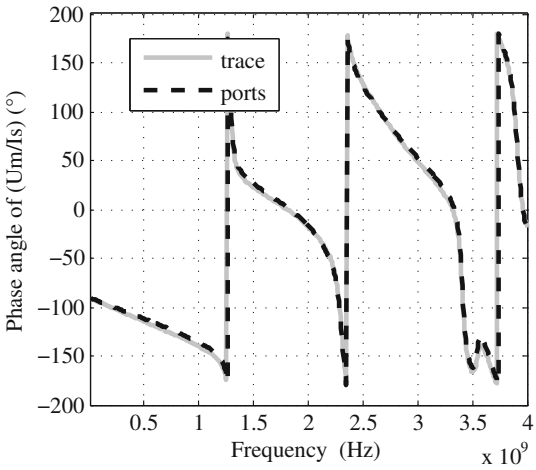


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.30: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm))to the results obtained with (5.6), (5.9) and a HFSS model with ports. The enclosure height h=10mm.

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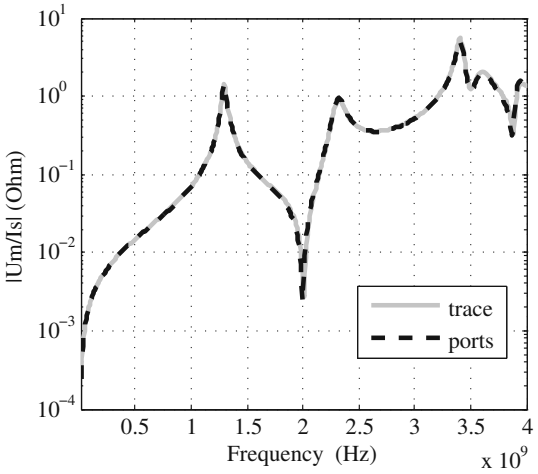

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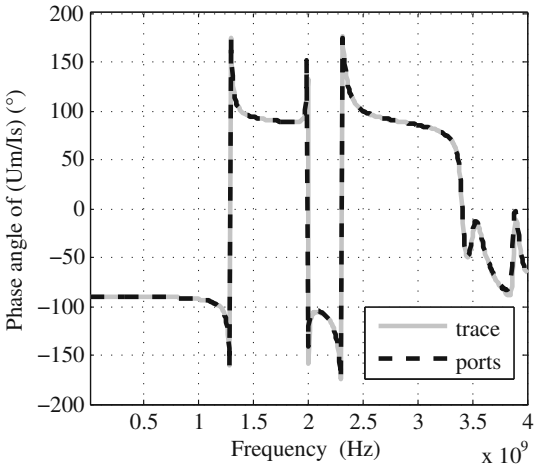

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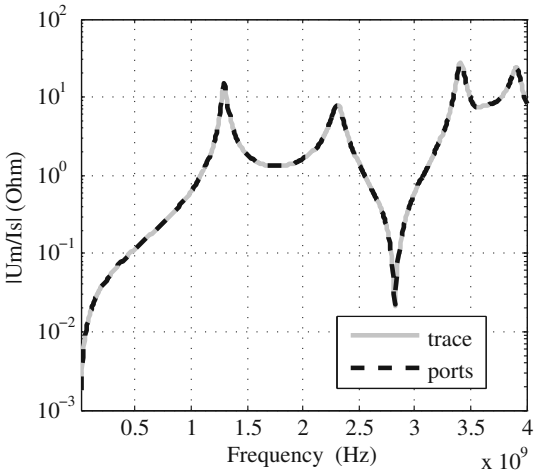

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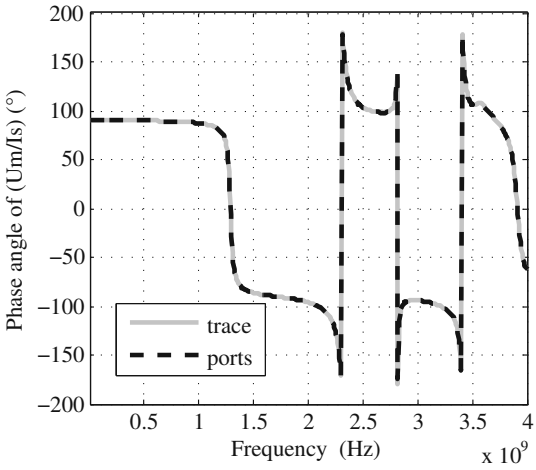

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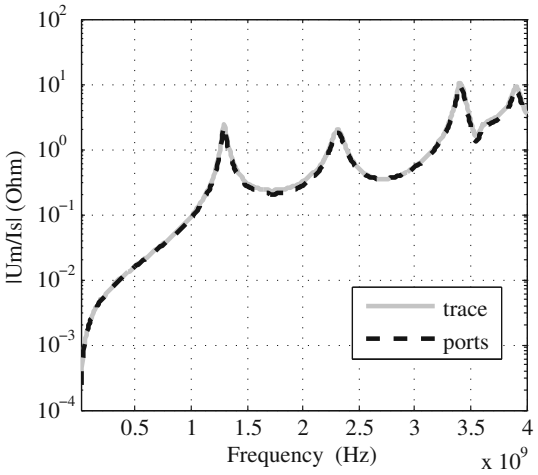
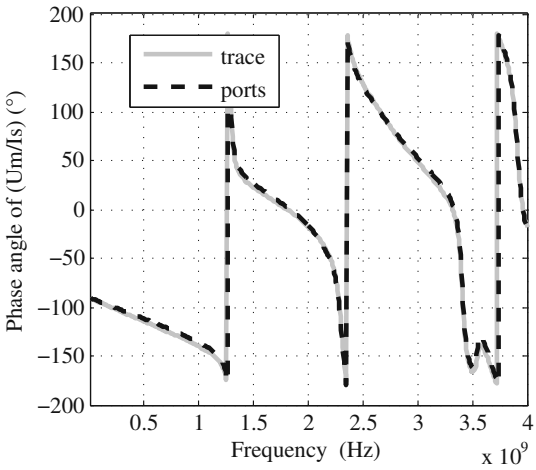


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.31: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm))to the results obtained with (5.6), (5.9) and a HFSS model with ports. The enclosure height h=10mm.

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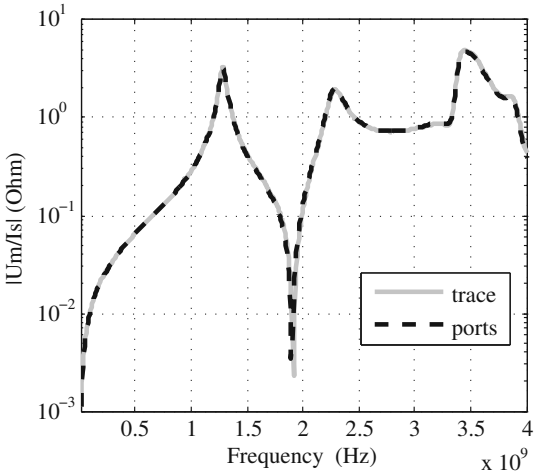

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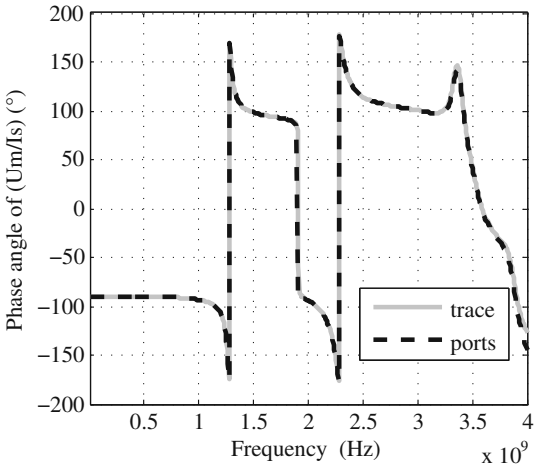

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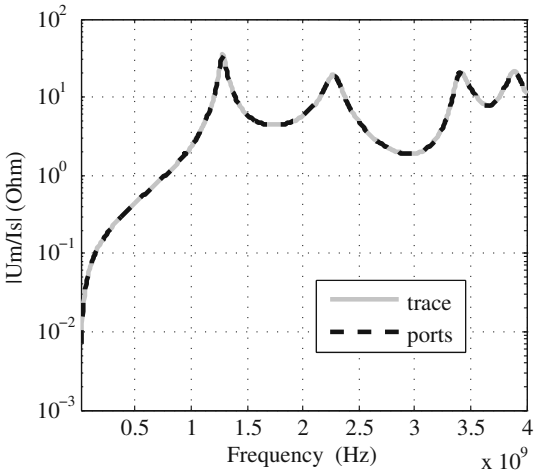
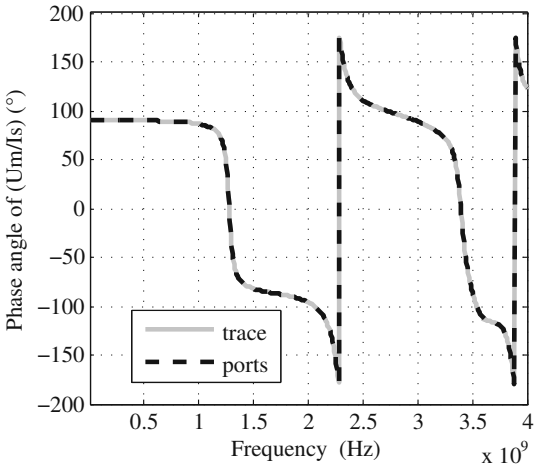


(c) Load: 1e9 Ohm, magnitude.



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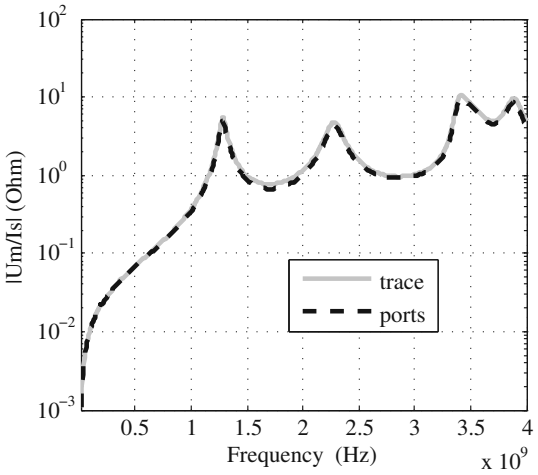
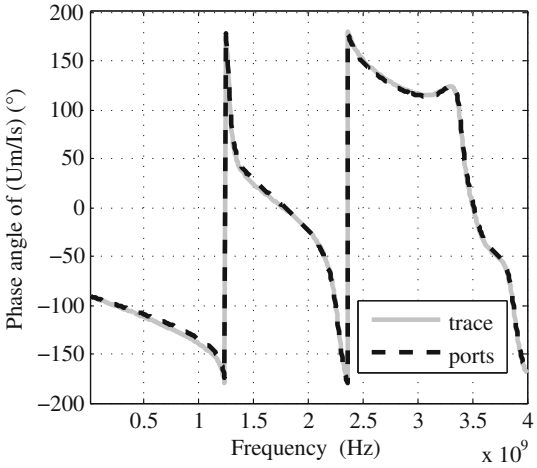


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.32: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm)) and the results obtained with (5.6), (5.9) and a HFSS model with ports. The enclosure height h=15mm.

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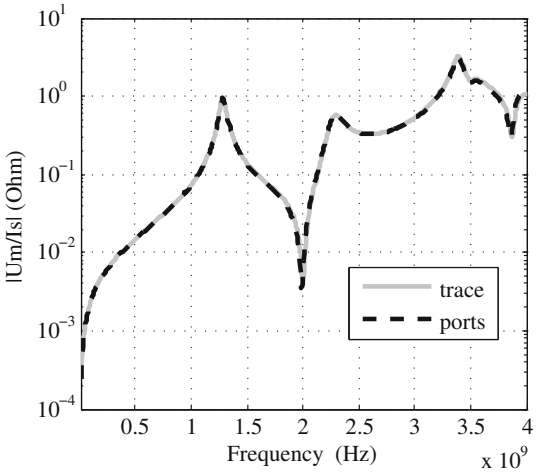
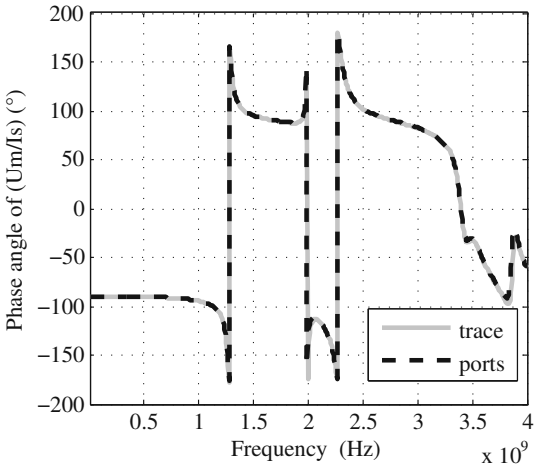


(a) Load: 0 Ohm, magnitude.



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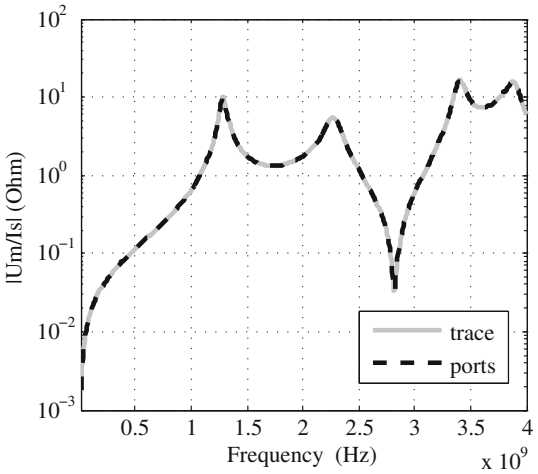
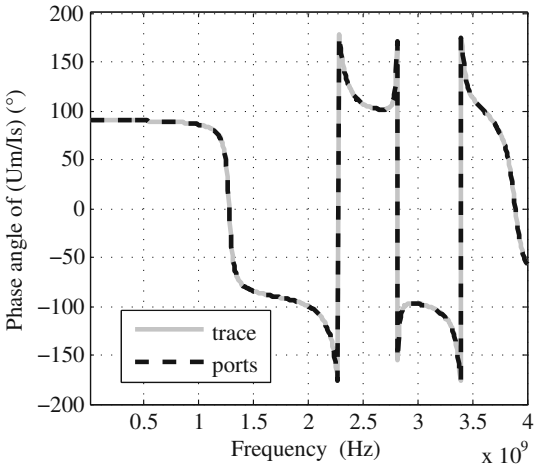


(c) Load: 1e9 Ohm, magnitude.



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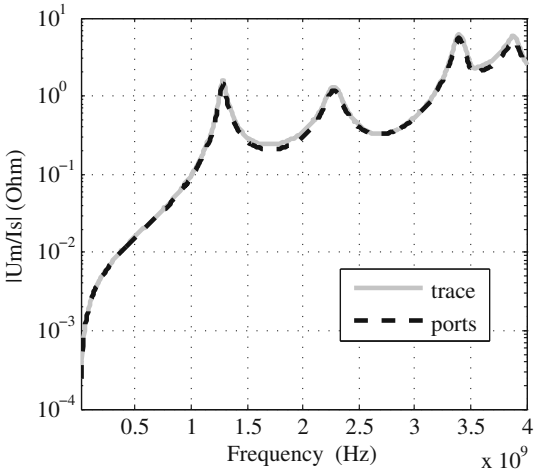
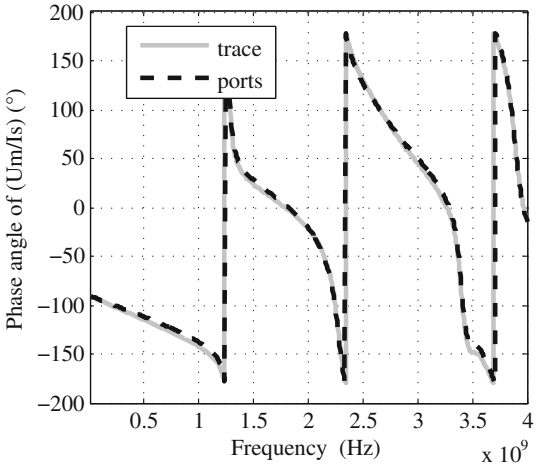


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.33: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm)) and the results obtained with (5.6), (5.9) and a HFSS model with ports. The enclosure height h=15mm.

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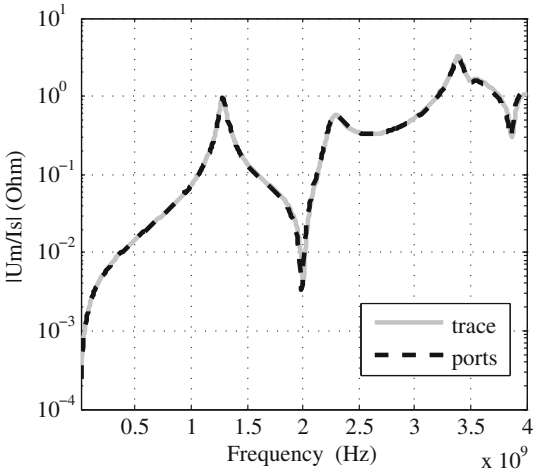

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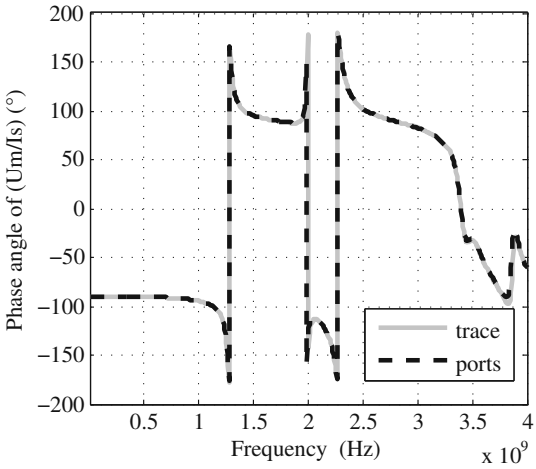
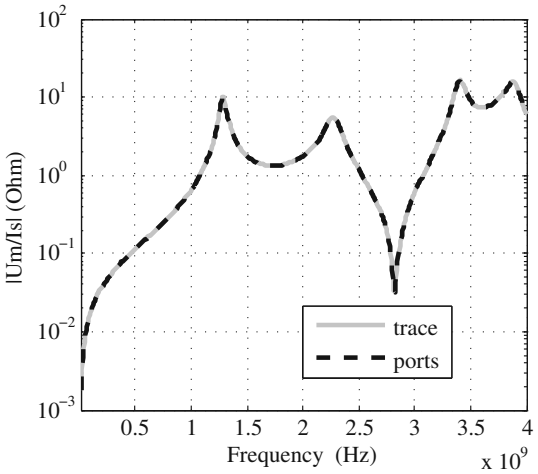


(b) Load: 0 Ohm, phase angle.



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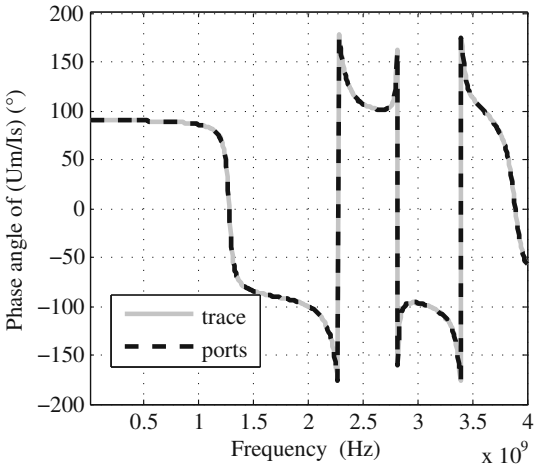
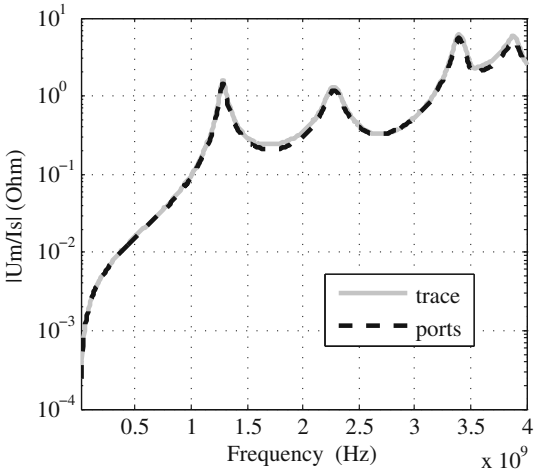
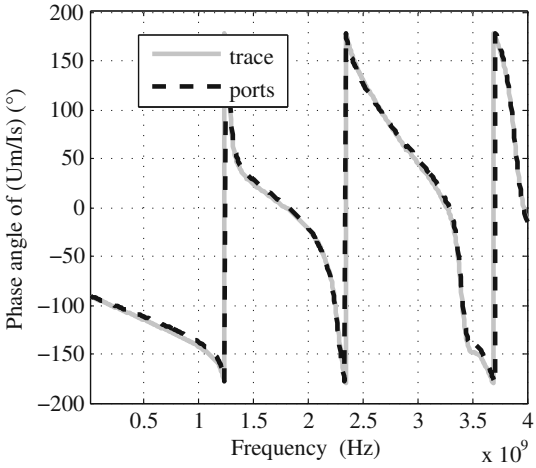


(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.34: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm)) and the results obtained with (5.6), (5.9) and a HFSS model with ports. The enclosure height h=15mm.

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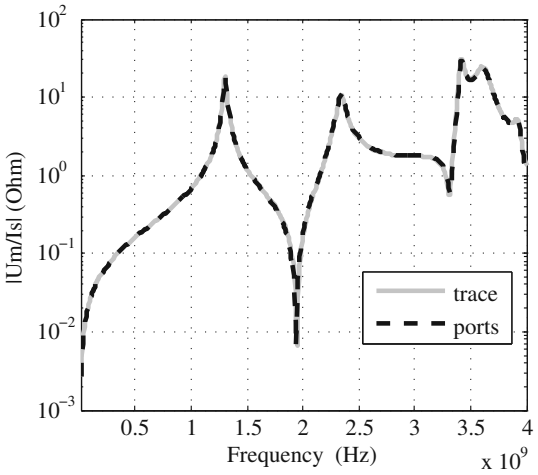
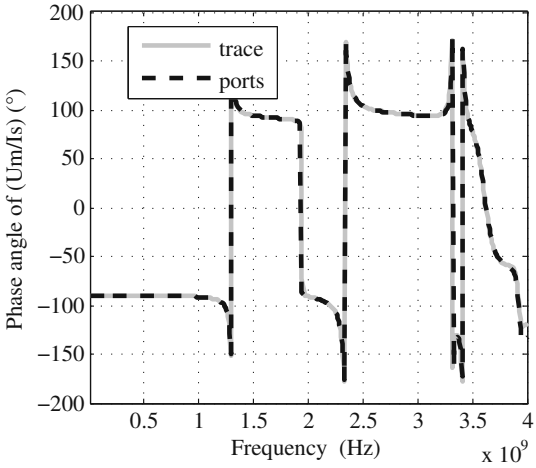
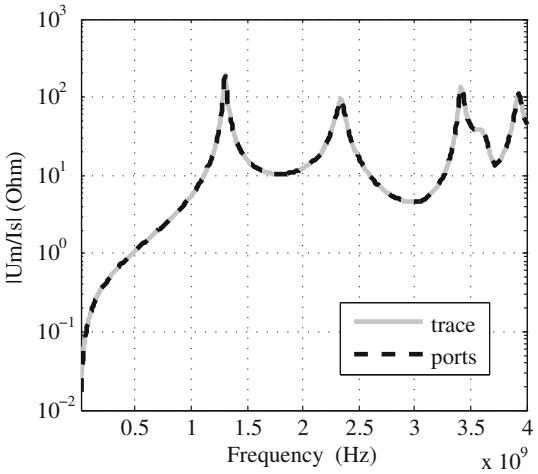


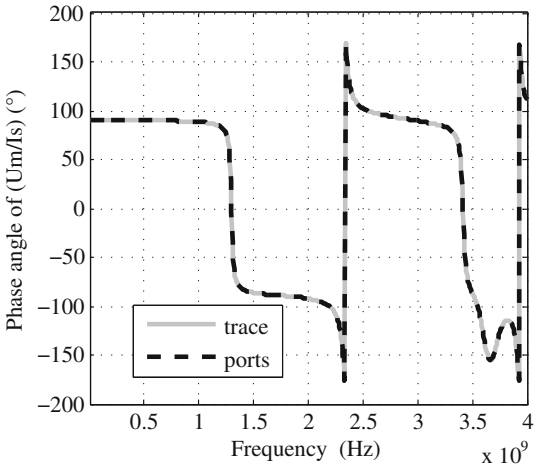
(a) Load: 0 Ohm, magnitude.



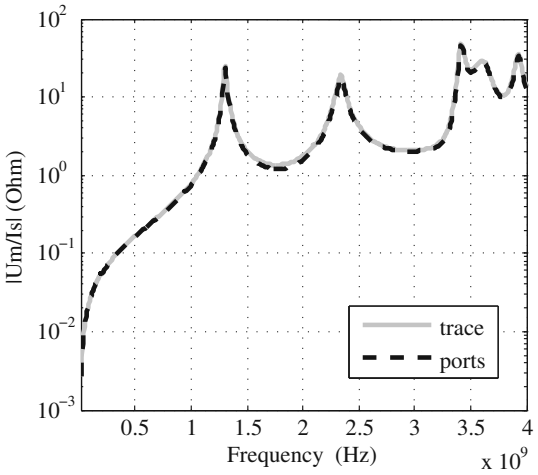
(b) Load: 0 Ohm, phase angle.



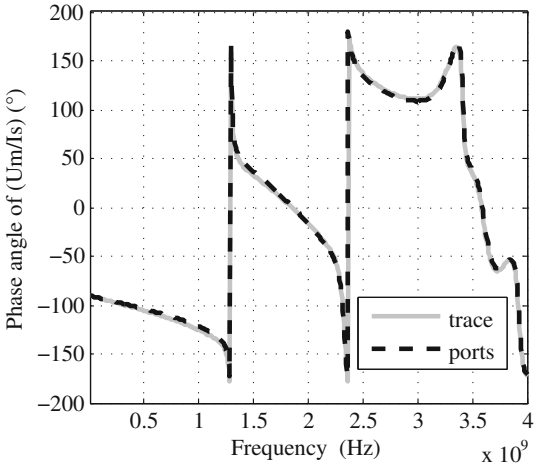
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.35: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm))and the results obtained with (5.6), (5.9) and a HFSS model with ports. The trace height is d=1.5mm.

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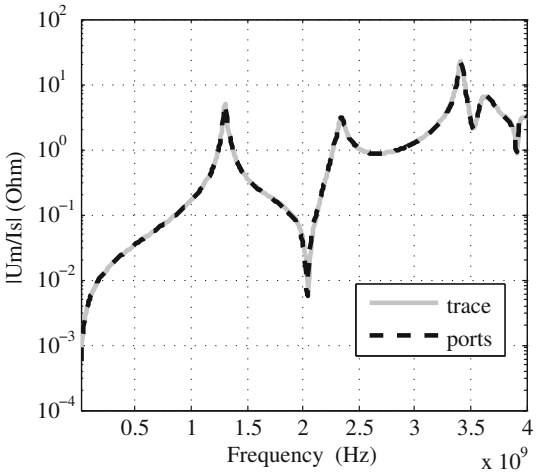

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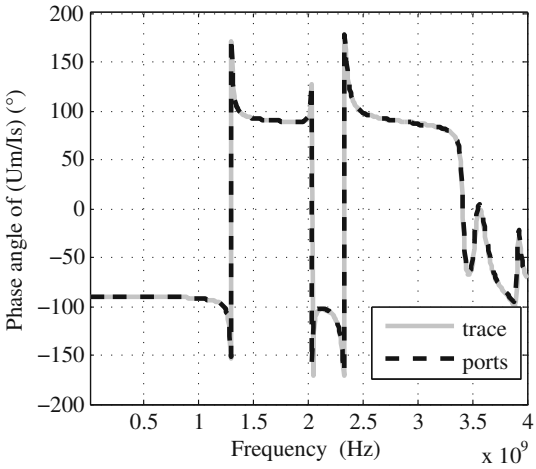
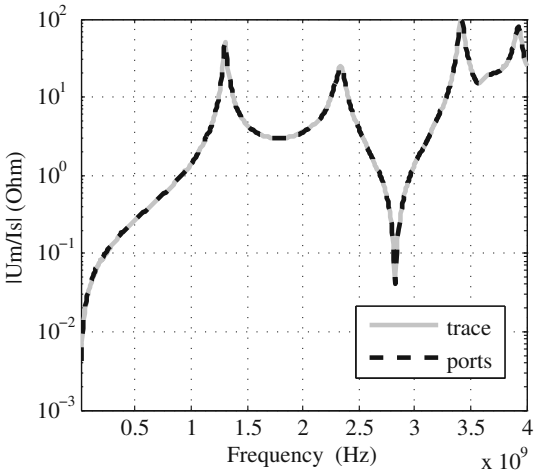
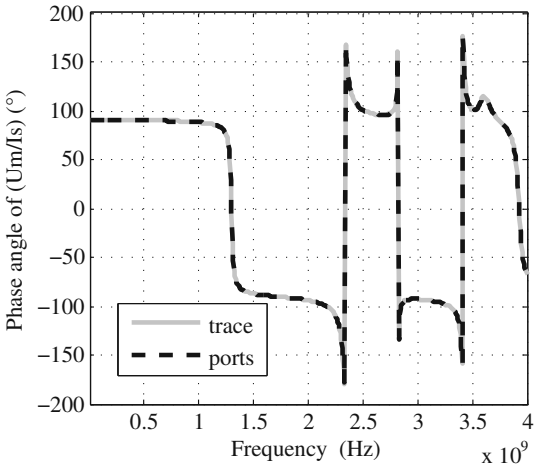


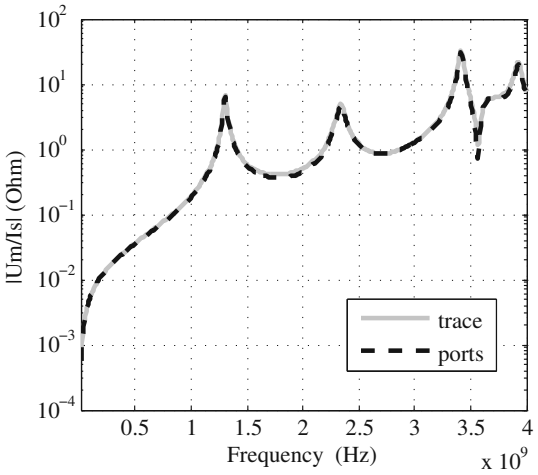
(b) Load: 0 Ohm, phase angle.



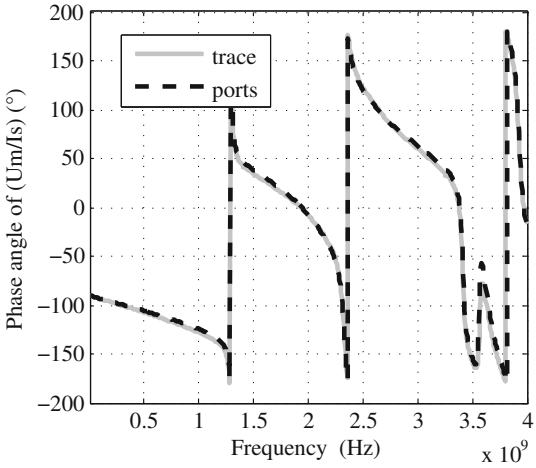
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.36: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm))and the results obtained with (5.6), (5.9) and a HFSS model with ports. The trace height is d=1.5mm.

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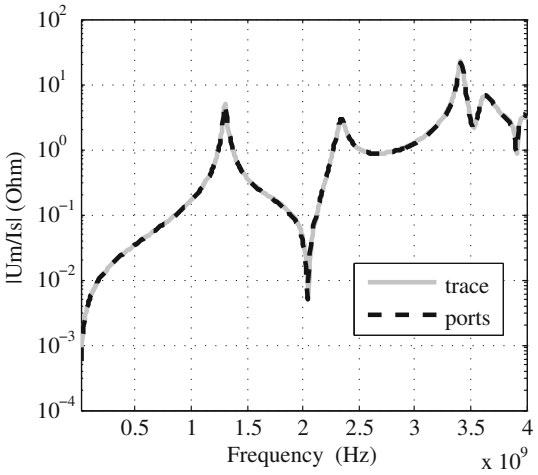
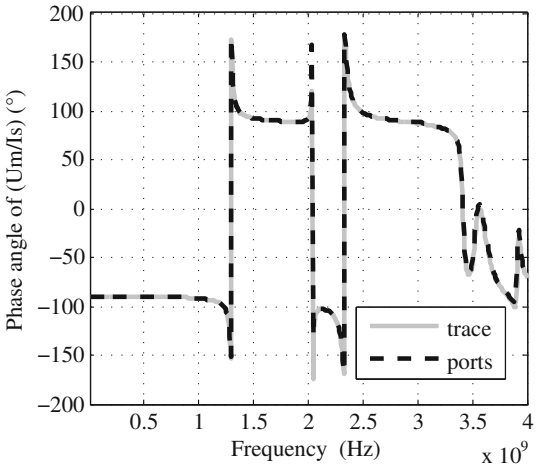
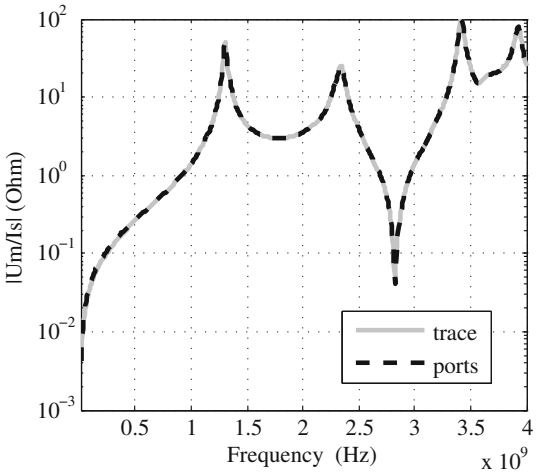


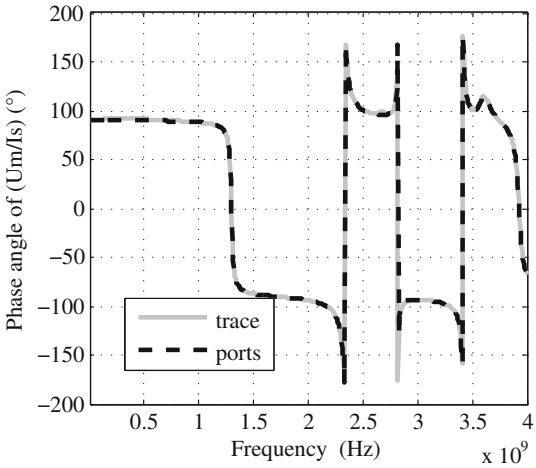
(a) Load: 0 Ohm, magnitude.



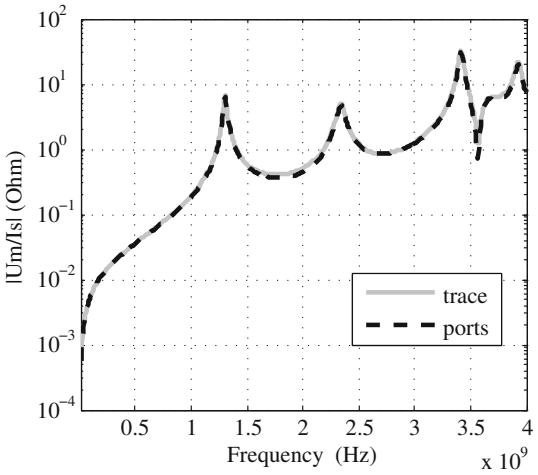
(b) Load: 0 Ohm, phase angle.



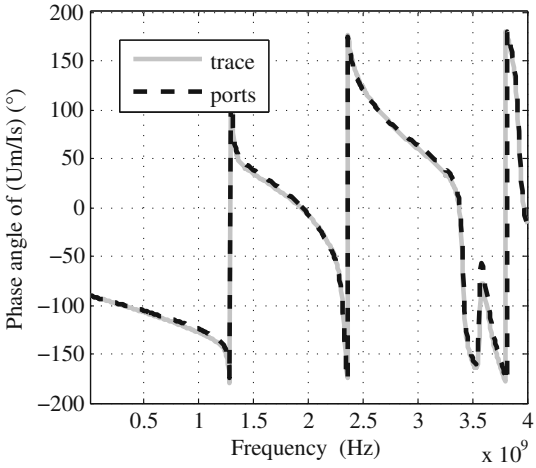
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.37: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm))and the results obtained with (5.6), (5.9) and a HFSS model with ports. The trace height is d=1.5mm.

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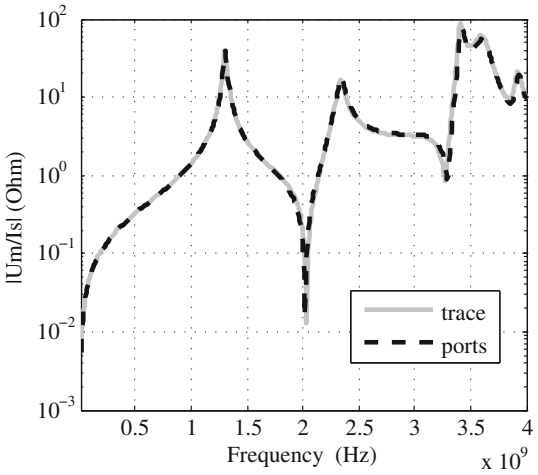
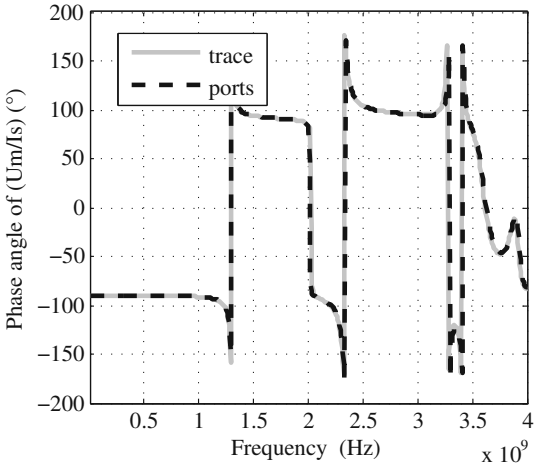
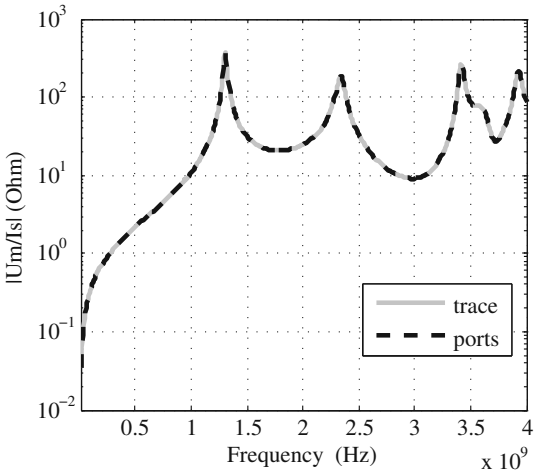


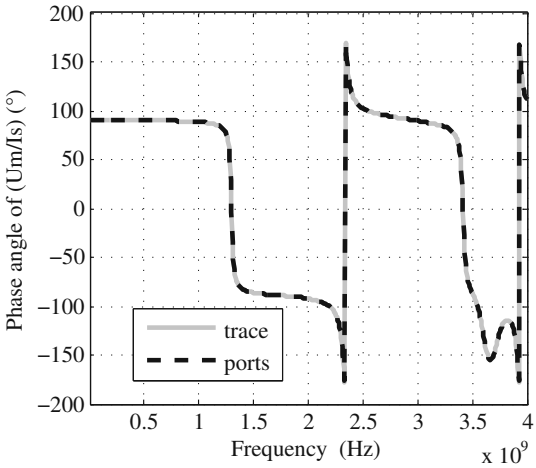
(a) Load: 0 Ohm, magnitude.



(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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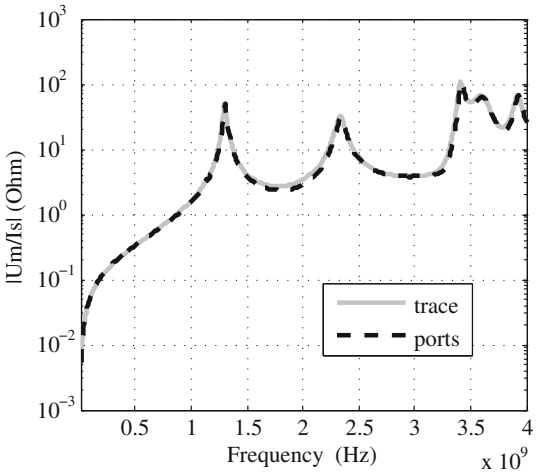
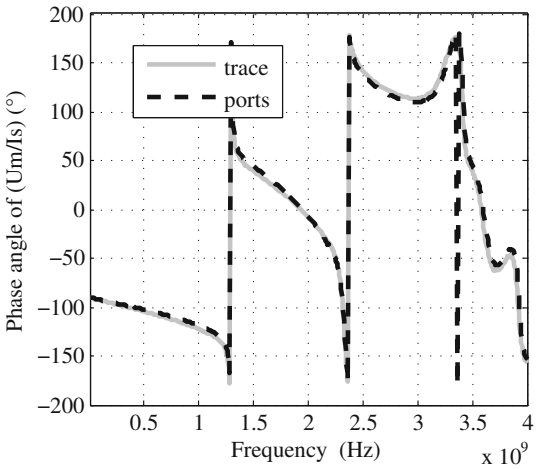


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.38: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm))to the results obtained with (5.6), (5.9) and a HFSS model with ports. The trace height is d=3mm.

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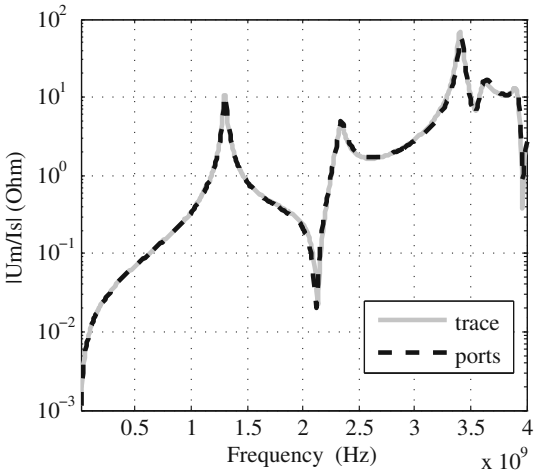

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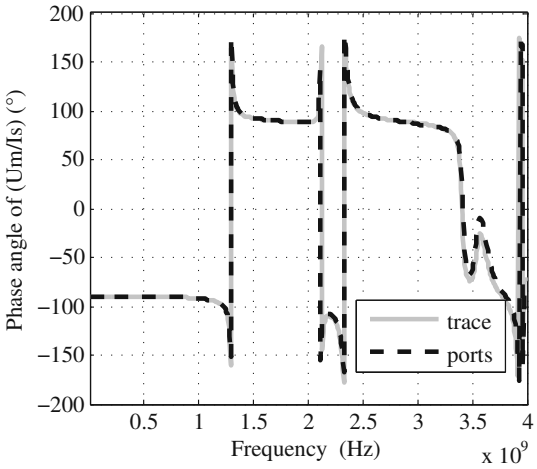
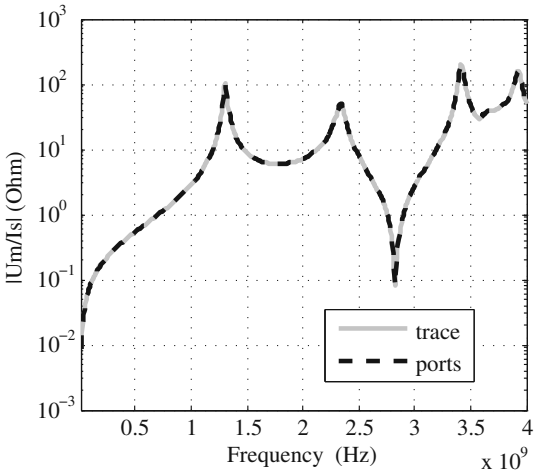
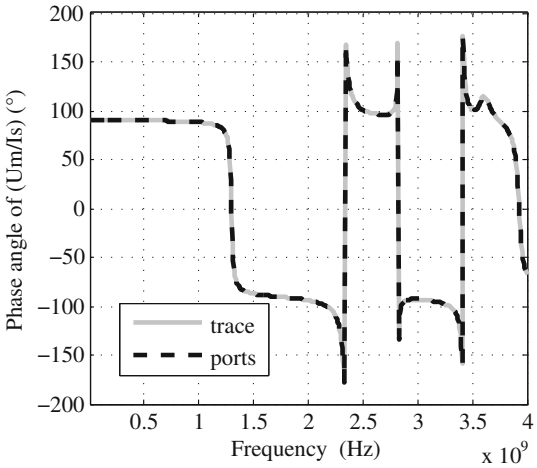


(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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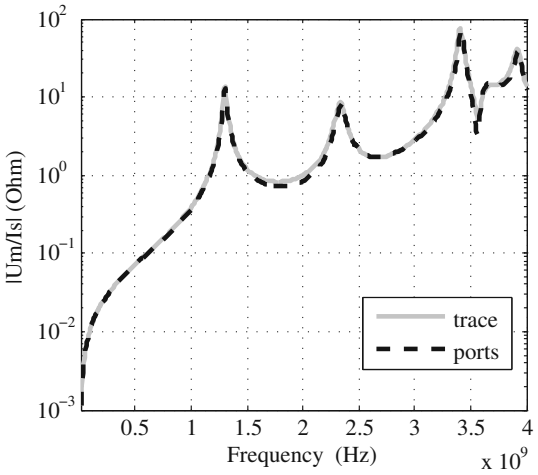
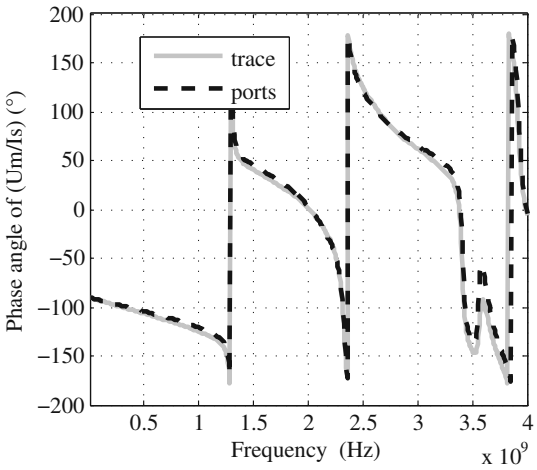


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.39: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm))to the results obtained with (5.6), (5.9) and a HFSS model with ports. The trace height is d=3mm.

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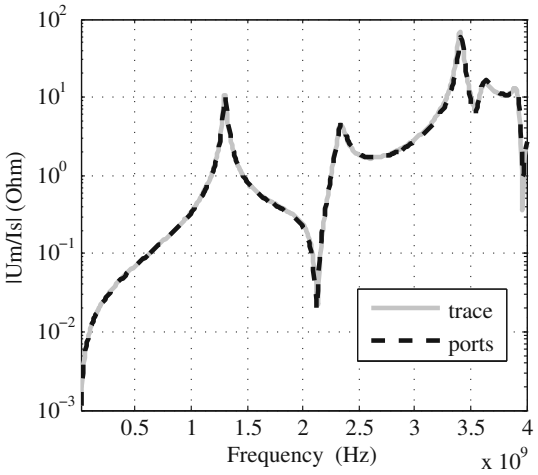
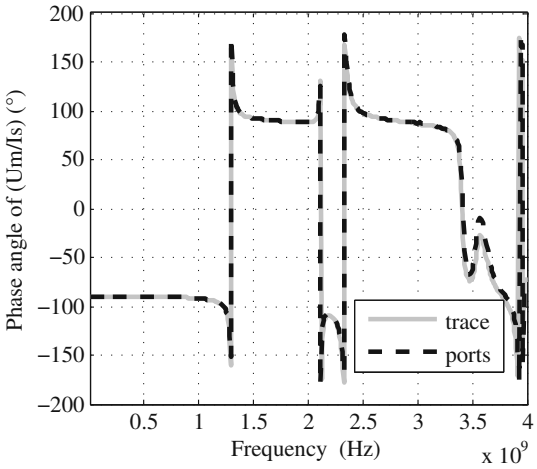
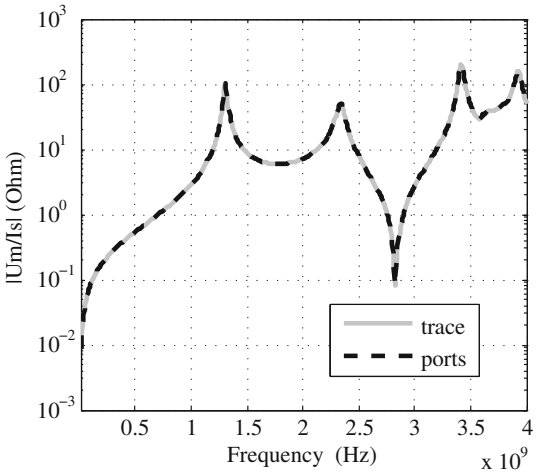


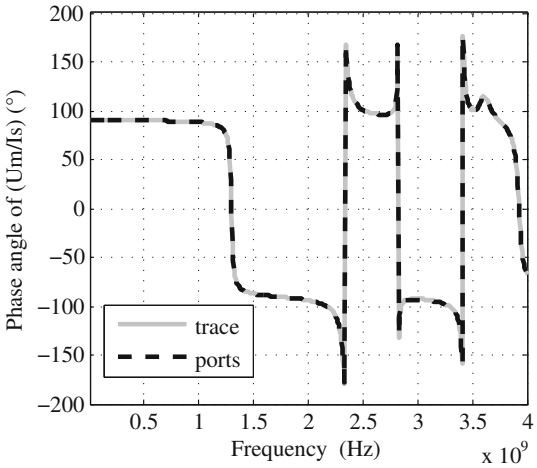
(a) Load: 0 Ohm, magnitude.



(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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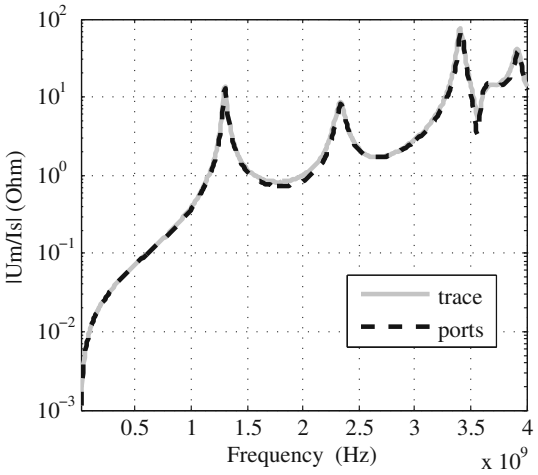
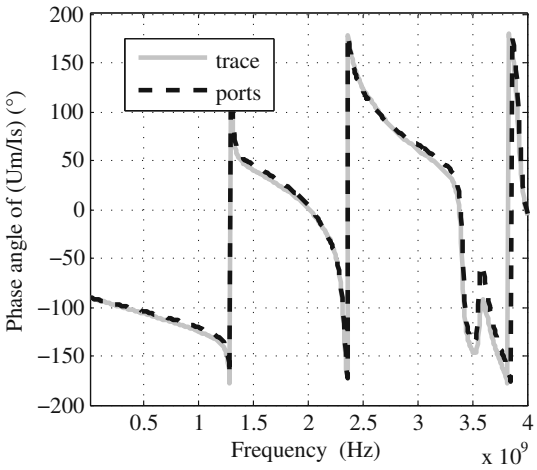


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.40: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm))to the results obtained with (5.6), (5.9) and a HFSS model with ports. The trace height is d=3mm.

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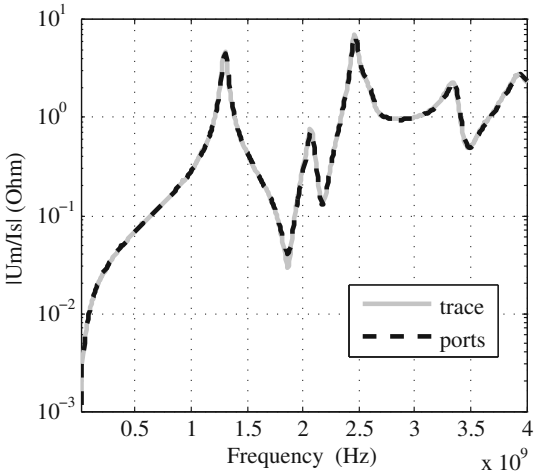
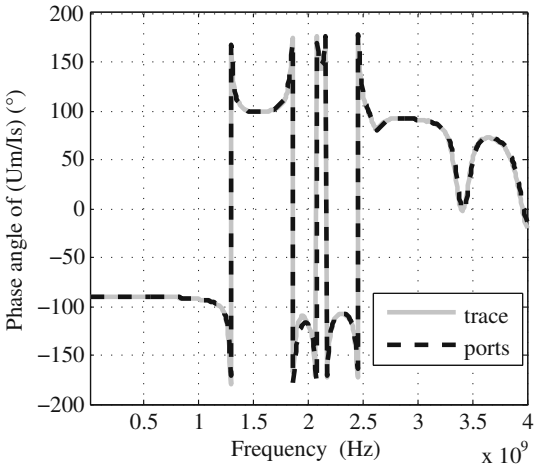
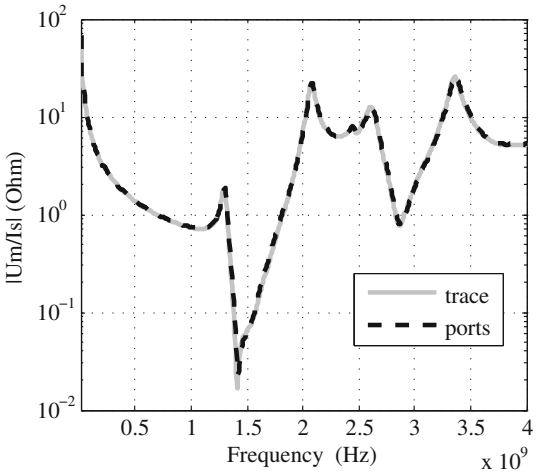


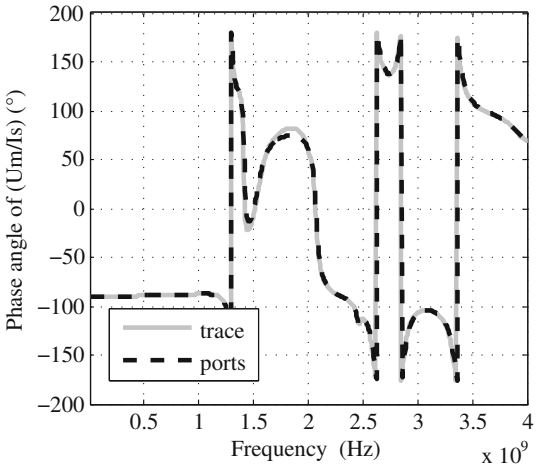
(a) Load: 0 Ohm, magnitude.



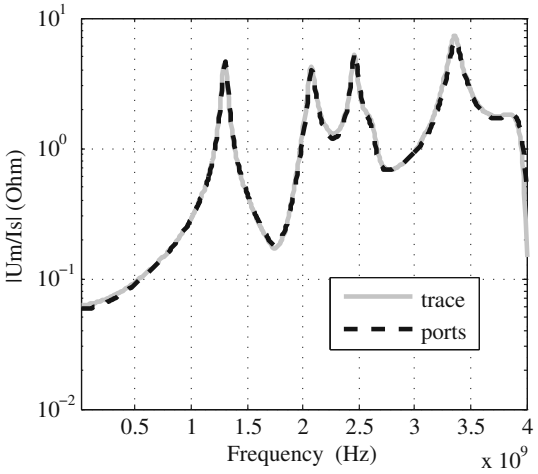
(b) Load: 0 Ohm, phase angle.



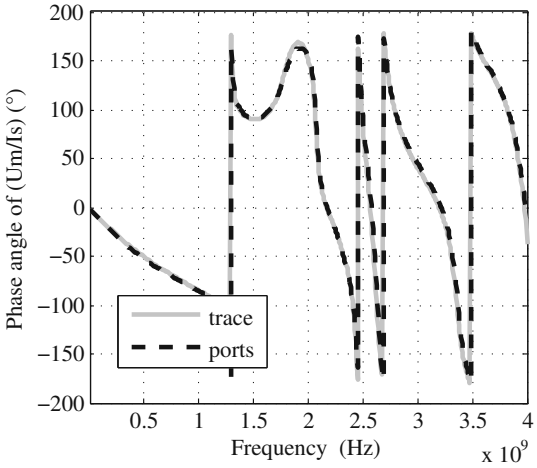
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.41: Transfer impedance from the trace source current to the slot measurement port at (67mm,104mm). Comparison of HFSS results from a model with a trace 5mm trace at position (67mm,50mm) to the results obtained with (5.6), (5.9) and a HFSS model with ports. The trace height is d=0.65mm.

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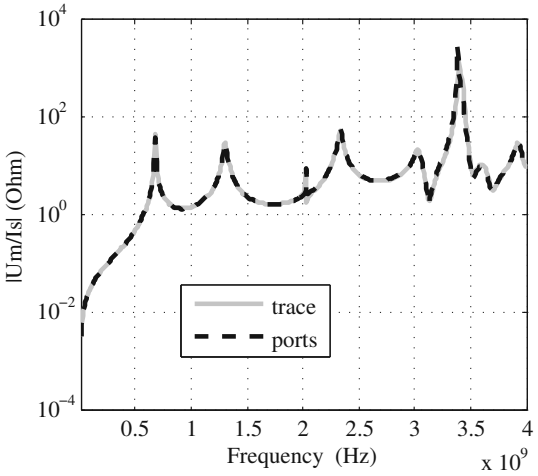
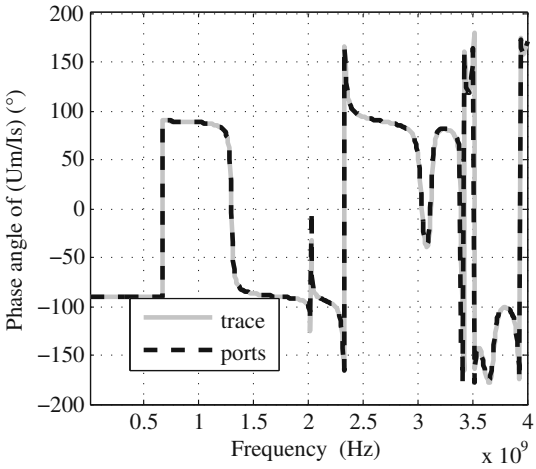
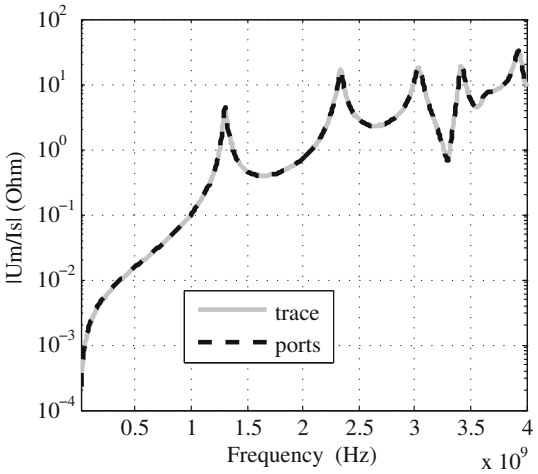


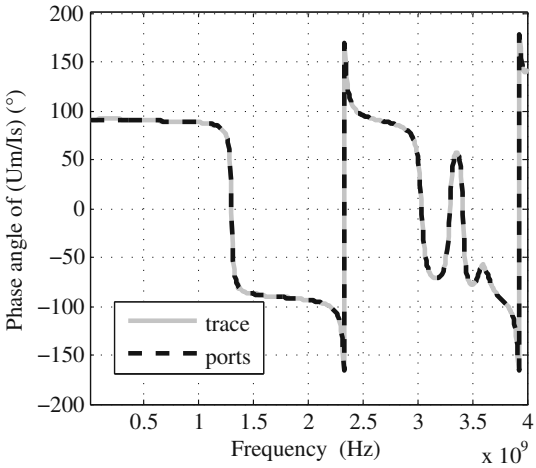
(a) Load: 0 Ohm, magnitude.



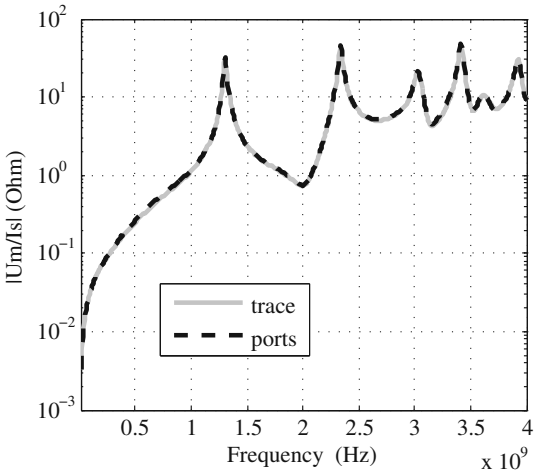
(b) Load: 0 Ohm, phase angle.



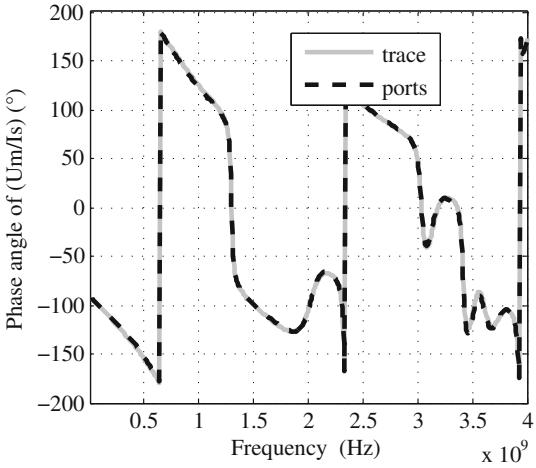
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.42: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). Comparison of HFSS results from a model with a trace (Figure 5.7(a)) and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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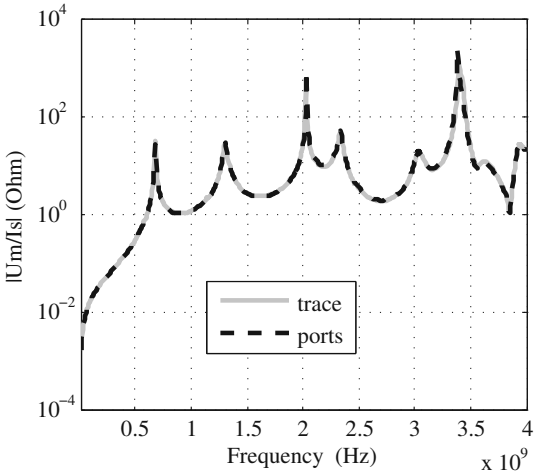
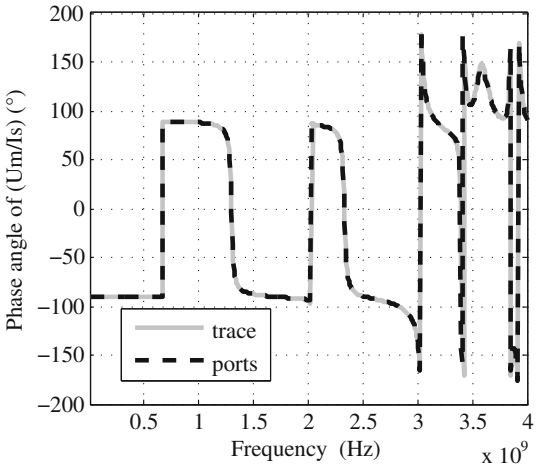
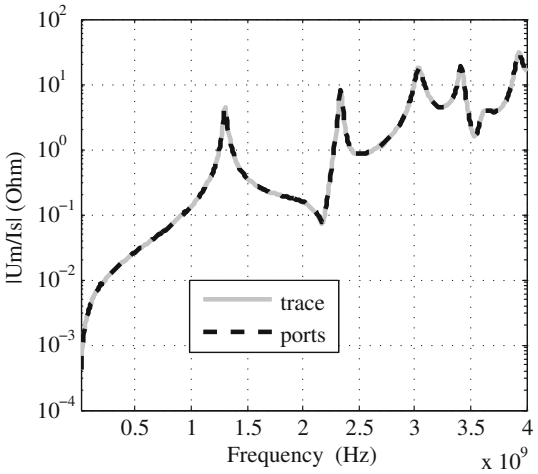


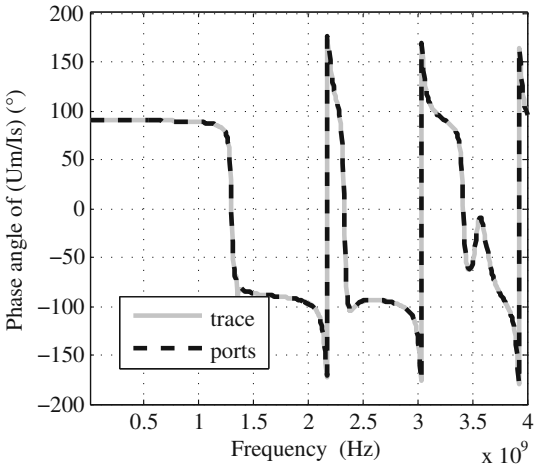
(a) Load: 0 Ohm, magnitude.



(b) Load: 0 Ohm, phase angle.



(c) Load: 1e9 Ohm, magnitude.



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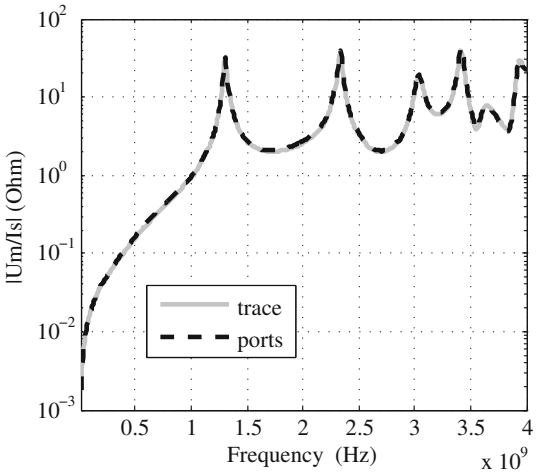
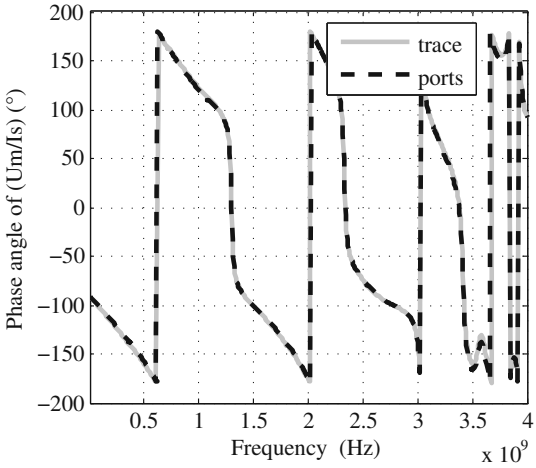


(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.43: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). Comparison of HFSS results from a model with a trace (Figure 5.7(a)) and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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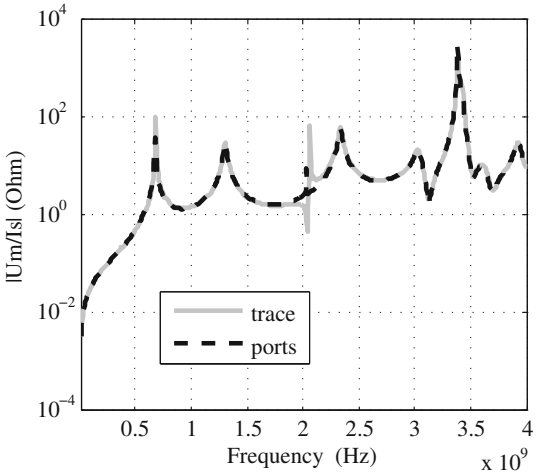

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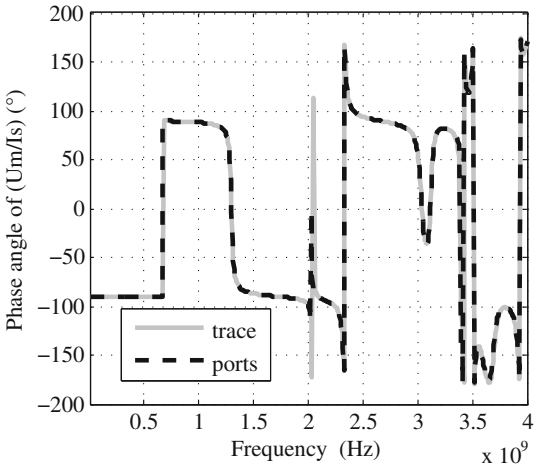
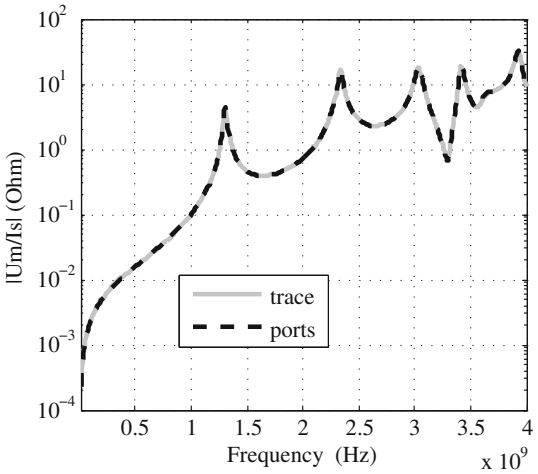
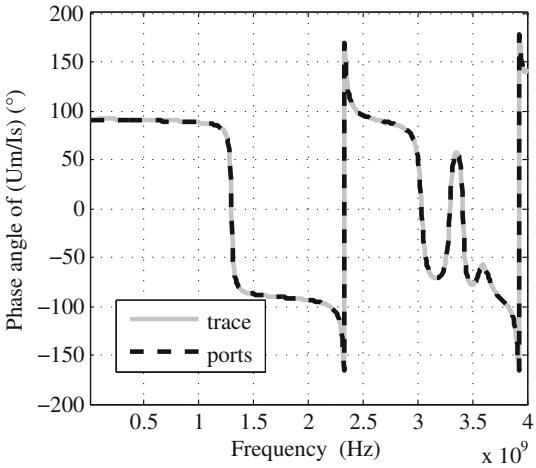


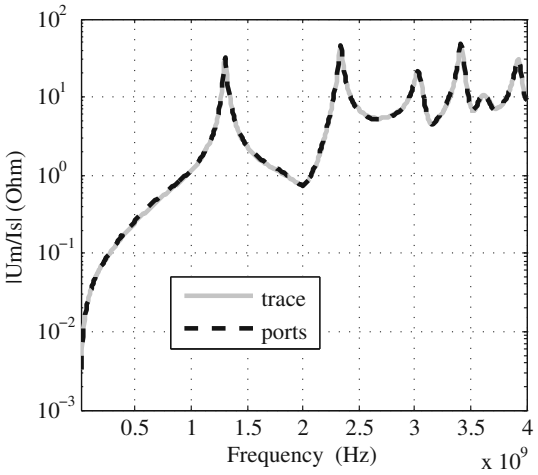
(b) Load: 0 Ohm, phase angle.



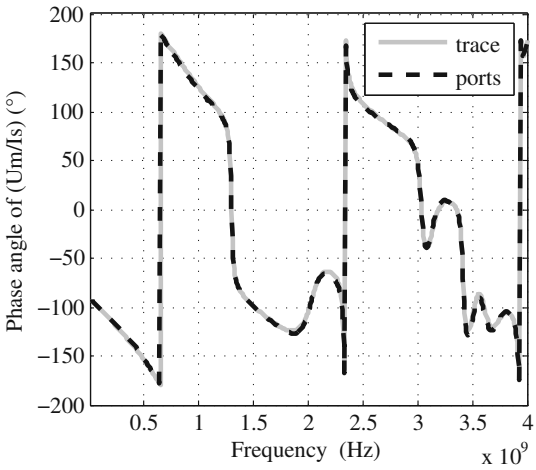
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.44: Transfer impedance from the trace source current to the slot measurement port at (10mm,104mm). Comparison of HFSS results from a model with a trace (Figure 5.7(b)) and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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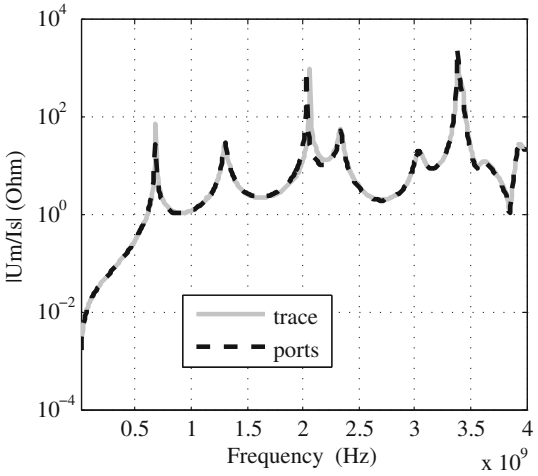
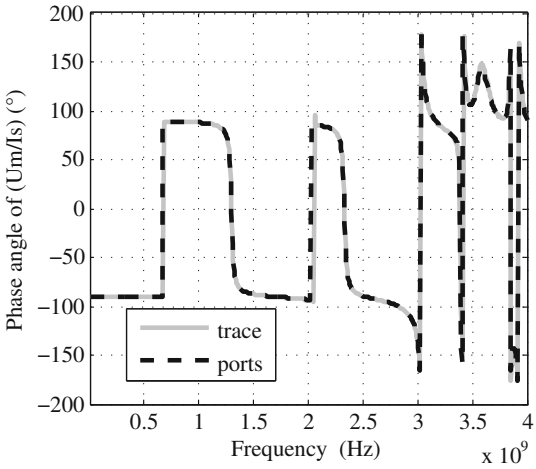
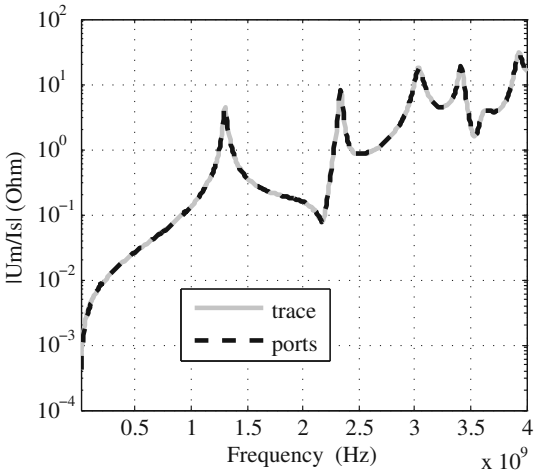


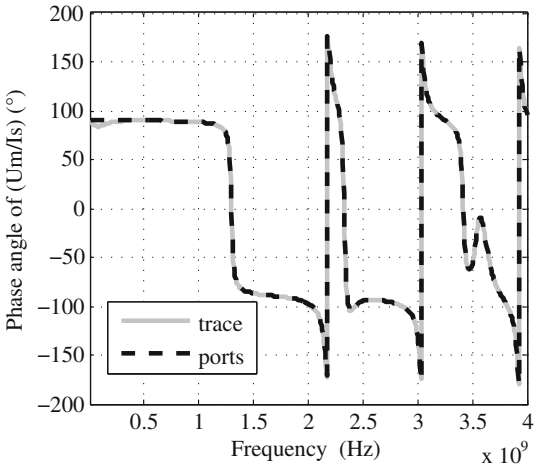
(a) Load: 0 Ohm, magnitude.



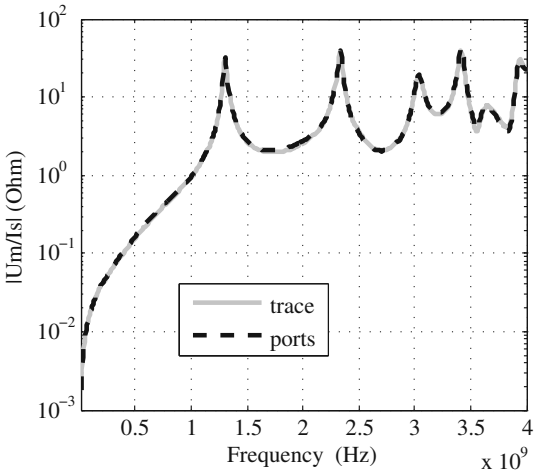
(b) Load: 0 Ohm, phase angle.



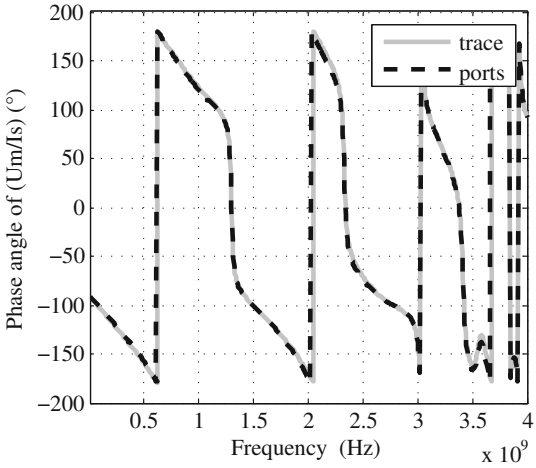
(c) Load: 1e9 Ohm, magnitude.



(d) Load: 1e9 Ohm, phase angle.



(e) Load: 50 Ohm, magnitude.



(f) Load: 50 Ohm, phase angle.

Figure A.45: Transfer impedance from the trace source current to the slot measurement port at (124mm,104mm). Comparison of HFSS results from a model with a trace (Figure 5.7(b)) and the results obtained with (5.6), (5.9) and a HFSS model with ports.

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Own Publications

Christian Poschalko and Siegfried Selberherr. Calculation of the Radiation from the Slot of a Slim Enclosure with a Cavity Resonator Model. In *Proceedings of the Asia-Pacific Symposium on Electromagnetic Compatibility*, pages 622-625, May 2008

Christian Poschalko and Siegfried Selberherr. Domain Separation with Port Interfaces for Calculation of Emissions from Enclosure Slots. In *IEEE Symposium on Electromagnetic Compatibility*, pages 1-6, August 2008

Christian Poschalko and Siegfried Selberherr. Radiated Emission from the Slot of a Slim Cubical Enclosure with Multiple Sources Inside. In *EMC-EUROPE 2008, International Symposium on Electromagnetic Compatibility*, pages 109-114, September 2008

Christian Poschalko and Siegfried Selberherr. Cavity Model for the Slot Radiation of an Enclosure Excited by Printed Circuit Board Traces With Different Loads. In *IEEE Transactions on Electromagnetic Compatibility*, volume 52, pages 18-24, February 2009

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Curriculum Vitae

Education

since 2005	Study for Doctorate of Technical Sciences, Institute for Microelectronics, Technische Universität Wien
1990 - 1995	Study of Electronics, Technische Universität Wien Field: Industrial Electronics and Control Engineering. Diploma Thesis: *Leistungsmessgerät für eine Plasmaaudiofrequenzanlage*
1985 - 1990	HTBLA Wien 22 Electrotechnik, (excellent success)

Professional Experience

since 2004	EMC Simulation, Robert Bosch AG, Vienna, Austria, *Start up with EMC-Simulation for the Bosch business unit DS (Diesel Systems) in 2004; EMC simulation for automotive electronics and development of simulation methods. Management of the Austrian part of the EUREKA research project PARACHUTE. Since 2008 at the Bosch unit DGS (Diesel and Gasoline Systems)*
1999 - 2004	Development Engineer, Robert Bosch AG, Vienna, Austria, *Test specifications and software development for embedded systems. Specification process automation by a new programming language, implemented to an ORACLE® hardware database*
1996 - 1999	Software Development Engineer, Fa. Ernst Krause & Co., Austria, *Programming of PLC and CNC controls for transfer machines and flexible processing centers; Control software architecture*

Other Activities

1995 - 1996	Civil Service, Apoplexy and Rheumatism Rehabilitation Hospital, Laab im Walde, Austria

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