Bias-tunable temperature coefficient of resistance in Ge transistors

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ABSTRACT

Ge-based bolometers are widely used for near-infrared detection for a broad range of applications such as thermography or chemical analysis. Notably, for the thermometers used in bolometers, integration, scaling, and sensitivity as well as functionality are of utmost importance. In this regard, Ge exhibits a favorable temperature sensitivity due to the relatively low bandgap and a high intrinsic charge carrier concentration. In this work, we demonstrate a nanoscale thermometer for bolometric applications on the base of Ge-on-insulator nanosheets with monolithic Al source/drain contacts envisioned for future wafer-scale integration. Importantly, electrostatic gating of the nanosheets allows the operation as a Schottky barrier field-effect transistor, providing tunability of the energy landscape and the involved charge carrier injection in interaction with the metal-semiconductor junctions. In this approach, the top-gate electrode and drain contact are connected, thus resembling a two-terminal device with bias-tunable temperature coefficient of resistance (TCR) values between 0%/K and −3.8%/K in the temperature range of T = 125–150 K. Moreover, in this configuration, even at room temperature, a maximum TCR value of −1.6%/K is achieved. The bias-tunable TCR exhibited in these devices may enable advanced concepts for room temperature bolometric applications and allow co-integration with nanoelectronics.

Till now, passive Ge bolometers are widely used for infrared (IR) detection as Ge offers an excellent temperature coefficient of resistance (TCR) over a wide temperature range.[1–3] Importantly, Ge features a relatively small bandgap, approximately half of that of Si, and a high intrinsic charge carrier concentration three orders of magnitude higher than that of Si. In terms of the temperature influence on the bandgap, $E_g = E_0 - \alpha T^2/(T + \beta)$ can be used to evaluate the temperature-dependent bandgap, where E_g is the indirect energy gap, E_0 is its value at 0 K, and α and β are constants.[4] In this consideration, the influence on the bandgap is described by dilatation of the lattice.[5] Thereof, the bandgap of Ge with $E_g = 0.74$ eV at 0 K results in a decrease by 16% to $E_g = 0.62$ eV at 400 K. In comparison, the bandgap of Si merely changes by 6% in the considered temperature range (values from Ref. 4). Especially, Schottky barriers (SBs) highly profit of the temperature dependent bandgap, as it is reduced at higher temperatures and, therefore, results in lower barriers supporting the injection of charge carriers, which is enhancing the temperature-sensitivity. In general, Ge is compatible with modern complementary metal-oxide-semiconductor (CMOS) technology and can be processed with common processing techniques at reasonable costs. Particular Ge-based bolometers require complex fabrication methodologies[3,6] but show remarkable TCR values between −1 and −6%/K, depending on doping and crystallinity.[2,7,8] Another fact to consider is that many Ge-based thermometers are often limited to operation in the liquid-He ($\approx$ 4 K) temperature regime.[9,10] Remarkably, vapor–liquid–solid (VLS) grown Ge nanowires (NWs), due to their small thermal mass, are of high interest for thermometers in bolometric applications. Bartmann et al. have already demonstrated the realization of an intrinsic Ge NW based microbolometer with a TCR value of −1.7%/K at room temperature.[11] However, due to limitations in the integration and exact placement of NWs, the industrial and large-scale integration of NWs is limited.[12] Therefore, top-down approaches based on Ge-on-insulator (GeOI) nanosheets (NSs) provide a promising solution to overcome the difficulties of device integration as well as ensure geometry freedom without losing the relevant thermometer properties. Additionally, NSs allow one to engineer the thermal conductance between the Ge and metal contacts by using appropriate NS widths and/or thicknesses. Moreover, GeOI even offers the possibility to fabricate parallel wires for enhanced applications, e.g., increased currents and/or logic circuits.[13,14] For applicable operation, well-defined contacts to the

semiconductor NSs are of high importance. In this respect, intruded Al contacts provide abrupt metal-semiconductor junctions, i.e., Schottky contacts.[15] An important aspect of Schottky junctions is their ability to be electrostatically tuned by placing a gate atop the semiconductor channel and overlapping the metal-semiconductor junctions, thus filtering the injected charge carriers, i.e., holes or electrons, by applying a negative or positive gate voltage, respectively.[16,17] Therefore, using a top-gated metal–semiconductor–metal heterostructure, a so-called Schottky barrier field-effect transistor (SBFET) is realized.[18,19] In this work, such a Ge SBFET is operated as a two-terminal device by electrically connecting the gate and drain electrodes. In this configuration, a tunable TCR and, consequently, its usability as a thermometer for bolometric applications is demonstrated and investigated in the temperature range between 77.5 and 400 K. Importantly, the unique metal–semiconductor–metal heterostructure inherently constitutes two electrostatically tunable Schottky junctions, which, in consequence, enable this remarkable tunability feature. Having a tunable TCR further allows us to operate the device in dedicated TCR regimes for the desired application. Importantly, most transistor applications require a TCR of ideally 0%/K to ensure thermal stability, whereas thermometers shall feature high TCR values. Therefore, TCR tunability allows the co-integration of thermometers and transistors with the same architecture and material system. In the past, Schottky diodes for bolometric applications were already proposed[20] but are limited to Si-based technology with TCR values in the regime of -2%/K at room temperature.[20,21] However, the use in a top-down Ge-based (SB)FET is unexplored so far.

The starting material for the proposed nanoscale Ge thermometer was a GeOI wafer with a ≈ 75 nm thick (100) oriented nominally intrinsic and not intentionally doped Ge device layer on top of a 150 nm thick buried oxide layer and Si handle wafer. Thereof, NSs were patterned with a Ge device layer of 20 nm and widths ≈ 265 nm by e-beam lithography (EBL) and reactive ion etching (RIE). Subsequently, the native Ge_xO_y was desorbed preventing the formation of Ge oxides, thus promoting a more stable device operation by reducing the number of trap states.[22,23] The desorption of the native oxide layer is achieved in ultra-high vacuum (1×10^{-10} mbar base pressure) at 600 °C for 30 min. Entire desorption of the native oxide is confirmed by x-ray photoemission spectroscopy (XPS) analysis on a Ge(100) test substrate [cf. Fig. 1(d)]. As gate oxide, 11 nm Al_2O_3 was deposited by atomic layer deposition (ALD). Afterward, Al source/drain pads were fabricated by optical lithography, selective oxide removal, sputter deposition, and liftoff techniques. Finally, having Al contacted to the Ge NSs, rapid thermal annealing (RTA) at 673 K was performed to initiate the metal-semiconductor exchange mechanism, which was thoroughly investigated by Wind et al.[15] Eventually, it needs to be considered that the channel length shall be well above the mean free path of Ge (>45 nm) to prevent a high contribution of temperature independent ballistic charge carriers, inhibiting thermometer applications.[24] In this sense, channel lengths between 400 and 1000 nm are targeted. In a last step, EBL and evaporation of Ti/Au (10 nm/100 nm) were utilized to fabricate a gate atop the metal-semiconductor junctions and Ge channel, which finally assembles a SBFET. Note that for proper electrostatic gating capabilities of the semiconductor energy bands, a sufficient overlap of the metal-semiconductor junctions needs to be ensured.[25] Figure 1(a) shows a false-colored scanning electron microscope (SEM) image of the fully
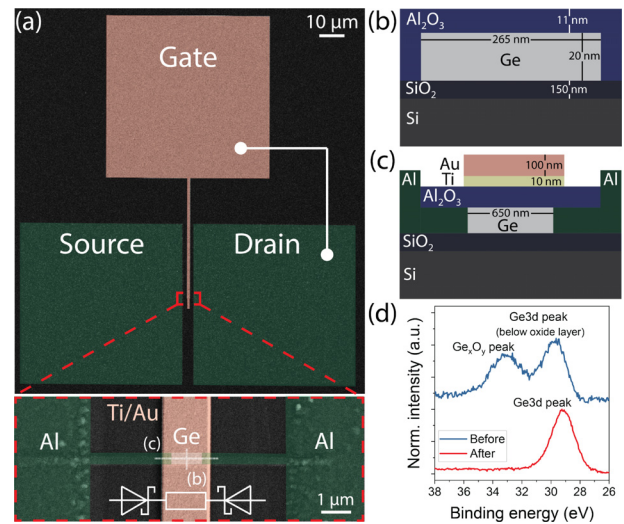

FIG. 1. (a) A colored SEM image of the SBFET architecture with an indicated bonding wire between the gate and drain electrodes. The lower image depicts a zoomed-in view of the SBFET. The two Schottky diode and resistor symbols illustrate the involved Al–Ge junctions and Ge channel, respectively. (b) and (c) show the vertically and horizontally schematic cross-section cuts through the device stack (dimensions are not in scale). (d) shows XPS data before (blue) and after (red) Ge_xO_y desorption.

featured device. Figures 1(b) and 1(c) show a schematic vertical and horizontal cross section view of the SBFET material stack. Finally, the gate and drain electrodes were bonded to obtain a two-terminal device promoting a diode characteristic (cf. Fig. 2). The thereof realized device consists of two electrostatic tunable Schottky junctions with Al being the anode and Ge being the cathode at the metal-semiconductor junctions and, thus, allows for similar thermometer mechanisms as proposed in other Schottky diode based thermometers for bolometers.[21] However, due to the electrostatic gating capabilities, different device operation modes can be set, further functionalizing the proposed device concept and even allowing suitability for nanoelectronic applications requiring a TCR of ideally 0%/K.

First, the I–V characteristic of the gate- and drain-wired SBFET is analyzed at room temperature. Figure 2 shows the corresponding plot with sweeping $V_D = V_{TG}$ from 2.5 to -2.5 V and setting the source potential V_S to 0 V. Due to the incorporated Schottky junctions of the Al–Ge–Al heterostructure, a diode characteristic is evident [cf. Fig. 1(a)]. In contrast, operating the device as a SBFET (without wired gate and drain electrodes), the device does not exhibit a diode characteristic but shows a quasi-ambipolar transfer characteristic.[19] This can be attributed to the fact that the energy band and drain potential are bent synchronously, only allowing injection of charge carriers from one Schottky junction (cf. insets in Fig. 2). Additionally, using the wired gate-drain configuration, a dedicated symmetry axis at $V_D = V_{TG} = 0$ V is obtained. Note that the forward direction occurs in the hole dominated p-branch ($V_D < 0$ V), whereas the reverse direction occurs in the electron dominated n-branch ($V_D > 0$ V). This behavior can be attributed to strong Fermi level pinning of Al close to the valence band of Ge.[26] Thus, the Schottky barrier for holes is relatively low (quasi-ohmic), whereas electrons need to overcome a
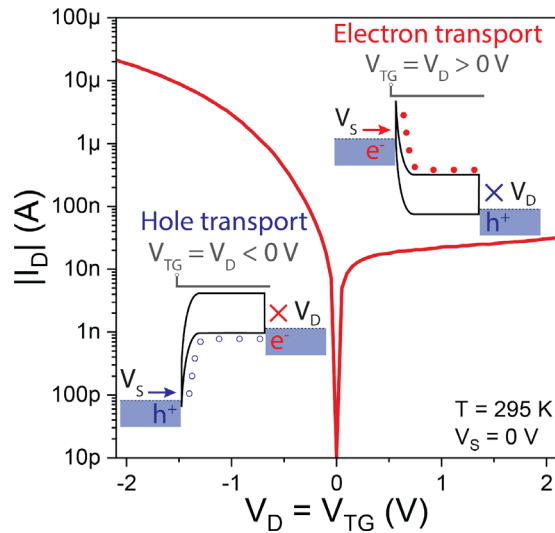
FIG. 2. I–V characteristic illustrating the forward diode characteristic in the hole dominant regime ($V_D = V_{TG} < 0\,V$) and current saturation (diode reverse operation) in the electron dominant regime ($V_D = V_{TG} > 0\,V$). The insets schematically illustrate the simplified bias-induced band bending mechanism for both charge carrier transport mechanisms. The empty blue dots as well as filled red dots illustrate the hole and electron transport, respectively. Note that the injection of the opposed charge carrier type is inhibited.

relatively high Schottky barrier. Note that the top-gate covering the Al–Ge junctions and Ge channel, as well as the drain potential, electrostatically bends the incorporated energy landscape and, therefore, tunes the characteristic of the Schottky junctions (cf. insets in Fig. 2). Thereof, two transport mechanisms need to be considered: thermionic emission (TE), which is the injection of charge carriers overcoming the Schottky barrier, and field emission (FE), which is the charge carrier injection via tunneling through a thinned barrier, induced by strong band bending ($|V_D| \gg 0\,V$). Due to the Fermi level pinning of Al close to the valence band of Ge, the current in the hole dominant regime increases steadily due to TE, offering an efficient charge carrier injection process for holes. Further increasing the bias, FE is getting the dominant contributor in consequence to a thinner barrier.[19] Importantly, in this regime merely the opposite Schottky junction (drain potential) needs to be considered, as the injecting Schottky contact (source potential) is fully transparent. In this respect, the hole current is also highly influenced by the corresponding width of the space charge region, which can also be tuned by material and dimension properties of the device, as the gate geometry, oxide thickness, and/or oxide material are highly impacting the tunneling probability.[19] In contrast, operating the device in the electron dominant regime, TE is the main contributor, as the barrier thickness is too large within the observed voltage regime and, thus, hinders efficient tunneling. In the evaluated device, the current remains relatively stable in the range between $V_D = V_{TG} = 0.5$ and $2\,V$ with current values of 18 and 32 nA, respectively. Accordingly, this stable regime further supports the dominance of the Schottky barrier experienced by electrons, as tuning the bands does not necessarily lead to higher currents. Remarkably, utilizing the electrostatic gating capabilities, the effective Schottky barrier height, i.e., the activation energy, can be tuned and, thus, allows precise

tuning of the involved transport mechanisms, i.e., TE and/or FE.[19] In respect to thermometers, TE is a highly temperature dependent transport mechanism, which needs to be accessed in terms of achieving high TCR values.

Figure 3 shows I–V characteristics at different temperatures ranging between 77.5 and 400 K. Note that currents in the n-branch at low temperatures, i.e., T = 77.5–100 K, cannot be properly resolved as they are below the resolution limit of the used measurement equipment ($\approx 100\,fA$). First, considering the p-branch, it can be deduced that at low bias voltages, a temperature dependency is evident, which can be attributed to dominant TE charge carrier transport. However, approaching $V_D = V_{TG} = -2\,V$, FE gets more dominant due to a higher tunneling probability induced by stronger band bending and in consequence a thinner barrier. Additionally, the temperature dependency vanishes in strong hole accumulation because FE and its transmission probability is temperature independent.[19] In contrast, electrons experience a dedicated Schottky barrier and also a much thicker barrier width up to the evaluated regime of $V_D = V_{TG} = 2\,V$. Therefore, TE is the only injection mechanism contributing to charge carrier transport in the n-branch. In consequence, a strong thermal dependency of the current I_D is evident. In the case of $\Delta T = T_2 - T_1 = 125$–400 K (cf. Fig. 3), a current change of 86.5 nA at $V_D = V_{TG} = 2\,V$ is achieved. Importantly, this mechanism can be attributed to thermally activated charge carriers, overcoming the Schottky barrier (TE). Noteworthy, evaluating the temperature range between 350 and 400 K, a current change of 20 nA is observed. As the current needs to be considered in respect to resistance, the TCR is defined as $\frac{1}{R_0}\,dR/dT$, with $R_0 = V_D/I_D$ denoting the resistance at the operation temperature and dR/dT being the resistance change per K.

Finally, Fig. 4 shows the extracted TCR values in dependence of the applied bias voltage of the Al-Ge SBFETs with wired gate and drain electrodes. According to previously discussed expressions (cf. Fig. 3), the TCR can be calculated using the following equation:
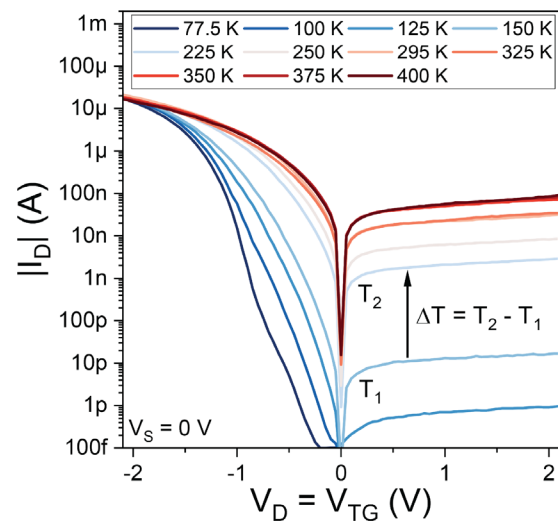

FIG. 3. I–V characteristics at temperatures ranging from 77.5 to 400 K indicating a strong temperature dependence in the n-branch ($V_D = V_{TG} > 0\,V$) due to the presence of a dedicated Schottky barrier and TE being the dominant charge carrier transport contributor.
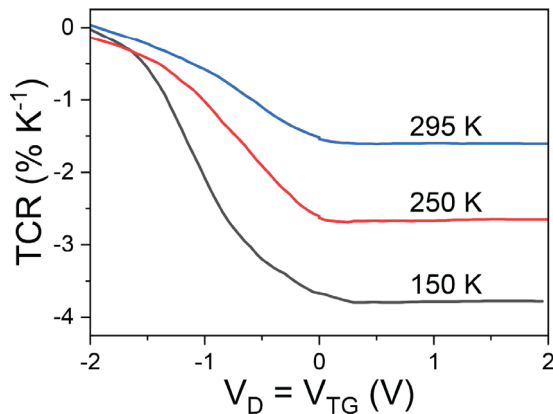
FIG. 4. Selected TCR curves extracted from I–V characteristics showing TCR tunability via the applied bias. Remarkably, in the n-branch ($V_D = V_{TG} > 0$ V), the TCR remains stable, due to the diode characteristic achieved by wiring the gate and drain electrodes.

$$TCR = \frac{1}{\Delta T}\frac{R_{DS}(T_2) - R_{DS}(T_1)}{R_{DS}(T_1)} = \frac{1}{\Delta T}\frac{R_{DS}(T_2)}{R_{DS}(T_1)} - 1$$
$$= \frac{1}{\Delta T}\frac{V_D/I_D(T_2)}{V_D/I_D(T_1)} - 1 = \frac{1}{\Delta T}\frac{I_D(T_1)}{I_D(T_2)} - 1. \quad (1)$$

In Eq. (1), ΔT is the considered temperature range (cf. Fig. 3), and R_{DS} ($= V_D/I_D$) is defined as the total resistance of the two-terminal device, consisting of the Schottky junction resistances as well as the Ge channel resistance. In general, the main contributing factor is the Schottky junctions, as they are defining the charge carrier injection capabilities, whereas in strong hole accumulation ($V_D < 0$ V), the Ge channel becomes the main resistance contributor, due to the quasi-ohmic contact properties for hole injection.[27,28] In the n-branch, where an explicit Schottky barrier is evident and charge carrier transport is merely possible via TE, the Schottky junction is the resistance dominating contributor. Consequently, in the temperature range of 125–150 K, a bias-tunable TCR is achieved with values of −0.3%/K at −2 V and −3.8%/K at 2 V. Note that negative TCR values are obtained as the resistance of the proposed devices is decreasing at elevated temperatures, which is a characteristic feature of semiconductors. Increasing the temperature leads to lower TCR values due to the fact that more thermally excited charge carriers are available and, therefore, occupy more states according to Fermi–Dirac statistics. Nevertheless, even in the temperature range of 250–295 K, maximum TCR values in the n-branch of −1.6%/K are achieved, promoting room temperature operability of the proposed thermometer.

In this work, a two-terminal device, i.e., a SBFET with wired gate and drain electrodes, is functionalized as a thermometer and characterized in terms of the involved temperature dependent electronic transport, especially TCR. Remarkably, operating the device as a two-terminal device, i.e., with wired gate and drain electrodes, a diode characteristic is obtained. Importantly, in the electron dominant transport regime, TE is the predominant charge carrier transport mechanism and, therefore, promotes a dedicated temperature dependency. In the p-branch, FE gets dominant due to the fact that the Fermi level pins close to the valence band. Due to the bias-dependent TE and FE transport mechanisms, tunability of the TCR with values between −0.3 and −3.8%/K in the 125–150 K temperature range is achieved. As the temperature dependency can also be turned off, i.e., TCR ≈ 0%/K, conventional nanoelectronic applications, e.g., transistors or logic circuits, can be realized with this device architecture even allowing co-integration paradigms on the base of the used GeOI platform. The proposed device concept might lead to more sensitive IR detectors, offering the possibility of tunable operation parameters for optimum performance, pulsed operation for reduced Joule heating, or direct addressing in detector arrays for camera application.

AUTHOR DECLARATIONS
Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

R. Behrle: Data curation (equal); Formal analysis (equal); Methodology (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **J. Smoliner:** Conceptualization (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Supervision (equal); Validation (lead); Writing – original draft (equal); Writing – review & editing (equal). **L. Wind:** Methodology (equal); Resources (equal); Writing – original draft (equal); Writing – review & editing (equal). **D. Nazzari:** Methodology (equal); Resources (equal). **A. Lugstein:** Resources (equal); Writing – original draft (equal); Writing – review & editing (equal). **W. M. Weber:** Validation (equal); Visualization (equal). **M. Sistani:** Formal analysis (equal); Funding acquisition (lead); Investigation (equal); Methodology (equal); Supervision (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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