Highly-Sensitive Integrating Optical Receiver With Large PIN Photodiode

Simon Michael Laube, Christoph Gasser, Kerstin Schneider-Hornstein, and Horst Zimmermann

***Abstract*—This paper presents a highly-sensitive monolithic optoelectronic receiver in 180 nm CMOS. An integrating front-end with noise matching via an negative Miller capacitance is proposed, to reduce the power penalty imposed by large PIN photodiodes (PDs). Three new multi-dot PIN PDs are integrated with the front-end. At a wavelength of 642 nm and reverse bias of 8 V, their responsivity (capacitance) is 0.38 A/W (29 fF), 0.36 A/W (33 fF), and 0.43 A/W (123 fF), respectively. Compared to our previous integrating PIN receivers, the light-sensitive area is up to 30 times larger. At a supply voltage of 1.8 V, wavelength of 642 nm, bit rate of 20 Mbit/s, and reference BER $= 2 \cdot 10^{-3}$, the prototype receiver achieves a sensitivity of -55.4 dBm for the first PD, -56.5 dBm for the second PD, and -53.4 dBm for the third PD. The best sensitivity equals a distance of only 21.2 dB to the quantum limit.**

***Index Terms*—CMOS, capacitive feedback, transimpedance amplifier, noise matching, negative capacitance, p-i-n photodiode, integrate-and-dump, correlated double sampling, quantum limit.**

I. Introduction

THE quantum limit (QL) sets a lower boundary on the number of photons necessary to achieve a given bit error probability (BER) in direct detection optical communication. This so-called shot noise limit is a fundamental consequence of the Poisson statistics of photons. Accomplishing detection at the QL is restrained by the quantum efficiency and noise of detectors, as well as the electronic noise of the front-end circuit. Monolithic optoelectronic receivers in CMOS technology are desirable in terms of cost and technological maturity, but suffer even more from the abovementioned issues, because photo detectors and circuits cannot be optimized independently. Thus far, the QL has remained untouched.

In the past, research of highly-sensitive optical receivers has focussed on single-photon avalanche diode (SPAD) detectors [1], [2], [3], [4], [5]. Their high intrinsic gain essentially creates digital pulses that overcome front-end noise. However, SPADs exhibit imperfections, such as high dark count rate (DCR) due to thermally generated carriers and/or tunneling, and after-pulsing. These imperfections limit the bit rate of single SPAD receivers [2]. Arrays of SPADs resolve these issues, at the price of increased circuit complexity, chip area and power consumption [1], [3], [4], [5]. Nevertheless, sensitivities as low as 11 dB above the QL have been reported [3], [4], [5].

Detector gain also enables highly-sensitive linear receivers. Avalanche photodiode (APD) receivers in (Bi)CMOS achieved a gap of 22 dB [6] and 20 dB [7] to the QL, respectively. A disadvantage of these receivers is the excess noise inherent to APDs [8], which makes sensitivity optimization all the more challenging.

Recently, PIN PD receivers without detector gain have approached SPAD receiver sensitivities [9], [10]. The key principle of the receiver is to integrate the photon-generated charges on the small parasitic capacitance of the PD and front-end transistors. A single-dot PIN PD with a diameter of 30 μm is used to keep the PD capacitance at a minimum. Although this benefits receiver sensitivity, the small PD size implies the need for highly accurate fiber alignment or lenses, which can be a practical constraint. Any photon absorbed outside the small light-sensitive area of the PD is lost. A gap of 18 dB to the QL was achieved [9], [10], which confirms the capabilities of PIN PDs for highly-sensitive receivers.

The purpose of this paper is to explore noise matching with negative capacitance (NC) to enable highly-sensitive optical receivers with increased PIN PD area. We propose a receiver in 180 nm CMOS (Sections II and III), together with three new low-capacitance large-area PIN detectors (Section IV). Our experimental results demonstrate competitive sensitivity (Section V).

II. Receiver Architecture

Our goal is to achieve receiver sensitivities near the shot noise QL for direct detection of on-off keying (OOK) modulated optical signals [11], [12],

$$\overline{P}_{\mathrm{QL}} = -\frac{\mathrm{hc}}{\lambda} \cdot \frac{B}{2} \cdot \ln\left(2 \cdot \mathrm{BER}\right), \tag{1}$$

where B is the bit rate. To that end, we must approximate a noiseless receiver as close as possible. If we only consider PIN PDs without intrinsic gain, the detector noise will be low due to small photocurrent. The attainable sensitivity is therefore limited by the electronic noise of the transimpedance amplifier (TIA) [13], and the quantum efficiency η of the PD. A typical wideband TIA topology is the resistive shunt-feedback TIA.

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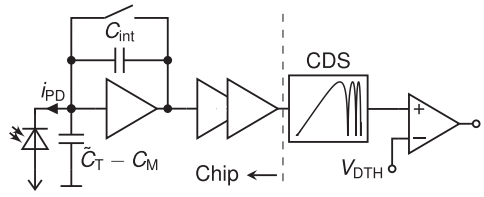

Fig. 1. Integrating receiver block diagram. The linear channel consists of an integrate-and-dump TIA with negative capacitance, post-amplifiers and correlated double sampling (CDS) equalizer. It is followed by the decision circuit. In our implementation of the proposed receiver, CDS and bit decision are done in software.

Its feedback resistor contributes significant thermal noise to the input-referred current noise power spectral density (PSD) [14]. This noise cannot be sufficiently reduced, because the feedback resistance is bounded by technology parameters [15]. Active feedback topologies that inject noise current directly into the receiver input node, such as the regulated cascode [16], exhibit similar limitations. Consequently, these topologies impede sensitivity optimization.

In this work we apply the integrating front-end with noiseless capacitive feedback. The integrator transfer function is the noise-optimal matched-filter response for sharp rectangular input pulses [13]. A practical implementation of the integrating front-end is the integrate-and-dump (I&D) topology [12], [17], where the integrator is reset after each bit to maintain its operating point. Fig. 1 shows a simplified schematic of the overall system architecture. The I&D TIA is comprised of an amplifier with feedback capacitor C_{int}, and a reset switch connected in parallel to the capacitor. The reset switch closes for a fraction of each bit period, disabling signal detection during this time. Return-to-zero (RZ) modulation is applied to the optical signal to avoid the power penalty due to the reset.

$\tilde{C}_{\text{T}}$ is the sum of all input node capacitances (without Miller effect), including the PD capacitance C_{PD}. These capacitances define the transfer function, noise, and sensitivity. Previous work by our group employed ultra-low capacitance single-dot PDs to reduce C_{PD} [9], [10]. In this work, we focus on larger PIN PDs. Noise matching based on NC [18], [19] counteracts the increase in PD capacitance. The theoretical optimal noise matching impedance is a NC that completely cancels the input node capacitance $\tilde{C}_{\text{T}}$ [13]. However, only active circuits can implement NC, which add additional noise to the system. The noise matching capacitance $-C_{\text{M}}$ adds to the input node capacitance $\tilde{C}_{\text{T}}$, as shown in Fig. 1. We define the effective integration capacitance as a measure of (front-end) output voltage per input charge [10]. For the architecture shown in Fig. 1, it is given by

$$C_{\text{int,eff}} = \frac{\tilde{C}_{\text{T}} - C_{\text{M}} + C_{\text{int}}(1 - A_0)}{-A_0}, \tag{2}$$

where A_0 is the voltage gain of the inverting front-end amplifier (i.e. A_0 is negative). With that, a first-order approximation of the TIA's transimpedance is

$$Z(s) = -\frac{1}{sC_{\text{int,eff}}}, \tag{3}$$

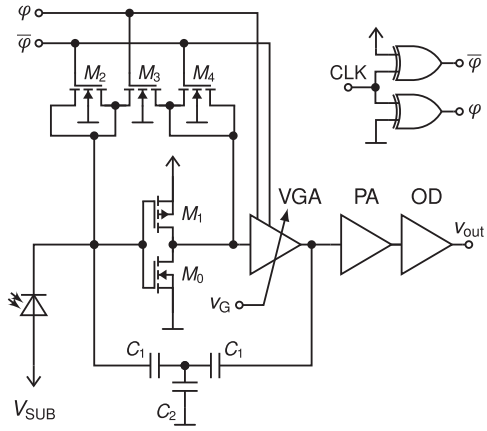

Fig. 2. Circuit of the proposed receiver.

and its input referred current noise PSD (neglecting flicker noise) is

$$S_i(f) = 4\text{k}T\Gamma\frac{(2\pi f)^2(\tilde{C}_{\text{T}} + C_{\text{int}} - C_{\text{M}})^2}{g_{\text{m}}}, \tag{4}$$

where g_{m} is the transconductance of the front-end transistor(s), and Γ is Ogawa's noise factor [20]. Eqs. (2) to (4) underline the need for low capacitance, and show the potential of the noise matching approach.

After post-amplification, CDS equalization [21] removes interference and noise from the signal. Firstly, CDS cancels the random offset voltage in each bit, caused by the reset-induced kT/C voltage noise at the input node. Small $\tilde{C}_{\text{T}}$ is crucial for the proposed architecture, but increases kT/C noise. Hence, offset voltages in the same order of magnitude as the desired signal are present. Secondly, low-frequency flicker noise is suppressed due to the high-pass frequency response of CDS (indicated in Fig. 1). CDS also decreases the signal-to-noise ratio (SNR) because two noisy samples are taken and subtracted, in contrast to conventional receivers where only one sample is needed.

Finally, the CDS output voltage is compared to the decision threshold V_{DTH} to resolve the bit. The value of V_{DTH} shall be chosen to minimize the BER.

III. Proposed Receiver

We propose an implementation of the receiver architecture discussed in Section II (Fig. 1) based on an inverter front-end with a consecutive variable-gain amplifier (VGA), that allows fine-tuning of the NC for optimized BER – see Fig. 2. All circuits are isolated from the negative substrate potential (V_{SUB}, PD anode) by a deep n-well. The positive supply voltage is 1.8 V.

A. Front-End

The integrating front-end TIA is a single inverter (M_0, M_1) operated at the center of its DC transfer characteristic, where it exhibits large gain ($A_0 = -40$) – see Fig. 2. This topology minimizes the effective integration capacitance, whereas both transistors contribute to the transconductance, thereby increasing the SNR. Similar to previous work [9], [10] there is no

dedicated integration capacitor C_{int}, only parasitic capacitance, most importantly the gate-drain overlap capacitances C_{gd} of M_0 and M_1. However, minimal inverter transistors are impractical, especially for large PDs, due to noise and bandwidth requirements. Considering the noise optimum [14], we sized M_0 and M_1 to match the capacitance of the smallest PD (cf. Section IV), and to set the operating point to $V_{\text{DD}}/2$; their gate length is minimal ($L_{\text{min}} = 180\,\text{nm}$). The integration capacitance C_{int} resulting after extraction of parasitic capacitances from the layout is approximately 3 fF.

Transistor M_3 resets the TIA after each bit to restore its operating point. It is actuated by periodic pulses on φ. M_2 and M_4 are minimum-size compensation transistors, that are half the size of M_3 to match capacitance. Their gates are driven by the inverted pulse signal $\overline{\varphi}$ to approximately cancel capacitive clock feedthrough and the channel charge released by M_3 when it turns off [22]. Without the compensation transistors, the injected charge creates a potentially large nuisance signal [23], [24] overlaying the bit signal. Theoretically, CDS will eliminate the overlaid signal, if it is equal in each bit, and if it is small enough to avoid saturation of any amplifier.

Off-chip circuitry feeds the single-ended clock signal CLK, which is complementary to the return-to-zero (RZ) modulation scheme (cf. Section V-A). Two on-chip XOR gates convert the CLK signal into the reset signals φ and $\overline{\varphi}$ by buffering and inverting CLK, respectively. Due to this simple topology, the relative phase and rise time of $\varphi/\overline{\varphi}$ are not tightly controlled.

B. Negative Miller Capacitance

Positive capacitive feedback to the TIA input is required to exploit the Miller effect for NC. Both, the input node and the TIA output, are extremely sensitive to capacitive loading. Additional capacitance at the input node raises $\tilde{C}_{\text{T}}$, thereby reducing transimpedance $Z(s)$, and increasing the input-referred noise $S_i(f)$ – see (3) to (4). On the other hand, capacitance at the output node reduces the TIA bandwidth, which is especially harmful for small front-end transistors with low g_{m}.

Our topology, shown in Fig. 2, addresses both design challenges. An inverting VGA with small input capacitance establishes positive gain between its output and the TIA input. Due to high gain, sub-fF feedback capacitance is required for NC. The capacitive voltage divider C_1–C_2–C_1 implements such a small equivalent capacitance using larger capacitors [25]. The matching capacitance seen at the TIA input is

$$C_{\text{M}} = -C_1 \frac{1 - A_0 A_1 + \kappa}{2 + \kappa}, \tag{5}$$

where A_1 is the VGA voltage gain, and $\kappa = C_2/C_1$. We chose $C_1 = 10\,\text{fF}$ and $C_2 = 100\,\text{fF}$ based on the expected PD capacitance (cf. Section IV). The VGA is a differential amplifier with cascoded input pair and source degeneration – see Fig. 3. Open-loop operation without feedback to the gate of M_9 reduces TIA loading. In addition, the Miller effect of M_9/M_{10} is cancelled by the cascode M_{11}/M_{12}. Transistor M_7 implements gain control via source degeneration of M_9 and M_{10}. VGA voltage gain can

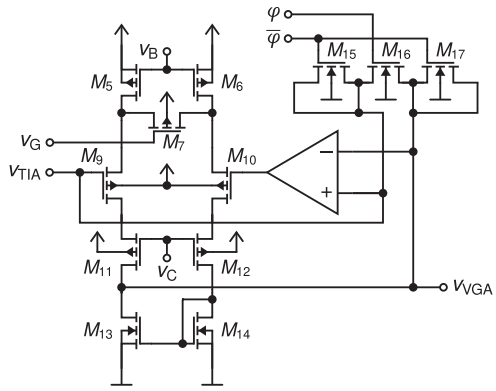

Fig. 3. Variable-gain amplifier circuit.

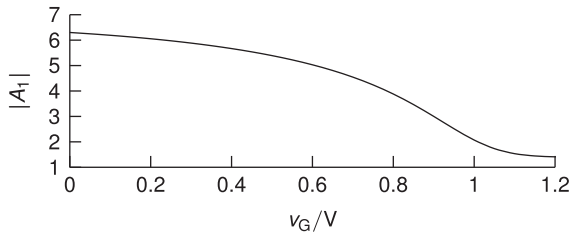

Fig. 4. Post-layout simulated midband gain control law of the VGA.

be approximated as

$$A_1(s) \approx \frac{g_{\text{v}} r_{\text{ds},13}}{1 + s r_{\text{ds},13} C_{\text{L}}}, \tag{6}$$

with

$$g_{\text{v}} = \frac{g_{\text{m},9}}{1 + \frac{g_{\text{m},9}}{2 g_{\text{ds},7}}}, \tag{7}$$

where C_{L} is the load capacitance seen by the VGA output. The drain-source conductance $g_{\text{ds},7}$ of M_7 is set by v_{G} and controls g_{v} according to (7). Thereby, the gain (numerator in (6)) is varied, whereas the bandwidth remains unchanged. The size of M_7 was chosen in relation to M_9 to achieve the desired tuning range of the gain – see Fig. 4. At $|A_1| = 3$ the absolute value of the NC is half of the total input node capacitance, including Miller effect of the TIA. The input pair M_9/M_{10} is designed for maximum transconductance, which is constrained by the admissible input capacitance (TIA loading) and DC operating point. The latter is a significant constraint, because of the $1.8\,\text{V}$ supply, TIA operating point at $0.9\,\text{V}$, and threshold voltages around $V_{\text{TH}} \approx 0.8\,\text{V}$. Co-optimization of the TIA and VGA yielded a combined maximum (post-layout) bandwidth of $57\,\text{MHz}$, pushing the TIA to a relatively high gain-bandwidth product of $4\,\text{GHz}$. Furthermore, proper noise matching required a flat loop gain frequency response around the desired bit rate, which is only present well below the bandwidth. Consequently, the achievable bit rate is limited to $B = 20\,\text{Mbit/s}$.

The operational amplifier in Fig. 3 driving the gate of M_{10} is a PMOS cascoded differential amplifier with low gain-bandwidth product. It provides DC feedback to set the VGA output operating point equal to the TIA operating point. Small cascoded

input transistors entail negligible capacitive loading for the TIA output, which drives M_9 and the positive amplifier input. Transistors M_{15}, M_{16} and M_{17} reset the capacitive voltage divider synchronously together with the TIA reset.

C. Post Amplifier & Output Driver

A post amplifier (PA) and output driver (OD) are necessary to drive subsequent DC-coupled $50\,\Omega$ equipment with sufficient amplitude – see Fig. 2. The PA is a PMOS differential amplifier with cascoded input pair, to minimize the capacitive load for the VGA. Its gain is set to $A_2 = 5$ via resistive feedback and the nominal post-layout simulated bandwidth is $f_2 = 54.7\,\mathrm{MHz}$. The OD uses a two-stage topology. A class AB push-pull power amplifier [26] based on low-voltage differential amplifiers [27] drives the chip output. The class AB stage itself is driven by a simple NMOS differential amplifier with unity-gain feedback around the power amplifier. Post-layout simulation results show that the push-pull stage can drive a maximum peak-to-peak voltage of $1.3\,\mathrm{V}$ into a load impedance of $Z_\mathrm{L} = 50\,\Omega \parallel 100\,\mathrm{pF}$ up to $65\,\mathrm{MHz}$.

IV. Photodiodes

Three different PIN PDs were integrated with the same receiver core circuit. This section details the physical structure of these PDs, and shows their characteristics obtained from measurements of separate test structures on the same wafer.

A. Cathode Geometry

Hemispherical cathode dots are a proven geometry for PIN PDs [28], [29], [30] and APDs [31], [32], offering very low capacitance at relatively large light-sensitive area. In this work we applied multi-dot cathode arrangements with different surface anode geometries, see Fig. 5, to increase the light-sensitive area further. The wafer substrate is a p+ doped bulk material, on which a $24\,\mu\mathrm{m}$ thick p− layer is grown epitaxially. In our PIN PDs, the bulk acts as the backside anode, whereas the p− layer forms the intrinsic (I) layer. The dot cathode consists of a hemispherical n-well region with a drawn surface radius of $2\,\mu\mathrm{m}$. It is contacted by an n+ region with a radius of $1\,\mu\mathrm{m}$. The choice of these radii influences the PD capacitance C_PD and responsivity $\mathcal{R}$. Direct comparison of previous designs indicates that shrinking the cathode radius [29] decreases C_PD and $\mathcal{R}$, whereas a larger radius [28] has the opposite effect. For this work, we chose the larger cathodes for increased $\mathcal{R}$, to optimize receiver sensitivity $\overline{P}$ based on the classical scaling law [13], [33]

$$\overline{P} \propto \frac{\sqrt{C_\mathrm{PD}}}{\mathcal{R}}, \tag{8}$$

which states that an increase of $\mathcal{R}$ is more effective than a reduction of C_PD. For the same reason, shallow trench isolation (STI) generation is blocked across the whole surface area of the PDs. The same cathode geometry was used in $350\,\mathrm{nm}$ CMOS technology by [10].

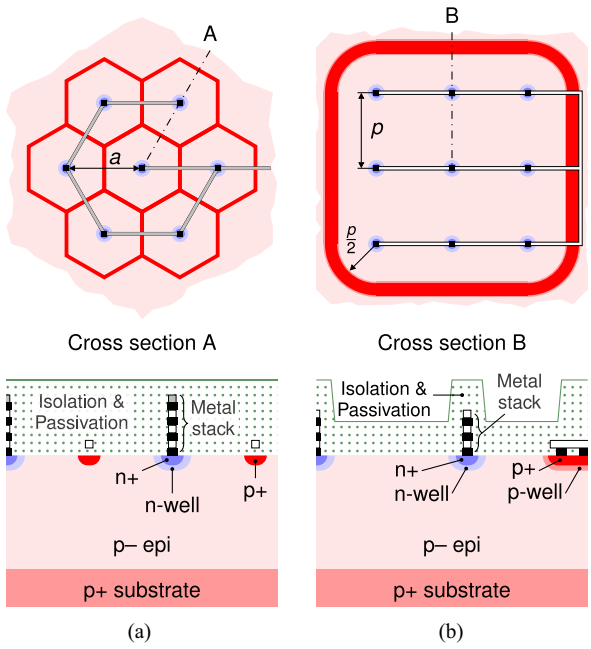

Fig. 5. Schematic top view (without anode metal) and cross-section of the multi-dot photodiodes. a) Seven-dot honeycomb photodiode. b) 3 × 3 matrix multi-dot photodiode.

B. Honeycomb Photodiode

In the first multi-dot PD, seven n+/n-well cathode dots are arranged in a hexagonal grid with distance $a = 30.41\,\mu\mathrm{m}$, as shown in Fig. 5(a). Thin ($0.8\,\mu\mathrm{m}$), hexagonal surface anodes are implanted around each of the dots, using the p+ source/drain implants of regular PMOS transistors. Contacts to the first metal layer are placed in each of the corners of the anode hexagons (not shown in top view). To reduce parasitic capacitances, the cathodes are interconnected on the topmost (fourth) metal layer by minimum-width metal lines – see Fig. 5(a). The resulting seven-dot honeycomb photodiode (7W-PD) is a parallel combination of seven single-dot PDs with modified surface anodes compared to the circular shape in [28], [29], [31], to maximize the light-sensitive area for this particular arrangement. From the geometry we find a total light-sensitive area of $A_\mathrm{7W} = 5315\ \mu\mathrm{m}^2$.

C. Matrix Multi-Dot Photodiodes

Matrix arrangement of cathode dots can improve the fill-factor and offers very large light-sensitive areas at low capacitance [30], [32]. Two different matrix PIN PDs are implemented in this work: A 3 × 3 multi-dot photodiode (3 × 3-PD), and a 6 × 6 multi-dot photodiode (6 × 6-PD). Fig. 5(b) illustrates their physical structure and defines the important dimensions of both PDs.

The n+/n-well cathode dots are arranged in a square matrix, separated by the pitch $p = 21\,\mu\mathrm{m}$. There is no surface anode between the dots, but a large, $5.2\,\mu\mathrm{m}$ wide p+/p-well anode ring encloses the matrix at half-pitch distance. All cathode dots are connected via the third metal layer. Minimum size metal lines on the third and fourth metal layer have approximately equal parasitic metal-to-substrate capacitance in this $180\,\mathrm{nm}$ CMOS

TABLE I
MEASURED PIN PD PARAMETERS AT A REVERSE BIAS OF 8 V AND 642 nm WAVELENGTH

Diode	C_{PD}/fF	$\mathcal{R}/(\mathrm{A/W})$	η
7W-PD	29.4	0.382	0.738
3×3-PD	32.7	0.357	0.689
6×6-PD	122.6	0.432	0.834

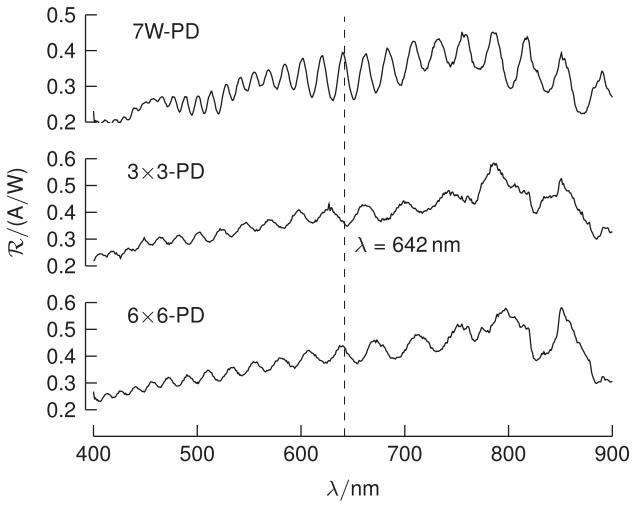

Fig. 6. Responsivity spectra $\mathcal{R}(\lambda)$ of the multi-dot PIN PDs, measured at a reverse voltage of 8 V.

technology, since the fourth metal layer is wider. In contrast to the 7W-PD, the cathode interconnect of the 3 × 3-PD and 6 × 6-PD does not cross the anode metal connection very often, which justifies the use of the third metal layer for these PDs. The total light-sensitive area amounts to $A_{3\mathrm{x}3} = 3874\ \mu\mathrm{m}^2$ for the 3 × 3-PD, and $A_{6\mathrm{x}6} = 15781\ \mu\mathrm{m}^2$ for the 6 × 6-PD.

Contrary to the 7W-PD, the matrix multi-dot PDs have an opto-window across the active area, where part of the isolation and passivation stack is removed for better transmittance – see Fig. 5(b). Since the cathode interconnect must not be covered by this opto-window, passivation ridges occur along the metal lines. The geometry of the 7W-PD results in uneven opto-window coverage of the PD due to these ridges. Therefore, the 7W-PD has no opto-window.

D. Photodiode Characteristics

Standalone test structures for the characterization of the three PIN PDs were integrated on the same wafer as the receivers. Table I shows the measured PD capacitance at a substrate bias of $V_{\mathrm{SUB}} = -8\,\mathrm{V}$, measured in a wafer prober using an LCR meter. The 7W-PD and 3 × 3-PD show inherently similar absolute capacitance, since the number of cathode dots only differs by two. The respective capacitance per dot is 4.20 fF for the 7W-PD, 3.63 fF for the 3 × 3-PD, and 3.41 fF for the 6 × 6-PD. This result manifests the physical structure of each PD, because the parasitic capacitance of the metal lines is shared between a higher number of dots with increasing diode size.

The DC responsivity spectra $\mathcal{R}(\lambda)$ shown in Fig. 6 were measured in the wafer prober by sweeping the wavelength with a monochromator, and measuring the photocurrent with a source meter. As expected, the periodic variation of $\mathcal{R}(\lambda)$, due to Bragg reflection in the oxide and passivation stack, is less for the 3 × 3-PD and 6 × 6-PD compared to the 7W-PD, because of the opto-window. The quantum efficiency η (proportional to $\mathcal{R}/\lambda$) of the 7W-PD peaks at around 600 nm and decreases for wavelengths above 750 nm. In contrast, both matrix multi-dot PDs exhibit constant η below 800 nm, because $R(\lambda)$ is approximately linear in this interval, before it drops at higher wavelengths. Considering this characteristic and available lab equipment, we tested our chips at $\lambda = 642\,\mathrm{nm}$, where high η can be expected for all PDs. The relevant $\mathcal{R}$ and η are shown in Table I. With regard to the required PD voltage V_{PD}, PD bandwidth is no concern due to the limited bandwidth of the receiver circuit (cf. Section III-B). Hence, all measurements were performed at $V_{\mathrm{SUB}} = -8\,\mathrm{V}$ ($V_{\mathrm{PD}} = -8.9\,\mathrm{V}$), based on previous experience with similar PDs in this process [28]. This moderate voltage permits on-chip generation of the photodiode bias even more easily as was done in [34].

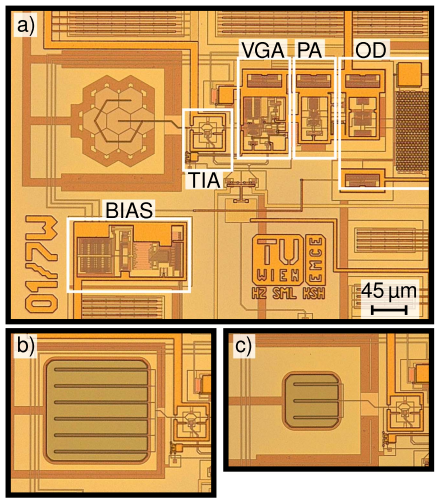

Fig. 7. Microphotograph of the integrating optical receiver. (a) Chip core consisting of the 7-dot honeycomb PIN photodiode, integrating TIA, and amplifier chain. (b) 6 × 6 multi-dot PIN photodiode (c) 3 × 3 multi-dot PIN photodiode. The micron bar is valid for all three images.

V. EXPERIMENTAL RESULTS

The receiver was fabricated in 180 nm high-voltage CMOS without process modifications. Fig. 7(a) shows a microphotograph of the receiver core and the 7W-PD; the 6 × 6-PD and 3 × 3-PD are shown in Fig. 7(b) and Fig. 7(c), respectively. The latter two images clearly show the opto-window of the PDs. Chip size is mostly defined by the number of bond pads. The total die measures 0.9 mm × 0.86 mm, whereas the core is around 0.6 mm × 0.2 mm, including the OD. The total power consumption excluding (including) the OD is 1.4 mW (35.3 mW).

A. Methods

We characterized the receivers by capturing a 1 Mbit sequence of the pseudorandom bit sequence (PRBS) $(2^{15} - 1)$ and the chip output signal with an oscilloscope (Keysight

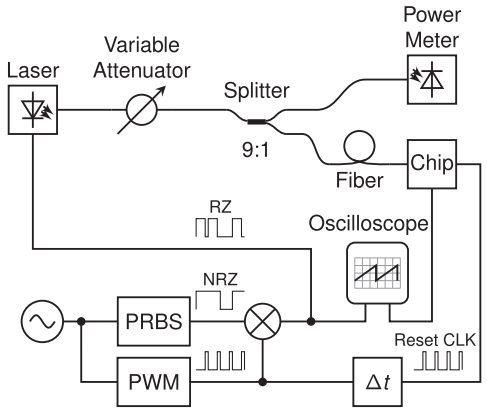

Fig. 8. Schematic of the BER measurement setup. The optical path (top half) shows the modulated light source, light attenuation and optical power measurement. The electrical path (bottom half) generates the RZ PRBS modulation signal for the laser, and the complementary chip reset signal.

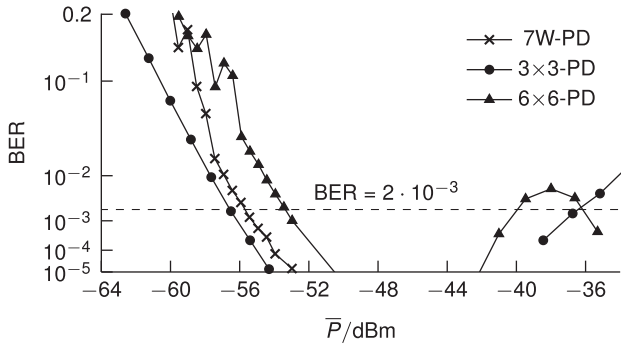

Fig. 9. Measured BER characteristic of the three receivers. BER values are plotted in the $-10\log(\mathcal{Q})$ coordinate system [13]. The lines are a visual aid and not measured data.

MSOV204A) at a sampling rate of $5\,\mathrm{GS/s}$ – see Fig. 8. All signal processing functions of the oscilloscope (e.g. averaging) are turned off to capture the raw chip output. The required chip stimuli are derived from a $20\,\mathrm{MHz}$ clock source that feeds a bit pattern generator (Sympuls BMG2500), and a custom discrete emitter-coupled logic (ECL) pulse-width modulation (PWM) signal generator. The pattern generator provides a $20\,\mathrm{Mbit/s}$ non-return-to-zero (NRZ) PRBS, which is gated by the PWM signal to obtain $80\,\%$ RZ modulation. This signal directly modulates the laser ($\lambda = 642\,\mathrm{nm}$). Short single-mode fibers guide the light from source to chip, passing through a variable attenuator and a splitter. The reference branch ($90\,\%$ branch) after the splitter measures the optical power to infer the power incident on the chip ($10\,\%$ branch). The exact splitting ratio was determined once using two power meters. Periodic reset of the integrating TIA is triggered via the PWM signal, which passes through a digital delay line (Δt) to align with the optical PRBS signal before it enters the chip.

A Python script performs CDS and bit decision on the stored oscilloscope waveforms. The minimal BER was determined by sweeping the CDS sample instants in $1\,\mathrm{ns}$ steps, and sweeping the decision threshold voltage in $0.4\,\mathrm{mV}$ steps ($12\,\mathrm{bit}$ resolution with a $1.8\,\mathrm{V}$ range). The digitized data stream is compared to the captured PRBS to determine BER. Any deterministic delay between the PRBS and chip data, caused by the optical fibers and wires, is compensated by the Python script as well.

A metal enclosure (dark box) shields the chip from all ambient light. Chip temperature is not tightly controlled in our setup; the ambient temperature was around $20\,^{\circ}\mathrm{C}$.

B. Sensitivity

Fig. 9 presents the experimental BER results of all three receivers. Data are plotted in the $-10\log(\mathcal{Q})$ coordinate system with the Personick $\mathcal{Q}$ factor [35] calculated from the measured BER. In this coordinate system, the noise-limited BER characteristic (i.e. sensitivity) is a linear, monotonically decreasing function of the optical power [13]. The BER results of all three receivers reflect this characteristic around their sensitivities for $\mathrm{BER} = 2 \cdot 10^{-3}$. At this reference BER, the 7W-PD achieves a sensitivity $\overline{P}$ (distance to QL ΔP) of $-55.4\,\mathrm{dBm}$ ($22.3\,\mathrm{dB}$) with NC matching of $-91\,\mathrm{fF}$; the 3×3-PD achieves $-56.4\,\mathrm{dBm}$ ($21.2\,\mathrm{dB}$) at a NC of $-91\,\mathrm{fF}$; and the 6×6-PD achieves $-53.4\,\mathrm{dBm}$ ($24.3\,\mathrm{dB}$) at a NC of $-151\,\mathrm{fF}$. The NC value is calculated from the applied v_G and post-layout simulated gain (A_0, A_1) using (5). Applying (2) we find an effective integration capacitance of $2.3\,\mathrm{fF}$ for the 7W-PD and 3×3-PD, which is slightly below the extracted value $C_\mathrm{int} = 3\,\mathrm{fF}$ (cf. Section II-I-A). For the 6×6-PD the optimum observed in measurements is $C_\mathrm{int,eff} = 3.1\,\mathrm{fF}$, which is the theoretical noise match $C_\mathrm{M} = \tilde{C}_\mathrm{T}$. This parity between experimental results and theory quantifies the benefit of the noise matching approach. Note that the best measured BER for each optical power was selected in Fig. 9. Hence, the data points of each curve may result from different NC settings. Evidently, the 3×3-PD performed best, requiring an average photon-generated charge of 250 electrons, at a total input-referred equivalent noise charge (ENC) of 83 electrons.

The 3×3-PD outperforming the 7W-PD is a counterintuitive result, considering the PD capacitance (cf. Table I). We surmise that the missing opto-window, and correspondingly high variation of $\mathcal{R}(\lambda)$, resulted in a 7W-PD receiver sample with less responsivity than predicted by Fig. 6. In other words, $\mathcal{R}(\lambda)$ of this sample may have a local minimum at $\lambda = 642\,\mathrm{nm}$. To support this assumption, we measured the substrate (PD anode) DC current of the 7W-PD and 3×3-PD receiver samples at different optical powers and found $\mathcal{R} = 0.301\,\mathrm{A/W}$ and $\mathcal{R} = 0.356\,\mathrm{A/W}$, respectively.

With the given measurement setup (see Section V-A), it is not possible to record longer bit sequences that are necessary to measure lower BERs. We applied the vertical eye-scanning method described in [36] to estimate the sensitivity for lower BER. In particular, threshold sweeps were performed at different optical powers, until the sensitivity for the lowest resolvable BER (highest $\mathcal{Q}$) was found. The resolvable BER in our setup depends largely on the chip output voltage swing. Table II shows the extended sensitivity results with the measured (estimated) CDS peak-to-peak signal voltage v_pp, and the measured (estimated) total root mean square (RMS) noise voltage $\overline{v}_\mathrm{n}$. The

TABLE II
EXTENDED SENSITIVITY RESULTS

Diode	BER	$\overline{P}$/dBm	ΔP/dB	v_{pp}/mV	$\overline{v}_{\mathrm{n}}$/mV
7W-PD	$2 \cdot 10^{-3}$	−55.4	22.3	469.2	149.9
	$3 \cdot 10^{-9}$‡	−47.9	24.4	864.3†	148.1†
3×3-PD	$2 \cdot 10^{-3}$	−56.5	21.2	345.9	116.9
	$2 \cdot 10^{-8}$‡	−52.1	20.7	743.4†	134.9†
6×6-PD	$2 \cdot 10^{-3}$	−53.4	24.3	569.2	186.9
	10^{-10}‡	−48.0	23.6	889.6†	137.6†

†Estimated result, based on [36].
‡Calculated from $\mathcal{Q} = v_{\mathrm{pp}}/\overline{v}_{\mathrm{n}}$.

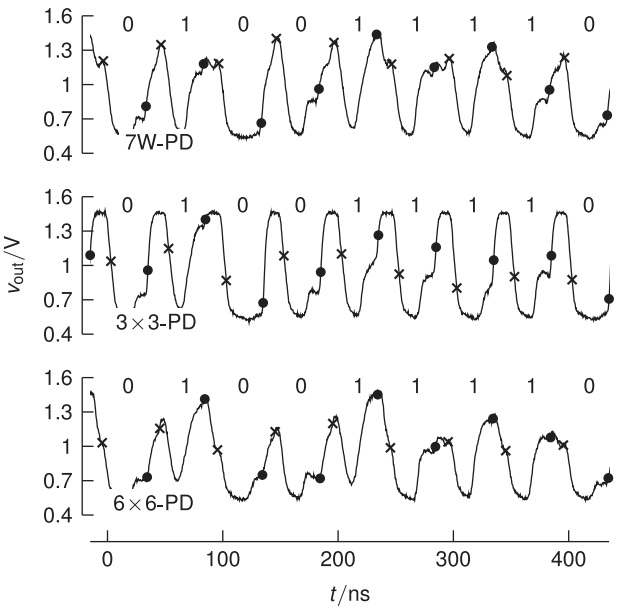

Fig. 10. Transient output voltage of the receivers at their respective sensitivities. The CDS sample points are marked by crosses (×) for the first sample, and dots (•) for the second sample. The binary value of the optical PRBS signal is annotated above each waveform.

extended sensitivity exhibits a similar distance ΔP to the respective QL, only 1 dB to 2 dB difference compared to the measured values at BER $= 2 \cdot 10^{-3}$. Note that the QL for BER $= 10^{-9}$ is 5 dB above that for BER $= 2 \cdot 10^{-3}$. These results suggest that our receivers can maintain their good sensitivity down to the BER $= 10^{-8}$ range.

C. Transient Voltage

A section of the captured transient waveforms and CDS sample instants at the sensitivity is shown in Fig. 10. The CDS output voltage for each bit is the difference of the second sample (marked by dots •) and the first sample (marked by crosses ×). Ideally, the waveforms should show ramp functions for 1 bits, remain constant during 0 bits, and return to the DC operating point after each bit. However, all three receivers show large transient responses after reset. Although this is partially expected due to clock feedthrough and our simple reset signal generation (cf. Fig. 2), simulation did not predict such large transients. One possible explanation is that the extraction of parasitic capacitances from the layout is not accurate enough. Another one would be that the positive feedback for NC contributes to this effect more than expected. Regardless of the overlaid nuisance signal, Fig. 10 shows that CDS yields distinct voltage differences for 0 and 1 bits. In particular, the CDS voltage of the 0 bits is mostly negative, whereas the CDS voltage of the 1 bits is mostly positive. Thereby, bit discrimination at the desired reference BER is achieved.

VI. COMPARISON

Table III compares this work to the state-of-the-art. The merit of our presented receiver is increased PIN PD area. Compared to other integrating PIN receivers, this work increases the PD area by a factor of 5.5 to 22.3 [9], and 7.5 to 30.5 [10]. In relation to [9], bit rate and the distance ΔP to the QL are comparable, whereas [10] achieves a higher bit rate at similar ΔP. Older resisitive high-sensitivity PIN receivers [37], [38] achieved $\Delta P \approx 25.5$ dB, comparable to our 6 × 6-PD receiver, but at higher bit rate $B = 622$ Mbit/s. However, the 6 × 6-PD considerably improves the PD area by a factor of 8 [38] and 50 [37], respectively. Note that these receivers do not employ CMOS front-ends, in contrast to our work. Ref. [37] utilizes InGaAs-InP technology, whereas [38] uses a BiCMOS process with bipolar front-end.

In comparison to previous avalanche photodiode (APD) receivers [6], [7], we achieved similar distance to the QL. However, the APD receivers have more than two times the light-sensitive area of our largest PIN PD, and operate at higher bit rates up to 1.25 Gbit/s. The APD receivers required −18.3 V [6] and −73.7 V [7] substrate bias, respectively.

Previous PIN and APD receiver circuits, as well as this work, employ only a single PD (one "pixel"). In contrast, SPAD receivers with single and multiple PDs (many pixels) have been reported, which require a differentiated comparison. Ref. [2] presents a single SPAD receiver that is closest to our work in terms of bit rate and light-sensitive area. Although the non-ideal behavior of the SPAD inhibits higher bit rates, it shows a superior sensitivity of −64 dBm, at 20 Mbit/s and a reverse voltage around 32 V, which is 8 dB better than our PIN receiver (3 × 3-PD). A slight bit rate improvement was achieved by a 4-SPAD array [1] operated at 30 V reverse bias, that has a PD area similar to our 6 × 6-PD receiver. At 50 Mbit/s, the SPAD comes 6 dB closer to the QL than our 6 × 6-PD receiver at 20 Mbit/s. Further bit rate and sensitivity improvements are enabled by large arrays of SPADs. Based on on-chip signal processing, the SPAD array with 64 × 64 devices in [3], with additional data presented in [4], achieved bit rates of up to 500 Mbit/s at a SPAD operating voltage of 15.2 V. At 50 Mbit/s the SPAD receiver is 10 dB closer to the QL than our best PIN receiver (3 × 3-PD). However, the size and complexity of the array and data processing is a disadvantage compared to our single PD approach. According to the authors, a large part of photons was lost due to fill factor and low photon detection probability [4]. A byproduct of the large SPAD array is its large light-sensitive area, that is currently unachievable by highly-sensitive PIN receivers.

TABLE III
COMPARISON TO STATE-OF-THE-ART

Ref.	Technology	Power cons. $P_S/\mathrm{mW}^\dagger$	PD Type (Reverse Bias)	PD Area $A_{PD}/\mu\mathrm{m}^2$	Bit Rate $B/(\mathrm{Mbit/s})$	BER	Wavelength λ/nm	Sensitivity $\overline{P}/\mathrm{dBm}$	Avg. Nr. of Photons $\overline{n}$	Dist. to QL $\Delta P/\mathrm{dB}$
[37]	InGaAs-InP	N/A	PIN (5 V)	314	622	10^{-9}	1300	−34.7	3565	25.5
[10]	350 nm CMOS	3.9	PIN (20 V)	517	100	$2\cdot10^{-3}$	642	−52.3	190	18.4
[9]	180 nm CMOS	2.6	PIN (20 V)	707	50	$2\cdot10^{-3}$	635	−56.4	147	17.3
[38]	0.6 µm BiCMOS	33	PIN (5 V)	1964	622	10^{-9}	660	−31.6	3696	25.7
[2]	350 nm CMOS	19	SPAD (32 V)	1964	20	$2\cdot10^{-3}$	635	−64.0	64	13.6
[2]	350 nm CMOS	41	SPAD (32 V)	1964	50	$2\cdot10^{-3}$	635	−57.0	128	16.6
[1]	350 nm CMOS	19	4×SPAD (30 V)	15000	50	$2\cdot10^{-3}$	635	−55.7	172	17.9
[6]	350 nm BiCMOS	251	APD (18.3 V)	31415	500	10^{-9}	675	−35.8	1788	22.5
[7]	350 nm CMOS	97	APD (73.7 V)	31415	1000	10^{-9}	675	−35.5	958	19.8
[7]	350 nm CMOS	140	APD (73.7 V)	125664	1000	10^{-9}	675	−34.7	1151	20.6
[3], [4]	130 nm CMOS	115	4096×SPAD (15.2 V)	1795600	50	$2\cdot10^{-3}$	450	−60.5	40	11.7
[3], [4]	130 nm CMOS	115	4096×SPAD (15.2 V)	1795600	100	$2\cdot10^{-3}$	450	−55.2	68	13.9
[5]	Not integrated	N/A	SPAD‡ (28 V)	9424900	400	10^{-3}	405	−50.8	42	11.3
This work	180 nm CMOS	1.4	PIN (8 V)	3874	20	$2\cdot10^{-3}$	642	−56.5	362	21.2
				5315				−55.4	466	22.3
				15781				−53.4	739	24.3

†Without output driver, if given.
‡Structurally, this device contains 5676 SPADs with all cathodes connected.

Ref. [5] employs an off-the-shelf SPAD array (silicon photomultiplier, SiPM) with 5676 devices and an operating voltage of 28 V, where each SPAD is passively quenched by a resistor. All devices are connected to a common cathode. Experimental results up to 2.5 Gbit/s are presented in [5]. At 400 Mbit/s the array achieves a sensitivity 10 dB closer to the QL than our best result, at almost 600 times more light-sensitive area than our 6 × 6-PD. Since this is not a monolithic receiver, size and power consumption of this approach are a clear disadvantage. Our proposed receiver has low power consumption, chip area, and PD bias of only −8 V. Furthermore, PIN PDs do not need strict bias control, that is necessary for APDs or SPADs to eliminate their strong temperature dependence of breakdown voltage and gain.

In a wider context, it is worth noting that photon-resolving receivers are in principle able to detect OOK modulated signals at or below the shot noise QL. The SPAD-based experiment reported by [39] surpasses the QL at 50 kbit/s and BER ≥ 0.1 with optical feedback that must be much faster (30 MHz) than the bit period. Albeit an impactful result, this setup is far from existing as a monolithic solution at reasonable bit rate, BER, and costs, which is the target of our work. The work on CMOS quanta image sensors (QIS) comes closer to this goal, by implementing photon-counting without detector gain [40], [41]. Although sample rates up to 33 MHz have been reported [41], this approach still requires multiple samples per bit for sufficiently low BER. Thus, the bit rate is rather low.

VII. CONCLUSION

The presented monolithic optoelectronic receiver greatly increased the light-sensitive area of the PIN PD compared to our previous work. Noise matching based on NC was introduced to the I&D TIA topology to compensate the additional capacitance. Three different PIN PDs were paired with the front-end, proving the versatility of the noise matching approach. A distance of 21.2 dB to 24.3 dB to the shot noise QL was verified experimentally. The major disadvantage of our receiver is its low bit rate, caused by the feedback bandwidth requirements. In the presented topology, the VGA gain-bandwidth product is at the technological limit, given the unavoidable capacitive load of the next stage, which has been reduced as much as possible. Future research will need to show if other topologies create a better balance between bit rate and the low input node capacitance required for highly-sensitive integrating TIAs with large PDs. The low supply voltage for the PIN photodiodes of only 8V and the insensitivity of their quantum efficiency to ambient temperature is a clear advantage compared to APDs and SPADs, which will justify further effort to achieve higher data rates.

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