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# Exploring negative differential resistance effects in monolithic Al-Ge-Al heterostructures

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**Ezgi Tatli**

# Abstract

Germanium (Ge) is of particular interest for the investigation of quantum effects due to its pronounced spin-orbit coupling and quantum confinement phenomena [1]. In addition to ongoing miniaturization, Ge presents notable performance advantages for integrated ICs owing to its elevated carrier mobility and compatibility with Complementary Metal-Oxide-Semiconductor (CMOS) technology [1]. Over recent years, Vapour Liquid Solid (VLS) grown nanowires (NWs) have served as the foundation for Al-Ge heterostructures [2], facilitating significant advancements in quantum ballistic transport, photonic, and plasmonic investigations [2]. This progress holds the potential for the development of a diverse array of cutting-edge devices [2]. Despite its potential, the large-scale integration of VLS-grown Ge-NWs poses significant challenges [2].

Negative Differential Resistance (NDR) phenomenon is a non-linear electrical behavior observed in a variety of materials and devices [3]. This study presents an in-depth investigation into the NDR behavior exhibited by Al-Ge-Al nanostructures. The results are observed in multiple NDR features in NWs. In the experimental section of this thesis, various analyses were conducted to investigate how the observed phenomena in Al-Ge-Al nanostructures depend on their physical dimensions [3]. This involved systematically varying parameters such as the length, width, and thickness of the NWs to understand their influence on properties like NDR behavior and conductivity. By meticulously controlling these parameters, i was able to uncover trends and correlations that shed light on the underlying physics governing the behavior of these nanostructures [3].

In essence, the NDR behavior observed in Al-Ge-Al NWs stems from intricate interactions among electronic states within the constituent materials. The investigation yields profound insights into the fundamental physics governing NDR phenomena in NW systems, offering promising avenues for future nano-electronic applications [3].

Crystallographic analyses uncover the exceptional purity and crystallinity of Al-Ge heterostructures, featuring nearly atomically sharp interfaces [4]. Our exploration of structures with diverse cross-sections demonstrates the versatility of the thermal Al-Ge exchange process, which exhibits no constraints based on specific orientations or geometric boundaries [4]. The markedly improved contact characteristics of the abrupt metal-semiconductor junction

contribute to a remarkable enhancement in the conductivity of annealed heterostructures [5]. Integration of these advanced heterostructures into field-effect transistor (FET) architectures enables precise modulation of drain current across multiple orders of magnitude [5].

# Kurzfassung

Diese Dissertation untersucht das Potenzial von Germanium (Ge) für die Erforschung quantenmechanischer Effekte und seine Vorteile für integrierte Schaltkreise aufgrund seiner Eigenschaften wie Spin-Ge nanosheets als Grundlage für Al-Ge-Heterostrukturen, die Fortschritte in verschiedenen Bereichen wie Quantentransport, Photonik und Plasmonik ermöglichen [1]. Trotz Herausforderungen bei der großflächigen Integration stellt die Arbeit eine Methodik zur Herstellung monolithischer Al-Ge-Al-Heterostrukturen im Wafer-Maßstab unter Verwendung von GeOI Substraten und Lithographietechniken vor [1]. Eine thermisch angetriebene Reaktion bildet Al-Ge-Heterostrukturen, die die Integration nanoskaliger Geräte mit präzisen Geometrien ermöglichen [2]. Die Studie untersucht auch das nichtlineare elektrische Verhalten, das als NDR in Al-Ge-Al-Nanostrukturen auftritt [2], identifiziert multiple NDR-Merkmale in NWs und untersucht ihre Abhängigkeit von den physikalischen Abmessungen [3]. Die Ergebnisse deuten auf das Potenzial von Al-Ge-Al-NWs als Schlüsselkomponenten für Hochfrequenzelektronik und energieeffizientes Computing hin [3]. Im Allgemeinen resultiert das NDR-Verhalten aus komplexen Wechselwirkungen zwischen elektronischen Zuständen innerhalb von Komponenten [3], was Einblicke in die grundlegenden physikalischen Prinzipien des NDR-Phänomens in NW-Systemen liefert und den Weg für zukünftige Anwendungen in der Nanoelektronik ebnet [3]. Unsere Untersuchung liefert tiefgreifende Einblicke in die grundlegende Physik, die NDR-Phänomene in NW-Systemen steuert, und bietet vielversprechende Ansätze für zukünftige nanoelektronische Anwendungen.

Kristallographische Analysen enthüllen die außergewöhnliche Reinheit und Kristallinität von Al-Ge-Heterostrukturen mit nahezu atomar scharfen Grenzflächen [4]. Unsere Untersuchung von Strukturen mit unterschiedlichen Querschnitten zeigt die Vielseitigkeit des thermischen Al-Ge-Austauschprozesses [4], der keine Einschränkungen hinsichtlich spezifischer Orientierungen oder geometrischer Grenzen aufweist. Die deutlich verbesserten Kontaktmerkmale der abrupten Metall-Halbleiter-Übergänge tragen zu einer bemerkenswerten Verbesserung der Leitfähigkeit von Al-Ge-Al Heterostrukturen bei [5]. Die Integration dieser fortschrittlichen Heterostrukturen in FET-Architekturen ermöglicht eine präzise Modulation des Drain-Stroms über mehrere Größenordnungen [5].

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# Table of Contents

# 1. Introduction

The emergence of semiconductor devices, most notably transistors, during the 1950s, represented a significant milestone in circuitry design's evolution [1]. This technological advancement paved the way for new circuit configurations, catalyzing in a paradigm shift with widespread implications across various aspects of our daily routine [1]. While Ge was used to create the first transistor [5], the Si Metal-Oxide-Semiconductor Field Effect Transistor have emerged as the most successful, thanks in part to its stable and superior SiO2 that acts as an insulator [5]. However, as MOSFET feature sizes continue to shrink, fundamental scaling limitations arise from short channel effects and greater leakage currents, which ultimately hinder the advancement of contemporary devices' performance [5, 6]. Gordon E. Moore's prediction that integrated circuits' processing power would double every 18 months due to a steady rise in transistor count has become legendary [7]. With the rapid downscaling of conventional planar CMOS technology, various challenges arose that led to the need for new materials and device concepts to meet the ever-increasing demands of "Moore's Law." [7], These advancements include the integration of strained Si, high-κ metal gate transistors [8], and the more recent adoption of the non-planar tri-gate architecture [8].

With regard of materials, Ge got in the focus of reserach, the most notable difference is the significantly greater charge carrier mobility displayed by Ge in comparison to Si [9]. From a processing perspective, it is worth mentioning that Ge and nanostructures can be used in conjunction with CMOS technology [9]. This compatibility makes it possible to seamlessly integrate Ge into existing Si technology workflows [9]. Moreover, the incorporation of Ge and SiGe nanostructures into CMOS technology has a positive impact on the efficiency of high-end VLSI systems [1, 9]. To fully utilize the favorable features of Ge, such as strong quantum confinement and superior charge carrier mobility, the use of nano-scale structures is critical. Among these structures, NWs present a compelling opportunity to investigate and capitalize on the distinctive properties of Ge across a range of electronic and optoelectronic applications [10]. Researchers can fully leverage the capabilities of Ge nanostructures in advanced devices with improved performance and functionality by carefully engineering and controlling their dimensions and morphology [11].

Additionally, it's essential to establish high-quality metal-semiconductor connections with precise definitions, as the interface and energy barrier it creates, significantly affect the injection of charge carriers [12]

One promising approach to achieve such interactions involves utilizing metal-semiconductor heterostructures, which involves establishing contact between the semiconducting material and metal contacts and then replacing the semiconductor with metal through thermally driven diffusion processes [13].

Recently, there has been a lot of interest in novel transport phenomena in nanostructures. Leo Esaki is credited with the discovery of the intrinsic NDR phenomenon, observed in a narrow Ge p-n junction in 1957 [14]. While employed at Sony, Esaki investigated semiconductor tunneling phenomena and observed that, under certain conditions, the current-voltage curve of the junction exhibited a negative slope [14]. He coined the term "tunnel diode" to describe this effect, marking the pioneering practical application of NDR [15]. The tunnel diode proved to be a highly advantageous component for the electronics industry, particularly in microwave amplifiers due to its rapid oscillation at high frequencies [15]. Subsequently, numerous researchers delved into the study of NDR and its potential applications. This led to the creation of various NDR devices.

The Gunn Effect, a phenomenon discovered by J.B. Gunn in 1963, represents a pivotal advancement in semiconductor physics, particularly in the realm of III-V compound semiconductors such as GaAs [16]. This effect, characterized by the emergence of NDR in certain semiconductor materials under high electric fields, has profound implications for both fundamental research and practical device applications [16]. GaAs, with its unique electronic properties and high electron mobility, stands as a prominent example of a material exhibiting the Gunn Effect. Understanding the behavior of GaAs under the influence of electric fields and its manifestation of NDR is crucial for exploring its potential in various electronic and optoelectronic applications [16].

This thesis delves into the manufacturing process of monolithic Al-Ge-Al heterostructures incorporated within a GeOI substrate's device layer. The main focus of the investigation is the thermally induced exchange reaction method, which has only been demonstrated with Ge NWs generated through the VLS method mentioned above. Using GeOI substrates offers the potential for achieving wafer-scale production of extensive arrays of nano-scaled devices with accurately defined geometries situated at predetermined locations. The objective is to facilitate NDR effects in Al-Ge structures produced through top-down methods by creating narrow structures with Ge segments of different thicknesses. The NDR phenomenon, which is observed in various materials and devices, is of particular interest due to its non-linear electrical behavior and potential applications in electronic devices.

This research aims to illuminate the complex mechanisms behind NDR in Al-Ge-Al nanowires, with a particular focus on the phenomenon of double NDR. Understanding both single and double NDR behaviors in these heterostructures is essential for maximizing their potential in advanced electronic applications. By unraveling the intricate interplay of various factors influencing NDR, like temperature, dimensionality, and material composition, this study aims to optimize device design and functionality in a range of electronic systems.

# 2. Theory

This chapter offers a concise overview of the physicochemical properties of Al-Ge material systems, fabrication techniques for GeOI substrates, and the solid-state diffusion process required for creating controlled Al-Ge heterostructures. Additionally, it delves into the theoretical foundations of metal-semiconductor interfaces and NDR phenomena. The chapter also examines the theoretical concepts relevant to the current study. The first part of the study focuses on the fundamental physicochemical properties of Al and Ge materials, while the subsequent section analyzes the characteristics specific to the Al-Ge system. This includes studying the electrical properties of the metal-semiconductor heterostructure and analyzing interfaces and impurity states within the structure.

## 2.1 Aluminum

Al is a metal that is in the 3$^{rd}$ group of the periodic table of elements.Al is the most abundant metallic element in earth's crust of which it constitutes about 8 percent by weight and the most widely used nonferrous metal. The name is derived from the Latin word *alumen,* used to describe potash alum, or Al potassium sulfate, $KAl(SO_4)_2 \cdot 12H_2O$ [17]. Al has the atomic number 13 and a relative atomic mass of 26.98 amu [17]. The melting point is 933K and the boiling point is 2790K [17]. As shown in Figure 2.1. Al has a crystalline structure with a fcc crystal [21]. The lattice constant of Al = 0.405 nm [18]. All-natural Al is the stable isotope of Al-27. Metallic Al and its oxide and hydroxide are nontoxic [17]. Today, Al is mainly extracted from the ore bauxite via highly energy-consuming electrolysis, achieving Al of approximately 99,99% purity [18]. Al is an excellent conductor of heat and electricity [18].

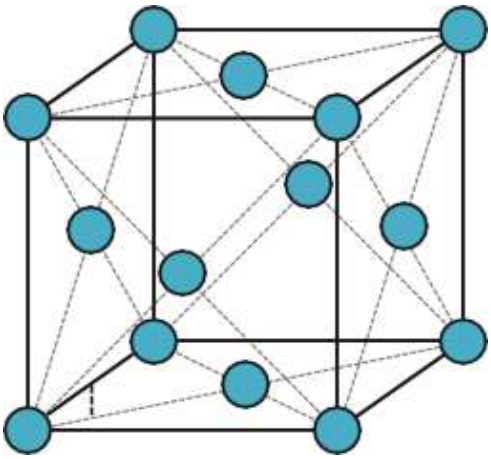

**Figure 2.1 :** Schematic representation of the fcc crystal structure of Al with a lattice constant of a = 4.05 Å [17]. The arrangement maximizes packing efficiency while maintaining symmetry [17]. Within the fcc lattice, some specific planes and directions exhibit maximum atomic density [17]. The {111} planes, which bisect the cube diagonally, are close packed in the fcc structure. Additionally, the <110> directions, which connect the centers of opposite faces of the cube, are close-packed, too [17].

Al boasts impressive mechanical and electrical properties, with a density of 2.7 $g.cm^{-3}$ and an electrical conductivity of 36 $mSmm^{-2}$ [18]. When it comes to metallization and interconnecting metals in microelectronic devices, Al is unequivocally the optimal choice [19]. Scientific research has demonstrated that unlike other metals, such as gold or copper, al obstructs the formation of deep traps in semiconductors like Si or Ge, making it the most scientifically sound and dependable option for electronic needs [19]. Additionally, when Al is used, it forms a natural oxide layer on its surface that acts as a passivation layer, protecting the underlying metal against oxidation and enhancing its performance [19]. This natural oxide layer provides a barrier against corrosion and prevents the formation of unwanted intermetallic compounds. Further, this oxide, possesses low electrical conductivity, making it extremely important to apply as an insulator in electronics and the chemical industry [19]. Al alloys with group 5 elements such as AlN, AlP, AlAs, and AlSb form compound semiconductors suitable for various electronic applications [19].

## 2.2 Germanium

In nature, Ge occurs only in mineral compounds like germanite, zinc ore, or coal. Clemens Winkler extracted in 1886 Ge by isolating from argyrodite. Ge is located in the group IV of the periodic tables of elements [20]. It has the atomic number 32 and a relative atomic mass of 72.64 amu. Ge has a crystal structure in a diamond with a lattice.In place of α 6.659 Å [20]. As

shown in Figure 2.2 the diamond lattice structure consists of two interpenetrating fcc lattices shifted by one-quarter of the lattice constant along the spatial diagonal. Each Ge atom forms a tetrahedron with its four surrounding neighbor atoms, which equals the number of valance electrons [20].

Ge is an indirect semiconductor with a band gap of $E_g$ = 0.66 eV at room temperature. The direct band gap at the Γ point is only 0.14eV larger with $E_{\Gamma 1}$ = 0.8eV, as shown in Figure 2.2b. Ge exhibits a notably higher absorption coefficient for incident photons than Si making it desirable for many optical devices. Due to its small energy band gap, Ge is becoming increasingly attractive for applications such as light-emitting diodes, lasers, and transistors [21]. In indirect bandgap semiconductors like Si and Ge, the process of electron excitation through photon absorption faces a significant challenge due to a disparity in momentum states [21]. Unlike direct bandgap materials where electrons can be excited across the bandgap with minimal momentum change, in indirect semiconductors, the momentum required to initiate electron transitions is substantially higher [21]. This discrepancy arises due to the differing momentum characteristics of electrons in the conduction band minimum, for Ge located at the L-point in the Brillouin zone, and those of photons emitted , often originating from the valence band maximum at the Γ-point [21]. As a result of this discrepancy, electron transitions involving photon absorption or emission in indirect bandgap semiconductors require a change in momentum, making the process less efficient compared to direct bandgap materials. This momentum mismatch leads to a lower probability of electron transitions and reduced optical absorption efficiency in indirect semiconductors, impacting their performance in optoelectronic devices such as photodetectors, and solar cells [21].

The first transistors, created by Shockley Bardeen and Brattain in 1947, were based on Ge due to their beneficial features [22]. Ge historically had an insignificant impact on transistor technology [22]. This is mostly because Si, unlike Ge, creates a high-quality oxide that functions as a good insulator and naturally passivates dangling bonds on the semiconductor-oxide interface [23]. In contrast to Si, the surface properties of Ge are predominantly governed by the quality of the oxide layer formed at the contact interface such as $Ge_2O_3$ and $Ge_2O$ [23]. oxide species present in addition to $GeO_2$ and GeO [23]. The creation of $GeO_2$ is particularly advantageous to lessen surface trapping because of the greater quality of the $GeO_2$/Ge interface [24].

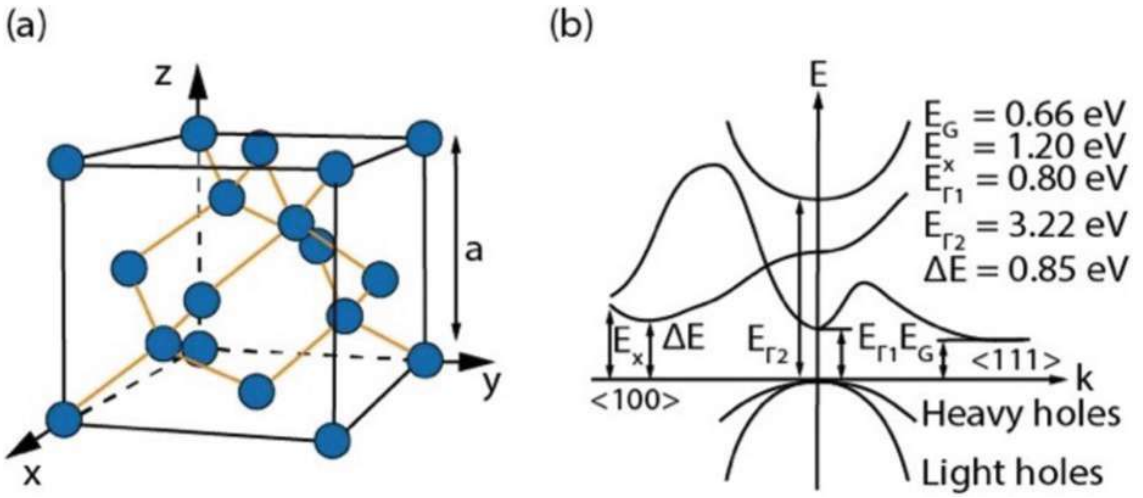


**Figure 2.2 :** a)The diamond cubic structure of Ge is depicted schematically in (b) The energy band diagram of Ge at 300 K displays a direct band gap at E = 0.8 eV and an indirect band gap $E_G$=0.66eV The energy gap between the top of the valence band and the conduction has a local minimum at the Γ-point, which is only 0.14 eV above its fundamental indirect band edge [21].

The electrical and optical properties of Ge are significantly impacted by changes in the oxide composition. However, none of these oxide species are stable at ambient temperatures [26]. The need for high-quality native oxide became less critical with the advent of high-dielectric materials used as gate oxides in sub-45 nm technology nodes [26]. Consequently, Ge has re-emerged as a promising semiconductor material for future high-performance devices.

In addition to its application in microelectronic and optoelectronic devices, Ge is widely used in various optical systems, including infrared spectrometers and fiber optics [26]. Furthermore, Ge oxides are utilized in the fabrication of wide-angle camera lenses and microscope objectives due to their high index of refraction and dispersion [27].

## 2.3 Ge on Insulator

GeOI stands out as a compelling integration platform in the realm of semiconductor science and technology [28]. By combining the exceptional charge carrier mobility of Ge with the structural advantages of SOI architecture, GeOI offers a promising pathway for advancing IC technologies [28]. Moreover, its remarkably low lattice mismatch with GaAs renders GeOI substrates exceptionally well-suited for the seamless integration of III–V compound transistors and optoelectronic functionalities [28]. This convergence of properties positions GeOI as a pivotal player in driving forward the frontiers of semiconductor research and enabling the realization of next-generation IC technologies with enhanced performance and functionality [28, 29].

## 2.4 Al-Ge System

In the realm of materials science, the exploration of Al-Ge heterostructure extends beyond the examination of individual characteristics to encompass their intricate interplay, nanowires. These nanoscale structures exhibit unique behaviors due to their high surface-to-volume ratio [30]. When Ge and Al are combined in NW configurations, their interactions and properties change significantly [30].The electrical and physicochemical properties of Al-Ge NWs are of particular interest, given their potential applications in nanoelectronics, photonics, and sensing devices. Understanding how these properties manifest at the nanoscale is crucial for harnessing the full potential of Al-Ge NWs in various scientific domains [30]. Moreover, the formation of Schottky contacts in Al-Ge NWs and their implications for device performance and functionality represent an area of active research [30]. By delving into the behavior of Al-Ge NWs, scientists and researchers gain valuable insights into the fundamental properties and potential applications of these materials at the nanoscale, driving advancements in nanotechnology and enabling the development of innovative nanoscale devices and systems [30].

Beyond only examining Ge and Al's characteristics, it is imperative to investigate how they interact with each other [30]. Consequently, the electrical and physicochemical properties of the Al-Ge material system are studied. When these materials come into contact, they form a Schottky contact, which will be briefly discussed [30]. The binary eutectic system of Al and Ge, as well as the solubility of the elements in one another, are discussed in the section on physicochemical properties.

### 2.4.1 Physico-Chemical Properties of Al-Ge

The phase diagram of the Al-Ge system is a crucial apparatus for understanding the thermal and structural behavior of alloys composed of Al and Ge across different compositions and temperatures. In this diagram, various phases and phase boundaries delineate the equilibrium conditions under which different phases coexist [31]. By studying the phase diagram of the Al-Ge system, one can anticipate phase transformations to optimize processing parameters for alloy manufacturing, thereby tailoring the alloy's material properties to meet specific application requirements [31]. Additionally, understanding the phase diagram is crucial for designing alloys with desired characteristics, such as mechanical strength, thermal stability, and electrical conductivity, in various engineering and industrial contexts [31]. The phase diagram of the eutectic system of the Al-Ge system proposed by McAllister and Murray is shown in

Figure 2.3. [31]. Ge has a melting point of about 938°C and Al, on the other hand, has a much lower melting point of about 660°C [31]. Al and Ge form a simple binary eutectic system that includes three solid phases. At lower temperatures, the phase diagram typically shows distinct regions corresponding to different phases, such as the α, Ge, and liquid, as well as areas of solid solution and intermetallic compounds. [31]. The Al-Ge binary alloy is a basic eutectic system where the position of the eutectic point is approx. [31]. Eutectic composition about 52% Ge and 48% Al and eutectic temperature of Al-Ge approximately 421°C. At this temperature and composition, the liquid Al-Ge alloy solidifies into a mixture of pure Ge and Al phases simultaneously.The mutual solubility of both elements is extremely on the implantation of Al into Ge is a common technique used in semiconductor device fabrication to introduce dopant atoms into the Ge substrate [31]. By understanding these characteristics, researchers can design ion implantation processes to introduce controlled amounts of Al dopants into Ge substrates while minimizing undesired effects such as phase segregation or the formation of unwanted compounds [31]. Al should have a high solid solubility of 4x $10^{20}$ $cm^{3}$ and is, therefore, suitable as a p-type dopant [31].

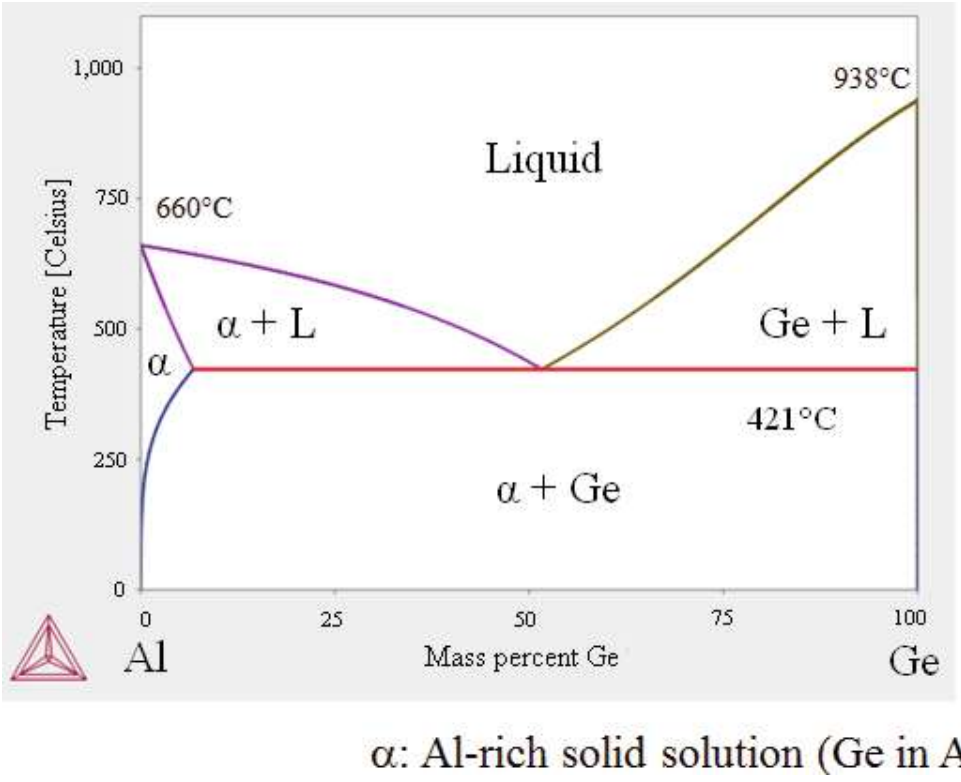


**Figure 2.3 :** The Al-Ge phase diagram shows a eutectic temperature of 420°C [31]. In this diagram, various phases and phase boundaries delineate the equilibrium conditions under which different phases coexist [31].

### 2.4.2 Understanding the Diffusion Mechanism in the Al-Ge Solid State System

Diffusion is a process resulting from the random motion of molecules by which there is a flow of matter from a region of high concentration to a region of low concentration [31]. It is usually a thermally driven process, which can be described by an Arrhenius or activation type of law if diffusion occurs at a state of thermodynamic equilibrium [31]. This implies that to achieve an equilibrium density of intrinsic point defects in the lattice, the diffusion time at a given temperature must be of sufficient duration [31]. This is in contrast to non-equilibrium diffusion, such as the phenomenon known as Transient Enhanced Diffusion, which is facilitated by a non-equilibrium population of point defects resulting from ion implantation [31]. The subsequent discussion will present evidence indicating the occurrence of abnormally rapid dopant diffusion in Ge, such as diffusion that is accelerated by radiation. However, the focus of this section will be on elucidating the theoretical framework for equilibrium thermal diffusion [31]. A random walk is a conceptual model used to describe the movement of particles within a material. In this model, particles move randomly and independently of each other, with each step being determined solely by chance [32]. This stochastic behavior mimics the unpredictable nature of molecular motion driven by thermal energy [32]. Formula 2.1 provides a detailed formal explanation of random walk:

$$R_N = a\sqrt{N} \tag{2.1}$$

$R_N$: This represents the characteristic radius or size of the structure that contains N units. It is typically measured in units of length nanometers , $a$ is a constant that relates to the specific system or context [nanometer]

The predominant mechanism relies on point defects within the crystalline solid, which facilitate the movement of atoms through the crystal lattice [33]. These defects enable the integration of atoms into interstitial sites within the host lattice, a phenomenon referred to as "interstitial solid solutions." Here, atoms, considerably smaller than those of the solvent, become integrated into the lattice while preserving its overall geometry [33]. The interstitial mechanism involves the migration of surplus atoms between interstitial sites within a lattice structure [33]. Conversely, the vacancy mechanism entails atom diffusion to neighboring vacancies within the lattice. Vacancies, the most common type of thermally induced atomic defects, are prevalent in metallic and ionic crystalline materials [33]. The dominance of the vacancy mechanism is also acknowledged in substitutional solutes, wherein the solute atoms are of comparable size to the

host atoms [33]. In a crystalline structure, the presence of agglomerates consisting of several vacancies, such as di- or tri vacancies, can be observed [33]. These clusters exhibit diffusion characteristics akin to monovacancies, albeit typically demonstrating greater mobility [33]. A diffusion vehicle comprises an interstitial atom roughly matching the size of lattice atoms. The process involves substituting an adjacent atom on a lattice or substitutional site, subsequently relocating it to another interstitial point [33]. The synchronized motion of both atoms signifies the presence of a collective process. Interdiffusion refers to the diffusion of atoms into a dissimilar material, expediting the equalization of concentration gradients [33]. The case is described by Fick's Laws which is employed to elucidate the flow of diffusing particles [33]. It is alternatively referred to as steady-state diffusion [33].

$$J = -D\nabla C \tag{2.2}$$

$$D = \frac{D_o e^{-E} a}{RT}, \tag{2.3}$$

$D$: Diffusion coefficient [$m^2/s$], $C$: Concentration gradient[$mol/m^3$], $J$ : Diffusion Flux [particles per unit area per unit time], $D_o$: Diffusion Constant, [$m^2/s$], $R$: Gas Constant, [J/mol·K], $T$: Temperature [K], $E_a$: Activation Energy joules [J],

In the absence of external sources or sinks, the number of diffusing particles remains constant in isolated systems during a diffusion process [34]. The formulation of a continuity equation is possible due to its adherence to the law of conservation [34]:

$$\nabla . \mathrm{J} = \frac{\partial \mathrm{C}}{\partial \mathrm{t}} \tag{2.4}$$

In binary alloys, each constituent material often has its diffusion coefficient. This leads to different diffusion fluxes for each material when Fick's first law is applied. Thus, understanding these variations helps to predict and control diffusion processes in the alloy [34]. The inequality between diffusion coefficients causes a displacement of the boundary between the two phases. This shift results from the overall movement of mass during the process of interdiffusion [34].

To preserve local equilibrium during the process of interdiffusion, lattice sites are generated on one side and removed on the other side [34]. The process of creating and eliminating vacancies is responsible for this achievement. The phenomenon under discussion is commonly referred to as the Kirkendall effect, which was first observed in the 1940s within a diffusion pair consisting of copper and brass [34]. The movement of the interface can be expressed by the

Kirkendall velocity $V_K$ in terms of the two intrinsic fluxes, $j_A$ *and* $j_B$, and their partial molar volumes $V_A$ *and* $V_B$ [42]*:*

$$V_K = -(VA_{jA} + VB_{jB}) \tag{2.5}$$

$$V_K = VB(D_B - D_A)\frac{\partial CB}{\partial x} \tag{2.6}$$

A simple description of isothermal diffusion in a binary substitutional alloy by an interdiffusion coefficient can be introduced with

$$D = C_B VBD_A + C_A\, VAD_B \tag{2.7}$$

Thus, it is possible to calculate the intrinsic diffusivities of both components by measuring the interdiffusion coefficient and the velocity of the Kirkendall plane. For abrupt interfaces between two material regions with different concentrations, the concentration profile can be approximated by a Heaviside step function $H(x)$. With Fick's first law, this results in a diffusion flux at the interface introduced with

$$J_{it}(x) = -D(C_B - C_A)\delta(x) \tag{2.8}$$

With the Dirac delta function $\delta(x)$ as the derivative of this step function [34].

Typically, the rate of diffusion displays temporal variability due to different rate-limiting mechanisms [35].

The relationship between the diffusion length L and the time t is directly proportional [35]. If the reaction between the metal reservoir and the NW is constrained by the surface area, the diffusion length is also influenced by the radius R of the NW, following the relationship L vs. $R^{-1}t$ [35]. When the reaction is limited by the surface area of the NW, the diffusion length is also influenced by the NW's radius, following the relationship: $L \propto R^{-1}t$ [35]. This means that as the NW gets smaller, the diffusion length increases more rapidly with time [35]. In instances where reaction durations are extended, the atoms involved in diffusion must traverse considerable distances within the material [35]. Consequently, diffusion becomes the constraining force in these scenarios. Hence, the magnitude of the length is contingent upon the square root of the duration [35]. The dependence of the diffusion of exchanged atoms on the surface is a significant factor in determining the value of L [35]. Additionally, the radius of the

NW also influences L, resulting in a relationship where L is a function of both the surface and NW radius [35].

| **Al-Ge exchange regimes** | *Diffusion length L* |
|---|---|
| **Metal reservoir limited** | $\sim R^{-1}t$ |
| **Interfacial exchange limited** | $\sim t$ *(independent of R)* |
| **Volume diffusion limited** | $\sim t$ *(independent of R)* |
| **Surface diffusion limited** | $\sim \underline{t}$ |

**Table 2.1 :** Potential diffusion rate-limiting processes of thermal exchange reaction and their influence on the "diffusion length" concerning the time t and the radius R of the NWs. The "diffusion length" typically refers to the average distance that atoms of one substance (e.g., Al) diffuse into the other substance (e.g., Ge) over a given time or under specific conditions. The diffusion length can vary depending on the exchange regime [34].

In most binary metal-semiconductor systems investigated for solid-state diffusion of metal into a semiconductor, the metal atoms are integrated into the lattice of the semiconductors, resulting in the formation of an intermetallic compound [35]. The study demonstrated the occurrence and spread of several silicide and germanide phases, such as those involving Ni [35], Cu [35], or Mn[35] within Si or Ge NWs [35]. The integration of nanoelectronics with CMOS technology is significantly facilitated by the utilization of these systems and their meticulous process control [35]. The primary impetus for the formation of intermetallic compounds is often to enhance the quality of contact between metal and semiconductor junctions. However, it should be noted that these quasi-metallic structures continue to have elevated levels of contact resistivity in comparison to pure metals [35]. Nevertheless, the substitution of metal atoms within a semiconductor NW through a heat-induced solid-state process, without the creation of intermetallic compounds, has only been documented in the binary Al-Ge [35] and pseud-binary Au-GaAs [35] systems. Hence, the semiconductor NW, typically synthesized via the VLS technique, is interfaced with metal contacts that exhibit significantly larger volumes in comparison to the nanowires [35]. Subsequently, a thermal annealing process is employed to initiate the exchange reaction. During the annealing of Al-Ge alloys, the material is heated to specific temperatures to activate dopants and rectify defects within the crystal structure [36].In the context of Al-Ge NWs, annealing plays a crucial role in optimizing their electrical and structural properties for various applications in electronics and photonics [36]. During annealing, the Al-Ge NWs are typically heated to temperatures below the melting point of the

alloy (See Figure 2.3). However, the temperature must be sufficiently high to facilitate diffusion processes, allowing Al and Ge to redistribute within the nanowires.The Al-Ge interface that is now developing exhibits a high degree of sharpness or perhaps atomic-level abruptness, despite the significant lattice mismatch between the two compounds. Moreover, there are no observable faults present at the interface [37].

The replacement of Ge with Al is attributed to the asymmetric diffusion behavior observed in this binary material system [38], Following the findings presented in Table 2.2, a distinct contrast in diffusion coefficients emerges between Ge in Al and the self-diffusion of Al, relative to the diffusivity of either element in Ge [38]. Notably, the diffusion coefficients of Ge in Al and the self-diffusion of Al exhibit considerably higher values compared to the diffusion rates observed for either Al or Ge in Ge [38]. Consequently, this disparity facilitates the diffusion of Ge atoms into the larger Al pad [38].

| ` | **Al** | **Ge** | **Al** | **Ge** |
|---|---|---|---|---|
| in: | **Al** | **Al** | **Ge** | **Ge** |
| $E_a$ **(kJ/mol)** | 123.5 | 121.3 | 332.8 | 303 |
| $D_0$ **($cm^2/s$)** | 0.137 | 0.48 | 1000 | 24.8 |
| $D$ **($cm^2/s$)** | $3.57 \cdot 10^{-11}$ | $1.86 \cdot 10^{-10}$ | $1.5 \cdot 10^{-23}$ | $7.61 \cdot 10^{-23}$ |

**Table 2.2 :** Activation energy $E_a$ and frequency factor $D_0$. Both activation energy and frequency factor are crucial parameters in the Arrhenius equation, which describes the temperature dependence of reaction rates or diffusion coefficients. The Arrhenius equation relates the rate constant (or diffusion coefficient) to temperature, activation energy, and the frequency factor, providing insights into how these parameters influence the kinetics of chemical reactions or diffusion processes at different temperatures [39].

Equation 2.9, derived from Fick's second law of diffusion, holds particular significance in elucidating the exchange mechanism of Al-Ge during the annealing process [38]. By applying this equation, one can quantitatively analyze how the diffusion length of Ge within Al evolves during annealing [38].

$$L = \sqrt{2Dt} \tag{2.9}$$

L:Diffusion length , D: diffusion coefficient , t time ,

This phenomenon indicates the presence of a process limited by diffusion, emphasizing the critical role of diffusion dynamics in governing the observed behavior [38]. The exchange

reaction comes to a halt when the concentration of dissolved Ge in the Al exceeds the solubility limit within the solid phase [38]. This critical threshold is usually reached at approximately

1.69 % at a temperature of 400°C [38]. It is noteworthy that the presence of Al atoms in the remaining Ge segment cannot be observed, as the diffusion coefficient of Al in Ge is exceptionally low [38].

The phenomenon of effective exchange in Al-Ge can be observed within a temperature range of 350°C to 410°C, with diffusion speeds ranging from approximately 3 nm/s to 20 nm/s [38]. The process of Al-Ge exchange can be seen in Figure 2.4 [38]. In this process, Al atoms diffuse from the contact pad into the Ge-NW [38].

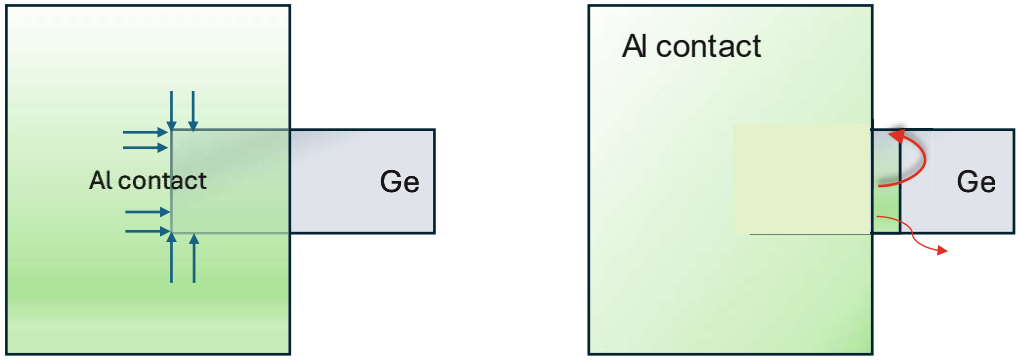


**Figure 2.4 :** İllustrates the phenomenon of solid-state diffusion involving the migration of Al atoms into a Ge. In this process, Al atoms diffuse from the contact pad into the Ge-NW [38]. By employing this technique, it is possible to fabricate Al-Ge-Al heterostructures featuring Ge channel lengths as small as sub-10 nm, regardless of the lithography process used and its spatial resolution [38].

### 2.4.3 Electronic Properties of Semiconductors

Semiconductors are compounds with electrical conductivity levels lying between those of metals and insulators [40]. Indeed, to discern between metallic and semiconducting behavior, analyzing the relationship between conductivity and temperature is a dependable approach. the conductivity in general depends on number of charge carriers mobility lattice imperfections, impurity atoms, grain boundaries, or thermal lattice agitation [40]. In metals, the carrier concentration remains constant with increasing temperature, while lattice motion intensifies [40]. This leads to a decrease in conductivity, influenced by both the quantity of carriers and their mobility [40]. In the Fugure 2.5 shows the energy levels of heavy holes, light holes, and the split-off band, often observed in materials like Si, Ge, and GaAs. The split-off band is a result of spin-orbit coupling, which lowers the energy of one set of valence bands. Conversely,

in semiconductors, carrier quantity significantly increases with rising temperature [40]. In the Fugure 2.5 shows the energy levels of heavy holes, light holes, and the split-off band, often observed in materials like Si, Ge, and GaAs. The split-off band is a result of spin-orbit coupling, which lowers the energy of one set of valence bands. Thus, despite the elevated lattice motion, conductivity increases with increasing temperature. The electrical characteristics of solids are primarily governed by their crystal lattice structure [40]. For instance, the crystal lattice of Ge as mentioned in Section 2.2, exhibits a diamond lattice with a lattice constant of 6.659 Å. The band structure (E-k relation) of different crystals can be derived by solving the Schrödinger equation using Bloch's theorem [40]. The establishment of broad, continuous energy bands arises from the proximity of atoms within the material, a fundamental characteristic that profoundly influences its electronic structure. These energy bands serve as the foundation for defining the permissible states available for electrons to occupy within the material [40]. However, it is noteworthy that there can exist energy regions between these bands where no permissible electronic states are accessible, thereby delineating the boundaries of electron motion within the material's electronic structure [40]. If the Fermi energy falls within a specific range, the material can be classified as either a semiconductor or an insulator, depending on its proximity to the adjacent energy bands known as the valence band and the conduction band [40]. These entities are of significant relevance because of their role as the main facilitators of charge carrier transportation. Semiconductors are classified as direct or indirect based on the alignment of their valence band maximum and conduction band minimum in momentum space [40]. For instance, semiconductors like GaAs are considered direct because these two energy extrema occur at the same momentum [40]. On the other hand, semiconductors like Si and Ge are categorized as indirect since their valence band maximum and conduction band minimum do not align in momentum space. The region separating these bands is referred to as the band gap [40].

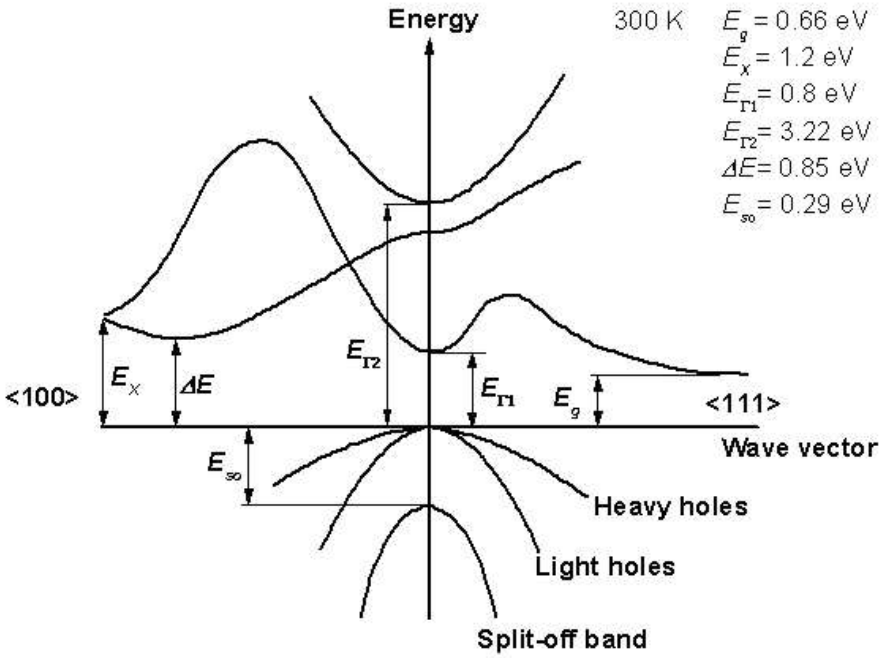


**Figure 2.5 :** The band structure characterizes the electron dynamics inside the given material, specifically delineating the energy levels associated with different momenta [49]. If the dispersion relation has a parabolic shape, like that observed in free space but with varying curvature, it can be effectively represented using the same mathematical framework by substituting the electron's mass with its effective mass. In the context of the conduction band, this provides [41].

$$E(k) = E_C + \frac{\hbar^2 . k^2}{2m*} \tag{2.10}$$

In the given context, $E_C$ represents the minimum energy level of the conduction band. The variable denotes the reduced Planck constant $\hbar$, which is mathematically expressed as the regular Planck constant (h) divided by 2π [42]. The effective mass approximation, commonly referred to as such, applies to a majority of widely used semiconductors in proximity to the band gap [42]. An analogous relationship may be formulated for vacancies in the valence band, wherein heavy and light holes are often characterized by two distinct effective masses [42].

The carrier concentration is an essential parameter for characterizing the carrier transport properties as it pertains to the occupation of the conduction and valence bands [42]. To determine this quantity [42], it is necessary to possess knowledge about the density of states D (E), which characterizes the number of energy states within a given energy range. Given the assumption of parabolic band edges, where the effective mass approximation is valid, the expression is given by [42].

$$D(E) = \left(\frac{2m^*}{k^2}\right)^{\frac{3}{2}} \frac{(E-E_C)^{\frac{1}{2}}}{2\pi^2} \tag{2.11}$$

This assumption holds for ideal three-dimensional systems and serves as a reasonable approximation for most semiconductor materials [42]. Figure 2.6(b) illustrates the Fermi distribution function $f(E)$ which characterizes the overall occupation of energy levels about temperature. It is given by.

$$f(E) = \frac{1}{1+\exp\left(\frac{E-E_F}{k_B T}\right)} \tag{2.12}$$

Where$k_B$ is the Boltzmann constant and T is the temperature [42]. The Fermi level is defined as the energy where at T= 0 K all energy states below are filled and above remain empty. To obtain the carrier concentration n in the conduction band, the integral of $D(E)$ and $f(E)$ is calculated for the desired energy range as illustrated in equation 2.14 [44].

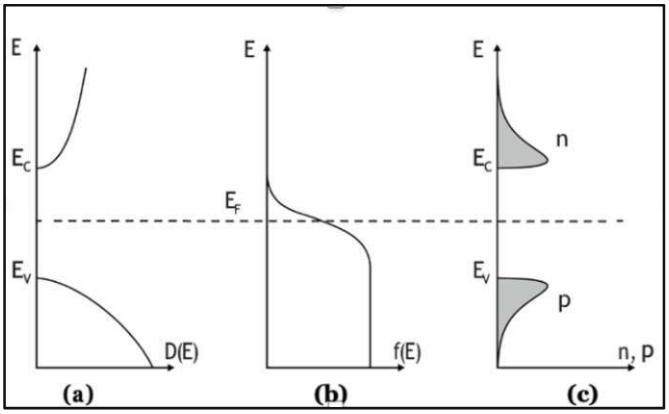


**Figure 2.6 :** (a) Density of states, which describes the number of available electronic states per unit volume at a given energy level in a material. In a semiconductor, the DOS typically shows an energy bandgap between the valence band (where electrons are bound to atoms) and the conduction band (where electrons are free to move). Below the bandgap, the DOS in the valence band is filled with electrons, while above the bandgap, the DOS in the conduction band is empty [44], (b) Fermi distribution which describes the probability of finding a particle (such as an electron) in a particular energy state at a given temperature in a system obeying Fermi-Dirac statistics. In an intrinsic semiconductor at thermal equilibrium, the Fermi level lies exactly in the middle of the bandgap, and the Fermi-Dirac distribution function determines the occupation probability of electronic states at different energy levels [44] and (c) carrier concentration which the carrier concentration refers to the number of charge carriers (electrons and holes) per unit volume for an intrinsic semiconductor in thermal equilibrium at finite temperature [44].

$$n = \int_{E_c}^{\infty} D(E) f(E) dE \tag{2.13}$$

By substituting the Boltzmann distribution in place of the Fermi distribution, which is a suitable approximation for non-degenerate semiconductors ($E - E_F * k_B T$), it is possible to derive a straightforward analytical solution for this integral [45]:

$$n = N_C \ \exp\left(\frac{E_F - E_C}{k_B T}\right) \tag{2.14}$$

With the effective density of states in the conduction band denoted as $N_C$. Similarly, the concentration of holes in the valence band can be determined by calculating [45]:

$$p = N_V \ \exp\left(-\frac{E_F - E_C}{k_B T}\right) \tag{2.15}$$

with $N_V$ the effective density of states in the valence band. It holds that [45]:

$$np = N_C N_V \ \exp\left(-\frac{E_g}{k_B T}\right) \tag{2.16}$$

The mass-action law refers to the property of being independent of the Fermi level [45]. The symbol "$E_g$" represents the band gap energy, which is determined by the difference between the $E_C$ and $E_V$ [45].

In the context of intrinsic semiconductors under thermal equilibrium conditions, it is seen that the number of electrons (n) is equal to the number of holes (p). This equality arises since for each electron generated in the conduction band, a matching hole is created in the valence band [45].

$$n_i = \sqrt{N_C \ N_V} \exp\left(-\frac{E_g}{2k_B T}\right) \tag{2.17}$$

Another significant attribute of a semiconductor is referred to as the intrinsic carrier density. According to the reference, at a temperature of 300 K, the value of $n_i$ for the element Ge is equal to 2.33 x $10^{13}$ $cm^{-3}$ [45].

As evidenced in equation (2.19) the parameter $n_i$ exhibits an exponential relationship with temperature, thereby serving as the primary factor that restricts the temperature range of semiconductor devices based on their band gap [45].

The intrinsic Fermi level is determined to be:

$$EFi = \frac{E_F + E_C}{2} + \frac{Tk_B}{2} + \ln\left(\frac{N_V}{N_C}\right) \tag{2.18}$$

which is for most semiconductors close to the middle of the band gap. The manipulation of carrier density can be achieved through the intentional introduction of a specific quantity and kind of impurity atoms, a process commonly referred to as doping [45].

As an illustration, when a group V atom replaces a Ge atom within the crystal lattice, an extra electron is introduced, exhibiting a relatively weak connection. This can be easily ionized resulting in an additional electron. Consequently, there is a displacement of the Fermi level towards higher energy levels [45]. It was doping with a group III element resulting in the generation of an extra hole and thus reduction of the Fermi energy. In a more accurate manner, and assuming the approximation that all dopant atoms have undergone ionization [41].

$$E_F = E_c + k_B\, T\left(ln\frac{N_D}{N_V}\right) \tag{2.19}$$

$$E_F = E_V - k_B\, T\left(ln\frac{N_A}{N_V}\right) \tag{2.20}$$

for group III (p-type) doping with $N_D$ and $N_A$ being the doping concentrations of donors and acceptors respectively.

In summary, at finite temperature and thermal equilibrium, the density of states, Fermi distribution, and carrier concentration collectively describe the behavior of electrons and holes in an intrinsic semiconductor, providing insights into its electrical and optical properties [45].

## 2.5 Negative Differential Resistance

NDR is an unconventional transport phenomenon in semiconductor devices where the current-voltage relationship deviates from the typical Ohm's Law observed in resistors [46]. Unlike traditional devices driven by diffusion and drift currents, NDR devices exhibit non-monotonic behavior due to quantum-mechanical tunneling across energy barriers [46]. This tunneling enables rapid switching and sharp transitions between states, making NDR devices attractive for high-speed applications requiring precise control over electronic states [46].

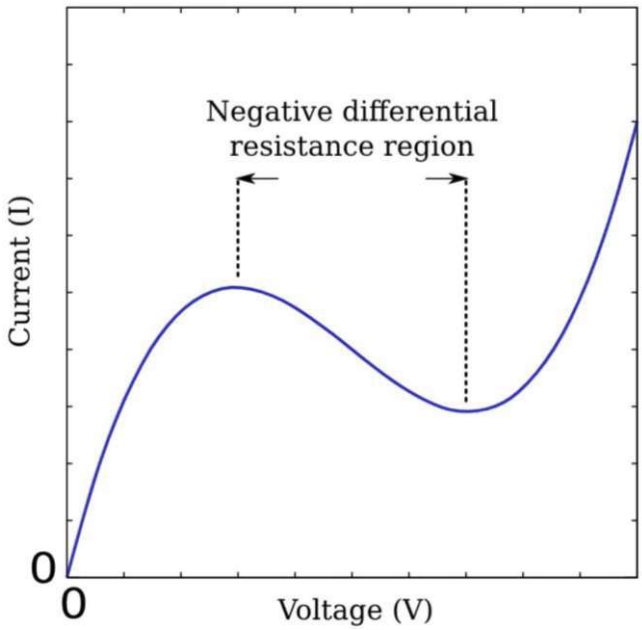


**Figure 2.7 :** In the current-voltage- (I-V) curve of a device with negative differential resistance initially, as the voltage applied across the device is increased [47], the current through the device also increases, following a typical positive slope as seen in conventional resistors or diodes [47]. At a certain voltage threshold, known as the peak voltage (Peak), the device enters the NDR region. In this region, as the voltage continues to increase beyond the Peak, the current passing through the device starts to decrease [47]. This negative slope is characteristic of NDR behavior. It's essential to note that in this region, increasing the voltage leads to a decrease in current, which is contrary to the behavior of most electronic components [47].

$$r_{diff} = \frac{dV}{dI} \tag{2.21}$$

When considering the V and I, it is seen that it assumes a negative value within that region.

NDR can arise from many mechanisms, including resonant tunneling, self-heating, charge trapping, and the transferred electron effect. The transferred electron effect, also recognized as the Gunn effect, is particularly well-established in GaAs [48].

NDR comes in two variants: intrinsic and extrinsic. One type is the VCNR, also referred to as short-circuit stable or "N" type, [49] Figure 2.8(a) typically exhibits a graph in the shape of the letter "N," featuring only one negative resistance region [49]. As voltage increases, there is a positive resistance resulting in a gradual increase in current until it reaches a maximum value (i1). The current then decreases in the region of negative resistance to a minimum value (i2) before increasing again [49]. Devices that exhibit this type of negative resistance include the tunnel diode, resonant tunneling diode, lambda diode, Gunn diode, and dynatron oscillators. The CCNR, also known as open-circuit stable or "S" type. In this type, the voltage is a single-

valued function of the current, while the current is a multivalued function of the voltage. According to Figure 2.8(b), when a negative resistance region is present, the graph of a circuit exhibits a characteristic curve in the shape of the letter "S". Such behavior is observed in a variety of electronic devices, including but not limited to the IMPATT diode, unijunction transistor, silicon-controlled rectifier , and other thyristors, electric arc, and gas discharge tubes [49]. This phenomenon has significant implications for the design and analysis of electronic circuits and is therefore of great academic interest to researchers and engineers in the field [49].

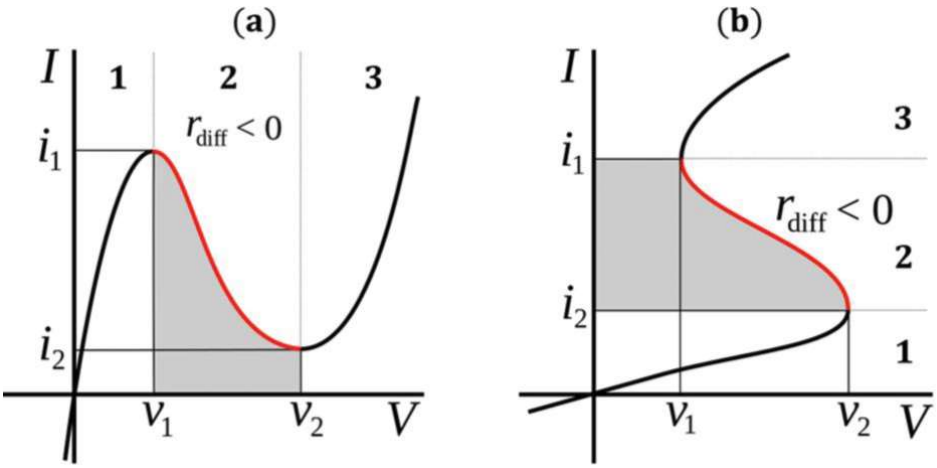


**Figure 2.8 :** (a) N-type negative differential resistance (VC-NDR). VC-NDR occurs when the current decreases as the voltage increases beyond a certain threshold. This behavior can arise due to quantum mechanical effects or electron transit-time effects in semiconductor devices (b) S-type negative differential resistance (CC-NDR), CC-NDR occurs when the current decreases as the voltage across the device increases beyond a certain threshold [49].

The schematic illustration described in Figure 2.9 depicts the transferred electron effect in Ge [50]. In this phenomenon, electrons are scattered from the L-point minimum to the X-point minimum. The X-point minimum is characterized by higher energy and lower mobility compared to the L-point minimum [50]. When an electric field is applied to the semiconductor, electrons are accelerated in the direction of the field. In the case of Ge, as electrons move through the crystal lattice under the influence of the electric field [50], they can gain enough energy to transition from the lower energy L-valley to the higher energy X-valley through scattering processes [50]. This scattering process, known as intervalley scattering, leads to a reduction in electron mobility because the X-valley typically has lower mobility compared to the L-valley. As a result, the overall conductivity of the material can decrease, leading to phenomena such as NDR in certain device configurations [50].

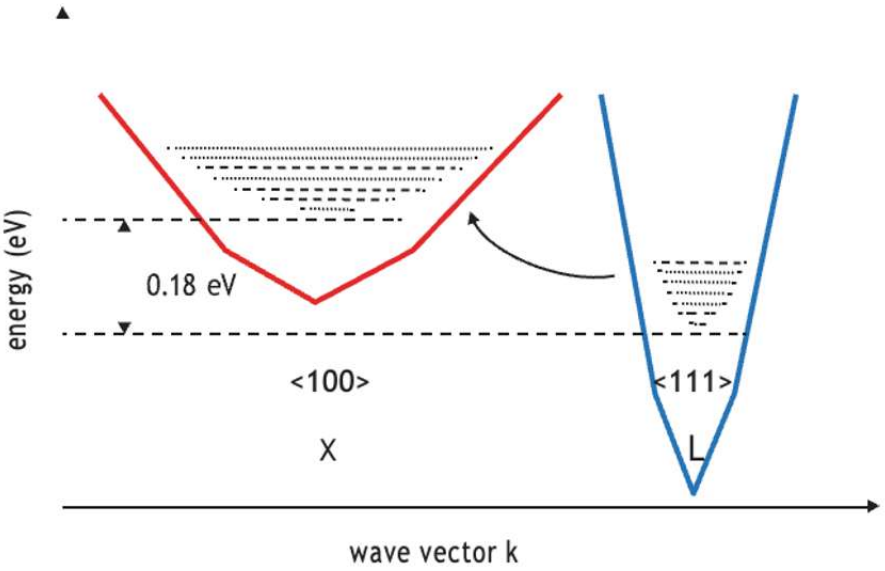


**Figure 2.9 :** Schematic illustration of the transferred electron effect in Ge. The transferred electron effect is a phenomenon observed in certain semiconductors, including Ge where the mobility of electrons exhibits a peculiar behavior under certain conditions. In the band structure of Ge, there are multiple valleys in the conduction band. The valleys of interest here are the L-valley and the X-valley. The L-valley is the lowest energy conduction band valley, while the X-valley is higher in energy. The X-valley typically has a lower mobility for electrons compared to the L-valley. Electrons from the L-point minimum are scattered to the X-point minimum, which has higher energy and lower mobility [50].

# 3. Experimental Part

Standard semiconductor manufacturing techniques are utilized to precisely define the dimensions, geometries, and spatial arrangements of Ge structures and Al pads on the GeOI wafer, ensuring precise fabrication [51].

In the experimental part, a GeOI wafer is utilized for device fabrication. This wafer comprises a single crystal Ge device layer oriented along the ⟨100⟩ direction, measuring 87 nm in thickness, situated atop a 150 nm thick $SiO_2$ insulator layer. Additionally, a doped Si handle wafer with a thickness of 525 µm supports the structure. A 60 nm thick $SiO_2$ layer serves as a protective coating to safeguard the underlying Ge layer from oxidation and contamination. Preceding fabrication, the GeOI substrate undergoes preparatory steps involving the removal of its protective $SiO_2$ layer using a buffered HF wet etching method.

## 3.1 Fabrication of Ge Micro and Nanostructures

Preceding fabrication, the GeOI substrate undergoes preparatory steps involving the removal of the protective $SiO_2$ layer using a buffered HF wet etching [52]. Optical photolithography techniques then define the precise contours of Ge device structures. This process involves first spin-coating the substrate with a TI Prime adhesion promoter, which is baked at 120°C for 2 minutes to enhance adhesion of the resist [53]. Next, the AZ5214 photoresist is spin-coated onto the substrate and baked at 100°C for 1 minute to harden the resist. See in Figure 3.1(a).

After the initial preparation, a 1:1 Cr mask is carefully aligned with the predefined patterns on the substrate and UV exposure is applied to transfer these geometries precisely onto the surface (Figure 3.1(b)). Subsequently, RIE is performed using $SF_6$ and $O_2$ gases to etch the Ge layer with high precision (Figure 3.1(c)). The underlying $SiO_2$ layer serves as an etch stop, ensuring controlled anisotropic etching profiles at a rate of 2.5 nanometers per second [53]. Finally, any residual photoresist is removed using a solvent mixture of acetone and isopropyl alcohol, thereby preparing the substrate for subsequent experimental processes and characterization See in Figure 3.1(d).

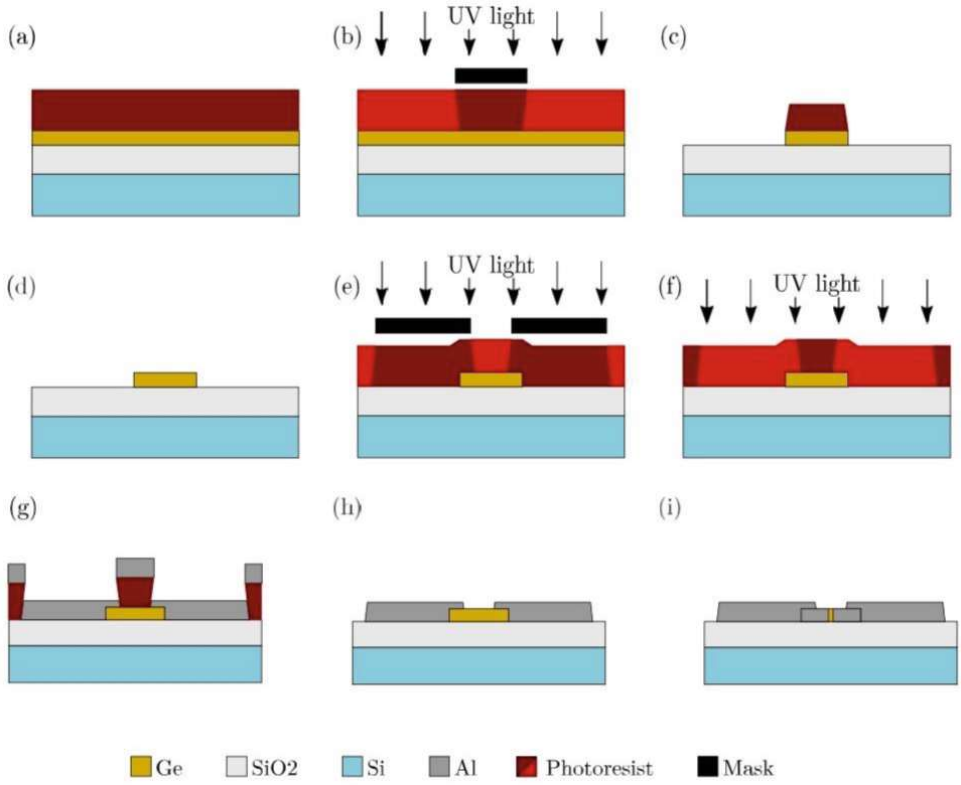


**Figure 3.1 :** Fabrication of monolithic Al-Ge heterostructures: (a) GeOI wafer with optical photoresist. (b) Pattern exposure with contact lithography. (c) Ge layer on the developed sample etched with RIE and (d) the resist is stripped. (e) For the fabrication of the Al contact pads, the photoresist is exposed using a negative mask. (f) reversal bake with subsequent flood exposure to invert the structure. (g) Al deposition for contact formation. (h) The lift-off is performed in acetone. (i) Thermal Al-Ge exchange to form a short Ge channel [53].

### 3.1.1 Al Contact Formation

In the subsequent experimental stages, the Ge structures undergo a process to establish contact with macroscopic Al pads [54]. Initially, an image reversal lithography method is employed, resulting in the formation of resist sidewalls with undercut features that are advantageous for the subsequent metal lift-off procedures [54]. This approach, successful in patterning the Ge device structures, is replicated for the fabrication of Al pads.

The pattern for the Al pads is transferred onto the sample, which has been spin-coated and pre-baked, using a contact mask and exposed to UV irradiation for 4 seconds (Figure 3.1e) [54]. Following this step, thermal treatment at 120°C alters the resist properties: exposed regions lose their ability to develop, while unexposed areas retain their photoactive properties [54]. Subsequently, a flood exposure lasting 20 seconds and a further bake at 120°C ensures uniform exposure of the entire sample to UV light (Figure 3.1f), facilitating the development of previously unexposed resist areas [54].

Sputtering is an essential technique for thin-film deposition, which involves the ejection of atoms from a target material through ion bombardment. In this work, magnetron sputtering was specifically employed for the fabrication of the samples [55]. Magnetron sputtering utilizes an inert gas plasma to bombard and accelerate ions toward the target material, which is performed in a vacuum chamber at low pressures to extend the mean free path of the ejected atoms, enhancing their likelihood of reaching the substrate [55].

The sputtering process was conducted using the "VonArdenne LS 320 S" system, which supports high-frequency Ar plasma for the deposition [55]. This system accommodates up to six targets and six sample holders, allowing for the sequential deposition of multiple material layers without exposure to ambient conditions between steps [55]. Once the vacuum is achieved, Ar is introduced, and the high-frequency field generator is activated to ignite the Ar plasma [55]. Deposition commences with the opening of a shutter between the target and the substrate, with the film thickness controlled by the sputtering rate and deposition duration [55].

Following the deposition of thin the Al films, a lift-off process is employed to define the final structures. After sputtering, the sample is treated with a solvent mixture to selectively dissolve the photoresist and any material deposited on top of it [53]. This process effectively removes the unwanted film, leaving behind the precisely defined Al pattern on the substrate [53].

## 3.2 Formation of Monolithic Al-Ge-Al Heterostructures with Thermal Exchange Reaction

The process involves utilizing thermal annealing to precisely adjust the length of the Ge channel, enabling the fabrication of nanoscale Ge devices that surpass the inherent limitations of optical lithography [56]. Metal diffusion into the Ge structure is achieved through RTA using a "UniTemp UTP 1100" system [56]. This process involves heating the sample to a controlled temperature of 350°C within a quartz chamber using 18 kW infrared lamps for a precisely timed duration of 240 seconds. The annealing process is performed in two cycles, each lasting 120 seconds. Crucially, this annealing is carried out in a protective atmosphere to forming gas consisting of 90% $N_2$ and 10% $H_2$ to prevent oxidation and maintain optimal process conditions [56]. During annealing, the interaction at the metal-semiconductor interface facilitates the migration of the metal atoms along the Ge structure, effectively shortening the length of the Ge segment [56].

After annealing, SEM examination to measure the length changes induced by the annealing. This iterative process continues until enough data points are collected to comprehensively analyze the diffusion kinetics. Throughout the experimental sequence, SEM imaging is crucial for real-time monitoring and verification of the annealing process's effectiveness and consistency [57].

## 3.3 Wet Chemistry Process for Ge Thinning

To reduce the thickness of the Ge structures, selective wet chemical etching is employed. This process utilizes a diluted solution of $H_2O_2$ and water [58]. Under these conditions, etch rates 40 nm/min is anticipated. For achieving optimal results, a rather slow etching rate was selected to ensure sufficient process control and to produce uniform structures [58]. Choosing a slower etch rate is essential for precise control over the etching process, which helps minimize surface roughness and ensures consistent uniformity across the wafer. This careful adjustment of the etch rate is crucial to preserving the structural integrity and performance of the Ge layers [58]. Furthermore, as Al exhibits minimal reactivity with the $H_2O_2$ solution, this etching procedure is compatible with fully-featured devices. This compatibility allows the process to be applied after the formation of contacts and the Al-Ge exchange [59].Consequently, it offers a significant advantage in terms of process integration, enabling precise Ge layer thinning even in the presence of pre-fabricated aluminum contacts [59]. By leveraging this selective wet chemical etching approach, it becomes feasible to achieve the desired reduction of the Ge thickness, ensuring both process control and uniformity, which are paramount for high-performance semiconductor device fabrication [59].

### 3.3.1 Electron Beam Lithography

Electron Beam Lithography (EBL) is an advanced method used to create precise patterns with very small features, down to the few nanometer scale [60]. It works by focusing an electron beam directly onto a surface coated with PMMA a production of devices possessing essential dimensions as minute as 10 nm. The sequential nature of EBL results in a relatively slow operation [60].

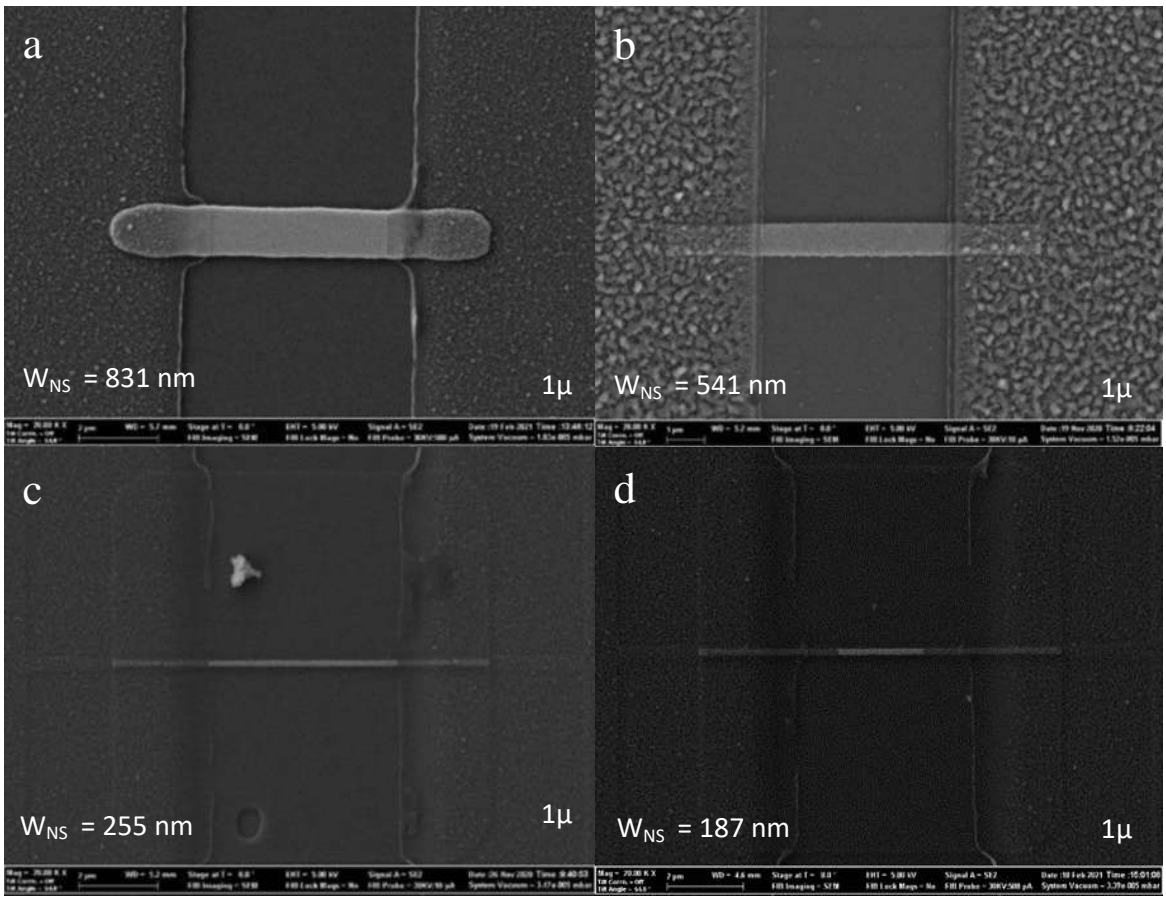


**Figure 3.2 :** SEM images show four different Ge nanosheet widths $W_{NS}$ on a single chip, wherein (a) $W_{NS}$ = 831 nm, (b) $W_{NS}$ = 541 nm, (c) $W_{NS}$ = 255 nm, and (d) $W_{NS}$ = 187 nm. Note that the height of $h_{NS}$ equals 75 nm for all Ge nanosheets

A combination of advanced fabrication techniques has been employed to develop nanoscale Ge structures. Initially, a specimen featuring larger microstructures, which have not undergone previous processing, is subjected to optical lithography and RIE [61].

Optical lithography defines the broader pattern, while RIE is used to etch the microstructures into the desired shapes [61]. To achieve nanoscale dimensions, EBL is employed in conjunction with additional RIE steps [61]. The process begins with a pre-structured Ge layer coated with PMMA, which simplifies the EBL process by reducing the need for extensive patterning [61]. Instead, EBL focuses on defining small etching windows within the pre-structured areas [61].

The procedure involves aligning a detailed pattern with the pre-existing structures (see Figure 3.2a-d). A concentrated electron beam is then used to expose these small windows [61]. The exposed PMMA resist become soluble in the developer, allowing selective etching of these areas and thus enabling the creation of nanometer-scale Ge structures [61].

The high resolution of EBL facilitates the formation of highly intricate patterns and the inclusion of additional structural elements that are crucial for achieving the desired nanoscale features [60].

## 3.4 Electrical Characterization

To rigorously assess the electrical properties of the fabricated Al-Ge-Al heterostructures, a needle probe station is employed in conjunction with a semiconductor analyzer (Keysight 4156B) [62]. This probe station is equipped with four independent SMUs, each known for its exemplary low-noise performance. These needle probe are accurately positioned on the Al contact pads, facilitated by an optical microscope to ensure precisen alignment. Figure 3.3 illustrates a schematic of the measurement setup utilized for this comprehensive electrical characterization. The Al-Ge-Al heterostructures on the GeOI substrate resemble Schottky barrier FET devices, where a p-doped Si substrate acts as a back-gate, and two Al pads serve as drain and source contacts. To establish a connection to the back gate, the $SiO_2$ layer is selectively removed using etching techniques, making it accessible from above [63]. SMUs control the voltages applied to the structure while precisely measuring the resulting current with resolutions down to several. To protect the devices, strict current limits are enforced to prevent potential damage during testing [63].

Measurements are performed under standard air conditions at room temperature. To minimize the impact of light and radiation, the probe station is placed inside a sealed dark enclosure [62].

Figure 3.4 illustrates the cryogenic Lakeshore PS-100 probe station, renowned for conducting experiments under vacuum conditions. Furthermore, including an integrated thermal control stage enables the establishment of consistent and dependable temperature settings.

The analyzer is equipped with four SMUs and two Voltage Source Units (VSUs). SMUs can apply a certain voltage and accurately measure the resulting current. Conversely, VSUs are limited to applying a predetermined voltage solely without any accompanying measurement functionalities. The analyzer provides an intuitive and visually enhanced user interface, which facilitates ease of operation and data [63].

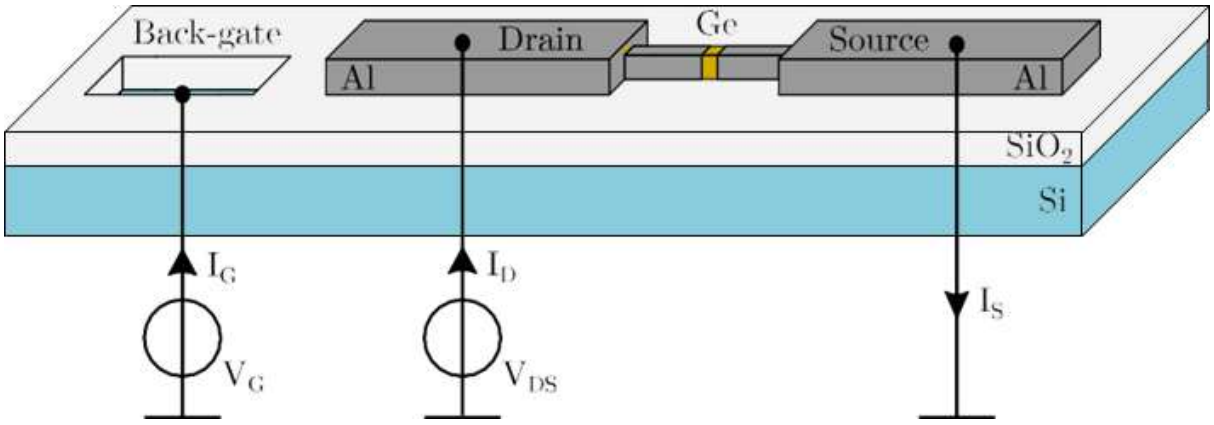


**Figure 3.3 :** Schematic illustration of the measurement setup for the electrical characterization of Al-Ge-Al heterostructures resembling a Schottky barrier FET device. The macroscopic contacts are accessed from the top using a needle prober. The doped Si substrate is used as a global back-gate [63].

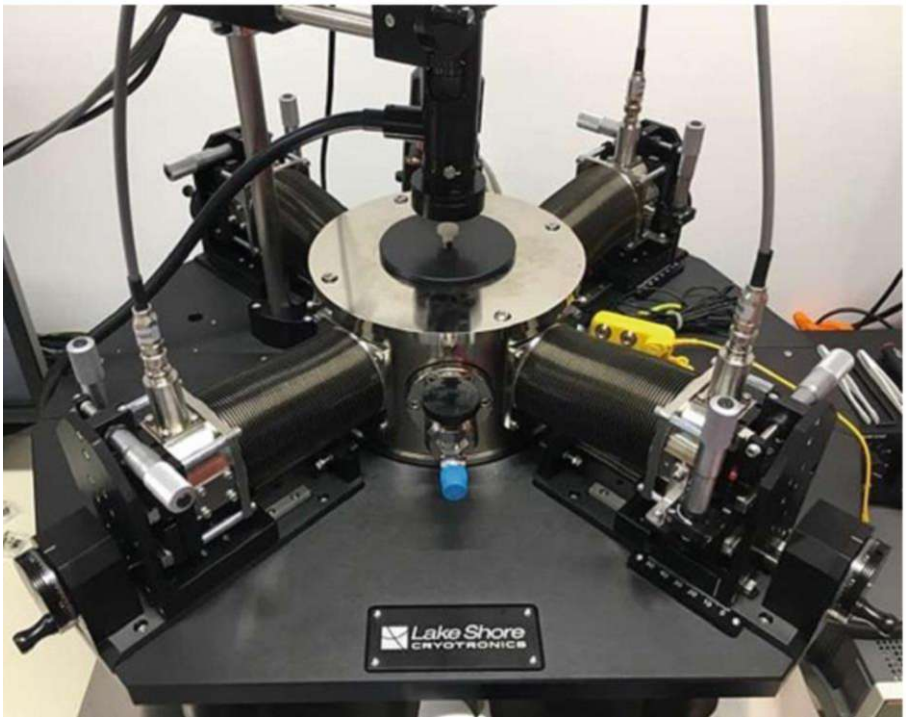


**Figure 3.4 :** The cryogenic Lakeshore PS-100 probe station. The Lakeshore setup possesses the capability to conduct measurements within a vacuum environment and is equipped with an integrated temperature control stage.

### 3.4.1 I/V Characteristics

In the context of basic I/V characterization of Al-Ge-Al heterostructures, the process involves varying the $V_{DS}$ while keeping a fixed back-gate voltage [63]. This helps in understanding the resistivity and contact properties of the fabricated structures. To determine the resistance (R), a linear fit around the zero voltage point is used, based on the equation:

$$R = \frac{V}{I} \tag{3.1}$$

The specific resistivity ρ of the Ge channel is then calculated using the geometric dimensions of the structure, with the following equation :

- R: Measured in ohms (Ω), it quantifies how much a material opposes the flow of electric current.
- V: Measured in volts (V), it represents the electric potential difference between two points.
- I : Measured in amperes (A), it indicates the flow of electric charge.

The resistance of the Al segments and contact pads is negligible compared to the Ge channel due to the significantly higher resistivity of Ge. The voltage sweep range for the I/V characterization depends on the heterostructure's dimensions [64]. For short-channel devices with large cross-sections, a typical range is around 20 mV [64]. For structures with thin and long Ge segments, the range can extend up to 1V. An appropriate step size is chosen to ensure adequate resolution in the measurements [64].

In summary, this characterization method allows researchers to quantitatively determine the electrical properties of the Al-Ge-Al heterostructure [65]. By relating the measured resistance to the physical dimensions and, the specific resistivity can be accurately calculated, providing insights into the performance and behavior of the fabricated structures [65].

### 3.4.2 Transfer Characteristics

The Al-Ge-Al heterostructure on GeOI includes a p-doped Si substrate that acts as a global back-gate. This setup allows for controlling carrier concentration and the transport of carriers above the effective Schottky barrier and through the Ge channel by applying a voltage to the back gate [65].To assess its electrostatic modulation capabilities, the transfer characteristic is documented by varying $V_G$ while measuring the resulting current flow $I_D$ at a given $V_{DS.}$ The gate voltage can be adjusted within a wide range of up to ±60 V due to the strong dielectric properties of the underlying $SiO_2$ layer. Hysteresis effects are investigated by sweeping the $V_G$ from -30 V to 30 V and back, aiming to understand surface trap impacts on device behavior [65].

Surface traps can capture and release charge carriers, causing shifts in the transfer characteristics and potentially impacting the device's reliability and switching behavior [65]. The results from these measurements provide insight into the dynamic response of the heterostructure and its potential for use in various electronic applications [66].

### 3.4.3 NDR Measurements

In this thesis, we conducted a series of NDR measurements on Al-Ge-Al heterostructure devices using GeOI substrates of varying geometries. Specifically, the devices studied, exhibited varying segment lengths and thicknesses, ranging from 87 nm to 16 nm. These measurements were designed to assess the behavior of NDR across different device configurations and under varying conditions. For the NDR effect, we increased $V_D$ to several volts., such as 0-50V respectively. We also applied a high positive gate voltage to see more NDR behavior. Experimental observations into two clear sections, focusing on both annealing and channel thickness and how each influences the NDR behavior of the Ge channels.

# 4. Results and Discussion

The initial section of this chapter focuses on the morphological characterization of the produced devices using several analysis techniques, Scanning Electron Microscopy (SEM), Transmission Electron Microscop (TEM), and Electron Backscatter Diffraction (EBSD). This study investigates the influence of structure size, geometry, and orientation on the thermally induced Al-Ge substitution process. In addition, the electrical properties of the Al-Ge-Al heterostructures are evaluated through measurements of their I/V characteristics, NDR behavior, and transfer characteristics. The study also introduces a wet chemical treatment aimed at reducing the cross-sectional area of the Ge segments, which plays a crucial role in the fabrication of the Al-Ge-Al heterostructure, as mentioned in Chapter 2. The experimental results demonstrate that the I/V electrical characterization outcomes vary with the dimensions of the Ge channel, while the NDR behavior's graphical representation shifts according to different Ge channel sizes. The first GeOI substrate, with an 85 nm thickness, served as the starting point for our investigation. We began by systematically reducing the thickness of the 85 nm Al-Ge channel in small increments. Through this gradual reduction, we observed significant improvements in the electrical properties, particularly in the I/V characteristics and NDR behavior, indicating a strong correlation between reduced channel thickness and enhanced performance.

These observations provided compelling evidence that thinning the Al-Ge channel positively impacts the NDR behavior of the Al-Ge heterostructure process. Encouraged by these results, we applied a more aggressive reduction strategy with a second GeOI substrate, initially 87 nm thick. Instead of incremental reductions, we opted to decrease the thickness directly to 16 nm using wet chemical etching, a process that will be thoroughly detailed in this chapter along with the corresponding results.

## 4.1 Analysis of the Al-Ge Substitution Process

The Al-Ge exchange mechanism has primarily been observed in NWs fabricated using the VLS method. To explore the feasibility of applying this mechanism to a patterned GeOI substrate with a [100] crystal orientation and an 85 nm-thick Ge device layer, we first investigated simple geometries.

The SEM image in Figure 4.1 shows a straight Ge structure with a width of 1 µm and a length of about 6 µm, which was fabricated using optical lithography followed by RIE. The Ge bar is connected to two macroscopic Al pads at either end, separated by about 6 µm. After subjecting the sample to RTA at 400°C for 45 seconds, it was observed that the Al from the contact pads began to diffuse into the Ge structure while Ge atoms simultaneously migrated from the Al reservoirs. Figures 4.1a and 4.1c illustrate the progressive replacement of Ge with Al after multiple annealing cycles. This process causes inward migration at the metal-semiconductor interface, leading to a gradual decrease in the length of the Ge channel. Specifically, the length of the Ge channel decreases from approximately 2,5 µm after 150 seconds to about 1µm after 210 seconds. The distinct chemical contrast between the unreacted monocrystalline Ge (bright) and the pure Al (dark) allows for clear identification of the metal and semiconductor regions in the SEM images.

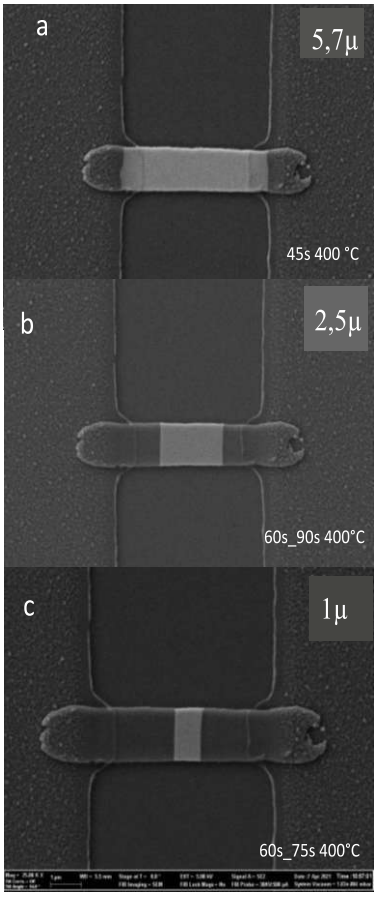


**Figure 4.1 :** (a) 5.7 µm long Ge structure annealed for 45 seconds at 400°C, showing minimal changes, (b) a 2.5 µm long Ge structure, treated for 90 seconds at 400°C, likely indicating a more pronounced effect of the annealing process, causing some reduction in the length or structural changes, (c) a 1 µm long Ge structure, annealed for 75 seconds at 400°C, showing a significantly smaller length, due to further material diffusion.

These images highlight the impact of annealing time and temperature on the physical dimensions of the Ge structures, with longer annealing times leading to a reduction in Ge segment length.

To further examine the Al-Ge interface and analyze the elemental composition of the structure, TEM and EDX were employed. Figure 4.2(a) shows the TEM image of the entire Al-Ge-Al heterostructure. On the other hand Figure 4.2(b) illustrates the EDX mapping with the elemental composition of the formed heterostructure. Figure 4.2(c) shows Ge around the Al part of the heterostructure, indicating that Ge diffuses through surface channels into the Al Pads.

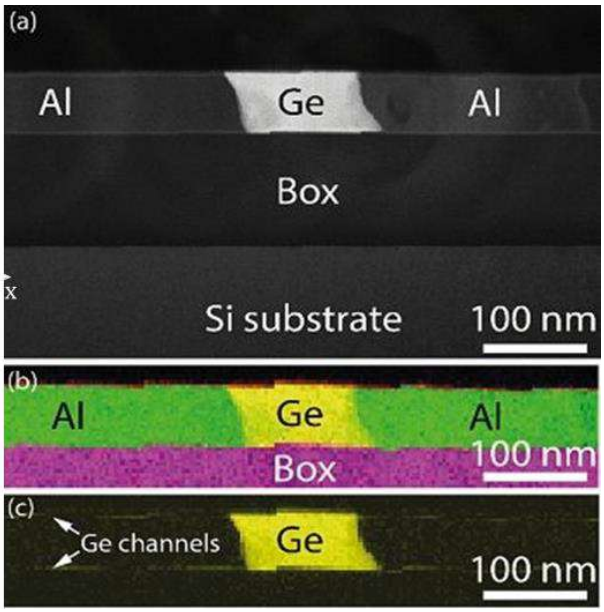


**Figure 4.2 :** (a) TEM image of the entire Al-Ge-Al heterostructure. (b) The EDX mapping shows the elemental composition of the formed heterostructure (Ge: yellow, Al: green, O: red, $SiO_2$: purple). (c) EDX image shows Ge around the Al part of the heterostructure, indicating that Ge diffuses through surface channels into the Al Pads.

## 4.2 The Impact of the Al-Ge Substitution Process to Transfer Characteristics of 85 nm GeOI

The transfer characteristic exhibits a correlation between the saturation current and the structural geometry. The electrical resistance of the devices increases as the segment length extends or the structures become thinner, due to longer electron paths and reduced cross-sectional area for current flow, respectively. Consequently, this increase in resistance leads to a reduction in the magnitude of the electric current flowing through the devices. Furthermore, it has been observed that devices with shorter Ge channels tend for the off state to drift towards

greater gate voltages.$V_G$ is applied using the Si substrate as a global back-gate to enable the operation of the Al-Ge-Al heterostructures as SB-FETs. To evaluate the ability of these structures to modulate charge carriers electrostatically, detailed transfer characterization measurements are performed.

Figure 4.3 presents the characteristics of two distinct Al-Ge-Al SB-FET devices. The black line corresponds to the unannealed 85 nm GeOI, while the blue line represents the annealed GeOI with a 1 µm Al-Ge channel. Both devices exhibit a pronounced p-type behavior, despite the absence of intentional doping in the Ge layer. This p-type characteristic is primarily attributed to the accumulation of holes at the semiconductor surface, which is likely due to trapped negative surface charges. These trapped charges lead to an upward bending of the energy bands at the Ge surface, a mechanism that helps maintain charge neutrality within the material.

Conversely, a positive gate voltage shifts the Fermi level towards the center of the energy band, reducing the number of charge carriers. As the Fermi level approaches its intrinsic position, the carrier concentration diminishes, significantly decreasing current flow. This process continues until the intrinsic Fermi level is reached, leading to a minimal current flow. The charge carriers experience a gradual reduction in their population, leading to the attainment of the intrinsic Fermi level and a subsequent decrease in the current flow.

When applying $V_{BG}$ ranging from 0 to 60 V, with a drain voltage $V_D$ of 1 V, the unannealed Ge channel is hardly responsive to current modulation. In contrast, the fabricated heterostructures with an annealed Al-Ge channel (blue line) respond strongly to the applied back-gate voltage and are easily controllable within the same range at $V_D$=1V.

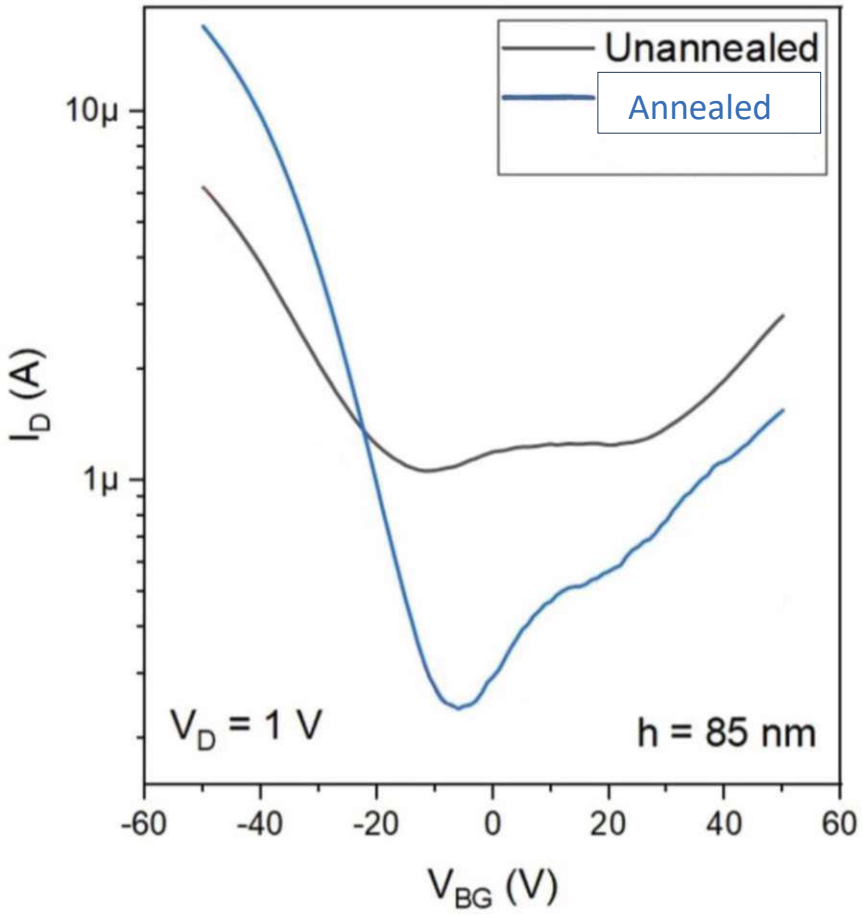


**Figure 4.3 :** Drain current as a function of back-gate voltage The graph shows the drain current $I_D$ versus back-gate voltage $V_{BG}$ for a device with an 85 nm thickness. It compares the performance of the device before (unannealed) and after annealing. The annealed device (blue curve) exhibits better gate control, with a sharper dip in current, indicating improved switching behavior and reduced leakage. Annealing improves the device's electrical performance by lowering the off-state current [66, 72].

## 4.3 The Annealing Effect on NDR Behavior of 85 nm GeOI

The NDR effect is most noticeable at the beginning of the measurement, where increased currents are observed at lower bias voltages. As trap states become filled, the Fermi level shifts toward the center of the energy gap, reducing the number of electrons available for transport within the channel. This corresponds with the expected duration of electron-dominated transport. Consequently, the NDR phenomenon gradually weakens over time and eventually disappears at a point referred to as the intrinsic point. In Figure 4.4(a), the black and red curves follow a very similar pattern, suggesting a short the annealing process does not significantly impact the I-V characteristics when the channel length remains constant at 5 µm.

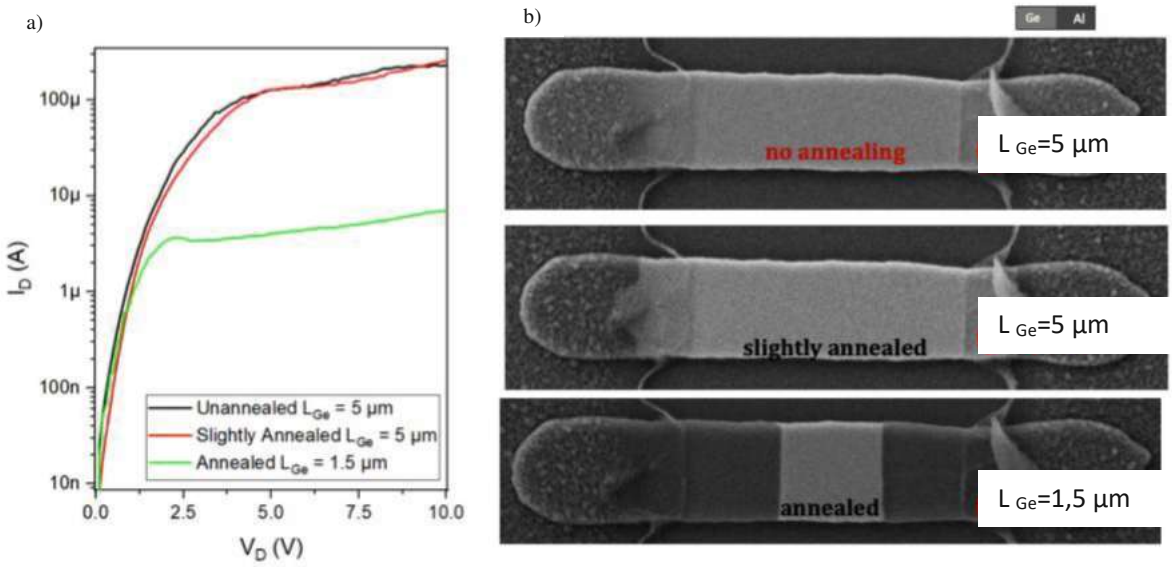


**Figure 4.4 :** a) The graph shows NDR in the device, influenced by the 85 nm GeOI layer. Reducing the Ge channel length to 1.5 µm causes different electrical behavior compared to 5 µm channels, with lower current due to confinement effects and surface states. Unannealed channels have smoother surfaces, while annealing causes subtle texture changes and reduces the channel length. b) The right side shows SEM images of the Ge channel devices under three different annealing conditions: No annealing: The top image shows a device with $L_{Ge}$= 5 µm, labeled with "no annealing."Slightly annealed: The middle image shows a device with $L_{Ge}$= 5 µm, labeled with "slightly annealed."Annealed: The bottom image shows a device with a shorter channel length of $L_{Ge}$= 1.5 µm, labeled with "annealed."

The curves show an almost linear rise in current with increasing $V_D$, indicative of a typical ohmic behavior without any clear signs of NDR in this range of drain voltages. The green curve, corresponding to the annealed Ge channel with a length of 1.5 µm, displays distinctly different behavior. The current is lower across the entire range of $V_D$ compared to the longer channels. However, the curve appears nonlinear, suggesting that annealing and shortening the Ge channel to 1.5 µm significantly affect the transport mechanism. Unlike the unannealed and slightly annealed channels, the green curve for the annealed and shortened channels does not show typical linear behavior. There may be NDR at higher VD indications, but further data would be needed to confirm this observation.

## 4.4 The Etching Effect on NDR Behavior of 85 nm GeOI

To expand our investigation, we included two additional devices with the same geometry but different Ge channel heights, Figure 4.5 shows one with $L_{Ge}$=1.5 µm and h=50 nm (dark blue line), and another with $L_{Ge}$=1.5 µm h=25 nm (turquoise blue line) The dark blue line displays a single NDR feature, starting at $V_D$=1.5 V with a current of 400 nA. Meanwhile, the turquoise

blue line exhibits two distinct NDR regions, indicating enhanced NDR behavior for the thinner device. These observations support our findings from the initial characterization of the 85 nm GeOI devices. The findings demonstrate that reducing the thickness of the Ge channel tends to enhance NDR behavior. This could be attributed to increased quantum effects, stronger confinement of carriers, or surface states that become more influential in thinner channels. The thinner the channel, the more pronounced and complex the NDR behavior becomes.

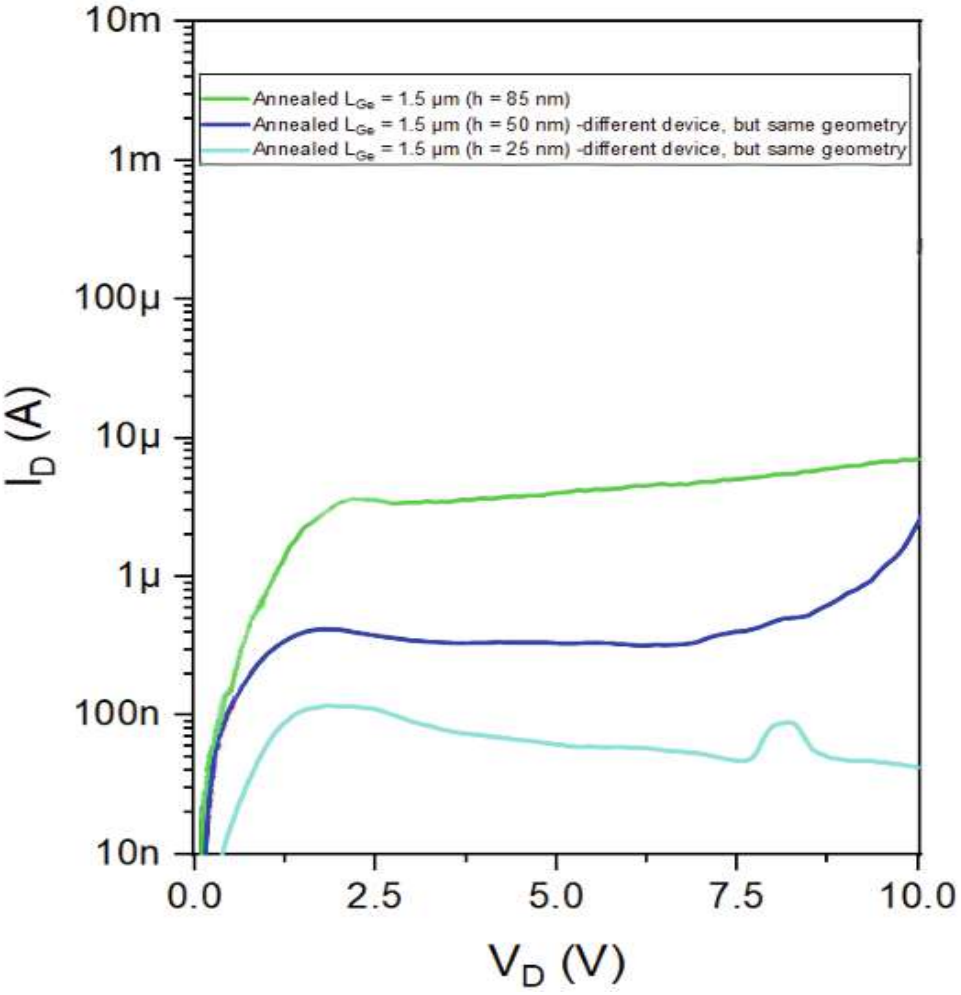


**Figure 4.5 :** The I-V characteristics show the effect of Ge channel thickness on performance. Thicker channels (85 nm) have higher currents, while thinner ones (50 nm and 25 nm) show increased resistance and reduced charge mobility.

Based on the measurement results, we identified the optimal thickness for achieving double NDR. To further refine our experiments, we directly reduced the thickness of the Ge channel from 87 nm to 16 nm for subsequent investigations.

## 4.5 The AFM Measurements of Al-Ge-Al Heterostructures with Reduced Channel Thickness

To examine the GeOI substrate integrated with the Al-Ge-Al heterostructure, we utilized the AFM characterization method. We aimed to showcase the details with high-resolution AFM images, as illustrated in Figures 4.6(a) and 4.6(b).

AFM topographic data, as illustrated in Figure 4.6 provide further detailed information about the structure, particularly regarding the height profile. Moreover, the attained etch rates may be ascertained. The entire Al-Ge-Al heterostructure's AFM image in Figure 4.6 demonstrates the notable height difference between the resistive Al leads and the etched Ge. The etching result was homogeneous, and the surface roughness did not noticeably increase. The anisotropic RIE technique results in a slightly wider bottom section of the bar without altering its overall form.

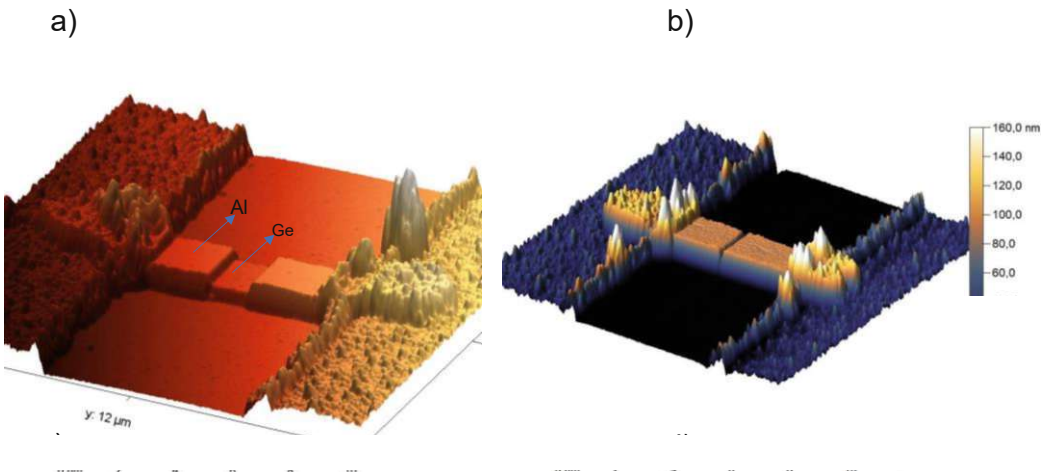


**Figure 4.6 :** Panels (a) and (b) show 3D topography images of a Ge-Al structure, highlighting surface morphology and roughness. The height differences between the Ge and Al regions are evident, with panel (a) showing a more pronounced surface texture.

## 4.6 Transfer Characteristics of 16 nm GeOI

Figure 4.7(a) shows the transfer characteristics of a 16 nm thick Ge channel transistor, where the $I_D$ is plotted as a function of the $V_G$ for various $V_D$. The x-axis represents the $V_G$ in V, ranging from -50 V to 50 V. The peak in current at $V_G$=−50 V then decreases until about $V_G$=-17 V where the $I_D$ indicates that the device operates with its lowest $I_D$ at this gate voltage for the range of $V_D$ values tested. The Y-axis is the $I_D$ in amperes A, shown on a logarithmic scale, spanning from the pA range up to µA. $V_D$ decreases, and the curves show less current and a

more gradual change concerning $V_G$, as expected in lower drain-source voltage conditions. The difference in the curves highlights the impact of different $V_D$ on device performance. Figure 4.7(b) shows a contour plot showing respect to $V_G$ and $V_D$. The color scale at the bottom represents the magnitude of the current being measured, with dark blue representing the lowest values and yellow representing the highest.

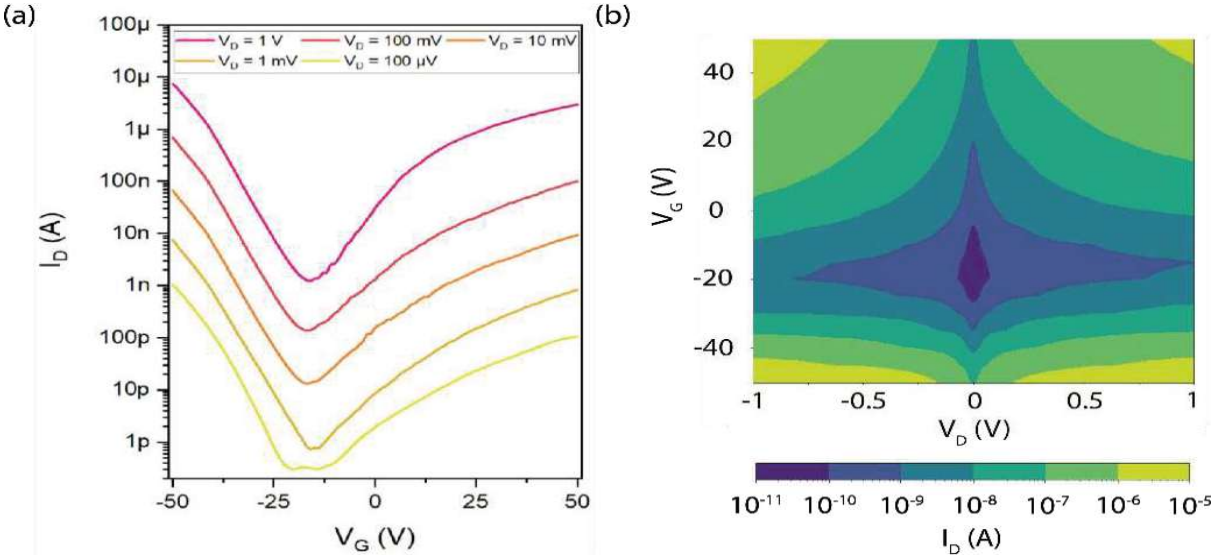


**Figure 4.7 :** a) The Transfer characteristics of a 16 nm GeOI device measured under different drain voltages. The graph illustrates the current-voltage relationship, highlighting the impact of varying drain voltages on the electrical performance of the device. The device behavior under different bias conditions provides insights into the resistivity and carrier transport mechanisms within the GeOI structure. b)The central dark region in the contour plot might represent the area in the device experiencing the lowest potential. This area could correspond to the region where carriers accumulate or where the potential well forms, supporting the high current observed in the left plot.

## 4.7 NDR Measurements of 16 nm GeOI

Based on the results from 87 nm GeOI, we identified the optimal length and width of the Ge channel for NDR. To further refine our experiments, we directly reduced the thickness of the Ge channel from 87 nm to 16 nm for subsequent investigations. However, due to the significant gating effect caused by surface traps, the NWs can be driven into a state where electron transport becomes dominant. Below are the NDR measurements of three Ge channels, each with different dimensions. The device in question likely operates as an SB-FET, where the $V_{BG}$ modulates the conductivity of a channel. Figure 4.8(b) shows the SEM image of the with length $L_{Ge}$= 1,8$\mu$ and width 16nm. Figure 4.8(a) shows the relationship between $I_D$ and $V_D$ for different values of a $V_{BG}$. Here are listed $V_{BG}$ respectively: $V_{BG}$ = 50V (Magenta) $V_{BG}$ = 40V (Red) $V_{BG}$ = 30V

(Orange) $V_{BG}$ = 20V (Yellow) $V_{BG}$ = 10V (Light Yellow) These back-gate voltages have a significant impact on the channel's conductivity, with higher $V_{BG}$ enhancing electron transport and leading to the observed NDR. Negative traps within the device are depleted to facilitate channel inversion in the Ge nanowire. This is achieved by applying a back-gate voltage of 10 V. This voltage is applied for several minutes to ensure that the system reaches a steady state where the current through the NW stabilizes. Negative traps, which can trap electrons and affect the device's behavior, are effectively emptied by this process. This depletion helps in making the channel conductive and ready for further measurements. After the initial depletion, the gate voltage $V_G$ is manually adjusted to 50 V. This high positive voltage helps to keep the traps discharged due to their extended filling time constants. The term "extended filling time constants" implies that once these traps are emptied, they take a relatively long time to be refilled with electrons. As a result, the channel experiences a high positive gate effect, which is crucial for observing specific electronic behaviors like NDR. First NDR Peak occurs at a relatively low $V_D$ around 2-3 V. The peak current at this point suggests that, under the influence of a sufficiently high $V_{BG}$, the device enters a conductive state where carriers move freely, resulting in a high $I_D$. After this peak, the current decreases with further increases in $V_D$, showing the NDR effect as the device moves out of the optimal transport conditions for conduction. The second NDR Peak occurs at a higher $V_D$ around 6-7 V. This secondary peak may correspond to another favorable alignment of energy levels or carrier distribution, allowing for increased current. This secondary NDR behavior might be due to a different conduction mechanism or a secondary energy barrier in the device, which again supports a high $I_D$ before returning to a lower current state.

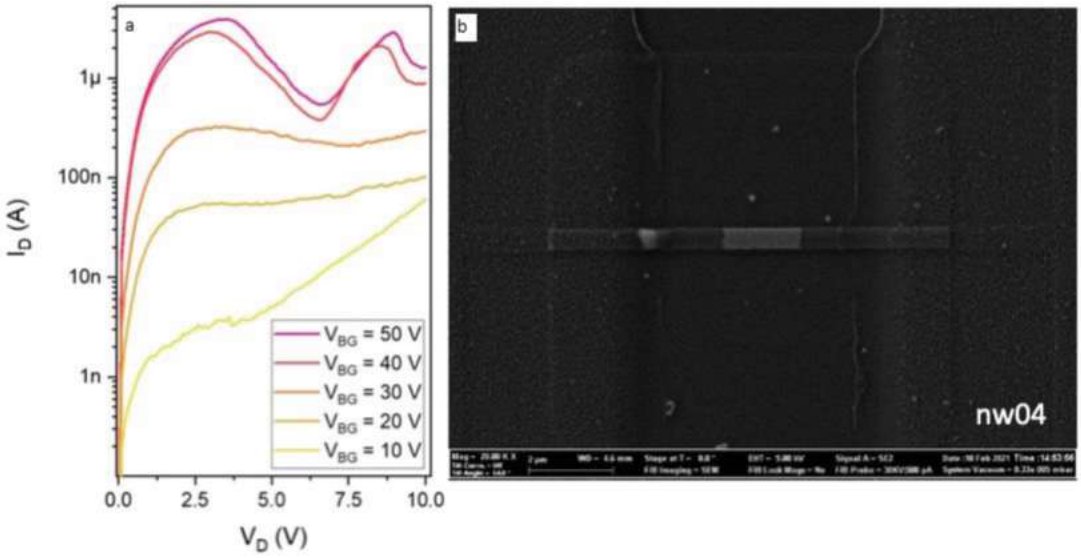


**Figure 4.8 :** a) Detailed NDR measurements of a 16 nm GeOI device (#NW04) alongside SEM images of the Ge channel with a segment length of 1800 nm. Notably, two distinct NDR peaks were observed at $V_{BG}$ = 50 V and $V_{BG}$ = 40 V. These peaks indicate that the interaction between surface traps and the applied electric field significantly impacts the electron transport dynamics within the Ge nanowire. At VBG = 10V and VBG = 20 V, ID increases until $V_D$ at 2.5 V arrives, then the graphic slop tends to decrease. b) SEM picture gives a physical view of the device, allowing us to correlate the electrical characteristics with the physical structure. For instance, the geometry and size of the channel in the SEM image can directly influence the current flow observed in the panel

## 4.8 Influence of the width of Ge Nanosheet on NDR

Following the NDR measurements of the 16 nm GeOI devices, we investigated the NDR behavior further by plotting the results for the devices with different widths. Figure 4.9(a) displays NDR features for each representing a distinct width of the devices. The pink line corresponds to a device width of 3 micrometers, the red line is 1 micrometer and the green line is 100nm. This version indicates the sequential narrowing of the Ge channel width. Figure 4.9(b) displays lines in different colors each representing a distinct width of the devices, but the here y axis shows the electrical field. The two NDR peaks in the Figure 4.9a and Figure 4.9b are more prominent in wider devices (3 µm, 2 µm) and become less distinct as the device width decreases.

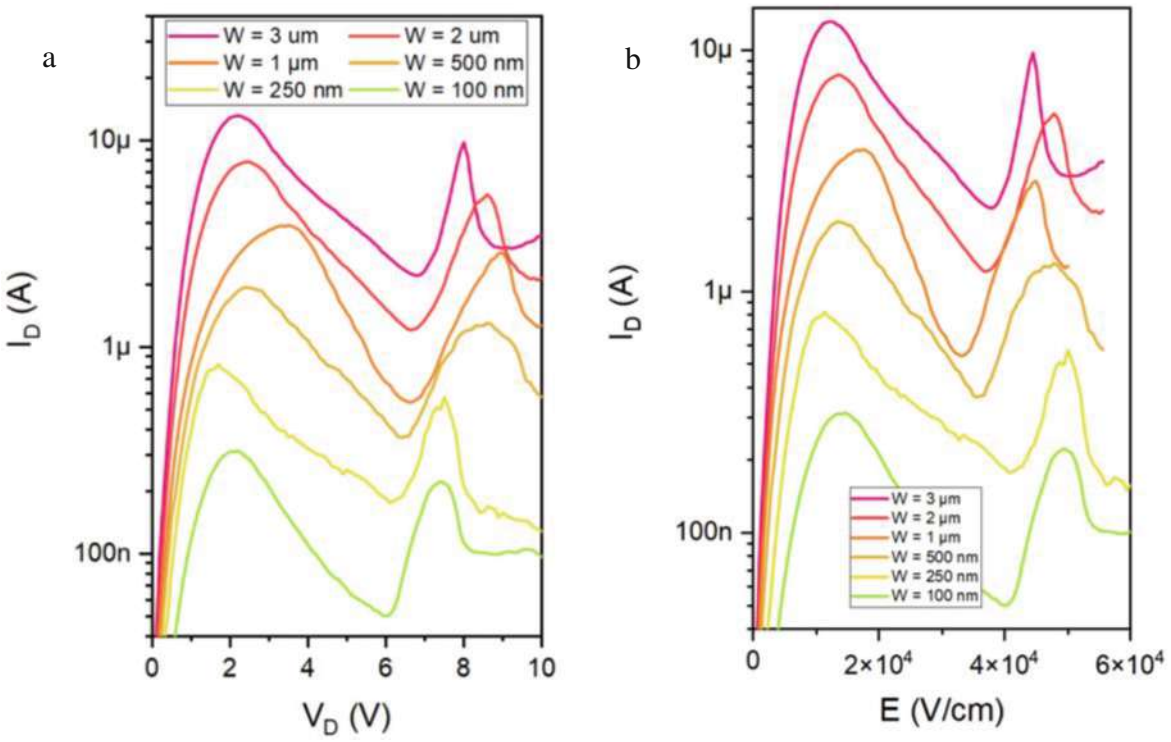


**Figure 4.9 :** a) Device width comparison of 87 nm GeOI Drain $I_D$-$V_D$, all devices have 2 peaks to indicate.This plot shows the $I_D$ versus drain voltage $V_D$ across devices with varying widths , ranging from 3 µm down to 100 nm. The plot illustrates how the device width influences the current response and NDR behavior. The two NDR peaks are more prominent in wider devices (3 µm, 2 µm) and become less distinct as the device width decreases. b) Device width comparison ID-E. This plot shows the ID versus E across devices with varying widths W from 3 µm down to 100 nm. The electric field is expressed in units of V/cm, indicating the strength of the applied field across the device. The two NDR peaks are more prominent in wider devices (3 µm, 2 µm) and become less distinct as the device width decreases

# 5. Summary and Outlook

This study presents the successful fabrication of freestanding Al-Ge-Al heterostructure nanobeams, building on the theoretical foundations outlined in Chapter 2 and the characterization methods detailed in Chapter 3. The thesis describes a thermally driven exchange process that creates monolithic Al-Ge-Al heterostructures on a GeOI substrate, enabling the production of ultra-short Ge segments at the nanoscale, surpassing the limitations of traditional lithography. SEM images reveal perfect crystallinity and nearly atomically smooth interfaces between the self-aligned Al leads and the Ge segment. The examination of irregular structures with widths ranging from 5 µm down to a few nanometers, along with varying geometries and orientations, shows no geometric constraints on the exchange process. EBSD studies confirm that the produced Al segments possess crystalline grain sizes in the micrometer range, with high-purity Al leads often exhibiting monocrystalline behavior as the structural size decreases.

Electrical characterizations reveal a notable improvement in contact properties post-annealing, attributed to the atomically precise Al-Ge interface. By applying a back-gate voltage to the p-doped Si substrate, the devices operate as SB-FETs, allowing substantial modulation of carrier transport across the Ge channel, which consistently exhibits p-type behavior. In structures with extended Ge segments, characteristic ambipolar behavior—typical of SB-FETs—is observed. The I/V electrical characterization results indicate that transport properties, including double NDR behavior, vary based on the Ge channel dimensions. This approach supports the integration of various novel Ge-based devices, such as CMOS-compatible nanoelectronics and photonic devices, into monolithic metal-semiconductor-metal heterostructures. Additionally, Al serves as a versatile building block for creating superconductor-semiconductor hybrid quantum systems, including SQUIDs, oscillators, and amplifiers [81].

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# List of Figures

**Page**

# List of Tables

**Page**

# List of Abbreviations

| Symbol | Description |
|---|---|
| Al | Al |
| $Al_2O_3$ | Aluminum Oxide, Alumina |
| AFM | Atomic Force Microscope |
| BHF | Buffered Hydrofluoric Acid |
| CMOS | Complementary Metal-Oxide-Semiconductor |
| EBL | Electron Beam Lithography |
| EDX | Energy Dispersive X-Ray Spectroscopy |
| fcc | Face Centered Cubic |
| FET | Field-Effect Transistor |
| Ge | Ge |
| GeO | Ge Monoxide |
| $GeO_2$ | Ge Dioxide |
| GeOI | Ge on Insulator |
| $H_2O$ | Water |
| HF | Hydrofluoric Acid |
| HI | Hydroiodic Acid |
| I/V | Current/Voltage |
| MOSFET | Metal-Oxide-Semiconductor |
| NW | Nanowire |
| RIE | Reactive Ion Etching |
| SEM | Scanning Electron Microscopy |
| Si | Silicon |
| $SiO_2$ | Silicon Oxide |
| DOS | Density of States |
| LED | Light Emitted Diodes |
| SMU | Source-Measure-Units |
| VSU | Voltage-Source- Units |
| µV | Microvolt |
| fA | Femtoampere |
| eSBH | Effect Schottky Barrier Height |

| | |
|---|---|
| K | Kelvin |
| SiGe | Silicon-Germanium |
| TED | Transient-enhanced Diffusion |
| VLS | Vapor-Liquid-Solid |

# List of Symbols

| Symbol | Description | Units |
|---|---|---|
| a | Lattice Constant | Å |
| A | Cross-Section Area | $cm^2$ |
| C | Concentration | $1/cm^3$ |
| D | Diffusion Coefficient | $cm^2/s$ |
| R | Electrical Resistance | *ohm* ($\Omega$) |