PhD Thesis

Exploration of Charge Carrier Transport in Si and Ge based Schottky Barrier Field-Effect Transistors

submitted in partial fulfillment
of the requirements of the degree of
Doctor in Engineering Sciences (Dr.techn.)

at Technische Universität Wien
Institute of Solid State Electronics

under supervision of
Univ.Prof. Dipl.-Ing. Dr.-Ing. Walter Michael Weber
and
Univ.Ass. Dipl.-Ing. Dr.techn. Masiar Sistani

by

Projektass. (FWF) Dipl.-Ing. Raphael Behrle
Matr.-Nr. 051832821

Vienna, October 2024

Abstract

In the quest to further increase the capabilities of modern transistors in terms of functional diversification, enhancing switching speeds, and reducing energy consumption, Schottky barrier field-effect transistors (SBFETs) are a promising platform for nanoelectronic devices beyond static operation. Attributed to the incorporated metal-semiconductor junctions in SBFETs, a thorough understanding of the charge carrier transport is of utmost importance for emerging reconfigurable electronics. In this work, Si, $Si_{1-x}Ge_x$, and Ge nanowires (NWs) are contacted with single-crystalline and mono-elementary Al. The technology enabler to achieve the thereof obtained abrupt metal-semiconductor interfaces is a thermally driven solid-state metal-semiconductor exchange mechanism. Using multi-parameter current/voltage sweeps and temperature-dependent bias spectroscopy allowed a systematic investigation of the charge carrier transport and mechanisms in the proposed Al-group IV based SBFETs, where the Al-Si material system revealed symmetric *n*- and *p*-type Schottky barriers (SBs). In contrast, the Al-$Si_{1-x}Ge_x$ and -Ge material systems exhibited dominant *p*-type conduction due to Fermi level pinning close to the valence band. Notably, bias spectroscopy allows the visualization of operation regimes, which cannot be accessed by single parameter sweeps. Using the gained insights of the charge carrier transport enabled the realization of the first-ever Al-Si based reconfigurable field-effect transistor (RFET), allowing dynamic altering between *n*- and *p*-type operation even during runtime. Further, bias spectroscopy allowed to determine optimal operation conditions of the proposed RFETs for their integration in a complementary inverter and wired-AND gate. Attributed to the inherently accessible negative differential resistance (NDR) in Al-Ge based SBFETs, the electronic transport of the NDR regime was analyzed, and NDR tunability was achieved by using a multi-gate architecture as well as creating cascode circuits. In this respect, overlapping NDR regions were obtained, which is required for the realization of NDR logic gates. Most notably, the realized devices and circuits complement conventional CMOS technology and, further contribute to an increased functional density, and may become valuable building blocks for emerging computing paradigms such as artificial intelligence and neuromorphic electronic applications.

Kurzfassung

Um die Fähigkeiten moderner Transistoren im Hinblick auf die Funktionsdiversifizierung und die Erhöhung der Schaltgeschwindigkeiten weiter zu steigern und den Energieverbrauch zu senken, sind Schottky-Barrieren-Feldeffekttransistoren (SBFETs) eine vielversprechende Plattform für adaptive nanoelektronische Bauelemente. Da SBFETs auf Metall-Halbleiter-Übergängen basieren, ist ein tiefes Verständnis des Ladungsträgertransports für rekonfigurierbare Elektronik von größter Bedeutung. In dieser Arbeit werden Si-, $Si_{1-x}Ge_x$- und Ge-Nanowires (NWs) mittels thermisch induziertem Metall-Halbleiter Austauschmechanismus über abrupte Metall-Halbleiter-Grenzflächen mit einkristallinen und monoelementarem Al kontaktiert. Die Verwendung von temperaturabhängigen Multi-Parameter-Strom-/Spannungs-Sweeps (Bias-Spektroskopie) ermöglichten eine systematische Untersuchung des Ladungsträgertransports und der zugrunde liegenden Mechanismen in den realisierten SBFETs. Die Analysen zeigten, dass das Al-Si Materialsystem symmetrische Schottky-Barrieren (SBs) für Elektronen und Löcher aufweist, während das Al-$Si_{1-x}Ge_x$- und -Ge Materialsystem eine dominante p-Typ Leitung zeigt, die auf ein Pinning des Fermi-Niveaus nahe dem Valenzband zurückzuführen ist. Insbesonders die Bias-Spektroskopie ermöglichte die Visualisierung von Betriebsregionen, die durch einzelne Parameter-Sweeps nicht zugänglich sind. Die gewonnenen Erkenntnisse über den Ladungsträgertransport ermöglichten die Realisierung des ersten rekonfigurierbaren Feldeffekttransistors (RFET) auf Al-Si-Basis, der den dynamischen Wechsel zwischen n- und p-Betrieb sogar während der Laufzeit erlaubt. Darüber hinaus konnten die optimalen Betriebsbedingungen für RFETs und die Integration in einen komplementären Inverter und ein Wired-AND-Gate untersucht werden. Desweiteren wurde der negative Differentialwiderstand (NDR) in Al-Ge-basierten SBFETs analysiert, und die NDR-Abstimmbarkeit durch die Verwendung einer Multi-Gate-Architektur sowie durch die Schaffung von Kaskodenschaltungen erreicht. In dieser Hinsicht wurden überlappende NDR-Bereiche erzielt, die für die Realisierung von NDR-Logikgattern erforderlich sind. Die realisierten Bauelemente und Schaltungen ergänzen die konventionelle CMOS-Technologie und tragen zu einer höheren Funktionsdichte bei. Sie könnten wertvollen Bausteinen für neue Computerparadigmen wie künstliche Intelligenz und neuromorphe Elektronik darstellen.

Acknowledgement

As a student's assistant and master's student in the "Emerging Nanoelectronic Devices" group, I enjoyed getting into the topic of nanowire electronics with all its manifold facets. This friendly and supportive environment remained also during my time as a PhD student with great colleagues at the Institute of Solid State Electronics. In the following, I would like to thank especially...

Prof. Walter M. Weber
for your precious feedback during group meetings, discussions, papers, and reviews. Moreover, I would like to thank you for the important industry-related aspects you provided during my PhD journey.

Dr. Masiar Sistani
for being such a great mentor and project leader throughout my time at the institute. Discussing new ideas and concepts with you was and is always great. Besides work-related topics, I also found a great friend in you!

Andreas Fuchsberger, Dr. Daniele Nazzari & Lukas Wind
for enjoyable (and also funny) discussions. I appreciated your feedback and our collaboration in every facet.

Prof. Alois Lugstein & Prof. Jürgen Smoliner
for always providing helpful advice on manuscripts, work-related concerns and sharing other great stories. Many thanks for your great assistance and time!

Bachelor's and master's students

for assisting with data acquisition and evaluation. It was also a pleasure to introduce you to the world of SBFETs - and discuss your critical questions!

Cooperation partners

for great cooperation, from nanowire growth to STEM analysis and the development of novel measurement techniques. Without you, this PhD thesis would not be what it is now!

Madlen

for your essential support throughout the entire PhD process. Being in a distance relationship was tough, but we made it! Many thanks for your patience and understanding! I love you!

Preface

The PhD thesis at hand was conducted within the scope of the Austrian Science Fund (FWF) project no. I 5383 (Grant DOI: 10.55776/I5383) under the title "Metastable nanoscale solid solutions and their integration", lead by Dr. Masiar Sistani, Institute of Solid State Electronics, TU Wien, as principal investigator.

In this context, Al-group IV (Si, $Si_{1-x}Ge_x$ and Ge) semiconductor nanowire (NW) heterostructures were analyzed and investigated from a nanoelectronics perspective, enabling a better understanding of the obtained junctions integrated into Schottky barrier field-effect transistors (SBFETs). In the thesis at hand, the main focus is set on the characterization of the obtained devices, where Prof. James F. Cahoon performed the Si NW synthesis at the Department of Chemistry, University of North Carolina at Chapel Hill, the $Si_{1-x}Ge_x$ NW growth was done by Dr. Bassem Salem at Université Grenoble Alpes, CNRS, CEA/LETI Minatec and the Ge NW growth was performed by Dr. Alois Lugstein at the Institute of Solid State Electronics, TU Wien as well as by Dr. Sven Barth at the Physics Institute, Goethe Universität Frankfurt. The structural analysis in terms of scanning transmission electron microscopy and energy dispersive X-ray investigations was done by Dr. Martien I. den Hertog, Institut Néel, CNRS, and Dr. Lilian Vogl, EMPA Thun. The integration of the proposed SBFETs and electrical characterization was carried out at the Institute of Solid State Electronics, TU Wien.

Publications published in the PhD program's scope are referenced according to "[RBx]" and are listed in a separate bibliography at the end of the thesis.

Contents

List of Figures

List of Tables

List of Symbols

Abbreviations

AI	Artificial intelligence
ALD	Atomic layer deposition
BEOL	Back end of line
BF	Bright field (STEM)
BG	Back gate
BTI	Bias temperature instability
CG	Control gate
CMOS	Complementary metal-oxide-semiconductor
CNL	Charge neutrality level
CNT	Carbon nanotube
C/V	Capacitance-voltage characteristics
CVD	Chemical vapor deposition
DOS	Density of states
DPG	Diphenylgermane
EBIC	Electron beam-induced current
EBL	Electron beam lithography
EDA	Electronic design automation
EDX	Energy dispersive X-ray spectroscopy
eSBH	Effective Schottky barrier height
fcc	face-centered cubic
FE	Field emission
FET	Field-effect transistor
FEOL	Front end of line
FOM	Figures of merit
GAA	Gate-all-around
GeOI	Germanium on insulator
GIDL	Gate-induced barrier lowering
(B)HF	(Buffered) Hydrofluoric acid

HAADF	High-angle annular dark-field (STEM)
HCl	Hydrogen chloride
HI	Hydroiodic acid
HZO	Hafnium Zirconium oxide
JJ-FET	Josephson junction field-effect transistor
II	Impact ionization
IRDS	International Roadmap for Devices and Systems
I/V	Current-voltage characteristics
LB	Landauer-Büttiker
LFN	Low-frequency noise
LN_2	Liquid nitrogen
ML	Machine learning
MOBILE	Monostable-bistable logic element
MOSFET	Metal-oxide-semiconductor field-effect transistor
MSJ	Metal-semiconductor junction
MVL	Multi-valued logic
NDC	Negative differential conductance
NDR	Negative differential resistance
NW	Nanowire
PG	Polarity gate
PMMA	Poly methyl methacrylate
PVR	Peak-to-valley (current) ratio
RFET	Reconfigurable field-effect transistor
RIE	Reactive ion etching
RT	Room temperature ($T = 293.15\,\mathrm{K}$)
RTA	Rapid thermal annealing
RTD	Resonant tunneling diode
SB	Schottky barrier
SBFET	Schottky barrier field-effect transistor
SBH	Schottky barrier height
SEM	Scanning electron microscopy
SMU	Source-measure unit
SOI	Silicon on insulator
STEM	Scanning transmission electron microscopy
TCAD	Technology computer-aided design
TCR	Temperature coefficient of resistance
TE	Thermionic emission
TFE	Thermal-assisted field emission
TG	Top gate
TMA	Trimethylaluminium
VLS	Vapor liquid solid
VLSI	Very-large-scale integration

VSU	Voltage-source unit
WKB	Wentzel-Kramers-Brillouin approximation
XPS	X-ray photoemission spectroscopy

Variables and Constants

a	Lattice constant
A^*	3D Richardson constant (effective Schottky barrier height)
a_B^*	Exciton Bohr radius
$at\%$	Atomic percentage
A_NW	Cross-section area of a NW
C_D	Depletion layer capacitance
C_ox	Oxide capacitance per unit area
D_it	Trap state density (in $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$)
d_NW	Diameter of a NW
E	Energy
E_a	Activation energy (effective Schottky barrier height)
E_C	Conduction band energy
$\mathcal{E}$	Electric field
$\mathcal{E}_\mathrm{crit}$	Critical electric field for NDR
$\mathcal{E}_\mathrm{ds}$	Electric field of dielectric strength
E_F	Fermi energy
E_Fm	Fermi energy of the metal
E_Fs	Fermi energy of the semiconductor
E_g	Band gap energy
$E_{\Gamma 1}$	Direct band gap energy in Ge ($k = 000$)
ε_0	Permittivity in vacuum ($8.854 \times 10^{-14}\,\mathrm{F/cm}$)
ε_r	Relative permittivity
ε_s	Relative semiconductor permittivity
EOT	Equivalent oxide thickness
E_V	Valence band energy
E_vac	Vacuum energy
$F(E)$	Fermi-Dirac distribution
G	Conductance
g_m	Transconductance
h	Planck's constant ($6.626 \times 10^{-34}\,\mathrm{J\,s}$)
$\hbar$	Reduced Planck's constant $\hbar = h/2\pi$
I_D	Drain current
J	Current density
k	Wave vector
k_B	Boltzmann constant ($1.381 \times 10^{-23}\,\mathrm{J/K}$)
L_SC	Semiconductor segment length
n	Slope coefficients (1D LB)
N_D	Donor concentration
m_0	Electron rest mass ($9.109 \times 10^{-31}\,\mathrm{kg}$)
m^*	Effective mass

m_{T}^{*}	Tunneling effective mass
μ	Charge carrier mobility
Φ	Electrical potential
ϕ_0	Energy determining CNL
ϕ_{B}	(Schottky) Potential barrier
ϕ_{bi}	Built-in potential barrier
ϕ_{m}	Metal work function
ϕ_{s}	Semiconductor work function
ψ_{cc}	Electrostatic potential at current control point (1D LB)
q	Elementary charge (1.602×10^{-19} C)
Q_{f}	Fixed oxide charge [in (charges)/cm^{-2}]
Q_{it}	Interface charge [in (charges)/cm^{-2}]
ρ	Resistivity
$\rho(\mathbf{r})$	Charge density function
r_{diff}	Differential resistance
R_{DS}	Drain-source resistance
σ	Conductivity
S	Subthreshold slope
S_{th}	Subthreshold swing
t	Time
T	Absolute temperature
$T(E)$	Transmission coefficient
τ_{c}	Mean collision time
T_{c}	Critical superconducting temperature
t_{ox}	Oxide thickness
T_{ox}	Oxidation temperature
t_{rr}	Reverse recovery time
V_{BG}	Back gate voltage
V_{bi}	Built-in voltage
V_{CG}	Control gate voltage
V_{D}	Drain voltage
V_{F}	Forward voltage
V_{FB}	Flat-band voltage
V_{G}	Gate voltage
V_{K}	”Kink” voltage: Transition TE $\rightarrow$ TFE/FE
V_{p}	Peak voltage (NDR)
V_{PG}	Polarity-gate voltage
V_{S}	Source voltage
V_{t}	Thermal voltage
V_{TG}	Top gate voltage
V_{th}	Threshold voltage
V_{v}	Valley voltage (NDR)

W_{d}	(Schottky) Depletion width
$wt\%$	Weight percentage
X_{s}	Electron affinity

Glossary

The following elaborates and defines the meaning of frequently used terms that appear throughout the thesis at hand. Moreover, the definitions shall support the reader by clarifying specific terms.

Ambipolarity:
In SBFET technology the term "ambipolarity" describes a transfer I/V characteristic (I_{D} vs. V_{G}), which exhibits a *n*- (positive V_{G}) and *p*-type (negative V_{G}) characteristic. Consequently, having a positive threshold voltage $V_{\mathrm{th}}^{\mathrm{n}}$ and a negative threshold voltage $V_{\mathrm{th}}^{\mathrm{p}}$ as well as associated on-currents $I_{\mathrm{on}}^{\mathrm{n/p}}$, combined in a single device.

Band structure vs. band diagram:
The (electronic) band structure describes the possible energy levels of electrons (conduction band) and holes (valence band), as well as band gaps.
The band diagrams used in the work at hand illustrate the electrostatic gating mechanism evident in SBFETs by electrostatically tuning the energy landscape of the metal-semiconductor junctions and the semiconductor. Thus, it does not impact the underlying band structure, which is defined by semiconductor properties. Note that throughout the work at hand, simplified band diagrams are used.

Bottom-up grown nanowires:
Nanowires are grown by a chemical reaction, i.e., chemical vapor deposition (CVD). In this respect, the vapor-liquid-solid (VLS) mechanism uses a metal catalyst (commonly Au droplets) as nucleation centers for nanowire growth. In general, the distinct positioning of bottom-up grown nanowires for further integration is challenging regarding very-large-scale integration (VLSI). Therefore, bottom-up grown nanowires are often considered in prototyping platforms.

Group IV semiconductor:
In this work, the term "group IV semiconductor" covers Si, Ge, and its compound $Si_{1-x}Ge_x$. Note that, in general, Graphene, Germanene, and Silicene, as well as SiC and carbon nanotubes are further examples of group IV semiconductors but are not covered in this work.

"Slow" and "fast" trap states:
In general, different origins of traps exist, whereas in this work, mainly interface charges denoted as Q_{it} and fixed charges denoted as Q_f are considered. Further, the lifetime of the trapped charge carriers is an important aspect to consider. In this respect, carriers trapped at the interface (Q_{it}) exhibit lifetimes in the µs- to ms-regime, whereas fixed oxide traps (Q_f) have lifetimes starting in the 100 ms-regime and can be as long as hours. Thus, traps at the interface are denoted as "fast" as they occupy trap states for a shorter time than fixed charges, which are "slow".

Transient stability:
In the scope of the work at hand, the term "transient stability" relates to two aspects: First, "slow" and "fast" traps at the semiconductor-dielectric interface influence the charge carrier transport because they may act as local gates. Remarkably, such trap states can be occupied for hours once a charge carrier gets trapped. Second, charging effects are caused by the relatively large area of the substrate in comparison to a single nanowire, which also affects the charge carrier transport. From an experimental point of view, subsequent measurement cycles and the hysteresis can be evaluated to get an impression of the transient stability. Another approach is to perform a transient measurement by applying a constant V_D and V_G (static operation) and monitor the current I_D over time.

Top-down nanowires:
Top-down nanowires exhibit a rectangular cross-section shape due to their fabrication from thin films, e.g., from Silicon-on-Insulator (SOI) or Germanium-on-Insulator (GeOI) substrates. Therefore, lithography and etching processes are used to fabricate nanowires, which are then also denoted as nanosheets. Importantly, top-down fabricated nanowires allow precise positioning and definition of the dimensions, enabling wafer-scale integration.

Chapter 1

Introduction

Today, metal-oxide-semiconductor field-effect transistors (MOSFETs) are the backbone of modern electronic devices, which is further driven by recent advances in artificial intelligence (AI) and machine learning (ML) as well as in robotics and autonomous systems, to name a few. [1] In this respect, more powerful nanoelectronics in terms of simultaneous calculations and higher switching speeds is desired. [2,3] Moore's law predicts that the number of transistors of an integrated circuit, and therefore its computing capabilities, will double itself approximately every two years. [4] In the last decades, this progress was mainly driven by continuous down-scaling of Si-based transistors and innovations in manufacturing processes, such as, e.g., Extreme-Ultraviolet lithography. [5–8] However, progressive down-scaling introduces undesired short-channel effects, as, e.g., increased gate leakage currents originating from quantum mechanical tunneling through the scaled gate oxide as well as increased off-currents or even punch through of the transistor channel, preventing a sufficiently low off-state of MOSFETs. [9–11] In this regard, Wang and Lundstrom evaluated a limit for source-to-drain tunneling, which is well below 10 nm. [12] Besides that, simulations of Si nanosheets showed sufficient transistor functionality with gate lengths down to 5 nm. [13] Nevertheless, down-scaling can lead to loss of gate control and increased energy consumption. [6,14] In bulk MOSFETs, an industrial approach tackling such issues is the introduction of halo implants or a low doped region, extending the source/drain regions and preventing the expansion of the depletion region. [15] However, doping and, more specifically, sharp doping profiles require a complex manufacturing infrastructure and high efforts in process development. [16] For better electrostatic gating capabilities, technologies such as FinFETs have evolved, providing an ultrathin body resulting in the achievement of fully depleted channels. [17, 18] Moreover, FinFET technology paved the way towards realizing three-dimensional (3D) stacked transistors, ensuring to continue Moore's law. [19]

Further, Gate-all-around (GAA) transistors emerged, which enable gating from each channel's facet, providing excellent gating capabilities with reduced short-channel effects. [20, 21] Nevertheless, fundamental physical limits of the underlying materials are reached, i.e., embracing the thermal fluctuation limit (~$100k_BT$: minimal switching energy guaranteeing error-free lifetime operation). [10]
In terms of further enhancing nanoelectronics, paradigms evolved, considering emerging materials and architectures as well as two-dimensional (2D)- and one-dimensional (1D)-confined channel geometries. [22,23] From a materials point of view, Si is still the semiconductor material of choice for a broad range of applications. The opportunity to thermally grow native SiO_2, which comes with a modest interface trap state density and highly optimized Si-technology manufacturing processes, makes it an advantageous semiconductor. [17, 24] However, other group IV semiconductors, such as Ge and $Si_{1-x}Ge_x$, have remarkable advantages for distinct applications, as e.g., in *p*-MOS transistors, BiCMOS technology and also as strain layers to increase the channel's charge carrier mobility. [25–28] Especially, the smaller band gap of Ge in comparison to Si [E_g(Ge) = 0.66 eV vs. E_g(Si) = 1.12 eV], and lower effective masses of approximately half of Si, allows to achieve higher switching speeds using of Ge. [29, 30] However, its native oxide, Ge_xO_y, may come with considerable drawbacks as, e.g., its water solubility and a potentially high interface trap state density. [31–33] Nevertheless, advancements in atomic layer deposition (ALD) technology, and hence the possibility to fabricate high-κ oxides and nitrides, [34, 35] allow to tackle drawbacks on the formation of the native Ge oxide. Importantly, using Ge-based materials and ALD techniques even allows co-integration with established Si-based complementary metal-oxide-semiconductor (CMOS) technology. [36, 37]
Regarding enhanced architectures, the functional diversification of devices on the transistor level is driven, e.g., by using multi-gates, allowing an increase in the functionality of single transistors and even logic gates. [38–40] A common term for such technologies is "Beyond CMOS", which covers the exploration of emerging materials and functionalities as well as considers emerging transistor architectures. [23] Attributed to the mature and highly optimized Si-technology, "Beyond CMOS" implementations depict add-on computing paradigms to the established CMOS technology, featuring *n*- and *p*-type FET operation on the same substrate. [41] Particularly, in the scope of "Beyond CMOS", Schottky barrier (SB) FETs (SBFETs) turned out to deliver a promising device architecture for the realization of emerging devices, such as multi-mode transistors, [42, 43] surface plasmon detectors [44, 45] and even Josephson junction FETs (JJ-FETs). [46, 47] In this context, SBFETs make explicit use of dedicated metal-semiconductor junctions (MSJs). [48–50] Considering an un-doped semiconductor and ideally identical SBs for electron and hole injection, the properties of MSJs can be facilitated to electrostatically tune the energy landscape of the conduction and valence band of the semiconductor, allowing to alter the injection and control of the electron and hole transport. [50, 51] Attributed to the non-ohmic source/drain contacts electron and hole potential barriers are evident at the MSJ.

Thus, the Fermi level pinning is of high importance, as it determines the actual SB heights (SBHs) exhibited to electrons and holes, [17,52] and thus highly influences the on-currents and transconductance of SBFETs. [49] As source/drain material, metal-silicides, and -germanides, as obtained, e.g., by Ni- or Co-reactions, [53] are of high relevance because of their well-established processing techniques in the semiconductor industry and electronic properties. [54–57] Metal-silicides and -germanides are created from a solid-state exchange reaction between the metal and the semiconductor, initiated, e.g., by rapid thermal annealing (RTA), enabling stable metal-silicide/germanide-semiconductor junctions. However, precise processing techniques, i.e., temperatures and timings, are required to obtain the desired material phase, e.g., $NiSi_2$ in the Ni-Si material system. [58] Another promising source/drain material is Al, which does not form any inter-metallic phases and features single-crystalline Al after the solid-state exchange. [59] As an essential asset concerning scaling, specific SBFET applications do not necessarily require doping profiles. [42, 60] Figure 1.1 shows a structural comparison of a bulk *n*-MOSFET vs. a SBFET with an un-doped channel, illustrating the general material stack differences, which undoubtedly get evident in the metal(source)-semiconductor-metal(drain) heterostructure and the non-existent doping areas in the proposed SBFET.

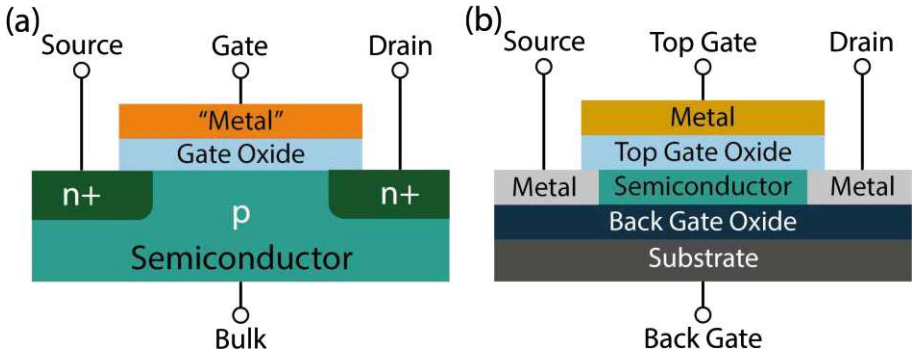


Figure 1.1: *Schematic material stack cross-sections of (a) a bulk n-MOSFET, and (b) a SBFET with an un-doped channel. The metal source/drain regions in SBFETs have advantages associated with low formation temperatures (here: Al-Ge at* 673 K *and Al-Si at* 773 K*) and their atomically abrupt nature. Note that source, drain, and bulk metallizations are not illustrated.*

From the wide range of 2D- and 1D-confined geometries, semiconductor nanowires (NWs) are essential in the "Beyond CMOS" era. Regarding transistor realizations, bottom-up grown NWs, with their cylindrical shape and potentially smooth surface, feature excellent gating capabilities using a surrounding gate stack. [24,49,61,62] Moreover, NWs provide a favorable geometry as a starting material for SBFETs, [50] as they feature enhanced lattice relaxation properties advantageous for heterojunction formation, which are not accessible in bulk systems. [63]

In the past, nanoscaled Al-Ge junctions embedded in Al-Ge-Al NW heterostructures drew great attention, attributed to their integration capability in superconductor-semiconductor devices, which enabled the exploration of quantum effects and the realization of JJ-FETs. [30,47,64] On the basis of NW SBFETs, also promising nanoelectronic device concepts were realized in the past. First, reconfigurable FETs (RFETs), which merge the properties of a *n*- and *p*-type transistor in a single device by using the capability of charge carrier filtering inherently provided by SBFETs. [42, 65, 66] Thus, enabling to switch between *n*- and *p*-type operation even during runtime. Weber et al. published essential contributions in this respect, leading to a profound understanding of RFETs. [42,49,67,68] Second, devices with negative differential resistance (NDR), whose function is inherently provided by the band structure of Ge, enabled by the accessibility of the transferred electron or Gunn effect. [69,70] Therefore, sufficiently high electric fields must be applied to the Ge channel, decreasing the current despite increasing the bias voltage. In the past, numerous NDR investigations on Ge-based NWs were carried out. [45,71–73] In this respect, certain NDR figures of merit (FOM) of Al-Ge-Al heterostructure SBFETs were already determined. [74] Importantly, in 2021 also on base of an Al-Ge-Al SBFET, a RFET architecture with a tunable NDR region was proposed by Sistani et al., [75] demonstrating a promising device towards the realization of multi-valued logic (MVL), [76] which perform calculations with a higher base than two.

1.1 Motivation

Based on the introduction and the discussed topics, the following section lays out the motivation of the PhD thesis at hand, focusing on the used materials, characterization methodologies, and derived devices and applications.

Characteristics of Al-group IV heterojunctions in SBFETs
In the past, Al as source/drain contacts in SBFETs was established to create heterojunctions with 1D-confined Ge nanostructures, i.e., Ge NWs. [45, 59] Thus, resulting in the formation of an abrupt metal-semiconductor interface without an inter-metallic phase and the possibility to create ultrascaled Ge quantum dots. [77] In this respect, the material system was investigated thoroughly from a low-temperature physics aspect, exploring quantum effects. [47, 64] Recently, based on Al-Ge-Al NW heterostructure SBFETs, also nanoelectronic applications were realized, such as RFETs and devices with NDR. [43,74,75] Setting the Al-Ge material system into perspective to Si and $Si_{1-x}Ge_x$ raises the question of fabricating NW-based heterostructure SBFETs based on Si. In the case of successfully achieving Al-Si and Al-$Si_{1-x}Ge_x$ based SBFETs, the charge carrier transport is of particular interest because of an expected difference of the Fermi level pinning evident in the thereof obtained MSJs. In particular, the Al-Si material system promises similar SBHs for electrons and holes. [78] Moreover, in transistor applications, relevant FOM, such as on- and off-currents, and the subthreshold slope, to name prominent parameters, [79] are of high interest and shall be evaluated for the obtained devices.

How do Si, $Si_{1-x}Ge_x$ and Ge NWs perform regarding the Al solid-state exchange mechanism? What are particular charge carrier transport mechanisms in Al-group IV Schottky junctions integrated in SBFETs?

Applying advanced characterization methodologies

In general, transfer (I_D vs. V_G) and output (I_D vs. V_D) characteristics are the two basic methods to characterize transistors electrically. [17] In SBFETs, the gate electrostatics and absolute temperature considerably impact the manifold charge carrier transport mechanisms. Moreover, the absolute temperature in the scope of thermionic emission (TE) plays an important role, as dedicated SBs are evident in the proposed devices. In this sense, advanced characterization methodologies are required to understand the charge carrier transport and operation regimes of SBFETs. Thus, inspired by low-temperature physics, [47,80] T-dependent bias spectroscopy shall be explored as a methodology to evaluate operation regimes of the proposed Al-group IV SBFETs. In this respect, bias spectroscopy allows to consider the influence of multiple parameters, which single-parameter sweeps can not cover.

How can advanced characterization methodologies, such as T-dependent bias spectroscopy, lead to a more profound understanding of Al-group IV semiconductor junctions and devices?

Utilizing Al-group IV SBFETs for emerging devices

Reconsidering the already stated research questions and raising the primary goal of the "Beyond CMOS" era in using emerging materials and architectures to realize device concepts, the obtained results shall be facilitated. Therefore, NDR in Ge-based devices has been investigated in the past in different geometries and device architectures. [70, 74] As mentioned previously, even a NDR-mode RFET on base of Al-Ge-Al NW heterostructures was proposed. [75] Additionally, essential contributions in the field of MVL were published, which also rely on NDR. [76,81] Therefore, a well-controllable and predictable NDR regime is required. In this context, resonant tunneling diodes (RTDs) based on group III-V semiconductors exhibit desired properties; however, they require complex device designs, which are pre-defined during fabrication. [17, 82] In the scope of the thesis at hand, an approach to evaluate dedicated NDR regimes in Al-Ge SBFETs shall be examined. Moreover, the possibility of tuning and enhancing the NDR functionality shall be investigated.

How can the understanding of Al-group IV SBFETs contribute to the realization of emerging devices? How can the obtained insights improve the tunability and enhancement of NDR in Ge-based SBFETs?

1.2 Outline

First, in **Chapter 2**, the theoretical background of the underlying materials and the proposed MSJs, as well as the involved charge carrier transport, is elaborated. Additionally, two important nanoelectronic device concepts – RFETs and devices with NDR – are discussed and presented in conjunction with state-of-the-art devices.
Chapter 3 presents the SBFET device integration and discusses the used structural and electrical characterization techniques. Regarding SBFET FOM, the focus is set on the applied methodologies used for their extraction. Additionally, the concept of bias spectroscopy is introduced.
Having discussed the underlying theory as well as experimental techniques, **Chapter 4** presents the obtained results, which may answer the previously stated research questions (cf. Section 1.1). Therefore, in the first step, the structural properties of the investigated Al-group IV MSJs are presented, followed by detailed electrical characterizations of the obtained SBFETs, where also T-dependent bias spectroscopy is used to compare the different material systems. In the next step, investigations of the first Al-Si based RFET and, thereof, realized basic logic circuits are presented. In the scope of facilitating Ge, NDR based on Al-Ge SBFETs and multi-gate SBFETs is exploited, enhancing NDR tunability. Further, the proposed SBFETs are implemented in cascode circuits, demonstrating increased NDR functionality. Finally, top-down fabricated Al-Ge based SBFETs are presented, on which a bias-tunable temperature coefficient of resistance (TCR) is demonstrated.
Lastly, **Chapter 5** summarizes the main aspects discussed in the PhD thesis at hand and reflects the stated research questions. Additionally, an outlook on potential extensions is given.

Appendix A provides additional insights on Al-Si and Al-Ge based SBFETs, which support the presented results. Further, Appendix B shows the first TCR results of Al-Si based SBFETs realized from silicon on insulator (SOI).

Finally, a selection of state-of-the-art vs. novelties regarding Al-group IV SBFETs is illustrated in Figure 1.2, laying out the achievements obtained in the scope of the PhD thesis at hand.

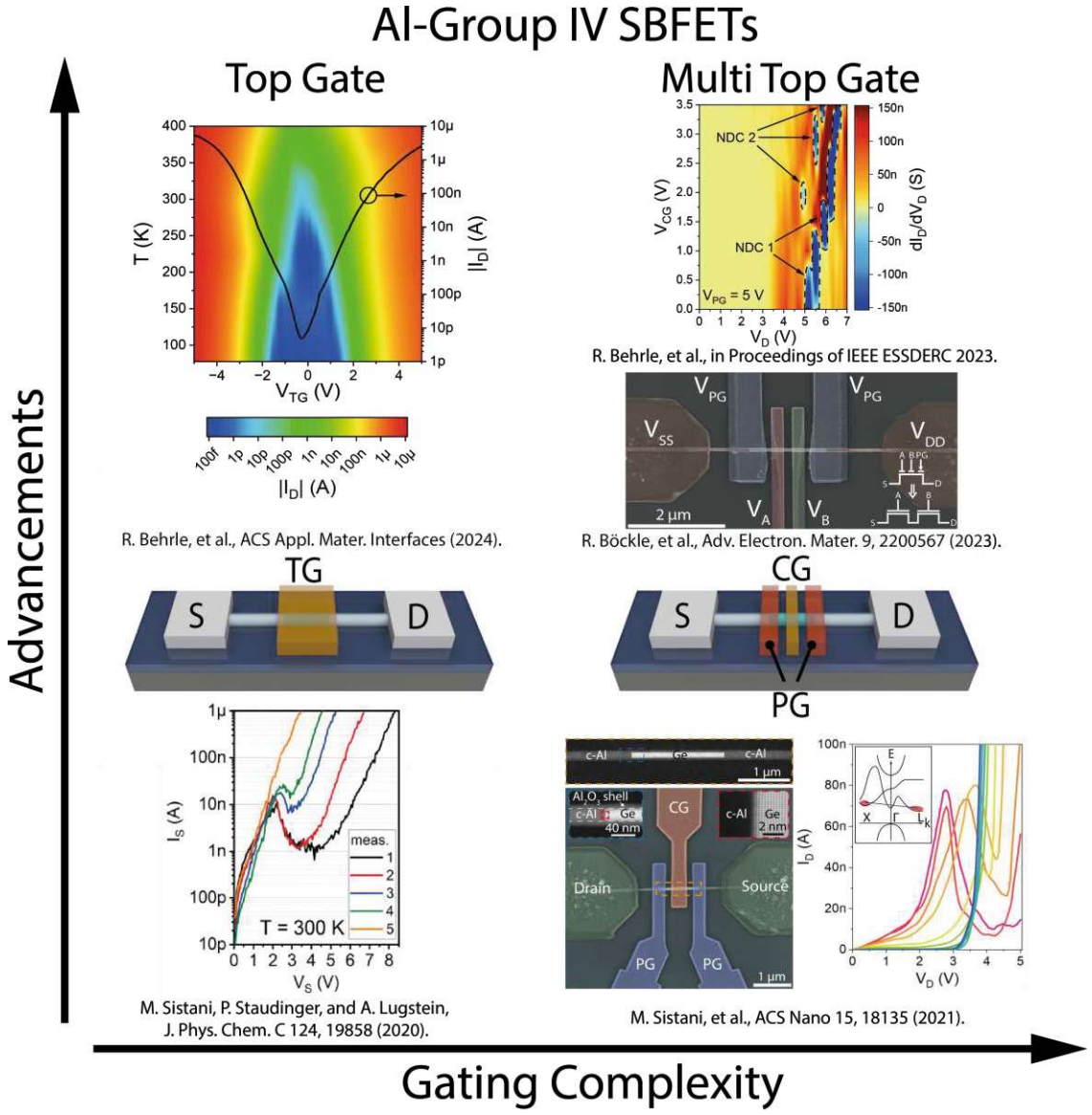


Figure 1.2: *Evolution of different Al-group IV SBFET architectures in applications and used methodologies. The bottom row shows past achievements based on the architectures illustrated in the middle. The top row shows highlights obtained within the PhD thesis at hand.*

Chapter 2

Background

This chapter discusses the theoretical background required to answer the stated research questions (cf. Section 1.1) and considers state-of-the-art methodologies as well as already-realized devices in relation to the proposed work.
First, Section 2.1 elaborates on the used materials and physical properties of semiconductor NWs. Next, Section 2.2 presents theoretical aspects of the heterojunction formation, where special attention is given to the thereof obtained SBs and their inherent electronic properties. Section 2.3 discusses the functional concept and involved charge carrier transport in SBFETs. Further, the modeling of the effective Schottky barrier height (eSBH), also denoted as activation energy E_a, is covered. Moreover, the transferred electron effect, enabling NDR in Ge, is elaborated. Lastly, Section 2.4 reviews and discusses state-of-the-art RFETs as well as Ge-based devices with NDR.

2.1 Materials

In contrast to more common silicides and germanides, in the work at hand, Al is used as source/drain metal contacts to the semiconductor because of its establishment in the Al-Ge material system broadly used within the low-temperature physics community exploring quantum effects. [30, 46, 47] Further, as the focus is set on Si, $Si_{1-x}Ge_x$ and Ge NWs, the gained CMOS knowledge obtained in the last decades is beneficial in terms of realizing "Beyond CMOS" devices. [49]
Therefore, this section introduces the materials used in the proposed Al-group IV SBFETs [cf. Figure 1.1(b)]. As the source/drain metal is a particular feature of SBFETs, Al as such is elaborated in Section 2.1.1, followed by a section covering the two group IV semiconductors, Si and Ge, as well as its compound $Si_{1-x}Ge_x$ in Section 2.1.2. Finally, Section 2.1.3 discusses the physical and structural properties of semiconductor NWs.

2.1.1 Aluminum

Aluminum (Al) is a metal with the atomic number 13 and exhibits a lower density of $2.67\,\mathrm{g/cm^3}$ at room temperature (RT) (293.15 K) in comparison to other common metals (cf. Fe: $7.87\,\mathrm{g/cm^3}$), making it favorable for a wide range of light-weight applications. For a free Al atom an empirical radius of 143 pm was evaluated. [83] Furthermore, without the influence of other elements, Al crystallizes as a face-centered cubic (fcc) crystal with a lattice constant of $a = 404.9\,\mathrm{pm}$ at RT. [84] Caused by its electron shell configuration with a few electrons available for metallic bonding, Al exhibits a relatively low melting point of 933.5 K, a low electrical resistivity of $2.65 \times 10^{-8}\,\Omega\,\mathrm{m}$ at RT and a thermal conductivity of $237\,\mathrm{W/(m\,K)}$. [85] The work function, which is the energy required to remove an electron from the Al bulk surface to vacuum, is in the range of 4.06 eV to 4.26 eV and is (theoretically) an important aspect to consider within the realization of SB-based devices as the work function directly determines the potential barrier when in intimate contact with a semiconductor (cf. Section 2.2.2). [17, 86] Due to its relatively low resistivity and high thermal conductivity, Al was used vastly in the past as a metallization and interconnect material. [87] Moreover, the use of Al was promoted by the lower influence of deep-level impurities acting as discrete energy levels within the Si or Ge band gap, whereas, e.g., Au impurities exhibit energy levels close to the intrinsic Fermi level. [17] However, increased on-currents revealed a significant drawback of bulk Al in terms of void formation and electromigration, [88, 89] causing avoidance of Al in front end of line (FEOL) processes. [87] Considering the exhibition of superconductivity at a critical superconducting temperature $T_\mathrm{c} = 1.2\,\mathrm{K}$ and a critical magnetic field of 10 mT, the use of Al was successfully demonstrated in superconductor-semiconductor-superconductor devices for the realization of Josephson junction FETs (JJ-FETs). [46, 47]

Aluminum oxide

In the era of high-κ dielectrics, the native oxide of Al, i.e., Al_2O_3 plays an important role in terms of semiconductor surface passivation reducing the density of interface traps (D_it), [90, 91] and additionally ensuring scaling paradigms [1]. The electrical insulator exhibits a band gap $E_\mathrm{g} \approx 8.7\,\mathrm{eV}$ and has a dielectric constant $\varepsilon_\mathrm{r} \approx 9$ for amorphous deposited Al_2O_3. [92] Therefore, a 10 nm thick layer of Al_2O_3 exhibits an equivalent oxide thickness EOT $= t_{\mathrm{high}-\kappa} \cdot (\varepsilon_{SiO_2}/\varepsilon_{\mathrm{high}-\kappa})$ of 4.3 nm. Further, it has a dielectric strength $\mathcal{E}_\mathrm{ds} \approx 13.5\,\mathrm{MV/cm}$. [86] Another important characteristic of Al_2O_3 is its high density of fixed charges (Q_f) with negative polarity, formed at the SiO_x interface, [93–95] leading to the repulsion of electrons at the $Si/SiO_x/Al_2O_3$ interface. Consequently, Al_2O_3 as gate oxide is not used in very-large-scale integrated (VLSI) Si-technology, but the suppression of surface recombination can be useful, e.g., in solar cells. [96] In this respect, Hiller et al. extracted negative fixed charges in $SiO_2/AlO_x/SiO_2$-stacks on Si with Q_f in the range of $10^{11} - 10^{12}\mathrm{cm^{-2}}$, using C/V measurements. [95] As the influence of interface and surface trapped charges are highly relevant for NWs, a more detailed discussion is given in Section 2.1.3.

In the past, Al was restricted in the FEOL of planar MOSFETs because of **void formation and electromigration with Si at high currents.** Notably, nanoscaled Al was successfully implemented for the **realization of superconductor-semiconductor junctions**, where **Al becomes superconducting** at $T_c = 1.2\,\mathrm{K}$. Attributed to the high oxygen reactivity, Al enables the formation of Al_2O_3, a high-κ dielectric ($\varepsilon_r \approx 9$) with $\mathbf{Q_f^-}$ **in the range of** $\mathbf{10^{12} - 10^{13}\,cm^{-2}}$.

2.1.2 Silicon and Germanium

This section discusses the two group IV semiconductors, Si and Ge, used as channel material for the proposed SBFETs. Additionally, the compound $Si_{1-x}Ge_x$ is considered. Moreover, their associated native oxides are discussed.
If not otherwise stated, information from "Semiconductor Devices: Physics and Technology" by S.M. Sze is used. [17]

Elemental Si
Si is a semiconductor with atomic number 14 and is in the 4$^{\mathrm{th}}$ group. It has its melting and boiling point at 1687.15 K and 3538.15 K, respectively. Empirically, a Si atom exhibits an atomic radius of 111 pm. Its electron affinity (Si crystal surface) $qX_s = 4.05\,\mathrm{eV}$ and is defined as the energy required to remove an electron from the conduction band E_C to vacuum. As mentioned in the introduction, Si is widely used for a broad range of electron devices. In this respect, Si used as channel material in transistors, exhibits a face-centered diamond cubic crystal structure with a lattice constant $a = 543\,\mathrm{pm}$ at RT. The band structure of Si, shown in Figure 2.1, reveals the indirect band gap nature of Si with $E_g(\mathrm{Si}) = 1.12\,\mathrm{eV}$. Thus, valence electrons excited by a photon need a momentum change to transit to the conduction band. Note that the Si surface orientation and any compressive or tensile strain have a crucial impact on the band structure. [97] Consequently, leading to a change of the effective mass m^* and further of the mobilities of electrons and holes μ_n/μ_p. [98,99] In this respect, the effective mass m^* is defined according to Equation (2.1), illustrating that the second derivative of the $E(k)$ relation (band structure) defines the (inverse) effective mass m^* and thus influences the mobility μ of the charge carriers. The mathematical relation between the effective mass m^* and mobility μ is discussed in detail in Section 2.3.3.

$$(m^*)^{-1} = \frac{1}{\hbar^2}\frac{\partial E}{\partial k^2} \tag{2.1}$$

Especially in nanoscaled structures, i.e., NWs, quantum effects also considerably impact the band structure (cf. Section 2.1.3), as reducing the dimensionality leads to band splitting. [100] Nevertheless, the illustrated bulk band structure shows the main characteristics of Si. Note that bulk parameters of Si compared to other relevant semiconductors are shown in Table 2.1.

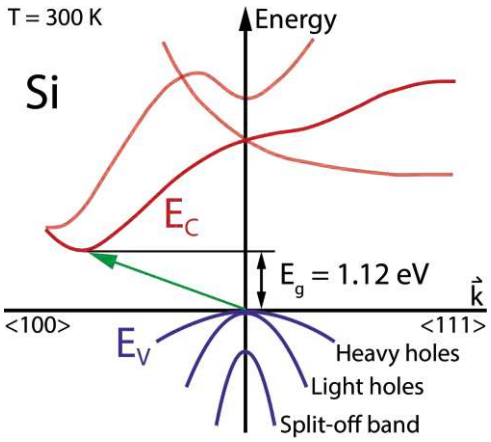


Figure 2.1: *Band structure of bulk Si. The green arrow indicates that charge carrier transition is only possible by an additional momentum component, e.g., phonon excitation, due to the indirect band gap E_g. The valence bands are illustrated as heavy and light holes as well as split-off bands. Image adapted from [101].*

Silicon dioxide

Attributed to the capability of growing native SiO_2 from Si paved the way for Si technology in the semiconductor industry. Moreover, thermally grown SiO_2 exhibits a relatively low density of interface trap states (D_{it}). Amorphous SiO_2 (grown by thermal oxidation) exhibits a band gap of 9 eV at 302 K and has a relative dielectric constant $\varepsilon_r = 3.7$ to 3.9. [17] The dielectric strength $\mathcal{E}_{ds} \approx 10\,\mathrm{MV/cm}$ depends on the level of impurities and defects, which act as localized electric field enhancements on the surface. In general, fixed charges Q_f in the Si/SiO_2 stack are positive because of incomplete Si bonds, which can be defined as a charge sheet at the interface with densities of about $10^{10}\mathrm{cm}^{-2}/\mathrm{eV}$ considering a ⟨100⟩-oriented Si crystal. [49] Besides its use as passivation, [102] it also progressed below ~2 nm thickness for the application as gate dielectric in MOSFETs. [103, 104] Moreover, SiO_2 is used for diffusion and ion implantation masks, where Si-nitrides also play an important role. Importantly, SiO_2 can be fabricated by wet and dry thermal oxidation, whereas dry thermal oxidation achieves a higher quality in yielding a lower density of trap states. In general, thermally grown SiO_2 with a thickness x consumes a layer of Si with a thickness of $0.44x$ (growing 100 nm SiO_2 consumes 44 nm Si). Regarding fabrication processes, SiO_2 can be patterned and etched using hydrofluoric acid (HF).

Si is the **most common semiconductor used for electron devices** and has an **indirect band gap** $E_g = 1.12\,\mathrm{eV}$. It enables the **growth of its high-quality native SiO_2** by thermal oxidation with low D_{it} in the $\sim 10^{10}\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ range.

Elemental Ge

Ge is located in the 4$^{\text{th}}$ group of the periodic system as well and is also an indirect semiconductor like Si. The melting and boiling temperature of Ge is 1211.4 K and 3106 K, respectively. An isolated Ge atom has an atomic radius of 122 pm. The electron affinity of the Ge surface is 4 eV and thus exhibits a similar value to Si (cf. Si: 4.05 eV). Moreover, Ge crystallizes in the same diamond crystal structure as Si with a lattice constant $a = 565.77$ pm. Figure 2.2 shows the band structure of bulk Ge with the conduction band E_{C} highlighted at $k = \langle 111 \rangle$ (also denoted as L-valley) as well as the 2$^{\text{nd}}$ conduction band (ΔE) at $k = \langle 100 \rangle$ (also denoted as X-valley). The direct band gap $E_{\Gamma 1}$ only exhibits an energy difference of 0.14 eV to the indirect band gap E_{g}. Thus, using band gap engineering approaches, i.e., applying strain, allows to realize light-emitting diodes or lasers. [105,106] The ΔE valley has an energy difference of 0.19 eV to the indirect band gap E_{g}, which plays the main role in the transferred electron effect, leading to NDR. [69] Note that a detailed discussion regarding the transferred electron effect, resulting in NDR is described in Section 2.3.3.

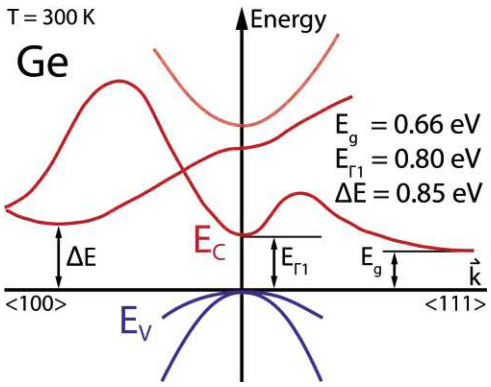


Figure 2.2: *Band structure of bulk Ge, revealing its indirect band gap E_{g}. The upper valence band E_{V} indicates heavy holes, whereas the stronger bent valence band illustrates light holes [cf. Equation* (2.1)*]. Image adapted from [107].*

Ge has an indirect band gap $E_g = 0.66\,\text{eV}$, which is ~67 % lower than that of Si. Thus, using Ge as channel material in transistors promises lower supply and threshold voltages. [61, 108] Attributed to the lower band gap, Ge has the drawback of higher source/drain leakage currents than Si. [109] In relation to Si, Ge exhibits hole mobility values, which are ~3 times higher, supporting faster switching speeds in *p*-type transistors. Although Ge has benefiting properties for the realization of transistors and was even used for the first-ever realized transistor by Bardeen and Brattain, [110] Ge was not broadly used in the past. This fact can be attributed to two issues: First, in Ge bulk based diodes and transistors, spontaneous screw dislocations occurred (Germanium whiskers), which may lead to electrical shorts. [111] Second, its native oxide Ge_xO_y, which may consist of different material phases, e.g., GeO_2 or Ge_2O_3, is soluble in water and is not stable at ambient conditions. Moreover, the fabrication of pure Ge is more cost-intensive compared to Si. [112]

Germanium oxides (Ge_xO_y)

In contrast to Si, which enables the fabrication of high-quality SiO_2 by thermal oxidation, Ge does not inherently feature the fabrication of a reliable native oxide. Nevertheless, two stable native oxides – GeO_2 and GeO – exist, where especially GeO_2 leads to a reduction of the density of interface trap states at the Ge/GeO_2 interface with values as low as $10^{11}\text{cm}^{-2}\text{eV}^{-1}$. [113, 114] However, also Ge_2O_3 and Ge_2O are formed during oxidation, which are not stable and exhibit D_{it} values up to $10^{15}\text{cm}^{-2}\text{eV}^{-1}$. [31, 115, 116] Moreover, all Ge_xO_y phases remain water soluble.

Ge has an **indirect band gap** $E_g = 0.66\,\text{eV}$, enabling **lower supply voltages** compared to Si. Moreover, its **high charge carrier mobility** promises higher switching speeds than Si. Ge **inherently features NDR functionality** by accessing the transferred electron effect. Its **native oxide Ge_xO_y consists of different oxide specimens**, which can be **water soluble** and are not stable at ambient conditions.

$Si_{1-x}Ge_x$ compound

Silicon-germanium is an alloy with a particular molar ratio of Si and Ge, and has the molecular formula $Si_{1-x}Ge_x$, which notation is also used throughout the work at hand. Considering the atom radii of Si (111 pm) and Ge (122 pm), reveals that Ge atoms are ~4 % larger than Si atoms. In this respect, the realization of stable $Si_{1-x}Ge_x$ structures was restricted in the past due to manufacturing challenges. However, such lattice mismatch issues can be tackled by the integration of $Si_{1-x}Ge_x$ in nanoscaled devices, i.e., NWs, because of their lattice relaxed nature (cf. Section 2.1.3). [49] In the same manner as for pure Si and Ge, $Si_{1-x}Ge_x$ crystallizes in a diamond cubic crystal structure. [117] Nowadays, $Si_{1-x}Ge_x$ is commonly used as source/drain material to strain the channel of *p*-MOSFETs, resulting in higher charge carrier mobilities and consequently increased on-currents. [98] Moreover, attributed to its compound nature, $Si_{1-x}Ge_x$ offers the possibility of band structure and band gap engineering within the boundaries of Si and Ge, which gets obvious in the corresponding semiconductor parameters in Table 2.1.
In terms of $Si_{1-x}Ge_x$ oxidation, LeGoues et al. found that Ge piles up at the $SiO_2/Si_{1-x}Ge_x$ interface with Ge playing a catalytic role, enhancing the reaction rate by a factor of approximately three. [118] Therefore, the formation of native SiO_2 is also possible on base of $Si_{1-x}Ge_x$. In this respect, on a $Si_{0.14}Ge_{0.86}$ sample a negative Q_f and D_{it} in the range of $10^{12}cm^{-2}$ was extracted by LeGoues et al. In terms of high-κ oxide deposition, the $Al_2O_3/Si_{0.7}Ge_{0.3}$ interface was investigated by Kavrik et al, [119] claiming $D_{it} = 10^{12}cm^{-2}eV^{-1}$.

$Si_{1-x}Ge_x$ allows to **engineer the band structure and (indirect) band gap within the range of pure Si and Ge**. It also features the **fabrication of native SiO_2**, however with the **drawback of a Ge pile-up** at the $SiO_2/Si_{1-x}Ge_x$ interface. In this context, Q_f^- and D_{it}^- in the range of $10^{12}cm^{-2}$ was extracted, which also holds for the $Al_2O_3/Si_{0.7}Ge_{0.3}$ interface.

Finally, Table 2.1 shows characteristic bulk parameters of the discussed group IV semiconductors, Si and Ge, as well as its compound $Si_{1-x}Ge_x$. For reference, parameters of the common group III-V semiconductor, GaAs, are also shown.

Parameter	**Elemental Si**	**Elemental Ge**	**$Si_{1-x}Ge_x$**[a]	**GaAs**
Band gap energy (eV)	1.12	0.66	0.80-1.05	1.42
Breakdown field (V/cm)	~3 $\times 10^5$	~1 $\times 10^5$	~1.5-2.5 $\times 10^5$	~4 $\times 10^5$
Effective mass				
Electrons (m_n^*/m_0)	0.26	0.12	~0.12-0.26	0.063
Holes (m_p^*/m_0)	0.49	0.33	~0.33-0.57	0.57
Intrinsic carrier concentration (cm^{-3})	9.65 $\times 10^9$	2.4 $\times 10^{13}$	1.8-0.6 $\times 10^{13}$	2.25 $\times 10^6$
Lattice constant (pm)	543	565	560-549	565
Mobility [$cm^2/(V\,s)$]				
μ_n (Electrons)	1450	3900	3300-2100	9200
μ_p (Holes)	505	1800	1537-813	320

Table 2.1: *Comparison of relevant bulk parameters of semiconductors under investigation, extracted from [17, 121]. Value ranges for $Si_{1-x}Ge_x$ are covering high to low Ge content. Note that m_0 is the free electron mass. Additionally, GaAs parameters are shown for comparison. Note that absolute values may differ for low-dimensional structures, i.e., NWs. [49]*

[a] Parameters for $Si_{1-x}Ge_x$ are extracted from [120] and show results of $Si_{0.25}Ge_{0.75}$ and $Si_{0.75}Ge_{0.25}$.

2.1.3 Semiconductor Nanowires

NWs are nanoscaled structures with a cylindric or facetted shape and a diameter in the nm-regime. Based on these structures, many different materials can be implemented, ranging from metallic, [122] semiconducting, [123] and even superconducting NWs, [124] demonstrating their versatile nature. [125,126] In general, the fabrication methodology can be differentiated between bottom-up grown NWs, which mostly use chemical vapor deposition (CVD) methodologies, e.g., vapor-liquid-solid (VLS) growth, [127] and top-down NWs, [128] where NWs with a rectangular shape (also denoted as nanosheets) are patterned from a thin film, i.e., silicon on insulator (SOI) [129]. Notably, using a bottom-up NW growth mechanism inherently defines the channel's diameter, allowing it to exclude lithography. In particular, etching processes may lead to higher surface roughness and dangling bond density, which certainly becomes relevant for top-down fabricated nanosheets. In this context, additional annealing steps are required for top-down NWs to reduce the density of trap states. [130] A significant advantage of bottom-up methodologies is the ability to use a wide variety of precursors, allowing the realization of compounds and heterostructures. [131]

Moreover, bottom-up grown NWs enable doping without the need for ion implantation, where desired doping atoms are supplied by the used precursor gas. [132] In terms of heterostructure formation, the lattice relaxation properties of NWs are beneficial, whereas the realization of heterostructures is a challenging task for bulk semiconductors. [63,126,131] For passivation or gate dielectric deposition, vertically VLS-grown NWs provide the possibility to cover them in a surrounding insulator, enabling GAA implementations. [20, 133, 134] Thus, providing the best achievable electrostatic gating capability compared to other gating concepts. [49] However, bottom-up, VLS-grown NWs have limitations in deterministic position control, as the growth catalyst defines the position of the NW growth. [135] Nevertheless, strategies including contact printing of parallel NW arrays, [136] and the growth of in-plane NWs in combination with guided or patterned ledges were proposed. [137] In this context, 3D-stacked NW integration methodologies were demonstrated as well. [138] In general, VLS-grown NWs exhibit a multi-facet cross-section, as shown in Figure 2.3(b). However, NWs are mostly illustrated as cylinders with a circular shape for simplification reasons. In the scope of the thesis at hand, the focus is set to nominally un-doped group IV semiconductor NWs, which build the channel material of SBFETs. Moreover, NWs grown by the VLS methodology will be considered unless otherwise stated.

VLS-grown semiconductor **NWs are a versatile platform, enabling the realization of radial heterostructures**, which is supported by their **inherent lattice relaxed nature**. NWs provide an **excellent gating capability**, enabled by their cylindrical shape, further exhibiting a **high surface-to-volume ratio**.

Semiconductor nanowires in nanoelectronics

In general, bottom-up grown NWs are promising building blocks in the ”Beyond CMOS” era due to previously mentioned aspects, which cover excellent gating capabilities and versatile material compositions as well as having decent lattice relaxation properties. Moreover, dimension scaling of NWs allows to engineer the band structure and, therefore, influencing the charge carrier transport, enabling particular advancements, as discussed next. As shown in Figure 2.3(a), considering a NW with diameter d_{NW} that is orders of magnitudes smaller than the channel length allows to set d_{NW} in relation to the exciton Bohr radius a_{B}^{*}, which is defined as the distance required to separate an electron and hole. [139] Thus, leading to discrete energy states and resembling an energy spectrum evident in a 1D-confined density of states (DOS) system. In general, the DOS determines the number of allowed states, which results in a quantization in low-dimensional systems. In bulk (3D) – with spatially free movement of charge carriers – a continuously increasing (parabolic) energy spectrum is evident, whereas, in 2D systems, the energy spectrum changes to constant terraces with decreasing DOS for higher energies.

In 1D systems, i.e., NWs, energy states, known as van Hove singularities, are accessible. Further, these are often denoted as 1D-confined systems because charge carrier movement is only possible in one spatially defined direction. [17] For the sake of completeness also quantum dot (0D) systems are mentioned, where merely discrete energy peaks are evident, resulting in single confined charge carriers. The exciton Bohr radius $a_{\mathrm{B}}^{*} = 4.9\,\mathrm{nm}$ and 24.3 nm for Si and Ge, respectively, showing that quantum confinement in Ge NWs takes place at a larger d_{NW} in comparison to Si. [139, 140] Regarding the DOS, quantum confinement leads to shifts and band splitting in the band structure, affecting the charge carrier distribution, effective masses m^{*}, charge carrier mobilities μ and quantum capacitances. In general, the band gap E_{g} increases with decreasing the diameter d according to $E_{\mathrm{g}} \sim d^{-\mathrm{n}}$, with n being a factor equal to unity or higher. [49, 141] Thus, on 1D-confined Si and Ge NWs – also considering the crystal orientation – the exhibition of a direct band gap was demonstrated. [99, 142] Regarding the NW channel length L_{SC}, the mean free path of charge carriers needs to be considered, as this may lead to an increased contribution of ballistic charge carriers. The characteristic of ballistic transport is that it is not diffusive, i.e., it does not scatter at impurities or other defects. Thus, the mobility μ does not play an important role, and the average carrier velocity does not depend on the lateral electric field. [49] Simulations by Gilbert et al., including phonon scattering in Si NW transistors, revealed a mean free path of ~1.4 nm, which also indicates the good scaling possibilities of the Si-technology. [143] For Al-Ge-Al NW heterostructures with nominally un-doped ⟨111⟩ oriented Ge NWs, Sistani et al. evaluated a RT mean free path of 45 nm. [64]

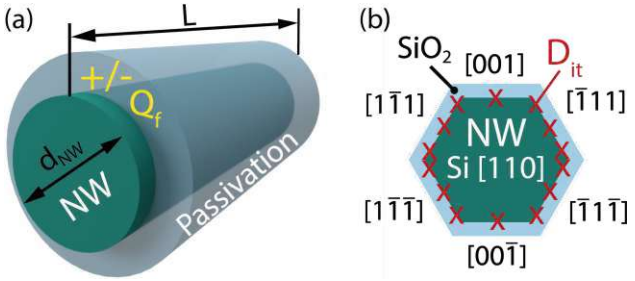


Figure 2.3: *(a) Illustration of a simplified NW with dimensions and indicated fixed oxide charges Q_{f}, which can be positive or negative. Additionally, a passivation/dielectric shell is shown. (b) Example of an ⟨110⟩-oriented Si NW showing a difference of D_{it} in correspondence to its surface orientations. The ⟨001⟩ and ⟨00$\bar{1}$⟩ surfaces exhibit a lower D_{it} in comparison to the other directions. Image adapted from [49].*

Another important aspect to consider is the influence of charged surfaces and trap states, which is, in particular, crucial for NW applications, [144,145] because of their large surface-to-volume ratio.

As shown in Figure 2.3(a), one distinguishes between fixed charges in the dielectric (Q_f), mainly responsible for threshold voltage shifting, [17] and interface trapped charges (Q_it) in charges/cm^{-2}, where the polarity – positive (donor) or negative (acceptor) – determines the particular influence on the charge carrier transport. [49, 145] The latter is commonly given as an interface trap state density D_it in cm^{-2}eV^{-1}, where $D_\mathrm{it} = Q_\mathrm{it}/q$. In terms of D_it the surface orientation needs to be considered, [146] as D_it exhibits different values in dependence of the crystal surface orientation, also shown in the example of an ⟨110⟩ Si NW in Figure 2.3(b). [49] In consequence, processed NWs, i.e., oxidized Si NWs, have a complex multi-facet surface with a high variability of D_it. Importantly, trapped charges act as local gate charges, electrostatically influencing the charge carrier transport along the channel and further impacting the total current flow through the NW, which can cause a reduction of the active diameter area and restrict charge carrier transport to the core of the NW. [49] Hence, a low D_it is desired, which, e.g., can be achieved at the Si/SiO_2 interface by terminating dangling bonds at the Si interface by annealing, reducing Q_it to values in the range of 10^{10}cm^{-2}. [49] An effective way to extract D_it is through C/V measurements, [147] which, however, is challenging on single NWs because of low capacitance values [136]. In this respect, low-frequency noise (LFN) investigations are a promising way to overcome the limitation of low capacitances. [148] Nevertheless, from an experimental point of view, the explicit origin of traps is difficult to obtain. [149] Further, mechanical stress (strain or compression) on the NW can be applied to tune the band structure and the band gap. [97, 150] Remarkably, the concept of mechanical stress was successfully demonstrated by induced strain during thermal oxidation of Si NWs. [151, 152] Reconsidering the dependence between the band structure [$E(k)$] and the effective mass m^* [cf. Equation (2.1)], also the effective channel mobility μ is highly influenced by a change of the band structure. Consequently, having a direct impact on the on-currents and switching speeds. [37, 98] In terms of the mobility extraction of single NWs, considering a MOSFET behavior with ohmic contacts in the triode and saturation region, Equation (2.2) holds:

$$\mu = \frac{\partial I_\mathrm{D}}{\partial V_\mathrm{D}} \left(\frac{W}{L_\mathrm{G}} Q_\mathrm{i} \right)^{-1}, \tag{2.2}$$

where I_D is the current through the NW, V_D is the applied bias, W corresponds to d_NW, L_G is the gate channel length and $Q_\mathrm{i} = C_\mathrm{ox}(V_\mathrm{G} - V_\mathrm{t})$ is the channel/inversion charge, with V_G being the applied gate voltage and V_t being the thermal voltage (25.86 mV at RT). Notably, the gate oxide capacitance C_ox of a single NW is again challenging to extract due to low values which are below the resolution limit of conventional measurement equipment. [90] Concerning MSJs and their associated SBs (cf. Section 2.3.1), strong band bending mechanisms and a low DOS result mainly in a diffusive charge carrier transport. [17, 50] Nevertheless, on the basis of top-down fabricated NWs, certain methodologies were used to extract the mobility, including the fabrication of up to 1000 parallel NWs, increasing the capacitance, [153] or fabricating symmetric Hall bars for the extraction of the mobility. [154]

Using semiconductor NWs in nanoelectronics, **fixed charges Q_f and interface trap charges Q_{it} are critical aspects to consider** in terms of threshold voltage shifting and hysteresis. As **NWs exhibit low capacitance values**, i.e., C_{ox}, the extraction of D_{it} and the μ of single NWs is hindered by conventional C/V and I/V measurement methodologies.

In the scope of the thesis at hand, Si NWs with $d_{NW} >> a_B^*$ (Si: $a_B^* = 4.1\,nm$) are used, preventing the exhibition of 1D-confined effects. However, the used Ge NWs exhibit diameters d_{NW} in the range of the exciton Bohr radius of Ge (Ge: $a_B^* = 24.3\,nm$). Therefore, quantum effects need to be taken into account. In respect to the channel length L_{SC}, all proposed SBFETs have channel lengths that are orders of magnitude longer than the mean free path with lengths in the ~µm-regime. Thus, diffusive charge carrier transport is guaranteed. Note that no dedicated electrical investigations in dependence on the surface crystal orientation of NWs were performed. However, the previously discussed relations shall lay out the manifold influences of the NW nature on the charge carrier transport.

2.2 Metal-Semiconductor Junctions

The underlying metal-semiconductor junctions (MSJs) build the base of the proposed SBFETs and are essential for the charge carrier transport. Thus, Section 2.2.1 discusses the solid-state exchange reaction of Al and Si as well as of Al and Ge from a theoretical materials perspective. Moreover, the use of Al as source/drain metal is set in relation to the commonly used metal-silicides and -germanides. Further, Section 2.2.2 elaborates on the involved charge carrier transport mechanisms evident in SBs and, in particular, discusses Fermi level pinning of the obtained Al-group IV semiconductors, which highly influence the charge carrier injection into the semiconductor channel.

2.2.1 Metal-Group IV Heterojunctions

A significant prerequisite for realizing SBFETs is the formation of reproducible and abrupt MSJs. A convenient methodology to achieve such junctions is a thermally induced diffusion process leading to an exchange of the semiconductor and metal. Notably, a considerable advantage of such MSJs embedded in NWs is that the interfaces are never exposed to ambient conditions, thus promising low defect density at the MSJ. In this respect, intensive research was carried out for metals, forming metal-silicides and -germanides in conjunction with Si and Ge, respectively. [56,57] Moreover, Al plays a vital role in solid-state exchange mechanisms when brought into contact with Ge because no inter-metallic phase is formed, resulting in single-crystalline Al connected to Ge. Additionally, Al exhibits superconductivity at a critical temperature $T_c = 1.2\,\mathrm{K}$, which was driving research of Al-Ge junctions in the scope of low-temperature physics, exploring quantum effects. [30, 47]
In the following, the underlying solid-state exchange mechanism of the Al-Si and Al-Ge material systems is discussed from a theoretical point of view. Experimental considerations and processing techniques are introduced in Chapter 3. In the final part of this section, a summary of the insights and the relation to metal-silicides and -germanides is elaborated.

For a better understanding of the following section, Figure 2.4(a) shows the underlying material stack and progress of the solid-state exchange reaction, whereas Figure 2.4(b) illustrates the finally obtained NW heterostructure. Generally, the solid-state exchange mechanism follows the same theoretical considerations for all investigated Al-group IV material systems.

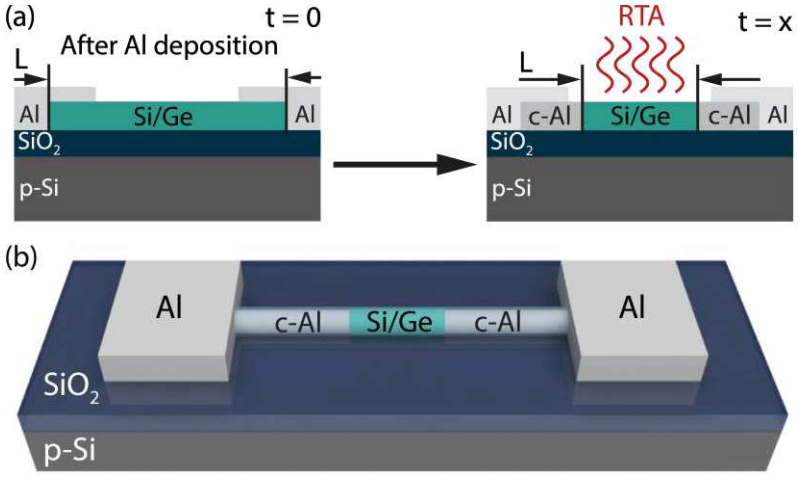


Figure 2.4: *(a) Material stack after Al deposition that progresses to reduced channel lengths L_{SC} by applying a rapid thermal annealing (RTA) process, initiating the solid-state exchange mechanism of Al and proposed group IV semiconductors. Moreover, Al allows subsequent annealing steps, enabling channel length adjustment without forming inter-metallic phases. (b) 3D illustration of the finally obtained NW metal-semiconductor heterostructure, including a passivation shell.*

Al-Si heterojunction

As discussed in Chapter 1, the Al-Si material system promises similar SBHs for the injection of electrons and holes, which is featured by symmetric Fermi level pinning. [78] Therefore, an ambipolar SBFET operation is expected, favoring the realization of RFETs. [43] In general, the Al-Si exchange mechanism can be analyzed from two perspectives. First, the Al-Si phase diagram describes the phases of the two materials in dependence on temperature and their molar ratio. Second, the diffusion coefficients of the corresponding materials at an absolute temperature. Therefore, in the first step, the Al-Si phase diagram shown in Figure 2.5 is analyzed to evaluate an appropriate annealing temperature, which was chosen at 773 K. In this respect, a rapid thermal annealing (RTA) process is used (cf. Section 3.1) to initiate the exchange mechanism. Importantly, a single eutectic point at a ratio of 12.6 wt % at $T = 820$ K is evident, leading to the fact that the exchange mechanism is indeed a solid-state reaction if executed at an annealing temperature of 773 K. Moreover, no inter-metallic stoichiometry is evident in the solubility gap of the phase diagram, as illustrated in Figure 2.5.

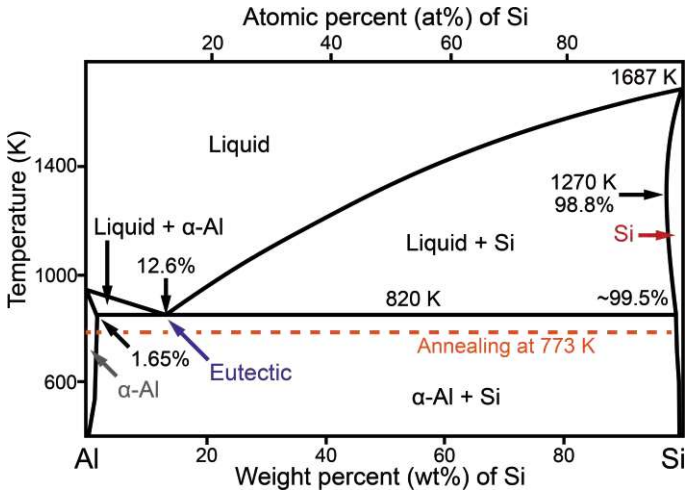


Figure 2.5: *Bulk binary Al-Si phase diagram. The chosen annealing temperature at* 773 K *is well below the eutectic temperature, enabling a solid-state exchange mechanism without forming intermetallic phases. %-values in the diagram are in weight percent* (wt %)*. Image adapted from [155].*

Next, the diffusion coefficients at a typical reaction temperature $T = 773\,\mathrm{K}$ are discussed, as illustrated in Table 2.2. Considerably, asymmetric diffusion kinetics are evident, where diffusion of Si in Al and Al in Al is comparatively high compared to Al in Si and Si self-diffusion, i.e., Si in Si. In this respect, Al atoms travel efficiently via a self-diffusion mechanism through the available Al and finally reach the Si surface, where they compensate for a Si atom. Thus, upon reaching the appropriate interface energy, a lattice space within the Si crystal is occupied. In this context, the lattice relaxed nature of NWs supports the MSJ assembly, although the lattice constants a of Al and Si differ (Al: 404.9 pm / Si: 543 pm, both at RT). Considering the diffusion coefficients and assuming Si diffusion in Al, enabled by interstitial occupation, Si atoms can diffuse across the entire Al segment and ultimately reach the Al pads and structure surface (cf. Figure 2.4). In this context, it is assumed that surface diffusion plays an important role.

Al in Al [156] (cm^2/s)	**Al in Si** [157] (cm^2/s)	**Si in Al** [158] (cm^2/s)	**Si in Si** [159] (cm^2/s)
6.2×10^{-10}	1.9×10^{-22}	4.4×10^{-8}	6.5×10^{-19}

Table 2.2: *Diffusion coefficients of the Al-Si material system. The diffusion coefficients are calculated for an annealing temperature of* $T = 773\,\mathrm{K}$*, whereas values of the indicated references were used.*

Al-Ge heterojunction

The thermally induced solid-state exchange mechanism can be evaluated in the same manner for the Al-Ge material system, where similar properties are evident. Compared to the Al-Si material system, Al-Ge junctions were broadly used in the past to explore quantum effects and nanoelectronic devices. [47, 64, 75] Concerning nanoelectronics, the inherent exhibition of NDR in Ge is of significant importance (cf. Section 2.3.3).
Starting with the Al-Ge phase diagram in Figure 2.6, a similar characteristic, but at lower temperatures, to the Al-Si material system with a single eutectic point at 51.8 wt % is evident. Again, no inter-metallic phases exist below the eutectic temperature $T = 693\,\mathrm{K}$, supporting the formation of single-crystalline MSJs. Here, an annealing temperature of 673 K was chosen to initiate the solid-state exchange mechanism. Moreover, consecutive annealing steps can be executed to define the channel length, which was proven by the fabrication of quantum disks with thicknesses below 10 nm. [77]

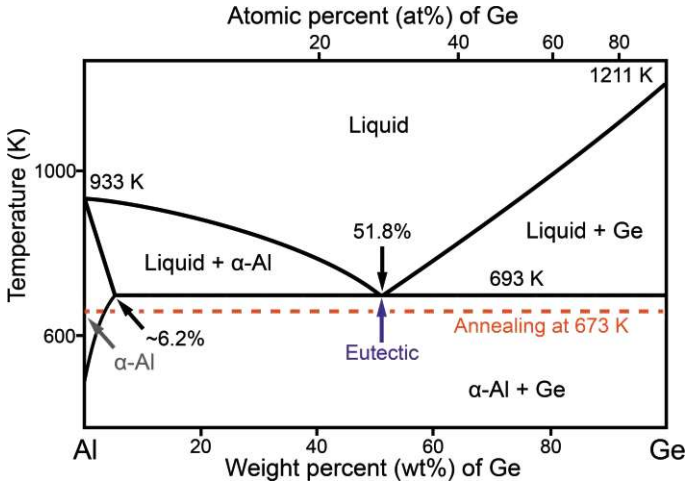


Figure 2.6: *Bulk binary Al-Ge phase diagram. The annealing temperature at* 673 K *is below the eutectic temperature, enabling a solid-state exchange mechanism without inter-metallic phases. %-values in the diagram are in weight percent (*wt %*). Image adapted from [160].*

The diffusion coefficients of the Al-Ge material system shown in Table 2.3 are analyzed in the next step, which again reveal asymmetric values but of a higher degree than the Al-Si material system. [156, 161] In this respect, the diffusion of Al in Ge and Ge self-diffusion is up to 13 orders of magnitude smaller than Al self-diffusion and Ge in Al diffusion. Thus, the same thermally driven diffusion mechanism is supported, as evident in the Al-Si material system. Note that the shown values are calculated for a proposed annealing temperature of 673 K.

Remarkably, the Al-Ge material system exhibits a lattice mismatch of $\Delta a = 161\,\mathrm{pm}$, however still maintaining abrupt and stress-free [59] MSJs as shown later in Section 4.1.3. However, at the interface, El Hajraoui et al. evaluated a rotation of 18° between the Al and Ge planes, which may be attributed to relaxation processes. [59] Similar investigations, but on top-down fabricated Al-Ge-Al heterostructures, were carried out by Wind et al. [162] In the latter work a rotation of 6° was evaluated. Remarkably, they also investigated the Al-Ge exchange mechanism in dependence of the crystal orientation by rotating the Ge-layer in steps of 22.5° from the initial $\langle 110 \rangle$ direction to an $\langle \bar{1}10 \rangle$ direction. Remarkably, no significant dependence on the exchange rate was observed, promoting the reproducible and stable Al-Ge exchange mechanism.

Al in Al [156] (cm^2/s)	**Al in Ge** [161] (cm^2/s)	**Ge in Al** [156] (cm^2/s)	**Ge in Ge** [156] (cm^2/s)
3.6×10^{-11}	1.5×10^{-23}	1.9×10^{-10}	1×10^{-22}

Table 2.3: *Diffusion coefficients of the Al-Ge material system. According to stated references, the diffusion coefficients are calculated for a temperature of* $T = 673\,\mathrm{K}$.

Al-$Si_{1-x}Ge_x$ heterojunction

Generally, one can expect that the Al-$Si_{1-x}Ge_x$ exchange mechanism follows a similar pattern as for the Al-Si and -Ge material systems. However, no dedicated Al-$Si_{1-x}Ge_x$ phase diagrams for certain Si/Ge compound ratios are available. In Reference [163], the inter-diffusion of Si and Ge is stated for different $Si_{1-x}Ge_x$ ratios, where values from approximately $10^{-28}cm^2/s$ to $10^{-19}cm^2/s$ for Si and Ge inter-diffusion can be calculated for an annealing temperature $T = 773\,\mathrm{K}$. However, no dedicated values are given for Al-$Si_{1-x}Ge_x$ diffusion.

Concerning the Al-$Si_{1-x}Ge_x$ exchange mechanism, Luong et al. performed investigations in a scanning transmission electron microscope (STEM) and analyzed the thereof obtained junctions on the basis of nominally un-doped and predominantly $\langle 111 \rangle$-oriented $Si_{0.67}Ge_{0.33}$ NWs. [164] Remarkably, they identified a Si-rich layer between the Al- and $Si_{0.67}Ge_{0.33}$-segment, which in theory may act as a Fermi level re-pinning interlayer, [165] because Al pins close to the middle of the Si band gap (cf. Section 2.2.2). [78]

Differences to metal-silicides and -germanides

Distinctly different in terms of the solid-state reaction, e.g., in NiSi, [57, 166] PtSi, [167] or CoSi [168], where the diffusive metal atoms react with the host Si lattice to form a compound phase at the interface to the pristine Si, in the proposed Al-group IV material systems no remaining Si or Ge within the intruded and reacted regions was found (cf. Section 4.1). The MSJ formation is further supported by asymmetric diffusion coefficients (cf. Table 2.2 and Table 2.3) as well as the phase diagrams (cf. Figure 2.5 and Figure 2.6). Consequently, Si and Ge are out-diffused and are entirely replaced by Al. In contrast, out-diffusion only plays a minor role for metal-silicides, as, e.g., in $NiSi_2$, most Si is retained, as the $NiSi_2$ exhibits a comparable Si density to the Si host lattice. [58] Moreover, the high Al purity of the Al leads was confirmed in the Al-Ge material system by electrical superconducting measurements. [47] Further, demonstrating a significant advantage of Al-group IV material systems due to the possibility of realizing superconductor-semiconductor devices. [169, 170] In terms of the annealing process, the Al-group IV solid-state exchange mechanism shows less variability in comparison to NiSi-Si junctions, because of a reproducible and deterministic metal phase without the formation of an inter-metallic phase. In this respect, metal-silicides also make use of alloying elements, e.g., W or Pt in $NiSi_2$, to improve morphology and stabilize crystallographic phases. [171] Therefore, limiting the flexibility in semiconductor processing that might introduce changes to the SBH, [172] which is avoided by the use of single-elementary Al. Nevertheless, thin ⟨110⟩-oriented Si NWs showed a direct lattice-matched $NiSi_2$ segment without the formation of different phases. [49] A significant advantage of silicides is their ability to use self-aligned processes resulting in salicides. [173] Attributed to the metal-salicide-semiconductor nature, selective metal etching can save an additional lithography process step promoting industrial applicability. [17] Regarding metal-Ge junctions forming germanides, such as NiGe, a higher variability and unpredictability in deterministic stabilization of phases impact the electronic transport and SBHs. [174, 175]

Phase diagrams and the asymmetric diffusion coefficients of the **Al-Si and Al-Ge material system support the formation of mono-elementary and single-crystalline Al leads to Si and Ge without the formation of inter-metallic phases.** Further, as demonstrated on the Al-Ge material system, nanoscale **Al provides void-free interfaces.** Moreover, **Al as source/drain material features superconducting and plasmonic applications** in SBFETs.

2.2.2 Schottky Barrier Characteristics

Achieving abrupt MSJs allows for elaborating the electronic properties regarding the Schottky barrier (SB) characteristics. In general, a SB is evident if the Schottky barrier height (SBH) $\phi_B > k_B T$. Importantly, having such non-ohmic, rectifying contacts allows the realization of SBFETs and their diversified functions in the scope of "Beyond CMOS". [23,50] Moreover, SB-based devices have proven their excellent suitability for high-frequency and microwave devices because of majority carrier transport without the necessity of depleting a space-charge region in comparison to *pn*-junction based devices. [17]

In the following, theory from "Semiconductor Devices: Physics and Technology" by S.M. Sze [17] and "Metal-Semiconductor Contacts" [176] by E. Rhoderick is used unless otherwise stated. Note that in these references doped semiconductors and a one-sided MSJ, i.e., the potential of the semiconductor is controlled by an additional ohmic junction, are considered.
A SB generally assembles when a metal and semiconductor are brought into contact. Thus, a dedicated potential barrier is evident. Naturally, applying a bias voltage, the SB can be operated in forward direction, influencing the effective SBH, as discussed later. Similar to *pn*-junctions, a space-charge region forms at the MSJ. In terms of describing the basic properties of an ideal SB, the following considerations need to be taken into account:

- The metal and semiconductor are in intimate contact without the presence of another material layer and impurities at the MSJ.
- At the MSJ, no inter-diffusion of the metal and semiconductor occurs.
- The space-charge region is confined to a depletion zone with width W_D.

In this respect, the width of the depletion zone W_D is given according to Equation (2.3).

$$W_D = \sqrt{\frac{2\varepsilon_0\varepsilon_s}{qN_D}(V_{bi} - V)}, \tag{2.3}$$

where ε_s is the permittivity of the semiconductor, N_D is the donor concentration (for a *n*-type semiconductor), V_{bi} is the built-in voltage and V is the applied bias. Analyzing Equation (2.3) allows to conclude that W_D is reduced with increasing the doping concentration. Further, this leads to the fact that the Fermi level is moving closer to the conduction band, and a stronger band bending towards the MSJ occurs. Further, the depletion width directly influences the junction capacitance $C_j = \varepsilon_s / W_D$, which is not constant, resulting from the bias dependency of W_D. In this respect, merely C_j is defining the switching speed or reverse recovery time t_{rr} in Schottky junctions, whereas in conventional *pn*-junctions also the recombination time of majority and minority charge carriers need to be considered. [17] Therefore, SB-based devices are often denoted as "majority carrier" type devices.

Typical t_{rr} values for Schottky junctions are ~100 ps and for *pn*-junctions several microseconds to ~100 ns. Moreover, Schottky junctions exhibit lower forward voltages V_F in comparison to *pn*-junctions, which are for Si Schottky diodes typically in the range of 0.2 V to 0.4 V.

Figure 2.7 illustrates the formation of the SB for a *n*-doped semiconductor [(a,b)] and a *p*-doped semiconductor [(c,d)], respectively, whereas (a) and (c) show the relevant energies of the metal and semiconductor when not in intimate contact and thus no SB has formed yet.

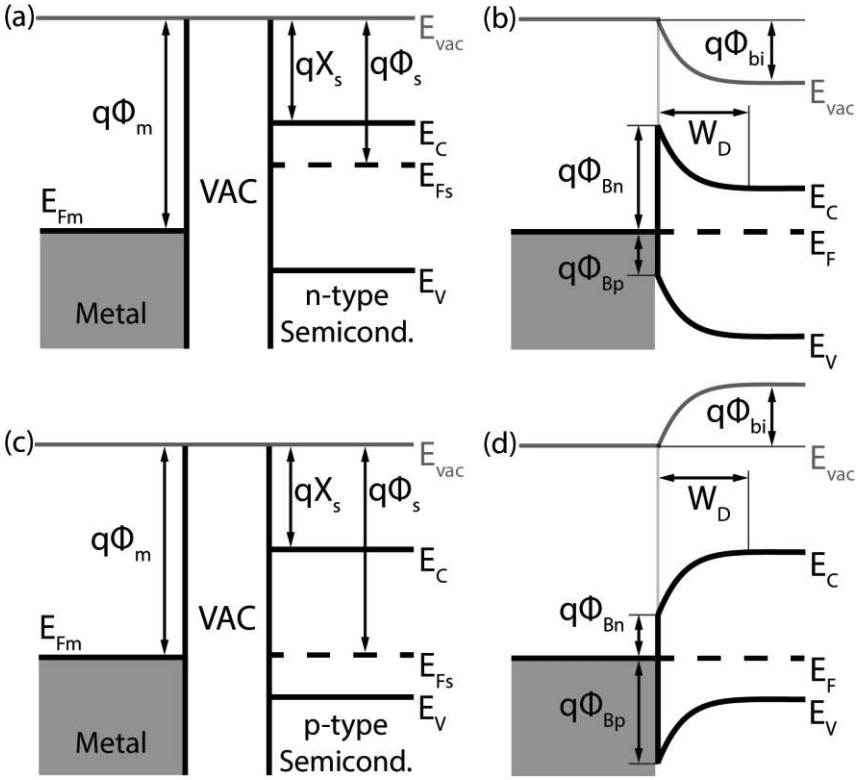


Figure 2.7: *(a) Metal and n-doped semiconductor before brought into contact with relevant energies. (b) Formation of SB when metal and semiconductor are in intimate contact, showing dedicated barriers for electrons ϕ_{Bn} and holes ϕ_{Bp}. (c) and (d) show the same configurations for a p-doped semiconductor. In (b) and (d), the thermal equilibrium is maintained, as the band edges are bent towards the MSJ.*

Finally, after bringing the metal and semiconductor in intimate contact [cf. Figure 2.7(b,d)] allows to deduce the following relations, where Equation (2.4) describes the metal work function ϕ_{m} and Equation (2.5) the electron affinity X_{s}. Note that the semiconductor work function ϕ_{s} is defined as the energy difference between the semiconductor Fermi level E_{Fs} and the vacuum energy level E_{vac}.

$$q\phi_{\mathrm{m}} = E_{\mathrm{vac}} - E_{\mathrm{Fm}}, \tag{2.4}$$

$$qX_{\mathrm{s}} = E_{\mathrm{vac}} - E_{\mathrm{C}}, \tag{2.5}$$

where E_{Fm} is the metal Fermi energy level and E_{C} is the energy level of the conduction band edge. Next, dedicated SBs for electrons ϕ_{Bn} (also denoted as n-type SB) [cf. Equation (2.6)] and holes ϕ_{Bp} (also denoted as p-type SB) [cf. Equation (2.7)] are derived.

$$q\phi_{\mathrm{Bn}} = q(\phi_{\mathrm{m}} - X_{\mathrm{s}}), \tag{2.6}$$

$$q\phi_{\mathrm{Bp}} = E_{\mathrm{g}} - q(\phi_{\mathrm{m}} - X_{\mathrm{s}}), \tag{2.7}$$

$$E_{\mathrm{g}} = q(\phi_{\mathrm{Bn}} + \phi_{\mathrm{Bp}}), \tag{2.8}$$

where E_{g} is the band gap energy consisting of the sum of the electron and hole SB [cf. Equation (2.8)].

When the metal and semiconductor are in intimate contact, the Fermi levels of the metal E_{Fm} and the semiconductor E_{Fs} level out by establishing thermal equilibrium, constituting a common Fermi level E_{F}. Thus, a charge carrier flow is guaranteed, causing band bending towards the MSJ within the depletion zone W_{D} and forming a built-in potential barrier ϕ_{bi}, which definition is given in Equation (2.9). Applying a bias voltage V with energy qV, which equals ϕ_{bi}, establishes a flat-band condition, holding $V = V_{\mathrm{FB}}$.

$$\phi_{\mathrm{bi}} = \phi_{\mathrm{m}} - \phi_{\mathrm{s}} \tag{2.9}$$

Regarding ϕ_{s}, the doping concentration plays a vital role as it directly affects the built-in potential ϕ_{bi}, leading to a higher degree of the band bending towards the MSJ.

Real Schottky barriers

So far, the formation of ideal SBs has been considered. However, in real applications, important aspects that highly influence the height and shape of the SB need to be taken into account, as the charge carrier transport in the proposed devices is mainly determined by the SB properties. One aspect to consider is the barrier lowering effect, which occurs in case the SB is no longer in equilibrium, i.e., applying a bias voltage and consequently changing the electrostatic landscape of the MSJ.

Figure 2.8 illustrates a change of the SB shape and height induced by barrier lowering effects. A possible origin is the image force lowering effect, known as the Schottky effect, indicated by the dashed curve. In this context, an electron with negative charge $-q$ at distance x from the metal surface in the semiconductor is evident, and electric field lines terminate at the metal/semiconductor interface. However, these field lines act positively with $+q$ at a distance $-x$ from the metal surface, depicting a mirror image of the electron charge (cf. inset in Figure 2.8). In correspondence to Figure 2.8, $\Delta\phi$ can be calculated according to Equation (2.10). [50]

$$\Delta\phi = \sqrt{\frac{q\mathcal{E}}{4\pi\varepsilon_s}}, \tag{2.10}$$

where $\mathcal{E}$ is the applied electric field across the MSJ.

Additionally, the barrier lowering effect causes the valence band to exhibit a shift towards E_{Fm} (not illustrated in Figure 2.8). However, due to practical reasons and the uncertainty of $\mathcal{E}$ across the MSJ, in the following illustrations, the ideal triangular-shaped SB is used. Besides the image force lowering effect, metal-induced gap states (MIGS) can also lower the SB, which follows a linear trend with $\mathcal{E}$ and can be as large as image force lowering. [177] Moreover, MIGS are identified to highly determine the Fermi level pinning as discussed thoroughly next. [78]

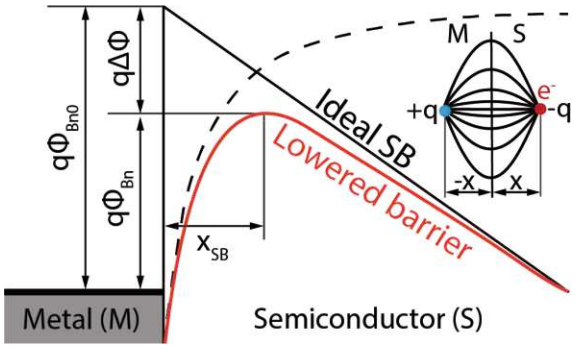


Figure 2.8: *Barrier lowering mechanisms lead to a reduction of the SBH and a shift of the SB (red solid curve), resulting in a different SB shape. In the illustration, the effect of image force barrier lowering (black dashed curve) is indicated, whereas the inset shows the proposed mechanism at the MSJ.*

Fermi level pinning at Schottky junctions

A significant and essential property of SBs is the concept of Fermi level pinning, which directly impacts the *n*- and *p*-type SBH. Considering previously stated equations, i.e., Equation (2.6) and Equation (2.7) as well as the semiconductor electron affinity X_s of *n*-doped Si and Ge, Al-Si and Al-Ge with Al having a metal work function $\phi_m = 4.20\,\text{eV}$ leads to the calculated values in Table 2.4.

Parameter	(Al-)Si	(Al-)Ge
E_g (eV)	1.12	0.66
X_s (eV)	4.05	4.00
$\boldsymbol{\phi_{Bn}}$ (eV)	**0.15**	**0.20**
$\boldsymbol{\phi_{Bp}}$ (eV)	**0.97**	**0.46**

Table 2.4: *Ideal n- and p-type SBHs of the Al-Si and Al-Ge material system derived from the work function of Al and the electron affinity of Si and Ge. Note that the corresponding semiconductor's surface electron affinity X_s is used.*

However, in real applications, the SBHs ϕ_{Bn} and ϕ_{Bp} do not match with the calculated ideal ones in Table 2.4. In this respect, Fermi level pinning comes into play, which may originate from different sources, as, e.g., inhomogeneities, i.e., MIGS, and surface states at the MSJ. [32, 178] Figure 2.9 illustrates the influence of surface states at the MSJ and its *n*- and *p*-type SBs. In general, Fermi level pinning is caused by an equilibrium condition of the free surface of a semiconductor. In contrast to a bulk semiconductor with an infinite collection of 1D potential wells, the Kronig-Penney model and Bloch's theorem cannot be used to derive the $E(k)$ relation at the surface. Instead, a model that treats the interface as a continuum of localized energy states within the band gap is applied. In order to maintain equilibrium, these states may be occupied or empty, as indicated by horizontal bars at the MSJ in Figure 2.9, where yellow bars depict occupied states below the Fermi level, leading to bending of the conduction and valence band. Moreover, the energy $q\phi_0$ determines the charge neutrality level (CNL), which describes an electrically neutral surface and builds the central aspect in explaining Fermi level pinning. [179] In dependence on the Fermi level energy and the CNL, positive or negative net charges lead to a shift of the conduction and valence band. Reconsidering the ideal SB and the absence of any surface states, $q\phi_0$ would pin according to the values stated in Table 2.4. In particular, empty surface states depict a net positive charge, whereas filled surface states exhibit a net negative charge, leading to an electric field, which causes band bending and therefore pins the Fermi level accordingly to E_{Fm}.
In the past, various approaches were proposed, allowing to tune the degree of Fermi level pinning, including dopant segregation [180, 181] at the MSJ or the introduction of an interlayer between the metal and semiconductor [182–184]. Both methodologies change the surface states and, thus, tune the Fermi level pinning.

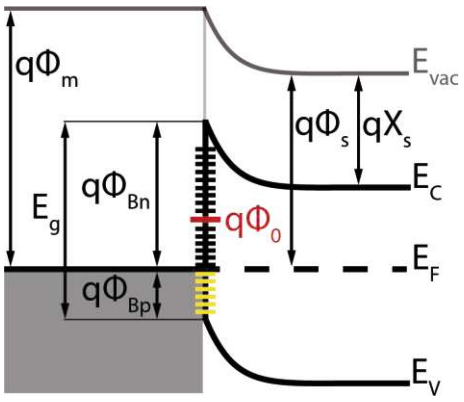


Figure 2.9: *Influence of surface states at the MSJ leading to distinct SBs for electron and hole injection. Consequently, determining Fermi level pinning that is significantly different compared to ideal MSJs. In respect to maintaining thermal equilibrium at the MSJ, the occupation of surface states may change, shifting ϕ_0 (CNL) and resulting in a difference of the n- and p-type SBHs.*

Nishimura et al. elaborated on the Fermi level pinning of the Al-Si and Al-Ge material system as illustrated in Figure 2.10(a,b), respectively. [78] In particular, they experimentally investigated the Al-Ge material system, where for the extraction of the SBH, mainly I/V characteristics were acquired. Additionally, C/V measurements were used for comparison.

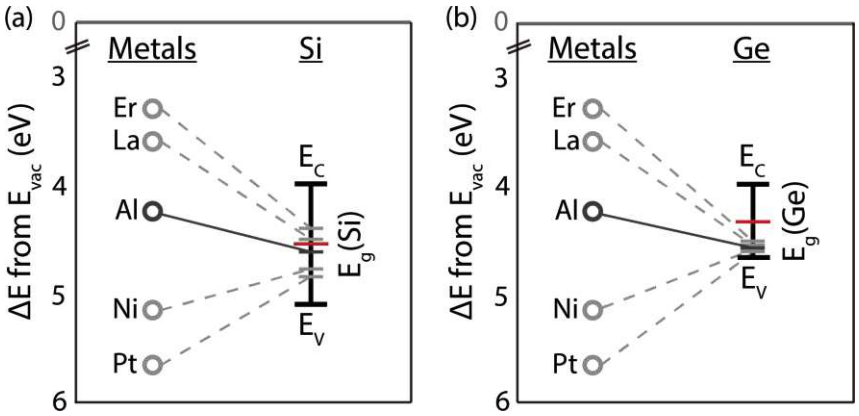


Figure 2.10: *In dependence of surface states, various selected metals pin differently to the band gap of (a) Si and (b) Ge, denoted as Fermi level pinning. Importantly, most metals pin close to the valence band of Ge, whereas in the metal-Si material system, the Fermi level pinning spreads wider. The red vertical bars indicate the middle of the band gap. Image adapted from [185].*

In the Al-Si material system, shown in Figure 2.10(a), it becomes evident that the selected metals pin differently within the band gap of Si. In 1965, Cowley and Sze published a work stating that ϕ_0 is approximately one-third of the Si band gap. [186] Thus, leading to a $\phi_{\mathrm{Bn}} = 0.75\,\mathrm{eV}$ and a $\phi_{\mathrm{Bp}} = 0.37\,\mathrm{eV}$ of an isolated Si surface, further causing a 66 %/34 % ratio between the n- and p-type SBH. Consequently, according to Figure 2.10(a), using metals with different metal work functions allows the tuning of the SBH in dependence of the used metal. Another solution for tuning the SBH is the selection of an appropriate passivation, influencing interface states. Tao et al. demonstrated ohmic SBs for Se- and Ti-passivated Si(100) and Si(001) surfaces, respectively. [187, 188] Importantly, Al, as proposed in the thesis at hand, is expected to pin relatively close to the middle of the Si band gap, promising similar SBHs for the injection of electrons and holes.
Analyzing the Al-Ge material system in Figure 2.10(b) shows that all selected metals pin close to the valence band E_{V} of Ge. In this respect, Thanailakis et al. evaluated that $\phi_0 = 0.13\,\mathrm{eV}$ above the valence band edge of Ge. [189] Moreover, Dimoulas et al. extracted similar values with $\phi_0 = 0.09\,\mathrm{eV}$, leading to $E_{\mathrm{Fs}} >> \phi_0$. [190] Therefore, causing a n- and p-type SB with a ratio of 86 %/14 %. Consequently, a high portion of negative charges at the interface is evident because of electron capturing (cf. Figure 2.9) enabled by acceptor-like states. [191] The fact of strong Fermi level pinning close to the valence band and the low ϕ_0 in Ge promotes its use in p-type transistors. [192] As all metals tend to pin close to the valence band, various solutions were proposed, mainly focusing on introducing interlayers between the metal and Ge surface. [193, 194]
For specific SBFET applications, i.e., RFETs, similar and ideally equal ϕ_{Bn} and ϕ_{Bp} are desired to ensure similar charge carrier injection mechanisms for electrons and holes, respectively.

Considering basic theory, the metal work function and semiconductor affinity define the SBH. However, **interface states lead to a shift of the CNL**. Moreover, the electrostatic landscape highly influences the shape and height of the SB. Importantly, in the **Al-Si material system, the Fermi level pins mid-gap to the band gap of Si**, whereas in the **Al-Ge material system, the Fermi level pins close to the valence band of Ge**.

2.3 Charge Carrier Transport in SBFETs

This section discusses the charge carrier transport based on the previously introduced SB properties but considers its implementation in SBFETs.
First, Section 2.3.1 elaborates on the electrostatic gating mechanism and the charge carrier transport in SBFETs. Next, Section 2.3.2 discusses the meaning and modeling of the effective SBH from a bulk (3D) and 1D-confined perspective. Finally, the transferred electron effect, allowing the realization of devices with NDR in Ge, is discussed in Section 2.3.3.

2.3.1 Schottky Barrier Field-Effect Transistors

As already mentioned, SBFETs are promising building blocks in the "Beyond CMOS" era, attributed to the unique charge carrier transport mechanisms inherently accessible by the nature of MSJs. The first SBFETs were proposed back in 1968 by Lefselter and Sze, [195] using n-doped Si and PtSi as source/drain contacts. Later, in the 1980s, SBFETs claimed to eliminate CMOS latch-up beside already proven advancements in high-speed switching. [196, 197] However, due to the exhibition of high resistance source/drain contacts caused by Schottky junctions and worse performance metrics in comparison to MOSFETs, no substantial progress towards industrial applications was driven. [50] Simulation methodologies and advanced nanoscale processing techniques set the focus back on SBFET exploration, [48] also considering carbon nanotubes (CNTs) embedded in SBFETs, [198] which are handled as a promising channel material by the International Roadmap for Devices and Systems (IRDS). [1] Lately, also SBFETs realized with 2D channel materials, as e.g., MoS_2 or WSe_2, were proposed. [199, 200]

Electrostatic gating of SBFETs

In the first step, the electrostatic gating capability of SBFETs, as illustrated in Figure 2.11, is discussed, further allowing the elaboration of the involved charge carrier transport mechanisms. As shown in Figure 2.11(a) a SBFET can be classified as two back-to-back Schottky diodes, [201] whereas one diode is operated in forward and the other in reverse direction. In this respect, the metal constitutes the anode (+), and the semiconductor the cathode (-). If the MSJs exhibit an ohmic characteristic, the channel resistance is the main factor contributing to the total resistance. Moreover, two identical SBs with the same electronic properties are desired, which is supported by the heterostructure formation process used in the work at hand (cf. Section 2.2). Generally, for visualization of the electrostatic landscape of SBFETs, band diagrams are used as depicted in Figure 2.11(b-d). In the used illustrations a top gate (TG) covering the MSJs and the semiconductor channel is considered. Note that simplified band diagrams are shown for better understanding (cf. Section 2.2.2). Additionally, mid-gap Fermi level pinning is considered here. First, applying a positive bias, i.e., $V_D > 0\,V$, leads to a downwards shift of the drain potential [cf. Figure 2.11(c)], resulting in a change in the slope of the conduction and valence band.

Attributed to the exhibition of a wide SB, no efficient charge carrier injection occurs, and charge carriers can merely be injected by overcoming the barrier if their energy $E > \phi_{\mathrm{Bn}}$ (cf. Figure 2.8 and Figure 2.9). [51] Next, applying a positive gate voltage, i.e., $V_{\mathrm{TG}} > 0\,\mathrm{V}$ [cf. Figure 2.11(d)], the conduction and valence bands (E_{C} and E_{V}) are being bent downwards, allowing sufficient injection of charge carriers (here: electrons), whereas the injection of holes is blocked caused by an extension of the SB width and height. Therefore, the SBFET is operated as a *n*-type transistor. Concerning the electrostatically induced band bending and charge carrier injection mechanism, simulations were conducted, supporting the stated facts. [202, 203]

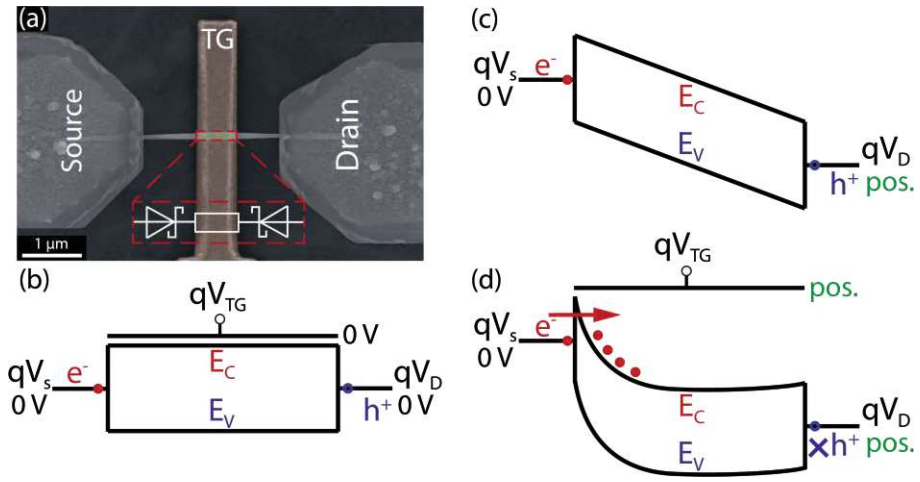


Figure 2.11: *(a) False color SEM image of a top gated SBFET. The inset illustrates the involved Schottky diodes and the channel resistance, which is indicated by a resistor. (b) Simplified illustration in case of* 0 V *bias. (c) Applying a positive bias at the drain electrode ($V_{\mathrm{D}} > 0\,\mathrm{V}$) leads to a shift of the drain potential. (d) Additionally, applying a bias to the TG electrode ($V_{\mathrm{TG}} > 0\,\mathrm{V}$) allows to bend the conduction and valence band, enabling the injection of charge carriers (here: electrons).*

Considering a metal TG, the metal work function ϕ_{m} needs to be set into relation to the semiconductor work function ϕ_{s}, as it highly determines the threshold voltages $V_{\mathrm{th}}^{\mathrm{n/p}}$. [204] In this context, the mismatch of the metal and semiconductor work functions causes an energy difference, consequently affecting the threshold voltage. Thus, in the ideal case, $\phi_{\mathrm{m}} = \phi_{\mathrm{s}}$ holds. Table 2.5 shows the work functions of various metals as well as the semiconductor work functions of un-doped (intrinsic) Si and Ge.

	i-Si	i-Ge	Al	Ti	Au	Cu	Ni
X_s (eV)	4.05	4.00	-	-	-	-	-
$\phi_{s/m}$ (eV)	4.61	4.33	4.16 ±0.11	4.33	4.50 ±0.24	4.82 ±0.29	5.20 ±0.16

Table 2.5: *Electron affinity X_s of un-doped (intrinsic) Si and Ge, and its thereof obtained work function $\phi_s = X_s - E_g/2$. The work function ϕ_m of potential gate metals is also listed. Values are taken from [86].*

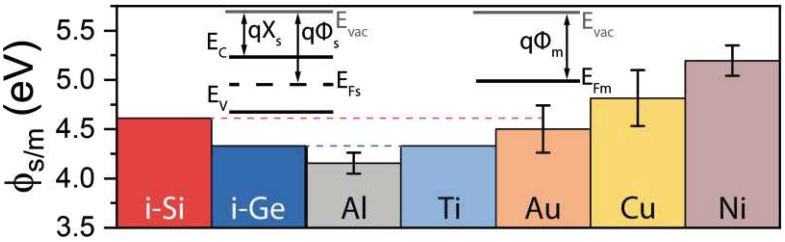


Figure 2.12: *Visual representation of the work function of intrinsic Si and Ge, and potential gate metals, listed in Table 2.5. The red and blue dotted lines show where ϕ_s of Si and Ge fits ϕ_m of the selected metals. The left and right insets depict the relevant energies for a semiconductor and metal, respectively.*

Notably, for intrinsic Si, the work function ϕ_m of Au fits well, whereas for Ge, the work function of Ti exhibits a matching work function with 4.33 eV. Nevertheless, it must be considered that due to fabrication constraints, Ni as gate material was used in previous works to remain on the same material system in the case of Ni-silicide source/drain contacts. [205] In terms of gating, also a highly degenerated substrate can be used for electrostatic gating, which is then denoted as "back gate" (BG). A BG architecture also allows the electrostatic tuning of both MSJs and the semiconductor channel; however, using a BG exhibits certain drawbacks discussed in Section 3.1.

Charge carrier injection and transport

Having the general SBFET gating capabilities discussed allows to analyze the involved charge carrier injection and transport, which is fundamentally different from MOSFETs. Therefore, Figure 2.13 illustrates the involved charge carrier injection mechanisms associated with SB-based devices and with SBs in general. In the following the scenario of electron injection and transport is considered, which also applies to holes.

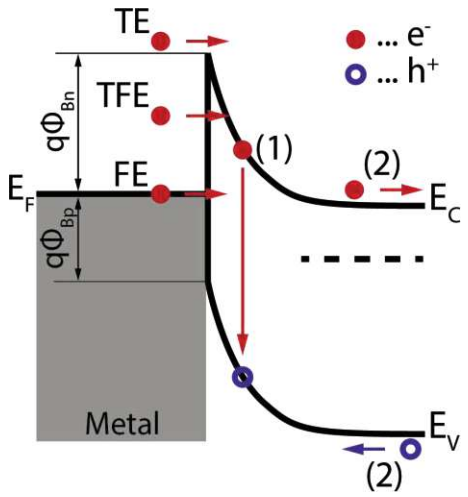


Figure 2.13: *SB-associated charge carrier injection contributions, excluding barrier lowering effects. Thermionic emission (TE), thermal-assisted field emission (TFE), and field emission (FE) may occur in conjunction. (1) Illustration of a recombination process in the depletion region. (2) Diffusion of an electron in the conduction band E_C and of a hole in the valence band E_V.*

In general, three charge carrier injection contributions can be classified. (I) Thermionic emission (TE) describes charge carrier injection over the SB. Consequently, charge carriers with potential energies higher than the SBH ϕ_B are required. Moreover, TE is a strongly T-dependent injection mechanism. (II) Field emission (FE) describes a current contribution from direct tunneling, where charge carriers originate from the Fermi level of the metal tunneling through the SB into the semiconductor's conduction or valence band. (III) Thermal-assisted field emission (TFE) constitutes charge carrier injection originating from charge carriers, which have a certain potential energy $> E_F$ and tunnel through the remaining SB. [50] Therefore, TFE is related to Fowler-Nordheim tunneling, which considers tunneling through a thin oxide layer as, e.g., evident in MOSFETs. [206] Next, TE and FE charge carrier injection mechanisms are elaborated in more detail.
The current contribution by TE is defined according to Equation (2.11), which in particular holds for bulk (3D) material systems, which derivation can be deduced from the classical Boltzmann transport equations as demonstrated by Baccarani. [207]

$$J_{TE} = A^* T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right)\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right], \tag{2.11}$$

where J_{TE} is the current density in A/m^{-2}, A^* is the (3D) effective Richardson constant in $Acm^{-2}K^{-2}$, T is the absolute temperature, q is the elementary charge, ϕ_B is the SBH, V is the applied bias and k_B is the Boltzmann constant. In general, J_{TE} consists of the sum of the TE-induced current flow from the metal to the semiconductor and vice-versa. [17]

Further, Equation (2.12) shows the involved parameters of the effective Richardson constant A^*.

$$A^* = \frac{4\pi q m^* k_B^2}{h^3}, \tag{2.12}$$

where h is Planck's constant. Note that the effective mass m^* plays an important role in Equation (2.12) and directly impacts the TE current contribution, which also needs to be considered in explaining FE. Importantly, in Equation (2.11), quantum reflections, optical-phonon scattering, and barrier lowering effects (cf. Figure 2.8) are neglected and therefore merely give an approximation of J_{TE}. The most important aspect of describing TE is its high-temperature dependence, which contributes quadratically according to Equation (2.11). Moreover, experimentally evaluating J_{TE} [cf. Equation (2.11)] allows the extraction of a parameter that corresponds to the SBH and is discussed in detail in Section 2.3.2. Additionally, in dependence of charge carrier confinement – 3D, 2D, or 1D – TE equations and associated solutions of Poisson's equations may vary because of considerations of accessible bands. [208]

Next, FE is discussed, which describes charge carrier injection by direct tunneling. FE is dominated by the transmission coefficient $T(E)$ shown in Equation (2.13) and derived under the consideration of the Wentzel-Kramers-Brillouin (WKB) approximation without considering quantum reflections and taking a triangle-shaped potential [$V(x) = q\phi_B - q\mathcal{E}x$] for simplicity into account. [50] Moreover, only a slowly-varying potential is considered as a boundary condition. [17]

$$T(E) = \exp\left[\frac{-4\sqrt{2m_T^*}}{3\hbar q\mathcal{E}}(q\phi_B - E)^{3/2}\right], \tag{2.13}$$

where E is the energy of the charge carrier, $\hbar$ is the reduced Planck's constant and m_T^* is the tunneling effective mass. Observing the transmission coefficient $T(E)$ allows to deduce that from a materials perspective, the tunneling effective mass m_T^* and the SBH ϕ_B are determining the transmission coefficient. Setting $T(E)$ in relation to TE allows to set $T(E) = 1$ for charge carriers overcoming the barrier. Further, the potential energy of charge carriers holds $E_{TE} >> E_{FE}$ (cf. Figure 2.13). Therefore, a change of the effective mass is expected, leading to a tunneling effective mass m_T^*, [207, 209] which also becomes evident in the SBFET characteristics investigated in Section 4.2. Further, Baldauf et al. showed that mechanical stress can be implemented to tune the tunneling probability. [210] Finally, the FE tunneling current density J_{FE} can be expressed according to Equation (2.14). [178]

$$J_{FE} = q\frac{4\pi m_T^*}{h^3}\int_0^\infty dE[F_m(E) - F_s(E)]\int_0^E T(E)dE_x, \tag{2.14}$$

where $F_m(E)$ and $F_s(E)$ are the Fermi-Dirac distributions in the metal and semiconductor, respectively. Remarkably, in comparison to TE [cf. Equation (2.11)], FE does not depend on the absolute temperature T.

In terms of TFE, charge carriers exhibit energies, which hold $E_F < E_{TFE} < \phi_B$ and consequently can tunnel through the remaining thinned SB. Further, TFE is explicitly evident at relatively high temperatures and electric fields, as charge carriers are thermally excited, and high electric fields lead to a thinning of the SB. Attributed to the TFE injection mechanism, the process relates to Fowler-Nordheim tunneling. [206] Considering low absolute temperatures, the charge carrier injection mechanism is dominated by FE, as charge carriers do not have sufficient potential energy, i.e., are not thermally excited.

Considerably, only the total current, constituting TE, FE, and TFE, can be analyzed by experimental means. Therefore, a dedicated classification of TE, FE, and TFE can be merely didactically interpreted, whereas technology computer-aided design (TCAD) simulations allow the modeling and analysis of each contribution separately. [211, 212] Consequently, no exact values for the n- and p-type SBHs can be evaluated as merely one charge carrier injection mechanism (TE or FE) would need to be isolated. Consequently, the experimentally extracted SBH is denoted as "effective" SBH (eSBH), depicting a metric of the energy required to inject charge carriers independently of the injection mechanism. Therefore, this energy is also denoted as activation energy E_a, as discussed in Section 2.3.2. Notably, the applied drain/source and gate bias, as well as absolute temperature, must be considered, as they highly influence the degree of TE, FE, and TFE charge carrier injection in SBFETs.

State-of-the-art $NiSi_2$-Si based SBFET

Finally, Figure 2.14 shows results of a state-of-the-art $NiSi_2$-Si based SBFET, proposed by Weber and Schwarz et al. [50] Figure 2.14(a) illustrates a transfer characteristic (I_d vs. V_g), which ambipolarity can be attributed to the exhibition of similar n- and p-type SBs evident for $NiSi_2$-Si MSJs. Interestingly, a shift of the transfer characteristics to more negative V_g values is observable for decreasing V_d, which is caused by the fact that the source voltage V_s is kept at a fixed potential, leading to a change of the injection capabilities in dependence of V_d (cf. Figure A.5). In general, the transfer characteristic shift can be reduced by symmetric biasing of SBFETs or even eliminated by applying simultaneously positive (n-type operation) or negative (p-type operation) biases, i.e., V_d and V_g. Moreover, Figure 2.14(b) shows simulations, which are used to analyze the different injection contributions, whereas also a change of the subthreshold slope becomes evident. Thus, a change of the effective mass m^* is assumed, which can be attributed to Equation (2.13). Finally, Figure 2.14(c,d) show the underlying band diagrams for electron and hole injection, respectively.

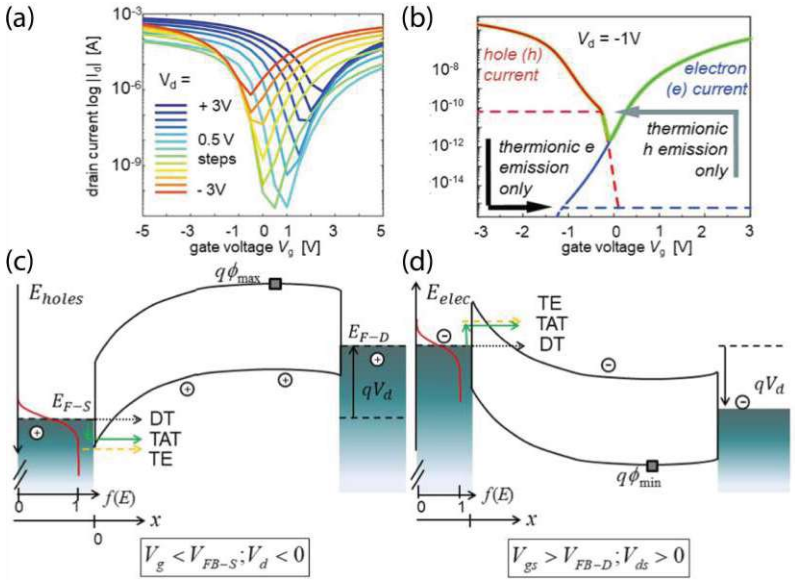


Figure 2.14: *State-of-the-art $NiSi_2$-Si NW-based SBFET as proposed by Weber and Schwarz et al. [50] (a) Transfer characteristics (I_d vs. V_g) of the SBFET at different bias voltages V_d. (b) Transport simulations reveal the onset of TE in dependence on the gate voltage V_g. (c,d) Band diagrams illustrating n- and p-type operation of the SBFET. Additionally, the distinct charge carrier injection mechanisms are indicated.*

SBFETs assemble from two MSJs, featuring two back-to-back Schottky diodes. Using a **gate electrode allows to electrostatically bend the conduction and valence band down- or upwards, favoring the injection of electrons or holes**. Charge carrier injection from the metal into the semiconductor can be **classified by TE, FE, and TFE**, whereas **TE and TFE are highly determined by the absolute temperature** and **FE is a temperature independent** process.

2.3.2 Modeling of an Activation Energy

For many nanoelectronic applications, the "effective SBH" for the injection of electrons and holes is essential as it physically describes the required minimum energy to inject a significant contribution of charge carriers into the semiconductor. Notably, the "effective SBH" dominantly depends on the Fermi level pinning (cf. Section 2.2.1), the applied bias (source/drain and gate voltage), and the absolute temperature T. Concerning the applied bias, the electrostatic landscape changes, whereas bending of the conduction and valence bands can lead to a thinned SB, increasing field emission (FE). Further, the absolute temperature determines the degree of thermal excitation of charge carriers overcoming the natural SB. Thus, increased temperatures lead to a higher thermionic emission (TE) contribution. Equation (2.11), describing the TE current, is commonly used to derive the "effective SBH" as it allows to isolate and extract ϕ_{B}. [RB1] However, experimentally measuring the current I_{D} through the SBFET does not allow to distinguish between the distinct injection contributions, i.e., TE and FE. Nevertheless, using Equation (2.15) promotes the extraction of an activation energy E_{a}, which considers the total energy required to inject charge carriers into the semiconductor channel, also considering FE. Thus, the term "activation energy E_{a}" is used from now on.

$$J_{\mathrm{D}} = A^{*}T^{2}\exp\left(-\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}T}\right)\left[\exp\left(\frac{qV_{\mathrm{DS}}}{k_{\mathrm{B}}T}\right)-1\right], \tag{2.15}$$

where $J_{\mathrm{D}} = I_{\mathrm{D}}/A$ with A being the NW cross-section area, is the measured current density through the SBFET, E_{a} is the previously defined activation energy and V_{DS} is the applied source/drain bias. In terms of applying Equation (2.15), certain considerations need to be taken into account. First, the stated equation is only valid for injecting charge carriers from a 3D metal into a (3D) bulk semiconductor, assuming a 3D band structure of the underlying semiconductor. Moreover, it merely depicts an approximation of J_{TE} because image force lowering and quantum reflection effects are neglected (cf. Section 2.2.2). Further, only the bias voltage V_{DS} is considered, whereas, in SBFETs, the gate voltage highly influences the charge carrier injection and transport. [51] In this context, gating also affects the charge carrier concentration in the semiconductor, tuning the Fermi level, the SBH, and, in consequence, the resistivity of the channel. [17] Using the 3D TE approach, different material systems were investigated in the past, even demonstrating negative activation energies in metal-Si junctions. [187,188] Moreover, Nishimura et al. also include results obtained by this so-called "3D TE" based methodology in their work exploring Fermi level pinning. [78]

Landauer-Büttiker theory

Attributed to the use of NWs in this thesis's scope, other E_a extraction methodologies shall be investigated, considering the 1D nature of NWs. As discussed in Section 2.1.3, the exciton Bohr radius a_B^* determines if a system exhibits a 1D DOS. [140] In this respect, the investigated Ge NWs have diameters d_{NW}, which are in the order of a_B^* (Ge: 24.3 nm), and therefore require an adapted methodology for the extraction of E_a. Although a 1D variant of Equation (2.15) exists, [213] which, however, does not consider the gate voltage explicitly, another methodology was exploited in cooperation with Dr. Aníbal Pacheco-Sanchez at Universitat Autònoma de Barcelona. In this respect, the 1D Landauer-Büttiker (LB) theory proved to be a sophisticated model for the extraction of an activation energy E_a, [214] which was already applied on SB-based CNT transistors and other NW FETs. [215,216] Generally, the 1D LB model considers quasi-ballistic conduction restricted to the first sub-bands. However, NWs with channel lengths longer than the mean free path are used (cf. Section 2.1.3); the 1D LB model considers 1D confinement and thus may promise a more accurate extraction of an activation energy. Considering Boltzmann statistics, the drain current I_D originating from TE in SBFETs can be defined according to Equation (2.16). [213, 217]

$$I_D \approx \frac{4q^2}{h}\frac{1}{V_t}\left\{\exp\left[\frac{n_g}{V_t}\left(V_G - V_{FB}\right) - \frac{E_a}{V_t} + \frac{n_d}{V_t}V_D\right]\right\}, \tag{2.16}$$

where $V_t = k_B T/q$ is the thermal voltage, n_g and n_d are gate and drain slope coefficients, respectively, V_{FB} is the flat-band voltage and E_a is an effective energy potential barrier over which pure TE is expected corresponding to the activation energy described above. In this context, the coefficients n_g and n_d are derived from an analytical model of Poisson's equation $\left(\Delta\Phi(\mathbf{r}) = -\frac{\rho(\mathbf{r})}{\varepsilon}\right)$. Further, depicting a relation to the electrostatic potential, which can be described by an equivalent circuit consisting of coupling capacitances between the contacts and the NW channel. In this respect, quantum capacitance must also be considered due to the 1D confined system. The electrostatic potential at a dedicated current control point ψ_{cc} at the channel is defined, [213] which considers V_S, V_D and V_G in combination to the slope coefficients. Material and technology parameters are also taken into account, such as the work function difference between the gate and channel, as well as fixed charges in the gate oxide and the device architecture. [217] Equations (2.17) show the thereof obtained derivation of the coupling coefficients n_g and n_d. Note that the slope coefficient n_s is derived in the same manner but is considered in this work within n_d, as V_{DS} is used.

$$n_g = \frac{d\psi_{cc}}{dV_G},\ n_d = \frac{d\psi_{cc}}{dV_D} \tag{2.17}$$

Note that n_g and n_d are approaching a value of "1" in case of excellent gating capabilities, i.e., evident for GAA architectures. Consequently, allowing to state $\psi_{cc} = n_g V_G$. In general, both V_G and V_D dependencies are considered explicitly in I_D by the LB model in contrast to the classical (3D) TE model, which neglects V_G in the derivation of E_a.

Moreover, the 1D LB model considers the absolute temperature linearly, whereas the temperature contributes quadratically in the classical 3D TE model [cf. Equation (2.15) vs. Equation (2.16)]. [213]

The experimental procedure to obtain E_a is explained thoroughly in Section 3.2.3. Note that the 1D LB model was only applied to Al-Ge based NW SBFETs because d_{NW} of the Ge NWs is in the order of a_B^* in Ge. Therefore, the discussion and extraction methodology of E_a regarding the 1D LB model is discussed only for Al-Ge NW-based SBFETs in Section 4.2.3.

Using TE models allows to experimentally **extract an activation energy E_a**, corresponding to an "effective SBH". Here, E_a is **defined as the minimum required energy to inject a high contribution of charge carriers into the semiconductor.** If **d_{NW} is approaching a_B^* the 1D LB model is used**, considering 1D confined MSJs.

2.3.3 Transferred Electron Effect in Ge

As already mentioned in Section 2.1.2, Ge exhibits a multi-valley conduction band landscape, allowing to initiate a transfer of electrons from the L- ($k = \langle 111 \rangle$) to the X-valley ($k = \langle 100 \rangle$), which is achieved by applying a sufficiently high electric field. This further results in negative differential resistance (NDR) in Ge-based devices, which can be used in SBFETs to realize logic circuits. [218, 219]
The so-called transferred electron effect or Gunn effect was first observed by J.B. Gunn in 1963 on GaAs and InP structures emitting microwave oscillations by applying a sufficiently high DC electric field. [220] In consequence, such devices were used in oscillator and power amplifier applications in the 1 GHz to 150 GHz range. [17] Importantly, the transferred electron effect can be initiated in any multi-valley band structure. However, electron transfer from a high-mobility valley to a low-mobility valley is required to observe NDR. In this respect, NDR was demonstrated on highly strained Si NWs, [221] n-type InSb structures [222] and diamond devices [223]. In the last few years, devices with NDR have been considered for multi-valued logic (MVL), [224–226] which promises for arithmetic operation schemes with radices or bases higher than two, enhancing "Beyond CMOS" paradigms. [227] In this respect, operating two NDR devices in series allows the realization of staircases with holding states. [81] Despite being a simple circuit, innovative logic elements, such as monostable-bistable logic elements (MOBILE), are proposed, which allow the implementation of reconfigurable NAND and NOR gates combined in a single logic cell. [82, 219] Moreover, stacking more than two devices with NDR demonstrated an efficient signed-digit MVL adder with improved circuit propagation delay and smaller area compared to its CMOS-based implementation. [218] However, most NDR devices are realized on group III-V resonant tunneling diodes (RTDs), coming with difficulties in CMOS integration. [228] Nevertheless, CMOS backend compatible solutions were demonstrated on metal/Nb-oxide/metal structures but showed high device-to-device variability concerning a current controlled NDR. [229]
In Ge, the observation of NDR can be described by analyzing the band structure illustrated in Figure 2.15(a). Here, the conduction band edge E_C (L-valley) is only 0.19 eV below the minimum of the second conduction band (X-valley). Thus, fulfilling important requirements for the exhibition of the transferred electron effect: [17]

- The energy difference ΔE needs to hold $\Delta E > k_B T$, ensuring that most electrons are in the L-valley (conduction band minimum). With $\Delta E = 0.19\,\text{eV}$ this condition is conveniently fulfilled up to an absolute temperature of 400 K ($k_B \cdot 400\,\text{K} = 0.034\,\text{eV}$).
- The energy difference ΔE needs to hold $\Delta E < E_g$, preventing avalanche breakdown before the transferred electron effect takes place. This requirement is also conveniently fulfilled up to temperatures of 400 K with $0.19\,\text{eV} < 0.62\,\text{eV}[E_g(\text{Ge})_{400\,\text{K}}$; cf. Equation (2.20)].
- Electrons in the L-valley have a lower effective mass m_L^* and higher mobility μ_L compared to the X-valley, with a higher effective mass m_X^* and lower mobility μ_X.

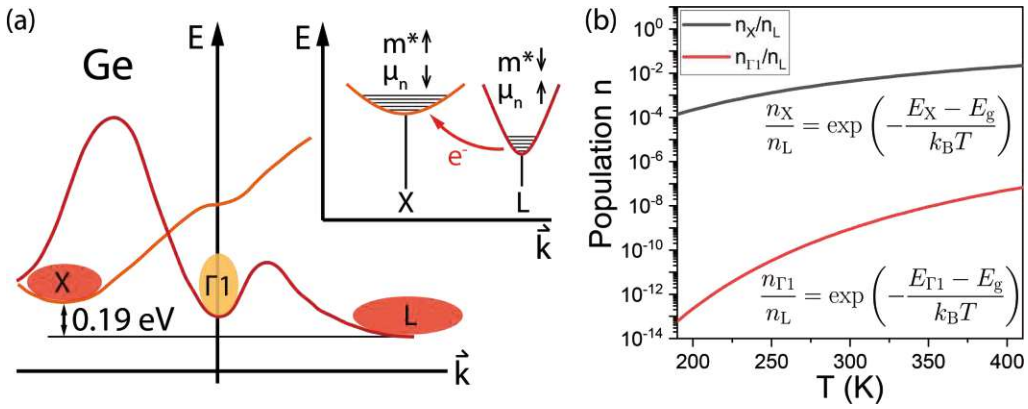


Figure 2.15: *(a) Band structure of Ge and associated valleys responsible for the transferred electron effect. Applying a sufficiently high electric field $\mathcal{E}_{\text{crit}}$ allows the transfer of electrons from the high-mobility L- to the low-mobility X-valley. (b) T-dependent charge carrier population ratios of the X- and Γ1-valley in relation to the L-valley. Increasing the temperature leads to a higher population of electrons in both valleys.*

Consequently, applying a sufficiently high electric field $\mathcal{E}_{\text{crit}}$ initiates the transferred electron effect. [69] In this respect, the band structure curvature is of relevance because it directly determines the effective mass m^* and charge carrier mobility μ [cf. Equation (2.1)]. Explaining the exhibition of NDR requires to set these parameters in relation to the current I, which is derived in the following. Equation (2.18) and Equation (2.19) give the definitions for the charge carrier velocity and further result in an expression of I. [17, 230] The starting point can be obtained by Newton's 2$^{\text{nd}}$ law:

$$a = \frac{F}{m^*}, \tag{2.18}$$

where a is the acceleration between collisions and $F = -q\mathcal{E}$ is the electric force exerted by an electric field. Further, the velocity v can be expressed by considering the mean collision time τ_{c}, defined as the time between collisions:

$$v = a\tau_{\text{c}} = -\frac{q\tau_{\text{c}}}{m^*}\mathcal{E} = \mu_{\text{n}}\mathcal{E} \propto I \tag{2.19}$$

Finally, I can be set in relation to the effective mass m^* and the mobility μ. Consequently, the transferred electron effect in Ge can be described as follows: Hot electrons are accelerated by a sufficiently high electric field $\mathcal{E}_{\text{crit}}$ and get scattered from the energetically favorable conduction band L-valley (indirect band gap), characterized by a low effective mass to the heavy effective mass X-valley. [69] Although the Γ1-valley ($k = \langle 000 \rangle$; direct band gap) is energetically closer to the L-valley, the coupling constant between the L- and X-valley is 4.05×10^8 eV/cm, whereas a lower value of 2×10^8 eV/cm is evident for scattering from the L- to the Γ1-valley. [230, 231]

Thus, a more efficient electron transfer from the L- to the X-valley is expected. The respective effective mass in the relevant regions are $m_{\mathrm{L}}^{*} = 0.082m_0$ and $m_{\mathrm{X}}^{*} = 0.288m_0$. [231] In general, the manifestation of the transferred electron effect is increasing correspondingly to a low occupation of the second conduction band (X-valley). In this context, low absolute temperatures and un-doped semiconductors (here: Ge) lead to a more pronounced NDR effect. Distinct NDR is further promoted by analyzing the charge carrier population in the X- and Γ1-valley in relation to the L-valley. Therefore, the temperature dependency of the indirect band gap energy E_{g} (L-valley) and the direct band gap energy $E_{\Gamma 1}$ (Γ1-valley) are considered [cf. Equations (2.20,2.21]. [107,232] Using Boltzmann statistics in the form of $\mathrm{e}^{-\mathrm{E}/(\mathrm{k_B T})}$ with E_{g} (L-valley) being the reference energy, allows determining the charge carrier population in the corresponding valleys as shown in Figure 2.15(b).

$$E_{\mathrm{g}} = 0.742 - 4.8 \cdot 10^{-4} T^2/(T + 235)(\mathrm{eV}), \tag{2.20}$$

$$E_{\Gamma 1} = 0.89 - 5.82 \cdot 10^{-4} T^2/(T + 296)(\mathrm{eV}), \tag{2.21}$$

where the absolute temperature T is in K. It can be deduced that increasing the absolute temperature means both valleys, the X- and Γ1-valley, are getting thermally populated. Therefore, a superposition of thermally excited charge carriers and electrons transferred by the Gunn effect is expected, leading to a less pronounced NDR effect. Additionally, an efficiency degradation of the transferred electron effect occurs due to an initially higher population in the X-valley. In general, it must be considered that changes in the Ge band structure induced, e.g., by mechanical stress or low-dimensional confinement effects, might lead to different physical properties that potentially inhibit NDR.

NDR figures of merit

The observation of NDR in the I/V characteristic is achieved by operating the device (here: SBFET) in *n*-type operation mode, as the multi-valley nature is only evident in the conduction band, i.e., for electrons. Therefore, increasing the applied bias voltage and measuring the current results in a negative slope of the current I as illustrated in Figure 2.16(a). [233] Hence, leading to NDR, in which resistance is defined according to:

$$r_{\mathrm{diff}} = \frac{\mathrm{dV}}{(-)\mathrm{dI}}. \tag{2.22}$$

Regarding the characterization of various performance metrics, figures of merit (FOM) of NDR devices can be extracted from their I/V characteristics. In this respect, Böckle et al. investigated NDR in Al-Ge-Al NW heterostructures in dependence of the NW diameter and channel length. [74] They showed that the critical electric field $\mathcal{E}_{\mathrm{crit}}$ = 10 kV/cm to 70 kV/cm. Notably, $\mathcal{E}_{\mathrm{crit}}$ vs. NW diameter and length follows an exponential trend.

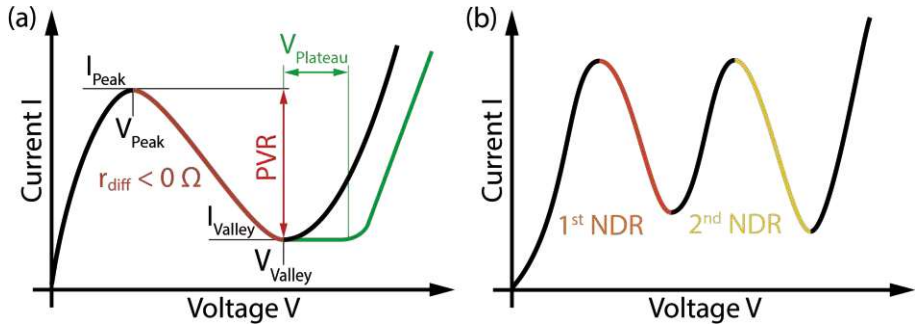


Figure 2.16: *(a) Typical NDR I/V characteristic with the indicated figures of merit (FOM). For better understanding, the green curve shows an extended* V_{Plateau}*. (b) Example of the exhibition of a "double" NDR required for distinct MVL applications.*

In this context, short channel lengths (~100 nm) require a higher $\mathcal{E}_{\mathrm{crit}}$ and devices with long channel lengths (~2 µm) already exhibit NDR at lower $\mathcal{E}_{\mathrm{crit}}$. The channel length dependency on $\mathcal{E}_{\mathrm{crit}}$ can be attributed to a reduced acceleration path in short devices, resulting in less energetic electrons. Further, it was shown that devices with channel lengths < 150 nm do not exhibit NDR anymore. Regarding group III-V semiconductors, $\mathcal{E}_{\mathrm{crit}}$ values of 3.2 kV/cm and 10.5 kV/cm were evaluated for GaAs and InP, respectively. [17]
One of the most important metrics is the peak-to-valley (current) ratio (PVR), which is defined according to Equation (2.23). The PVR is a dimensionless quantity that needs to be greater than "1" for observing NDR. A high and transiently stable PVR is generally desired for NDR device applications.

$$\mathrm{PVR} = \frac{\mathrm{I_{Peak}}}{\mathrm{I_{Valley}}} \tag{2.23}$$

Concerning already investigated Al-Ge based SBFETs, a RT PVR of ~40 was extracted, which decreases with increasing temperatures to a value of ~5 at $T = 350$ K. [74] Further, it was demonstrated that by tuning the gate voltage and operating the device in stronger electron conduction mode, the PVR could be enhanced, due to a more efficient transport of electrons. Moreover, a higher gate voltage causes a thinning of the SB and, therefore, an increased tunneling injection contribution (cf. Section 2.3.1). Another important prerequisite for applications that use NDR, i.e., MVL, is the exhibition of a "double" NDR as illustrated in Figure 2.16(b). In this respect, two dedicated and separated NDR regions are required, often realized by a combination of MOSFETs and NDR devices, e.g., RTDs. [224, 225] Lately, the exhibition of such multi-NDR I/V characteristics was demonstrated on staircase-stacked 2D materials, i.e., WSe_2/h-BN. [81, 226] Moreover, a distinct degree of tunability of the NDR region is required for the operation of logic circuits, e.g., necessary in reconfigurable NAND and NOR gates. [219]

In **Ge-based devices, NDR is accessed by the transferred electron effect**, which is inherently enabled the multi-valley conduction bands of Ge. Therefore, a sufficiently high electric field $\mathcal{E}_{\text{crit}}$ needs to be applied, allowing to scatter **electrons from the L- to the X-valley**. Thus, NDR becomes evident due to a **change of the charge carrier mobility**. A **high and temperature stable PVR, as well as a tunable NDR region, is desired** for device realization and its implementation in circuits.

2.4 Nanoelectronic Devices

In the past, essential device concepts were realized based on SBFETs, which focus on diversifying computing paradigms in the scope of "Beyond CMOS" (cf. Chapter 1). As introduced in the previous sections, Al-group IV based SBFETs have enormous potential in facilitating charge carrier injection and transport properties for the realization of emerging device concepts. In particular, enabling fine-grain reconfigurability on the transistor level, inherently accessible by the ambipolar nature of the proposed SBFETs attributed to the exhibition of distinct *n*- and *p*-type SBs and associated electron or hole transport.
In this respect, the following discusses state-of-the-art device concepts based on Al-group IV SBFETs considered in this thesis. First, Section 2.4.1 discusses RFETs and presents two different gating concepts using a multi-gate architecture. Thus enabling to switch between *n*- and *p*-type operation during run-time, combined in a single device. Next, Section 2.4.2 shows Ge-based NDR device realizations in terms of facilitating the transferred electron effect inherently provided by the multi-valley conduction band of Ge.

2.4.1 Reconfigurable Field-Effect Transistors

The following section discusses the manifold aspects that must be considered in realizing RFETs. Therefore, in the first step, the requirements for RFETs are elaborated.
In general, a RFET is a type of transistor which fulfills the following requirements, which in particular considers its use in circuits: [65]

- Fast and reversible operation as *n*- or *p*-type FET in the same device, which is enhanced using an intrinsic or low-doped semiconductor channel.
- Equal *n*/*p*-type I/V characteristics, in particular having equal threshold voltages $|V_{\mathrm{th}}|^{\mathrm{n/p}}$, subthreshold slopes $S^{\mathrm{n/p}}$ and on-currents $I_{\mathrm{on}}^{\mathrm{n/p}}$.
- Sufficient drivability strength is particularly required in circuit applications.
- Single supply voltage with low power consumption.
- Scalability, which is an important prerequisite for the use of RFETs in circuits and large-scale integration.

In this respect, SBFETs provide a promising platform, whereas RFETs depict a further diversification of SBFETs, utilizing additional gates for tuning the energy landscape (cf. Section 2.3.1). Thus, allowing to merge *n*- and *p*-type transistor functionality in a single device by facilitating the ambipolar nature of SBFETs. In this context and in relation to the stated requirements, SBFETs provide fast switching speeds inherently enabled by the "majority carrier" characteristic of SBs. Further, due to the exhibition of distinct *n*- and *p*-type SBs and appropriate tuning of the conduction and valence bands, the injection of electrons or holes can be favored (cf. Section 2.2.2), blocking the opposed charge carrier type.

In terms of equal n- and p-type I/V characteristics, the Fermi level pinning plays a crucial role as it is the dominant metric, defining the charge carrier injection capabilities (cf. Section 2.2.1). In this respect, equal ϕ_{Bn} and ϕ_{Bp}, respectively corresponding E_{a} values for n- and p-type operation are required. However, due to the exhibition of distinct SBs, ohmic source/drain contacts are generally difficult to realize and, therefore, limit the current. However, as RFETs unfold their full potential in reconfigurable logic gates, high on-currents $I_{\mathrm{on}}^{\mathrm{n/p}}$, a low I_{off}, steep subthreshold slopes $S^{\mathrm{n/p}}$ as well as equal threshold voltages $|V_{\mathrm{th}}|^{\mathrm{n/p}}$ are desired. In the case of a NW-based RFET, such functionality is achieved, e.g., by placing two top gates (TGs) atop the two MSJs and tuning the charge carrier injection capability. Thus, determining the injection of electrons (positive potential) or holes (negative potential) and consequently defining the RFET's operation as a n- or p-type transistor. Therefore, such gates are denoted as "program gates" (PGs). Further, in relation to conventional MOSFETs, a gate covering the remaining semiconductor channel allows the electrostatic tuning of the charge carrier transport through the RFET, which is therefore denoted as the "control gate" (CG). As shown later, also other RFET gating concepts were utilized in the past relying on different injection and charge carrier concentration control mechanisms. [65]

State-of-the-art RFETs

In the past, various RFET implementations were realized using intrinsic or lightly doped Si [39, 67, 234] and Ge [29, 75, 235, 236] NWs fabricated from bottom-up and top-down approaches as well as CNTs [237] and graphene [238]. Additionally, p^{+}-i-n^{+} Si NWs were successfully implemented for RFET operation. [239] Further, also promising reconfigurable transistors on base of 2D materials, i.e., $MoTe_2$, black phosphorus or ReS_2/WSe_2, connected by various metals were demonstrated. [240–242] In terms of the used source/drain metal contacts, Ni plays an important role and is broadly used for the realization of SBFETs as discussed in Section 2.1. In this respect, most of the cited Si- and Ge-based RFETs also use Ni-silicides and -germanides, respectively, whereas the referenced CNT- and graphene-solution facilitate Ti as source/drain electrodes. A discussion about the selection of the gate metal is given in Section 2.3.1, whereas, e.g., for Si-based devices Ti/Al, [67] poly-Si, [234] or Ni/Al [39] is used. Thus, showing that non-matching work functions are also used due to fabrication concerns. The Ge-based devices use Ti/Al [235] and Ti/Au [236], where Ti is defining the work function, which matches with Ge (cf. Section 2.3.1). In terms of achieving symmetric on-currents, the main objective is to have equal effective SBHs/$E_{\mathrm{a}}^{\mathrm{n/p}}$. Therefore, based on intruded source/drain $NiSi_2$ contacts in bottom-up grown intrinsic Si NWs, oxide-induced compressive stress to the Schottky junctions resulted in a mean symmetric factor $I_{\mathrm{on}}^{\mathrm{n/p}}$ of 0.98 for an identical drain and gate bias. [243, 244] Importantly, the same mechanism was applied to top-down fabricated Si NWs with an on-current symmetry factor of 1.6. [245]

As discussed in Section 2.2.1, Ge exhibits Fermi level pinning close to the valence band for most metals, including Ni-germanides and Al, [75, 235] and therefore shows a high asymmetry towards an enhanced p-type characteristic.

In the following, two state-of-the-art RFETs are presented, illustrating the underlying mechanism that enables reconfigurability between n- and p-type operation. In the review paper, "Reconfigurable Nanowire Electronics - A Review", Weber et al. published a comprehensive study of NW-based RFETs. [65] In this respect, an intrinsic $NiSi_2$-Si ($\langle 110 \rangle$ axial crystal orientation) NW-based RFET as shown in Figure 2.17(a) with the CG being atop the source-sided MSJ and the PG being at the drain-sided MSJ, is discussed. Figure 2.17(b,c) shows the underlying band bending mechanism, where a negative V_{D} as well as negative V_{PG} at the drain-sided MSJ leads to hole transmission (p-type operation) and vice-versa with positive bias to electron transmission (n-type operation). Thus, exhibiting the corresponding transfer characteristic (I_{D} vs. V_{CG}) for $V_{\mathrm{PG}} = \pm 3\,\mathrm{V}$ and $V_{\mathrm{D}} = \pm 1\,\mathrm{V}$. In this realization, the same absolute values for V_{PG} and V_{CG} were used, which is an important aspect to consider for further circuit implementations. Moreover, the advantage of low static power consumption is evident, as the off-current $I_{\mathrm{off}}^{\mathrm{n/p}}$ is in the fA-regime. Nevertheless, an asymmetry between the n- and p-type on-current $I_{\mathrm{on}}^{\mathrm{n/p}}$ of a factor ~10 is evident. In respect to the effective SBH (here: activation energy E_{a}), values of 650 meV and 470 meV were extracted for electrons and holes, respectively. [65] As mentioned, later works on the basis of the $NiSi_2$-Si material system implemented radially compressive stress to Si, achieving a symmetry close to "1". [243,245] As evident in the false-color SEM image [cf. Figure 2.17(a)], a large portion of the channel length is not covered by the metal TGs, leading to potential influences of adsorbates. Thus influencing the charge carrier transport mechanism, which can also be facilitated, e.g., in sensor applications. [246–248] In the referenced work by Weber et al. [65], they however claim that prior to TG fabrication I_{D} vs. V_{BG} characteristics were measured, which exhibited the same $I_{\mathrm{on}}^{\mathrm{n/p}}$. In this respect, simulations revealed that the highest charge carrier concentration is in the center of the NW in the case of transistor operation in the on-state. [65, 67] Using this technology, Heinzig et al. demonstrated the first reconfigurable inverter with a single supply voltage. [67]

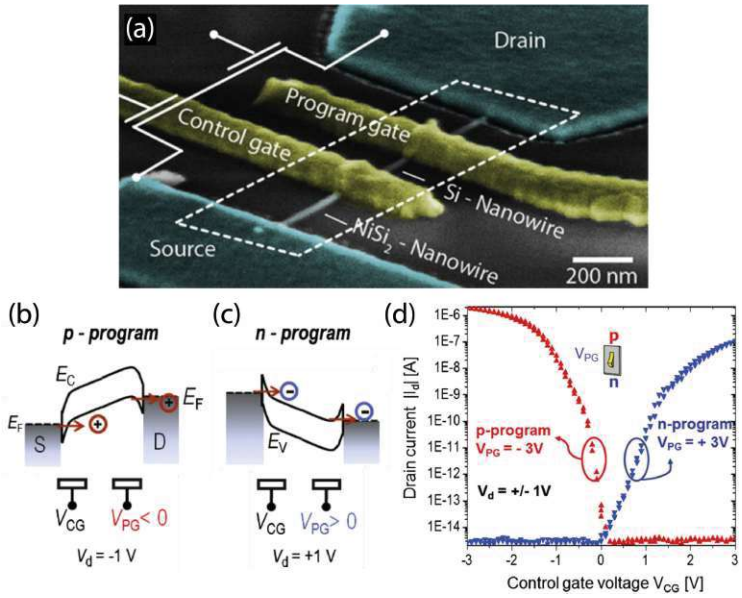


Figure 2.17: *(a) False-color SEM image of a $NiSi_2$-Si based RFET with two TGs covering the MSJs for setting the charge carrier type (PG) and tuning the charge carrier concentration in the channel (CG). Here, ⟨110⟩ intrinsic Si NWs with a SiO_2 gate oxide shell were used. (b,c) Band diagrams of the proposed RFET illustrating the functional mechanism of charge carrier filtering. (d) Typical transfer characteristic (I_D vs. V_{CG}) demonstrating n- and p-type operation in respect to V_{PG}. Images from [65].*

Concerning the gating mechanism, Figure 2.17 used selective charge carrier injection and concentration control at the contacts, which is the most common RFET gating methodology. [43] However, another RFET solution by Schwalke et al. uses the concept of polarity selection at the contacts and control of the charge carrier concentration within the channel, [65] as illustrated in Figure 2.18. [39] Moreover, they used SOI as a starting material, which is patterned to fabricate top-down, rectangular-shaped NWs. After the fabrication of the NWs, they were oxidized to form a 8 nm thick SiO_2 gate dielectric. Attributed to the use of Ni as source/drain metal and TG material [here: front gate (FG)], they also used a silicidation process to obtain NiSi-Si MSJs [cf. Figure 2.18(a)]. As it is evident in the transfer characteristic in Figure 2.18(b), a dedicated *n*- and *p*-type characteristic can be obtained, which has an I^{n}_{on}/I^{p}_{on} symmetry factor of ~2, whereas the asymmetry is attributed to a difference of the electron and hole mobility $\mu_{n/p}$. In this RFET realization, the low *p*-doped BG acts as PG, determining the injection of the charge carrier type. Using a relatively thick BG oxide (145 nm) requires a relatively high BG voltage up to 20 V. Figure 2.18(c,d) show the underlying band diagrams, leading to RFET operation. It can be deduced that the FG acts as the CG, which introduces an additional potential barrier for controlling the charge carrier flow within the channel.

Moreover, they measured the BG characteristic with floating FG and evaluated an off-current $I_{\text{off}} = 10\,\text{pA}$. In terms of circuits, the authors used the obtained RFETs and implemented them in a CMOS-based inverter, demonstrating their use in Boolean logic gates. However, different supply voltages were necessary to compensate for asymmetry. Additionally, using the proposed device concept, non-volatile memory function was demonstrated by charge carrier trapping in the BG oxide, which is achieved by a combination of Fowler-Nordheim tunneling and impact ionization, leading to a shift of the subthreshold characteristic.

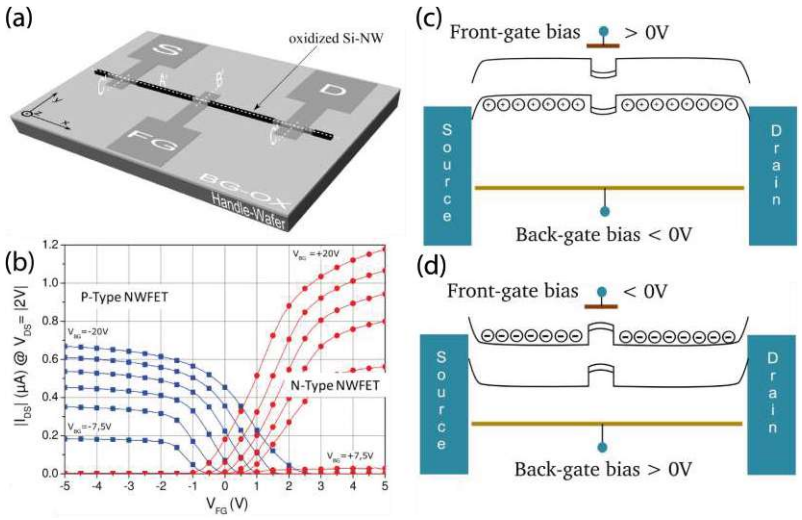


Figure 2.18: *(a) Schematic illustration of the RFET device architecture using the BG as PG and the FG as CG. Further, NiSi MSJs are utilized with an Al capping. (b) Transfer characteristic of the proposed RFET revealing an $I^{\text{n}}_{\text{on}}/I^{\text{p}}_{\text{on}}$ ratio of ~2. (c,d) Band diagrams illustrating the charge carrier filtering process for p- and n-type operation, respectively. Images from [39].*

Based on bottom-up grown and top-down fabricated NWs, Al-Ge based RFETs were proposed, [75, 236]. However, as mentioned in the introduction of this section, a high asymmetry between *n*- and *p*-type operation is evident in the Al-Ge MSJ. Nevertheless, a NDR-mode RFET on the base of Al-Ge bottom-up grown NW SBFETs was proposed, [75] which uses the inherently accessible transferred electron effect implemented in a RFET gating architecture. Combining the two functionalities provides a versatile platform for the implementation of reconfigurable electronics. Thus allowing the realization of adaptive circuits within the scope of "Beyond CMOS".

Scaling and applying RFETs

In terms of RFET scaling, simulations have been published in the past, evaluating the minimal structural sizes and dependencies, such as TG dimensionality and channel lengths. [65, 212, 249] Baldauf et al. studied the scalability of RFETs and used ring oscillator structures to evaluate the power consumption and oscillation frequency on both Si and Ge NWs. [212] Moreover, they investigated the critical overlap of the PG gate and the source/drain region, which should be as small as possible to prevent too high capacitances and decrease dynamic power consumption. In summary, a RFET operability down to a channel length of 50 nm was evaluated.
Further, concerning TCAD simulations of Si-based RFETs, sufficient reconfigurable operation with 10 nm technology (gate length and gate spacing down to 10 nm each) was shown. [249] In the scope of circuit realizations, it was evaluated that numerous approaches are possible that not only reduce the transistor count but also overcompensate the intrinsic drawback of lower on-currents in SB-based devices. [250] Therefore, although the structural sizes of RFETs exceed state-of-the-art CMOS MOSFETs, a reduced area for the same logic operation can be achieved. Moreover, RFETs enable applications arising in hardware security, [241] due to a non-distinguishable transistor design and non-existent doping. [250, 251] Concerning logic circuits, Trommer et al. created various circuits combining multiple Boolean logic cells in a single circuit, which can be reconfigured during run-time, where the additional gate allows the configuration of the cell as NAND or NOR. [252] Moreover, XOR and XNOR reconfigurable circuits have been proposed by De Marchi et al. [253] Lately, in terms of circuit integration, RFET research has made significant progress towards electronic design automation (EDA), whereas DC compact models for RFETs, [202] and SBFETs [203] were proposed.

RFETs are transistors, which allow run-time reconfiguration between *n*- and *p*-type operation in a single device, inherently **accessible by the ambipolar nature of SBFETs**. Its implementation in circuits requires **equal *n*/*p*-type I/V characteristics**, which is **dominantly defined by the effective *n*- and *p*-type SBH**. RFETs enable Boolean logic circuits with a **reduced transistor count and enable hardware secure designs**.

2.4.2 Negative Differential Resistance Devices

In Section 2.3.3, the transferred electron effect and its physical mechanism in Ge are thoroughly discussed. In this respect, the multi-valley conduction bands with a sufficiently low ΔE between the L- and X-valley and a change of the charge carrier mobility enable NDR. Moreover, the NDR I/V characteristic and its main FOM are introduced, whereas essential limitations, such as the minimum required channel length and $\mathcal{E}_{\mathrm{crit}}$ are elaborated in the scope of Ge NW-based SBFETs.
However, setting NDR in a broader context shows that most devices exhibiting NDR are realized by using quantum wells and group III-V semiconductors, [233] in which NDR is obtained by resonant tunneling effects. [233,254] Another way to exploit tunneling-induced NDR is the Esaki tunneling diode, which is based on a similar concept and reaches PVR values up to ~100. [255,256] A detailed explanation of group III-V semiconductor concepts is given in the work "Negative Differential Resistance Devices and Circuits" by Berger and Ramesh. [233]

As the work at hand focuses on the transferred electron effect in Ge, important Ge-based state-of-the-art devices with NDR are discussed. The first observations of NDR induced by the transferred electron effect in bulk Ge were made in the mid to late 1960s. [71,257] However, device realizations were achieved much later, which can be attributed to more advanced processing techniques and the capability to fabricate nanoscaled devices. In this respect, NDR was demonstrated in Ni/Ge based Schottky diodes with low PVR values in the temperature range of 100 K to 230 K. [72] Based on transistors, Kazazis et al. made an important step towards Ge-based devices that exhibit NDR in the work "Negative differential resistance in ultrathin Ge-on-insulator FETs". [70] In the latter, they exploited GeOI to realize devices with NDR. Besides the evaluation of the typical transfer (I_{D} vs. V_{GS}) and output (I_{D} vs. V_{DS}) I/V characteristics, NDR was observed at cryogenic temperatures in the temperature range of 77 K to 4.2 K. They claim that besides the confined Ge between a SiO_2 and LaYO layer [cf. Figure 2.19(c)] and thereof obtained inter-valley and inter-subband electron transfer effects, the transferred electron effect enables NDR [cf. Figure 2.19(a-c)]. Moreover, charge trapping at the Ge/LaYO and Ge/SiO_2 interface of hot electrons is considered for the exhibition of NDR. Figure 2.19(d,e) shows the thereof obtained NDR I/V characteristics at $T = 77$ K and $T = 4.2$ K, respectively. Even at a cryogenic temperature of 4.2 K, rather low PVR values ~1 are achieved.

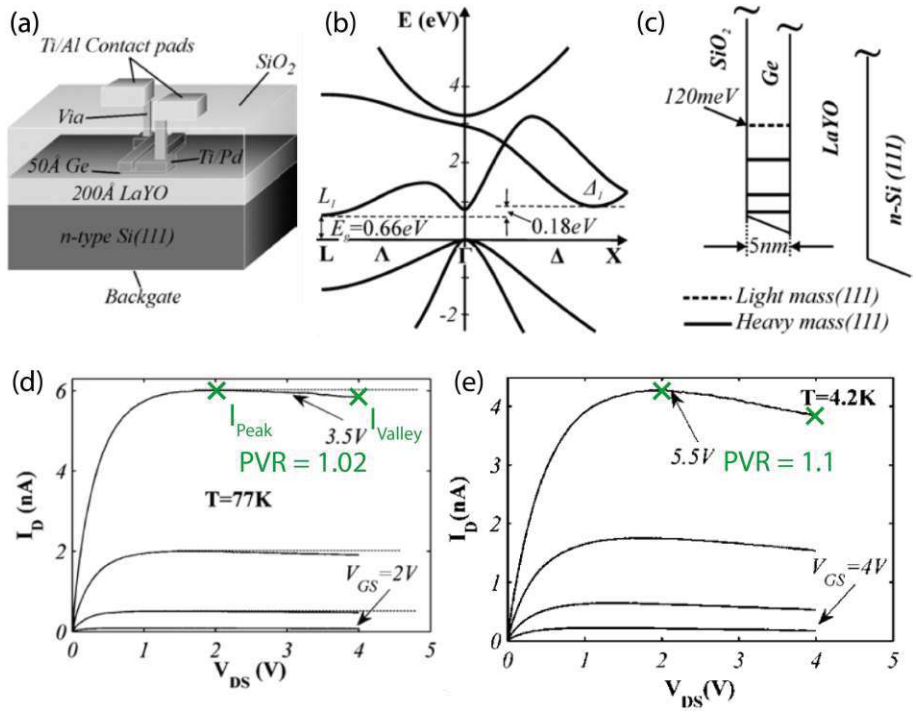


Figure 2.19: *(a) Device architecture with a* 5 nm *thick Ge layer confined by SiO_2 and LaYO. Note that the BG is used to gate and drive the device in electron conduction mode. (b) Band structure of Ge with indicated conduction valleys and energy differences. (c) Heterostructure of confined Ge between SiO_2 and LaYO, whereas the n-doped Si handle wafer is used as BG. (d,e) NDR I/V characteristics at $T = 77\,\mathrm{K}$ and $T = 4.2\,\mathrm{K}$, respectively. Additionally, $I_{\mathrm{Peak}}|_{V_{\mathrm{DS}}=2\,\mathrm{V}}$ and $I_{\mathrm{Valley}}|_{V_{\mathrm{DS}}=4\,\mathrm{V}}$ are indicated. Images from [70].*

Another concept, which is based on the proposed Al-Ge-Al NW heterostructure integrated in a SBFET architecture, was published by Brunbauer et al. in the work "Gate-Tunable Electron Transport Phenomena in Al-Ge⟨111⟩-Al Nanowire Heterostructures". [73] Importantly, depicting the first observation of NDR in Al-Ge based devices. Notably, the NDR characteristic showed remarkable results with PVR values of ~40 at RT. Moreover, they propose that the transferred electron effect in Ge is mainly responsible for the pronounced NDR. Figure 2.20 gives an insight into the used NW architecture and the obtained results.

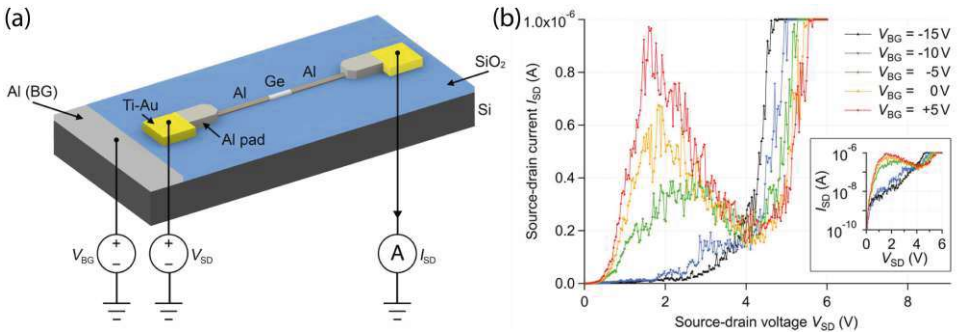


Figure 2.20: *(a) Al-Ge-Al NW heterostructure in SBFET configuration, where the BG (Si handle wafer) is used for electrostatic gating. (b) Thereof obtained NDR I/V characteristics at different BG biases V_{BG}. The PVR is enhanced by driving the device in stronger n-type operation ($V_{\mathrm{BG}} > 0\,\mathrm{V}$). Images from [73].*

As shown in Figure 2.20, using V_{BG} allows tuning the energy bands and thus leads to a more pronounced NDR characteristic with an increased PVR. Further, increasing V_{SD} allows to initiate the transferred electron effect, where I_{Peak} occurs at $V_{\mathrm{SD}} = \sim 2\,\mathrm{V}$ and $r_{\mathrm{diff}} < 0\,\Omega$ is evident in the range of $V_{\mathrm{SD}} = 2\,\mathrm{V}$ to $4\,\mathrm{V}$. Moreover, at $V_{\mathrm{SD}} = \sim 4\,\mathrm{V}$ the onset of impact ionization becomes evident, resulting in a steep increase of I_{SD}. However, using BG devices bears drawbacks regarding the exhibition of NDR. First, as most of the Ge channel is uncovered and prone to ambient conditions, adsorbates may influence the charge carrier transport and provide trap states. Thus, the PVR and NDR stability in terms of the $r_{\mathrm{diff}} < 0\,\mathrm{V}$ position might vary due to a changed electrostatic landscape of the transistor. In this respect, Pregl et al. described distinct considerations in using back gated devices. [136] Moreover, back gated devices do not allow individual gating of different devices on a single chip, as all devices on the chip are electrostatically gated simultaneously, therefore hindering the realization of circuits. Notably, Böckle et al. [74] and Sistani et al. [75] already published works, considering top gated NW-based Al-Ge-Al SBFETs, which, however, merely feature rudimental tunability of the NDR region.

Using Ge inherently enables NDR functionality, which was already demonstrated on Ni/Ge based Schottky diodes, GeOI-based transistors, and Al-Ge-Al SBFETs. However, many realizations **require cryogenic temperatures for the exhibition of NDR.** Moreover, **state-of-the-art devices do not feature distinct NDR tunability**.

Chapter 3

Experimental Techniques

This chapter discusses the experimental methodologies and gives insights into the measurement equipment and data evaluation techniques used in the scope of the thesis at hand. Section 3.1 discusses the device integration, laying out the steps towards the investigated metal-semiconductor junctions (MSJs) and Schottky barrier field-effect transistors (SBFETs). Additionally, Section 3.2 describes the electrical characterization setup and thereof evaluated parameters and characteristics, which in particular considers SBFET figures of merit (FOM) and the method of bias spectroscopy.

3.1 Device Integration

For SBFET characterization, a device design is required, reducing parasitic effects and ensuring accessibility for electrical probing. Therefore, this section starts with a description of the SBFET integration, starting from the substrate containing the as-grown NWs, and also includes considerations for scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDX) investigations. Note that the integration follows the same procedures for all investigated Al-group IV material systems. Particular differences, which mainly concern the used precursors for NW growth and the fabrication of the gate oxides are mentioned in the structural characterization results in Section 4.1.

Prior to the actual SBFET integration, NW substrates were provided, as shown exemplarily in Figure 3.1; illustrating a scanning electron microscopy (SEM) image of ⟨111⟩-oriented bottom-up grown and nominally un-doped (intrinsic) Ge NWs. Attributed to the VLS synthesis mechanism initiated by Au catalyst particles, mainly vertically arranged NWs are evident. Note that in the scope of the work at hand, only NWs are used, which are nominally un-doped, here called intrinsic semiconductor NWs.

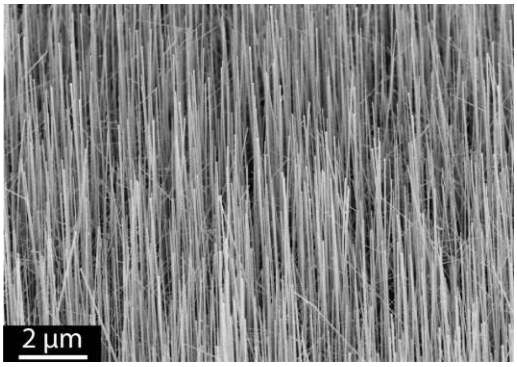


Figure 3.1: *SEM side-view of a NW substrate containing VLS-grown intrinsic and* ⟨111⟩*-oriented Ge NWs. Si and* $Si_{1-x}Ge_x$ *NW substrates were provided in the same manner. Image adapted from [258].*

In the next step, a fraction of the NW substrate is cut by cleaving, which is then further oxidized (in the case of Si NW substrates) or placed into an atomic layer deposition (ALD) system (in the case of Ge and $Si_{1-x}Ge_x$ NW substrates) for the fabrication of the conformal passivation shell. Note that the dielectric passivation finally serves as SBFET gate oxide. In this respect, Si NWs are dry oxidized at $T = 900\,°C$ within an ATV PEO601 furnace for the fabrication of SiO_2, whereas Al_2O_3 with a trimethylaluminium (TMA)-water precursor in a Cambridge or Vecco ALD chamber is deposited for Ge and $Si_{1-x}Ge_x$ NWs at $T = 200\,°C$. Details regarding the actual oxide thicknesses are given in Section 4.1, whereas basically the oxidation duration and number of ALD cycles define the oxide thickness.
In general, unpassivated Si NWs with a thin native oxide in the range of 1.5 nm to 2 nm exhibit rather large Q_f and D_{it} values. [49] Further, Berghuis et al. investigated the ALD $Al_2O_3/Ge_xO_y/Ge$ interface and extracted $Q_f \sim -1.8 \times 10^{12}$ cm^{-2}. [259] Importantly, having passivated NWs still on the substrate allows safe storage without degradation of the semiconductor core avoiding further oxidation. The Au growth catalyst at the tip of the NWs is not intentionally removed, as it is assumed that it does not have any influence, attributed to the fact that the NW is connected and intruded on both radial ends by Al, as discussed later. To deposit and further integrate the already passivated NWs, the cleaved NW substrate is placed in isopropanol, where ultrasonic agitation is applied to achieve a suspension of NWs in isopropanol. Next, the NWs are placed on a pre-patterned host chip called "hexpad" by drop-casting with a micropipette and a subsequent nitrogen flow. An illustration of such a hexpad is shown in Figure 3.2, consisting of a 500 µm thick degenerately *p*-doped Si substrate and a 100 nm thick SiO_2 layer atop. The hexagonal arranged contact pads are fabricated by optical lithography and evaporation of 100 nm to 120 nm Au acting as contact pads.

Note that the dots in-between, triangular-shaped areas, and rectangular area at the bottom are contacts to the *p*-doped Si substrate acting as back gate (BG). Therefore, BHF (6:1 volume ratio of 40 % NH_4F in water to 49 % HF in water) etching of the 100 nm thick BG oxide is performed before the Au deposition. Additionally, a microscope image with an already connected NW (here: Field 09) is shown in Figure 3.2.

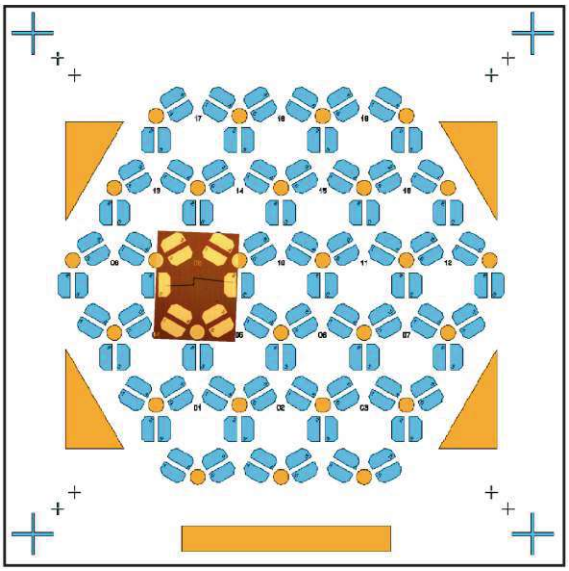


Figure 3.2: *Layout of "Hexpad" host chip, which is used to integrate the proposed SBFETs. The* 11×11cm *chip contains 19 fields with hexagonal arranged Au contact pads. The inset of a microscope image in field 09 shows an already connected NW with Al leads.*

By drop-casting the NWs on the "hexpad", they are randomly distributed, requiring SEM imaging to indicate favorable NWs for further processing and integration. After identification of single NWs with low tapering, decent diameters d_{NW} below ~50 nm as well as sufficient NW lengths > ~3 µm, the "hexpad" is transferred into an electron-beam lithography (EBL) system (eLine Raith) for the fabrication of the Al source/drain contacts and leads to the "hexpad's" Au pads. Using a positive tone poly methyl methacrylate (PMMA) resist and matching developer, the desired structures are patterned and dissolved. Next, an etch process is used before Al sputtering to remove the dielectric and native oxide at the contact areas of the NWs. Therefore, on Si NWs with a SiO_2 shell a BHF dip is sufficient, whereas the Ge and $Si_{1-x}Ge_x$ NWs require an additional HI [3 parts H_2O & 1 part HI (57 %) resulting in a 14 % HI] dip for ~6 s to remove any remaining Ge_xO_y. [258] Experimentally, a BHF (6:1) etch rate of ~1 nm/s for SiO_2 as well as Al_2O_3 was evaluated, where additional 2 s to 3 s are added, ensuring complete removal of any residual oxide.

Finally, 125 nm of Al is deposited by sputtering, building the source/drain regions of the transistor. In the last step, lift-off techniques by subsequent acetone and light ultrasonic treatment, as well as microscopy imaging, were performed to ensure the absence of short circuits due to fencing and complete removal of the resist. In this state, the Al is only in intimate contact with the semiconductor NW surface, as no solid-state reaction has occurred within the NW yet. Thus, in combination with Fermi level pinning (cf. Section 2.2.1), a high density of uncontrollable Al/(oxide)/semiconductor interface defects may exist. Therefore, as discussed in Section 2.2.1, a RTA process in forming gas atmosphere (90 % N_2 & 10 % H_2) is performed to initiate the solid-state exchange reaction between Al and the group IV semiconductor, where 673 K and 773 K is used for the Al-Ge and Al-Si as well as Al-$Si_{1-x}Ge_x$, respectively. Consequently, L_{SC}~1 µm is targeted by the intrusion of Al into the NW. Importantly, consecutive annealing cycles can be performed due to the non-existent inter-metallic phases of the proposed Al-group IV material systems (cf. Section 2.2.1). Further details regarding the annealing rates and crystal orientations of the integrated NWs are discussed in Section 4.1.
Figure 3.3(a,b) shows the thereof obtained heterostructure after RTA, forming two MSJs within the NW. Further, Figure 3.3(b) depicts a 3D illustration of one MSJ and the passivation coating of the NW. As the passivation layer is fabricated before the NW deposition onto the "hexpad", the dielectric is in direct contact with the BG oxide. Consequently, applying a bias to the BG enables electrostatic gating tunability. However, attributed to the high surface-to-volume ratio and the thereof exposed, but passivated, semiconductor, this gating architecture exhibits considerable drawbacks, such as influences of adsorbates (cf. Section 2.1.3) or body charging effects. [260, 261]

For better electrostatic gating capabilities and precise tuning of the energy landscape, top gated SBFETs are used as depicted in Figure 3.3(c,d). Therefore, in the first step, the semiconductor channel L_{SC} (after RTA) is determined by SEM inspection by conductivity and material contrast, and the top gates (TGs) are connected to the "hexpad" layout connecting an unused Au pad (cf. Figure 3.2). EBL is used for patterning using the same resist and techniques as discussed previously. After releasing the reacted resist, 10 nm Ti and 100 nm Au is evaporated, whereas the Ti acts as an adhesion layer and as TG material, attributed to its matching work function (cf. Section 2.3.1) and Au as bonding material. Attributed to the well-known TG fabrication parameters of Ge SBFETs, [75, 262] the same TG stack is used for Si and $Si_{1-x}Ge_x$ based SBFETs. Importantly, for single top gated SBFETs, the obtained Ω-shaped TG covers the MSJs and the semiconductor channel for excellent electrostatic gating capabilities. Further, the impact of adsorbates on the charge carrier transport is minimized, as the semiconductor is not prone to ambient conditions.

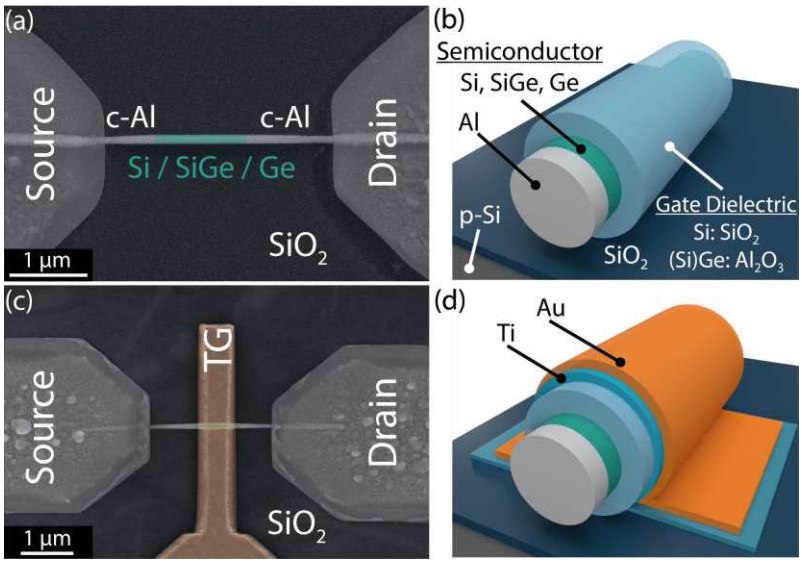


Figure 3.3: *(a) False-color SEM image of a NW with Al contacts after the solid-state exchange reaction initiated by RTA. (b) 3D illustration of the deposited NW. Note that the NW passivation is in direct contact with the BG oxide. (c) False-color SEM image of a top gated device, where the TG covers the complete semiconductor channel and overlaps both MSJs. (d) 3D illustration of the top gated device, showing the Ω-shaped TG for efficient electrostatic gating.*

Thus, the key process steps can be summarized as listed in the following:

- Nanowire growth (VLS)
- Gate oxide formation
  - Si: Thermal SiO_2
  - $Si_{1-x}Ge_x$ & Ge: ALD Al_2O_3
- Nanowire deposition
- Al contact formation
  - BHF etching
  - $Si_{1-x}Ge_x$ & Ge: HI dip
  - Al sputtering and lift-off
  - RTA in H_2/N_2 for exchange
    - Al-Si & Al-$Si_{1-x}Ge_x$: 773 K
    - Al-Ge: 673 K
- Top gates formation
  - Ti/Au evaporation and lift-off

Summary of the process scheme for fabricating the proposed Al-group IV based SBFETs from top to bottom.

In the case of fabricating a multiple TG SBFET, as considered in Sections 4.3 and 4.4, the same fabrication techniques are applied. Further, after fabricating and analyzing the TGs by SEM, a soft bake-out at 373 K for 15 min is performed at ambient conditions prior to electrical measurements. Thus reducing the density of "slow" trap states and setting the SBFET closer to an initial state. [17]

Heterojunction characterization

In order to characterize the heterojunction, scanning transmission electron microscopy (STEM) is needed. Attributed to the thick handle wafer (500 µm *p*-Si + 100 nm SiO_2) of the "hexpad", STEM cannot be directly performed. [147] Therefore, lacey carbon grids and Si_3N_4 membrane chips with a thickness of 40 nm are used, which are discussed in the following.

Characterizing the MSJ from a structural point of view is a challenging task, as a sufficiently high imaging resolution is required, enabling the analysis on an atomic level. Hence allowing the detection of any inter-mixing of the metal and semiconductor, as well as the determination of any potential compound material or cavity. In this sense, SEM imaging is insufficient, as it merely delivers a surface characterization with a resolution of ~1 nm, depending on the acceleration voltage. [263] Moreover, in correspondence to the selected mode (secondary or back-scattered electrons), only the top few nanometers of the structure can be visualized. In contrast, STEM allows a resolution < 1 nm and also operates at higher acceleration voltages (SEM: ~5 kV; STEM: 200 kV), allowing a thorough analysis of the sample.

In the scope of the thesis at hand, STEM and EDX investigations were performed to analyze the proposed Al-group IV semiconductor MSJs. In particular, bright field (BF) and high-angle annular dark-field (HAADF) STEM imaging were used for MSJ characterization. Additionally, on an Al-$Si_{0.5}Ge_{0.5}$ based SBFET electron beam-induced current (EBIC) investigations within a STEM system were performed. Therefore, the thickness of the handling substrate needs to be < 100 nm because electrons need to transmit through the sample for detection. [147] As STEM investigations were performed by two collaboration partners, two different handling substrates were used.[1] First, lacey carbon grids were used to investigate the thermally grown SiO_2 on Si NWs, which are commercially available for many STEM setups. In general, transferring NWs onto a lacey carbon grid enables a simple and fast method for STEM investigations, further providing a mechanically stable substrate for NW core and shell investigations. However, lacey carbon grids do not allow the evaluation of the proposed Al-group IV MSJs, as no Al source/drain pads can be fabricated. Nevertheless, in the scope of this thesis, lacey carbon grids are used for STEM and EDX investigations of the SiO_2 shell, which is discussed thoroughly in Section 4.1.1. Figure 3.4 shows a SEM image of a lacey carbon grid with already deposited and SiO_2-passivated Si NWs.

[1] Lacey carbon grid: Dr. Lilian Vogl, EMPA Thun, Switzerland.
Si_3N_4 membrane: Dr. Martien I. den Hertog, Institut Neél, Grenoble, France.

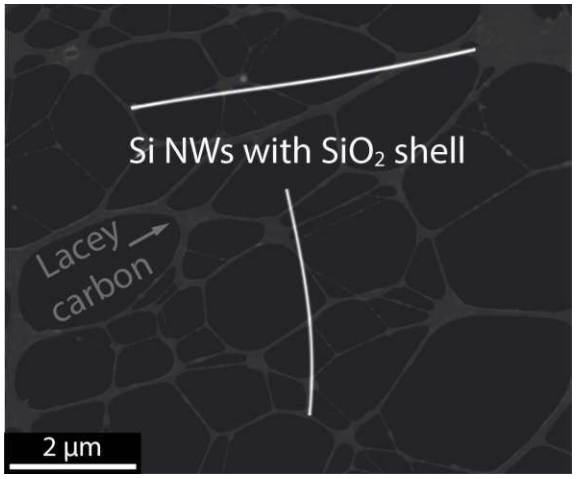


Figure 3.4: *SEM image of a commercial lacey carbon grid for STEM investigations. The grid already contains SiO_2-passivated Si NWs. In the scope of this thesis, these grids are used to investigate the SiO_2 gate oxide and determine its thickness.*

In contrast, a more advanced substrate is required for investigations of the proposed Al-group IV MSJs, enabling the deposition of Al and solid-state exchange reaction between Al and the group IV semiconductor. In this respect, 40 nm thick Si_3N_4 membranes are used as illustrated in Figure 3.5. The used membrane chip with Ti/Pt pads was designed and provided by Dr. Martien I. den Hertog, Institut Neél, France. [264] In contrast to the commercially available lacey carbon grids, the membrane chip allows the fabrication of Al source/drain regions and the application of RTA, enabling the desired MSJs. In general, the same fabrication steps as for the "hexpad" integration are used. As shown in Figure 3.5(b), NWs (yellow rectangles) are connected to the Ti/Pt bond pads for electrical investigations, whereas also dummy Al pads are used (green rectangles) for investigations of the MSJs only. Concerning STEM and EDX analysis, a considerable drawback in using Si_3N_4 is the evidence of a strong Si signal, which is, in particular, interfering in EDX investigations.
The STEM measurement equipment, which uses the Si_3N_4 membrane chips, consists of a probe-corrected FEI Titan Themis and Jeol Neo Arm, working at 200 kV and the capability of performing in-situ electrical measurements. In terms of NWs, due to their radial nature, the observation direction is of significant importance in STEM investigations, as elaborated in Section 4.1.

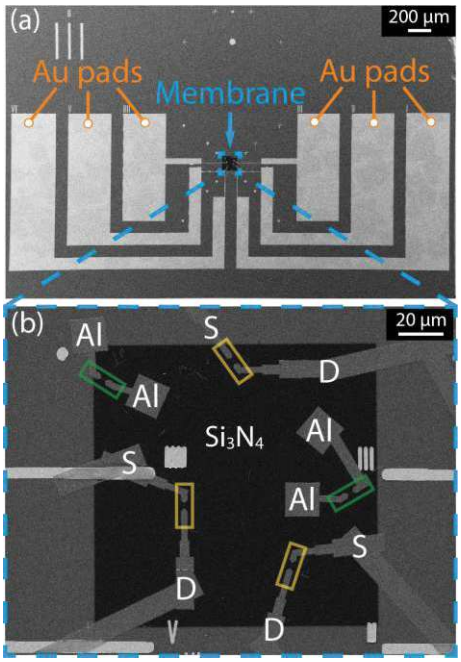


Figure 3.5: *(a) Si_3N_4 membrane chip, showing the Au pads for electrically connecting NWs within the STEM system. (b) Zoomed view of the membrane containing NWs. Note that green boxes indicate NWs, which are merely used for the MSJ characterization, whereas NWs marked by yellow boxes also allow electrical measurements, e.g., required for EBIC investigations.*

Using the proposed Si_3N_4 membrane chip with its Ti/Pt pads allows for EBIC investigations, which already proved to be an essential analysis tool in investigating NWs based on $Si_{0.67}Ge_{0.33}$ [265] or GaAs/AlGaAs core-shell structures [266]. [267] In general, EBIC allows the identification of buried junctions or defects in semiconductors and is, therefore, of particular interest in analyzing MSJs. In this respect, the technique depends on the formation of electron-hole pairs induced by the e-beam of the STEM. [92] Therefore, as illustrated in Figure 3.6, a current amplifier is used for the measurement of the induced (drift) current, which intensity depends on the built-in electric field qV_{bi} at the MSJ (cf. Section 2.2.2). In combination with STEM and the relatively high e-beam energy of 80 kV, electrons are only partly absorbed and allow a co-use with EBIC for precise localization of junctions. Consequently, the e-beam scans across the sample and is mapped accordingly to the STEM image. Therefore, depletion regions can be determined and tuned by applying an external bias, i.e., V_{DS}. Note that, attributed to the Si_3N_4 membrane chip, electrostatic gating cannot be accessed. In the scope of the work at hand, EBIC allows for qualitative analysis of the degree of equality of the two back-to-back Schottky junctions, as positive and negative charge carriers are separated, resulting in the total collected current through the sample.

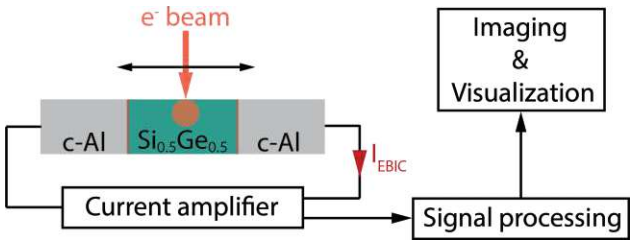


Figure 3.6: *Schematic EBIC setup used for the characterization of an Al-$Si_{0.5}Ge_{0.5}$ based SBFET. The e-beam generates electron-hole pairs in the NW and, therefore, allows the determination of local electric fields and defects. Using EBIC combined with STEM allows for direct mapping of the MSJ's position.*

In the scope of the thesis at hand, STEM and EDX investigations are conducted for all proposed Al-group IV material systems, whereas EBIC was merely demonstrated on Al-$Si_{0.5}Ge_{0.5}$ based SBFETs. Notably, this is attributed to the fact that the Al-$Si_{1-x}Ge_x$ MSJs do not exhibit sharp profiles as evident in the Al-Si and Al-Ge material system (cf. Section 4.1).

Intrinsic group IV semiconductor NWs are integrated into SBFETs by fabricating Al source/drain contacts and intruding the Al into the NW, enabling MSJs. Therefore, "hexpads" are used as handling substrates for electrical probing. The **structural investigation of the obtained MSJs is done by STEM and EDX**, utilizing **lacey carbon grids and Si_3N_4 membrane chips**. **In combination with STEM, an EBIC study was performed on Al-$Si_{0.5}Ge_{0.5}$-Al NW heterostructures**.

3.2 Electrical Characterization

After the integration of the proposed group IV NWs into SBFETs, the electrical characterization was performed. Therefore, this section focuses on the used measurement equipment and discusses the evaluation of extracted data. First, Section 3.2.1 elaborates on the electrical measurement equipment, followed by an explanation of the extraction methodologies of SBFET FOM in Section 3.2.2. As the activation energy E_a is of essential relevance in SBFETs (cf. Section 2.3.2), Section 3.2.3 discusses the evaluation methodology based on the 3D TE model. Lastly, Section 3.2.4 highlights bias spectroscopy and sets it in relation to low-temperature physics and first principles obtained from SBFETs.

3.2.1 Experimental Equipment

For the electrical data acquisition, a semiconductor analyzer in combination with a Lake Shore PS-100 cryo-probe station was used, as illustrated in Figure 3.7. For the conduction of measurements at cryogenic temperatures (here: min. 77 K), a vacuum pump stage (Pfeiffer HiCube with a backing pump and turbo pump) is directly connected to the experimental chamber of the Lake Shore system, reaching vacuum levels of ~1×10^{-6} mbar. Further, cryogenic temperatures are achieved by using liquid nitrogen (LN_2), reaching a minimum temperature of ~77 K. A Lake Shore model 336 temperature controller was used to set temperatures, which is directly connected to the heating stage within the experimental chamber [cf. Figure 3.7(b,c)]. Further, a Keysight B1500A semiconductor analyzer with four Source-measure units (SMUs) and two Voltage-source units (VSUs) was used for the acquisition of electrical data. Thus allowing to apply and/or sweep DC voltages, required to extract the desired I/V characteristics. Moreover, the installed SMUs allow for pulsed operation, allowing for the minimization of charging and charge carrier trapping effects by reducing the involved time constants. Consequently, continuous vs. pulsed I/V measurements allow to get an impression of the origin of hysteresis effects, which is crucial in particular in Al-Ge based SBFETs, due to the potential impact of native Ge_xO_y and its associated high density of trap states.

For the characterization and extraction of SBFET FOM, basically transfer (I_D vs. V_G at fixed V_D) and output (I_D vs. V_D at fixed V_G) characteristics are required. Note, that if not otherwise stated $V_S = 0$ V. In terms of NDR devices, output characteristics at $V_G > 0$ V (n-type operation) are performed by additionally considering sufficiently high V_D to initiate the transferred electron effect (cf. Section 2.3.3). Moreover, attributed to the probe station setup and the temperature controller, a temperature range of 77 K to 400 K can be accessed, thus allowing a thorough T-dependent charge carrier transport characterization of the proposed Al-group IV material systems.
Integrating RFETs in logic circuits needs additional measurement equipment, as a logic circuit's functionality is properly described by transient measurements, i.e., I_D vs. t.

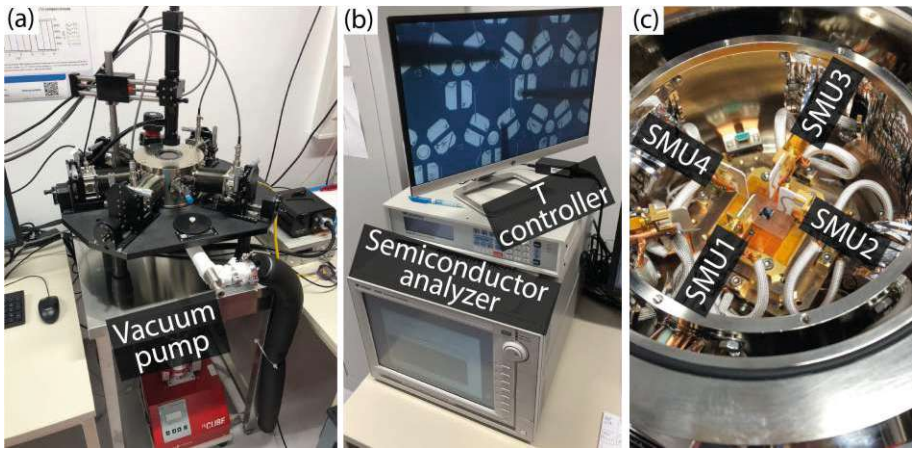


Figure 3.7: *(a) Lake Shore PS-100 probe station with connected Pfeiffer vacuum pump system. (b) Live microscope image visualizing the position of the contact needles. The Lake Shore 336 temperature controller and the Keysight B1500A semiconductor analyzer are also shown. (c) Image of the experimental chamber and stage showing probing needles and associated SMUs.*

Therefore, the generation of the input signals is done by a Yokogawa FG300 function generator connected to VMUs of an HP 4156B semiconductor analyzer.
In terms of the maximum applicable V_{DS}, the breakdown field of the proposed group IV semiconductors needs to be considered, which is 3 V/nm and 1 V/nm for Si and Ge, respectively (cf. Table 4.1). Further, in terms of the gate voltage V_{G}, the maximum bias is evaluated experimentally on a dummy SBFET before defining a dedicated measurement routine due to potential variations in the gate oxide thickness t_{ox} and quality. [17] However, in device realizations and in particular in circuits, the same (absolute) bias values are desired, which can be achieved by optimizing the device design, such as channel length L_{SC}, gate oxide thickness t_{ox} and selection of gate oxide material.

I/V characteristics are acquired by a Keysight B1500A semiconductor analyzer, using a Lake Shore PS-100 probe station, capable to perform **investigations in vacuum and in the temperature range of** 77 K **to** 400 K. Additionally, **transient measurements** are acquired by using an HP 4156B semiconductor analyzer and a Yokogawa FG300 function generator.

3.2.2 SBFET Figures of Merit

For a fair and comprehensive comparison of the proposed Al-group IV material systems, the same parameters and extraction methodologies need to be applied. Therefore, the transfer characteristic provides a valuable data set, allowing the extraction of important SBFET FOM. In this respect, Cheng et al. defined distinct parameters that shall be considered for characterizing emerging FETs. [79] Beside structural NW parameters, such as the semiconductor NW core diameter d_{NW}, the gate oxide thickness t_{ox} and the NW channel length L_{SC}, electrical parameters illustrated in Figure 3.8 are considered. From the transfer characteristic, the on-currents $I_{\mathrm{on}}^{\mathrm{n/p}}$ of the *n*- ($V_{\mathrm{G}} > 0\,\mathrm{V}$) and *p*-branch ($V_{\mathrm{G}} < 0\,\mathrm{V}$) as well as the off-current I_{off} are directly extracted. In this respect, the transistor research community normalizes currents to the channel width (in µA/µm), whereas in NW electronics, the NW diameter d_{NW} is used for normalization. Thus allowing a fair comparison of the currents between different device dimensions and architectures. Moreover, it is advised that I_{off} is extracted at $V_{\mathrm{G}} = 0\,\mathrm{V}$ and I_{on} at $V_{\mathrm{D}} = V_{\mathrm{G}}$, which however, bears two challenging aspects. First, attributed to fixed oxide charges (cf. Section 2.1.3), the transfer characteristic might be shifted horizontally, caused by trapped charges, e.g., trapped electrons in the oxide cause a shift towards a more positive V_{G}, as electrons are negatively charged. [262] Consequently, I_{off} being the minimum current in an ambipolar transfer characteristic is not evident at $V_{\mathrm{G}} = 0\,\mathrm{V}$. Another challenge in this context is the history of the investigated device, i.e., at which environmental conditions (adsorbates being dependent on ambient or vacuum conditions) and in which operation modes (applied bias voltages determine the accessible energy of trap states) the device was stored or operated. Further, the absolute temperature needs to be considered, as thermally excited charge carriers may occupy higher energy trap states. [268] Second, in many experimental transistor concepts, $V_{\mathrm{D}} = V_{\mathrm{G}}$ cannot be ensured due to non-optimized gate dielectrics and device architectures. Therefore, assuring a fair comparison needs an explicit definition of V_{D} and V_{G}. Moreover, having on- and off-currents evaluated allows to calculate the $I_{\mathrm{on}}^{\mathrm{n}}/I_{\mathrm{on}}^{\mathrm{p}}$ ratio, being an important dimensionless parameter in particular for the realization of RFETs. Further, defining the *n*- and *p*-type driving capabilities in logic circuits. Another important metric is the $I_{\mathrm{on}}^{\mathrm{n/p}}/I_{\mathrm{off}}$ ratio, quantifying the transistor's on-to-off capability.

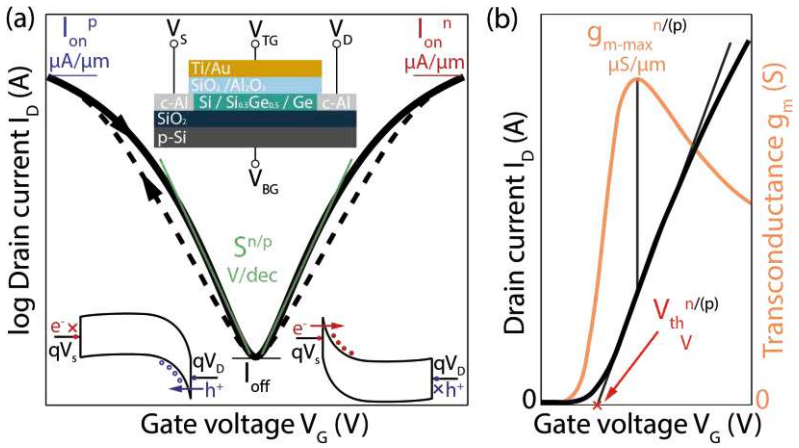


Figure 3.8: *(a) Idealized ambipolar transfer characteristic of a SBFET with equal n- and p-type branch. Additionally, relevant FOM are highlighted. The upper inset shows the naming convention of the applied bias at the corresponding electrodes. Moreover, the lower insets show V_G-dependent band diagrams. (b) Linear representation of the n-type transfer characteristic and the extraction of the transconductance g_m as well as the threshold voltage V_{th}. The same procedure applies to the p-type transfer characteristic.*

The following parameters are extracted using methodologies presented in "Semiconductor Material and Device Characterization" by D.K. Schroder. [147] In this context, the extraction of the inverse subthreshold slope $S^{n/p}$ (in V/dec, where a decade corresponds to a ten times increase of the drain current I_D) is discussed next. In this respect, a steep slope with low values is desired, determining an efficient transition between the on- and off-state. Evaluating $S^{n/p}$ requires to apply a tangent in the TE-dominated regime as indicated in Figure 3.8(a) and set its slope in correspondence to Equation (3.1).

$$S^{n/p} = \left(\frac{\partial \log(I_D)}{\partial V_G} \right)^{-1} \tag{3.1}$$

The subthreshold swing S_{th} is theoretically defined according to Equation (3.2).

$$S_{th} = \ln(10) \frac{k_B T}{q} \left(1 + \frac{C_d}{C_{ox}} \right), \tag{3.2}$$

where C_d is the depletion layer capacitance (in SBFETs also junction capacitance C_j), which attributed to the use of SB-based devices, exhibits low values (cf. Section 2.2.2). Regarding C_{ox}, the occupation of interface trap states and charging effects must be considered additionally. [79] Considering Equation (3.2), a minimum subthreshold swing is reached by letting $C_d \to 0$ and/or $C_{ox} \to \infty$, leading to the expression $S_{th-min} = \ln(10) k_B T/q$, which is known as the thermionic limit with a value of 60 mV/dec at $T = 300$ K. In this context, distinct switching mechanisms need to be accessed to achieve $S < 60$ mV/dec.

In respect to NW-based implementations, GAA Si p-FETs with an average $S_{\mathrm{th}} = 14\,\mathrm{mV/dec}$ were realized by suppressing band tail effects and neutral defect scattering. [269] Moreover, Kim et al. proposed p^{+}-n^{+}-i-n^{+} doped Si NWs, reaching values as low as 0.1 mV/dec by accessing positive feedback of charge carriers in the channel. [270] Further, negative capacitance gate-stacks encompassing a ferroelectric, such as HZO (Hafnium Zirconium oxide), allow to increase the performance of steep subthreshold devices with $S < 60\,\mathrm{mV/dec}$ due to internal voltage amplification. [271]
Next, the transconductance g_{m} is considered, which extraction is schematically illustrated in Figure 3.8(b). As stated in Equation (3.3), g_{m} is calculated directly from the transfer characteristics data, which is a major FOM for transistors applied in amplifiers. [17]

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{G}}} \tag{3.3}$$

Similar to the on- and off-current normalization, the transconductance is also normalized to the NW diameter d_{NW} (unit: µS/µm). In the case of on-current saturation as indicated in Figure 3.8, a distinct $g_{\mathrm{m-max}}$ can be extracted, allowing for comparison of different material systems and device architectures. Further, the transconductance g_{m} is used to evaluate the threshold voltage $V_{\mathrm{th}}^{\mathrm{n/p}}$ as a physics-based method. Therefore, a modified linear interpolation method, as illustrated in Figure 3.8(b), is used. Thus, $g_{\mathrm{m-max}}$ is evaluated and vertically projected to the transfer I/V data at the V_{G} value. At the corresponding I_{D} value a tangent is applied and interpolated to $I_{\mathrm{D}} = 0\,\mathrm{A}$, where the interception determines V_{th}. Note that g_{m} and I_{D} data need to be visualized linearly for this procedure. In general, the linear interpolation method requires the calculation of the threshold voltage according to $V_{\mathrm{th}} = V_{\mathrm{intercept}} - V_{\mathrm{DS}}/2$. [147] However, this equation strictly holds for negligible series resistance that is typically not evident in SB-based devices. Therefore, regarding a fair comparison of the proposed Al-group IV based SBFETs, $V_{\mathrm{intercept}} = V_{\mathrm{th}}$ is applied.
In general, transfer characteristics can be measured by performing a single V_{G} sweep, e.g., starting at $V_{\mathrm{G}} = 5\,\mathrm{V}$ and sweeping to $-5\,\mathrm{V}$. Additionally, as indicated by the dashed curves in Figure 3.8(a), a double sweep, e.g., starting at $V_{\mathrm{G}} = 5\,\mathrm{V}$ and sweeping to $-5\,\mathrm{V}$ and subsequently back to 5 V reveals a hysteresis. Consequently, extracting V_{th} of the forward and backward sweep and calculating the difference $V_{\mathrm{th-forward}} - V_{\mathrm{th-backward}}$ results in a metric for the hysteresis. In this respect, trap states at the oxide/semiconductor interface, as well as fixed charges in the oxide, are influencing the threshold voltage V_{th}, resulting in hysteresis effects (cf. Section 2.1.3). [262, 272] Certainly, fixed charges in the oxide Q_{f} in the oxide cause permanent V_{th} shifts. Therefore, also time constants concerning the trapped charge carrier's lifetime need to be taken into account, whereas additionally, the device's history impacts the trap states' occupation. Thus, to improve gating efficiency, besides reducing C_{ox}, low D_{it} and Q_{f} values are desired, directly leading to reduced hysteresis effects.

Reconsidering the previously mentioned history and transient stability, i.e., hysteresis, of SBFETs, the accurate extraction of its FOM bears challenges that need to be considered. The following gives an overview of the most important aspects to consider in evaluating SBFET FOM:

- Adsorbates:
  Due to the Ω-shaped metal TG architecture, the channel is entirely shielded and the influence of adsorbates is significantly decreased and does, therefore, not play an essential role in evaluating the proposed SBFETs. However, in devices where the oxide-covered semiconductor channel is in contact to ambient conditions, i.e., back gated SBFETs, adsorbates highly influence FOM by electrostatically influencing the charge carrier transport (cf. Section 2.1.3).

- Density of interface trap states D_{it} and fixed charges Q_{f}:
  Trap states at the semiconductor/oxide interface are the main contributors to transiently unstable devices, highly impacting the I/V characteristics by capturing charge carriers. Therefore, material systems with low D_{it} are desired for reliable and reproducible transistor operation. In contrast, Q_{f} can be engineered to tune the threshold voltage V_{th} and position the transfer characteristic horizontally. [49]

- Absolute temperature:
  According to Fermi-Dirac statistics, the absolute temperature determines the degree of thermal excitation of charge carriers. Therefore, decreasing the temperature reduces the charge carrier concentration, known as freeze-out. [17] Consequently, reducing the probability of charge carrier trapping and, therefore, the density of trapped states.

- Sweeping mode, rate and direction:
  As trapped states are highly determined by their occupation density and capture cross-section, the sweeping mode, i.e., continuous or pulsed, the rate, i.e., step width between two subsequent data points, as well as the voltage's slope and direction of sweeping, i.e., from 0 V, positive or negative bias, the state of the involved traps are determined. Attributed to a changed occupation of energy states and the history of measurements, the I/V characteristics are prone to variations.

To reduce history effects, e.g., caused by SEM imaging or prior electrical measurements, a soft bake-out routine at 373 K for 15 min was performed at ambient conditions, bringing the device closer to its initial state by reducing the density of trapped charge carriers. [268]

In terms of evaluating the previously discussed FOM, Python scripts were developed to extract parameters, providing a fast and reliable routine for investigating and comparing SBFET FOM. During the script development, extracted parameters were cross-checked by manual evaluations with the software tool "OriginPro 2022". With respect to the visualized I/V data a Savitzky-Golay smoothing filter is applied, ensuring the originality of the shown data.

Output characteristics, i.e., I_D vs. V_D at fixed V_G are used for SBFET characterization as well, where the linear and logarithmic representation is used individually. In this respect, the linear visualization allows the interpretation of the I/V linearity and enables the evaluation of the potential ohmic behavior of the proposed SBFETs. Moreover, information about the saturation properties for given bias voltages of the underlying device can be extracted. In contrast, plotting I_D on a logarithmic scale allows the extraction of distinct operation regimes discussed in Section 2.3.1. Using T-dependent output characteristics builds the basis for evaluating an activation energy E_a, being a minimum energy required to inject charge carriers from the metal into the semiconductor.

3.2.3 Extraction of an Activation Energy

As elaborated in Section 2.3.2, different theoretical models and considerations for extracting an activation energy E_a can be applied. As the 3D TE model is used for all proposed Al-group IV material systems, a thorough description of its application and derivation is given in the following. Note that in Figure 3.9, the procedure for a top gated Al-Ge based SBFET is illustrated, which, is applied in the same manner to the other investigated material systems.
The starting point is the already introduced 3D TE model of the current (density) (cf. Section 2.3.2), shown in Equation (3.4). [17]

$$J_D = A^* T^2 \exp\left(-\frac{E_a}{k_B T}\right)\left[\exp\left(\frac{qV_D}{k_B T}\right) - 1\right], \tag{3.4}$$

considering $V_S = 0\,V$. Note that the effective 3D Richardson constant A^* is unknown in most experimental configurations. Thus, E_a is evaluated by acquiring T-dependent output characteristics in the temperature range $T = 295\,K$ to $400\,K$, in $\Delta T = 20\,K$ steps (exception: $\Delta T|_{295K-320K} = 25\,K$). As shown in Figure 3.9(a), obtaining the output characteristics at different V_{TG} allows to evaluate gate-dependent E_a values. After rearranging and applying the natural logarithm to Equation (3.4), an Arrhenius expression according to Equation (3.5) is obtained [cf. Figure 3.9(b)].

$$\ln\left(\frac{J_D}{T^2}\right) = \left(-\frac{E_a}{k_B} + \frac{qV_D}{k_B}\right)\frac{1}{T} + \ln(A^*), \tag{3.5}$$

where the left-hand side term follows a linear $1/T$ trend with slope $m = -E_a/k_B + qV_D/k_B$. In respect to the derivation of Equation (3.5), $\exp\left[qV_D/(k_B T)\right] >> 1$ holds, which is considered as a boundary condition discussed in Section 2.3.2. Finally, Equation (3.6) shows the expression to obtain E_a, using the slope m extracted from Figure 3.9(b).

$$E_a = qV_D - mk_B \tag{3.6}$$

Further, Figure 3.9(c) depicts that for each V_D data point, a dedicated E_a value exists. This property is further facilitated in evaluating V_D- and V_{TG}-dependent activation energy maps presented in Section 4.2. Furthermore, using linear fitting to $V_D = 0\,V$ allows to deduce distinct V_{TG}-dependent E_a values. Performing the same methodology and procedure for $V_{TG} = 5\,V$ to $-5\,V$ in $1\,V$ steps, results in Figure 3.9(d), showing the activation energy in dependence of V_{TG}. In addition, considering the subthreshold regime, a linear fit can be applied to estimate the flat-band voltage V_{FB}. Note that a thorough discussion and interpretation of the activation energy E_a is given in Section 4.2.
Moreover, the 1D LB model was also applied on top-gated Al-Ge based SBFETs due to the 1D-confined Ge NW channel (cf. Section 2.1.3). Therefore, its extraction methodology and evaluation, as well as comparison to the 3D TE model, are discussed in Section 4.2.3.

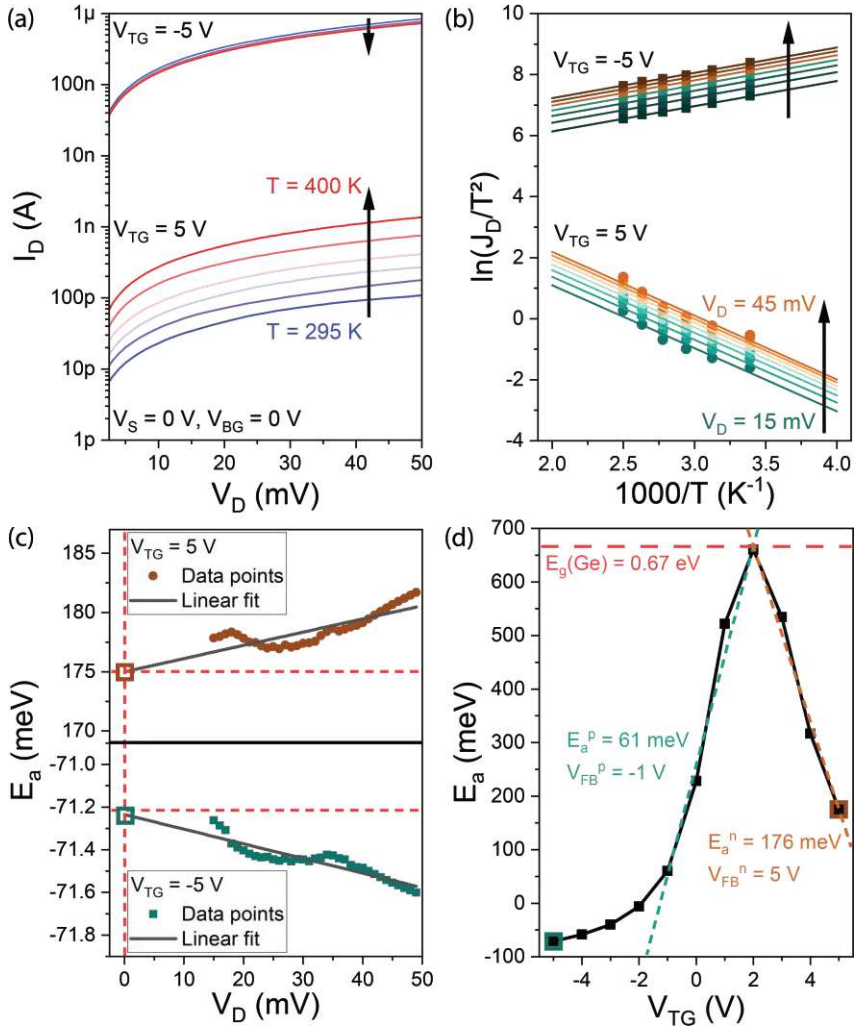


Figure 3.9: *Activation energy E_a extraction methodology based on a top gated Al-Ge based SBFET. (a) T-dependent output characteristics in strong electron and hole accumulation at V_{TG} = 5 V and −5 V, respectively. (b) Arrhenius plots of the two corresponding V_{TG} values and for selected bias V_D. The x-axis has been multiplied by a factor of 1000 for plotting purposes. (c) Linear fitting of the V_D-dependent E_a values to $V_D = 0$ V of the selected V_{TG} biases. (d) V_{TG}-dependent E_a values with indicated $E_a^{n/p}$ and $V_{FB}^{n/p}$. Images from [RB1].*

Important SBFET FOM, are the on-currents $I_{on}^{n/p}$, the off-current I_{off}, the subthreshold slope $S^{n/p}$, the transconductance $g_{m(-max)}^{n/p}$, the threshold voltage $V_{th}^{n/p}$, the hysteresis, the activation energy $E_{n/p}$ and flat-band voltage $V_{FB}^{n/p}$.

3.2.4 Bias Spectroscopy

In general, bias spectroscopy measurements are broadly used in low-temperature physics, investigating transport phenomena, such as superconductivity or Coulomb blockades. [47, 80] Thus, enabling the determination of dedicated operation regimes of the underlying structures. A prominent device example is the JJ-FET, which transfer characteristic in Figure 3.10(a) is illustrated as a transport map by conducting consecutive I_{D} (here: $G = I_{\mathrm{D}}/V_{\mathrm{D}}$) vs. V_{G} transfer I/V measurements at different V_{D} biases and at $T =$ ~400 mK. Rearranging the acquired data in a matrix, where each horizontal line represents a single transfer characteristic, allows for the distinction between the different transport regimes, therefore visualizing a profound understanding of the bias dependencies. Another example on the base of parallel printed $NiSi_2$-Si NW SBFETs is shown in Figure 3.10(b), where the transfer characteristic is illustrated as a transport map. Here, the transport regimes elaborated in Section 2.2.2 are indicated as well, which visualization is inhibited by single transfer characteristics.

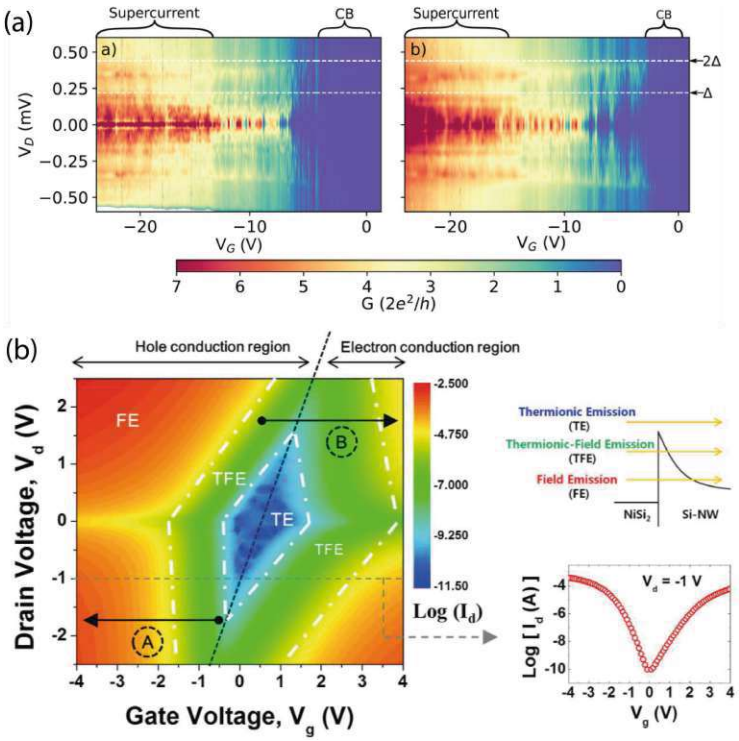
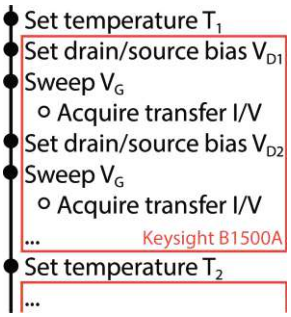


Figure 3.10: *(a) Typical transport maps used in low-temperature physics for the investigation of superconductivity or Coulomb blockades, where the z-axis illustrates the conductance $G = I_{\mathrm{D}}/V_{\mathrm{D}}$. Image from [47]. (b) Transport map obtained from a $NiSi_2$-Si based SBFET and indicated injection mechanisms. Additionally, a single transfer characteristic is shown in the bottom right corner at $V_{\mathrm{d}} = -1\,\mathrm{V}$. Image from [273].*

An essential prerequisite for acquiring bias spectroscopy data is the assurance of transiently stable devices, attributed to the fact that consecutive I/V measurements are performed. Thus allowing the acquisition of transfer characteristics with a primary sweep of V_G and a secondary sweep of V_D. Notably, influencing the occupation of trap states at every single sweep (cf. Section 3.2.2). In this respect, a low D_{it} is required, which is in particular challenging in Ge-based devices, attributed to the potential formation of Ge_xO_y (cf. Section 2.1.2).
For the acquisition of I/V data suitable for bias spectroscopy, the following measurement routine is used to obtain T-dependent bias spectroscopy data of the transfer characteristic, which, however, can also be applied to output I/V data:



Measurement procedure to acquire T-dependent bias spectroscopy data.

In the scope of the thesis at hand, bias spectroscopy maps of I_D, g_m and E_a are used to reveal operation regimes and underlying transport properties which cannot be visualized by single I/V sweeps. Notably, the same procedure can be applied to output characteristics, enabling the visualization and determination of T-dependent transport mechanisms, such as TE, FE, or TFE.

For a **comprehensive understanding, bias spectroscopy maps of I_D, g_m and E_a allow to determine distinct transport and operation regimes**, which can not be accessed by single parameter I/V sweeps.

Chapter 4

Results and Discussion

The following chapter presents the results obtained by investigating the stated research questions (cf. Section 1.1), whereas the theoretical concepts elaborated in Chapter 2 and experimental techniques in Chapter 3 are considered. All investigations consider results from nominally intrinsic group IV semiconductor NWs.
First, Section 4.1 presents the proposed Al-group IV MSJs from a material composition and structural point of view, [RB2,RB3] whereas in Section 4.2 the charge carrier transport of the thereof realized SBFETs is discussed, starting with the electrical characterization of the individual material systems, additionally considering T-dependent bias spectroscopy. [RB1,RB3,RB4] Lastly, a summary is presented, comparing and setting the SBFET FOM and main characteristics of the investigated material systems into relation. Following the results obtained in Section 4.2, "Beyond CMOS" devices are realized from the gained insights. Therefore, the first Al-Si based RFET and thereof realized basic logic circuits are discussed in Section 4.3. [RB2, RB5, RB6] Further, Section 4.4 presents a throughout NDR characterization methodology using bias spectroscopy as well as investigating NDR cascode circuits, enabling enhanced NDR functionality. [RB4, RB7] Lastly, Section 4.5 discusses a top-down fabricated Al-Ge based SBFET, which demonstrates a bias-tunable temperature coefficient of resistance (TCR). [RB8]

4.1 Structural Characterization of Al-Group IV Junctions

This section elaborates on the heterojunction formation of Al-Si, Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge MSJs, which is crucial for realizing and operating the proposed SBFETs. Therefore, STEM and EDX investigations were carried out on lacey carbon grid and Si_3N_4 membranes, as discussed in Section 3.1. Moreover, the fabricated passivation shells are elaborated, which also build the gate dielectric in the proposed Al-group IV SBFETs. Notably, the same RTA process, however, at different temperatures, was carried out to initiate the solid-state exchange mechanism between Al and nominally un-doped Si, $Si_{0.5}Ge_{0.5}$ as well as Ge NWs (cf. Section 2.2).

4.1.1 Al-Si Heterojunction

The starting point for investigations on the Al-Si exchange mechanism are intrinsic and predominantly ⟨112⟩-oriented Si NWs grown in a home-built, hot-wall CVD system using silane (SiH_4, Voltaix), hydrogen chloride (HCl anhydrous; Matheson TriGas, 5N research purity grade), and hydrogen (H_2, Matheson TriGas, 5N semiconductor grade) as a carrier gas, following procedures by Kim et al. [274] Further, Au nanoparticle catalysts of a nominal diameter of 80 nm (Sigma-Aldrich) are immobilized on the growth substrates composed of Si wafers with 600 nm thermal oxide (NOVA Electronic Materials) by functionalizing the substrate with poly-L-lysine (Sigma-Aldrich) followed by the functionalization with Au nanoparticles. Substrates are cleaned in a UV-ozone cleaner and inserted in a 1 in quartz-tube furnace (Lindberg Blue M) for growth. Finally, the NW nucleation is performed at 753 K with 2 sccm of SiH_4, 4 sccm of HCl, and 194 sccm of H_2 at 20 torr total reactor pressure for 20 min until a desired NW length of 20 µm is achieved after 80 min.[1]

Fabrication of the native SiO_2 shell

After the NW growth, the Si NWs are thermally oxidized in O_2 atmosphere, using an ATV PEO601 furnace, and subsequently annealed in N_2 atmosphere for the same duration and temperature to effectively reduce fixed charges. [146] As no oxidation results were available of intrinsic ⟨112⟩-oriented Si NWs with nominal diameters of 80 nm, various oxidation durations are investigated to evaluate the SiO_2 growth rate. The relevant oxidation temperature was extracted from Krylyuk et al., who carried out investigations on ⟨111⟩-oriented Si NWs. [275] In the latter work, a temperature of 900 °C in O_2 atmosphere is used, which is also proposed by Liu et al., [276] claiming better performance metrics in terms of hysteresis and subthreshold slopes. Note that during heating-up 200 sccm N_2 was supplied. Next, 50 sccm O_2 was used during oxidation at $T = 900$ K. Finally, an annealing step with 200 sccm N_2 was performed at the oxidation temperature.

[1] The Si NW growth was performed by Corban G.E. Murphey and Prof. James F. Cahoon at the Department of Chemistry, University of North Carolina at Chapel Hill, United States.

Oxidation durations of 2.5 min, 3 min,[2] 5 min and 10 min were used and analyzed. Figure 4.1 shows the thereof obtained SiO_2 thicknesses evaluated by a combination of STEM and EDX linescans of oxidized NWs suspended on lacey carbon grids (cf. Section 3.1).

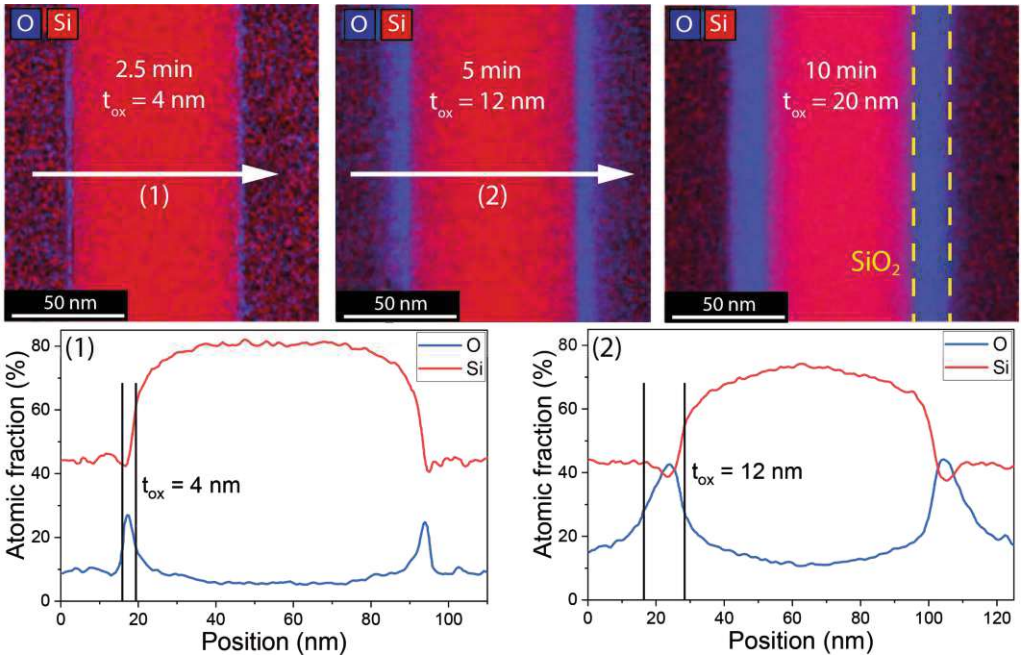


Figure 4.1: *STEM EDX analysis in the top row illustrates the oxidized Si NWs with an increasing SiO_2 thickness attributed to longer oxidation durations. (1) and (2) indicate the performed EDX linescans for oxidation durations of* 2.5 min *and* 5 min*, respectively. Additionally, in the* 10 min *oxidation EDX plot, the SiO_2 shell is highlighted. t_{ox} values are nominal values.*

In this context, it needs to be considered that due to the oxidation process and its associated temperature ($T_{ox} = 900\,°C$), the NW surface might become more circular, resulting in more complex crystal orientations at the Si/SiO_2 interface. [277] Additionally, mechanical strain is induced, whose intensity depends on the actual surface crystal orientation. [278] Further, Figure 4.1 indicates that sequential steps of oxidation and etching would allow for reducing d_{NW} of the Si NW. With respect to the oxide growth, t_{ox} follows approximately a typical diffusion-limited oxide growth, as discussed in the following. Moreover, beyond the selected oxidation duration, it is expected that eventually SiO_2 formation will become self-limiting as the induced strain reduces O_2 diffusion. [279]

[2] STEM and EDX investigations were done by Martien I. den Hertog at Institut Néel, CNRS, France. Detailed results of these analyses are discussed in the subsection "Al-Si junction".

Figure 4.2 shows the obtained SiO_2 thicknesses t_{ox} vs. the previously mentioned oxidation durations. Note that within the error bars, caused by uncertainties of the t_{ox} extraction via STEM, a quadratic fit may be applied according to the Deal-Groove model, [17] whereas the dashed line merely illustrates a visual guide.

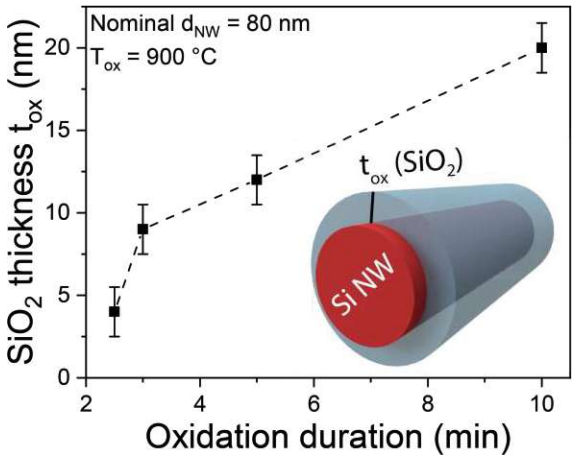


Figure 4.2: *SiO_2 thickness t_{ox} vs. oxidation duration illustrating a fast oxidation rate for low SiO_2 thicknesses. Increasing the oxidation duration leads to a diffusion-limited behavior within the limits of typical errors in the extraction of t_{ox}.*

Observing Figure 4.2 allows to estimate the expected SiO_2 thickness t_{ox}, which further acts as the gate oxide of the Al-Si based SBFETs. In the thesis at hand $t_{ox} = 9\,\text{nm}$ was chosen, corresponding to an oxidation duration of 3 min with a subsequent N_2 annealing again for 3 min at 900 °C.

Al-Si junction

Consequently, after the fabrication of the 9 nm thick SiO_2 passivation shell, the nominally un-doped ⟨112⟩-oriented Si NWs were transferred to the Si_3N_4 membrane chip for STEM and EDX analysis. The detailed processing steps are elaborated in Section 3.1. Additionally, the theoretical aspects discussed in Section 2.2.1 need to be taken into account, which promote the formation of single-crystalline Al contacts to Si without the formation of inter-metallic phases. Finally, after the solid-state exchange initiated by RTA at $T = 773\,\text{K}$ in H_2/N_2 atmosphere, a channel length of ~1 µm is obtained. The mean annealing rate extracted from 19 Al-Si-Al NW heterostructures on "hexpads" was evaluated to be $(31 \pm 8)\,\text{nm/s}$. In this respect, exchange rate variations might be caused by different Al-Si contact surfaces, e.g., patchy oxide layers between the Al and Si contact areas or local temperature inhomogenities. Figure 4.3 shows the result of the Al-Si solid-state exchange mechanism by increasing the magnification on the left-sided MSJ.

Using extended RTA allows the fabrication of fully exchanged NWs, which consist of pure Al, which might be an useful approach for the realization of interconnects (cf. Figure A.1).

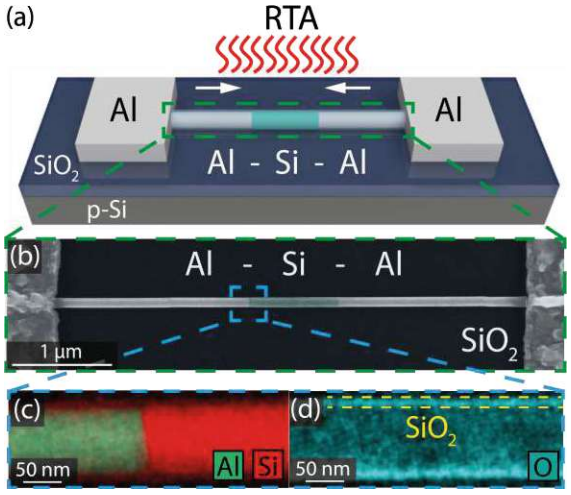


Figure 4.3: *(a) Schematic illustration of the Al-Si-Al NW heterostructure and indicated RTA process. (b) False-color SEM image showing a device with* $L_{SC} = 1\,\mu m$.[a] *(c) STEM EDX map revealing the abrupt Al-Si interface without inter-metallic phases.*[b] *(d) An additional EDX map shows the O marker, where a unified* SiO_2 *shell is evident, surrounding the complete NW.*

[a] SEM image from [RB2].
[b] EDX image from [RB6].

Next, BF and HAADF STEM analysis of the Al-Si nanojunction is performed to gain further insights into the crystallinity of the proposed MSJ. Especially, the crystal orientation has a significant influence on the electronic transport, as it impacts the band structure and, in consequence, influences the charge carrier effective masses and mobilities as well as on-currents (cf. Section 2.1.3). [58, 100] Figure 4.4 shows STEM images of two individual NWs [(a,b) and (c,d)], where a dedicated difference in the shape of the junction is evident. First, Figure 4.4(a,b) shows HAADF STEM images of an Al-Si nanojunction, which exhibits a straight junction indicated by the blue dashed line. Additionally, the SiO_2 passivation shell is visualized. Observing the Al-Si nanojunction in the Si [110] zone axis (observation along this direction) allows to visualize the (111) planes of Si along the [110] direction of observation. In this context, considering the [110] observation direction enables to perform dense, strongly diffracting, and rather large lattice spacing imaging [cf. Si in Figure 4.4(b)]. [280] Considering the lattice spacing, taking the diamond cubic crystal structure into account and using a crystallographic database allows to extract the crystal orientation of Si, which was determined to be $\langle 111 \rangle$. [263] Note that the used Si NWs were nominally grown in $\langle 112 \rangle$ crystal orientation.

Besides having straight Al-Si junctions, many interfaces exhibited a "V-shape" as shown in Figure 4.4(c-d), where the tip of the "V-shaped" junction correlates to the location of the Si twin boundary. Thus, twin (111) Si boundary planes are evident extending along the growth axis, which was already reported for ⟨112⟩-grown Si NWs. [281,282] A potential root cause of such twins is impurities, which are, however, not detectable in the NW itself. [263]

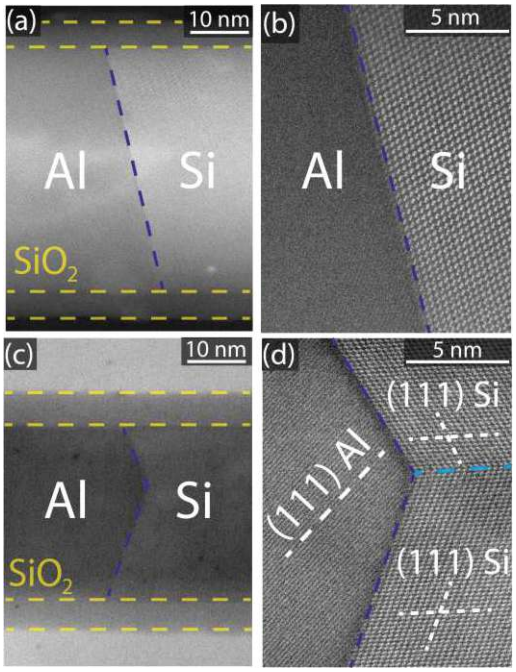


Figure 4.4: *(a) HAADF STEM image of the Al-Si heterojunction with the indicated nanojunction and SiO_2 passivation shell. (b) HAADF STEM image of the junction shown in (a), where the Si part of the NW is oriented along the [110] direction of observation. (c) BF STEM image of another Al-Si heterojunction, revealing a "V-shaped" MSJ interface. (d) HAADF STEM image with indicated crystal planes at the Al-Si interface. Additionally, the twin (111) Si planes are shown, whereas also (111) Al planes are indicated. The Si part of the NW is oriented along the [110] direction of observation.*

Rotating the NW allows further investigations of the (111) Si twins, as illustrated in Figure 4.5. Moreover, a rotation between the crystals of the Al and Si segments is evident. Therefore, it is not possible to image the two families of {111} planes in both segments using the same STEM image. Consequently, a delicate rotation of the NW needs to be done. First, the observation is set to the Si [110] zone axis, consequently allowing the visualization of the Si lattice, which is defined as 0° rotation, as indicated in Figure 4.5(a). Considering the zoomed-in views [(1.1) and (1.2) in (a)] allows to analyze the crystal lattice of Si.

Next, the NW is rotated by 13.4° to the Al [110] zone axis, resulting in the visualization of the (111) Al planes, as shown in Figure 4.5(b). Notably, the Al-Si interface (indicated by the dashed blue line) is no longer clearly visualized because the edge moves on after rotation. It can be assumed that Al preferentially nucleates at the Si ⟨111⟩ boundary, giving a straight junction for twin-free NWs and a "V-shape" for twined interfaces. [58]

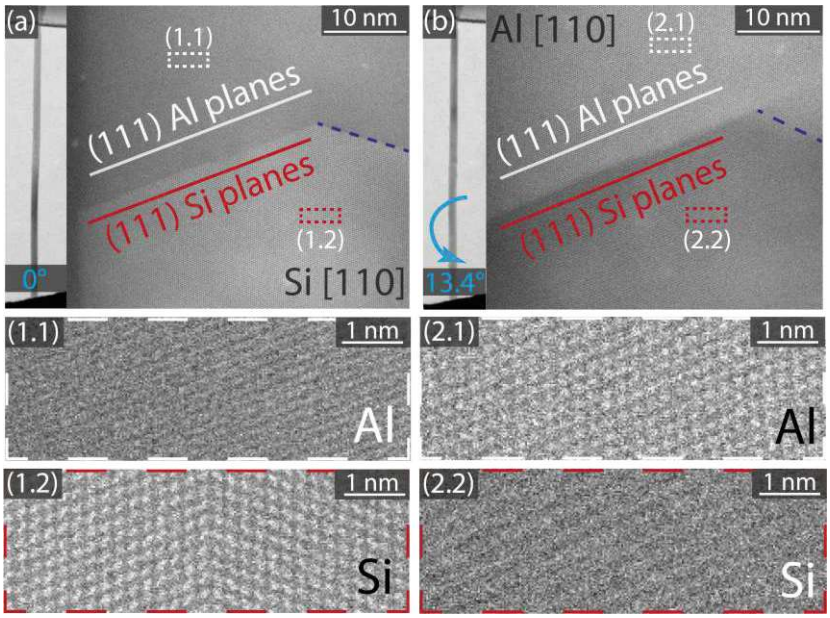


Figure 4.5: *(a) The left image shows a BF STEM image of the NW with* 0° *rotation. The HAADF STEM image on the right indicates the (111) Al and Si planes when the Si region is oriented on the [110] zone axis. The lower panel shows zoomed-in views of the Al and Si regions in this direction. (b) Next, the NW is rotated by* 13.4°*. Thus, observation in the Al [110] zone axis is illustrated in the HAADF STEM image, allowing to determine the crystal orientation of the Al. Using this direction of observation the crystallinity of Al is revealed as shown in the zoomed-in views.*

Regarding nanoelectronic device realizations, the "V-shaped" Al-Si nanojunction does not exhibit a significant drawback, as both facets have the same crystal orientation. Thus, in terms of the electronic properties, no interplay is expected. However, concerning top gate (TG) fabrication, the "V-shaped" interface needs to be taken into account, as for sufficient gating the complete MSJ needs to be covered (cf. Section 3.1).
As previously mentioned, Al is not used in FEOL due to stress-induced voiding and void nucleation via electromigration, [89, 283–285] or inter-diffusion, causing unwanted doping. [286] However, as the NW Al leads are single-crystalline, they may be more resilient to electromigration than poly-crystalline Al contacts. In the scope of device reliability, these concerns are important aspects to consider, which, however, are beyond the scope of the thesis at hand.

In summary, the presented Al-Si-Al NW heterostructure is the first reported single-elementary metal-Si junction, which provides abrupt and flat junctions. Moreover, in the investigated MSJs, no void-formation, spiking, or electromigration was detected in contrast to bulk. Further, regarding device integration, the Al-Si material system promises for symmetric effective SBHs, as further investigated in Section 4.2.1.

STEM and EDX analysis revealed **monolithic, single-elementary, and void-free Al-Si MSJs** based on intrinsic ⟨112⟩-oriented Si NWs. Notably after the solid-state exchange mechanism, **(111) Al and Si planes at the MSJ, as well as "V-shaped" (111) Si twin facets**, were identified.

4.1.2 Al-$Si_{0.5}Ge_{0.5}$ Heterojunction

In the scope of the thesis at hand, NWs with different $Si_{1-x}Ge_x$ compound ratios – $Si_{0.33}Ge_{0.67}$, $Si_{0.5}Ge_{0.5}$ and $Si_{0.7}Ge_{0.3}$ – are considered.[3] However, in terms of comparing the different Al-group IV based SBFETs, $Si_{0.5}Ge_{0.5}$ NWs are used throughout structural and electrical characterizations due to its alignment between Si and Ge. Note that in Section 4.2.2, further details in this respect are given.

The intrinsic $Si_{1-x}Ge_x$ NW growth was performed using the VLS method, facilitating silane and germane as precursors and Au as the catalyst. The thereof obtained nominally un-doped NWs exhibit a nominal $d_{NW} \approx 50\,nm$ and lengths $> 3\,\mu m$. Attributed to using a Si (111) substrate and selected catalyst particle size, the NWs are predominantly grown along the $\langle 111 \rangle$ direction. [265] Prior to the $Si_{0.5}Ge_{0.5}$ NW deposition on the 40 nm thick Si_3N_4 membrane chip, the NWs were passivated with a 10.5 nm thick ALD Al_2O_3 shell at $T = 474\,K$. Thus, providing a conformal coating of the NW core without potential Ge pile-up caused by thermal oxidation within the semiconductor NW (cf. Section 2.1.2). Finally, after the fabrication of the Al source/drain pads, the solid-state exchange reaction is initiated by RTA at $T = 773\,K$, leading to channel lengths $L_{SC} \approx 500\,nm$, as illustrated in Figure 4.6. The mean annealing rate of 33 Al-$Si_{0.5}Ge_{0.5}$-Al NW heterostructures on Si_3N_4 membranes was evaluated to be $(18 \pm 1)\,nm/s$, considering Al intrusion from both sides. Additionally, the annealing rate of 35 Al-$Si_{0.5}Ge_{0.5}$-Al NW heterostructures on "hexpads" was evaluated to be $(5 \pm 1)\,nm/s$, approximately a factor of three slower annealing rate compared to the exchange on the Si_3N_4 membrane chips. In this context, it is assumed that the higher thermal absorption of the "hexpad" causes slower annealing rates in comparison to the Si_3N_4 membranes with a low thermal capacity. Concerning the Al-$Si_{0.5}Ge_{0.5}$ MSJ, in comparison to the Al-Si or Al-Ge interface (cf. Section 4.1.1 and Section 4.1.3), no atomically abrupt interfaces are obtained, which may be related to poor surface quality. [164] Therefore, hindering the determination of a distinct crystal orientation as shown in Figure 4.6(b).

[3] The $Si_{1-x}Ge_x$ NW growth was performed by Dr. Bassem Salem at Université Grenoble Alpes CNRS, CEA/LETI Minatec, Grenoble INP, LTM, France.

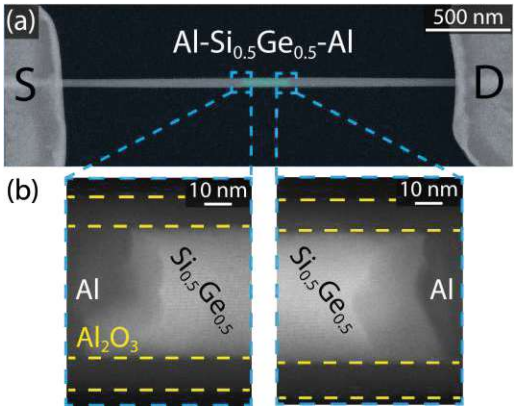


Figure 4.6: *(a) False-color SEM image of the investigated Al-$Si_{0.5}Ge_{0.5}$-Al NW heterostructure analyzed on the Si_3N_4 membrane chip. (b) HAADF STEM images of the two opposing Al-$Si_{0.5}Ge_{0.5}$ nanojunctions.*

For further clarification of the MSJ and its composition, EDX analysis is performed as illustrated in Figure 4.7, where Si, Ge, Al, and O markers are visualized. Note that a Si signal is also obtained outside the NW due to the underlying Si_3N_4 membrane. Previously published works on the Al-$Si_{1-x}Ge_x$ solid-state exchange mechanism proposed the formation of a Si-rich inter-layer between the Al- and $Si_{1-x}Ge_x$-segment. [164, 265] Importantly, setting this inter-layer formation into perspective to the topic of Fermi level pinning would allow an NW-integrable solution towards Fermi level re-pinning. Notably, the use of inter-layers to re-pin the Fermi level was proposed in other works also, however, on the basis of other materials, e.g., Tb or Si-nitrides. [184, 287] In particular, considering Al-group IV MSJs, a Si-rich interlayer would even promote close to mid-gap Fermi level pinning (cf. Section 2.2.2), desired for symmetric SBFET applications, e.g. RFETs. However, in all investigated Al-$Si_{1-x}Ge_x$ MSJs in the work at hand, no clear Si-rich layer was detected, which can be partly attributed to different $Si_{1-x}Ge_x$ compound ratios in comparison to the proposed $Si_{0.67}Ge_{0.33}$ in [164]. Furthermore, in the latter work NWs with a native oxide shell, consisting of an ~1 nm thick mixture of Al_2O_3 and SiO_2 in dependence of the lateral NW location, and NWs with a 20 nm thick ALD Al_2O_3 passivation layer were investigated. Thus, in combination with the different Si/Ge compound ratios, variances in the passivation shell, i.e., different surface diffusion, and differences in the RTA setup might cause the absence of the Si-rich inter-layer in the investigated NWs. Further, Conlan et al. merely achieved a Si-rich interlayer at one MSJ, whereas the other MSJ exhibited an Al-SiGe contact. [265] They attributed the non-existence of the inter-layer to differences at the NW surface.

Importantly, observing the overlay EDX map in Figure 4.7 reveals that no Si and Ge X-ray lines are present in the Al leads within the resolution limit of the STEM EDX setup. The visible Al signal on and at the NW originates from the 10.5 nm thick Al_2O_3 passivation shell.

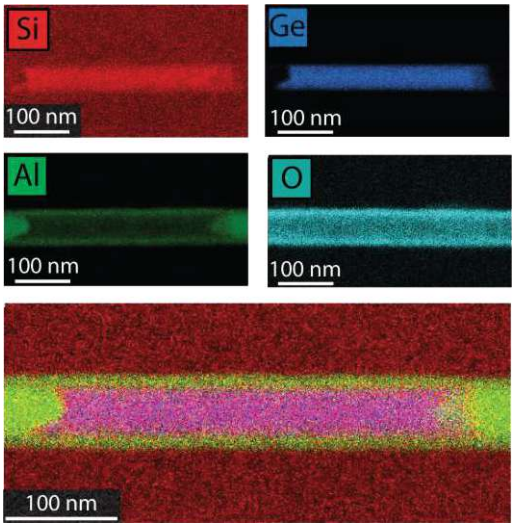


Figure 4.7: *EDX analysis of the corresponding Al-$Si_{0.5}Ge_{0.5}$-Al NW heterostructure analyzed in Figure 4.6. The bottom image shows an overlay of the considered materials. Attributed to the use of a Si_3N_4 membrane, a strong Si signal is extracted also outside the NW. In correspondence to Reference [164], no Si-rich inter-layer is evident in the investigated MSJs.*

Complementary to the non-flat MSJs of the Al-$Si_{0.5}Ge_{0.5}$-Al NW heterostructure, shown in Figure 4.6, additional EBIC investigations were carried out on a Al-$Si_{0.5}Ge_{0.5}$-Al NW heterostructure with $d_{NW} = 70\,nm$ and $L_{SC} = 840\,nm$. Therefore, following Figure 3.6, EBIC measurements with an e-beam acceleration voltage of 80 kV were conducted, as illustrated in Figure 4.8(b,c). Prior to the in-situ STEM EBIC investigations, an I/V characteristic, i.e., I_D vs. V_D with $V_S = 0\,V$ was acquired, as shown in Figure 4.8(a). Conducting a V_D sweep from $-1\,V$ to $1\,V$ allows to analyze the MSJ symmetry as charge carriers are injected from both MSJs in correspondence to the band bending. Thus, a $\Delta I_D = 7.8\,pA$ was evaluated, depicting the difference between the two MSJs. Consequently, also a difference in the EBIC is evident as shown in Figure 4.8(b,c), which, however, allows to determine the two opposing Schottky contacts with depletion widths of ~350 nm and ~320 nm for the source- and drain-sided MSJ, respectively. Consequently, in top gated SBFET applications, a MSJ overlap in the evaluated regime must be ensured for efficient gating. Further, the sign of the EBIC indicates that the metal induces an upward band bending in the semiconductor (cf. Section 2.2.2).

Considering a higher current at the source-sided MSJ, it can be concluded that the SBH exhibits lower values than the drain-sided MSJ. As no bias, i.e., $V_{\mathrm{D}} = V_{\mathrm{S}} = 0\,\mathrm{V}$ is applied, a positive and negative current contribution is induced. However, applying a bias would lead to a distinct EBIC peak at one of the MSJs in correspondence to the applied bias. [265] Moreover, it needs to be considered that these variations might also be caused by a difference in fixed oxide charges (Q_{f}).

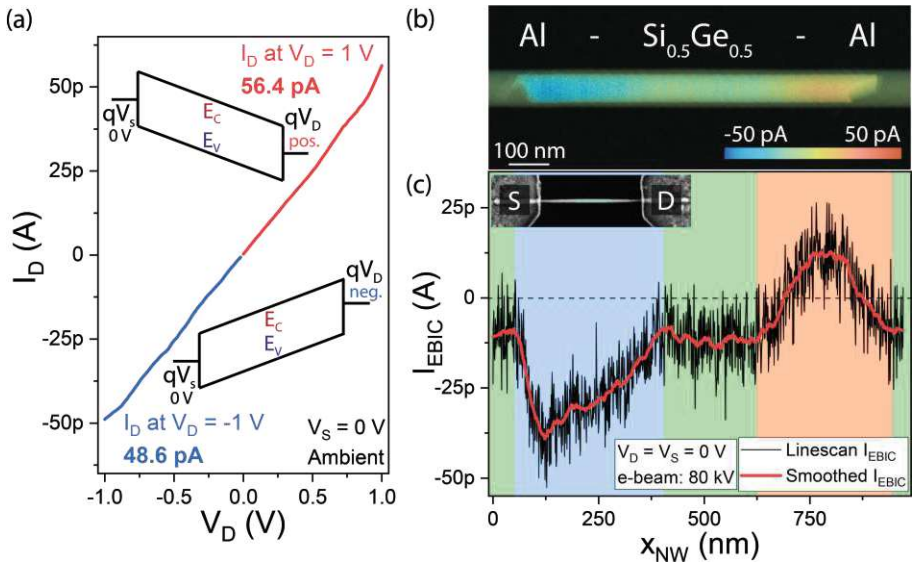


Figure 4.8: *(a) I/V characteristic of the proposed Al-$Si_{0.5}Ge_{0.5}$-Al NW heterostructure at ambient conditions. The insets illustrate the band diagrams at negative and positive V_{D}. (b) EBIC data of the Al-$Si_{0.5}Ge_{0.5}$-Al NW heterostructure, obtained by STEM and EBIC overlay. (c) EBIC linescan data is acquired by a horizontal scan on the NW. The left top inset shows the source/drain configuration.*

In conclusion, **Al-$Si_{0.5}Ge_{0.5}$ MSJs with single-elementary Al leads are obtained**, which, however, **do not exhibit flat interfaces**. Nevertheless, no inter-diffusion of the metal and semiconductor in the observed regimes was detected. Additional **EBIC investigations revealed relatively broad depletion regions in the range of** 300 nm, which needs to be considered for further top gated SBFET integration.

4.1.3 Al-Ge Heterojunction

As described previously, the Al-Ge material system has been thoroughly investigated and applied in the past. [59,77] However, due to the use of germane (GeH_4) precursors in most VLS-grown Ge NWs, challenges with the formation of native oxide Ge_xO_y arise. [31,288] In particular, Ge_xO_y exhibits a relatively high density of interface trap states (D_{it}) and is unreliable due to its water solubility (cf. Section 2.1.2). In this respect, advances to improve the Ge NW surface were driven by conformal deposition of high-κ passivation shells. In particular, ALD Al_2O_3 was exploited on Ge NWs, improving the transient stability of transistor characteristics by reducing D_{it} and preventing further oxidation of Ge. [259,262] Nevertheless, residual Ge_xO_y between the semiconductor/dielectric interface may impact the charge carrier transport, resulting from a relatively high D_{it}. Figure 4.9(a) shows a transfer characteristic of an intrinsic ⟨111⟩-oriented Ge NW grown with germane (GeH_4) as precursor, which is further integrated in an Al-Ge-Al NW top gated SBFET device. [4] In addition Figure 4.9(b) depicts a similar measurement, however, using an intrinsic ⟨111⟩-oriented Ge NW, which used diphenylgermane (DPG; $C_{12}H_{12}Ge$) as precursor.[5]

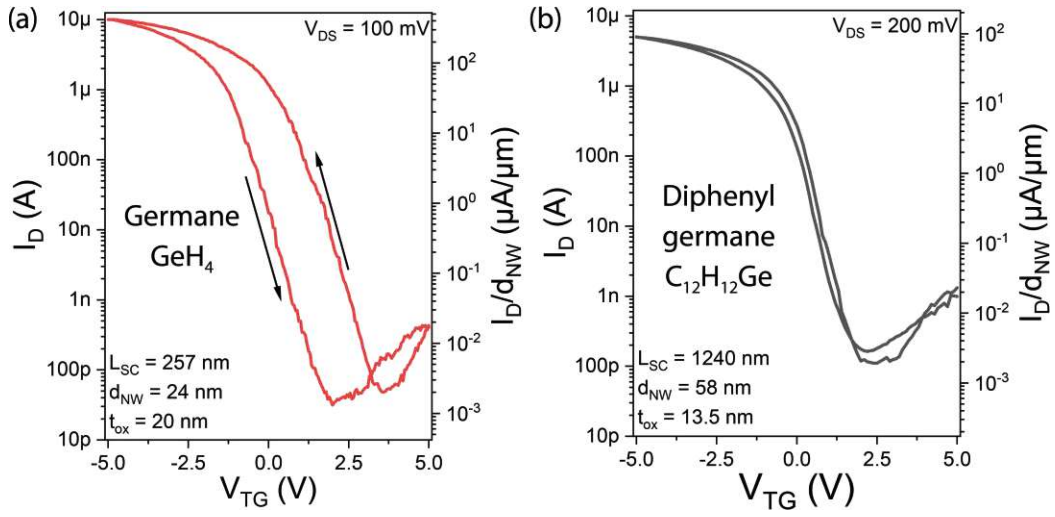


Figure 4.9: *Comparison of transfer characteristics of two intrinsic ⟨111⟩ oriented Al-Ge-Al NW heterostructures integrated in top gated SBFETs, where (a) a germane and (b) a diphenylgermane precursor is used for the Ge NW growth. Both SBFETs use ALD Al_2O_3 as gate dielectric, however with different t_{ox}. Importantly, a significant difference in the hysteresis is evident.*

[4] The Ge NW growth with the germane precursor was performed by Dr. Alois Lugstein at the Institute of Solid State Electronics, TU Wien, Austria.

[5] The Ge NW growth with the DPG precursor was performed by Dr. Sven Barth at the Physics Institute, Goethe Universität Frankfurt, Germany.

Comparing the two transfer characteristics in Figure 4.9 reveals a significant difference in the hysteresis, originating from a forward and consecutive backward V_{TG}-sweep. In this respect, at $I_D = 10\,nA$, a hysteresis of 1.75 V and 0.16 mV for the germane and DPG precursor was extracted, respectively. Consequently, the SBFET using the DPG precursor for the Ge NW growth exhibits a lower transient dependence compared to Ge NWs, that are grown with germane. For analyzing the root cause of the difference in hysteresis, further details regarding the Ge NW growth with DPG are discussed in the following:

The (DPG) Ge NWs were grown on (111) Ge single crystal substrates by low-pressure CVD in a cold-wall reactor. The substrates were placed on a graphite susceptor, and the temperature was adjusted by high-frequency heating. Before the use, the substrates were coated with a 1 nm thick Au film by sputtering. The Ge substrate was heated to 748 K under dynamic vacuum before DPG (40 mg DPG reservoir at 295 K; process pressure $<$ 10 mbar to 3 mbar) was introduced to the CVD chamber for 20 min to 30 min. The Au seeds act as catalytic sites for the precursor decomposition. DPG decomposition in the absence of the metal for substrate temperatures up to 774 K has not been observed, which prevents tapering of NWs in the investigated growth temperature window of 624 K to 774 K. Similar growth procedures using the same precursor under LPCVD conditions have been reported in the literature. [289, 290] After disconnecting the precursor supply and a 10 min waiting period, the substrates were cooled down to RT.
The stability of the synthesized Ge NWs against degradation, such as surface oxidation over time and the formation of reliable interfaces in post-growth processing, can be related to surface termination with phenyl ligands originating from the precursor. Similar effects have been described in the growth of Ge NWs using a co-feed of GeH_4 with GeH_3CH_3, leading to a reduced tapering tendency by surface termination with alkyl ligands. [291,292] While Ge-H remains reactive and cleaves under reduced pressure, the stability of the Ge-aryl bond passivates the NW surface. After the growth of the ~70 nm thick Ge NWs, they were conformally coated with 13.5 nm thick Al_2O_3 by ALD at a temperature of 474 K.
Attributed to the transient stability, the DPG-grown Ge NWs are used throughout the structural and electrical characterizations in the work at hand. However, to initiate the metal-semiconductor solid-state exchange reaction by RTA a temperature $T = 673\,K$ in H_2/N_2 atmosphere was applied, whereas for the germane-based Ge NWs the Al-Ge solid-state exchange a temperature $T = 623\,K$ was sufficient [293]. Further, 31 Al-Ge-Al DPG-based NW heterostructures exhibited a mean annealing rate of $(5 \pm 1)\,nm/s$ on "hexpads", considering Al intrusion from both sides. In this context, El Hajraoui et al. determined that the annealing rate of Al-Ge NWs is diameter-dependent and follows a parabolic behavior, with faster exchange rates for thinner NWs as a result of volume diffusion. [59] Figure 4.10 shows the thereof obtained MSJ using the DPG-based Ge NWs.

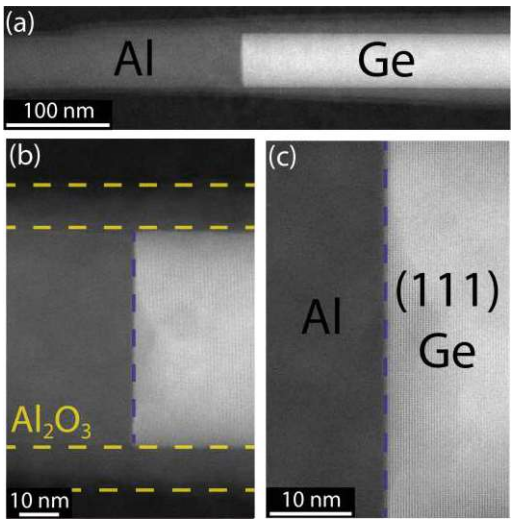


Figure 4.10: *(a) Overview of HAADF STEM image of an Al-Ge heterojunction with DPG-based Ge NWs. (b-c) Zoomed-in STEM images of the Al-Ge MSJ, wherein (b), the Al_2O_3 passivation layer is indicated. Moreover, a flat interface is obtained between Al and (111) Ge planes, corresponding to the crystal orientation of the Ge growth substrate.*

As evident in Figure 4.10, an abrupt and flat Al-Ge MSJ is revealed on the DPG-based Ge NWs, like on Ge NWs grown with a germane precursor. [59] Notably, (111) Ge planes in the Ge segment were identified, which are in correspondence with the ⟨111⟩ crystal orientation of the growth substrate. Moreover, conformal coating of the 13.5 nm thick Al_2O_3 passivation shell is verified in the observed NW segment. Further verifying the single-elementary nature of the obtained Al-Ge MSJ, an EDX analysis is performed, identifying potential metal-semiconductor inter-diffusion or inter-metallic phases. Therefore, Figure 4.11 shows Al, Ge, and O color maps reflecting the intensity of element-specific X-ray emission lines of the proposed MSJ.

Although DPG is used as a precursor, comparable structural properties are obtained compared to Ge NWs grown with germane. [59, 293] In this context, no residual Al or Ge atoms are evident in the observed NW regimes and within the resolution limit of the STEM EDX system. Attributed to the Al_2O_3 passivation shell, an Al and O signal is acquired around the NW core. Moreover, tapering of the NW towards the Al segment is observable, which might be caused by over-etching during the oxide removal.

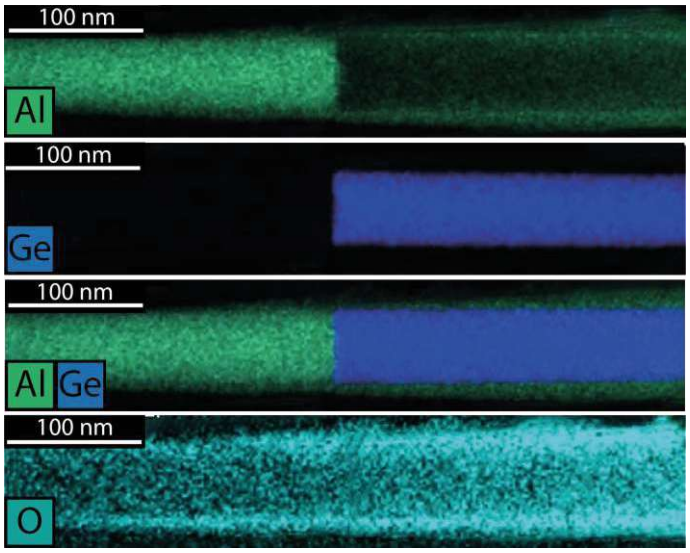


Figure 4.11: *EDX analysis of a DPG-based Al-Ge MSJ with indicated Al, Ge, and O markers. Considerably, no residual Al and Ge atoms are evident within the resolution limit of the STEM EDX system.*

In correspondence to previous investigations of Al-Ge NWs, similar results are obtained although DPG-based Ge NWs are used, which, however, promise more transiently stable transistors compared to germane-based Ge NWs. Notably, attributed to the intrinsic phenyl ligand surface passivation formed during synthesis the formation of native Ge_xO_y is hindered, thus enabling higher transient stability.

STEM and EDX analysis revealed **monolithic, single-elementary, and void-free Al-Ge MSJs** based on intrinsic ⟨111⟩-oriented Ge NWs. Notably, **using a diphenylgermane precursor for the Ge NW growth, an intrinsic phenyl ligand passivation harms the Ge_xO_y formation** and increases the transient stability of Ge-based NW electronics. Thus enabling further exploitation in the scope of nanoelectronics.

4.2 Electronic Transport in Al-Group IV SBFETs

After analyzing the proposed Al-group IV MSJs from a structural point of view and proving the formation of abrupt and single-crystalline MSJs with pure Al and group IV semiconductor channels, this section investigates the realized top gated SBFETs (cf. Section 3.1) from an electronic transport perspective.
Notably, using the same materials, except for the semiconductor NW and gate oxide, allows a comprehensive comparison of the underlying charge carrier injection and transport in the proposed Al-group IV based SBFETs. In this context, bias spectroscopy maps of I_{D}, g_{m} and E_{a} are used for a better understanding of transport mechanisms and operation regimes, which cannot be visualized by single I/V measurements. In the last step, Section 4.2.4 sets the extracted SBFET properties of the investigated material systems in relation to each other.

In this section, the publications "Understanding the Electronic Transport of Al-Si and Al-Ge Nanojunctions by Exploiting Temperature-Dependent Bias Spectroscopy" [RB3] (Al-Si and Al-Ge based SBFETs), "Mapping Electronic Transport in Ge Nanowire SBFETs: From Tunneling to NDR" [RB4] and "Thermionic Injection Assessment in Germanium Nanowire Schottky Junction FETs by Means of 1D and 3D Extraction Methods" [RB1] (Al-Ge based SBFETs) are covered.

4.2.1 Al-Si based SBFET

The properties of the obtained Al-Si MSJs are thoroughly discussed in Section 4.1.1 from a structural perspective. Moreover, considering the electronic Schottky properties of the Al-Si material system (cf. Section 2.2.2), similar n- and p-type SBs are expected, which is investigated in the following by using electrical characterization methodologies introduced in Section 3.2.2.

For the Al-Si based SBFETs, bottom-up grown intrinsic ⟨112⟩-oriented Si NWs integrated into a top gated SBFET architecture with Al source/drain contacts are considered. The proposed SBFETs have a channel length $L_{\mathrm{SC}} \approx 1\,\mu\mathrm{m}$ and a diameter $d_{\mathrm{NW}} \approx 70\,\mathrm{nm}$. Moreover, a 9 nm thick thermal SiO_2 shell, acting as gate dielectric, was grown by dry thermal oxidation. Note that the detailed fabrication process of SBFETs is discussed in Section 3.1, whereas the Al-Si material composition is thoroughly elaborated in Section 4.1.1. Figure 4.12 shows the thereof obtained material stack, which is further considered in the scope of the charge carrier transport investigations.

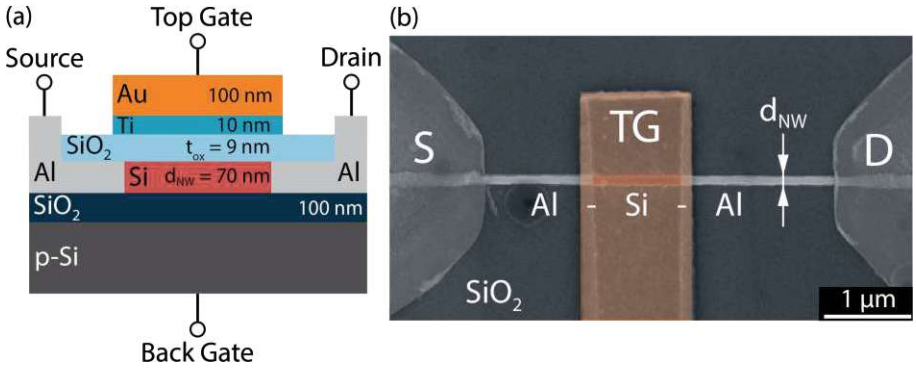


Figure 4.12: *(a) Material stack of an Al-Si based SBFET. Additionally, the electrode terminals are indicated. The Si channel length* $L_{\mathrm{SC}} = 1\,\mu\mathrm{m}$*. Note that the dimensions in the illustration are not in scale. (b) False-color SEM image of an investigated Al-Si based SBFET with indicated* d_{NW}*.*

As shown in Figure 4.12, using an Ω-shaped top gate (TG) covering the complete Si channel and Al-Si junctions harms influences of adsorbates on the transport and ensures sufficient electrostatic gating capabilities. [50] Note that the back gate electrode [cf. Figure 4.12(a)] is floating if not otherwise stated, i.e., no voltage is applied to the corresponding electrode. Notably, attributed to the Ω-shaped TG and the radial nature of the NW the TG dominates the electrostatic gating (cf. Figure A.8).

Transfer characteristics

As elaborated in Section 3.2.2, the transfer characteristics deliver important insights into understanding the involved transport phenomena and allow the extraction of essential transistor FOM. Therefore, Figure 4.13 shows transfer characteristics recorded at $T = 295\,\mathrm{K}$ by sweeping V_{TG} from $5\,\mathrm{V}$ to $-5\,\mathrm{V}$ and vice versa for different V_{DS} ranging from $0.25\,\mathrm{V}$ to $2\,\mathrm{V}$. A transfer characteristic of a back gated Al-Si SBFET is shown in Figure A.2. For better visibility only the forwards sweep from $5\,\mathrm{V}$ to $-5\,\mathrm{V}$ is visualized. Additionally, a symmetric biasing with $V_{\mathrm{D}} = -V_{\mathrm{S}}$ was applied, and therefore $V_{\mathrm{DS}} = V_{\mathrm{D}} - V_{\mathrm{S}}$ holds. Note that a detailed summary of the extracted values is given in Section 4.2.4, whereas in the following the phenomenological characteristics are discussed.

As expected from the Al-Si MSJ (cf. Section 2.2.1) a relatively symmetric behavior of the on-currents $I_{\mathrm{on}}^{\mathrm{n/p}}$ is evident, caused by the mid Fermi level pinning in relation to the Si band gap. [78] [RB2] Thus, resulting in an $I_{\mathrm{on}}^{\mathrm{n}}/I_{\mathrm{on}}^{\mathrm{p}}$ ratio of 0.65 at $V_{\mathrm{DS}} = 1\,\mathrm{V}$ without explicitly introducing measures to achieve symmetry like strain engineering [245]. Regarding the vertical shift of the transfer characteristics of $\sim -0.4\,\mathrm{V}$ from its vertical symmetry axis at $V_{\mathrm{TG}} = 0\,\mathrm{V}$, the history of the device as well as interface trap states need to be considered as discussed in Section 3.2.2.

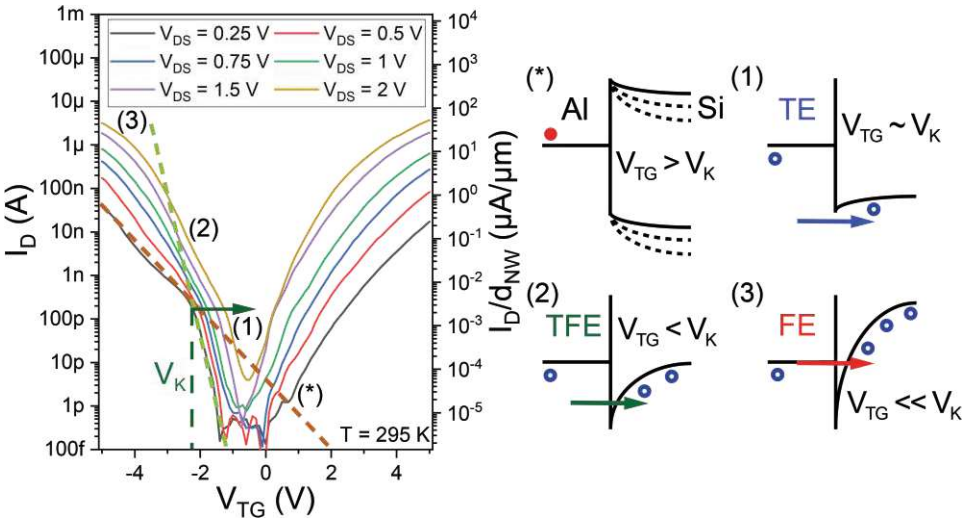


Figure 4.13: *Transfer characteristics of the Al-Si based SBFET illustrating the forwards sweep from* $V_{TG} = 5\,V$ *to* $-5\,V$ *at different* V_{DS} *ranging from* $0.25\,V$ *to* $1\,V$. *Measurements are acquired at* $T = 295\,K$. *(*) shows a simplified illustration at* $V_{TG} > V_K$ *in the electron dominant regime. The dotted lines depict an increase of* V_{TG} *leading to stronger band bending. (1-3) show simplified illustrations of the Al-Si MSJ and its associated injection mechanisms (here: holes) in dependence of* V_{TG}. *Additionally, the "kink" voltage* V_K, *where the transport changes from TE to TFE/FE is indicated in the I/V at* $V_{DS} = 0.25\,V$.

First, as shown in Figure 4.13(*) with $V_{TG} > V_K$ and being positive, thus operating the SBFET in n-type, leads to a downwards shift with increasing V_{TG} of the semiconductor's energy landscape. Another important characteristic, which becomes obvious in the p-branch ($V_{TG} < 0\,V$) of the transfer characteristic, is the presence of a "kink" at V_K, indicating a change of the inverse subthreshold slope $S = \Delta V_{TG}/\Delta \log_{10}(I_D)$. Further, considering the different injection mechanisms, i.e., TE and TFE/FE, labeled as (1-3) in Figure 4.13, allows to analyze the underlying mechanisms, leading to a change of S in the didactically marked regimes. First, as illustrated in (1), at $V_{TG} \approx V_K$, merely TE contributes to charge carrier injection, as charge carriers (here: holes) can only be injected by overcoming the SB due to weak band bending and insufficient SB thinning. Therefore, tunneling, i.e., FE, cannot contribute, as the barrier is too broad. However, increasing V_{TG} as shown in (2), and therefore inducing stronger band bending, results in a thinning of the SB and tunneling, i.e., TFE, contributes to the charge carrier transport. The transition between TE and TFE/FE gets then reflected by a shallower slope at V_K. [211] In Figure 4.13, the corresponding TE slope is indicated by the dashed light-green line, whereas the dashed brown line illustrates the slope in the TFE/FE dominant regime. Further, increasing V_{TG} allows an even more efficient tunneling contribution, leading to dominant FE of charge carriers, as illustrated in (3).

Moreover, FE leads to an increase in the number of charge carriers in the channel, which further enhances the band bending, favoring an even more efficient injection of charge carriers. [51] Notably, the TE to TFE/FE transition and the evidence of such a "kink" was already described by theoretical investigations in the past. [211,212] Further, Römer et al. investigated the discussed charge carrier injection and electrostatic gating in SBFETs on the basis of physics-based models. [202, 203] However, observing this "kink" in an experimental setup requires transiently stable Si NWs, attributed to a low interface trap state density at the Si/SiO_2 interface. Notably, in the *n*-branch, such a "kink" is not evident, which might be caused by different tunneling effective masses of electrons and holes and a slightly higher SBH for electrons (cf. Section 2.3.1).

Next, the V_{DS}-dependency on S, V_{th} and V_K, as illustrated in Figure 4.14 is analyzed. Investigating the inverse subthreshold slope S in the TE dominant regime of the *p*-branch [light-green symbols in Figure 4.14(a)] shows that S^p remains relatively constant at ~0.4 V/dec. Further, proving the injection of charge carriers via TE and showing that the device geometry does not suffer from short-channel effects, such as drain-induced barrier lowering. However, analyzing the TFE/FE slopes S^n in the *n*- and *p*-branch [red and blue symbols in Figure 4.14(a), respectively], shows a decrease from $S \approx 1.3\,V/dec$ at $V_{DS} = 0.25\,V$ to ~0.6 V/dec at $V_{DS} = 2\,V$. Thus demonstrating that V_{DS}-induced band bending leads to thinner SBs and more efficient injection of charge carriers. Additionally, the acceleration path of charge carriers increases due to a higher difference in the source/drain potentials. Analyzing the V_{DS}-dependency of V_{th} and V_K, as shown in Figure 4.14(b), reveals a decrease of $|V_{th}|$ when increasing V_{DS}. Additionally, V_K shifts from $-2\,V$ at $V_{DS} = 0.25\,V$ to $-1.1\,V$ at $V_{DS} = 2\,V$. In the same manner, as discussed previously, the stronger band bending, induced by an increased V_{DS} as well as a higher charge carrier concentration in the channel, leads to lower absolute V_{th} and V_K values.

It is expected that the electron and hole mobilities in the *n*- and *p*-branch may impact I_D and switching speeds. However, in the case of Si NWs with similar *n*- and *p*-type SBs, as evident for the Al-Si and $NiSi_2$-Si material system, and sufficiently short channel lengths the influence of the injection barrier defines the total electronic transport mechanism. Therefore, the SBs are further dominating over influences of the charge carrier mobility for channel lengths of 1 µm and shorter. [55]

For a fair comparison between the different Al-group IV material system SBFET FOM at $V_{DS} = 1\,V$ are considered, which are summarized and listed in Section 4.2.4. Nevertheless, as proposed in Section 3.2.4, single I/V sweep measurements do not reflect the complete transport and operation regimes. In particular, the T-dependency, which strongly affects TE is only partly covered. Therefore, in the next step, T-dependent bias spectroscopy is performed.

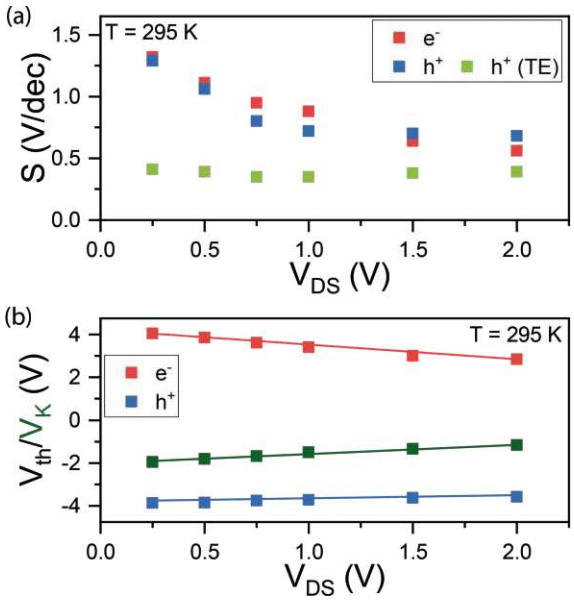


Figure 4.14: *V_{DS}-dependency of the Al-Si based SBFET on (a) Inverse subthreshold slope S of n- and p-type operation, where the S of holes in the TE regime remains relatively constant. (b) V_{th} and V_{K}, both decrease in absolute values with increasing V_{DS} due to stronger band bending, leading to a more efficient injection of charge carriers. The lines serve solely as visual guides. Data are extracted from Figure 4.13.*

Bias spectroscopy

As already introduced, bias spectroscopy is applied to the transfer characteristic in terms of its T-dependency. Moreover, the transconductance g_{m}, derived from transfer characteristics, is visualized by maps to cover its bias dependency.

Starting with T-dependent transfer maps of the Al-Si based SBFET at $V_{\mathrm{DS}} = 1\,\mathrm{V}$ over $T = 77.5\,\mathrm{K}$ to $400\,\mathrm{K}$, as shown in Figure 4.15, main transport regimes and their T-dependencies are visualized. Notably, as considered in the initial assumption, a relatively symmetric characteristic, with $V_{\mathrm{TG}} = 0\,\mathrm{V}$ being the vertical symmetry axis, is evident. Further supporting the relative mid-gap Fermi level pinning of the Al-Si material system. Importantly, as illustrated in the top inset of Figure 4.15, at $V_{\mathrm{TG}} = 0\,\mathrm{V}$, where merely TE contributes to charge carrier injection, distinct n- and p-type SBs are evident, which also gets reflected by its strong temperature dependency in the range of $V_{\mathrm{TG}} \approx -2\,\mathrm{V}$ to $2\,\mathrm{V}$. In this TE-dominant regime, increasing the temperature leads to a higher portion of charge carriers overcoming the SB, due to a higher degree of thermal excitation. Considering I_{D} in strong electron and hole accumulation, i.e., $|V_{\mathrm{TG}}| \approx 3.5\,\mathrm{V}$ to $5\,\mathrm{V}$, stable operation regimes over the investigated temperature regime are evident.

In this respect, due to strong band bending, which results in thinned SBs and dominant charge carrier injection via FE, the electronic transport shows a weak T-dependency. The T-independence of FE also gets reflected in the mathematical description of the FE-associated current, elaborated in Section 2.3.1.

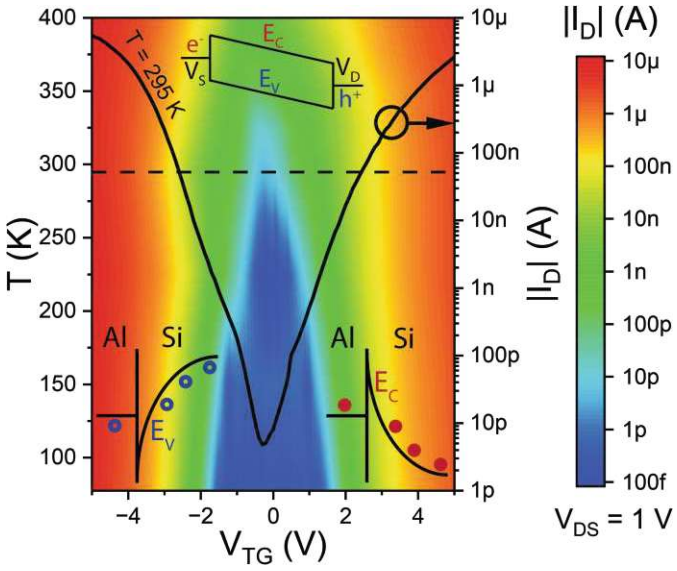


Figure 4.15: *T-dependent transfer characteristic map of the proposed Al-Si based SBFET at $V_{\mathrm{DS}} = 1\,\mathrm{V}$. The black curve shows the conventional transfer I/V data at $T = 295\,\mathrm{K}$, showing data of the horizontal dashed line. The upper inset shows the band diagram at $V_{\mathrm{TG}} = 0\,\mathrm{V}$ and $V_{\mathrm{DS}} > 0\,\mathrm{V}$. The lower insets show the Al-Si MSJ at $|V_{\mathrm{TG}}| = 5\,\mathrm{V}$.*

Next, the transconductance $g_{\mathrm{m}} = dI_{\mathrm{D}}/dV_{\mathrm{TG}}$ is derived and elaborated in terms of bias-dependent maps. Consequently, a qualitative measure of the inverse subthreshold slope and insight into the transport phenomena of the Al-Si material system is given. Figure 4.16 shows the g_{m} map extracted with V_{DS} ranging from 0.1 V to 2 V and also taking V_{TG} into account ranging from −5 V to 5 V. Note, that the temperature is kept constant at $T = 295\,\mathrm{K}$. Analyzing $|g_{\mathrm{m}}|$ in strong accumulation ($|V_{\mathrm{TG}}| = 5\,\mathrm{V}$) reveals two important characteristics. First, no dedicated $g_{\mathrm{m-max}}^{\mathrm{n/p}}$ can be extracted because the SBFET is not reaching saturation, which can be attributed to the non-optimized Si channel length and gate oxide dimensionality. In this context, stronger band bending, induced by applying higher V_{TG}, would be required for saturation. However, in the proposed SBFET design, the gate dielectric does not support higher voltages, which would lead to electrical breakdown. In this respect, device scaling and using different high-κ gate dielectrics might enable the operation of the SBFET in saturation.

Second, the g_m map reveals asymmetric values at $|V_{TG}| = 5\,V$, which correlates with the slopes in strong accumulation (cf. $V_{DS} = 1\,V$ in Figure 4.13). Nevertheless, due to the absence of a distinct g_{m-max}, a steady slope is evident, which is particularly crucial for specific applications, as e.g., amplifiers. [294]

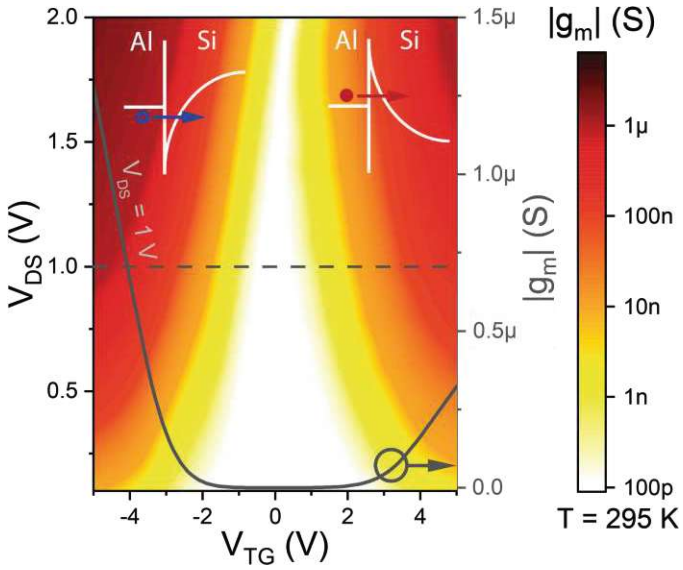


Figure 4.16: *V_{DS}-dependent map of g_m of the Al-Si based SBFET with V_{DS} ranging from 0.1 V to 2 V derived from transfer characteristics at $T = 295\,K$. The gray curve shows g_m data at $V_{DS} = 1\,V$ indicated by the dashed line. The two insets schematically illustrate the injection of electrons and holes.*

Notably, the T-dependent transfer characteristic map and bias-dependent transconductance map already reveal essential transport characteristics of the Al-Si based material system and allow the extraction of SBFET relevant FOM. In this respect, the low hysteresis is attributed to the high-quality, thermally grown SiO_2, which is also reflected by pulsed transfer characteristics, as shown in Figure A.3.

Analyzing the **transfer characteristic for different V_{DS} revealed a "kink" in the *p*-branch** of the Al-Si based SBFET, which **indicates the transition from TE to TFE/FE** in dependence of V_{TG} and the thereof induced band bending. **Using T-dependent bias spectroscopy** in terms of I_D and g_m maps, **allows to visualize the symmetric nature of the Al-Si based SBFET**, which is inhibited by single parameter sweeps only.

Output characteristics

As introduced in Section 3.2.2, the linear output characteristics, as depicted in Figure 4.17(a), allow the evaluation of the linearity and saturation properties of the underlying devices, whereas the logarithmic output characteristic maps shown in Figure 4.17(b) enable a didactic classification of the different injection mechanism, i.e., TE, FE, and TFE, in dependence of T and the applied biases. Thus, output maps at distinct temperatures, i.e., $T = 77.5\,\mathrm{K}$, $295\,\mathrm{K}$ and $400\,\mathrm{K}$, are illustrated, covering the temperature regime of interest. First, concerning the linear representations shown in Figure 4.17(a) of the output characteristics, a non-linear characteristic at low V_{DS} in the range between $-0.5\,\mathrm{V}$ and $0.5\,\mathrm{V}$ is evident, indicating distinct n- and p-type SBs because of the bias-tunable energy barriers at the junctions. [17] With respect to I_{D} it can be deduced that increasing the temperature also leads to an increase of I_{D}, which proves that TE is the dominating injection mechanism. Moreover, it can be deduced that a lower contact resistivity becomes evident for higher $|V_{\mathrm{TG}}|$ and higher T, which is further analyzed in Figure 4.17(b). Note that due to the symmetry of the Al-Si material system (cf. Figure 4.15) and for better visualization, only the I/Vs for $V_{\mathrm{TG}} = 0\,\mathrm{V}$ to $5\,\mathrm{V}$ are shown. Additionally, due to the limited V_{DS} (here: $V_{\mathrm{DS}} = -0.5\,\mathrm{V}$ to $0.5\,\mathrm{V}$), saturation is not reached due to an insufficiently high lateral electric field. Therefore, with respect to analyzing saturation, output characteristics with $|V_{\mathrm{DS}}|$ up to $2\,\mathrm{V}$ are compared for the different Al-group IV material systems in Section 4.2.4 (cf. Figure 4.39). Second, analyzing the output maps in Figure 4.17(b) shows that TE contribution steadily increases with increasing temperature because thermally excited charge carriers are overcoming the SBs. Next, FE, which is the injection contribution originating from the Fermi level of the metal into the semiconductor through direct tunneling, is discussed. Here, charge carriers have minimal potential energy but are efficiently injected at high biases (here: $|V_{\mathrm{DS}}| = 2\,\mathrm{V}$ and $|V_{\mathrm{TG}}| = 5\,\mathrm{V}$) due to strong band bending and thus thinned tunneling barriers. Therefore enabling an efficient and T-independent charge carrier injection (cf. Section 2.2.1). Moreover, the output maps in Figure 4.17(b) reveal a vertical ($V_{\mathrm{DS}} = 0\,\mathrm{V}$) and a horizontal ($V_{\mathrm{TG}} = 0\,\mathrm{V}$) symmetry axis, further promoting the symmetrical nature of the Al-Si material system. In particular, at $T = 77.5\,\mathrm{K}$, charge carrier transport is merely possible by TFE and FE, as a high portion of charge carriers are frozen-out and are therefore not able to overcome the SB due to a lack of thermal excitation.

Having output I/V data over the considered temperature range (here: $77.5\,\mathrm{K}$ to $400\,\mathrm{K}$) further allows to extract an activation energy E_{a}, which depicts the minimal required energy to inject charge carriers into the semiconductor. In this context, similar $E_{\mathrm{a}}^{\mathrm{n/p}}$ for the injection of electrons and holes are expected, corresponding to the symmetry between the n- and p-branch.

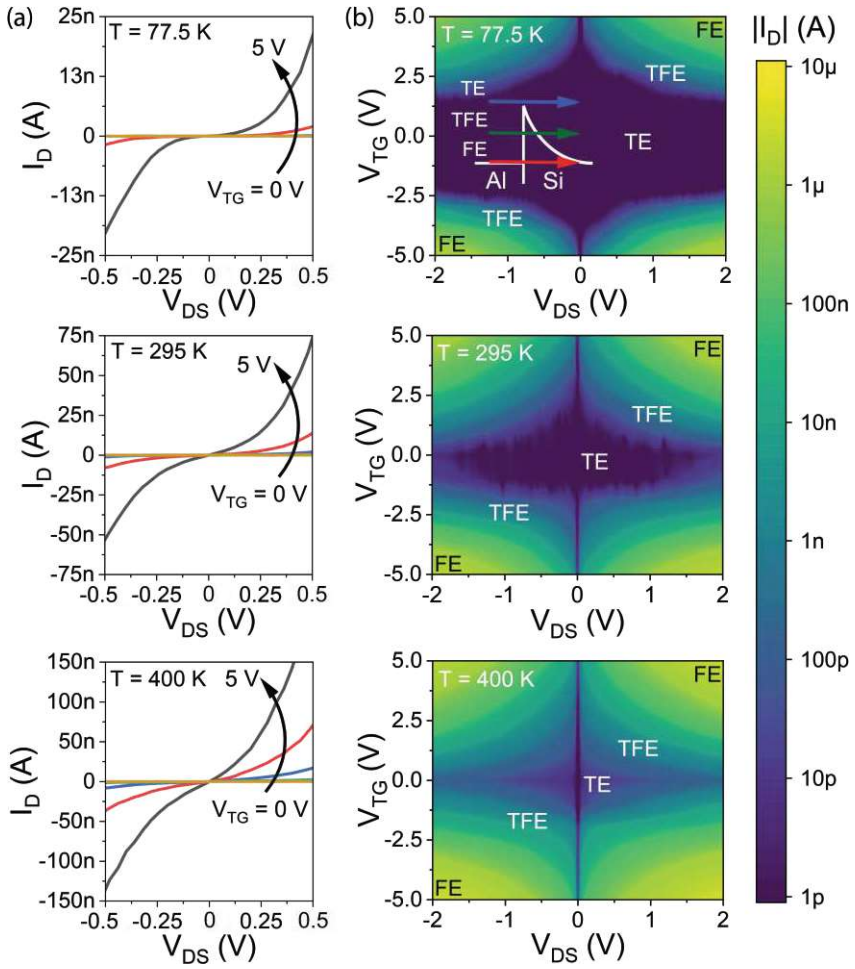


Figure 4.17: *Analysis of output characteristics of the Al-Si based SBFET for* $T = 77.5\,\mathrm{K}$, $295\,\mathrm{K}$ *and* $400\,\mathrm{K}$. *(a) Linear representation of output I/Vs in the n-branch (*$V_{\mathrm{TG}} = 0\,\mathrm{V}$ *to* $5\,\mathrm{V}$ *in* $1\,\mathrm{V}$ *steps). In the low* V_{DS}*-regime (*$V_{\mathrm{DS}} = -0.5\,\mathrm{V}$ *to* $0.5\,\mathrm{V}$*), where TE dominates, a non-linear characteristic is evident, indicating a distinct SB. (b) Output maps in dependence of* V_{TG}*. Additionally, TE, TFE, and FE regimes are didactically indicated as dominating mechanisms. The inset in the* $77.5\,\mathrm{K}$ *map illustrates the injection mechanisms for electrons.*

Using bias spectroscopy in terms of output characteristic maps, **allows to visualize distinct operation regimes**. In this respect, a **non-linear output characteristic** was evaluated, indicating **distinct *n*- and *p*-type SBs**.

Activation energy E_a

Additional processing of the output I/V data shown in Figure 4.17 allows for investigations of the activation energy E_a, as elaborated in Section 2.3.2 and Section 3.2.3. Using the discussed 3D TE model for the extraction allows to obtain V_{TG}-dependent activation energies as illustrated in Figure 4.18(a). Further, applying a linear fit in the TE dominant regime ($-2\,V < V_{TG} < 2\,V$), enables the extraction of intrinsic activation energies $E_a^{n/p}$ and flat-band voltages $V_{FB}^{n/p}$. Remarkably, adding the n- and p-type E_a values reveals a value of 540 meV, which is close to $E_g(Si)/2 = 560\,meV$. Notably, depicting a strong indication of mid-gap Fermi level pinning to the Si band gap. Furthermore, the relation to the Si band gap also becomes evident at the off-point (V_{TG}~0 V), which exhibits a mean value also close to $E_g(Si)/2$. Thus further promoting the mid-gap Fermi level pinning to the Si band gap exhibited by the Al-Si material system. Additionally, in terms of the flat-band voltages the same absolute $|V_{FB}| = 2\,V$ is extracted for the injection of electrons and holes. As briefly introduced in Section 3.2.3, without fitting to $V_{DS} = 0\,V$, an E_a map in dependence on V_{TG} and V_{DS} can be created as shown in Figure 4.18(b). Note that in Figure 4.18(b) the off-point is at $V_{TG} = 1\,V$ due to the consideration of taking V_{TG} and V_{DS} into account for the extraction of E_a, whereas in Figure 4.18(a) the interpolation to $V_{DS} = 0\,V$ is applied (cf. Section 3.2.3). Importantly, the Al-Si based SBFET exhibits positive and similar E_a values for both electron and hole injection. Here, the vertical symmetry axis at $V_{TG} \approx 1\,V$ is evident, which shows again values close to $E_g(Si)/2$. However, increasing V_{TG}, and therefore inducing stronger band bending, thins the tunneling barriers and a more efficient injection of charge carriers is achieved by FE, resulting in an E_a in the 10 meV-regime. In the corresponding E_a map the regimes are accordingly indicated using the relation to k_BT.

Evaluating $E_a^{n/p}$, corresponding to "effective" n- and p-type SBHs, reveal similar energies required to inject electrons and holes respectively. **Adding the intrinsic E_a^n and E_a^p** reveal **values close to E_g(Si)/2**, indicating **similar barriers for electron and hole injection**.

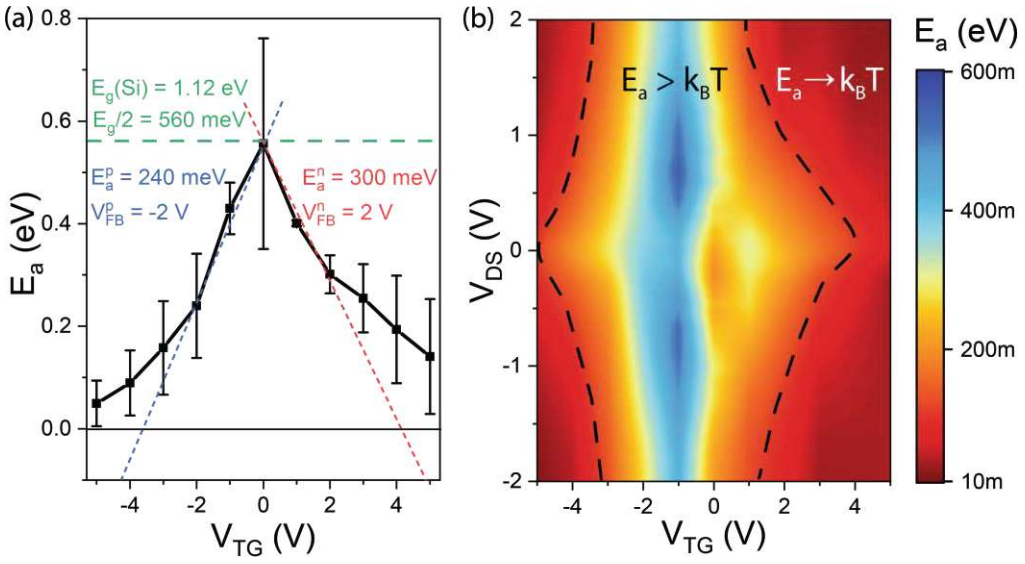


Figure 4.18: *Extraction of the activation energy E_a using the 3D TE model. (a) V_TG-dependent E_a of three similar Al-Si based SBFETs. Additionally, $E_\mathrm{a}^{\mathrm{n/p}}$ and $V_\mathrm{FB}^{\mathrm{n/p}}$ are extracted in the TE-dominant regime. (b) E_a map extracted from output characteristics of a representative Al-Si based SBFET. The highlighted regimes indicate a distinct SB ($E_\mathrm{a} > k_\mathrm{B}T$), whereas for $|V_{TG}| > 0\,\mathrm{V}$, E_a approaches values of $k_\mathrm{B}T$.*

4.2.2 Al-$Si_{0.5}Ge_{0.5}$ based SBFET

In the following, Al-$Si_{1-x}Ge_x$ based SBFETs are investigated, whereas for the detailed elaboration on the electronic transport Al-$Si_{0.5}Ge_{0.5}$ based SBFETs are considered (cf. Section 4.1.2). Therefore, bottom-up grown, nominally un-doped ⟨111⟩-oriented $Si_{0.33}Ge_{0.67}$, $Si_{0.5}Ge_{0.5}$ and $Si_{0.7}Ge_{0.3}$ NWs integrated in a top gated SBFET architecture are used. The thereof realized SBFETs have nominal channel lengths $L_{SC} \approx 1\,\mu m$ and diameters $d_{NW} \approx 50\,nm$. As gate dielectric a 10.5 nm thick ALD Al_2O_3 shell was deposited. Details regarding the structural properties of the Al-$Si_{0.5}Ge_{0.5}$ MSJ are discussed in Section 4.1.2. Figure 4.19 shows the material stack and a false-color SEM image of an Al-$Si_{0.5}Ge_{0.5}$ based SBFET with indicated gate and source/drain electrodes. Note that in all electrical measurements, the BG electrode was kept floating if not otherwise stated.

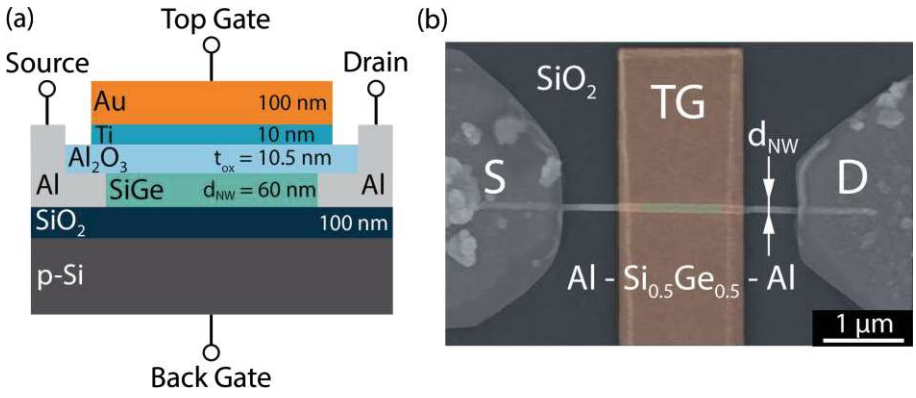


Figure 4.19: *(a) Material stack of the Al-$Si_{1-x}Ge_x$ based SBFET. Additionally, the electrode terminals are indicated. In the following $Si_{0.5}Ge_{0.5}$ is investigated with a channel length L_{SC} = 1.1 µm. Note that the dimensions in the illustration are not in scale. (b) False-color SEM image of an investigated Al-$Si_{0.5}Ge_{0.5}$ based SBFET.*

For comparison of the different $Si_{1-x}Ge_x$ compound ratios, the same top gated SBFET architecture, as shown in Figure 4.19, using $Si_{0.33}Ge_{0.67}$, $Si_{0.5}Ge_{0.5}$ and $Si_{0.7}Ge_{0.3}$ as channel material, was used. Therefore, allowing a fair identification of characteristic differences in dependence of the Si/Ge ratio.

Transfer characteristics

As mentioned, $Si_{0.33}Ge_{0.67}$, $Si_{0.5}Ge_{0.5}$ and $Si_{0.7}Ge_{0.3}$ NWs acting as semiconductor channel material were investigated in a first step. Therefore, Figure 4.20 shows transfer characteristics of the different Al-$Si_{1-x}Ge_x$ based SBFETs, where for a fair comparison the conductivity $\sigma = (I_D/V_{DS}) \cdot (L_{SC}/A_{NW})$, with $A_{NW} = d_{NW}^2/4 \cdot \pi$, is used instead of I_D, taking the individual channel lengths and diameters into account.

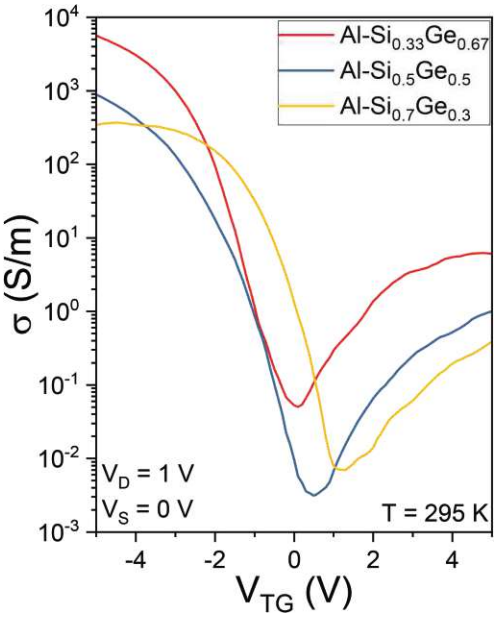


Figure 4.20: *Transfer characteristic comparison, expressed in terms of conductivity σ, of $Si_{0.33}Ge_{0.67}$, $Si_{0.5}Ge_{0.5}$ and $Si_{0.7}Ge_{0.3}$ NW channels integrated in individual top gated SBFETs. Note that for a comprehensive comparison the conductivity σ is used instead of the current I_D.*

In comparison to the Al-Si based SBFET discussed in Section 4.2.1, the $Si_{1-x}Ge_x$ based SBFETs show a much weaker *n*-type characteristic (cf. $V_{TG} > 0\,V$). Therefore, the Ge content needs to be considered, which causes dominant Fermi level pinning close to the valence band as evident in Al-Ge MSJs (cf. Section 2.2.2). Further, the on- and off-currents (here conductivities σ) of the individual Si/Ge compound ratios clearly depict the influence of Ge: Increasing the Ge content shifts the transfer characteristic horizontally to higher absolute values, which is attributed to the smaller band gap as well as lower E_a^p for higher Ge concentration. In this context, the higher source/drain leakage current, i.e., I_{off} at $V_{TG} = 0\,V$, is essentially affected. Analyzing the steepest inverse subthreshold slopes S in the *p*-branch of the individual SBFETs reveals a degradation from 0.35 V/dec of the $Si_{0.33}Ge_{0.67}$ to 0.6 V/dec of the $Si_{0.7}Ge_{0.3}$ indicating dominant *p*-type conduction for increased Ge-content. Notably, $S^n > 1\,V/dec$ in contrast further demonstrates weak electron conduction.
In terms of detailed charge carrier transport characteristics, the $Si_{0.5}Ge_{0.5}$ NWs were used because the on-currents $I_{on}^{n/p}$ lay in-between the two other compound ratios and also fit well to the pure Si and Ge NW channels integrated into the same SBFET architecture.

Applying the same characterization methodology as for the Al-Si based SBFET (cf. Section 4.2.1), Figure 4.21 shows V_{DS}-dependent transfer characteristics at $T = 295\,K$ of the Al-$Si_{0.5}Ge_{0.5}$ based SBFET. Hence, V_{DS} was gradually increased from 0.25 V to 2 V. Again, for better visualization, only the forwards sweep direction is illustrated.

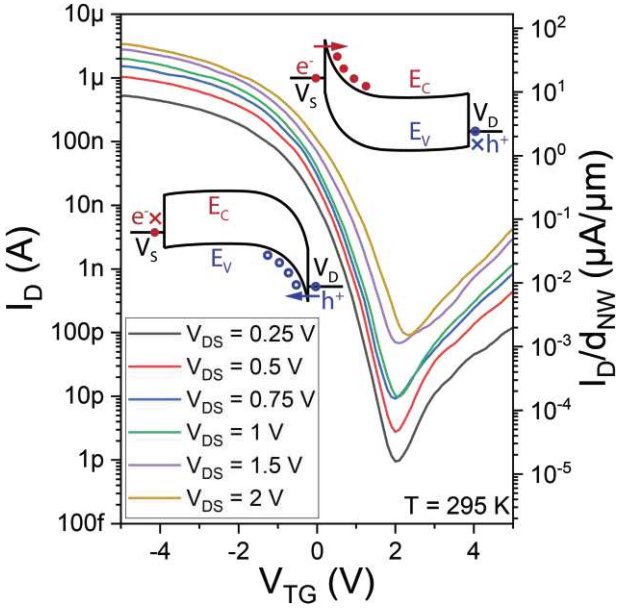


Figure 4.21: *Transfer characteristics of an Al-$Si_{0.5}Ge_{0.5}$ based SBFET illustrating the forwards sweep from $V_{TG} = 5\,V$ to $-5\,V$ at different V_{DS} ranging from 0.25 V to 2 V. Measurements are acquired at $T = 295\,K$. The left and right insets show the corresponding band diagrams for hole and electron injection, respectively.*

Regarding the location of I_{off} in respect to V_{TG}, an offset of ~2 V is evident, which might be caused by using Al_2O_3 as gate dielectric. In this respect, residual Ge_xO_y constituting an Al_2O_3/Ge_xO_y interface further promotes a shift towards a more dominant *p*-type characteristic (cf. Section 2.1.1). [259] Attributed to the shift, remarkably high *p*-type on-currents are achieved, highlighting the use of $Si_{1-x}Ge_x$ as channel material for *p*-type transistors. [295] Further, investigating the V_{DS}-dependent inverse subthreshold slopes $S^{n/p}$ and threshold voltages $V_{th}^{n/p}$ in the corresponding electron and hole regimes, reveals no explicit V_{DS} dependency, as illustrated in Figure 4.22. Notably, the V_{DS} independence on the S and V_{th} depicts a vital feature of the Al-$Si_{0.5}Ge_{0.5}$ based SBFET, as it allows a versatile application in circuits. Note that SBFET FOM at $V_{DS} = 1\,V$ are summarized in Section 4.2.4.

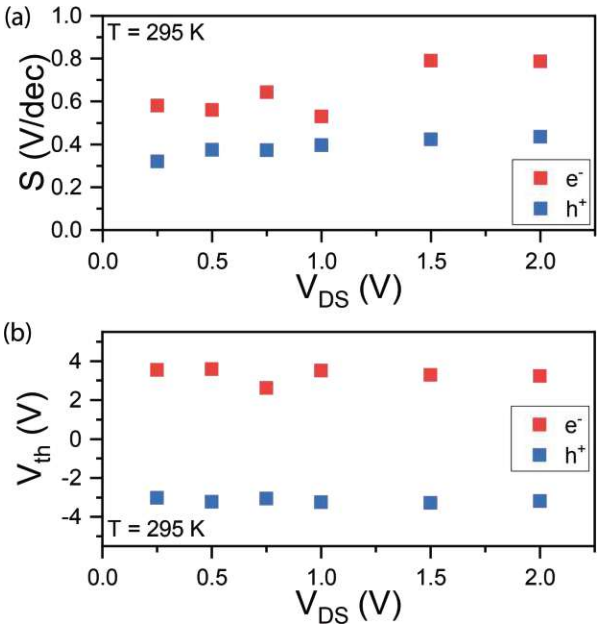


Figure 4.22: *Extraction of the V_{DS}-dependent (a) inverse subthreshold slopes $S^{\mathrm{n/p}}$ and (b) threshold voltages $V_{\mathrm{th}}^{\mathrm{n/p}}$ for electron and hole conduction of an Al-$Si_{0.5}Ge_{0.5}$ based SBFET.*

In the next step, bias spectroscopy is used to analyze the T-dependency and to investigate the different transport mechanisms as well as transport regimes. Therefore, the same methodology as proposed in Section 4.2.1 for the Al-Si based SBFET is used.

Bias spectroscopy

For the analysis of the T-dependent transport mechanisms of the proposed Al-$Si_{0.5}Ge_{0.5}$ based SBFET, a T-dependent transfer map, as shown in Figure 4.23 is used. The temperature range of $T = 77.5\,\mathrm{K}$ to $400\,\mathrm{K}$ is considered and a source/drain bias $V_{\mathrm{DS}} = 1\,\mathrm{V}$ is applied. Analyzing the temperature influence on I_{D} reveals that from $T \approx 77.5\,\mathrm{K}$ to $295\,\mathrm{K}$ in the p-branch ($V_{\mathrm{TG}} < 0\,\mathrm{V}$) a steady slope with ~$20\,\mathrm{mV/K}$ towards lower V_{TG} with increasing the temperature is visible. In other words, considering $I_{\mathrm{D}} \approx 100\,\mathrm{nA}$, at $T = 77.5\,\mathrm{K}$ a $V_{\mathrm{TG}} \approx -4.25\,\mathrm{V}$ is required, whereas at $T = 295\,\mathrm{K}$ a V_{TG} of ~ $-0.25\,\mathrm{V}$ is required. Thus, indicating a distinct p-type SB for temperatures up to $T = 295\,\mathrm{K}$. However, further increasing the temperature to $400\,\mathrm{K}$ shows that the T-dependency diminishes, indicating efficient charge carrier injection caused by a high portion of thermally excited charge carriers overcoming the SB. In this regime, it is assumed that FE is not dominating due to weak band bending ($V_{\mathrm{TG}} \approx 0.1\,\mathrm{V}$) and a broad SB width. The corresponding behavior is indicated by gray-dashed lines in Figure 4.23.

However, considering the transmission probability $T(E)$ elaborated in Section 2.3.1 indicates that $T(E)$ is approaching unity and therefore leading to the observed T-independent behavior in the temperature range from 295 K to 400 K. In regard to the off-state, a strong T-dependency over V_{TG} is evident, which can again be attributed to a more pronounced Fermi level pinning closer to the valence band of $Si_{0.5}Ge_{0.5}$ and in general a smaller band gap than of Si (cf. Table 2.1). In this context, the same temperature dependency with ~20 mV/K is evident, supporting the presence of distinct n- and p-type SBs.
Attributed to a weak n-type conduction ($V_{TG} > 0$ V), I_D slightly increases for increasing the temperature, as charge carriers can only overcome the n-type SB with sufficiently high thermal excitation.

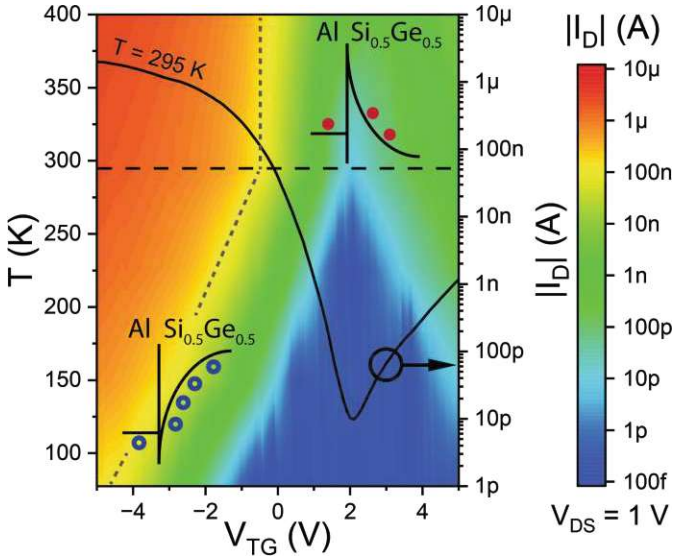


Figure 4.23: *T-dependent transfer characteristic map of the proposed Al-$Si_{0.5}Ge_{0.5}$ based SBFET at $V_{DS} = 1$ V. The black curve shows the conventional transfer I/V data at $T = 295$ K, indicating data of the horizontal dashed line. The gray-dashed lines illustrate the T-dependency in the corresponding temperature regimes. The lower left and top right insets illustrate the MSJ for hole and electron injection, respectively.*

Next, the transconductance g_m is visualized by means of bias spectroscopy considering $T = 295$ K and varying V_{DS} in the range of 0.1 V to 2 V over $V_{TG} = -5$ V to 5 V. As shown in Figure 4.24, the transconductance in the p-branch does not show a steady slope towards strong hole accumulation, but exhibits a degradation of g_m^p. In this context, such degradation and a distinct g_{m-max} is typically visible in SBFETs with distinct SBs at specific bias conditions. [296] In general, explaining g_m-degradation requires to distinguish between the junction and channel resistance.

Importantly, in the proposed Al-$Si_{0.5}Ge_{0.5}$ based SBFET at $T = 295\,\mathrm{K}$ a high portion of holes are efficiently injected into the semiconductor, as discussed previously. Further allowing to conclude that the channel resistance with predominant phonon scattering is the main resistance contributor for the proposed operation regime. Notably, the described mechanism was also proposed for CNT-based SBFETs. [297] Besides phonon scattering, also surface scattering caused by a high degree of surface roughness was determined to be responsible for g_m-degradation. [296] Attributed to the relatively higher n-type SB, merely $g_\mathrm{m}^\mathrm{n} = 2.6\,\mathrm{nS}$ at $V_\mathrm{TG} = 5\,\mathrm{V}$ is extracted. In respect to $g_{\mathrm{m-max}}^\mathrm{n}$ no saturation or degradation is evident, resulting in a similar g_m characteristic as evident for the Al-Si based SBFET.

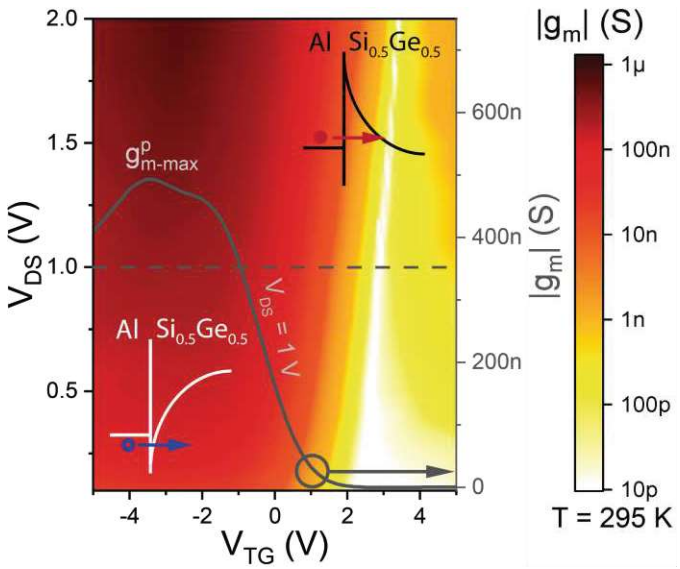


Figure 4.24: *V_DS-dependent map of g_m with V_DS ranging from 0.1 V to 2 V derived from transfer characteristics at $T = 295\,\mathrm{K}$ of the Al-$Si_{0.5}Ge_{0.5}$ based SBFET. The gray curve shows g_m data at $V_\mathrm{DS} = 1\,\mathrm{V}$ indicated by the horizontal dashed line. The two insets illustrate the injection of electrons and holes, respectively.*

The transfer characteristics of the **Al-$Si_{0.5}Ge_{0.5}$ based SBFET shows a predominant *p*-type characteristic**, attributed to **Fermi level pinning closer to the valence band of $Si_{0.5}Ge_{0.5}$**, originating from the incorporated Ge. Using T-dependent bias spectroscopy **reveals a strong T-dependency of the *p*-branch in the range of** 77.5 K **to** 295 K**, whereas from T** = 295 K **to** 400 K**, merely a weak T-dependency is evident**. Analyzing g_m, revealed a degradation in the p-branch with a distinct $g_{\mathrm{m-max}}^\mathrm{p}$.

Output characteristics

Figure 4.25 shows linear output characteristics and maps for distinct temperatures T = 77.5 K, 295 K and 400 K. Concerning the linear output characteristics for $V_{TG} = 0\,V$ to $-5\,V$, shown in Figure 4.25(a) at $T = 77.5\,K$ a strong non-linearity is observed, indicating the dominant existence of a distinct p-type SB. However, further increasing the temperature shows that the output I/V curves are becoming linear, indicating a quasi-ohmic contact between Al and $Si_{0.5}Ge_{0.5}$ for the injection of holes. Moreover, I_D increases with elevated temperatures, which is attributed to a higher thermal excitation of charge carriers overcoming the p-type SB. Note that output characteristics for $|V_{DS}|$ up to 2 V, allowing to investigate the saturation properties, are shown in Section 4.2.4. Analyzing the output maps in Figure 4.25(b) shows that, again, the TE-dominant regime certainly evident at $V_{TG} > 0\,V$, exhibits a strong T-dependency. Thus indicating that electrons experience a distinct SB over the complete investigated temperature range. Furthermore, increasing V_{TG} or V_{DS} does not lead to sufficient band bending due to a too broad n-type SB, preventing direct tunneling. Concerning, the p-type characteristic at $V_{TG} < 0\,V$, efficient injection of holes merely gets evident at $T = 295\,K$ and remains T-independent for temperatures up to 400 K, as discussed previously. In terms of symmetry and in contrast to the Al-Si based SBFET output characteristics, merely a vertical symmetry axis at $V_{DS} = 0\,V$ is evident, due to weak n-type conduction, attributed to Fermi level pinning closer to the valence band of $Si_{0.5}Ge_{0.5}$.

The T-dependency in the p-branch is further highlighted in the output characteristics, where the **linear I/V data at 295 K to 400 K demonstrate quasi-ohmic junction properties**. In the temperature regime from **77.5 K to 295 K a non-linear output I/V is evident, indicating a distinct *p*-type SB**.

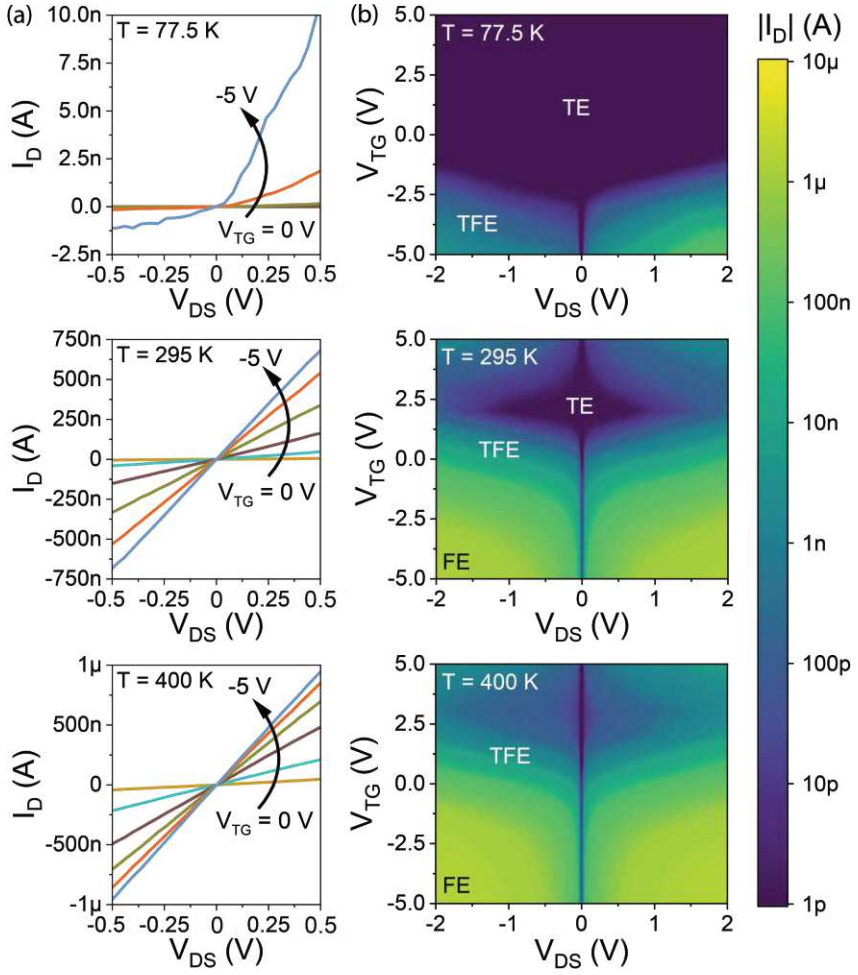


Figure 4.25: *Analysis of output characteristics of the Al-$Si_{0.5}Ge_{0.5}$ based SBFET. (a) Linear representation of output I/Vs in the p-branch ($V_{\mathrm{TG}} = 0\,\mathrm{V}$ to $-5\,\mathrm{V}$ in $1\,\mathrm{V}$ steps). In the low V_{DS}-regime ($-0.5\,\mathrm{V}$ to $0.5\,\mathrm{V}$), where TE dominates, the non-linear characteristic at $77.5\,\mathrm{K}$ becomes linear for increased temperatures (here: $295\,\mathrm{K}$ and $400\,\mathrm{K}$). Thus, a quasi-ohmic contact for the injection of holes is established for $T > 295\,\mathrm{K}$. (b) Output characteristic maps in dependence of V_{TG} at $T = 77.5\,\mathrm{K}, 295\,\mathrm{K}$ and $400\,\mathrm{K}$. Additionally, TE, TFE, and FE regimes are didactically indicated, where the FE regime corresponds to $T(E) \approx 1$.*

Activation energy E_a

As depicted in Figure 4.26, the activation energy E_a is extracted in the same manner as for the Al-Si based SBFET, using the 3D TE model. Figure 4.26(a) shows the V_{TG}-dependent activation energies, where again, the intrinsic $E_a^{n/p}$ and $V_{FB}^{n/p}$ are indicated in the TE-dominant regime. In respect to the intrinsic activation energies, the sum of the n- and p-type E_a results in a value of 301 meV, indicating a lower band gap than evident in the Al-Si material system with 540 meV (cf. Section 4.2.1). In this context, the Ge-content, due to the Ge's smaller band gap, causes the decrease of both n- and p-type E_a. Remarkably, and as already shown in the previously discussed measurements, a low ($E_a^p \approx k_B T$) and even negative E_a^p value is extracted in strong hole accumulation. Notably, due to the closer Fermi level pinning to the valence band of the Al-$Si_{0.5}Ge_{0.5}$ junction and strong band bending ($V_{TG} < -3$ V), resulting in thinned SBs and an efficient tunneling contribution. Further supporting the statement of quasi-ohmic contacts for holes in the Al-$Si_{0.5}Ge_{0.5}$ material system. In this context, negative activation energies were also shown in CNTs with Pd contacts also claiming quasi-ohmic injection of charge carriers [298] as well as in n-type Si contacted by Ti and in reverse-biased Ni-Ge SB diodes [72,188]. In contrast for the injection of electrons in strong accumulation, a positive $E_a > 100$ meV remains for $V_{TG} > 1$ V. A more detailed discussion and possible reasons, leading to negative E_a values will be discussed in Section 4.2.3. Concerning Figure 4.26(b) the V_{DS}-independent injection mechanism gets highlighted in strong hole accumulation ($V_{TG} < -3.5$ V), as no significant change of E_a can be indicated. In contrast, where TE dominates ($E_a > k_B T$) a V_{DS}- and V_{TG}-dependency becomes evident, as shown in Figure 4.26(b).

E_a^p reveals negative values in strong hole accumulation, associated with the quasi-ohmic nature of the Al-$Si_{0.5}Ge_{0.5}$ junction for $T =$ 295 K to 400 K. In contrast, **E_a^n remains positive** in the n-branch.

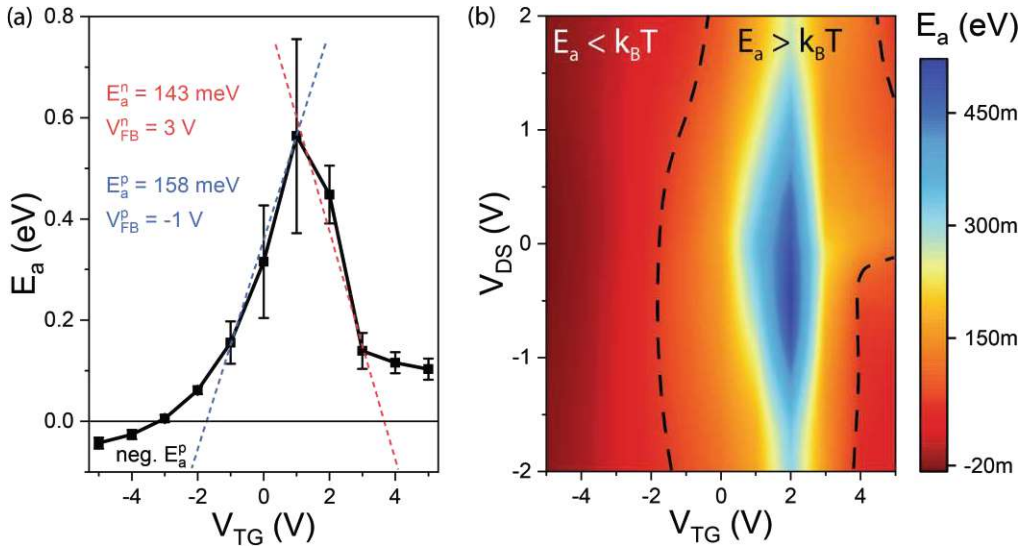


Figure 4.26: *Extraction of the activation energy E_a using the 3D TE model. (a) V_TG-dependent E_a of four similar Al-$Si_{0.5}Ge_{0.5}$ based SBFETs. Additionally, $E_\mathrm{a}^\mathrm{n/p}$ and $V_\mathrm{FB}^\mathrm{n/p}$ are extracted in the TE dominant regime. (b) E_a map extracted from output characteristics of a representative Al-$Si_{0.5}Ge_{0.5}$ based SBFET. The highlighted regimes indicate a distinct SB ($E_\mathrm{a} > k_\mathrm{B}T$) and quasi-ohmic Schottky junctions ($E_\mathrm{a} < k_\mathrm{B}T$).*

4.2.3 Al-Ge based SBFET

As discussed in Section 4.1.3, bottom-up grown intrinsic ⟨111⟩-oriented Ge NWs were used for the realization of the pure Ge based SBFETs. In this respect, the technological breakthrough allowing a thorough investigation of bottom-up grown Ge NWs is the use of DPG as a growth precursor, enabling the incorporation of an intrinsic phenyl ligand surface passivation during synthesis. [290] Therefore, achieving sufficient transient stability for its application in SBFETs. Figure 4.27 illustrates the used material stack and the integration of the proposed Ge NWs into a top gated SBFET architecture. Here, $L_{SC} = 1\,\mu m$ and $d_{NW} = 53\,nm$. In respect to d_{NW}, the Bohr radius of Ge ($a_B^* = 24.3\,nm$) needs to be taken into account, which dimensionality is in the order of the used Ge NW's diameter. In particular, for the evaluation of an activation energy E_a, this relation is considered by also applying the 1D Landauer-Büttiker (LB) theory for its extraction (cf. Section 2.3.2). As gate dielectric a 13.5 nm thick ALD Al_2O_3 is used.

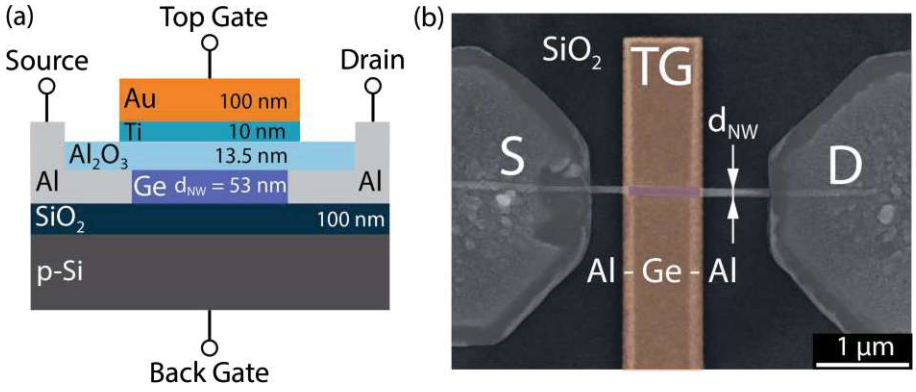


Figure 4.27: *(a) Material stack of an Al-Ge based SBFET. Additionally, the electrode terminals are indicated. The Ge NW channel length $L_{SC} = 1\,\mu m$. Note that the dimensions in the illustration are not in scale. (b) False-color SEM image of a representative Al-Ge based SBFET.*

In the same manner, as in the previous Al-group IV based SBFET investigations, the BG electrode was kept floating, if not otherwise stated. Attributed to the dominance of the Ω-shaped TG, the electrostatic gating from the BG can be neglected, as illustrated in Figure A.8.

Transfer characteristics

For the extraction of SBFET-related FOM the transfer characteristics in dependence on V_{DS} are analyzed, as shown in Figure 4.28. Therefore, different V_{DS} ranging from 0.25 V to 2 V at $T = 295$ K are considered, whereas V_{TG} is swept from 5 V to −5 V and vice-versa. Again, only the forward sweep is shown for better visualization. Moreover and equal to the other investigated material systems, $V_D = -V_S$ and $V_{DS} = V_D - V_S$.

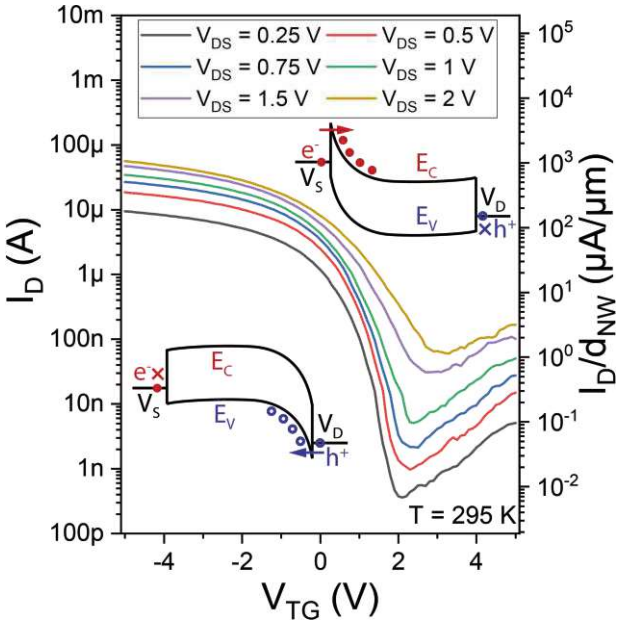


Figure 4.28: *Transfer characteristics illustrating the forwards sweep from $V_{TG} = 5$ V to -5 V at different V_{DS} ranging from 0.25 V to 2 V. Measurements are acquired at $T = 295$ K. The left and right insets show the corresponding band diagrams for hole and electron injection, respectively.*

As it already became evident in the Al-$Si_{1-x}Ge_x$ based SBFET, a predominant *p*-type conduction occurs in the Al-Ge based SBFET, which is even more enhanced due to the use of pure Ge as channel material. Attributed to strong Fermi level pinning close to the valence band of the Ge band gap, merely a weak *n*-type conduction is observable (cf. Section 2.2.2). [78] In this context, a quasi-ohmic contact for hole injection is expected over the complete investigated temperature operation regime. In general, the on- and off-currents (I_D) exhibit higher values, in comparison to the other Al-group IV based SBFETs, due to a smaller band gap of Ge with $E_g(\mathrm{Ge}) = 0.66$ eV. Thus leading to an enhanced injection of charge carriers via TE compared to the Si-containing channel materials. Again, due to the use of Al_2O_3, fixed charges lead to a vertical shift of the transfer characteristic, which correlates with the Al-$Si_{0.5}Ge_{0.5}$ based SBFET (cf. Section 4.2.2).

Attributed to a relatively high source/drain leakage current, the ”kink”, indicating the transition from TE to TFE/FE, is not clearly visible in the I/V data compared to the Al-Si based SBFET (cf. Section 4.2.1).

Analyzing the inverse subthreshold slopes $S^{n/p}$ of the Al-Ge based SBFET, as shown in Figure 4.29(a), an increase of S at higher V_{DS} becomes evident, due to a higher portion of charge carriers being injected by FE. Moreover, a dominant asymmetry between $S^{n/p}$ is evident, which indicates different injection capabilities of electrons and holes. Notably, this characteristic is also visible in the V_{DS}-dependent threshold voltages $V_{th}^{n/p}$ shown in Figure 4.29(b), where the n-branch exhibits significantly higher values compared to the p-branch. Note that V_{th}^{n} is further increased due to the vertical shift of the transfer characteristic. Nevertheless, at $V_{DS} = 1.5\,V$ and $2\,V$ a contrary behavior between electron and hole transport becomes evident. Concerning n-type operation, a decrease of V_{th} is observable due to an increased portion of charge carriers being injected via FE, whereas in the p-branch V_{th}^{p} remains relatively constant over the observed regime, further indicating quasi-ohmic junctions for hole injection.

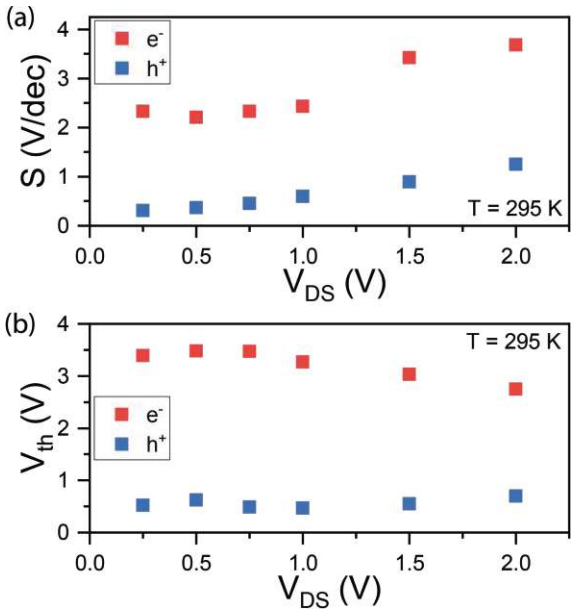


Figure 4.29: *Extraction of the V_{DS}-dependent (a) inverse subthreshold slopes $S^{n/p}$ and (b) threshold voltages $V_{th}^{n/p}$ for electron and hole conduction of an Al-Ge based SBFET.*

In a next step, Figure 4.30(a) shows conventional T-dependent transfer characteristics at $V_{DS} = 1\,V$. Due to the dominance of the p-branch, specific aspects in the hole conduction regime are considered in the following. Attributed to an effective charge carrier freeze-out at $T = 77.5\,K$ an I_{on}^{p}/I_{off} of more than eight orders of magnitude is evident. Further, upon heating, I_{off} is significantly increasing from 70 fA at $T = 77.5\,K$, which is the noise floor of the used measurement equipment, to 30 nA at 400 K. Thus depicting an increase of six orders of magnitude higher charge carrier concentration in the channel, reducing S^{p} significantly, as shown in Figure 4.30(b). Furthermore, this leads to a shift of the threshold voltage V_{th}^{p} as illustrated in Figure 4.30(c). Concerning the on-current I_{on}^{p} in the respective p-type regime [cf. inset in Figure 4.30(a)], up to RT I_D increases due to a higher thermal excitation of charge carriers overcoming the SB. However, further increasing the temperature leads to a decrease of I_{on}^{p}, which indicates that the junction resistance of the SB becomes less significant in comparison to the Ge channel resistance. Thus, I_{on}^{p} changes from 33 µA at $T = 225\,K$ to 24 µA at $T = 400\,K$. In this context, phonon scattering is assumed to be the dominant mechanism in the semiconductor channel contributing to the total resistance. [299] Moreover, the observed temperature dependency in the p-type regime is a strong indicator for a thinned SB with a high tunneling probability and thus constituting a quasi-ohmic, i.e., highly transparent junction for the injection of holes.
In contrast, I_{on}^{n} of the n-branch shows a steady increase from 10 pA at $T = 77.5\,K$ to 80 nA at $T = 400\,K$, indicating a distinct SB for electrons. Thus, TE-limited injection with the contact resistance being the dominant contributor to the total resistance is expected.

In terms of the hysteresis, and in particular considering the use of DPG, transfer characteristics acquired under V_{TG}-pulsed conditions exhibited remarkably low hysteresis values over the investigated temperature regime (cf. Figure A.9).

In comparison to the Al-$Si_{1-x}Ge_x$ based SBFET, the **predominant *p*-type characteristic is even more enhanced in the Al-Ge material system**, due to **strong Fermi level pinning close to the valence band of Ge**. Notably, **quasi-ohmic contacts for the injection of holes** are evident in the temperature regime between 77.5 K and 400 K. In the relatively weak n-branch, TE dominates the characteristic.

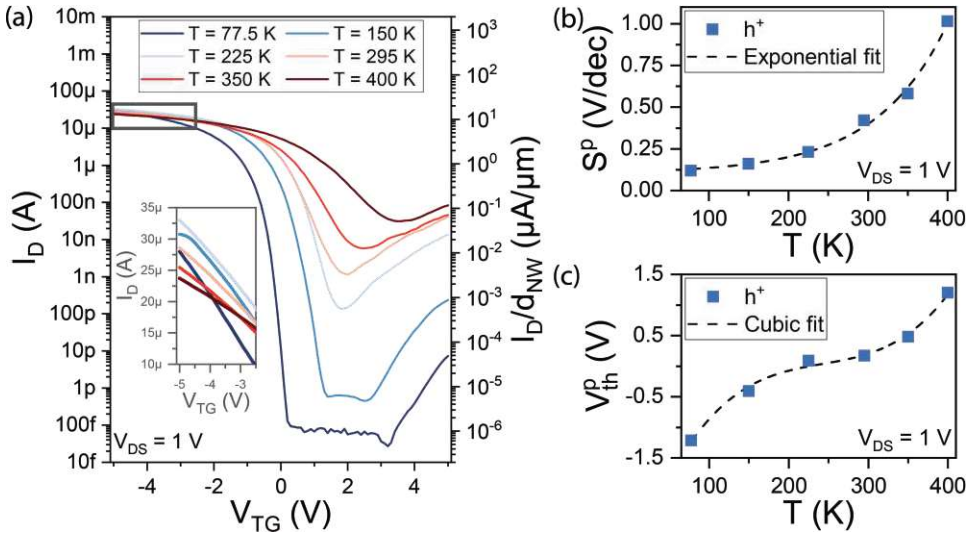


Figure 4.30: *(a) T-dependent transfer characteristics for temperatures ranging from* 77.5 K *to* 400 K*. The inset shows the temperature dependency on* I^{p}_{on} *in strong hole accumulation (*V_{TG} = −5 V *to* −2.5 V*). T-dependency of (b)* S^p *and of (c)* V^p_{th} *for hole conduction showing an exponential and cubic fit, respectively.*

Bias spectroscopy

Attributed to the used DPG precursor for the growth of the proposed Ge NWs, transiently stable SBFETs are obtained, allowing investigations by means of bias spectroscopy. Therefore, Figure 4.31 shows the T-dependent transfer map of the Al-Ge based SBFET at V_{DS} = 1 V in the temperature range of 77.5 K to 400 K. In correspondence to Figure 4.30(a), a strong temperature dependency in the n-branch becomes evident due to the reduced band gap of Ge in comparison to Si or $Si_{0.5}Ge_{0.5}$ as well as dominant Fermi level pinning close to the valence band of Ge. Notably, in the p-branch a relatively T-stable I_D is visible, attributed to an efficient injection of charge carriers (here: holes), resulting from the quasi-ohmic contact properties of the Al-Ge junction. Similarly to the Al-$Si_{0.5}Ge_{0.5}$, a slope of ~7 mV/K becomes evident between the two regimes. Notably, exhibiting a significantly weaker T-dependency in comparison to the Al-$Si_{0.5}Ge_{0.5}$ material system (~20 mV/K), due to a more enhanced Fermi level pinning close to the valence band of Ge. In general, this indicates two distinctly different injection capabilities for electrons and holes.

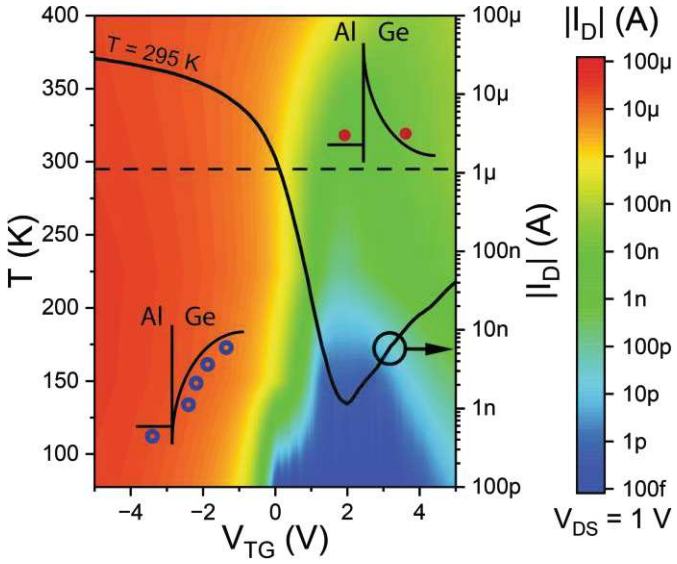


Figure 4.31: *T-dependent transfer characteristic map of the proposed Al-Ge based SBFET at* $V_{\mathrm{DS}} = 1\,\mathrm{V}$. *The black curve shows the conventional transfer I/V data at* $T = 295\,\mathrm{K}$, *illustrating data of the horizontal dashed line. The low right and top left insets schematically depict the MSJ for hole and electron injection, respectively.*

Next, as illustrated in Figure 4.32 the bias-dependent transconductance g_{m} map at $T = 295\,\mathrm{K}$ is analyzed. Attributed to the pure Ge channel, again, a degradation in the p-branch is evident, which results from the dominance of the channel resistance and its associated phonon scattering for the injection and transport of holes. [297] Thus, depicting a significant identification of a quasi-ohmic contact at $T = 295\,\mathrm{K}$. In particular, increasing V_{DS} and further thinning the SB leads to a significant $g_{\mathrm{m}}^{\mathrm{p}}$ degradation. Attributed to the weak n-type characteristic, occurring in consequence of a relatively high n-type SB, $g_{\mathrm{m}}^{\mathrm{n}}$ merely reaches a value of 2.6 nS at $V_{\mathrm{TG}} = 5\,\mathrm{V}$. In general, higher g_{m} values are reached in the p-branch of the Al-Ge SBFET (~2.4 µS at $V_{\mathrm{TG}} = -5\,\mathrm{V}$) compared to the Al-Si based SBFET with a value of 1.3 µS at the same bias conditions.

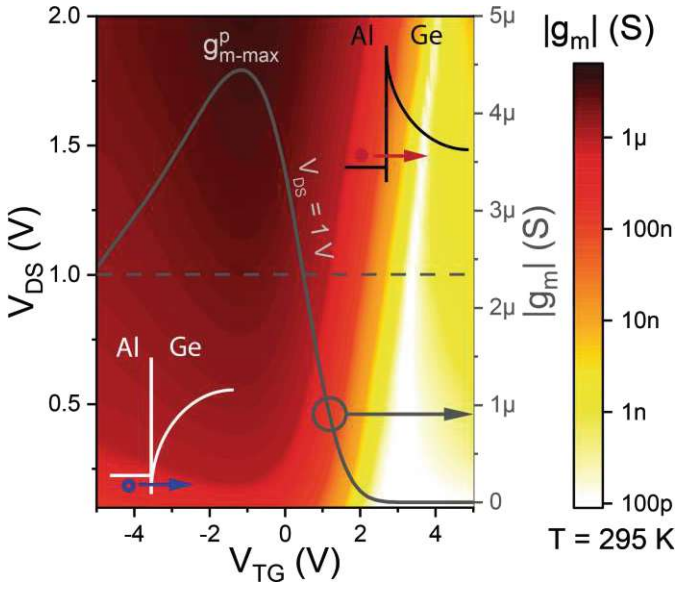


Figure 4.32: *V_{DS}-dependent map of g_m with V_{DS} ranging from 0.1 V to 2 V derived from transfer characteristics at $T = 295$ K of the Al-Ge based SBFET. The gray curve shows g_m data at $V_{DS} = 1$ V indicated by the horizontal dashed line. The two insets illustrate the injection of electrons and holes, respectively.*

Further investigating the assumption of quasi-ohmic contacts, the g_m degradation in strong hole accumulation is analyzed by a T-dependent g_m map, as shown in Figure 4.33. Remarkably, in the proposed Al-Ge based SBFET, the degradation appears to be bias- and T-independent in case of strong hole accumulation. This is contrary to other SBFET realizations with distinct SBs, where g_m, except for applying high V_{DS}, is continuously enhanced for an increasing V_{TG}. [300] Therefore, besides phonon scattering, a saturation of hole injection due to strong Fermi level pinning close to the valence band of Ge appears to be a dominant factor. Moreover, it becomes evident, that g^p_{m-max} becomes lower with increased temperatures, which can be attributed to a decreasing scattering mean free path, i.e., reduced phonon scattering at lower temperatures. Notably, the decrease of g^p_{m-max} follows a quadratic increase with increasing temperature, as illustrated in the inset of Figure 4.33.

Investigating the **transconductance g_m by means of bias spectroscopy showed a degradation and the exhibition of a g^p_{m-max} in strong hole accumulation**. This effect can be attributed to the **quasi-ohmic contact properties** over the investigated temperature range of 77.5 K to 400 K.

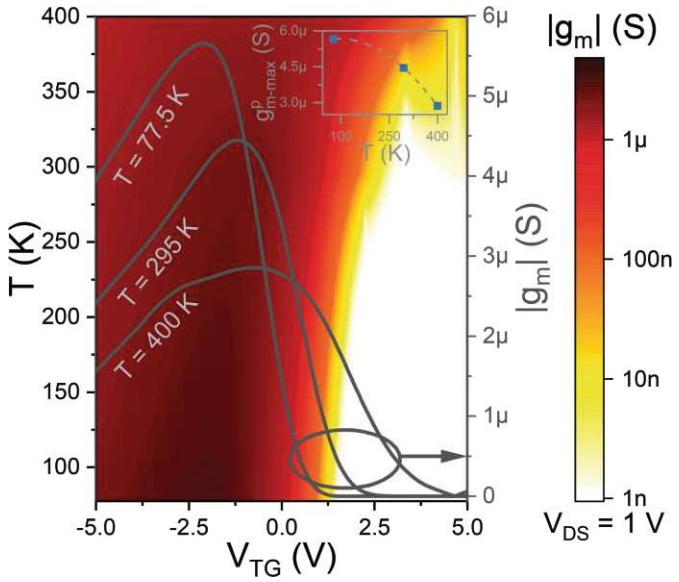


Figure 4.33: *T-dependent map of g_m with temperatures ranging from 77.5 K to 400 K at V_DS = 1 V. Additionally, g_m data at T = 77.5 K, 295 K and 400 K are shown. The top right inset depicts a quadratic decrease of $g^\mathrm{p}_{\mathrm{m-max}}$ for increased temperatures.*

Output characteristics

Assessing the different injection mechanisms, linear output characteristics, and maps at T = 77.5 K, 295 K and 400 K, are used, as illustrated in Figure 4.34. For the acquisition of the data, $V_\mathrm{DS} = -2$ V to 2 V and $V_\mathrm{TG} = -5$ V to 5 V sweeps are considered. With respect to the determination of quasi-ohmic contacts, the linear output characteristics shown in Figure 4.34(a) provide an essential indication of the proposed transparency of the junction. Notably, over the considered T-range, a purely linear I/V characteristic in the low V_DS range of -0.5 V to 0.5 V becomes evident, which strongly indicates a quasi-ohmic junction and allows the assumption of a non-existent SB for the injection of holes over the investigated temperature range. Correlating to the T-dependent transfer characteristics, shown in Figure 4.30, I_D decreases for increasing the temperature, which is associated with the dominance of the Ge channel's resistance. For the analysis of the saturation properties, output characteristics for $|V_\mathrm{DS}|$ ranging up to 2 V are discussed in Section 4.2.4.
Analyzing the output maps, illustrated in Figure 4.34(b), allows to distinguish between two cases associated with electron and hole injection. First, in the n-branch at $V_\mathrm{TG} > 0$ V, where a distinct SB is evident, the junction resistance dominates the total resistance. Thus, TE limits the overall transport. Second, as evident for the injection of holes at $V_\mathrm{TG} < 0$ V, where a quasi-ohmic and transparent junction is evident, FE limits the transport. Consequently, the different transport regimes, TE, TFE, and FE, can be didactically determined.

Comparing the output maps of the selected temperatures shows that a T-increase from RT to 400 K leads to a strong I_D increase in the TE regime, whereas in the TFE and FE regimes, I_D remains relatively stable. In relation to the described n- and p-type SBs, the observed characteristic correlates well, as the n-type SB is substantially higher than for holes and therefore shows a significant T-dependency. In contrast, the p-type SB, due to its transmission probability close to unity, does not show a T-dependency, which is characteristic of FE-dominant charge carrier injection.

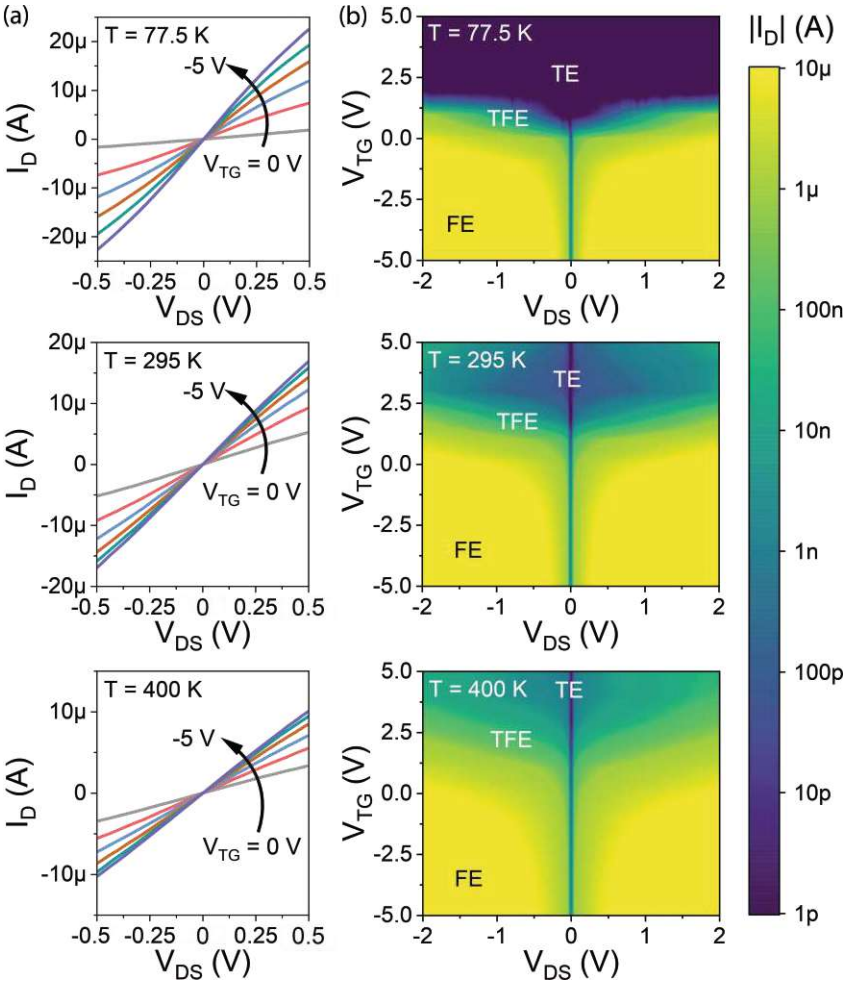


Figure 4.34: *Analysis of output characteristics of the Al-Ge based SBFET. (a) Linear representation of the output I/V in the p-branch ($V_{TG} = 0\,V$ to $-5\,V$ in $1\,V$ steps). In the low V_{DS}-regime ($-0.5\,V$ to $0.5\,V$), where TE dominates, a linear characteristic is evident, indicating a transparent SB for the injection of holes. (b) Output characteristic maps in dependence of V_{TG} at $T = 77.5\,K$, 295 K and 400 K. Additionally, TE, TFE, and FE regimes are didactically indicated.*

The **quasi-ohmic contact for the injection of holes in the Al-Ge MSJ is further highlighted by the linearity of the output I/V data** over the investigated temperature regime of 77.5 K to 400 K.

Activation energy E_a

In the following, the activation energy E_a is extracted using the 3D TE model approach, which was also used for investigations in the previously discussed material systems. However, due to the fact that d_{NW} of the used Ge NWs (~50 nm) is in the order of the atomic Bohr radius a_B^* of Ge (24.3 nm), the 1D Landauer-Büttiker (LB) theory is applied for the investigation of E_a as well. Note that a thorough discussion from a theoretical point of view is given in Section 2.3.2.

In the first step, the obtained results extracted, using the 3D TE model are discussed. Figure 4.35(a) shows the V_{TG}-dependent E_a results. In accordance with the previously discussed quasi-ohmic *p*-type junction, near-zero and even negative E_a values are evident in hole accumulation, where $V_{TG} = -2\,V$ to $-5\,V$. Notably, reconsidering the T-dependent transfer characteristic shown in Figure 4.30(a), the increase of temperature resulted in a decrease of the hole current I_{on}^{p}, supporting the observed behavior in Figure 4.35(a). Additionally, considering the positive slope m of the underlying Arrhenius plot (cf. Section 3.2.3) in strong hole accumulation indicates that the channel resistance is limiting the total current and the Al-Ge junction is transparent for holes. In contrast, in the electron dominant regime a positive barrier from $V_{TG} = 3\,V$ to $5\,V$ is evident. Following the assumption that electrons experience a distinct SB that is close to E_g(Ge) (~0.66 eV), at the intrinsic point ($V_{TG} \approx 2\,V$), an E_a value close to the band gap of bulk Ge is extracted. Thus, proving the suitability of the 3D TE model in the TE-dominant regime. Therefore, the intrinsic $E_a^{n/p}$ and $V_{FB}^{n/p}$ values are extracted by linear fitting in this regime.
Analyzing Figure 4.35(b) shows that the transparent regime in comparison to the Al-$Si_{0.5}Ge_{0.5}$ based SBFET gets extended and starts at $V_{TG} < 0\,V$ due to stronger Fermi level pinning close to the valence band of Ge. In this respect, a change in V_{TG} and V_{DS} does not significantly influence E_a.

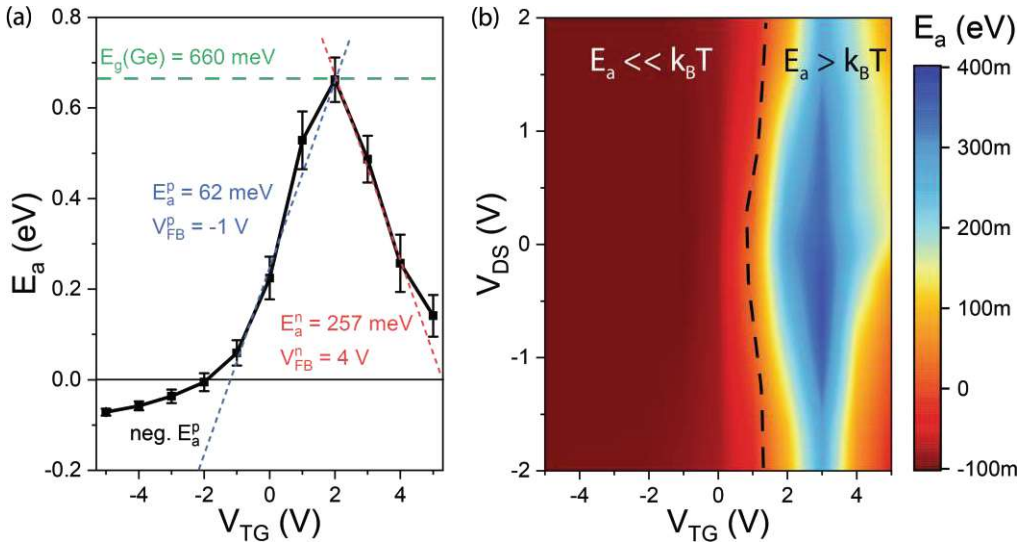


Figure 4.35: *Extraction of the activation energy E_a using the 3D TE model. (a) V_TG-dependent E_a of three similar Al-Ge based SBFETs. Additionally, $E_\mathrm{a}^{\mathrm{n/p}}$ and $V_\mathrm{FB}^{\mathrm{n/p}}$ are extracted in the TE-dominant regime. (b) E_a map extracted from output characteristics of a representative Al-Ge based SBFET. The highlighted regimes indicate a distinct SB ($E_\mathrm{a} > k_\mathrm{B}T$) and transparent Schottky junctions ($E_\mathrm{a} << k_\mathrm{B}T$).*

1D Landauer Büttiker theory

As mentioned in the introduction of this section, the 1D LB model was applied to the Al-Ge based SBFETs as well, which theoretical considerations are elaborated in Section 2.3.2. In the past, the 1D LB model was verified by numerical device simulations on CNT and NW FETs, proving its feasibility for the extraction of an activation energy. [215, 216]
In this respect, Figure 4.36 shows the experimental approach for the derivation of the 1D activation energy. In the first step, as shown in Figure 4.36(a), T-dependent transfer characteristics at different V_DS are extracted, which build the base for the investigations. Reconsidering the basic 1D LB equation introduced in Section 2.3.2 and applying the natural logarithm as well as performing some rearrangements leads to Equation (4.1).

$$\ln\left(\frac{I_\mathrm{D}}{T}\right) \approx \frac{q}{k_\mathrm{B}T}\left[n_\mathrm{g}(V_\mathrm{GS} - V_\mathrm{FB}) - E_\mathrm{a} + n_\mathrm{d}V_\mathrm{DS}\right], \tag{4.1}$$

where E_a can be obtained by applying the following methodology. After the acquisition of the T-dependent transfer characteristics at different V_DS [cf. Figure 4.36(a)], an Arrhenius plot with $\ln(I_\mathrm{D}/T)$ vs. $1/T$ is created, as shown in Figure 4.36(b). Next the slope of the obtained Arrhenius plot, i.e., $\alpha = \partial[\ln(I_\mathrm{D}/T)]/\partial(1/T)$ is calculated for the different V_TG data points and for each V_DS, as illustrated in Figure 4.36(c).

Lastly, by obtaining a value $\alpha|_{V_{\mathrm{DS}}\to 0}$ for each V_{TG} an energy function related to the applied bias and E_{a} is extracted, where $E_{\mathrm{a}} = -(k_{\mathrm{B}}\beta)/q$. Thus, allowing to plot E_{a} vs. V_{TG} as illustrated in Figure 4.36(d). In the same manner as for the 3D TE model, the intrinsic $E_{\mathrm{a}}^{\mathrm{n/p}}$ and flat-band voltage $V_{\mathrm{FB}}^{\mathrm{n/p}}$ is estimated in the corresponding TE regime.

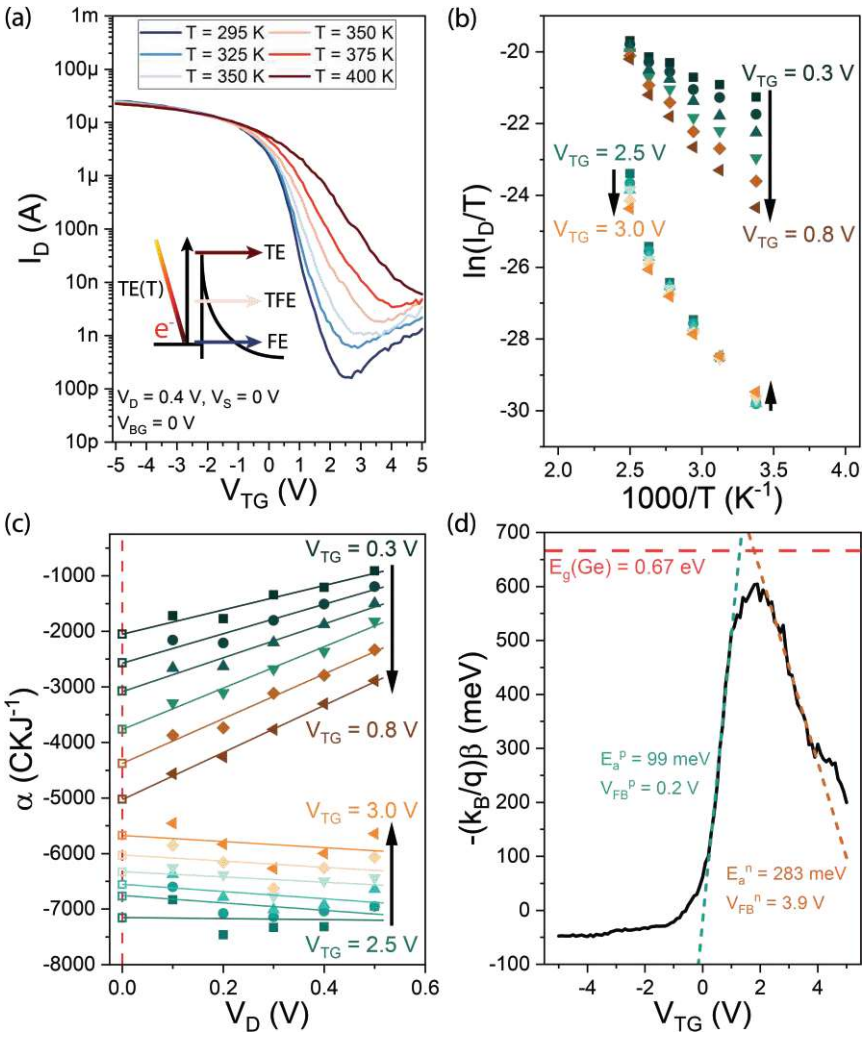


Figure 4.36: *Extraction of E_{a} via 1D LB theory. (a) T-dependent transfer characteristic at $V_{\mathrm{D}} = 0.1\,\mathrm{V}$. (b) Arrhenius plot derived from Equation (4.1) at $V_{\mathrm{D}} = 0.1\,\mathrm{V}$ and for representative V_{TG} values. (c) Extracted slopes vs. V_{D} obtained from the Arrhenius plot. (d) V_{TG}-dependent E_{a} plot. Additionally, the extracted n- and p-type E_{a} and V_{FB} in the TE dominate regime are indicated. Note that data in (b) and (c) show data corresponding to the n- and p-type subthreshold regime. Images from [RB1].*

Finally, the E_a extraction methodologies, i.e., 3D TE and 1D LB, are compared in Figure 4.37, where distinct differences can be identified. For the analysis, four individual Al-Ge based SBFETs were considered, resulting in the indicated standard deviation bars, whereas the table in the inset states the mean values. Notably, using transfer characteristics at different V_{DS} as the underlying dataset allows a higher resolution for the determination of the TE-dominant regime. In terms of the negative E_a in strong hole accumulation, the 3D TE methodology leads to higher negative values compared to the 1D LB model. With respect to the interpolation to $V_{DS} = 0\,V$, the 1D LB model explicitly considers electrostatic gating with the slope $\beta = -(qE_a)/k_B + q/k_B\,[n_g(V_{TG} - V_{FB})]$, whereas in the 3D TE model the slope $m = -E_a/k_B$. At $V_{TG} = 5\,V$, where the injection and transport of electrons dominate, also a lower E_a is extracted by the 3D TE model. However, at the off-point ($V_{TG} \approx 2\,V$), where the Al-Ge based SBFET is operated in the TE-dominant regime and no electrostatic gating effects are evident, the 3D TE model provides a more accurate value close to the band gap energy of Ge. Notably, further confirming the close Fermi level pinning close to the valence band of Ge. In this respect, an applicable sanity check is to sum up the extracted intrinsic n- and p-type $E_a^{n/p}$ to check if they equalize to the band gap of Ge with $E_g(Ge) = 0.66\,eV$. Considering the mean values of four similar SBFETs (cf. table in Figure 4.37), a ΔE, being the difference to $E_g(Ge)$ in bulk, of 395 meV and 210 meV for the 3D TE and 1D LB model, respectively, is extracted, further highlighting better suitability of the 1D LB model for NW applications with d_{NW} in the order of the atomic Bohr radius a_B^*. Note that for a precise determination of ΔE, also the fact of an increased E_g needs to be considered in the case of quantum confinement (cf. Section 2.1.3). [49]

In conclusion, the following differences between the 3D TE and 1D LB model can be identified, leading to the observed differences in Figure 4.37:

- The 3D TE model has a T^2 dependency, whereas the 1D LB model relies on a linear T dependency.
- In the 3D TE model only V_{DS} is considered and V_{TG} is implied within E_a. In contrast, the 1D LB model thoroughly considers V_{DS} and V_{TG} in the derivation of E_a.
- The 3D TE model assumes injection from a 3D metal into a 3D semiconductor, whereas for NW applications the injection from a 3D metal into a quasi-1D semiconductor is performed.

In terms of applications, the transparent MSJ properties of the Al-Ge material system are beneficial to the realization of superconductor-semiconductor devices, [64] as for example used in Al-Ge-Al heterojunction based JJ-FETs. [47, 80]

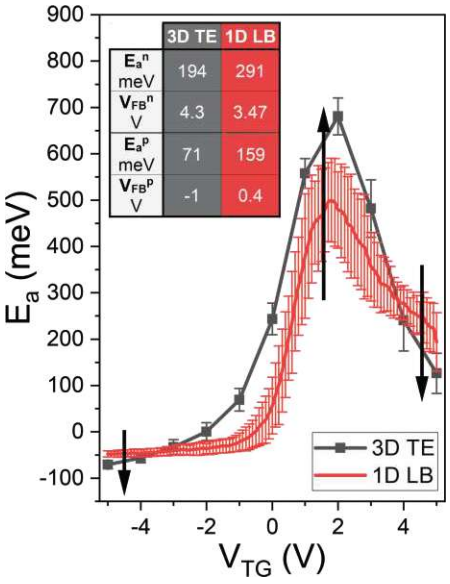


Figure 4.37: *Comparison of the V_{TG}-dependent E_a extracted by 3D TE (gray) and 1D LB (red) theory of the Al-Ge based SBFET. The table shows the extracted values from the TE dominant regime of four similar devices as shown in Figure 4.36. The black arrows illustrate the relative difference between 3D TE and 1D LB at dedicated points of interest. Image from [RB1].*

For the **analysis of the activation energy, the 3D TE model as well as the 1D LB model were used, which both show negative E_a values in strong hole accumulation**, further promoting the presence of a quasi-ohmic contact for the injection of holes. As the investigated Al-Ge based SBFETs use Ge NWs, whose **diameter d_{NW} is in the order of Ge's atomic Bohr radius a_B^***, the **1D LB model provided more accurate values in comparison to the 3D TE model**.

4.2.4 Comparison of Al-group IV based SBFETs

Finally, as already introduced in the discussion of the individual Al-group IV based SBFETs, the following covers a thorough comparison of the extracted SBFET FOM introduced in Section 3.2.2. In this respect, the Al-Si, Al-$Si_{0.5}Ge_{0.5}$, and Al-Ge based SBFET's transfer characteristics (here conductivity σ instead I_D) are illustrated in Figure 4.38(a), where specific properties become evident. Note that $V_{DS} = 1\,V$, $T = 295\,K$ and only the forwards sweep from $V_{TG} = 5\,V$ to $-5\,V$ is considered.

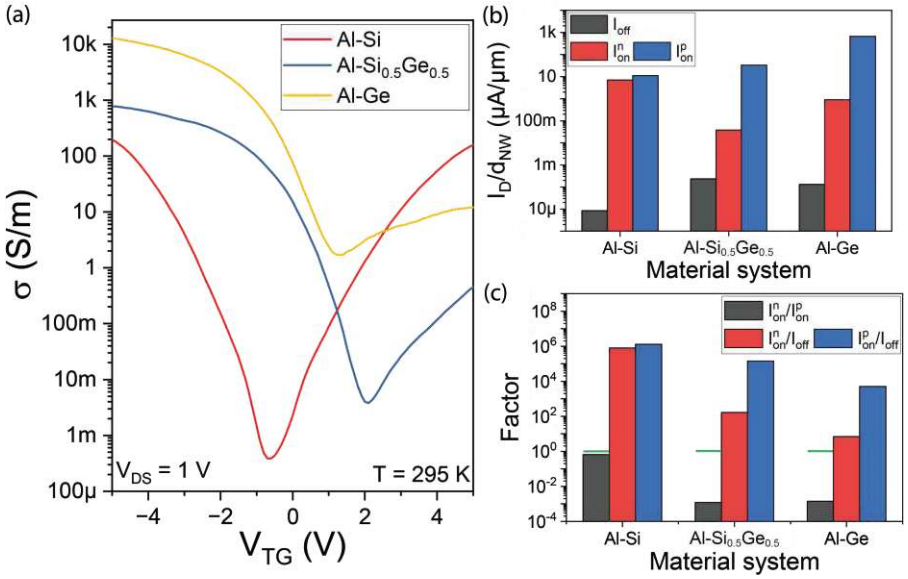


Figure 4.38: *(a) Transfer characteristics comparison of the investigated Al-group IV based SBFETs. The transfer I/Vs are expressed in terms of the conductivity σ, taking the channel's individual dimensionality into account. (b) Comparison of $I_{on}^{n/p}$ and I_{off} normalized to the individual d_{NW} of the investigated SBFETs. (c) Analysis of the I_{on}^{n}/I_{on}^{p} ratio and $I_{on}^{n/p}/I_{off}$ ratios of the investigated Al-group IV based SBFETs. The horizontal green bar indicates an ideal I_{on}^{n}/I_{on}^{p} symmetry of unity.*

Due to certain differences between the *n*- and *p*-type branch, Figure 4.38(b) visualizes the normalized $I_{on}^{n/p}/d_{NW}$ and I_{off}/d_{NW} of the individual Al-group IV SBFETs, where in particular an increase of I_{off} and I_{on}^{p} is observable for SBFETs with Ge content. First, the off-current of the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFET increases due to higher source/drain leakage caused by the smaller band gap of Ge in comparison to Si. The smaller band gap also gets reflected comparing I_{on}^{n} of the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFET, which increases for the pure Ge channel, although a distinct *n*-type SB is evident. Further, I_{on}^{p} is enhanced with increasing Ge content, due to its dominant Fermi level pinning close to the valence band, favoring the injection of holes.

Next, Figure 4.38(c) illustrates the ratios between the n- and p-type on-currents as well as sets them into perspective to the off-current. In this context, the relatively mid-gap Fermi level pinning of the Al-Si material system is reflected by obtaining an $I_{\mathrm{on}}^{\mathrm{n}}/I_{\mathrm{on}}^{\mathrm{p}}$ close to unity, whereas the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFETs show a clear favoring of p-type conduction. Moreover, due to the larger band gap of Si, the $I_{\mathrm{on}}^{\mathrm{n/p}}/I_{\mathrm{off}}$ ratios of the Al-Si based SBFET exhibit higher values in comparison to SBFETs with Ge content. In this respect, Zhao et al. formulated an approximation that reflects the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio in correspondence to E_{g} [cf. Equation (4.2)]. [301]

$$\frac{I_{\mathrm{on}}}{I_{\mathrm{off}}} \approx \frac{1}{4}\exp(E_{\mathrm{g}}/(2k_{\mathrm{B}}T)) \tag{4.2}$$

Consequently, by the selection of the channel material the $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio can be tuned. With respect to the $I_{\mathrm{on}}^{\mathrm{n}}/I_{\mathrm{on}}^{\mathrm{p}}$ ratio, the Al-Si based SBFET shows a remarkable symmetry close to unity without the implementation of additional measures. Therefore, the Al-Si material system is promising for reconfigurable field-effect transistor (RFET) applications. Nevertheless, other parameters (cf. Section 2.4.1), such as for example $V_{\mathrm{th}}^{\mathrm{n/p}}$, need to be taken into account as well.

Next, linear output characteristics are compared for a comprehensive and complete understanding of the saturation properties of the individual Al-group IV based SBFETs. Therefore, Figure 4.39 shows output characteristics on the linear I_{D} axis for $|V_{\mathrm{DS}}|$ ranging up to 2 V in n- and p-type operation. As discussed in Section 4.2.1, saturation in the Al-Si based SBFET is not reached due to non-optimized geometries, i.e., channel length and gate dielectric. In contrast, analyzing the p-type operation of the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFET indicates operation towards saturation, attributed to its strong Fermi level pinning properties close to the valence band of Ge and $Si_{0.5}Ge_{0.5}$ band gap. However, in n-type operation the V_{th} shift towards p-type operation becomes evident with relatively high currents for the Al-Ge based SBFET at $V_{\mathrm{TG}} \approx 0$ V.

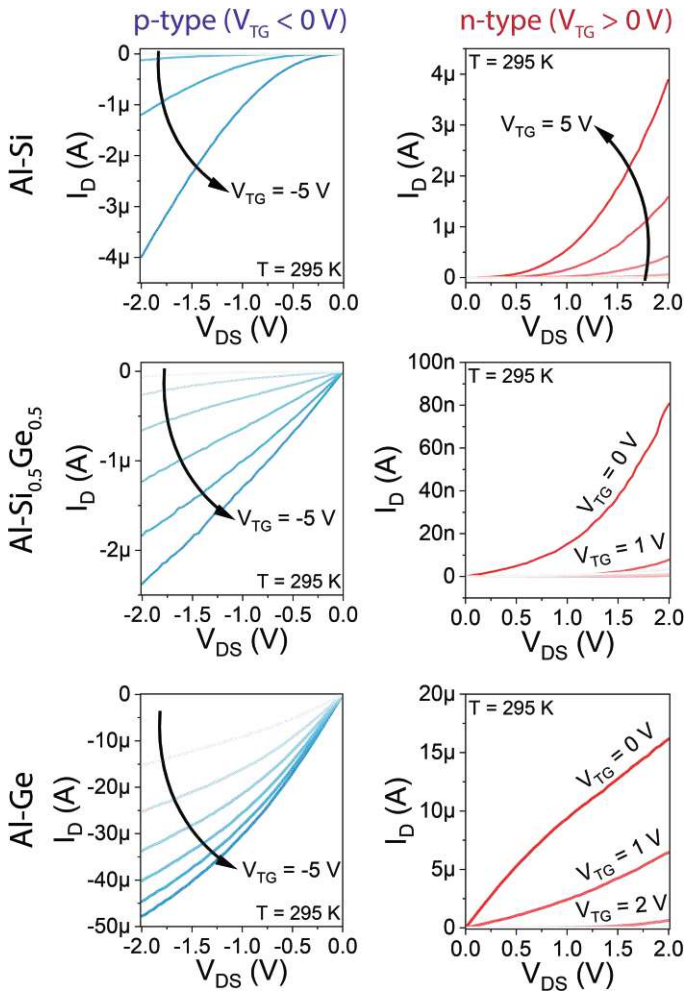


Figure 4.39: *Output characteristics comparison of the investigated Al-group IV based SBFETs. The left-hand column shows I/Vs of the p-type operation ($V_{DS} = 0\,V$ to $-2\,V$ and $V_{TG} \leqslant 0\,V$), whereas the right-hand column illustrates I/Vs of the n-type operation ($V_{DS} = 0\,V$ to $2\,V$ and $V_{TG} \geqslant 0\,V$) of the individual material systems. Attributed to the V_{th} shift in the Al-Si$_{0.5}$Ge$_{0.5}$ and Al-Ge based SBFETs, a relatively high I_D is measured for $V_{TG} \approx 0\,V$. Due to strong Fermi level pinning close to the valence band in the Ge-based SBFETs tendencies of saturation become evident in p-type operation.*

Table 4.1 summarizes the already discussed and extracted Al-group IV SBFET FOM (cf. Section 3.2.2). Therefore, relevant parameters extracted from transfer characteristics and the thereof derived maximum transconductance g^{p}_{m-max} as well as intrinsic activation energies $E_a^{n/p}$ and flat-band voltages $V_{FB}^{n/p}$ are listed.

Note that due to the absence of a g_m degradation in the Al-Si based SBFET and in the n-branch of the Al-$Si_{0.5}Ge_{0.5}$ as well as Al-Ge based SBFET, g^{p}_{m-max} is only listed for the p-branch of the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFETs, as they are operated in saturation and consequently exhibit a g^{p}_{m} degradation.

Parameter	**Al-Si SBFET (Section 4.2.1)**	**Al-$Si_{0.5}Ge_{0.5}$ SBFET (Section 4.2.2)**	**Al-Ge SBFET (Section 4.2.3)**
$\mathbf{d_{NW}}$ (nm)	70	60	53
Nominal t_{ox}	9 nm SiO_2	10.5 nm Al_2O_3	13.5 nm Al_2O_3
$\mathbf{L_{SC}}$ (µm)	1	1.1	1
$\mathbf{I^{n/p}_{on}}$ (µA/µm)	500 nA/765 nA 7/11	2.3 nA/2 µA 38×10^{-3}/33.3	48 nA/35 µA 0.9/660
$\mathbf{I_{off}}$ (µA/µm)	600 fA 8.5×10^{-6}	14 pA 233×10^{-6}	7 nA 132×10^{-6}
$\mathbf{I^{n}_{on}/I^{p}_{on}}$ ratio	0.65	1.2×10^{-3}	1.4×10^{-3}
$\mathbf{I^{n/p}_{on}/I_{off}}$ ratio	$0.8 \times 10^{6}/1.3 \times 10^{6}$	$164.3/143 \times 10^{3}$	$6.9/5 \times 10^{3}$
$\mathbf{V^{n/p}_{th}}$ (V)	3.9/−4.1	3.5/−3.3	3.4/0.5
Hysteresis$^{n/p}$ (V)	0.02/0.04	0.7/2	0.16/0.65
$\mathbf{S^{n/p}}$ (V/dec)	0.3/0.2	0.5/0.4	1.8/0.6
$\mathbf{g^{n/p}_{m-max}}$ (µS/µm)	[a]	[a]/490 nS [a]/8.2	[a]/4.4 µS [a]/83
$\mathbf{E^{n/p}_{a}}$ (meV)	300/240	143/158	3D TE: 257/62 1D LB: 291/159
$\mathbf{V^{n/p}_{FB}}$ (V)	2/−2	3/−1	3D TE: 4/−1 1D LB: 3.5/0.4

Table 4.1: *Comparison of figures of merits (FOM) of the investigated Al-group IV SBFETs, extracted from transfer characteristics with $V_{TG} = 5\,V$ to $-5\,V$. Additionally, the parameters were extracted at $V_{DS} = 1\,V$ and $T = 295\,K$.*

[a] As the SBFET is not operated in saturation, no g_{m-max} can be extracted for the Al-Si based SBFET and for the n-branch of the Al-$Si_{0.5}Ge_{0.5}$ as well as Al-Ge based SBFET.

With respect to the maximum transconductance $g_{\mathrm{m-max}}^{\mathrm{n/p}}$, as discussed previously, only for the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFET values in the p-branch could be extracted. Notably, the Al-Ge based SBFET exhibits one order of magnitude higher $g_{\mathrm{m-max}}^{\mathrm{p}}$ compared to the Al-$Si_{0.5}Ge_{0.5}$ based SBFET, which can be attributed to the dominant p-type conduction caused by the strong Fermi level pinning close to the valence band of Ge. Moreover, $g_{\mathrm{m-max}}^{\mathrm{p}}$ is exhibited at $V_{\mathrm{TG}} = -3.75\,\mathrm{V}$ and at $V_{\mathrm{TG}} = -1.2\,\mathrm{V}$ for the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFET, respectively, indicating that the $g_{\mathrm{m}}^{\mathrm{p}}$ degradation for pure Ge occurs at a lower V_{TG}, which also correlates with the investigated E_{a} map of the Al-Ge based SBFET shown in Figure 4.35.
Next, $V_{\mathrm{th}}^{\mathrm{n/p}}$ of the Al-group IV SBFETs are considered. Again, the relatively high symmetry between the n- and p-type operation regimes of the Al-Si based SBFET becomes evident. Notably, also the Al-$Si_{0.5}Ge_{0.5}$ based SBET shows a considerable symmetry with $V_{\mathrm{th}}^{\mathrm{n}} = 3.5\,\mathrm{V}$ and $V_{\mathrm{th}}^{\mathrm{p}} = -3.3\,\mathrm{V}$. In contrast, the Al-Ge-based SBFET exhibits a high asymmetry, which can be majorly attributed to a dominant horizontal shift of the transfer characteristic (cf. Section 2.1.3). Further, considering the hysteresis, as illustrated in Figure 4.40(b), the superior quality of the Si/SiO_2 interface becomes evident with a minimal hysteresis in the 10 mV-regime. Considerably, the Al-Ge based SBFET shows a better hysteresis performance than the Al-$Si_{0.5}Ge_{0.5}$ based SBFET, due to the use of DPG for the Ge NW growth (cf. Section 4.1.3), whereas for the $Si_{0.5}Ge_{0.5}$ NW growth a combination of silane and germane was used. Thus, the existence of native Ge_xO_y cannot be excluded for the Al-$Si_{0.5}Ge_{0.5}$ based SBFET, leading to a significantly higher hysteresis. Regarding the inverse subthreshold slopes $S^{\mathrm{n/p}}$, all Al-group IV based SBFETs showed $S^{\mathrm{n}} > S^{\mathrm{p}}$ because the activation energy E_{a}^{n} is higher compared to $E_{\mathrm{a}}^{\mathrm{p}}$. Notably, $S^{\mathrm{n/p}}$ has a high symmetry in the Al-Si based SBFET with values of a few 100 mV/dec. Moreover, the Al-$Si_{0.5}Ge_{0.5}$ based SBFET exhibits a distinct symmetry, however, with higher values, which might be attributed to residual Ge_xO_y between the $Si_{0.5}Ge_{0.5}/Al_2O_3$ interface. In contrast, analyzing $S^{\mathrm{n/p}}$ of the Al-Ge based SBFET shows a high asymmetry, with $S^{\mathrm{n}} = 1.8\,\mathrm{V/dec}$, indicating weak electron transport properties which correlate with the strong Fermi level pinning close to the valence band. Finally, comparing the intrinsic activation energies $E_{\mathrm{a}}^{\mathrm{n/p}}$, as shown in Figure 4.40(c), the high asymmetry of the Al-Ge based SBFET becomes evident, with a substantially higher n-type SB compared to the p-type SB. Notably, incorporating Ge, as shown for the Al-$Si_{0.5}Ge_{0.5}$ based SBFET, the band gap becomes smaller in comparison to the Al-Si material system. Moreover, a relatively high symmetry of $E_{\mathrm{a}}^{\mathrm{n/p}}$ is existent, which highlights the potential use of Al-$Si_{0.5}Ge_{0.5}$ in nanoelectronic applications, requiring same injection capabilities. However, due to the potential existence of Ge_xO_y, the symmetry gets degraded in the Al-$Si_{0.5}Ge_{0.5}$ based SBFET.

Concerning the flat-band voltages $V_{\mathrm{FB}}^{\mathrm{n/p}}$ in Figure 4.40(d), once more reveals the symmetric nature of the Al-Si material system, whereas $V_{\mathrm{FB}}^{\mathrm{n}}$ of the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFET increases, due to a substantially higher *n*-type SB in the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFETs. Thus, requiring a higher bias for the establishment of the flat-band condition. In contrast, $V_{\mathrm{FB}}^{\mathrm{p}}$ decreases with increasing Ge content, attributed to the reduction of the *p*-type SB.

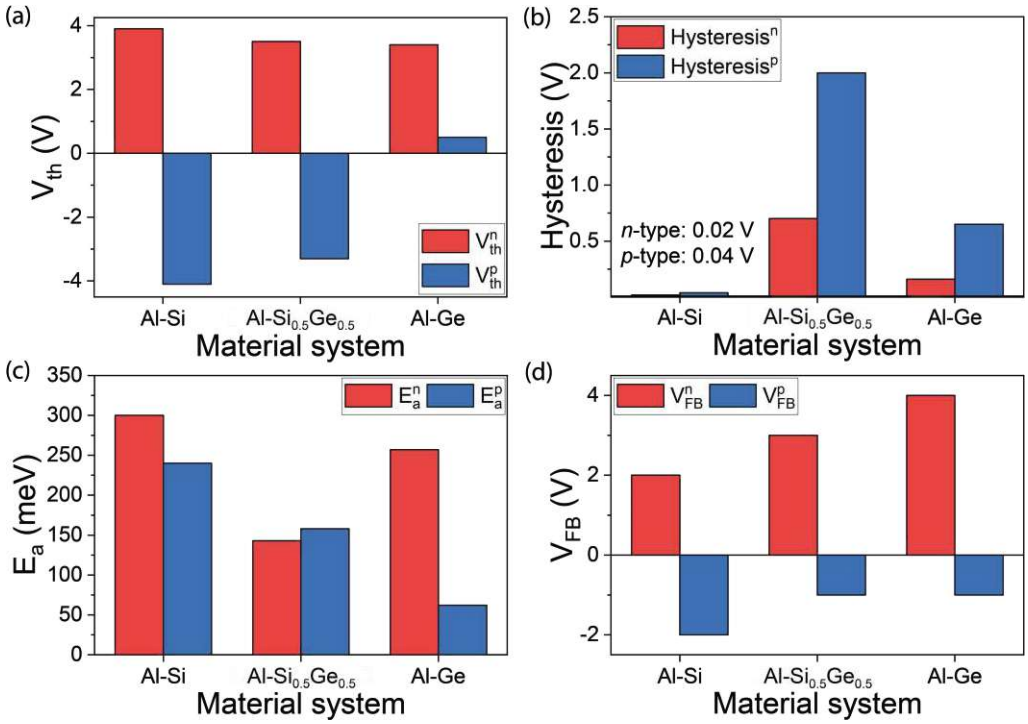


Figure 4.40: *Illustration of FOMs in terms of absolute values of (a)* $V_{\mathrm{th}}^{\mathrm{n/p}}$*, (b)* $\mathrm{Hysteresis}^{\mathrm{n/p}}$*, (c)* $E_{\mathrm{a}}^{\mathrm{n/p}}$ *and (d)* $V_{\mathrm{FB}}^{\mathrm{n/p}}$ *of the investigated Al-group IV based SBFETs. The red and blue bars indicate n- and p-type operation, respectively.*

Reconsidering the research questions stated in Section 1.1, now allows to derive certain nanoelectronic applications, whereas the high symmetric nature of the Al-Si based SBFET can be facilitated for the realization of RFETs and logic applications. Further, the methodology of bias spectroscopy can be applied to Al-Ge based SBFETs, which are used for NDR devices, to thoroughly investigate NDR operation regimes.
As the investigated Al-$Si_{0.5}Ge_{0.5}$ based SBFET architecture still needs further engineering, no dedicated applications are derived in the scope of the thesis at hand.

Al-Si based SBFET:

The **Al-Si based SBFET exhibits distinct symmetric properties** in terms of $I_{\mathrm{on}}^{\mathrm{n}}/I_{\mathrm{on}}^{\mathrm{p}}$, $|V_{\mathrm{th}}^{\mathrm{n/p}}|$ and $S^{\mathrm{n/p}}$. Further, the $I_{\mathrm{on}}^{\mathrm{n/p}}/I_{\mathrm{off}}$ ratio in the 10^6-regime, exhibits a ~three orders of magnitude higher value than SBFETs with incorporated Ge. Additionally, the **Si/SiO_2 promotes low hysteresis values** in the 10 mV-regime. Consequently, **allowing the implementation of RFETs** on the base of the Al-Si material system.

Al-Ge based SBFET:

The **Al-Ge based SBFET exhibits a high asymmetry** favoring p-type operation, supporting its application in p-type transistors. Nevertheless, due to the **intrinsic exhibition of NDR in Ge**, the **Al-Ge based SBFET allows for the realization of NDR based devices**. Further, utilizing T-dependent bias spectroscopy enables a thorough investigation of the NDR's operation regimes.

4.3 Towards Al-Si Electronics

Attributed to the symmetric nature in terms of I_{on}^{n}/I_{on}^{p} and $V_{th}^{n/p}$ evident in Al-Si based SBFETs, as presented in Section 4.2.1, the material system provides a suitable platform for the realization of RFETs and associated logic gates.
This section is organized as follows: First, Section 4.3.1 presents the first-ever Al-Si based RFET, which is elaborated in detail considering the involved charge carrier transport mechanisms as well as setting relevant FOM in perspective to state-of-the-art Si- and Ge-based RFETs. Next, Section 4.3.2 discusses basic logic gates realized with the proposed Al-Si based RFET.

In this section, the publications "Reconfigurable Complementary and Combinational Logic Based on Monolithic and Single-Crystalline Al-Si Heterostructures" [RB5] and "Nanoscale Reconfigurable Si Transistors: From Wires to Sheets and Unto Multi-Wire Channels" [RB6] are covered.

4.3.1 Realization of an Al-Si RFET

The base of the proposed Al-Si based RFET is the same nominally ⟨112⟩-oriented and un-doped Si NWs, which were already considered in the previous structural and electrical investigations (cf. Section 4.1.1 and Section 4.2.1). Note that the functional mechanism and requirements of RFETs are elaborated in Section 2.4.1. The Si NWs exhibit a diameter $d_{NW} \approx 80\,\text{nm}$ and are en-wrapped in a ~9 nm thick thermally-grown SiO_2 shell. Again, the thermally induced solid-state exchange reaction to obtain an Al-Si-Al NW heterostructure was performed at $T = 773\,\text{K}$ by RTA. Thus, providing the necessary single-elementary metal contacts and abrupt MSJs (cf. Section 4.1.1). Moreover, as proposed in Section 4.2.1, the used Al-Si material system does not make use of additional measures, such as e.g., strain engineering or doping to achieve a relatively high symmetry in terms of the *n*- and *p*-type on-currents as well as threshold voltages.
For RFET integration, the Al-Si-Al NW heterostructure with a channel length of $L_{SC} = 1.5\,\mu\text{m}$ is embedded in a three-gate architecture, allowing for enhanced functionality compared to a conventional FET. Attributed to the use of polarity gate (PG) electrodes, which are placed directly atop the abrupt Al-Si MSJs, reconfigurability between *n*- and *p*-type operation as well as efficient suppression of I_{off} is achieved [cf. Figure 4.41(b,c)]. Applying a positive V_{PG} bias allows the injection of electrons and the blocking of holes. In contrast, a negative V_{PG} leads to predominant hole conduction, i.e., *p*-type operation of the RFET. Consequently, the device operation can be altered between *n*- and *p*-type operation in a single transistor and even during run-time. In correspondence to conventional FETs, the control gate (CG) allows for tuning of the semiconductor energy landscape, resulting in an adjustment of the charge carrier density in the channel and further enables to turn the transistor on or off by applying a corresponding bias V_{CG}.

In this context, the CG introduces or suppresses, respectively, an additional potential barrier in the semiconductor channel.
Figure 4.41(a) shows a SEM image of the fabricated and investigated Al-Si based RFET. Using a NW and the proposed three-gate architecture allows for efficient gate-tunability by placing the Ω-shaped CG top gate electrode in between the Ω-shaped PG electrodes, which are directly placed atop the two MSJs. Consequently, the CG couples directly to the semiconductor active region and avoids capacitive coupling to the Schottky junctions. [51] Moreover, the two PGs are electrically connected, supporting the realization of a symmetric device architecture. Further, reducing complexity as well as enabling low off-currents in comparison to asymmetric biasing of the PG electrodes. Nevertheless, independently biasing the PG electrodes might lead to more symmetric $I_{\mathrm{on}}^{\mathrm{n/p}}$ with drawbacks of reduced on-currents and an increased signal wiring overhead. In terms of scaling, self-aligned processes have already been shown for the fabrication of RFETs, simplifying device fabrication and promoting down-scaling. [234]
Figure 4.41(d) shows *n*- and *p*-type transfer characteristics with $V_{\mathrm{PG}} = 5\,\mathrm{V}$ and $-5\,\mathrm{V}$, respectively. The corresponding simplified band diagrams for electron and hole conduction mode are illustrated in Figure 4.41(b,c), where the dotted line shows the electrostatic influence of the CG. Moreover, in Figure 4.41(d) a transfer characteristic of a "quasi single top gated" device with $V_{\mathrm{PG}} = V_{\mathrm{CG}}$ is shown, illustrating the same $I_{\mathrm{on}}^{\mathrm{n/p}}$. Attributed to the more precise band tuning capabilities of the three gated RFET, steeper subthreshold slopes $S^{\mathrm{n/p}}$ and lower off-currents I_{off} are achieved. Importantly, due to the use of thermally-grown native SiO_2 as gate dielectric, a low hysteresis is obtained.

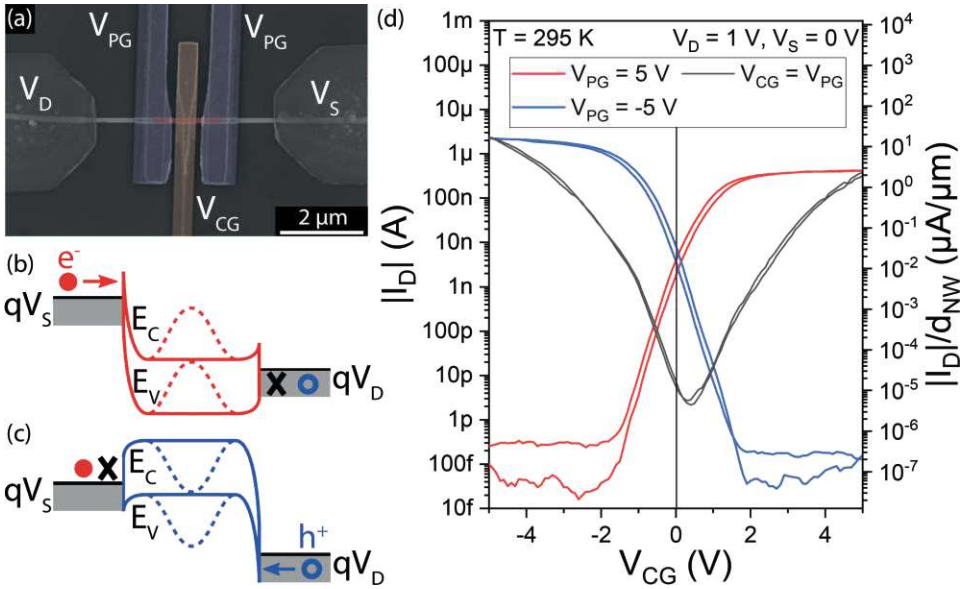


Figure 4.41: *(a) False-color SEM image of a multi-gate Al-Si based SBFET, constituting a RFET with PG and CG, being highlighted in blue and orange, respectively. (b,c) Band diagrams for electron and hole injection, respectively. The dotted line indicates the influence of the CG. (d) n- and p-type subthreshold transfer characteristics illustrating the function mechanism of the RFET. Moreover, a quasi single top gated SBFET transfer characteristic with $V_{PG} = V_{CG}$ is illustrated (gray solid line).*

Next, the V_{DS}-dependency at $T = 295\,K$ on the RFET's n- and p-type transfer characteristics is investigated, as illustrated in Figure 4.42. Here, different drain biases V_D, ranging from 0.25 V to 1 V in 0.25 V steps are acquired, considering $V_S = 0\,V$. Note that for n-type operation ($V_{PG} = 5\,V$) a positive V_D, and for p-type operation ($V_{PG} = -5\,V$) a negative V_D is applied (cf. Figure A.5). Moreover, T-dependent n- and p-type RFET transfer characteristics were investigated, showing especially for I_{off} an increase at elevated temperatures, due to a higher contribution of charge carriers injected by TE (cf. Figure A.4). For comparison to existent RFET realizations on base of Al-Si and -Ge, as well as on metal-silicide and -germanides, Table 4.2 summarizes relevant RFET figures of merit (FOM), which are extracted at $|V_D| = 1\,V$. Notably, the Al-Si based RFET features a low $I_{off}^{n/p}$, which is below the sensitivity limit of the used measurement equipment. Further, indicating efficient suppression of static power consumption in the off-state as well as suppression of gate-induced barrier lowering (GIDL), because the CG electrode screens the lateral source/drain electric field. An approach to increase $I_{on}^{n/p}$ is the use of parallel fabricated SOI-based nanosheets, which were already used to demonstrate the Al-Si solid-state exchange, allowing gate-width scalilng. [RB6] Moreover, on base of Si NWs, parallel contact printing can be facilitated for the integration of parallel arrays enhancing I_{on}. [136] Lastly, an on-current symmetry I_{on}^{n}/I_{on}^{p} of ~0.35 is achieved, which seems to be quite large. However, this symmetry is substantially closer to unity in comparison to prior-art Si-based RFETs based on state-of-the-art Ni-silicide contacts with asymmetry factors of 2-5 times higher than in the proposed Al-Si material system (cf. Table 4.2). [67, 302–304] Notably, the relatively high symmetry is achieved without any additional measures, as e.g., precise strain engineering [245] or asymmetric biasing of V_{PG}. The still remaining I_{on}^{n}/I_{on}^{p} asymmetry might be attributed to slight barrier asymmetry and differences in the effective tunneling masses of electrons and holes, influencing the tunneling probability. [305]

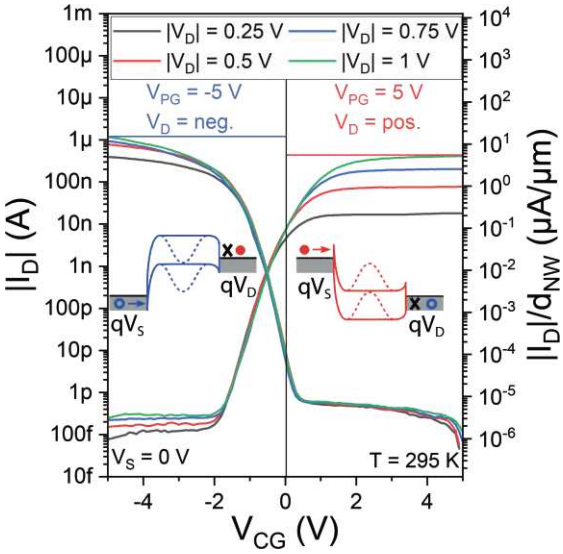


Figure 4.42: *V_{DS}-dependent RFET transfer characteristics of n- and p-type operation ranging from $V_{DS} = 0.25\,V$ to $1\,V$. Note that V_{CG} sweeping is performed from the off- to the on-state. Additionally, $I_{on}^{n/p}$ at $|V_D| = 1\,V$ is indicated by horizontal bars. The insets illustrate the corresponding band diagrams for electron and hole injection.*

As shown in Table 4.2, the Al-Si based RFET merely dominates in terms of symmetry, whereas the $NiSi_2$-Si based RFET [67] exhibits better values with respect to $I_{on}^{n/p}$, I_{off} and $S^{n/p}$. This might be attributed to a non-optimized gate oxide thickness as well as no sufficient scaling of the proposed Al-Si based RFET with channel lengths ~1 µm and diameters ~80 nm. Notably, considering Ge in RFET applications once more reveals the strong Fermi level pinning close to the valence band of Ge and increased $I_{off}^{n/p}$, due to higher source/drain leakage, attributed to the smaller band gap of Ge.

Parameter	Al-Si	$NiSi_2$-Si [67]	Al-Ge [75]	Ni_2Ge-Ge [235]
$\mathbf{I}^{n}_{on}$ (µA/µm)	3.34	5.30	0.02	0.47
$\mathbf{I}^{n}_{off}$ (µA/µm)	4.09×10^{-6}	0.15×10^{-6}	50×10^{-6}	167×10^{-6}
$\mathbf{I}^{p}_{on}$ (µA/µm)	35	94	52.8	5.6
$\mathbf{I}^{p}_{off}$ (µA/µm)	1.40×10^{-6}	0.15×10^{-6}	6.00×10^{-5}	56.0×10^{-5}
$\mathbf{I}^{n}_{on}/\mathbf{I}^{p}_{on}$ ratio	0.4	0.06	379×10^{-6}	84×10^{-3}
$\mathbf{I}^{n}_{on}/\mathbf{I}^{n}_{off}$ ratio	0.8×10^{6}	35×10^{6}	400	281
$\mathbf{I}^{p}_{on}/\mathbf{I}^{p}_{off}$ ratio	25×10^{6}	627×10^{6}	880×10^{3}	10×10^{3}
$\mathbf{V}^{n}_{th}$ (V)	0.36	[a]	1	0.4
$\mathbf{V}^{p}_{th}$ (V)	-0.7	[a]	-1.4	-0.2
$\mathbf{S}^{n}$ (mV/dec)	280	220	800	215
$\mathbf{S}^{p}$ (mV/dec)	290	90	700	150

Table 4.2: *Comparison of relevant and available RFET FOM of selected silicide, germanide, and Al-based NW RFET concepts with Si and Ge channels. Note that a source/drain bias of* $V_{DS} = 1\,V$ *is considered.*

[a] No values available.

Complementing the electrical characterization of the proposed Al-Si based RFET, output characteristics as well as I_D-transport maps are investigated, as shown in Figure 4.43, where (a,b) and (c,d) illustrate *n*- and *p*-type operation, respectively. The linear output characteristics [cf. Figure 4.43(a,c)] use matching polarities of the V_D-sweep and V_{PG} with positive and negative for *n*- and *p*-type operation, respectively. Notably, both I/Vs exhibit a non-linear increase of the V_{CG}-dependent characteristic, indicating progressive tuning of the barrier shape, which is a typical feature of SBFETs. [50, 51] Analyzing the transport maps in Figure 4.43(b,d) reveal well-defined on- and off-states, confirming the operational stability of the Al-Si based RFET, which is required for its use in circuits. Moreover, these transport maps allow to visualize optimal operation points of the device by selecting appropriate bias voltages. Attributed to the symmetry of $I^{n/p}_{on}$ and $V^{n/p}_{th}$, logic gates can be realized, even with an equal supply voltage of $|V_{PG}| = |V_{CG}| = V_D = 3\,V$ (cf. Figure A.6). In this respect, using 3 V sufficiently tunes the incorporated energy landscape of the semiconductor and drives an appropriately high drain current I_D. Again, using scaled or a different gate dielectric, i.e., a high-κ dielectric, would allow for a decrease in the supply voltage without drawbacks on the performance. [212]

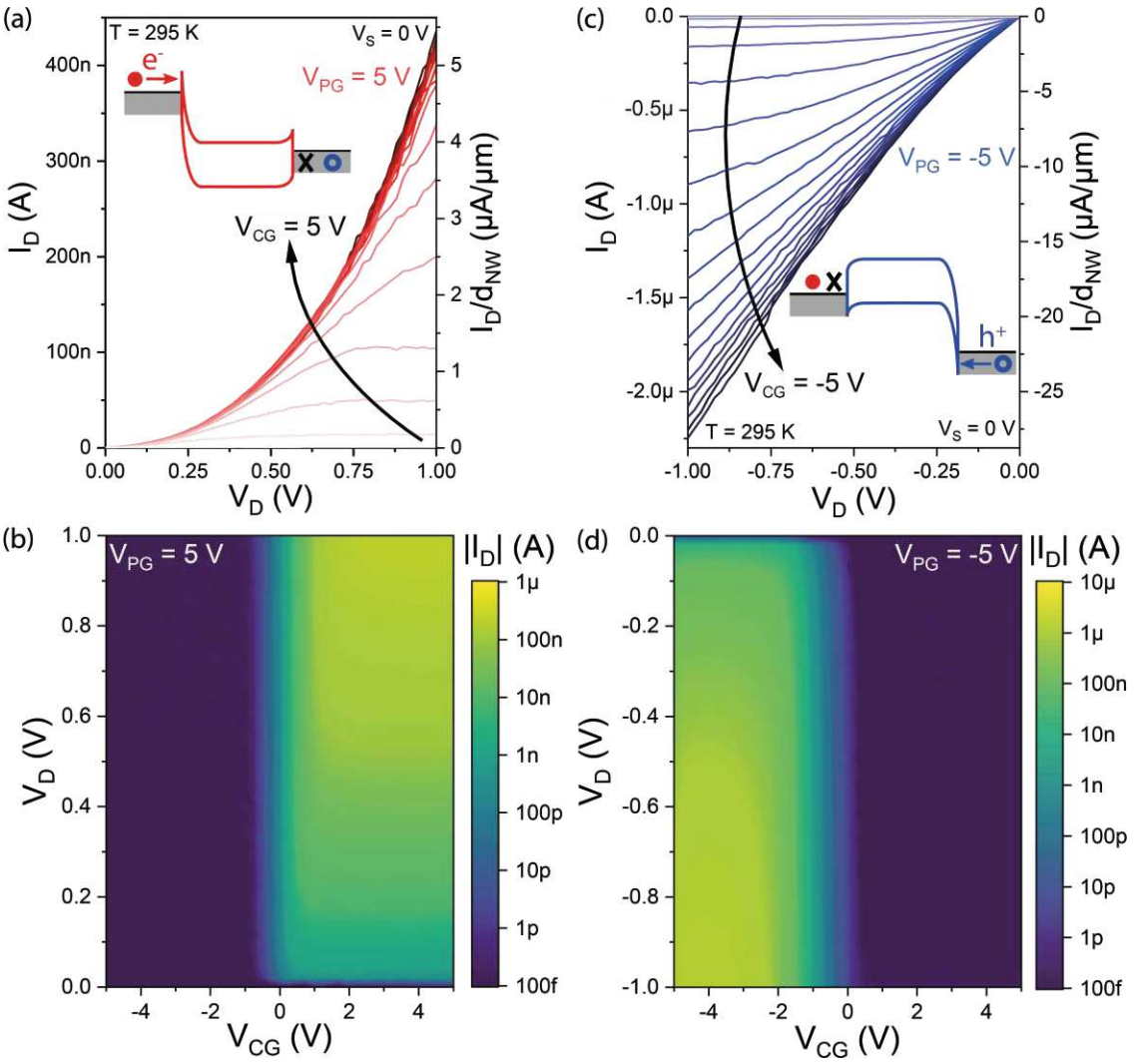


Figure 4.43: *(a) Linear representation of the n-type output characteristics ($V_{PG} = 5\,V$) for $V_{CG} = 0\,V$ to $5\,V$ in $250\,mV$ steps. (b) Semi-logarithmic transport map of the n-type operation, indicating a unipolar characteristic with well-defined on- and off-states. (c,d) illustrate data of the p-type operation with $V_{PG} = -5\,V$. The insets in (a,c) depict simplified band diagrams of the n- and p-type on-states.*

A major drawback of VLS-grown NWs is the exact placement, which bears a challenge in CMOS integration and the realization of complex logic circuits. In this respect, a feasible approach is the use of in-plane solid-liquid-solid grown NWs in combination with guided or patterned ledges. [137] Thus, allowing to control the NW diameter, alignment, orientation, and pitch. [138]. Consequently, the VLS-grown Al-Si-Al NW RFET integration depicts a prototyping vehicle, that can be applied to more advanced SOI technology for VLSI. [RB6] [306]

Using the Al-Si based SBFET technology with single-crystalline and mono-elementary Al leads **allows the realization of RFETs**, which are capable of **switching between *n*- and *p*-type operation even during runtime**. Notably an **inherently high symmetry factor** of 0.4 I_{on}^{n}/I_{on}^{p} is achieved without the introduction of additional measures.

4.3.2 Basic Logic Circuits

As proposed in Section 4.3.1, the Al-Si based RFET is applied in basic logic gates to demonstrate its application in circuits. Therefore, in the first step, a complementary inverter is realized, as illustrated in Figure 4.44. In this context, the low-side RFET, i.e., connected to $V_{SS} = 0\,V$ is operated in *n*-type operation (pull-down transistor) by applying $V_{PG} = 3\,V$. The high-side RFET (pull-up transistor) is connected to $V_{DD} = 3\,V$ and is operated in *p*-type operation ($V_{PG} = -3\,V$). An actual SEM image of the device layout with an overall NW length of ~20 µm is illustrated in Figure 4.44(a), where two Si regions and three Al segments are evident. Attributed to the complementary nature of the circuit, the output signal V_{OUT} is extracted from the Al electrode connecting the two Al-Si based RFETs. The device architecture reveals one of the key advantages of RFETs, which is its exact same device layout, geometry, and composition for both *n*- and *p*-type operation. Thus, providing a vast variety of applications such as functional diverse adaptive computing paradigms and hardware secure circuits. [241, 307, 308] In general, demonstrating this fundamental logic gate, the Al-Si material system proves its applicability in complementary logic gates.
Next, the transient operation of the proposed Al-Si based RFET inverter is investigated in Figure 4.44(b), where both CGs act as the input signal V_{IN}, which is driven by a function generator (cf. Section 3.2.1). As it becomes evident in the output signal V_{OUT}, the expected toggling between the supply voltages $V_{DD} = 3\,V$ and $V_{SS} = 0\,V$ is observable. In this context, inverter operation is ensured with a symmetric supply voltage of $|3\,V|$, whereas a reduction of the supply voltage leads to insufficient inverter functionality (cf. Figure A.7). Moreover, to avoid an electric breakdown in the proposed realization, $V_{SS} = -3\,V$ was avoided. Therefore, only symmetric and not single supply can be shown here. [243, 309] Attributed to its complementary nature – one RFET is operated in *n*- and the other in *p*-type operation – the current I_D through the two RFETs in series reveals a negligible current flow in the high- and low-states states. However, at the state transitions, where switching of V_{IN} occurs, current-peaks of ~200 pA become evident, which is a characteristic feature of complementary logic gates. Notably, inverting the polarity of V_{PG} and consequently operating both RFETs in the opposite mode, leads to the qualitative same results. This is an important asset in terms of realizing more complex combinational logic gates, as it enables flexibility of the proposed inverter, which cannot be accessed in conventional CMOS technology due to its predefined operation mode, defined by geometry and doping profiles.

With respect to the signal overhead, Trommer et al. proposed a concept for flipping the supply line voltages on the fly. [310] Through the use of a single inverter the supply lines and PGs can be changed jointly, enabling a full output swing.

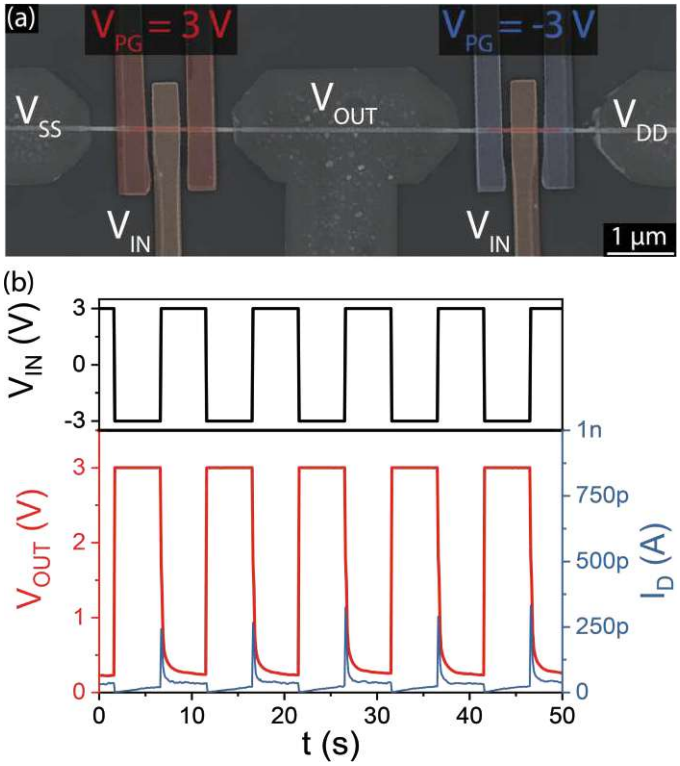


Figure 4.44: *(a) False-color SEM image of two Al-Si based RFETs in series, constituting a complementary inverter by using reconfiguration on transistor level. (b) Transient investigation of the RFET-based inverter with biases, i.e., source/drain and TG voltage, of* $|3\,\mathrm{V}|$*. Peaks in the* I_D *vs. t curve indicate complementary inverter functionality.*

Further exploiting the concept of multi-gate Al-Si based SBFETs, a wired-AND gate can be realized by adding a second CG in the middle of the Si channel, resulting in an additional electrode to turn the RFET on or off. In the scope of a wired-AND both independent CGs are used as input signals (V_A and V_B) constituting a wired-AND gate. [252, 311] Figure 4.45(a) shows a false-colored SEM image of the realized wired-AND gate with two Ω-shaped CGs between the PGs, covering the Al-Si MSJs. Notably, as it becomes evident in the transient operation, as shown in Figure 4.45(b), the current I_{DD} through the device defines the logic output, depicting a difference to conventional AND realizations based on CMOS technology, which commonly uses a voltage level as output. Note that, again, a symmetric supply bias of $|3\,V|$ is used for sufficient operation. Attributed to sufficient current drive capabilities, the proposed Al-Si based wired-AND gate is well-suited as a replacement for the parallel "pull-down" branch of NAND logic gates realized by conventional MOSFET technology [cf. Figure 4.45(c)]. Lastly, reconfigurability of RFET polarity and supply voltage would allow for compact NAND/NOR operability. [244, 306]

Note that the transistor count can further be reduced by using multiple inputs, i.e., placing a higher number of CGs, where merely the semiconductor channel length limits the total amount of inputs.

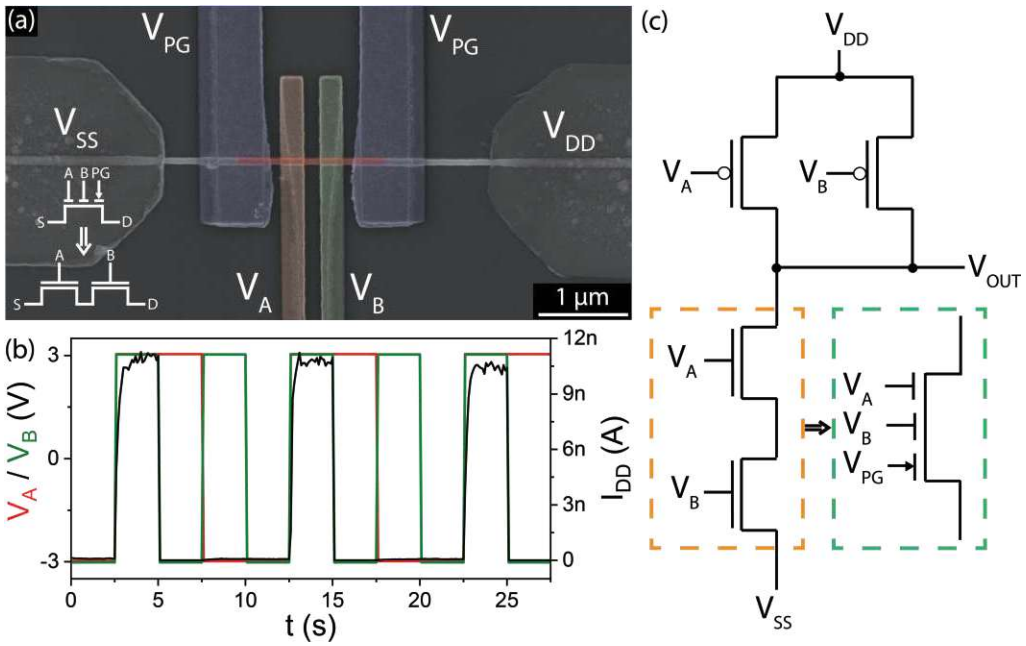


Figure 4.45: *(a) False-color SEM image of a multi-gate Al-Si-Al NW heterostructure, constituting a wired-AND gate. The left lower inset illustrates the equivalent of conventional transistor technology. (b) Transient behavior of the proposed wired-AND gate in n-mode. Here, the frequencies of* V_A *and* V_B *are* 0.1 Hz *and* 0.2 Hz*, respectively. Note that* I_{DD} *defines the output variable of the wired-AND gate. (c) Example of a NAND logic gate realized with conventional transistor technology, where the orange rectangle indicates the part that can be replaced by a wired-AND gate.*

Note that in the work at hand, rather low frequencies of 0.1 Hz and 0.2 Hz are used for the generation of the input signals. Unfortunately, also attributed to the absence of a back end of line (BEOL) interconnect technology, our lab-based design and equipment exhibit high parasitic capacitances, limiting the operation speed. However, TCAD simulations by Baldauf et al. demonstrated switching speeds of Si-based RFETs in the GHz-regime. [212]

Using bias spectroscopy to illustrate I_D-transport maps allows the **extraction of optimal operations points**, which leads to the use of symmetric biases (here: |3 V|) for input and supply lines. Therefore, a **complementary inverter and a wired-AND logic gate** were realized by the exploitation of Al-Si based RFETs. Notably, enhancing the **flexibility for its integration in advanced logic circuits**.

4.4 Advancing NDR in Al-Ge SBFETs

As discussed in Section 2.4.2, Ge features the inherent exhibition of negative differential resistance (NDR). Therefore, the following section discusses the enhancement of NDR in Al-Ge based SBFETs with a single top gate and a multi-gate architecture. In this context, bias spectroscopy, as introduced in Section 3.2.4 and already applied in Section 4.2.3, is employed for a thorough investigation of the NDR region and its physical transport mechanism.
Note that the theoretical background on NDR, and in particular on Ge-based NDR devices, is elaborated in Section 2.4.2. Additionally, in Figure A.10 latest simulation results obtained by Dr. Felipe Murphy-Armando, University College Cork, evaluating the charge carrier concentration and mobilities in the relevant conduction valleys are shown. These investigations are still ongoing and beyond the scope of the thesis at hand.

In this section, the conference proceedings "Bias Spectroscopy of Negative Differential Resistance in Ge Nanowire Cascode Circuits" [RB7] and "Mapping Electronic Transport in Ge Nanowire SBFETs: From Tunneling to NDR" [RB4] are covered.

4.4.1 NDR in Al-Ge based SBFETs

As starting material the already proposed VLS-grown and nominally un-doped ⟨111⟩-oriented Ge NWs, grown with the diphenylgermane (DPG) precursor, are considered (cf. Section 4.1.3). Prior to SBFET integration, the nominally 50 nm in diameter d_{NW} wide Ge NWs were en-wrapped in a 13.5 nm thick ALD Al_2O_3 shell, which later acts as the SBFET's gate oxide. Again, to achieve the desired Al-Ge-Al NW heterostructure, the Ge NW is contacted by Al and the thermally induced longitudinal Al-Ge exchange reaction is initiated by RTA at $T = 673\,\mathrm{K}$. Thus providing quasi-1D monolithic Al-Ge-Al NW heterostructures with single-crystalline and mono-elementary Al leads. For the realization of NDR-based devices, the same Ω-shaped top gate (TG) architecture, as introduced in Section 4.2.3, is used in the first step.

As an essential requirement for the exhibition of NDR in Al-Ge based SBFETs, a sufficiently high electric field in the electron dominant regime (here: $V_{\mathrm{TG}} = 5\,\mathrm{V}$) needs to be applied. In this context, the combination of efficient electrostatic gating and geometric confinement of the Al-Ge-Al NW heterostructure with the Ω-shaped TG supports an efficient transferred electron effect, enabling distinct NDR in the proposed Ge-based device. Attributed to the use of DPG for the Ge NW growth, transiently stable devices are obtained, which further allow investigations of the manifold influences, such as bias voltages and temperature, on the NDR characteristics. Figure 4.46 shows a typical NDR I/V characteristic ($\log_{10} I_{\mathrm{D}}/V_{\mathrm{D}}$) of the proposed Al-Ge based SBFET at $T = 77.5\,\mathrm{K}$. Notably, allowing to identify the distinct transport mechanism by analyzing the slopes.

S1 depicts thermionic emission (TE), which is in particular pronounced at $T = 77.5\,\mathrm{K}$, due to low thermal excitation of charge carriers and a pronounced electron SB (cf. Section 2.2.1). Further, increasing V_D leads to a stronger band bending, resulting in TFE/FE, which is indicated by **S2**. Reaching the critical electric field E_crit at ~$1 \times 10^6\,\mathrm{V/m}$, leads to an electron transfer from the L- to the X-valley of the Ge's conduction band (cf. Section 2.4.2). Consequently, a significant mobility decrease occurs, resulting in NDR and a negative slope **S3**. Further increasing V_D, leads to an avalanche-like increase of I_D, which can be attributed to hot electrons at high electric fields [cf. inset in Figure 4.47(a)]. This effect is also denoted as impact ionization (II) characterized by **S4**. Notably, the flattening after II might be caused by self-heating of the Al-Ge based SBFET at high drain current densities.

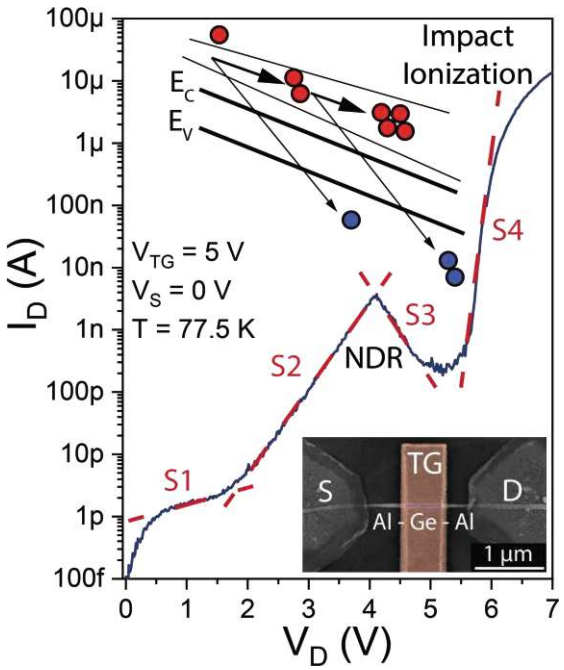


Figure 4.46: *NDR I/V characteristic at $V_\mathrm{TG} = 5\,\mathrm{V}$ and $T = 77.5\,\mathrm{K}$. The slopes S1-S4 denote the different transport regimes. The lower right inset shows a false-color SEM image of the investigated Al-Ge based SBFET. The top inset illustrates impact ionization, causing an avalanche-like increase of I_D after the NDR region.*

In the next step, the T-dependency of the NDR's peak- and valley-region is investigated in Figure 4.47. This is of essential relevance in understanding the physical transport, due to the expected involvement of different charge carrier injection mechanisms. In this sense, attributed to higher thermal activation with increasing temperatures, the peak- and valley-voltage V_Peak and V_Valley (here: V_p and V_v) shift by $8.5\,\mathrm{mV/K}$ for both, V_p and V_v. Notably, up to $T = 350\,\mathrm{K}$ a peak-to-valley ratio (PVR) of 5 is achieved.

In particular, the exhibition of NDR up to $T = 350\,\mathrm{K}$ is an important requirement for the application of NDR-based devices in circuit implementations, as sufficient NDR is still achieved at elevated temperatures. Further increasing the temperature leads to a vanishing of the NDR, attributed to thermally activated transport in the L-valley and a strongly decreased transferred electron efficiency (cf. Section 2.4.2).

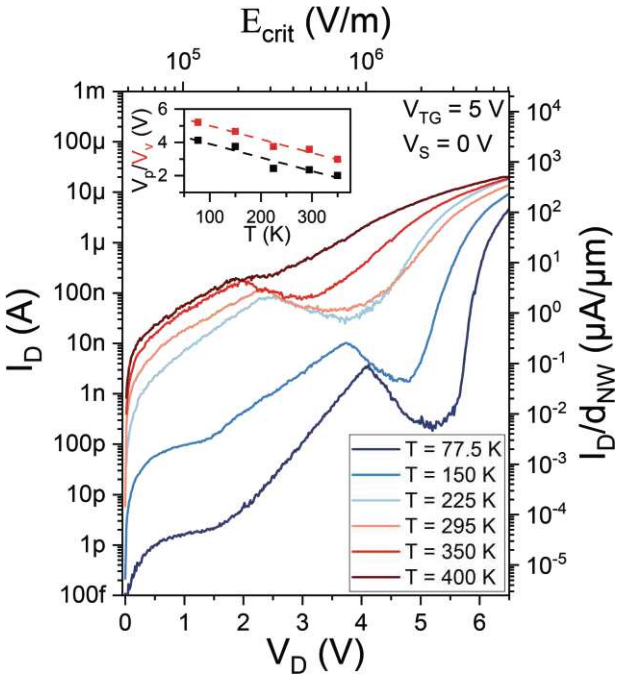


Figure 4.47: *T-dependent NDR I/V characteristics for $V_{\mathrm{TG}} = 5\,\mathrm{V}$. The top inset shows the T-dependency of V_{p} and V_{v}, indicating a linear voltage downshift with increasing temperatures. The linear fit serves solely as a visual guide.*

Next, T-dependent bias spectroscopy in the temperature range between $T = 225\,\mathrm{K}$ to $400\,\mathrm{K}$ is used to investigate key features of NDR in the proposed Al-Ge based SBFET, as illustrated in Figure 4.48. In this respect, the PVR at RT ($T = 295\,\mathrm{K}$) is a factor of 6.5 larger in comparison to state-of-the-art Si/SiGe RTDs and a factor of 3.5 larger of AlAs/GaAs NDR devices. [233] Additionally, in Figure 4.48(a), the NDR I/V characteristic at $T = 225\,\mathrm{K}$ is illustrated, where slopes are identified in the same manner as in Figure 4.46. However, attributed to a higher temperature (here: 225 K; in Figure 4.46 77.5 K), the plateau at low V_{D}, indicating TE is not visible, due to a higher thermal activation. Therefore, S1 directly indicates electron transport in the L-valley. For more precise identification and localization of the NDR regime, the negative differential conductance NDC, defined according to $dI_{\mathrm{D}}/dV_{\mathrm{D}}$, is visualized in Figure 4.48(b). Consequently, negative values correspond to the NDR regime.

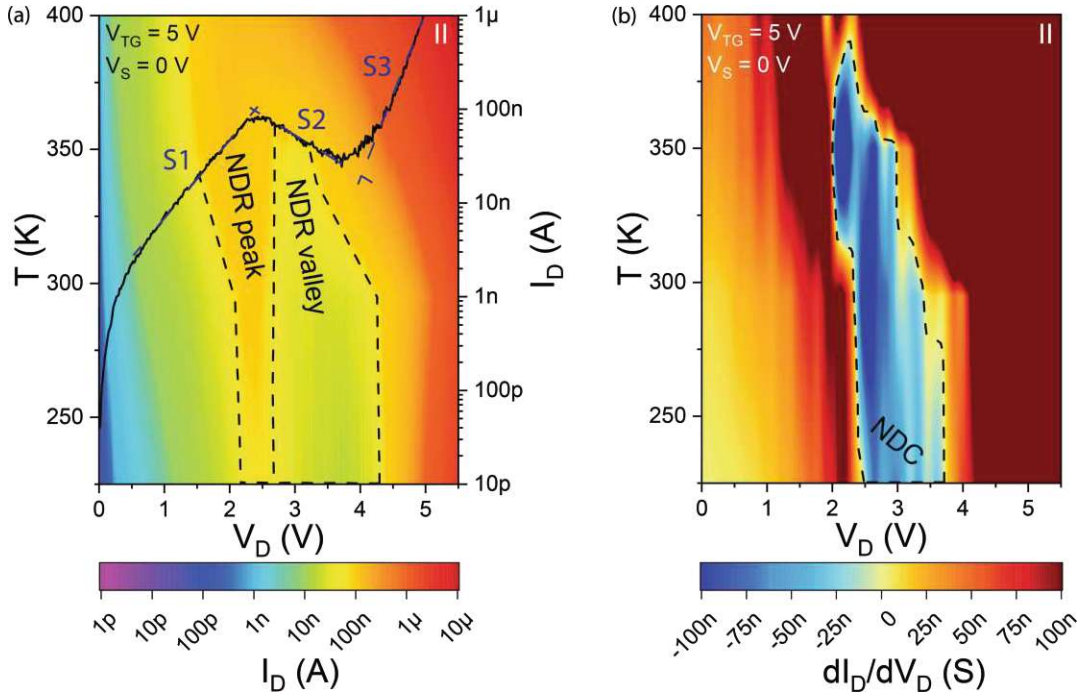


Figure 4.48: *(a) T-dependent bias spectroscopy of the NDR characteristic acquired from an Al-Ge based SBFET in the temperature range between* 225 K *and* 400 K*. The right y-axis shows the* $\log_{10} I/V$ *at* $T = 225$ K *as reference. Additionally, S1-S3 indicate the involved transport regimes. (b) Derived T-dependent NDC map from data in (a).*

Having identified the corresponding T-dependent transport regimes and mechanisms, the NDR region itself is investigated from a tunability perspective. Therefore Figure 4.49 shows bias-dependent transport maps, considering V_{TG} and V_{D}, where V_{TG} is increased from 3.5 V to 7 V in 0.5 V steps. In this context, bias spectroscopy allows the visualization of the corresponding NDR peak- and valley regions. Remarkably, the NDR region spreads from $V_{\mathrm{TG}} = 4.75$ V to 7 V with a progressive enhancement attributed to internal field modulation. Above a specific threshold bias (V_{D}), the onset of impact ionization (II) becomes evident. In case of inefficient electron injection, i.e., insufficient band bending induced by V_{TG}, II occurs at lower V_{D}, and the transferred electron effect is not initiated. Regarding the extracted PVR values, a mean PVR of 10 is achieved. Again, for a distinct identification of the NDR regime, a NDC map is calculated and visualized in Figure 4.49(b). In this respect, a linear I_{D} peak shift with a slope of $2V_{\mathrm{TG}}/V_{\mathrm{D}}$ becomes evident, where the peak width remains fairly constant. Notably, increasing V_{TG} leads to a broadening of the NDR valley, and the II regime is shifted towards higher V_{D} because the gate/drain potential difference becomes smaller.

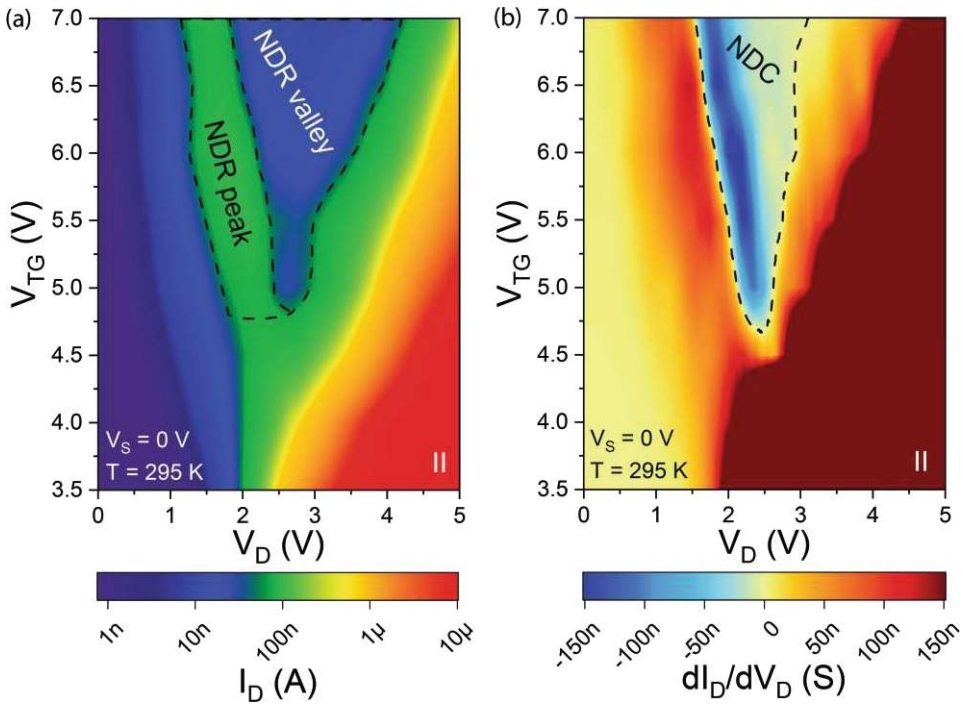


Figure 4.49: *(a) Bias spectroscopy illustrating the V_{TG}- and V_D-dependency on the NDR characteristic of the Al-Ge based SBFET. Notably, revealing a distinct NDR peak and valley region. (b) Derived bias-dependent NDC map from data in (a).*

To achieve NDR tunability, and in particular, modulating the NDR position, a cascode circuit of Al-Ge based SBFET NDR devices was realized as shown in the inset of Figure 4.50(a). The cascode circuit, realized by two Al-Ge based SBFETs in series functions as described in the following: The low-side SBFET (T_2; V_{TGL}) operates in NDR-mode by setting $V_{TGL} = 5\,V$, resulting in electron dominant transport. In contrast, the high-side SBFET (T_1; V_{TGH}) is used as a resistive element, enabling a shift of the NDR region. As it becomes evident in the transport map shown in Figure 4.50(a), for $V_{TGH} = -2\,V$ to $1.25\,V$, a stable NDR regime with respect to V_D is achieved. This characteristic is attributed to the fact that T_1 is operated in the *p*-branch and, therefore, acts like a low resistive load, due to the quasi-ohmic Al-Ge junction properties (cf. Section 4.2.3). Consequently, a high portion of V_D drops over T_2. However, as V_{TGH} becomes more positive, T_1 is progressively operated towards *n*-type operation, and V_D is more evenly distributed among T_1 and T_2. Further, this leads to a modulation of the NDR-peak for $V_{TGH} = 1.25\,V$ to $2.5\,V$. Notably, the described modulation feature is well visualized in the NDC map shown in Figure 4.50(b).

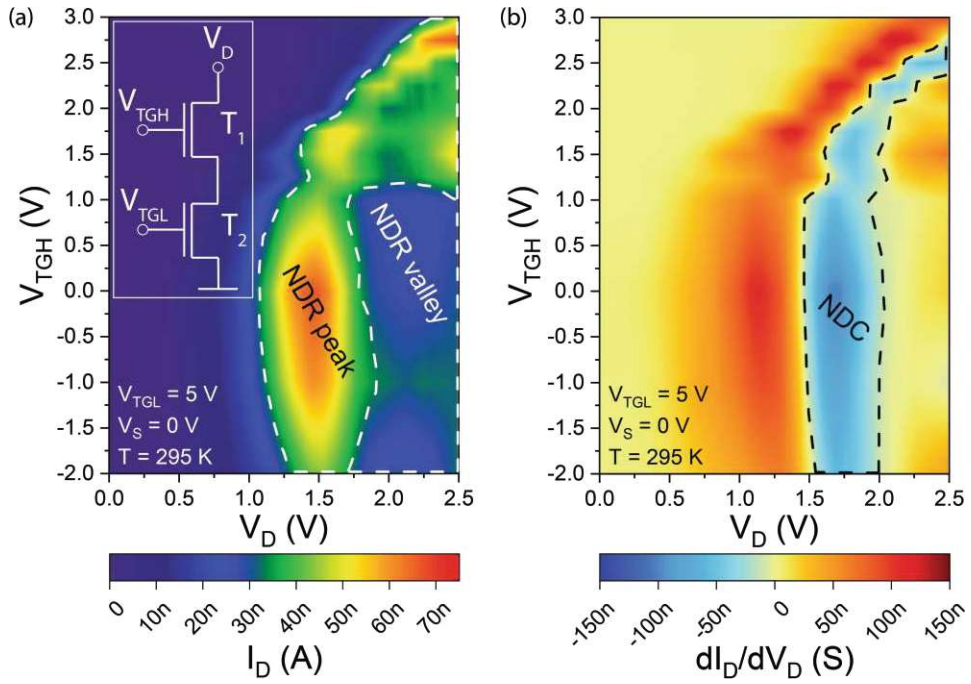


Figure 4.50: *(a) Bias spectroscopy of two cascoded Al-Ge based SBFETs as illustrated in the left inset. $V_{\mathrm{TGL}} = 5\,\mathrm{V}$ (T_2), operating the lower Al-Ge based SBFET in NDR mode, whereas V_{TGH} (T_1) is swept from $-2\,\mathrm{V}$ to $3\,\mathrm{V}$ by means of bias spectroscopy. (b) Derived V_{TGH}-dependent NDC map from data of (a).*

NDR I/V characteristics were used to **investigate the different transport mechanisms, leading to the transferred electron effect and the exhibition of NDR**. Therefore, T- **as well as bias-dependent transport maps are used for distinct indications of the NDR and NDC regions**. Using a **cascode circuit**, consisting of two Al-Ge based SBFETs in series, **allows to induce a V_{TG}-dependent NDR region shifting**.

4.4.2 NDR in multi-gate Al-Ge based SBFETs

Attributed to the higher flexibility of a multi-gate architecture, which was already facilitated for the realization of Al-Si based RFETs (cf. Section 4.3.1), the same gating concept is used for a more precise tuning of the charge carrier transport in Al-Ge based NDR devices. Thus, enabling polarity control by the proposed RFET design with two independent gates: The program gates (PGs), which cover both Al-Ge MSJs, and the control gate (CG) in between covering the Ge channel.
Figure 4.51(a) shows the considered multi-gate Al-Ge based NDR device, allowing to switch between n- and p-type operation by applying a positive or negative V_{PG} bias. In this context, Figure 4.51(b) shows the thereof obtained transfer characteristics for sweeping V_{CG} from the off- to the on-state and consequently modulating the charge carrier concentration in the channel. As indicated by the green curve, the ambipolar nature of the Al-Ge based SBFET can be transposed in unipolar n- and p-type operation. Moreover, an efficient suppression of source/drain leakage is achieved, which limits the static power consumption despite the low band gap of Ge. As discussed in Section 4.2.3, the low, and even negative, activation energy $E_{\mathrm{a}}^{\mathrm{p}}$ for the injection of holes results in strongly asymmetric on-currents $I_{\mathrm{on}}^{\mathrm{n/p}}$. Notably, this fact constitutes an essential drawback of Ge-based RFETs (cf. Section 4.3.1), [235, 236] as all technologically relevant metal-Ge MSJs exhibit strong Fermi level pinning close to the valence band, favoring the injection and transport of holes (cf. Section 2.2.2). [78]

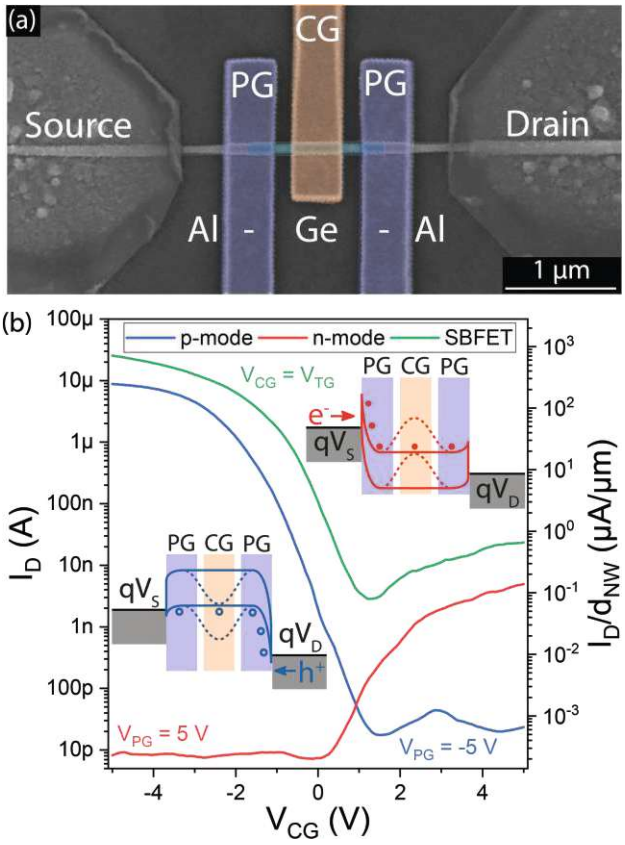


Figure 4.51: *(a) False-color SEM image of the proposed Al-Ge based multi-gate NDR device, which uses the RFET notation for its top gates, i.e., PG and CG. (b) Transfer characteristics of the Al-Ge based multi-gate device, operated in n- and p-mode with $V_{PG} = 5\,V$ and $-5\,V$, respectively. Additionally, the green curve illustrates the transfer characteristic of a top gated Al-Ge based SBFET with $L_{SC} = 1.1\,\mu m$. The insets depict schematic band diagrams of the gating mechanism, resulting in unipolar electron and hole conduction.*

In the next step, the impact of electrostatic gating on the exhibition of NDR in the proposed multi-gate SBFET architecture is investigated for fixed $V_{CG} = 5\,V$, allowing the transport of electrons, and sweeping V_{PG}. The corresponding transport map is illustrated in Figure 4.52. Importantly, NDR in Ge is accessed in case of electron conduction due to the fact that the transferred electron effect can only occur in the multi-valley conduction band landscape (cf. Section 2.4.2). Consequently, NDR is only evident for positive V_{PG}, enabling the injection of electrons. Moreover, the NDR effect becomes more pronounced for increased V_{PG}, leading to a higher degree of band bending, resulting in a higher contribution of electrons being injected by direct tunneling (FE). At $V_{PG} \approx 3.5\,V$ injected electrons are sufficiently accelerated across the channel and consequently lead to the transferred electron effect, yielding stable and reproducible NDR, as also indicated by the NDC map in Figure 4.52(b).

Here, the advantage of using NDC maps is reflected, as no negative conductance values are obtained for $V_{PG} < 3.5\,V$, indicating that NDR cannot be accessed.

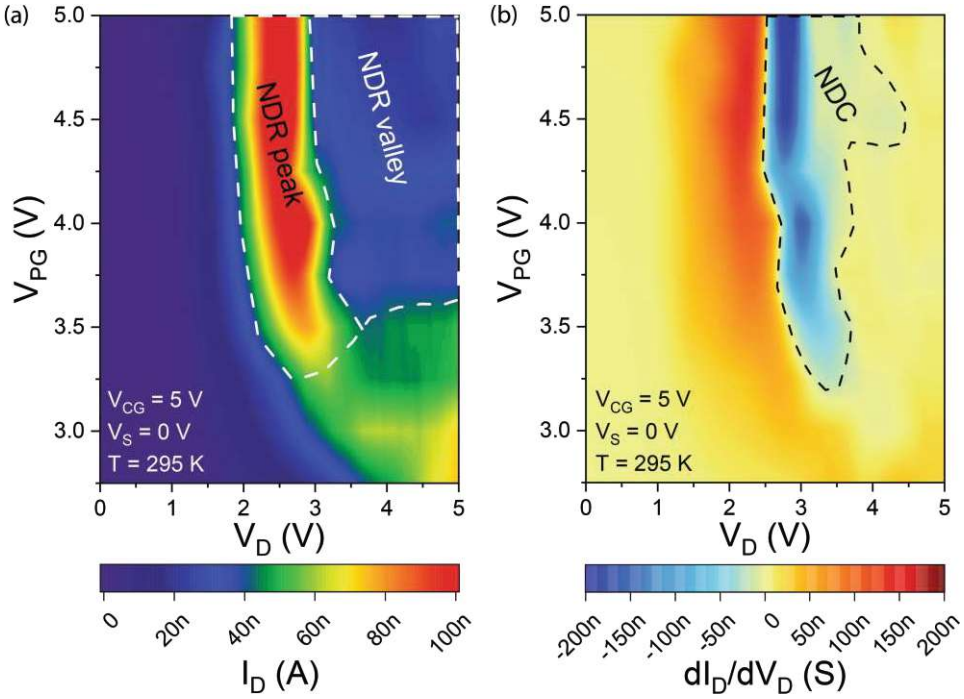


Figure 4.52: *(a) V_{PG}-dependent bias spectroscopy of the Al-Ge based multi-gate SBFET with $V_{CG} = 5\,V$. Notably, a distinct NDR region becomes evident at $V_{PG} > 3.5\,V$. (b) Derived NDC map from data of (a).*

Following the investigations of the injection capabilities tuned by V_{PG}, the influence of the CG is investigated by keeping $V_{PG} = 5\,V$, favoring the injection of electrons and sweeping V_{CG}. As shown in Figure 4.53, the NDR region exhibits a CG-dependent tunability, where the NDR peak can be effectively shifted by ~2 V applying V_{CG} between 3 V and 5 V. In this context, a maximum RT PVR of ~10 is achieved. The transport mechanism leading to this shift can be described as follows: Applying a higher V_{CG}, e.g., 5 V, leads to stronger band bending of the semiconductor landscape and thus an enhanced acceleration path for electrons, leading to the fact that the transferred electron effect takes place at lower V_D. In contrast, lower V_{CG} causes less band bending, and therefore, a higher electric field (V_D) is required to initiate the transferred electron effect. Notably, the multi-gate Al-Ge based NDR device constitutes an integrated version of the cascode circuit of two Al-Ge based SBFET NDR devices (cf. Figure 4.50). In this context, the multi-gate architecture exhibits a different NDR region characteristic, but with a more distinct modulation capability of the NDR region.

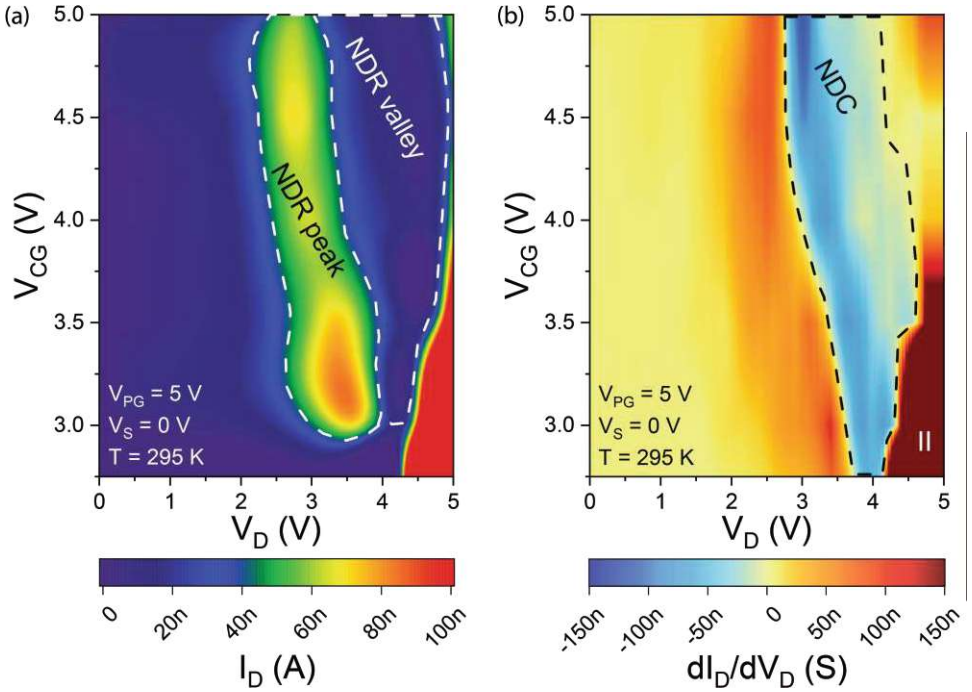


Figure 4.53: *(a) V_{CG}-dependent bias spectroscopy of the Al-Ge based multi-gate SBFET with $V_{PG} = 5\,V$. Varying V_{CG} allows to modulate the position of the NDR region. Additionally, up to V_{CG} ~4 V and $V_D > 4.25\,V$, impact ionization (II) becomes evident. (b) Derived NDC map from data of (a).*

In the scope of further enhancing the tunability of the NDR region, a cascode circuit of two multi-gate Al-Ge based NDR devices was created, as shown in the inset of Figure 4.54(a). Using this configuration allows to use V_{CG} of the high-side transistor (T_1) as input, resulting in an I/V characteristic with overlapping NDR regions (cf. Section 2.4.2). In particular, being a relevant characteristic for the realization of MOBILE devices, allowing the implementation of reconfigurable NAND/NOR logic gates. [82] Here, the functional mechanism can be described as follows: The CG of T_1 is tuning the operation mode of the high-side transistor, resulting in its function as a resistive load or operation in NDR-mode. Moreover, the low-side transistor, T_2, is hardwired to operate constantly in NDR-mode with $V_{PG} = V_{CG} = 5\,V$. As it becomes evident in the NDC map, shown in Figure 4.54(b), for a V_{CG} up to ~1 V, the NDR region allows to be shifted, due to increased resistance of T_1, resulting from a progressive shift towards more dominant electron conduction mode. However, further increasing V_{CG} at T_1 leads to the exhibition of NDR due to efficient electron injection and, therefore, to an overlapping NDR region. The "double" NDR is achieved due to the fact that in the scenario of $V_{CG} > 1.75\,V$, both transistors are operated in electron conduction mode, i.e., NDR-mode.

Similarly to the cascode circuit with single TG Al-Ge based SBFETs, the quasi-ohmic junction properties of the Al-Ge MSJ in *p*-type operation enables the functionality of "double"-NDR, in particular, for the operation of T_1.

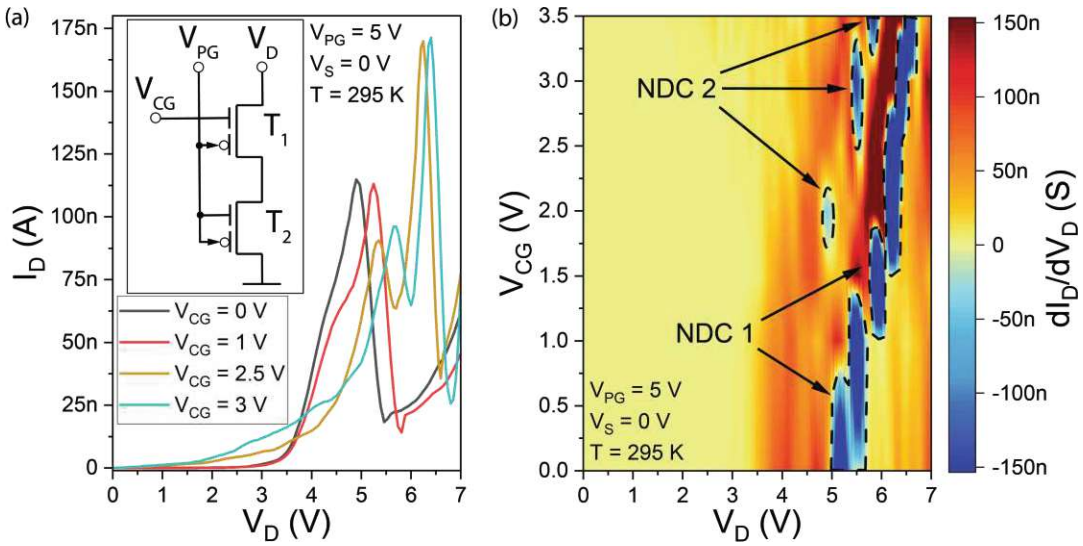


Figure 4.54: *(a) Cascode circuit of two Al-Ge based multi-gate SBFETs, enabling tunability and the construction of a double NDR. In correlation to the cascoded Al-Ge based single top gated SBFET, the low-side device, i.e., T_2, is operated in NDR mode, whereas T_1 allows switching between quasi-ohmic and NDR operation. (b) Derived NDC map from data of (a). Notably, two distinct NDC regimes become evident.*

Using an RFET multi-gate configuration with PG and CG and creating **bias-dependent transport maps, reveals that a V_{CG}-dependent shift of the NDR region can be obtained**, while the applied V_{PG} **merely defines the onset of the transferred electron effect**. Additionally, using **a cascode circuit of multi-gate Al-Ge based SBFET allows the realization of a "double"-NDR characteristic**, which again enables tunability in correlation to the applied V_{CG}.

4.5 Approaching Top-Down Integration

As discussed in Section 2.1.3, VLS-grown bottom-up NWs bear significant challenges in precise placement and wafer-scale integration, resulting from their predefined positioning, related to the growth mechanism. Therefore, as already mentioned, top-down approaches, e.g., based on Ge- (GeOI) or Si on insulator (SOI), depict a promising solution for highly integrated circuits, which certainly becomes relevant for more complex reconfigurable logic gates. [244, 245]
In the scope of Al-group IV material systems, Wind et al. demonstrated the proposed solid-state exchange mechanism on the basis of Al-Ge [162] and Al-Si [RB2] top-down fabricated nanosheets from GeOI and SOI, respectively. In this context, Böckle et al. used the Al-GeOI material system for the demonstration of the first top-down realized Al-Ge based RFET. [236] Attributed to the gained insights on the T-dependent charge carrier transport mechanism, in particular of the Al-Ge material system (cf. Section 4.2.3), due to its T-independent hole injection and its strong T-dependency for electron injection, this temperature characteristic can be exploited in a device with a tunable temperature coefficient of resistance (TCR). In this context, Bartmann et al. demonstrated the realization of a Ge NW-based microbolometer with TCR = 1.7 %/K at RT. [312] However, NW-based solutions exhibit limitations with respect to integration and exact placement, which inhibits its industrial and wafer-scale integration. [136] With respect to the realizations of devices with a high TCR, i.e., thermometers, top-down nanosheets allow for a distinct design of the thermal conductance of the Ge channel and metal contacts (here: Al) by engineering the nanosheet's width and thickness. Additionally, GeOI provides the capability of fabricating parallel wires to increase currents. [313, 314]

This section covers the publication "Bias-tunable temperature coefficient of resistance in Ge transistors". [RB8]

4.5.1 Tunable TCR on GeOI

As briefly mentioned in the introduction of this section, Al-Ge MSJs provide a favorable T-sensitivity, resulting from the Ge's relatively small band gap and a high intrinsic charge carrier concentration (cf. Section 2.1.2). Therefore, passive Ge bolometers are widely used for infrared detection due to their excellent TCR over a wide range of temperatures. [315–317] In this context, Ge-based bolometers were proposed, which, however, require complex fabrication methodologies, but exhibit high TCR values between 1 %/K and 6 %/K in dependence on doping and crystallinity. [317–319] A significant drawback is that many Ge-based thermometers are often limited to operation in the liquid-He T-regime ($T = 4\,\mathrm{K}$). [320, 321]

In the scope of the work at hand, Al-Ge based SBFETs are considered, which rely on the T-dependent charge carrier transport mechanism elaborated in Section 4.2.3. In this context, Schottky diodes for bolometric applications were already demonstrated but were limited to Si-based technology with TCR values of ~2 %/K at RT. [322, 323]

For the proposed Al-Ge based SBFET, adapted as a TCR device, i.e., thermometer, the starting material was a GeOI wafer with a 75 nm (100)-oriented intrinsic and nominally undoped Ge device layer on top of a 150 nm thick buried oxide layer and Si handle wafer [cf. Figure 4.55(b)]. Nanosheets were then patterned with a thickness of 20 nm and a width of ~265 nm by e-beam lithography (EBL) and reactive ion etching (RIE). Notably, the native Ge_xO_y was desorbed to prevent the formation of Ge oxides, resulting in transiently more stable device operation, due to a reduced number of interface trap states. [262, 288] In this context, desorption of the native Ge_xO_y was performed in ultra-high vacuum (1×10^{-10} mbar base pressure) at 600 °C for 30 min. As illustrated in Figure 4.55(d), the success of the Ge_xO_y was confirmed by X-ray photoemission spectroscopy (XPS) analysis on a Ge(100) test substrate. As gate dielectric, a 11 nm thick Al_2O_3 layer was deposited by ALD. Next, Al source/drain pads were fabricated by optical lithography, selective oxide etching, Al sputter deposition, and lift-off techniques (cf. Section 3.1). In the same manner, as it was applied to obtain Al-Ge-Al NW heterostructures, the Al-Ge exchange mechanism was initiated by RTA at 673 K. [162] For the realization of a TCR device, exhibiting a distinct T-dependency, a channel length above the mean free path in Ge (> 45 nm) is desired to prevent a high contribution of T-independent ballistic charge carriers. [64] Consequently, Ge channel lengths between 400 nm and 1000 nm were targeted. Finally, for the realization of the SBFET, a Ti/Au (10 nm/100 nm) top gate (TG) was fabricated by EBL and evaporation. For efficient electrostatic gating capabilities of the Ge energy landscape, a sufficient overlap of the MSJs has to be considered. Figure 4.55(a) shows a false-color SEM image of the thereof realized device, wherein the zoomed-in view, the actual TG and Ge channel are illustrated. Moreover, Figure 4.55(b,c) show schematically vertical and horizontal cross-section views of the device stack. Finally, the gate and drain electrode were bonded together to realize a two-terminal device promoting a diode characteristic (cf. Figure 4.56). In this context, two electrostatically tunable Schottky junctions, with Al being the anode and Ge being the cathode, are realized. Consequently, similar physical transport mechanisms are obtained, as proposed in other Schottky diode based thermometers for bolometric applications. [323] However, in the proposed Al-Ge based SBFET, different device operation modes can be set, further enhancing the device concept.

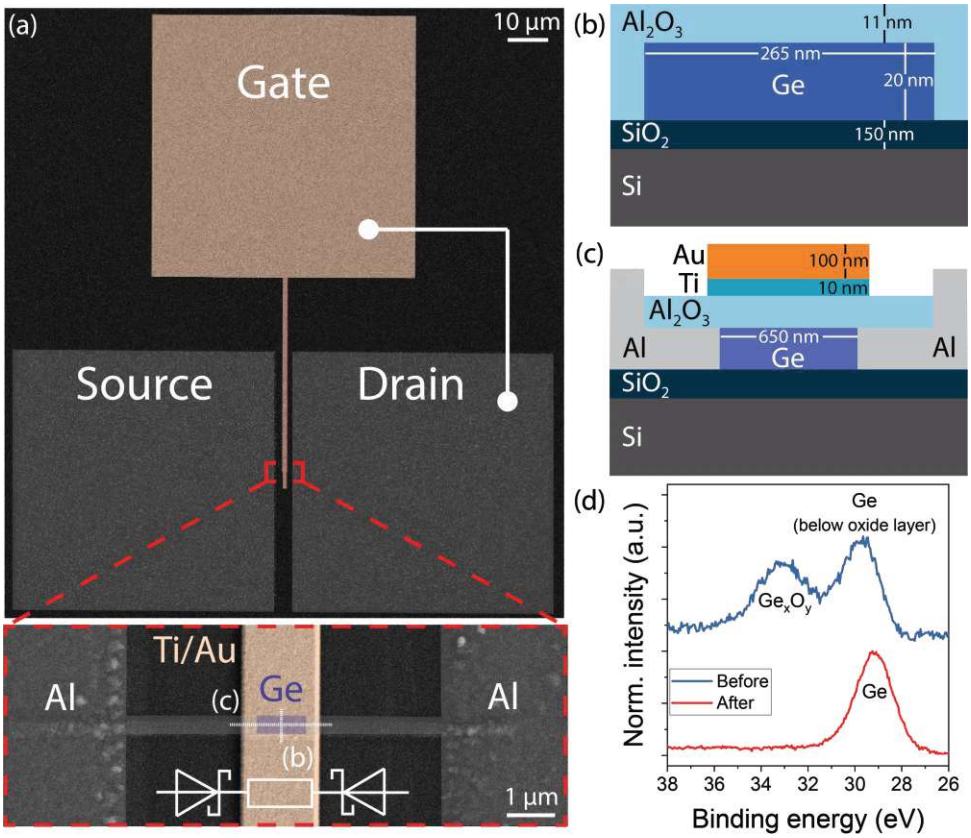


Figure 4.55: *(a) False-color SEM image of the Al-Ge based SBFET, fabricated from GeOI, with indicated wiring between the gate and drain electrodes. The lower image shows a zoomed-in view of the SBFET, where the two Schottky diodes and resistor symbol illustrate the Al-Ge junctions and Ge channel, respectively. (b,c) Schematic vertical and horizontal cross-section cuts of the device stack. Note that dimensions are not in scale. (d) XPS data before (solid blue) and after (solid red) Ge_xO_y desorption.*

In the first step, the I/V characteristic at RT of the Al-Ge based SBFET with the connected gate and drain electrodes is investigated. Figure 4.56 shows the corresponding I/V data for sweeping $V_D = V_{TG}$ from 2.5 V to −2.5 V and additionally setting $V_S = 0$ V (cf. Figure A.11). Attributed to the incorporated Schottky junctions and the simultaneous shift of the drain potential and the Ge's energy landscape (cf. insets in Figure 4.56), a diode characteristic becomes evident. In contrast, operating the device as a SBFET, without an electrical connection between the gate and drain electrodes, the device exhibits a quasi-ambipolar transfer characteristic (cf. Section 4.2.3). Moreover, the wired gate-drain configuration exhibits a vertical symmetry axis at $V_D = V_{TG} = 0$ V, as merely one charge carrier type can be injected, resulting from the electrical connection between the gate and drain electrode.

In the proposed device, the forward diode operation is evident in the hole-dominant regime at $V_D = V_{TG} < 0\,V$, whereas reverse operation is obtained in the electron-dominant regime at $V_D = V_{TG} > 0\,V$. In this context, strong Fermi level pinning close to the valence band of Ge in the Al-Ge material system leads to the observed characteristic, discussed in detail in Section 4.2.3. Furthermore, charge carrier injection by thermionic emission (TE) and field emission (FE) needs to be taken into account, where especially in the *p*-branch, the current increases steadily due to TE and a low activation energy E_a^p. Notably, in the hole dominant regime merely the Schottky junction at the drain needs to be considered, as the injection Schottky junction at the source is fully transparent. Consequently, the hole current at $V_D = V_{TG} < 0\,V$, is also influenced by the corresponding width of the space charge region, which can be tuned by dimension properties, such as, e.g., gate geometry, oxide thickness, and material, affecting the tunneling probability. [RB9] In the *n*-branch at $V_D = V_{TG} > 0\,V$, it can be speculated that TE is the dominant contributor of electron injection, as the barrier thickness is too wide within the observed voltage range, and thus hinders efficient FE. Consequently, the current I_D remains relatively constant in the observed range between $V_D = V_{TG} = 0.5\,V$ and $2\,V$ with $I_D = 18\,nA$ and $32\,nA$, respectively. Moreover, this relatively constant I_D further supports the limiting dominance of a *n*-type SB, where electrostatically tuning the energy landscape of Ge does not necessarily lead to higher currents. Considering the discussed charge carrier transport mechanism in the scope of thermometers, TE is a highly T-dependent transport mechanism, which is accessed in terms of achieving high TCR values, as discussed next.

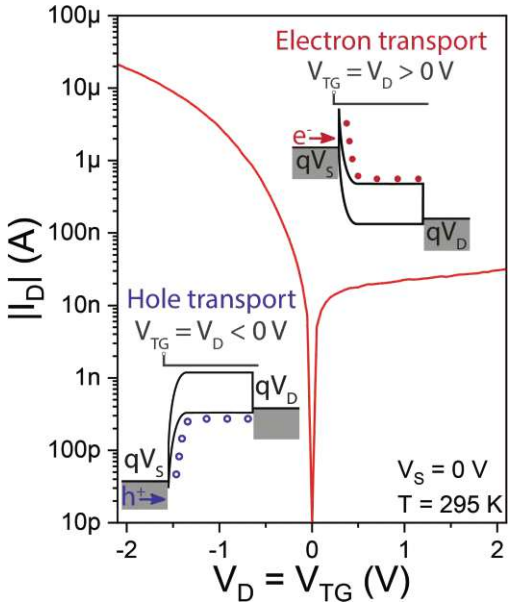


Figure 4.56: *I/V characteristic at $T = 295\,\mathrm{K}$ illustrating a diode characteristic of the Al-Ge based SBFET, which is operated in forwards direction for hole transport ($V_\mathrm{D} = V_\mathrm{TG} < 0\,\mathrm{V}$) and in reverse operation (diode saturation) for electron transport ($V_\mathrm{D} = V_\mathrm{TG} > 0\,\mathrm{V}$). The insets schematically illustrate simplified band diagrams for both charge carrier transport mechanisms.*

Next, the I/V characteristic of the wired gate-drain Al-Ge based SBFET is investigated for varying the temperature between 77.5 K and 400 K, as illustrated in Figure 4.57. Note that I_D at low temperatures, i.e., 77.5 K to 100 K, in the n-branch cannot be resolved, as values are below the resolution limit of the used measurement equipment (cf. Section 3.2.1). In the p-branch at low $V_\mathrm{D} = V_\mathrm{TG}$, a particular T-dependency is evident, which can be attributed to dominant TE of holes. However, approaching $V_\mathrm{D} = V_\mathrm{TG} = -2\,\mathrm{V}$ leads to a FE-dominant charge carrier (here: holes) injection due to stronger band bending and thinner barriers. Consequently, the T-dependency vanishes in strong hole accumulation (cf. Section 4.2.3). In contrast, in the n-branch a distinct n-type SB is evident, resulting in TE being the limiting charge carrier (here: electrons) injection mechanism. Consequently, a strong T-dependency of I_D becomes evident. As indicated in Figure 4.57, between $\Delta T = T_2 - T_1$ a $\Delta I_\mathrm{D} = 86.5\,\mathrm{nA}$ in the T-range of 125 K-400 K is extracted. The mechanism itself, leading to a change in I_D, can be attributed to thermally activated electrons, overcoming the n-type SB by TE. Evaluating the temperature range between 350 K and 400 K a ΔI_D of 20 nA is observed. In this context, the current I_D needs to be considered in respect to resistance R, where TCR is defined as $1/R_0 \times dR/dT$, with $R_0 = V_\mathrm{D}/I_\mathrm{D}$ being the resistance at the operation temperature and dR/dT being the resistance change per K.

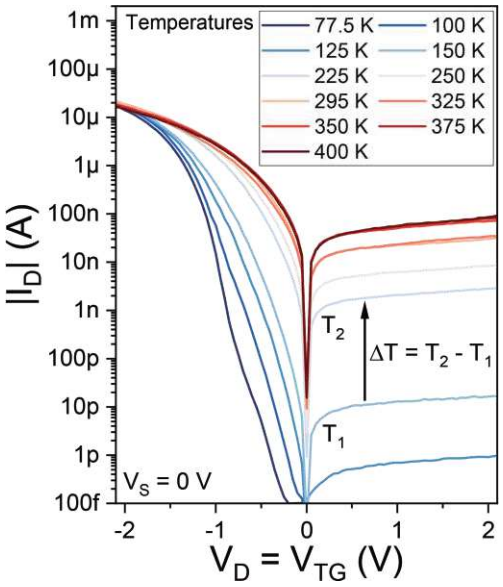


Figure 4.57: *I/V characteristics of the proposed Al-Ge based SBFET for temperatures ranging from* 77.5 K *to* 400 K*. Notably, a strong T-dependency becomes evident for* $V_\mathrm{D} = V_\mathrm{TG} > 0\,\mathrm{V}$ *(n-type conduction) due to a distinct n-type SB and dominant TE charge carrier transport.*

Finally, Figure 4.58 shows the extracted TCR values in dependence on $V_\mathrm{D} = V_\mathrm{TG}$ of the Al-Ge based SBFET with gate-drain wired electrodes. On the basis of previously discussed expressions, the TCR can be calculated according to the following equation:

$$\begin{aligned}\mathrm{TCR} &= \frac{1}{\Delta T}\frac{R_\mathrm{DS}(T_2) - R_\mathrm{DS}(T_1)}{R_\mathrm{DS}(T_1)} = \frac{1}{\Delta T}\frac{R_\mathrm{DS}(T_2)}{R_\mathrm{DS}(T_1)} - 1 \\ &= \frac{1}{\Delta T}\frac{V_\mathrm{D}/I_\mathrm{D}(T_2)}{V_\mathrm{D}/I_\mathrm{D}(T_1)} - 1 = \boldsymbol{\frac{1}{\Delta T}\frac{I_\mathrm{D}(T_1)}{I_\mathrm{D}(T_2)} - 1},\end{aligned} \tag{4.3}$$

where ΔT is the considered temperature range (cf. Figure 4.57) and $R_\mathrm{DS}(= V_\mathrm{D}/I_\mathrm{D})$ is the total resistance of the device, consisting of the Schottky junction resistances and the Ge channel resistance. In this context, the Schottky junctions are the main limiting factor, due to their direct influence on the charge carrier injection capabilities, which particularly holds for the n-type SB. In strong hole accumulation ($V_\mathrm{D} = V_\mathrm{TG} < 0\,\mathrm{V}$), the Ge channel becomes the resistance-defining element, due to the quasi-ohmic contact properties of the Al-Ge MSJ (cf. Section 4.2.3).
Finally, a bias-tunable TCR is achieved, which facilitates the T-dependent and -independent properties, wherein the temperature range of 125 K-150 K a value of $-0.3\,\%/\mathrm{K}$ at $-2\,\mathrm{V}$ and $-3.8\,\%/\mathrm{K}$ at $2\,\mathrm{V}$ is achieved. Notably, negative TCR values are extracted as the resistance in the proposed Al-Ge based SBFETs decreases for elevated temperatures, which is a characteristic feature of most semiconductors. [17] According to Fermi-Dirac statistics, increasing the temperature leads to more thermally excited charge carriers, resulting in more occupied states, resulting in lower TCR values.

Nevertheless, even in the temperature range between 250 K and 295 K, maximum TCR values in the *n*-branch of −1.6 %/K are achieved. Consequently, promoting RT-operability of the proposed Al-Ge based SBFET with wired gate and drain electrodes for thermometer applications.

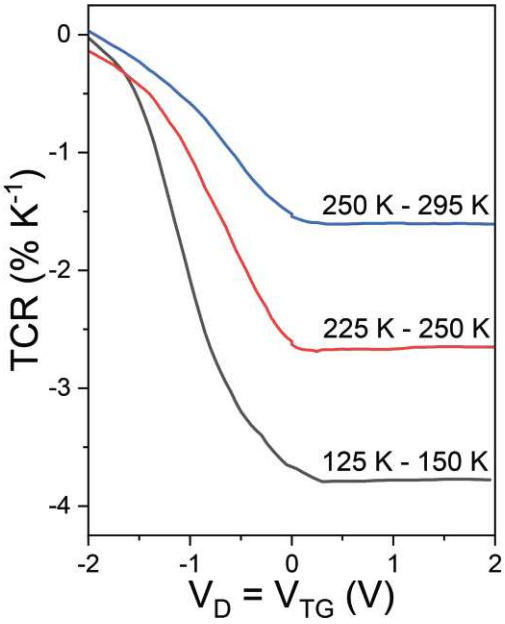


Figure 4.58: *Selected TCR data extracted from I/V characteristics acquired at different temperatures (cf. Figure 4.57), demonstrating the bias-tunability of TCR. Notably, in the n-branch, the TCR remains constant due to the operation of the diode characteristic in reverse direction. In contrast, in the p-branch the TCR approaches zero, due to dominant FE.*

Notably, the proposed Al-Ge based SBFET with wired gate and drain electrodes allows for nanoelectronic co-integration approaches due to its bias-tunable TCR. In this context, operating the device as a *p*-type transistor and consequently with a TCR of ~0 %/K, as desired in nanoelectronic applications, a versatile platform is realized. Consequently, transistors or even logic gates on the basis of the GeOI platform can be realized in conjunction with thermometers for bolometric applications. Moreover, enhanced functionality might be achieved by pulsed operation to reduce Joule heating or the fabrication of parallel nanosheets that allow for direct addressing in detector arrays.

Due to the exhibition of similar *n*- and *p*-type SBs in the Al-Si material system, first TCR results based on SOI are acquired as well, considering the same architecture and measurement methodology. Therefore, preliminary results are shown in Appendix B.

Using Al-Ge based SBFETs and inter-connecting the gate and drain electrode, the device is **operated as a thermometer, exhibiting a bias-tunable TCR.** Consequently, the two-terminal device exhibits a **diode I/V characteristic, which shows a distinct T-dependency** for electron and hole conduction. In the proposed configuration, a **bias-tunable TCR with values between -0.3 %/K and -3.8 %/K** was achieved in the p- and n-branch. **At RT a maximum TCR value of -1.6 %/K was extracted**.

Chapter 5

Conclusion and Outlook

In summary, the presented PhD thesis is a systematic experimental study of NW-based Al-Si, -$Si_{1-x}Ge_x$ and -Ge metal-semiconductor-metal heterostructures integrated into single and multi top gated SBFETs. Therefore, structural and electrical analyses were conducted to thoroughly understand the incorporated MSJs and the involved charge carrier transport mechanisms dependent on the integrated semiconductor channel materials. Al-group IV-based SBFETs exhibit ambipolar transfer characteristics, resulting from specific and important n- and p-type SBs that are, in turn, caused by unique Fermi level pinning properties at the junctions. In this context, certain SBFET FOM, such as $I_{\mathrm{on}}^{\mathrm{n/p}}$, $V_{\mathrm{th}}^{\mathrm{n/p}}$, the hysteresis, $S^{\mathrm{n/p}}$ and $g_{\mathrm{m}}^{\mathrm{n/p}}$ were acquired. Taking the SBFET's dimensionality into account and considering the same Al-lead properties allowed a comprehensive comparison of the electrical performance of the different channel material systems. Applying advanced characterization methodologies, such as bias- and T-dependent spectroscopy, identified distinct operation regimes dependent on the charge carrier injection mechanisms. An essential aspect of the obtained MSJs was the determination of the n- and p-type "effective" SBHs, denoted as activation energies $E_{\mathrm{a}}^{\mathrm{n/p}}$, which are significantly influencing the charge carrier injection and transport. In this respect, the major contributor was determined to be the Fermi level pinning between the metal (here: Al) and the corresponding semiconductor. For the extraction of $E_{\mathrm{a}}^{\mathrm{n/p}}$, the 3D TE model was applied to all investigated material systems, whereas for the Al-Ge material system also, the 1D LB model was used. In this context, justification is given due to the diameter of the Ge NWs being in the order of the exciton Bohr radius $a_{\mathrm{B}}^{*} = 24.3\,\mathrm{nm}$.

After identifying and characterizing distinct charge carrier transport mechanisms in the different Al-group IV based SBFETs, the gained insights were applied to realize specific nanoelectronic applications. In this context, the Al-Si material system exhibited favorable characteristics in terms of relatively symmetric n- and p-type SBHs, which are essential for realizing RFETs. Moreover, using these Al-Si based RFETs allowed the demonstration of basic logic circuits, such as an inverter and wired-AND gate. On the base of the Al-Ge material system, using multi-gate SBFETs and cascode circuits enabled tunability of the NDR region and even showed the exhibition of a "double" NDR feature, as visualized by bias spectroscopy. Moreover, in the Al-Ge material system, attributed to distinct T-dependent and -independent charge carrier injection in the n- and p-type operation mode, respectively, a bias-tunable TCR device, based on top-down fabricated nanosheets from GeOI, was demonstrated.

In the following, the stated research questions are reflected, where the most critical insights in correspondence to Section 1.1 are highlighted. Additionally, an outlook on potential enhancements concerning the research questions is discussed. Note that the corresponding outlook topics are highlighted in the individual parts.

Characteristics of Al-group IV heterojunction in SBFETs

At first, in Section 4.1, the structural properties of the fabricated Al-Si, -$Si_{0.5}Ge_{0.5}$, and -Ge NW metal-semiconductor-metal heterostructures were investigated, which were achieved by the use of RTA to initiate a solid-state exchange mechanism between Al and the corresponding un-doped VLS-grown group IV NW. For a thorough analysis of the thereof obtained MSJs BF and HAADF STEM, as well as EDX methodologies, were used for imaging. As passivation, also acting as gate dielectric, native thermally grown SiO_2 was used for the Si NWs, whereas the Al-$Si_{0.5}Ge_{0.5}$ and -Ge NWs were coated via ALD Al_2O_3. Importantly, in all investigated Al-group IV material systems, single-crystalline and mono-elementary Al leads connected to the semiconductor were achieved without forming inter-metallic phases. Moreover, no inter-diffusion between Al and the group IV semiconductors was detected in the resolution limits of the STEM system.
Using electrical characterization methodologies allowed a comprehensive comparison of the different top-gated Al-group IV SBFETs, where the fabricated Ω-shaped TG covers the semiconductor channel and overlaps both MSJs. Consequently, specific charge carrier transport mechanisms were identified. In this context, the Fermi level pinning plays a crucial role for each material system, as discussed below.

Al-Si material system

Analyzing the Al-Si interface from a structural point of view revealed a ⟨111⟩-oriented V-shaped twin interface, although initially un-doped ⟨112⟩-oriented Si NWs were used. Notably, this structural characteristic was already observed in ⟨112⟩-oriented Si NWs in the past. [282]

Investigating the charge carrier transport in Al-Si based SBFETs showed a relatively symmetric $I_{\mathrm{on}}^{\mathrm{n}}/I_{\mathrm{on}}^{\mathrm{p}}$ of 0.65 without introducing any additional measures, such as strain engineering. In terms of $E_{\mathrm{a}}^{\mathrm{n/p}}$, similar electron and hole injection capabilities were extracted, resulting from Fermi level pinning of Al close to the middle of the Si band gap. Consequently, similar *n*- and *p*-type SBs are evident, enabling the observed symmetry in the Al-Si material system.

Al-$Si_{0.5}Ge_{0.5}$ material system

Non-flat MSJs in the Al-$Si_{0.5}Ge_{0.5}$ material system were observed, where EBIC investigations were carried out in addition to map the space charge regions of the obtained Schottky junction. In this respect, widths of ~300 nm were extracted.

From an electrical perspective, the Ge-content highly influences the charge carrier transport mechanism due to dominant *p*-type behavior. In this context, the Fermi level pinning shifts towards the valence band of $Si_{0.5}Ge_{0.5}$, due to a significant incorporation of Ge. In particular, at elevated temperatures $T > 295\,\mathrm{K}$, linear output characteristics were extracted, indicating quasi-ohmic contacts for the injection of holes.

Al-Ge material system

Concerning the Al-Ge MSJ, which was investigated thoroughly in the past, a technological break-through in terms of preventing the formation of native Ge oxides is the use of a diphenylgermane precursor (DPG) for the bottom-up NW VLS growth, terminating the Ge surface with phenyl ligands. In this respect, the I/V hysteresis is significantly reduced, allowing the realization of transiently stable SBFETs and device realizations, i.e., NDR devices.

In the Al-Ge material system, a pre-dominant *p*-type conduction mode became evident, where near-zero and slightly negative $E_{\mathrm{a}}^{\mathrm{p}}$ values were extracted, indicating quasi-ohmic junction properties for the injection of holes. This is further proven by *T*-independent linear output I/V characteristics over the investigated temperature range between 77.5 K and 400 K.

The following gives an outlook that would further contribute to a better understanding and improvement of Al-group IV NWs and the obtained heterojunctions.

- **Insights on the NW surface crystal orientation**
  In terms of the band structure, as well as the density of interface trap states D_{it}, the NW surface crystal orientation is of high relevance, as discussed in Section 2.1.3 and proposed in Reference [49] by Weber et al.

As an outlook, a NW would need to be cut radially, e.g., by a focused ion beam, revealing the crystal orientation of each NW facet. Using similar STEM techniques as proposed in Section 4.1 would then allow to evaluate distinct surface crystal orientations.
Consequently, the lowest D_{it} values and highest effective charge carrier mobilities can be expected in correspondence with the NW surface crystal orientation as shown in Reference [153].

- **Single-source precursor for the growth of $Si_{1-x}Ge_x$ NWs**
  Comparing the hysteresis of the Al-$Si_{0.5}Ge_{0.5}$ and Al-Ge based SBFETs revealed values of 0.7 V/2 V and 0.16 V/0.65 V for the *n*- and *p*-branch, respectively. In this context, the higher hysteresis evident in the Al-$Si_{0.5}Ge_{0.5}$ material system might be attributed to the use of silane and germane as growth precursor, lacking surface passivation and thus promoting the formation of native Ge oxides. Similarly, as proposed for the Ge NW growth, using DPG as a precursor, a single-source precursor could be used for the $Si_{1-x}Ge_x$ NW VLS-growth, which prevents the formation of Ge_xO_y. Behrle et al. proposed a first principle, which led to as-grown $Si_{1-x}Ge_x$ NWs with an Au-decorated surface,[1] where Au surface diffusion from the substrate caused the formation of an Au shell during the NW growth. [RB10] Using an oxidation/etching procedure allowed the removal of the Au-shell, which, however, comes with the drawback of a rougher NW surface. For a thorough understanding, further efforts are required in the precursor development and the evaluation of the thereof obtained D_{it}.

Applying advanced characterization methodologies

Using thermally grown SiO_2 as gate dielectric for the Al-Si based SBFETs and using DPG as a precursor for the Ge NW growth enabled transiently stable Al-Si and -Ge based SBFETs, which promote the application of bias spectroscopy. Notably, analyzing I_D, g_m, and E_a maps allow to gain essential insights on the charge carrier injection and transport mechanisms in dependence on the manifold influences evident in SBFETs, which are not accessible by single parameter sweeps. In this context, T-dependent bias spectroscopy to create I_D maps allows didactically identifying involved transport mechanisms, such as TE, TFE, and FE. Moreover, deriving g_m maps revealed a degradation and exhibition of g_{m-max} in the case of quasi-ohmic contacts. The g_m degradation can be attributed to the dominance of the semiconductor channel resistance in comparison to junctions and became, in particular, evident in Al-$Si_{1-x}Ge_x$ and -Ge based SBFETs, due to Fermi level pinning close to the valence band of $Si_{1-x}Ge_x$ and Ge.

[1] The single-source precursor development and $Si_{1-x}Ge_x$ NWs with the Au-decorated surface growth was performed by Dr. Sven Barth at the Physics Institute, Goethe Universität Frankfurt, Germany.

In the scope of Ge-based NDR devices and, thereof, built cascode circuits, T-dependent bias spectroscopy provides an essential tool to investigate the influence of the temperature, the electrostatic gating, and the applied bias on the exhibition of NDR. Attributed to the transferred electron effect, which is leading to NDR in Al-Ge based SBFETs, the manifold transport features can be visualized in a single plot, which cannot be accessed by individual I/V characteristics. In particular, T-dependent NDR shifting in conjunction with the applied gate bias in the case of multi-gate Al-Ge based SBFETs, allows a thorough understanding of the NDR tunability in the proposed devices and cascode circuits.

As an outlook, the following bullet points elaborate on potential characterization methodologies, which would allow to gain additional insights into the proposed Al-group IV based SBFETs.

- **Low-frequency noise in Al-group IV based SBFETs**
  In the past, low-frequency noise (LFN) analysis has proven to be a useful methodology to gain insights on surface trapping and scattering mechanisms in NW-based transistors. [148] In this respect, Behrle et al. conducted first investigations on back-gated Al-Ge-Al NW heterostructures, considering VLS-grown and nominally undoped Ge NWs grown with a germane precursor. [RB11] Attributed to the Ge_xO_y/Al_2O_3 gate stack and the back gated SBFET architecture, a distinct transient instability is observed. Thus, the use of native Ge_xO_y (cf. Section 2.1.2) and the BG architecture, became evident. Nevertheless, LFN results were similar to those of other Ge-based transistors, demonstrating the feasibility of the methodology. [324, 325] In this context, using LFN analysis allows the extraction of the so-called Hooge parameter α, being a dimensionless indicator to compare the noise intensity in different semiconductor materials and devices. Moreover, LFN analysis enables the extraction of D_{it}, which is otherwise inhibited by conventional C/V measurements due to low capacitance values in the proposed NW-based SBFETs (cf. Section 2.1.3).

  As an outlook, applying LFN analysis, particularly on Ge NWs grown with the DPG precursor, would allow a direct comparison of the Hooge parameter and D_{it}, considering the same crystal orientation and gate material stack. Moreover, the use of an Ω-shaped TG allows fully gating the entire active region and should allow the exclusion of any influences on the trapping mechanisms caused by ambient conditions, i.e., adsorption of molecules on the NW surface. Furthermore, LFN analysis would enable investigations and comparisons of advanced high-κ gate dielectrics, such as, e.g., HfO_2, ZrO_2, or its combination HZO, which are highly anticipated for the fabrication of ferroelectric gate stacks [326]. In this respect, scaling, i.e., approaching an EOT of 1 nm and below to further reduce the gate capacitance and decrease voltage levels for sufficient electrostatic gating, is targeted.

- **In-situ MSJ formation and bias temperature instability**
  To gain further valuable insights on the formation of the obtained Al-group IV MSJs, in-situ STEM heating experiments, as already demonstrated on the Al-Ge [59] or Al-$Si_{1-x}Ge_x$ [265] NW-based material systems are required for a better understanding of the junction formation. Recently, similar investigations have been carried out on top-down fabricated Al-Si junctions. [327] Additionally, to assess stability during operation, analysis concerning to electromigration is required for a better understanding of the long-term performance and variability of the proposed devices. [88] In this respect, sufficiently high currents and stress factors at the metal-semiconductor-metal heterojunctions need to be considered, which in turn leads to an increase in the junction temperature at the metal-semiconductor interface. Attributed to the thermally induced solid-state exchange mechanism, this accelerated testing procedure might cause structural changes in the metal and/or semiconductor. [328]
  A recent work entitled "Reliability of Reconfigurable Field Effect Transistors: Early Analysis of Bias Temperature Instability" (presented at IPFA'24) by Galderisi et al. elaborates on first principles for investigating bias temperature instability in RFETs, [329] which might be of significant relevance in terms of considering low- and high-temperature charge carrier transport in the proposed Al-group IV SBFETs and its effects on the threshold voltages.

Utilizing Al-group IV SBFETs for emerging devices

Applying the gained insights on the structural and electrical characteristics of the Al-Si, -$Si_{1-x}Ge_x$ and Ge based SBFETs, allowed the derivation of specific nanoelectronic applications, which are summarized in the following.
Attributed to the symmetric nature of the *n*- and *p*-type SBs in the Al-Si material system, the first Al-Si based RFET and realized basic logic circuits were investigated. In this context, a three TG RFET architecture was used to dynamically switch between *n*- and *p*-type operation, achieving a I_{on}^{n}/I_{on}^{p} ratio of 0.4 without the introduction of additional measures. Notably, the symmetry also gets evident in $V_{th}^{n/p}$ with values of 0.36 V and −0.7 V, exhibiting a ratio of ~2 and $S^{n/p}$ with values of 280 mV/dec and 290 mV/dec. Using output I_D maps enabled the evaluation of an optimal operation point for the realization of a complementary inverter where a symmetric supply line of |3 V| was determined. Therefore, two RFETs in series, implemented on a single NW, where the low-side RFET is operated in *n*-type operation and the high-side RFET in *p*-type operation, constitute the proposed inverter. Further highlighting the flexibility of the Al-Si based RFET, a wired-AND gate with a dual CG device architecture was realized. Notably, such multi-CG RFETs depict a solution towards reducing the transistor count in logic circuits, e.g., NAND gates. Importantly, the demonstrated Al-Si based RFET exhibits a high degree of flexibility that is favorable for the implementation of reconfigurable electronics.

The realized logic gates feature a high potential for co-integration with CMOS technology and might provide an essential step towards "Beyond CMOS" concepts enabling diversification and alternative computing paradigms.
Using an RFET gating architecture on the Al-Ge based SBFETs allows distinct tunability of the NDR region. In this context, the PG voltage enables modulation of the PVR, whereas the CG voltage enables shifting of the NDR region with respect to the applied bias voltage. Further, integrating these multi-gate Al-Ge based SBFETs in a cascode circuit achieves an I/V characteristic exhibiting a "double" NDR feature. In the scope of "Beyond CMOS" technology, the proposed Al-Ge based NDR devices exhibit a CMOS-compatible add-on platform for the realization of logic functions, e.g., based on MOBILE or MVL concepts, [81, 82] and even reconfigurable electronics [219].
Due to the T-dependency of distinct charge carrier transport mechanisms, in relation to the n- and p-type SB, a two-terminal device, i.e., a SBFET with connected gate and drain electrodes, was adapted as a thermometer and characterized in terms of TCR. Notably, connecting the gate and drain electrodes of the Al-Ge based SBFET enables a diode characteristic, where in reverse operation (electron dominant regime), T-dependent TE dominates. In contrast, in forward operation (hole dominant regime), a weak T-dependency due to FE, associated with strong Fermi level pinning close to the valence band of Ge, is evident. Consequently, bias-dependent TE and FE charge carrier transport mechanisms can be set, reaching TCR values between $-0.3\,\%/\mathrm{K}$ and $-3.8\,\%/\mathrm{K}$ in the temperature range of 125 K to 150 K. Importantly, in the hole dominant regime, a TCR of near $0\,\%/\mathrm{K}$ is achieved, which is a desired property for transistor and logic gate applications. Further, this leads to the possibility of co-integration paradigms on the same platform, whereas merely the applied bias determines its functionality.

Attributed to the use of NWs and its associated drawbacks in deterministic and precise positioning as well as large-scale integration feasibility, the following discusses latest insights on Al-group IV top-down integration approaches.

Top-down fabrication of SBFETs
As introduced in Section 2.1.3, NWs bear a particular challenge regarding precise positioning on the substrate, hindering extensive circuit integration. Therefore, in the scope of the PhD thesis at hand, Section 4.5.1 proposes a device realization based on nanosheets fabricated from GeOI. A significant advantage of this top-down approach is the flexible positioning of the fabricated nanosheets, which further supports the realization of more complex circuits and their wafer-scale integration. Another essential advantage is the capability of developing self-aligned processes as already established for the NiSi-Si material system. [330]
In the scope of top-down fabricated Al-group IV based SBFETs, Wind et al. demonstrated the solid-state exchange mechanism on Al-Si nanosheets based on SOI [RB2] and on Al-Ge nanosheets [162] fabricated from GeOI.

In particular, on the basis of the Al-Si material system, due to its inherently symmetric *n*- and *p*-type SBs, [331] an RFET-based full adder was recently realized, demonstrating the potential to fabricate more complex logic circuits. [309] Concerning Al-$Si_{1-x}Ge_x$ and -Ge based SBFETs, Fuchsberger et al. achieved remarkable results in terms of on-current symmetry required for the realizations of RFETs. [332, 333] Therefore, a device architecture with molecular beam epitaxy grown $Si_{1-x}Ge_x$ and Ge layers on SOI wafers, which are capped with a thin Si layer, were used. Notably, the Si capping layer allows the fabrication of SiO_2 by thermal oxidation, preventing the formation of native Ge oxides. Moreover, applying a solid-state exchange mechanism by RTA leads to the formation of an Al-Si-Ge/$Si_{1-x}Ge_x$ multi-heterojunction, serving mid-gap Fermi level pinning due to the formation of a Si inter-layer between the Al and Ge/$Si_{1-x}Ge_x$. Consequently, Al-$Si_{1-x}Ge_x$ and -Ge based RFETs were realized, [332, 333] overcoming the issue of strong Fermi level pinning close to the valence band of $Si_{1-x}Ge_x$ and Ge, but accessing the enhancements provided by the use of Ge. Moreover, NDR in the proposed Al-Ge based SBFETs was exploited by Fuchsberger et al. as well, demonstrating a significant step towards reconfigurable NDR logic. [334]

Appendix A

Additional Insights on Al-Group IV SBFET

The following provides additional results and experiments obtained from investigations on the Al-Si and Al-Ge based SBFETs. Note that, if not otherwise stated, top gated SBFETs are considered. Additionally, supporting information concerning the Al-Si based RFET realization and its associated logic circuits is given.

A.1 Al-Si based SBFET

Fully exchanged Al-(Si) NW [RB2]
For extended annealing, the NW appeared to be composed of pure Al with a resistivity $\rho = (6.3 \pm 1.2) \times 10^{-8}\,\Omega\,\mathrm{m}$, which is less than three times larger than that of bulk Al [156] and can be attributed to a size effect given by the increased surface scattering in NWs compared to bulk. [335] Figure A.1 shows the resistivity of such Al NWs obtained from two-point I/V measurements in the temperature range between $T = 77.5\,\mathrm{K}$ to $400\,\mathrm{K}$. In agreement with the decrease of phonon scattering at lower temperatures of metals, [336] a decreasing resistivity of such Al NWs was found. Importantly, as the resistivity of the obtained Al NWs is approximately five orders of magnitude smaller compared to the used Si NWs, which have a resistivity of $\rho = (2.2 \pm 1.2) \times 10^{3}\,\Omega\,\mathrm{m}$, the parasitic resistance of the Al leads to the Si channel should be negligible. Further, remarkably high breakdown current densities of $J_{\mathrm{max}} = (1.0 \pm 0.1) \times 10^{12}\,\mathrm{A/m^2}$, comparable to Ni_xSi_{1-x}-Si NWs, were obtained. [166]

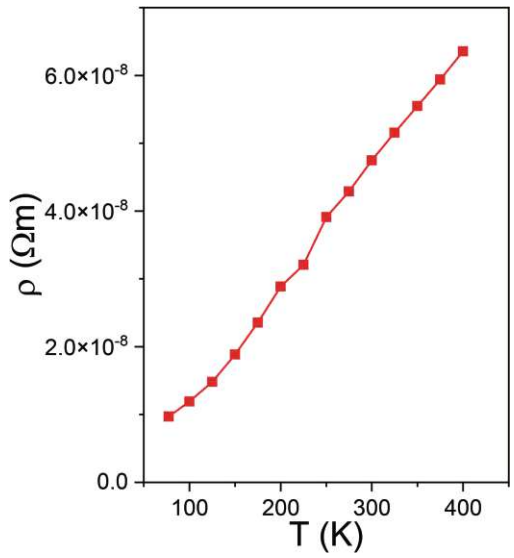


Figure A.1: *T-dependent resistivity ρ of an Al NW in the range from $T = 77.5\,\mathrm{K}$ to $400\,\mathrm{K}$ obtained from the proposed Al-Si exchange at $T = 773\,\mathrm{K}$. Attributed to a decrease in phonon scattering at lower temperatures in metals, [336] a lower resistivity is acquired at lower temperatures.*

Transfer characteristic of a back gated Al-Si based SBFET [RB2]
Figure A.2 shows a typical transfer characteristic at $V_{\mathrm{DS}} = 1\,\mathrm{V}$ and $T = 295\,\mathrm{K}$ of a back gated Al-Si based SBFET with a length $L_{\mathrm{SC}} = 1\,\mu\mathrm{m}$ and a diameter $d_{\mathrm{NW}} = 80\,\mathrm{nm}$. Sweeping the voltage at the back gate electrode V_{BG} first from $40\,\mathrm{V}$ to $-40\,\mathrm{V}$ and consequently back to $40\,\mathrm{V}$ reveals a distinct hysteresis, which is certainly higher in comparison to the top gated SBFET with hysteresis values in the $10\,\mathrm{mV}$-regime (cf. Section 4.1.1). The increase of the hysteresis can be attributed to charging effects and a different trap state behavior of the back gate oxide. [50, 337]

Transfer characteristics under pulsed V_{TG} conditions
Figure A.3 shows forwards and backwards sweeps of an Al-Si based SBFET under pulsed V_{TG} conditions with $1\,\mathrm{ms}$ and a base voltage of $0\,\mathrm{V}$. Hence, allowing to exclude any charging effects caused by the top gate. In this respect, no distinct hysteresis could be extracted.

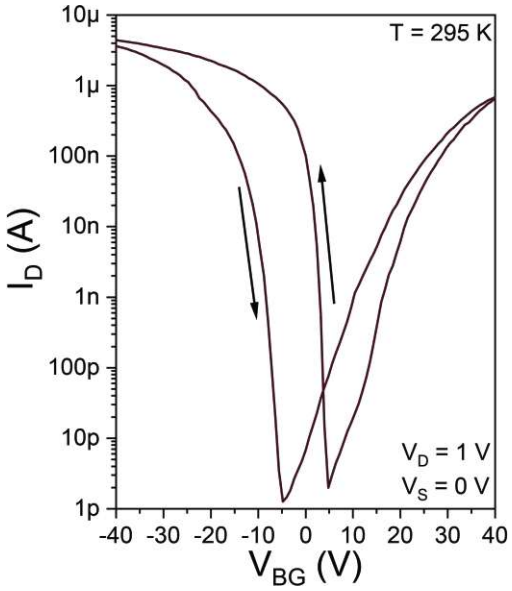


Figure A.2: *Transfer characteristic of a back gated Al-Si based SBFET acquired by a forwards and backwards sweep of* V_{BG} *from* 40 V *to* −40 V *and vice versa at* $V_{\mathrm{DS}} = 1\,\mathrm{V}$ *and* $T = 295\,\mathrm{K}$. *In contrast to a top gated SBFET, a dedicated hysteresis becomes evident.*

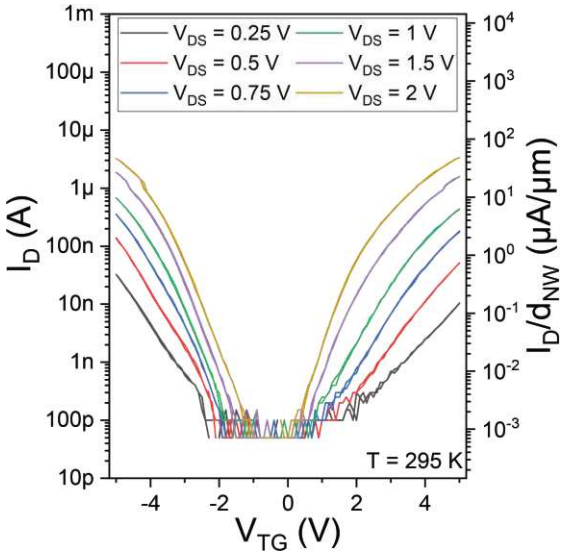


Figure A.3: *Transfer characteristics of an Al-Si based SBFET under pulsed* V_{TG} *conditions with* 1 ms, *a base voltage of* 0 V *and acquiring 202 measurement points per* V_{DS}. *Analyzing the hysteresis, extracted from the forwards and backwards* V_{TG}*-sweep, no distinct hysteresis can be extracted.*

T-dependent transfer characteristics of an Al-Si based RFET

Figure A.4 shows the T-dependency of the proposed Al-Si based RFET in the T-range of 295 K to 400 K at $V_{DS} = 1$ V. Correlating to the obtained insights in Section 4.2.1, I_{off} increases gradually with higher temperatures by about two orders of magnitude, which can be attributed to thermally excited charge carriers and the domination of TE in the off-states. Moreover, $I_{on}^{n/p}$ increases with elevated temperature, indicating dedicated SBs.

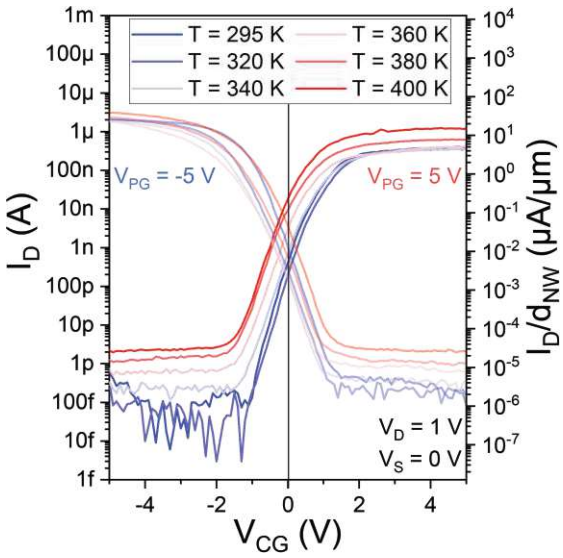


Figure A.4: *T-dependent n- and p-type transfer characteristics in the T-range between* 295 K *and* 400 K *of the proposed Al-Si based RFET. Notably, up to* 400 K*, distinct RFET functionality is proven.*

Influence of different V_{PG} and V_D polarities

Figure A.5 shows the influence of (a) positive and (b) negative bias polarity V_D on the RFET characteristics. Firstly, considering Figure A.5(a), shows that a "fanning" of the transfer characteristic in the p-type operation occurs. In general, such a "fanning" is a typical characteristic in SBFETs, as the charge carrier injection mechanism relies on tuning the energy landscape of the semiconductor. [49] Applying a positive V_D and setting $V_S = 0$ V leads to a negative shift of the drain potential in relation to the source potential. Thus, electrons (positive V_{PG}) are injected from source, which remains constant. Consequently, no "fanning" occurs. In contrast, holes (negative V_{PG}) are injected from drain, which is varied between 0.25 V and 1 V, resulting in constant change of the injection capabilities, leading to the observed "fanning". Figure A.5(b) shows the same characteristic for negative V_D, where the n-type SB is tuned, resulting in a "fanning" for the n-type transfer characteristic.

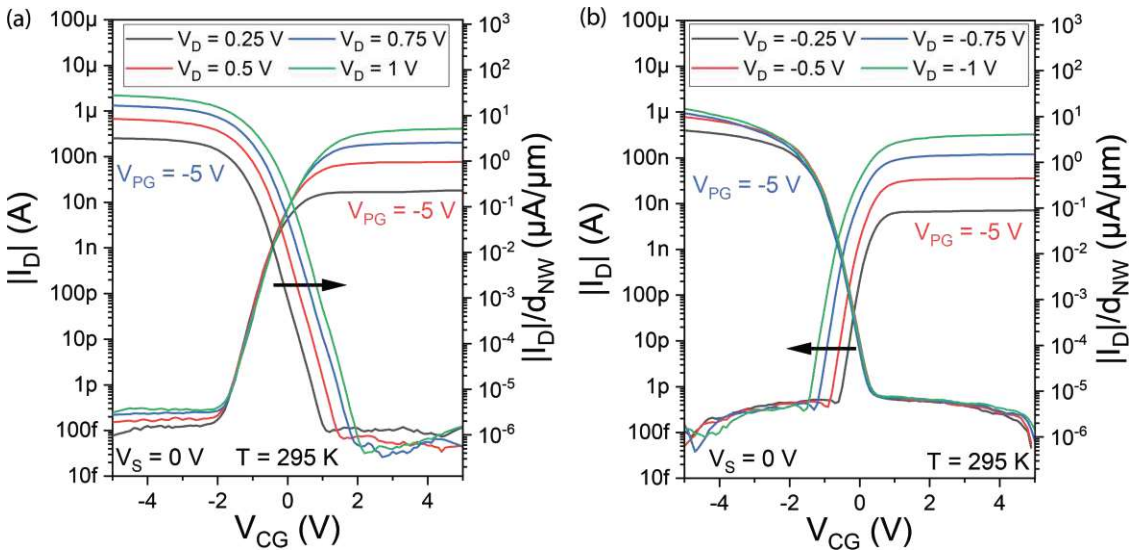


Figure A.5: *n- and p-type transfer characteristics of an Al-Si based RFET for (a) positive V_D and (b) negative V_D. Notably, a "fanning" becomes evident for non-matching V_{PG} and V_D polarities, due to changed injection properties caused by changing V_D and keeping V_S constant. Consequently, a V_D-dependent V_{th} is existent.*

Visualization of operation regimes of the Al-Si based RFET

Figure A.6 shows the output maps for symmetric |3 V| biasing, where (a) *n*- and (b) *p*-type operation modes are illustrated. With respect to the implementation of the proposed Al-Si based RFETs into logic circuits, symmetric voltage levels are desired, allowing its operation from a single power supply.

Al-Si based RFET inverter with |2 V| bias

Figure A.7 shows the transient V_{IN} and V_{OUT} characteristic of the Al-Si based RFET inverter, in case of using |2 V| bias, instead of |3 V|. Consequently, no distinct charge carrier separation is achieved, leading to undefined off-states. In other words, an insufficient band bending leads to the non-existent inverter functionality.

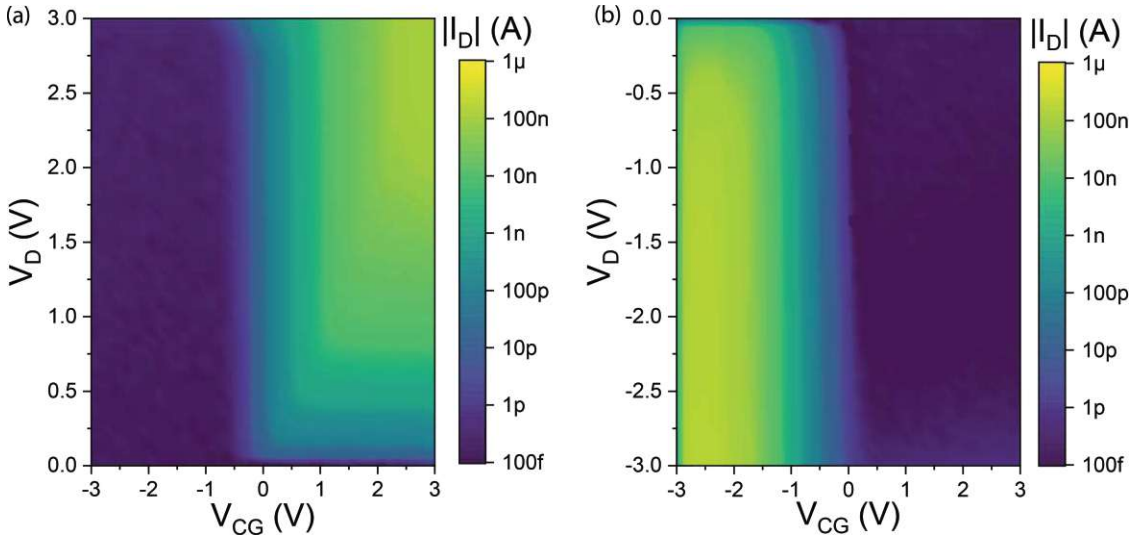


Figure A.6: *Output maps of the proposed Al-Si based RFET, allowing the evaluation of the operation regimes under symmetric bias conditions (here: |3 V|) of V_{D}, V_{PG} and V_{CG}, which is desired for its implementation in logic circuits. (a) and (b) show the corresponding maps for n- and p-type operation.*

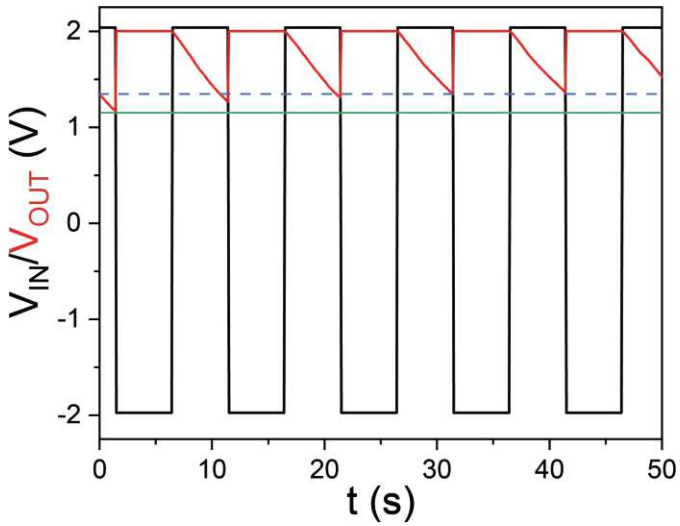


Figure A.7: *Analysis of the Al-Si based RFET inverter, considering an input voltage of |2 V|. Due to weak band bending, the charge carrier transport cannot be prohibited, leading to insufficient charge carrier blocking. As indicated by the solid green and dashed blue line, charging effects also occur, as the transport of charge carriers is not strictly separated.*

A.2 Al-Ge based SBFET

Influence of BG and TG on an Al-Ge based SBFET In general, using a top gate (TG) in combination with a back gate (BG) allows electrostatic gating from two different perspectives. Notably, this concept may also be used for the realization of RFETs, [39,49] as discussed in Section 2.4.1. In this context, Figure A.8 shows the influence of applying a V_{BG} bias on the transfer characteristic of an Al-Ge based SBFET. Sweeping V_{TG} from 5 V to −5 V and vice versa shows that V_{BG} in the range between 30 V and −30 V merely has a minor impact on $I_{\mathrm{on}}^{\mathrm{n/p}}$ and on the hysteresis [cf. Figure A.8(a)], but does not lead to a significant change in the characteristics. Note that due to the NW architecture, the weak BG influence can be attributed to the dominance of the Ω-shaped TG, which "overrules" the electrostatic gating effect from the BG.

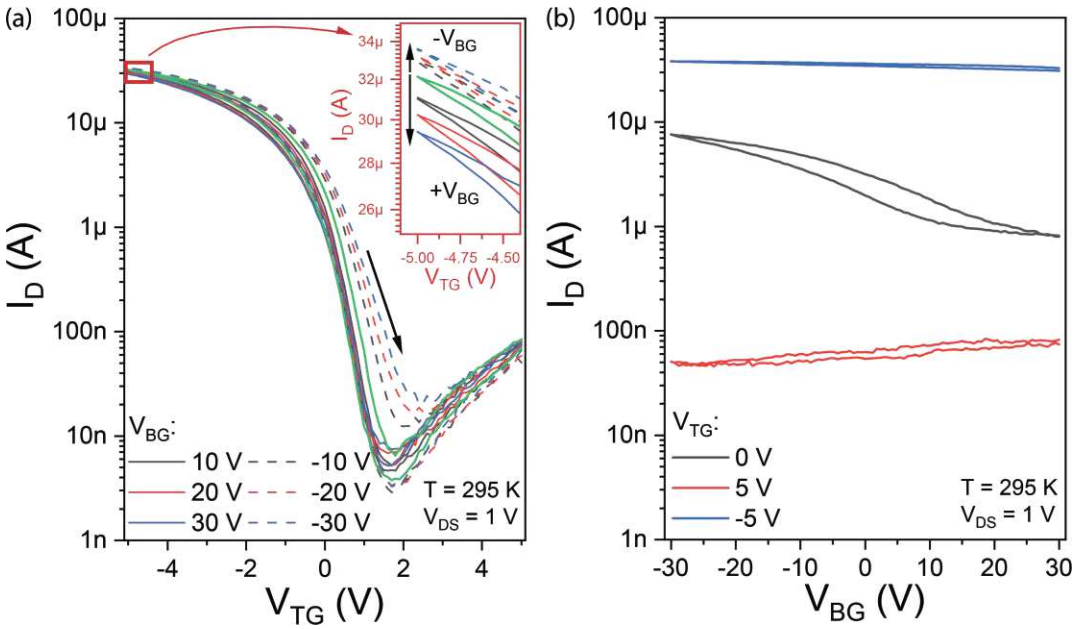


Figure A.8: *(a) Transfer characteristic of an Al-Ge based SBFET, sweeping V_{TG} and setting different V_{BG}. The upper right inset shows a zoomed view of $I_{\mathrm{on}}^{\mathrm{p}}$, where merely a weak impact on the current becomes evident with tuning V_{BG}. Moreover, the hysteresis is affected, due to different charge carrier trapping conditions induced by the application of a BG bias. (b) Transfer characteristic, sweeping V_{BG} from 40 V to −40 V and vice-versa, showing that no sufficient band bending can be achieved, due to the dominance of the TG.*

Transfer characteristics under pulsed V_{TG} conditions

Figure A.9 shows T-dependent transfer characteristics obtained from a forwards and subsequent backwards sweep of V_{TG} starting at 5 V. Notably, an insignificant hysteresis up to 350 K indicates a reduced density of trap states, which can be attributed to the use of DPG for the Ge NW growth. At I_{off} a minor hysteresis becomes evident, which is most likely attributed to thermally excited charge carriers, i.e., TE, overcoming the SB. In the p-branch the hysteresis might be attributed to recombination of trapped electrons. Importantly, $I_{on}^{n/p}$ and its T-dependency are in accordance with continuous measurements presented in Section 4.2.3.

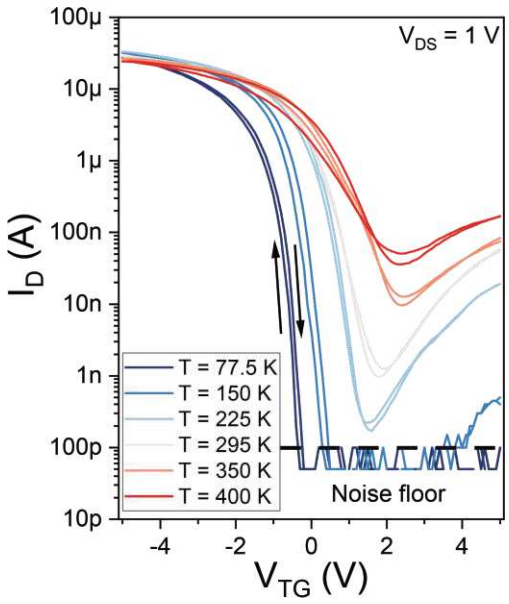


Figure A.9: *T-dependent transfer characteristics in the range between* 77.5 K *and* 400 K *of the proposed Al-Ge based SBFET under pulsed V_{TG} conditions with* 1 ms *and a base voltage of* 0 V. *The noise floor is indicated by the black dashed line at* 100 pA. *Notably, up to* 350 K *no substantial hysteresis becomes evident.*

Simulation of charge carrier population of conduction bands concerning NDR
Figure A.10 shows first simulation results,[1] considering $E_F = 0.6\,eV$, indicating the Fermi level pinning close to the valence band of Ge as evident in the Al-Ge material system. For the simulation, an intentionally un-doped Ge nanosheet with a thickness of 4 nm is considered. Figure A.10(a) shows the relative charge carrier intensity n_i/n_T, with n_i being the intrinsic charge carrier concentration and n_T is the increase of the charge carrier concentration, due to thermally excitation. Note that k_BT on the x-axis is associated with the applied bias. In this context, it can be seen that by increasing the bias, the charge carrier concentration in the L-valley decreases and increases in the X-valley, which can be associated with the transferred electron effect, responsible for the exhibition of NDR in Ge. Moreover, Figure A.10(b) shows the corresponding mobilities in the L-, X- and Γ-valleys, where the total mobility decreases for increasing the bias, as expected for the exhibition of NDR. Finally, Figure A.10(c) shows the combined charge carrier concentration and mobility plots of the considered conduction band valleys, which further supports the previously discussed physical mechanism responsible for the exhibition of NDR. Notably, the charge carrier concentration and mobility in the Γ valley (direct band gap of Ge) do not contribute significantly, as already proposed in Section 2.4.2.

[1] The presented simulation results were obtained by Dr. Felipe Murphy-Armando at Tyndall Photonics, University College Cork, Ireland in cooperation with Dr. Alois Lugstein and Dr. Masiar Sistani.

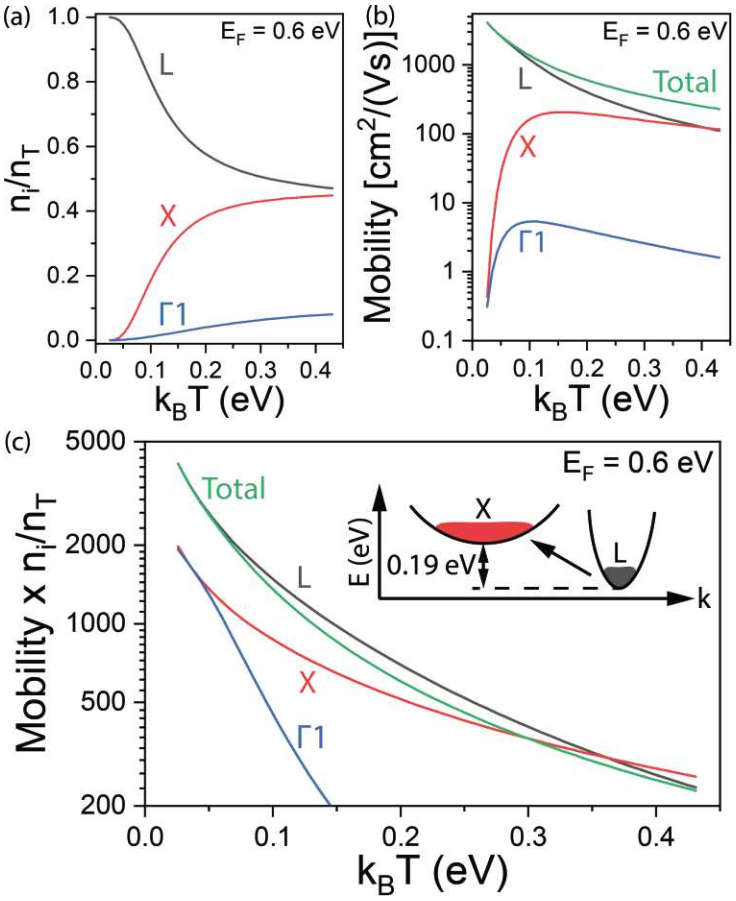


Figure A.10: *Calculation of the (a) relative charge carrier concentration n_i/n_T, (b) the electron mobility in the relevant conduction band valleys, and (c) the combination of both. In the scope of the simulations the L-, X- and Γ-valleys are considered. As illustrated in the inset, the transferred electron effect is expected to occur from the L- to the X-valley.*

Influence of V_{TG} sweep direction on transfer characteristic

Figure A.11 shows differences when sweeping from (a) $V_{\mathrm{TG}} = 5\,\mathrm{V}$ to $-5\,\mathrm{V}$ or (b) separating the V_{TG}-sweep direction from $0\,\mathrm{V}$ to $5\,\mathrm{V}$ and $0\,\mathrm{V}$ to $-5\,\mathrm{V}$. The shown transfer characteristics were extracted from Al-Ge based SBFETs, fabricated from Ge-on-insulator (GeOI), and were evaluated in the scope of TCR investigations, presented in Section 4.5.1. It is assumed that capacitive as well as charge trapping effects lead to the observed behavior.

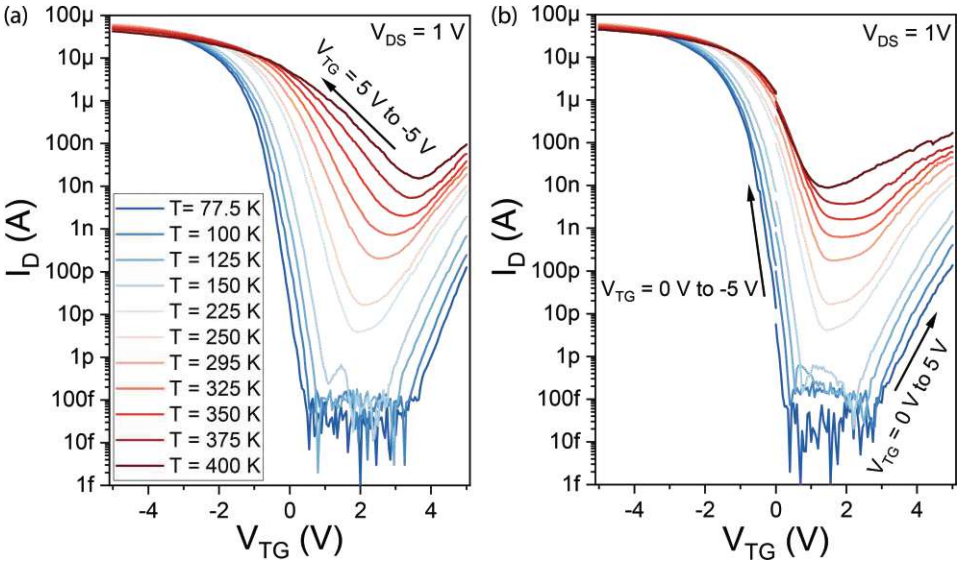


Figure A.11: *T-dependent transfer characteristics of an Al-GeOI based SBFET, where a (a) sweep from $V_{\mathrm{TG}} = 5\,\mathrm{V}$ to $-5\,\mathrm{V}$ and a (b) sweeps from $V_{\mathrm{TG}} = 0\,\mathrm{V}$ to $5\,\mathrm{V}$ and $V_{\mathrm{TG}} = 0\,\mathrm{V}$ to $-5\,\mathrm{V}$ are shown. Notable $I_{\mathrm{on}}^{\mathrm{n/p}}$ as well as I_{off} are not directly affected. However, threshold voltages $V_{\mathrm{th}}^{\mathrm{n/p}}$ and the $S^{\mathrm{n/p}}$ are directly affected, due to a variation of occupation of charge carrier traps.*

Appendix B

TCR on SOI based Nanosheet SBFETs

In the following, the first results of a bias-tunable TCR on the basis of Al-Si based SBFETs, realized from Silicon on insulator (SOI), are presented. In this context, the dedicated n- and p-type SBs evident in the Al-Si material system promise bias tunability of the TCR over a wider V_{TG} range compared to the Al-Ge material system. In this context, TE depicts the considerable operation regime enabling a bias-tunable TCR, due to its strong T-dependency. For the characterization, the same approach as discussed in Section 4.5.1 was used, also with respect to the device wiring with $V_{\mathrm{D}} = V_{\mathrm{TG}}$. Importantly, the presented data of the Al-Si based SBFET require a more thorough data processing and analysis.

I/V characteristics of the proposed Al-Si based "TCR" SBFET

Figure B.1 shows the acquired T-dependent I/V characteristics of the Al-Si based SBFET in TCR bias-tunability configuration, i.e., electrically connected drain and top gate electrodes. Moreover, the temperature range between 295 K and 400 K is considered, whereas at $T < 295\,\mathrm{K}$, I_D reaches the noise floor, hindering the extraction of distinct current values. The distinct T-dependent steps in the p-branch might be attributed to non sufficient band bending and dominant TE, whereas at a certain (threshold) $V_\mathrm{D} = V_\mathrm{TG}$ ~$-1.2\,\mathrm{V}$, FE starts to dominate.

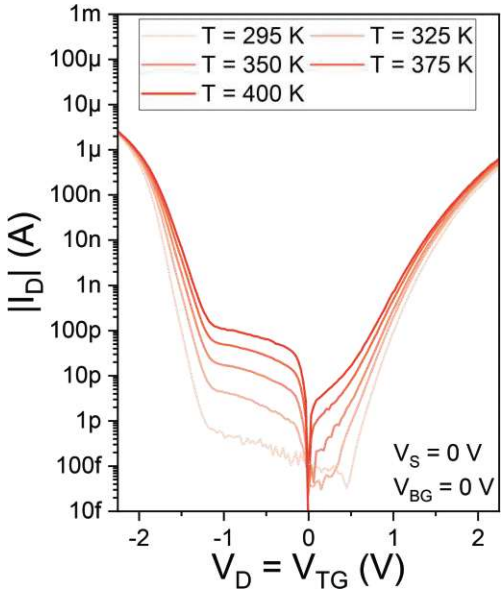


Figure B.1: *T-dependent I/V characteristics in the temperature regime between* 295 K *and* 400 K*, where a steady increase of $|I_\mathrm{D}|$ becomes evident for increasing the temperature. Notably, in the p-branch a dedicated separation is observable, which can be attributed to dominant TE. At $T <$* 295 K *no distinct I_D values can be extracted due to limitations of the measurement equipment, i.e., reaching the noise floor.*

V_{TG}-dependent TCR of Al-Si based "TCR" SBFET

Figure B.2(a,b) shows extracted TCR values of the *p*- and *n*-branch, as illustrated in Figure B.1. Notably, a bias-tunable TCR becomes evident over the investigated $V_D = V_{TG}$ range between $-2.25\,V$ and $2.25\,V$. Thus, demonstrating distinct *n*- and *p*-type SBs in the Al-Si material system. Remarkably, even at elevated temperatures TCR values in the range between ~$0\,\%/K$ and ~$-3.5\,K$ are extracted.

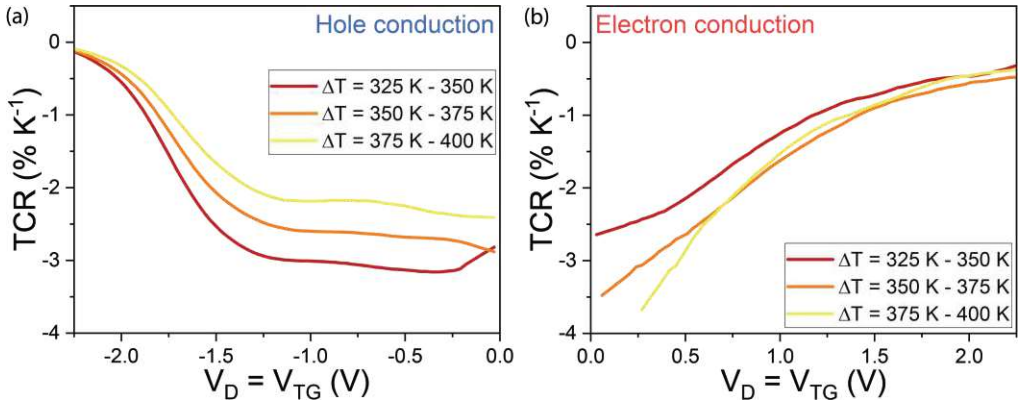


Figure B.2: *TCR curves extracted from T-dependent I/V characteristics of the (a) p-branch with $V_D = V_{TG} < 0\,V$ and (b) n-branch with $V_D = V_{TG} > 0\,V$. Notably, even at elevated temperatures bias-tunable maximum TCR values in the range between $-0.1\,\%/K$ and $-3.5\,\%/K$ are acquired.*

Bibliography

[1] IRDS, "International Roadmap for Devices and Systems (IRDS)," Tech. Rep. Executive Summary, IEEE, 2023.

[2] R. K. Cavin, V. V. Zhirnov, G. I. Bourianoff, J. A. Hutchby, D. J. Herr, H. H. Hosack, W. H. Joyner, and T. A. Wooldridge, "A long-term view of research targets in nanoelectronics," *Journal of Nanoparticle Research*, vol. 7, pp. 573–586, 12 2005.

[3] R. Chau, B. Doyle, S. Datta, J. Kavalieros, and K. Zhang, "Integrated nanoelectronics for the future," *Nature Materials*, vol. 6, pp. 810–812, 11 2007.

[4] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 82–85, 1998.

[5] K. J. Kuhn, "Considerations for ultimate CMOS scaling," *IEEE Transactions on Electron Devices*, vol. 59, no. 7, pp. 1813–1828, 2012.

[6] S. Chopra and S. Subramaniam, "A Review on Challenges for MOSFET Scaling," *International Journal of innovative Science, Engineering & Technology*, vol. 2, no. 4, pp. 1055–1057, 2015.

[7] S. Salahuddin, K. Ni, and S. Datta, "The era of hyper-scaling in electronics," *Nature Electronics*, vol. 1, pp. 442–450, 8 2018.

[8] R. K. Ratnesh, A. Goel, G. Kaushik, H. Garg, Chandan, M. Singh, and B. Prasad, "Advancement and challenges in MOSFET scaling," *Materials Science in Semiconductor Processing*, vol. 134, p. 106002, 11 2021.

[9] F. Assad, Z. Ren, D. Vasileska, S. Datta, and M. Lundstrom, "On the performance limits for Si MOSFET's: A theoretical study," *IEEE Transactions on Electron Devices*, vol. 47, no. 1, pp. 232–240, 2000.

[10] D. Mamaluy and X. Gao, "The fundamental downscaling limit of field effect transistors," *Applied Physics Letters*, vol. 106, p. 193503, 5 2015.

[11] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H. S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–287, 2001.

[12] J. Wang and M. Lundstrom, "Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?," *Technical Digest - International Electron Devices Meeting*, pp. 707–710, 2002.

[13] A. K. Gundu and V. Kursun, "5-nm Gate-All-Around Transistor Technology with 3-D Stacked Nanosheets," *IEEE Transactions on Electron Devices*, vol. 69, pp. 922–929, 3 2022.

[14] P. Kocanda and A. Kos, "Static and dynamic energy losses vs. temperature in different CMOS technologies," *Proceedings of the 22nd International Conference Mixed Design of Integrated Circuits and Systems, MIXDES 2015*, pp. 446–449, 8 2015.

[15] Y. S. Lin, C. C. Wu, C. S. Chang, R. P. Yang, W. M. Chen, J. J. Liaw, and C. H. Diaz, "Leakage scaling in deep submicron CMOS for SoC," *IEEE Transactions on Electron Devices*, vol. 49, pp. 1034–1041, 6 2002.

[16] Y. Nishi and R. Doering, *Handbook of semiconductor manufacturing technology*. Marcel Dekker, 2000.

[17] S. Sze and K. K. Ng, *Physics of Semiconductor Devices*. Wiley, 2006.

[18] F. M. Bufler, R. Ritzenthaler, H. Mertens, G. Eneman, A. Mocuta, and N. Horiguchi, "Performance Comparison of n-Type Si Nanowires, Nanosheets, and FinFETs by MC Device Simulation," *IEEE Electron Device Letters*, vol. 39, pp. 1628–1631, 11 2018.

[19] M. Radosavljevic, C. Y. Huang, W. Rachmady, S. H. Seung, N. K. Thomas, G. Dewey, A. Agrawal, K. Owens, C. C. Kuo, C. J. Jezewski, R. Nahm, N. Briggs, T. A. Tronic, T. Michaelos, N. A. Kabir, B. Holybee, K. Jun, P. Morrow, A. Phan, S. Shivaraman, H. W. Then, V. Kapinus, M. K. Harper, P. D. Nguyen, K. L. Cheong, S. Ghose, K. Ganguly, C. Bomberger, J. M. Tan, M. A. El Qader, A. A. Oni, P. Fischer, R. Bristol, M. Metz, S. B. Clendenning, B. Turkot, R. Schenker, M. J. Kobrinsky, and J. Kavalieros, "Opportunities in 3-D stacked CMOS transistors," *Technical Digest - International Electron Devices Meeting, IEDM*, vol. 2021-December, pp. 1–34, 2021.

[20] J.-S. Yoon, J. Jeong, S. Lee, J. Lee, and R.-H. Baek, "Gate-All-Around FETs:

Nanowire and Nanosheet Structure," in *Nanowires - Recent Progress*, IntechOpen, 10 2021.

[21] N. Loubet, T. Hook, P. Montanini, C. W. Yeung, S. Kanakasabapathy, M. Guillom, T. Yamashita, J. Zhang, X. Miao, J. Wang, A. Young, R. Chao, M. Kang, Z. Liu, S. Fan, B. Hamieh, S. Sieg, Y. Mignot, W. Xu, S. C. Seo, J. Yoo, S. Mochizuki, M. Sankarapandian, O. Kwon, A. Carr, A. Greene, Y. Park, J. Frougier, R. Galatage, R. Bao, J. Shearer, R. Conti, H. Song, D. Lee, D. Kong, Y. Xu, A. Arceo, Z. Bi, P. Xu, R. Muthinti, J. Li, R. Wong, D. Brown, P. Oldiges, R. Robison, J. Arnold, N. Felix, S. Skordas, J. Gaudiello, T. Standaert, H. Jagannathan, D. Corliss, M. H. Na, A. Knorr, T. Wu, D. Gupta, S. Lian, R. Divakaruni, T. Gow, C. Labelle, S. Lee, V. Paruchuri, H. Bu, and M. Khare, "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," in *Digest of Technical Papers - Symposium on VLSI Technology*, vol. 5, pp. T230–T231, IEEE, 6 2017.

[22] R. K. Cavin, P. Lugli, and V. V. Zhirnov, "Science and engineering beyond moore's law," *Proceedings of the IEEE*, vol. 100, pp. 1720–1749, 5 2012.

[23] IRDS, "IRDS 2023: Beyond CMOS and Emerging Research Materials," tech. rep., IEEE, 2023.

[24] K. Bhol, B. Jena, and U. Nanda, "Silicon Nanowire GAA-MOSFET: a Workhorse in Nanotechnology for Future Semiconductor Devices," *Silicon*, vol. 14, pp. 3163–3171, 5 2022.

[25] D. L. Harame, S. J. Koester, G. Freeman, P. Cottrel, K. Rim, G. Dehlinger, D. Ahlgren, J. S. Dunn, D. Greenberg, A. Joseph, F. Anderson, J. S. Rieh, S. A. Onge, D. Coolbaugh, V. Ramachandran, J. D. Cressler, and S. Subbanna, "The revolution in SiGe: Impact on device electronics," *Applied Surface Science*, vol. 224, pp. 9–17, 3 2004.

[26] P. S. Goley and M. K. Hudait, "Germanium based field-effect transistors: Challenges and opportunities," *Materials*, vol. 7, no. 3, pp. 2301–2339, 2014.

[27] K. Saraswat, "Germanium MOSFETs for Nanoelectronics," *ECS Transactions*, vol. 3, pp. 817–821, 12 2006.

[28] B. Mheen, Y. J. Song, J. Y. Kang, and S. Hong, "Strained-SiGe complementary MOSFETs adopting different thicknesses of silicon cap layers for low power and high performance applications," *ETRI Journal*, vol. 27, no. 4, pp. 439–445, 2005.

[29] W. M. Weber, J. Trommer, A. Heinzig, and T. Mikolajick, "Germanium-based

polarity-controllable transistors," in *Functionality-Enhanced Devices: An alternative to Moore's Law*, ch. 2, pp. 13–25, Institution of Engineering and Technology, 2018.

[30] G. Scappucci, C. Kloeffel, F. A. Zwanenburg, D. Loss, M. Myronov, J. J. Zhang, S. De Franceschi, G. Katsaros, and M. Veldhorst, "The germanium quantum information route," *Nature Reviews Materials*, vol. 6, pp. 926–943, 10 2021.

[31] R. H. Kingston, "Review of germanium surface phenomena," *Journal of Applied Physics*, vol. 27, pp. 101–114, 2 1956.

[32] S. Zhang, E. R. Hemesath, D. E. Perea, E. Wijaya, J. L. Lensch-Falk, and L. J. Lauhon, "Relative influence of surface states and bulk impurities on the electrical properties of Ge nanowires," *Nano Letters*, vol. 9, pp. 3268–3274, 9 2009.

[33] H. Tanaka, J. Suda, and T. Kimoto, "Impacts of surface roughness scattering on hole mobility in germanium nanowires," *2015 Silicon Nanoelectronics Workshop, SNW 2015*, pp. 1–2, 2015.

[34] I. Kim, J. Koo, J. Lee, and H. Jeon, "A comparison of Al2O3/HfO2 and Al 2O3/ZrO2 bilayers deposited by the atomic layer deposition method for potential gate dielectric applications," *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers*, vol. 45, pp. 919–925, 2 2006.

[35] S. M. George, "Atomic layer deposition: An overview," *Chemical Reviews*, vol. 110, pp. 111–131, 1 2010.

[36] B. Vincent, J. F. Damlencourt, Y. Morand, A. Pouydebasque, C. Le Royer, L. Clavelier, N. Dechoux, P. Rivallin, T. Nguyen, S. Cristoloveanu, Y. Campidelli, D. Rouchon, M. Mermoux, S. Deleonibus, D. Bensahel, and T. Billon, "The Ge condensation technique: A solution for planar SOI/GeOI co-integration for advanced CMOS technologies?," *Materials Science in Semiconductor Processing*, vol. 11, pp. 205–213, 10 2008.

[37] R. Cheng, Z. Chen, S. Yuan, M. Takenaka, S. Takagi, G. Han, and R. Zhang, "Mobility enhancement techniques for Ge and GeSn MOSFETs," 2 2021.

[38] M. Mongillo, P. Spathis, G. Katsaros, P. Gentile, and S. De Franceschi, "Multifunctional devices and logic gates with undoped silicon nanowires," *Nano Letters*, vol. 12, pp. 3074–3079, 6 2012.

[39] U. Schwalke, T. Krauss, and F. Wessely, "Dopant-Free CMOS on SOI: Multi-Gate Si-Nanowire Transistors for Logic and Memory Applications," *ECS Transactions*, vol. 53,

pp. 105–114, 5 2013.

[40] P. E. Gaillardon, *Functionality-enhanced devices an alternative to moore's law*. London: Institution of Engineering and Technology, 11 2018.

[41] R. Jacob Baker, *CMOS: Circuit Design, Layout, and Simulation*, vol. 3rd. IEEE Press Series on Microelectronic Systems, 2011.

[42] W. M. Weber, L. Geelhaar, F. Kreupl, E. Unger, H. Riechert, L. Lamagna, M. Fanciulli, G. Scarpa, and P. Lugli, "Tuning the polarity of Si-nanowire transistors without the use of doping," in *2008 8th IEEE Conference on Nanotechnology, IEEE-NANO*, pp. 580–581, IEEE, 8 2008.

[43] T. Mikolajick, G. Galderisi, S. Rai, M. Simon, R. Böckle, M. Sistani, C. Cakirlar, N. Bhattacharjee, T. Mauersberger, A. Heinzig, A. Kumar, W. M. Weber, and J. Trommer, "Reconfigurable field effect transistors: A technology enablers perspective," *Solid-State Electronics*, vol. 194, p. 108381, 8 2022.

[44] A. L. Falk, F. H. Koppens, C. L. Yu, K. Kang, N. De Leon Snapp, A. V. Akimov, M. H. Jo, M. D. Lukin, and H. Park, "Near-field electrical detection of optical plasmons and single-plasmon sources," *Nature Physics*, vol. 5, pp. 475–479, 7 2009.

[45] M. Sistani, M. G. Bartmann, N. A. Güsken, R. F. Oulton, H. Keshmiri, M. A. Luong, Z. S. Momtaz, M. I. Den Hertog, and A. Lugstein, "Plasmon-Driven Hot Electron Transfer at Atomically Sharp Metal-Semiconductor Nanojunctions," *ACS Photonics*, vol. 7, pp. 1642–1648, 7 2020.

[46] J. Ridderbos, M. Brauns, J. Shen, F. K. de Vries, A. Li, E. P. Bakkers, A. Brinkman, and F. A. Zwanenburg, "Josephson Effect in a Few-Hole Quantum Dot," *Advanced Materials*, vol. 30, p. 1802257, 11 2018.

[47] J. Delaforce, M. Sistani, R. B. Kramer, M. A. Luong, N. Roch, W. M. Weber, M. I. den Hertog, E. Robin, C. Naud, A. Lugstein, and O. Buisson, "Al-Ge-Al Nanowire Heterostructure: From Single-Hole Quantum Dot to Josephson Effect," *Advanced Materials*, vol. 33, p. 2101989, 10 2021.

[48] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Transactions on Electron Devices*, vol. 53, pp. 1048–1058, 5 2006.

[49] W. M. Weber and T. Mikolajick, "Silicon and germanium nanowire electronics: Physics of conventional and unconventional transistors," *Reports on Progress in*

Physics, vol. 80, p. 066502, 6 2017.

[50] M. Schwarz, T. D. Vethaak, V. Derycke, A. Francheteau, B. Iniguez, S. Kataria, A. Kloes, F. Lefloch, M. Lemme, J. P. Snyder, W. M. Weber, and L. E. Calvet, "The Schottky barrier transistor in emerging electronic devices," 6 2023.

[51] J. Knoch, M. Zhang, J. Appenzeller, and S. Mantl, "Physics of ultrathin-body silicon-on-insulator Schottky-barrier field-effect transistors," *Applied Physics A: Materials Science and Processing*, vol. 87, pp. 351–357, 3 2007.

[52] R. T. Tung, "The physics and chemistry of the Schottky barrier height," *Applied Physics Reviews*, vol. 1, p. 11304, 1 2014.

[53] J. A. Kittl, A. Lauwers, O. Chamirian, M. Van Dal, A. Akheyar, M. De Potter, R. Lindsay, and K. Maex, "Ni- and Co-based silicides for advanced CMOS applications," *Microelectronic Engineering*, vol. 70, pp. 158–165, 11 2003.

[54] Karen Maex and Marc van Rossum, *Properties of Metal Silicides*. Institution of Engineering and Technology, 1995.

[55] W. M. Weber, L. Geelhaar, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Pamler, C. Chèze, H. Riechert, P. Lugli, and F. Kreupl, "Silicon-nanowire transistors with intruded nickel-silicide contacts," *Nano Letters*, vol. 6, pp. 2660–2666, 12 2006.

[56] J. A. Kittl, K. Opsomer, C. Torregiani, C. Demeurisse, S. Mertens, D. P. Brunco, M. J. Van Dal, and A. Lauwers, "Silicides and germanides for nano-CMOS applications," *Materials Science and Engineering: B*, vol. 154-155, pp. 144–154, 12 2008.

[57] W. Tang, B. M. Nguyen, R. Chen, and S. A. Dayeh, "Solid-state reaction of nickel silicide and germanide contacts to semiconductor nanochannels," *Semiconductor Science and Technology*, vol. 29, p. 054004, 5 2014.

[58] F. Fuchs, M. Bilal Khan, D. Deb, D. Pohl, J. Schuster, W. M. Weber, U. Mühle, M. Löffler, Y. M. Georgiev, A. Erbe, and S. Gemming, "Formation and crystallographic orientation of NiSi2-Si interfaces," *Journal of Applied Physics*, vol. 128, p. 085301, 8 2020.

[59] K. El Hajraoui, M. A. Luong, E. Robin, F. Brunbauer, C. Zeiner, A. Lugstein, P. Gentile, J. L. Rouvière, and M. Den Hertog, "In Situ Transmission Electron Microscopy Analysis of Aluminum-Germanium Nanowire Solid-State Reaction," *Nano Letters*, vol. 19, pp. 2897–2904, 5 2019.

[60] F. Wessely, T. Krauss, and U. Schwalke, "CMOS without doping: Multi-gate silicon-nanowire field-effect-transistors," *Solid-State Electronics*, vol. 70, pp. 33–38, 4 2012.

[61] J. Appenzeller, J. Knoch, M. T. Björk, H. Riel, H. Schmid, and W. Riess, "Toward nanowire electronics," *IEEE Transactions on Electron Devices*, vol. 55, pp. 2827–2845, 11 2008.

[62] J. X. Wei Lu, "Semiconductor Nanowires: From Next-Generation Electronics to Sustainable Energy," *Journal of Physics D: Applied Physics*, vol. 39, no. 21, p. R387, 2015.

[63] C. Thelander, P. Agarwal, S. Brongersma, J. Eymery, L. F. Feiner, A. Forchel, M. Scheffler, W. Riess, B. J. Ohlsson, U. Gösele, and L. Samuelson, "Nanowire-based one-dimensional electronics," *Materials Today*, vol. 9, pp. 28–35, 10 2006.

[64] M. Sistani, P. Staudinger, J. Greil, M. Holzbauer, H. Detz, E. Bertagnolli, and A. Lugstein, "Room-Temperature Quantum Ballistic Transport in Monolithic Ultrascaled Al-Ge-Al Nanowire Heterostructures," *Nano Letters*, vol. 17, pp. 4556–4561, 8 2017.

[65] W. M. Weber, A. Heinzig, J. Trommer, D. Martin, M. Grube, and T. Mikolajick, "Reconfigurable nanowire electronics - A review," *Solid-State Electronics*, vol. 102, pp. 12–24, 12 2014.

[66] T. Mikolajick, A. Heinzig, J. Trommer, T. Baldauf, and W. M. Weber, "The RFET - A reconfigurable nanowire transistor and its application to novel electronic circuits and systems," *Semiconductor Science and Technology*, vol. 32, p. 043001, 3 2017.

[67] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick, and W. M. Weber, "Reconfigurable silicon nanowire transistors," *Nano Letters*, vol. 12, pp. 119–124, 1 2012.

[68] W. M. Weber, J. Trommer, M. Grube, A. Heinzig, M. Konig, and T. Mikolajick, "Reconfigurable silicon nanowire devices and circuits: Opportunities and challenges," in *Design, Automation & Test in Europe Conference & Exhibition (DATE)*, (New Jersey), pp. 1–6, IEEE Conference Publications, 4 2014.

[69] P. N. Butcher, "The Gunn effect," *Reports on Progress in Physics*, vol. 30, pp. 97–148, 1 1967.

[70] D. Kazazis, A. Zaslavsky, E. Tutuc, N. A. Bojarczuk, and S. Guha, "Negative differential resistance in ultrathin Ge-on-insulator FETs," *Semiconductor Science and Technology*, vol. 22, pp. S1–S4, 1 2007.

[71] B. J. Elliott, J. B. Gunn, and J. C. McGroddy, "BULK NEGATIVE DIFFERENTIAL CONDUCTIVITY AND TRAVELING DOMAINS IN n-TYPE GERMANIUM," *Applied Physics Letters*, vol. 11, pp. 253–255, 10 1967.

[72] M. K. Husain, X. V. Li, and C. H. de Groot, "Observation of negative differential conductance in a reverse-biased Ni/ Ge schottky diode," *IEEE Electron Device Letters*, vol. 30, pp. 966–968, 9 2009.

[73] F. M. Brunbauer, E. Bertagnolli, and A. Lugstein, "Gate-Tunable Electron Transport Phenomena in Al-Ge<111>-Al Nanowire Heterostructures," *Nano Letters*, vol. 15, pp. 7514–7518, 11 2015.

[74] R. Böckle, M. Sistani, K. Eysin, M. G. Bartmann, M. A. Luong, M. I. den Hertog, A. Lugstein, and W. M. Weber, "Gate-Tunable Negative Differential Resistance in Next-Generation Ge Nanodevices and their Performance Metrics," *Advanced Electronic Materials*, vol. 7, p. 2001178, 3 2021.

[75] M. Sistani, R. Böckle, D. Falkensteiner, M. A. Luong, M. I. Den Hertog, A. Lugstein, and W. M. Weber, "Nanometer-Scale Ge-Based Adaptable Transistors Providing Programmable Negative Differential Resistance Enabling Multivalued Logic," *ACS Nano*, vol. 15, pp. 18135–18141, 11 2021.

[76] S. Karmakar and F. C. Jain, "Future Semiconductor Devices for Multi-Valued Logic Circuit Design," *Materials Sciences and Applications*, vol. 03, no. 11, pp. 807–814, 2012.

[77] M. A. Luong, E. Robin, N. Pauc, P. Gentile, M. Sistani, A. Lugstein, M. Spies, B. Fernandez, and M. I. Den Hertog, "In-Situ Transmission Electron Microscopy Imaging of Aluminum Diffusion in Germanium Nanowires for the Fabrication of Sub-10 nm Ge Quantum Disks," *ACS Applied Nano Materials*, vol. 3, no. 2, pp. 1891–1899, 2020.

[78] T. Nishimura, K. Kita, and A. Toriumi, "Evidence for strong Fermi-level pinning due to metal-induced gap states at metal/germanium interface," *Applied Physics Letters*, vol. 91, p. 123123, 9 2007.

[79] Z. Cheng, C. S. Pang, P. Wang, S. T. Le, Y. Wu, D. Shahrjerdi, I. Radu, M. C. Lemme, L. M. Peng, X. Duan, Z. Chen, J. Appenzeller, S. J. Koester, E. Pop, A. D. Franklin, and C. A. Richter, "How to report and benchmark emerging field-effect transistors," *Nature Electronics*, vol. 5, pp. 416–423, 7 2022.

[80] M. Sistani, J. Delaforce, R. B. Kramer, N. Roch, M. A. Luong, M. I. Den Hertog, E. Robin, J. Smoliner, J. Yao, C. M. Lieber, C. Naud, A. Lugstein, and O. Buisson,

"Highly Transparent Contacts to the 1D Hole Gas in Ultrascaled Ge/Si Core/Shell Nanowires," *ACS Nano*, vol. 13, pp. 14145–14151, 12 2019.

[81] M. Andreev, J. W. Choi, J. Koo, H. Kim, S. Jung, K. H. Kim, and J. H. Park, "Negative differential transconductance device with a stepped gate dielectric for multi-valued logic circuits," *Nanoscale Horizons*, vol. 5, pp. 1378–1385, 10 2020.

[82] K. J. Chen, T. Akeyoshi, and K. Maezawa, "Monostable-bistable transition logic elements (Mobiles) based on monolithic integration of resonant tunneling diodes and fets," *Japanese Journal of Applied Physics*, vol. 34, pp. 1199–1203, 2 1995.

[83] J. A. Dean and N. A. Lange, *Lange's chemistry handbook*, vol. 4. McGraw-Hill Professional, 15 ed., 1999.

[84] J. W. Arblaster, *Selected values of the crystallographic properties of elements*. ASM International, 2018.

[85] N. Greenwood and A. Earnshaw, "7 - Aluminium, Gallium, Indium and Thallium," in *Chemistry of the Elements*, pp. 216–267, Butterworth-Heinemann, 1 1997.

[86] D. R. Lide, *CRC Handbook of Chemistry and Physics*. CRC Press, 2007.

[87] C. Steinbruchel and B. L. Chin, *Copper interconnect technology*. SPIE Publications, 2001.

[88] K. Kemmochi and K. I. Hirano, "Electromigration of grain boundaries in aluminum," *Thin Solid Films*, vol. 25, pp. 353–361, 2 1975.

[89] F. Yost, D. Amos, and A. Romig, "Stress-driven diffusive voiding of aluminum conductor lines," in *International Reliablity Physics Symposium*, pp. 193–201, Institute of Electrical and Electronics Engineers (IEEE), 1 2003.

[90] P. Mensch, K. E. Moselund, S. Karg, E. Lortscher, M. T. Bjork, and H. Riel, "Interface state density of single vertical nanowire MOS capacitors," *IEEE Transactions on Nanotechnology*, vol. 12, no. 3, pp. 279–282, 2013.

[91] D. K. Simon, P. M. Jordan, T. Mikolajick, and I. Dirnstorfer, "On the Control of the Fixed Charge Densities in Al2O3-Based Silicon Surface Passivation Schemes," *ACS Applied Materials and Interfaces*, vol. 7, pp. 28215–28222, 12 2015.

[92] S. Kasap and P. Capper, *Springer Handbook of Electronic and Photonic Materials*. Springer Handbooks, Cham: Springer International Publishing, 2007.

[93] H. Huff and D. Gilmer, eds., *High Dielectric Constant Materials*, vol. 16 of *Springer Series in Advanced Microelectronics*. Berlin, Heidelberg: Springer Berlin Heidelberg, 2005.

[94] B. Hoex, J. J. Gielis, M. C. Van De Sanden, and W. M. Kessels, "On the c-Si surface passivation mechanism by the negative-charge-dielectric Al2O3," *Journal of Applied Physics*, vol. 104, p. 113703, 12 2008.

[95] D. Hiller, D. Tröger, M. Grube, D. König, and T. Mikolajick, "The negative fixed charge of atomic layer deposited aluminium oxide - A two-dimensional SiO2/AlO xinterface effect," *Journal of Physics D: Applied Physics*, vol. 54, p. 275304, 7 2021.

[96] F. Werner, B. Veith, D. Zielke, L. Kühnemund, C. Tegenkamp, M. Seibt, R. Brendel, and J. Schmidt, "Electronic and chemical properties of the c-Si/Al2O3 interface," *Journal of Applied Physics*, vol. 109, 6 2011.

[97] M. V. Fischetti and S. E. Laux, "Band structure, deformation potentials, and carrier mobility in strained Si Ge, and SiGe alloys," *Journal of Applied Physics*, vol. 80, no. 4, pp. 2234–2252, 1996.

[98] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld, "Strained Si, SiGe, and Ge channels for high-mobility metal-oxide- semiconductor field-effect transistors," 1 2005.

[99] C. Harris and E. P. O'Reilly, "Nature of the band gap of silicon and germanium nanowires," *Physica E: Low-Dimensional Systems and Nanostructures*, vol. 32, pp. 341–345, 5 2006.

[100] J. Wang, A. Rahman, G. Klimeck, and M. Lundstrom, "Bandstructure and orientation effects in ballistic Si and Ge nanowire FETs," in *Technical Digest - International Electron Devices Meeting, IEDM*, vol. 2005, pp. 530–533, IEEE, 2005.

[101] Ioffe Institute, "NSM Archive - Band structure and carrier concentration of Silicon (Si)," 2024.

[102] C. Guo, L. Luo, G. Yuan, X. Yang, R. Zhang, W. Zhang, and S. Lee, "Surface Passivation and Transfer Doping of Silicon Nanowires," *Angewandte Chemie*, vol. 121, pp. 10080–10084, 12 2009.

[103] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan, and K. C. Saraswat, "Germanium nanowire field-effect transistors with SiO2 and high-κ HfO2 gate dielectrics," *Applied Physics Letters*, vol. 83, pp. 2432–2434, 9 2003.

[104] H. Bijo Joseph, S. Kumar Singh, V. Nagarajan, a. , D. Ghosh, M. Singh Parihar, G. Alastair Armstrong, S. Kim, and S. Cho, "Analysis on performances of ultra-thin vertical MOSFET depending on position of gate-drain misalignment," *Japanese Journal of Applied Physics*, vol. 63, p. 054002, 5 2024.

[105] R. E. Camacho-Aguilera, Y. Cai, N. Patel, J. T. Bessette, M. Romagnoli, L. C. Kimerling, and J. Michel, "An electrically pumped germanium laser," *Optics Express*, vol. 20, p. 11316, 5 2012.

[106] M. Kaschel, M. Schmid, M. Gollhofer, J. Werner, M. Oehme, and J. Schulze, "Room-temperature electroluminescence from tensile strained double-heterojunction Germanium pin LEDs on Silicon substrates," *Solid-State Electronics*, vol. 83, pp. 87–91, 5 2013.

[107] Ioffe Institute, "NSM Archive - Band structure and carrier concentration of Germanium (Ge)," 2024.

[108] C. Claeys and E. Simoen, *Germanium-Based Technologies: From Materials to Devices*. Elsevier B.V., Oxford, UK, 2007.

[109] R. Pillarisetty, "Academic and industry research progress in germanium nanodevices," 11 2011.

[110] J. Bardeen and W. H. Brattain, "Transistor, a semiconductor triode," *Proceedings of the IEEE*, vol. 86, no. 1, pp. 29–30, 1998.

[111] E. I. Givargizov and N. N. Sheftal, "Morphology of Germanium Whiskers," *Kristall und Technik*, vol. 7, pp. 37–41, 1 1972.

[112] D. P. Brunco, B. De Jaeger, G. Eneman, A. Satta, V. Terzieva, L. Souriau, F. E. Leys, G. Pourtois, M. Houssa, K. Opsomer, G. Nicholas, M. Meuris, and M. Heyns, "Germanium: The Past and Possibly a Future Material for Microelectronics," *ECS Transactions*, vol. 11, pp. 479–493, 12 2007.

[113] M. Houssa, G. Pourtois, M. Caymax, M. Meuris, M. M. Heyns, V. V. Afanas'Ev, and A. Stesmans, "Ge dangling bonds at the (100) Ge/ GeO2 interface and the viscoelastic properties of GeO2," *Applied Physics Letters*, vol. 93, p. 161909, 10 2008.

[114] L. Tsetseris and S. T. Pantelides, "Morphology and defect properties of the Ge-GeO2 interface," *Applied Physics Letters*, vol. 95, p. 262107, 12 2009.

[115] D. Schmeisser, R. D. Schnell, A. Bogen, F. J. Himpsel, D. Rieger, G. Landgren,

and J. F. Morar, "Surface oxidation states of germanium," *Surface Science*, vol. 172, pp. 455–465, 7 1986.

[116] D. Kuzum, T. Krishnamohan, A. J. Pethe, A. K. Okyay, Y. Oshima, Y. Sun, J. P. McVittie, P. A. Pianetta, P. C. McIntyre, and K. C. Saraswat, "Ge-interface engineering with ozone oxidation for low interface-state density," *IEEE Electron Device Letters*, vol. 29, pp. 328–330, 4 2008.

[117] Ioffe Institute, "NSM Archive - Silicon Germanium (SiGe)," 2024.

[118] F. K. LeGoues, R. Rosenberg, T. Nguyen, F. Himpsel, and B. S. Meyerson, "Oxidation studies of SiGe," *Journal of Applied Physics*, vol. 65, no. 4, pp. 1724–1728, 1989.

[119] M. S. Kavrik, P. Ercius, J. Cheung, K. Tang, Q. Wang, B. Fruhberger, M. Kim, Y. Taur, P. C. McIntyre, and A. C. Kummel, "Engineering High-k/SiGe Interface with ALD Oxide for Selective GeOx Reduction," *ACS Applied Materials and Interfaces*, vol. 11, pp. 15111–15121, 4 2019.

[120] V. Semiconductor, "The General Properties of Si, Ge, SiGe, SiO2 and Si3N4," tech. rep., Virginia Semiconductor, 2002.

[121] Ioffe Institute, "NSM Archive - Physical Properties of Semiconductors," 2024.

[122] Y. Song, A. L. Schmitt, and S. Jin, "Ultralong single-crystal metallic Ni2Si nanowires with low resistivity," *Nano Letters*, vol. 7, pp. 965–969, 4 2007.

[123] W. Lu and C. M. Lieber, "Semiconductor nanowires," *Journal of Physics D: Applied Physics*, vol. 39, no. 21, 2006.

[124] F. Altomare and A. M. Chang, *One-Dimensional Superconductivity in Nanowires*. John Wiley & Sons, 2013.

[125] J. Hu, T. W. Odom, and C. M. Lieber, "Chemistry and physics in one dimension: Synthesis and properties of nanowires and nanotubes," *Accounts of Chemical Research*, vol. 32, pp. 435–445, 5 1999.

[126] C. M. Lieber and Z. L. Wang, "Functional nanowires," *MRS Bulletin*, vol. 32, pp. 99–108, 1 2007.

[127] R. S. Wagner and W. C. Ellis, "Vapor-liquid-solid mechanism of single crystal growth," *Applied Physics Letters*, vol. 4, pp. 89–90, 3 1964.

[128] N. Singh, K. D. Buddharaju, S. K. Manhas, A. Agarwal, S. C. Rustagi, G. Q. Lo, N. Balasubramanian, and D. L. Kwong, "Si, SiGe nanowire devices by top-down technology and their applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 11, pp. 3107–3118, 2008.

[129] S. Barraud, B. Previtali, V. Lapras, R. Coquand, C. Vizioz, J. M. Hartmann, and M. Cassé, "Top-down fabrication and electrical characterization of Si and SiGe nanowires for advanced CMOS technologies," *Semiconductor Science and Technology*, vol. 34, 6 2019.

[130] R. G. Hobbs, N. Petkov, and J. D. Holmes, "Semiconductor nanowire fabrication by bottom-up and top-down paradigms," *Chemistry of Materials*, vol. 24, pp. 1975–1991, 6 2012.

[131] L. J. Lauhon, M. S. Gudlksen, D. Wang, and C. M. Lieber, "Epitaxial core-shell and core-multishell nanowire heterostructures," *Nature*, vol. 420, pp. 57–61, 11 2002.

[132] Y. Cui, X. Duan, J. Hu, and C. M. Lieber, "Doping and electrical transport in silicon nanowires," *Journal of Physical Chemistry B*, vol. 104, pp. 5215–5216, 6 2000.

[133] G. Larrieu, Y. Guerfi, X. L. Han, and N. Clement, "Vertical field effect transistor with sub-15nm gate-all-around on Si nanowire array," *European Solid-State Device Research Conference*, vol. 2015-Novem, pp. 202–205, 11 2015.

[134] Y. Guerfi and G. Larrieu, "Vertical Silicon Nanowire Field Effect Transistors with Nanoscale Gate-All-Around," *Nanoscale Research Letters*, vol. 11, pp. 1–7, 12 2016.

[135] S. T. Picraux, S. A. Dayeh, P. Manandhar, D. E. Perea, and S. G. Choi, "Silicon and germanium nanowires: Growth, properties, and integration," *Jom*, vol. 62, pp. 35–43, 4 2010.

[136] S. Pregl, A. Heinzig, L. Baraban, G. Cuniberti, T. Mikolajick, and W. M. Weber, "Printable parallel arrays of Si nanowire schottky-barrier-FETs with tunable polarity for complementary logic," *IEEE Transactions on Nanotechnology*, vol. 15, pp. 549–556, 5 2016.

[137] L. Yu and P. R. I Cabarrocas, "Growth mechanism and dynamics of in-plane solid-liquid-solid silicon nanowires," *Physical Review B - Condensed Matter and Materials Physics*, vol. 81, p. 085323, 2 2010.

[138] R. Hu, S. Xu, J. Wang, Y. Shi, J. Xu, K. Chen, and L. Yu, "Unprecedented Uniform 3D Growth Integration of 10-Layer Stacked Si Nanowires on Tightly Confined Sidewall

Grooves," *Nano Letters*, vol. 20, pp. 7489–7497, 10 2020.

[139] J. Kaur, A. Parmar, and S. K. Tripathi, "Understanding quantum confinement in nanowires: basics, applications and possible laws," *Journal of Physics: Condensed Matter*, vol. 26, p. 423202, 9 2014.

[140] Y. Wu and P. Yang, "Germanium nanowire growth via simple vapor transport," *Chemistry of Materials*, vol. 12, pp. 605–607, 3 2000.

[141] D. D. Ma, C. S. Lee, F. C. Au, S. Y. Tong, and S. T. Lee, "Small-diameter silicon nanowire surfaces," *Science*, vol. 299, pp. 1874–1877, 3 2003.

[142] H. Scheel, S. Reich, and C. Thomsen, "Electronic band structure of high-index silicon nanowires," *physica status solidi (b)*, vol. 242, pp. 2474–2479, 10 2005.

[143] M. J. Gilbert, R. Akis, and D. K. Ferry, "Phonon-assisted ballistic to diffusive crossover in silicon nanowire transistors," *Journal of Applied Physics*, vol. 98, p. 94303, 11 2005.

[144] G. D. Yuan, Y. B. Zhou, C. S. Guo, W. J. Zhang, Y. B. Tang, Y. Q. Li, Z. H. Chen, Z. B. He, X. J. Zhang, P. F. Wang, I. Bello, R. Q. Zhang, C. S. Lee, and S. T. Lee, "Tunable electrical properties of silicon nanowires via surface-ambient chemistry," *ACS Nano*, vol. 4, pp. 3045–3052, 6 2010.

[145] M. Amato and R. Rurali, "Surface physics of semiconducting nanowires," *Progress in Surface Science*, vol. 91, pp. 1–28, 2 2016.

[146] R. R. Razouk and B. E. Deal, "Dependence of Interface State Density on Silicon Thermal Oxidation Process Variables," *Journal of The Electrochemical Society*, vol. 126, pp. 1573–1581, 9 1979.

[147] D. K. Schroder, *Semiconductor Material and Device Characterization: Third Edition*. Hoboken, NJ, USA: John Wiley & Sons, Inc., 10 2005.

[148] S. Vitusevich and I. Zadorozhnyi, "Noise spectroscopy of nanowire structures: Fundamental limits and application aspects," 3 2017.

[149] R. T. Tung, "Formation of an electric dipole at metal-semiconductor interfaces," *Physical Review B - Condensed Matter and Materials Physics*, vol. 64, p. 205310, 11 2001.

[150] K. H. Hong, J. Kim, S. H. Lee, and J. K. Shin, "Strain-driven electronic band

structure modulation of Si nanowires," *Nano Letters*, vol. 8, pp. 1335–1340, 5 2008.

[151] S. M. Koo, A. Fujiwara, J. P. Han, E. M. Vogel, C. A. Richter, and J. E. Bonevich, "High inversion current in silicon nanowire field effect transistors," *Nano Letters*, vol. 4, pp. 2197–2201, 11 2004.

[152] Y. Sun, S. E. Thompson, and T. Nishida, *Strain effect in semiconductors: Theory and device applications*. No. 1, Boston, MA: Springer US, 1 ed., 2010.

[153] O. Gunawan, L. Sekaric, A. Majumdar, M. Rooks, J. Appenzeller, J. W. Sleight, S. Guha, and Wilfried Haensch, "Measurement of carrier mobility in silicon nanowires," *Nano Letters*, vol. 8, pp. 1566–1571, 6 2008.

[154] A. Echresh, H. Arora, F. Fuchs, Z. Li, R. Hübner, S. Prucnal, J. Schuster, P. Zahn, M. Helm, S. Zhou, A. Erbe, L. Rebohle, and Y. M. Georgiev, "Electrical characterization of germanium nanowires using a symmetric hall bar configuration: Size and shape dependence," *Nanomaterials*, vol. 11, p. 2917, 10 2021.

[155] J. L. Murray and A. J. McAlister, "The Al-Si (Aluminum-Silicon) system," *Bulletin of Alloy Phase Diagrams*, vol. 5, pp. 74–84, 2 1984.

[156] W. Gale and T. Totemeier, "13 - Diffusion in metals," in *Smithells Metals Reference Book*, pp. 1–120, Butterworth-Heinemann, 8 ed., 2004.

[157] V. Cirigliano, J. F. Donoghue, E. Golowich, D. Demireva, and B. Lämmel, "On the diffusion of Al into Si under the influence of laser radiation from a Nd:YAG laser," *Journal of Physics D: Applied Physics*, vol. 30, p. 1972, 7 1997.

[158] A. Paccagnella, G. Ottaviani, P. Fabbri, G. Ferla, and G. Queirolo, "Silicon diffusion in aluminium," *Thin Solid Films*, vol. 128, pp. 217–223, 6 1985.

[159] H. J. Gossmann, C. S. Rafferty, H. S. Luftman, F. C. Unterwald, T. Boone, and J. M. Poate, "Oxidation enhanced diffusion in Si B-doping superlattices and Si self-interstitial diffusivities," *Applied Physics Letters*, vol. 63, pp. 639–641, 8 1993.

[160] A. J. McAlister and J. L. Murray, "The Al-Ge (Aluminum-Germanium) system," *Bulletin of Alloy Phase Diagrams*, vol. 5, pp. 341–347, 8 1984.

[161] H. Bracht and N. Stolwijk, "Diffusion in Ge," in *Diffusion in Semiconductors* (D. L. Beke, ed.), Landolt-Börnstein - Group III Condensed Matter, ch. 2, Berlin/Heidelberg: Springer-Verlag, 33a ed., 1998.

[162] L. Wind, M. Sistani, Z. Song, X. Maeder, D. Pohl, J. Michler, B. Rellinghaus, W. M. Weber, and A. Lugstein, "Monolithic Metal-Semiconductor-Metal Heterostructures Enabling Next-Generation Germanium Nanodevices," *ACS Applied Materials and Interfaces*, vol. 13, pp. 12393–12399, 3 2021.

[163] H. Bracht and N. A. Stolwijk, "Diffusion in Si-Ge alloys," in *Diffusion in Semiconductors* (D. Beke, ed.), ch. 2, Berlin/Heidelberg: Springer-Verlag, 33a ed., 1998.

[164] M. A. Luong, E. Robin, N. Pauc, P. Gentile, T. Baron, B. Salem, M. Sistani, A. Lugstein, M. Spies, B. Fernandez, and M. Den Hertog, "Reversible Al propagation in SixGe1-xnanowires: Implications for electrical contact formation," *ACS Applied Nano Materials*, vol. 3, pp. 10427–10436, 10 2020.

[165] D. Connelly, C. Faulkner, P. A. Clifton, and D. E. Grupp, "Fermi-level depinning for low-barrier Schottky source/drain transistors," *Applied Physics Letters*, vol. 88, p. 012105, 1 2006.

[166] Y. Wu, J. Xiang, C. Yang, W. Lu, and C. M. Lieber, "Single-crystal metallic nanowires and metal/semiconductor nanowire heterostructures," *Nature*, vol. 430, pp. 61–65, 7 2004.

[167] Y. C. Lin, K. C. Lu, W. W. Wu, J. Bai, L. J. Chen, K. N. Tu, and Y. Huang, "Single crystalline PtSi nanowires, PtSi/Si/PtSi nanowire heterostructures, and nanodevices," *Nano Letters*, vol. 8, pp. 913–918, 3 2008.

[168] Y.-C. Chou, W.-W. Wu, S.-L. Cheng, B.-Y. Yoo, N. Myung, L. J. Chen, and K. N. Tu, "In-situ TEM observation of repeating events of nucleation in epitaxial growth of nano CoSi2 in nanowires of Si.," *Nano letters*, vol. 8, pp. 2194–9, 8 2008.

[169] M. Sistani, J. Delaforce, K. Bharadwaj, M. Luong, J. Nacenta Mendivil, N. Roch, M. Den Hertog, R. B. Kramer, O. Buisson, A. Lugstein, and C. Naud, "Coulomb blockade in monolithic and monocrystalline Al-Ge-Al nanowire heterostructures," *Applied Physics Letters*, vol. 116, p. 13105, 1 2020.

[170] K. Aggarwal, A. Hofmann, D. Jirovec, I. Prieto, A. Sammak, M. Botifoll, S. Martí-Sánchez, M. Veldhorst, J. Arbiol, G. Scappucci, J. Danon, and G. Katsaros, "Enhancement of proximity-induced superconductivity in a planar Ge hole gas," *Physical Review Research*, vol. 3, p. L022005, 4 2021.

[171] T. Luo, M. Bertoglio, C. Girardeaux, and D. Mangelinck, "Evolution of early formed NiSi2 during the reaction between Ni(W, Pt) films and Si (001)," *Micro and Nano Engineering*, vol. 1, pp. 49–55, 11 2018.

[172] L. Knoll, Q. T. Zhao, S. Habicht, C. Urban, K. K. Bourdelle, and S. Mantl, "Formation and characterization of ultra-thin Ni silicides on strained and unstrained silicon," *IWJT-2010: Extended Abstracts - 2010 International Workshop on Junction Technology*, pp. 52–56, 2010.

[173] H. Iwai, T. Ohguro, and S. i. Ohmi, "NiSi salicide technology for scaled CMOS," *Microelectronic Engineering*, vol. 60, pp. 157–169, 1 2002.

[174] H. Yu, M. Schaekers, T. Schram, W. Aderhold, A. J. Mayur, J. Mitard, L. Witters, K. Barla, N. Collaert, N. Horiguchi, A. V. Y. Thean, and K. De Meyer, "Low-resistance titanium contacts and thermally unstable nickel germanide contacts on p-type germanium," *IEEE Electron Device Letters*, vol. 37, pp. 482–485, 4 2016.

[175] N. S. Dellas, S. Minassian, J. M. Redwing, and S. E. Mohney, "Formation of nickel germanide contacts to Ge nanowires," *Applied Physics Letters*, vol. 97, p. 263116, 12 2010.

[176] E. Rhoderick and R. Williams, *Metal-Semiconductor Contacts*. Oxford: Oxford University Press, 1988.

[177] J. M. Andrews and M. P. Lepselter, "Reverse current-voltage characteristics of metal-silicide Schottky diodes," *Solid-State Electronics*, vol. 13, pp. 1011–1023, 7 1970.

[178] L. E. Calvet, *Electrical Transport in Schottky Barrier MOSFETs*. PhD thesis, Yale University, 2001.

[179] R. T. Tung, "Recent advances in Schottky barrier concepts," *Materials Science and Engineering: R: Reports*, vol. 35, no. 1-3, pp. 1–138, 2001.

[180] J. Knoch, M. Zhang, Q. T. Zhao, S. Lenk, S. Mantl, and J. Appenzeller, "Effective Schottky barrier lowering in silicon-on-insulator Schottky-barrier metal-oxide-semiconductor field-effect transistors using dopant segregation," *Applied Physics Letters*, vol. 87, pp. 1–3, 12 2005.

[181] S. Nagarajan, T. Mikolajick, and J. Trommer, "Dopant segregation effects on ohmic contact formation in nanoscale silicon," *Solid-State Electronics*, vol. 208, 2023.

[182] A. Agrawal, J. Lin, M. Barth, R. White, B. Zheng, S. Chopra, S. Gupta, K. Wang, J. Gelatos, S. E. Mohney, and S. Datta, "Fermi level depinning and contact resistivity reduction using a reduced titania interlayer in n-silicon metal-insulator-semiconductor ohmic contacts," *Applied Physics Letters*, vol. 104, p. 112101, 3 2014.

[183] R. Islam, G. Shine, and K. C. Saraswat, "Schottky barrier height reduction for holes by Fermi level depinning using metal/nickel oxide/silicon contacts," *Applied Physics Letters*, vol. 105, p. 182103, 11 2014.

[184] S. B. Eadi, J. C. Lee, H. S. Song, J. Oh, G. W. Lee, and H. D. Lee, "Effective Schottky barrier lowering of NiGe/p-Ge(100) using Terbium interlayer structure for high performance p-type MOSFETs," *Scientific Reports*, vol. 10, pp. 1–9, 3 2020.

[185] R. D. Clark, "Emerging applications for high K materials in VLSI technology," *Materials*, vol. 7, pp. 2913–2944, 4 2014.

[186] A. M. Cowley and S. M. Sze, "Surface States and Barrier Height of Metal-Semiconductor Systems," *Journal of Applied Physics*, vol. 36, pp. 3212–3220, 10 1965.

[187] M. Tao, D. Udeshi, S. Agarwal, R. Kolappan, Y. Xu, E. Maldonado, and W. P. Kirk, "Se-passivated Si(100) surface for low and negative Schottky barriers," in *Extended Abstracts of the Fourth International Workshop on Junction Technology, IWJT 2004*, vol. 4, pp. 119–122, IEEE, 2004.

[188] M. Tao, D. Udeshi, S. Agarwal, E. Maldonado, and W. P. Kirk, "Negative Schottky barrier between titanium and n-type Si(0 0 1) for low-resistance ohmic contacts," *Solid-State Electronics*, vol. 48, pp. 335–338, 2 2004.

[189] A. Thanailakis, D. S. Chan, and D. C. Northrop, "Activation energy for the slow states in the aluminium-germanium contact," *Journal of Physics D: Applied Physics*, vol. 5, pp. 1930–1936, 10 1972.

[190] A. Dimoulas, P. Tsipas, A. Sotiropoulos, and E. K. Evangelou, "Fermi-level pinning and charge neutrality level in germanium," *Applied Physics Letters*, vol. 89, p. 252110, 12 2006.

[191] P. Tsipas and A. Dimoulas, "Modeling of negatively charged states at the Ge surface and interfaces," *Applied Physics Letters*, vol. 94, p. 012114, 1 2009.

[192] D. D. Zhao, T. Nishimura, C. H. Lee, K. Nagashio, K. Kita, and A. Toriumi, "Junctionless Ge p-Channel metal-oxide-semiconductor field-effect transistors fabricated on ultrathin ge-on-insulator substrate," *Applied Physics Express*, vol. 4, p. 031302, 3 2011.

[193] Y. Zhou, M. Ogawa, X. Han, and K. L. Wang, "Alleviation of Fermi-level pinning effect on metal/germanium interface by insertion of an ultrathin aluminum oxide," *Applied Physics Letters*, vol. 93, p. 202105, 11 2008.

[194] D. R. Gajula, P. Baine, M. Modreanu, P. K. Hurley, B. M. Armstrong, and D. W. McNeill, "Fermi level de-pinning of aluminium contacts to n-type germanium using thin atomic layer deposited layers," *Applied Physics Letters*, vol. 104, p. 012102, 1 2014.

[195] M. P. Lefselter and S. M. Sze, "SB-IGFET: An Insulated-Gate Field-Effect Transistor Using Schottky Barrier Contacts for Source and Drain," *Proceedings of the IEEE*, vol. 56, no. 8, pp. 1400–1402, 1968.

[196] M. Sugino, L. A. Akers, and M. E. Rebeschini, "CMOS Latch-up elimination using Schottky barrier PMOS," in *Technical Digest - International Electron Devices Meeting*, pp. 462–465, IEEE, 1982.

[197] S. Swirhun, E. Sangiorgi, A. J. Weeks, R. M. Swanson, K. C. Saraswat, and R. W. Dutton, "A VLSI-Suitable Schottky-Barrier CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 1, pp. 114–122, 1985.

[198] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, "Carbon Nanotubes as Schottky Barrier Transistors," *Physical Review Letters*, vol. 89, p. 106801, 8 2002.

[199] Y. Zhou, L. Tong, Z. Chen, L. Tao, Y. Pang, and J. B. Xu, "Contact-engineered reconfigurable two-dimensional Schottky junction field-effect transistor with low leakage currents," *Nature Communications*, vol. 14, pp. 1–10, 7 2023.

[200] J. Park, J. Son, S. K. Park, D. S. Lee, and D. Y. Jeon, "Two-dimensional material-based complementary ambipolar field-effect transistors with ohmic-like contacts," *Nanotechnology*, vol. 34, p. 325705, 5 2023.

[201] R. Labar and T. K. Kundu, "Fabrication and Characterization of Back-to-Back Schottky Diode in Ni/ZnO/Ag Nanojunction," *Journal of Electronic Materials*, vol. 51, pp. 223–231, 1 2022.

[202] C. Roemer, G. Darbandy, M. Schwarz, J. Trommer, A. Heinzig, T. Mikolajick, W. M. Weber, B. Iniguez, and A. Kloes, "Physics-Based DC Compact Modeling of Schottky Barrier and Reconfigurable Field-Effect Transistors," *IEEE Journal of the Electron Devices Society*, vol. 10, pp. 416–423, 2022.

[203] C. Roemer, N. Dersch, G. Darbandy, M. Schwarz, Y. Han, Q. T. Zhao, B. Iñíguez, and A. Kloes, "Compact modeling of Schottky barrier field-effect transistors at deep cryogenic temperatures," *Solid-State Electronics*, vol. 207, p. 108686, 9 2023.

[204] G. Shao and G. Shao, "Work Function and Electron Affinity of Semiconductors: Doping Effect and Complication due to Fermi Level Pinning," *Energy & Environmental Materials*, vol. 4, pp. 273–276, 7 2021.

[205] B. Sun, B. Richstein, P. Liebisch, T. Frahm, S. Scholz, J. Trommer, T. Mikolajick, and J. Knoch, "On the Operation Modes of Dual-Gate Reconfigurable Nanowire Transistors," *IEEE Transactions on Electron Devices*, vol. 68, no. 7, pp. 3684–3689, 2021.

[206] G. Krieger and R. M. Swanson, "Fowler-Nordheim electron tunneling in thin Si-SiO2-Al structures," *Journal of Applied Physics*, vol. 52, no. 9, pp. 5710–5717, 1981.

[207] G. Baccarani, "Current transport in Schottky-barrier diodes," *Journal of Applied Physics*, vol. 47, pp. 4122–4126, 9 1976.

[208] J. Appenzeller, M. Radosavljević, J. Knoch, and P. Avouris, "Tunneling Versus Thermionic Emission in One-Dimensional Semiconductors," *Physical Review Letters*, vol. 92, p. 4, 1 2004.

[209] C. R. Crowell and V. L. Rideout, "Normalized thermionic-field (T-F) emission in metal-semiconductor (Schottky) barriers," *Solid-State Electronics*, vol. 12, pp. 89–105, 2 1969.

[210] T. Baldauf, A. Heinzig, J. Trommer, T. Mikolajick, and W. M. Weber, "Tuning the tunneling probability by mechanical stress in Schottky barrier based reconfigurable nanowire transistors," *Solid-State Electronics*, vol. 128, pp. 148–154, 2 2017.

[211] J. Beister, A. Wachowiak, A. Heinzig, J. Trommer, T. Mikolajick, and W. M. Weber, "Temperature dependent switching behaviour of nickel silicided undoped silicon nanowire devices," *Physica Status Solidi (C) Current Topics in Solid State Physics*, vol. 11, pp. 1611–1617, 11 2014.

[212] T. Baldauf, A. Heinzig, T. Mikolajick, and W. M. Weber, "Scaling Aspects of Nanowire Schottky Junction based Reconfigurable Field Effect Transistors," *2019 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon, EUROSOI-ULIS 2019*, pp. 1–4, 4 2019.

[213] A. U. Pacheco-Sánchez, *Determination of key device parameters for short-and long-channel Schottky-type carbon nanotube field-effect transistors*. PhD thesis, TU Dresden, 2019.

[214] M. Di Ventra, "Electrical transport in nanoscale systems," *Electrical Transport in*

Nanoscale Systems, vol. 9780521896, pp. 1–476, 1 2008.

[215] A. Pacheco-Sanchez and M. Claus, "Device design-enabled Schottky barrier height extraction for nanoFETs based on the 1D Landauer-Büttiker equation," *Applied Physics Letters*, vol. 111, p. 163108, 10 2017.

[216] A. Pacheco-Sanchez, Q. Torrent, and D. Jiménez, "Schottky-like barrier characterization of field-effect transistors with multiple quasi-ballistic channels," *Journal of Applied Physics*, vol. 132, p. 24501, 7 2022.

[217] M. Claus, *Modeling of Ballistic Carbon Nanotube Transistors for Analog High-Frequency Applications*. PhD thesis, TU Dresden, 2011.

[218] A. F. Gonzalez, M. Bhattacharya, S. Kulkarni, and P. Mazumder, "Standard CMOS implementation of a multiple-valued logic signed-digit adder based on negative differential-resistance devices," in *Proceedings of The International Symposium on Multiple-Valued Logic*, pp. 323–328, IEEE Comput. Soc, 2000.

[219] D. S. Liang, C. C. Tai, K. J. Gan, C. S. Tsai, and Y. H. Chen, "Design of AND and NAND logic gate using NDR-based circuit suitable for CMOS process," in *IEEE Asia-Pacific Conference on Circuits and Systems, Proceedings, APCCAS*, pp. 1325–1328, IEEE, 12 2006.

[220] J. B. Gunn, "Microwave oscillations of current in III-V semiconductors," *Solid State Communications*, vol. 1, pp. 88–91, 9 1963.

[221] D. Shiri, A. Verma, R. Nekovei, A. Isacsson, C. R. Selvakumar, and M. P. Anantram, "Gunn-Hilsum Effect in Mechanically Strained Silicon Nanowires: Tunable Negative Differential Resistance," *Scientific Reports 2018 8:1*, vol. 8, pp. 1–10, 4 2018.

[222] J. E. Smith, M. I. Nathan, J. C. McGroddy, S. A. Porowski, and W. Paul, "GUNN EFFECT IN n-TYPE InSb," *Applied Physics Letters*, vol. 15, pp. 242–245, 10 1969.

[223] N. Suntornwipat, S. Majdi, M. Gabrysch, I. Friel, and J. Isberg, "Observation of transferred-electron oscillations in diamond," *Applied Physics Letters*, vol. 115, 11 2019.

[224] K. S. Berezowski and S. B. Vrudhula, "Multiple-Valued Logic Circuits Design Using Negative Differential Resistance Devices," in *37th International Symposium on Multiple-Valued Logic (ISMVL'07)*, pp. 24–24, IEEE, 5 2007.

[225] S. Shin and K. R. Kim, "Multiple negative differential resistance devices with ultra-high peak-to-valley current ratio for practical multi-valued logic and memory applica-

tions," *Japanese Journal of Applied Physics*, vol. 54, p. 06FG07, 6 2015.

[226] Y. Meng, W. Wang, W. Wang, B. Li, Y. Zhang, and J. Ho, "Anti-Ambipolar Heterojunctions: Materials, Devices, and Circuits," *Advanced Materials*, vol. 36, p. 2306290, 4 2024.

[227] K. Smith, "A multiple valued logic: a tutorial and appreciation," *Computer*, vol. 21, pp. 17–27, 4 1988.

[228] Si-Young Park, R. Anisha, P. Berger, R. Loo, Ngoc Duy Nguyen, S. Takeuchi, and M. Caymax, "Si/SiGe Resonant Interband Tunneling Diodes Incorporating δ-Doping Layers Grown by Chemical Vapor Deposition," *IEEE Electron Device Letters*, vol. 30, pp. 1173–1175, 11 2009.

[229] M. Herzig, M. Weiher, A. Ascoli, R. Tetzlaff, T. Mikolajick, and S. Slesazeck, "Multiple slopes in the negative differential resistance region of NbOx-based threshold switches," *Journal of Physics D: Applied Physics*, vol. 52, p. 325104, 6 2019.

[230] W. Fawcett and E. G. Paige, "Negative differential mobility of electrons in germanium: A Monte Carlo calculation of the distribution function, drift velocity and carrier population in the (111) and (100) minima," *Journal of Physics C: Solid State Physics*, vol. 4, pp. 1801–1821, 9 1971.

[231] C. Jacoboni, F. Nava, C. Canali, and G. Ottaviani, "Electron drift velocity and diffusivity in germanium," *Physical Review B*, vol. 24, pp. 1014–1026, 7 1981.

[232] E. Conwell, "High field transport in semiconductors," in *Solid State Physics* (F. Seitz, D. Turnbull, and H. Ehrenreich, eds.), Academic Press, 1967.

[233] P. R. Berger and A. Ramesh, "Negative Differential Resistance Devices and Circuits," in *Comprehensive Semiconductor Science and Technology*, vol. 1-6, pp. 176–241, Elsevier, 1 2011.

[234] M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P. E. Gaillardon, Y. Leblebici, and G. De Micheli, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs," in *Technical Digest - International Electron Devices Meeting, IEDM*, pp. 1–8, IEEE, 12 2012.

[235] J. Trommer, A. Heinzig, U. Mühle, M. Löffler, A. Winzer, P. M. Jordan, J. Beister, T. Baldauf, M. Geidel, B. Adolphi, E. Zschech, T. Mikolajick, and W. M. Weber, "Enabling Energy Efficiency and Polarity Control in Germanium Nanowire Transistors by Individually Gated Nanojunctions," *ACS Nano*, vol. 11, pp. 1704–1711, 2 2017.

[236] R. Böckle, M. Sistani, B. Lipovec, D. Pohl, B. Rellinghaus, A. Lugstein, and W. M. Weber, "A Top-Down Platform Enabling Ge Based Reconfigurable Transistors," *Advanced Materials Technologies*, vol. 7, p. 2100647, 1 2022.

[237] Y. M. Lin, J. Appenzeller, and P. Avouris, "Novel carbon nanotube FET design with tunable polarity," *Technical Digest - International Electron Devices Meeting, IEDM*, pp. 687–690, 2004.

[238] N. Harada, K. Yagi, S. Sato, and N. Yokoyama, "A polarity-controllable graphene inverter," *Applied Physics Letters*, vol. 96, no. 1, p. 012102, 2010.

[239] T. Kim, D. Lim, J. Son, K. Cho, and S. Kim, "Reconfiguration of operation modes in silicon nanowire field-effect transistors by electrostatic virtual doping," *Nanotechnology*, vol. 33, p. 415203, 7 2022.

[240] S. Larentis, B. Fallahazad, H. C. Movva, K. Kim, A. Rai, T. Taniguchi, K. Watanabe, S. K. Banerjee, and E. Tutuc, "Reconfigurable Complementary Monolayer MoTe2 Field-Effect Transistors for Integrated Circuits," *ACS Nano*, vol. 11, pp. 4832–4839, 5 2017.

[241] P. Wu, D. Reis, X. S. Hu, and J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics*, vol. 4, pp. 45–53, 1 2021.

[242] Y. Shingaya, A. Zulkefli, T. Iwasaki, R. Hayakawa, S. Nakaharai, K. Watanabe, T. Taniguchi, and Y. Wakayama, "Dual-Gate Anti-Ambipolar Transistor with Van der Waals ReS2/WSe2 Heterojunction for Reconfigurable Logic Operations," *Advanced Electronic Materials*, vol. 9, no. 1, p. 2200704, 2023.

[243] A. Heinzig, T. Mikolajick, J. Trommer, D. Grimm, and W. M. Weber, "Dually active silicon nanowire transistors and circuits with equal electron and hole transport," *Nano Letters*, vol. 13, pp. 4176–4181, 9 2013.

[244] J. Trommer, A. Heinzig, T. Baldauf, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Functionality-Enhanced Logic Gate Design Enabled by Symmetrical Reconfigurable Silicon Nanowire Transistors," *IEEE Transactions on Nanotechnology*, vol. 14, pp. 689–698, 7 2015.

[245] M. Simon, B. Liang, D. Fischer, M. Knaut, A. Tahn, T. Mikolajick, and W. M. Weber, "Top-Down Fabricated Reconfigurable FET with Two Symmetric and High-Current On-States," *IEEE Electron Device Letters*, vol. 41, pp. 1110–1113, 7 2020.

[246] P. Dai, A. Gao, N. Lu, T. Li, and Y. Wang, "A back-gate controlled silicon nanowire sensor with sensitivity improvement for DNA and pH detection," *Japanese Journal of Applied Physics*, vol. 52, p. 121301, 12 2013.

[247] F. M. Zörgiebel, S. Pregl, L. Römhildt, J. Opitz, W. Weber, T. Mikolajick, L. Baraban, and G. Cuniberti, "Schottky barrier-based silicon nanowire pH sensor with live sensitivity control," *Nano Research*, vol. 7, pp. 263–271, 2 2014.

[248] S. Pregl, L. Baraban, V. Sessi, T. Mikolajick, W. M. Weber, and G. Cuniberti, "Signal and Noise of Schottky-Junction Parallel Silicon Nanowire Transducers for Biochemical Sensing," *IEEE Sensors Journal*, vol. 18, pp. 967–975, 2 2018.

[249] P. Cadareanu and P. E. Gaillardon, "A TCAD Simulation Study of Three-Independent-Gate Field-Effect Transistors at the 10-nm Node," *IEEE Transactions on Electron Devices*, vol. 68, pp. 4129–4135, 8 2021.

[250] M. Raitza, A. Kumar, M. Völp, D. Walter, J. Trommer, T. Mikolajick, and W. M. Weber, "Exploiting transistor-level reconfiguration to optimize combinational circuits," in *Proceedings of the 2017 Design, Automation and Test in Europe, DATE 2017*, pp. 338–343, IEEE, 3 2017.

[251] S. Rai, J. Trommer, M. Raitza, T. Mikolajick, W. M. Weber, and A. Kumar, "Designing efficient circuits based on runtime-reconfigurable field-effect transistors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, pp. 560–572, 3 2019.

[252] J. Trommer, A. Heinzig, T. Baldauf, T. Mikolajick, W. M. Weber, M. Raitza, and M. Völp, "Reconfigurable nanowire transistors with multiple independent gates for efficient and programmable combinational circuits," in *Proceedings of the 2016 Design, Automation and Test in Europe Conference and Exhibition, DATE 2016*, pp. 169–174, Research Publishing Services, 2016.

[253] M. D. Marchi, J. Zhang, S. Frache, D. Sacchetto, P. E. Gaillardon, Y. Leblebici, and G. D. Micheli, "Configurable logic gates using polarity-controlled silicon nanowire gate-all-around FETs," *IEEE Electron Device Letters*, vol. 35, no. 8, pp. 880–882, 2014.

[254] M. Tsuchiya, H. Sakaki, and J. Yoshino, "Room temperature observation of differential negative resistance in an alas/gaas/alas resonant tunneling diode," *Japanese Journal of Applied Physics*, vol. 24, pp. L466–L468, 6 1985.

[255] H. Grubin, *The physics of semiconductor devices*, vol. 15. Wiley-Interscience, 12 2004.

[256] H. Schmid, C. Bessire, M. T. Björk, A. Schenk, and H. Riel, "Silicon nanowire Esaki diodes," *Nano Letters*, vol. 12, pp. 699–703, 2 2012.

[257] D. M. Chang and J. G. Ruch, "MEASUREMENT OF THE VELOCITY FIELD CHARACTERISTIC OF ELECTRONS IN GERMANIUM," *Applied Physics Letters*, vol. 12, pp. 111–112, 2 1968.

[258] M. Sistani, *Transport in ultra-scaled Ge quantum dots embedded in Al-Ge-Al nanowire heterostructures*. PhD thesis, TU Wien, 2019.

[259] W. J. Berghuis, J. Melskens, B. Macco, R. J. Theeuwes, M. A. Verheijen, and W. M. Kessels, "Surface passivation of germanium by atomic layer deposited Al2O3 nanolayers," *Journal of Materials Research*, vol. 36, pp. 571–581, 2 2021.

[260] E. H. Nicollian, C. N. Berglund, P. F. Schmidt, and J. M. Andrews, "Electrochemical Charging of Thermal SiO2 Films by Injected Electron Currents," *Journal of Applied Physics*, vol. 42, pp. 5654–5664, 12 1971.

[261] K. I. Seo, S. Sharma, A. A. Yasseri, D. R. Stewart, and T. I. Kamins, "Surface charge density of unpassivated and passivated metal-catalyzed silicon nanowires," *Electrochemical and Solid-State Letters*, vol. 9, p. G69, 1 2006.

[262] M. Sistani, P. Staudinger, and A. Lugstein, "Polarity Control in Ge Nanowires by Electronic Surface Doping," *Journal of Physical Chemistry C*, vol. 124, pp. 19858–19863, 9 2020.

[263] M. I. den Hertog, *Characterization of silicon nanowires by transmission electron microscopy*. PhD thesis, Université Joseph Fourier - Grenoble I, 2010.

[264] M. Spies, Z. Sadre Momtaz, J. Lähnemann, M. Anh Luong, B. Fernandez, T. Fournier, E. Monroy, and M. Den Hertog, "Correlated and in-situ electrical transmission electron microscopy studies and related membrane-chip fabrication," *Nanotechnology*, vol. 31, p. 472001, 9 2020.

[265] A. P. Conlan, M. A. Luong, P. Gentile, G. Moldovan, M. I. Den Hertog, E. Monroy, and D. Cooper, "Thermally propagated Al contacts on SiGe nanowires characterized by electron beam induced current in a scanning transmission electron microscope," *Nanotechnology*, vol. 33, p. 035712, 10 2021.

[266] G. Chen, T. McGuckin, C. J. Hawley, E. M. Gallo, P. Prete, I. Miccoli, N. Lovergine, and J. E. Spanier, "Subsurface imaging of coupled carrier transport in GaAs/AlGaAs core-shell nanowires," *Nano Letters*, vol. 15, pp. 75–79, 1 2015.

[267] F. Donatini, A. De Luna Bugallo, P. Tchoulfian, G. Chicot, C. Sartel, V. Sallet, and J. Pernot, "Comparison of Three E-Beam Techniques for Electric Field Imaging and Carrier Diffusion Length Measurement on the Same Nanowires," *Nano Letters*, vol. 16, pp. 2938–2944, 5 2016.

[268] E. Gaubas and J. Vanhellemont, "Dependence of carrier lifetime in germanium on resisitivity and carrier injection level," *Applied Physics Letters*, vol. 89, p. 142106, 10 2006.

[269] Y. Han, J. Sun, B. Richstein, F. Allibert, I. Radu, J. H. Bae, D. Grutzmacher, J. Knoch, and Q. T. Zhao, "Steep Switching Si Nanowire p-FETs With Dopant Segregated Silicide Source/Drain at Cryogenic Temperature," *IEEE Electron Device Letters*, vol. 43, pp. 1187–1190, 8 2022.

[270] M. Kim, Y. Kim, D. Lim, S. Woo, K. Cho, and S. Kim, "Steep switching characteristics of single-gated feedback field-effect transistors," *Nanotechnology*, vol. 28, p. 055205, 2 2017.

[271] M. H. Lee, K. T. Chen, C. Y. Liao, S. S. Gu, G. Y. Siang, Y. C. Chou, H. Y. Chen, J. Le, R. C. Hong, Z. Y. Wang, S. Y. Chen, P. G. Chen, M. Tang, Y. D. Lin, H. Y. Lee, K. S. Li, and C. W. Liu, "Extremely Steep Switch of Negative-Capacitance Nanosheet GAA-FETs and FinFETs," in *Technical Digest - International Electron Devices Meeting, IEDM*, vol. 2018-Decem, pp. 1–31, IEEE, 12 2018.

[272] D. K. Schroder, "Oxide and Interface Trapped Charges, Oxide Thickness," in *Semiconductor Material and Device Characterization*, pp. 319–387, John Wiley & Sons, Inc., 4 2005.

[273] D. Y. Jeon, S. Pregl, S. J. Park, L. Baraban, G. Cuniberti, T. Mikolajick, and W. M. Weber, "Scaling and Graphical Transport-Map Analysis of Ambipolar Schottky-Barrier Thin-Film Transistors Based on a Parallel Array of Si Nanowires," *Nano Letters*, vol. 15, pp. 4578–4584, 7 2015.

[274] S. Kim, D. J. Hill, C. W. Pinion, J. D. Christesen, J. R. McBride, and J. F. Cahoon, "Designing Morphology in Epitaxial Silicon Nanowires: The Role of Gold, Surface Chemistry, and Phosphorus Doping," *ACS Nano*, vol. 11, pp. 4453–4462, 5 2017.

[275] S. Krylyuk, A. V. Davydov, I. Levin, A. Motayed, and M. D. Vaudin, "Rapid thermal oxidation of silicon nanowires," *Applied Physics Letters*, vol. 94, 2 2009.

[276] B. Liu, Y. Wang, T.-t. Ho, K.-K. Lew, S. M. Eichfeld, J. M. Redwing, T. S. Mayer, and S. E. Mohney, "Oxidation of silicon nanowires for top-gated field effect transistors,"

Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, vol. 26, pp. 370–374, 5 2008.

[277] E. A. Irene, H. Z. Massoud, and E. Tierney, "Silicon Oxidation Studies: Silicon Orientation Effects on Thermal Oxidation," *Journal of The Electrochemical Society*, vol. 133, pp. 1253–1256, 6 1986.

[278] P. Sutardja and W. G. Oldham, "Modeling of Stress Effects in Silicon Oxidation," *IEEE Transactions on Electron Devices*, vol. 36, no. 11, pp. 2415–2421, 1989.

[279] H. I. Liu, D. K. Biegelsen, F. A. Ponce, N. M. Johnson, and R. F. Pease, "Self-limiting oxidation for fabricating sub-5 nm silicon nanowires," *Applied Physics Letters*, vol. 64, pp. 1383–1385, 3 1994.

[280] E. E. Hunter and M. Silver, "Practical Electron Microscopy: A Beginner's Illustrated Guide," *Practical Electron Microscopy*, 9 1993.

[281] A. H. Carim, K.-k. Lew, and J. M. Redwing, "Bicrystalline Silicon Nanowires," *J. Am. Chem. Soc*, vol. 410, no. 19, p. 3165, 2001.

[282] V. Schmidt, J. V. Wittemann, and U. Gösele, "Growth, thermodynamics, and electrical properties of silicon nanowires," *Chemical Reviews*, vol. 110, pp. 361–388, 1 2010.

[283] J. T. Yue, W. P. Funsten, and R. V. Taylor, "Stress Induced Voids in Aluminum Interconnects During Ic Processing.," in *Annual Proceedings - Reliability Physics (Symposium)*, pp. 126–137, IEEE, 3 1985.

[284] M. A. Korhonen, W. R. LaFontaine, P. Borgesen, and C. Li, "Stress-induced Nucleation of Voids in narrow Aluminum-based Metallizations on Silicon Substrates," *Journal of Applied Physics*, vol. 70, pp. 6774–6781, 12 1991.

[285] M. A. Korhonen, C. A. Paszkiet, and C. Y. Li, "Mechanisms of thermal Stress Relaxation and Stress-induced Voiding in narrow Aluminum-based Metallizations," *Journal of Applied Physics*, vol. 69, pp. 8083–8091, 6 1991.

[286] T. Y. Tan and U. Gösele, "Diffusion in semiconductors," in *Diffusion in Condensed Matter: Methods, Materials, Models*, vol. 3, pp. 165–208, Berlin/Heidelberg: Springer-Verlag, 2005.

[287] B. Richstein, L. Hellmich, and J. Knoch, "Silicon Nitride Interface Engineering for Fermi Level Depinning and Realization of Dopant-Free MOSFETs," *Micro*, vol. 1,

pp. 228–241, 11 2021.

[288] L. Zhang, H. Li, Y. Guo, K. Tang, J. Woicik, J. Robertson, and P. C. Mcintyre, "Selective Passivation of GeO2/Ge Interface Defects in Atomic Layer Deposited High-k MOS Structures," *ACS Applied Materials and Interfaces*, vol. 7, pp. 20499–20506, 9 2015.

[289] M. Sistani, M. G. Bartmann, N. A. Güsken, R. F. Oulton, H. Keshmiri, M. S. Seifner, S. Barth, N. Fukata, M. A. Luong, M. I. Den Hertog, and A. Lugstein, "Nanoscale aluminum plasmonic waveguide with monolithically integrated germanium detector," *Applied Physics Letters*, vol. 115, p. 161107, 10 2019.

[290] S. Barth, R. Jimenez-Diaz, J. Samà, J. D. Prades, I. Gracia, J. Santander, C. Cane, and A. R. Romano-Rodriguez, "Localized growth and in situ integration of nanowires for device applications," *Chemical Communications*, vol. 48, pp. 4734–4736, 4 2012.

[291] I. R. Musin and M. A. Filler, "Chemical control of semiconductor nanowire kinking and superstructure," *Nano Letters*, vol. 12, pp. 3363–3368, 7 2012.

[292] S. V. Sivaram, N. Shin, L. W. Chou, and M. A. Filler, "Direct Observation of Transient Surface Species during Ge Nanowire Growth and Their Influence on Growth Stability," *Journal of the American Chemical Society*, vol. 137, pp. 9861–9869, 8 2015.

[293] S. Kral, C. Zeiner, M. Stöger-Pollach, E. Bertagnolli, M. I. Den Hertog, M. Lopez-Haro, E. Robin, K. El Hajraoui, and A. Lugstein, "Abrupt Schottky Junctions in Al/Ge Nanowire Heterostructures," *Nano Letters*, vol. 15, pp. 4783–4787, 7 2015.

[294] E. Sánchez-Sinencio and J. Silva-Martínez, "CMOS transconductance amplifiers, architectures and active filters: A tutorial," *IEEE Proceedings: Circuits, Devices and Systems*, vol. 147, no. 1, pp. 3–12, 2000.

[295] K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, "Past, Present and Future: SiGe and CMOS Transistor Scaling," *ECS Transactions*, vol. 33, p. 3, 10 2010.

[296] S. J. Park, D. Y. Jeon, V. Sessi, J. Trommer, A. Heinzig, T. Mikolajick, G. T. Kim, and W. M. Weber, "Channel Length-Dependent Operation of Ambipolar Schottky-Barrier Transistors on a Single Si Nanowire," *ACS Applied Materials and Interfaces*, vol. 12, pp. 43927–43932, 9 2020.

[297] M. S. Purewal, B. H. Hong, A. Ravi, B. Chandra, J. Hone, and P. Kim, "Scaling of resistance and electron mean free path of single-walled carbon nanotubes," *Physical Review Letters*, vol. 98, p. 186808, 5 2007.

[298] J. Svensson, A. A. Sourab, Y. Tarakanov, D. S. Lee, S. J. Park, S. J. Baek, Y. W. Park, and E. E. Campbell, "The dependence of the Schottky barrier height on carbon nanotube diameter for Pd-carbon nanotube contacts," *Nanotechnology*, vol. 20, p. 175204, 4 2009.

[299] J. Svensson and E. E. Campbell, "Schottky barriers in carbon nanotube-metal contacts," *Journal of Applied Physics*, vol. 110, p. 111101, 12 2011.

[300] D. Y. Jeon, T. Baldau, S. J. Park, S. Pregi, L. Baraban, G. Cuniberti, T. Mikolajick, and W. M. Weber, "In-depth electrical characterization of carrier transport in ambipolar Si-NW Schottky-barrier FETs," in *European Solid-State Device Research Conference*, pp. 304–307, IEEE, 9 2017.

[301] Y. Zhao, D. Candebat, C. Delker, Y. Zi, D. Janes, J. Appenzeller, and C. Yang, "Understanding the impact of Schottky barriers on the performance of narrow bandgap nanowire field effect transistors," *Nano Letters*, vol. 12, pp. 5331–5336, 10 2012.

[302] D. Sacchetto, Y. Leblebici, and G. De Micheli, "Ambipolar gate-controllable SiNW FETs for configurable logic circuits with improved expressive capability," *IEEE Electron Device Letters*, vol. 33, pp. 143–145, 2 2012.

[303] T. A. Krauss, F. Wessely, and U. Schwalke, "Novel Electrostatically Doped Planar Field-Effect Transistor for High Temperature Applications," *ECS Meeting Abstracts*, vol. MA2014-02, pp. 1895–1895, 4 2014.

[304] L. Yojo, R. C. Rangel, K. R. Sasaki, and J. A. Martino, "Reconfigurable back enhanced (BE) SOI MOSFET used to build a logic inverter," *SBMicro 2017 - 32nd Symposium on Microelectronics Technology and Devices: Chip on the Sands, co-located Symposia: 30th SBCCI - Circuits and Systems Design, 2nd INSCIT - Electronic Instrumentation, 7th WCAS - IC Design Cases and 17th SForum - Undergraduate*, pp. 1–4, 8 2017.

[305] G. Pridham, "Physics of Semiconductor Devices," *Electronics and Power*, vol. 16, no. 1, p. 34, 1970.

[306] L. Wind, A. Fuchsberger, O. Demirkiran, L. Vogl, P. Schweizer, X. Maeder, M. Sistani, and W. M. Weber, "Reconfigurable Si Field-Effect Transistors With Symmetric On-States Enabling Adaptive Complementary and Combinational Logic," *IEEE Transactions on Electron Devices*, vol. 71, no. 2, pp. 1302–1307, 2024.

[307] S. Rai, A. Rupani, P. Nath, and A. Kumar, "Hardware Watermarking Using Polymorphic Inverter Designs Based on Reconfigurable Nanotechnologies," in *Proceed-*

ings of IEEE Computer Society Annual Symposium on VLSI, ISVLSI, vol. 2019-July, pp. 663–669, IEEE Computer Society, 7 2019.

[308] T. Mikolajick, G. Galderisi, M. Simon, S. Rai, A. Kumar, A. Heinzig, W. M. Weber, and J. Trommer, "20 Years of reconfigurable field-effect transistors: From concepts to future applications," *Solid-State Electronics*, vol. 186, p. 108036, 12 2021.

[309] L. Wind, M. Maierhofer, A. Fuchsberger, M. Sistani, and W. M. Weber, "Realization of a Complementary Full Adder Based on Reconfigurable Transistors," *IEEE Electron Device Letters*, vol. 45, pp. 724–727, 4 2024.

[310] J. Trommer, A. Heinzig, S. Slesazeck, T. Mikolajick, and W. M. Weber, "Elementary aspects for circuit implementation of reconfigurable nanowire transistors," *IEEE Electron Device Letters*, vol. 35, pp. 141–143, 1 2014.

[311] M. Simon, J. Trommer, B. Liang, D. Fischer, T. Baldauf, M. B. Khan, A. Heinzig, M. Knaut, Y. M. Georgiev, A. Erbe, J. W. Bartha, T. Mikolaiick, and W. M. Weber, "A wired-AND transistor: Polarity controllable FET with multiple inputs," *Device Research Conference - Conference Digest, DRC*, vol. 2018-June, pp. 1–2, 8 2018.

[312] M. G. Bartmann, M. Sistani, N. Luhmann, S. Schmid, E. Bertagnolli, A. Lugstein, and J. Smoliner, "Germanium nanowire microbolometer," *Nanotechnology*, vol. 33, 3 2022.

[313] T. Akatsu, C. Deguet, L. Sanchez, F. Allibert, D. Rouchon, T. Signamarcheix, C. Richtarch, A. Boussagol, V. Loup, F. Mazen, J. M. Hartmann, Y. Campidelli, L. Clavelier, F. Letertre, N. Kernevez, and C. Mazure, "Germanium-on-insulator (GeOI) substrates - A novel engineered substrate for future high performance devices," *Materials Science in Semiconductor Processing*, vol. 9, pp. 444–448, 8 2006.

[314] M. Vinet, C. L. Royer, P. Batude, J. F. Damlencourt, J. M. Hartmann, L. Hutin, K. Romanjek, A. Pouydebasque, and O. Thomas, "Germanium on insulator and new 3D architectures opportunities for integration," *International Journal of Nanotechnology*, vol. 7, no. 4-8, pp. 304–319, 2010.

[315] A. E. Lange, E. Kreysa, S. E. McBride, P. L. Richards, and E. E. Haller, "Improved fabrication techniques for infrared bolometers," *International Journal of Infrared and Millimeter Waves*, vol. 4, pp. 689–706, 9 1983.

[316] C. N. Chen and J. S. Shie, "Fabrication of a sensitive germanium microbolometer for tympanic thermometry," *Sensors and Materials*, vol. 11, no. 6, pp. 369–382, 1999.

[317] A. Torres, A. Kosarev, M. L. García Cruz, and R. Ambrosio, "Uncooled microbolometer based on amorphous germanium film," *Journal of Non-Crystalline Solids*, vol. 329, pp. 179–183, 11 2003.

[318] W. M. Bullis, F. H. Brewer, C. D. Kolstad, and L. J. Swartzendruber, "Temperature coefficient of resistivity of silicon and germanium near room temperature," *Solid-State Electronics*, vol. 11, pp. 639–646, 7 1968.

[319] R. Jimenez, M. Moreno, A. Torres, A. Morales, A. Ponce, D. Ferrusca, J. Rangel-Magdaleno, J. Castro-Ramos, J. Hernandez-Perez, and E. Cano, "Fabrication of microbolometer arrays based on polymorphous silicon-germanium," *Sensors (Switzerland)*, vol. 20, p. 2716, 5 2020.

[320] F. J. Low, "Low-Temperature Germanium Bolometer," *Journal of the Optical Society of America*, vol. 51, no. 11, p. 1300, 1961.

[321] C. E. Jones, A. R. Hilton, J. B. Damrel, and C. C. Helms, "The Cooled Germanium Bolometer as a Far Infrared Detector," *Applied Optics*, vol. 4, p. 683, 6 1965.

[322] F. D. Shepherd and J. E. Murguia, "Application of Schottky barrier bolometer arrays to cooled sensors," in *Infrared Technology and Applications XXVI*, vol. 4130, p. 86, SPIE, 12 2000.

[323] V. A. Yuryev, K. V. Chizh, V. A. Chapnin, S. A. Mironov, V. P. Dubkov, O. V. Uvarov, V. P. Kalinushkin, V. M. Senkov, O. Y. Nalivaiko, A. G. Novikau, and P. I. Gaiduk, "Pt silicide/poly-Si Schottky diodes as temperature sensors for bolometers," *Journal of Applied Physics*, vol. 117, p. 204502, 5 2015.

[324] C. C. Wu and C. J. Lin, "Impurity-limited mobility of semiconducting thin wires in n-type gallium arsenide," *Journal of Applied Physics*, vol. 83, pp. 1390–1395, 2 1998.

[325] W. Wu, H. Wu, W. Sun, M. Si, N. Conrad, Y. Zhao, and P. D. Ye, "Mobility Fluctuation-Induced Low-Frequency Noise in Ultrascaled Ge Nanowire nMOSFETs with Near-Ballistic Transport," *IEEE Transactions on Electron Devices*, vol. 65, pp. 2573–2577, 6 2018.

[326] A. Vinod, P. Kumar, and B. Bhowmick, "Impact of ferroelectric on the electrical characteristics of silicon-germanium based heterojunction Schottky barrier FET," *AEU - International Journal of Electronics and Communications*, vol. 107, pp. 257–263, 7 2019.

[327] J. Wang, Q. Liu, R. Feng, H. Ye, X. Xu, R. Wang, T. Wang, and X. Wang, "In-Situ

Observation of Atomic Diffusion at Epitaxial Al-Si Interface," *physica status solidi (RRL)-Rapid Research Letters*, p. 2400175, 7 2024.

[328] G. E. Ponchak, "II. Metal-Semiconductor Junctions," in *GaAs MMIC Reliability Assurance Guideline for Space Applications*, vol. 24, 1996.

[329] G. Galderisi, T. Mikolajick, and J. Trommer, "Reliability of Reconfigurable Field Effect Transistors: Early Analysis of Bias Temperature Instability," *2024 IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, pp. 1–7, 7 2024.

[330] T. Morimoto, T. Ohguro, H. S. Momose, T. Iinuma, I. Kunishima, K. Suguro, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, and H. Iwai, "Self-Aligned Nickel-Mono-Silicide Technology for High-Speed Deep Submicrometer Logic CMOS ULSI," *IEEE Transactions on Electron Devices*, vol. 42, pp. 915–922, 5 1995.

[331] L. Wind, A. Fuchsberger, O. Demirkiran, L. Vogl, P. Schweizer, X. Maeder, M. Sistani, and W. M. Weber, "Reconfigurable Si Field-Effect Transistors With Symmetric On-States Enabling Adaptive Complementary and Combinational Logic," *IEEE Transactions on Electron Devices*, vol. 71, no. 2, pp. 1302–1307, 2024.

[332] A. Fuchsberger, L. Wind, M. Sistani, R. Behrle, D. Nazzari, J. Aberl, E. Prado Navarrete, L. Vukusic, M. Brehm, P. Schweizer, L. Vogl, X. Maeder, and W. M. Weber, "Reconfigurable Field-Effect Transistor Technology via Heterogeneous Integration of SiGe with Crystalline Al Contacts," *Advanced Electronic Materials*, vol. 9, no. 6, p. 2201259, 2023.

[333] A. Fuchsberger, L. Wind, D. Nazzari, L. Kuhberger, D. Popp, J. Aberl, E. P. Navarrete, M. Brehm, L. Vogl, P. Schweizer, S. Lellig, X. Maeder, M. Sistani, and W. M. Weber, "A Run-Time Reconfigurable Ge Field-Effect Transistor with Symmetric On-States," *IEEE Journal of the Electron Devices Society*, vol. 12, pp. 83–87, 2024.

[334] A. Fuchsberger, L. Wind, D. Nazzari, A. Dobler, J. Aberl, E. P. Navarrete, M. Brehm, L. Vogl, P. Schweizer, S. Lellig, X. Maeder, M. Sistani, and W. M. Weber, "A Reconfigurable Ge Transistor Functionally Diversified by Negative Differential Resistance," *IEEE Journal of the Electron Devices Society*, 2024.

[335] D. K. Ferry, S. M. Goodnick, and J. Bird, *Transport in Nanostructures*. Cambridge University Press, 2009.

[336] C. Durkan and M. Welland, "Size effects in the electrical resistivity of polycrystalline nanowires," *Physical Review B*, vol. 61, p. 14215, 5 2000.

[337] O. Wunnicke, "Gate capacitance of back-gated nanowire field-effect transistors," *Applied Physics Letters*, vol. 89, p. 83102, 8 2006.

List of Publications

[RB1] R. Behrle, A. U. Pacheco-Sánchez, S. Barth, W. M. Weber, and M. Sistani, "Thermionic Injection Assessment in Germanium Nanowire Schottky Junction FETs by Means of 1D and 3D Extraction Methods," *Applied Physics Letters*, 2024.

[RB2] L. Wind, R. Böckle, M. Sistani, P. Schweizer, X. Maeder, J. Michler, C. G. Murphey, J. Cahoon, and W. M. Weber, "Monolithic and Single-Crystalline Aluminum-Silicon Heterostructures," *ACS Applied Materials and Interfaces*, vol. 14, pp. 26238–26244, 6 2022.

[RB3] R. Behrle, C. G. Murphey, J. F. Cahoon, S. Barth, M. I. den Hertog, W. M. Weber, and M. Sistani, "Understanding the Electronic Transport of Al-Si and Al-Ge Nanojunctions by Exploiting Temperature-Dependent Bias Spectroscopy," *ACS Applied Materials and Interfaces*, vol. 16, pp. 19350–19358, 4 2024.

[RB4] R. Behrle, M. Bažiková, S. Barth, W. M. Weber, and M. Sistani, "Mapping Electronic Transport in Ge Nanowire SBFETs: From Tunneling to NDR," in *2023 IEEE Nanotechnology Materials and Devices Conference, NMDC 2023*, pp. 889–894, IEEE, 10 2023.

[RB5] R. Böckle, M. Sistani, M. Bažíková, L. Wind, Z. Sadre-Momtaz, M. I. den Hertog, C. G. Murphey, J. F. Cahoon, and W. M. Weber, "Reconfigurable Complementary and Combinational Logic Based on Monolithic and Single-Crystalline Al-Si Heterostructures," *Advanced Electronic Materials*, vol. 9, no. 1, p. 2200567, 2023.

[RB6] L. Wind, R. Behrle, M. I. den Hertog, C. G. Murphey, J. F. Cahoon, M. Sistani, and W. M. Weber, "Nanoscale Reconfigurable Si Transistors: From Wires to Sheets and Unto Multi-Wire Channels," *Advanced Electronic Materials*, vol. 10, p. 2300483, 2 2024.

[RB7] R. Behrle, M. I. Den Hertog, A. Lugstein, W. M. Weber, and M. Sistani, "Bias Spectroscopy of Negative Differential Resistance in Ge Nanowire Cascode Circuits," in *European Solid-State Device Research Conference*, vol. 2023-Septe, (Lisbon), pp. 37–40, 9 2023.

[RB8] R. Behrle, J. Smoliner, L. Wind, D. Nazzari, A. Lugstein, W. M. Weber, and M. Sistani, "Bias-tunable temperature coefficient of resistance in Ge transistors," *Applied Physics Letters*, vol. 124, no. 9, 2024.

[RB9] R. Behrle, M. Bažiková, S. Barth, W. M. Weber, and M. Sistani, "Mapping Electronic Transport in Ge Nanowire SBFETs: From Tunneling to NDR," in *2023 IEEE Nanotechnology Materials and Devices Conference, NMDC 2023*, pp. 889–894, IEEE, 10 2023.

[RB10] R. Behrle, V. Krause, M. S. Seifner, B. Köstler, K. A. Dick, M. Wagner, M. Sistani, and S. Barth, "Electrical and Structural Properties of Si1-xGex Nanowires Prepared from a Single-Source Precursor," *Nanomaterials*, vol. 13, p. 627, 2 2023.

[RB11] R. Behrle, M. Sistani, A. Lugstein, Z. Sadre Momtaz, M. I. Den Hertog, D. Pogany, and W. M. Weber, "Low-frequency noise in quasi-ballistic monolithic Al-Ge-Al nanowire field effect transistors," *Applied Physics Letters*, vol. 122, p. 243504, 6 2023.

Dipl.-Ing. Raphael Behrle

formerly Raphael Böckle

Updated October 13, 2024

Email: raphael.behrle@gmail.com
Address: Dorfstraße 33, 6800 Feldkirch, Austria
Phone: +43 664 405 70 27
Citizenship: Austrian

Research interests

Group IV nanowire electronics, Schottky barrier field-effect transistors, Negative differential resistance in Ge nanodevices, Reconfigurable electronics, Bias spectroscopy

Education

TU Wien — Vienna, Austria
PhD in Emerging Nanoelectronic Devices — 09/2021 – Present
Advisors: Prof. Dr. Walter M. Weber and Dr. Masiar Sistani

TU Wien — Vienna, Austria
MA in Microelectronics and Photonics — 10/2018 – 07/2021
Advisors: Prof. Dr. Walter M. Weber and Dr. Masiar Sistani

University of Applied Sciences Technikum Wien — Vienna, Austria
BA in Electronics and Business (Distance Study) — 09/2015 – 06/2018

Honors

Young Scientist Award (20th GADEST)	2024
Best Student Paper Award (IEEE NMDC)	2023
Best Poster Award (Nanowire Week)	2023
Young Researcher Award (EMRS Spring Meeting)	2023

Research experience

Emerging Nanoelectronic Devices, Institute of Solid State Electronics, TU Wien
Mentor: Prof. Dr. Walter M. Weber — 07/2020 – 09/2024
Mr. Behrle's research focus lies on the integration of group IV nanowires into Schottky barrier field-effect transistors. Thus, in-depth investigations of the charge carrier transport of the underlying material systems and device architectures allow to extract detailed operation and transport regimes. Further, allowing the realization of emerging nanoelectronic devices, such as reconfigurable field-effect transistors or devices with negative differential resistance.

Publications

Thermionic Injection Assessment in Germanium Nanowire Schottky Junction FETs by Means of 1D and 3D Extraction Methods
Raphael Behrle, Aníbal Pacheco-Sanchez, Sven Barth, et al.
Applied Physics Letters, ***in review***.

Understanding the Electronic Transport of Al-Si and Al-Ge Nanojunctions by Exploiting Temperature-Dependent Bias Spectroscopy
Raphael Behrle, Corban G. E. Murphey, James F. Cahoon, et al.
ACS Applied Materials & Interfaces, 2024.

Bias-tunable temperature coefficient of resistance in Ge transistors
Raphael Behrle, Jürgen Smoliner, Lukas Wind, et al.
Applied Physics Letters, 2024.

Mapping Electronic Transport in Ge Nanowire SBFETs: From Tunneling to NDR
Raphael Behrle, Martina Bažíková, Sven Barth, et al.
IEEE Proceedings NMDC, 2023.

Bias Spectroscopy of Negative Differential Resistance in Ge Nanowire Cascode Circuits
Raphael Behrle, Martien I. den Hertog, Alois Lugstein, et al.
IEEE Proceedings ESSDERC, 2023.

Nanoscale Reconfigurable Si Transistors: From Wires to Sheets and Unto Multi-Wire Channels
Lukas Wind, Raphael Behrle, Martien I. den Hertog, et al.
Advanced Electronic Materials, 2023.

Low-frequency noise in quasi-ballistic monolithic Al-Ge-Al nanowire field effect transistors
Raphael Behrle, Masiar Sistani, Alois Lugstein, et al.
Applied Physics Letters, 2023.

Reconfigurable Field-Effect Transistor Technology via Heterogeneous Integration of SiGe with Crystalline Al Contacts
Andreas Fuchsberger, Lukas Wind, ..., Raphael Behrle, et al.
Advanced Electronic Materials, 2023.

Electrical and Structural Properties of $Si_{1-x}Ge_x$ Nanowires Prepared from a Single-Source Precursor
Raphael Behrle, Vanessa Krause, Michael S. Seifner, et al.
MDPI Nanomaterials, 2023.

Reconfigurable Complementary and Combinational Logic Based on Monolithic and Single-Crystalline Al-Si Heterostructures
Raphael Böckle, Masiar Sistani, Martina Bažíková, et al.
Advanced Electronic Materials, 2022.

Composition Dependent Electrical Transport in $Si_{1-x}Ge_x$ Nanosheets with Monolithic Single-Elementary Al Contacts
Lukas Wind, Masiar Sistani, Raphael Böckle, et al.
Small, 2022.

Monolithic and Single-Crystalline Aluminum-Silicon Heterostructures
Lukas Wind, Raphael Böckle, Masiar Sistani, et al.
ACS Applied Materials & Interfaces, 2022.

Reconfigurable Field Effect Transistors: A Technology Enablers Perspective
Thomas Mikolajick, Giulio Galderisi, ..., Raphael Böckle, et al.
Solid-State Electronics, 2022.

A Top-Down Platform Enabling Ge Based Reconfigurable Transistors
Raphael Böckle, Masiar Sistani, Boris Lipovec, et al.
Advanced Materials Technologies, 2021.

Bias-Switchable Photoconductance in a Nanoscale Ge Photodetector Operated in the Negative Differential Resistance Regime
Masiar Sistani, Raphael Böckle, Maximilian G. Bartmann, et al.
ACS Photonics, 2021.

Nanometer-Scale Ge-Based Adaptable Transistors Providing Programmable Negative Differential Resistance Enabling Multivalued Logic
Masiar Sistani, Raphael Böckle, David Falkensteiner, et al.
ACS Nano, 2021.

Polycrystalline Ge Nanosheets Embedded in Metal-Semiconductor Heterostructures Enabling Wafer-Scale 3D Integration of Ge Nanodevices with Self-Aligned Al Contacts
Masiar Sistani, Raphael Böckle, Lukas Wind, et al.
Advanced Electronic Materials, 2021.

Gate-Tunable Negative Differential Resistance in Next-Generation Ge Nanodevices and their Performance Metrics
Raphael Böckle, Masiar Sistani, Kilian Eysin, et al.
Advanced Electronic Materials, 2021.

Ge quantum wire memristor
Raphael Böckle, Masiar Sistani, Philipp Staudinger, et al.
IOP Nanotechnology, 2020.

Talks and posters

Comparative Study of Charge Carrier Transport in Al-Si and Al-Ge Nanowire Heterostructure Transistors
September 2024
Talk at 20th GADEST (Bad Schandau, Germany)

Mapping Electronic Transport in Ge Nanowire SBFETs: From Tunneling to NDR
October 2023
Talk at IEEE NMDC 2023 (Paestum, Italy)

Bias Spectroscopy of Negative Differential Resistance in Ge Nanowire Field Effect Transistors
October 2023
Talk at Nanowire Week 2023 (Atlanta, United States)

Comparison and Analysis of Charge Carrier Transport in Al-Si/Ge Nanowire Heterostructure Field-Effect Transistors
October 2023
Poster at Nanowire Week 2023 (Atlanta, United States)

Bias Spectroscopy of Negative Differential Resistance in Ge Nanowire Cascode Circuits
September 2023
Talk at IEEE ESSDERC/ESSCIRC 2023 (Lisbon, Portugal)

Electrical Transport in Monolithic Al-Si/Al-Ge Heterojunction based Nanowire Schottky Barrier Field-Effect Transistors
September 2023
Highlight Lecture at EUROMAT 2023 (Frankfurt am Main, Germany)

Reconfigurable Silicon Transistors with Single-Elementary Metal Contacts for Complementary and Combinational Logic
May 2023
Talk at EMRS 2023 Spring Meeting (Strasbourg, France)

Reconfigurable Complementary and Combinational Logic based on Monolithic and Single-Crystalline Al-Si Heterostructures
September 2022
Talk at DPG 2022 (Regensburg, Germany)

Low-frequency Noise in Room-temperature quasi-ballistic Ge NW Transistors
April 2022
Poster at Nanowire Week 2022 (Chamonix, France)

Bias-Switchable Photoconductance in a Nanoscale Ge Photodetector Operated in the Negative Differential Resistance Regime
April 2022
Poster at Nanowire Week 2022 (Chamonix, France)

Top-down Fabricated Ge-based Reconfigurable FETs
September 2021
Talk at EUROMAT 2021 (Online)

Industry experience

Tridonic Technology and Innovation — Dornbirn, Austria
Head of Digital Engineering — July 2024 –
Management of advanced modeling and simulation services, as well as responsible for the lifetime management program covering LED systems, including drivers, modules, and batteries for emergency lighting systems.

Tridonic Research and Development — Dornbirn, Austria
Design Engineer — November 2013 – September 2018
Design and product support (hardware change management) of LED drivers as well as electronic component (passive and active) qualification and assessment.

Extracurricular

TU Wien Space Team — October 2018 – March 2024
Development of LoRa ground station network
Initiator and project leader of CubeSat mission ”SpaceTeamSat1”

Raphael Behrle — Date