Highly sensitive 10 Gb/s PAM-4 optical receiver circuit for three-dimensional optoelectronic integration

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Abstract: This study presents a 0.35 µm silicon germanium bipolar complementary metal-oxide-semiconductor 10 Gb/s receiver circuit optimised for photonic–electronic three-dimensional integration. Measurements were conducted on a test-chip with a voltage-input signal, which was converted to a current via a series resistor. On the basis of measurement results and using the expected value of the photodetector responsivity of 1 A/W, the PAM-4 circuit consumes 145 mW, sensitivity is −21.8 dBm at 10 Gb/s, and at a bit error rate = 10^{-9}.

1 Introduction

It is not feasible to fabricate high-speed optical detectors operating at standard 1.3 and 1.55 µm communication wavelengths in silicon (Si) alone. Instead, such optoelectronic integrated circuits (OEICs) can be produced using, for example, indium phosphide-based technology, but fabrication of such monolithically integrated circuits is sometimes too expensive for a given application. As another possibility, photonic components can be produced on a dedicated substrate, while electronics is fabricated on Si. That is the cost-effective way in which circuits' performance also can be optimised independently. However, the question of connecting the photonic devices and the electronic circuits then arises. The circuits can be connected by means of wire bonding, which imposes parasitic inductance of the bond wire and the rather large parasitic capacitances of the two additional bond pads, which degrade the bandwidth (BW) and noise performance. Another possibility is to stack the photonic and electronic wafers one on top of the other and to connect them by means of small structures resembling vias in a so-called three-dimensional (3D) integration, such that the parasitics are minimised.

This work will present the receiver (RX) circuit designed for such a 3D optoelectronic co-integration. The measurements were performed on a test-chip with electrical input. The circuit uses a pulse amplitude modulation format with four distinct levels (PAM-4, sometimes also called 4-PAM), which allows for the symbol rate to be halved compared with the bit-rate. The presented RX operates at 10 Gb/s, while the symbol rate equals 5 Gbaud. This allows the design of the circuits with relaxed BW requirements, but with somewhat worst signal-to-noise ratio compared with the simple binary modulation.

2 3D-integration

Fig. 1 shows the cross-section of a 3D-integrated OEIC. 3D-integration allows for the RX circuitry to be optimised independently of the photodetector, which is produced in a dedicated technology, while keeping the parasitics at a much lower value than in conventional wire-bonded optical RXs. The lateral germanium (Ge) waveguide PIN photodetector is expected to have a junction capacitance of about 4 fF, while the total capacitance of the interconnection structures (C_{Minipad} and C_{IWC} in parallel) is expected to be about 15 fF. That is a large decrease in parasitics, compared with the conventional external photodetectors whose capacitances are in the order of 200 fF. The 3D-integrated OEIC avoids ∼150 fF bond-pad capacitances and about 1 nH parasitic inductance at the input of the circuit, which would be unavoidable if a wire-bonded photodetector was used.

Fig. 2*a* depicts the block diagram of the RX circuit. RX is built by an input transimpedance amplifier (TIA) shown in detail in Fig. 2*b*, a linear post-amplifying stage and a 50 Ω output buffer. An operational amplifier in an integrating topology together with a dummy TIA comprises an offset compensation network and converts the single-ended photocurrent input into a differential signal at the output of the circuit. The differential topology secures good rejection of common-mode disturbances, minimises temperature effects, provides immunity to process tolerances and doubles the output voltage swing. The dummy TIA has the same topology and component values as the TIA, except for the added Miller capacitor between base and collector of its input transistor, used for BW decrease and thus noise reduction. The TIA consists of a common-emitter stage built by T_1 and R_C, two emitter-followers $T_2 - T_{i2}$ and $T_3 - T_{i3}$, and the feedback network comprised of R_{fb} and C_{fb}, whereas R_{ref} and T_{ref} are auxiliary elements which provide the bias voltage for emitter-followers' current sources. The feedback loop is closed from the second emitter-follower. That way the input of the TIA is somewhat isolated from the input of the post-amplifier and an appropriate DC voltage is provided for the post-amplifier by the first emitter-follower.

The input referred noise current of the circuit in Fig. 2*b* can be expressed as [1]

$$I_n^2(f) = \frac{4k_{\text{B}}T}{R_{\text{fb}}} + \frac{2qI_{\text{C1}}}{\beta_1} + 2qI_{\text{C1}} \cdot \frac{\left(2\pi C_{\text{T}}\right)^2}{g_{m1}^2} \cdot f^2 + 4k_{\text{B}}TR_{\text{b1}} \cdot \left(2\pi C_{\text{T}}\right)^2 \cdot f^2, \quad (1)$$

where $C_{\text{T}} = 303$ fF is the total capacitance at the input node including photodetector's, connection's, and input transistor's contributions, R_{b1} is the base resistance of T_1, and the other quantities are shown in Fig. 2*b*. It can be observed that the dominant noise sources are proportional to C_{T}^2 and thus it is essential to decrease the input capacitance as much as possible, which is fulfilled by employing 3D-integration.

3 Measurement setup

A purely electrical test-chip was fabricated and characterised. Purely electrical characterisation is a common way of testing the optical RX circuits. For example, in [2], the optical RX circuit was tested by probing the electrical signals on the input pads, and

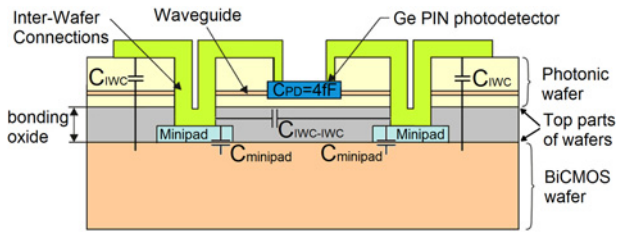

Fig. 1 *Cross-section of 3D-integrated OEIC*

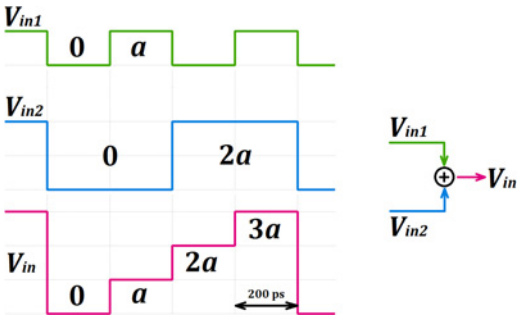

Fig. 3 *Conceptual way of generating input PAM-4 voltage, with unity amplitude a indicated on the waveforms*

the photodiode capacitance was emulated by a combination of 70 fF bond-pad capacitance and an additional 150 fF on-chip metal capacitor. The optical RX circuit from [3] was tested by wafer probing without additional capacitances, which emulate attached photodetector (PD). The performance with supposed PD was extrapolated from *S*-parameter measurements performed on the circuit without the photodetector attached.

The configuration of the circuit measured in this work is shown in Fig. 2*a*, with an AC-coupled on-chip resistor at the input. The role of the resistor is to convert the 5 Gbaud (10 Gb/s) PAM-4 voltage signal at the input of the circuit into a PAM-4 current signal, as if an equivalent photodetector was connected at the input. The parasitic capacitance of this resistor and interconnections, denoted C_{par}. in Fig. 2*a*, correspond to the expected capacitance of the 3D-integrated PD.

PAM-4 input signal was generated using two SYMPULS bit-pattern generators. The sum of these two binary signals results in the PAM-4 signal applied to the input of the circuit. This is conceptually shown in Fig. 3.

The symbol error rate was determined according to the formula [4, 5]

$$\text{SER} = \frac{3}{2} Q\left(\sqrt{\frac{4E_{\text{B}}}{5N_O}}\right), \tag{2}$$

where E_{B} is the average bit energy and $N_O = 2\sigma^2$ is the noise power spectral density [1]. Both of these quantities were calculated in MATLAB from the measured eye-diagrams. The Q-function is defined as $Q(x) = 0.5\ \text{erfc}(x/\sqrt{2})$. If the Gray code is employed and errors are occurring when an adjacent symbol is received instead of the correct one, which are both reasonable assumptions, then the bit error rate (BER) can be calculated as follows:

$$\text{BER} = \frac{\text{SER}}{2} = \frac{3}{4} Q\left(\sqrt{\frac{4E_{\text{B}}}{5N_O}}\right). \tag{3}$$

4 Results and comparison

Fig. 4 depicts the measured PAM-4 eye-diagrams at 10 Gb/s at the input as well as the output of the circuit. Fig. 5 shows the frequency transfer characteristic obtained with a Rohde & Schwarz ZVM Vector Network Analyzer, and the BER curve. The PAM-4 sensitivity at 10 Gb/s with BER = 10^{-9} is –21.8 dBm, under the assumption of an infinite extinction ratio and a photodetector responsivity of 1 A/W. The measured transimpedance amplification equals 95 dBΩ. The simulated –3 dB BW of the circuit is 3.6 GHz, whereas in the measurements it amounts to 5.6 GHz. The reason for this BW increase can be observed in Fig. 4*b* as a small peaking caused by printed circuit board (PCB) parasitics, which negatively affect the noise performance.

Table 1 shows the comparison of the designed circuit with the reported state-of-the-art broadband optical RXs. Circuits from [6] to [9] are 3D-integrated optical RXs and all of these operate with binary modulation, which means they are less sensitive to noise than PAM-4 RXs. Discussion on sensitivities of these RXs will be presented later in this section.

References [10–14] report on PAM-4 optical RXs. Circuits [10, 11] are designed for wire-bonded PDs and their post-layout simulation results are presented. They operate at 56 and 40 Gb/s, respectively. Sensitivities of both of those circuits are estimated based on the reported input referred noise currents and on the assumptions of a photodetector with unity responsivity and BER equal to 10^{-9}. References [12, 13] present bipolar complementary metal-oxide-semiconductor (BiCMOS) PAM-4 optical RXs with wire-bonded and monolithically integrated photodiode, respectively. RX from [12] operates at 64 Gb/s and shows –3 dBm sensitivity and 0.44 A/W responsivity of the used PD, and at a BER of 10^{-3}, which was enough for employed forward error correction mechanism. The PAM-4 optical RX from [13] had a measured –16 dBm sensitivity, which is a good value considering that responsivity of its photodetector was only 0.51 A/W. The circuit from [14] is an

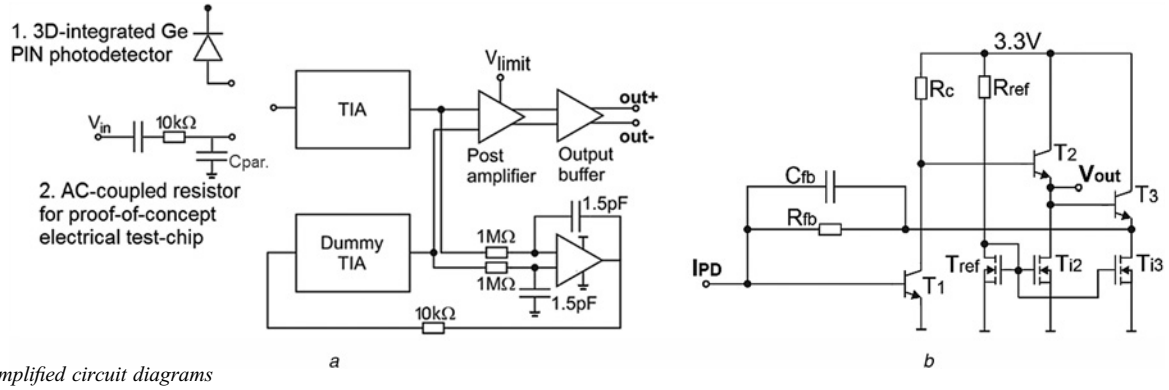

Fig. 2 *Simplified circuit diagrams*
a RX block diagram
b TIA schematic representation

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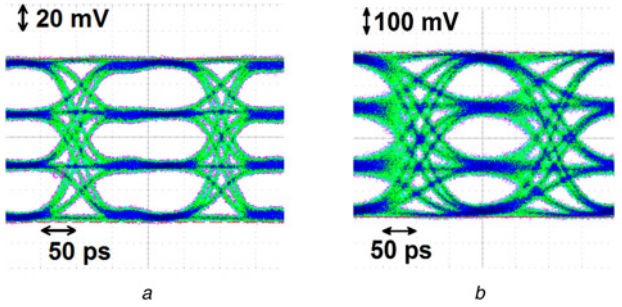

Fig. 4 *PAM-4 eye-diagrams*
a Input
b Differential output

optical RX for 3D-integrated OEICs designed in the same technology as the RX presented in this paper. These two circuits show nearly the same sensitivity. As mentioned in the explanation of Fig. 5*a*, the sensitivity of the presented RX is degraded because of the BW increase compared with simulations, caused by various PCB parasitics. According to the simulation results of the RX its sensitivity would be –24 dBm, so a redesign of the PCB could possibly improve the sensitivity by 2 dB. The area of the circuit presented in this paper equals 0.574 mm^2, whereas the RX from [14] occupies 0.632 mm^2, which is a considerable difference of nearly 10%. The RX from [14] has the largest power consumption of all circuits in Table 1.

According to Säckinger [1], the sensitivity of the broadband optical RX degrades between 10 and 15 dB per each decade of the bit-rate increase, where 10 dB rate corresponds to the extreme case in which the photodetector's noise dominates. Since the photodetector does not contribute to the majority of the noise for a PIN-RX front-end, which is especially the case for 3D-integrated PIN-RXs, it should be assumed that the sensitivity degradation rate in this case is larger than 10 dB per decade. To provide a more in-depth comparison of the sensitivity performance, Fig. 6 shows the sensitivities of PAM-4 optical RXs from Table 1. Fig. 6 also plots the lines with 10 and 15 dB slopes (per decade), both originating at the point which represents our circuit's sensitivity. As can be observed, sensitivities of all PAM-4 circuits are located above the 10 dB per decade line, and RXs from [10, 11]

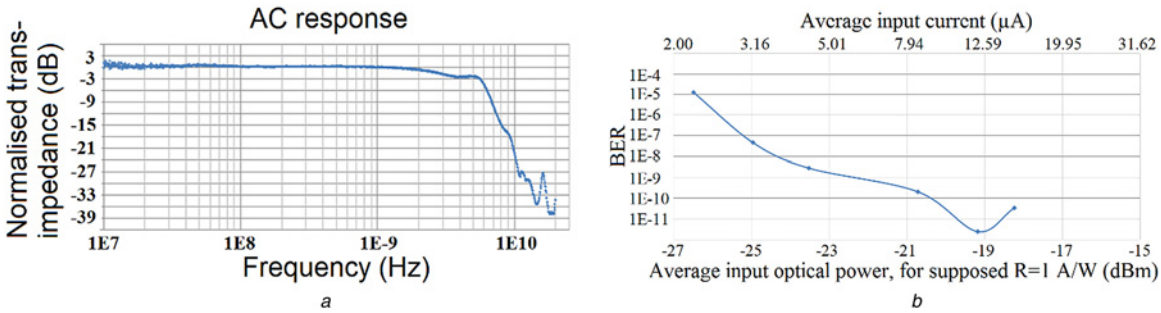

Fig. 5 *Measurement results*
a Transfer AC characteristic
b BER curve

Table 1 Comparison with state-of-the-art optical RXs

Reference	Technology	Data-rate, Gb/s	Sensitivity, responsivity, BER	Power consumption	Chip area	Type
[6] JLT'16	28 nm CMOS	25	–14.9 dBm, $R = 0.2$ A/W, BER = 10^{-12}	4.3 mW (0.17 pJ/bit)	0.0018 mm^2 (active area)	3D-integrated binary optical RXs
[7] ESSCIRC'14	65 nm CMOS	28	–11.5 dBm, $R = 0.88$ A/W, BER = 10^{-12}	86 mW (3.7 pJ/bit)	2 mm^2	
[8] ESSCIRC'15	65 nm CMOS	7	–14.5 dBm, $R = 0.73$ A/W, BER = 10^{-10}	2.38 mW (0.34 pJ/bit)	0.0025 mm^2 (active area)	
[9][a] SPIE'10	0.35 μm BiCMOS	10	–23.1 dBm, $R = 0.5$ A/W, BER = 10^{-9}	175 mW (17.5 pJ/bit)	0.702 mm^2	
[10][a] MWCAS'15	FinFET	56	estimated –12.9 dBm, if $R = 1$ A/W, BER = 10^{-9}	6.3 mW (0.11 pJ/bit)	0.015 mm^2 (active area)	PAM-4 wire-bonded optical RXs
[11][a] ISCAS'14	28 nm CMOS	40	estimated –13.5 dBm, if $R = 1$ A/W, BER = 10^{-9}	56 mW (1.4 pJ/bit)	0.018 mm^2 (active area) total 0.5 mm^2	
[12] ISCAS'15	130 nm SiGe BiCMOS	64	–3 dBm, $R = 0.44$ A/W, BER = 10^{-3}	165 mW (2.578 pJ/bit)	0.99 mm^2 per channel	
[13] ICM'10	0.6 μm BiCMOS	2.5	–16 dBm, $R = 0.52$ A/W, BER = 10^{-9}	100 mW (40 pJ/bit)	1 mm^2	PAM-4 monolithically integrated optical RX
[14][b] JSTQE'16	0.35 μm SiGe BiCMOS	10	–21.7 dBm, $R = 0.9$ A/W, BER = 10^{-9}	188 mW (18.8 pJ/bit)	0.632 mm^2	PAM-4 3D-integrated optical RXs
this work[b]	0.35 μm BiCMOS	10	–21.8 dBm, $R = 1$ A/W, BER = 10^{-9}	145 mW (14.5 pJ/bit)	0.574 mm^2	

[a]Post-layout simulation results
[b]Measured on an electrical input test-chip with assumed photodetector's responsivity

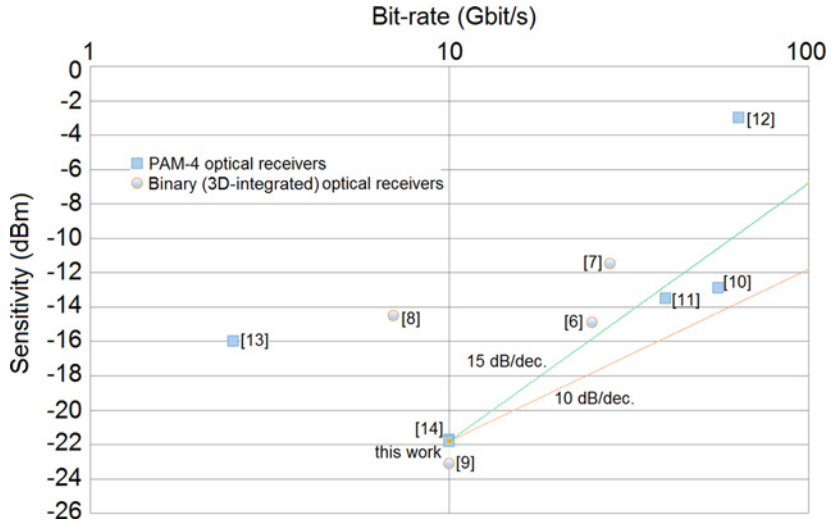

Fig. 6 *Sensitivity comparison of the optical RXs from Table 1*

are the only ones below the line with the slope of 15 dB per decade of the bit-rate increase. However, those values are estimated based on the reported post-layout results.

The minimum theoretical difference in sensitivities of PAM-4 and binary RXs is ~4.8 dB, for the same value of input referred noise current and the same value of BER. Therefore, our circuit shows good sensitivity compared with presented 3D-integrated binary RXs. The optical RX from [9] has a 1.8 dB better sensitivity than our circuit. The other 3D-integrated binary circuits [6–8] have the sensitivities above both lines in Fig. 6. It should be noted, however, that the RX from [6] employed a photodetector with a responsivity of only 0.2 A/W, whereas 3D-integrated optical RXs from [7, 8] had PDs with relatively good responsivities of 0.88 and 0.73 A/W, respectively. All of the presented nanometre-scale CMOS RXs have a much lower-power consumption than our circuit.

5 Conclusion

This paper presents a 0.35 µm BiCMOS circuit for 3D-integrated 10 Gb/s optical RX. The circuit employs PAM-4 modulation in order to relax the BW requirements. It is shown that 3D optoelectronic integration can enable a design of highly sensitive RXs, due to the miniature parasitics at the input node, and at the same time allowing photodetectors to be optimised in a dedicated technology. Comparison of the sensitivity with state-of-the-art PAM-4 as well as 3D-integrated binary optical RXs is performed; presented BiCMOS circuit has a better sensitivity than nanometre-scale CMOS binary RXs, but at the cost of a worst power consumption. The results were experimentally verified on a test-chip with electrical input.

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