Implementation of Negative Differential Resistance-Based Circuits in Multigate Ge Transistors

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***Abstract*— The co-integration of negative differential resistance (NDR) and Si-based CMOS technology might be a promising concept for multimode devices and circuits with enhanced performance and functionality. Here, we report on Ge-based multigate Schottky barrier field-effect transistors (SBFETs) operated in an NDR mode. A detailed and systematic study of the influence of electrostatic gating in single transistors as well as cascode circuits is carried out. We experimentally demonstrate that a single multigate SBFET can replace a cascode circuit of individual NDR devices. The realized devices and circuits contribute to compact logic gates and memory devices based on NDR complementing conventional CMOS technology.**

***Index Terms*— Adaptive electronics, cascode circuit, germanium, multigate transistor, negative differential resistance (NDR).**

I. Introduction

With an ever-increasing demand for performance, computational systems are believed to be advanced toward functional diverse adaptability to enable emerging self-learning electronic paradigms. This would leverage circuit performance beyond the limits encountered in miniaturization. In this regard, confined Ge plays a vital role due to its conduction band (CB) landscape, which supports the electron transfer effect between neighboring valleys, resulting in negative differential resistance (NDR) [1], [2]. However, the investigation of NDR in group-IV semiconductors was in the past restricted to operation at cryogenic temperatures [3] or bottom–up nanowires [4], [5] and was compromised by transient effects attributed to interface traps [6], [7]. Despite that, motivated by conceptually, new multivalue logic (MVL) devices based on cascoded NDR devices, creating a staircase of holding states, [8] faster and more compact logic circuits were conceived. Additionally, the self-latching action of cascoded NDR devices is highly relevant for emerging compact logic gates and memory devices [9]. The basic building block for such applications is the MOBILE latch [7], which is based on two identical NDR devices. To harness the advantages of NDR, co-integration of conventional combinational logic with NDR elements is a rewarding concept to investigate [9], targeting, e.g., multimode circuits with enhanced performance and added functionality beyond the capabilities of CMOS.

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II. Device Platform

The technological platform of the proposed Ge-based Schottky barrier field-effect transistors (SBFETs) is based on the integration of an ultrathin Ge layer on a Si-on-insulator (SOI) by ultralow-temperature molecular beam epitaxy [10], bypassing Ge on insulator (GeOI) processing issues and providing a low-cost alternative to GeOI platforms [11]. As indicated for the SBFET in Fig. 1(a), the contact formation relies on a thermally induced exchange reaction [10], where a nanoscale single-crystalline Al contact is established. Importantly, Al–Si–Ge multiheterojunctions with an ultrathin Si layer between the Al contact and the Ge channel are formed. This allows stable operability and processability in CMOS-compatible processes, as Ge is completely encapsulated by Si and is not in direct contact with Al. The associated Ge on SOI (GeSOI) platform is illustrated as stack in Fig. 1(b), with a SiO_2/ZrO_2 gate dielectric stack. The thick SiO_2 interlayer offers a low interface trap density reducing border trap effects as well as trapping into the high-k dielectric despite the high gate fields applied [10].

III. Negative Differential Resistance

The multi-valley CB landscape of Ge is assumed to be the origin of the demonstrated NDR effect in the proposed SBFET devices. In particular, the transferred electron effect [1], [2], where L-valley electrons are accelerated and consequently scattered into a higher CB minimum (X-valley) exhibiting

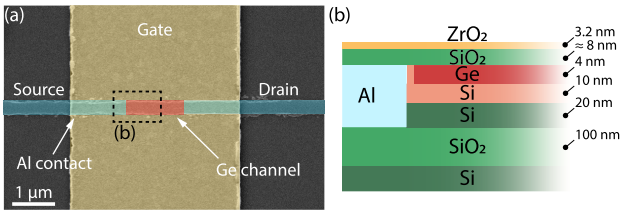

Fig. 1. (a) SEM image of NDR-mode SBFET. (b) Schematic illustration of the fabricated GeSOI nanosheet structure.

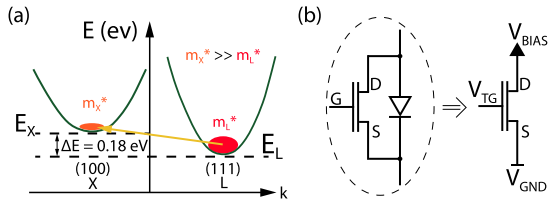

Fig. 2. (a) Sketch of the CB landscape of Ge enabling NDR by electron transfer from the L- to the X-valley. (b) Equivalent circuit of the controllable NDR-mode SBFET comprising a FET with an NDR diode in parallel, with source (S), drain (D), and gate (G) indicated.

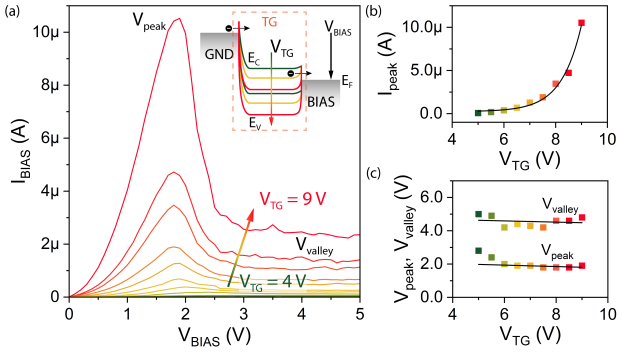

Fig. 3. (a) *I*/*V* characteristic and respective schematic band diagram of the GeSOI SBFET. (b) Exponential fit of the NDR peak current as a function of the gate voltage. (c) Gate-voltage dependence of the peak and valley positions.

higher effective electron mass and therefore resulting in a lower conductivity and ultimately into an NDR [9], as shown in Fig. 2(a). Furthermore, as it will be shown, this NDR behavior can be controlled by electrostatic gating so that the proposed structure can be interpreted as an NDR device controlled by a transistor, which combines two functionalities into a single device [see Fig. 2(b)]. At present, such NDR devices are commonly fabricated from complex III–V semiconductor stacks [9] that are complex, extensive in chip area, and expensive to co-integrate with Si-CMOS platforms.

Taking the acceleration of electrons into consideration, it is evident that a sufficiently high bias (electric field) has to be applied to allow those charge carriers to populate the X-valley. As shown below, a high gate voltage V_{TG} is required to thin the effective Schottky barrier, which results in a more efficient injection of electrons by a combination of tunneling and thermionic emission. In combination with the applied bias, the downward band bending enables the electron transfer from the L- to the X-valley. Accordingly, Fig. 3(a) shows the occurring NDR of an SBFET, where gating happens simultaneously at both metal–semiconductor junctions and the channel. As V_{TG} is increased, the energy level is consequently lowered and electrons are accelerated in dependency of the associated band bending near the source junction. So for higher gate voltages, thinner barriers arise that allow charge carriers to efficiently pass through tunneling. As sketched in the inset of Fig. 3(a), the highest voltage drop occurs at the source junction side, where electrons are expected to gain sufficient kinetic energy. Thereto, a higher V_{TG} is consistent with a higher electron injection, leading to a more pronounced NDR and consequently a higher peak current. With lower V_{TG}, the opposite effect occurs, resulting in a lowered peak current till the NDR effect disappears completely. Interestingly, the peak current follows an exponential relation depending on the gating voltage [see Fig. 3(b)], which is attributed to an enhanced injection given by the exponential voltage dependency of the tunnel current in SBFETs [12]. Moreover, a very constant peak position V_{peak} at approx. 1.9 V is retained [see Fig. 3(c)], which is an important feature for stabilizing the NDR effect in circuits. The outliers at a gating of 5–5.5 V can be explained as this is the region where the NDR effect vanishes out. Also, the valley position V_{valley}, defined here as the inflection point beyond the NDR segment, exhibits a very constant relation. Actually, the valley region is more like a plateau than a concrete voltage point, which is an important feature for circuit applicability of NDR as the valley region is less prone to temperature-dependent voltage variations [13]. This is a main concern in, i.e., Ge nanowire-based NDR-devices [4], where a small valley region is followed by a steep current increase due to impact ionization.

TABLE I
PVR VALUES OF VARIOUS GROUP-IV-BASED NDR DEVICES. THE GeSOI PLATFORM SHOWS THE BEST PVR. * THIS WORK

Device architecture	PVR	Temperature (K)
GeOI (LaYO BOX) [3]	1.2	4.2
Si/SiGe tunnel diode [15]	1.8	295
GeOI (Al-Ge-Al junction)*	2	295
Si Esaki diode [16]	3.8	295
Ge on SOI (Al-Si-Ge junction)*	**6.5**	295

Setting the evaluated NDR effect into perspective with other group-IV NDR devices based on various mechanisms, Table I compares the current peak-to-valley ratio (PVR). There, all Ge-containing device architectures rely on the transferred-electron effect, contrary to the Si and Si/SiGe Esaki and resonant tunneling diodes, respectively. As a further control reference, we included SBFETs based on GeOI platforms with 20-nm device layer processed as described in [14] featuring direct Al–Ge junctions, i.e., excluding the Si interlayer. As evident, the proposed GeSOI platform exhibits a PVR of approx. 6.5 at RT as a mean value of ten representative structures, which is significantly higher and more temperature stable than the evaluated NDR devices fabricated on GeOI platforms.

IV. Cascode Circuit

In the following, a cascode circuit of SBFETs is analyzed, as depicted in Fig. 4(a). This circuit offers the potential to control the occurring NDR effect by either the "upper" SBFET, which means closer to the bias contact, or the

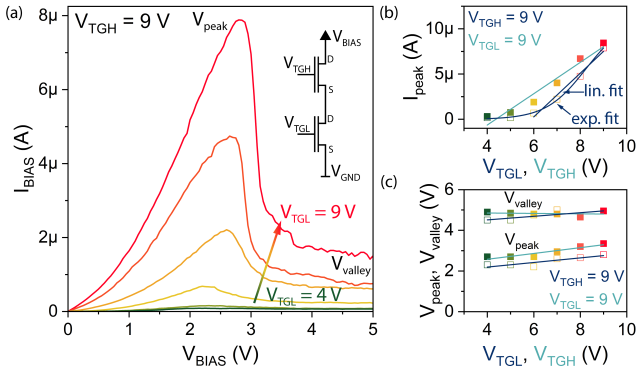

Fig. 4. (a) *I*/*V* characteristic and respective circuit diagram of a two Ge SBFET cascode. (b) Fits of the NDR peak current as a function of the gate voltages. (c) Gate-voltage dependence of the peak and valley positions of the NDR region for varying the gate electrodes of both Ge SBFETs.

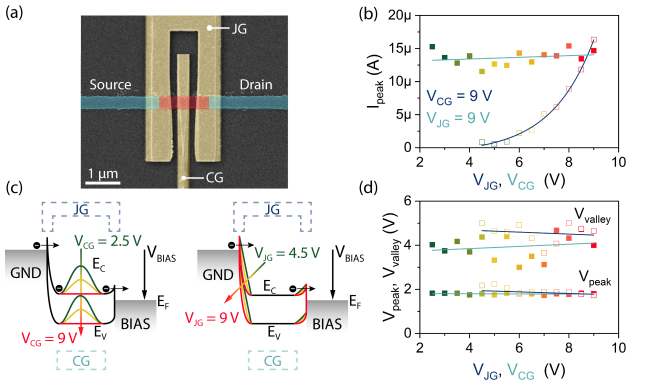

Fig. 5. (a) SEM image of a triple-gated SBFET. (b) Influence of electrostatic gating on the peak current for varying both the JG and the CG with respective fits. (c) Schematic band diagrams illustrating the gating of the CG (left) and JG (right). (d) Peak and valley position shift as a function of V_{JG} and V_{CG}.

"lower" SBFET, closer to the ground potential. For a set V_{TGH} of 9 V and a range of V_{TGL} from 9 to 4 V, referred here as the V_{TGL} sweep, the peak current is slightly lower than for the individual SBFETs and the peak position is right-shifted. Also, for the corresponding V_{TGH} sweep, the determined characteristics are similar. This can be attributed to small differences in NDR behavior for the individual SBFETs, as well as to the changed voltage drop over the single structures, comparable to a voltage divider. The NDR effect is present down to a gating voltage of approx. 4 V for each gate sweep. As evident in Fig. 4(b), the peak current follows a supra-linear relation for the V_{TGL}-sweep and a higher linear relation for the V_{TGH} sweep. Indeed, excluding the two lowest gating voltages for the V_{TGL}-sweep, a near linear relation can be extracted. Additionally, the general NDR behavior is "decreasing" stronger for the V_{TGL}-sweep. This can be attributed to differences in the NDR behavior of single SBFETs but also to the fact that electrons injected by the source (GND) are slowed down more effectively. However, as shown in Fig. 4(c), the peak voltage position V_{peak} can be adjusted with both sweep options in a very linear manner. This tunability feature is highly relevant when correcting the effects of device-to-device variabilities in circuits. Eventually, the peak voltage position reaches that of an individual SBFET. In that case, the swept SBFET is no longer in NDR mode and thus reveals an ohmic resistance, ultimately suppressing the NDR effect, even for the not-swept device. For individual SBFETs, the valley voltage position remains stable within the plateau area.

V. Multigate Transistor Implementation

Next, we investigate the decoupling of the tunnel barrier injection from the channel-related band bending by introducing a triple independently gated SBFET, as presented in Fig. 5(a), which offers two additional degrees of freedom, accordingly. In this arrangement, the junction gate (JG) sets the charge carrier mode by either allowing electrons (positive voltages) or holes (negative voltages) to pass the barrier. The control gate (CG), considering NDR aspects, introduces a further barrier to the acceleration path of the charge carriers, making it possible to tune the peak currents. To investigate the controllability of the NDR effect, either the JG is set constant and the CG is swept (CG-sweep) or the CG is set constant and the JG is swept (JG-sweep) as illustrated with band diagrams in Fig. 5(c). Importantly, the NDR based on the transferred-electron effect is only possible for electrons as this implies the use of the CB landscape, so the JG must be set to both positive and sufficiently high voltages for electrons to gain sufficient kinetic energy necessary to allow electron transfer. Interestingly, the peak current for the JG-sweep is modulated with an exponential relation, whereas the CG-sweep shows a linear relation between gating and peak current, as evident in Fig. 5(b). Both dependencies are expected, as the injection of charge carriers through direct tunneling exhibits an exponential relation as the barrier width is thinned down [12], whereas the CG-related modulation can be interpreted as a further electrostatic barrier (series resistance) to the acceleration path. The peak current decrease is more pronounced for the JG-sweep, resulting in a faster disappearance of the NDR behavior at approx. 4.5 V, contrary to the CG-sweep, where the NDR peak is visible down to approx. 2.5 V and even lower. Taking the peak and valley voltage positions into account, it is evident that both remain very constant in ranges similar to the NDR SBFET described above. Remarkably, the JG-sweep peak voltage positions are very similar to those of the SBFET, especially in their increase at lower voltages, indicating a vanishing NDR effect. The ability to control the peak current at very equal peak voltage positions makes the device very favorable for adaptive applications, where the peak current is sensed at one specific voltage level, also considering read-out circuit optimization.

Nonetheless, it would be desirable to have two independently controllable linear relations over an equal voltage range, while retaining a constant peak voltage position. Therefore, the SBFET cascode and the triple-gated arrangement are combined and extended to the multi-CG transistor, with two independent CGs and two connected JGs over the metal–semiconductor junctions, as shown in Fig. 6(a). The working principle is similar to the triple-gated configuration, where electrons are able to pass the tunnel barriers at the

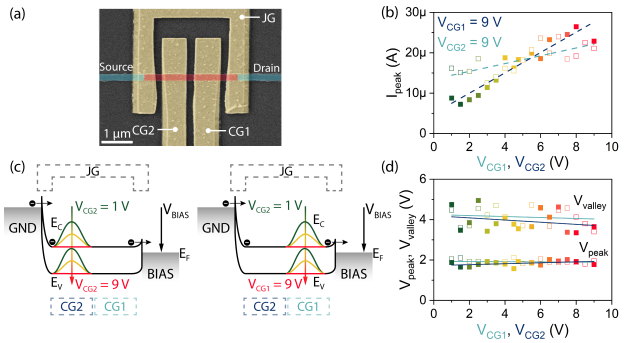

Fig. 6. (a) SEM image of a multi-CG SBFET. (b) Influence of gating on the peak current for varying both CGs with respective fits. (c) Schematic band diagrams illustrating the gating of CG1 (right) and CG2 (left). (d) Peak and valley position shift as a function of the voltage applied to CG1 and CG2.

junctions and two individually controllable electrostatic barriers, CG1 and CG2, accordingly. Note that CG1 is closer to drain (BIAS) and CG2 is closer to source (GND), i.e., to the electron injection side. By increasing the bias and consequently decreasing the associated energy level, electrons are accelerated as the JG is set to positive voltages (allowing electrons passing the barriers) and the CGs are swept. For the CG1-sweep, presented in the right band diagram in Fig. 6(c), CG2 is set to 9 V, while CG1 is swept from 9 to 1 V, contrary to the CG2-sweep, where CG2 is swept from 9 to 1 V and CG1 is set to 9 V, as shown in the left band diagram in Fig. 6(c). Remarkably, as visible in Fig. 6(b), the peak current value decreases by reduced gating in a linear fashion with two different slopes, while keeping the peak and valley voltage position very constant in similar ranges as for the single SBFET and the triple-gated arrangement over the complete gating range, as represented in Fig. 6(d). So, the multi-CG configuration offers two linear degrees of freedom in controlling the peak current while retaining the very same peak voltage position level. This constant voltage position is advantageous considering the ability to optimize systems to certain voltage ranges, such as current read-out systems. Furthermore, the reproducible difference in peak currents in linear dependency of the applied gating situation is an important aspect of establishing MVL devices or multi-mode circuits with enhanced performance and beyond CMOS functionality that allows application-specific optimization by co-integration of common combinational logic and NDR logic [9].

VI. Conclusion

In conclusion, the proposed SBFETs, with their various gate arrangements, offer a reproducible but gating-controllable NDR behavior with high peak currents at constant peak positions and a wide valley region. Aiming for more degrees of freedom in controllability, additional SBFETs (cascode) or gates are introduced. Combining the concepts of the SBFET cascode, with its two controllability features but altering peak voltage positions, and the triple-gated configuration, with its distinction between tunnel barrier control and channel band bending, the multi-CG arrangement provides linear peak controllability at constant voltage positions. These features are inherit properties of fundamental device primitives for adaptive circuits and MVL. Notably, there are still remaining challenges to overcome, such as the ultra-low temperature MBE process, which is not an industry standard for the deposition of Si and Ge, as high-capacity MBE production tools are just starting to emerge. However, we believe that the co-integration of reconfigurable combinational logic and NDR based logic may lead to the integration of circuits exploiting run-time reconfiguration, e.g., hardware secure circuits as well as compact logic and memory gates like compact MOBILE latches with enhanced performance and functionality.

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